

4107

COMPUTER DISPLAY TERMINAL

*Please Check for
CHANGE INFORMATION
at the Rear of This Manual*

First Printing DEC 1983

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COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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MANUAL REVISION STATUS

PRODUCT: 4107 Computer Display Terminal

This manual supports the following versions of this product: Serial Numbers B010100 and up.

REV DATE	DESCRIPTION
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OPERATORS SAFETY SUMMARY

This general safety information is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that can result in damage to the equipment or other property.

WARNING statements identify conditions or practices that can result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL



This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment



DANGER high voltage.



Protective ground (earth) terminal.



ATTENTION — refer to manual.



Refer to manual.

POWER SOURCE

This product is designed to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

OPERATORS SAFETY SUMMARY

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing the power supply shield, soldering, or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

X-RADIATION

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the CRT enclosure.

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

HANDLING

Due to the weight of the Display Module, and its component subassemblies, at least two persons are required to perform installation or service to prevent injury to personnel or damage to the Display Module.

IMPLOSION PROTECTION

Whenever the implosion shield is removed from the CRT, protection against implosion hazard is reduced. Service personnel should wear full face masks and protective clothing at any time the CRT is removed from the CRT module or the implosion shield is not in place.



Figure 1-1. 4107 Computer Display Terminal.

Section 1

INTRODUCTION

USING THIS MANUAL

This manual contains service information for the 4107 Computer Display Terminal. This manual describes all parts of the terminal except for the Display Module.

Because the Display Module is a separate OEM product within the 4107, all significant information is contained in the *Display Module for the 4107, Service Manual*. A short-form adjustment procedure is included in this manual (for convenience), but the detailed adjustments, theory, and repair procedure are in the Display Module manual. Display Module disassembly and reassembly procedures are contained in Section 6.

The terminal is compatible with the 4105, and with Tektronix 4110 series terminals (4113, 4115, etc.). Applications designed for use with the 4105 can also be used with the 4107. See NOTE. Applications designed for use with the 4107 can also be used with the 4113B and 4115B terminals.

All peripherals to this terminal are covered in their separate service manuals. These include hard copy units, printers, and programmability unit.

NOTE

The 4107 contains 256k bytes more processor memory than the 4105. See the discussion of the RAM3 Board in Section 4, Theory of Operation.

RELATED DOCUMENTS

The following documents contain detailed information on the use of the 4107 terminal:

- *4107/4109 Operator's Manual*
- *4107/4109 Command Reference Manual*
- *Display Module for the 4107, Service Manual*

INSTALLATION INFORMATION

Section 8 provides complete instructions for installing the 4107 terminal. Immediately after receiving the 4107, unpack and inspect it for possible shipping damage. Do not throw away the shipping container until the terminal passes the damage inspection and is fully operational. Run the Self Test program to be sure the terminal works (see Section 5, Checks and Adjustments). Also verify that all accessories checked on the Accessories Packing Slip are included and work properly.

PRODUCT DESCRIPTION

The 4107 is a low-cost color graphics terminal. The primary applications are:

- multiple-user CAD/CAM systems
- text/graphics entry/editing
- general-purpose business terminal.

The 4107 presents graphics and text data on a high-resolution color raster-type CRT. There are 480 lines of 640 pixels (per line) on the 13V screen (a 13V size color tube is about the same size as a black and white 15 inch diagonal measure tube). The display refreshes at the rate of 60 Hz. Both, graphics and text data, are displayable in color (selected from 64 possible hues). A total of 25 colors are displayable at one time:

- 16 colors are displayable in the graphics part of the display.
- 8 colors may be used to display text/dialog data (for character foreground and background).
- 1 color shows the crosshair graphics cursor (when present).

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The character background may be a specified color or it may be transparent, thus revealing the graphics behind it. The dialog data (to/from the host) is presented in a scrollable area extending up from the bottom of the screen.

The keyboard is detached and contains the usual keyset, a numeric keypad, 12 special-purpose function keys, and a graphics joydisk. The joydisk controls the position of the graphics cross-hair cursor. Figure 1-2 shows the major modules in the 4107.

An RS-232 connector, on the rear panel connects to the host. The Two Port Peripheral Interface (2PPI) provides two RS-232 connectors on the rear panel for peripheral devices such as plotters and a graphics tablet unit. There is also a separate copier connector for the Tektronix 4695 color copier.

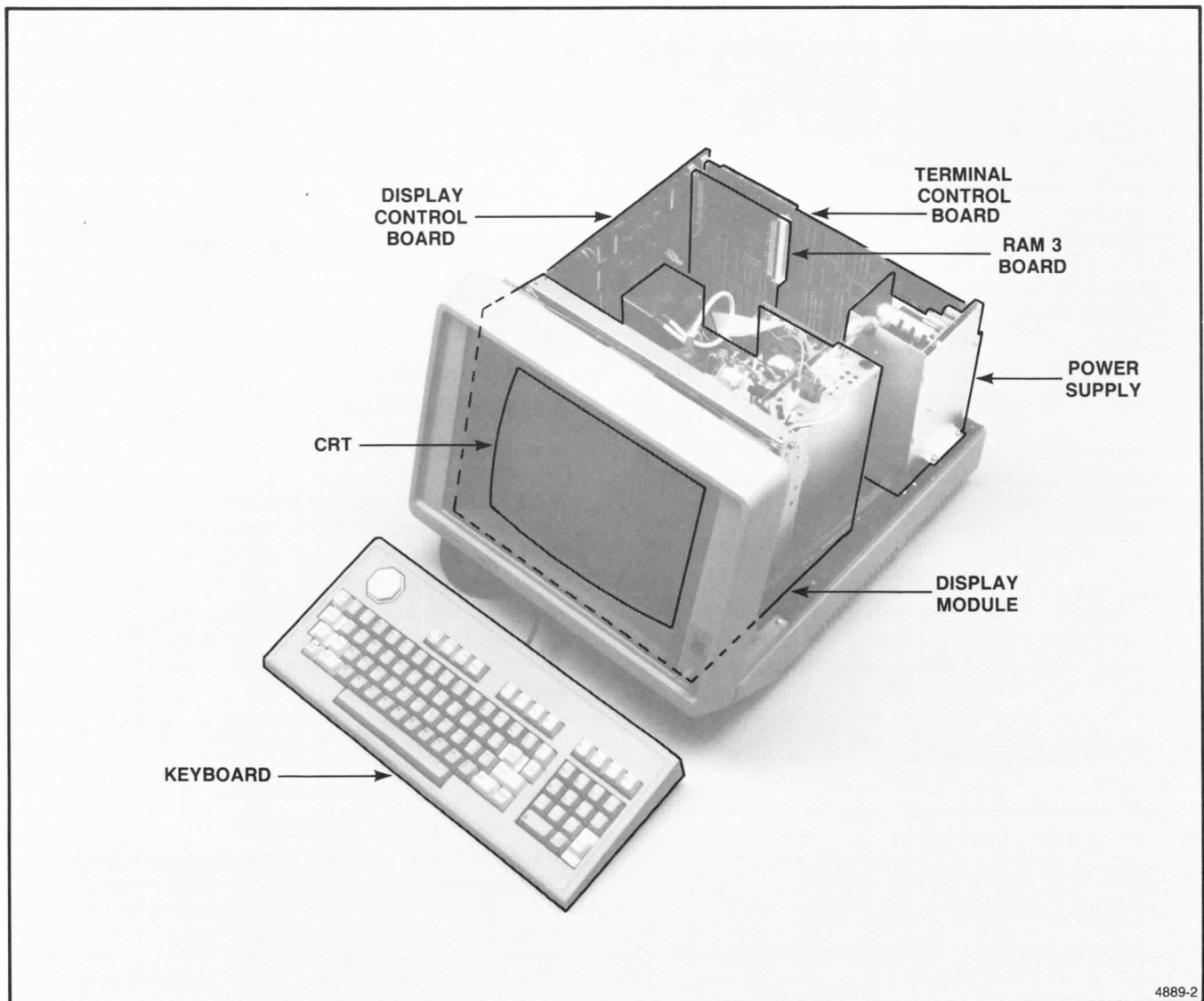


Figure 1-2. 4107 Functional Modules.

CONTROLS, INDICATORS AND CONNECTORS

The 4107 has the following features on the front of the terminal main cabinet (see Figure 1-3):

- **POWER switch.** This is a push-button switch that shows green when the power switch is pushed in.
- **BRIGHTNESS control.** This potentiometer allows the user to adjust the brightness level of the display screen.
- **Display screen.**

The keyboard has the following features (also shown in Figure 1-3):

- **Alphanumeric keyset.** Contains the standard typewriter/terminal keyset.
- **Numeric keypad.** This keyset is intended for numeric data entry in certain applications where calculations are performed.
- **Predefined function keys** (dialog, setup, save copy, set color).
- **Function keys** (F1 through F8).
- **Joydisk.** Moves screen position of graphics cross-hair cursor.
- **CAPS LOCK indicator light.** Indicates the caps key is in the upper-case condition.

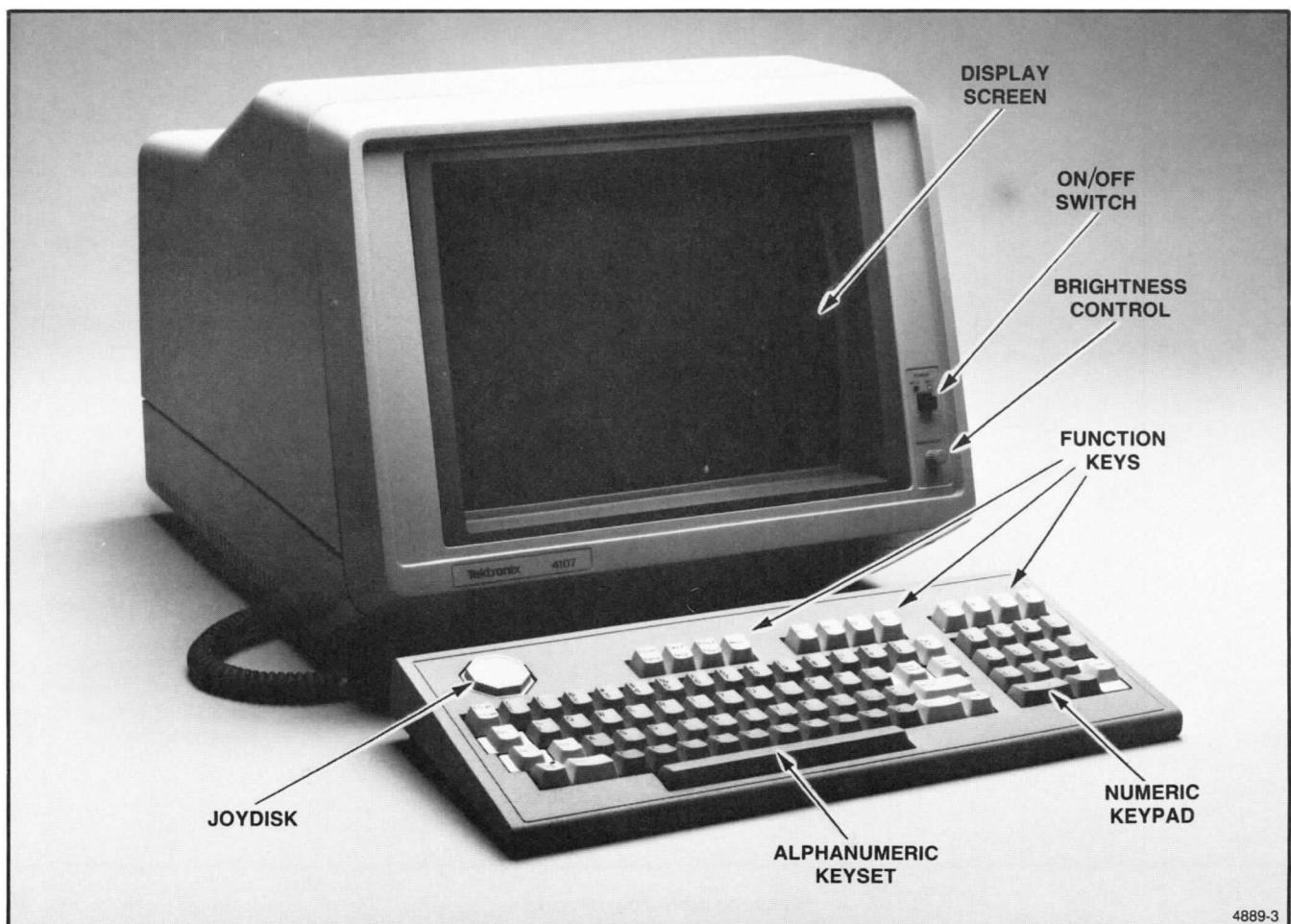


Figure 1-3. Front Panel Features.

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Rear panel features are (see Figure 1-4):

- AC power connector.
- Line voltage selector switches. Selects either 115V or 230V mains. Both switches must read same voltage.
- COPIER connector. Accepts connecting cord from Tektronix copier or printer.
- COMPUTER connector. Accepts an RS-232 cable to the host system.
- 2PPI connectors. Accepts RS-232 cables to two peripheral devices.
- KYBD connector. Accepts the 5-pin DIN connector on the keyboard cord.
- SELF TEST switch. This push-button activates the Self Test diagnostic program inside the 4107.
- RESET switch. This push-button resets the operating parameters to their default settings.

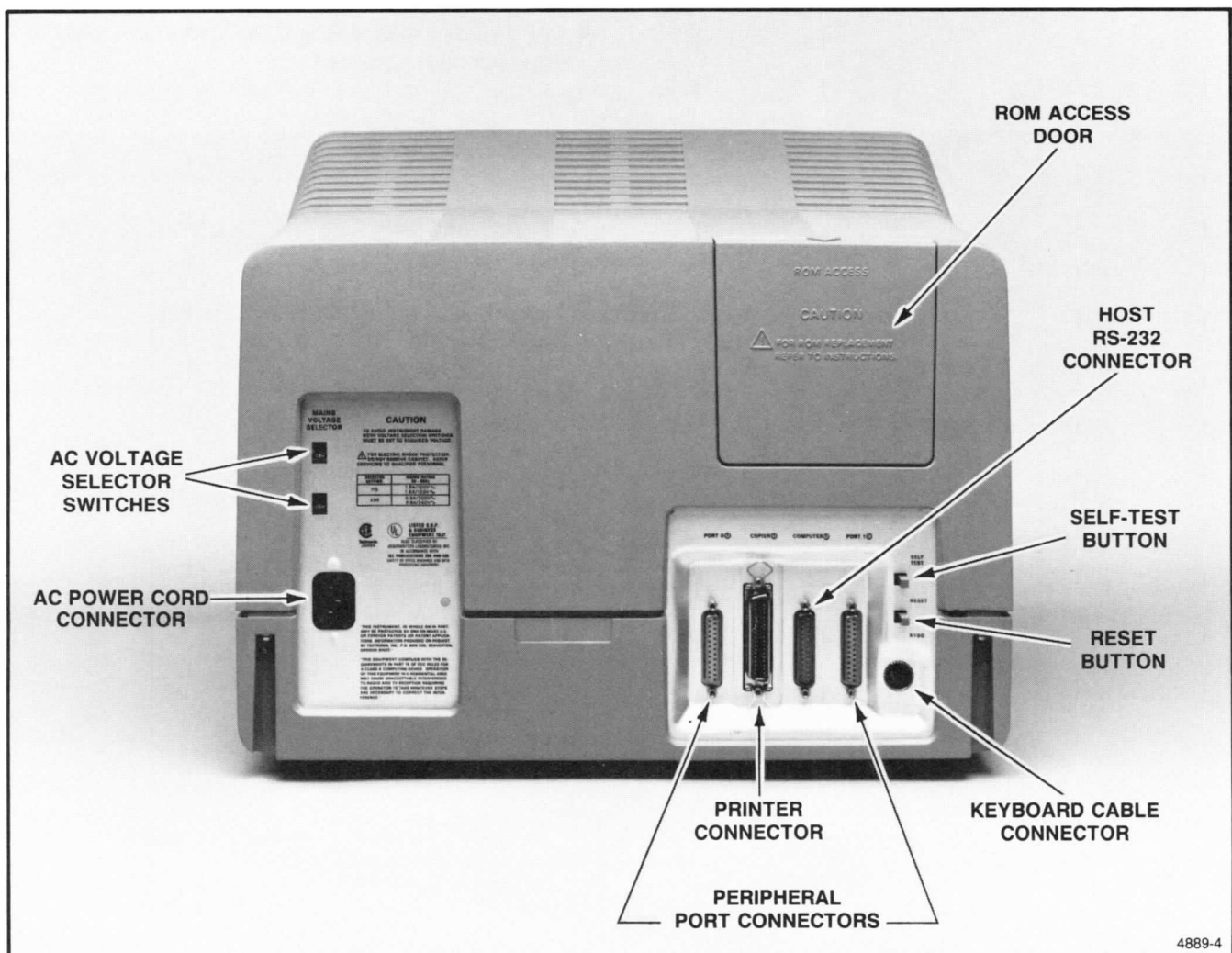


Figure 1-4. Rear Panel Features.

The 4107 also contains a bell indicator that functions with Self Test and also acts as a prompt from the host.

Section 3, Operating Information, provides more detailed information about the controls and indicators.

OPTIONS

Table 1-1 lists the 4107 options in numerical order. Option numbers beginning with an alpha designation are grouped at the end of the table.

Table 1-1
4107 OPTIONS

Option #	Description
Option 4A	United Kingdom keyboard option
Option 4B	French keyboard option
Option 4C	Swedish keyboard
Option 4F	Danish/Norwegian keyboard
Option 4G	German keyboard
Option 4K	Katakana Keyboard
Power Cord Options:	
Option A1	European Power Cable (220V)
Option A2	U.K. Power Cable (240V)
Option A3	Australian Power Cable (240V)
Option A4	North America Power Cable (240V)
Option A5	Swiss Power Cable (240V)

ACCESSORIES

These accessories are listed in the mechanical parts list (Section 14) where part numbers are given for each item. Standard accessories are supplied with each 4107, and optional accessories may be ordered separately, and in addition to, standard accessories.

Standard Accessories

- *4107/4109 Reference Guide*
- *4107/4109 Programmers Reference Manual*
- *4107/4109 Operator's Manual*
- Keyboard (detached item with connecting cable)
- Keyboard overlays
- Power cord set
- RS-232 Host Port cable

Optional Accessories

- *4107 Service Manual*
- *Display Module for the 4107 Service Manual*
- RS-232 loop-back connector
- Copier Port loop-back connector
- Alignment graticule

Section 2

SPECIFICATION

This characteristic/specifications section lists two different types of specifications: those that are classified as environmental, physical, or “static” specifications (specifications that cannot be verified by the user); and those that are actual operational parameters (specifications that are user verifiable). Use the checks and adjustment procedures in Section 5 to verify the user-verifiable specifications. (User-verifiable specifications are listed only in Tables 2-4 and 2-5.)

The following terms are used in these specification tables:

Characteristic: A property of the product.

Supplemental Information: Statements that describe typical performance for characteristics of secondary importance that are not usually verified by the manual’s Performance Check Procedure, or statements that further explain related performance requirements.

CHARACTERISTICS/SPECIFICATIONS

The remainder of this section summarizes characteristics and performance specifications of the 4107. In order for these specifications to be achieved and to ensure proper performance, the following conditions must be met:

1. The 4107 must be adjusted at an ambient temperature of 68 to 86 degrees F (20 to 30 degrees C).

2. The 4107 must be operating in an environment as specified in Section 8, *Installation*.
3. A warm-up time of at least 20 minutes must precede operation.
4. The 4107’s power source must meet specified power requirements. See Section 5, Checks and Adjustments, and refer to Table 2-5 (Power Supply Specifications). The 4107 is designed to be operated from a power source with its neutral line at or near ground potential. It is not intended for operation from two phases of a multiphase system.

The following tables contain specifications and characteristics for the 4105.

Table	Description
2-1	Physical Dimensions
2-2	Electrical Specifications
2-3	Environmental Specifications
2-4	Display Module Electrical Specifications
2-5	Power Supply Module Electrical Specifications
2-6	Installation Requirements
2-7	Graphics Characteristics
2-8	Alphanumeric Characters
2-9	Communication Performance
2-10	Processor Memory Map

SPECIFIC TIONS

**Table 2-1
PHYSICAL DIMENSIONS^a**

Characteristic	Performance Requirement
Weight	45 lbs (21 kg)
Length	19.5 in (495 mm)
Width	16.5 in (419 mm)
Height	13.89 in (352 mm)
Display Area	'13V': 9.4 x 7.1 in (240 x 180 mm)

^a These specifications do not include the Keyboard or Adjustable Base.

**Table 2-2
ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirement
Nominal Input Voltages: 115V 230V	87—128V, 174—250V
Max. Input Power	200 W
Frequency Range	48—66 Hz
Fuse	4 A Slow-blow

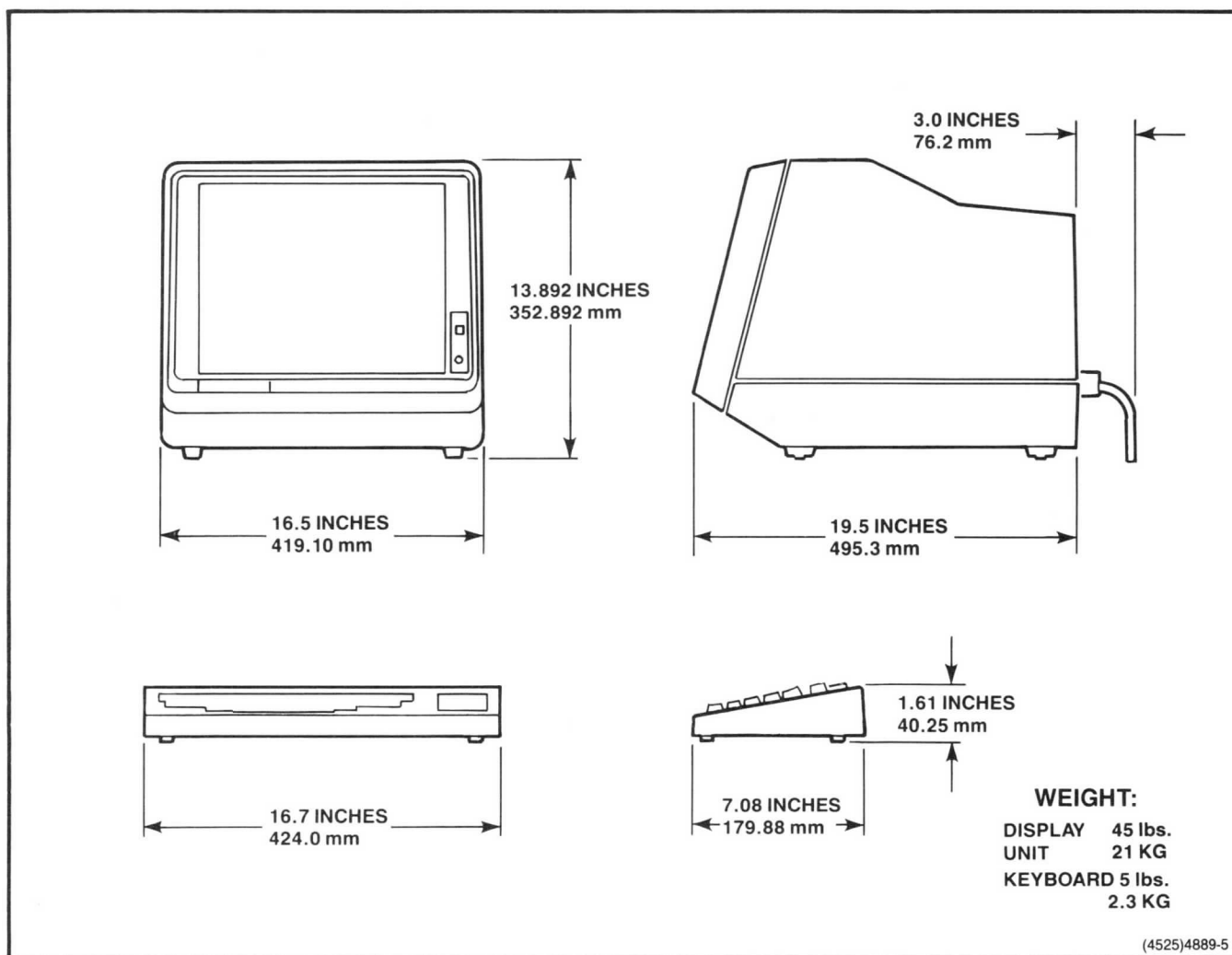


Figure 2-1. 4107 Physical Dimensions.

Table 2-3
ENVIRONMENTAL SPECIFICATIONS

Characteristic	Performance Requirement
Temperature	
Operating	+ 50 to + 104° F (+ 10 to + 40° C)
Nonoperating	-40 to + 149° F (-40 to + 65° C)
Altitude	
Operating	To 10,000 ft (3,050 m)
Nonoperating	To 40,000 ft (12,200 m)
Humidity	
Operating	10 to 75% rel. hum. (non-cond.)
Nonoperating	10 to 95% rel. hum. (non-cond.) Allow a four-hour drying out period, after worst-case storage conditions.
Vibration	Withstands 0 to .015 in displacement, at 10 to 55 to 10 Hz (all 3 major axes)
Shock	Main cabinet withstands a 20-g shock to all faces.
Electrostatic Immunity	
Operating	No interruption of operation, loss of data, or change of operating mode from 15 kV discharge.
Nonoperating	No damage to terminal from 20 kV discharge.

Table 2-4
DISPLAY MODULE ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirement
Power consumption	80 Watts (nominal)
Vertical frequency	60 Hz (nominal) 59.97 Hz (+/- .05%)
Active displayed lines per vertical scan	480 lines
Horizontal pixel count per line	640 pixels
Horizontal frequency	31.5 kHz (+/- .05% of nominal rate)
Horizontal blanking time	6.349 μs
Vertical blanking time	1.429 ms
Linearity	better than +/-7%
Sync Pulse Timing	
(Horizontal):	
H front porch	0.952 μs
H sync pulse	2.897 μs
H back porch	2.540 μs
(Vertical):	
V front porch	222 μs
V sync pulse	190 μs
V back porch	1020 μs
Phosphor	P22 short-persistence
Luminance	25 ft-lamberts (for "white")

NOTE

A slight moire effect may be visible on the screen under some lighting conditions. This effect is allowed; not out of spec.

SPECIFICATIONS

**Table 2-5
POWER SUPPLY MODULE
ELECTRICAL SPECIFICATIONS**

Characteristic	Performance Requirement
+ 5.1 V secondary:	
• Accuracy–	+ /-3% nom. V @ 8.8A load,
• Regulation–	within 6% of nom. voltage,
• Rated full load current–	9 A,
• Minimum load current–	1 A
+ 12 V secondary:	
• Accuracy–	+ /-0.5 V @ 350 mA load,
• Regulation–	+ /-20% of nom. voltage,
• Rated full load current–	650 mA,
• Minimum load current–	0 A
-12 V secondary:	
• Accuracy–	+ /-0.5 V @ 100 mA load,
• Regulation–	+ /-20% of nom. voltage,
• Full load current–	650 mA,
• Minimum load current–	0 A
+ 21 V secondary:	
• Accuracy–	+ /-0.5 V @ 20 mA load,
• Regulation–	20 to 22 V,
• Full load current–	20 mA,
• Minimum load current–	0 A

**Table 2-6
INSTALLATION REQUIREMENTS**

Characteristic	Supplemental Information
Heat dissipation:	
Typical	450 BTU/hr
Max load	570 BTU/hr
Surge Current	34 A (typical) @ turn on
Cooling clearance	3 inches rear 2 inches top and sides
Distance from EMI sources	Terminal's display should be as far removed from motors, fans, or other electromagnetic devices as possible.

**Table 2-7
GRAPHICS CHARACTERISTICS**

Characteristic	Supplemental Information
Resolution	640 horizontal by 480 vertical resolvable pixels.
Addressability	4096 x 4096 points.
Graphics Command Syntax	Compatible with 4100- and 4010-style escape syntaxes.
Line Types	Solid, Dashed, Erase.
Graphics Primitives	Vectors, panels (polygons), and text
Number of Colors available	In graphics region, 16 colors, selected from 64 possible color mixtures. In the dialog area, another 8 colors selected from the same 64 possibilities.
Interactive Graphics	Joydisk (on the keyboard) controls a cross-hair graphic cursor.

Table 2-8

ALPHANUMERIC CHARACTER SETS

Character Set	Supplemental Information
Standard Character Set	<p>Full ASCII character set.</p> <p>95 displayable characters (counting "space" as a displayable character)</p> <p>In "Snoopy mode" all 128 characters are displayable.</p> <p>The graphic representations of control characters conform to ANSI x3.32.</p>
Supplementary Character Set	<p>This set is 94 special characters (rulings, math symbols, etc.) accessible via the SO (Shift Out) control.</p>
Optional Character Sets	<p>United Kingdom (Option 4A)</p> <p>French (Option 4B)</p> <p>Swedish (Option 4C)</p> <p>Danish/Norwegian (Option 4F)</p> <p>German (Option 4G)</p> <p>Katakana (Option 4K)</p>
Character Format	<p>80-columns x 32-line screen display</p> <p>7 x 9 dot matrix in a 8 x 15 character cell (with descenders)</p>

See Appendix E for details.

Table 2-9

COMMUNICATION PERFORMANCE

Characteristic	Supplemental Information
Alphanumeric (only) communications rate	38.4 kBaud (without H/W flagging)
Simple (line) graphics communications rate	19.2 kBaud (without H/W flagging)
Two Port Peripheral Interface (2PPI).	<p>2 RS-232 ports, communicates with RS-232 peripheral devices such as plotters or graphics input tablets</p> <p>19.2 kBaud maximum (without H/W flagging)</p>
Hard Copy Interface	<p>Hard copy device such as the Tektronix 4695.</p> <p>Centronics-style parallel interface.</p>

Section 3

OPERATING INFORMATION

This section provides a familiarization procedure intended to help the service person exercise the 4107 and get acquainted with its overall operating characteristics. You should have a general ideal of how the terminal behaves, from the operator's point of view, before attempting any extensive troubleshooting.

You should use this section when performing on-site troubleshooting. First, run Extended Self Test (Appendix C). Then, if problems persist, this may indicate improper use of the 4107. By working through this familiarization procedure, you may determine whether or not the 4107 functions as expected.

NOTE

The terminal must be installed before you can complete the exercises in this session. If it has not been installed, see Section 8 before you continue. The terminal should NOT be on-line to a computer during the session.

This section contains six short exercises designed to help you learn about the terminal before you log on to a host computer.

- Exercise 1 introduces Setup mode and some of the Setup commands.
- Exercise 2 shows how to create graphics from the keyboard. It introduces some of the graphics concepts used by the terminal.
- A short discussion of the Menu key and the use of programmed keys for viewing functions and for the color interface precedes the following exercises.
- Exercise 3 shows how to modify color definitions from the keyboard with the terminal's interactive *color interface*.
- Exercise 4 introduces views, the viewing keys, and the *zoom* and *pan* functions.
- Exercise 5 introduces GIN (Graphics Input).
- Exercise 6 shows how to program keys.

Please allow about one hour to complete this session. Exercises 1 through 4 should be done in sequence, and at one sitting if possible, since each exercise assumes that the terminal is just as the previous exercise left it. If you do any exercise independently of the others, first give the **FACTORY** command (see Exercise 1); this will set up the terminal so the exercise will work as described here.

You will find information about some of the commands in these exercises in the *Setup Commands* section of the *4107/4109 Operators Manual*. Details on all terminal commands are found in the *4107/4109 Programmers Reference Manual*.

NOTE

Several steps in the following exercises tell what your alternatives are BEFORE telling what action to take. Be sure to read each step all the way through before you take any action.

EXERCISE 1: SETUP MODE

Setup mode allows you to give English-style *Setup commands* from the keyboard to set a variety of terminal parameters. This exercise acquaints you with Setup mode and how to enter Setup commands.

To enter a Setup command, type the command name followed by a space, then enter any parameters (separated by spaces), then press the Return key. All command names have been spelled out in the examples, but you can abbreviate a command name to as few characters as necessary to distinguish it from other commands (usually two or three characters).

If you make a mistake typing a command, use the Rub Out key to erase characters, one by one, back to the error, then complete the command in correct form. Or you can enter Ctrl-X (hold down the Ctrl key and press X) to erase the entire line, then reenter the correct command. If you have already pressed Return, you will probably get an error message. Just reenter the command in the correct form.

1. Press the POWER switch on the front of the display unit to turn the terminal on. In a few seconds a blinking cursor (an underline) appears on the screen. If you don't see the cursor, adjust the BRIGHTNESS knob just below the POWER switch.

When the terminal is first turned on, the entire screen is defined as the *dialog area*. This area is used to display your conversations with the terminal (and later, with the computer).

Press the Setup key (located at the top of the keyboard) to put the terminal in Setup mode. An asterisk appears at the left margin, next to the cursor. This is the Setup mode prompt; it tells you that the terminal is waiting for your input.

To make sure that the exercises will work as described, type in the following command after the Setup prompt, then press the Return key:

FACTORY

This resets all terminal operating parameters to their factory settings, erases the screen, and removes the terminal from Setup mode. Now press the SETUP key again to return the terminal to Setup mode.

You can return these parameters to their powerup values for the convenience of the next user or to run an applications program by doing any of the following:

- Turn the terminal off, then back on again.
- Press the RESET button on the rear of the terminal.
- Enter the RESET command in Setup mode. (This command, like FACTORY, removes the terminal from Setup mode.)

All commands and messages in this session are shown in upper case; to make your entries match the displays, press the Caps Lock key (at the lower left corner of the keyboard). All alphabetic characters will be displayed as capitals; numerals and other characters are not affected.

2. One of the things you can do in Setup mode is change the colors used in the dialog area. Each color is identified by a number called a *color index* (more on this in Exercise 3). The DAINDEX (Dialog Area Index) command selects the dialog area colors. Enter the following command. (Be sure to enter a space before each number. Also remember to press Return to end the command.)

DAINDEX 1 2 4

This command changes the dialog area colors to white letters (color 1) in red character cells (color 2) on a blue background (color 4). Note that the part of the dialog area below the * changes to blue. All new information in the dialog area will be in the new colors. At this point you may want to adjust the BRIGHTNESS knob, just below the POWER switch, for best viewing.

3. The STATUS command is another useful command. If you forget a terminal setting, or if the terminal behaves unexpectedly, the STATUS command can often help. This command has several forms. The form **STATUS command-name** gives you the status of parameters set with the given command. For example, enter:

STATUS EDITCHARS

The following message is displayed, showing the terminal's three *editing characters*:

EDITCHARS. **C_N** **~**

The symbol indicates that ASCII Delete is the *character-delete* character. Pressing Rub Out generates an ASCII Delete character, which deletes the character just to the left of the cursor. To illustrate, type a few characters, *but don't press Return*. Instead press Rub Out several times to erase the characters and back-space the cursor to the * prompt.

The **C_N** symbol indicates that ASCII Cancel is the *line-delete* character. Enter several characters, *but don't press Return*. Instead, enter Ctrl-X to generate an ASCII Cancel character, which erases the line you just typed.

The **~** character is the *literal character*. The use of this character is explained in Exercise 6.

- Now enter the following command:

STATUS

This lists all the Setup commands that set terminal parameters, and the current parameter settings.

- Press the bottom of the *joydisk* (at the upper left of the keyboard) to scroll the list down. Notice that you can't scroll clear to the beginning of the message. The message is too long to fit in the dialog area's memory, so part of the message has been lost.

Now press the top of the *joydisk* to scroll the list back up.

- One way to avoid losing output in this way is to use *Ctrl-S* and *Ctrl-Q*. Enter the command **STATUS** again, but quickly enter *Ctrl-S* to halt output of the Status message. Then enter *Ctrl-Q* to start printing the message again. With a bit of practice at finding these keys, you can stop and start output whenever you want.

You can also increase the number of lines in the *dialog buffer* — the part of terminal memory used to store information displayed in the dialog area. For example, enter the commands:

**DABUFFER 200
STATUS**

Now you can scroll clear to the beginning of the Status message.

- Notice that the complete Status message is divided into functional categories. One category is titled **DIALOG**, since it lists information about the dialog area. Enter the command:

STATUS DIALOG

This displays just the entries under the **DIALOG** heading (Figure 3-1). Note the line:

DAINDEX. 1 2 4

Here you see the dialog area color indices that you set in Step 2.

- Finally enter:

STATUS ED

This displays all commands that begin with the character string ED (there are two of them). You can enter this form of the STATUS command with any character string to display the status of commands that begin with the given string.

- Press either S Eras or D Eras (the shifted version of S Eras) at the upper left of the typewriter portion of the keyboard. Since the dialog area takes up the entire screen, either key erases the dialog area.

You have now learned how to enter Setup mode, how to modify terminal parameters, and how to find the status of these parameters. *Without making any changes to what you have done*, proceed to Exercise 2.

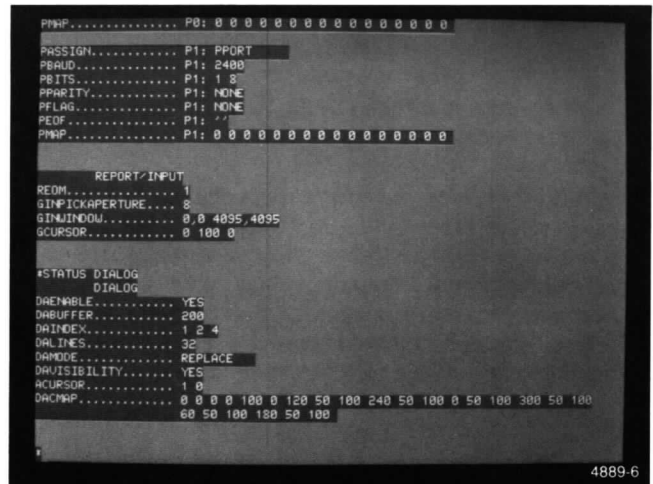


Figure 3-1. Dialog Area Display.

EXERCISE 2: ENTERING LOCAL GRAPHICS

Normally graphic displays are created by a host software package. In this exercise, however, you will create a graphic display from the keyboard. This exercise illustrates a few of the graphics capabilities of the terminal, and also prepares a display for Exercises 3 and 4.

To do this procedure, the terminal should be as you left it at the end of Exercise 1 (the terminal must still be in Setup mode).

1. Enter the following commands:

```
DAINDEX 0 3 3
DALINES 5
```

The first command changes the dialog area colors to black text on a green background (both character cell and dialog background colors are set to color 3). The **DALINES 5** command sets the dialog area to the bottom five lines of the screen. The remainder of the display can now be used as the *graphics area*.

Two graphics concepts used by the terminal are those of *panel* and *segment*.

A *panel* is simply a closed polygon with one or more boundaries; examples are triangles, rectangles, outlines of buildings, etc. In terminal graphics a panel is normally used to represent one object: a house, a window on a house, a circuit board element, or a bar on a graph are just a few examples. Simple commands allow you to create a panel and fill the interior of the panel with a color or a pre-defined *fill pattern*. (You will do this in this exercise.)

A *segment* is a collection of one or more graphics objects, treated as a single unit. Often a segment is used as a kind of a subpicture. For example, on a circuit board, a block of circuit description might be defined as a segment. A segment, even though it consists of several distinct graphic objects, can be manipulated as a unit. A single command can be used to move, copy, rotate, or scale the segment, or to set segment *attributes* as keys for other types of graphic operations.

Segments, panels, and other graphics concepts are discussed in detail in the *4107/4109 Programmers Reference Manual*.

2. Enter the following sequence of commands exactly as shown. (If you should make an error entering the commands, enter **SGCLOSE**, then **SGDELETE 1**. This will delete the segment; then you can reenter the correct commands.)

```
SGOPEN 1
FILLPATTERN -4
BEGINPANEL 500 1000 1
DRAW 2000 1000
DRAW 2000 2500
DRAW 500 2500
ENDPANEL
SGCLOSE
```

The **SGOPEN** command opens a definition for segment number 1. All graphics commands until an **SGCLOSE** command (to close the segment definition) will define parts of segment 1.

The **FILLPATTERN** command sets a *fill color* or *fill pattern* to fill the interior of each panel you define. This particular command sets the fill pattern to -4, which specifies color index 4 (deep blue).

BEGINPANEL begins a *panel definition*. The first vertex of the panel is at the point with xy-coordinates (500,1000). The final parameter of 1 specifies that the border of the finished panel will be displayed, rather than covered by the fill pattern.

The **DRAW 2000 1000** command draws a vector (line segment) from the previous vertex (500,1000) to the point (2000,1000). You will see this vector drawn as soon as you enter the command. Each **DRAW** command draws a vector from the previous point to the point with the specified xy-coordinates.

ENDPANEL draws the last side of the panel, fills the panel with blue, and outlines it; **SGCLOSE** closes the segment definition. The display now looks like Figure 3-2.

- Now open a segment definition for segment 2 and draw a red star inside the box with the following sequence of commands:

```

SGOPEN 2
FILLPATTERN -2
BEGINPANEL 850 1250
DRAW 1250 2300
DRAW 1650 1250
DRAW 650 1900
DRAW 1850 1900
ENDPANEL
    
```

The display now looks like Figure 3-3. The middle of the star is open due to the way in which the boundary of the star intersects itself.

- Now enter the following sequence of commands:

```

FILLPATTERN 6
BEGINPANEL 2500 1000 1
DRAW 3500 1000
DRAW 3500 2500
DRAW 2500 2500
ENDPANEL
SGCLOSE
    
```

A rectangle is drawn beside the blue square and filled with pattern 6 (Figure 3-4). (There are several dozen fill patterns available. You will have a chance to explore these in Exercise 6.) The final command closes the definition of segment 2. Note that this segment contains both the star drawn in Step 3 and the rectangle filled with the brick pattern drawn in this step.

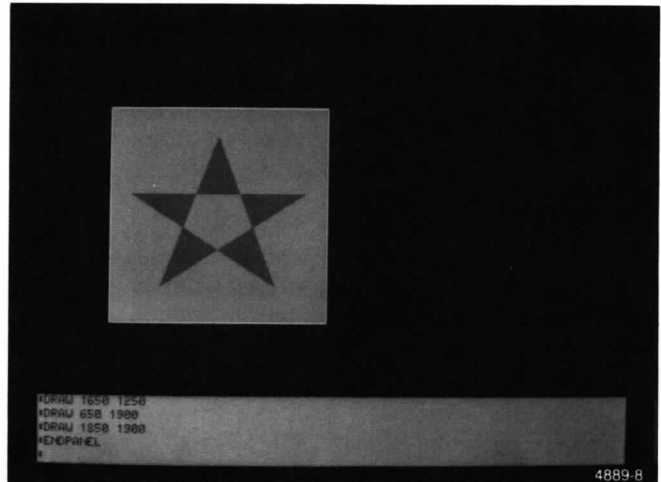


Figure 3-3. Box With Star.

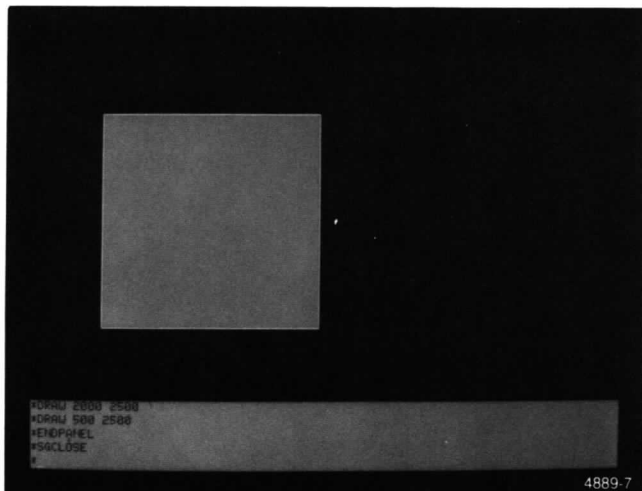


Figure 3-2. Display of One Segment.

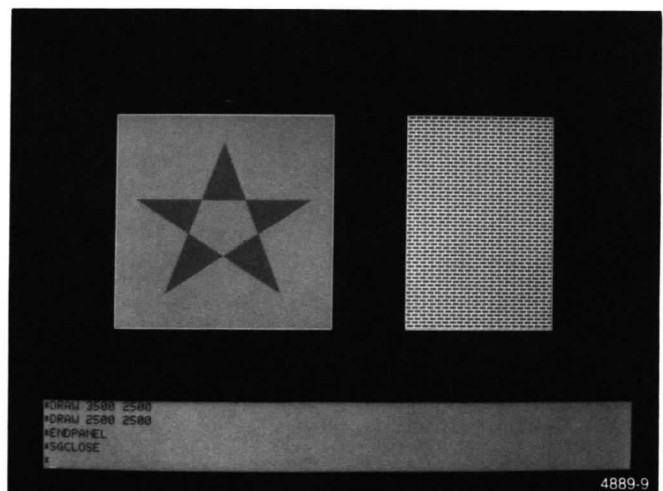


Figure 3-4. Completed Graphic Display.

OPERATING INFORMATION

5. Now let's explore some of the properties of segments. First, enter the following commands:

```
FILLPATTERN 15
BEGINPANEL 400 2600 1
DRAW 3600 2600
DRAW 2000 3000
ENDPANEL
```

Since no segment definition is open, this triangle is not part of a segment definition. Now press G Erase (Shift-Dialog) and note carefully what happens. The entire screen is momentarily erased, *but segments 1 and 2 are redrawn*. Information that is not part of a segment (the triangle, in this case) is lost, while segments are retained.

6. Segments can also be manipulated in various ways. For example, you can make a segment invisible. Enter the command:

```
SGVISIBILITY 2 NO
```

The star and brick wall that comprise segment 2 disappear; they are still defined in terminal memory, but are now invisible (Figure 3-5). Now give the command:

```
SGVISIBILITY 2 YES
```

and segment 2 reappears.

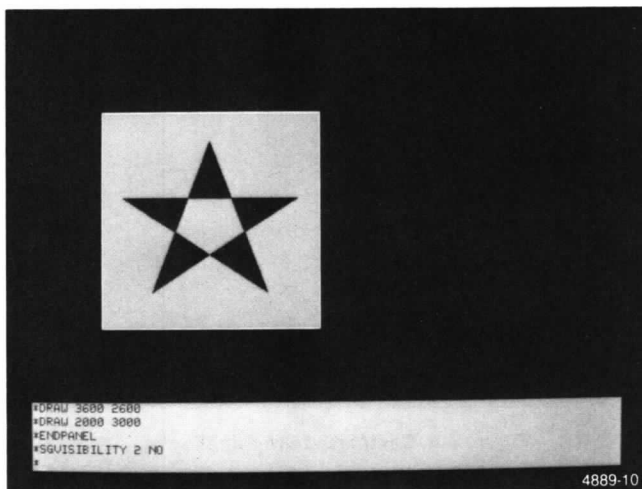


Figure 3-5. Display With Segment 2 Invisible.

7. Segments can also be made to blink on and off as a means of visual enhancement. To illustrate this, enter the command:

```
SGHIGHLIGHT 2 YES
```

Segment 2 begins to blink on and off. Now give the command:

```
SGHIGHLIGHT 2 NO
```

The blinking stops, and the display in Figure 3-4 is left on the display.

8. There are several types of segment transformations. To illustrate, enter the following command:

```
SGTRANSFORM 1 1 -2 1 -2 0 0 2500 1500
```

The blue square is erased and redrawn in a different size and at a different location. Note that the red star is also erased. Just press G Erase; all segments are redrawn, including the red star which is part of segment 2. (Figure 3-6).

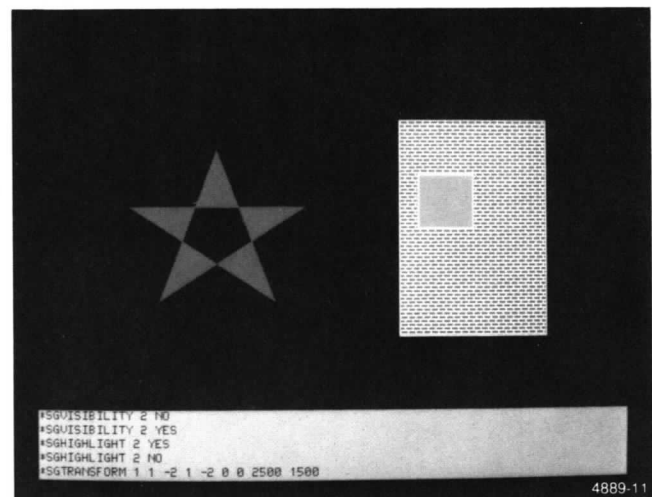


Figure 3-6. Display With Transformed Segment.

- The SGTRANSFORM command can also change the x- and y-scales independently to alter the aspect ratio, and can rotate segments. For example, enter the following:

```
SGTRANSFORM 1 1 -1 1 -4 75 0 1000 1800
```

Now press G Eras to redraw the display. Segment 1 is now only one eighth as high as it is wide, and it has been rotated 75 degrees from the horizontal (Figure 3-7).

Now return segment 1 to its original size and position with the command:

```
SGTRANSFORM 1 1 0 1 0 0 0 0 0
```

Note that the blue square now covers the red star. To change the display priority so the star is visible, give the commands:

```
SGVISIBILITY 2 NO
SGVISIBILITY 2 YES
```

A complete explanation of the SGTRANSFORM command is included in the Programmers manual. The examples here are given without explanation of the parameters, and are just to illustrate some of the graphics capabilities of the terminal.

There are many other segment operations that the terminal can perform. These include copying one segment into another segment definition, and grouping segments together into *matching classes* so that all the segments in a class can be treated by a single command. The complete

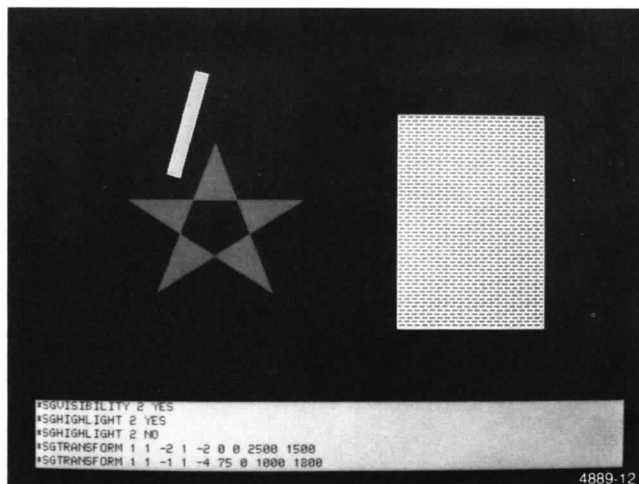


Figure 3-7. Display With Segment Scaled and Rotated.

set of segment operations and the complete graphics capabilities of the terminal are discussed in the Programmers manual.

Now let's look at the relationship between the graphics area and the dialog area.

- Occasionally you may want to examine more than five lines of dialog area at a time. You can increase the size of the dialog area so that it covers all or part of the graphics area, without destroying any graphics.

To illustrate, increase the size of the dialog area to 22 lines by entering:

```
DALINES 22
```

Notice that the dialog area now covers most of the graphics area.

- Press the Dialog key. The dialog area disappears and the complete graphics display is visible. Press the Dialog key again and the dialog area reappears.
- Now give the following commands:

```
DAINDEX 3 0 0
STATUS C
```

The display now looks like Figure 3-8. The command **DAINDEX 3 0 0** sets the dialog text color to color 3 (green) and the character cell and background colors to *transparent*. As the Status message scrolls up, notice that the graphics display shows through the dialog area background as though the dialog background were a pane of clear glass.

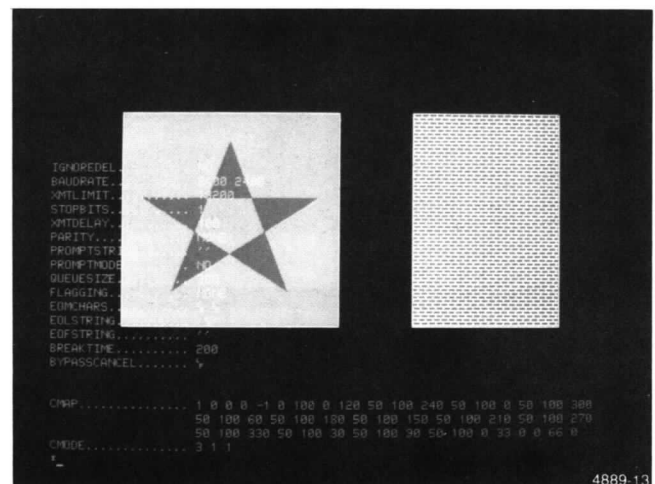


Figure 3-8. Display With Transparent Dialog Area.

OPERATING INFORMATION

13. Finally, set the dialog area back to 5 lines by entering:

DALINES 5

You are now ready to explore the use of the Menu key. The following discussion explains menu operation in general. Then Exercises 3 and 4 show how to use the color interface to modify the colors on the display, and how to use the viewing keys. Without making any changes to what you have done, read *The Menu Key*, then proceed to Exercise 3.

THE MENU KEY

In the middle of the row of function keys along the top of the keyboard is a key labeled *Menu*. This key gives you access to two sets of terminal functions:

- The color interface. This allows you to modify the colors displayed on the screen just by pressing a few keys.
- The terminal's Zoom, Pan, and View features. These allow you to select portions of a graphics display for more detailed viewing.

First press the Menu key. The terminal goes into Menu mode and displays a brief menu (Figure 3-9). In Menu mode, the terminal suspends any other activities temporarily and saves any information from the host until it can be processed (that is, until the terminal leaves Menu mode).

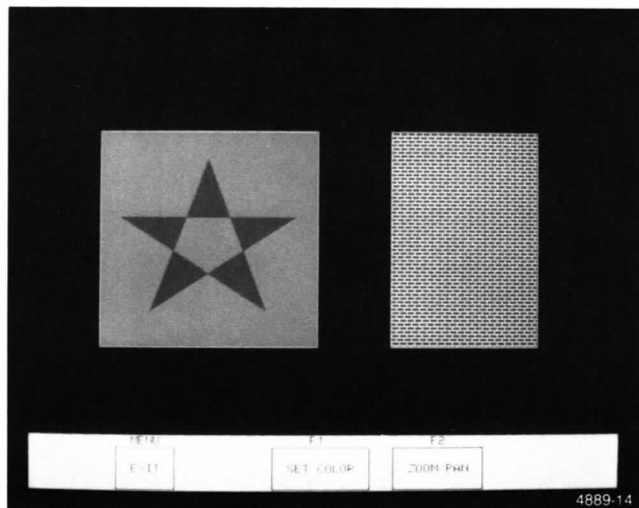


Figure 3-9. Menu Mode Display.

When you see this menu, you can do any of the following:

- Press Menu again to exit Menu mode and return to whatever the terminal was doing before you pressed Menu.
- Press F1 to activate the interactive Color Interface. Function keys F1 — F5 are programmed to modify color definitions.
- Press F2 to activate Viewing mode. Function keys F1 — F5 are programmed to perform viewing functions.

Figure 3-10 shows the mode transitions and what keys control them. In particular, note that pressing Menu in Menu mode, Viewing mode or Set Color mode returns you to "normal" terminal operation — that is, to whatever the terminal was doing before you pressed Menu.

Now press the Menu key again to exit Menu mode.

Exercise 3 explores what happens when you press F1: SET COLOR to activate the interactive color interface. Exercise 4 explores what happens when you press F2: ZOOM/PAN to activate the viewing keys menu. Without making any changes to what you have done, proceed to Exercise 3.

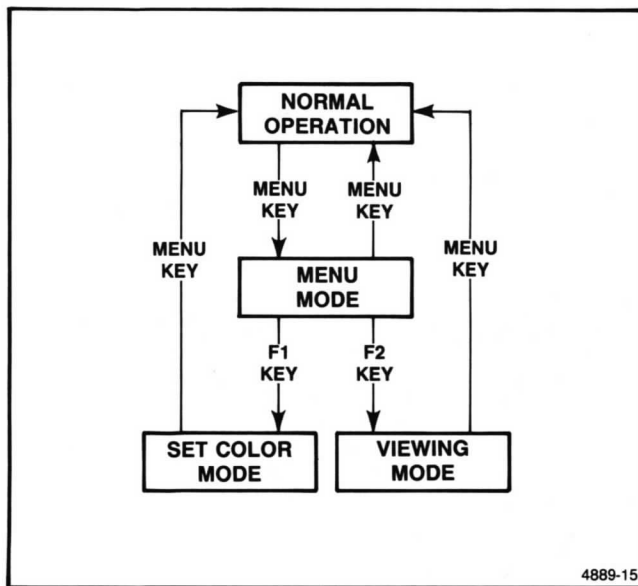


Figure 3-10. Menu Mode Transitions.

EXERCISE 3: USING THE COLOR INTERFACE

This exercise explores the terminal's interactive *color interface*. The color interface allows you to modify colors from the keyboard and to see the colors change as you modify them. Then you can keep the new colors, try others, or keep the ones you started with. Before you use the color interface, however, a bit of explanation will be helpful.

The terminal contains a *palette* of 64 distinct colors to choose from. The terminal defines each color in terms of the HLS (hue, lightness, and saturation) system of color specification, shown in Appendix F of the *4107/4109 Operators Manual*. With the terminal's color interface, however, you need not remember HLS parameters for the colors you want to display.

Colors for display are labeled by numbers called *color indices*. There are 16 *graphic indices* (for the graphics area) and 8 *dialog indices* (for the dialog area).

One way to change colors on the display is to change the indices. You have already done this several times. For example, the **DAINDEX 1 2 4** command in Exercise 1 set the dialog area color indices: *color 1* (or *index 1*) for text characters, *color 2* for character cells, and *color 4* for the background. Currently, color 1 is white, color 2 is red, and color 4 is deep blue.

With the color interface you can also change the actual color definition — the HLS values — assigned to any index. For example, you can change dialog index 1 from white, say, to brown. Thereafter, all text in the dialog area will be displayed in brown.

There are three ways to use the color interface to modify a color definition; for convenience these are referred to as Methods 1, 2, and 3. In this exercise you will use all three methods. First, however, let's get acquainted with the color interface itself.

Activate the Color Interface

1. Press the Menu key (located in the row of function keys across the top of the keyboard). When the menu appears, press F1 (now defined to be SET COLOR). This places the terminal in Set Color mode, activates the color interface, and displays a banner across the bottom of the screen.

Part of the banner shows how the function keys F1 — F5 are now programmed. Set Color mode temporarily suspends any macros (special key definitions) assigned to these function keys. When you exit the color interface, the macros are automatically re-assigned to the keys. (Exercise 6 shows how to program a macro into a function key.)

Note the flashing message **Press S Eras key to erase screen and display current colors. DO NOT PRESS S Eras NOW.** We will explore this option later in this exercise.

2. There is a crosshair cursor centered at the bottom left of the screen. Press the upper right of the joystick to move the crosshair around a bit. Note that the **Press S Eras** message disappears as soon as you move the crosshair. Then move the crosshair cursor over the blue portion of the box with the star.

Now take a few moments to examine the white banner at the bottom of the screen (Figure 3-11). The left part of the banner indicates that the cursor is in the *graphics* area. It also displays a small square of the color under the color index (4).

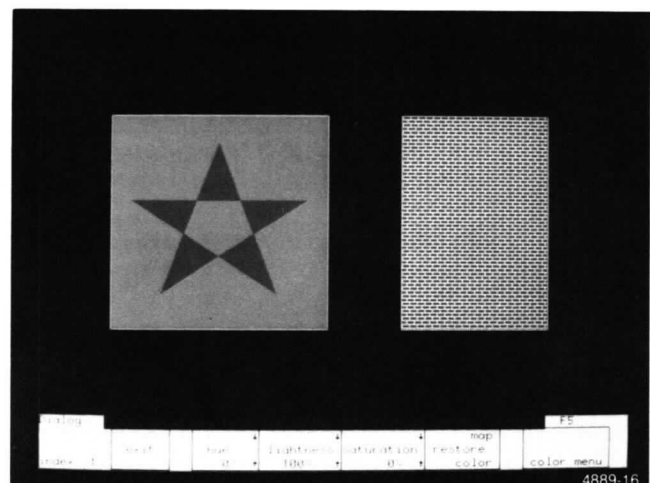


Figure 3-11. Color Interface Banner.

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Note the label *Surface 1* just above the color square. This indicates that the small dot of color under the crosshair belongs to graphics surface 1. The terminal can define up to four separate graphics surfaces and use these for multilayered displays, as discussed briefly under *Features* earlier in this section. Surfaces are usually defined by the host application program, and at power-up there is always just one graphics surface defined.

The boxes labeled F1, F2, and F3 show the hue, lightness, and saturation (HLS) values for this color.

The rest of the banner shows which function keys are programmed when the color interface is active. Table 3-1 summarizes the action of the function keys.

Now press Menu to exit the color interface, and proceed to Method 1.

Table 3-1
COLOR INTERFACE KEYS SUMMARY

Key	Action
F1	INCREASE HUE. Increases hue by 10°.
Shift-F1	DECREASE HUE. Decreases hue by 10°.
F2	INCREASE LIGHTNESS. Increases lightness by 10 units.
Shift-F2	DECREASE LIGHTNESS. Decreases lightness by 10 units.
F3	INCREASE SATURATION. Increases saturation by 25 units.
Shift-F3	DECREASE SATURATION. Decreases saturation by 25 units.
F4	RESTORE COLOR. Restores the HLS values before the last cursor movement. If cursor has not moved since HLS changes, F4 restores the color; if cursor has moved, no effect.
Shift-F4	RESTORE COLOR MAP. Restores all color settings to their values before you entered Set Color mode.
F5	COLOR MENU. Displays a menu of nine predefined colors for selection via the crosshair cursor.
Shift-F5	VIEW MENU. Turns the color banner on or off. When the banner is off, the dialog area is displayed even though Set Color mode is still active.

Method 1: Modify a Displayed Color

This method allows you to modify any displayed color.

NOTE

The displays for this exercise were prepared using a 4109. HLS values are slightly different from those given in the text.

1. Press Menu, then press F1 to activate the color interface. Ignore the **Press S Eras** message. Note that the crosshair is back at the lower left corner of the screen. Move the crosshair over the blue square again.
2. The color under the crosshair (blue) has hue 0°, lightness 50%, and saturation 100%. Modify this color definition as follows:

- Press F1 until the hue setting at the bottom of the screen reads 150°. Since the terminal's Autorepeat feature is on, you can hold the key down instead of pressing it repeatedly. If you go past 360, the hue setting just wraps around to zero.

Note that pressing F1 *increases* the hue setting. Pressing Shift-F1 *decreases* the hue setting, with wraparound to 360 if you go past zero.

- Now press Shift-F2 until the lightness reads 30%.
- Leave the saturation at 100%.

3. You have redefined color 4 in the graphics area to brown, with HLS values of 150, 30, 100 (Figure 3-12). You can now do any of the following:

- Before you move the crosshair, press F4 to restore the original color.

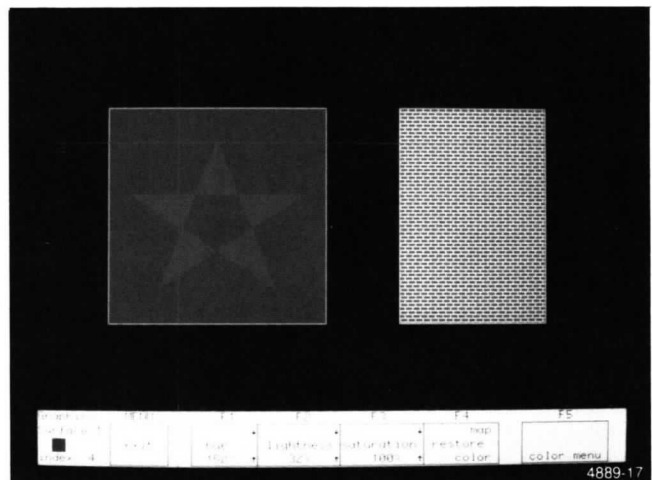


Figure 3-12. Display With Modified Color.

- Move the crosshair to another color and modify it. Note from Table 3-1 that once you move the crosshair, colors already modified are not affected by F4; however, Shift-F4 resets all colors.
- Press Menu to exit the color interface and save the modified color definition(s). These definitions are saved until you turn the terminal off or modify the colors again. (The new colors are *not* saved when the terminal is turned off.)

Now press Menu to exit the color interface and save brown (150, 30, 100) as the color definition assigned to index 4. When you exit the color interface, the dialog area reappears and the new graphics area colors remain in effect. All future occurrences of color 4 in the graphics area will be the same color as the box.

Method 2: Color Menu

Another way to modify a color is to use function key F5. This key displays a menu of predefined colors that you can select just by moving the crosshair to the appropriate color name.

1. Press Menu, then press F1 to activate the color interface. Move the crosshair to the red star.
2. Press F5 and hold it down. This displays a menu of nine color names beside the cursor (Figure 3-13A).
3. Hold down F5 and move the crosshair over the color menu. Notice that the star changes to the color whose name is under the crosshair. Move the crosshair up and down the menu. (You may also want to hold down the Shift key to slow the cursor.) Move the crosshair to the color name **olive** (Figure 3-13B). Then release the crosshair; the star remains olive.

Notice that when you change the color of the star, the color of the brick pattern changes too. This is because the bricks have the same color index (2) as the star. When you modify one occurrence of a color in the graphics display, *all* occurrences of that color are modified.

4. Press F4 to return the star to its original color. Then press Menu to exit the color interface.

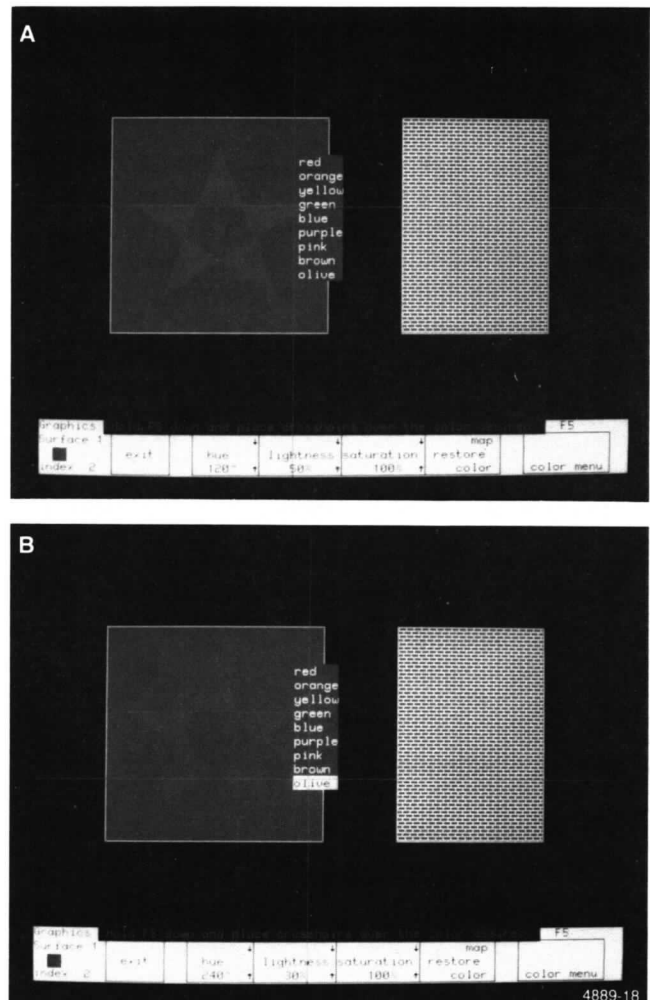


Figure 3-13. Using the Color Menu.

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Method 3: Redefine the Color Map

Method 3 allows you to modify the complete *color map* (the assignment of colors to color indices).

1. Press Menu, then press F1 to activate the color interface. *Do not move the crosshair.* Instead, press S Erase and the display shown in Figure 3-14A appears. This shows the 16 graphic indices and the 8 dialog indices, along with color samples and HLS values.

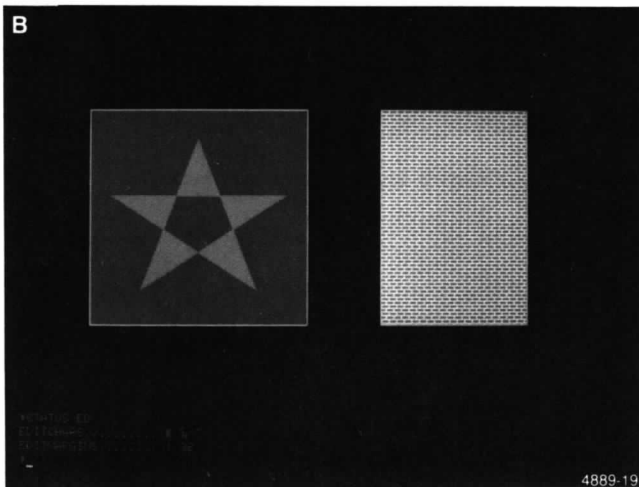
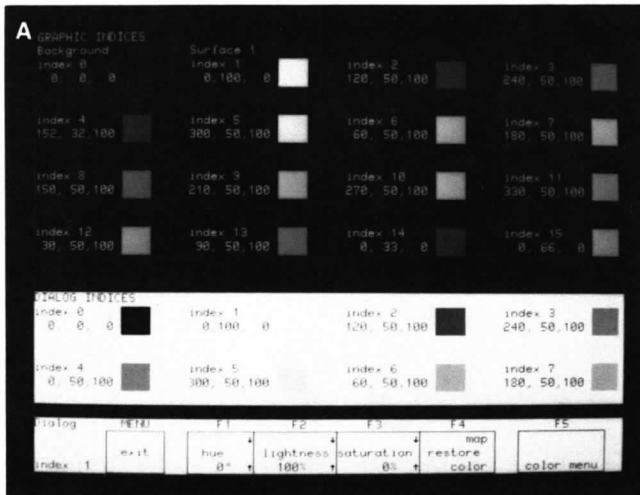


Figure 3-14. Complete Color Map.

2. Move the crosshair to the square sample of index 3 in the dialog area. Using F1, change its hue to 130. Leave the lightness and saturation unchanged.
3. Now move the crosshair to the square sample of index 2 in the graphics area. Use F1 to change the hue value to 150.
4. Now move the crosshair to index 4 in the graphics area. Press F5 and use the color menu to change index 4 to *olive*.
5. You can now do any of the following:

- Without moving the crosshair, press F4 to restore the color you just changed.
- Press Shift-F4 to restore *all* the previous colors.
- Press Menu to save the new colors.

Press Menu. The three color indices that you have just modified are saved to their previous values and the graphics display reappears.

6. Note that the new color definitions are now in effect: segment 1 (the square) is now displayed in olive, and the brick pattern in the rectangle is displayed in brown. Now give the command:

STATUS ED

Dialog text is now displayed in the new dialog index 3 (Figure 3-14B).

Look carefully at the display for a moment. Note that the bricks and the star do not appear to be the same color. Also, the reddish brown text appears almost red against the black dialog area background. How a given color is perceived depends on a number of factors, including how much of the color is displayed and the color(s) of surrounding areas. It is wise to remember this when you redefine colors.

EXERCISE 4: THE VIEWING KEYS

This exercise explores how you can control the graphic display using the terminal's viewing keys.

1. First press Setup to remove the terminal from Setup mode. The viewing functions will not work with the terminal in Setup mode.
2. Press Menu, then press F2: ZOOM/PAN. This puts the terminal in Framing mode and displays the viewing keys menu, shown in Figure 3-15. This menu shows the functions of F1 through F5 (at the bottom of each box) and their shifted versions (at the top of each box).

Any macro definitions already assigned to these keys are suspended while this mode is active.

3. Note that there is a dotted border around the entire graphics area — the *framing box* — and a pair of dotted brackets that form opposite corners of a rectangle. Also notice that the word *ZOOM* is displayed on a different background in the banner at the bottom of the screen. This indicates that the terminal's *zoom* function is active.

Press on the bottom or on the left of the joydisk, and the framing box (and zoom indicators) decrease in size. Then press on the top or the right of the joydisk, and the framing box increases in size.

Use the joydisk to decrease the framing box until it includes only part of the box and star. Then press F3 (UPDATE VIEW). The screen is redrawn *with the part of the picture that was in the framing box now filling the entire graphics area* (Figure 3-16). Note that the framing box now includes the entire graphics area.

4. Now press on the right of the joydisk to increase the size of the framing box. The dotted border does not appear, but the pair of framing corners expands until most of the screen is included. Press F3 again to *zoom out* to a larger window. You cannot zoom out to a larger window than the original window in effect when you created the graphics.
5. Now press Shift-F2, OVERVIEW, to return to the original view. The framing box shows the part of the original view that was displayed in the previous view.
6. Next press F2 (PAN). Without modifying the view, the terminal activates its pan function. Note that the dotted brackets in the framing box have been replaced by a crosshair, and that the word *PAN* in the banner is displayed on a different background.

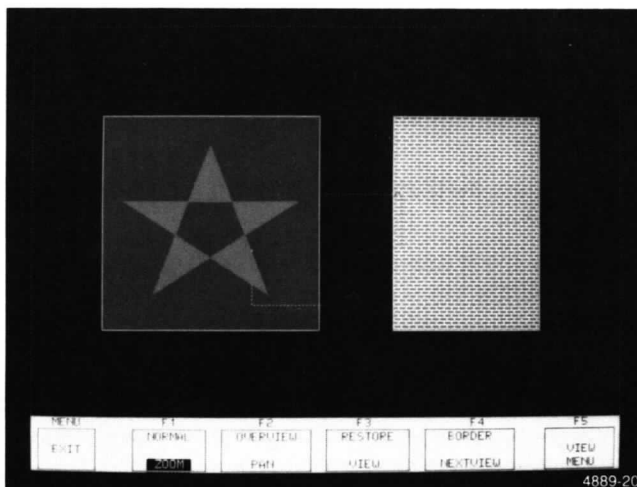


Figure 3-15. Viewing Keys Menu.

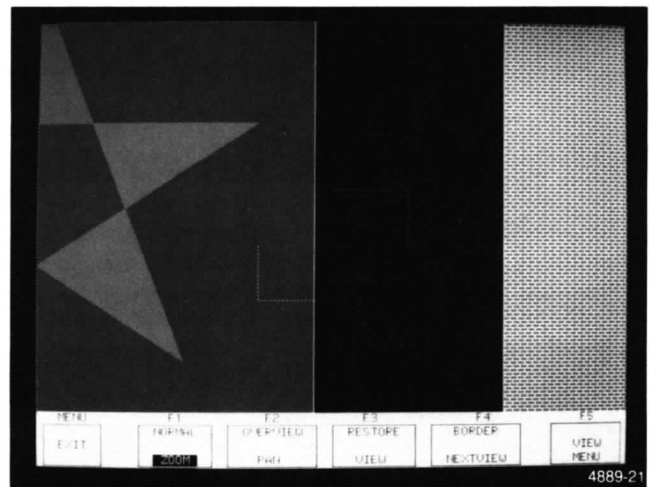


Figure 3-16. Display After Zoom and UPDATE VIEW.

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7. Now press on the joydisk to move the framing box and pan indicator around. Press the top of the joydisk to move the box up; press the right of the joydisk to move the box to the right; etc. Position the framing box over the star (Figure 3-17A). You may have to increase the display intensity in order to see the framing box.
8. Now press F3, UPDATE VIEW, to redraw the display. The part of the picture inside the framing box now fills the entire graphics area, with the crosshair in the middle of the display (Figure 3-17B). If you move the crosshair around and press F3 again, you see a different part of the display, but the size does not change.
9. Now press F1 (ZOOM). The crosshair is replaced by the zoom brackets, the word *ZOOM* in the banner is highlighted, and you are now in Zoom mode. You can shift from Zoom to Pan, or Pan to Zoom, at any time just by pressing F1 or F2.

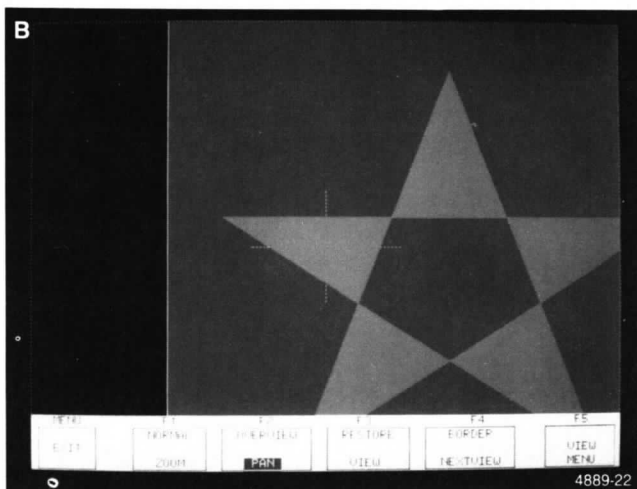
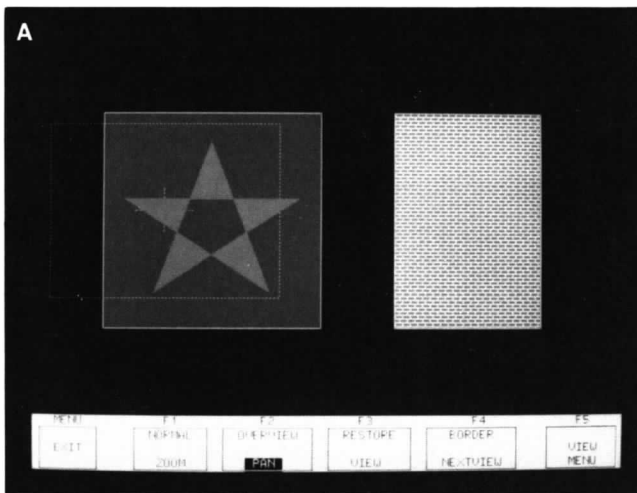


Figure 3-17. Display With Pan.

10. The terminal can define and store up to four different *views*. In fact, you have already done this. Each time you pressed F3, UPDATE VIEW, in the preceding steps the terminal saved that *view* in its memory, including the viewing mode (Zoom or Pan).

Pressing Shift-F3, RESTORE, displays the most recent view — that is, the view that was on the screen when you pressed F3 the last time and the viewing mode (Zoom or Pan). Pressing RESTORE again displays the next most recent view, and so on, up to a limit of four views. When you have cycled through all the saved views, pressing RESTORE again takes you back to the first one.

Try this now. Press RESTORE several times and note that the resulting displays are those that were displayed when you pressed F3, UPDATE VIEW. The original view is always saved, so you can always get back to the display you started with.

11. Now press F5, VIEW MENU. The ZOOM/PAN menu disappears and the dialog area reappears. You can press Setup to enter Setup mode; the terminal will suspend ZOOM/PAN mode until you exit Setup mode.

Press F5 again and the ZOOM/PAN menu reappears.

The Dialog key is also active in ZOOM/PAN mode; it toggles the ZOOM/PAN menu (or dialog area) on and off.

12. Press F5 so the ZOOM/PAN menu is not displayed. Then press Shift-F4, BORDER. A solid border appears around the edge of the graphics area, framing the entire display. Press Shift-F4 again to turn the border off.

This illustrates the basic use of the zoom and pan functions. To summarize:

- In Zoom mode you can zoom in or out to make parts of the picture larger or smaller.
- In Pan mode you can move across, up, or down the picture to display different, perhaps widely separated, parts of the picture.
- You can switch from Zoom to Pan and vice versa simply by pressing the appropriate function key.
- Pressing F3, UPDATE VIEW, saves the current view; you can cycle through the three most recent views and the original view with Shift-F3, RESTORE.

It is recommended that you experiment further with the ZOOM/PAN menu and functions to get better acquainted with them. Table 3-2 will serve as a handy reference; it lists the functions of each key, including their control versions. Note that a key, its shifted version, and its control version may have different meanings.

Table 3-2
VIEWING KEYS SUMMARY

Key	Action
F1	ZOOM. Activates zoom function and displays framing box. Joydisk changes size of framing box. Press F1 again to cancel zoom function.
Shift-F1	NORMAL. Readjusts aspect ratio to match original window of current view.
Ctrl-F1	FIXED ZOOM. Equivalent to pressing ZOOM, decreasing size of framing box, then pressing VIEW.
F2	PAN. Activates pan function and displays framing box. Joydisk changes location of framing box. Press F2 again to cancel pan function.
Shift-F2	OVERVIEW. Selects default window of entire screen (4095x3127) for current view and renews the current view.
Ctrl-F2	SUPER OVERVIEW. Selects a "super window" that includes all of 4096x4096 terminal space.
F3	(UPDATE) VIEW. Sets the window for the current view to match the framing box and renews the current view.
Shift-F3	RESTORE. Restores the current view's window and framing box to their status before the last VIEW, OVERVIEW, or SUPER OVERVIEW operation.
Ctrl-F3	UPDATE NEXT VIEW. Equivalent to pressing NEXT VIEW (F4), UPDATE VIEW (F3), then LAST VIEW (Ctrl-F4), in that order.
F4	NEXT VIEW. Saves status of the current view and makes the next higher numbered view the current one.
Shift-F4	BORDER. Turns the border around the current view on or off.
Ctrl-F4	LAST VIEW. Similar to NEXT VIEW, but selects the next lower numbered view.
F5	VIEW MENU. Turns display of the ZOOM/PAN menu on or off. When the menu is turned off, the dialog area reappears.

EXERCISE 5: GIN (GRAPHIC INPUT)

This exercise gives a brief introduction to GIN (Graphic Input) mode and two of the GIN features you may find useful: *inking* and *rubberbanding*.

The terminal can perform a variety of graphic input functions using the 4957 Graphics Tablet. Occasionally, a 4662 or 4663 plotter may be used for GIN. In this exercise, you will input a few GIN points from the keyboard.

Since GIN is almost always done under host control, the full range of GIN capabilities is discussed in the Programmers manual. Also, the host program controlling GIN should generally give instructions on how to do GIN for the particular application.

1. With the terminal in Setup mode, enter the following commands:

GINENABLE 0 5
GININKING 0 2

The GINENABLE command turns on GIN mode and instructs the terminal to remain in GIN mode until 5 points have been input from the terminal's keyboard, with the joydisk as the GIN device. As soon as the GINENABLE command has been entered, a crosshair cursor appears on the screen.

The GININKING command turns on the inking feature. You will see how this operates shortly.

2. Now press Setup. The terminal leaves Setup mode and enters GIN mode.

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3. Now move the crosshair around the screen with the joydisk, then press any key on the terminal keyboard. Since inking is turned on, a vector is drawn from the origin to the screen location under the crosshair (Figure 3-18A).

When the terminal is connected to a host computer, pressing a key as you did above will send the coordinates of the point under the crosshair to the computer. These coordinates can be stored or processed in some way, depending on the applications program. This is the real purpose of GIN mode, to send coordinate information to the computer; vectors drawn on the screen are simply for visual reference.

4. Now move the crosshair to another location and again press any key on the keyboard. Each time you do this a vector is drawn from the previous location to the current one (Figure 3-18B).

Since GIN was enabled for only 5 points, after the fifth point has been located in this way, the crosshair disappears and the terminal leaves GIN mode.

5. Now press G Eras. Since the inked GIN vectors are not part of a segment definition, they are erased.
6. Now press Setup again, then enter the commands:

```
GINENABLE 0 5
GINRUBBERBAND 0 2
```

This enables GIN mode for another 5 points and turns on the terminal's *rubberbanding* feature. Now press Setup to leave Setup mode, and move the cursor around the screen. As you do, a vector — called a *rubberband line* — is continuously drawn from the last point located to the current crosshair location.

Since inking feature is still turned on, each time you locate a point by pressing a key, a vector is drawn to that location, just as in the steps above.

After 5 points have been located in this way, the terminal leaves GIN mode and the crosshair disappears. Press G Eras to clear the screen of the GIN vectors that were drawn.

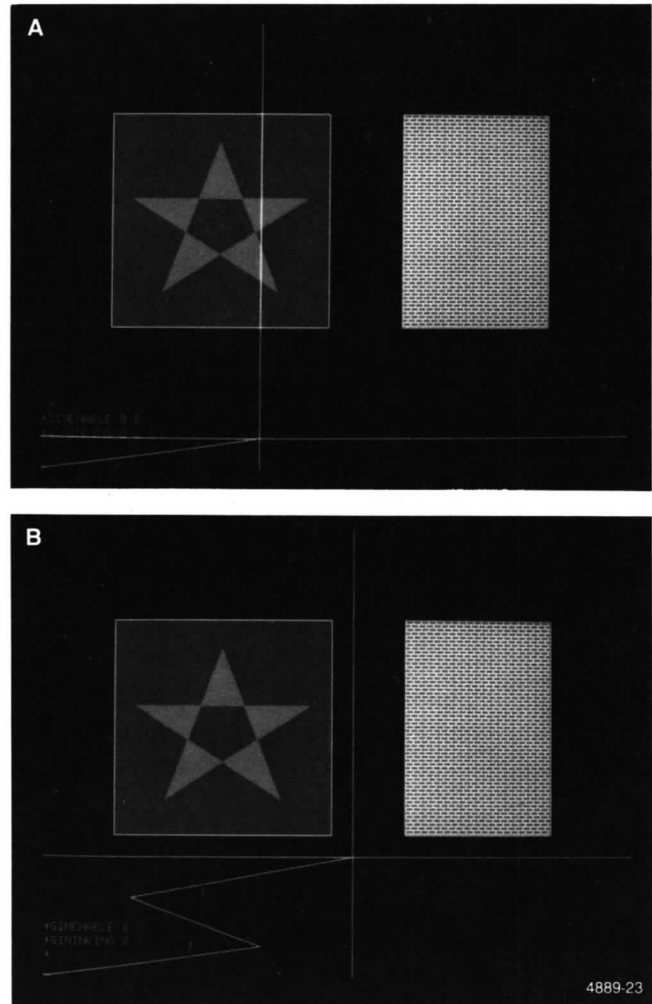


Figure 3-18. Graphic Input With Inking.

EXERCISE 6: PROGRAMMING A KEY

Each key on the terminal keyboard generates a default meaning when the key is pressed. For example, the A key generates the ASCII code for the *a* character (or *A*, when Shift is also pressed). However, you can program a key to generate a different character, or even a sequence of characters, for your convenience.

A sequence of characters programmed into a key is called a *macro*. When you press the key, the macro is *expanded* — that is, the characters are entered into the terminal just as if you typed them in one by one. A macro may contain text, commands to the terminal or host, or a combination of these.

All keys except *Shift*, *Ctrl*, and *Caps Lock* can be programmed from either the keyboard or the host.

NOTE

Be cautious about programming alphanumeric keys. For example, if you program the Return key, you cannot use it to terminate a command.

Macros are identified by *macro numbers* in the range from -150 through 32767. Macros -150 through 143 correspond to keys on the keyboard (including their Shifted, Ctrl, and Ctrl-Shifted versions). Macros 144 through 32767 do not correspond to keys.

This exercise shows how to program a key, how to save the macro even when the terminal is turned off (if you wish), and how to return a programmed key to its default meaning. In addition, the exercise allows you to explore the terminal's predefined *fill patterns* at your leisure.

There are four commands that allow you to program a key:

- **LEARN** lets you program only keys. When you enter LEARN, the terminal prompts you as to what to do next. LEARN macros are lost when the terminal is turned off or reset.
 - **NVLEARN** works like LEARN, but NVLEARN macros can be saved in nonvolatile memory by NVSAVE.
1. Exercise 2 introduced the FILLPATTERN command. Since you will use this command several times in the next few steps, program Function Key F5 to generate the command name, followed by a space:

DEFINE F5 "FILLPATTERN "C_R

Be sure to type in the key name F5, not press the F5 key. Since you must separate the pattern number from the command name by a space, putting the space in the macro saves time. The quotation characters serve as *delimiters* for the defined string, and are required for the DEFINE and NVDEFINE commands.

To execute a Setup command, the command must end with a C_R — a Carriage Return. You can include the C_R character in a DEFINE macro, as follows.
 2. Enter the command **STATUS EDITCHARS**C_R and examine the message:

EDITCHARS. R_U C_N ~

The third character, ~, is the *literal character*. This character allows you use DEFINE and NVDEFINE to create macros containing *control characters* — that is, characters that would normally be executed. The next step shows an example.

- **DEFINE** lets you define a macro for any key or macro number (including macros 144 and up which do not correspond to any keys). A macro created with DEFINE will be lost when you turn off the terminal or reset it.
- **NVDEFINE** works just like DEFINE, but NVDEFINE macros can be saved in nonvolatile memory by NVSAVE. When you turn the terminal off, then back on again, the macro will still be defined.

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3. Program F6 to execute the BEGINPANEL command:

```
DEFINE F6 "BEGINPANEL 1000 1000 1 ~ CR"
```

The ~ before the C_R within quotes tells the terminal that the next character is a literal character and not to be executed. When you press Return, the cursor backspaces over the ~ and prints the C_R symbol instead of performing a Carriage Return operation. (You must press Return again to terminate the DEFINE command.)

The LEARN and NVLEARN commands let you program keys without worrying about literal characters. However, function keys F1 and F2 are reserved for displaying prompts, so if you want to program these keys, you must use DEFINE/NVDEFINE.

4. To see how LEARN/NVLEARN works, let's use LEARN to program F7 to complete the panel definition begun by F5 and F6.

First enter the command:

```
LEARN
```

The terminal responds with the following prompt:

Press the key to be defined:

Press F7. The number 134 (the macro number for F7) is displayed and the terminal displays the next prompt:

Enter definition. (F1 terminates definition, F2 deletes last character)

Just enter the following definition for F7, and press F1 to terminate the definition:

```
DRAW 2000 1000CR DRAW 2000 3000CR  
DRAW 1000 3000CR ENDPANELCR
```

Note that you can press Return and not have to worry about the literal character, as you did with DEFINE. If you make a mistake, use F2 to back up and correct the error (just like you use the Rub Out key in Setup mode).

Notice that we have programmed one key to contain several commands. (You can do this with DEFINE/NVDEFINE also, but each time you enter C_R, you must precede it by a literal character.) You can even make a key definition longer than one line: just keep typing and the text will *wrap around* to the next line.

Now that you have programmed these keys, let's use them to explore some of the terminal's predefined color patterns.

5. Press F5. The command name FILLPATTERN appears, followed by a space. Enter an integer between 1 and 16, then press Return. The fill pattern for subsequent panels is now set. This fill pattern remains the same until you change it or turn off the terminal.
6. Now press F6. The BEGINPANEL command is executed and displayed in the dialog area. You will not see anything in the graphics area yet.
7. Now press F7. The panel begun in Step 5 is completed and filled with the pattern that you selected in Step 2.
8. You can now explore the patterns that are available with Function Keys F1 — F3:
 - Press F5 and enter a pattern number, then press Return.
 - Press F6 to begin the panel definition.
 - Press F7 to draw the panel and fill it with the pattern you have chosen.

Valid pattern numbers are:

- | | |
|----------|--|
| -16 — 0 | Colors 0 — 16. For example, pattern -5 is the same as graphics area color 5. |
| 1 — 16 | Textured patterns: stripes, diagonals, etc. |
| 50 — 174 | Dithered color patterns. These patterns use closely spaced dots of different colors to simulate additional colors. |

All predefined patterns are shown in Appendix J of the *4107/4109 Operators Manual*. Note, however, that these patterns use the terminal's factory default color map. Since you have modified the color map in this session, some patterns will look different on the screen.

9. The **MACROSTATUS** command allows you to examine a macro definition without executing it. For example, enter the following:

MACROSTATUS F3

The terminal prints the macro assigned to F3 on the screen, but does not execute it. You can examine all currently defined macros with the command **MACROSTATUS -1**.

10. You can delete a macro and return the key to its default meaning with the **LEARN** or **DEFINE** command. For example, to delete the macro assigned to F5 enter:

DEFINE F5

11. You may also want to try the following:
- Define keys to draw other boxes on the screen. Then you can compare different colors or patterns.
 - Use the color interface (Method 1 or 2) to modify the patterns. The dithered color patterns use the colors in the default color map. If you change the color map, pattern displays will be modified accordingly.

SUMMARY

This completes the familiarization procedure. Section 1 of the *4107/4109 Operators Manual* contains similar information but with color illustrations (instead of gray tones); that manual also contains references to the 4109, which you should ignore. Refer to that manual for more detailed information about 4107 commands and functions.

Section 4

THEORY OF OPERATION

This section describes the theory of operation of the Terminal Control board, Display Control board, RAM3 board, Power Supply Module, and the keyboard. Display Module theory is covered in its own separate service manual.

This theory write-up requires that the reader be generally knowledgeable about basic digital design. Certain abbreviations and acronyms have found their way into common use in the industry. Such terminology is used (sparingly)

because most digital-service technicians are aware of these terms.

Since many people assimilate and retain pictorial information more readily than text information, this section includes many illustrations and diagrams. The block diagrams present conceptual information, while the timing diagrams emphasize operating characteristics.

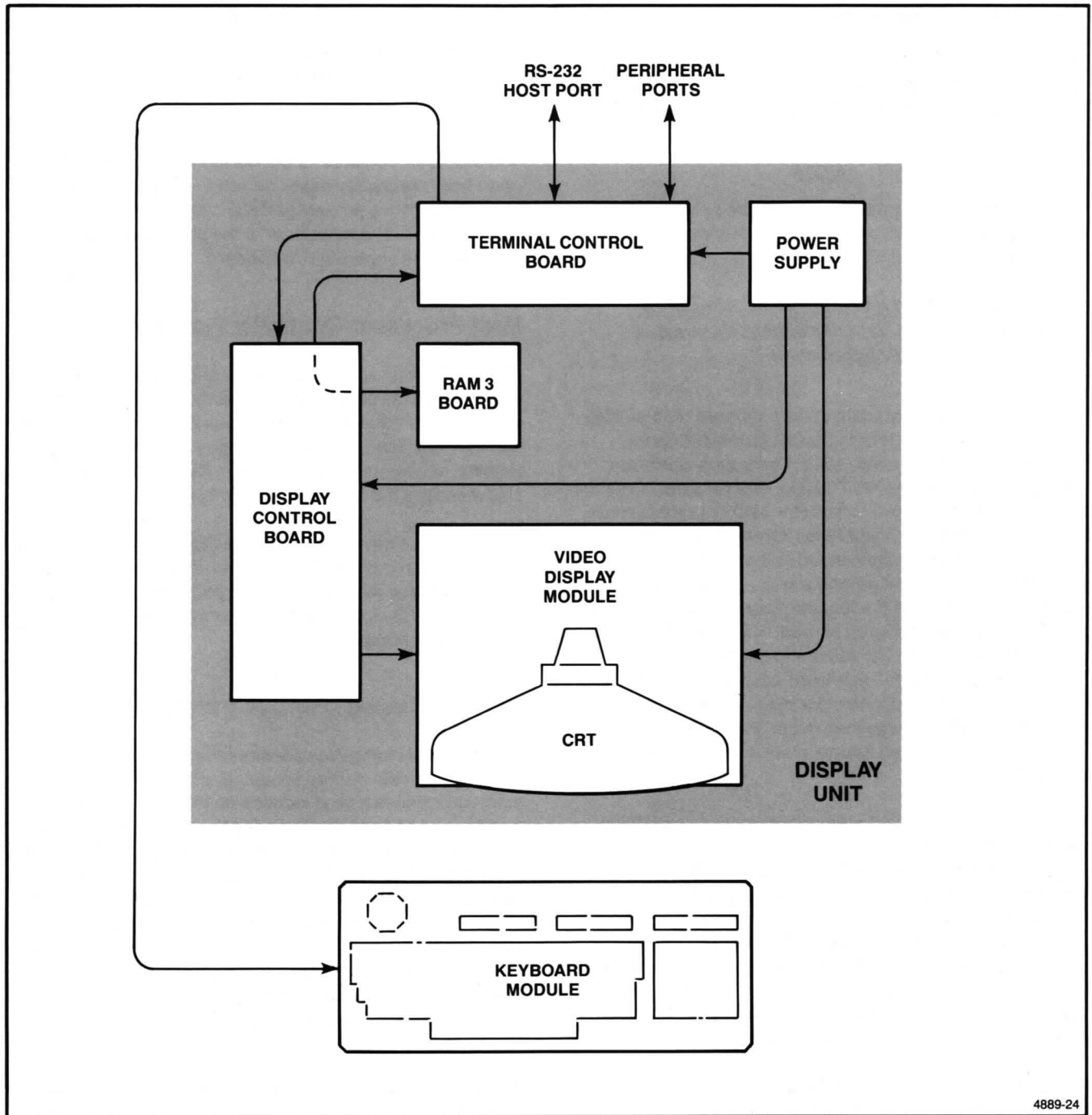
OVERVIEW

The 4107 Terminal is a computer display terminal that displays alphanumerics and graphics in color. It can be used for text editing, graphics display, and other general purpose input/output. The terminal's firmware decodes commands entered by the operator or sent by a host computer. The Programmer's Reference manual describes the range of firmware-related features. This theory discussion focuses on the hardware aspects of the terminal and only describes the firmware features needed for troubleshooting. The 4107 contains a Self Test routine in ROM that is the principal diagnostic tool for fault isolation.

Figure 4-1 is a block diagram of the 4107 terminal. This diagram shows the main functional modules of the terminal. These are:

- Terminal Control board
- Display Control board
- RAM3 (memory) board
- Color Display Module (approx. 15" diagonal measure)
- Keyboard Module
- Power Supply Module

Next is a simplified description of how the terminal processes data to make color graphics and text on the CRT screen. The detailed theory descriptions follow this overview (grouped under module or board headings).



4889-24

Figure 4-1. 4107 System Block Diagram.

GENERAL OPERATION

Let's begin by examining the general aspects of 4107 operation; namely, the processing, storage, and display of data. Refer to Figure 4-2 while reading this functional description.

NOTE

The term "dialog text" refers to alpha characters displayed in response to host-terminal command/data flow.

The term "pixel" (picture element) refers to the individual data dots on the display; the smallest unit of displayable information.

First, the operator enters data at the keyboard. The processor and keyboard/host interfaces (on Terminal Control board) convert this data into ASCII characters which are sent to the host over the RS-232 line. The response from the host may be alphanumeric character data or graphics data. In either case, the processor takes it from the host port and sends it to the appropriate memories (both are on the Display Control board). The graphics data memory consists of four bit-planes. Each of the four bit-planes stores data for all pixel locations on the display screen. These graphics memories then write four bits of data per pixel to the Color Map. The Color Map converts each four-bit pixel into one of sixteen colors, according to the color index loaded by the processor. This Color Map then sends the color coded pixels to the three guns (red, green, blue) in the Display Module's CRT.

Dialog data passes from the processor to the Dialog Memory list. At the appropriate times this list sends its contents (character bytes) to the Character ROM. The ROM converts each character byte into a corresponding pattern of pixels. As successive scan lines are read, this creates the character within a 7 x 9 pixel area. (See NOTE below). The serial stream of character bits enters the Color Map (along with graphics data). This map adds the color value to the alpha pixels and sends them to the Display Module, where they are superimposed on the graphics data image.

The "character attributes" (blinking or not, background transparent or opaque, etc.) are programmable via firmware codes. This attribute data is added to the dialog data by custom logic arrays located just ahead of the Color Map.

NOTE

Text characters occupy a 7 x 9 area in a 8 x 15 pixel cell. This allows room for borders, underline, and special characters.

The processor requires its own random access memory, apart from the display memories on the Display Control board. Part of this processor RAM is located on the Terminal Control board. The remainder of the processor RAM is located on the separate RAM3 board.

Host-Processor-Controller Functions

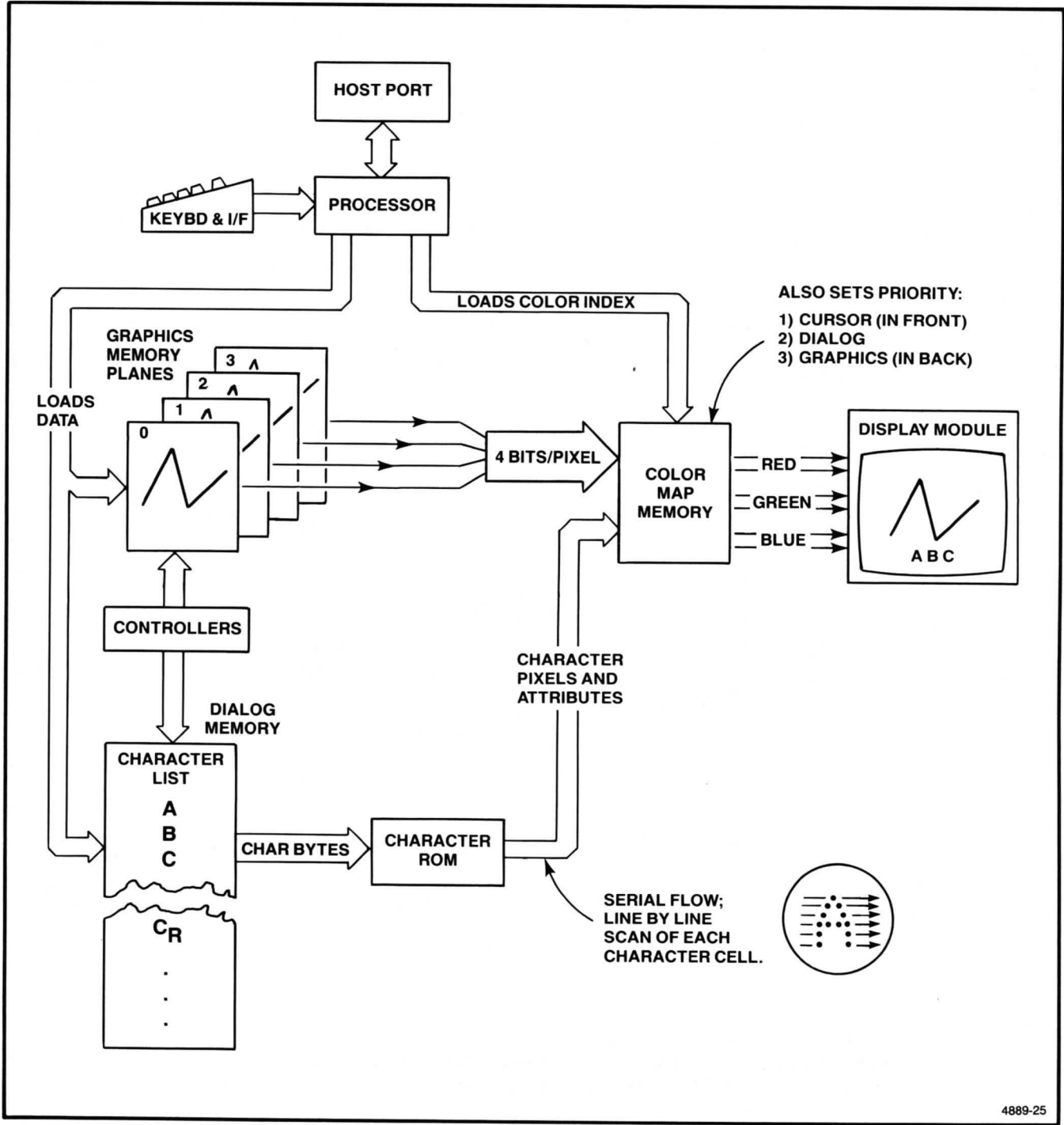
The host system sends commands and data to the 4107, which enters the host I/F. The processor executes these 4107-style commands, and manages host-terminal communications. The processor manages all functions in the terminal according to its firmware in ROM. This processor also manages the operations of the Display Control board.

The processor has direct access to the graphics and alpha memories, as do other DMA devices. The Display Control board accesses memory locations and sends the data to the screen for refresh without processor intervention; this provides faster operation.

Graphics/Dialog Displays and the Color Map

Graphics and dialog data are stored in memory arrays that correspond to the display screen. Each location in graphics memory matches a pixel location on the screen. The dialog memory is a list that sends data to the screen as whole characters (not pixels). The graphics/dialog data from these memories refer to a color index map on the way to the display screen. The color map is also a memory and stores the color index values written by the processor (in response to operator commands). The color map translates pixel data into one of the defined colors for display on the screen. The color map can be reprogrammed (via the processor) to contain any eight colors from a possible 64 color combinations.

The display screen contains a fixed "graphics area", and a scrollable "dialog area." See Figure 4-3. The dialog area background index is normally transparent, so the graphics area shows through on the screen. The display also features two types of cursors: the graphics cross-hair cursor, and the dialog cursor, of which there are two types: underline and full block.



4889-25

Figure 4-2. 4107 Functional Diagram.

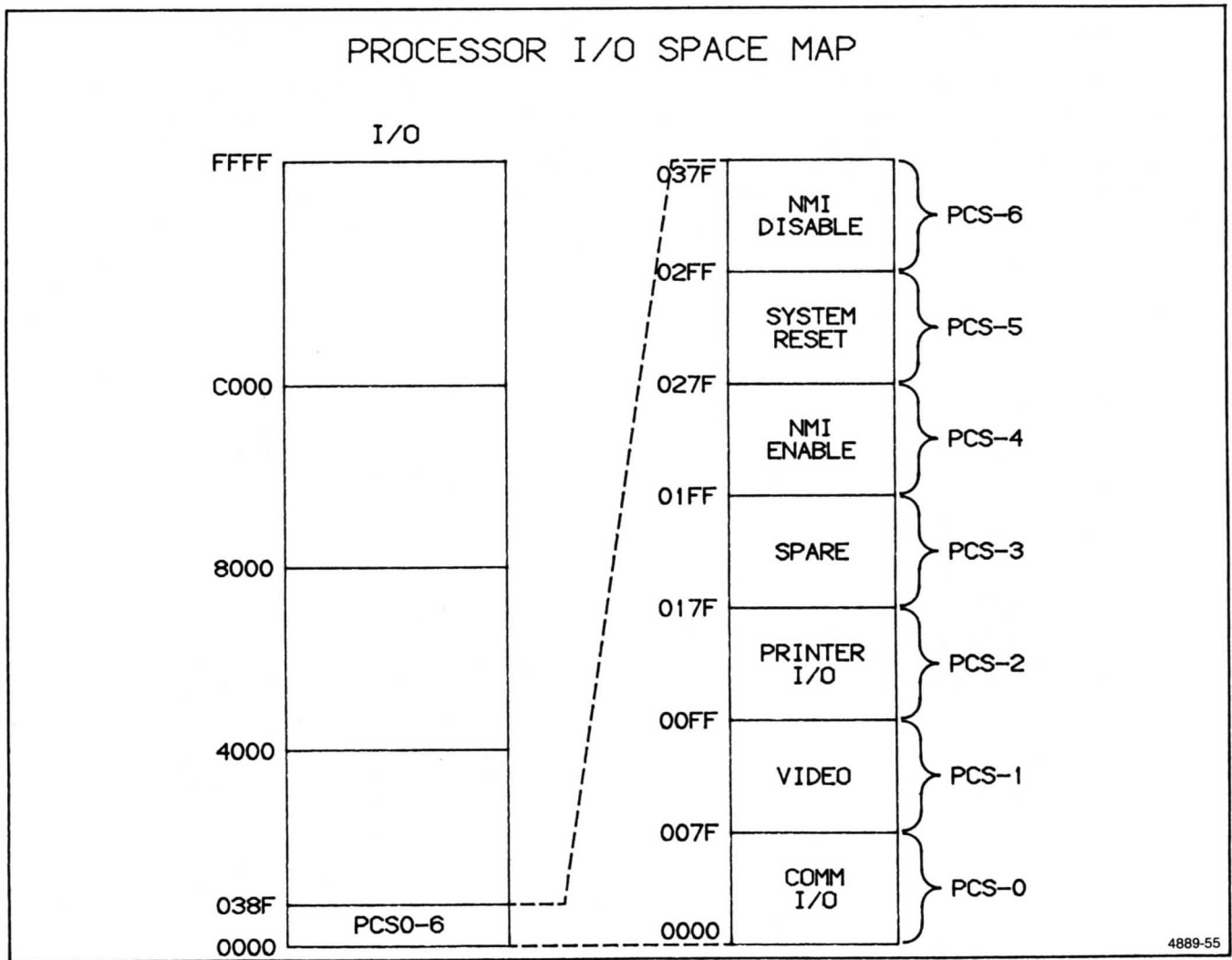


Figure 4-5. Map of I/O Address Space.

TERMINAL CONTROL BOARD

The following text describes the theory of operation of the Terminal Control board. This board contains the processor, main memory, and the interface units to the keyboard, host, and peripherals. Figure 4-6 shows the functional blocks that comprise the Terminal Control board.

The timing for the processor, its memory, and other devices, comes from 14.7456 Mhz crystal oscillator on the Terminal Control board.

A 96-pin connector passes data and control information to the Display Control board. Another such connector (physically located on the Display Control board) connects the Terminal Control board to the RAM3 memory board.

GENERAL BOARD OPERATION

The Terminal Control board architecture is based on the 80186 microprocessor. The board contains two busses:

- Processor address bus
- Processor data bus

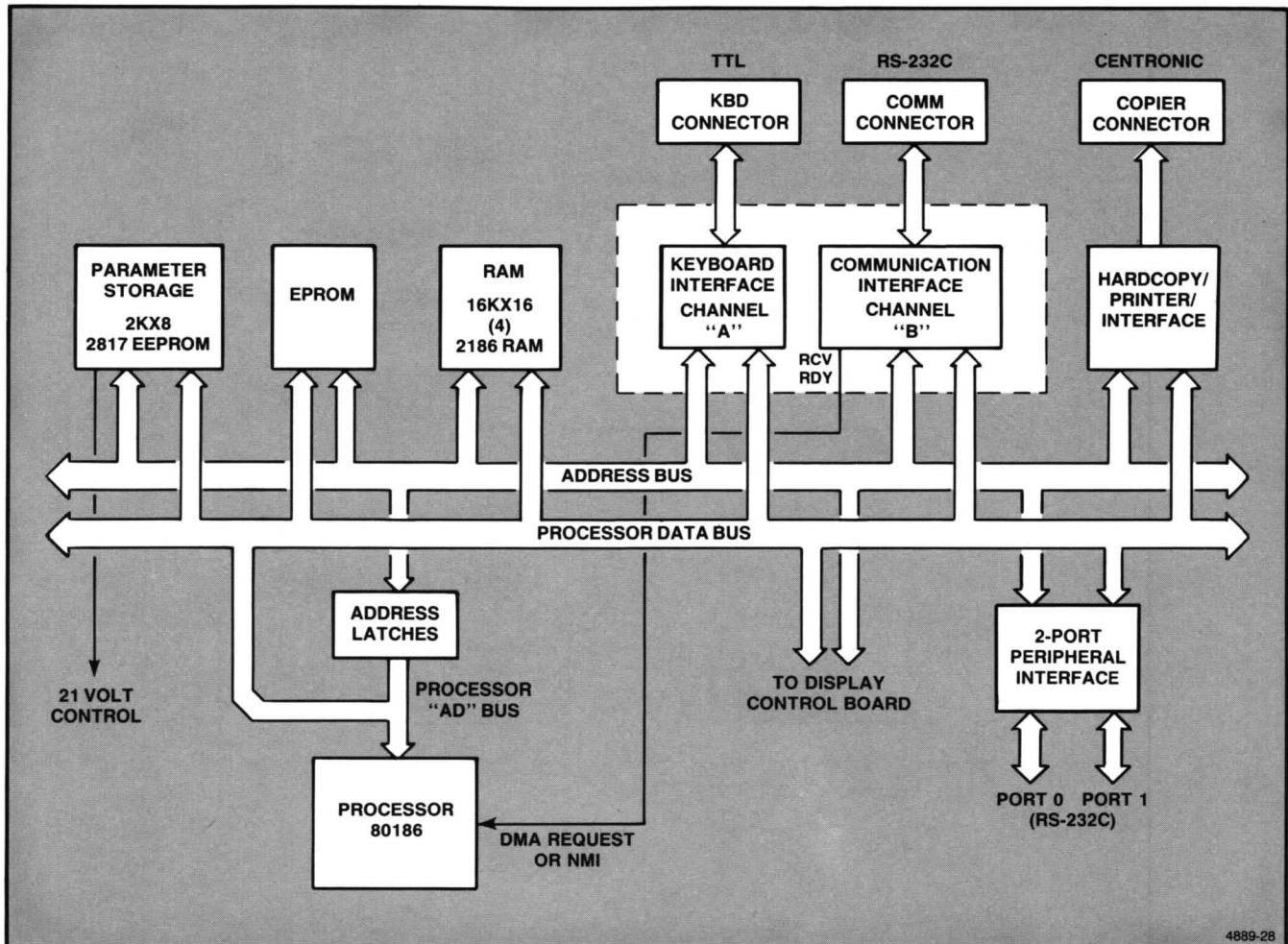


Figure 4-6. Terminal Control Board Block Diagram.

NOTE

The following text, on tinted pages, refers only to circuit blocks INSIDE the 80186 processor chip.

PROCESSOR BLOCK

The processor is an Intel 80186 16-bit high integration microprocessor. The processor can directly access up to 1 Mbyte of memory, and operates at 7.3728 MHz. (An external 14.7456 MHz crystal oscillator, on the Terminal Control board, feeds a divide-by-two counter in the processor.) The 80186 is a powerful microprocessor and also combines many peripheral functions on the single 68-pin chip. The

processor contains the following functional blocks:

- Execution unit (ALU and registers)
- Clock generator
- Programmable interrupt controller
- Programmable timers
- Programmable DMA
- Chip-select unit
- Bus I/F unit

Figure 4-7 is a simplified functional block diagram of the 80186, and shows these functions as sub-blocks. The following theory discussion describes each of these sub-block. Figure 4-8 shows the 80186 pin locations and their associated signal names, which are defined in Table 4-1.

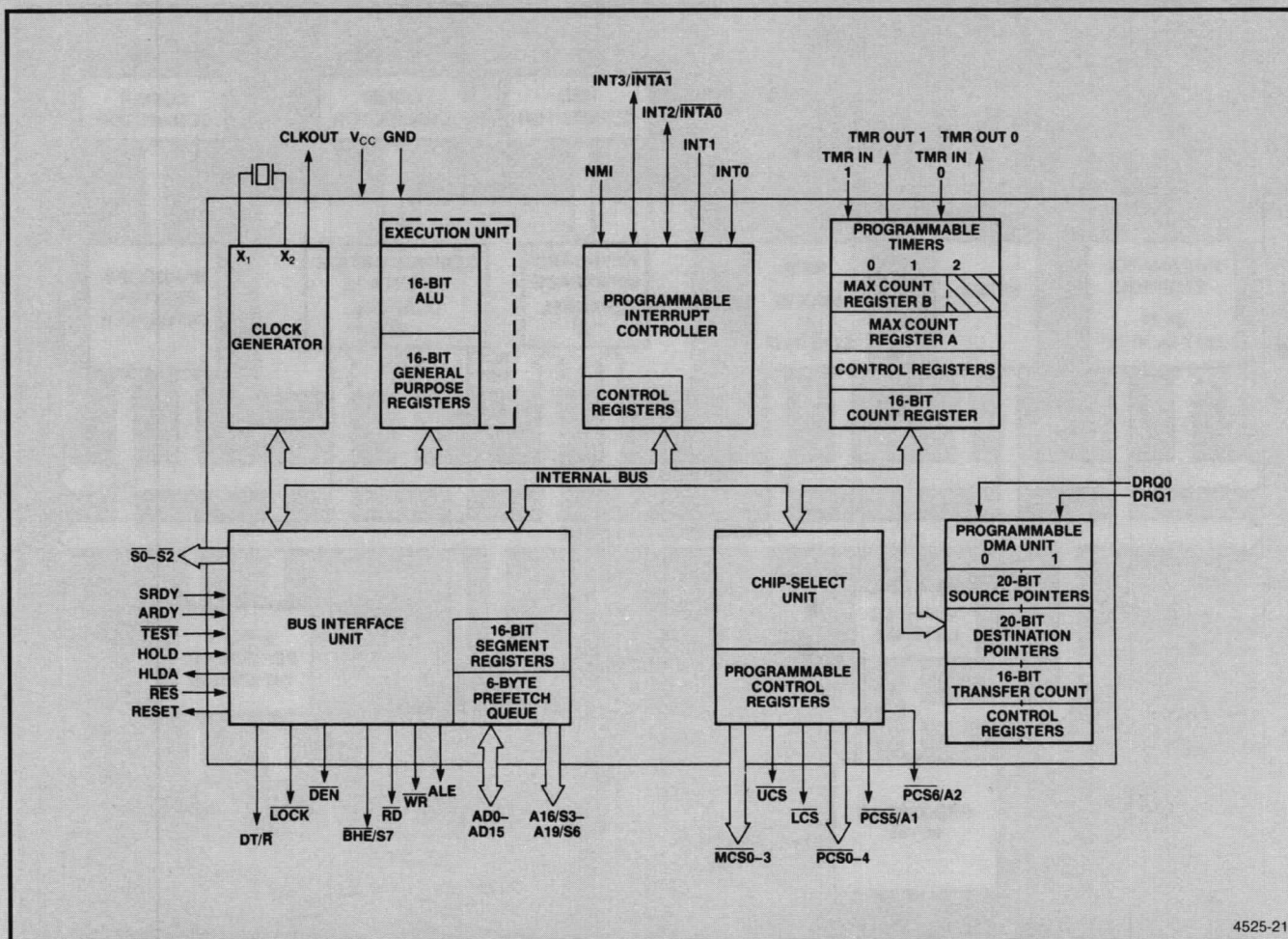


Figure 4-7. Processor Functional Block Diagram.

Table 4-1
PROCESSOR PIN DESCRIPTIONS

Pin	Name	Description
1	AD15	Address/Data Line
2	AD7	Address/Data Line
3	AD14	Address/Data Line
4	AD6	Address/Data Line
5	AD13	Address/Data Line
6	AD5	Address/Data Line
7	AD12	Address/Data Line
8	AD4	Address/Data Line
9	Vcc	+ 5V power in
10	AD11	Address/Data Line
11	AD3	Address/Data Line
12	AD10	Address/Data Line
13	AD2	Address/Data Line
14	AD9	Address/Data Line
15	AD1	Address/Data Line
16	AD8	Address/Data Line
17	AD0	Address/Data Line
18	DRQ0	DMA Request 0
19	DRQ1	DMA Request 1
20	TMR IN 0	Input to Timer 0
21	TMR IN 1	Input to Timer 1
22	TMR OUT 0	Output from Timer 0
23	TMR OUT 1	Output from Timer 1
24	RES	Reset (input)
25	PCS0	Programmable Chip Select #0
26	Vss	Ground
27	PCS1	Programmable Chip Select #1
28	PCS2	Programmable Chip Select #2
29	PCS3	Programmable Chip Select #3
30	PCS4	Programmable Chip Select #4
31	PCS5/A1	Programmable Chip Select #5
32	PCS6/A2	Programmable Chip Select #6
33	LCS	Lower bank Chip Select
34	UCS	Upper bank Chip Select
35	MCS3	Middle bank Chip Select #3
36	MCS2	Middle bank Chip Select #2
37	MCS1	Middle bank Chip Select #1
38	MCS0	Middle bank Chip Select #0
39	DEN	Data bus Enable
40	DT/R	Data Transmit or Receive enable
41	INT3/INTA1	Interrupt in #3 / Interrupt Acknowledge #1
42	INT2/INTA0	Interrupt in #2 / Interrupt Acknowledge #0
43	Vcc	+ 5V power in
44	INT1	Interrupt in #1
45	INT0	Interrupt in #0
46	NMI	Non-Maskable Interrupt enable
47	TEST	Test (processor) enable (input)
48	LOCK	Lock (inhibit) processor activity
49	SRDY	System Ready enable (input)

Table 4-1 (cont)
PROCESSOR PIN DESCRIPTIONS

Pin	Name	Description
50	HOLD	Hold processor in present state
51	HLDA	Hold Acknowledged output
52	S0	Processor Status line #0
53	S1	Processor Status line #1
54	S2	Processor Status line #2
55	ARDY	Acknowledged peripherals Ready
56	CLKOUT	CLock output signal
57	RESET	Reset processor (input)
58	X2	Crystal clock input
59	X1	Clock input
60	Vss	Ground
61	ALE/QS1	Address Latch Enable / Cue Status 0
62	RD/QSMD	Read enable / Cue Status of Memory Devices
63	WR/QS1	Write enable / Cue Status 1
64	BHE	Byte High Enable
65	A19/S6	Address line 19 / Status line 6
66	A18/S5	Address line 18 / Status line 5
67	A17/S4	Address line 17 / Status line 4
68	A16/S3	Address line 16 / Status line 3

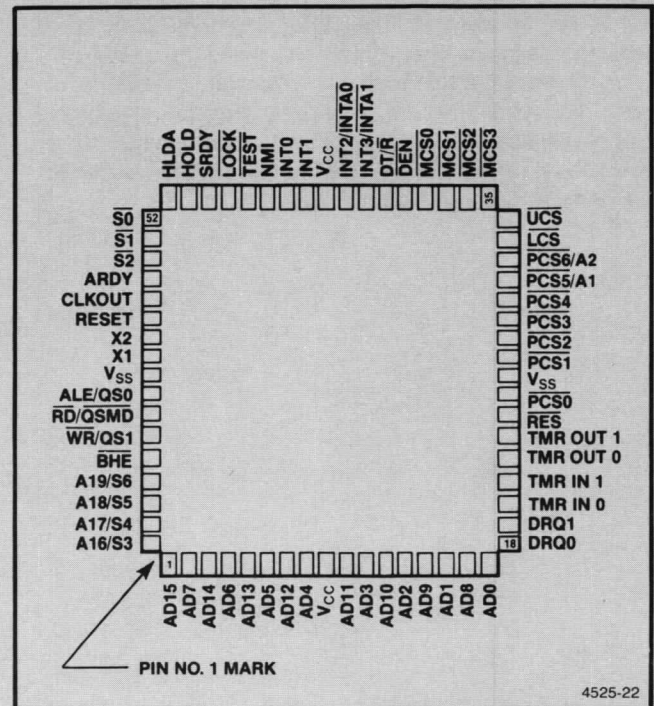


Figure 4-8. Processor Pin Descriptions.

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Execution Unit

The Execution Unit consists of the 16-bit Arithmetic Logic Unit (ALU) and a collection of registers. The registers contain data, instructions, addresses, status and control information. The ALU is the heart of the chip, performing calculations and processing the instructions and data according to the system firmware. The manufacturer's data sheet provides detailed information about processing power and the 80186 instruction set. Such information is related more to design than maintenance and is not included in this manual.

Registers. The Registers are divided into the following categories:

- General registers
- Segment registers
- Base and index registers
- Status and control registers

The general registers store arithmetic and logical operands. The segment registers store locations (memory "segments") in processor memory. Such segments are immediately accessible for code, stack, and data. The base and index registers contain base addresses and indexes to particular locations within a segment. The status and control registers contain instruction pointers and the status word. The purpose of the status word is covered following the Memory Segments discussion.

Memory Segments. Processor memory is organized into pieces of memory called segments. Segmented memory is a means of dividing memory into functional units thus simplifying programming. Each segment is a linear unbroken memory space. Segment size is variable and may be as large as 64K.

Memory is accessed by a two-part address: a pointer, and an offset. The pointer is a 16-bit base address for a segment. The base address is contained in one of four registers (code, data, stack, extra). The actual physical address is obtained by shifting the base address left by four bits, and then adding the 16-bit offset. This results in a 20-bit physical address for accessing the 1 Mbyte addressable space.

Status Word. The processor records certain results of logical and arithmetic operations in the "status word" register. This word controls other aspects of processor operation. The status word is 16 bits wide and resides at location F002(X) immediately following the RESET condition. The manufacturer's data sheet contains detailed status bit definitions.

Clock Generator

This circuit block provides the timing for the processor and peripheral circuitry. Refer to the external clock circuit block description for more details.

Programmable Interrupt Controller

This block within the processor prioritizes and services the many interrupts received by the processor. Some interrupts are generated by external circuitry, while other (internal) interrupts come from blocks in the processor itself. This circuit block ranks these requests for service by the CPU. The internal interrupt sources (Timers and DMA channels) may either be enabled/disabled by their own control registers or by mask bits in the interrupt controller. The Interrupt controller has its own control registers that set its operating modes. Figure 4-9 depicts the logical layout of the interrupt controller.

The timing and interrupt signals enter the Interrupt Priority Resolver. Four interrupt inputs (INT1 to INT3 and NMI) enter the Resolver and the output goes to the "Interrupt" input of

the CPU. A bank of control registers connects to the internal address/data bus and provides firmware information to the Priority Resolver. Several housekeeping registers (right side of diagram) store: interrupt requests, masks, and status. These registers pass information back and forth to the resolver as needed. The Interrupt Status register also makes interrupt status available to the rest of the processor via its internal bus. The block labeled Vector Generation Logic creates address vectors so interrupts trigger the proper service routine.

The functions of the interrupt controller are controlled by programming in firmware. One item of interest is that the interrupt routines may be nested. This means that it is possible for an interrupt routine to be interrupted by another higher priority interrupt routine.

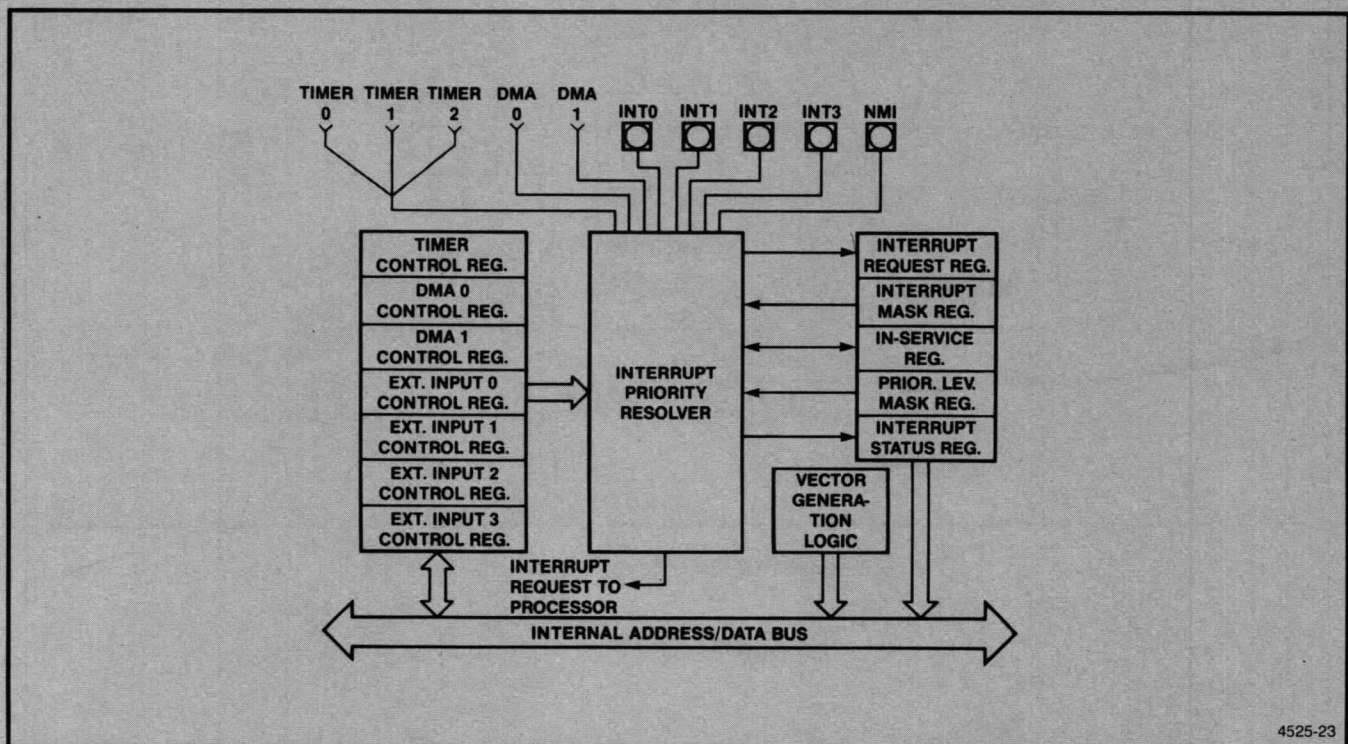


Figure 4-9. Programmable Interrupt Controller Block Diagram.

Programmable Timers

The processor includes three, 16-bit, programmable timers. See Figure 4-10.

Timer 0 rings the bell. Timers 1 and 2 detect when and how long a keyboard key is held down. A 500 msec initial delay occurs before key repeats take effect. Then, the character/key is repeated every 100 msec while the key is pressed. A fast repeat (10 msec) takes effect when the Shift key is used with key repeat. The timer circuits determine all these repeat times.

Programmable DMA

The processor's Programmable DMA block allows fast DMA data transfers between the following system areas:

- Memory to I/O
- Memory to memory
- I/O to I/O

DMA requests come either from the CPU (via the Internal Bus), or come from the Communications Interface block (via the external DRQ0 and DRQ1 input lines).

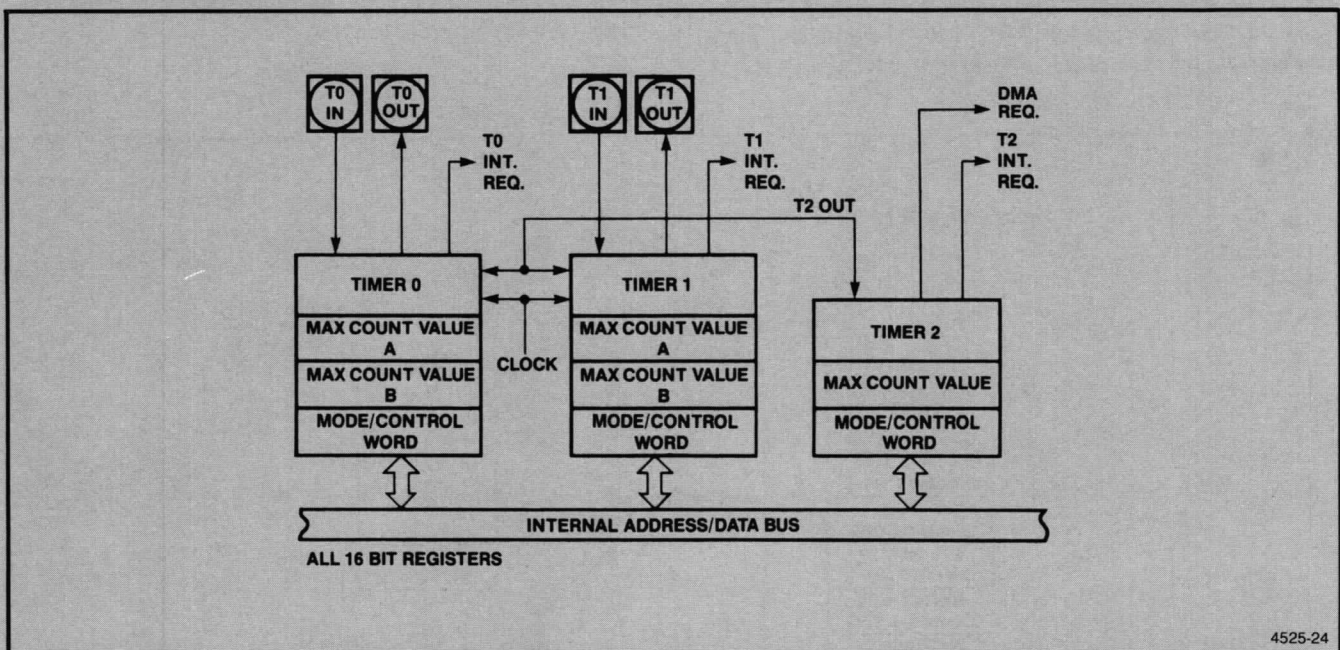


Figure 4-10. Timer Block Diagram.

The DMA allows data transfers in either bytes or words, and to or from even or odd addresses. This circuit block provides two DMA channels, and each contains a 20-bit source pointer and a 20-bit destination pointer. Each DMA data transfer occupies two bus cycles: one to fetch data, and the other to store it. Figure 4-11 shows the functional parts within this DMA circuit block.

Chip Select/Ready Generation Block

This block allows the firmware to select several peripherals and memory sections via the processor's chip select lines. This block also works with the Bus Interface block to generate the READY signals (via firmware and the Internal Bus). The chip select lines are used as follows:

- PCS0 – controls/selects the Keyboard/Comm I/F chip
- PCS1 – selects the VIDIO (video input/output) on the Display Control board

- PCS2 – selects the Printer/Copier I/F chip
- PCS4 – selects the NMI (non-maskable interrupt) Enable Flip-Flop
- PCS5 – disables NMI and turns off system reset
- PCS6 – performs system reset.

This block also generates the Memory Chip Select lines: MCS0 –MCS2, LCS, and UCS. The MCS0 – MCS3 lines operate in conjunction with the UCS (Upper Chip Select) to control four areas of program memory; see Figure 4-3, again. The LCS line selects the following areas in lower memory:

- EEPROM
- 32K System Memory
- Dialog RAM (on Display Control board).

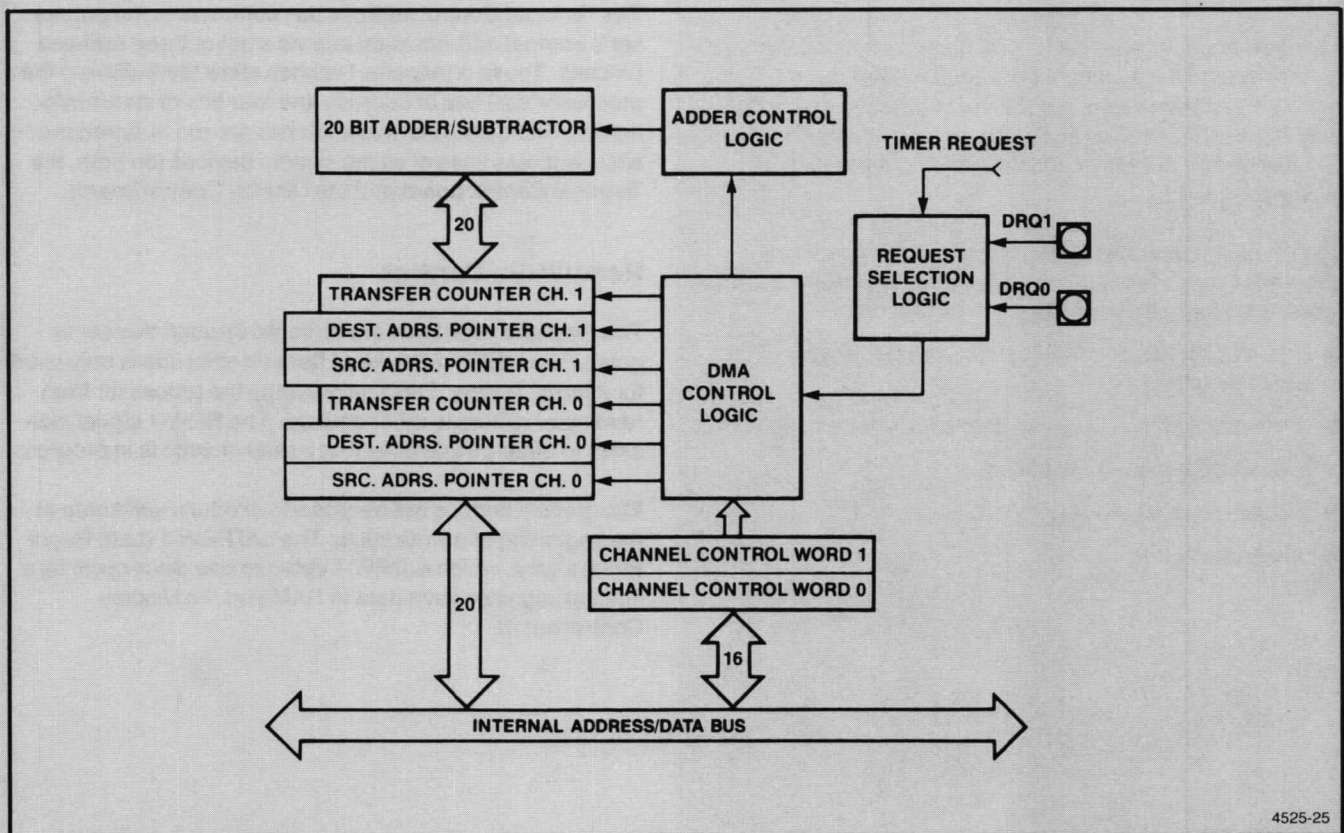


Figure 4-11. DMA Unit Block Diagram.

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Bus Interface Unit

This part of the chip operates between the internal bus (inside the chip) and the Terminal Control board bus (outside the chip). The functions of this block come under four general categories:

- Memory/peripheral control
- Transceiver control
- Internal bus acquisition and arbitration
- Internal bus controller and reset.

The RD, WR, and ALE lines control the bus and strobe data between memory and the microprocessor. The ALE (address latch enable) line strobes the address latches on the multiplexed address/data lines.

The transceiver control subblock drives the DT/R and DEN control lines. These lines control the data bus transceivers in the Processor Interface portion of the Display Control board.

The Hold and Hold-acknowledged features of the processor are not used. These pinouts go to the Display Control-Terminal Control ribbon cable, but are not connected on the Display Control board. Therefore, the processor's internal bus is not acquired by outside masters and no arbitration circuitry is required.

The remaining function of this block is to handle house-keeping chores required following a bus reset. After an RES input, this block performs the following actions:

- drives DEN, RD, and WR high for one clock cycle, after which they float
- drives S0-S2 high (passive), then allows them to float
- drives LOCK high, then it floats
- tristates AD0-15, AD16-19, BHE, and DT/R
- drives HLDA low.

NOTE

The remaining processor circuit block headings describe the blocks located OUTSIDE the processor chip.

Clock Circuitry

The 14.7456 Mhz crystal oscillator on this board clocks the processor. The processor's X1 (clock) input sends this clock signal to an internal oscillator that makes the processor clock waveform. A divide-by-two counter derives the signal for the processor's own use. A CLKOUT signal, from the processor, makes this clock signal available for peripheral circuits. The Clock circuitry also amplifies the crystal clock signal, TERMCLK-1, to the non-TTL level required by the processor.

Address Latches

The Terminal Control address bus connects to the processor's internal address/data bus via a set of three Address Latches. These transparent latches store (demultiplex) the processor's 20 bits of address and four bits of status information. The outputs of these latches are the buffered processor address lines of all the system devices (on both, the Terminal Control board and the Display Control board).

Read/Write Control

The read and write lines are buffered through this set of gates. The MDEN-1 (Memory Data Enable) line is only used for internal testing. This line prevents the processor from reading or writing to other devices. The BRW-1 signal indicates to other bus devices that a read or write is in progress.

The processor does not necessarily produce valid data at the beginning of a write cycle. The LATERW-1 (Late Read/Write) signal, which is BRW-1 delayed one clock cycle by a flip-flop, signifies valid data to RAMs on the Display Control board.

Reset Block

The processor's input RESET line uses a switch and typical RC-type reset circuit. The diode discharges the capacitor when power is turned off; this circuit assures a proper processor reset when power is turned on again.

RESET Control

The processor's reset output line is controlled by the programmable select lines PCS5 and PCS6. These lines disable NMI and turn off the system reset via a set of cross-coupled AND gates.

NMI Logic

This set of logic controls the Non-Maskable Interrupt control line. The AND-OR gate pair, in the NMI line, allows this line to work for both testing, and actual system use. A test pin on the test connector controls the NMI line. Also, the Keyboard/Communications interface (a type-2681 DUART) requests NMI if the host sends a character while the NMI-Enable Flip-flop is enabled.

Ready Logic

A pair of AND-OR gates, in the ARDY (ready) line, combines the ready signals from various inputs. READYOR comes from the Test Connector and forces the processor ready regardless of the states of the other ready signals. RAMRDY (RAM ready), DISPRDY (display ready), and RDYAND (another test connector signal) are ANDed together, then ORed with RDYOR, to drive the processor's ARDY input.

Other Circuitry

Other assorted gates, in the the input control lines to the processor, function as follows. The inverter in the HOLD line allows this line to be used by an external device; otherwise, the line would have to be grounded.

System Address Decode

This circuit block accepts address lines from the processor and decodes them into memory/peripheral selector lines. This block consists of a "custom gate array" chip and several discrete gates. The gate array's address inputs are A14 through A19 (except A17). This chip also accepts several status and control lines from the processor: ALE/QS0, LCS, BHE, A0, BWR, LATERW, and LS2. The selector outputs are listed in Table 4-2.

Table 4-2

ADDRESS SELECTOR OUTPUTS

	Signal Name	Selected Area
Memory Addresses	RAMCS0-0	Memory; 0 - 3FFF (EVEN)
	RAMCS1-0	Memory; 0 - 3FFF (ODD)
	RAMCS2-0	Memory; 4000 - 7FFF (EVEN)
	RAMCS3-0	Memory; 4000 - 7FFF (ODD)
	2817CS-0	Erasable ROM; 10000 - 17FFF
	ALPHACS-0	Alpha Memory; 18000 - 1FFFF
	GRAPHCS-0	Graphics Memory; 40000 - 80000
Byte&Word Write Enables	TESTCS-0	Memory test area; 20000 - 40000
	HIWR-0	Late High Write decode
	LOWR-0	Late Low Write decode

NON-VOLATILE MEMORY

The Non-Volatile Memory block consists of a 2K x 8-bit EEPROM memory chip. This chip is an Electrically Erasable Programmable ROM. (It replaces a CMOS RAM with battery backup, thus eliminating a battery and increasing reliability). The EEPROM is used to store non-volatile parameters such as: baud rates, prompt mode strings, and definitions for keys.

The inputs and outputs of the EEPROM block are: address, data, and control. See Figure 4-12, a functional block diagram. The address inputs connect to the board address bus lines: A0 through A10. The data inputs and outputs connect to the Processor Data Bus lines, AD0 to AD7. The control lines are connected to:

- 2817CS – chip select
- BRD – read command (buffered)
- LOWR – write command (to low memory)
- 21 Volts – required to read or write to the chip.

The chip's status output, which is labeled RDY/BUSY, becomes the signal: 2817RDY. The processor checks this line, prior to reading or writing, to be assured that a previous write cycle is not still in progress.

Because the chip has limited write cycle life, the system writes to the 2817 only as necessary. Before writing a parameter into the chip, it checks to see if the value has actually changed from the already stored value. If no change is detected, then no write operation occurs.

The EEPROM timing and wait states are set for a relatively slow operating cycle. Since the EEPROM is only read at power up or when parameters are updated, access can be slower. Consequently, the chip operates on a 450 nsec cycle. The WAIT states are determined by the status of the READY line.

The following are some constraints regarding wait states:

- To read the chip, two 80186 wait states are required.
- To write to the chip, no wait states are required.
- Other devices, independent of the processor, must always check BUSY status, if they do not know the previous activity of the processor.

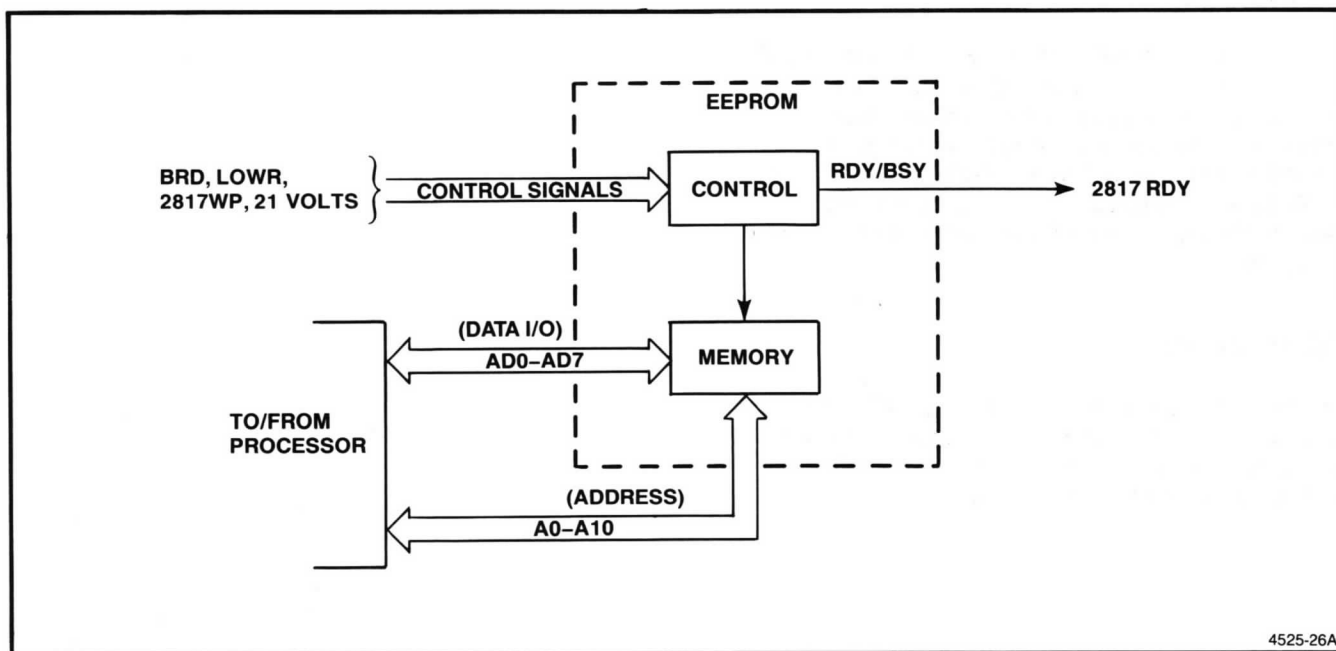


Figure 4-12. Non-Volatile Memory Block Diagram.

PROGRAM MEMORY BLOCK

The Program Memory block contains the system firmware. The design will accommodate several types of EPROM chips but the 27128 and 27256 are the most likely to be used.

Figure 4-13 shows the arrangement of the eight EPROMs that comprise this circuit block. The odd and even addresses are assigned to alternate EPROMs in four pairs. The lower three pairs are enabled by processor select lines: MCS1, MCS2, and MCS3. The last pair of EPROMs is selected by the processor select line, UCS. At power-up the UCS signal is the only chip select that is active. This automatically selects the upper bank, which contains the power-up codes. This also assures that all other ROMs are inactive until power-up is completed and the system is fully initialized.

When 27128 and 27256 EPROMs are used, the bank size is 64K words. System firmware (rather than hardware) manages the addressing of EPROMs and allocation of bank sizes (in processor address space). Consequently, straps are not needed to change address boundaries or chip types.

The processor clock sets the length of time for a read and write cycle. The 14.7456 MHz clock results in a clock period of 135 nsec. The chip select access time requirement is 3 clock periods (405 nsec). The address access time for these chips is 314 nsec, and the read enable access time is 143 nsec.

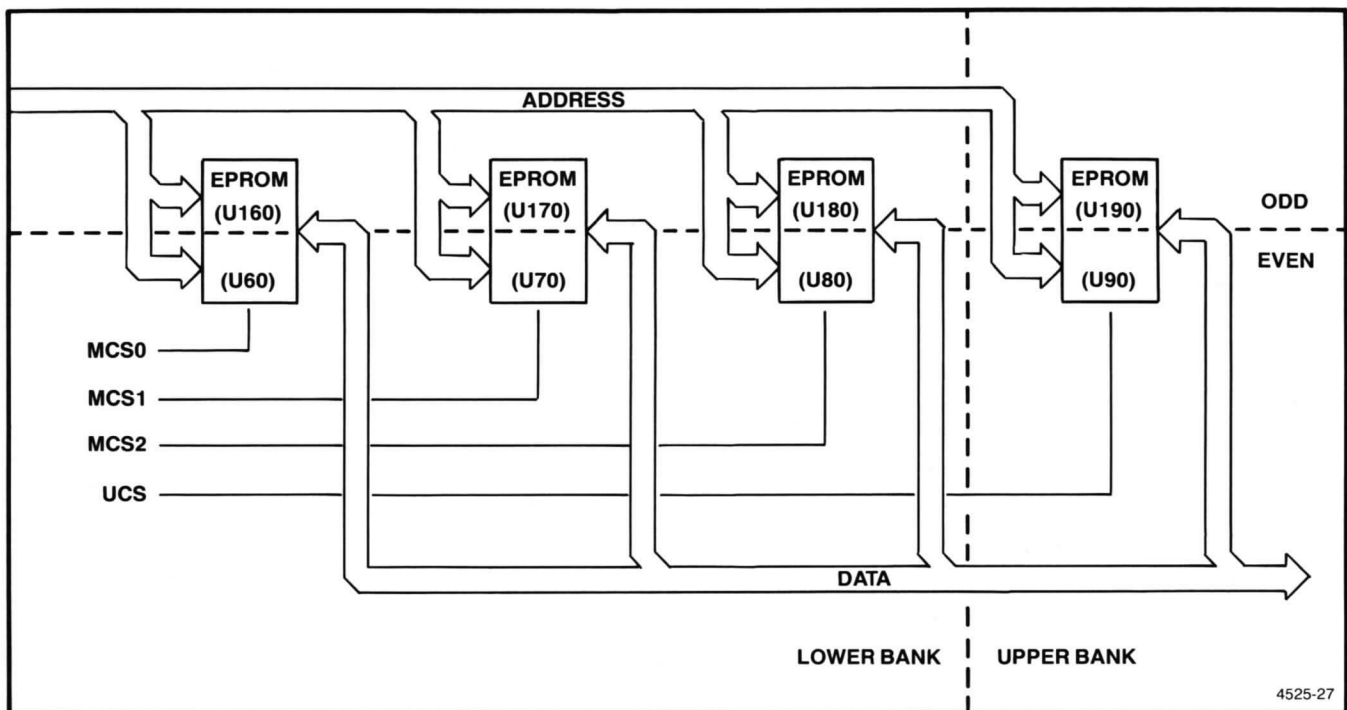


Figure 4-13. Program Memory Block Diagram.

SYSTEM RAM BLOCK

The RAM block consists of four 8K x 8 bit RAM chips. The 2186 RAM is designed to operate with the 80186 and is the principal component in this circuit block. This RAM stores firmware related data, user-defined key definitions, etc. Figure 4-14 shows the functional arrangement of these RAMs and their signal lines. The four RAMs are divided into two pairs. Each pair is divided between odd and even addresses. One pair is "low" RAM (addresses 0000 – 3FFF), while the other is "high" RAM (addresses 4000 – 7FFF). Notice that the "chip selects" are separate for each RAM.

The 2186 is called a "pseudo static" RAM chip, because it provides its own refresh for the dynamic cells. This self-refreshing feature is desirable, but could result in unstable data if an access were to occur while such a refresh were in progress. To avoid this problem, the RAM "ready" lines go false during static refresh, causing the system to wait until the refresh cycle is complete. The 510 ohm pull-up resistor on the READY line provides current for the open-drain output.

There are no straps associated with these RAMs because their parameters are fixed.

The Display List (segment) Memory is located on the RAM3 board for the 256k bytes of RAM (address 20000 – 3FFFF and C0000 – DFFFF).

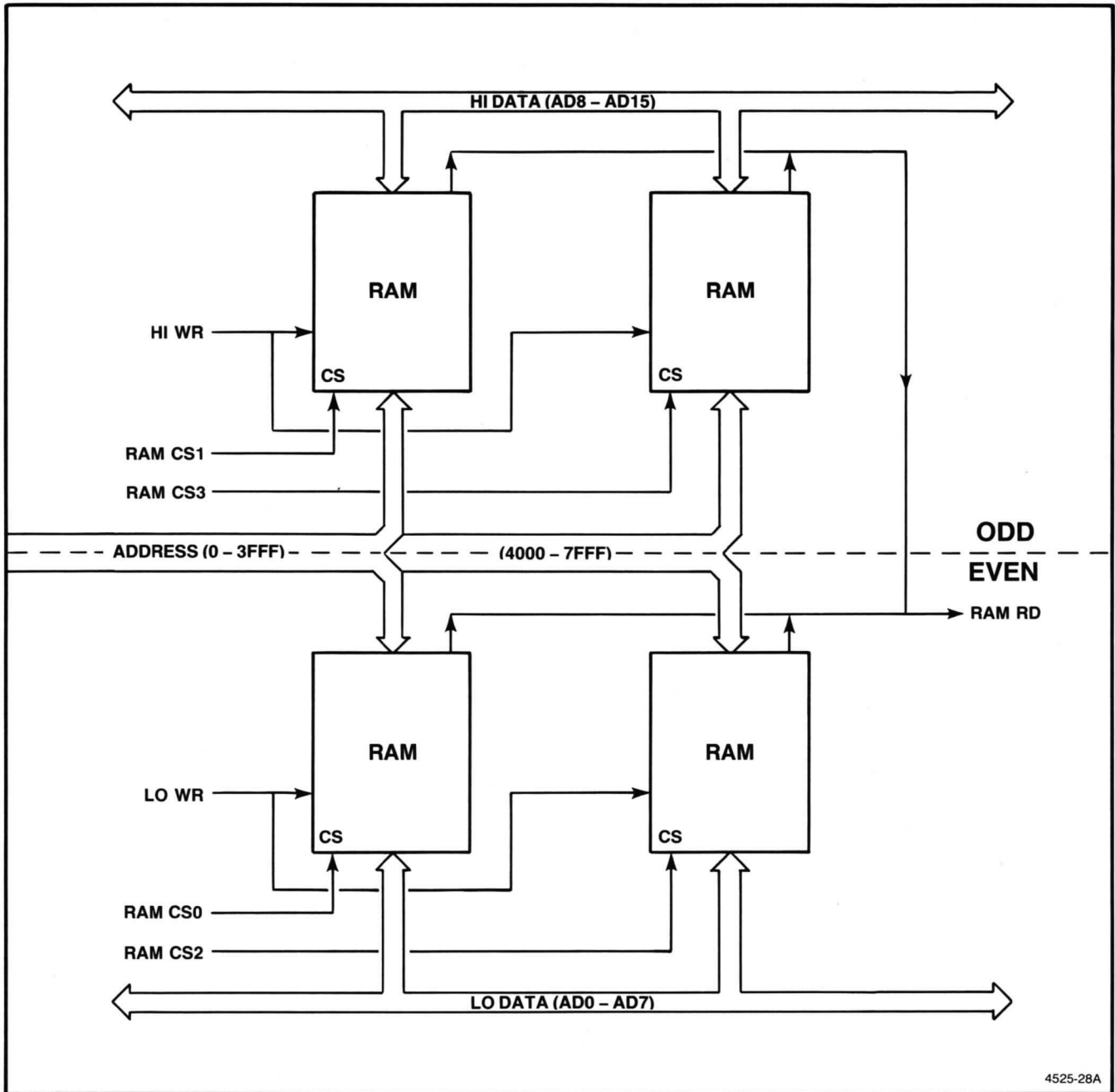


Figure 4-14. RAMs Block Diagram.

KEYBOARD AND COMMUNICATIONS PORT BLOCKS

The Keyboard-to-Processor Interface and the Host Communications-to-Processor Interface are both handled by a single two-channel chip (a DUART). The basic functional arrangement of these circuits is shown in Figure 4-15.

Notice that both channels connect to the Processor Data Bus and Address Bus. Also the processor may receive DMA requests, or non-maskable interrupts, directly from the Host Communications Port via the RCV/RDY line.

DUART Transceiver Chip

The DUART (Dual Asynchronous Receiver/Transmitter) is a 2681 chip. Figure 4-16 is the generalized block diagram for this DUART chip. In this diagram the two channels are called channels "A" and "B." Channel A shows its func-

tional details. Since channel B is identical in hardware composition to channel A, the diagram omits the detail in Channel B. Channel A functions as the Keyboard I/F, and Channel B is the Host Port I/F for the terminal.

The 2681 possesses the following features:

- Both channels are full-duplex asynchronous
- Quadruple buffered receiver data registers
- Programmable data format
- Programmable baud rates for each channel

The chip contains a multi-purpose, 7-line input port, and a multi-purpose 8-bit output port. The chip also contains a timing block that either provides timing for the chip, or accepts external timing (as from the processor). An Interrupt Control and an Operation Control block manage the read, write, interrupts, and address decoding functions.

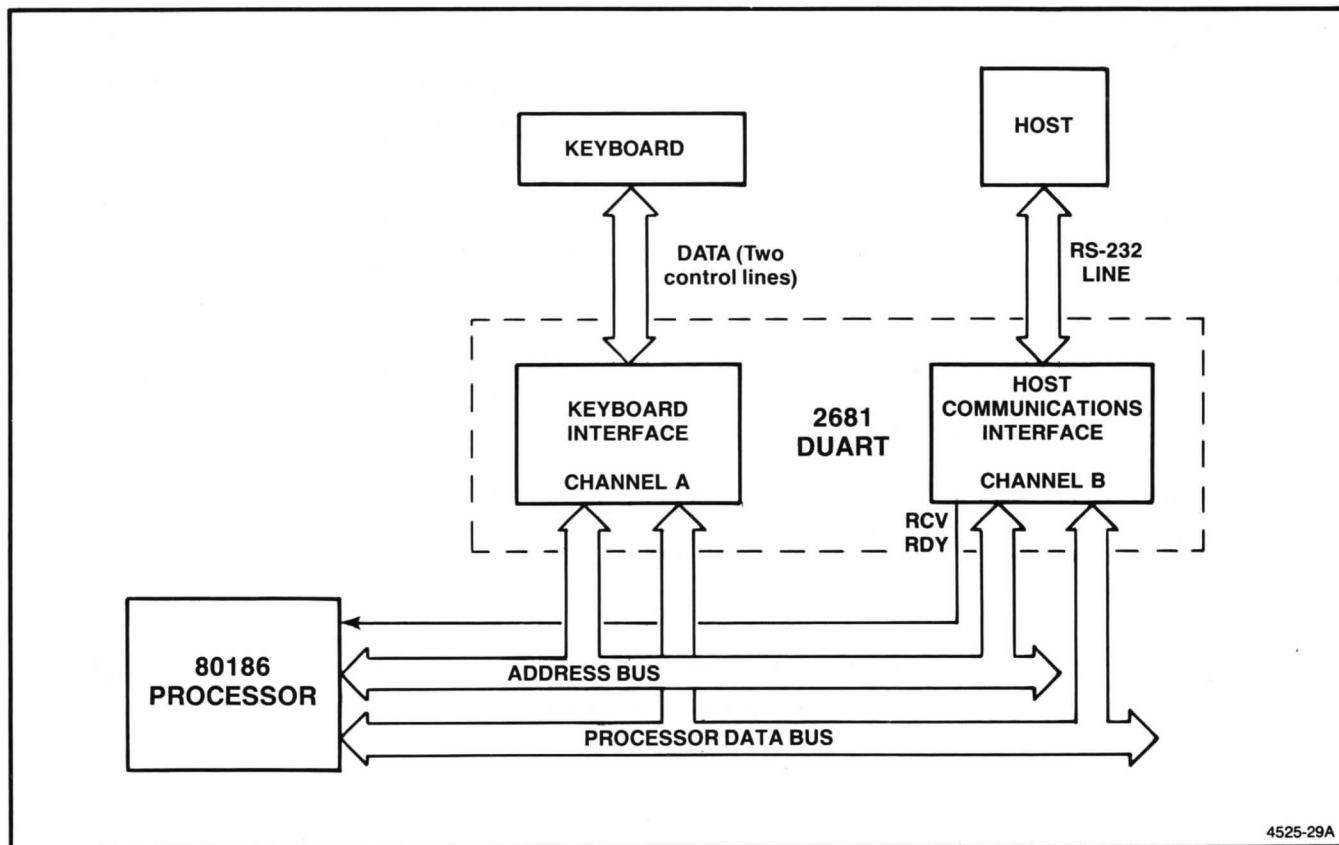
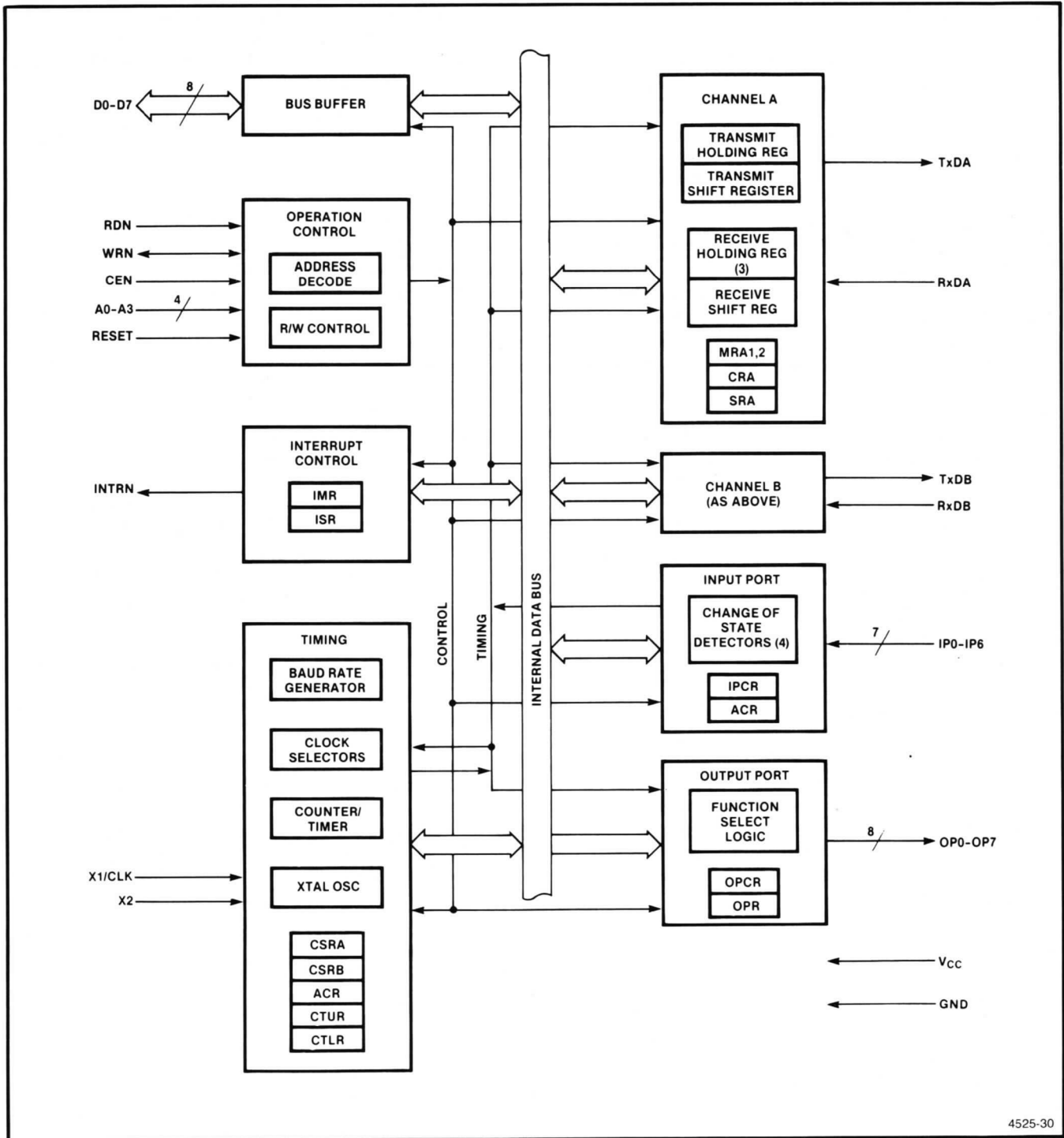


Figure 4-15. Keyboard and Host Comm I/F Blocks.



4525-30

Figure 4-16. DUART General Block Diagram.

Keyboard Interface

This circuitry provides the data input, data output, reset, and power supply to the keyboard. This description covers both the external circuitry and the internal DUART functions. This circuitry is described first as it functions when the keyboard generates data; next, the same circuits are described during information flow to the keyboard.

As a key is pressed, data flows from the keyboard toward the RXDA (Receive data, channel A) input of the DUART. This data path flows through two intermediate circuit blocks shown in Figure 4-17. The first circuit is a set of diodes and resistors that function as a level shifter; this circuitry also provides termination for the keyboard driver circuit. The second circuit is called the clamping gate; it prevents the keyboard from overrunning the 2681.

The DUART's OP4 output makes the RXRDA-0 (receive ready channel A) signal. When the DUART receives a character from the keyboard, it asserts this line, which activates the clamping gate. The clamping gate holds KBRDATA-1 low, which is monitored by the keyboard. The keyboard will not send any more characters to the DUART until this line goes high. The clamping gate also forces the DUART's RXDA line inactive, so the DUART cannot interpret the clamp as a character. After the processor has read the data out of the DUART, the DUART negates the RXDYA line; this releases the clamp, which alerts the keyboard that it is again free to send. This implements the keyboard-to-processor handshake protocol.

Before the processor sends a command to the keyboard, it first reads the DUART's IP4 status line. If the keyboard is not ready to receive a command, it clamps KBTDATA-1 low; this makes IP4 go high. While this condition is true, the processor waits to send the next command until the keyboard releases KBTDATA-1. This implements the processor-to-keyboard handshake protocol.

During Self Test, the keyboard is held in a reset condition (via OP3 of the DUART) while the local interface circuitry is being tested. The KBTEST-1 signal enables the 74LS38 (U275C); this causes the transmitted data on KBRDATA-1 to loop back into KBRDATA-1, where it is received by the DUART as if it had come from the keyboard. This allows both the input and the output data paths to be verified by Self Test.

The 14.7456 MHz DISPCLK signal clocks the DUART. The system clock passes through a pair of flip-flops configured as a divide-by-four counter, which provides the 3.6864 MHz clock required by the DUART.

The general purpose output, OP3, is programmable to reset the Keyboard.

Host Communications Interface

Channel B of the 2681 DUART is the host communications interface. The external circuitry to the chip is minimal, consisting of buffers and a combinational logic chip for the DTR signal. Table 4-3 relates the RS-232 connector pin numbers to their corresponding DUART pin numbers. The table also gives both RS-232 names and DUART names.

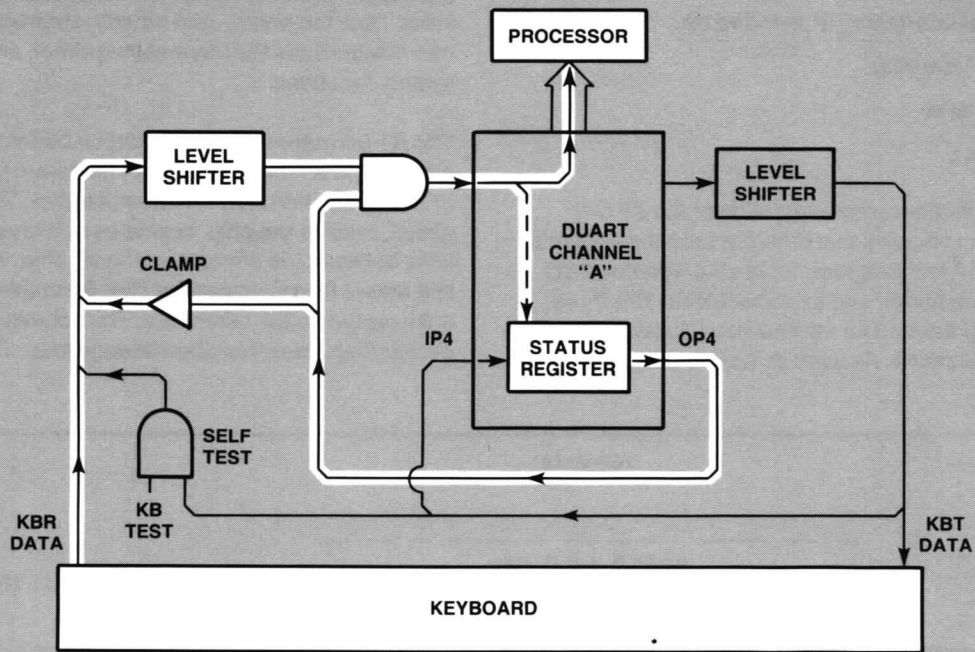
The OP7 output from the DUART is used with Self Test to light an LED for certain error codes.

The DTR (Data Terminal Ready) condition is derived from the logic states of three DUART output lines. The first line, OP5 is the same as the RXDB (buffered receive data available) input to the DUART. The states of the other two lines, OP2 and OP6, are determined internally, by programming of the DUART.

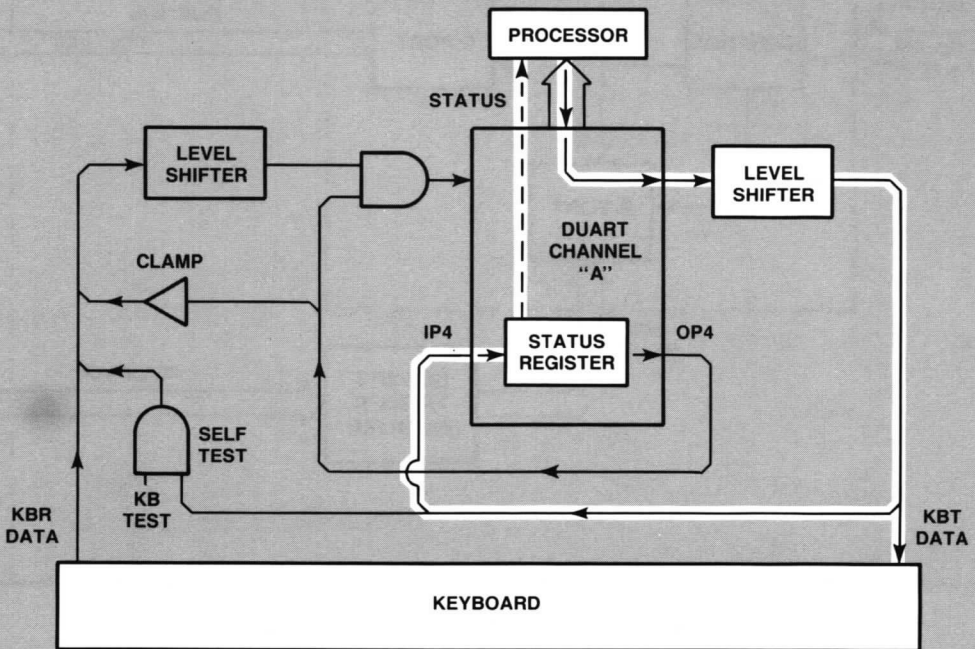
The timing and other general DUART functions were covered under the Keyboard Interface heading.

Table 4-3
HOST PORT INTERFACE PIN NUMBERS

RS-232 Connector			DUART Connector	
Pin	Name	(to/from Host)	Pin	Name
1	Chassis	Ground	11	TXDB
2	TDATA	(to)	10	RXDB
3	RDATA	(from)	12	OP1
4	RTS	(to)	4	IP1
5	CTS	(from)	36	IP2
6	DSR	(from)		
7	Signal	Ground	7	IP0
8	DCD	(from)	W493	(pin 29 OP0)
11	SRTS(A)	(to)	2	IP3
12	SDCD	(from)	38	IP5
15	TC	(from)	37	IP6
17	RC	(from)	W493	(pin 29 OP0)
19	SRTS(C)	(to)	14	OP5
20	DTR	(to)	26	OP6 > combined
			28	OP2



A. KEYBOARD INTERFACE, DURING RECEIVE CYCLE (FROM KEYBOARD).



B. KEYBOARD INTERFACE, DURING TRANSMIT CYCLE (TO KEYBOARD).

4889-29

Figure 4-17. Keyboard Interface.

HARD-COPY/PRINTER INTERFACE

Terminal-to-printer interfacing is provided by:

- an 8255A interface chip,
- a 10-bit buffer, and
- a schmitt trigger.

Figure 4-18 is a functional representation of the I/F chip and the supporting circuitry that together form the Printer I/F block. The 8255A is a programmable chip with three I/O ports, an input data buffer, and a control block. The three ports may be programmed for various uses depending on the particular application. As used in this circuitry, the A

Port functions as a data output port (supplying the data lines to the printer). The B Port functions as a feedback input, from the printer, and other system status. The C Port handles the lines that control the printer, and other system functions.

The A Port output passes through a buffer on its way to the printer's data input connector. The data input, to the 8255A I/F chip, is buffered by an internal buffer. The schmitt trigger circuit, outside the chip, regulates and inverts the feedback lines between the printer and the I/F chip. The acknowledge line enters Port C, instead of Port B, so this feedback line is not inverted as the others are. The schmitt trigger still clamps/regulates this acknowledge line.

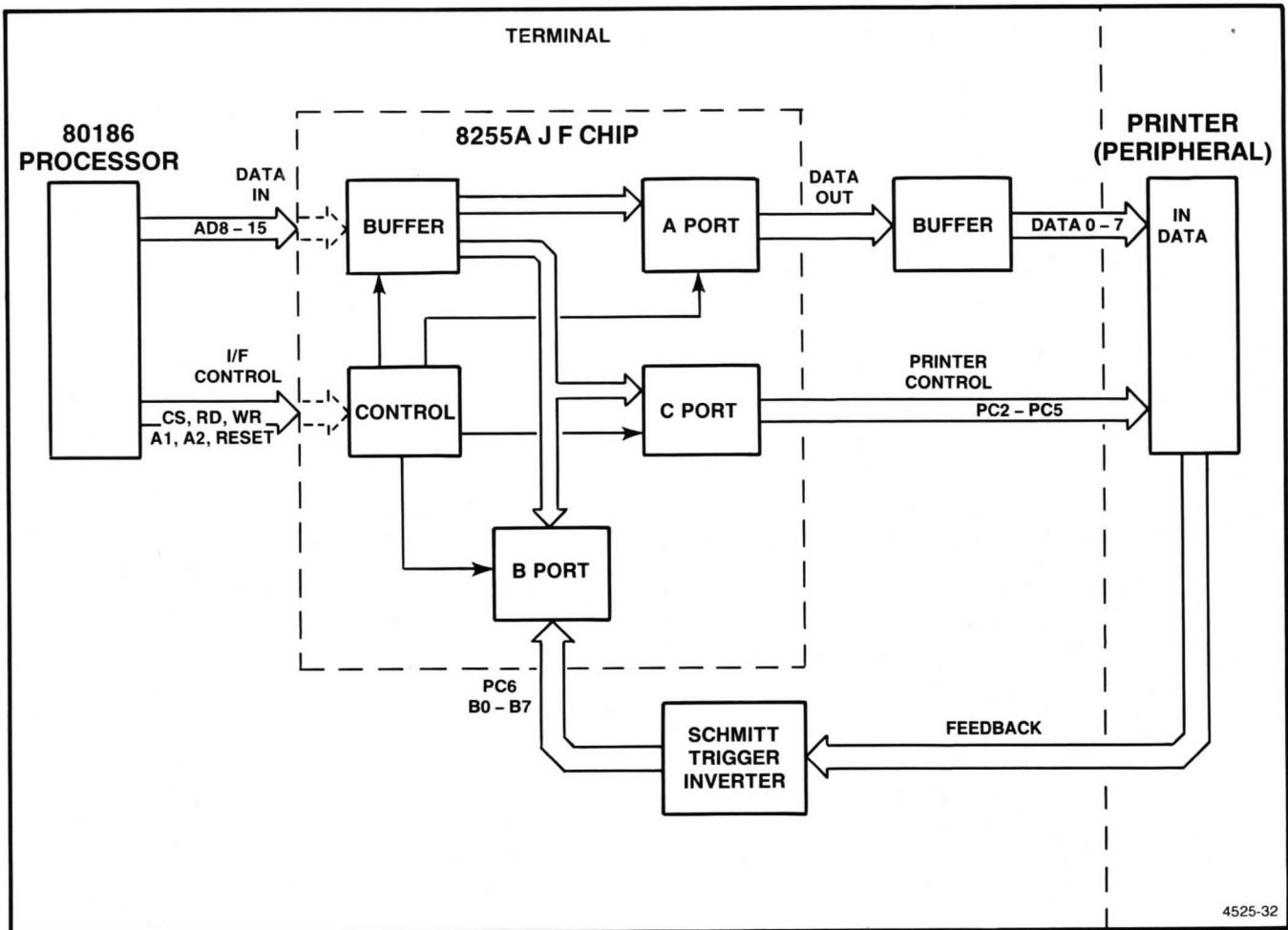


Figure 4-18. Printer Interface to Block Diagram.

2-PORT PERIPHERAL INTERFACE

The terminal has two RS-232 ports, through which it communicates with RS-232 peripheral devices such as plotters or graphic input tablets. These two ports, and their associated firmware, are known as the 2PPI, 2-Port Peripheral Interface. The 2PPI uses the 2681 DUART (Dual Asynchronous Receiver/Transmitter) chip, shown in Figure 4-16. The 2681 contains a multipurpose, 7-line input port, and a multipurpose 8-bit output port. The chip also contains a timing block that either provides timing for the chip, or accepts external timing from the processor. An Interrupt Control and an Operation Control block manage the read, write, interrupts, and address decoding functions.

There is also an 8-line data buffer to minimize the potential of receiver overrun. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART. Each channel A and B have a Transmit Holding Register, Transmit Shift Register, Receiver Holding Register, Receiver Shift Register, Mode Register, Command Register, and a Select Register.

The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and operational parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled to the CPU.

The 2681 possesses the following features:

- Both channels are full-duplex asynchronous.
- Quadruple buffered receiver data registers.
- Programmable data format.
- Programmable baud rates for each channel.

The DUART, that drives the two RS-232 style connector peripheral ports, is chip-selected by PCS-0. The chip uses address lines A1 through A4. It also connects to data lines AD8 through AD15 (high byte). The write enable is driven by BHE and BWR. The read enable is controlled by BRD. The interrupt output is ORed with PRINTERINT-1 and they drive INT2-1.

The 2PPI has the following RS-232 output pins:

- FGND (pin 1) – frame ground or chassis ground.
- TDATA, transmitted data (pin 2) – The terminal receives data from the peripheral device on this signal line.
- RDATA, received data (pin 3) – The terminal transmits data to the peripheral device on this signal line.
- RTS, request-to-send (pin 4)
- CTS, clear-to-send (pin 5) – Used for DTR/CTS flagging between the terminal and its peripheral device. By asserting CTS, the terminal grants permission for the peripheral device to send data to it.
- DSR, data-set-ready (pin 6)
- SGND, signal ground (pin 7)
- DCD, data-carrier-detect (pin 8)
- DTR, data-terminal-ready (pin 20) – Used for DTS/CTS flagging between the terminal and its peripheral device. By asserting DTR, the peripheral device grants permission for the terminal to send data to it.

BELL CIRCUIT

The “speaker” for this terminal is a small audio transducer that provides the bell tone (prompt). This circuit is driven by one of the timer outputs from the processor. Firmware determines the output frequency, which in most cases will be about 2000 Hz.

KEYBOARD MODULE THEORY

The Keyboard Module is physically separate from the terminal, the only connection is by a cable. The Keyboard Module contains:

- the alphanumeric keyset
- the numeric keypad
- graphics joy-disk
- twelve special-purpose function keys
- a keyboard controller chip
- Two character decoder chips
- Other associated circuitry (drives CAPS LOCK key LED, etc.)

Figure 4-19 depicts the arrangement of the various functional parts of the keyboard module.

The keyboard operates through a full duplex serial interface. The data protocol is 1200 baud asynchronous. The timing and data transmission is typical of a standard DUART, and is a serial data stream as depicted in Figure 4-20.

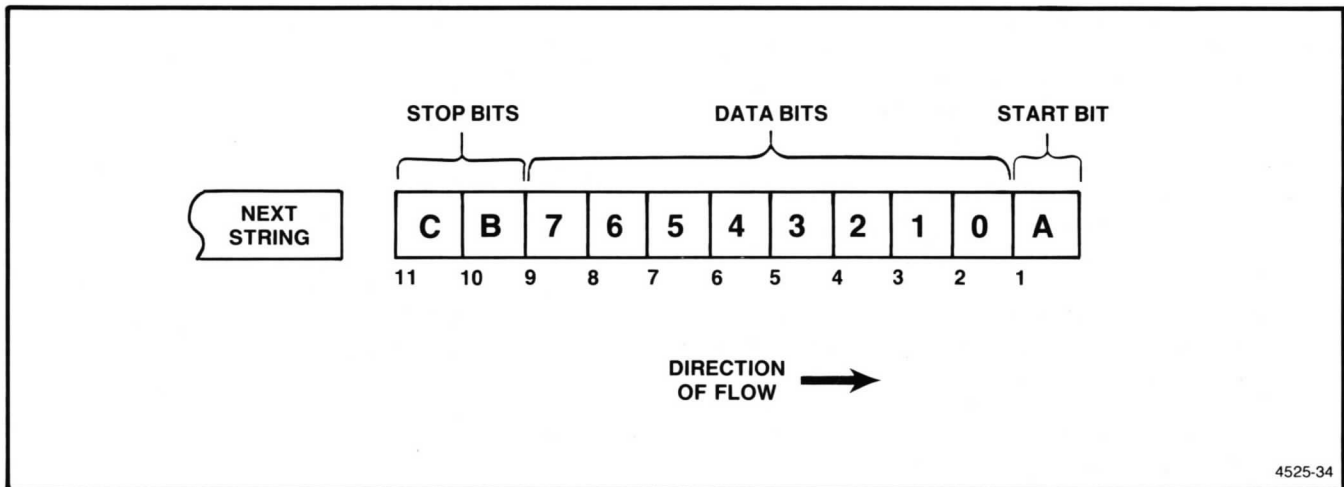


Figure 4-20. Serial Character Format.

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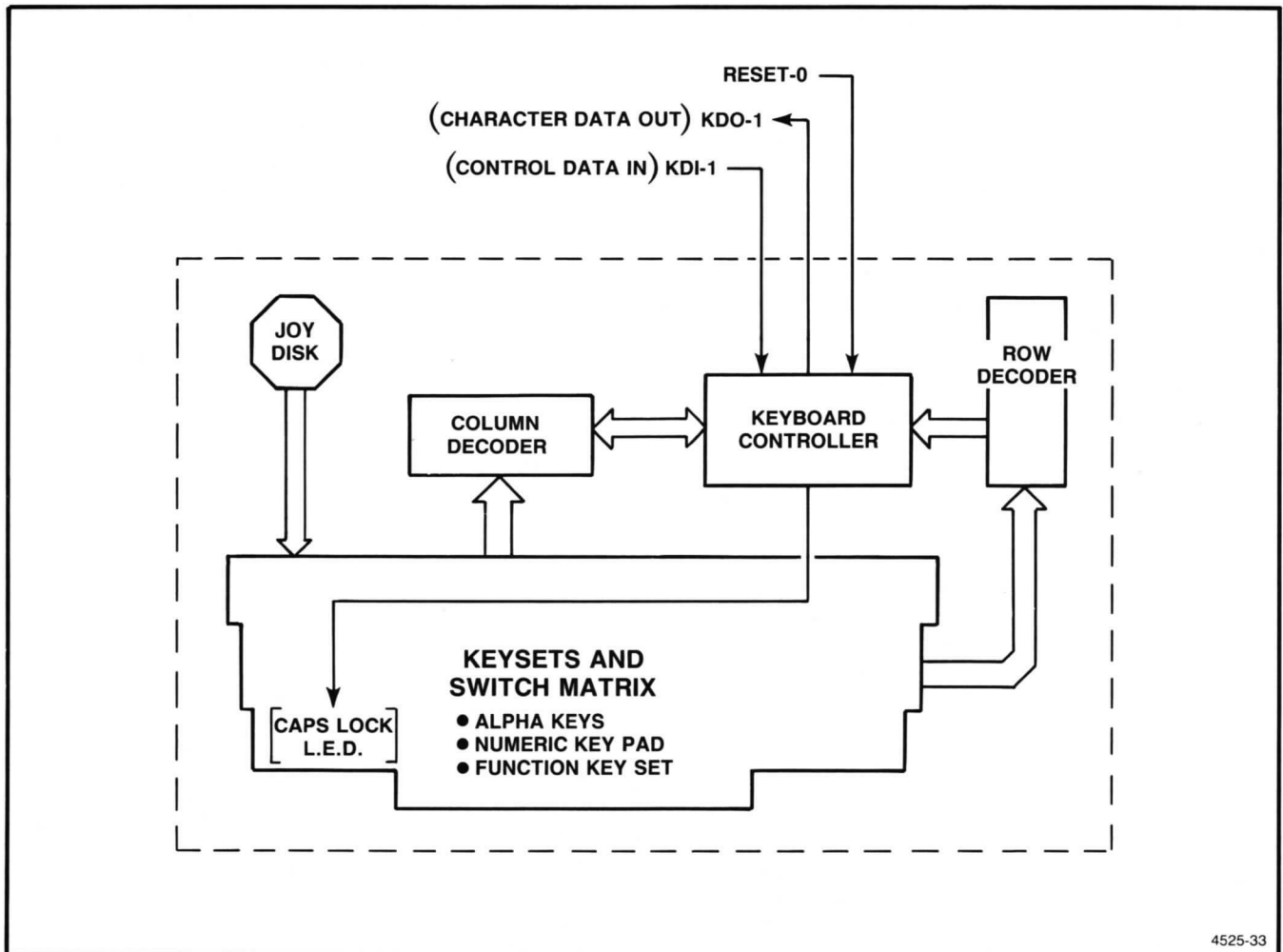


Figure 4-19. Keyboard Module Block Diagram.

KEYBOARD CONTROLLER IC

The keyboard controller is a microprocessor that interfaces between the keyboard and the rest of the terminal. It operates between the Keyboard/Host Comm I/F (on the Terminal Control board), and the key character decoders (on the keyboard module). Figure 4-21 is a functional block diagram of this keyboard controller chip. This controller scans the keys and then debounces the key codes when a key is pressed. The controller places the key characters in an output queue; an 8 byte FIFO. Characters then exit the FIFO over the KDO-1 output line.

The terminal processor manages this controller according to the firmware in the terminal's ROMs. The controller receives control or flagging information (from the processor and Keyboard/Host-Comm I/F) over its KDI-1 and RESET-1 input lines.

The Keyboard Module interface consists of five lines:

- KDI-1 (pin 1) – Keyboard Data In (to the Keyboard Module)
- KDO-1 (pin 2) – Keyboard Data Out (to the main terminal)
- RESET-0 (pin 4) – Reset to the keyboard
- GND (pin 5) – Ground to the keyboard
- + 12V (pin 6) – Vcc power to keyboard

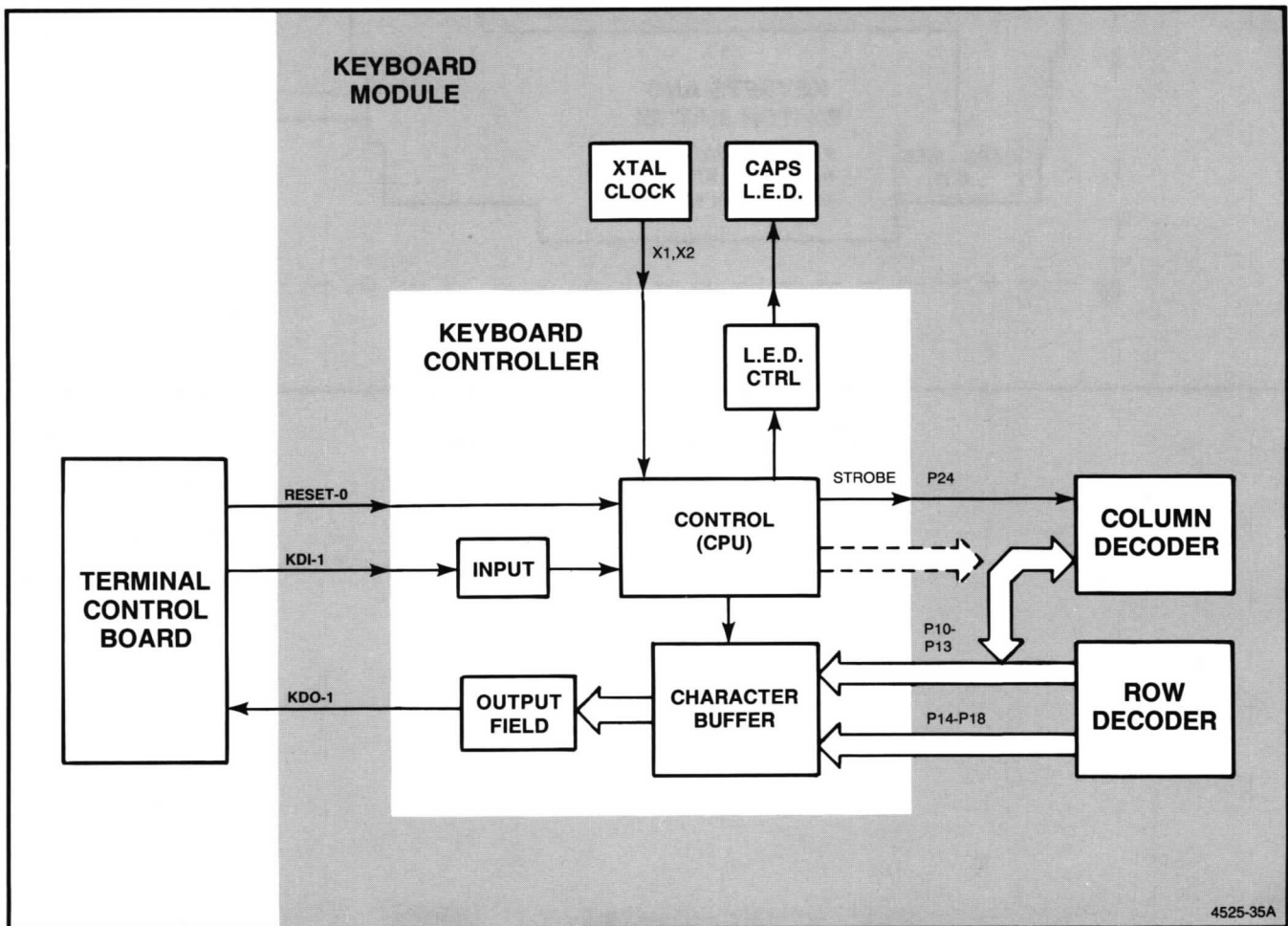


Figure 4-21. Keyboard Controller Block Diagram.

OPERATION OF THE CHARACTER DECODERS AND KEYBOARD

The two keysets (alphanumeric and numeric pad) and the joy disk all consist of key switches that make contact at row-

column intersections in a matrix of circuit runs. When a key is pressed, a connection is formed between one row and one column in the matrix. A unique combination of row and column connections specifies each particular key. See Figure 4-22.

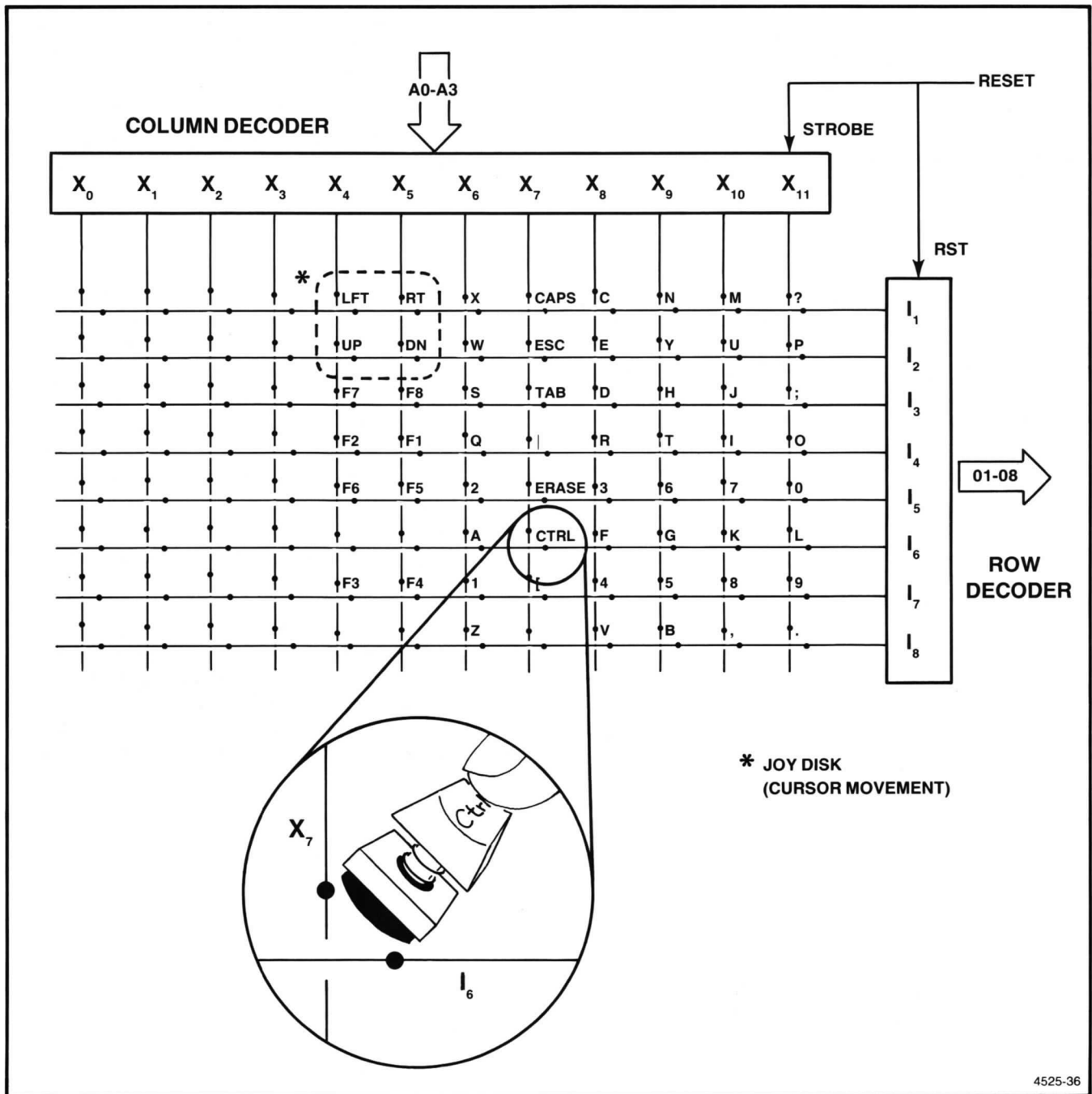


Figure 4-22. Key Matrix and Row/Column Decoders.

CHARACTER GENERATION

Sequence of events for generating a key code:

- 1) The keyboard controller places a strobe on the column decoder; this disables the outputs of the column decoder, but allows the controller to sequentially read the column line states.
- 2) The controller then sequentially reads the status of the column lines in the key matrix (via the column decoder chip).
- 3) When the controller detects a key is pressed, it reads all the row lines (via the Row Decoder) to see which row is also active.
- 4) From the known active row and active column, the controller generates the appropriate character code. This code is actually two codes: a press code, and a release code. The press code falls in the range of 00(Hex) to 55(Hex) and are listed in Appendix D. (Table D-1 lists codes for North American key sets; foreign key codes are also listed in that appendix). The release codes are formed by adding 80(Hex) to each corresponding press-key-code.
- 5) The controller sends a serial character code to the Terminal Control board over the KDO-1 output line. See Figure 4-20, again.

DISPLAY CONTROL BOARD CIRCUIT THEORY

OVERVIEW AND GENERAL DESCRIPTION

The Display Control Board (DCB) generates and stores all of the graphics and dialog (text) data, and it makes control signals for the Display Module. The DCB consists of four major functional units (see Figure 4-23):

- Processor interface (via terminal's system bus).
- Graphics memory and control logic. The graphics memory stores 1024 by 512 pixels, of which 640 horizontal by 480 vertical pixels are displayable. The bit map is four bits deep, allowing sixteen graphics colors to be displayed at once.
- Dialog (alphanumeric) memory and control. This circuitry consists of the dialog memory, its controller chip, and other control logic. The dialog memory is list driven and provides the text on the dialog part of the display screen.
- Pixel Priority Control Logic and Color Map. The pixel priority logic places the cursors, graphics, and dialog text on the proper layers on the display. The Color Map is programmable by the user and allows any dialog/graphics/graphic-cursor values to be reprogrammed to any one of the available colors.
- Timing, syncs, and clocks. This circuitry controls the timing of the display system and synchronizes the various circuit blocks and the display module to itself.

Figure 4-24 is a detailed block diagram of the DCB. The block names correspond to the names on the schematics (Section 11), except where a block is divided into even smaller functional blocks. The Graphics Memory Control block and Graphics Memory (Planes 0, 1, 2, 3) are shown as dotted boxes and are divided into smaller functional units.

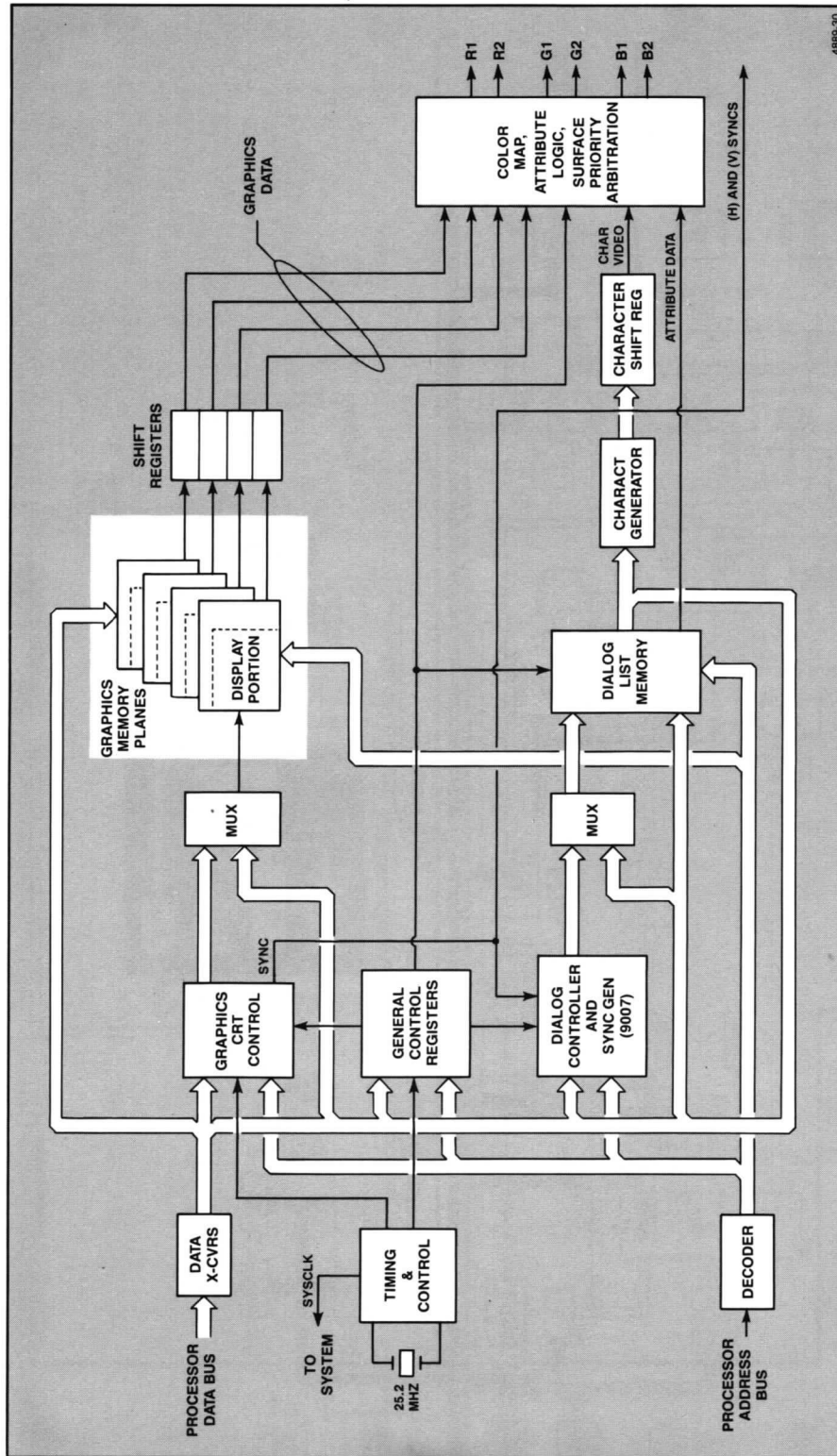


Figure 4-23. Display Control Board Simplified Block Diagram.

THEORY OF OPERATION
 DISPLAY CONTROL BOARD

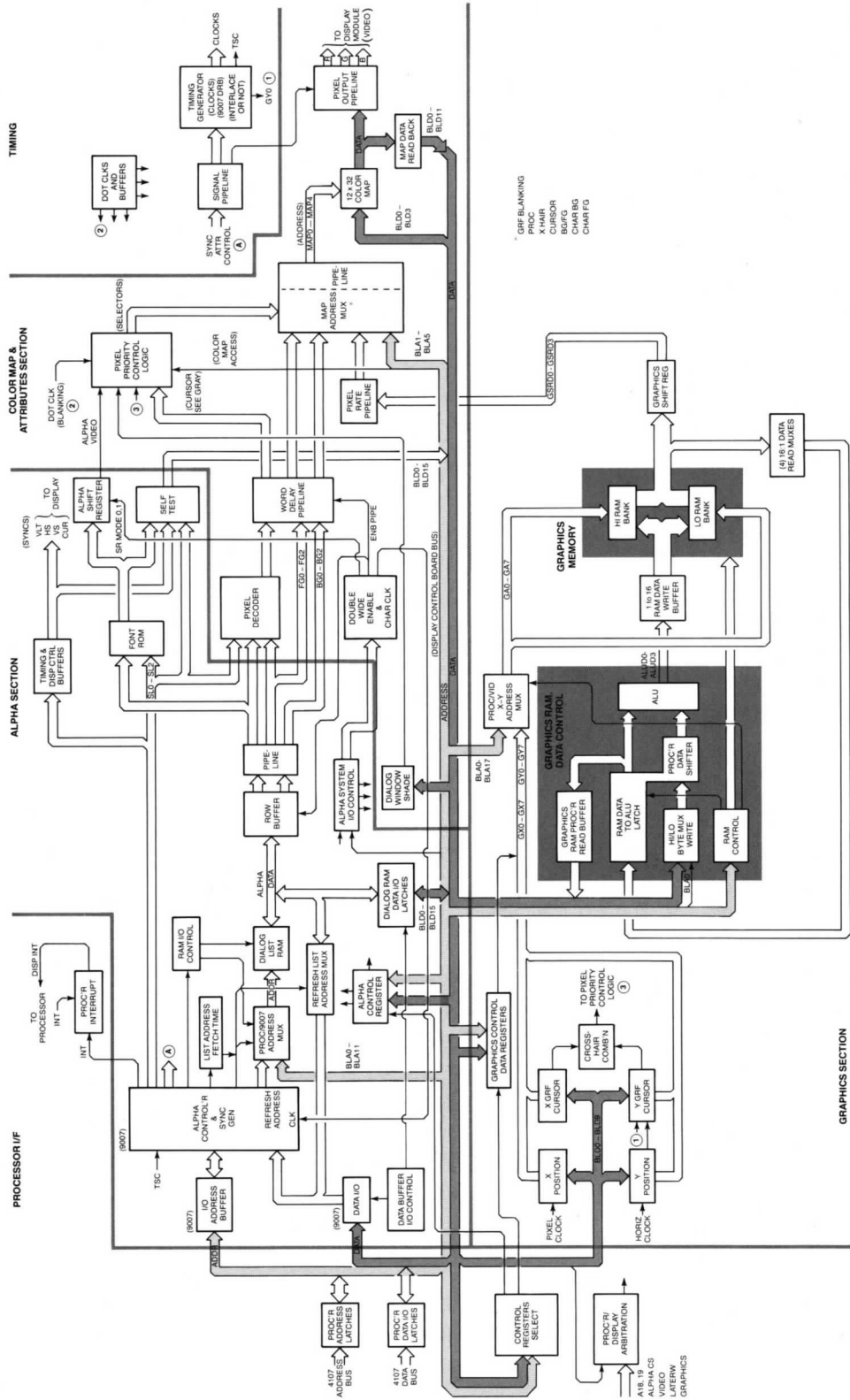


Figure 4-24. Display Control Board Detailed Block Diagram (for enlarged version, see Figure 10-4).

PROCESSOR INTERFACE

The DCB receives data, address, and status information from the processor (on the Terminal Control Board) via a set of latches, collectively called the Processor Interface; the data latches retain data passing to and from the processor.

These blocks interface between the DCB's main bus and the system processor bus (on the Terminal Control board). This portion of the circuitry also includes the control registers for the Alpha and Graphics I/O circuits; this block converts DCB bus addresses and data for the alpha and graphics circuits. See Figure 4-25.

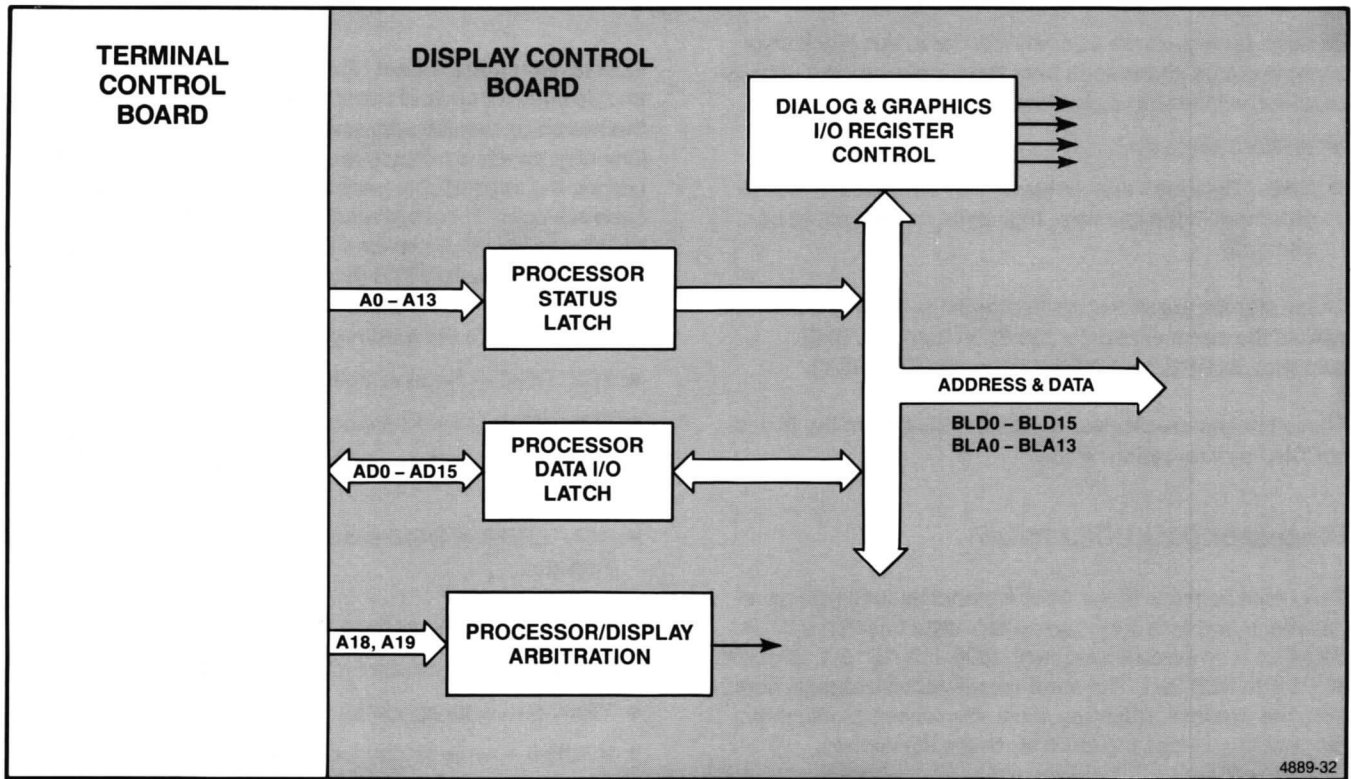


Figure 4-25. Processor Interface to Display Control Board.

Processor Address Latches

This block consists of three latches that capture address and status information from the processor's AD bus. The system address lines, A0-1 through A13-1, are latched and placed on the DCB address bus as BLA0 through BLA17-1 ("big latch" address).

Besides serving as the address interface, this block also accepts status information from the processor. The latches receive the following status lines:

- WRCY-1 Write cycle
- BHE-1 Byte high enable (used with address bit, AO, to determine if the low byte, high byte, or both are to be enabled).

These signals are all transferred onto the DCB bus and are named the same except for the BL in front (i.e. BHE becomes BLBHE, and WRCY becomes BLWRCY).

These latches are clocked by BLCLOCK-0 from the Processor/Display Arbitration circuit.

Processor Data I/O Latches

This block consists of two bi-directional latches that pass data back and forth from the system data bus to the DCB data bus. The system data lines, AD0-1 to AD15-1, become BLD0-1 to BLD15-1. The send versus receive signals come from the Processor/Display Arbitration circuit block; this block also provides the clock for these I/O latches.

These latches pass read data from the DCB to the processor in the usual manner. However, when the processor writes instructions to the DCB (processor-to-display write cycle), these latches operate as follows: The processor writes address, data, and status into the latch upon BLCLOCK-0. Then, the processor is free to execute other operations (bus cycle, etc.) while the DCB is acting on this instruction. If the processor tries to send another instruction to the DCB before it has finished executing the first instruction, the READY line causes the processor to wait until this instruction is executed. This scheme speeds up operations, by permitting the processor to perform other operations while the DCB is busy.

Alpha & Graphics Control Registers

This block consists of three pairs of registers: the alpha and graphics registers selector, the alpha control/status register, and the graphics control/status register. The alpha and graphics registers are bi-directional, allowing a status read as well as control write.

Control Registers Select. This register makes the I/O enable lines for several circuit blocks on the DCB. Each of the two chips receive address inputs via BLA1-1 to BLA6-1. One chip sends word/byte read requests to the addressed blocks; the second chip generates word write strobes for certain blocks. The word read register is enabled by the VIDIO and RENB (Front-End PAL). The word write register is enabled by the HWSTB (hardware strobe) line.

The outputs from the read register are:

- TESTRD-0 — Read enable for Self Test buffer.
- FONTRD-0 — Read enable for alpha Font ROM buffer.
- GCNTRD-0 — Read enable for the Graphics Control Register.
- ACNTRD-0 — Read enable for the Alpha Control Register.

The outputs from the write register are:

- XPAN-0 — write strobe for the X-Crosshair Pan register.
- YPAN-0 — write strobe for the Y-Crosshair Pan register.
- XCUR-0 — write strobe for the X-Cursor register.
- YCUR-0 — write strobe for the Y-Cursor register.
- TBWIN-0 — write strobe for the "top/bottom alpha window shade."
- GCNTLWR-0 — write strobe for the Graphics Control Register.
- ACNTLWR-0 — write strobe for the Alpha Control Register.

Alpha Control Register. This register interfaces between the board's data bus and the alpha/dialog control lines. The register accepts control input from the processor and sends this out over its main output lines. The register also allows the processor to read the current status of the same control lines. These control lines are:

- CHARBLINKCLOCK-1 — Character blink clock; accepts alpha character blink command (See NOTE).
- CUBLINKCLK-1 — Cursor blink clock; accepts alpha cursor command (See NOTE).
- BLOCKCUR-1 — Changes alpha cursor from two-line to full-cell cursor.
- XPRNTENB-1 — Blocks out graphics in cells where alpha characters also appear on display. When set, it enables graphics pixels to be seen behind characters that have a background color of 0.
- APAGE0-1 to APAGE2-1 — to Character Font ROM; not used in current applications (smaller ROMs do not require it).
- CLRPIX-0 — "Clear pixel" sets the pixel value to black (no video); used only for testing.
- VRESET-0 — "Video reset" is used to test the video section.
- ATTRTEST-1 — This allows Self Test to check the attribute gate array.
- VIDOFF-1 — not used in 4107.
- CAL-1 — not used in 4107.
- STOPPIX-1 — This line allows the processor to read the Color Map without causing interference on the display screen; it temporarily disables the clock enable to the video output register.
- ODD-1 — not used in 4107.

NOTE

The blink rate for alpha characters and cursor is controlled by firmware (not these hardware registers).

These register chips are clocked in the write direction by ACNTLWR-0 (the enable pins are tied active). The chips are clocked in the status-read direction by RAMRDCLK-0; the read enable comes from ACNTLRD-0.

Graphics Control Data Registers. The terminal uses this register to set up the various graphic circuitry control parameters.

This block consists of two registers which receive control signals from the DCB data bus. These latches decode their data input lines (from the processor) into actual control signals for the various graphics circuit blocks. The processor may also read these latches, to examine the current status of these control lines.

These registers send out the following graphics control lines:

- SHIFT0-1 to SHIFT3-1 — These lines control the shift modes of the data shifter PAL, which controls the shift register's shift/count operations. See Table 4-6 (Data Shifter Modes) for details.
- GPAGE1-1 — This selects "graphics page 1" (versus "page 0") for reading data from graphics memory.
- GWREN0-0 to GWREN3-0 — These are separate write enable lines for the four memory planes in the graphics bit map.
- ALU0-1 to ALU2-1 — These lines select one of eight modes for the ALU (writing data into the graphics memory). See Table 4-5 (ALU Modes) for details.
- WRBOTH-1 — This enable allows simultaneous writing to both halves of the graphics memory; this is used primarily for fast screen erase.

The two chips that make this register, are permanently enabled in the write direction and are clocked by GCNTLWR-0. The same chips are read enabled by GCNTLRD-0; the chips are read-clocked by RAMRDCLK-0.

Processor Interrupt

This block provides interrupt feedback to the processor. The alpha controller chip generates an interrupt signal called INT-1. This signal is ORed with the system interrupt signal (INT-0), from the additional 96-pin connector. The resulting signal, DISPINT-1, is placed back on the system bus to the processor. This signal tells the processor that the DCB is generating an interrupt and wants service.

Processor/Display Arbitration

This block is a programmable array logic chip that could be called the "front end PAL" (since it drives the control PALs for the alpha and graphics systems). The main function of this chip is arbitration between the processor and the DCB for controlling the alpha and graphics sections. The chip functions as a two-bit state machine (four states) that tells the processor if the DCB is busy or not. The four states and jump conditions are shown in Figure 4-26. The chip accepts numerous inputs that indicate the busy condition of the DCB. When the board conditions are right and the right PAL states are up, the processor can access the DCB.

The inputs for this chip are certain control lines on the DCB bus and certain control and I/O lines from the system bus. These inputs are combined by the internal logic array to make the required output signals. The outputs control the Processor I/O Data Latch and the Graphics and Alpha Control Registers. These input lines and conditions are:

- GBUSY-0 — Graphics system busy report.
- ABUSY-0 — Alpha system busy report.
- LS2-0 — Not I/O space. "Latched status 2"; a processor status bit that indicates whether the current bus cycle is a memory access or an I/O access.
- A18-1 — Upper Address bits.
- A19-1 — Upper Address bits.
- ALPHACS-0 — Alpha system chip select from processor.
- VIDIO-0 — Processor access to certain parts of the DCB not accessed by ALPHACS-0.
- LATERW-0 — Late read or write, from Terminal Control board. (This is BRW-1 delayed by one processor clock cycle.)
- SMRESET-0 — same as SYSRES (system reset) from processor.
- BLWRCY-1 — Latched version of write cycle from processor.
- WRCY-1 — Write Cycle from processor
- APAGE1-1 — This distinguishes between Page 0 and Page 1 of memory. Used during write operations to graphics memory, this provides latched information selecting either Page 0 or Page 1 of graphics memory for a write cycle operation.

The processor sends a request via A18, A19, alpha chip select, and video I/O. This is translated into an alpha request (ALPREQ-1) or graphics request (GRFREQ-1), which go to the alpha or graphics state machines. These state machines respond by executing the request and placing ABUSY or GBUSY on the inputs of this chip. The "page 0" signal tells which half of the graphics bit map RAMs are being accessed. The "ready" output becomes DISPRDY-1, which allows the processor to complete the current bus cycle and start the next. The WENB (write enable) output enables the input data latch so the processor can write data to the DCB. The RENB-0 line enables the contents of the DCB's read data latch onto the processor data bus during read operations.

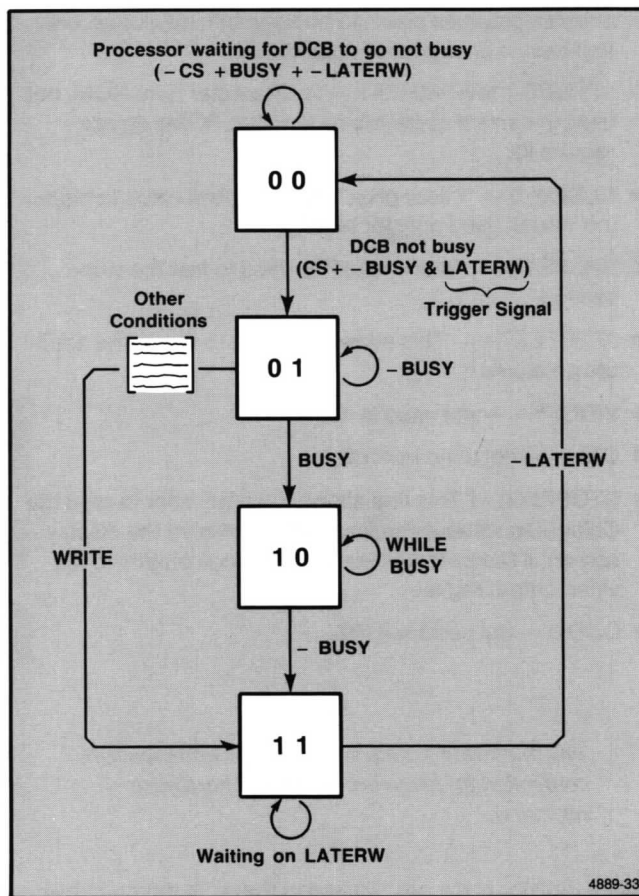


Figure 4-26. Front-End PAL States.

DIALOG (ALPHA) SECTIONS

This part of the DCB theory describes the circuitry that creates, stores and writes alphanumeric data on the display screen. The most common use for alpha data in this terminal is in terminal-to-host communication (and echo on the screen); hence the term "dialog area." The dialog circuitry contains its own memory, controller chip, character font generator, and I/O circuitry to the board bus and to the Color Map.

Alpha Controller

The alpha controller consists of a type-9007 crt controller chip and various blocks of supporting circuitry.

9007 I/O Address Buffer. This circuit buffers the DCB address bus lines, BLA1-1 to BLA5-1, and places them on the alpha controller's address inputs, VA0 through VA5, during a 9007 I/O cycle.

9007 Data I/O. This bi-directional latch passes data between the DCB data bus and the alpha controller's data inputs. Viewed from the board side of the bus, the inputs to this latch are, BLD0-1 through BLD7-1. The latch's outputs feed the controller's data I/O lines, VD0 through VD7. The Data Buffer I/O Control block determines the direction of data flow through this latch.

Alpha Controller & Sync Generator (9007). This controller chip manages the dialog/alpha portion of the display. As such, it acts independently of the main processor and controls the activity of the Dialog RAM and Character Generator blocks.

The 9007 controller addresses the Dialog List RAMs and controls the other dialog circuits. The controller contains a series of internal registers that increment according to firmware, to remember which character row is currently addressed. The Dialog CRT Controller also controls the character row buffers and makes the timing and sync (vertical and horizontal) signals for other Display Control board logic and for the Display Module. Figure 4-27 is a functional block diagram of the Dialog CRT Controller chip.

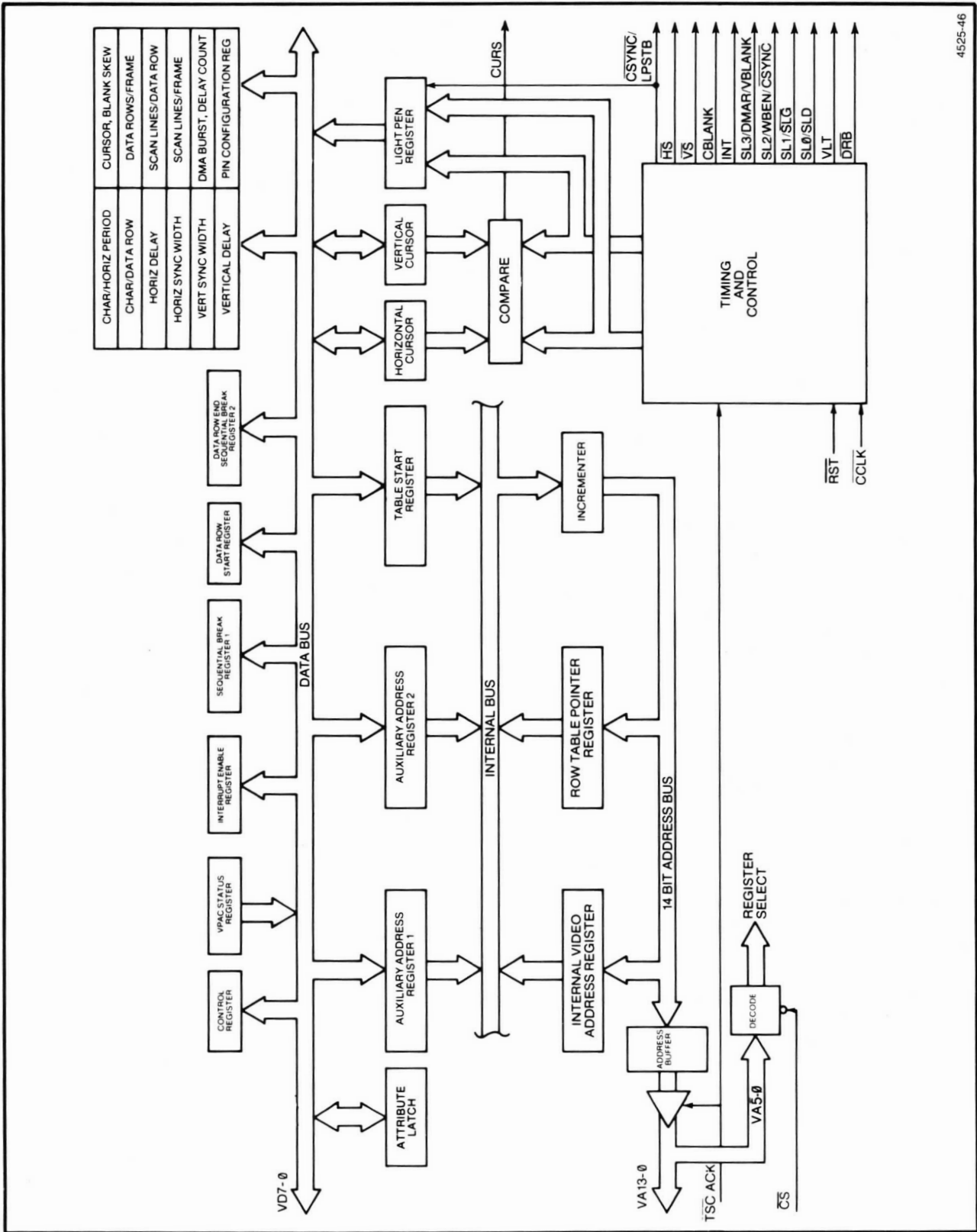
Processor I/O Address Bus lines A1 through A5, plus WRCY (write cycle) pass through an input buffer and drive VA0 to VA5. These lines connect to the 9007's input address pins of the same names.

VA0 to VA5 serve as both input and output lines for addresses. When serving as inputs (driven by the processor) VA0 – VA4 address an internal register (VA5 selects read or write: 1 = read, 0 = write). During output, all thirteen lines pass addresses for screen dialog refresh. Such addresses go to the Dialog Memory RAM. Video data cannot be displayed while the processor is writing the 9007; this is because six address bits are taken up during such a write. The dialog control state machine prevents interference during such a write.

The eight-bit data port (VD0 – VD7) handles both incoming and output data. Input data comes from either: the processor I/O (DAT0 – DAT7) via the DC board data bus, or the refresh video list address. The refresh dialog list address comes from the output of the Dialog RAMs through a multiplexer that selects between alternate bytes in the 16 bit List RAM word. Data to and from the DC board data bus passes through a bi-directional latch, U477. The B port of this latch accepts incoming bus data, while the A port accepts incoming data from the controller chip (going out to the bus and to the Processor).

At the beginning of each display screen character row, the 9007 reads a row table to see where the data for this row of characters begins. The 9007 then fetches data from the Dialog List (without intervention from the processor), causing their display on the CRT.

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Figure 4-27. Dialog CRT Controller Chip (9007).

Figure 4-28 shows timing relationships for several 9007 signals.

The address in/out direction is controlled by:

- TSC [pin 33] – Tri-State Control input. When this control line is active low, the address port is in the input mode (processor I/O); when it is high, the address port outputs the CRT Controller addresses.

The remaining input/control lines serve the following functions:

- CCLK [pin 14] – Character Clock input accepts CCLK-0 (Character Clock) signal, from the Timing Generator PAL.
- RST [pin 26] – Reset input, accepts the VRESET-0 (Video System Reset) signal. This is a hardware reset to the 9007.
- CS [pin 25] – Chip Select input accepts the signal, 9007CS-0 (Dialog Controller Chip Select) which comes from the alpha control state machine. This signal selects the 9007 for processor I/O through its data port (VD0 – VD7).

The following output/control lines serve these functions:

- CBLANK [pin 35] – Composite Blanking output signal passes through the Character Pipeline on its way to the attribute logic.
- CURS [pin 34] – Alpha Cursor output (CURS-1) feeds the attribute logic and the double-high & double-wide circuit. This signal is true during the row and column where the alpha cursor is positioned, and at the beginning of a double-wide character row.

- INT [pin 27] – output signal, DISPINT-1 (Display Interrupt), exits the board on the Display Module connector. It generates the vertical rate interrupt.
- VLT [pin 11] – Visible Line Time tells the display circuitry which part of the horizontal scan is available for data display.
- DRB [pin 15] – Data Row Boundary identifies (to the display) each new character row. It occurs on every fifteenth scan line and is active for the whole scan line (including most of the blanking interval).
- HS [pin 13] – Horizontal Sync, is used for Display Module sync.
- VS [pin 12] – Vertical Sync for the Display Module.

A set of four address outputs select one of the fifteen scan lines per character cell. These outputs are: SL0 thru SL3 [pins 28 – 31] – Scan Lines 1 to 15 select (binary decoded).

The 9007's TSC input is driven active (low) by the Timing Generator circuit block.

RAM I/O Control. This circuit simply gates the read enable signal with TSC-0 to make the output enable signal for the dialog RAMs. The high and low chip select lines, that enable the dialog RAMs, are shown with this block.

List Address Fetch Time. This block combines some 9007 timing signals and uses this to set the proper time for the list address to be placed on the 9007 data bus. This AND gate and driver accepts the horizontal sync output from the 9007 and combines it with the tri-state control signal.

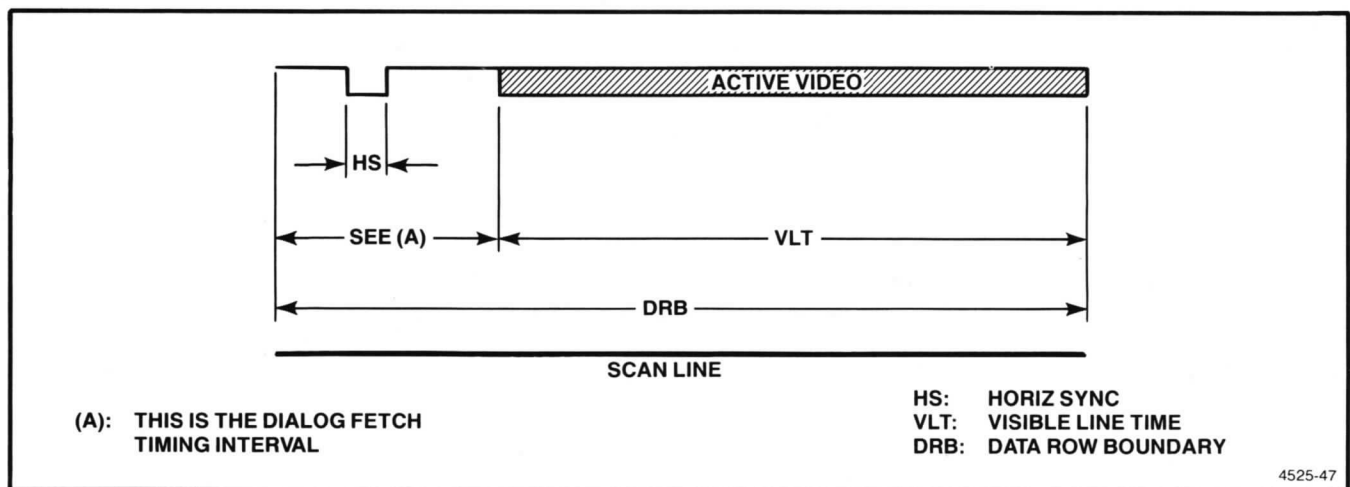


Figure 4-28. Dialog Fetch Timing Diagram.

Data Buffer I/O Control. This circuit determines the direction of data flow through the 9007 Data I/O Latch and through the Dialog Memory Data I/O Latch. The circuit consists of several groupings of AND gates. They logically combine the input signals to make outputs that enable these data transfers:

- Processor to 9007
- 9007 to processor
- Processor to RAM
- RAM to processor

Dialog Memory and I/O

The Dialog List Memory consists of several smaller functional groups, as indicated in the upper part of Figure 4-29. These sub-blocks are:

- Dialog Memory Address MUX
- Dialog List RAM
- Refresh List Address MUX
- Row Buffer and Pipeline

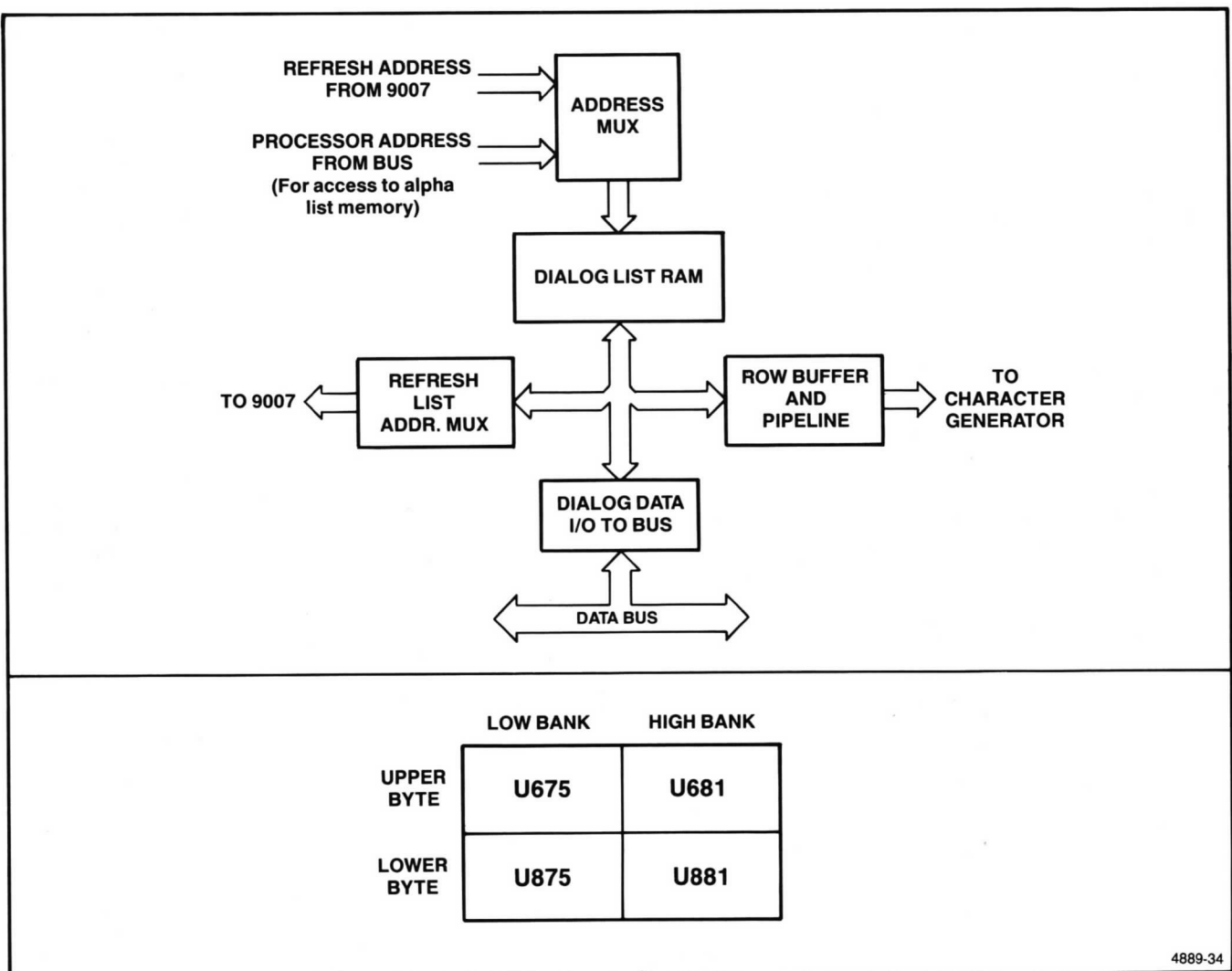


Figure 4-29. Dialog List Memory Diagram.

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The dialog memory provides storage for: a row link-list table, and the lists of character codes/attributes for each row of displayed characters. The RAMs are either addressed directly by the processor (when building lists) or by the 9007 controller (in refresh mode). The address MUX selects one of these address sources. The RAM I/O Control circuitry selectively enables different physical RAMs, depending on the address selected. Data is then written into, or read from, the RAMs via a set of data latches that interface with the DCB data bus. This allows the processor to write to or read from this dialog memory list. A second output latch sends character data to the character generator. The third output latch passes dialog data back to the 9007's data input (for refresh only). The refresh data is essentially MUXed with the processor data going into the 9007. This is shown in Figure 4-29.

Processor/9007 Address MUX. The address MUX switches between the address lines from the processor (BLA1 to BLA12), and the address lines from the 9007 controller (VA0 to VA11). This sub-block consists of three MUX chips that switch between these two sets of address lines. The control input for these MUXes is the TSC-0 clock signal from the Timing Generator circuitry.

Dialog List RAM. The Dialog List RAM provides 8K bytes of memory for dialog text storage. The standard terminal contains four chips, divided into two banks, each with upper and lower bytes. See the lower part of Figure 4-29.

Dialog RAM Data I/O Latches. This pair of latches is the data I/O port for the dialog list RAMs. These latches store lines BLD0 through BLD15 going into memory, and D0 through D15 coming out of memory. RAMRDCLK-0 clocks these latches to write processor data into the RAMs. The enable for reading RAM data onto the DCB bus comes from the Data Buffer I/O Control block.

Refresh List Address MUX. This block is a 16-to-8 MUX chip. The Refresh List Address MUX accepts output data from the Dialog List RAMs and sends it back into the 9007 during list address fetch time. The 9007 then sets the RAMs' address lines and control inputs for the fetch. The inputs to the MUX are the sixteen data lines (D0 through D15). The MUX switches between the low and high data bytes, and places its output on VD0 through VD7 (going into the 9007).

Row Buffer. The Row Buffer passes dialog list output data to the character generator circuits. This block consists of two byte-wide, 80 character buffers. Each buffer has enable and clock controls. These buffers store a single row of characters of the first scan line (DRB time). The row buffers then provide the character data for the remaining scan lines of the character row, freeing memory for processor accesses. (This eliminates 14 rows of access to the RAMs, which is RAM access time that the processor can use.)

Pipeline. The pipeline acts with the Row Buffers to pass dialog data to the character generator. These two pipeline latches provide the timing necessary to compensate for propagation delay through the parts.

The sixteen data lines are labeled according to functions at the Pipeline outputs. These following data lines are collectively known as "character attributes":

- D0 to D7 C0 to C7 (Character code)
- D8 to D10 FG0 to FG2 (Foreground code)
- D11 to D13 BG0 to BG3 (Background code)
- D14 BLINKENB (Blink enable)
- D15 UNDERLINE (Underline enable)

Character Generator Operation

The alpha character generator circuit consists of a character ROM, an output data latch, alpha shift registers, and some discrete logic used to create double-wide characters. This circuit block functions with the Character Attribute Pipeline and the Character Attribute and Control Logic to actually make alpha screen characters.

How Alpha Characters are Produced. This is an overview explanation of how alpha/dialog characters are generated. Refer to Figure 4-30 while reading this explanation.

The Character ROM receives an eight-bit address from the Dialog RAM output latch. These ROM address lines, C0 through C7, specify a particular character stored in the ROM. The ROM's SL0 to SL3 inputs determine the character-matrix-row location along the current scan line. The accessed character-matrix-row exits the ROM as an 8-bit parallel character code. Each 8-bit code is loaded into a shift register and converted to a serial stream. This serial stream then enters the pixel-priority circuit, along with other attribute data (such as underline, blink, etc.). This logic is a combinatorial array of logic gates arranged to select the desired pixel outputs for any one of many input conditions. The serial data from the character ROM, along with the other input signals, allow the pixel-priority logic to decide which pixel source should generate the next pixel on the CRT. Several of these signals have been pre-processed to allow the attribute logic to perform its task. There are also several signals that are pipelined to align all of the pixels.

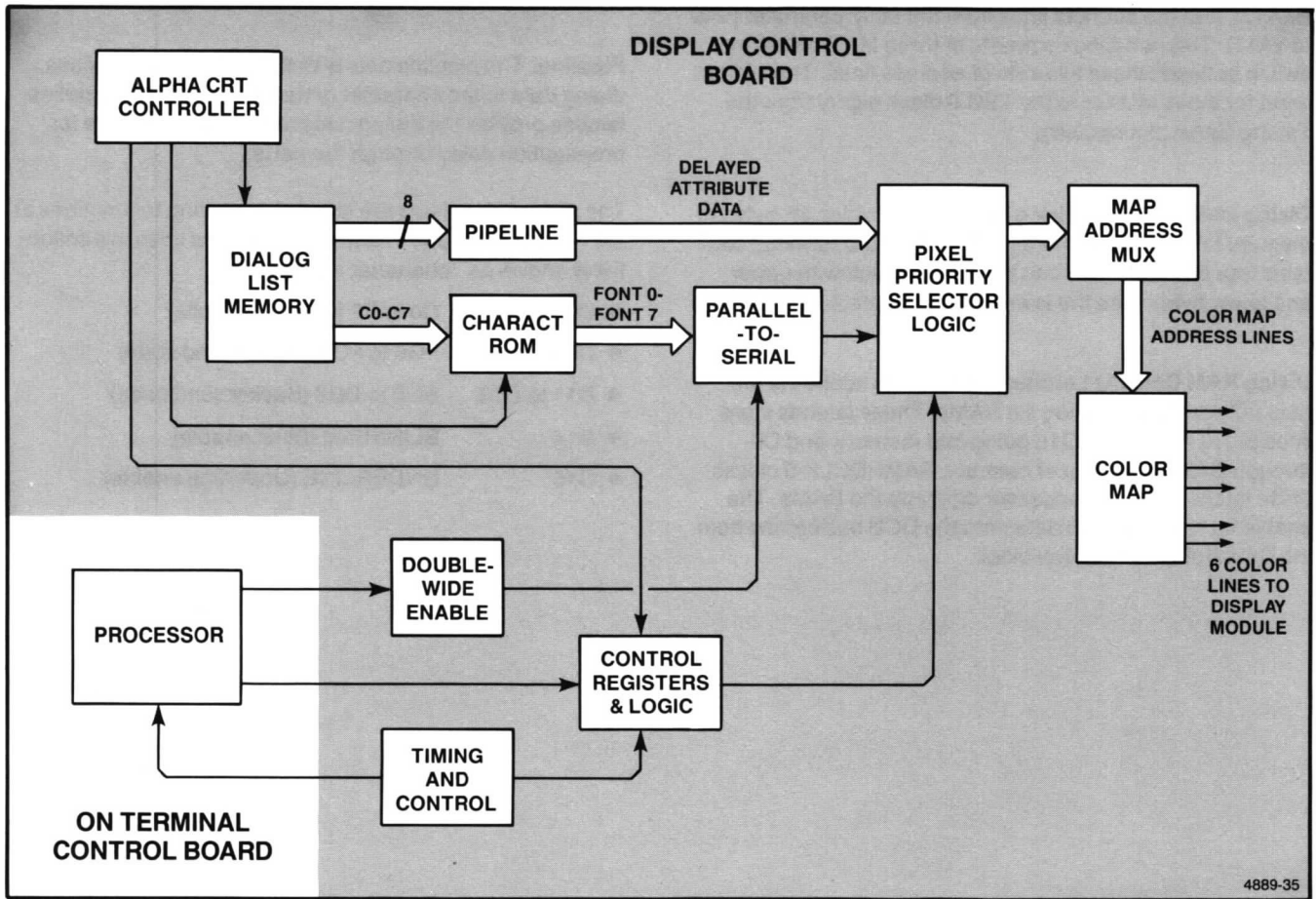


Figure 4-30. How Alpha Characters are Produced.

This selection information exits on one of the eight outputs of the custom logic circuit, which act as a selector for the address needed to generate the desired pixel:

- 0 Processor access to color map
- 1 Blanking of the screen
- 2 Crosshair cursor
- 3 Alpha cursor
- 4 Graphics pixels
- 5 Character foreground
- 6 Character background
- 7 (not used)

After the pixel-priority logic selects the desired pixel source, this data is translated into color codes by the Color Map. The Color Map is programmed by the processor. The Color Map's outputs are latched and sent to the Display Module as two bits each of RV (red video), GV (green video), and BV (blue video).

Font ROM. The Font ROM contains the pixel patterns for the dot-matrix alpha-character fonts that are included in the standard terminal. The first four address line inputs are programmed to select one of fifteen rows within a character matrix. The remaining eight inputs access a particular character code. (The character occupies a 7 by 9 area in an 8 by 15 cell; see Figure 4-31). The ROM stores pixel patterns for 255 different characters.

The character data exits on outputs O0 to O7. These data bits are presented to the alpha shift register.

Alpha Shift Register. This sub-block is a pair of 4-bit shift registers connected in series. This circuitry converts the 8-bit parallel output of the Character ROM into a serial pixel stream. The Q3 output of the first register connects to the DSR (data shift right) input of the second register. The Q3 output of the second register passes the serial character stream to the Alpha Video input of the pixel-priority logic. The Double-Wide Enable block controls the shift and load functions of this block. The two shift/load inputs (SRMODE0 and SRMODE1) are decoded according to Table 4-4.

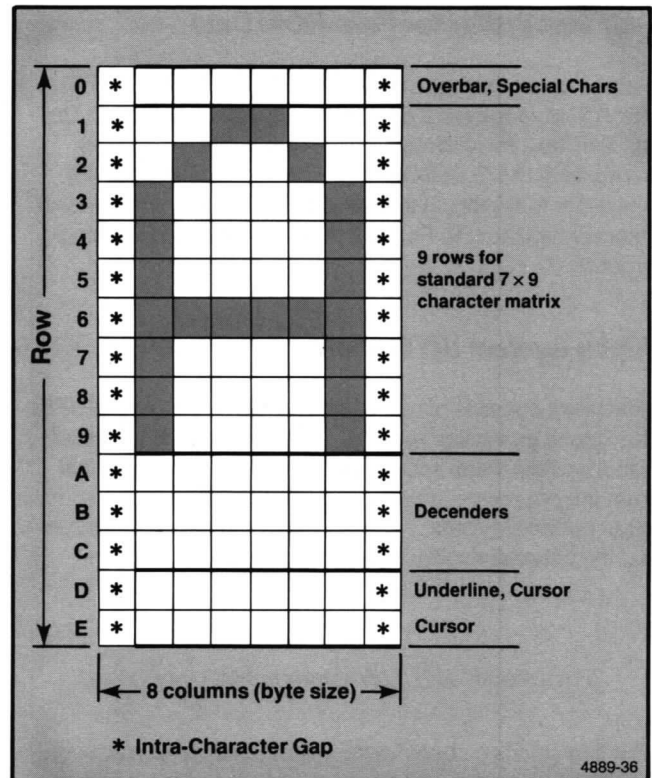


Figure 4-31. Alpha Character Cell.

Table 4-4
SHIFT REGISTER MODES

SRMODE0	SRMODE1	Function
0	0	Hold
0	1	Shift right
1	0	Shift left
1	1	Load next character

Self Test Buffer for Font ROM Data

This buffer enables the output of the Font ROM, FONT0 to FONT7, onto the DCB data bus, BLD0 through BLD7. During Self Test, the processor uses this buffer to read the contents of the Font ROM. This data is compared to the character font table in the system EPROMs; the processor thus verifies that the Font ROM is correct and is working properly.

Alpha System I/O Control

This block consists of two custom array logic chips (NOTE), the "alpha controller" and "alpha I/O logic." These combinational logic chips accept address and control signals from the processor, from system and board clocks, and from other control sources; and they make the signals that control the entire dialog/alpha system.

NOTE

Also called "PAL" (Programmable Array Logic).

The first chip is a state machine that accepts: (a) request lines from the processor/display arbitration block, and (b) status lines from the alpha circuits. It sends state information to the second chip via pins 15 through 20. This controller chip also makes the ABUSY-0 status signal, and the MAPIO-0 status signal. Figure 4-32 shows the control states of this chip.

The second chip makes the appropriate control signals for the dialog memories and related blocks based on information from the controller state machine. It chip selects the 9007, makes the high and low RAM-write control lines, and a strobe and clock:

- ADREN-0 — Address enable
- HWSTROBE-0 — Hardware strobe
- ARAMWR-0 — Enables a write to the alpha RAMs.
- 9007CS-0 — Chip select for the 9007 controller chip.
- AHIWR-0 — Write strobe to high bank of dialog RAM.
- ALOWR-0 — Write strobe to low bank of dialog RAM.
- RAMRDCLK-0 — During write cycles, it clocks data into the RAM data input registers; during read cycles, it clocks RAM data into the registers so the processor can read it.
- MAPWR-0 — selects a write to the Color Map.

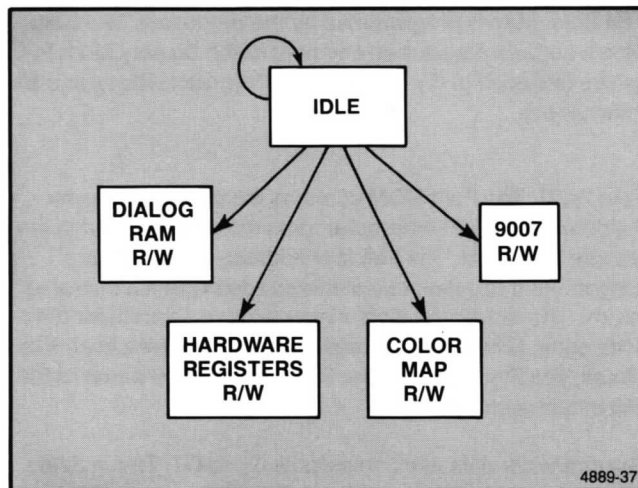


Figure 4-32. Alpha System I/O States.

GRAPHICS SECTION

Graphics data on the screen comes from the four-plane graphics bit map. This graphics memory is a RAM array, organized to store 1024 by 512 pixels (with four bits per pixel). The dimensions of the memory corresponds to the

640 by 480 display area on the screen, and the four bits-per-pixel provides the pixels' color information. Figure 4-33 shows this memory organization as it relates to the display screen. The graphics control circuitry provides refresh addresses for the graphics memories during display cycles.

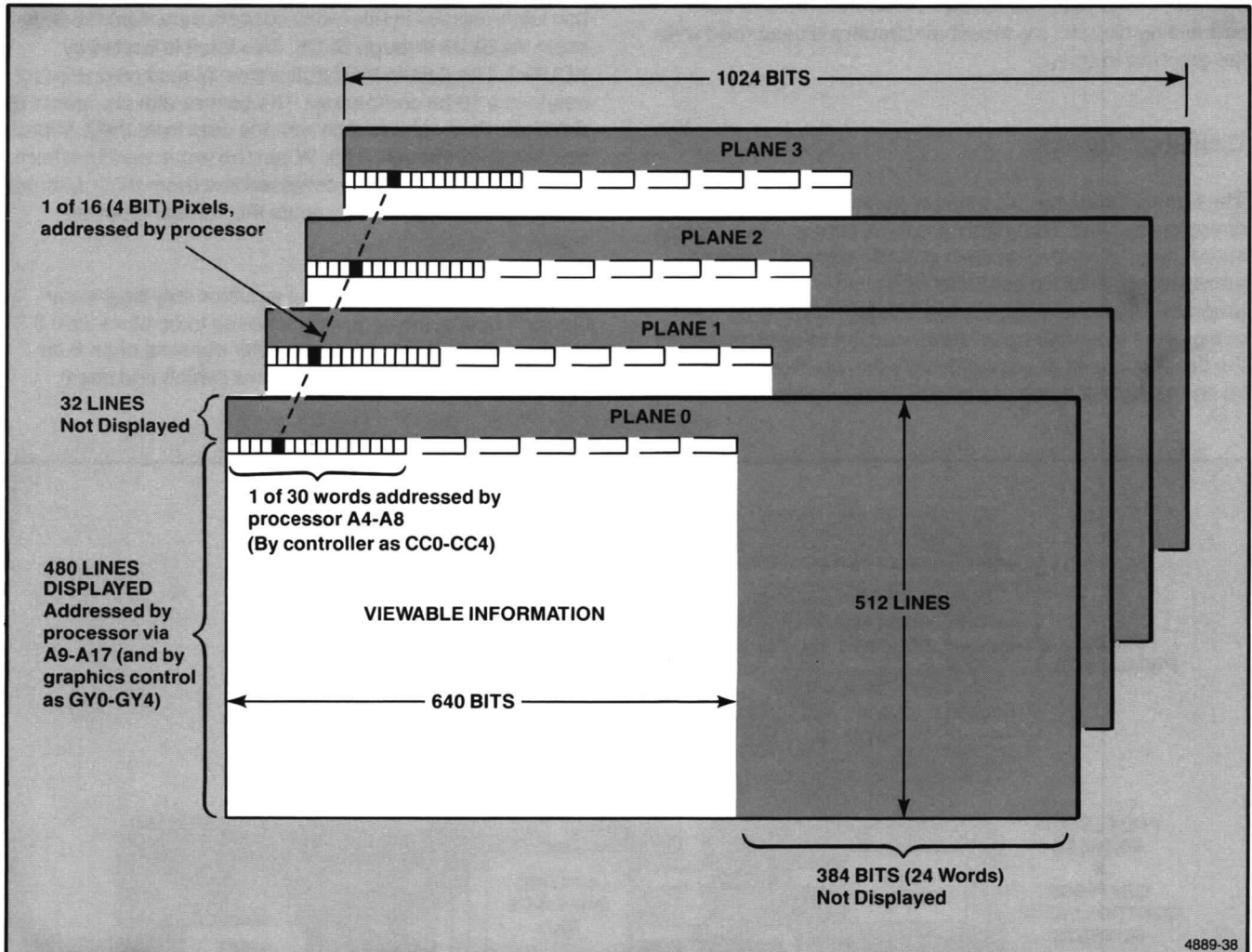


Figure 4-33. Graphics Memory Organization.

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The graphics memory circuitry consists of these super-blocks:

- The RAM and associated I/O circuits (1)
- RAM addressing and cursor circuits (2)
- Memory control and data input (3)

These functional parts (as numbered) are depicted in Figure 4-34. Since the crosshair circuit is closely related to the addressing circuits, the crosshair circuitry is described with the graphics memory.

Crosshair Cursor

The terminal displays two kinds of cursors: an underline dialog cursor, and a crosshair graphics cursor. The graphics cursor may be used to locate a point on a graphic screen presentation and then send that point to the applications program. Under program control, the joydisk may be used to move the crosshair up or down, and left or right. Next, are the descriptions of the circuit blocks that create the horizontal and vertical line components of this crosshair cursor.

Figure 4-35 shows the arrangement of the blocks that make the cursor. This diagram also shows the graphics address counters, which are related to the cursor blocks.

X Graphics Cursor. This block makes the vertical line part of the crosshair cursor. Since the location of this line is specified by an X ordinate value along the horizontal axis, the circuit is called the X Graphics Cursor block. The position latch/register in this block accepts data from the processor via BLD0 through BLD9. This latch is loaded by XCUR-0. The data in this latch is then placed on one set of inputs of a 10-bit comparator. The comparator compares the data from the position latch with the data from the X address counter, GX0 through GX9. When the requested line (from processor) matches the addressed line (from the X address counter) the comparator outputs the vertical crosshair signal.

Because the X component of the cursor may be greater than 640 pixels, the comparator needs to be more than 8-bits wide. Therefore, the comparator consists of an 8-bit comparator chip and two XOR gates (which add bits 9 and 10).

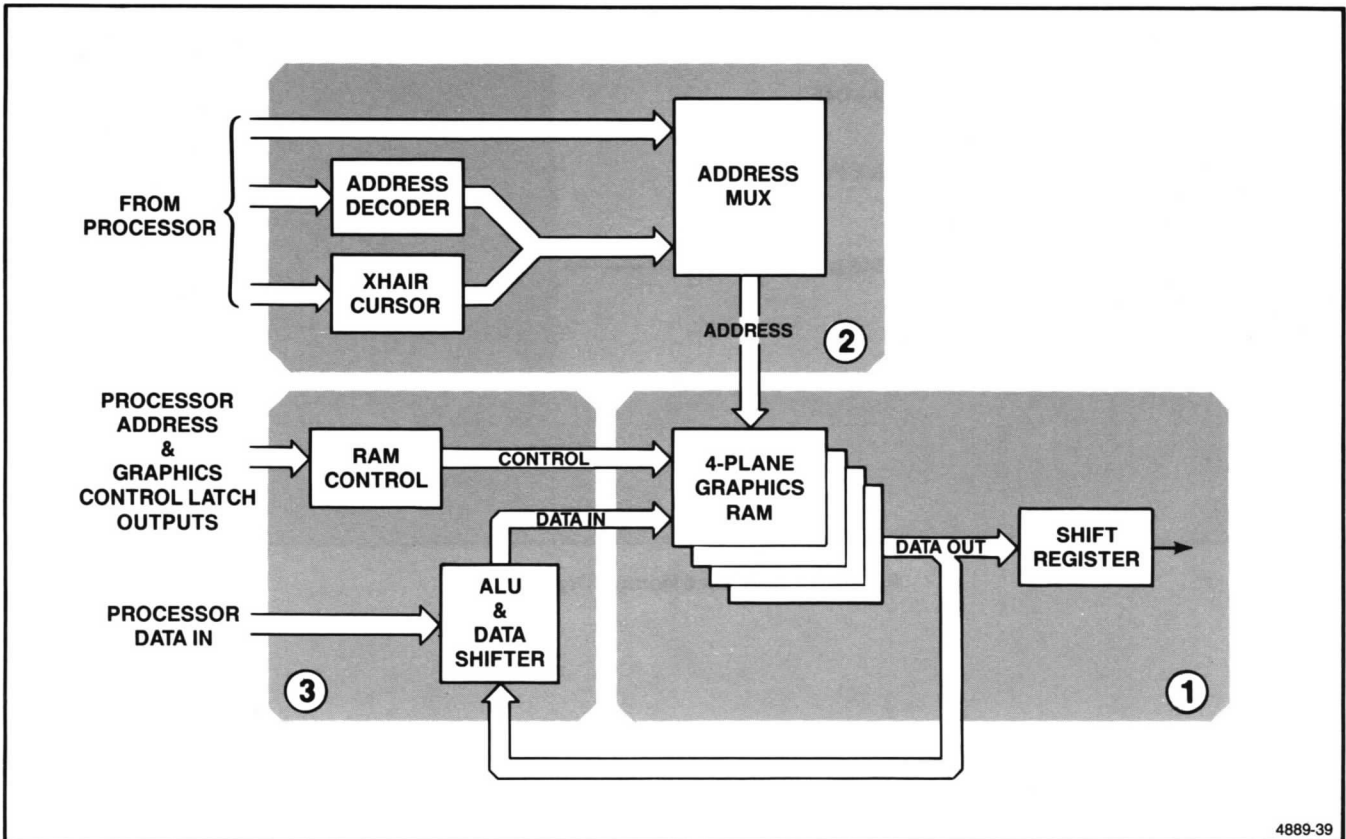


Figure 4-34. Graphics Memory Super-Block Diagram.

Y Graphics Cursor. This block makes the horizontal line part of the crosshair cursor. Because the location of this line is specified by a Y ordinate value along the vertical line, the circuit is called the Y Graphics Cursor block. The position register/latch in this block accepts data from the processor via BLD0 through BLD8. This latch is loaded by YCUR-0. The data in this latch is placed on one set of inputs of a 9-bit comparator. The comparator compares the data from the position latch with the data from the Y address counter, GY0 through GY8. When the requested line (from the processor) matches the addressed line (from the Y address counter) the comparator outputs the horizontal crosshair signal.

The XOR gate, connected to GY0, and the 8-bit chip combine to make a 9-bit comparator.

Crosshair Combination. The Crosshair Combination block combines the X and Y cursor signals and makes two other signals: XHAIR-1 and INTERSECT-0. XHAIR-1 makes the hole at the center of the intersect point. (This allows you to see the pixel beneath the crosshair intersection.) An XOR gate combines the two inputs to make this signal.

The INTERSECT-0 signal is not used by the terminal; it is only used during factory testing of this board.

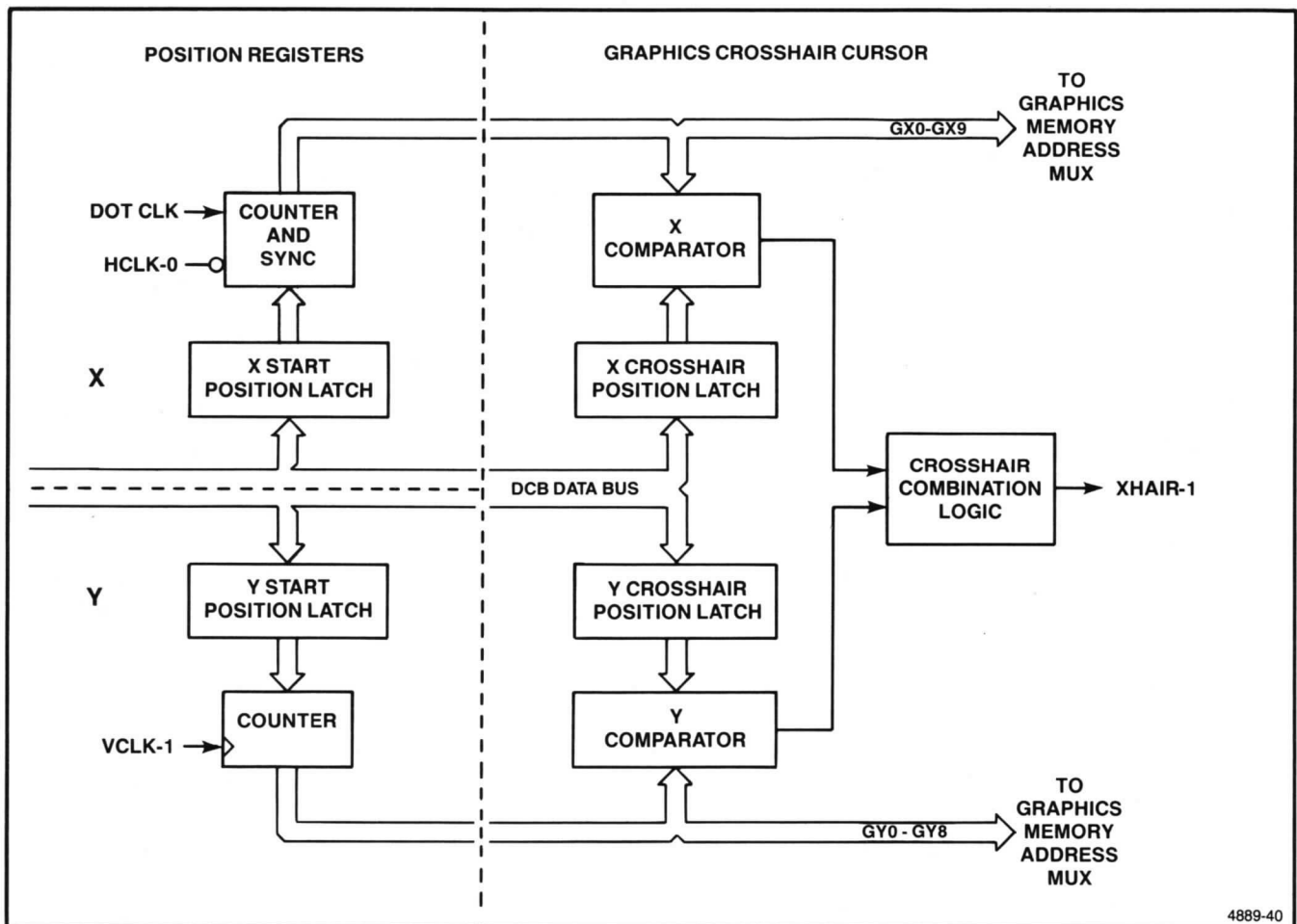


Figure 4-35. Graphics Cursor and Position Register Blocks.

RAM Addressing Blocks

The graphics RAMs are either addressed directly by the processor or by the X and Y Graphics Address blocks (during screen refresh cycles). The X and Y address counters provide the screen address during refresh memory cycles. The register in the X Addressing block selects the starting horizontal screen position for graphics (panning is accomplished by firmware). The address MUXes in these blocks select an address from either the processor or the address counters. See Figures 4-34 and 35 again.

X Position Block. This block outputs the proper X address to the Graphics RAMs to correspond with the writing beam horizontal position on the display screen.

The block consists of a loading latch and a 10-bit counter. The latch provides the initial X address for the X counter, which is loaded by HCLK-0 during the horizontal retrace time. The counter counts at the horizontal pixel rate of 25 MHz and sequentially sends addresses to the RAMs for each word along the scan line. The counter is made up of four 4-bit binary counter chips. One chip keeps the graphics and dialog displays synchronized. The other three counter chips act in parallel and send addresses, GX0 through GX9, to the RAMs (via the MUX) and to the crosshair circuit.

Y Position Block. This block contains a loading latch (register) and a 9-bit counter. The latch provides the initial value for the Y-axis counter, which is loaded by VCLK-0 during vertical retrace time. The counter counts at the vertical scan rate of 60 KHz and sequentially sends addresses to the RAMs for each scan line on the display screen; HCLK-0 clocks this counter on each horizontal retrace time. The counter is a 10-bit counter chip. The counter's outputs, GY0 through GY8, go to the Graphics Address MUX and the Y-crosshair circuit. Input pin 13 is the tri-state output enable for the PAL. The pin is connected to a "pull-down" resistor, to the Window Shade PAL, and to the Graphics Control Register; this allows a board tester to tri-state the outputs of these devices during testing.

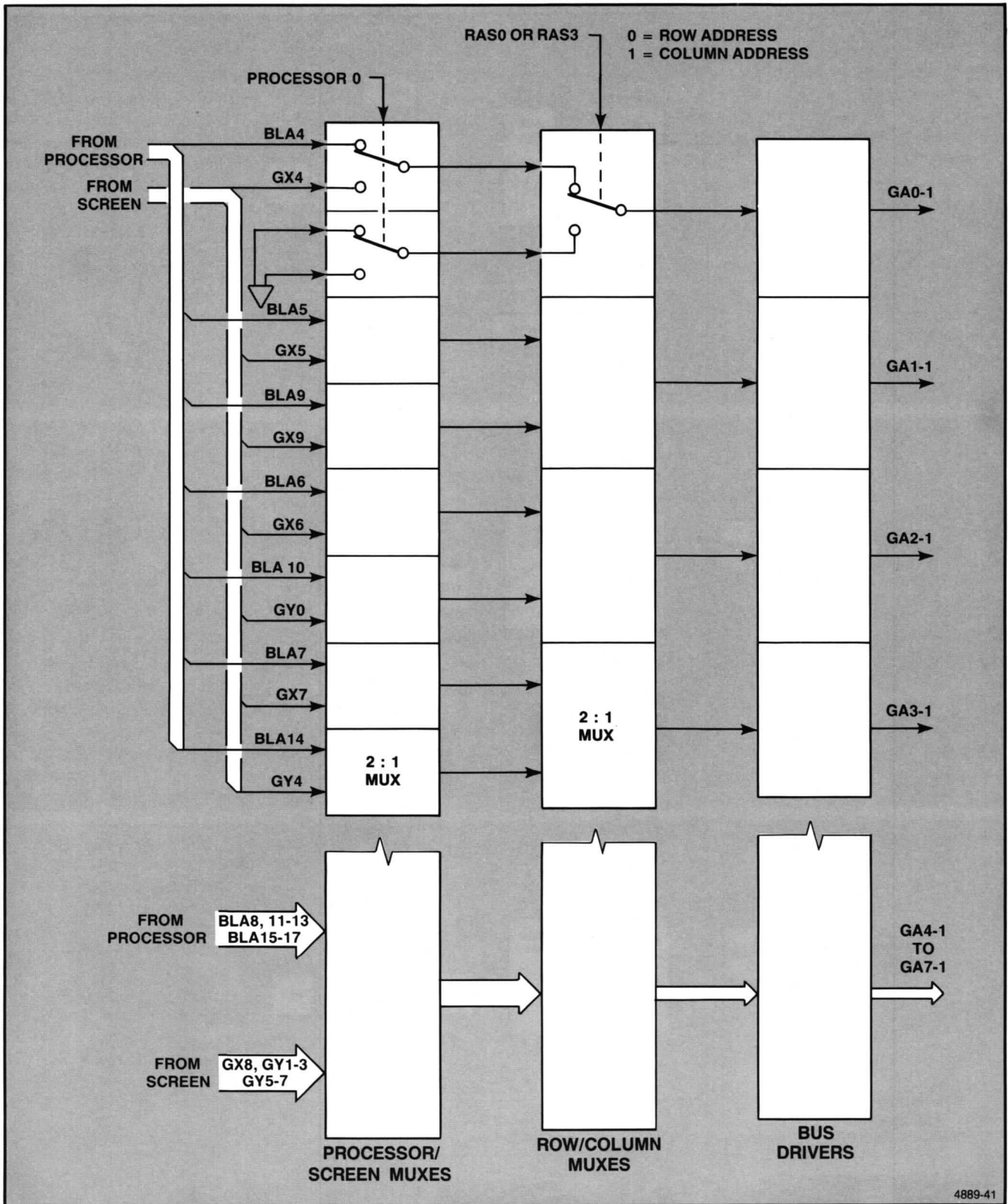
Graphics Memory Address MUX. This MUX sends addresses to the Graphics RAMs; it selects an address from either the processor or from the X and Y graphics position registers. The graphics address MUX is a 2-stage multiplexer. The first stage uses the state of PROCESSOR-0 (signal) to select either: 1) the XY position register output, or 2) the processor address bus, as the source for the next memory address. The second stage is a clocked MUX that provides the row/column address MUXing for the RAM; see Figure 4-36.

The RASn-0 outputs of the RAS/CAS PAL are ORed together by U217A; this provides the row/column address select signal for the second stage of the Graphics Memory Address MUX.

Graphics RAM Control and Data Input

The graphics memory array is controlled by signals from a custom ALU. The ALU selects and modifies the data going into the RAM. The following functional and block descriptions provide detail about this part of the graphics memory.

Two types of memory cycles are used, depending on the type of ALU operation being performed. When the ALU is set for "replace mode," and no write-protect bits are asserted, the graphics controller performs a write-only cycle. If any write-protect bits are asserted, or if the selected ALU mode is a "bit modification mode" (AND, OR, XOR), a read-modify-write cycle is performed. During such time, the current contents of the selected pixel location are read, operated on by the ALU, and then written back into the pixel locations in memory. See Figure 4-37.



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Figure 4-36. Graphics Memory Address MUX.

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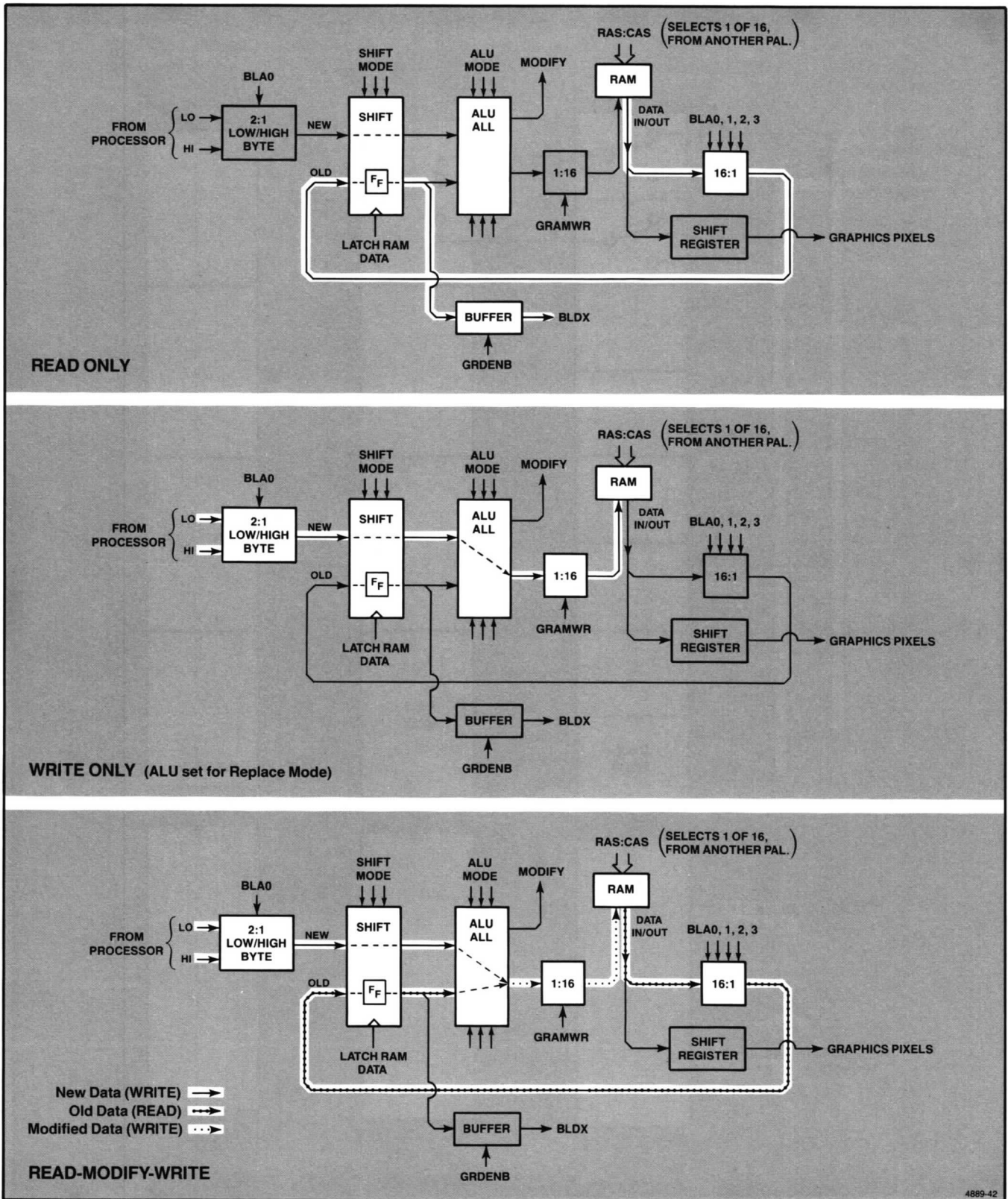


Figure 4-37. Graphics Memory Cycles.

ALU. The ALU (arithmetic logic unit) modifies pixel data as requested by the processor via the ALU mode-select inputs. The ALU is a custom array logic chip that modifies data going into the RAMs according to one of 8 different ALU function modes. The ALU does not alter a pixel if its associated write-protect bit has been set; the WRDIS0-1 to WRDS3-1 (write disable) lines prevent the ALU from modifying or over-writing data for the corresponding ALU modes. A 3-bit input, ALU0 to ALU2 (from the Graphics Control Register), selects the ALU mode; the selection decision is made by the processor. Figure 4-38 is a functional diagram of the ALU.

The 16 operating modes of the ALU are listed in Table 4-5.

Table 4-5
ALU MODES AND FUNCTIONS

ALU0	ALU1	ALU2	Explanation of Operation Performed
0	0	0	Replace current pixel contents with processor data.
0	0	1	"XOR" current pixel contents with processor data.
0	1	0	"OR" current pixel contents with processor data.
0	1	1	"AND" current pixel contents with processor data.
1	0	0	Replace current pixel data with 0's.
1	0	1	Replace current pixel data with 5's.
1	1	0	Replace current pixel data with A's.
1	1	1	Replace current pixel data with 1's.

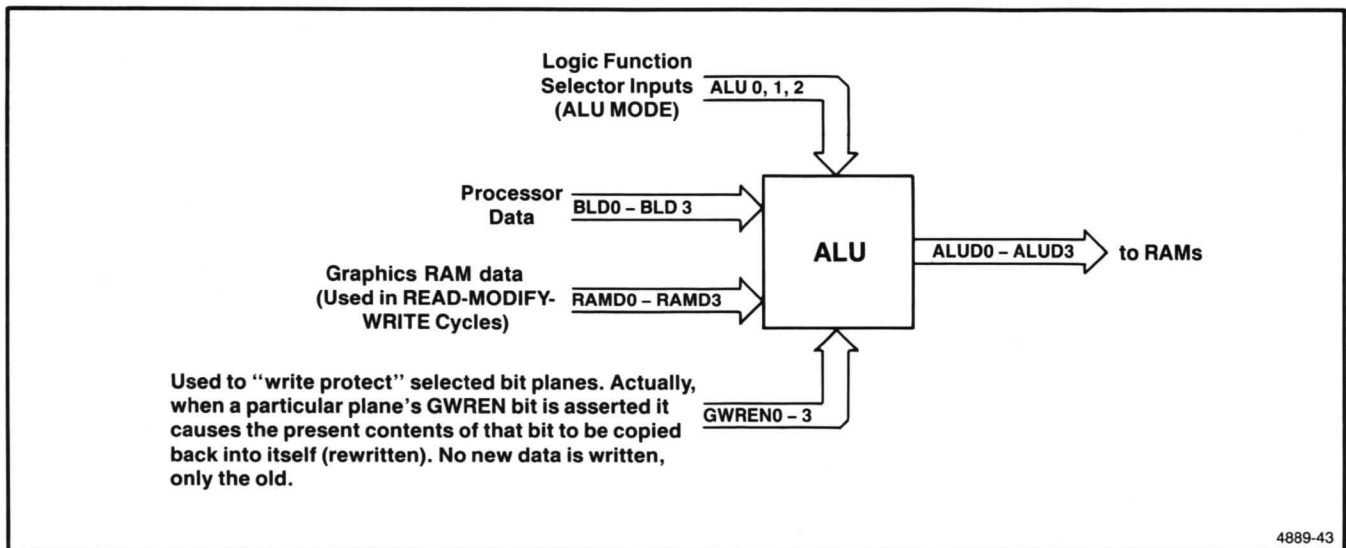


Figure 4-38. ALU Functional Block Diagram.

RAM Data-to-ALU Latch. Data enters the ALU from two sources: data read from the RAMs (during the read portion of a read-modify-write cycle), and data coming from the processor. Data from the RAMs passes through the RAM data latch on its way to the ALU; from the ALU it passes back into the RAMs (during a write cycle). This latch is actually part of a 20R4A custom array logic chip. (The other part of this chip is the Data Shifter in the processor-to-ALU data path.) This RAM data latch accepts RAM data, RAMD0 through RAMD3, from the 16-to-1 RAM Output Data MUX. During a read cycle, graphics RAM data is clocked into this latch by a clock signal from U215 (the Graphics Output Enable Write PAL). The SHIFT0 to SHIFT3 inputs control the data shifter modes: the number of bit positions, and the direction (left or right) that incoming processor data is shifted before being sent to the ALU. The four output lines, from this part of the chip, go to the ALU and to the Graphics RAM Processor Read Buffers.

Graphics RAM Processor Read Buffers. A pair of Graphics RAM Data Buffers direct the graphics memory read data to the proper bits of the DCB data bus during a processor read cycle. One of the buffers presents data on the lower four bits of both bytes (high and low) of the DCB data bus. This is done to ensure that the processor receives data on the proper half of the bus for both even and odd addresses. The other buffer forces zeroes on the remaining four bits of the high and low bytes of the DCB data bus, during a read of the graphics memory. Because the graphics memory is only four bits deep, these bits complete the data byte being read. Otherwise, these bits would have to be masked by an additional operation after being read by the processor.

Hi/Lo Byte Write MUX. During write cycles, data is transferred from the processor data bus to the inputs of the Data Shifter PAL by this high/low byte multiplexer. The write multiplexer selects between the low and high processor data bytes for writes to even and odd bytes, sending the correct data to the RAMs during write cycles.

Processor Data Shifter. The Data Shifter parallel shifts the bit positions of the new data coming from the processor and the old data coming from the RAMs (going to the ALU). The data shifter is contained in the second half of the Graphics RAM Data Latch PAL. This circuit shifts the incoming processor data by a specified number of bit positions, either to the left or the right. The circuit also contains test modes, used by the terminal's Self Test firmware to verify data path integrity in this section of the DCB.

The Data Shifter is part of a custom logic array (or PAL). Its control inputs are bits 12 through 15, and these combine to shift the data in one of 16 different modes; see Table 4-6.

Table 4-6
DATA SHIFTER MODES

Control Bits				Functions
15 ^c	14	13	12	
0	0	0	0	Shifts new processor data no spaces; moves old data from RAMs ^a .
0	0	0	1	Shifts new processor data left 1 space; reads old data from RAMs ^a .
0	0	1	0	Shifts new proc'r data left 2 spaces ^a .
0	0	1	1	Shifts new proc'r data left 3 spaces ^a .
0	1	0	0	Shifts new proc'r data right no spaces ^a .
0	1	0	1	Shifts new proc'r data right 1 space ^a .
0	1	1	0	Shifts new proc'r data right 2 spaces ^a .
0	1	1	1	Shifts new proc'r data right 3 spaces ^a .
1	0	0	0	Write new data as 0's (bin) ^a .
1	0	0	1	Write new data as 0's (bin); Read old data as 1's (bin).
1	0	1	0	Write new data as 1's (bin) ^b ; Read old data same as in RAMs.
1	0	1	1	Read old RAM data as 0's (bin) ^b .
1	1	0	0	Read old RAM data as A's (hex) ^b .
1	1	0	1	Read old RAM data as 5's (hex) ^b .
1	1	1	0	Read old RAM data as C's (hex) ^b .
1	1	1	1	Read old RAM data as 3's (hex) ^b .

^a Reads old RAM data the same as it is currently stored in the RAMs.
^b Writes new data into RAMs as 1's (binary).
^c A "1" on Bit 15 signifies Test Mode; a "0" means normal operation.

RAM Control. The graphics RAM Control circuit generates the row and column address strobes (RAS and CAS) for the RAMs, and it controls data output from the RAMs. The block consists of three custom array logic chips; see Figure 4-39. The first chip accepts control lines from the DCB bus and controls the other two chips. The second chip is the RAS and CAS generator; and the third chip is the write enable and output enable control logic for the RAMs. The third chip also provides the clock signal for the RAM Data-to-ALU Latch.

The RAS/CAS generator performs a two-fold function. During a screen refresh cycle, all RAS and CAS control lines are asserted, enabling 16 RAMs (one graphic word) simultaneously. (16-pixel words are read and loaded into the Graphics Shift Register during screen cycles). During a processor byte read or write operation, a certain combination of the RAS/CAS lines are used to select one of the 16 RAMs. However, a word write operation by the processor, causes all of the RAS and CAS lines to be asserted, thus performing a 16-pixel-at-a-time write.

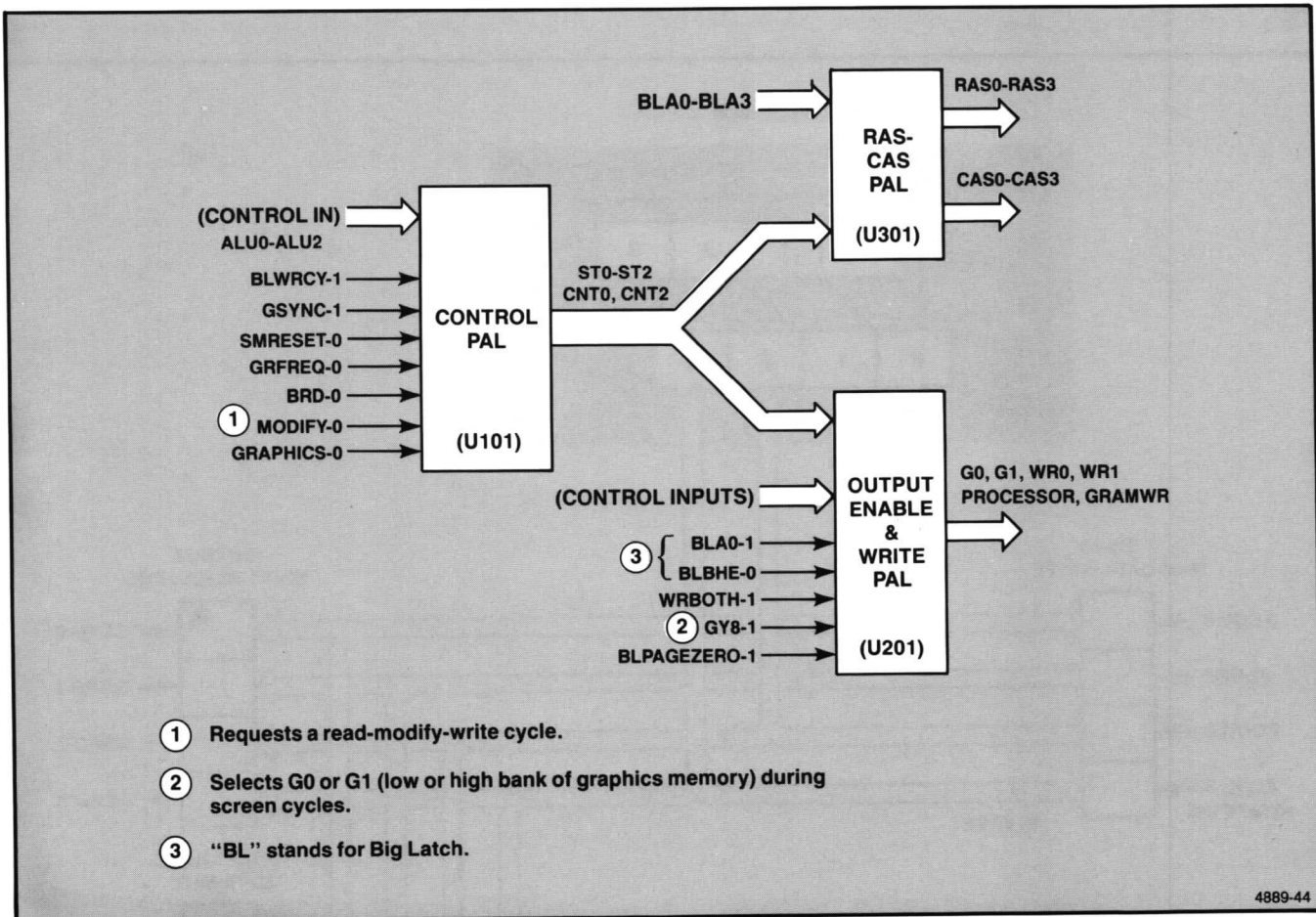


Figure 4-39. RAM Control Circuit.

Graphics Memory and Data Output

See Figure 4-40.

The 512K bytes of graphics memory is divided into four bit planes. Each of these memory planes contain these functional sub-blocks:

- 1-to-16 data input buffer
- RAM array (two 16K sections, divided into four bit-planes)
- Output data shift register
- 16-to-1 data output MUX

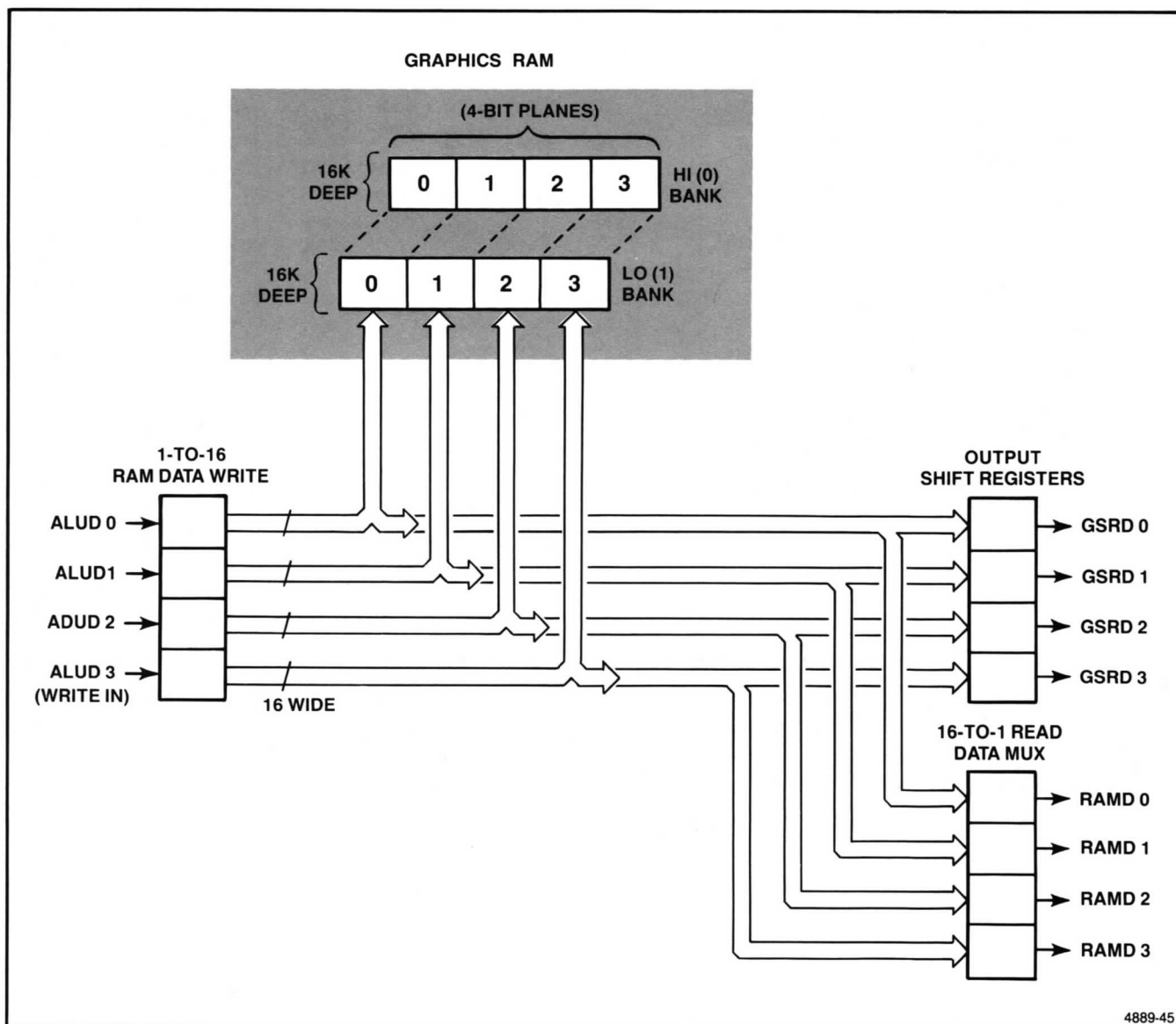


Figure 4-40. Graphics Memory Planes Block Diagram.

The graphics memory is organized as a “two-page” system; the read addresses are repeated in each page. This system is required because the upper half of the graphics RAM shares its address space with the system ROMs (firmware). When writing to the RAMs, you can use the entire address space because the ROMs are not enabled for writes. However, when reading these RAMs, the processor and display would have to distinguish between RAM and ROM in the upper (common) address space. Therefore, the lower RAM address space is duplicated and called page 0 and page 1. This region is 40000 to 7FFFF. The entire RAM write region is 40000 to BFFFF. The “page control” bit, in the Graphics Control Register, selects Page 0 or Page 1 for read operations. This 2-page addressing scheme is depicted in Figure 4-41.

A graphics word contains 16 pixels. Each pixel is individually addressable by the processor and consists of a 4-bit data byte. Thus, each RAM chip stores one of the 16 pixels in a graphics word. Also, each bit of a RAM is an element of a bit plane. The low order bits (00 to 0F) are Plane 0, up through the high order bits (30 to 3F) which are Plane 3.

The RAM address comes from the Graphics Memory Address MUX, described earlier in this section. The 4-bit outputs of the RAMs go to an output shift register (then, to the color map address MUX) as GSRD0 to GSRD3. RAM data is also read back to the ALU and processor (via the 16-to-1 MUX and a read data latch) during memory read operations.

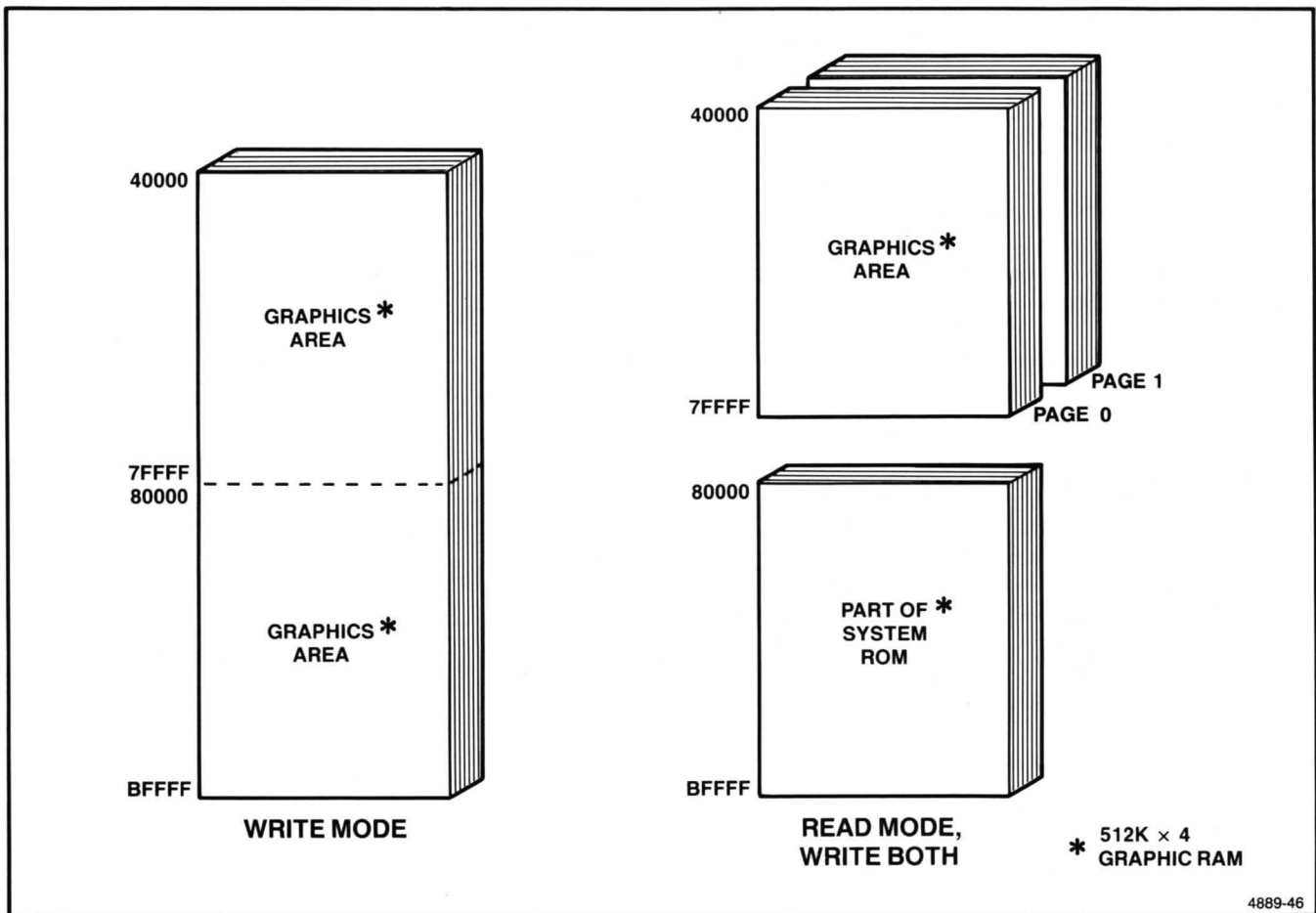


Figure 4-41. Two-page Memory System.

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1-to-16 RAM Data Write Buffers. RAM input data passes through a set of four 1-to-16 buffer sets. (Two 8-bit buffers, per set, provide the 1-to-16 bit extensions.) Only four data lines come from the ALU, but each RAM bank has 64 data ports. For this reason, each buffer takes an ALU output line and makes it into 16 separate RAM inputs. Consequently, the first buffer accepts the first output from the ALU, ALU0, and extends it into RAM data inputs 00 to 0F. Likewise, the second buffer extends ALU1 into inputs 10 to 1F, ALU2 supplies 20 to 2F, and ALU3 supplies 30 to 3F.

While a buffer is placing identical pixel data on all 16 inputs, the RAM RAS/CAS generator is selecting only one of these 16 RAMs for data input.

Low and High RAM Banks. The graphics memory is a 512K RAM array. Functionally, it is divided into four bit-planes, with each plane storing one bit per pixel. Looking at the schematic, this is not obvious. Each RAM chip in the array contains four bits per memory location; hence the four planes of graphics memory.

A more obvious feature of the RAM array is the two-page addressing system (already described). The schematic shows that the RAMs are split into two groups (the low and high banks) which corresponds to the two pages in memory address space. See Figure 4-41, again.

The RAM enables come from the Graphics System Control block.

Graphics Shift Register. The RAM output data must pass to the display in a serial stream. So this block converts the graphics output data from parallel to serial. The four 16-bit shift registers in this block convert the 16-bit words, from each of the four bit planes, to a serial data path. The four data streams are labeled GSRD0 to GSRD3. These data streams go through a pixel delay pipeline and on to the Color Map address MUX.

16-to-1 Data Read MUXes. One of the RAM output data paths is back to the ALU and processor read latch. The ALU and latch accept only four data lines, while the RAMs have 64 data ports. The 16-to-1 Data MUXes provide the function of merging these 64 data lines into the four ALU inputs. The MUX's switch positions are controlled by the BLD0 through BLD3 lines from the processor. The first MUX accepts RAM data lines 00 to 0F and makes RAMD0. The next MUX accepts data lines 10 to 1F and makes RAMD1. The other two MUXes operate the same; converting 20 to 2F into RAMD2, and converting 30 to 3F into RAMD3.

Graphics System Control Registers. See description under Alpha and Graphics Control Registers (Processor Interface), earlier in this section.

PIXEL PRIORITY CONTROL AND COLOR MAP SECTIONS

The Color Map and the Pixel Priority Control logic are grouped here into one superblock description.

The alpha and graphics data appear on different layers on the display screen. Depending on their pixel priorities, some images are in front of (and cover) others. The Pixel Priority Logic accepts operator input (via the processor and firmware) and display pixels of five different types, and it accordingly places these images on different layers on the screen. The priority and placement of these attributes are set by a pair of state machines in two programmed array logic (PAL) chips. The priority codes from the main attribute PAL, along with the alpha and graphics data, are MUXed together and sent to the Color Map. The Color Map then converts the combined pixel priority, graphics, and dialog information into standard RBG-encoded color signals for the Display Module.

This part of the DCB also contains some pipeline latches, that keep the alpha, graphics, and attribute data synchronized along their parallel paths to the Color Map.

Pixel Priority Control

Each dialog/alpha character in the display list is allocated two bytes of information. The first 8-bit byte addresses the character symbol in the Font ROM. The second 8-bits sets the attributes of the displayed character. Figure 4-42 shows this scheme. When the two most significant bits are a zero, the character appears opaque and on the front surface. The background and foreground each have 3-bit fields that contain an index value for selecting one of eight dialog colors. These indices are sent to the Color Map where the actual color selections occur. The combinations of attributes are logically arranged according to the two programmed array logic chips mentioned earlier.

The graphics images: crosshair cursor, and other stored patterns, also have certain display characteristics. The Pixel Decoder and Pixel Priority Control Logic PALs prioritize and merge the dialog and graphics images (with attributes), causing them to appear to be on different layers on the display screen.

Pixel Decoder. This 20L8A logic array accepts pixel priority requests from the alpha and graphics control registers (and 9007); it also accepts the identification code of the current character. The chip decodes and merges these request signals and sends its outputs to the Pixel Priority Control Logic PAL.

The inputs to this Pixel Decoder are:

- C0-1 through C7-1 Character code; used to generate EOLLOCK-1 signal when an end-of-line character is encountered.
- CURS-1 Cursor request signal; asserted by 9007 when the current character position coincides with the contents of the 9007's cursor position register.
- BLOCKCUR-1 Cursor mode select; when 0, selects underline cursor; when 1, selects full-cell cursor (not supported by firmware in this product).
- XPRNTENB-1 Transparent enable: when bit = 0, lets graphics be viewed behind dialog characters whose background index is 0. When bit = 1, the background of characters (with index = 0) becomes opaque, covering the graphics.
- SL0-1 through SL3-1 Scan line counter output from 9007; used to decide which lines to use for cursor underline and for underlined characters.
- UNDERLINE-1 Character attribute bit from character pipeline; when bit = 1, the current character is underlined.
- BG0-1 through BG2-1 Indicates the background color index attribute for current character. Used to generate SEEGRAPHICS-1 signal when XPRNTENB = 0 and the current character's background index is 0.

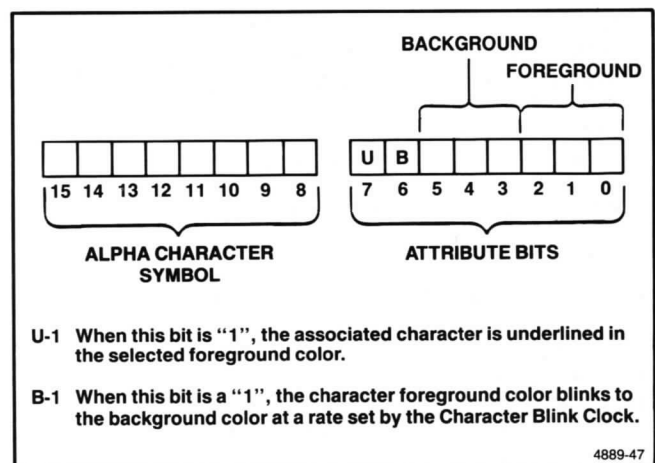


Figure 4-42. Byte Format.

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The outputs of this logic chip are:

- EOLLOCK 1 When an end-of-line character is encountered (character codes 80 and 90 Hex), this signal is generated, disabling the clock enable of the character pipeline stage (that follows the row buffers).
- CURSOR-1 Enables the alpha cursor.
- SEEGRAPHICS-1 Makes the dialog background transparent (index = 0), showing graphics.
- DOUNDERLINE-1 Enables the underline (part of alpha character cell).

Pixel Priority Control Logic. This block consists of a 20R8A programmed array logic chip. This state machine accepts pixels from five different sources and selects the correct source for the pixel being displayed. The priorities for pixels sources is:

1. Graphics crosshair cursor
2. Alpha cursor
3. Alpha foreground
4. Alpha background
5. Graphics

The PAL assesses the state of the current incoming pixel sources, selects one source according to the priority list, and enables the selected source to address its entry in the Color Map.

The pixel source selections are overridden by either: a processor access to the Color Map, or by display screen blanking intervals. (The processor has highest priority).

This PAL then selects one of eight 4-line inputs to the Color Map. These Color Map inputs come from:

- Processor (color map I/O)
- Crosshair cursor
- Alpha cursor background vs. foreground
- Retrace blanking
- Graphics data out
- Alpha character background vs. foreground
- (One is not used except for testing)

Each of the above items corresponds to one of this PAL's output control lines. These control lines switch/control the Map Address MUX.

The inputs to the PAL are:

- COLORMAPACCESS-0 Same as MAP I/O request from processor.
- ALPHAVIDEO-1 This is the serial alpha character stream coming from the Alpha Shift Register.
- PIPECBLANK-1 This shuts off video (makes a black screen). Pipelined version of the composite blanking signal from the 9007. Active during H Sync and V Sync intervals.
- ATTRTEST-1 Self Test control line for testing this PAL.
- XHAIR-1 This requests the crosshair cursor.
- DIALOGENB-0 This puts the window shade up, making dialog area visible. See NOTE, following this list.
- BLOCKCUR-1 This requests a full-cell block cursor, instead of the 2-line underline cursor. (Not used in this product.)
- CURBLNKCLK-1 This sets the blink rate for blinking cursor.
- CURSOR-1 Alpha cursor request signal.
- SEEGRAPHICS-1 This makes the dialog area transparent for alpha characters whose background index is 0.
- DOUNDERLINE-1 Requests underline-mode with alpha characters.
- BLNKCHAR-1 Enables character/cursor blink-mode.

This PAL is clocked by DOTCLK5.

NOTE

The dialog area scrolls up from the BOTTOM of the screen; when the shade is up, the dialog area covers the screen.

Delay Pipeline. This block adds the necessary pipeline delay to these signals:

- the attribute signals coming from the Dialog List
- the graphics pixels coming from the Graphics Memory (before they reach the color map's address MUX).

This circuit consists of two latch chips and part of a third one. The background and foreground signal groups pass through one alpha character delay and one pixel delay pipeline stage, while the graphics data passes through only one pixel rate stage. The CURSOR, SEEGRAPHICS, DOUNDERLINE, and BLINKCHAR signals also are pipelined just once. These pipeline latches are clocked by DOT-CLK5 (from the Dot Clocks circuit). The latches' outputs are permanently enabled. U657 operates at the character clock rate, while U655 operates at the pixel clock rate.

Dialog Window Shade. The Window Shade block determines the starting character row and the number of character lines for the dialog window shade as it appears on the display screen. This circuit consists of a control latch/register and a state-machine (programmed array logic) chip.

The latch receives two 5-bit words of control data (BLD0 through BLD4, and BLD8 through BLD12). The first five bits designates the screen location of the first visible character row. This is the top or starting point of the dialog window shade. The second five bits designates the number of visible character lines after the first line.

The two control words enter the data inputs (pins 2 to 11) of the custom state-machine. The WINCLK-1 signal (from the Timing Generator) clocks this chip. This clock pulse occurs when DRB and HSYNC coincide, outside the vertical retrace time; this phases the chip with the character rows until it reaches the last visible line. Then, during vertical retrace time WINCLK clocks rapidly; this resets the chip to its last state so it is ready for the next display frame. The chip outputs this information on its pin 16 (DIALOGENB-0). This signal is high until it reaches the first visible dialog line (top of window shade). Then it goes low until it reaches the last visible dialog line (bottom of window shade), after which it goes high again. This signal goes to the Attribute Control block.

VRESET initializes this chip to its first state.

Color Map Section

The Color Map works closely with several other blocks to translate dialog and graphics pixels into color encoded pixels for the color Display Module. The processor writes to the map and sets the color index values. The map then sends the translated pixel data to the display. The following blocks are part of the Color Map section and pass addresses and data to and from the map:

- Map Address MUX
- Pipeline
- Pixel Output Pipeline
- Map Data Read Back

Map Address MUX. Not counting the processor, there are six sources of addresses for the Color Map:

- Graphics cursor (crosshair)
- Blanking address (during CBLANK time)
- Alpha character foreground
- Alpha character background
- Graphics pixel data

This MUX circuit selects one of these address inputs for the Color Map. The outputs of the Pixel Priority Control PAL control the output enable inputs of a set of 74F240 buffers. These buffers are combined to form a 24-to-4 line MUX-equivalent; only one buffer is enabled at a time, according to the next pixel source to be selected. The outputs of these buffers provide the Color Map address for the corresponding pixel source.

Pipeline. This pipeline is a buffer that compensates for propagation delays in the address path to the Color Map. It is located between the Map Address MUX and the map.

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Color Map. The Color Map is a memory array that stores 32 words of 16-bit color-index information. Only the lower 12 bits of each word are used to store actual color codes. These 12 bits are divided into three 4-bit groups, as indicated in Figure 4-43. This illustration also shows how the map memory is divided into color index regions for: graphics, dialog background and foreground, cursor background and foreground, crosshair background and foreground, and blanking.

Figure 4-43 also shows that only half of the bits are used (2, 3, 6, 7, 10, 11) to control color gun levels, in the 4107 application. Each 2-bit group decodes into a four-level index; each index sets the output level on one of the three color guns in the Display Module. Table 4-7 defines this scheme.

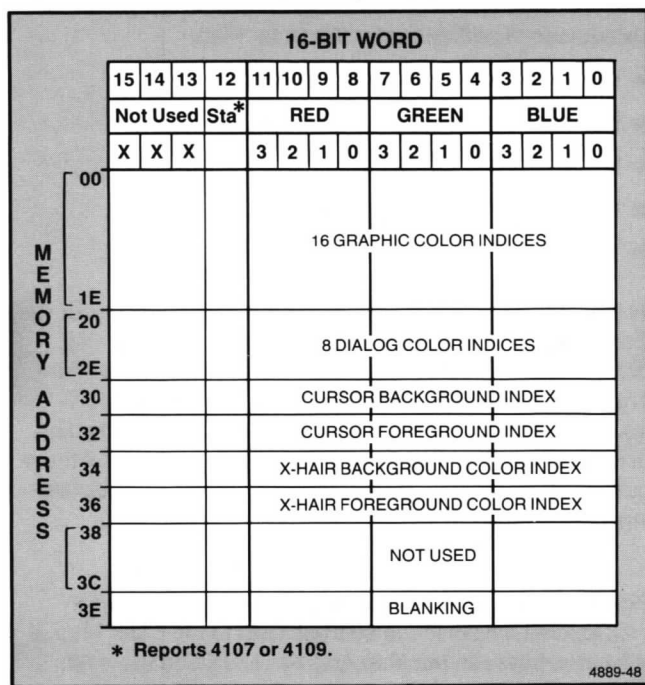


Figure 4-43. Color Map Organization.

Table 4-7
COLOR INDEXES

Index	Field Value	Gun Level
0	00	0%
1	01	7%
2	10	36%
3	11	100%

The extra, unused bits in the map, are used only in other applications of the DCB.

The Color Map hardware consists of an array of six 24 by 4-bit RAM chips. The processor writes index data to the RAMs via BLD0 to BLD11. The processor can also read map data over these lines. The RAMs are addressed via MAP0 to MAP3. MAP4-1 enables a read from the upper half of the map; MAP4-0 enables a read from the lower half of the map. MAPWR-0 is the write enable for the entire Color Map. The firmware uses bit-13 to prevent interference with the display image while map accesses are taking place.

Pixel Output Pipeline. Color Map output data passes through this pipeline before exiting on the output connector to the Display Module. This pipeline compensates for propagation delays, so the output pixel data and the sync signals both reach the display at the same time.

This block also provides the signal currents needed to drive the monitor interface circuitry in the Display Module.

Map Data Read Back. The processor reads Color Map data from the RAMs by looking at the contents of the Map Data Read Back latches. This pair of latch chips place Color Map data on bus lines BLD0 through BLD11. When the processor wants to read the Color Map, it sends an address to the graphics decoder. The decoder then sends a MAPIO and a BLWRCY signal; these signals are ANDed together to enable these output data latches.

An additional input to these buffers, YEP3-0, indicates the presence of the RAM3 board.

TIMING, SYNC, AND CLOCKS

This heading covers an assortment of blocks that make the timing signals for the many parts of the DCB.

Double-Wide Enable and Character Clock

This block generates the signals that tells the alpha shift-register to make double-wide (and double-high) alphanumeric characters. These DHDW control signals are SRMODE0 and SRMODE1. The block consists of a programmed array logic chip that combines several input conditions to make the two shift-register mode signals. (See Alpha Shift Register block description for details.) If the 9007's cursor signal occurs during HSYNC (horizontal sync time) then the array makes the proper combination of SRMODE0 and SRMODE1 to produce double-wide characters for the current character row.

This block also makes the character clock signal (CCLK-0), and the Word Delay Pipeline enable signal (ENBPIPE). CCLK is the alpha character clock that runs the 9007 and the character pipeline register. The ENBPIPE signal also clocks the 9006; it occurs once for every eight dot clocks, at the end of each character cell.

Timing Generator (and Signal Pipeline)

The Timing Generator is a programmed logic array that combines several time- and state-dependant signals to make more timing signals for other DCB circuit blocks. This block can be divided into three functional groups:

- The first part makes the HCLK and the VCLK signals. These clock the X and Y Address Counters (respectively). This part also makes the WINCLK signal, that clocks the Alpha Window Shade counter.
- The second part makes the TSC (Tri-State Control) signal that goes to the 9007.
- The third part of the chip makes the GY0 interlace-or-not signal that addresses the graphics memories. A divide-by-two flip-flop makes a signal that indicates (for interlaced mode) whether the display is showing the odd or even field. The flip-flop's inputs are PIPEVS-0 and HS-0. If HS-0 occurs at the beginning of PIPEVS, then an even field is displayed.

The gate array's GY0 tracks this input signal for 30 Hz interlaced mode. However, for non-interlaced mode, GY0 tracks the YDCGY0 signal (which is the least significant bit from the Y Position down-counter).

Signal Pipeline

This block is simply a pipeline latch for the input signals that go to the Timing Generator. The block performs a character delay on these signals: HS-0, VS-0, CBLANK-1, and CSYNC-0. The CBLANK signal exits on pin 19 and splits, where part of it is run through the latch to give it two delays. This twice-delayed CBLANK is AND gated with the original (undelayed) CBLANK to make the Composite Blanking signal for the Display Module.

Before entering the Pipeline, the VS-0 and HS-0 signals exit the 9007 and each passes through an AND gate that acts as a buffer/driver.

Dot Clocks and Buffers

This block generates the dot clock, that sets the rate of pixel data going through the DCB toward the display. This clock signal is used to clock and synchronize several other circuit blocks. A 25.2 MHz oscillator drives the circuit. The oscillator output enters a divide-by-two flip-flop. The resulting 12.6 MHz clock and the 25.2 MHz clock then enter a MUX that selects one or the other (depending on whether the DCB is in interlaced or non-interlaced mode). The INTERLACE-1 signal from the Alpha Control Register switches this MUX (actually three NAND gates and one inverter). The output of the MUX fans out into six identical signals called DOTCLK1 through DOTCLK6. These clocks are individually buffered and sent to different circuit blocks. Splitting the dot clock into separate lines, eliminates the following undesirable effects: line overloading, propagation delays, and line reflections.

RAM3 BOARD THEORY OF OPERATION

The RAM3 board provides 256K bytes of memory for storage of picture segment and display list information. This board is located just behind the Terminal Control board and connects to the DCB via a 96-pin DIN connector.

The address location of the RAM3 memory is split into two banks. The address of the lower 128K bytes is from 20000 to 3FFFF and the address of the upper 128K bytes is from C0000 to DFFFF. These two banks make up the 256K bytes

of auxiliary processor memory. Figure 4-44 shows the six blocks that make up the RAM3 board; these are:

- Board Control (address decoder)
- Data Output Latch
- Input Data Buffer
- RAM Controller
- Dynamic RAM
- Clock (oscillator)

The RAM3 board's circuit blocks are described next.

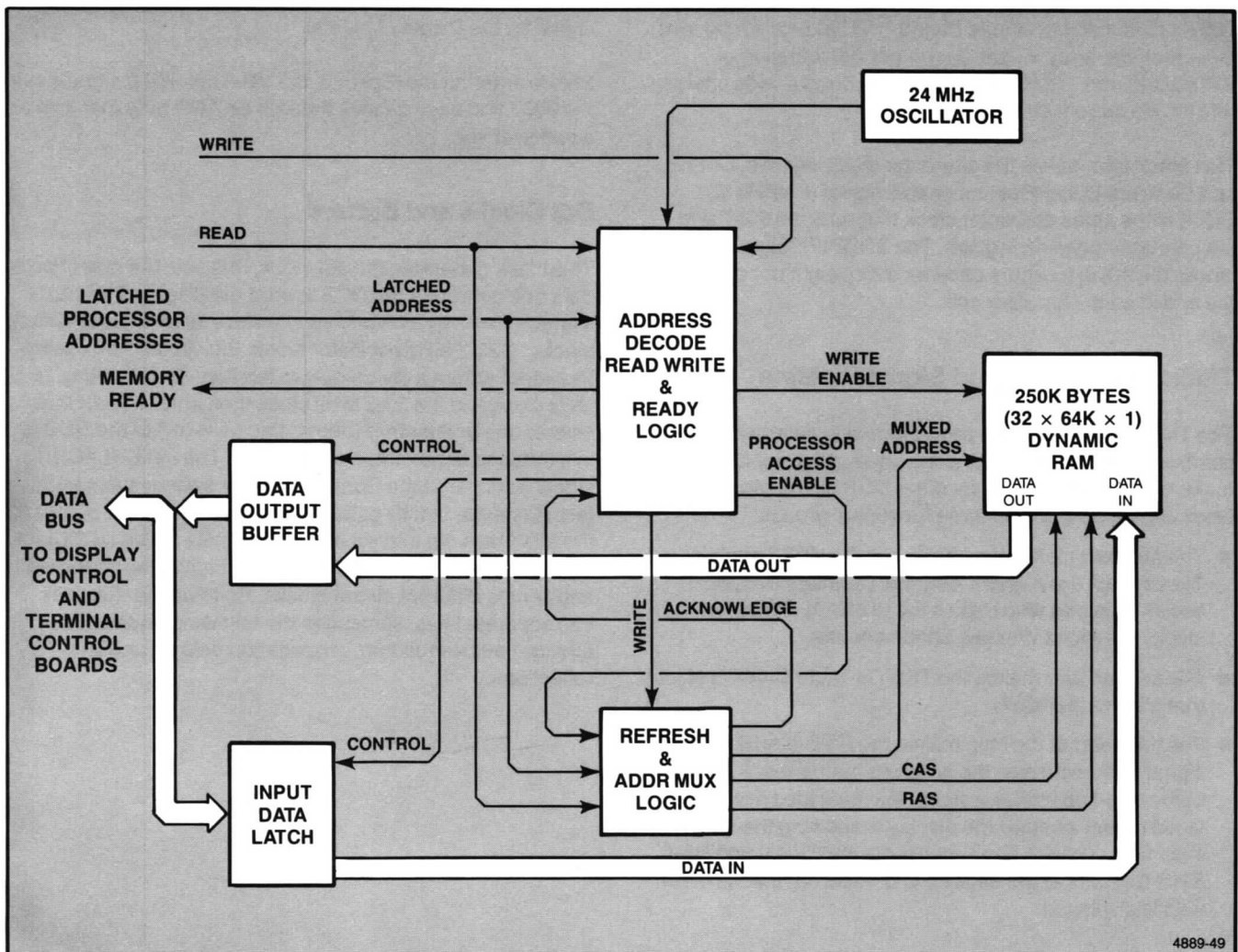


Figure 4-44. RAM3 Board Functional Block Diagram.

RAM ADDRESS DECODER

The PAL in this block decodes the A16 thru A19 and A0 lines, which controls the PCS line to the 8203 RAM Controller. The PAL also sends the ready signal (memory ready) to the processor. The write enable (WE) signal from the 8203 is combined with A0-1 and BHE-0 to generate the WEHI and WELO signals. The "write enable high" (WEHI) and the "write enable low" (WELO) signals, from this PAL, control which half (high byte or low byte) of memory is written by the processor.

DATA OUTPUT LATCHES

Data output from the RAMs on this board are latched by two 74LS373 chips, which are enabled by the control PAL. These chips latch the data onto the processor bus's 16 data lines (AD0 thru AD15).

INPUT DATA BUFFERS

These two 74LS244s buffer the 16 data bits from the processor data bus onto the memory data bus.

RAM CONTROLLER

This block multiplexes the RAM address lines and provides the RAM refresh signals. The 8203 RAM Controller performs the memory refresh operations needed to maintain the data in the dynamic memory devices. It performs these functions:

- Arbitrates between processor access cycles and refresh cycles
- Multiplexes the memory addresses
- Provides the memory control strobes (RAS, CAS, and WE)
- Generates the acknowledge signal used to latch memory read data into the output data latch
- Generates the READY handshake signal that signifies the completion of a memory operation.

RAM BLOCK

The memory on this board consists of 256K bytes of RAM in a 64K by 16-bit array. This functions as auxiliary memory to the processor.

CLOCK

The clock for the RAM3 board is a four-pin 24.0 MHz crystal oscillator requiring only a +5V supply.

POWER SUPPLY MODULE THEORY

The Power Supply Module supplies power to all other boards in the terminal. Without the Power Supply Module, the terminal cannot run. The board provides the the following voltages:

- + 21 Volts
- + 12 Volts
- -12 Volts
- + 5

If the + 5 volt supply rises to a value of + 6.25 volts (+ or - 0.50 volts), or if any of the current limits are exceeded, circuitry on the board senses this and shuts the power supply down.

The Power Supply Module consists of the following functional blocks:

- AC Power
- EMI Filtering
- Line Select
- Rectifier and Filter
- Kick Start
- Pulse Width Modulator (PWM)
- Base Drive
- Primary Snubber
- Housekeeping & Regenerative Drive
- Main Transformer
- Control Loop Sense and Drive
- + 21 Volt Outputs
- + 12 and -12 Volt Outputs
- + and -12 Volt Current Limit
- Over Voltage Protect
- + 5 Volt Output
- + 5 Volt Current Limit

Each of these blocks is discussed briefly in the first part of this section, and discussed more thoroughly later on.

OVERVIEW

The Power Supply Module is based on a discontinuous mode fly-back, high-efficiency, switching type design. This type of supply provides the advantages of lower weight, smaller volume, and reduction in size over conventional supplies. The principle of a switching supply is shown in the simplified drawing of Figure 4-45.

A switching supply uses a Pulse Width Modulator (PWM) to produce a signal with a given pulse width. The pulse width is varied by the PWM, to keep the supplies in regulation as line voltage and load fluctuates. The PWM is shown on Figure 4-45 as a controlled switch.

The transformer is switched on and off at a fixed rate (in this case, at 25 KHz). During the on time, energy is stored in the primary coil of the transformer. During the off time, this energy is released to the secondary, where a capacitor and diode are connected. During the off time of the secondary, the capacitor supplies the output voltage. The diode provides isolation of the two windings.

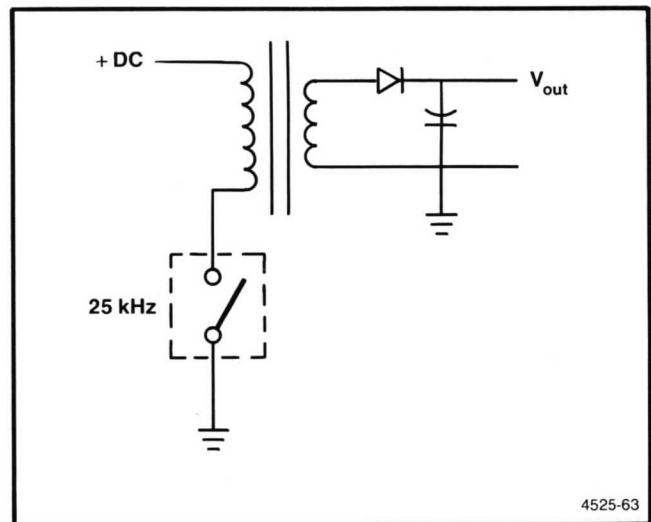


Figure 4-45. A Switching Supply.

Simplified Descriptions of Blocks

The following text gives a short and simplified description of each of the blocks shown in Figure 4-46. The next part of this section contains the more detailed descriptions of the circuit blocks.

AC Power. AC power acts as an input to the power supply (the AC Power Block).

EMI Filter. The EMI Filter block eliminates high frequency noise created by the switching of the power supply. This filter prevents such noise from flowing back into the AC lines.

Rectifier and Filter and Line Select. The Rectifier and Filter block rectifies the AC voltage to a high voltage DC signal (between 200 and 400 volts). The setting of the Line Select switches tells the Rectifier which of two methods to use to accomplish this.

Kick Start. The Kick Start is used to start the Pulse Width Modulator (PWM) when the power supply is first turned on.

Pulse Width Modulator (PWM). The PWM supplies a 25 KHz pulse used by the Base Drive block.

Housekeeping and Regenerative Drive, Base Drive, and Primary Snubber. Using the pulse supplied by the PWM, these blocks act together to chop the high voltage DC and deliver it to the primary coil of the Main Transformer.

Main Transformer. The Main Transformer transfers energy from the high voltage, line connected dc side, to the low voltage secondary side.

Voltages. The secondary transformer outputs are rectified to form the output voltages of the supply.

Over Voltage and Current Limit. These blocks sense if a voltage has risen excessively high, or if the current limit of the supply is exceeded, and breaks the control loop back to the PWM. This causes the supply to shut down.

Control Loop Sense and Drive. This block forms a feedback loop back to the PWM. The loop senses load and line variations, and adjusts the PWM pulse-width to keep the supplies in regulation. If current flow in the loop is broken, the supply shuts down.

**THEORY OF OPERATION
POWER SUPPLY**

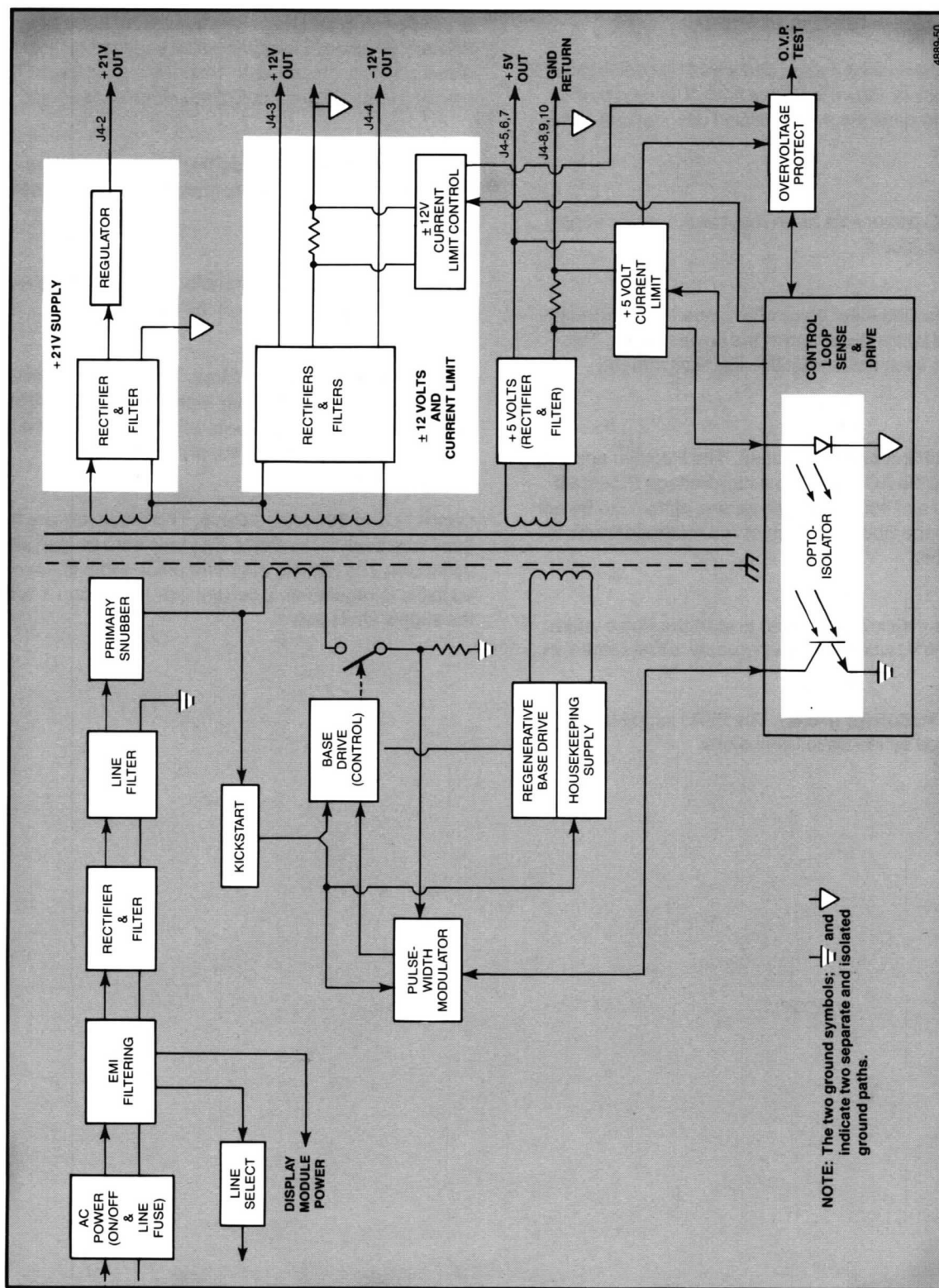


Figure 4-46. Power Supply Detailed Block Diagram.

DETAILED DESCRIPTIONS OF CIRCUIT BLOCKS

During the following discussion, refer to the Power Supply Module schematic, along with the block diagram. The block diagram shows how each block relates to one another, while the schematics are used when describing how each block functions.

AC Power

The AC Power section consists of the AC plug, a fuse, and the power switch.

AC power comes into the supply via a power cord connected to the AC plug. The power supply is protected by a 4A fuse and turned on by the power switch. The fuse is mounted on the power supply circuit board, and is not an externally accessible part.

EMI Filtering

The EMI filtering section is used to keep high frequency (Khz range and up) noise created by the switching of the supply from getting back onto the AC line. The filtering of this section does not affect the 60 Hz input signal, which is delivered to the Rectifier and Filter block. The EMI Filtering block consists of a thermal resistor, a series of capacitors and inductors, and two power resistors.

One of the inductors is a common-mode rejection transformer. This transformer has its two coils connected to opposite sides of the AC line, hence current is flowing in equal and opposite directions, creating a net flux of zero. When a high frequency signal enters this transformer, it meets a high opposing inductance. The signal then takes the alternate path (through the capacitors) to ground.

A thermistor limits surge current to the two main 100 μ f capacitors (in the Rectifier and Filter block) when power to the supply is first turned on. The thermistor then heats up, which lowers its resistance, while the supply is operating. The thermistor normally runs hot during operation of the supply.

Two power resistors, working with an energy storing capacitor, isolate the high frequency switching noise that is generated by the converter. This prevents such noise from going back into the AC line.

Line Select

The Line Select block consists of two switches. The setting of these switches depends on which AC input (115 or 230 volts) the supply is operating from.

CAUTION

The line select switches must both be set to the same setting. Failure to do this could result in damage to the power supply or the monitor.

One switch selects the AC input for the power supply, the other selects the input for the Display Module's degauss coil and its power supply. The setting of the line select switch determines if the diode bridge in the Rectifier and Filter block acts as a voltage doubler or a full-wave bridge (see the next block description).

Maintenance Test

This circuit limits the width of the PWM pulse when power is applied to the supply. This block consists of a transistor that is used to manually control the pulse width during testing/maintenance. This circuit allows you to manually control the voltage on pin 2 of the test connector (using a special test fixture).

Base Drive

The Base Drive block chops the primary voltage (+ 300 volts dc) to provide switching of the primary winding (pins 7 and 8) of the main transformer. This is accomplished by alternating a switching transistor between on and off states. The main components of this block are two transistors (the base drive and primary switching transistors), a series of diodes, and a capacitor.

The output pulse of the PWM is fed directly to the base of the base drive transistor, where it is used to turn on and off this transistor. When the base drive transistor is on, the switching transistor is off, and vice versa.

When the base drive transistor is off, its collector is high, causing current to flow through the three diodes and into the base of the primary switching transistor. At the same time, the Housekeeping and Regenerative drive also supplies current through the resistors, diodes, and into the base of the switching transistor. These two current supplies ensure that the switching transistor remains turned on. The voltage drop across the diodes is approximately 2 volts, which causes the capacitor to charge to + 2 volts.

When the base drive transistor turns on, its collector is pulled low. The capacitor now applies a negative two volts to the base of the switching transistor, ensuring fast turn off.

This cycle is repeated for each pulse from the PWM.

Primary Snubber

The Primary Snubber consists of two diodes, a capacitor, and a high wattage resistor.

When the primary switching transistor (in the Base Drive block) is starting to turn off, a voltage spike of up to a 800 volts or more occurs. This is the result of energy stored in primary leakage inductances. The snubber acts to steer current through the capacitor and diodes back into the primary (+ 300 volts) supply, preventing the high current from going through the switching transistor. After the transistor has completed turning off, the resistor rapidly discharges the capacitor, dissipating about 3 watts of power through the resistor.

Housekeeping and Regenerative Drive

This block forms a closed loop into the base drive block, and supplies drive for both halves of the transformer cycle (on and off times). The components of this block are a transformer winding, three diodes, a capacitor, and resistors.

When the primary switching transistor (in the Base Drive block) is turned on, pin 3 of the winding is polarized positive. This provides extra base drive current to the transistor, ensuring enough current to operate near the saturated region. When the switching transistor is turning off, pin 3 goes to ground.

The capacitor and diode connected to pin 2 delivers supply voltages to the Base Drive and PWM blocks. When the switching transistor is off, pin 2 is at approximately + 15 volts, and the capacitor charges. When pin 2 is low, the capacitor supplies the + 15 volts.

Main Transformer

The Main Transformer provides power from the primary to the secondary in order to develop the individual voltage supplies.

The Main Transformer is configured in a fly-back type of configuration. During the on time of the primary (as determined by the switching transistor), energy is stored in the primary coil. During the off time of the primary, this energy is released into the secondary coils. The energy released is filtered to become the individual voltage sources. A more thorough discussion of this process is covered at the beginning of this section.

Control Loop Sense and Drive

This block of circuitry forms a loop from the secondary windings of the transformer back to the PWM. When this loop is closed, the PWM is allowed to function. The loop senses the load on the supplies, and feeds back to the PWM, telling it to widen or narrow the PWM pulse width. When this loop is opened, such as when an overvoltage protect block opens it, the power supply shuts down. The primary components of this block are the opto-isolator, control regulator, capacitor, and a series of resistors.

As the + 5 volt supply is initialized (when the power supply is first turned on) the REF pin of the Control Regulator approaches + 2.5 volts. When the REF pin reaches + 2.5 volts, the Control Regulator turns on and begins to shunt excess drive current from opto-isolator. Current through the opto-isolator (which is held at a fixed value) feeds back to the PWM and maintains the PWM pulse-width. The current through the opto-isolator is modulated by the control regulator and varies with the load on the supplies. The opto-isolator current then adjusts PWM pulse-width accordingly to maintain regulation.

The cathode of the Control Regulator can be brought to ground by an over current or over voltage condition on the supplies. This stops current through the opto-isolator, breaking the control loop, and the power supply shuts down.

+ 21 Volt Output

Approximately 27 volts appears across the secondary winding of the main transformer. A series regulator chip then drops this voltage down and regulates it to + 21 volts, for use in the EPROMs. The main components in this block are three capacitors, two resistors, a diode, and the series regulating chip.

+ 12 and -12 Volts

When the secondary of the transformer is on, the diodes conduct and the capacitor charges. The output of the secondary is + 12 and -12 volts, which is delivered as the output voltages. When the secondary is off, the diodes are reversed biased, preventing discharge of the capacitor back into the transformer. The charge of the capacitor carries the supply through until the secondary is again turned on.

+ 12 and -12 Volt Current Limit

This block senses whether the current limit of the + or - 12 volt supplies is being exceeded. If so, this block causes the power supply to shut down (by breaking the loop formed in the Control Loop Sense and Drive block). This block consists of two transistors, resistors, and a diode.

If current through one of the + or - 12 volt capacitors is sensed by the resistor, one of the two transistors begins conducting (depending on which supply was sensed). This shunts drive current away from the opto-isolator and shuts down the supply.

Over-Voltage Protector

This block allows an over voltage (a runaway voltage) on the + 5 volt supply to shut down the power supply. The main components of this block are a Silicon Controller Rectifier (SCR), zener diode, capacitor, and resistors.

If the + 5 volt supply rises above + 5.6 volts, the zener diode turns on and begins conducting. When the zener has sourced enough current to raise it another 0.6 volts, the SCR turns on. This, in turn, pulls the cathode of the control regulator (in the Control Loop Sense and Drive block) to ground, no current goes through the opto-isolator, the control loop is broken, and the supply shuts down.

+ 5 Volt Output

The + 5 volt supply basically operates the same way as the + and 12 volt supplies. The capacitor charges during the on time of the secondary winding, and then supplies the output voltage when the transformer is off. The diodes provide isolation when the secondary has turned off. The remaining components in this block (capacitors, inductor, and a resistor) are used to filter out any noise created by the switching of the supply. Since this voltage is used for all of the TTL devices in the terminal, it is important that the supply be free of high frequency noise.

+ 5 Volt Current Limit

This block senses whether the + 5 Volt supply has exceeded the current limit. If this happens, this block causes the supply to shut down. The main components of this block are two transistors, a zener diode, and a sense resistor.

The + 12 volt supply is used to set the zener diode at + 10 volts. This provides a constant voltage for this circuit to use. Current flows down through the 10 Kohm resistor and turns on Q257. The voltage at the base of Q352 is set by the 330 ohm resistor. The current sense resistor is connected between the two emitters of the transistors. When the current through this resistor gets large enough, it raises the emitter of Q257 to a higher voltage. When this voltage plus the collector-emitter voltage of Q257 equals approximately + 0.65 volts, Q352 turns on. This shuts down the opto-isolator (no current flows), the control loop is broken, and the supply shuts down.

Section 5

CHECKS AND ADJUSTMENTS

This section describes the checks and adjustments for the 4107. The Display Module is the main analog part of the terminal and is the focus of attention in this section. (The Power Supply Module has no adjustments.)

The first part of this section lists the performance check procedures for the 4107. The remainder of the section deals with the adjustment procedures for the Display Module. These adjustment procedures require the use of certain display patterns. To put these patterns on the screen, go into the Adjustment part of Self Test and press certain Function Keys (see Table 5-2). Appendix C provides a complete description of Self Test.

PERFORMANCE VERIFICATION PROCEDURE

The performance/functional check procedure for the 4107 consists of running Self Test and Extended Self Test and verifying that no errors are found. Appendix C contains the complete description of the Self Test program, including operating information and error messages.

To perform the complete performance check procedure, you will also need certain test equipment and test fixtures. The luminance check requires use of a photometer, such as the TEKTRONIX J16 (with FtL probe). The display image size and linearity checks require use of a special calibration graticule. See NOTE below. Finally, the host-port, peripheral ports, and copier-port checks require use of special loopback connectors. See NOTE again.

NOTE

Contact a service representative at your nearest TEKTRONIX Field Office for information about acquiring these special test fixtures.

ADJUSTMENT PROCEDURES

This adjustment procedure first lists the test equipment that is needed to measure the adjustment parameters. Next, is a summary of the checks (and expected results) for the Display Module. And last, are the detailed procedures for performing the adjustments.

The following checks and adjustments require access to internal parts, so remove the terminal's cover as described in Section 6. Also, turn on the terminal and wait for a 5 minute warm-up before performing these checks and adjustments.

RECOMMENDED TEST EQUIPMENT

Table 5-1 lists the test equipment needed to check and adjust the 4107. The listed equipment specifications are the minimum required to perform these tests. If alternate equipment is used, it must meet or exceed this specification.

Table 5-1

RECOMMENDED TEST EQUIPMENT

Description of Equipment	Equipment Minimum Specification	Example
Oscilloscope (dual trace)	Vertical: 5 mV/div. Time base: 10 ns/div. 80 MHz	TEKTRONIX SC 504
Scope probe	10:1 attenuation	TEKTRONIX P6108
Digital Voltmeter	0 – 100V DC & AC (p-p) 0.1 % accuracy	TEKTRONIX DM 501
High Voltage Probe	20 kV	FLUKE Model 80K-40
Photometer and Luminance Probe	Capable of reading 100 ft-lamberts max	TEKTRONIX J16, with J6503 probe
Flat blade screwdriver	1/8 inch (10 inch long)	
Display graticule	Contains screen adjustment pattern	TEKTRONIX 067-1150-00
RTV silicon adhesive/sealant		Dow-Corning 3145

CHECKS AND ADJUSTMENTS

SUMMARY OF DISPLAY MODULE CHECKS

The following table of performance checks is extracted from the adjustment procedures. You may use this to validate the performance of the Display Module without doing the detailed adjustment procedure.

Table 5-2

SUMMARY OF DISPLAY MODULE CHECKS

Step	Check	Expected Result
1	TP1 – on Main Video board	+ 95 Volts
2	Power supply checks	See Table 5-3
3	High Voltage check	25 KV (+ /- 1000 V)
4	Grid bias, G1 (screen adjustment)	- 42 Volts (on connector A9)
5	Z-axis (color balance)	Red - 5, green - 13, blue - 2
6	Size check (coarse)	Pattern dimensions: 24 x 18 cm.
7	Focus	Visual
8	Purity (degauss)	Visual, is red pure?
9	Convergence	Visual, alignment of R,G,B
10	Vertical size	Pattern border: 180 mm
11	Horizontal size	Pattern border: 240 mm
12	Pin-cushion effect	Visual, square corners and rectangular screen pattern

DISPLAY MODULE ADJUSTMENT PROCEDURES

The checks and adjustments for the Display Module are covered in the following sequence:

- Display Module power supply adjustments
- High Voltage adjustment
- Horizontal and Vertical Hold adjustments
- Grid bias adjustment
- Z-axis adjustment
- Deflection coarse adjustment
- Focus adjustment
- Purity and coarse convergence adjustments
- Final convergence adjustment
- Vertical deflection adjustment
- Horizontal deflection adjustment
- Pin-cushion correction adjustment.

These checks and adjustments are listed as independent items; however, the success of these checks depends on performing them in the above sequence.

Table 5-3

SELF TEST ADJUSTMENT KEYS

Key Name	Key Function
F1	Reset Non-volatile Parameters
F2	Keyboard Switch Test
F3	RS-232 Interface Menu
F4	Hard Copy Menu
F5	Display Pattern Menu
F6	Graphics Tablet Test
F7	Exit the current menu
F8	Exit Self Test

Display Module Power Supply Adjustments

WARNING

Use extreme caution when performing this adjustment procedure. Lethal voltages are present on the Socket board and the High Voltage assembly on the Main Video board.

See Figure 5-1 for locations of test points. Use the CRT support frame for a ground point.

1. Check – The +95 V output at TP1 on the Main Video board.
2. Adjust – VR81, on top of the power supply enclosure, to give a reading a +95V +/- 2V on TP1 (Main Video board).
3. Check – Voltages and tolerances indicated in Table 5-4. No adjustments will be made here. These checks merely verify that the Display power supply is adjusted properly and main voltages are reaching principal destinations.

Table 5-4

DISPLAY MODULE POWER SUPPLY CHECKS

Nominal voltage	Test point	Range (tolerance)
+ 8.5 V	TP 6	+/-0.5 V
+ 20 V	TP 5	+/-2 V
-20 V	TP 4	+/-2 V
+ 58 V	TP 3	+/-2 V
+ 95 V	TP 1	+/-2 V
GRND	TP 2	

High Voltage Supply Adjustments

WARNING

Lethal voltages exist at the CRT anode button, and proper precaution must be taken to prevent injury.

NOTE

This check is not necessary if a complete adjustment was performed, a picture is present, and the adjustment checks were all within tolerance.

The high voltage anode button is located on top of the CRT, just under the rubber boot on the end of the high voltage cable.

1. Power down the 4107 and wait two minutes, allowing the high voltage to drain down.
2. With terminal power off, connect the Fluke high voltage probe to the CRT anode button.

WARNING

Be sure to connect the ground wire of the high voltage probe to a chassis ground before turning on power to the terminal.

3. Set the voltmeter to the 200 V scale and connect the high voltage probe to the meter.
4. Power up the terminal.
5. Set 4107's BRIGHTNESS control to make the screen black.
6. Check – high voltage. It should read: 25 kV +/-1000 V.

NOTE

If this reading does not match the specification, replace the Main Video board. If replacing this board does not cure the problem, replace the CRT.

Horizontal and Vertical Hold Adjustments

This procedure requires use of the Self Test Grid Pattern. Run Self Test; from the main menu, select F6 (Adjustment Menu). Table 5-5 defines operation of the Display Pattern function keys.

The horizontal hold procedure is first, followed by vertical hold. Figure 5-1 shows the locations of the horizontal and vertical hold adjustments, R516 (labeled 'O' in figure) and R407 (labeled 'I').

1. From the main Adjustment Menu (in Self Test), press Function Key F5, Display Pattern Menu. Then press Function Key F1; this displays the 'grid pattern'.
2. Adjust – R516 ('H HOLD' on the Main Video board) clockwise until sync is lost, and note the position of the potentiometer.
3. Adjust – R516 counterclockwise until sync is lost, and note this second position of the potentiometer.
4. Adjust – R516 between these two positions and center the grid pattern horizontally on the screen.

Or, place the alignment graticule over the screen, and align the displayed grid pattern with the alignment graticule.
5. Adjust – R407 (V HOLD) clockwise until sync is lost, and note the position of the potentiometer.
6. Adjust – R407 counter-clockwise until sync is lost, and note this second position of the potentiometer.
7. Center the potentiometer between these two positions, or center it between breakup and the opposing end of the pot adjustment.

**Table 5-5
DISPLAY PATTERN MENU**

Key Name	Key Function
F1	Calls Grid Pattern.
F2	Calls Gray Scale Pattern.
F3	Calls White Screen Pattern.
F4	Calls Color Pattern.
F5	Calls 'H' Pattern.
F6	Calls Crosshair Pattern.
Shifted F1	Sets video amplifier to 0 level.
Shifted F2	Sets video amplifier to maximum level.
Shifted F3	Calls Dot Pattern
Dialog key	Toggles red video on and off.
Setup key	Toggles green video on and off.
SCopy key	Toggles blue video on and off.
Shifted Dialog key	Increments the red intensity level.
Shifted Setup key	Increments the green intensity level.
Shifted SCopy key	Increments the blue intensity level.
Menu	Turns menu (dialog) on or off.
F7	Exits back to Adjustments Menu.
F8	Exits Self Test.

Grid Bias Check and Adjustment

The following procedure is relatively complicated. Therefore, first read through the procedure while referring to Figure 5-2, to see the entire process in perspective. Then, go back and perform the procedure step-by-step.

Also, this procedure uses generic terminology, calling colors "first color," "second color," etc., instead of red, green, blue. This is required because there is no predetermined order in which colors will appear. A parallel example, in Table 5-6 at the end of this procedure, explains the process in simplified but concrete terms (i.e., red, green, blue).

- Power up the 4107, run Adjustment Self Test, and call the Display Pattern Menu (F5). Display a black screen by turning off all three guns; toggle these Function Keys to turn off the three guns:
 - Dialog (to turn off red gun)
 - Setup (to turn off green gun)
 - SCopy (to turn off blue gun).
- The "sub-brightness" control is R554 (see 'R' call-out in Figure 5-1), located on the Main Video board. Using a long screwdriver, turn the "sub-brightness" control fully counter-clockwise (to minimum value).

WARNING

Lethal voltages are present on the Socket board. Exercise caution while performing the following steps.

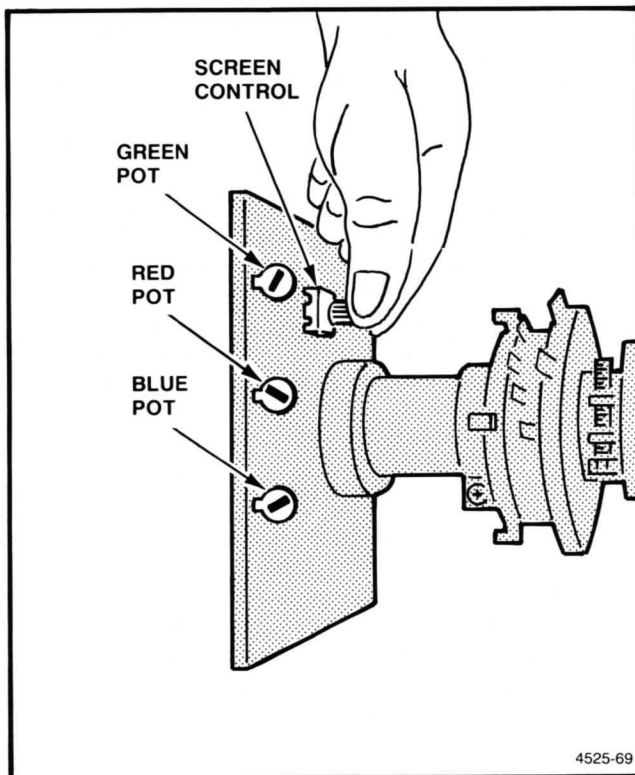


Figure 5-2. Grid Bias Adjustment Locations.

- The "screen" control is a hand-adjustable potentiometer, R372 (labeled 'K' in Figure 5-1). This control is located on the Socket board. Use fingers to turn the knob on this control fully clockwise (to minimum value).
- With screwdriver adjust all the "low light" potentiometers to full clockwise. These pots are labeled R348, R338, and R358, and are located across the top of the Socket board. See 'J', 'L', and 'M' on Figure 5-1.
- Connect the digital voltmeter's ground cable to the chassis, and place the meter's voltage probe so it makes electrical contact with red wire entering the top of connector A9. See Figure 5-3.
- Adjust the "sub-brightness" control, R554, to give a meter reading of -37 V (G1 value).

The adjustments up to this point are placing the color guns in a known minimum state.

¹ "Screen" refers to the CRT screen grid; not the display screen.

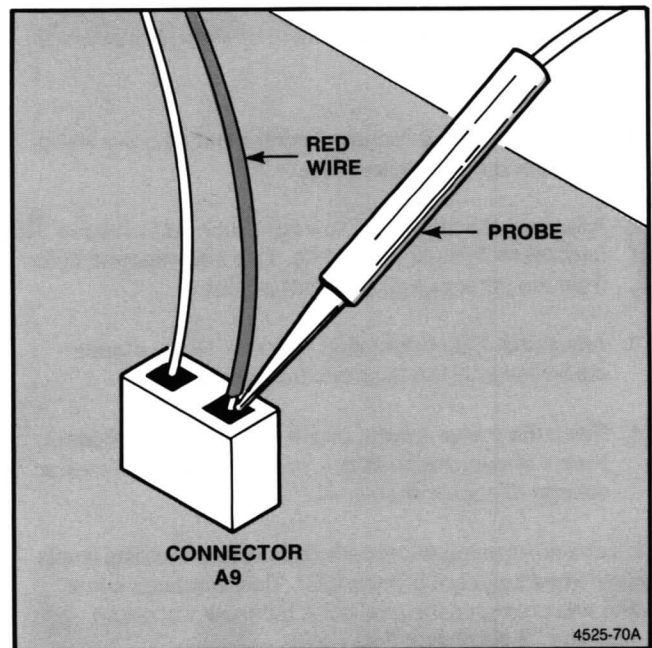


Figure 5-3. Obtaining G1 Voltage from Connector A9.

CHECKS AND ADJUSTMENTS

- Now, adjust the "screen" control, R372, counter-clockwise until the first color just appears as a faint line along the vertical edges of the screen. Ignore the white cursor.

NOTE

Use a notepad or other light-shade over the CRT screen to eliminate reflections. This makes it easier to see the faint colors written on the screen.

- Then, adjust the first color's "low light" control counter-clockwise until that color just disappears. (Note: if the first color to appear is red, then adjust the low light pot labeled "R338.")
- Next, adjust the "screen" control until the second color shows along the edges of the screen.
- Turn the "low light" pot, for the second color, counter-clockwise until that color just disappears.

NOTE

If any of the first colors reappear, adjust the corresponding pot(s) counter-clockwise until they also disappear.

- Finally, adjust the "screen" control until the last (third) color becomes barely visible.
- Adjust up the other two "low light" controls until the faint raster lines appear white. This adds enough color from the other two guns to make white.
- Adjust the "sub-brightness" control, R554, counter-clockwise until the faint raster is just cut off.
- Place the meter voltage probe on connector A9 (as in Step 5 above) and read the meter. It should indicate a voltage of approximately -42 V.

This check/adjustment procedure balances the bias levels on the three color grids in the CRT. This produces a true white and precedes the final color balance procedure (under the "Z-Axis" heading, next).

Table 5-6

SAMPLE GRID-BIAS ADJUSTMENT

Step	Procedure
1	Set all adjustments to min.: R554 full CCW ^a R372 full CW R338, R358, R348 full CW.
2	Set R554 so G1 reads -37 V.
3	Adjust R372 CCW until faint red line appears.
4	Adjust red pot (R338) CCW til red disappears.
5	Adjust R372 CCW until faint green line appears.
6	Adjust green pot (R348) CCW til green disappears.
7	Adjust R372 CCW until faint blue line appears.
8	Adjust R338 and R348 CW to make faint raster white.
9	Adjust R554 CCW til raster is just cut off. G1 voltage at A9 will read approx -42 V.

^a CW means clockwise. CCW means counter-clockwise.

Z-Axis Adjustment

This procedure pertains to the "Z-Axis" or "white balance" adjustments. In color video technology Z-axis refers to the white (vs. chroma) part of the video signal. So the Z-axis adjustments establish the white color balance, independent of brightness or saturation. (Saturation is the amount of white mixed with hue.)

In this procedure you will set the three (R,G,B) gain controls to their center positions. Then, using the Gray Scale Pattern (key F2), adjust each of these controls to the threshold of "blooming." (See NOTE.) Then you will use a photometer to check the relative intensities of red, green, and blue. The R,G,B controls are then adjusted to yield the standard color mixture ratio: red - 5 (25%) green - 13 (65%) blue - 2 (10%).

NOTE

"Blooming" is caused by overdriving one of the video amplifiers (R, G, B) into saturation. This results in one of the three colors dominating the screen image. Blooming is easily recognized by turning the front panel BRIGHTNESS control to maximum, and observing the the effect on the right-hand edges of the gray blocks of the Gray Scale Pattern.

1. The color gain potentiometers are:
 - Red gain – R301 (indicated by 'D' in Figure 5-1)
 - Green gain – R311 (indicated by 'E')
 - Blue gain – R321 (indicated by 'F').

Adjust each of these potentiometers so the control knob is centered between the CW and CCW limits of adjustment.
2. Turn the front panel's BRIGHTNESS control to maximum (CW).
3. Enter Adjustment Self Test and put up the Gray Scale Pattern: First, press F5 (calls the Display Pattern menu), then press F2 (calls Gray Scale Pattern).
4. Adjust the red gain (R301) up until blooming begins to show on the screen. Then back off on R301 until this red blooming just disappears.
5. Adjust the green gain (R311) until green blooming appears; then adjust R311 back until this blooming just disappears.
6. Adjust the blue gain (R321) until blue blooming appears; then adjust R321 back until blooming just disappears.

The following steps determine the reference color that is used to adjust the color balance between the three colors.

7. Press the F3 key; this makes the screen all white. Place the photometer head against the CRT screen. Read and record the indicated intensity value (in foot-lamberts).
8. Press the Dialog and SCopy keys; this turns off the red and blue guns, filling the screen with green. Using the photometer, record the green intensity value.
9. Press the Setup and SCopy keys; this turns off green and makes the screen blue. Using the photometer, record the blue intensity value.

10. Press the Dialog and SCopy keys; this turns off blue (makes the screen red.) Using the photometer again, read and record this value.
11. Perform calculations as follows:
 - a. Divide the recorded green intensity value by 13.
 - b. Divide the recorded blue intensity value by 2.
 - c. Divide the recorded red intensity value by 5.
 - d. Compare the three numbers; the lowest number indicates the "reference color." See example, Table 5-7.
12. Fill the screen with the reference color. Using the photometer, adjust the front panel BRIGHTNESS control so the reference color intensity measures the same as the ratio number for that color (green-13, blue-2, or red-5).
13. Fill the screen with one of the other two colors. Using the photometer, again, adjust the GAIN control for this color so the indicated intensity matches that color's ratio number.
14. Fill the screen with the remaining color. Read the photometer and adjust the GAIN control for that color to its ratio number, as with the other two.
15. Check each color for its proper reading: 13 – green, 2 – blue, 5 – red.

Table 5-7

SAMPLE COLOR BALANCE EXERCISE

Photometer Readings	Color Ratio Numbers	Readings Divided by Ratio Numbers ^a	Lowest Number
Green = 39	13	3	
Blue = 6.2	2	3.1	
Red = 11.5	5	2.3	<-

^a Calculations: $39 / 13 = 3$, $6.2 / 2 = 3.1$, $11.5 / 5 = 2.3$

CHECKS AND ADJUSTMENTS

Deflection, Coarse Adjustment

This procedure is the coarse adjustment of vertical and horizontal deflection. The fine adjustments for deflection come later. If necessary, this coarse adjustment precedes the focus, purity, and convergence adjustments.

1. Fill the screen with the grid pattern: From Adjustment Self Test, first press Function key F5; then press Function key F1.
2. Install the graticule over the display screen.
3. Check – to see if the borders of the displayed pattern are approximately 24 by 18 centimeters.

If the pattern is approximately this size, skip the rest of this procedure and go to the Focus and Purity adjustments.

4. See Figure 5-4A. If the vertical height of the pattern is less than 18 cm., adjust R426 CW (clockwise). R426 is labeled 'H' in Figure 5-1.

If the vertical height is greater than 18 cm., adjust R426 CCW (counter-clockwise).

5. See Figure 5-4B. If the horizontal dimension of the test pattern is less than 24 cm., adjust L553 CCW. (Use a plastic hex-driver to adjust the core of this variable inductor.)

If the horizontal dimension is greater than 24 cm., adjust L553 clockwise.

6. Remove the graticule from the screen.

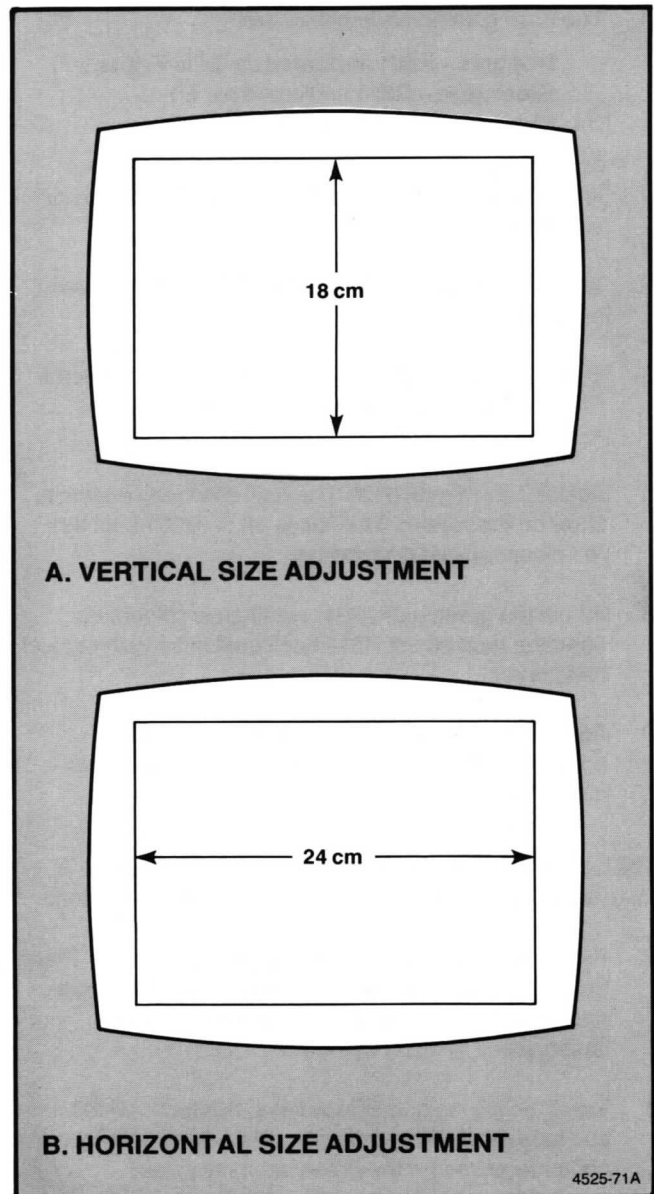


Figure 5-4. Coarse Deflection Adjustments.

Focus Adjustment

WARNING

Use extreme caution when performing this adjustment. Lethal voltages are present on the Socket board and on the High Voltage assembly (on the Main Video board).

The focus adjustment is a simple one step procedure. The control device for focus is located on the back of the high voltage assembly, mounted on the Main Video board. This control is labeled FOCUS and is called out as 'N' on Figure 5-1.

With power on and Self Test active, place the "H pattern" on the screen. Then carefully reach into the area between the Terminal Control board and the High Voltage assembly, and grasp the FOCUS control knob. Rotate the FOCUS control knob back and forth, while viewing the screen. Adjust this control to achieve the best overall screen focus when viewing the displayed pattern. This is purely a visual check (not measurable). Also, display some alpha characters on the screen and verify that the focus remains good.

This completes the focus check and adjustment.

Purity and Coarse Convergence Adjustments

Continuing with power on and Self Test active, place a red field on the screen (press Dialog Key). Check for a pure red screen (absence of other hues). If color is not pure, continue with this procedure. Otherwise, go to the Final Convergence procedure, next.

Purity adjustment:

1. Turn power off, wait awhile, and turn power back on.² This automatically degausses the CRT. If this is not sufficient to fully degauss the CRT, proceed. Call Self Test again, and obtain red field.
2. Place an external degaussing coil next to the CRT. Energize the coil and move over and around the CRT, in circular motions both directions. Now slowly move the coil away from the front of the CRT. At a distance of 8 to 10 feet, turn off the coil.
3. Examine the red field and evaluate the purity. Was the degaussing procedure sufficient to make a pure field? If not, repeat step 2 until purity is obtained.

If this procedure does not produce purity, replace the CRT. (See CRT replacement procedure in Section 6).

Coarse convergence adjustment:

4. Turn off the terminal.
5. Remove the Display Control board.

² Leaving power off 20 minutes allows the thermistor to cool off. Otherwise, on-off-on does not degauss.

CHECKS AND ADJUSTMENTS

6. Loosen the deflection yoke (unscrew the clamp) just enough to let it slide toward the rear on the CRT neck (see Figure 5-5).
7. Free the wedges from the front of the yoke.
8. Use a sharp knife to remove paint from the purity and convergence rings. This allows you to rotate them.
9. Install the Display Control board in the terminal.
10. Power up the terminal, and place a red field on the screen.

WARNING

Use extreme care in the following steps. Lethal voltages are present in the adjustment area.

11. Adjust the purity rings to obtain the purest red "ball" in the center of the display. See Figure 5-5, again.
12. Slowly move the yoke forward until the most uniform and pure red field is obtained over the entire screen. Examine the field with a hand magnifier and readjust the yoke and purity rings slightly for best red "beam landing" (least illumination of the blue and green phosphor dots by the red beam).

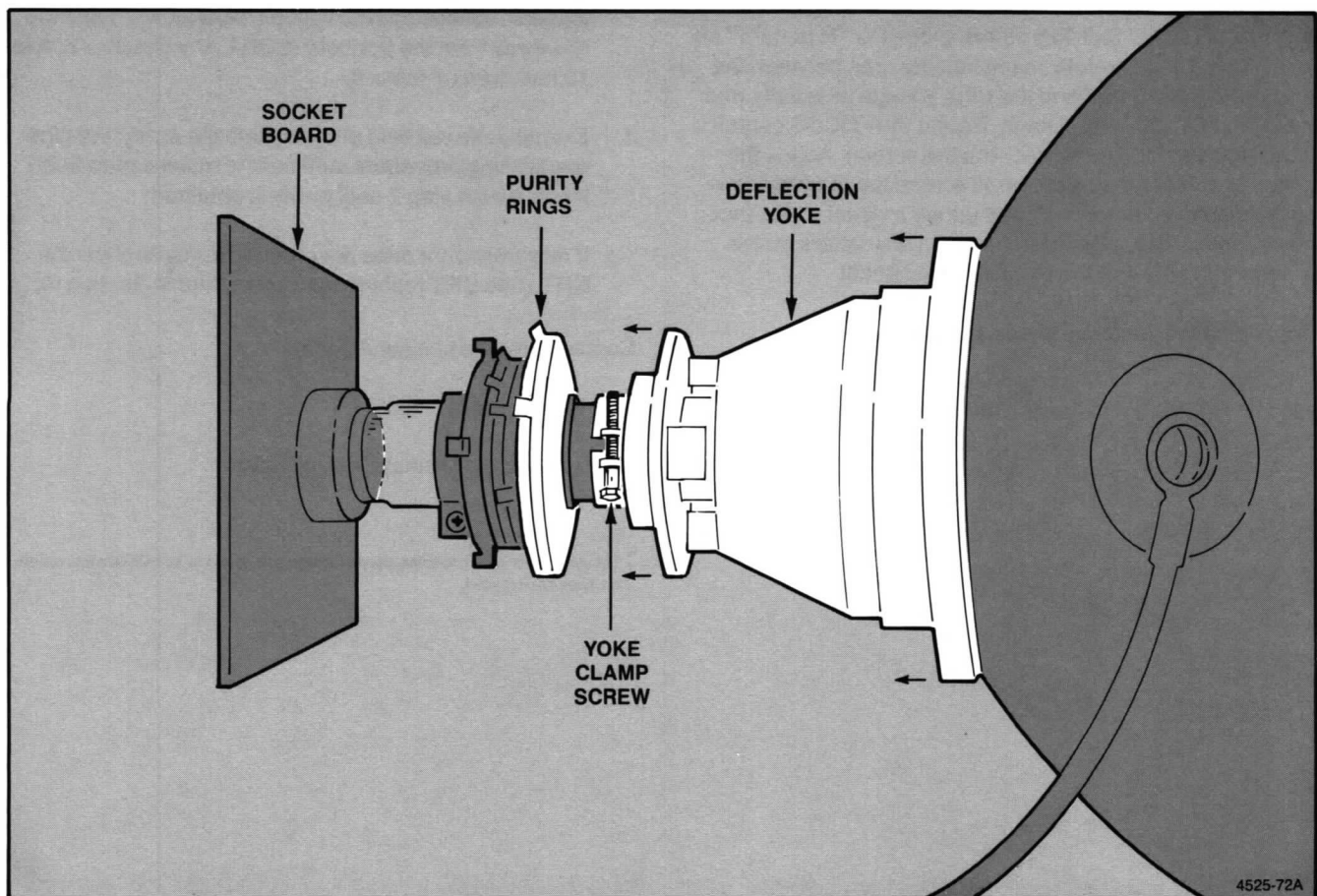


Figure 5-5. Yoke Clamping Screw and Purity Rings.

13. Tilting the yoke left-right or up-down affects convergence. Using the top two wedges, position the yoke to achieve the best overall convergence. (See NOTE.) Use RTV silicon compound to secure the wedges in position. See Figure 5-6.

14. Turn the terminal power off, and remove the Display Control board.
15. Tighten the yoke clamp (loosened in Step 6) and install the lower wedge. This completes the purity and coarse convergence procedure.

NOTE

Insert the wedges between the yoke and the CRT funnel, with the adhesive side touching the CRT. The adhesive will stick to the CRT. The wedges are placed 120 degrees apart; two on the top, and one on the bottom. See that the opening of the yoke is equidistant from the CRT all around the funnel (see Figure 5-6).

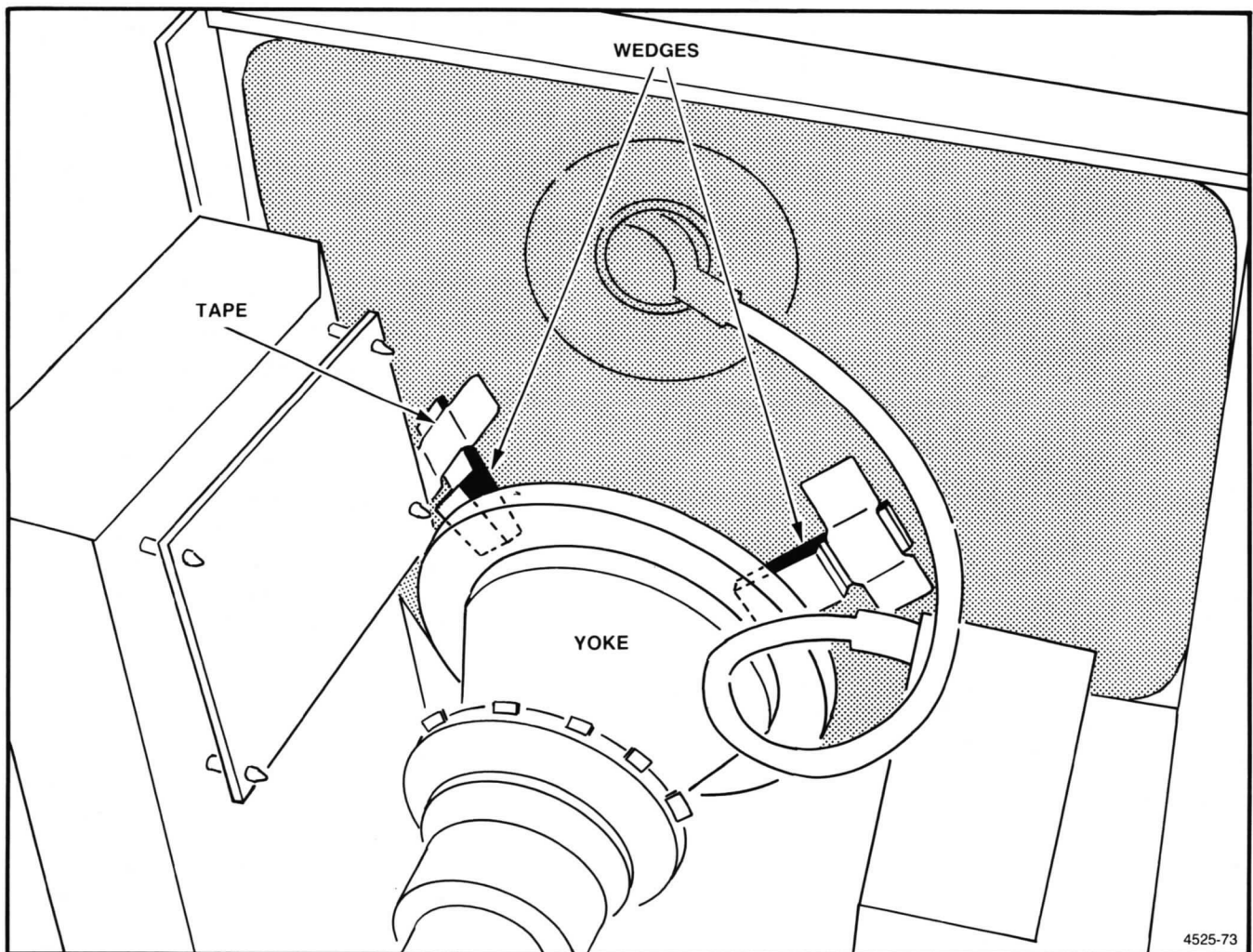


Figure 5-6. Placing Wedges between Yoke and CRT Funnel.

CHECKS AND ADJUSTMENTS

Final Convergence Adjustment

Before adjusting for Final Convergence, do the Purity and Coarse Convergence procedure (immediately preceding this adjustment).

1. Run Self Test and display the grid pattern.
2. Using the grid pattern (F1), check the convergence over the entire screen.

NOTE

The convergence specification is 0.4 mm between red and green, and between green and blue (over the entire screen). See Figure 5-7.

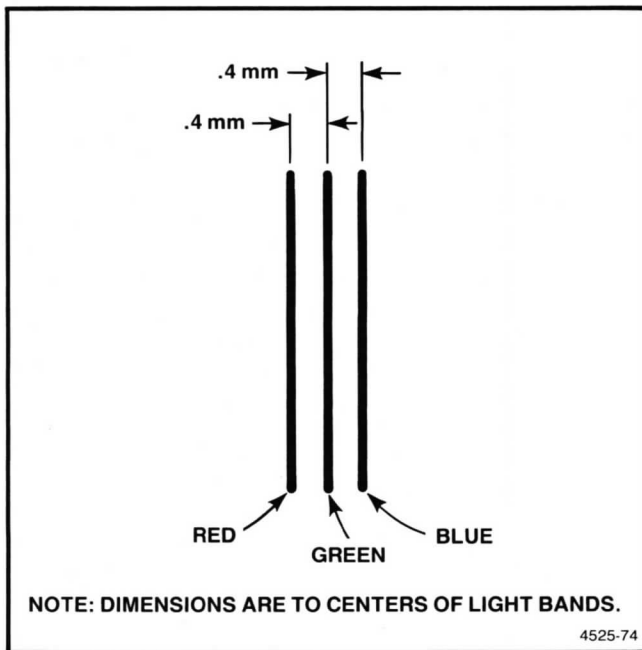


Figure 5-7. Measuring Convergence.

3. If convergence meets the specification, go to the vertical deflection adjustment. Otherwise, proceed to adjust the convergence.
4. Press the Setup key; this turns off the green gun (leaving only the red and blue guns on).

NOTE

Scrape off the paint that fastens the rings to each other. Then loosen the threaded gray clamp-ring (Figure 5-8) to allow smooth movement of the convergence rings.

5. Match the red and blue images at the center of the screen by rotating the four-pole magnet (the center pair of convergence rings, on the neck of the CRT). See Figure 5-8.
6. Turn on the green gun (press Setup key).
7. Match up the red, green, and blue images at the center of the screen, by rotating the six-pole magnet (rear pair of rings).
8. If necessary, nudge the yoke from side to side to achieve the best overall convergence on the whole screen. Secure the yoke in the optimum position by pressing in the wedges and tightening the yoke fastening screw.

CAUTION

In the following step, **DO NOT** place the tape-magnets closer than 20 mm from the HV anode cap. And do not tape them over paper labels.

9. If the convergence on the fringe areas is not acceptable, place one or more thin tape-magnets around the funnel to achieve the best effect. Then, press these magnets onto the funnel. Verify convergence around all edges of screen.
10. Check – purity. If purity was adversely affected by this procedure, redo the purity adjustment. If you must adjust purity, recheck convergence when finished.
11. Retighten the gray clamp-ring in Figure 5-8.

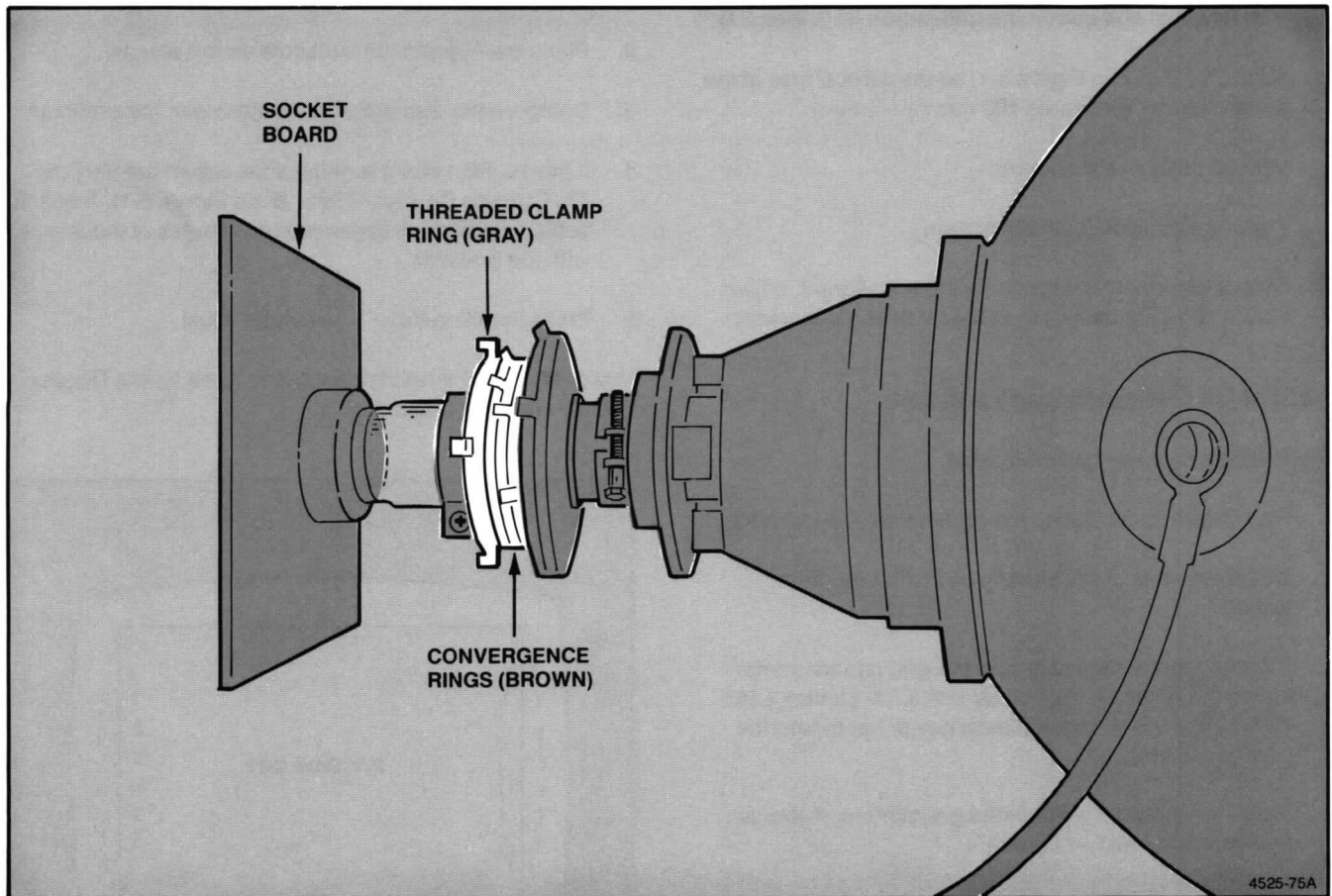


Figure 5-8. Convergence Rings and Threaded Clamp-Ring.

CHECKS AND ADJUSTMENTS

Vertical Deflection Adjustment

This is a final check and adjustment of vertical deflection (or vertical size) and vertical position.

Vertical deflection adjustment:

1. Run Self Test and call up the grid pattern (F5, then F1).
2. Adjust R426 ('H' in Figure 5-1) so the vertical size of the pattern border measures 180 mm (+/-2 mm).

Vertical position adjustment:

3. Place the graticule over the screen.
4. If the grid pattern and graticule are not aligned, adjust R420 ('G' in Figure 5-1) to achieve vertical alignment.

Horizontal Deflection Adjustment

This is a final check of horizontal size.

1. Run Self Test and call up the grid pattern (F5, then F1).
2. Install graticule, if not already on the screen from last test.
3. If the horizontal dimensions of the grid pattern do not match the graticule, adjust the H WIDTH control, L555 ('Q' in Figure 5-1). Use a plastic hex driver to turn the core of this inductor.
4. Check – horizontal width of the grid pattern. It should measure 240 mm (+/-2 mm).
5. If the grid pattern and graticule are not aligned horizontally, adjust the H POSI control, R566 ('P' in Figure 5-1), to reposition and center the pattern horizontally.

Pin-Cushion Adjustment

Pin-cushion effect is shown in Figure 5-9. This amounts to either a shrinking or bulging of the sides of the displayed image.

1. Run Self Test and call up the grid pattern.
2. Place the Adjustment Graticule on the screen.
3. Compare the displayed grid pattern with the graticule.
4. If pin-cushion effect is noticeable, adjust the Vertical Pin Cushion Control, R754 ('B' on Figure 5-1). Adjust to achieve maximum alignment of the sides of the image with the graticule.
5. Press Function Key F8, to exit Self Test.

This completes the adjustment procedures for the Display Module and for the terminal.

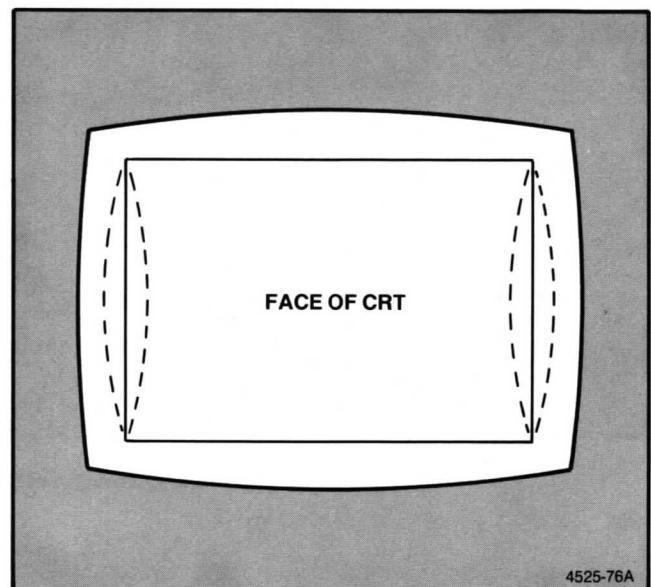
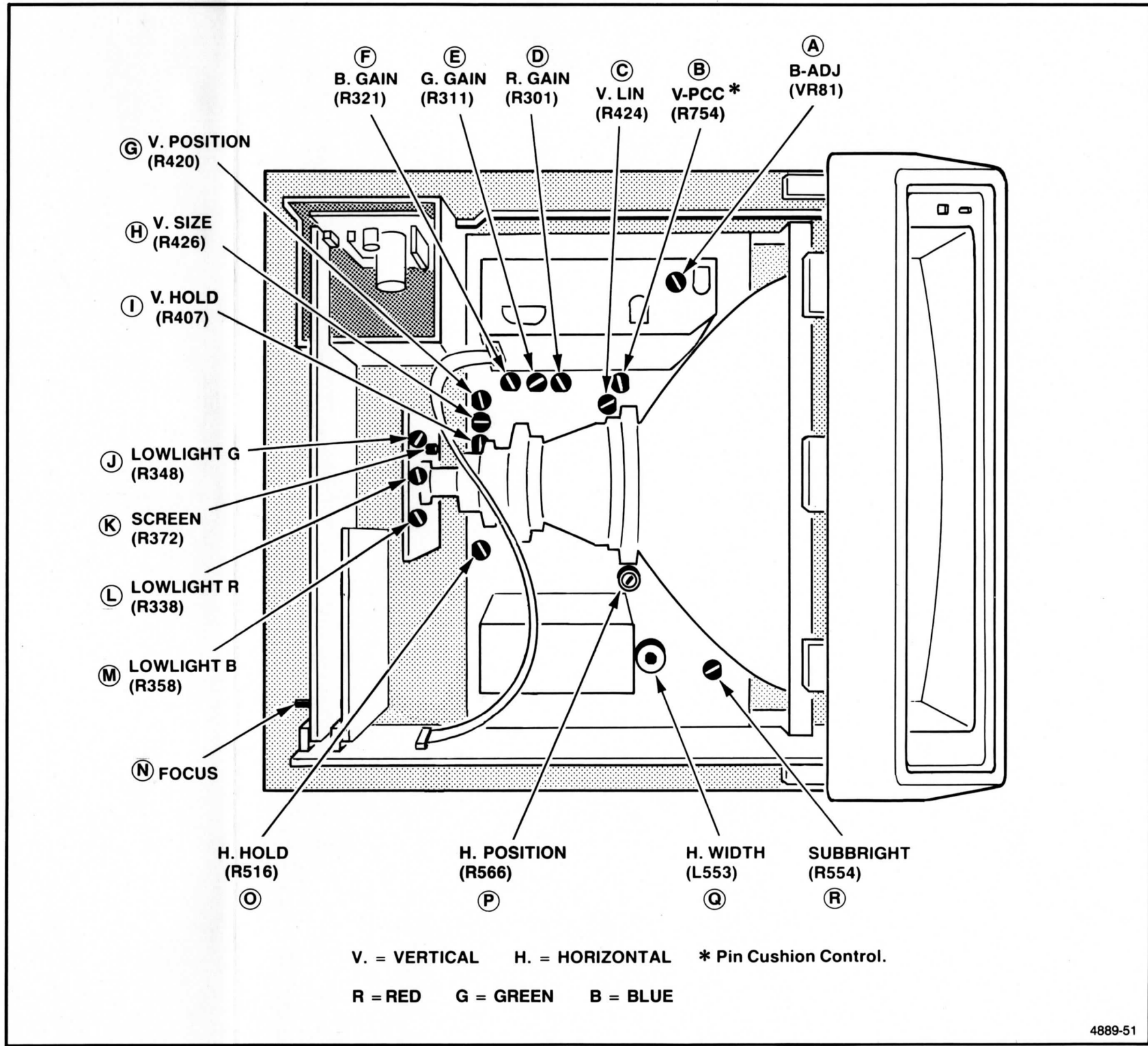


Figure 5-9. Pin-Cushion Effect.



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Figure 5-1. Display Module Test Points and Adjustments.

Section 6

MAINTENANCE

This section contains the disassembly and reassembly procedures required for trouble shooting, calibration, and repair access to the 4107 terminal. This section contains the preventive and corrective maintenance procedures for the terminal (including a summary of maintenance information for the Power Supply Module and the Display Module).

SAFETY CONSIDERATIONS

Before performing any of the maintenance procedures listed in this section, carefully read the Service Safety Summary at the front of this manual.

PREVENTIVE MAINTENANCE

The 4107 terminal is designed to require very little routine or preventive maintenance. No routine lubrication or cleaning is required. If cleaning or maintenance is deemed necessary (due to an adverse operating environment), perform the following procedures on a yearly P-M schedule.

CLEANING AND PREVENTIVE MAINTENANCE

Read ALL of the warnings and cautions in this cleaning section before attempting any of the cleaning procedures given here.

CAUTION

To avoid damage to the plastics used in the Display Module and keyboard, do NOT use cleaning agents that contain benzene, acetone, toluene, xylene, or similar chemicals.

Cleaning the CRT Screen

Clean the face of the display CRT using a soft cloth dampened with a solution of mild detergent and water.

WARNING

Disconnect the line power cord before cleaning any parts inside the 4107. Dangerous voltages exist inside the display module and may cause injury if contacted.

Occasionally, remove any accumulated dust from the inside of the Display Module. Dust conducts electricity under high humidity conditions. The 4107's interior is best cleaned with a vacuum cleaner. Remove any remaining dust with a soft bristle brush (paint brush) or a cloth dampened with mild detergent and water solution. To clean narrow spaces, use a cotton-tipped applicator.

CAUTION

Static charge can be generated by a brush with synthetic bristles. Such static charges will damage solid state components, so use a brush with natural soft bristles. (Read the Static Protection tips in the Disassembly Procedures, later in this section.)

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Cleaning the Keyboard

This procedure describes how to clean off the residue of liquids, such as coffee, soft drinks, and so forth, that have been spilled on the keyboard.

CAUTION

The cleaning procedure uses water, so try to avoid getting water on any parts susceptible to water damage, and dry thoroughly.

CAUTION

Do not tear or lose the exposed foil contacts on the foam switch pads.

NOTE

Drying times may be shortened by forced air drying at a maximum temperature of 165° F (60° C).

1. Refer to the Keyboard Removal procedure in this section in order to separate the keyboard assembly into the printed circuit board and the switch and frame assembly.
2. Use a soft artists' brush to remove any dust or foreign matter from the key contacts (foil on the bottom of the foam switch pads).
3. Wash the frame assembly thoroughly in clean, lukewarm water. Avoid damaging the foam pads.
4. Shake the excess water out of the assembly, and set it on blocks to dry in the air for about two to four days. Cleaning off the residue left by some cleaning fluids may require more than one washing.
5. Wash the circuit board thoroughly in clean lukewarm water. Use a soft sponge or cloth to dry the board.
6. Set the circuit board on blocks to dry in the air for about one day.
7. Reassemble the keyboard assembly.

WARNING

If a dampened cloth is used for cleaning any parts of the terminal that are only accessible with the cover removed, take extreme care to NOT leave any remaining water or moisture in the terminal when the cover is reinstalled. This situation could provide a potentially lethal shock hazard to the user when power is reapplied to the terminal.

ROUTINE VISUAL INSPECTION

Inspect the terminal occasionally for such defects as broken connections, damaged circuit boards, loose connectors, heat damaged parts, broken structural foam mounting features (circuit board retainers), and general mechanical fitness. If the terminal is used in a high vibration environment, pay particular attention to connectors, cable strain relief, and the CRT mounting bracket. Refer to the parts replacement procedure for appropriate details.

The corrective procedure for most visible defects is repair or replacement; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the unit. It is important to correct the cause of overheating to prevent a recurrence of the damage.

POWER SUPPLY MODULE MAINTENANCE

The Power Supply Module contains automatic current limiting protection, and does not require routine maintenance.

Fuse Replacement

The Power Supply contains just one fuse, mounted on the bottom of the power supply circuit board. This fuse's only function is that of fire protection, in the event of a malfunction/overload. If the fuse burns out, first check for a possible overload that should be corrected. Then replace the fuse with one of the proper value as indicated in Table 6-1. This fuse is referred to as F101 on the circuit board, schematic, and in the Replaceable Electrical Parts list (Section 9).

See Figure 6-5, in the Disassembly Procedures, for the location of this fuse.

Table 6-1
FUSE REPLACEMENT VALUES

Voltage Selected	Fuse Amperage
110V (nominal)	4.0 A (slow blow)
220V (nominal)	4.0 A (slow blow)

DISASSEMBLY/REASSEMBLY PROCEDURES

This part of the maintenance section describes procedures for removing and disassembling modules or major pieces of the terminal. A set of procedures at the end of this section describes the repair and replacement of components and smaller assemblies in the terminal.

These procedures require only those tools common to a service tool kit.

Unless a specific reassembly procedure is given, perform assembly by following the disassembly procedures in reverse order.

NOTE

Unless otherwise stated, all screws mentioned in these procedures are POZIDRIVE®.

REMOVING THE MAIN COVER PANEL

The terminal's main cover panel is fastened by two screws in the rear, and retainer tabs in the front. See Figure 6-1. To remove the two screws, first elevate the rear of the terminal or slide it so it extends slightly over the edge of table. Pointing the screwdriver up, unscrew these screws. Then, pull back and up on the cover piece. This will release the retainer tabs in front. Now, lift off the cover.

ELECTROSTATIC DISCHARGE PRECAUTIONS

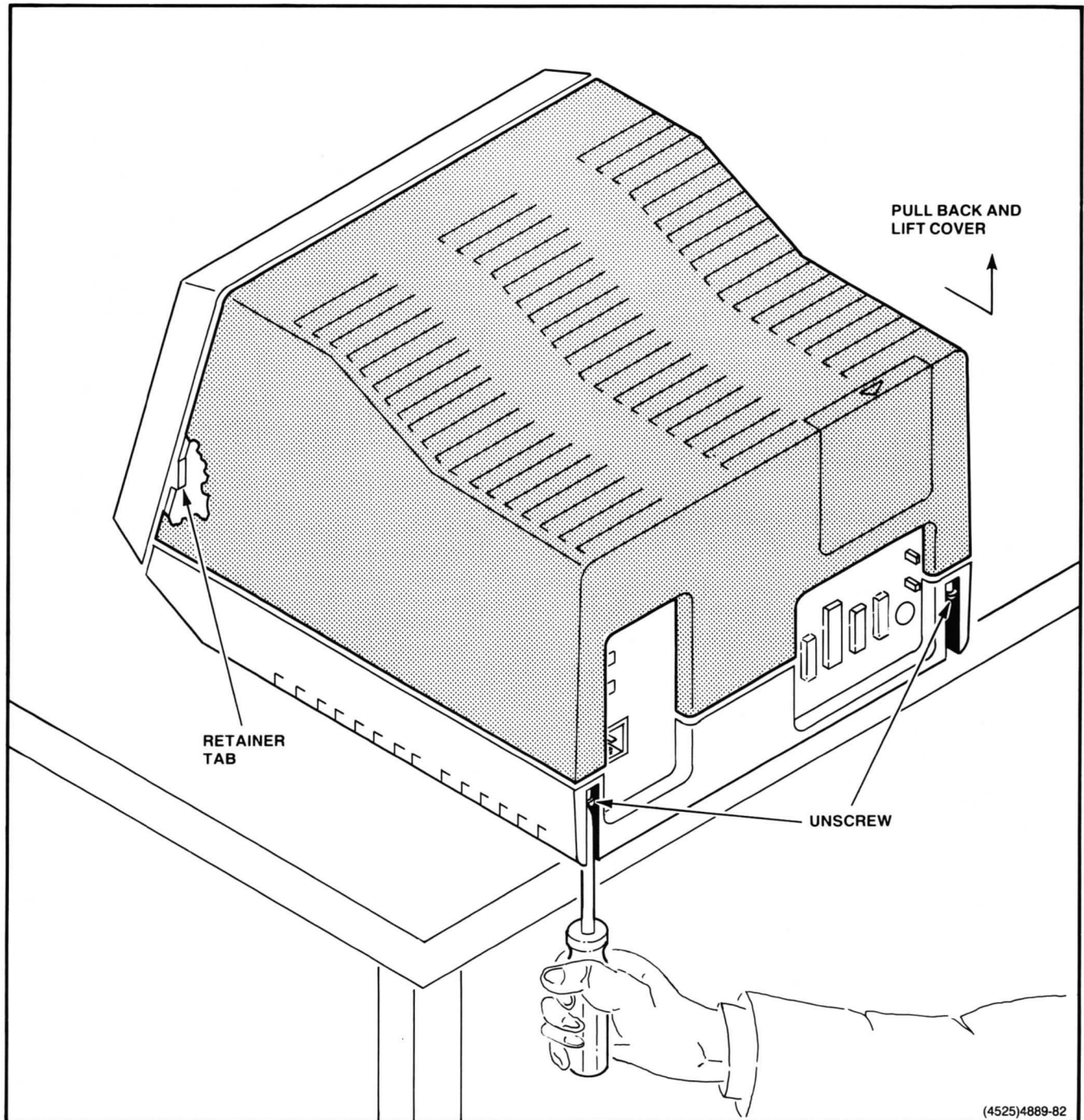
This product contains components that are highly sensitive to electrostatic discharge. To prevent damage to such components and to maintain product reliability, **do NOT** touch or remove the circuit boards or components from the 4107 until the following conditions are met.

Safe Handling of Static-Sensitive Components

Handle all static-sensitive components (such as ROMs, EEROMs, custom logic arrays, etc.) in a static-safeguarded work area. A static-safe area is any area capable of controlling static charge on conductive materials, people, and non-conductive materials.

Transportation of Static-Sensitive Components

Transport all static-sensitive components in static shielded containers/packages. A "static shield" container must be capable of protecting from static discharge as well as static fields.



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Figure 6-1. Removing Cover Panel.

REMOVING THE TERMINAL CONTROL, RAM3, AND DISPLAY CONTROL BOARDS

CAUTION

Read "Safe Handling of Static-Sensitive Components" (previous heading) before performing this and the following procedures.

The Terminal Control and Display Control boards are mounted across the side and back of the terminal (instead of in a card cage). The RAM3 board is mounted behind the Terminal Control board. Any board may be removed first; the following procedure describes removing the Display Control board first. The following procedure is depicted in Figure 6-2; each circled number (on the illustration) corresponds to a step in the procedure.

1. Unplug the ribbon cable that connects the Display Control board to the Display Module.
2. Pull the Display Control board away from the Terminal Control and RAM3 boards; they are attached to each other by two 96-pin DIN connectors. This physically separates the three boards.
3. Lift the Display Control board up out of its retainer slots, and remove from the terminal.
4. Now the RAM3 board is free. Remove this board from the terminal by lifting it out of its dove-tail mounts.
5. Unplug the ground-wire that attaches to the upper-left corner of the connector panel, at the rear of the terminal. (The other end of this wire remains connected to the power supply.)
6. The Terminal Control board attaches to the power supply via a 10-pin connector on the upper-left extension of the board. Unplug the board from this connector by gently springing it away from the power supply.
7. Remove the Terminal Control board by lifting it straight up and out of the terminal. (The rear connector panel is mounted to this board, and slides in vertical grooves that secure it to the back of the terminal cabinet.)

CAUTION

Before installing the Terminal Control, RAM3, and Display Control boards in the terminal, observe the following. First, see that all pins on the 96-pin connectors are straight. Then, place the boards in the terminal, align the connectors, and carefully push them together. Carelessness can easily result in bent pins, which may cause the power supply to "crowbar" (which shuts down the supply).

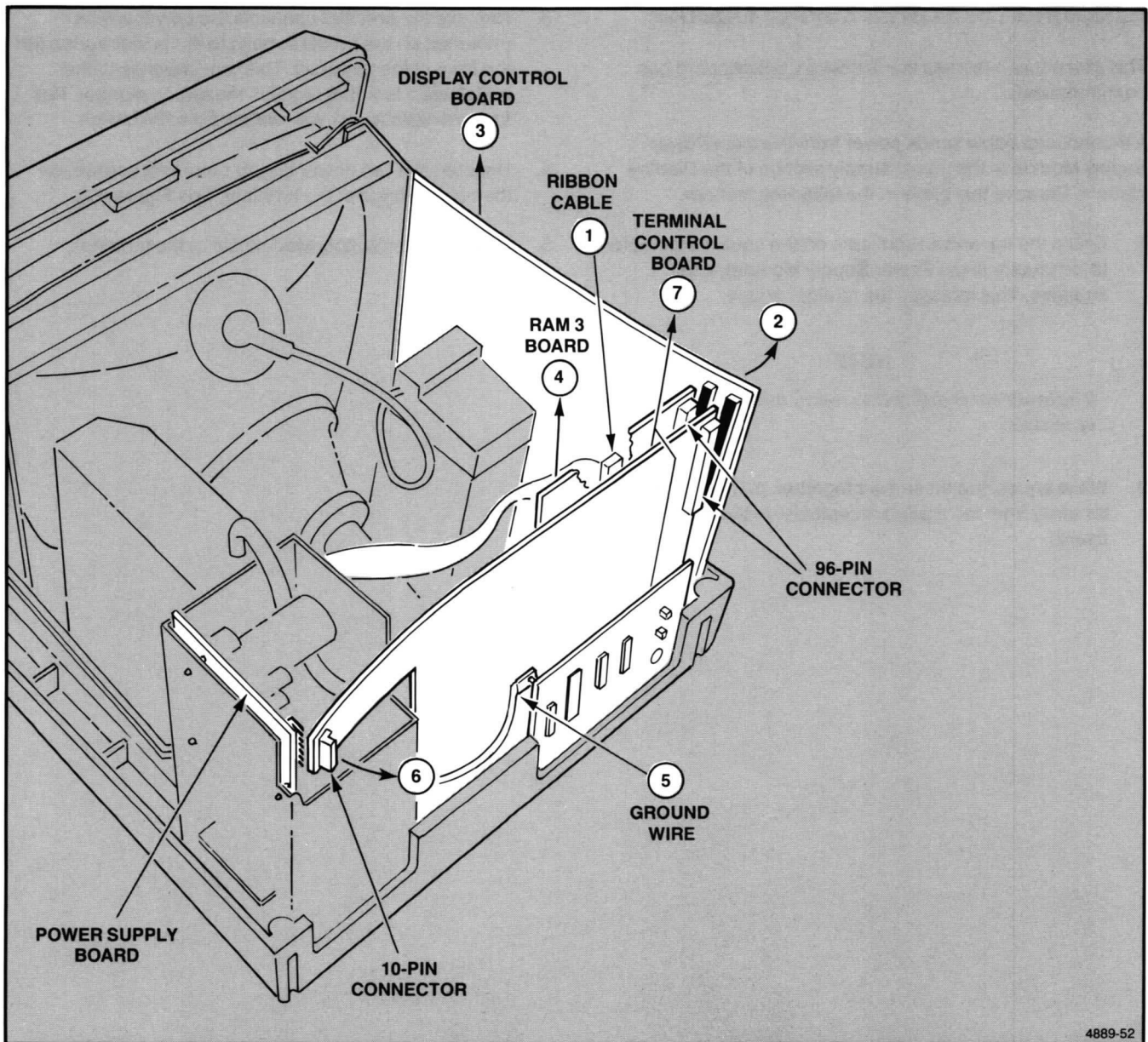


Figure 6-2. Terminal Control, RAM3, and Display Control Circuit Boards.

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REMOVING THE POWER SUPPLY MODULE

This procedure assumes the Terminal Control board has been removed.

A 9-conductor cable sends power from the main Power Supply Module to the power supply section of the Display Module. Remove this cable in the following manner.

1. Grasp the top and bottom ears on the square connector (9-conductor in the Power Supply Module), and squeeze. This releases the retainer snaps.
2. While squeezing these ears together, pull the connector away from the mating receptacle on the circuit board.
3. Remove the arm that connects the power switch (mounted on the power supply) to the power button (on the front of the terminal). This arm attaches to the switch via a fork that straddles the switch plunger. Pull forward and the fork will release from the switch.
4. Unscrew the two power supply mounting screws, on the outside edge of the terminal. See Figure 6-3.
5. Lift the Power Supply Module out of the terminal.

NOTE

The lower ear is difficult to reach, but it IS accessible.

2. While squeezing these ears together, pull the connector away from the mating receptacle on the circuit board.

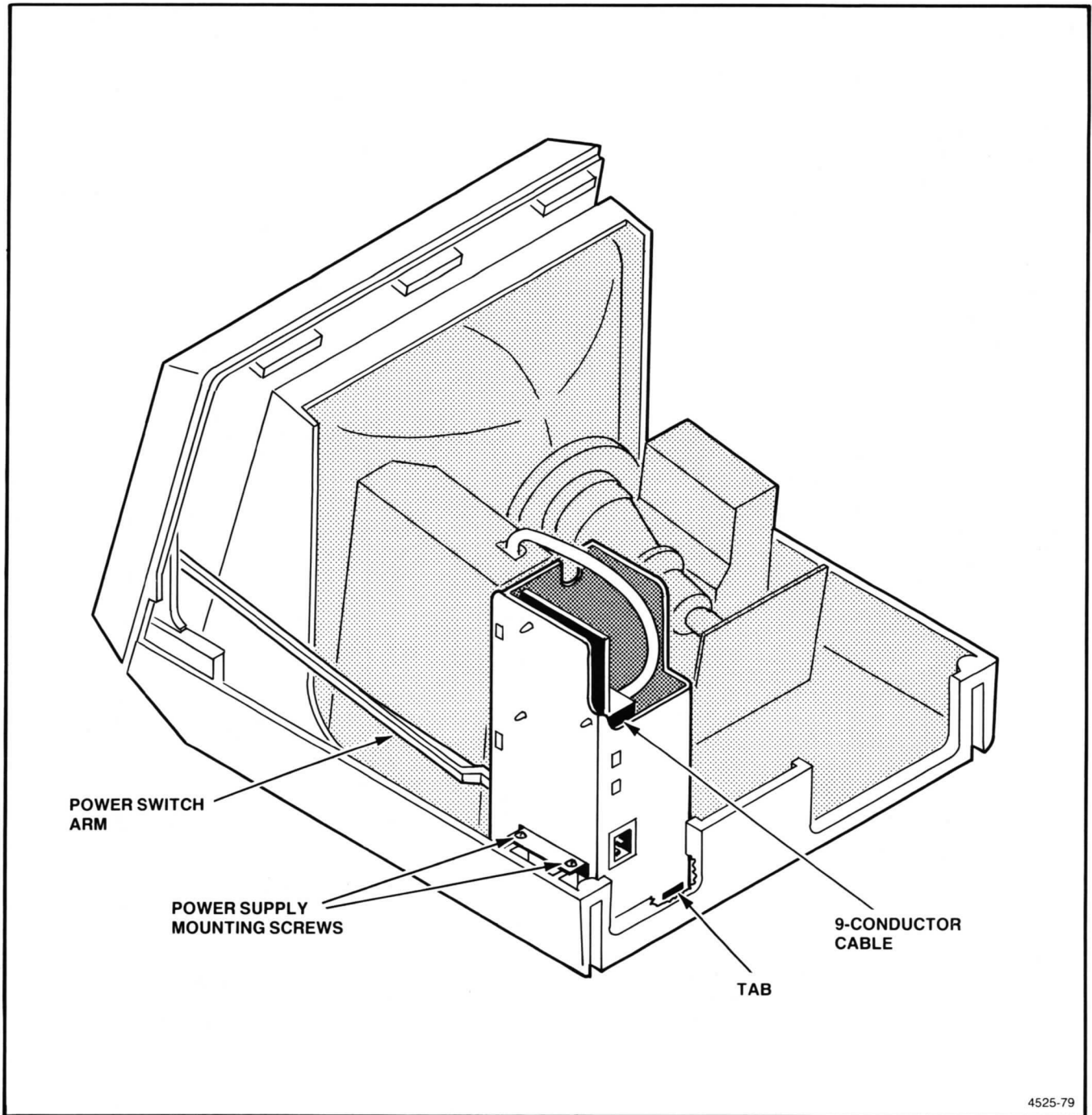


Figure 6-3. Power Supply Mounting Screws.

DISASSEMBLY OF THE POWER SUPPLY MODULE

1. Position the Power Supply Module as shown in Figure 6-4. Unscrew the screw called-out in the in-set of this figure. This screw fastens an access panel that is hinged with three ears/slots.
2. Now, swing this wrap-around panel out, around the hinge.
3. Slip the ears out of the slots, and remove this panel from the rest of the Power Supply Module.

This provides access to internal parts for: inspection, adjustment, or removal/replacement of components.

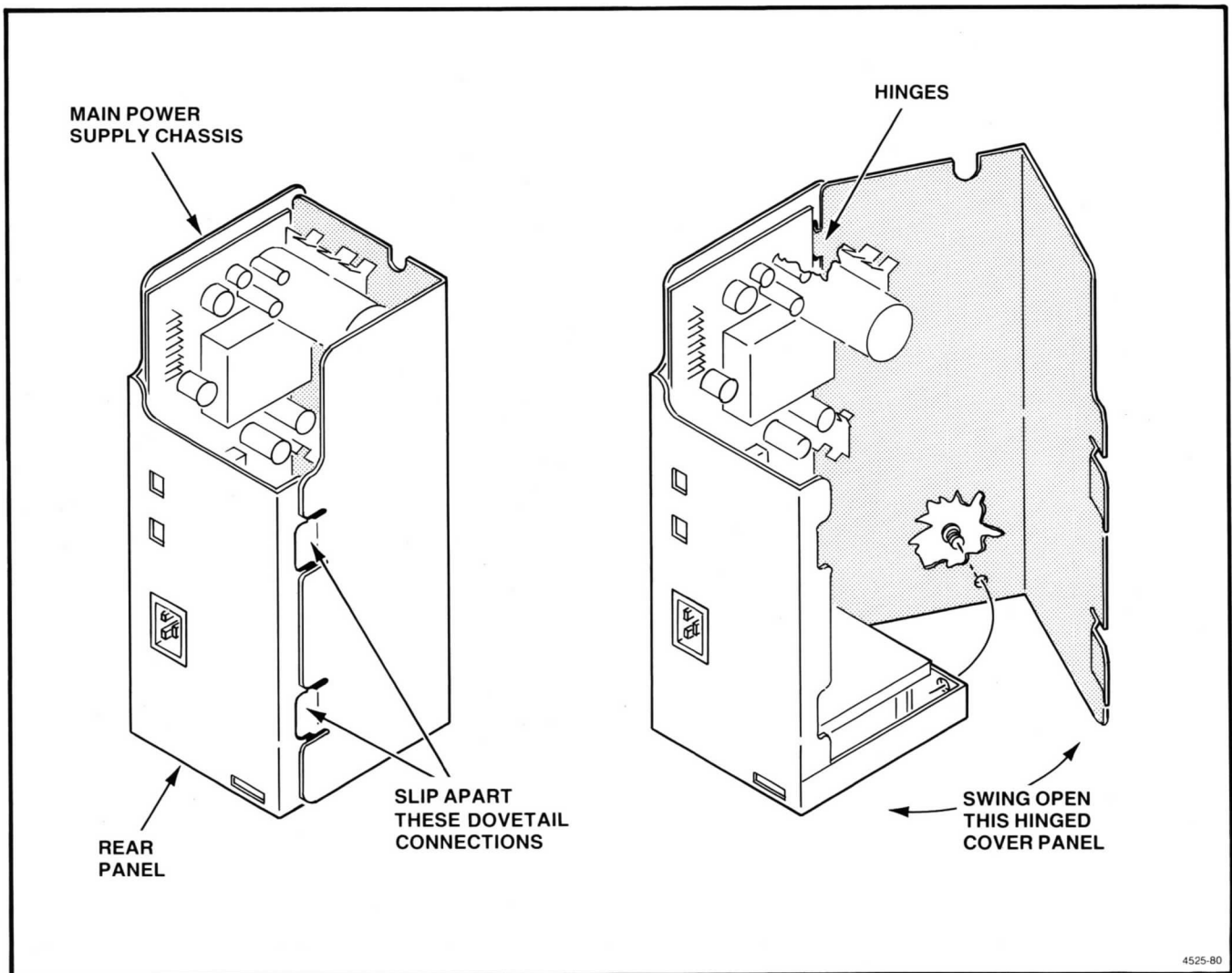


Figure 6-4. Opening the Power Supply Hinge Panel.

Replacing the Power Supply Fuse

A fire protection fuse is located at the bottom of the power supply circuit board (just behind the AC power receptacle). See Figure 6-5.

If this fuse burns out, that indicates a serious overload problem. First, check all loads and the components serving such loads, and repair the overload condition. Then replace this fuse. Use only a 4A (250 V) Slow Blow fuse.

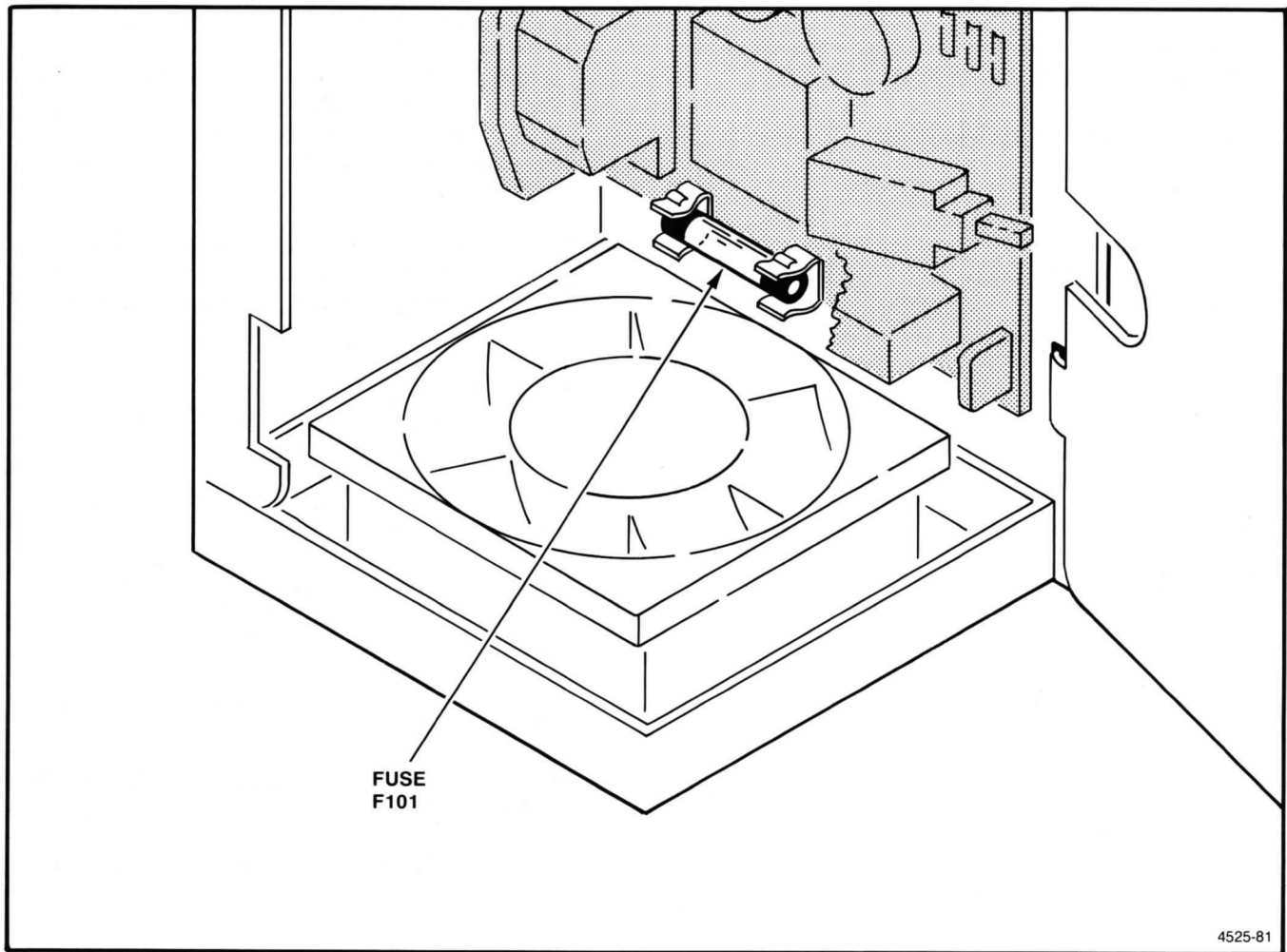


Figure 6-5. Power Supply Module Fuse Location.

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Removing the Cooling Fan

The cooling fan may be removed as follows:

1. First, unplug the fan power cord from the two-prong connector (J3) on the upper end of the power supply circuit board.
2. Then, unscrew the two 5/16" hex screws that mount the fan to the bottom of the power supply case.
3. Lift the fan and screen sideways out of the power supply.

NOTE

When installing this fan, be sure to mount it so it blows air INTO the power supply.

Removing the Power Supply Circuit Board

The circuit board is mounted to the power supply chassis by five snap-on connectors, and by the AC power receptacle unit.

1. First, disconnect the circuit board's ground wire, by unscrewing the nut that mounts it to the chassis.
2. Figure 6-6 illustrates removing the AC power receptacle from the chassis. First, using a scribe and hammer, tap the mandrel (pin) through each of the two rivets. Now, push out the rivets. The AC receptacle is free from the chassis.

These rivets may be reused by pushing each rivet through the chassis and receptacle holes, and then driving each mandrel in until flush with the top of the rivet head.

3. Remove the screw that fastens the AC power receptacle to the circuit board and to the chassis. See Figure 6-6, again.
4. Locate the five snap-on fasteners that mount the circuit board to the chassis.
5. One at a time, squeeze together the lock-ears, on the chassis side of each fastener. Push the fasteners into their holes, to keep the ears from popping out again.
6. Push the boss, on the AC power receptacle, through its hole in the chassis.
7. Then, push the five fasteners through their holes in the chassis.
8. This releases the circuit board. Lift it out of the chassis.

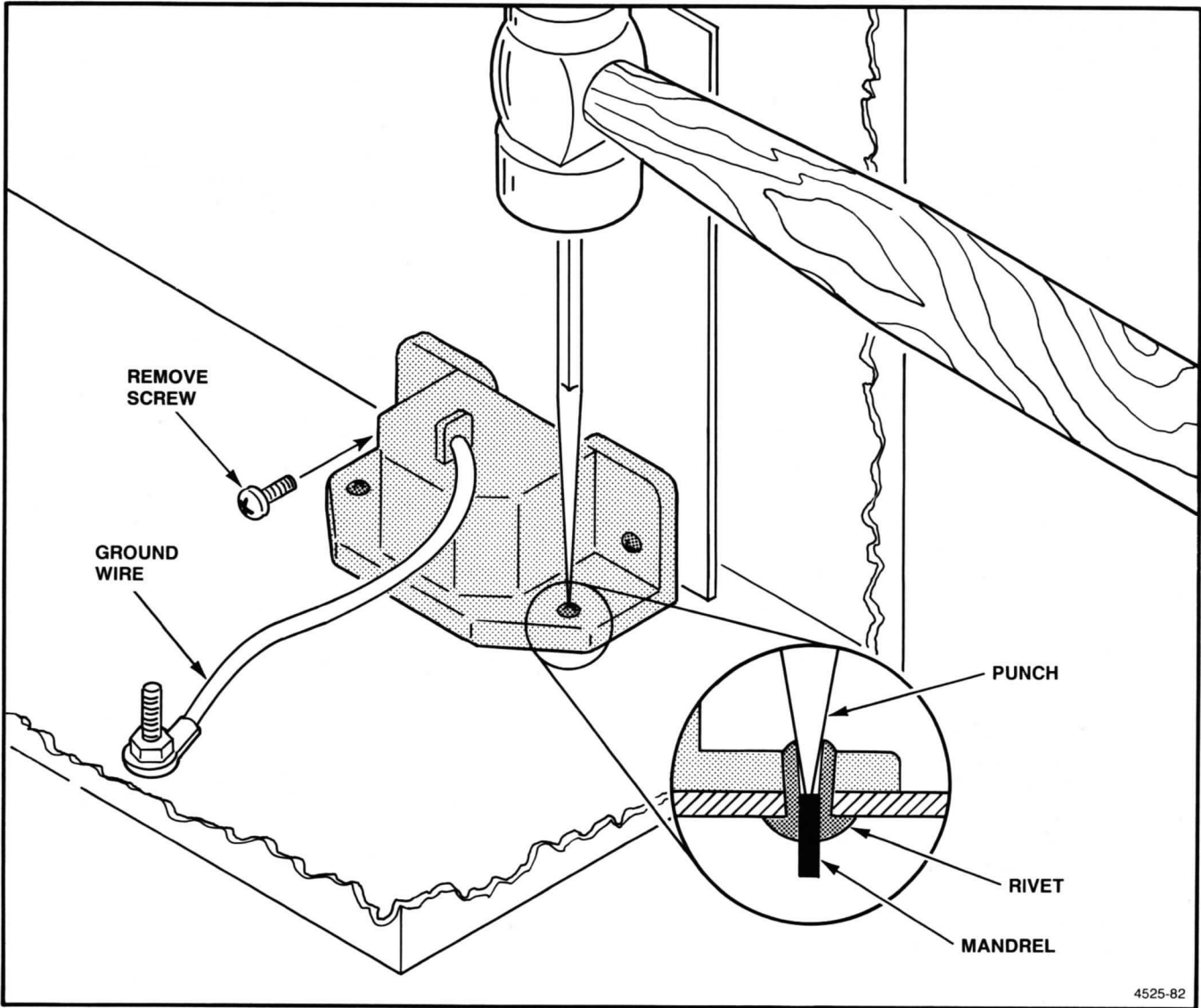


Figure 6-6. Removing Power Receptacle Rivets.

REMOVING THE DISPLAY MODULE FROM THE TERMINAL

The Display Module mounts to the terminal with six screws. These screws are located in rails on each side of the Display Module. They screw into threaded brass inserts in the base of the terminal. See Figure 6-7.

WARNING

Lethal voltages are present at the High Voltage anode on the CRT. Discharge this H.V. connection before performing the following procedure. Bodily contact with such voltage may cause shock injury or death.

Procedure:

1. Discharge the High Voltage Anode button on the CRT. Using an insulated screwdriver, slip the blade under the rubber anode cover; then lay the screwdriver shaft against the grounded metal frame.
2. Remove the main front bezel that surrounds the CRT and contains the BRIGHTNESS and POWER controls. This bezel attaches with two screws (one on each side). See Figure 6-7.
3. Unclamp the Terminal Control board's ground wire from the Display Module chassis.
4. Unplug the ribbon cable from connector J31 on the Display Control board.
5. Remove the Terminal Control board, RAM3 board, and Display Control board.

NOTE

Disconnect the Power control rod from the on-off switch on the main Power Supply Module.

5. Remove the BRIGHTNESS control from the back side of the bezel by spreading the retainer forks that slip over the top and bottom of the brightness pot. This releases the potentiometer from the back side of the bezel, while the knob remains attached to the front of the bezel.
6. If the Power Supply Module is still installed, remove it using the procedure earlier in this section.
7. Unscrew part way the six Display Module mounting screws.
8. Slide the Display Module to the rear (in the screw slots). The slots are open at the front end, allowing the screw heads to be free when the Display Module is slid back.
9. Unplug all remaining Display Module connecting cables.

CAUTION

Exercise care when lifting, to avoid back injury.

10. Now, lift the Display Module out of the terminal.

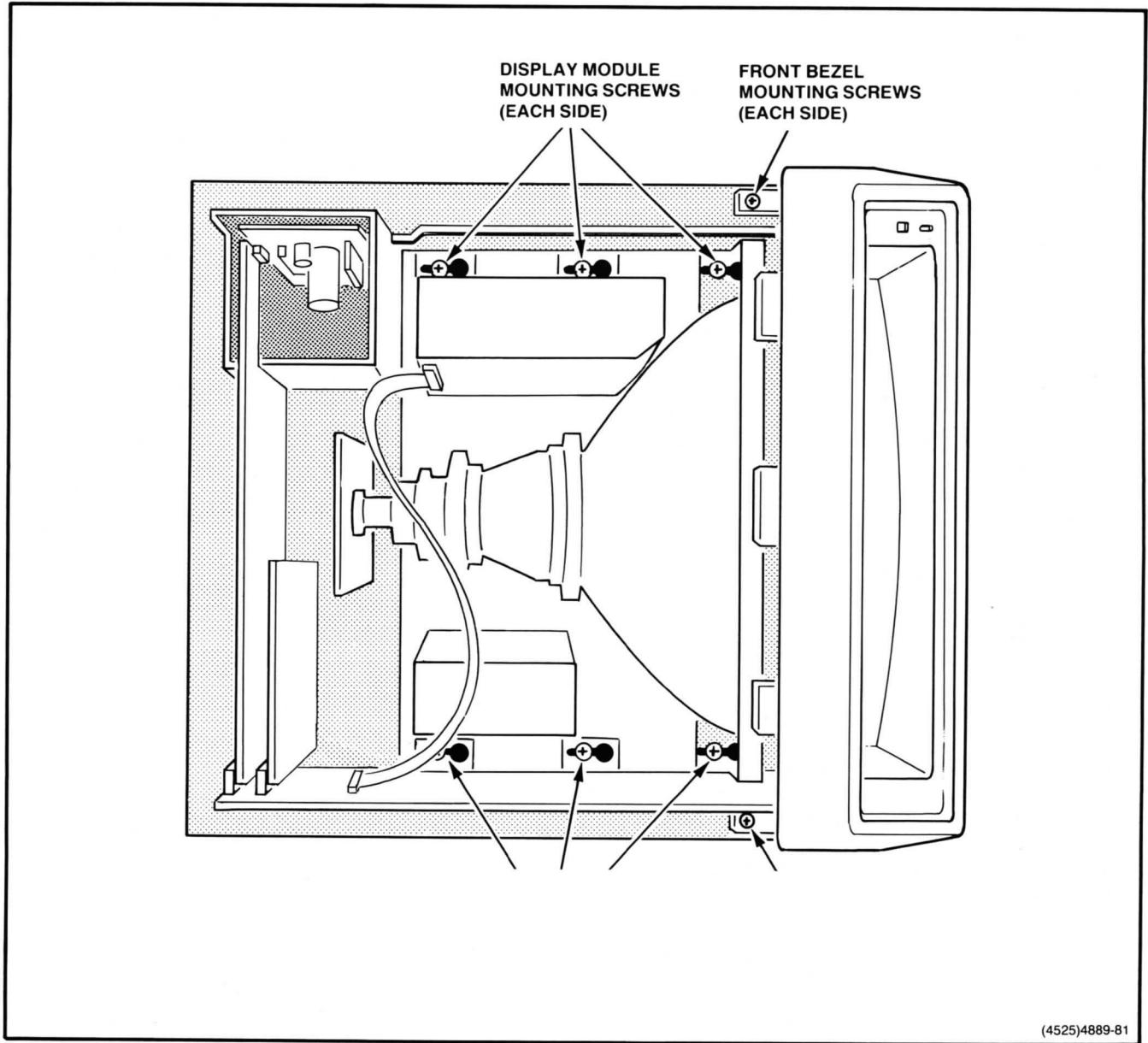


Figure 6-7. Mounting Screws for the Front Bezel and Display Module.

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REMOVING AND REINSTALLING THE DISPLAY CRT

The following CRT removal procedure assumes the Display Module is outside the terminal.

WARNING

Lethal voltages are present at the High Voltage anode on the CRT. Discharge this H. V. connection before performing the following procedure. Bodily contact with such voltage may cause shock injury or death.

1. Discharge the High Voltage anode button on the CRT; see WARNING.
2. Remove the High Voltage anode cable from the CRT connector button.
3. Unplug the CRT socket and circuit board from the CRT. A silicon gum may have been used to glue the socket to the CRT; use a knife to peel this gum away from the socket.
4. Unplug the wire from L3 on the CRT Socket board.
5. Remove the four screws that clamp the front corners of the CRT to the display chassis. Remove the lower bracket also. Place the washers and screws in labeled containers (to prevent misplacing them or confusing them with other similar, but different, screws). See Figure 6-8.

6. Unplug the deflection yoke cables from connector "A2", on the Main Video Board.

NOTE

The yoke assembly is part of the CRT, and is not to be removed from the CRT.

7. Place a soft pad on the bench-top and in front of the CRT. (Upon removal the CRT will rest on this protective pad.)

WARNING

The CRT may be damaged by careless handling when removing it from the terminal. Protect it from sharp, solid objects. If the CRT cracks and explodes, serious personal injury is likely.

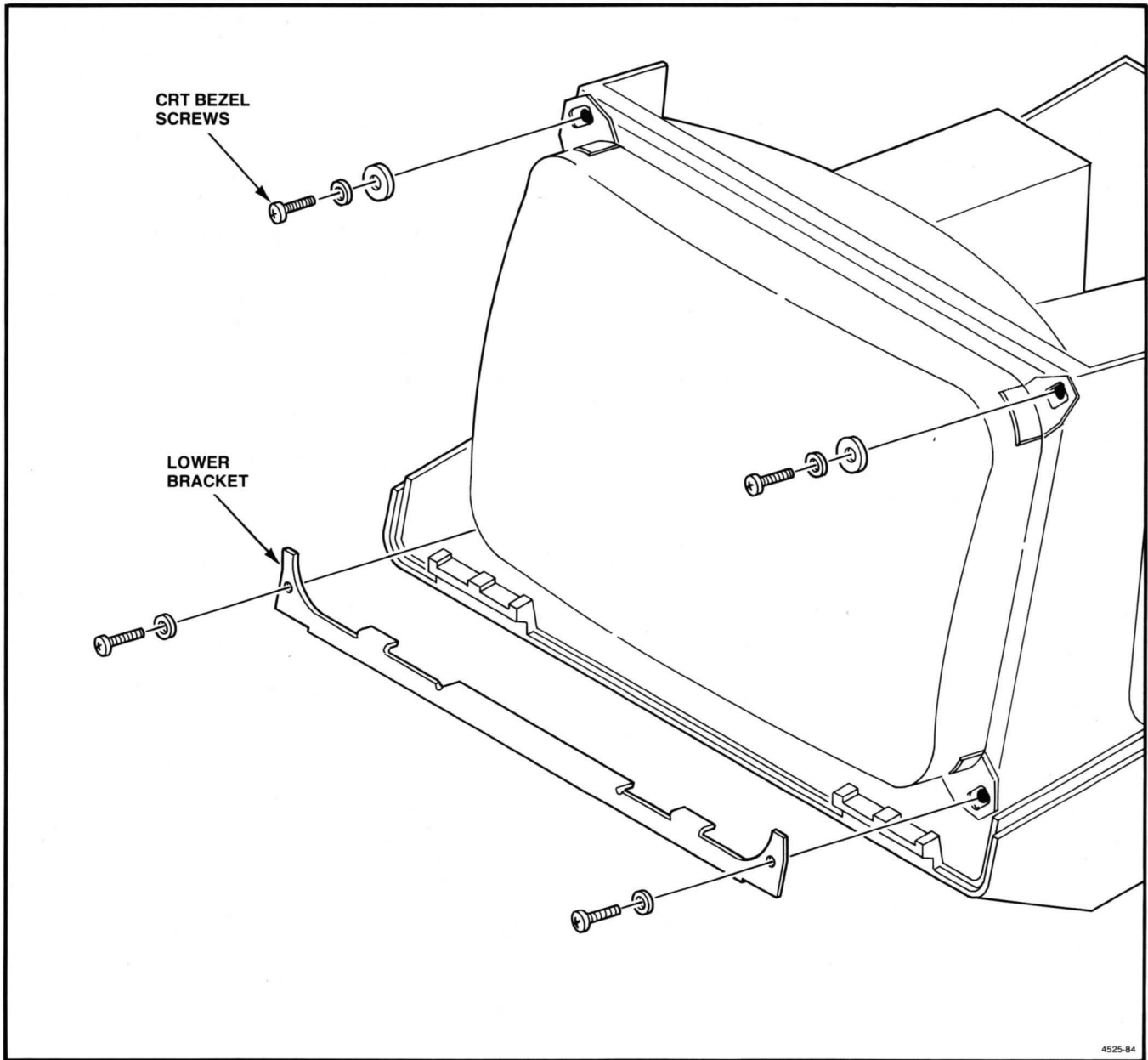


Figure 6-8. CRT Forward Mounting Screws.

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8. Rock the CRT forward as indicated in Figure 6-9. Then pull the CRT out of the front of the Display Module, and lower it onto the protective pad.

To install the CRT, follow the previous steps in reverse order.

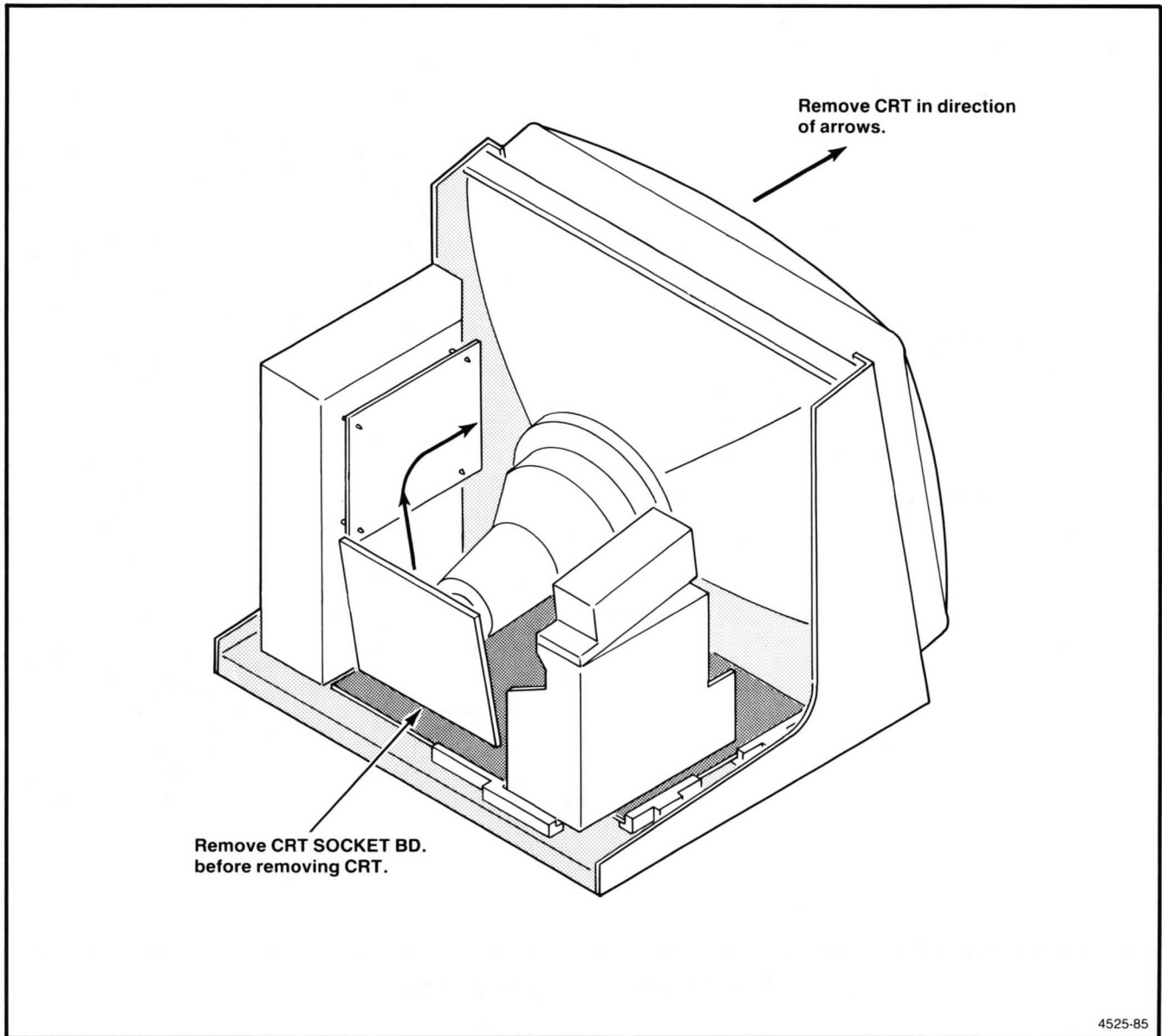


Figure 6-9. Removing the CRT.

REMOVING THE DISPLAY MODULE CIRCUIT BOARDS AND HIGH VOLTAGE SECTION

The Display Module consists of the following boards and assemblies. These are identified by numbers in this list, which are also used in Figure 6-10.

- ① Display CRT (removal just described),
- ② Display Module power supply "TNP82560-24" (in a protective metal enclosure),
- ③ Interface board "TNP81125" (mounted beside the power supply enclosure),
- ④ Main Video board "TNP82866" and high-voltage section (mounted under the CRT), and
- ⑤ CRT Socket board "TNP95909" (mounted on the CRT neck socket).

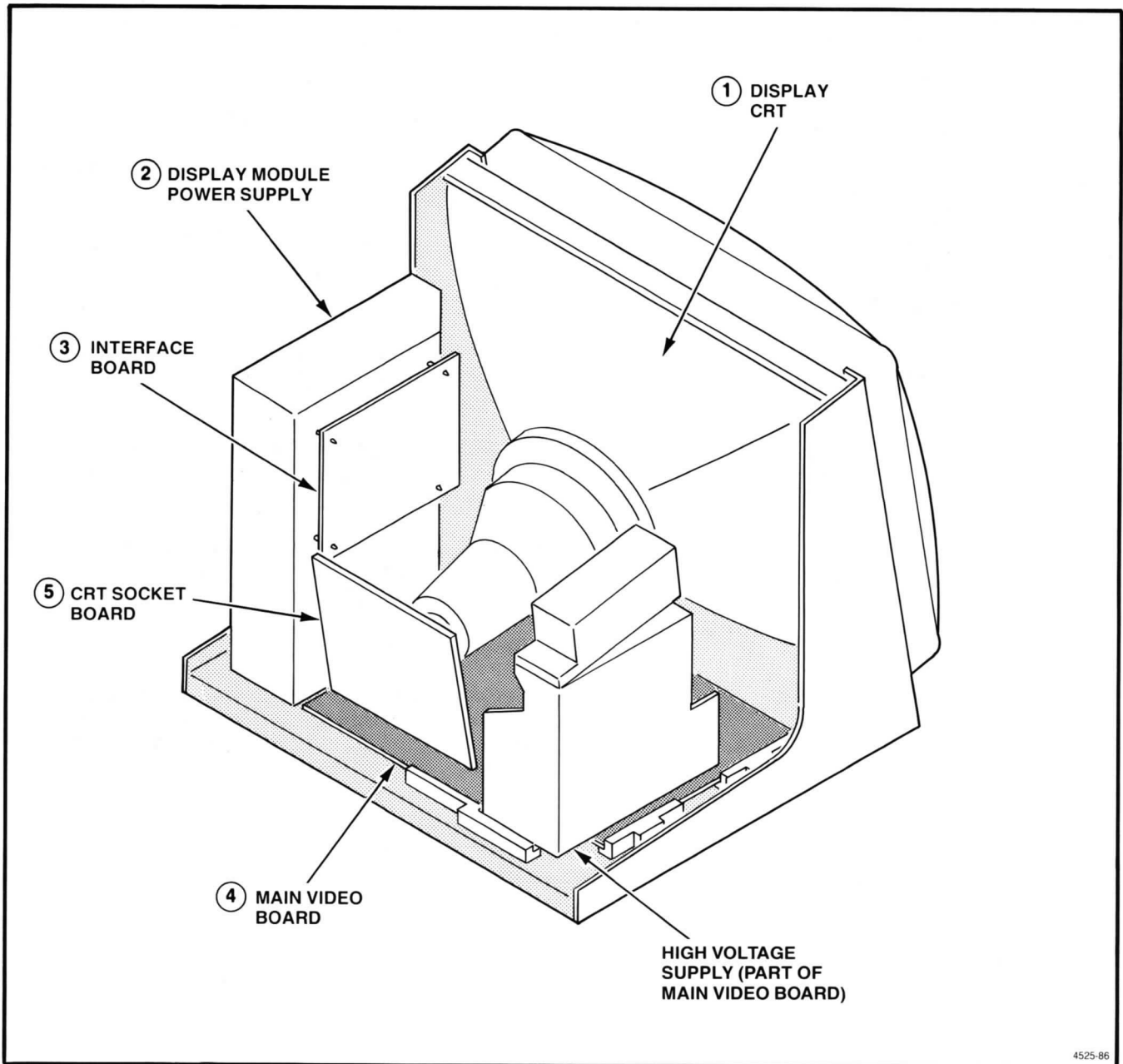


Figure 6-10. Display Module Boards and Assemblies.

NOTE

The CRT Socket board is the most vulnerable. It is wise to remove it first.

Removing the CRT Socket Board

A silicon gum glues the CRT Socket board to the neck socket of the CRT. Use a knife to peel the gum away from the socket. Then remove the board by gently prying it away from the CRT socket. Unplug the 2-wire plug from connector "L3" on the Socket board; these plug wires connect to the CRT grounding strap.

Removing the Display Module Power Supply

The following procedure (steps 1 through 8) is the recommended procedure for removing the Display Module's power supply. An alternate method of removing this supply follows the last step of this procedure.

1. Unplug the 9-pin square connector in the main Power Supply Module. This cable/plug supplies AC voltages to the display power supply.
2. Remove the main Power Supply Module. See the procedure earlier in this section.
3. Unplug the 4-pin plug, emerging from the "AC OUT" hole in the display power supply.
4. Unplug the 2-pin plug, coming from the "DC OUT" hole in the display power supply.
5. Unscrew the forward-facing screw on the bottom-rear corner of the display power supply; see screw (D) in Figure 6-11.
6. Unscrew the screw that fastens a bracket to the upper-front outside panel of the display power supply enclosure. See (A) in Figure 6-11.
7. Push forward and then lift up on the display power supply. It will snap out when free of the retainer hooks beneath it.
8. At this point, the power supply is free but the Interface board remains attached to it. Go to "Removing the Interface Board," next.

Alternate procedure:

The display power supply can be removed without removing the main Power Supply Module. To do this, remove three screws labeled (A), (B), and (C) in Figure 6-11. Then unplug the cables and lift out the assembly.

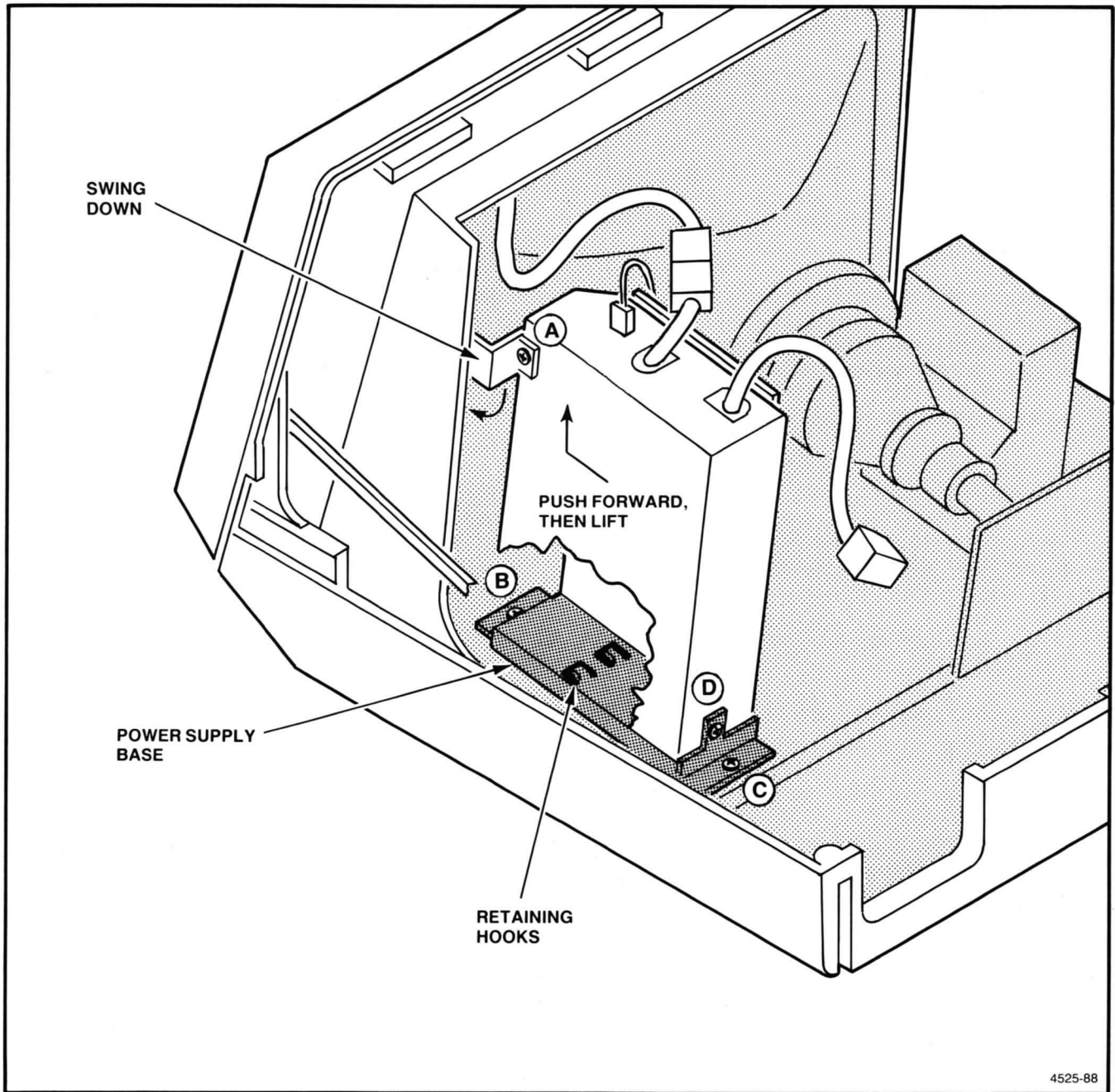


Figure 6-11. Display Power Supply Mounting Screws.

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Removing the Interface Board

The Interface board is part of the Display Module. It is mounted on the Display Module's power supply. Refer to Figure 6-12 while performing this procedure.

1. Unplug the 20-conductor ribbon cable from the Display Control Board. Push the ears (on the mounted socket) out/away from the plug; this ejects the plug part of the connector.
2. Remove the display power supply from the Display Module (with Interface board attached). This provides easy access to the Interface board. See preceding heading, "Removing Display Module Power Supply."
3. Unplug the cable from "DC OUT" on this power supply.
4. Unplug the two connectors at F12 and F13, at the front of the Interface board.
5. Disconnect the forward ferrite loop from the chassis by unwrapping its red connecting strap. See (A) in Figure 6-12.
6. Unplug the cables from connectors A4 and A5 on the Main Video board.
7. Unplug the cables from connectors F12 and F13 on the Interface board.
8. Clip and remove all cable restraints on the Display Module.
9. Pull the cables through the ferrite loop as follows: First, pull the 2-wire power cable and connector through. Then, pull the remaining cables, saving the cable/connector A4 until the last. (Connector A4 is larger and needs more clearance.)
10. Using pliers, squeeze together the retainer ears on each of the four stand-offs that mount this board to the side of the power supply enclosure. Press the stand-offs into their respective holes in the Interface board. The stand-offs remain attached to the power supply, and the Interface board is free.

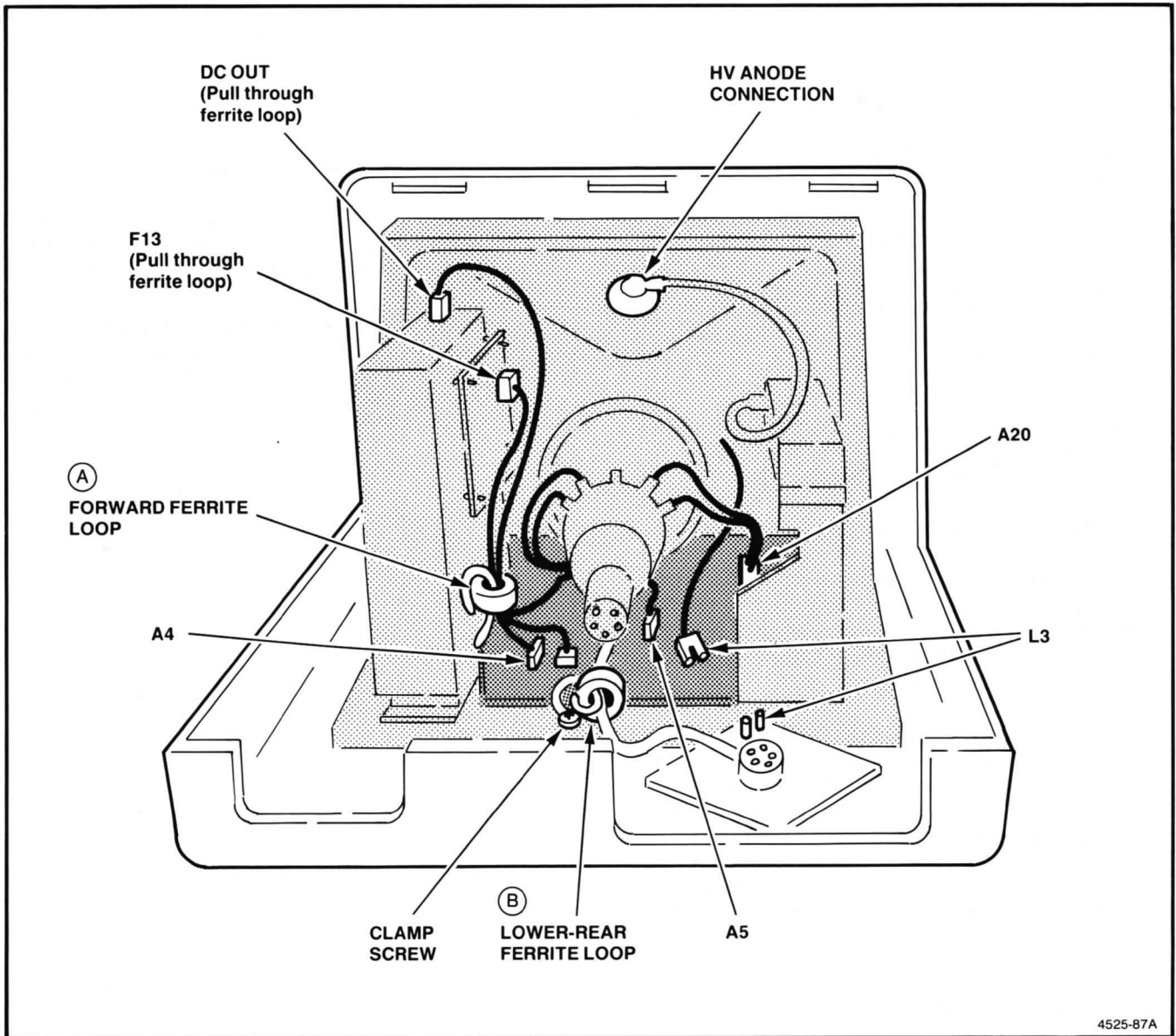


Figure 6-12. Removing the Ferrite Loops.

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Removing the Main Video Board and H.V. Section

It is easier to access the Main Video board after the Display Module is removed from the terminal. However, if you need to remove the board with the Display Module installed, use the following procedure.

NOTE

The CRT Socket board and Main Video board compose one field replaceable unit. Therefore, these boards remain connected together upon removal and are shipped as one unit.

1. Remove the Display Control board, the RAM3 board, the Terminal Control board, and the Power Supply Module. (Refer to previous procedures.)
2. Remove the CRT Socket board, as indicated earlier.
3. Unwrap the red strap that holds the lower-rear ferrite loop to the chassis. Refer back to ③ in Figure 6-12. The ferrite loop remains on the wires passing through the loop. Disconnecting the loop-strap provides the needed freedom for these wires.
4. The Main Video board is attached to the chassis by four grooved brackets. See Figure 6-13. Unscrew the two screws from the rear bracket and remove it from the back-end of the circuit board. Also, remove the left-rear bracket² from the side of the board.
5. Discharge the HV Anode connection, and unplug the HV Anode cable from the CRT.
6. Unplug the yoke wires from connector A2 on the Main Video board.
7. Unplug A4, A5, and A6 on the Main Video board.
8. Unplug F13 from the Interface board. Pull cables from F13 and DC OUT through the forward ferrite loop (if still installed). Refer back to Figure 6-12.
9. At this point, the CRT Socket board and Main Video board are free from the rest of the terminal and may be removed. Slide the Main Video board toward the back of the Display Module and lift it out.

Then, just loosen the forward bracket on the same side of the board. This allows enough freedom to remove the board.

² This is as viewed from the front of the terminal.

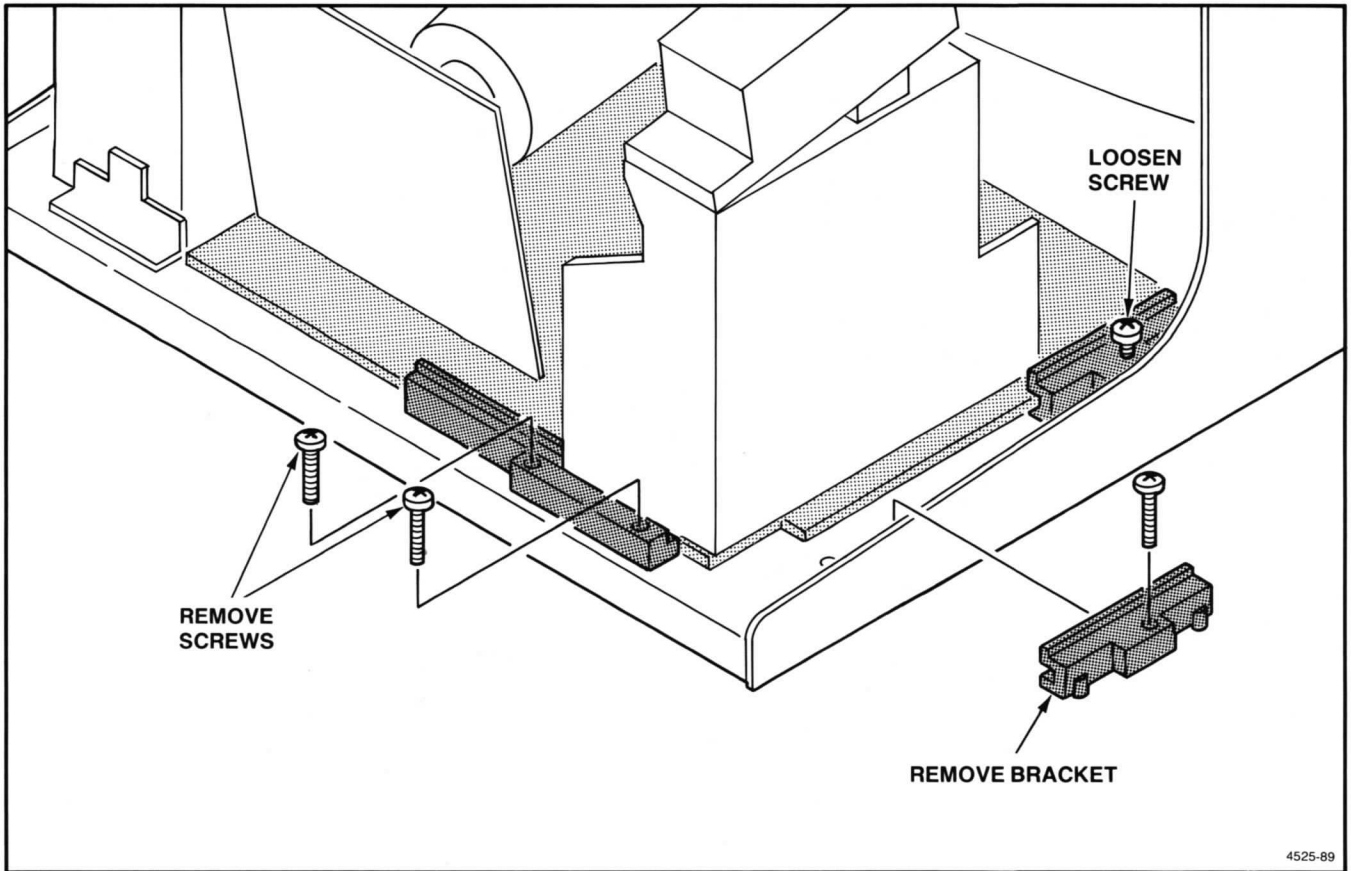


Figure 6-13. Loosening/Removing Brackets from the Main Video Board.

DISASSEMBLING THE KEYBOARD MODULE

The Keyboard Module is physically separate from the main terminal. It is only connected by a 5-conductor cord. This procedure describes the steps in unplugging the keyboard, and in disassembling it into its component parts. Steps 1 through 5 tell how to access the inside of the Keyboard Module. Steps 6 through 8 describe removal of the keyboard cable. And, steps 9 through 12 tell how to remove the keypad assembly.

1. Unplug the keyboard cable from its 5-conductor connector on the terminal's rear panel.
2. Unscrew the four screws in the corners of the keyboard bottom panel. See Figure 6-14.
3. Flip the elevating bails outward, as in Figure 6-14.

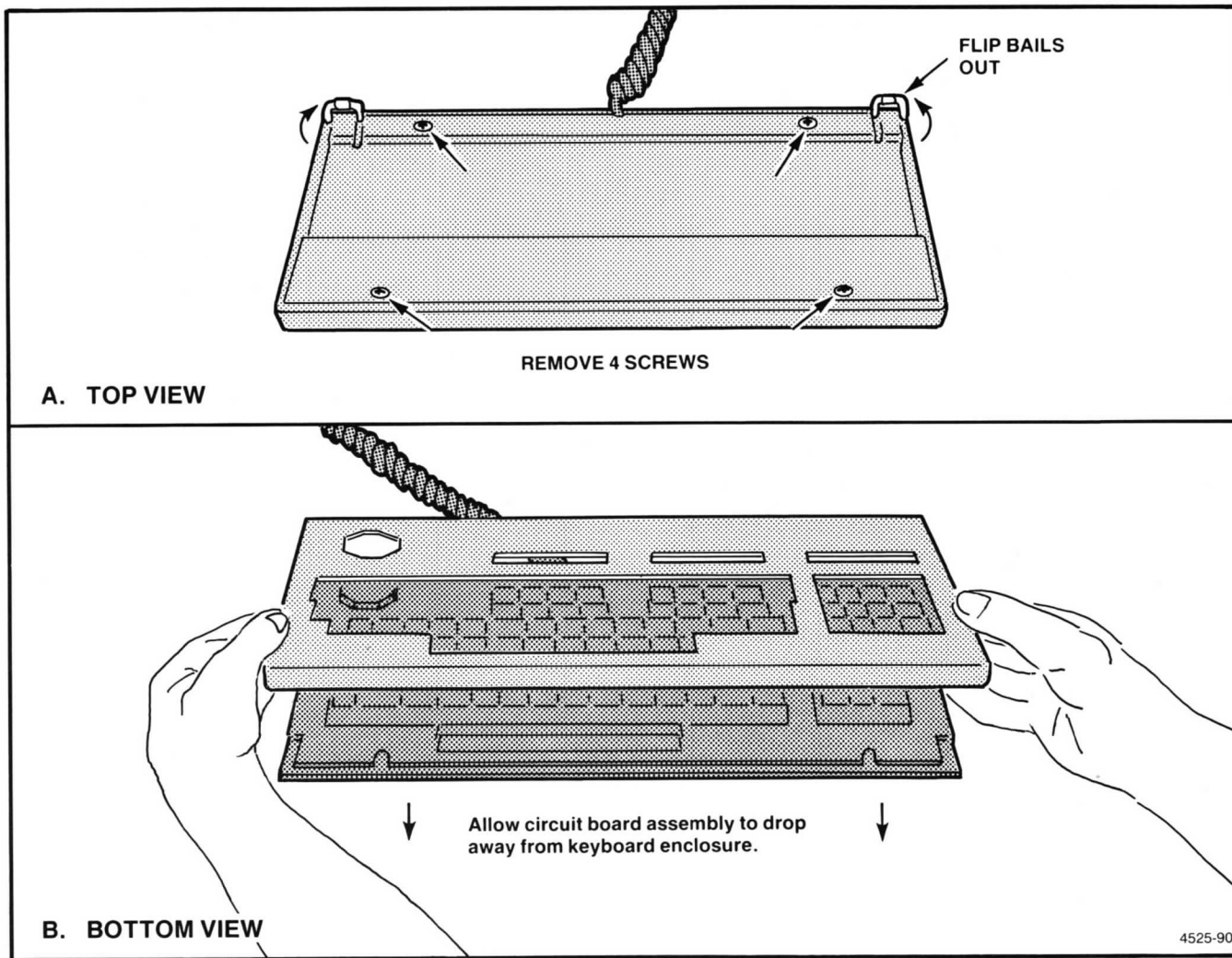


Figure 6-14. Separating the Keyboard Enclosure from the Keyboard and Bottom Panel.

4. Pull the circuit-board/keypad assembly away from the under-side of the keyboard enclosure.
5. Unscrew the two screws that attach the bottom panel to the circuit-board/keypad assembly. These two screws act as a hinge. See Figure 6-15.
6. Unplug the keyboard-cable's ground wire from its spade-lug connector.
7. Unplug the 5-pin keyboard-cable connector.
8. Remove the 1/4" nut and lock washer in Figure 6-16, and remove the cable's strain relief strap.

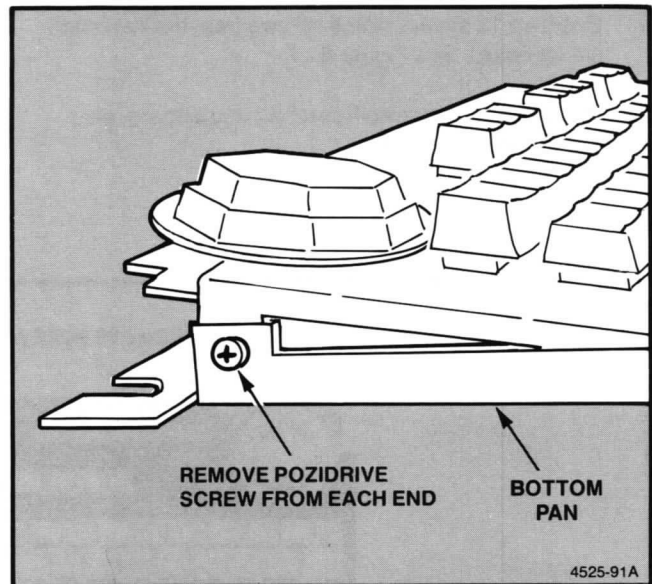


Figure 6-15. Removing the Keyboard Bottom Panel.

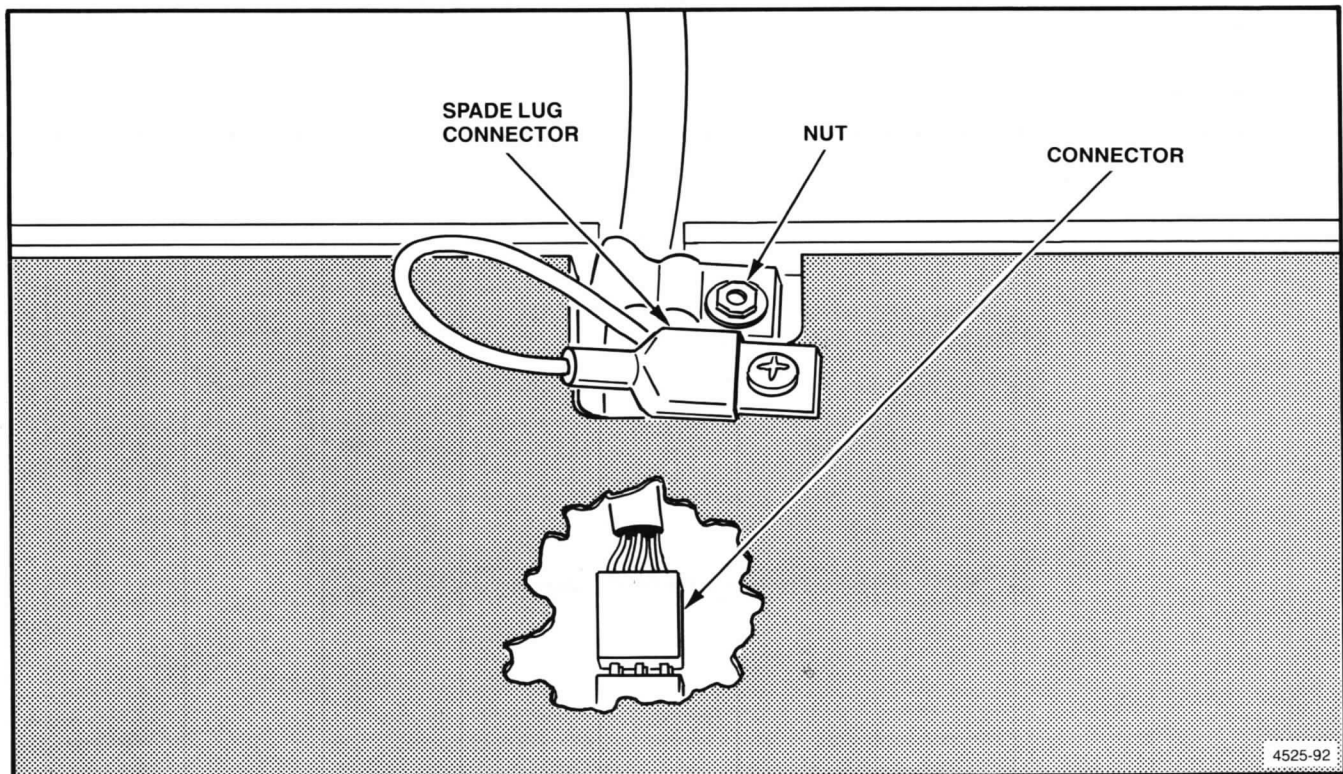


Figure 6-16. Disconnecting the Keyboard Cable.

MAINTENANCE

9. Unscrew 13 small Phillips screws from the keyboard circuit board. See Figure 6-17.
10. Unscrew three screws from this circuit board, also shown in Figure 6-17.
11. Unscrew one screw from the keypad's metal housing (located between the "Menu" and "F1" keys, on the opposite side of the keyboard).
12. Now separate the keypad assembly from the circuit board. The key switches are now accessible for cleaning or repair.

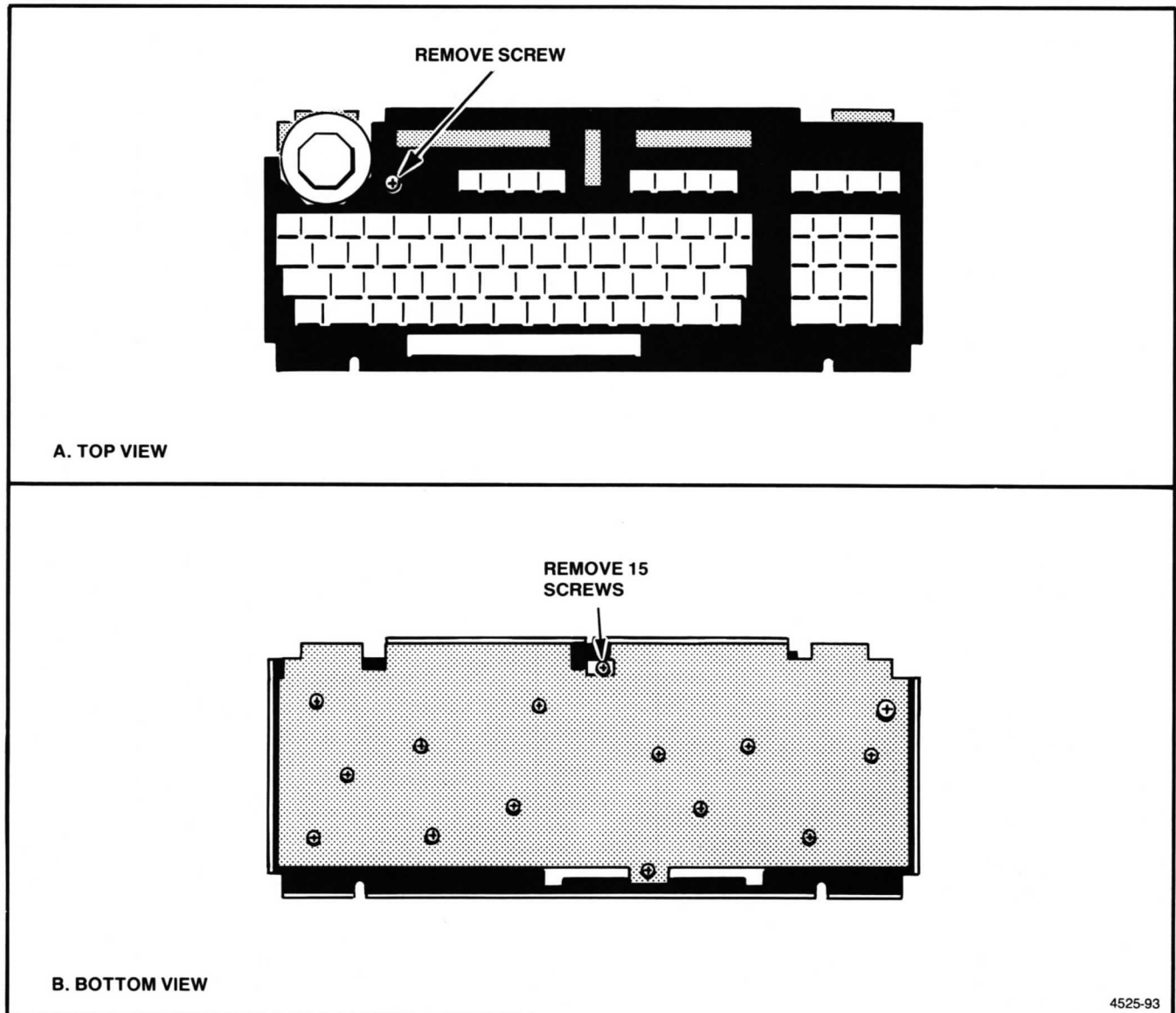


Figure 6-17. Keyboard Circuit Board Mounting Screws.

Replacing Keyboard Key Caps

A key cap may be removed by simply pulling straight up on the key. A gripping device, such as a rubber glove, may facilitate removal of key caps from their switches. It is not necessary to remove the keyboard from the terminal to replace a keycap.

1. Position the key so that its nomenclature is pointing in the proper direction (not upside down or sideways). See Figure 6-18.
2. Then insert the fork (under cap) into the receptacle in the key switch plunger. Be sure the spring is still in place (around the plunger). Push the keycap all the way onto the switch so that it rests level with the other keys, when released.

NOTE

The BREAK key has a stronger spring. This feature prevents the touch-typist from accidentally exiting a program while typing.

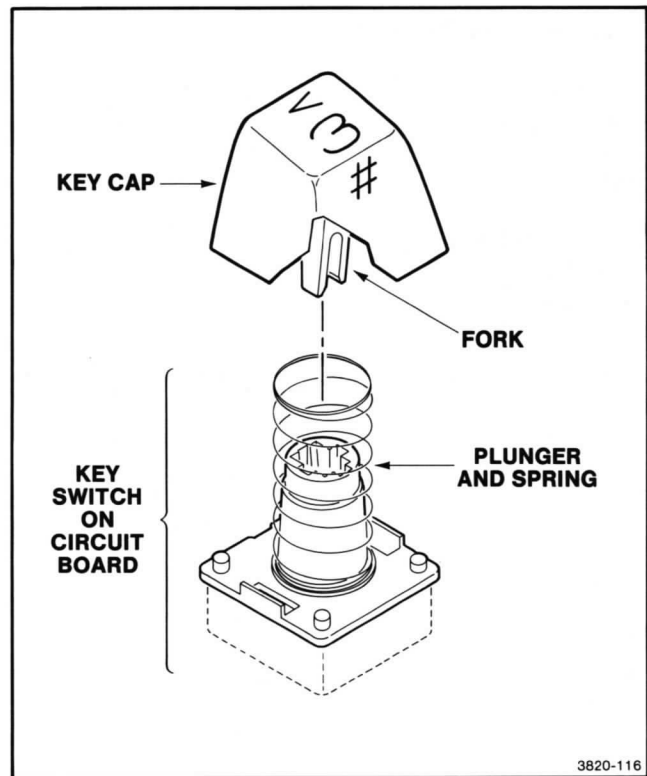


Figure 6-18. Installing Replacement Key Cap.

Replacing the Joydisk

The Joydisk mounts on the keypad assembly with a pivot, screw, nut, and spring. The spring holds tension between the pivot point and the nut (that threads onto the screw). See Figure 6-19.

To remove the Joydisk, unscrew the nut by hand. This provides access to the capacitive pads for cleaning or replacement.

When installing the Joydisk, place the disk so its screw goes into the hole in the keypad. Then place the spring over the screw, and thread the nut onto the screw (compressing the spring). Adjust the spring tension by setting the nut to a distance of .240 inch from the keypad bottom surface. See Figure 6-19 again.

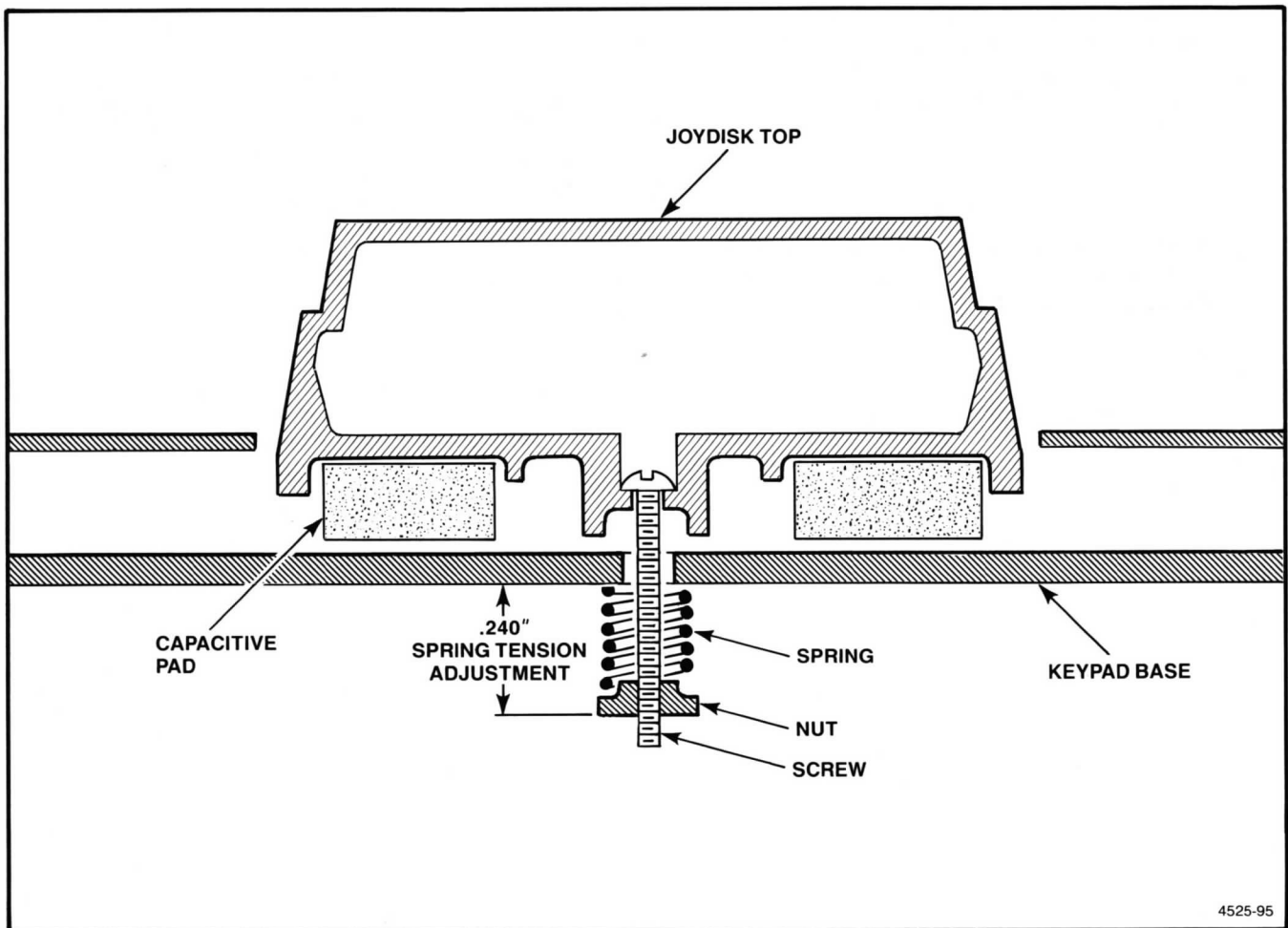


Figure 6-19. Installing the Joydisk and Adjusting the Spring Tension.

TROUBLESHOOTING AND CORRECTIVE MAINTENANCE

Fault isolation for the 4107 is best handled in the following manner. Carefully observe all symptoms of the problem and list them. Check the main user functions (Section 3) and note any problems. Then run Self Test and record the error message(s) displayed on the screen. (If the Display Module doesn't work, a crude message appears on the LEDs inside the back of the terminal.) After discovering which main module is malfunctioning, remove, repair, and replace it.

SELF TEST DIAGNOSTIC ROUTINE

Appendix C contains a complete description of the Self Test diagnostic program, and a list with explanations of all error messages. This program is designed such that the operator may run Self Test and report the findings to the local service center. This facilitates trouble shooting by narrowing the problem before the technician arrives.

The primary error reporting device is the display screen; all error messages are sent to the screen. If the display is faulty, no messages will appear while Self Test is running, but the bell will ring and LEDs may flash. This clue indicate bad Display Module.

INITIAL/VISUAL CHECKS

Aside from Self Test certain simple visual tests may help isolate a problem to the functional block level. The following basic suggestions help when trouble shooting the 4107.

Display Module Problems

The Display Module uses three-color, raster-scan technology, and is much like the display section of most color television receivers. Display problems may be grouped as follows:

- Blank screen – can mean
 - burned out filament in CRT, or
 - loss of 25KV high voltage to CRT, or
 - loss of low voltage to accelerating anodes of CRT (from LV power supply module). If high voltage is low, check multiplier circuits.
- Low contrast – Check video amplifier stages and condition of CRT.
- Dot of light – Check the horizontal and vertical deflection circuits.
- Only a horizontal line – Check the vertical deflection circuitry.
- Vertical line only (no deflection) – Check horizontal deflection circuits.
- Raster on screen but no information – Check the data path through the video amplifier sections.
- No color (only black and white) – Check the programming of the Color Map. (If white is pure, this means all three color guns are operational.)

These are customary checks when troubleshooting a color raster display.

COMPONENT LEVEL REPAIR PROCEDURES

The use of Self Test and visual checks should provide fault isolation to the board/module level. Normally the defective board/module is sent to a regional service center where component level repairs are performed with ease. If on-site component repairs are necessary, follow these helps.

- Check the power inputs to various chips on the board to verify that +5V or +12V is reaching all parts of the board. (First, verify that power supply works).
- Examine the board for obvious signs of excessive heat (especially on analog or discrete circuitry, such as the Display Module boards and power supply board).
- If the bell fails, examine/replace the small round transducer, located just above the processor (on the Terminal Control board).
- Replace the CRT if one gun fails. See procedure earlier in this section.

NOTE

Certain components, such as High-Voltage supplies or high-efficiency circuits, may produce excessive and harmful radiation if replaced by non-Tektronix parts. Such components are identified in the electrical parts list (Section 9).

Section 7

OPTIONS

LIST OF OPTIONS

Table 7-1 lists the 4107 options in numerical order. Option numbers beginning with an alpha designation are grouped at the end of the table.

Table 7-1
4107 OPTIONS

Option #	Description
Option 4A	United Kingdom keyboard option
Option 4B	French keyboard option
Option 4C	Swedish keyboard
Option 4F	Danish/Norwegian keyboard
Option 4G	German keyboard
Power Cord Options:	
Option A1	European Power Cable (220V)
Option A2	U.K. Power Cable (240V)
Option A3	Australian Power Cable (240V)
Option A4	North America Power Cable (240V)
Option A5	Swiss Power Cable (240V)

NOTE

The ADS01 (Adjustable Display Stand) is not defined as an option. However, this product is intended for use with the 4107. It provides tilt-elevate-glide movement of the display unit (for optimum viewing of the screen). See the separate manual for this auxiliary product.

OPTIONS 4A-4F INSTALLATION PROCEDURES

Five optional keyboards are available for this terminal:

- Option 4A – United Kingdom Keyboard
- Option 4B – French Keyboard
- Option 4C – Swedish Keyboard
- Option 4F – Danish/Norwegian
- Option 4G – German

Changing a standard (North American) keyboard to one of the optional keyboards is accomplished by exchanging keyboard units.

First, unplug the cable of the standard keyboard from its connector on the back of the display unit.

Then, plug the cable from the optional keyboard into the same connector.

(No change in EEPROMs is required.)

Section 8

INSTALLATION

This section covers unpacking, installing, and checkout of the 4107 terminal. This section also provides repackaging instructions if reshipment of the terminal is necessary.

Installation consists of unpacking the terminal, checking for correct options and accessories, checking operating voltage and fuse selection, connecting the terminal to a host computer, applying power, running Self Test, and verifying communications between the host computer and the terminal.

The terminal is preassembled and requires no assembly for initial installation. The only options to the terminal are external, and do not require disassembly of the terminal. Installation of optional keyboards and the Adjustable Display Stand are described later in this section.

UNPACKING THE TERMINAL

You may want to refer to Figure 8-5 to see how the pieces are arranged inside the shipping carton. Then, follow this procedure:

WARNING

Lifting awkward or heavy objects can cause personal injury. When moving the shipping carton or the terminal, be sure to use recommended safe lifting methods (or have an assistant help) to avoid back injury.

1. Cut the strapping bands from the carton.
2. Slide the Top Cover from over the foam pads.

3. Remove the Keyboard Container box and the Accessory Box.
4. Lift the 4107 free of the carton and inspect for obvious damage.
5. **RETAIN THE PACKING MATERIALS** in case shipping damage requires repackaging for repair; see repackaging instructions at the end of this section.
6. Remove the accessories from the Accessory Box, and see that the enclosed packing list corresponds to included standard accessories and ordered optional accessories.

Standard accessories included with the 4107 are:

- *4107/4109 Operator's Manual*
- Power cord (U.S., U.K., Australian, or European)
- Keyboard module with connecting cord (North American, U.K., French, Danish/Norwegian, Swedish, German, or Katakana).
- *4107/4109 Reference Guide*
- *4107/4109 Programmer's Reference Manual*
- Function Key Overlays

Optional accessories available include:

- *4107 Service Manual*
- *Display Module for 4107, Service Manual*
- RS-232 Host Port cable
- RS-232 Loop-back connector
- Copier Port Loop-back connector
- Display screen alignment graticule

INSTALLATION

INSTALLATION PROCEDURE

Installation of the terminal does not require accessing any internal parts. Only qualified service technicians should open the terminal's cover; in such cases all cautions and warnings must be observed.

WARNING

Dangerous voltages exist within the terminal. Normal electrical precautions should be observed whenever working inside the terminal.

SITE SELECTION

The 4107 is intended for use in normal office or research/design environments. Tektronix terminals are engineered to withstand semi-harsh operating environments; see Section 2 (Specification) for detailed operating limits.

The 4107 will operate in a temperature environment between +10°C and +40°C. The 4107's maximum heat dissipation is 590 BTU/hour; this information may be used to calculate loading on the air-conditioning system (significant only when installing a large number of terminals).

Provide a power source that allows surge currents of 55 A (at nominal 120V line voltage).

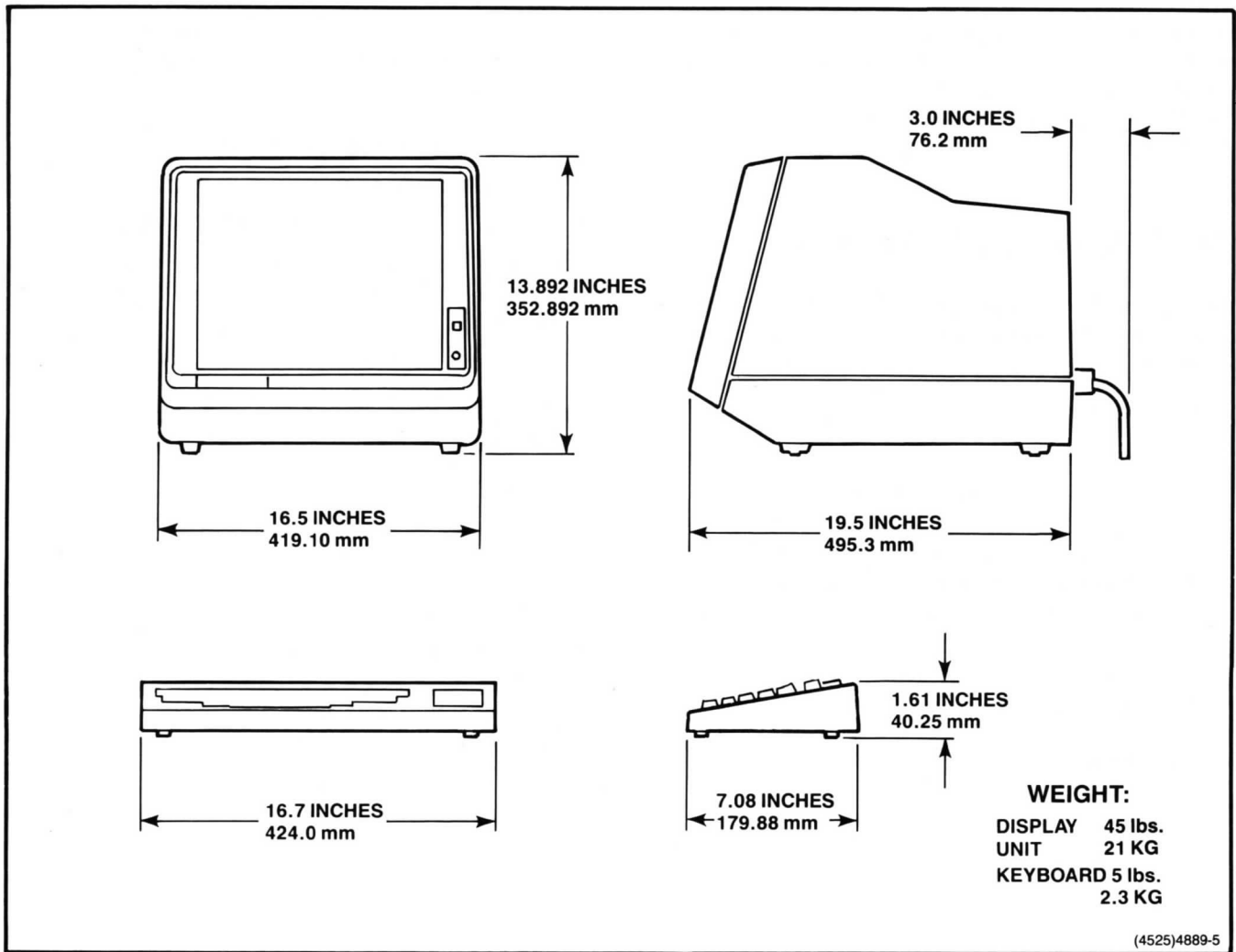


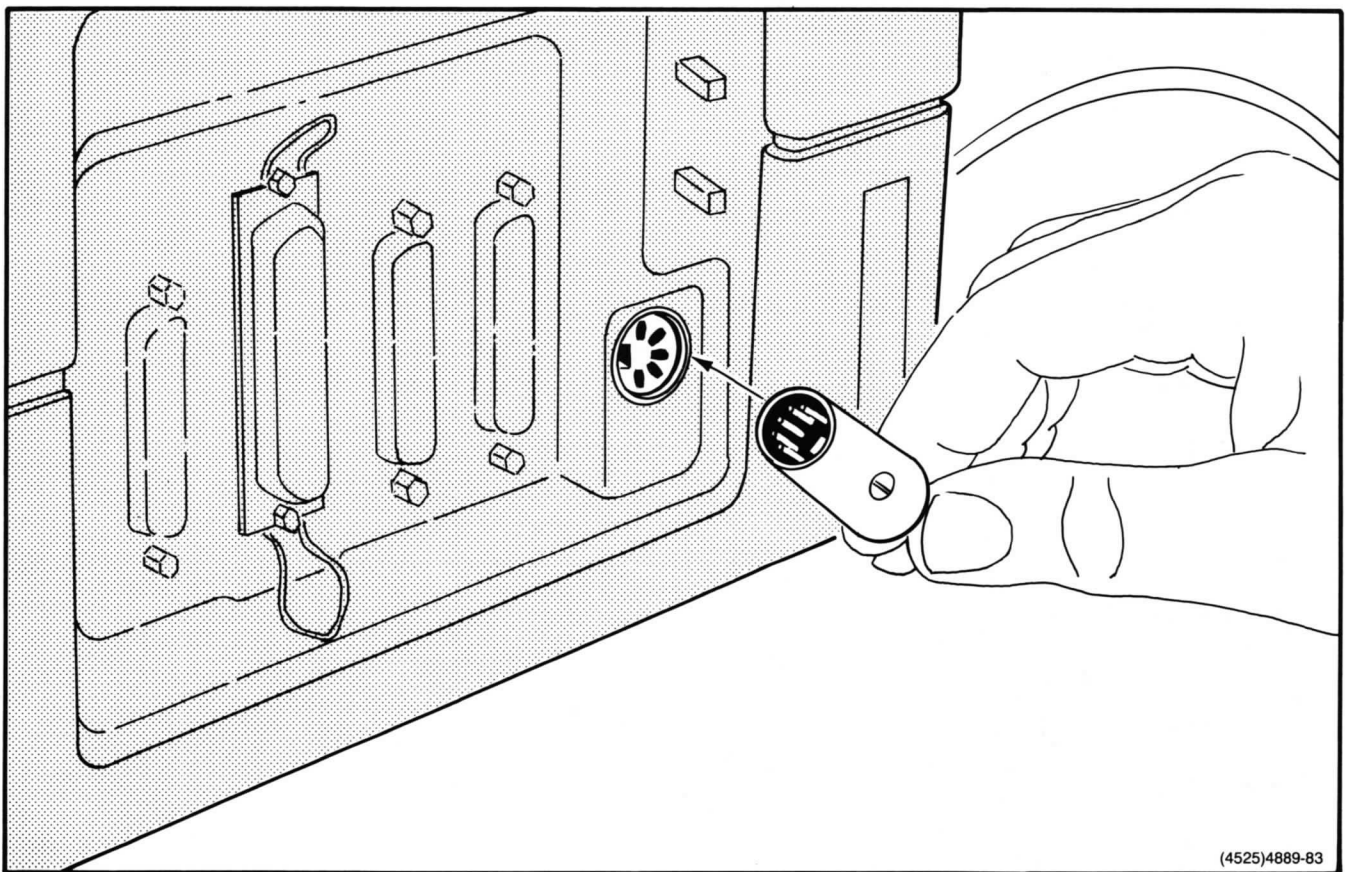
Figure 8-1. 4107 Overall Physical Dimensions.

Once the terminal is unpacked, place it on a stable desktop or the place it is to be used. Figure 8-1 shows the dimensions of the 4107. This figure may be used to determine how much space is needed for the terminal. Notice that the Adjustable Display Stand adds to these dimensions.

Allow at least 3 inches of clearance behind the 4107, to ensure adequate cooling. Also, the 4107 should not be placed near other equipment containing large motors, fans, or other electromagnetic devices. Large magnetic fields will distort the display image.

CONNECTING THE KEYBOARD CABLE

The keyboard is a separate unit and passes data and power to/from the terminal through its coiled cable. This cable connects to the rear of the terminal. Align the connector keyslot and prongs; then insert the cord connector (male) into the jack (female) labeled KBD, on the terminal. See Figure 8-2.



(4525)4889-83

Figure 8-2. Rear Panel and Keyboard Cable Connector.

INSTALLATION

CONNECTING TO THE HOST COMPUTER

Connect the RS-232 cable to the Host Port connector on the rear of the 4107. Connect the other end of this cable to the modem or other computer connection. Access an active port to the host system.

CONNECTING TO PERIPHERALS

Before connecting any peripheral device to the 4107, read the installation instructions and setup information in that peripheral's operators manual. Some peripherals make use of the programmable keys on the 4107 to execute certain operations in the peripheral (such as copying part of the display). Become familiar with such information.

Connect those devices that use an RS-232-C interface to the 4107 peripheral ports labeled, PORT 0 and PORT 1 (on the rear panel). See Figure 8-3. Such peripherals include TEKTRONIX 4660-series plotters, and the TEKTRONIX 4957 graphics tablet.

1. Plug the RS-232 cable into PORT 0 (or PORT 1).
2. Screw the plug-fasteners into each end of the RS-232 connector.

The TEKTRONIX 4690-series copiers/printers use a Centronics-type interface. Connect this type of peripheral device to the 4107 connector labeled: COPIER. This connector has two bails; slip them over the plug, securing it to the terminal. See Figure 8-4.

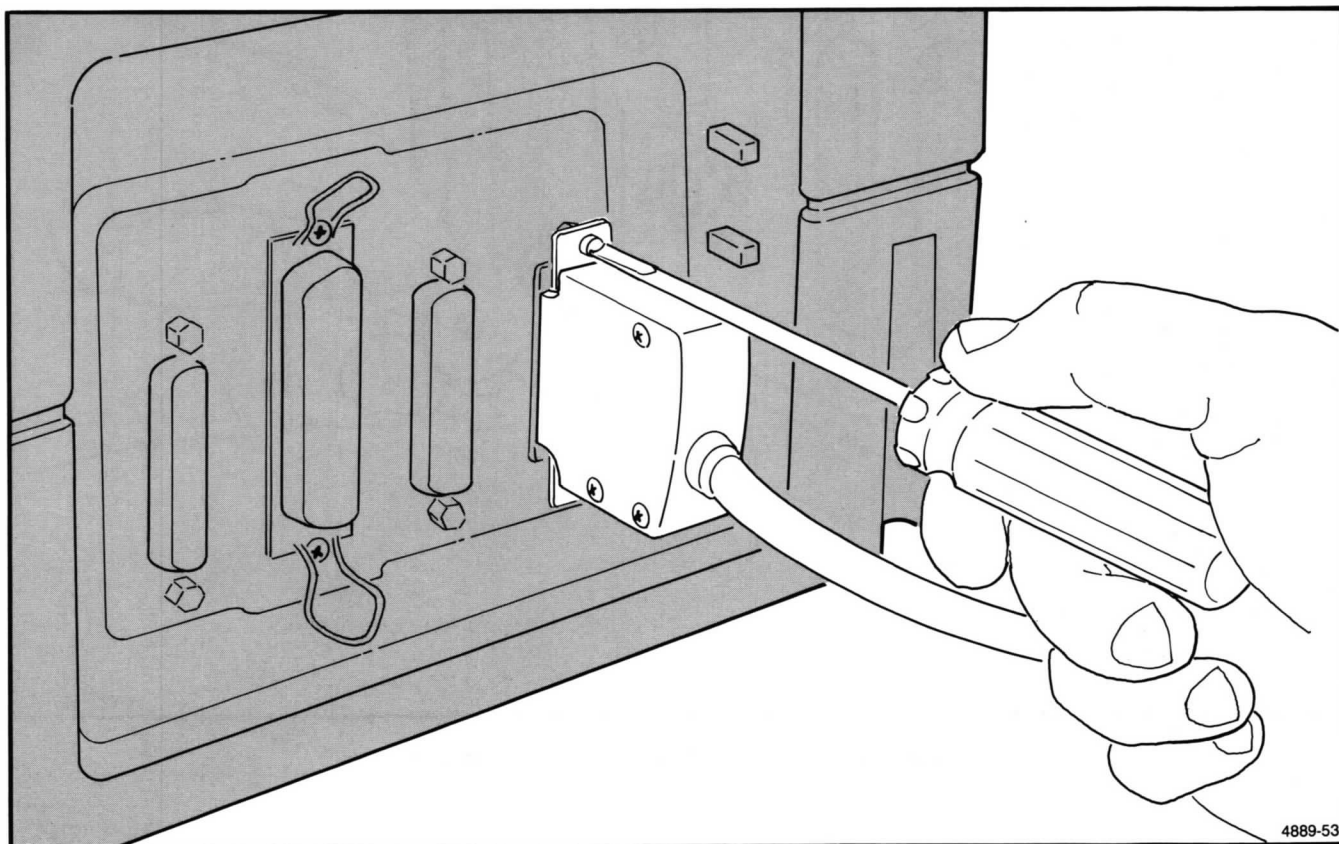


Figure 8-3. Connecting an RS-232 Cable to Peripheral Port 1.

APPLYING POWER

Before applying power, check the settings of the voltage selector switches. See that both voltage selector switches (on the rear panel) match the nominal voltage level of the AC power outlet that will supply the terminal.

Power is applied to the 4107 by plugging the female end of the power cord into the AC power socket on the back of the terminal. Then plug the male end of the same cord into the AC power outlet. Now, turn on the 4107 by pressing the power button located near the lower right corner of the display screen. After the power is turned on, a cursor should appear in the upper left corner of the display screen.

After power is turned off, wait 5 seconds before turning power on again. This allows time for capacitors to discharge so the 4107 will reset properly on power up.

RUNNING SELF TEST

The 4107 is connected to the computer and has power applied. However, you should run the Self Test program before logging onto the computer. This will verify that the terminal is functioning properly. Refer to Appendix C for explanations of any error messages that may appear on the screen. When Self Test is finished and all circuitry proves good, the cursor will blink in the upper left corner of the screen. It is ready for operation.

USING THE TERMINAL

Now you may log onto the host computer and use the 4107 as a terminal. Section 3, Operating Information, provides a complete explanation of how to use the terminal, once it is operational. You should use several system commands to satisfy yourself that the 4107 performs as expected.

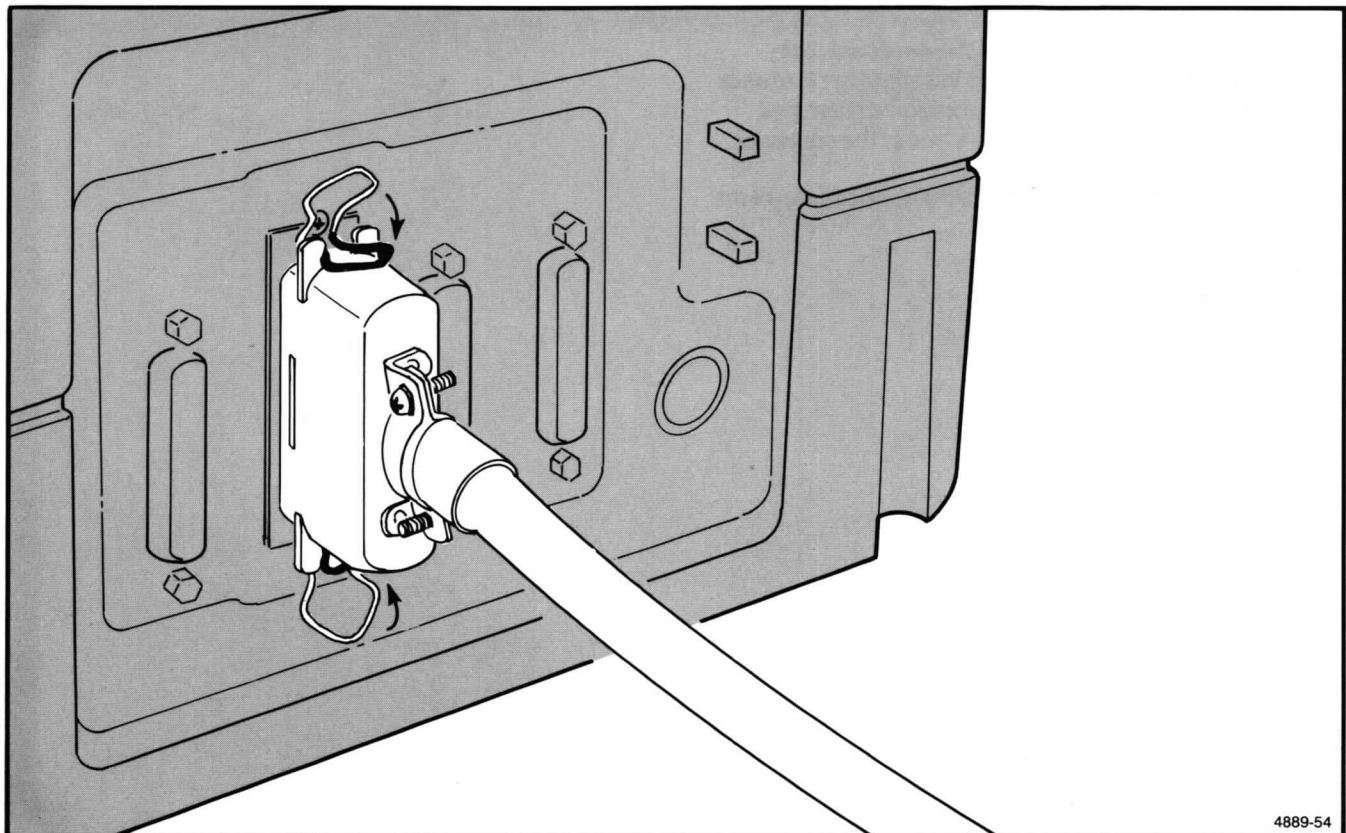


Figure 8-4. Connecting the Centronics-type Plug into COPIER Connector.

4889-54

INSTALLATION

REPACKAGING THE TERMINAL

In the event that the 4107 needs to be shipped, for servicing or to be used in a different location, follow this repackaging procedure. Study Figure 8-5 along with the procedure.

1. Place the cardboard Bottom Tray (F) on a convenient work surface.
2. Place the foam Bottom Pad (E) on the Bottom Tray (F).
3. Place all manuals, cords and other needed accessories in the Accessory Box (D). Ship only the items that are needed at the destination. Then place this box in the cutout at one end of the Bottom Pad.
4. Unplug all cords from the 4107. Then, place the 4107 in its cutout in the Bottom Pad; the 4107 faces away from the Accessory Box.
5. Place the foam Top Pad (C) over the 4107.
6. Place the Keyboard Module in the Keyboard Container(B). The keys face up and the spacebar is toward the lid hinge. The cord passes through a notch and rests in a pocket across the front end of the container.
7. Place the Keyboard Container in its cutout on top of the Top Pad (C).
8. Place the cardboard Cover Carton (A) over the top of the foam pads (face down), and slide it down. The open edges of the carton slide inside the lips on the Bottom Tray (F).
9. Wrap the assembled carton with Strapping Bands (G). Marks on the carton show where to place these bands.
10. Label the carton with: model number, serial number, and source and destination as required.

This completes the procedure.

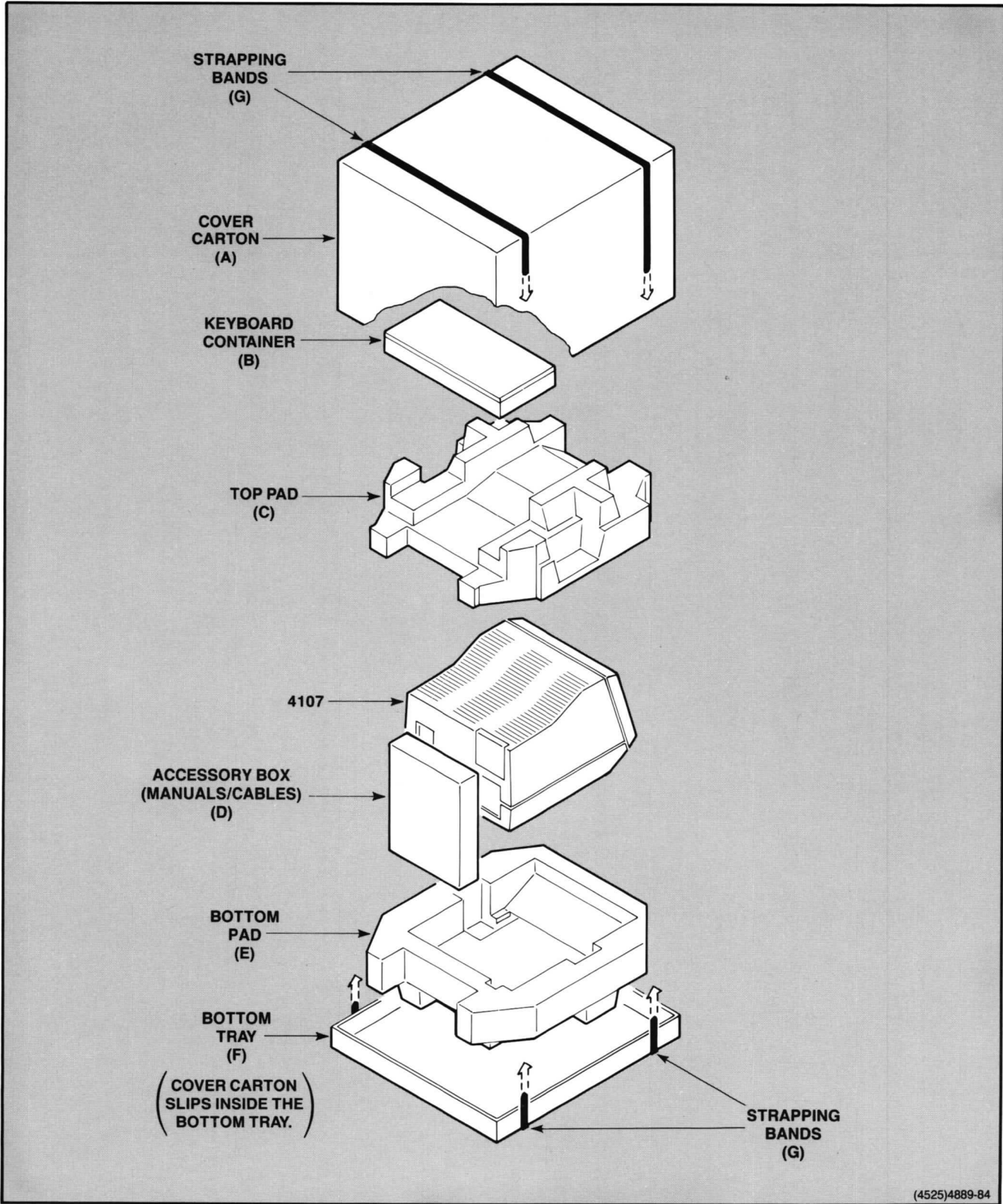


Figure 8-5. Repackaging Diagram.

Section 9

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

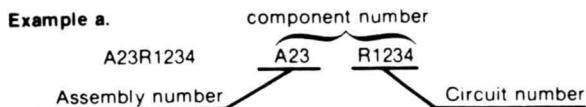
The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

ABBREVIATIONS

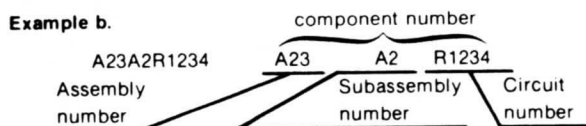
Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:



Read: Resistor 1234 of Assembly 23



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

REPLACEABLE ELECTRICAL PARTS

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000JB	STAR MICRONICS INC.	200 PARK AVE SUITE 08	NEW YORK, NY 10166
000LI	TOPTRON CORP		TOKYO, JAPAN
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02113	COILCRAFT INC.	1102 SILVER LAKE RD.	CARY, IL 60013
02660	BUNKER RAMO CORP., CONNECTOR DIVISION	2801 S 25TH AVENUE	BROADVIEW, IL 60153
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
13606	SPRAGUE ELECTRIC CO. TRANSISTOR DIV.	PEMBROKE RD.	CONCORD, NH 03301
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
22753	U. I. D. ELECTRONICS CORP.	4105 PEMBROKE RD.	HOLLYWOOD, FL 33021
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
32694	OPTRON, INC.	1201 TAPPAN CIRCLE	CARROLLTON, TX 75006
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50364	MONOLITHIC MEMORIES	1165 E ARQUES AVENUE	SUNNYVALE, CA 94086
52833	KEYTRONIC CORP., OCR DIV.	SPOKANE INDUSTRIAL PK., P. O. BOX 14687	SPOKANE, WA 99214
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
53848	SMC MICROSYSTEMS CORP.	35 MARCUS BLVD.	HAUPPAUGE, NY 11787
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
59821	CENTRALAB INC	7158 MERCHANT AVE	EL PASO, TX 79915
60705	SUB NORTH AMERICAN PHILIPS CORP		
71400	CERA-MITE CORP. BUSSMAN MFG., DIVISION OF MCGRAW- EDISON CO.	1327 6TH AVE. 2536 W. UNIVERSITY ST.	GRAFTON, WI 53024 ST. LOUIS, MO 63107
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
81312	WINCHESTER ELECTRONICS DIVISION		
82389	LITTON INDUSTRIES, INC.	MAIN ST. AND HILLSIDE AVE.	OAKVILLE, CT 06779
91637	SWITCHCRAFT, INC.	5555 N. ELSTON AVE.	CHICAGO, IL 60630
T0016	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
T0032	FUJITSU-AMERICA, INC.	1208 E. ARQUES AVENUE	SUNNYVALE, CA 94086
T1043	POWELL ELECTRONICS	411 FAIRCHILD DR.	MT. VIEW, CA 94040
	DALE ELECTRONICS CORP	PO BOX 3164	TEMPE, AZ 85282

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscnt	Name & Description	Mfr Code	Mfr Part Number
CIRCUIT BOARD ASSEMBLIES					
A1	670-8234-00		CKT BOARD ASSY:TERMINAL CONTROL	80009	670-8234-00
A2	670-8233-00		CKT BOARD ASSY:DISPLAY CONTROL	80009	670-8233-00
A3	670-7196-00		CKT BOARD ASSY:RAM THREE	80009	670-7196-00
A4	119-1592-01		KEYBOARD ASSY:4107		
A4	119-1619-01		KEYBOARD ASSY:UNITED KINGDOM		
A4	119-1618-01		KEYBOARD ASSY:FRENCH		
A4	119-1621-01		KEYBOARD ASSY:SWEDISH		
A4	119-1620-01		KEYBOARD ASSY:DANISH/NORWEGIAN		
A4	119-1622-01		KEYBOARD ASSY:GERMAN		
A4	119-1678-01		KEYBOARD ASSY:KATAKANA		
A4A1	118-2975-01		KEYBOARD:W/O ENCLOSURE	80009	118-2975-00
A4A1	-----		(STANDARD ONLY)		
A4A1	118-3276-01		KYBD ASSY:UNITED KINGDOM	80009	118-3276-00
A4A1	-----		(OPTION 4A ONLY)		
A4A1	118-3277-01		KYBD ASSY:DANISH/NORWEGIAN	80009	118-3277-00
A4A1	-----		(OPTION 4F ONLY)		
A4A1	118-3278-01		KYBD ASSY:SWEDISH	80009	118-3278-00
A4A1	-----		(OPTION 4C ONLY)		
A4A1	118-3280-01		KYBD ASSY:FRENCH	80009	118-3280-00
A4A1	-----		(OPTION 4B ONLY)		
A4A1	118-1678-01		KYBD ASSY:KATAKANA	80009	119-1678-00
A4A1	-----		(OPTION 4K ONLY)		
A5	620-0005-00		POWER SUPPLY:	80009	620-0005-00
A1 TERMINAL CONTROL BOARD					
A1	670-8234-00		CKT BOARD ASSY:TERMINAL CONTROL	80009	670-8234-00
A1C20	285-1257-00		CAP.,FXD,PLSTC: 0.0056UF,1%,200V	13606	192P56292
A1C25	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C26	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1C30	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C31	290-0804-00		CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A1C35	281-0773-00		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C40	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C50	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C60	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C70	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C80	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C90	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C125	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C130	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C135	283-0144-00		CAP.,FXD,CER DI:33PF,1%,500V	59660	801-547P2G330G
A1C140	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C145	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1C150	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C160	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C170	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C180	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C190	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C235	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C240	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscnt	Name & Description	Mfr Code	Mfr Part Number
A1C245	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C250	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C255	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C260	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C265	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1C270	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C275	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C280	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C285	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C290	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C335	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C340	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C345	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C375	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C380	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C425	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1C435	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C437	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C440	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C445	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C495	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1C496	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C497	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C535	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C540	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C545	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C594	283-0167-00		CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A1C598	283-0167-00		CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A1C599	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A1CR20	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR31	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR33	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR395	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR396	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR397	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR481	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR482	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR486	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR491	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR525	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR526	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR527	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR528	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR596	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR597	152-0141-02		SEMICONV DEVICE:SILICON,30V,150MA	01295	1N4152R
A1DS273	150-1036-00		LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A1DS275	150-1036-00		LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A1DS280	150-1036-00		LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A1J13	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	81312	96S-6043-0731-0
A1J21	131-2898-00		CONN,RCPT,ELEC:PCB MOUNT,36 CONTACT	02660	57-40360-22-398
A1J22	131-0813-00		CONN,RCPT,ELEC:CKT BD,25 CONT,FEM	80009	131-0813-00
A1J25	131-1741-00		CONN,RCPT,ELEC:PCT MOUNT,5 CONTACT	80009	131-1741-00
A1J28	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	81312	96S-6043-0731-0

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A1L597	108-0474-00		COIL,RF:2UH	80009	108-0474-00
A1L599	108-0474-00		COIL,RF:2UH	80009	108-0474-00
A1LS20	119-1427-00		XDCR,AUDIO:6V,30MA,1-4.2 KHZ	000JB	QMB-06
A1P11	131-2908-00		CONN,RCPT,ELEC:CKT BD,1 X 10,0.156	27264	09-62-3102
A1P20	131-0971-00		CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	71468	DB25-SH
A1P23	131-0971-00		CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	71468	DB25-SH
A1Q38	151-0220-00		TRANSISTOR:SILICON,PNP	07263	S036228
A1Q39	151-0220-00		TRANSISTOR:SILICON,PNP	07263	S036228
A1Q135	151-0220-00		TRANSISTOR:SILICON,PNP	07263	S036228
A1R20	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R21	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R33	321-0217-00		RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	MFF1816G17800F
A1R34	321-0227-00		RES.,FXD,FILM:2.26K OHM,1%,0.125W	91637	MFF1816G22600F
A1R37	315-0511-00		RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R38	315-0511-00		RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R39	315-0122-00		RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A1R130	315-0122-00		RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A1R131	315-0221-00		RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R134	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R135	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R137	315-0330-00		RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A1R150	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R240	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R251	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R252	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R253	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R285	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R286	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R287	315-0821-00		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R295	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R350	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R351	315-0821-00		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R355	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R356	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R357	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R358	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R359	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R360	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R361	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R362	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R363	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R364	315-0100-00		RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R370	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R371	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R395	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R396	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R397	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R398	315-0151-00		RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A1R399	315-0821-00		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R426	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R427	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscnt	Name & Description	Mfr Code	Mfr Part Number
A1R435	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R436	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R437	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R438	315-0511-00		RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R445	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R446	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R447	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R448	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R449	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R450	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R473	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R474	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R475	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R480	315-0821-00		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R483	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R484	315-0681-00		RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A1R485	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R490	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R491	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R591	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1S490	260-2111-00		SWITCH,PUSH:1 BUTTON,1 POLE,BEAM FIND	59821	ORD BY DESCR
A1S493	260-2111-00		SWITCH,PUSH:1 BUTTON,1 POLE,BEAM FIND	59821	ORD BY DESCR
A1U25	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U30	156-1735-00		MICROCIRCUIT,DI:NMOS,2048 X 8 EPROM		
A1U36	156-1631-00		MICROCIRCUIT,LI:ADJ SHUNT REGULATOR	01295	TL431C-LP
A1U40	156-1734-00		MICROCIRCUIT,DI:8192 X 8 PSUEDO STATIC RAM		
A1U50	156-1734-00		MICROCIRCUIT,DI:8192 X 8 PSUEDO STATIC RAM		
A1U60	160-2379-01		MICROCIRCUIT,DI:16384 X 8 EPROM,PROGRAMMED	80009	160-2379-01
A1U70	160-2377-01		MICROCIRCUIT,DI:16384 X 8 EPROM,PROGRAMMED	80009	160-2377-01
A1U80	160-2375-01		MICROCIRCUIT,DI:32768 X 8 EPROM,PROGRAMMED	80009	160-2375-01
A1U90	160-2373-01		MICROCIRCUIT,DI:32768 X 8 EPROM,PROGRAMMED	80009	160-2373-01
A1U125	156-1841-00		MICROCIRCUIT,DI:16 BIT MICROPROCESSOR,68 P	34649	80186
A1U135	156-0323-02		MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A1U140	156-1734-00		MICROCIRCUIT,DI:8192 X 8 PSUEDO STATIC RAM		
A1U150	156-1734-00		MICROCIRCUIT,DI:8192 X 8 PSUEDO STATIC RAM		
A1U160	160-2380-01		MICROCIRCUIT,DI:16384 X 8 EPROM,PROGRAMMED	80009	160-2380-01
A1U170	160-2378-01		MICROCIRCUIT,DI:16384 X 8 EPROM,PROGRAMMED	80009	160-2378-01
A1U180	160-2376-01		MICROCIRCUIT,DI:32768 X 8 EPROM,PROGRAMMED	80009	160-2376-01
A1U190	160-2374-01		MICROCIRCUIT,DI:32768 X 8 EPROM,PROGRAMMED	80009	160-2374-01
A1U235	156-1258-01		MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A1U240	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U245	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U250	156-0180-04		MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00NP3
A1U255	156-1724-00		MICROCIRCUIT,DI:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A1U260	156-1855-00		MICROCIRCUIT,DI:STTL,BUS INTERFACE LATCHES		
A1U265	156-1570-01		MICROCIRCUIT,DI:PRDM PRPHL INTFC	34335	AM8255A-5 P/D CB
A1U275	156-0467-02		MICROCIRCUIT,DI:QUAD 2-INP NAND BFR,SCRN	01295	SN74LS38
A1U280	156-0388-03		MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A1U285	156-0878-01		MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A1U290	156-1737-00		MICROCIRCUIT,DI:DUAL ASNCHRONUS RECEIVER		
A1U335	156-0321-02		MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A1U340	160-1953-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	50364	160-1953-00 HAL1

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U345	156-0462-02			MICROCIRCUIT,DI:HEX INVERTER,SCREENED	01295	SN7414
A1U375	156-1080-01			MICROCIRCUIT,DI:HEX BUFFERS U/OC HV	27014	DM7407
A1U380	156-0462-02			MICROCIRCUIT,DI:HEX INVERTER,SCREENED	01295	SN7414
A1U385	156-0878-01			MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A1U435	156-1724-00			MICROCIRCUIT,DI:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A1U437	156-1737-00			MICROCIRCUIT,DI:DUAL ASNCHRONUS RECEIVER		
A1U440	156-0878-01			MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A1U445	156-0878-01			MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A1U495	156-0879-01			MICROCIRCUIT,DI:QUAD LINE DRIVER,SCRN	80009	156-0879-01
A1U535	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A1U540	156-0879-01			MICROCIRCUIT,DI:QUAD LINE DRIVER,SCRN	80009	156-0879-01
A1U545	156-0879-01			MICROCIRCUIT,DI:QUAD LINE DRIVER,SCRN	80009	156-0879-01
A1VR490	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A1Y485	119-1591-00			OSC,XTAL CLOCK:14.7456MHZ,0.01%	T1043	X033-B-14.7456

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2 DISPLAY CONTROL BOARD						
A2	670-8233-00			CKT BOARD ASSY:DISPLAY CONTROL	80009	670-8233-00
A2C1	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A2C115	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C125	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C131	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C147	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C161	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C171	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C185	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C201	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C207	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C215	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C221	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C227	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C231	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C247	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C261	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C271	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C285	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C301	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C307	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C327	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C347	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C361	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C371	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C401	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C407	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C415	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C425	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C431	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C447	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C461	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C471	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C501	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C507	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C513	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A2C525	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C531	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C533	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C547	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C601	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C607	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C615	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C635	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A2C647	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C655	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C657	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C661	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C671	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C681	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C701	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C707	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscnt	Name & Description	Mfr Code	Mfr Part Number
A2C715	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C720	290-0745-00		CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A2C725	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C731	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C735	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C737	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C801	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C805	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C807	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C811	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C815	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C825	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C831	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C857	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C871	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2C881	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A2DS87	150-1029-00		LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
A2J31	131-3092-00		CONN,RCPT,ELEC:HEADER,2 X 10,VERTICAL		
A2J37	131-3154-00		CONN,RCPT,ELEC:CKT BD,RTANG,2 X 20,MALE		
A2P35	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR,0.125	81312	96P-6043-0723-3
A2P39	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR,0.125	81312	96P-6043-0723-3
A2R162	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R163	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R167	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R168	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R172	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R173	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R218	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R231	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R258	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R259	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R362	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R363	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R364	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R421	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R431	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R531	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R533	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R554	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R576	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R577	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R751	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R765	315-0470-00		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A2R886	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A2R887	315-0472-00		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2U101	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U105	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U107	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U111	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2U115	160-2382-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2382-00
A2U121	156-1933-00		MICROCIRCUIT,DI:16 BIT SHIFT REGISTER		
A2U125	156-1761-00		MICROCIRCUIT,DI:16:1 MUX,SCRN		
A2U127	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U131	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U135	156-0469-02		MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A2U137	156-1935-00		MICROCIRCUIT,DI:SYNCHRONOUS PRESETTABLE BIN		
A2U141	156-1702-00		MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U147	160-2386-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2386-00
A2U155	160-2385-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2385-00
A2U161	156-1743-00		MICROCIRCUIT,DI:QUAD 2 INPUT NOR GATE	07263	74F02(PCQR OR DC
A2U165	156-1722-00		MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A2U167	156-0479-02		MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A2U171	156-0479-02		MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A2U175	156-1080-01		MICROCIRCUIT,DI:HEX BUFFERS U/OC HV	27014	DM7407
A2U181	160-2393-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2393-00
A2U185	156-1839-00		MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U187	156-0982-03		MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A2U201	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U205	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U207	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U211	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U215	160-2383-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2383-00
A2U217	156-1957-00		MICROCIRCUIT,DI:DUAL 4 INPUT NAND GATE	04713	74F20 NDS OR JDS
A2U221	156-0530-02		MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A2U225	160-2392-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2392-00
A2U231	156-1702-00		MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U235	156-1935-00		MICROCIRCUIT,DI:SYNCHRONOUS PRESETTABLE BIN		
A2U237	156-1935-00		MICROCIRCUIT,DI:SYNCHRONOUS PRESETTABLE BIN		
A2U241	156-1702-00		MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U247	160-2384-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2384-00
A2U251	156-1839-00		MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U255	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U257	156-1611-00		MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A2U261	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U265	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U267	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U271	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U275	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U281	156-1934-00		MICROCIRCUIT,DI:64 BIT RANDOM ACCESS MEMORY		
A2U285	156-1839-00		MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U287	156-0982-03		MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A2U301	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U305	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U307	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U311	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U335	156-1273-01		MICROCIRCUIT,DI:8 BIT EQUAL TO COMPTR,SCRN	80009	156-1273-01
A2U337	156-1935-00		MICROCIRCUIT,DI:SYNCHRONOUS PRESETTABLE BIN		
A2U347	160-2394-00		MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2394-00
A2U351	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U355	156-1839-00		MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U357	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U361	156-1743-00		MICROCIRCUIT,DI:QUAD 2 INPUT NOR GATE	07263	74F02(PCQR OR DC
A2U365	156-1722-00		MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2U367	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2U371	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2U375	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U381	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A2U385	156-1736-00			MICROCIRCUIT,DI:HIGH PERFORMANCE BUS INTERF		
A2U387	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A2U401	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U405	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U407	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U411	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U415	160-2387-00			MICROCIRCUIT,DI:ARRAY LOGIC,PRGM	80009	160-2387-00
A2U421	156-1933-00			MICROCIRCUIT,DI:16 BIT SHIFT REGISTER		
A2U425	156-1761-00			MICROCIRCUIT,DI:16:1 MUX,SCRN		
A2U427	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U431	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U435	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A2U437	156-1273-01			MICROCIRCUIT,DI:8 BIT EQUAL TO COMPTR,SCRN	80009	156-1273-01
A2U441	156-1702-00			MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U447	156-1723-00			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE	07263	74F08
A2U451	156-1744-00			MICROCIRCUIT,DI:ASTTL,OCTAL BUFFER/LINE	07263	74F240
A2U455	156-1744-00			MICROCIRCUIT,DI:ASTTL,OCTAL BUFFER/LINE	07263	74F240
A2U457	156-1704-00			MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U461	156-1722-00			MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A2U465	156-1963-00			MICROCIRCUIT,DI:NONINVERTING R		
A2U467	156-1839-00			MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U471	156-1839-00			MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U475	156-1839-00			MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U487	156-1723-00			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE	07263	74F08
A2U501	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U505	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U507	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U511	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U515	156-1740-00			MICROCIRCUIT,DI:OCTAL DYNAMIC MEM DRIVER	34335	AM2968DCB
A2U521	156-1933-00			MICROCIRCUIT,DI:16 BIT SHIFT REGISTER		
A2U525	156-1761-00			MICROCIRCUIT,DI:16:1 MUX,SCRN		
A2U527	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U531	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U533	156-1800-00			MICROCIRCUIT,DI:QUAD 2 INPUT EXCLUSIVE OR	07263	74F86(PCQR OR DC
A2U535	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A2U537	160-2395-00			MICROCIRCUIT,DI:ARRAY LOGIC		
A2U541	156-1702-00			MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U547	156-1724-00			MICROCIRCUIT,DI:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A2U585	156-1909-00			MICROCIRCUIT,DI:QUAD 2 INP MULTIPLEXER		
A2U587	156-2001-00			MICROCIRCUIT,DI:TTL,QUAD 2-INPUT MULTIPLEXE	07263	74F257PCQR OR DC
A2U591	156-1736-00			MICROCIRCUIT,DI:HIGH PERFORMANCE BUS INTFC		
A2U601	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U605	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U607	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U611	156-1859-00			MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U615	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A2U637	156-1839-00			MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U641	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A2U647	156-1744-00			MICROCIRCUIT,DI:ASTTL,OCTAL BUFFER/LINE	07263	74F240
A2U651	160-2389-00			MICROCIRCUIT,DI:ARRAY LOGIC		

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A2U655	156-1702-00		MICROCIRCUIT,DI:STTL,10 BIT REGISTER,W/3-ST	34335	AM29821DCB
A2U657	156-1963-00		MICROCIRCUIT,DI:NONINVERTING R		
A2U661	156-1963-00		MICROCIRCUIT,DI:NONINVERTING R		
A2U665	156-1944-00		MICROCIRCUIT,DI:SINGLE ROW BUFFER		
A2U675	156-2012-00		MICROCIRCUIT,DI:NMOS,2048 X 8 SRAM		
A2U681	156-2012-00		MICROCIRCUIT,DI:NMOS,2048 X 8 SRAM		
A2U685	156-1909-00		MICROCIRCUIT,DI:QUAD 2 INP MULTIPLEXER		
A2U687	156-2001-00		MICROCIRCUIT,DI:TTL,QUAD 2-INPUT MULTIPLEXE	07263	74F257PCQR OR DC
A2U701	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U705	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U707	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U711	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U715	156-1936-00		MICROCIRCUIT,DI:QUAD 2-INP 4-BIT RGTR		
A2U717	156-0530-02		MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A2U721	160-2390-00		MICROCIRCUIT,DI:ARRAY LOGIC		
A2U727	160-2396-00		MICROCIRCUIT,DI:ARRAY LOGIC		
A2U731	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U735	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U741	156-1704-00		MICROCIRCUIT,DI:OCTAL D-TYPE FF,W/3-ST OUT	07263	74F374(PCQR OR D
A2U747	156-1961-00		MICROCIRCUIT,DI:BIDIRECTIONAL UNIVERAL		
A2U785	156-1909-00		MICROCIRCUIT,DI:QUAD 2 INP MULTIPLEXER		
A2U787	156-1763-00		MICROCIRCUIT,DI:CRT VIDEO PROCESSOR & CNTRL	53848	CRT9007PBI
A2U801	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U805	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U807	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U811	156-1859-00		MICROCIRCUIT,DI:MOS,DYNAMIC RAM,SCRN		
A2U815	156-1936-00		MICROCIRCUIT,DI:QUAD 2-INP 4-BIT RGTR		
A2U821	156-1933-00		MICROCIRCUIT,DI:16 BIT SHIFT REGISTER		
A2U825	156-1761-00		MICROCIRCUIT,DI:16:1 MUX,SCRN		
A2U827	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U831	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A2U835	156-1724-00		MICROCIRCUIT,DI:QUAD 2 INPUT OR GATE,SCRN	04713	74F32(ND OR JD)
A2U837	156-1839-00		MICROCIRCUIT,DI:OCTAL BIDIRECTIONAL		
A2U841	156-1722-00		MICROCIRCUIT,DI:HEX INVERTER,SCRN	04713	MC74F04
A2U847	156-1961-00		MICROCIRCUIT,DI:BIDIRECTIONAL UNIVERAL		
A2U851	156-1744-00		MICROCIRCUIT,DI:ASTTL,OCTAL BUFFER/LINE	07263	74F240
A2U855	160-2381-00		MICROCIRCUIT,DI:4096 X 8 EPROM		
A2U857	160-2391-00		MICROCIRCUIT,DI:ARRAY LOGIC		
A2U861	156-1963-00		MICROCIRCUIT,DI:NONINVERTING R		
A2U865	156-1944-00		MICROCIRCUIT,DI:SINGLE ROW BUFFER		
A2U875	156-2012-00		MICROCIRCUIT,DI:NMOS,2048 X 8 SRAM		
A2U881	156-2012-00		MICROCIRCUIT,DI:NMOS,2048 X 8 SRAM		
A2U885	156-0323-02		MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A2Y157	119-1721-00		MICROCIRCUIT,DI:HEX INVERTER,BURN IN	01295	SN74S04

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A3 RAM 3 BOARD					
A3	670-7196-00		CKT BOARD ASSY:RAM THREE	80009	670-7196-00
A3C225	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C315	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C341	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C511	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C515	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C521	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C525	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C531	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C535	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C541	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C545	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C711	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C715	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C721	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C725	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C731	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C735	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C741	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3C745	283-0423-00		CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A3J49	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	81312	96S-6043-0731-0
A3P48	131-2866-00		CONN.,RCPT,ELEC:MALE 3 X 32,RTANG,0.1	T0032	00-8257-096-00
A3R221	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A3R222	315-0330-00		RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A3R223	315-0222-00		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A3R224	315-0330-00		RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A3U221	160-2397-00		MICROCIRCUIT,DI:ARRAY LOGIC		
A3U311	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A3U321	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A3U325	156-1697-00		MICROCIRCUIT,DI:STTL,64K DRAM CONTROLLER	34649	D8203-3
A3U335	156-0956-02		MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A3U345	156-1065-01		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A3U411	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U415	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U421	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U425	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U431	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U435	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U441	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U445	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U511	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U515	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U521	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U525	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U531	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U535	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U541	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U545	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A3U611	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U615	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U621	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U625	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U631	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U635	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U641	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U645	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U711	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U715	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U721	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U725	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U731	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U735	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U741	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3U745	156-1876-00		MICROCIRCUIT,DI:NMOS,65536 X 1 BIT DYNAMIC		
A3Y231	119-1329-00		OSCILLATOR,RF:CRYSTAL CONTROLLED,24MHZ	75378	MX0-50-1

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A4 KEYBOARD					
A4	119-1592-01		KEYBOARD ASSY:4107		
A4	----		(STANDARD)		
A4	119-1619-01		KEYBOARD ASSY:UNITED KINGDOM		
A4	----		(OPTION 4A, UNITED KINGDOM)		
A4	119-1618-01		KEYBOARD ASSY:FRENCH		
A4	----		(OPTION 4B, FRENCH)		
A4	119-1621-01		KEYBOARD ASSY:SWEDISH		
A4	----		(OPTION 4C, SWEDISH)		
A4	119-1620-01		KEYBOARD ASSY:DANISH/NORWEGIAN		
A4	----		(OPTION 4F, DANISH/NORWEGIAN)		
A4	119-1622-01		KEYBOARD ASSY:GERMAN		
A4	----		(OPTION 4G, GERMAN)		
A4	119-1678-01		KEYBOARD ASSY:KATAKANA		
A4	----		(OPTION 4K, KATAKANA)		
A4A1	118-2975-01		KEYBOARD:W/O ENCLOSURE	80009	118-2975-00
A4A1	----		(STANDARD ONLY)		
A4A1	118-3276-01		KYBD ASSY:UNITED KINGDOM	80009	118-3276-00
A4A1	----		(OPTION 4A ONLY)		
A4A1	118-3277-01		KYBD ASSY:DANISH/NORWEGIAN	80009	118-3277-00
A4A1	----		(OPTION 4F ONLY)		
A4A1	118-3278-01		KYBD ASSY:SWEDISH	80009	118-3278-00
A4A1	----		(OPTION 4C ONLY)		
A4A1	118-3280-01		KYBD ASSY:FRENCH	80009	118-3280-00
A4A1	----		(OPTION 4B ONLY)		
A4A1	118-1678-01		KYBD ASSY:KATAKANA	80009	119-1678-00
A4A1	----		(OPTION 4K ONLY)		
A4A1C1	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C2	118-3189-00		CAP.,FXD,ELEC:10UF,10V		
A4A1C3	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C4	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C5	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C6	290-0284-00		CAP.,FXD,ELCTL:4.7UF,10%,35V	56289	150D475X9035B2
A4A1C8	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C9	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1C10	290-0535-00		CAP.,FXD,ELCTL:33UF,20%,10V	56289	196D336X0010KA1
A4A1C11	281-0819-00		CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A4A1CR2	118-3003-00		SEMICON DVC,DI:IN4148	52833	21-04148-000
A4A1CR3	118-3003-00		SEMICON DVC,DI:IN4148	52833	21-04148-000
A4A1CR4	118-3003-00		SEMICON DVC,DI:IN4148	52833	21-04148-000
A4A1CR9	150-1036-00		LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A4A1CR?	150-1036-00		LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A4A1CR?	----		(FOR S78 OPTION 4K ONLY)		
A4A1J1	118-3001-00		CONN,RCPT,ELEC:RTANG,6 PIN	52833	39-00757-000
A4A1JS1	118-3033-00		SWITCH:	52833	61-04032-001
A4A1R1	315-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4A1R6	315-0121-00		RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A4A1R7	315-0332-00		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A4A1R8	315-0821-00		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A4A1R9	315-0181-00		RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A4A1R10	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A4A1R11	315-0271-00		RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A4A1S1 THRU	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S44	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S45	118-3018-00		SWITCH:	52833	61-04031-002
A4A1S45	-----		(LEFT SWITCH)		
A4A1S45	118-3029-00		SWITCH:	52833	61-04031-001
A4A1S45	-----		(RIGHT SWITCH)		
A4A1S46	260-2177-00		SW,CAPACITIVE:30MM,LOW PROFILE W/LED		
A4A1S47 THRU	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S72	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S73	118-3018-00		SWITCH:	52833	61-04031-002
A4A1S73	-----		(LEFT SWITCH)		
A4A1S73	118-3029-00		SWITCH:	52833	61-04031-001
A4A1S73	-----		(RIGHT SWITCH)		
A4A1S74 THRU	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S77	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S77	-----		(OPTION 4K ONLY)		
A4A1S78	260-2177-00		SW,CAPACITIVE:30MM,LOW PROFILE W/LED		
A4A1S78	-----		(OPTION 4K ONLY)		
A4A1S79 THRU	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S86	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S86	-----		(OPTION 4K ONLY)		
A4A1S74	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
THRU					
A4A1S86	260-2176-00		SW,CAPACITIVE:30MM,LOW PROFILE		
A4A1S86	-----		(OPTION 4A,B,C,F,G,ONLY)		
A4A1U1	118-0941-00		MICROCIRCUIT,LI:KYBD DETECTOR,CAPACITIVE	52833	22-00908-003
A4A1U2	156-0973-00		MICROCIRCUIT,DI:1024 X 8 PROM	80009	156-0973-00
A4A1U3	156-3024-00		MICROCIRCUIT,DI:1024 X 8 PROM	52833	20-08748-308
A4A1U4	156-0153-02		MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM8006
A4A1U5	156-1080-01		MICROCIRCUIT,DI:HEX BUFFERS U/OC HV	27014	DM7407
A4A1VR6	156-0277-01		MICROCIRCUIT,LI:POSITIVE VOLTAGE REG	04713	MC7805CTD
A4A1Y1	118-3011-00		XTAL UNIT,QTZ:4.608 MHZ	52833	48-00300-107
A4A1Z1	118-3012-00		MICROCKT,HYBRID:	52833	22-00920-000

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A5 POWER SUPPLY ASSY					
A5	620-0005-00		POWER SUPPLY:	80009	620-0005-00
A5B1001	119-1635-00		FAN,TUBE AXIAL:12VDC,1.44W,80MM BRUSHLESS		
A5C5	285-1259-00		CAP.,FXD,ELCTLT:0.015UF,10%,250V		
A5C11	285-1259-00		CAP.,FXD,ELCTLT:0.015UF,10%,250V		
A5C51	290-0778-00		CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A5C105	285-1259-00		CAP.,FXD,ELCTLT:0.015UF,10%,250V		
A5C111	285-1259-00		CAP.,FXD,ELCTLT:0.015UF,10%,250V		
A5C118	283-0008-00		CAP.,FXD,CER DI:0.1UF,20%,500V	56289	3C37X7R104M500B
A5C133	290-0844-00		CAP.,FXD,ELCTLT:100UF,-10+75%,35 WVDC	54473	ECE-A35V100L
A5C151	281-0773-00		CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A5C161	290-0942-00		CAP.,FXD,ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A5C163	290-0768-00		CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A5C164	290-0800-00		CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A5C216	283-0008-00		CAP.,FXD,CER DI:0.1UF,20%,500V	56289	3C37X7R104M500B
A5C221	290-0683-00		CAP.,FXD,ELCTLT:100UF,+20%,200V		
A5C230	285-0932-00		CAP.,FXD,PLSTC:1UF,10%,400V	14752	230B1E105K
A5C235	290-0942-00		CAP.,FXD,ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A5C261	290-0686-00		CAP.,FXD,ELCTLT:8400UF,+100%-10%,12V		
A5C267	290-0800-00		CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A5C311	283-0057-00		CAP.,FXD,CER DI:0.1UF,+80-20%,200V	56289	2C20Z5U104Z200B
A5C314	281-0774-00		CAP.,FXD,CER DI:0.022UF,20%,100V	12969	CGE223MEZ
A5C318	290-0683-00		CAP.,FXD,ELCTLT:100UF,+20%,200V		
A5C320	290-0778-00		CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A5C323	281-0826-00		CAP.,FXD,CER DI:2200PF,5%,100V	12969	CGB222KEX
A5C336	290-0768-00		CAP.,FXD,ELCTLT:10UF,+50-10%,100V	54473	ECE-A100V10L
A5C338	283-0425-00		CAP.,FXD,CER DI:650PF,10%,1000V	60705	ORD BY DESCR
A5C351	290-0778-00		CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A5C361	290-0778-00		CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A5CR117	152-0848-00		SEMICOND DEVICE:RECT BRIDGE,600V,2A,FAST		
A5CR137	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR138	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR156	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR157	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR158	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR232	152-0523-00		SEMICOND DEVICE:RECTIFIER,SI,100V	12969	VES1102
A5CR233	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR234	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR235	152-0400-00		SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A5CR237	152-0400-00		SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A5CR239	152-0400-00		SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A5CR334	152-0398-00		SEMICOND DEVICE:SILICON,200V,1A	04713	SR3609RL
A5CR337	152-0400-00		SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A5CR362	152-0827-00		SEMICOND DEVICE:RECT,SI,45V,3A	04713	MBR2545CT
A5CR363	152-0141-02		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5DS301	150-0035-00		LAMP,GLOW:90V,0.3MA,AID-T,WIRE LD	000LI	JH005/3011JA
A5F101	159-0149-00		FUSE,CARTRIDGE:4A,250V,SLOW-BLOW	71400	MDA 4 AMP
A5FL201	119-1168-00		CAPACITOR-RES:0.1UF,20% & 22 OHM,10%,250V	14752	RG1782-1

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A5J1	131-3000-00		CONN,RCPT,ELEC:PWR,3 MALE,250VAC,6A	82389	EX41004
A5J2	131-1737-00		CONN,RCPT,ELEC:9 CONTACT,W/LOCKING EARS		
A5J3	131-0608-00		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5J3	-----		(QUANTITY OF 2)		
A5J4	131-2909-00		CONN,RCPT,ELEC:MOLEX,1 X 10,0.156 SP	27264	09-71-1101
A5J5	131-0608-00		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5J5	-----		(QUANTITY OF 2)		
A5J6	131-0608-00		TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5J6	-----		(QUANTITY OF 2)		
A5L114	108-1209-00		COIL,RF:FXD TOROIDAL,122UH MIN 3ADC		
A5L161	108-0554-00		COIL,RF:5UH	80009	108-0554-00
A5L214	108-1209-00		COIL,RF:FXD TOROIDAL,122UH MIN 3ADC		
A5Q129	151-0503-00		SCR:SILICON,TO-92	04713	SCR5138
A5Q133	151-0190-00		TRANSISTOR:SILICON,NPN	07263	S032677
A5Q257	151-0190-00		TRANSISTOR:SILICON,NPN	07263	S032677
A5Q266	151-0190-00		TRANSISTOR:SILICON,NPN	07263	S032677
A5Q267	151-0190-00		TRANSISTOR:SILICON,NPN	07263	S032677
A5Q314	151-0188-00		TRANSISTOR:SILICON,PNP	04713	SPS6868K
A5Q331	151-0378-00		TRANSISTOR:NPN,SI,TO-220	T0016	2SC3178
A5Q332	151-0710-00		TRANSISTOR:SILICON,NPN	27014	2N6715/92 PU01A
A5Q352	151-0190-00		TRANSISTOR:SILICON,NPN	07263	S032677
A5Q357	151-0503-00		SCR:SILICON,TO-92	04713	SCR5138
A5R51	323-0214-00		RES.,FXD,FILM:1.65K OHM,1%,0.50W	75042	CECT0-1651F
A5R52	321-0099-00		RES.,FXD,FILM:105 OHM,1%,0.125W	91637	MTF1816G105R0F
A5R123	301-0154-00		RES.,FXD,CMPSN:150K OHM,5%,0.50W	01121	EB1545
A5R132	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R133	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A5R161	308-0755-00		RES.,FXD,WW:0.75 OHM,5%,2W	75042	BWH-R7500J
A5R216	301-0154-00		RES.,FXD,CMPSN:150K OHM,5%,0.50W	01121	EB1545
A5R220	308-0778-00		RES.,FXD,WW:3 OHM,5%,5W	91637	CW-5-3R000J
A5R224	308-0568-00		RES.,FXD,WW:35 OHM,5%,5W	91637	CW5-35R00J
A5R225	308-0778-00		RES.,FXD,WW:3 OHM,5%,5W	91637	CW-5-3R000J
A5R229	305-0104-00		RES.,FXD,CMPSN:100K OHM,5%,2W	01121	HB1045
A5R231	308-0568-00		RES.,FXD,WW:35 OHM,5%,5W	91637	CW5-35R00J
A5R235	308-0363-00		RES.,FXD,WW:3K OHM,5%,8W	91637	RS8-B30000J
A5R257	308-0757-00		RES.,FXD,WW:0.025 OHM,3%,5W	91637	LVR5-GR0250H
A5R266	315-0431-00		RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A5R311	315-0915-00		RES.,FXD,CMPSN:9.1M OHM,5%,0.25W	01121	CB9155
A5R313	315-0183-00		RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A5R314	315-0243-00		RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A5R322	315-0203-00		RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A5R323	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R325	308-0590-00		RES.,FXD,WW:0.25 OHM,5%,3W	91637	RS2BER2500J
A5R326	301-0471-00		RES.,FXD,CMPSN:470 OHM,5%,0.50W	01121	EB4715
A5R331	301-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
A5R334	305-0431-00		RES.,FXD,CMPSN:430 OHM,5%,2W	01121	HB4315
A5R338	301-0822-00		RES.,FXD,CMPSN:8.2K OHM,5%,0.50W	01121	EB8225
A5R343	315-0131-00		RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A5R344	315-0103-00		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R345	301-0391-00		RES.,FXD,CMPSN:390 OHM,5%,0.50W	01121	EB3915
A5R346	315-0682-00		RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Name & Description	Mfr Code	Mfr Part Number
A5R347	321-0246-00		RES.,FXD,FILM:3.57K OHM,1%,0.125W	91637	MFF1816G35700F
A5R348	315-0102-00		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R354	315-0331-00		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A5R355	321-0248-00		RES.,FXD,FILM:3.74K OHM,1%,0.125W	91637	MFF1816G37400F
A5R356	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A5R362	315-0101-00		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A5R367	315-0431-00		RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A5RT16	307-0746-00		RES.,THERMAL:5 OHM,10%,7A/DEG C	15454	SG-6
A5S25	260-2116-00		SWITCH,SLIDE:DPDT,10A,125VAC	22753	SE1022-SD-CE-P-R
A5S35	260-2116-00		SWITCH,SLIDE:DPDT,10A,125VAC	22753	SE1022-SD-CE-P-R
A5S305	260-2047-01		SWITCH PUSH:DPST,4A,250 W/CKT PINS	31918	601805
A5T105	120-1449-00		XFMR,COM MODE:	02113	P104
A5T245	120-1496-00		XFMR,PWR,SPTDN:HF FLYBACK	80009	120-1496-00
A5U317	156-1799-00		MICROCIRCUIT,LI:SWITCHED MODE PWR SUPPLY	18324	NE5561N
A5U341	156-0430-00		CPLR,OPTOELECTR:LED & PHOTOTRANS,10KV	32694	OP11264B
A5VR122	152-0599-00		SEMICONV DEVICE:ZENER,SI,200V	04713	1N6303A
A5VR129	152-0571-00		SEMICONV DEVICE:ZENER,0.4W,16V,5%	04713	SZ35014K1
A5VR135	152-0168-00		SEMICONV DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4
A5VR151	156-1529-00		MICROCIRCUIT,LI:THREE TERMINAL ADJUSTABLE	04713	LM317LZ
A5VR216	152-0599-00		SEMICONV DEVICE:ZENER,SI,200V	04713	1N6303A
A5VR342	152-0149-00		SEMICONV DEVICE:ZENER,0.4W,10V,5%	04713	SZG35009K3
A5VR353	156-1631-00		MICROCIRCUIT,LI:ADJ SHUNT REGULATOR	01295	TL431C-LP
A5VR362	152-0175-00		SEMICONV DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008

Section 10

DIAGRAMS

INTRODUCTION

This section includes the block diagrams, address space diagrams, and interconnect diagrams for the 4107. Some of these diagrams are part of the theory section; they are repeated here for easy reference while reading other parts of the manual.

BLOCK DIAGRAMS

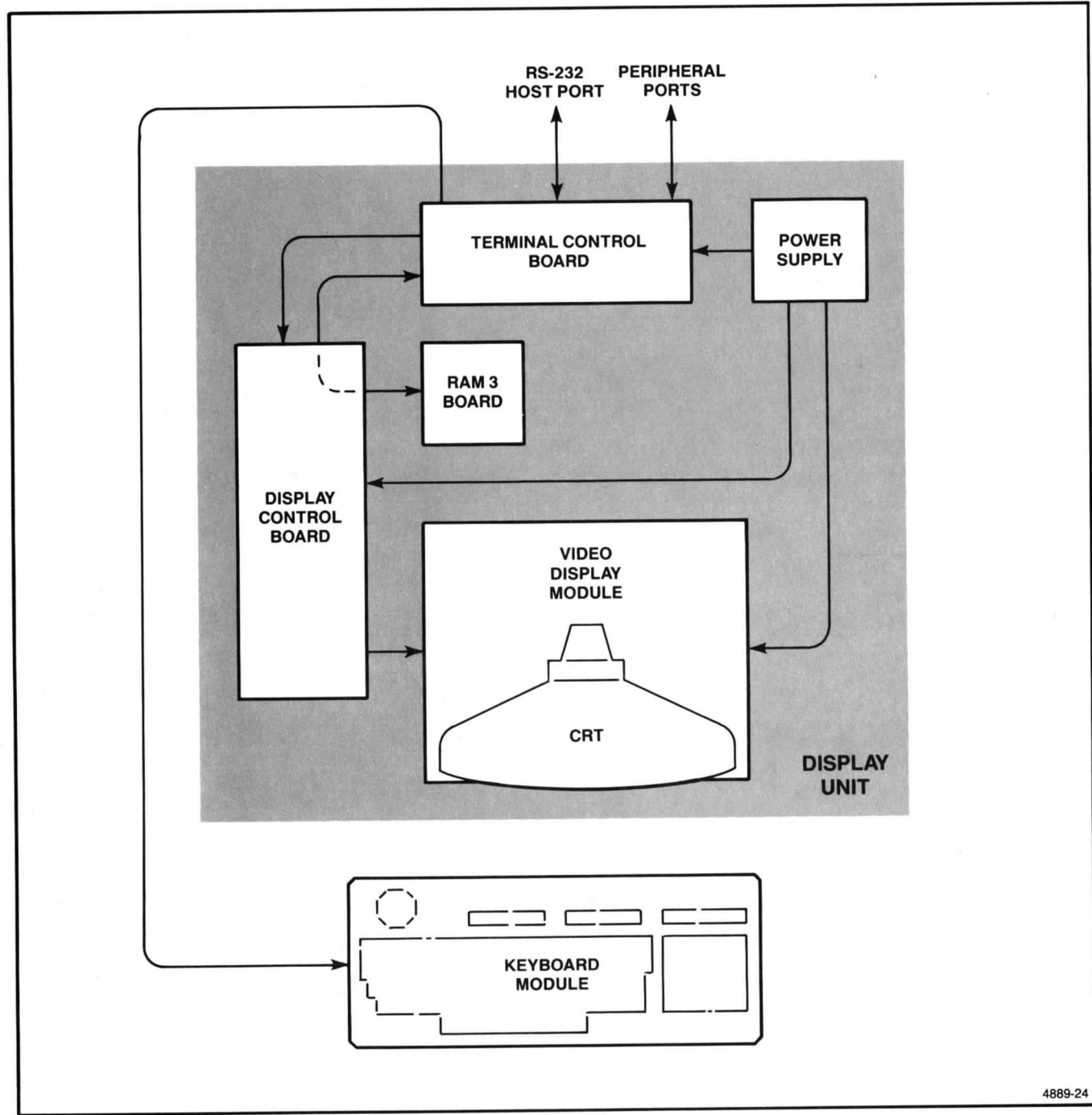
- System Block Diagram
- Terminal Control Block Diagram
- Keyboard Module Block Diagram
- Power Supply Block Diagram
- Display Module Block Diagram

ADDRESS SPACE DIAGRAMS

- Map of Memory Address Space
- Map of I/O Address Space
- Map of Host Comm I/O Space
- Map of 2-Port Peripheral Interface I/O Space
- Map of Video I/O Space
- Map of Printer Interface I/O Space

INTERCONNECT DIAGRAMS

- Main Interconnect Diagram
- Display Module Interconnect Diagram



4889-24

Figure 10-1. System Block Diagram.

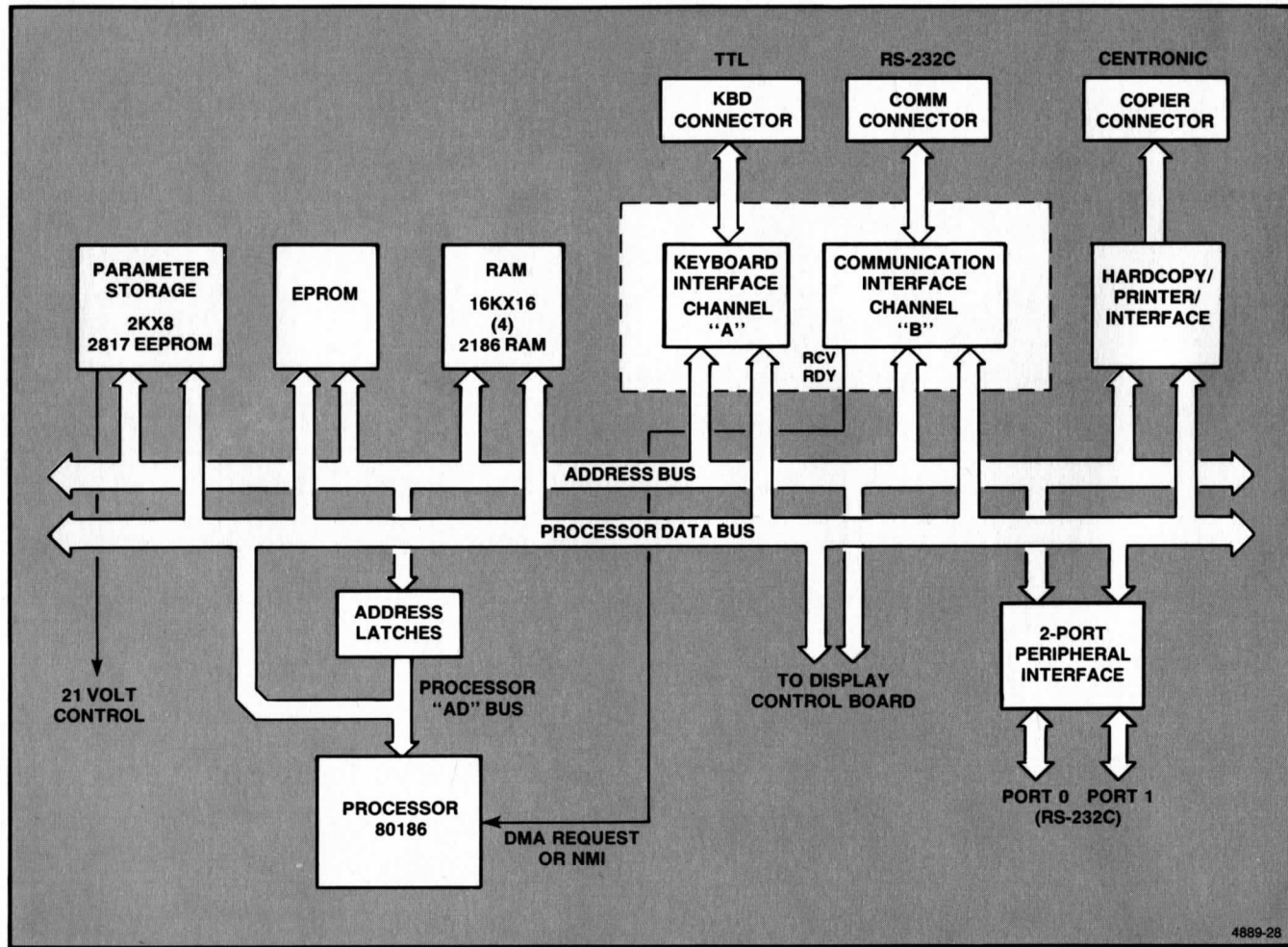


Figure 10-2. Terminal Control Block Diagram.

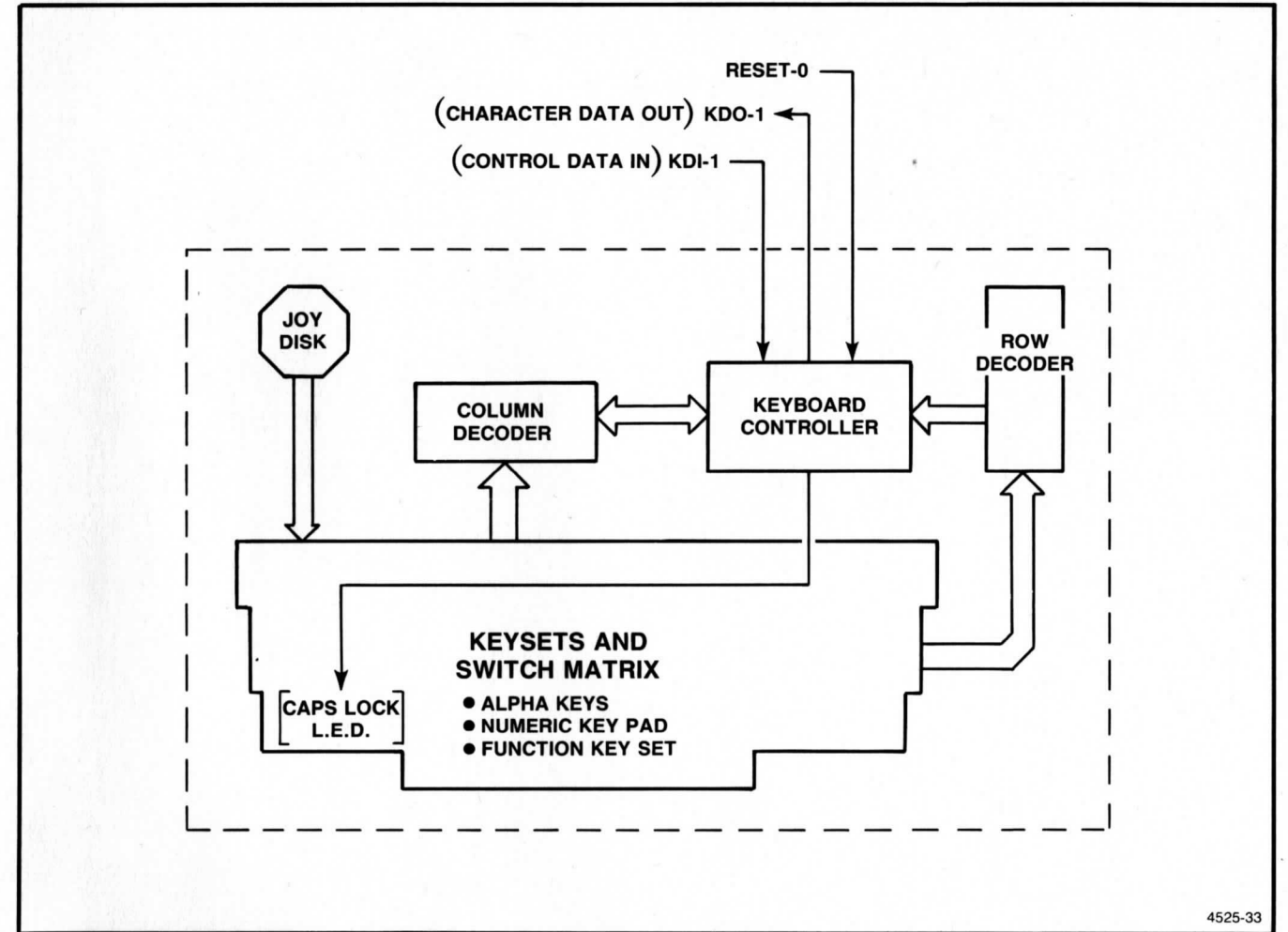


Figure 10-3. Keyboard Module Block Diagram.

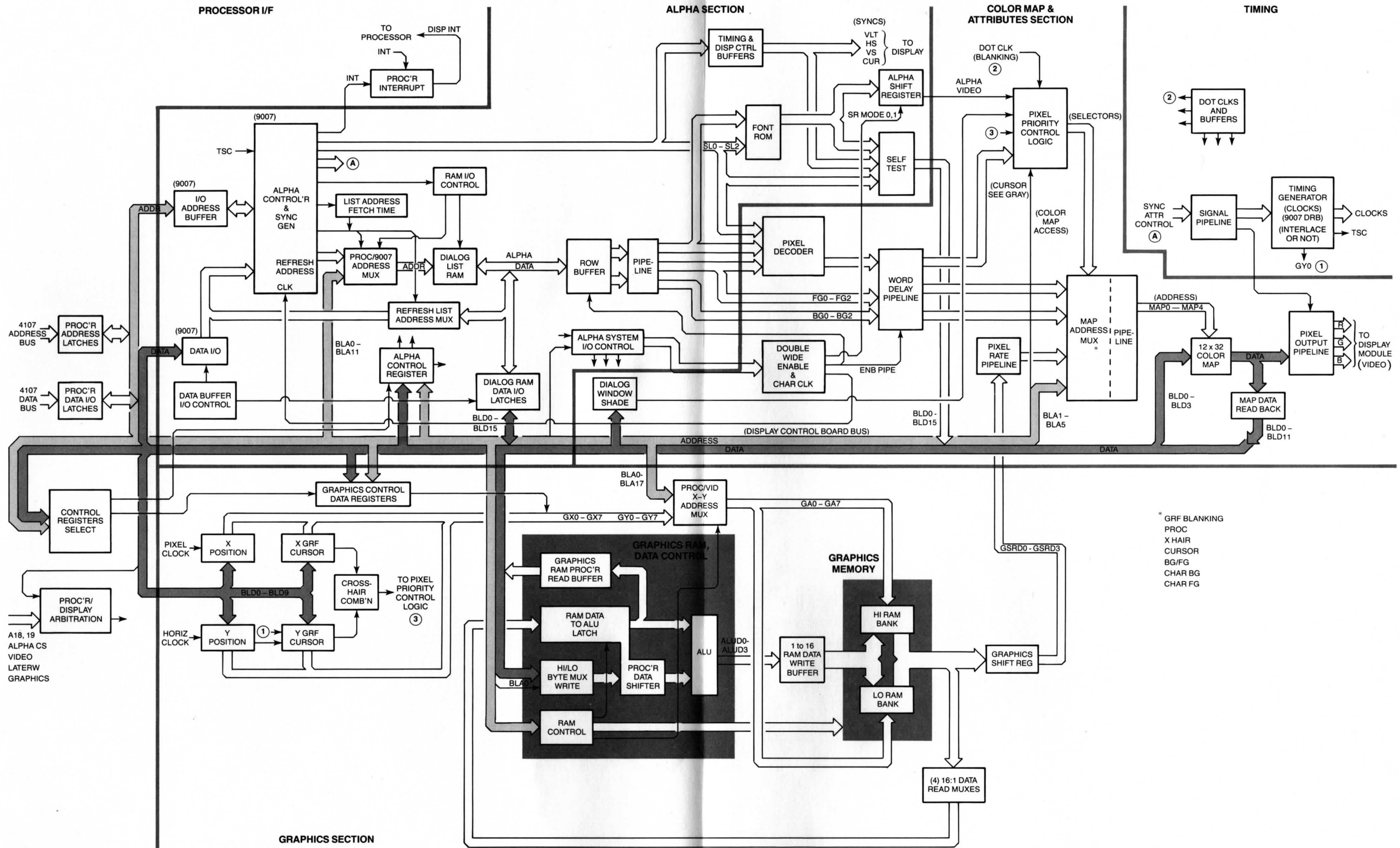


Figure 10-4. Display Control Block Diagram.

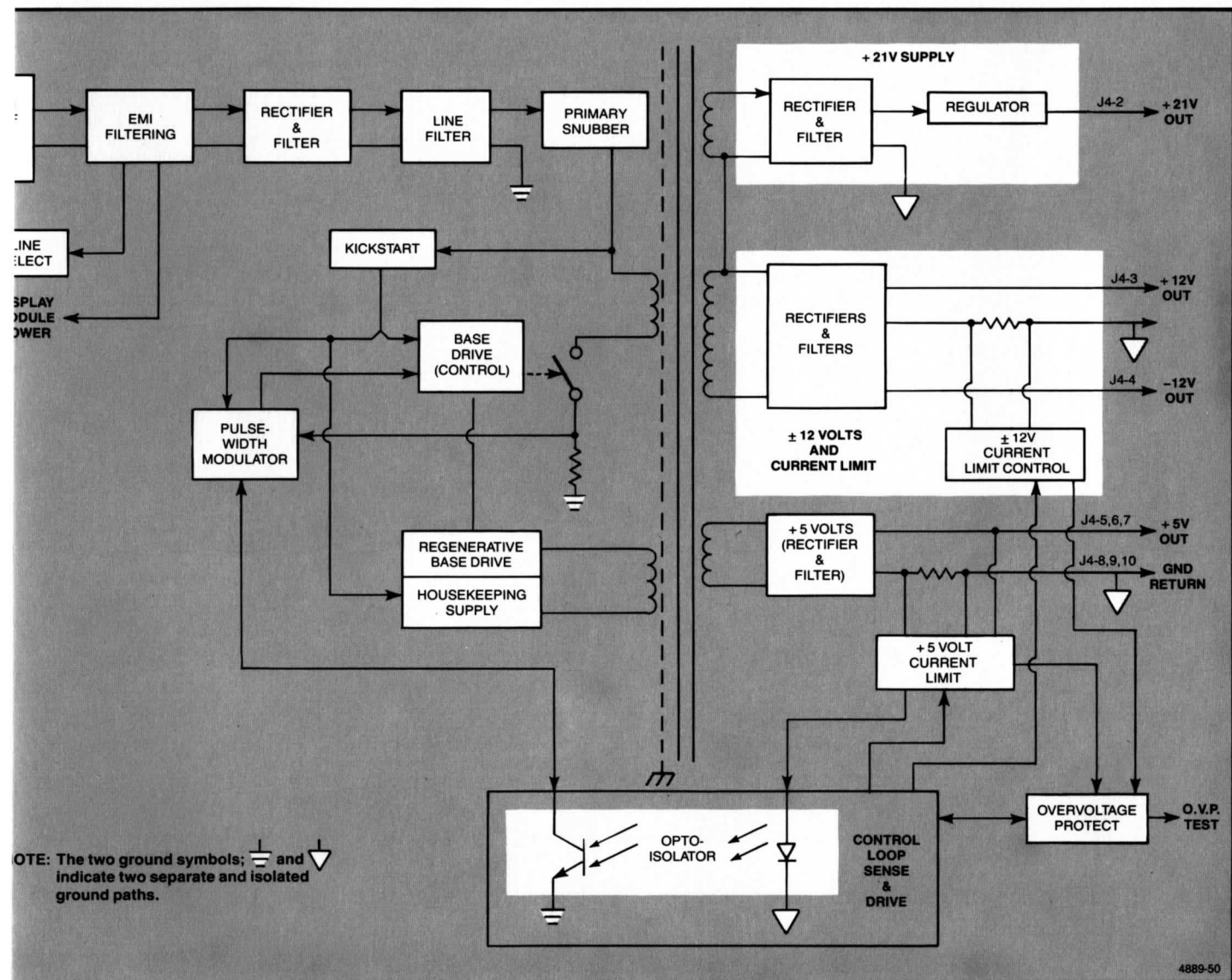


Figure 10-5. Power Supply Block Diagram.

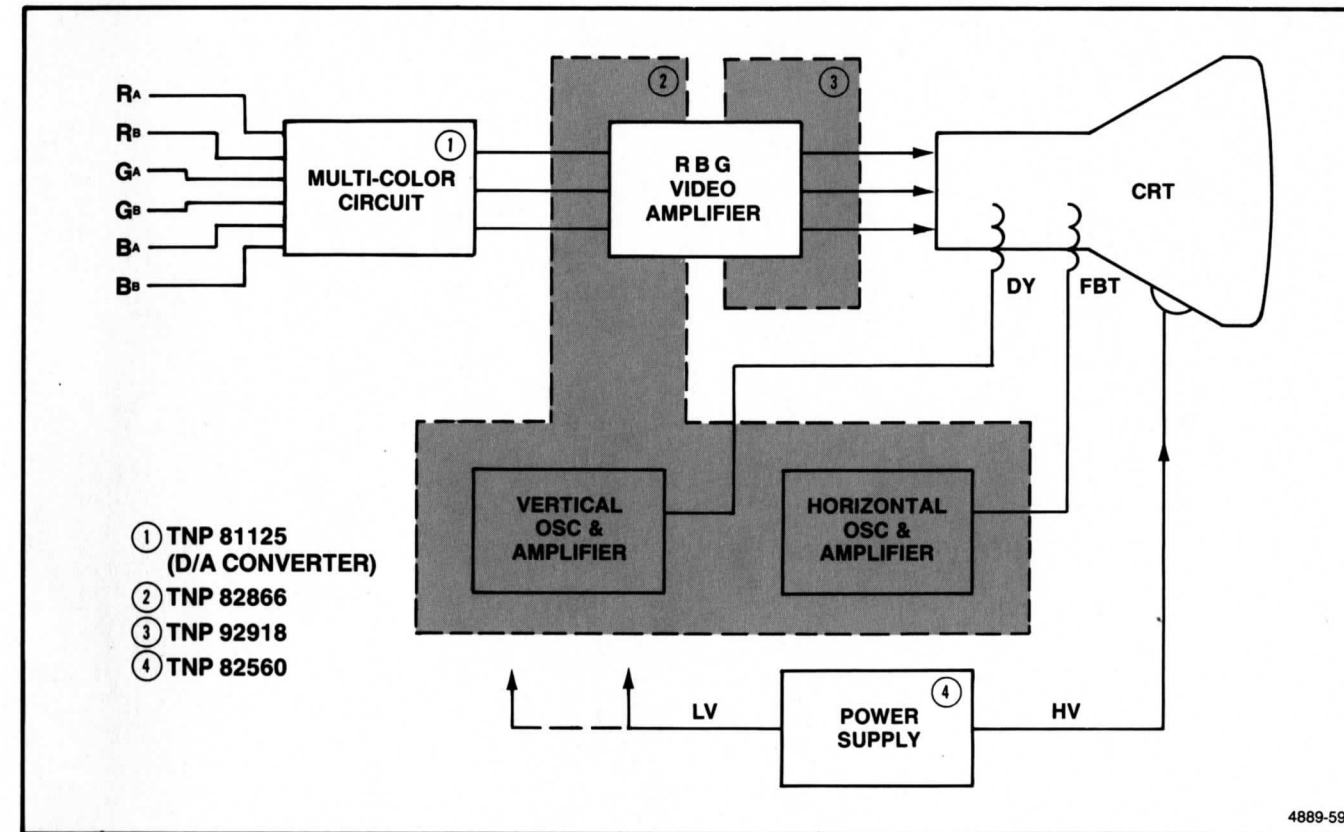


Figure 10-6. Display Module Block Diagram.

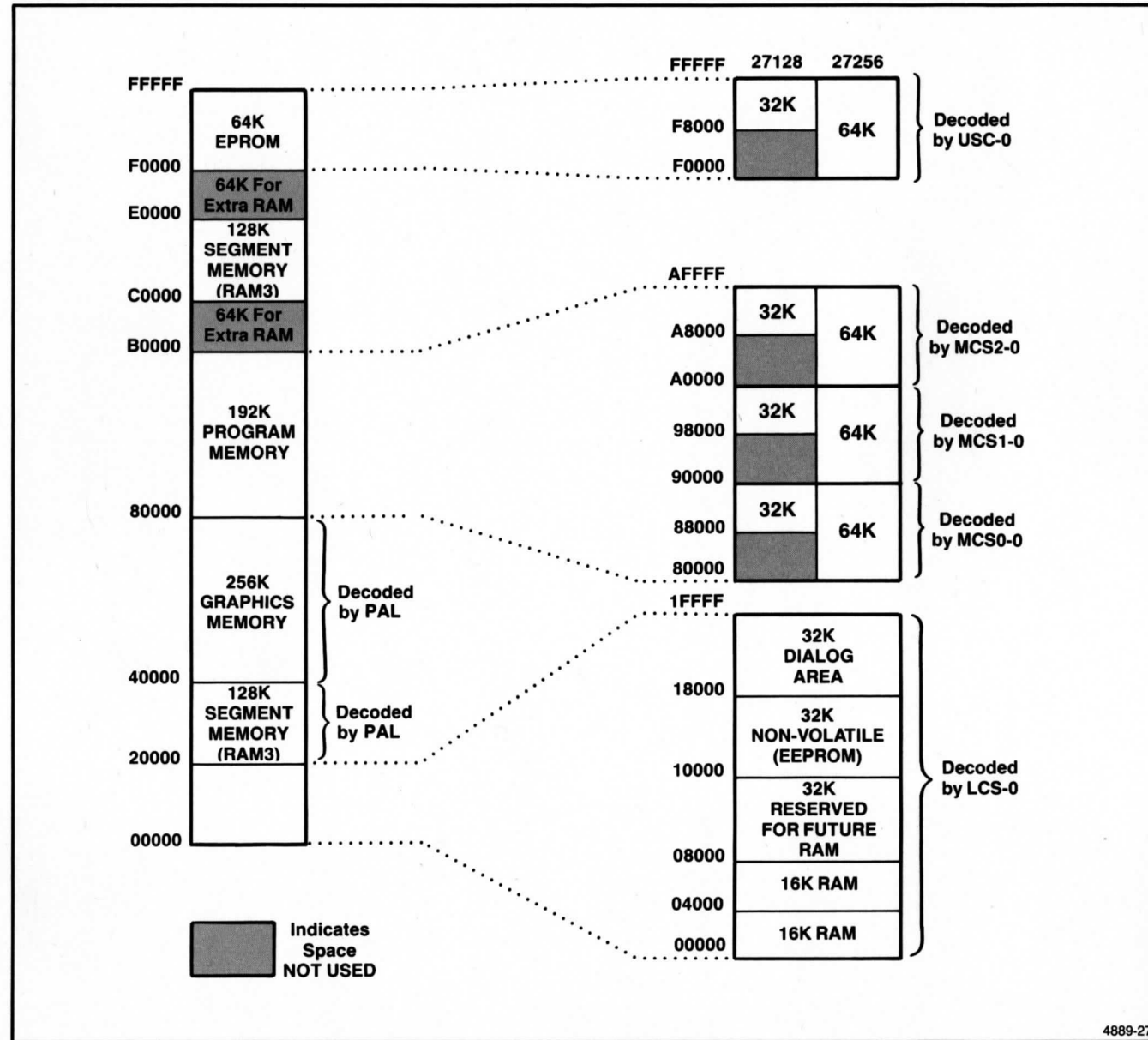


Figure 10-7. Map of Memory Address Space.

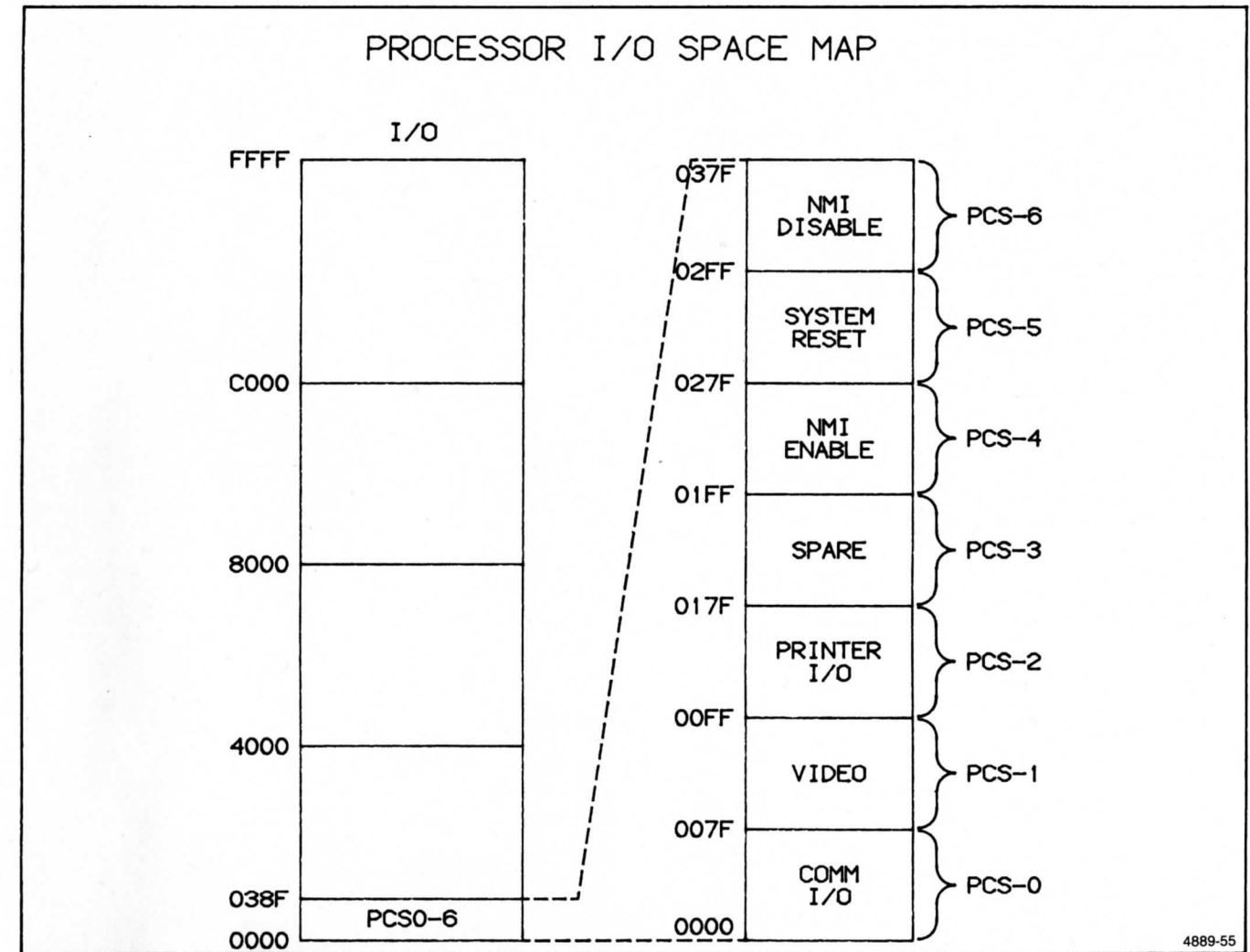
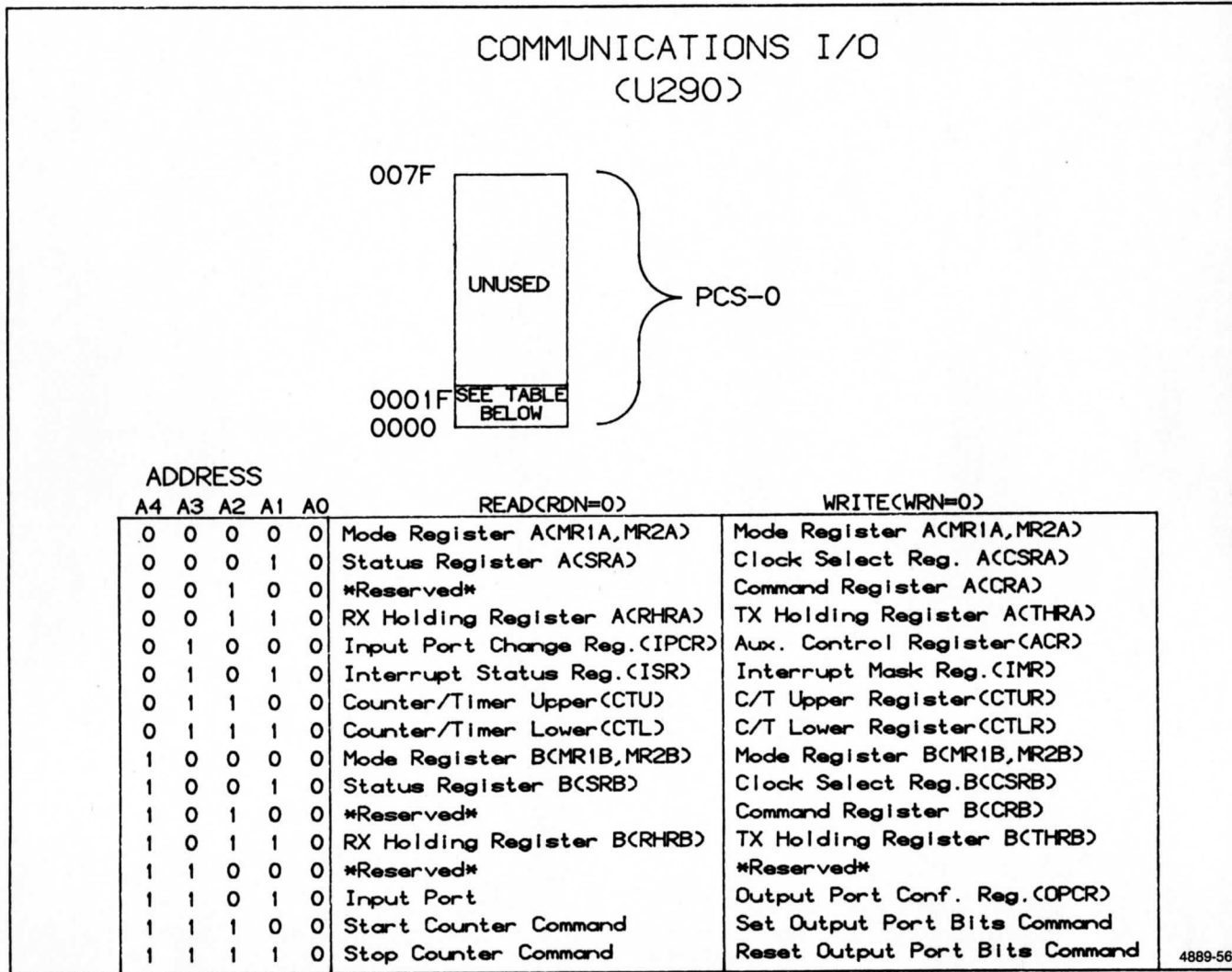
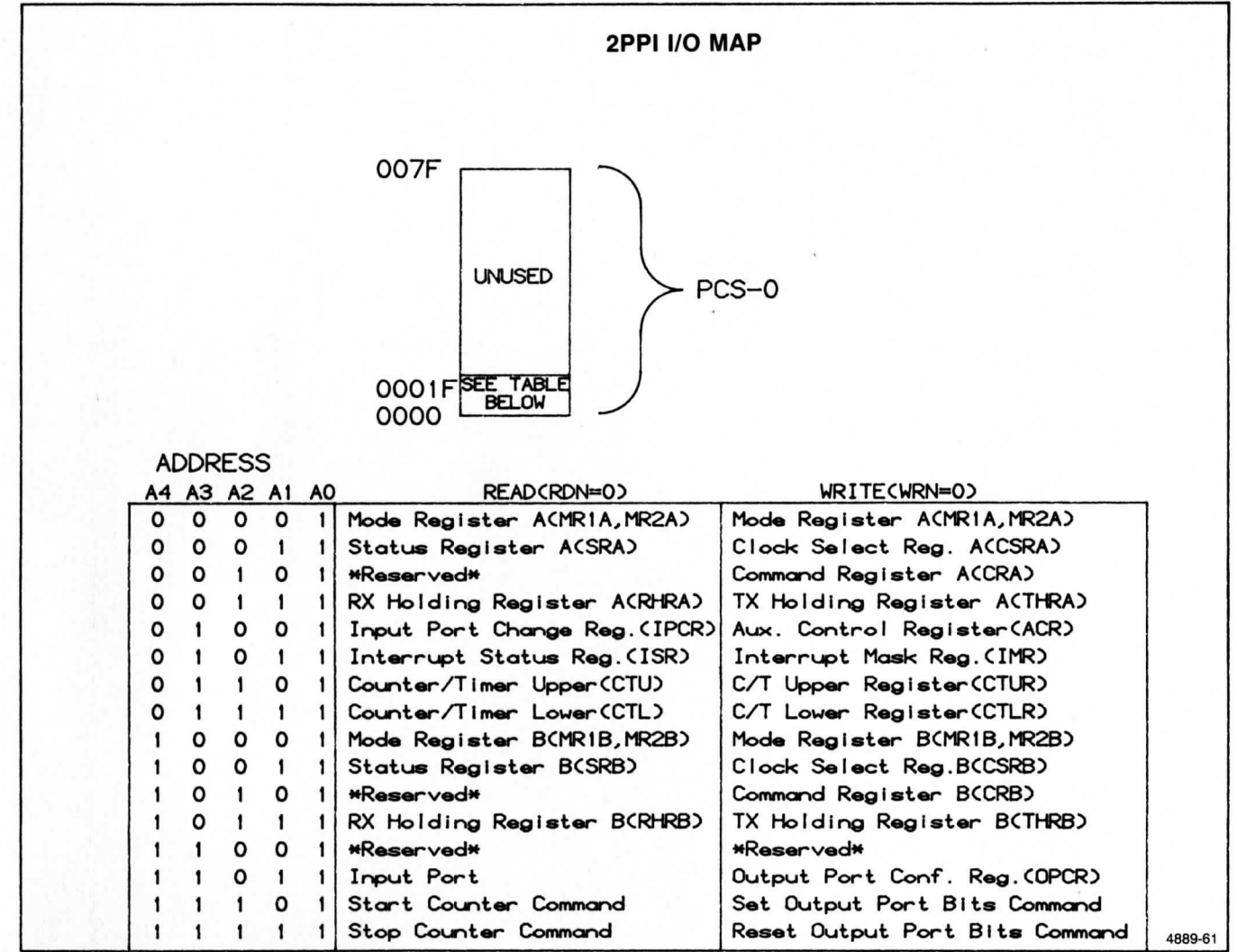


Figure 10-8. Map of Processor I/O Address Space.



NOTE: THIS DUART USES LOW DATA BYTE (See Chip U290)

Figure 10-9. Map of Communications Space.



(U437) NOTE: THIS DUART USES HI DATA BYTE
PORT A IS P20
PORT B IS P23

Figure 10-10. Map of 2PPI I/O Space.

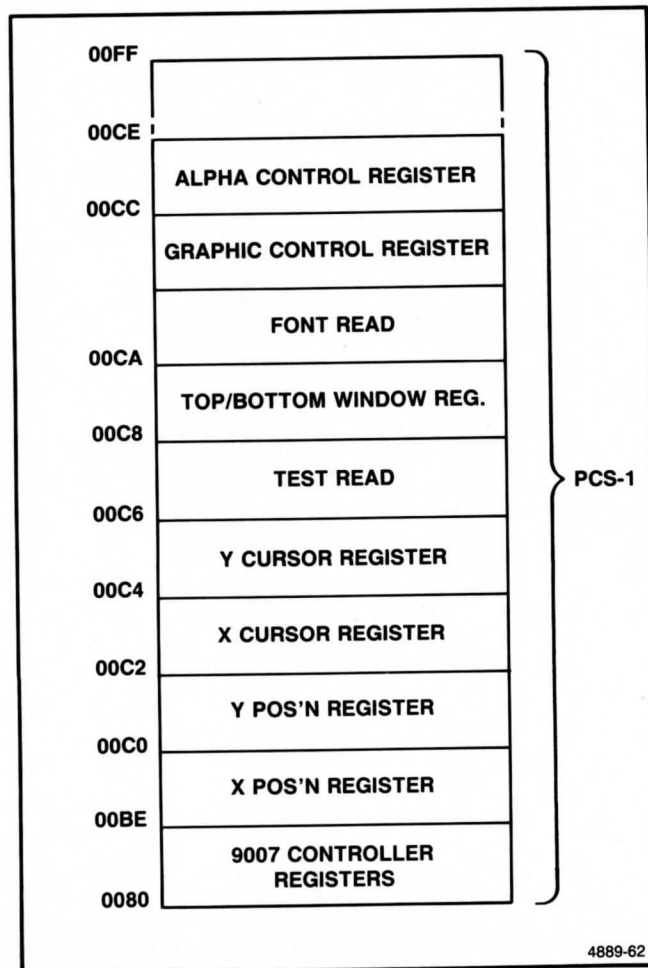


Figure 10-11. Map of Video I/O Space.

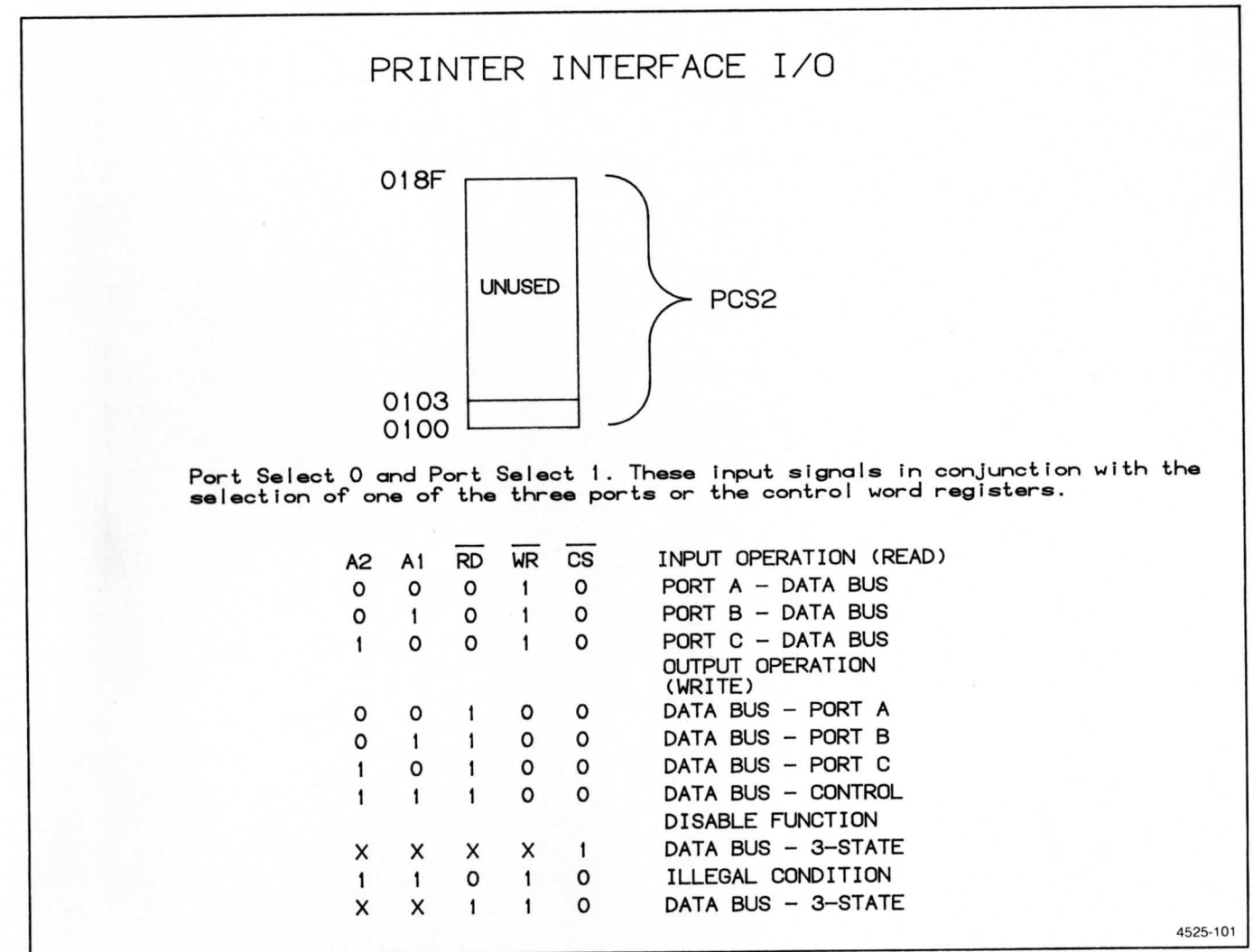
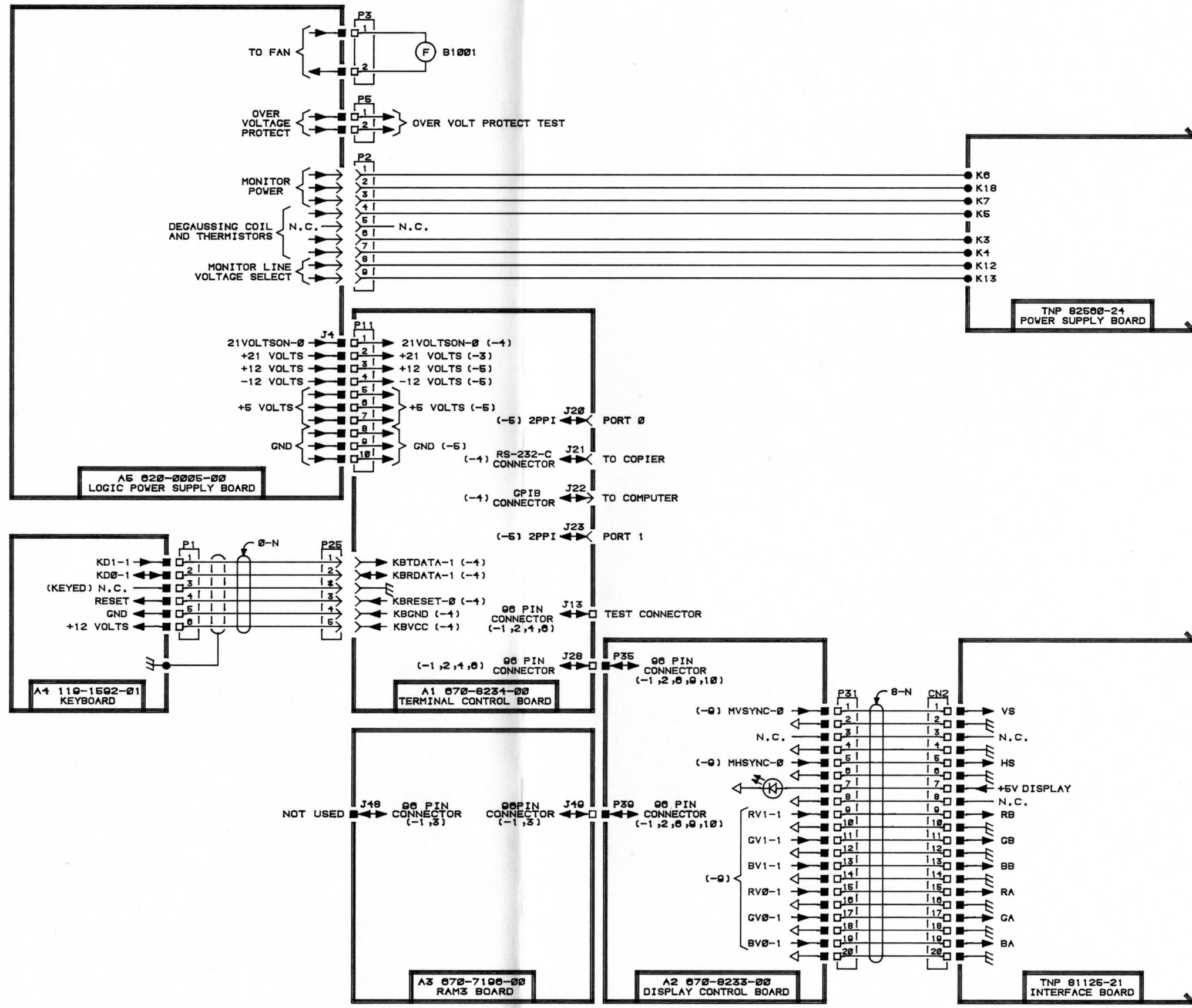
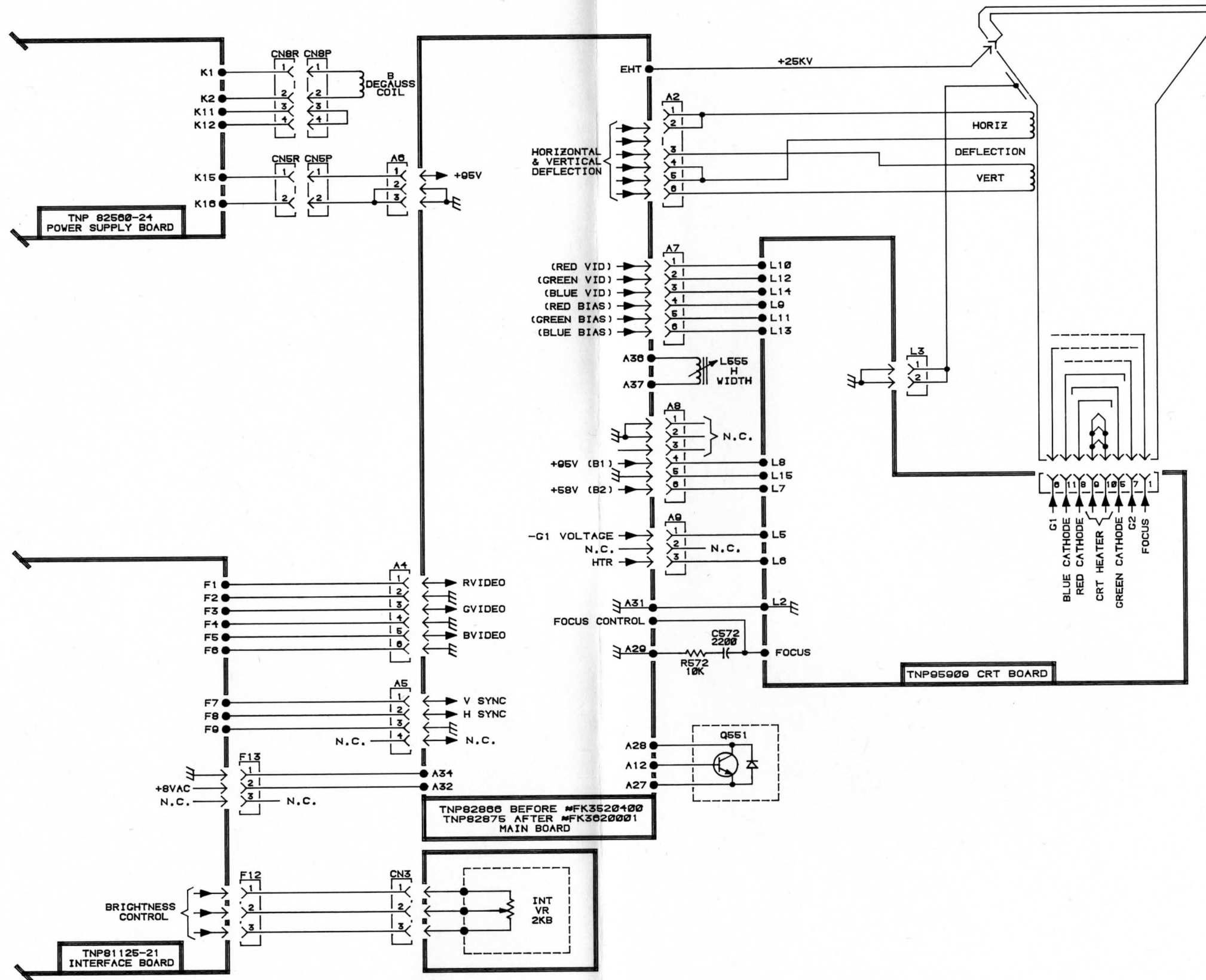


Figure 10-12. Map of Printer Interface I/O Space.

VIDEO I/O & PRINTER INTERFACE I/O MAPS
FIGURES 10-11, 10-12



INSTRUMENT: <p style="text-align: center;">4107</p>	NOTES: P25-PIN * IS THE CONNECTOR BODY KEYWAY. <p style="text-align: center;">4880-11</p>	DIAGRAM: <p style="text-align: center;">MAIN INTERCONNECT</p>	SHEET: <p style="text-align: center;">1 OF 1</p>
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INSTRUMENT: 4107	NOTES: 	DIAGRAM: DISPLAY MODULE INTERCONNECT	SHEET: 1 OF 1
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Section 11 SCHEMATICS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μ F).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

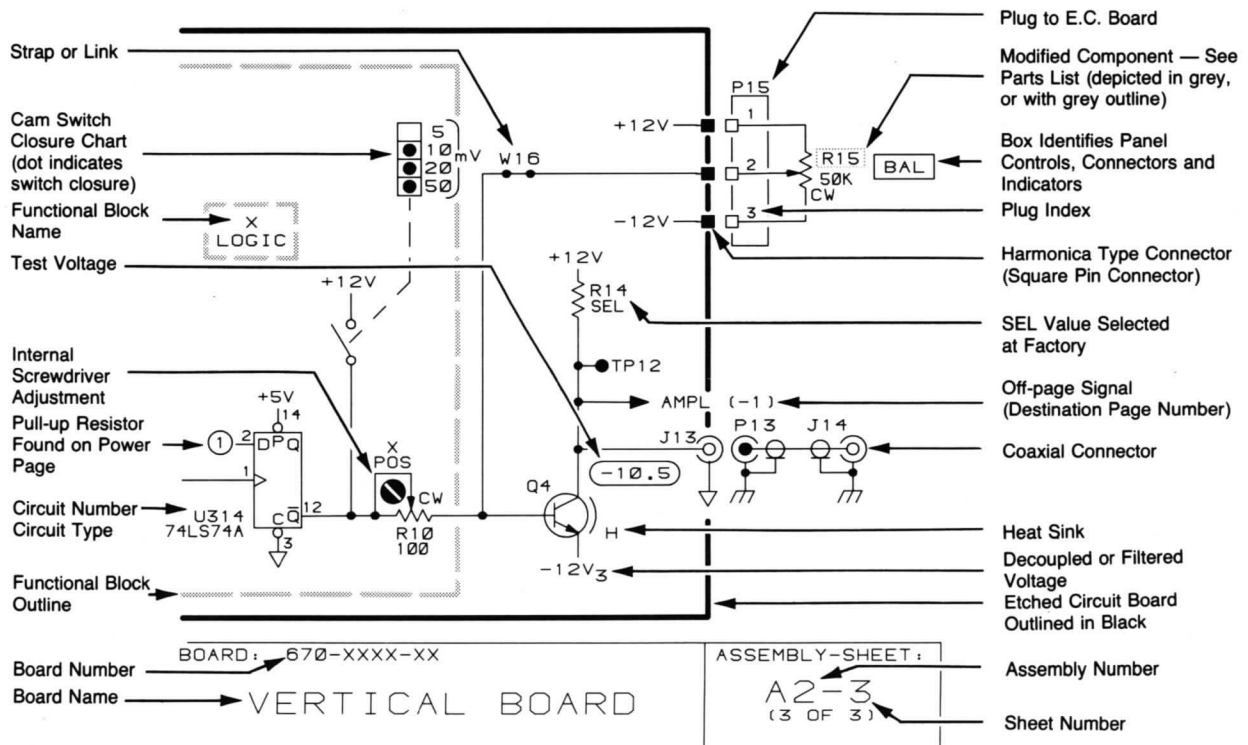
Abbreviations are based on ANSI Y1.1-1972. Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc., are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc.)	H	Heat dissipating device (heat sink, heat radiator, etc.)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



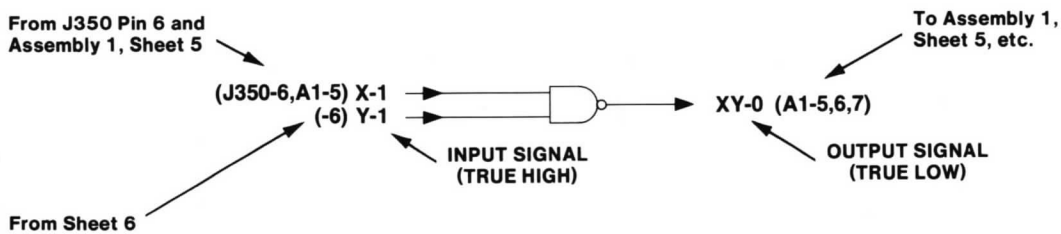
1. True High and True Low Signals

Signal names on the schematics are followed by -1 or a -0. A TRUE HIGH signal is indicated by -1, and a TRUE LOW signal is indicated by -0.

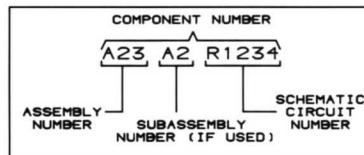
SIGNAL -1 = TRUE HIGH
SIGNAL -0 = TRUE LOW

2. Cross-References

Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.



3. Component Number Example



CHASSIS-MOUNTED COMPONENTS HAVE NO ASSEMBLY NUMBER PREFIX—SEE END OF REPLACEABLE ELECTRICAL PARTS LIST.

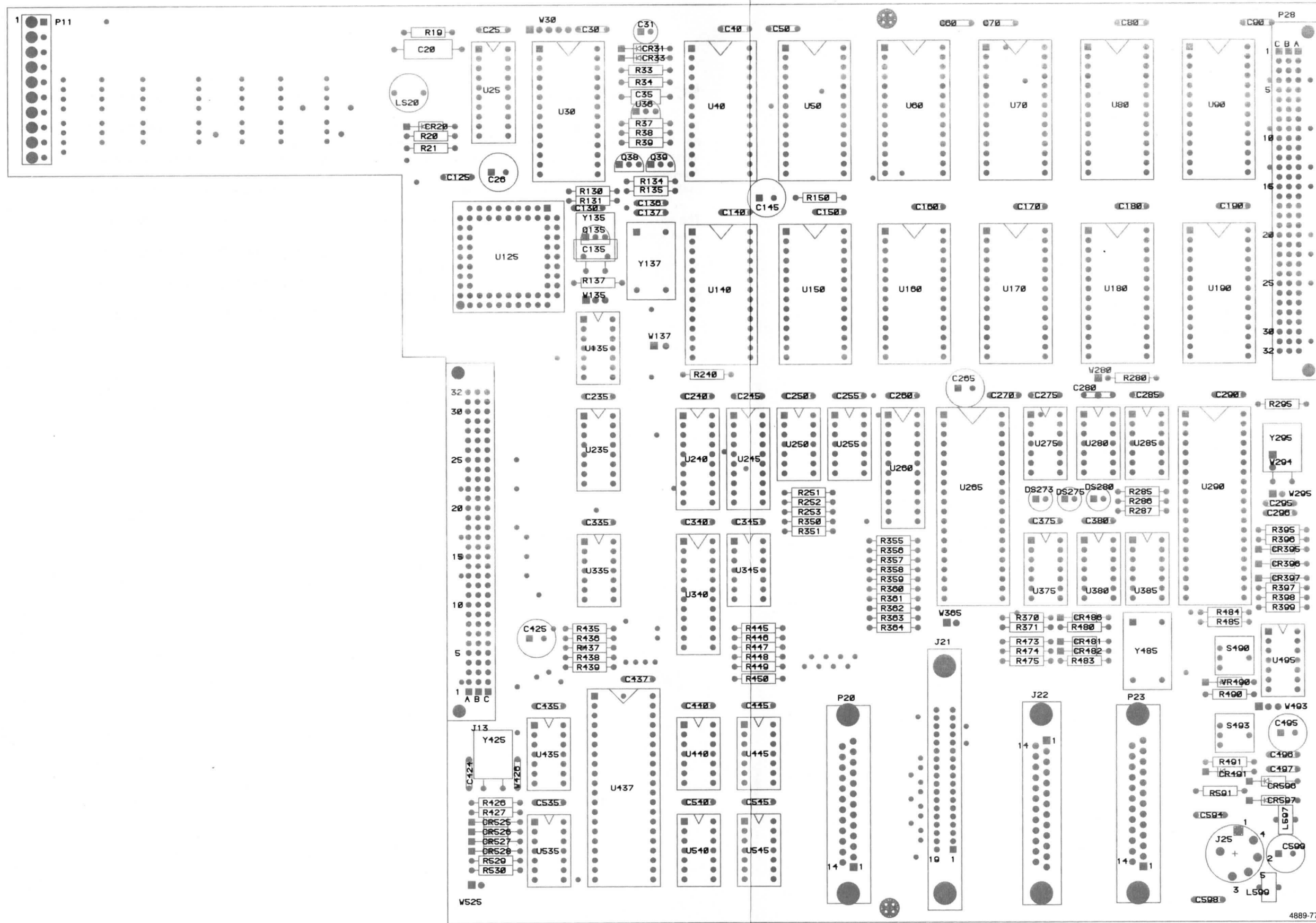
SCHEMATICS LIST

This section contains the schematic diagrams and component location diagrams for all 4107 circuit boards except those that are part of the Display Module (an OEM product). A separate service manual contains parts lists and schematics for the 119-1594-00 Display Module.

The schematics and diagrams in this section are arranged in the following order:

1. Terminal Control Board Component Locations
2. Terminal Control Board Schematics (A1-1 thru A1-6)
3. Display Control Board Component Locations
4. Display Control Board Schematics (A2-1 thru A2-10)
5. RAM3 Board Component Locations
6. RAM3 Board Schematics (A3-1 thru A3-3)
7. Keyboard (119-1593-00) Component Locations
8. Keyboard (119-1593-00) Schematic (A4-1)
9. Logic Power Supply Component Locations
10. Logic Power Supply Schematic (A5A1-1)

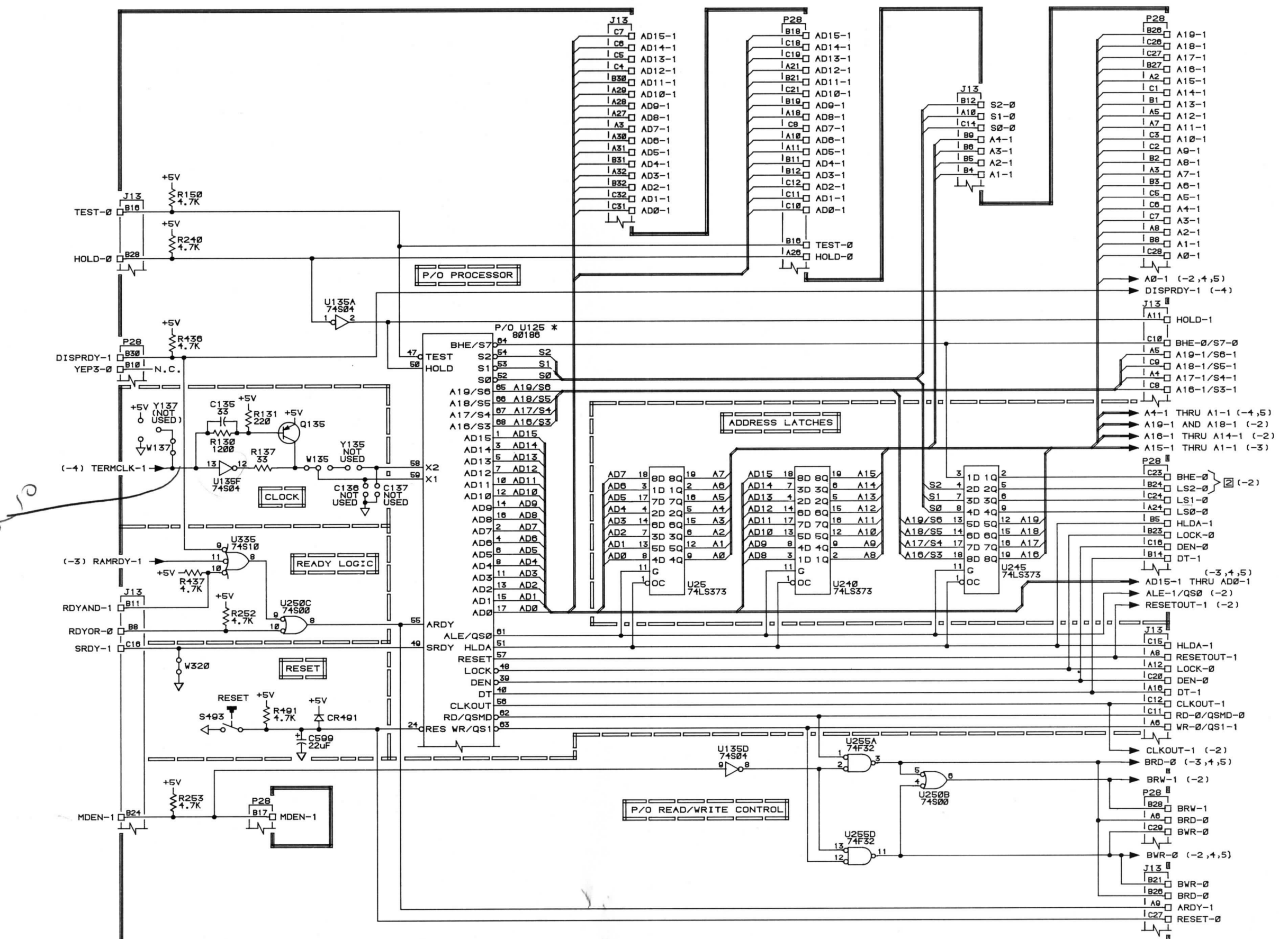
TERMINAL CONTROL
COMPONENT LOCATIONS



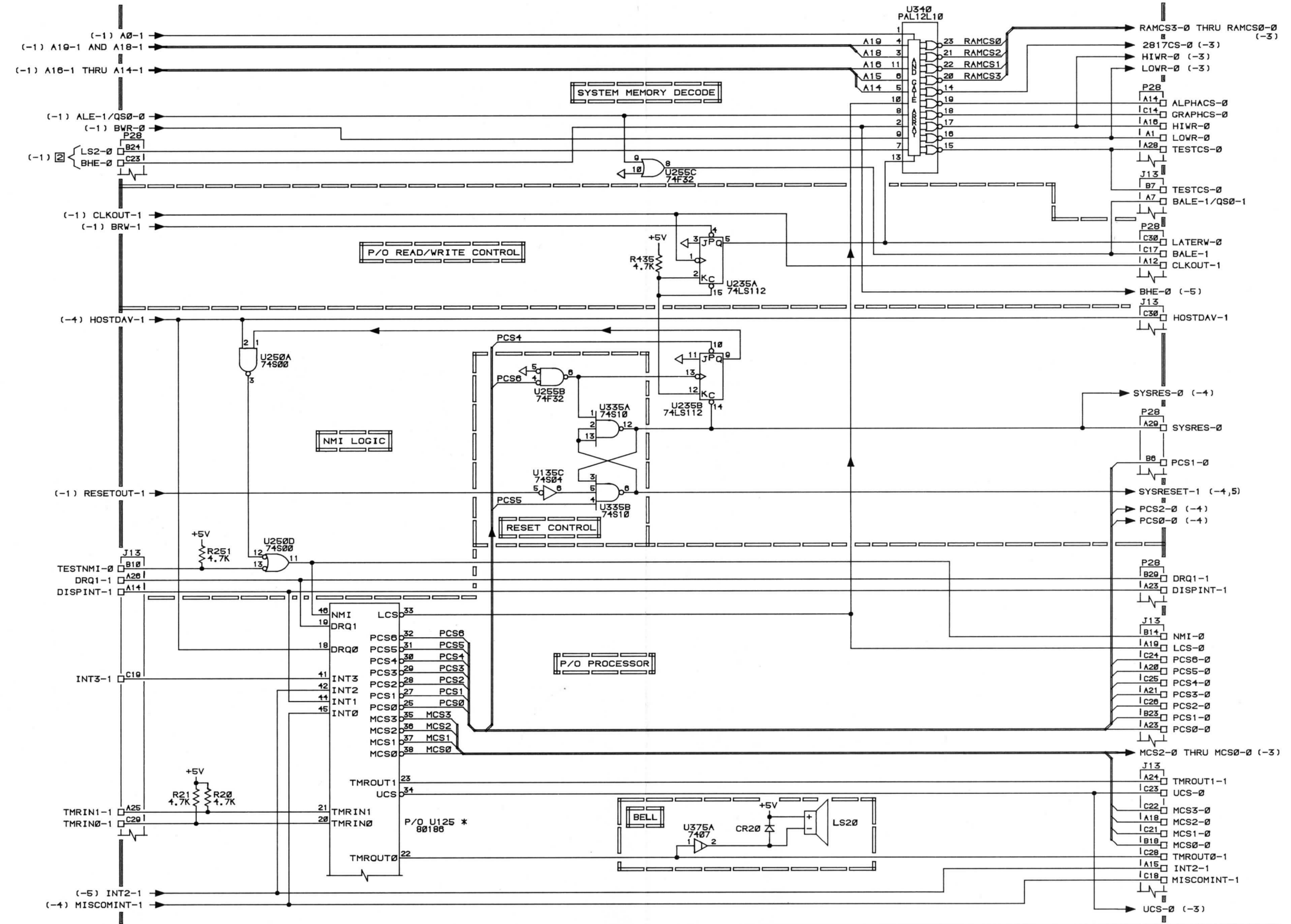
Terminal Control (670-8234-00) Component Locations.

4889-77

Handwritten note: *11/10/10*

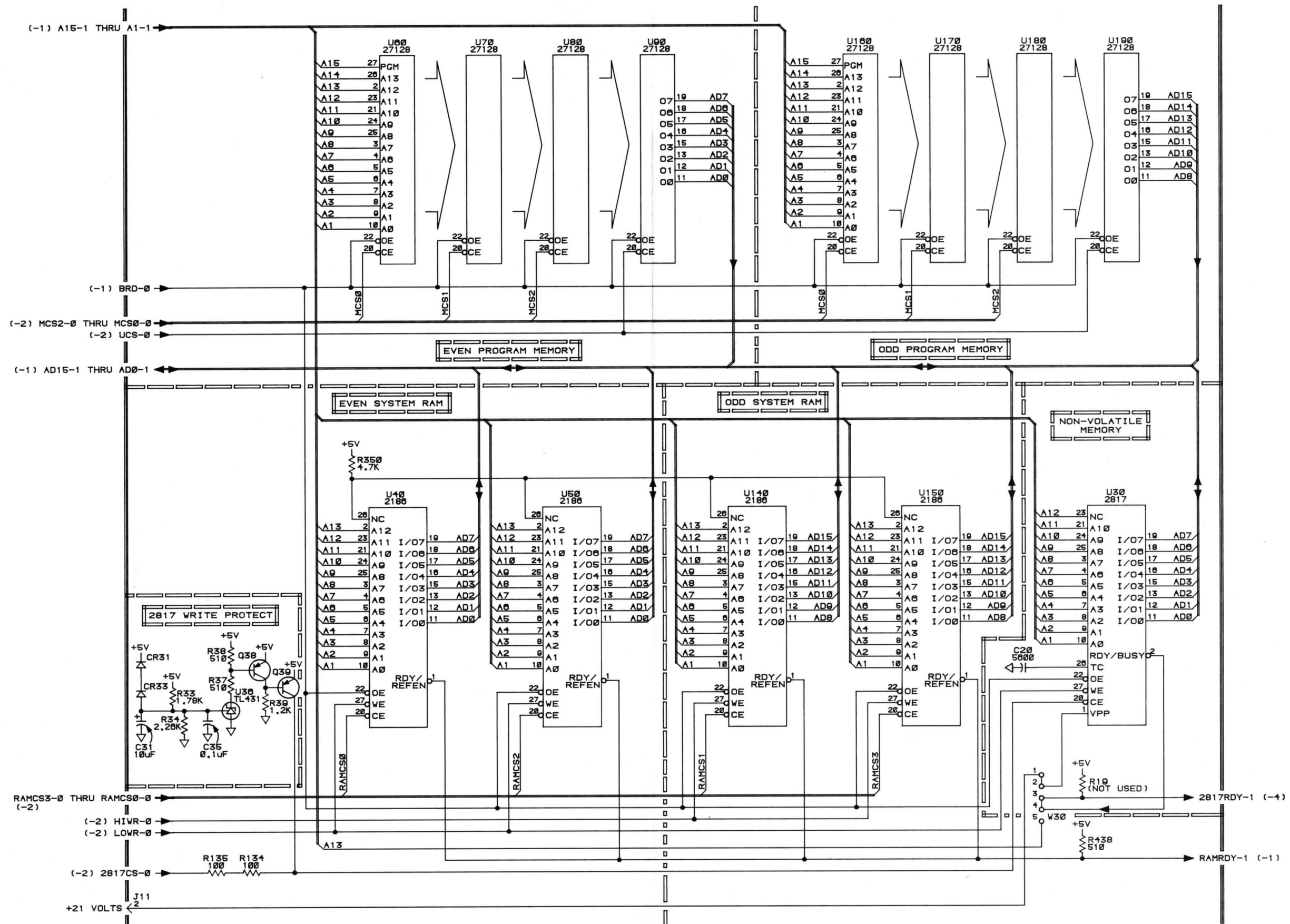


INSTRUMENT: 4107	NOTES: * P/O U125 ON SHEET #2 <input type="checkbox"/> INDICATES SHOWN MORE THAN ONCE AND WHERE (-)	BOARD: 670-8234-00 TERMINAL CONTROL BOARD	ASSEMBLY-SHEET: A1-1 (1 OF 6)
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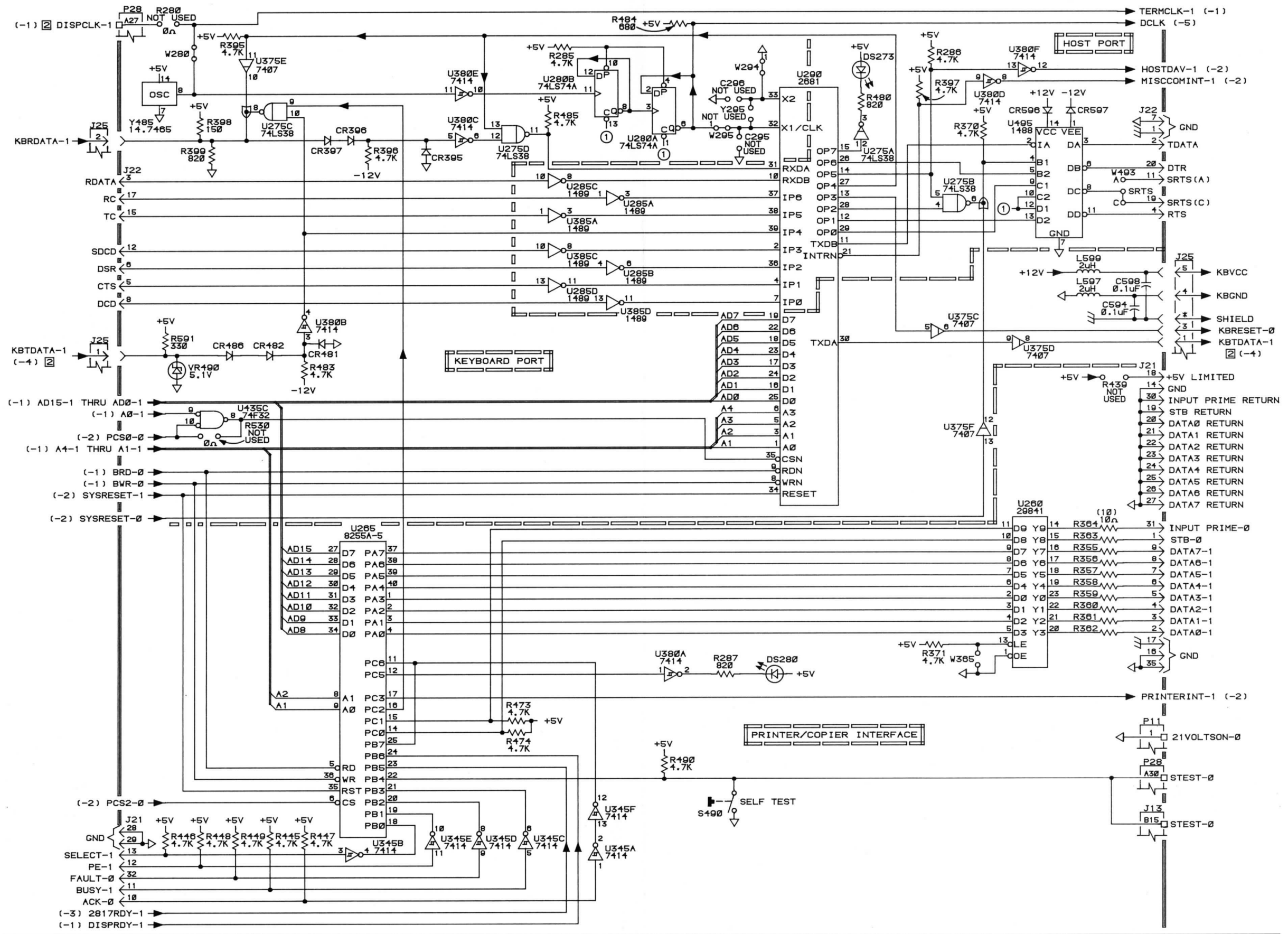
INSTRUMENT: 4107	NOTES: * P/O U125 ON SHEET #1 <input type="checkbox"/> INDICATES SHOWN MORE THAN ONCE AND WHERE (-)	BOARD: 670-8234-00 4889-52 TERMINAL CONTROL BOARD	ASSEMBLY-SHEET: A1-2 (2 OF 6)
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TERMINAL CONTROL BOARD 670-8234-00 A1-2

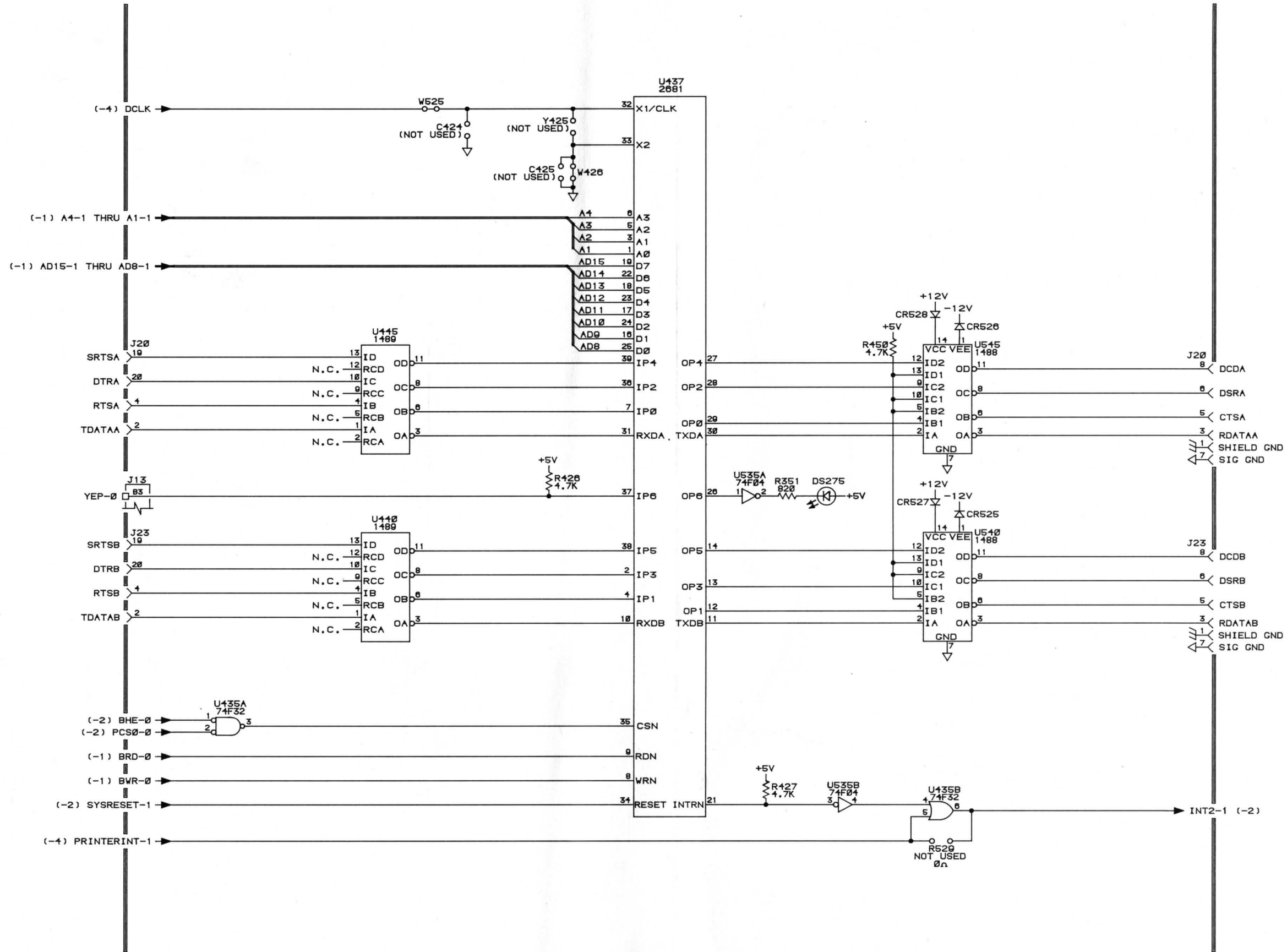


INSTRUMENT: <p style="text-align: center;">4107</p>	NOTES: <p style="text-align: center;">4880-S3</p>	BOARD: 670-8234-00 <p style="text-align: center;">TERMINAL CONTROL BOARD</p>	ASSEMBLY-SHEET: <p style="text-align: center;">A1-3 (3 OF 6)</p>
--	--	---	---

TERMINAL CONTROL
 670-8234-00
 A1-3

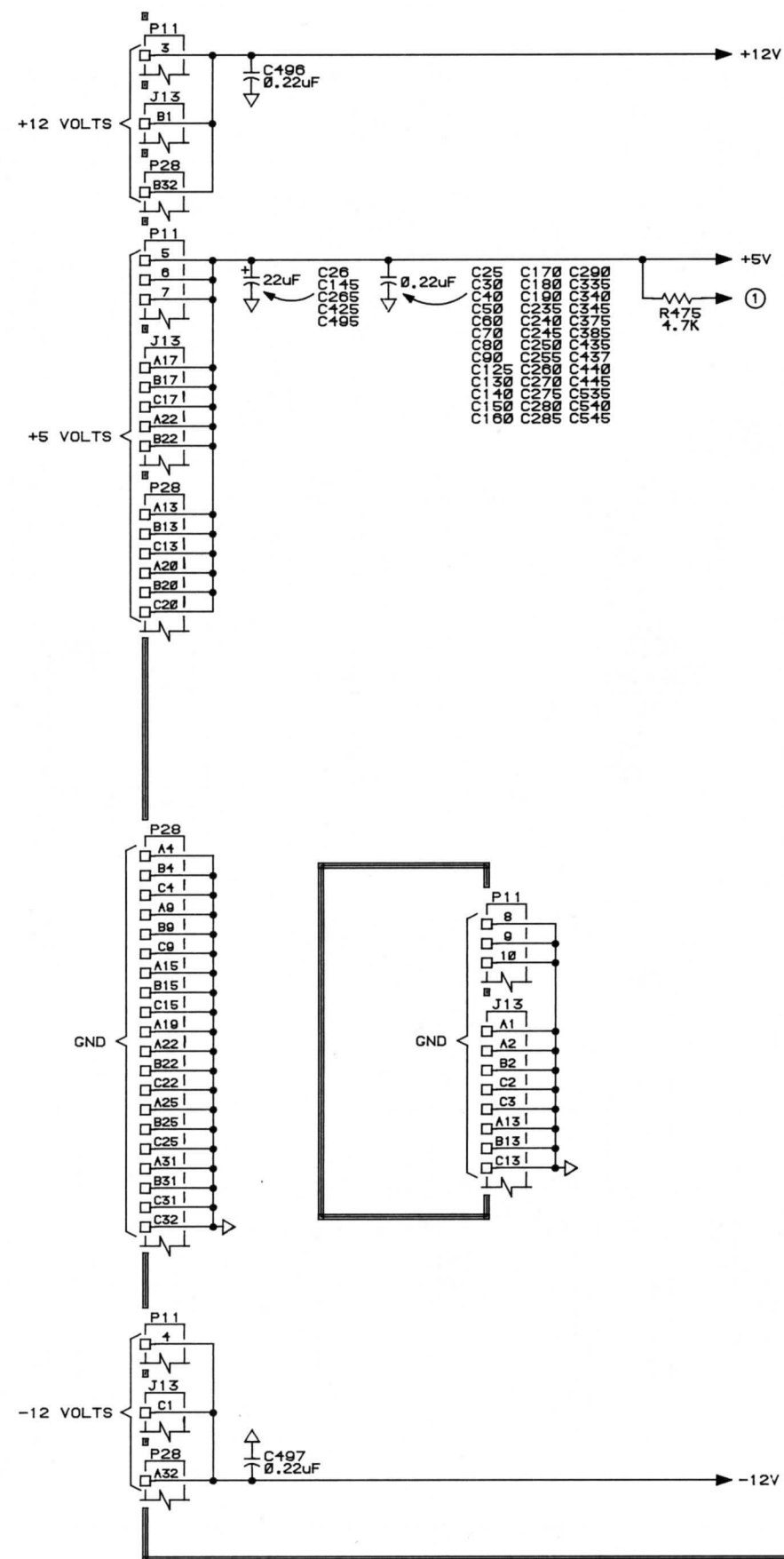


INSTRUMENT: 4107	NOTES: *THIS CONNECTOR PIN IN P25 IS THE CONNECTOR BODY KEYWAY. □ INDICATES SHOWN MORE THAN ONCE AND WHERE (-) 4889-S4	BOARD: 670-8234-00 TERMINAL CONTROL BOARD	ASSEMBLY-SHEET: A1-4 (4 OF 6)
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INSTRUMENT: 4107	NOTES:	BOARD: 670-8234-00 TERMINAL CONTROL BOARD 2 PPI	ASSEMBLY-SHEET: A1-5 (5 OF 6)
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1880-S5



DEVICE TYPE	PINS	
	+5V	GND
ALL 14 PIN IC'S	14	7
74LS112	16	8
74LS373	20	10
29841 PAL12L10	24	12
8255A-5	26	7
27128	28, 1	14
2186-25 2817	28	14
2681	1, 40	20

INSTRUMENT :
4107

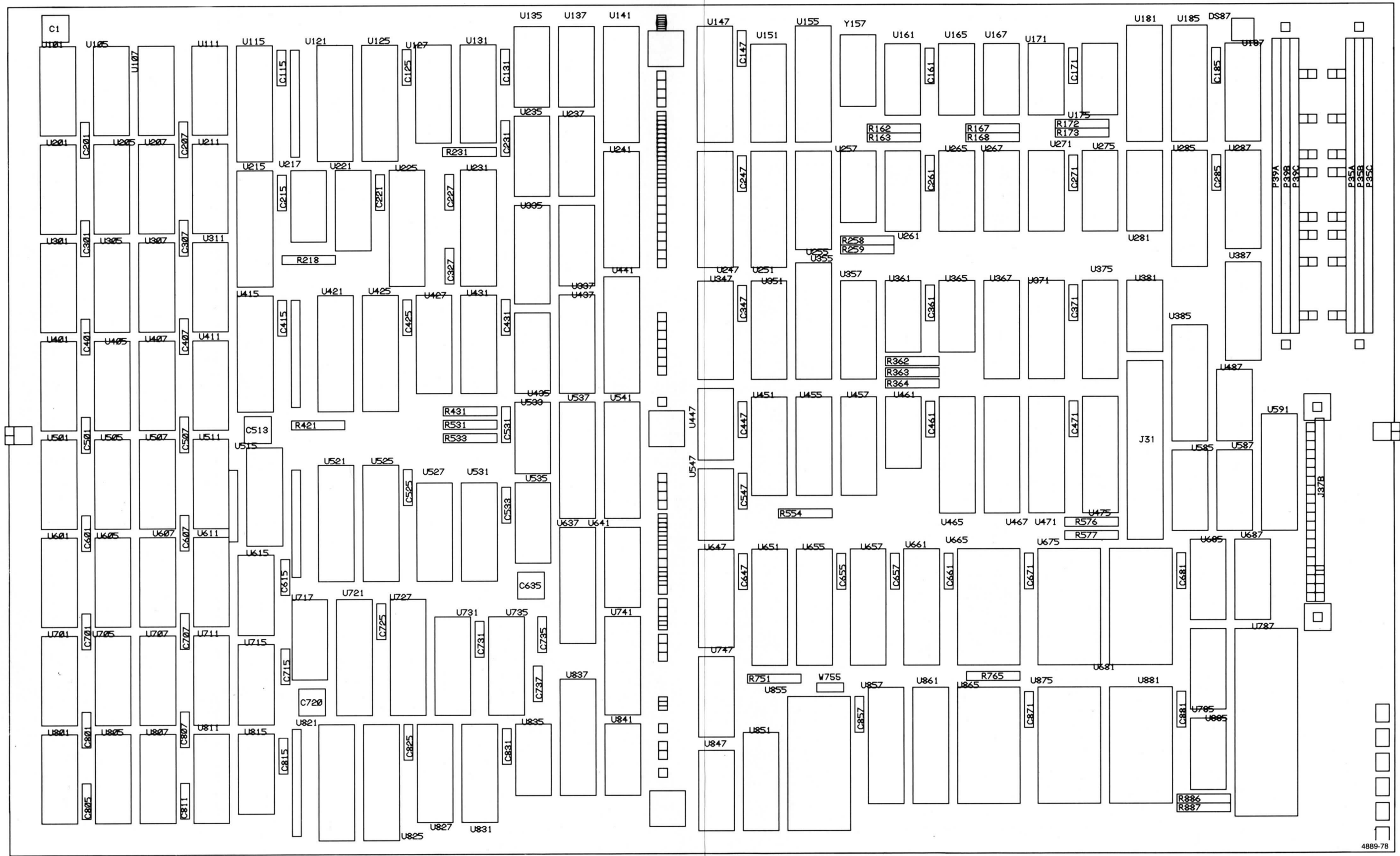
NOTES :

4889-56

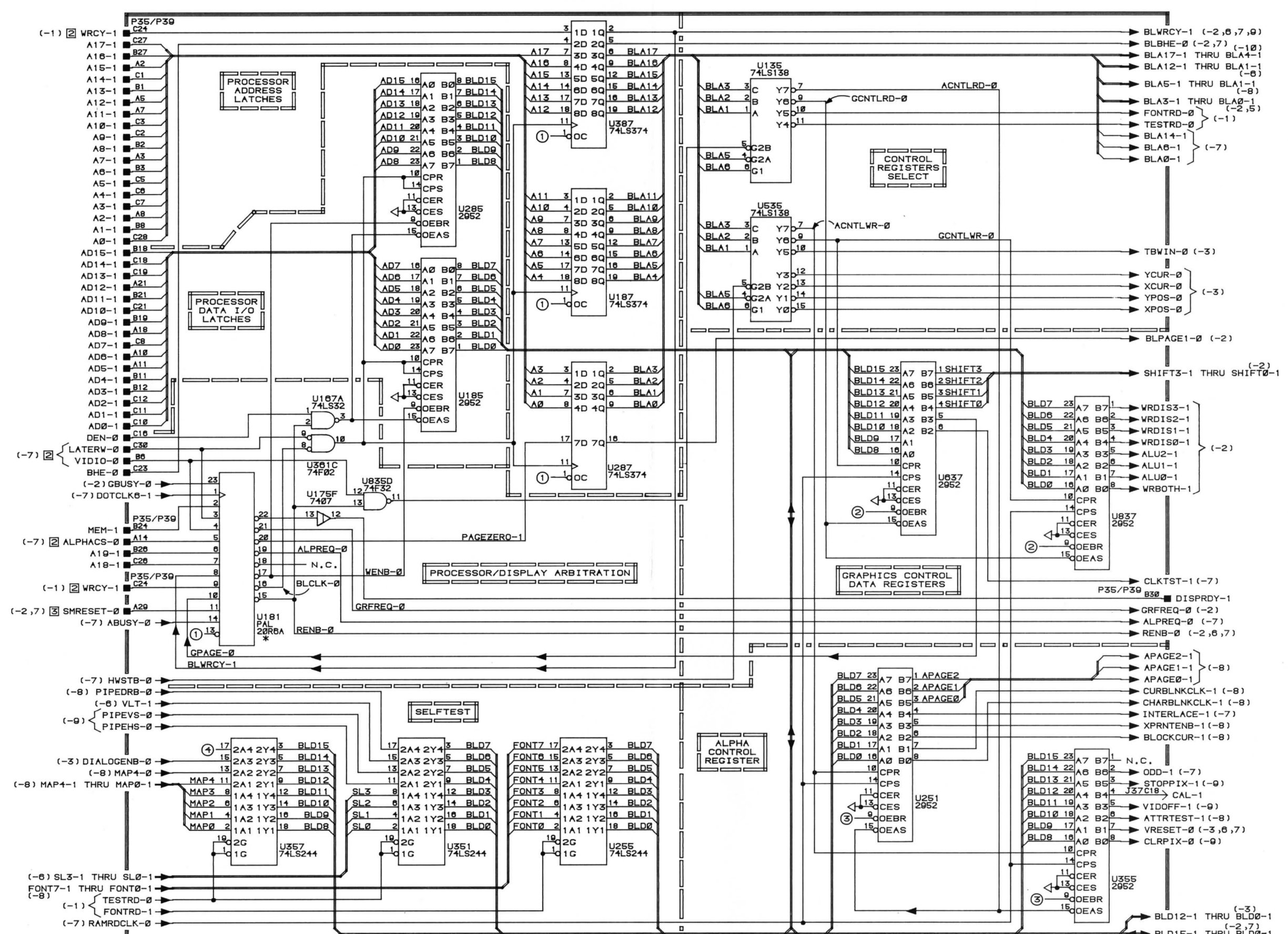
BOARD : 670-8234-00
TERMINAL CONTROL BOARD
POWER

ASSEMBLY-SHEET :
A1-6
(6 OF 6)

DISPLAY CONTROL
COMPONENT LOCATIONS



Display Control (670-8233-00) Component Locations.



INSTRUMENT:
4107

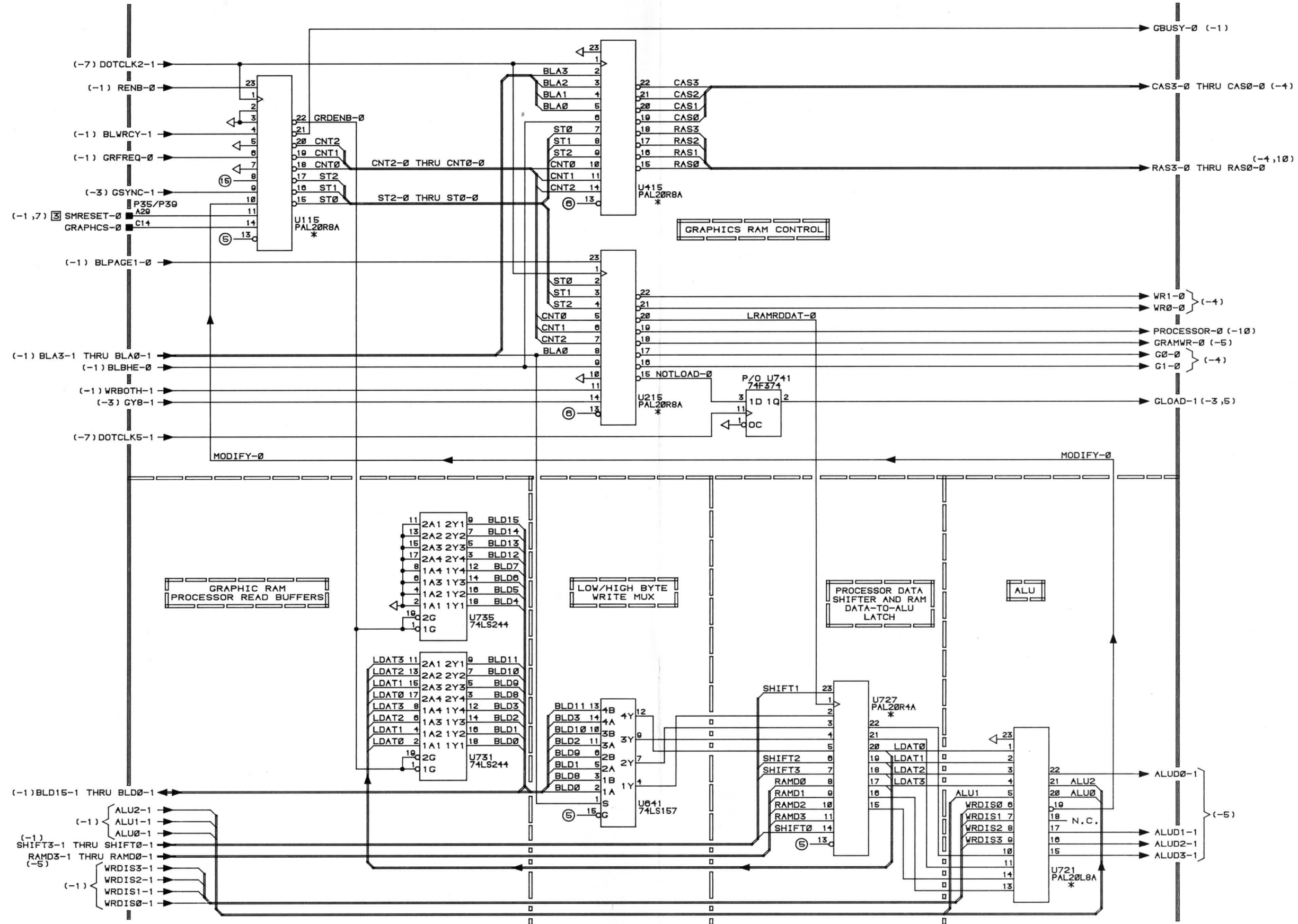
NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY.
4889-S7

INDICATES SHOWN MORE THAN ONCE AND WHERE (-)

BOARD: 670-8233-00
DISPLAY CONTROL BOARD

ASSEMBLY-SHEET:
A2-1
(1 OF 10)

DISPLAY CONTROL 670-8233-00 A2-1



INSTRUMENT:
4107

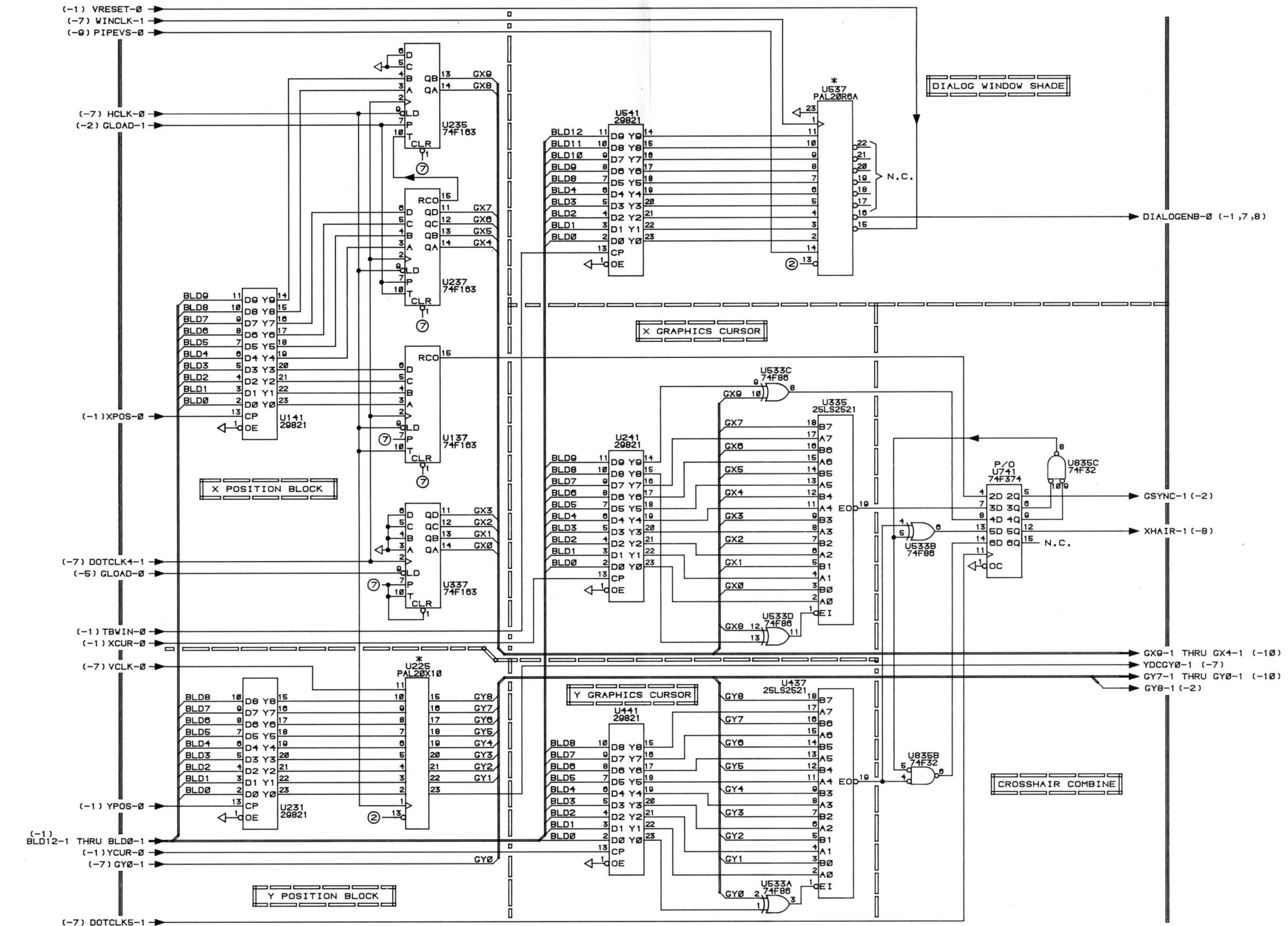
NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY.

4889-SB

INDICATES SHOWN MORE THAN ONCE AND WHERE (-)

BOARD: 670-8233-00
DISPLAY CONTROL BOARD

ASSEMBLY-SHEET:
A2-2
(2 OF 10)



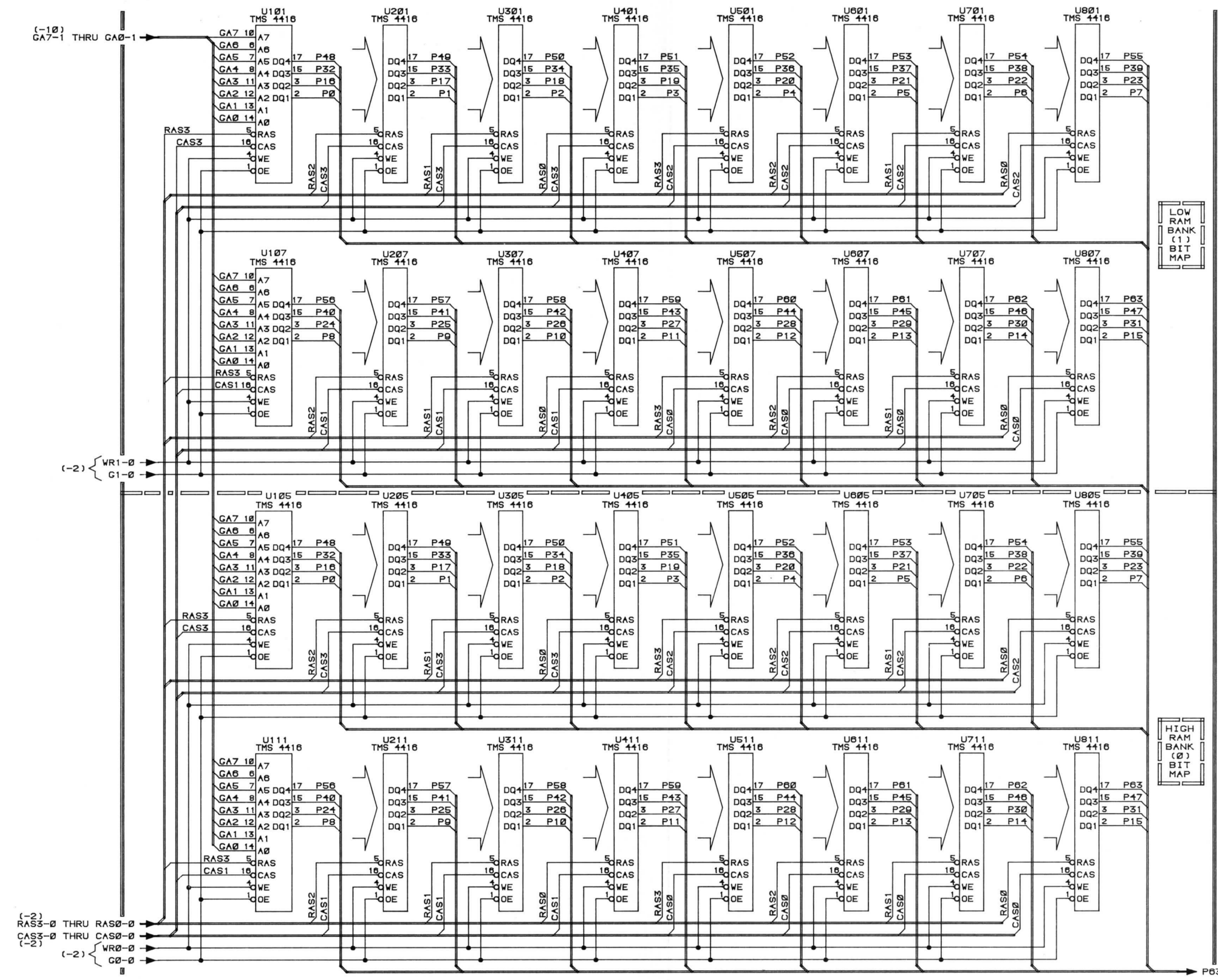
INSTRUMENT:
4107

NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY.

4889-S9

BOARD: 670-8233-00
DISPLAY CONTROL BOARD

ASSEMBLY-SHEET:
A2-3
(3 OF 10)



LOW
RAM
BANK
(1)
BIT
MAP

HIGH
RAM
BANK
(0)
BIT
MAP

INSTRUMENT:
4107

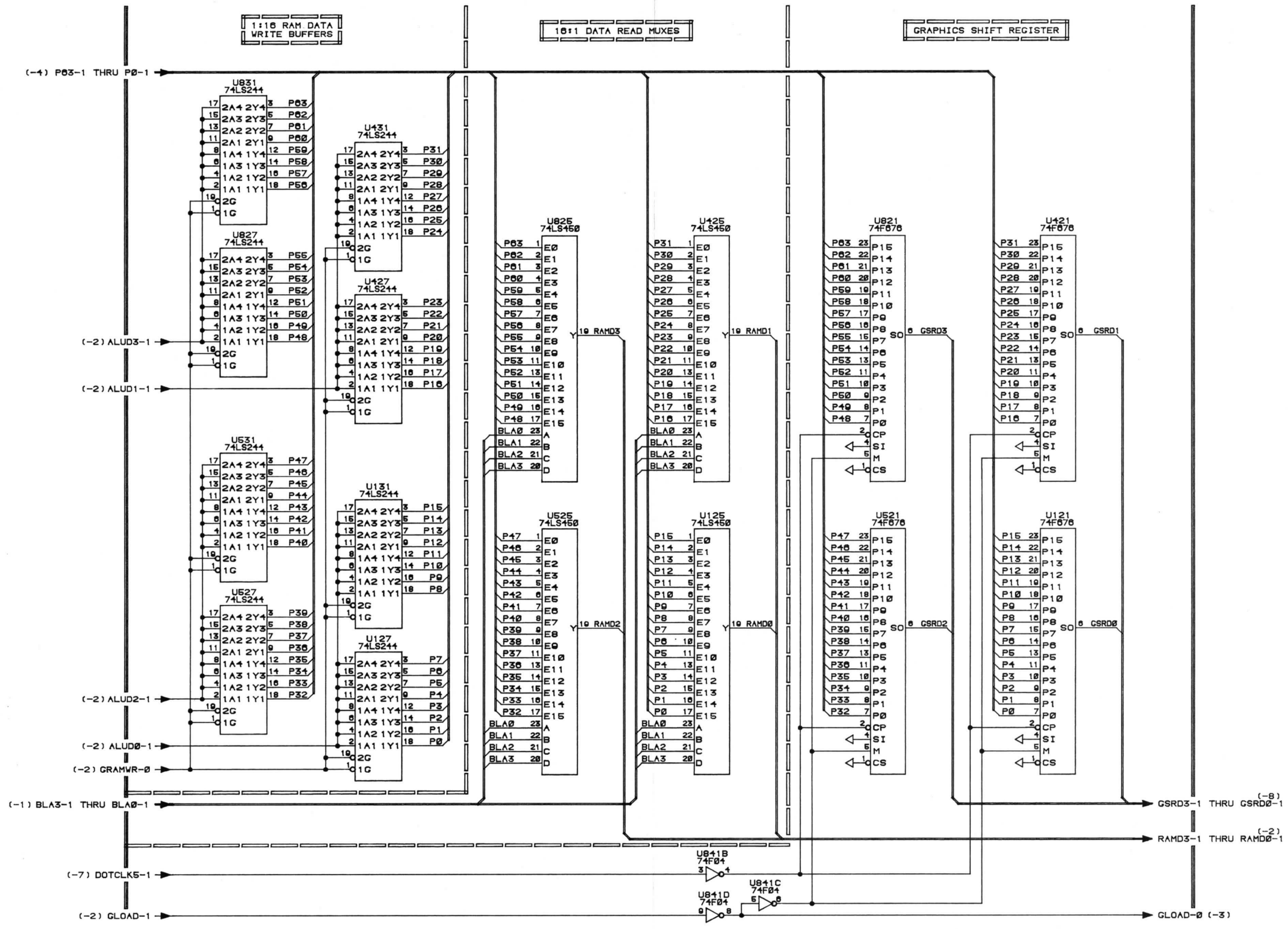
NOTES:
4889-S10

BOARD: 670-8233-00
DISPLAY CONTROL BOARD

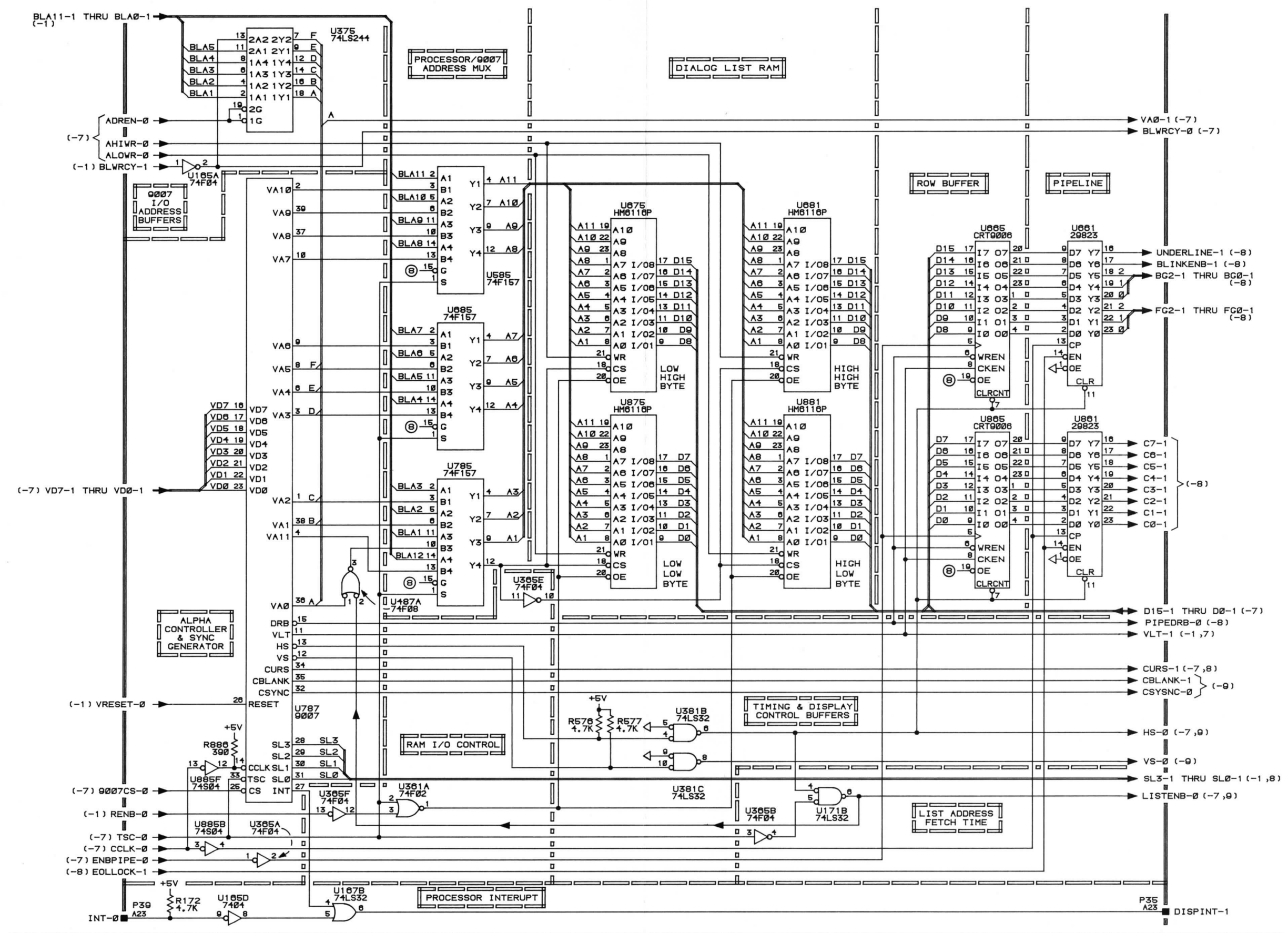
ASSEMBLY-SHEET:
A2-4
(4 OF 10)

DISPLAY CONTROL
670-8233-00

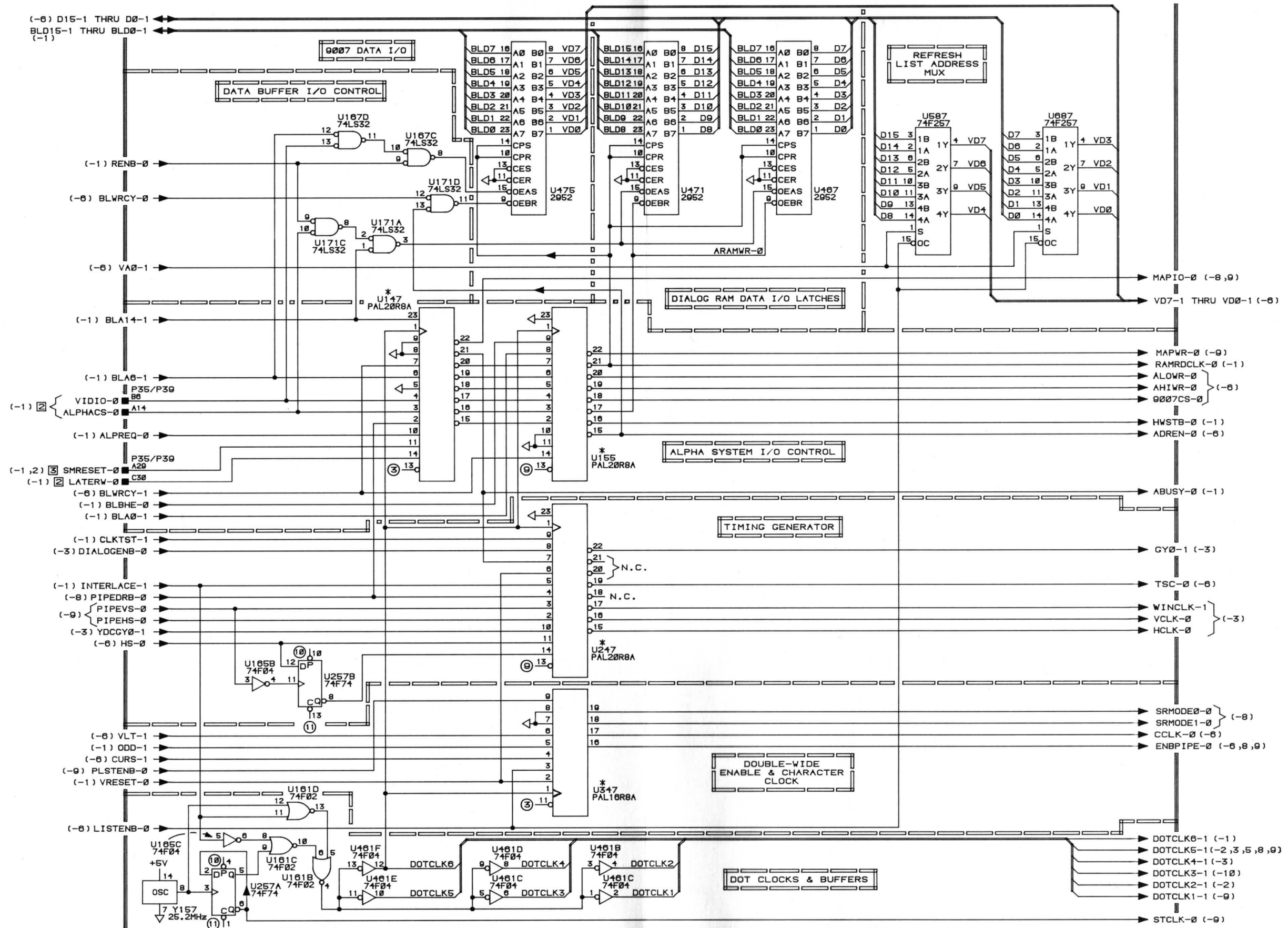
A2-4



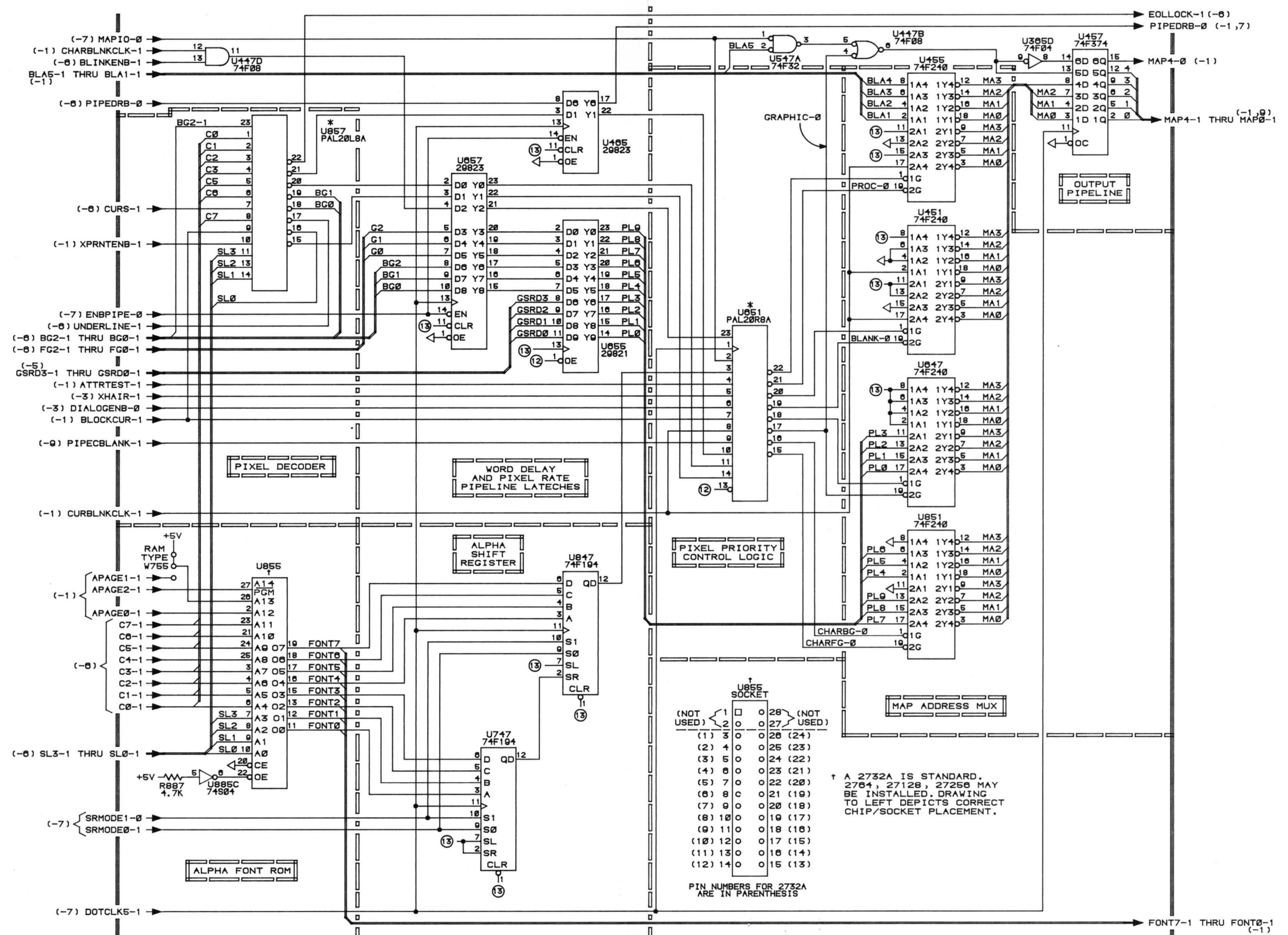
INSTRUMENT: 4107	NOTES:	BOARD: 670-8233-00 4889-S11 DISPLAY CONTROL BOARD	ASSEMBLY-SHEET: A2-5 (5 OF 10)
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INSTRUMENT: 4107	NOTES: 4889-S12	BOARD: 670-8233-00 DISPLAY CONTROL BOARD	ASSEMBLY-SHEET: A2-6 (6 OF 10)
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INSTRUMENT: 4107	NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY □ INDICATES SHOWN MORE THAN ONCE AND WHERE (-)	BOARD: 670-8233-00 DISPLAY CONTROL BOARD	ASSEMBLY-SHEET: A2-7 (7 OF 10)
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INSTRUMENT:
4107

NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY

4889-S14

BOARD: 670-8233-00
DISPLAY CONTROL BOARD

ASSEMBLY-SHEET:
A2-8
(8 OF 10)

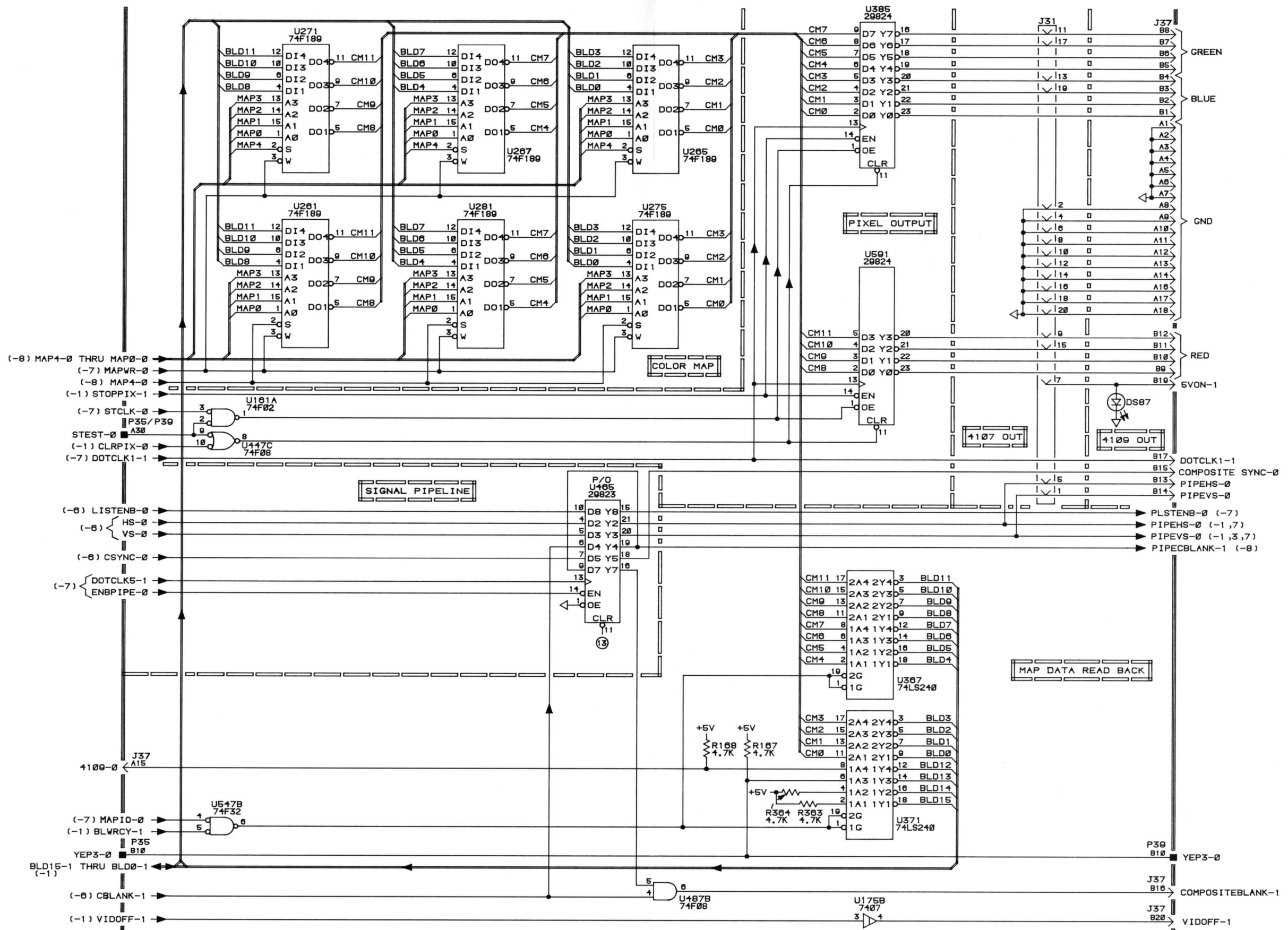
U855 SOCKET

(NOT USED)	1	0	28	(NOT USED)
(1)	3	0	26	(24)
(2)	4	0	25	(23)
(3)	5	0	24	(22)
(4)	6	0	23	(21)
(5)	7	0	22	(20)
(6)	8	0	21	(19)
(7)	9	0	20	(18)
(8)	10	0	19	(17)
(9)	11	0	18	(16)
(10)	12	0	17	(15)
(11)	13	0	16	(14)
(12)	14	0	15	(13)

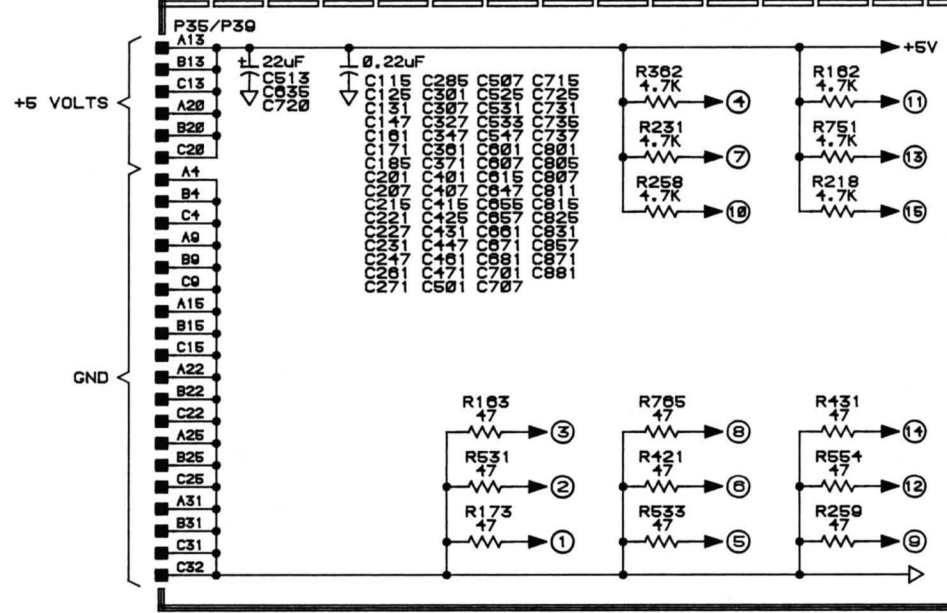
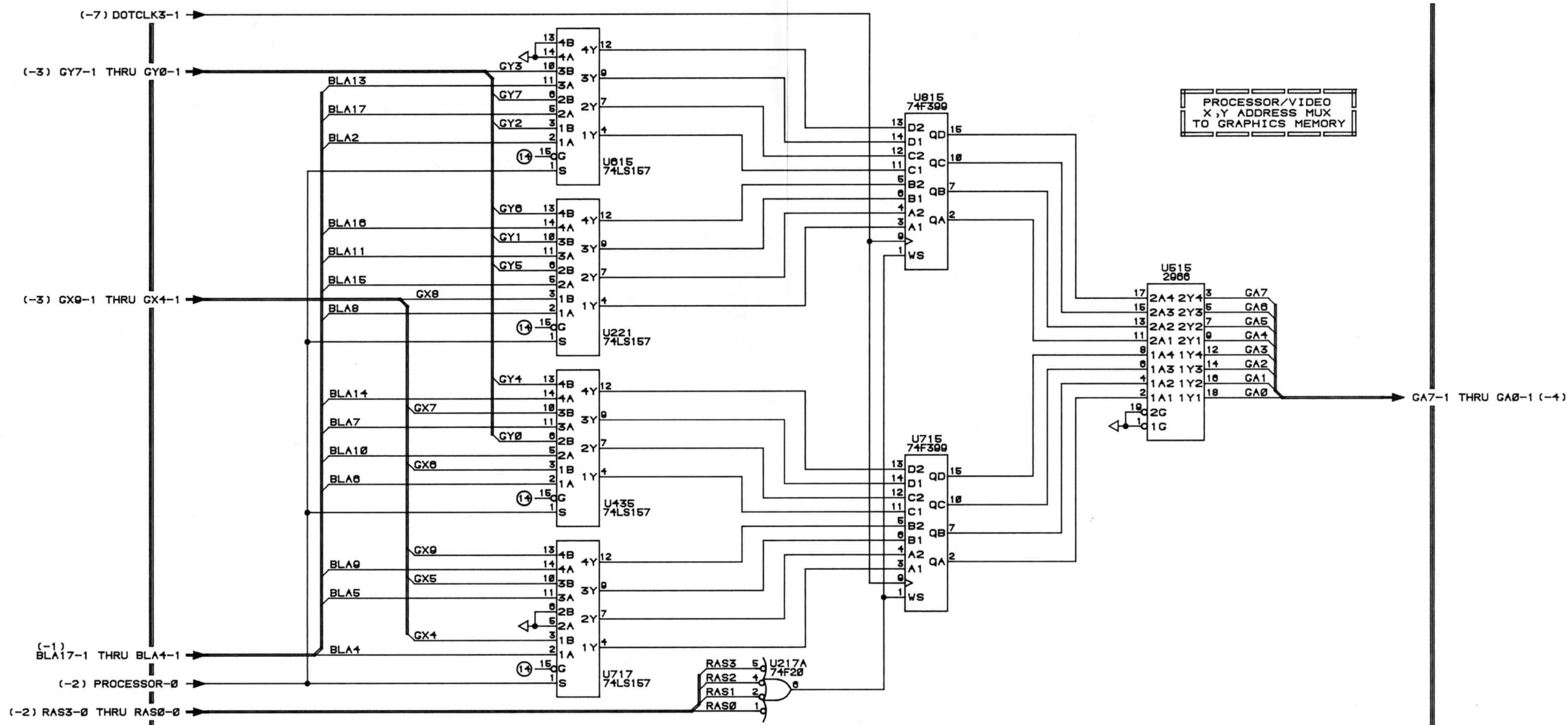
PIN NUMBERS FOR 2732A ARE IN PARENTHESIS

† A 2732A IS STANDARD. 2764, 27128, 27256 MAY BE INSTALLED. DRAWING TO LEFT DEPICTS CORRECT CHIP/SOCKET PLACEMENT.

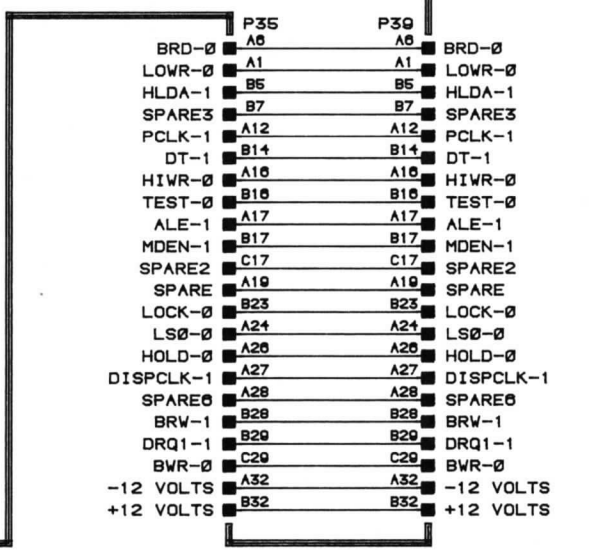
DISPLAY CONTROL
670-8233-00
A2-8



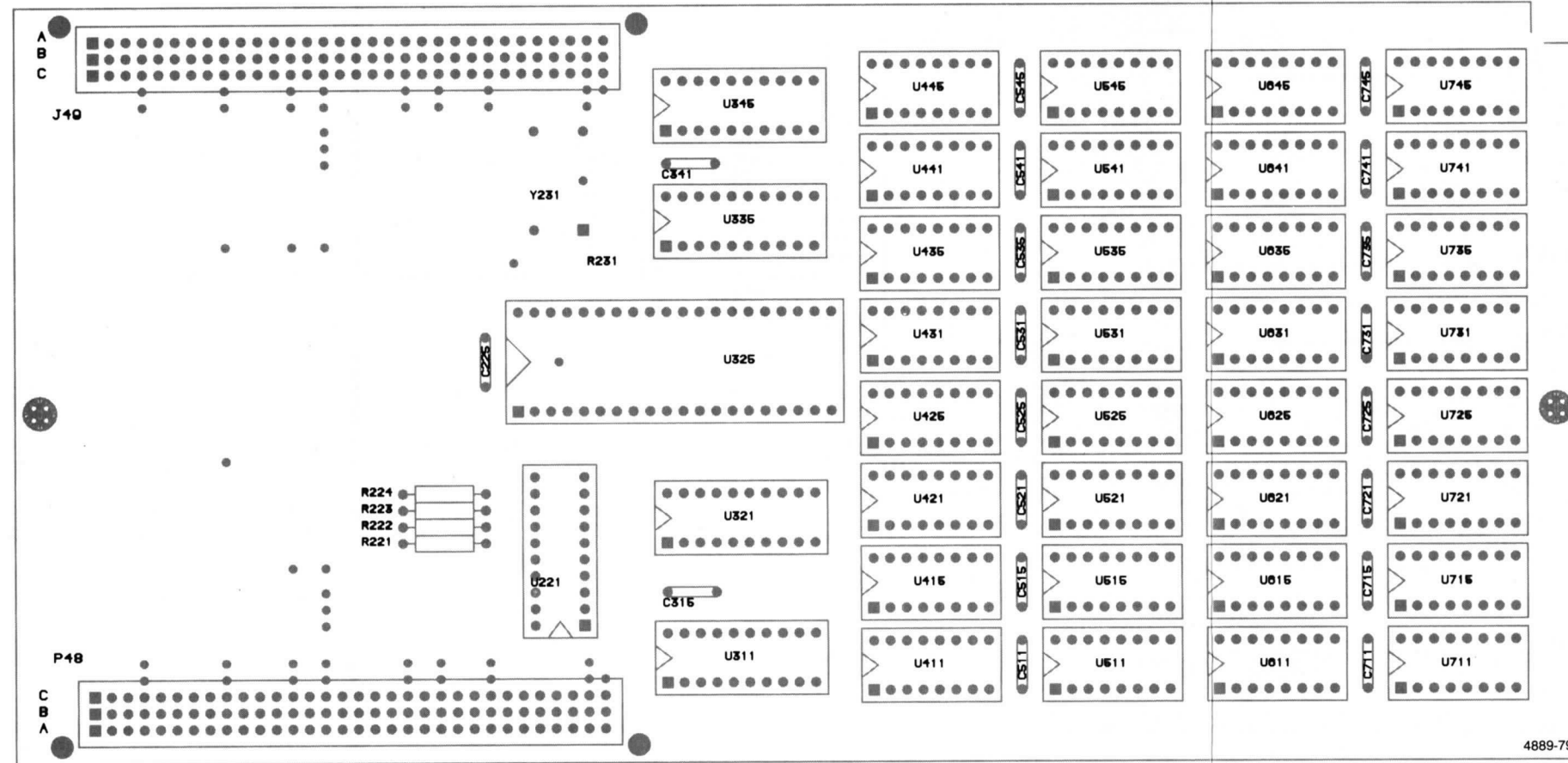
INSTRUMENT: 4107	NOTES:	BOARD: 670-8233-00 4889-S15 DISPLAY CONTROL BOARD	ASSEMBLY-SHEET: A2-9 (9 OF 10)
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IC SUPPLIES		
DEVICE TYPE	PIN	
	+5V	GND
ALL 14 PIN IC'S	14	7
ALL 16 PIN IC'S	16	8
TMS4418	9	18
ALL 20 PIN IC'S	20	10
CRT9006	13	24
OTHER 24 PIN IC'S	24	12
2732A	28	14
9007	21	40

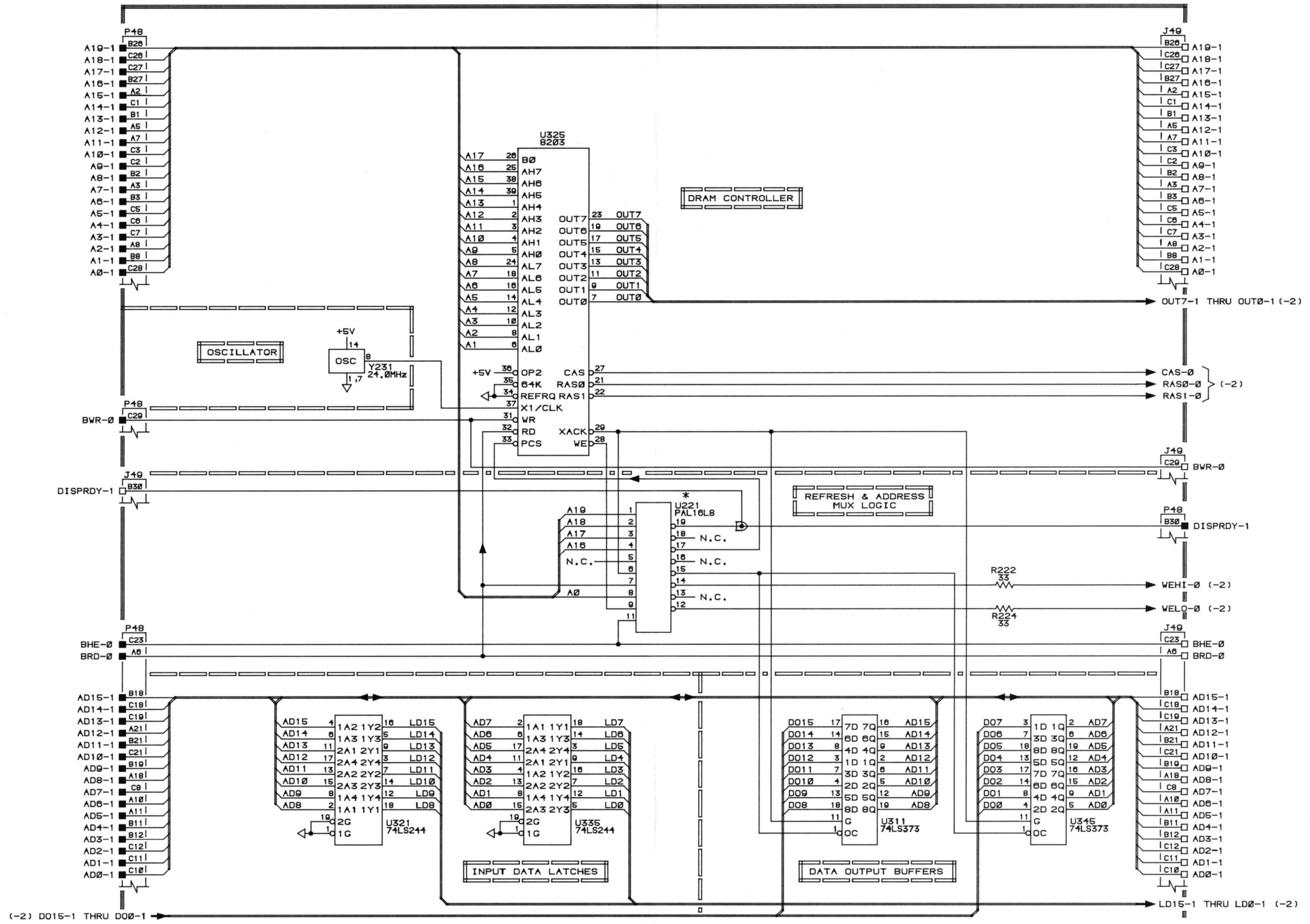


RAM 3
COMPONENT LOCATIONS

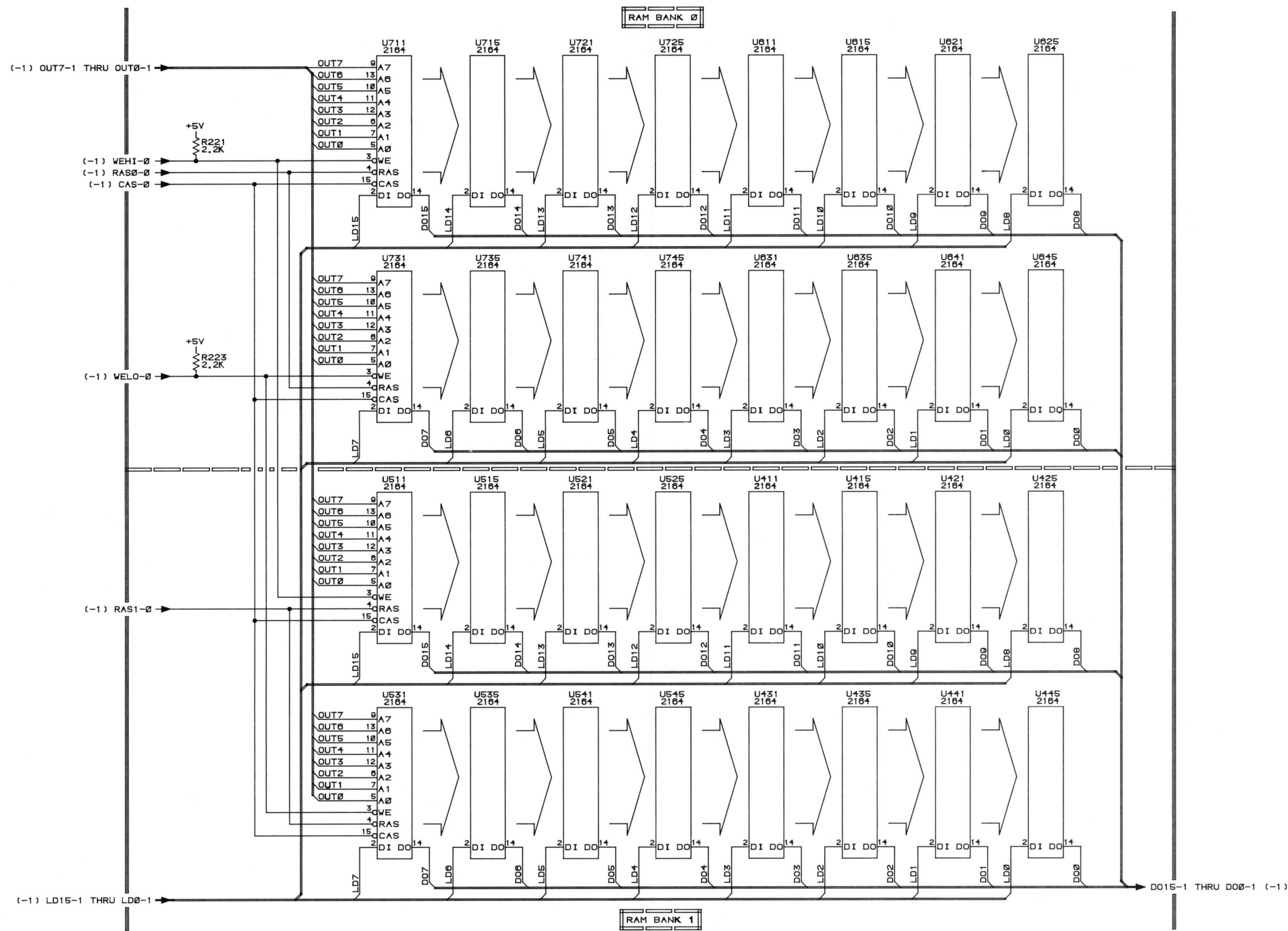


4889-79

RAM 3 (670-7196-00) Component Locations.



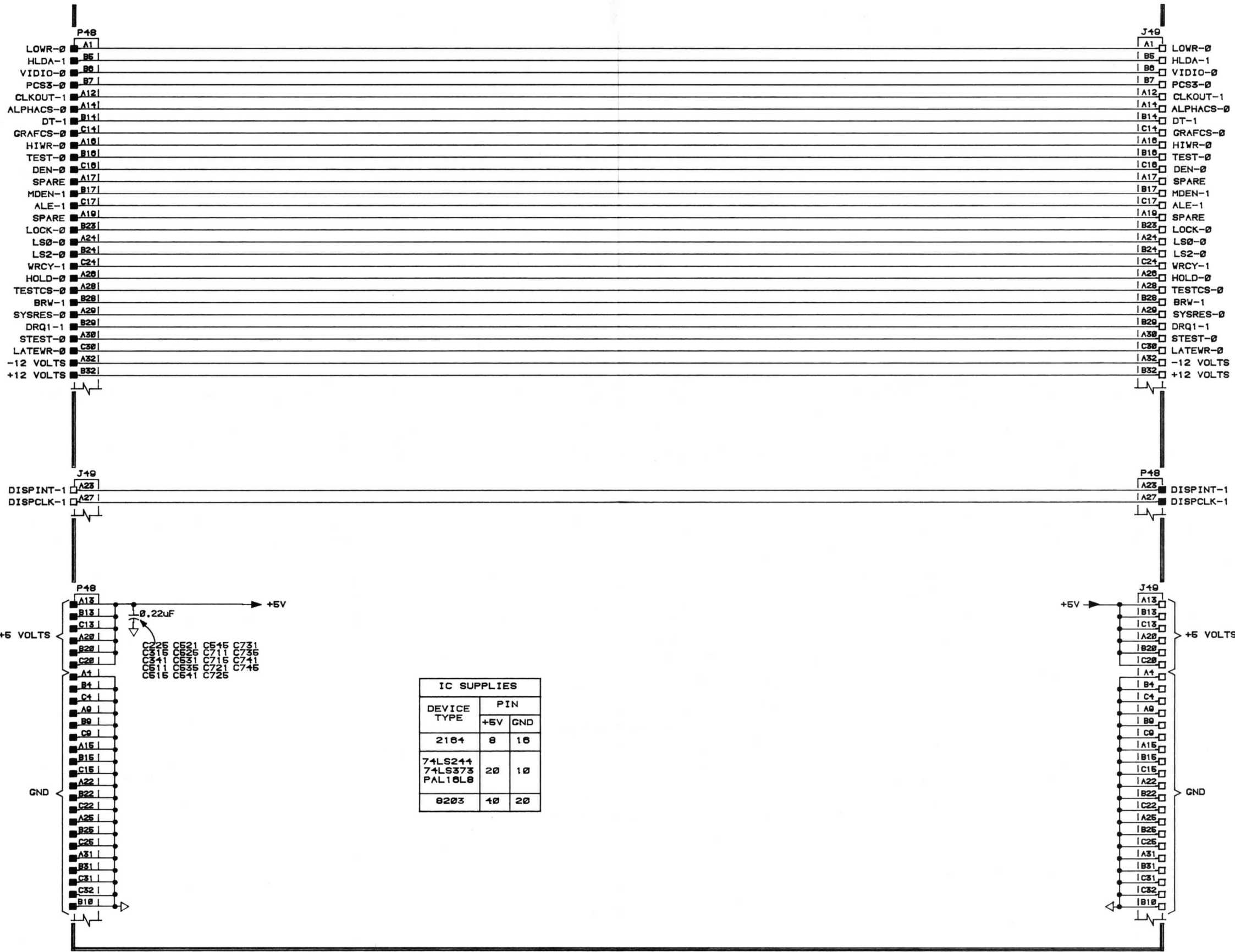
INSTRUMENT: <p style="text-align: center;">4107</p>	NOTES: * REFER TO THE THEORY OF OPERATION SECTION OF THE SERVICE MANUAL FOR FURTHER DESCRIPTIONS OF PAL DEVICES AND THEIR RELATED CIRCUITRY. <p style="text-align: center;">4889-S17</p>	BOARD: 670-7196-00 <p style="text-align: center;">RAM 3 BOARD</p>	ASSEMBLY-SHEET: <p style="text-align: center;">A3-1 (1 OF 3)</p>
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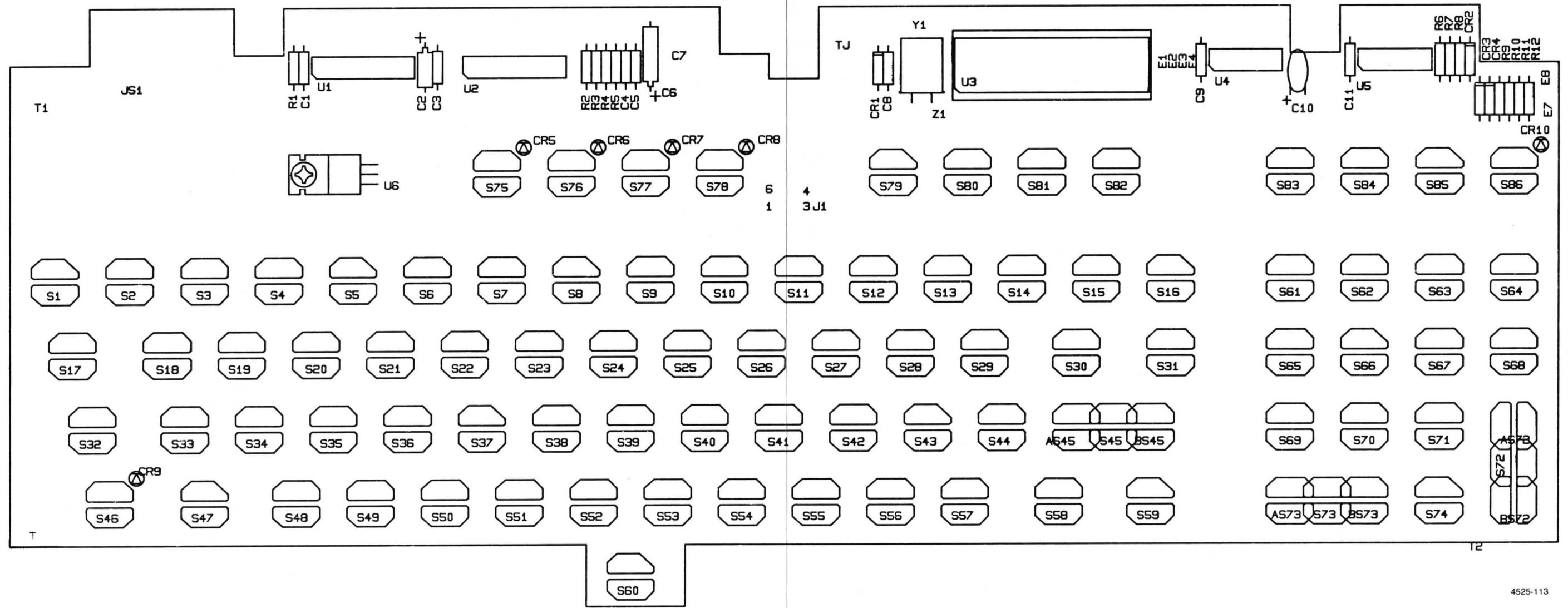


INSTRUMENT: 4107	NOTES:	BOARD: 670-7196-00 4889-S18 RAM 3 BOARD	ASSEMBLY-SHEET: A3-2 (2 OF 3)
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RAM3
670-7196-00

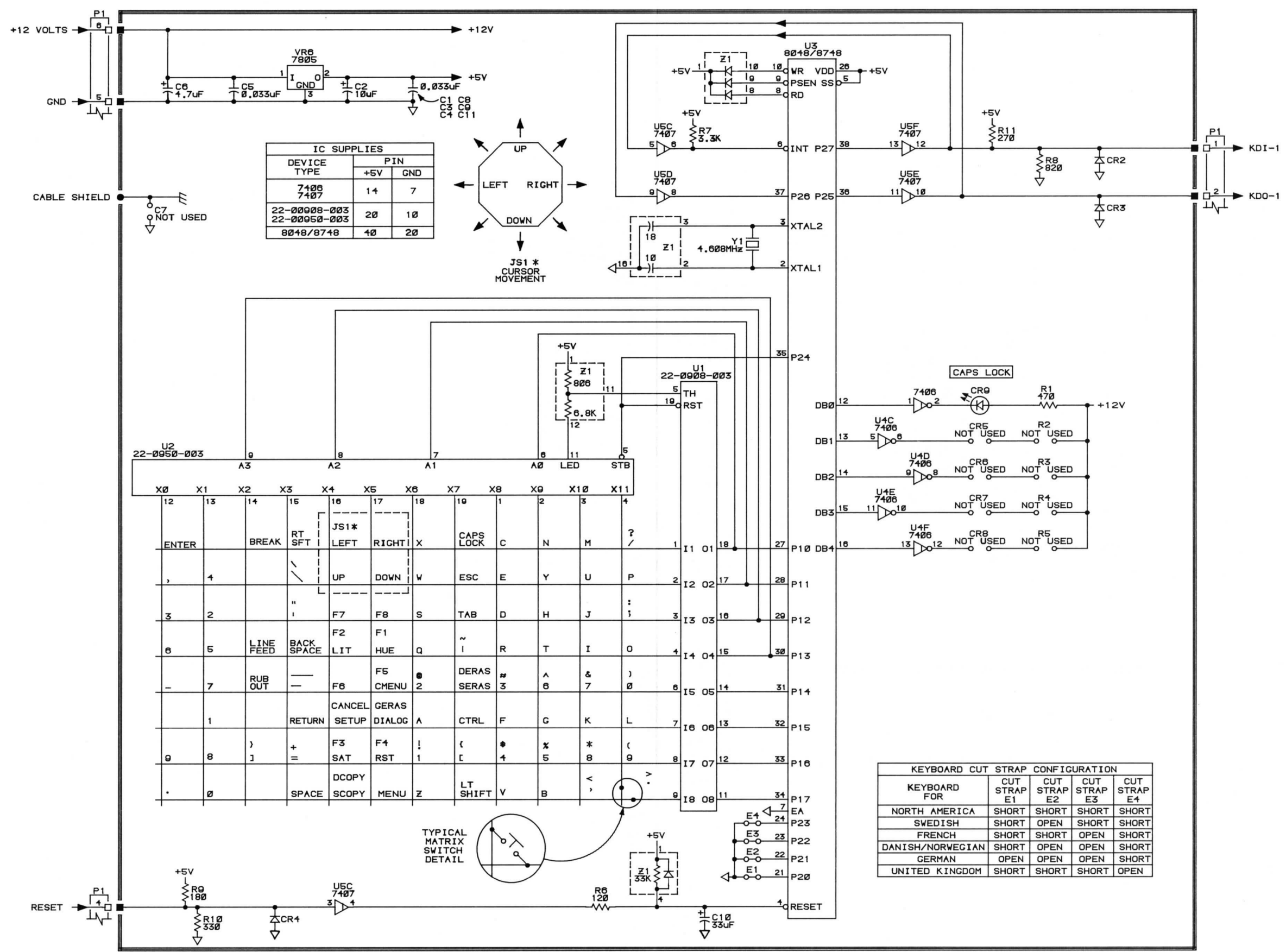
A3-2





Keyboard (119-1592-00) Component Locations.

119-1592-00 KEYBOARD
COMPONENT LOCATIONS



INSTRUMENT:
119-1592-01
(FOR USE WITH 4107)

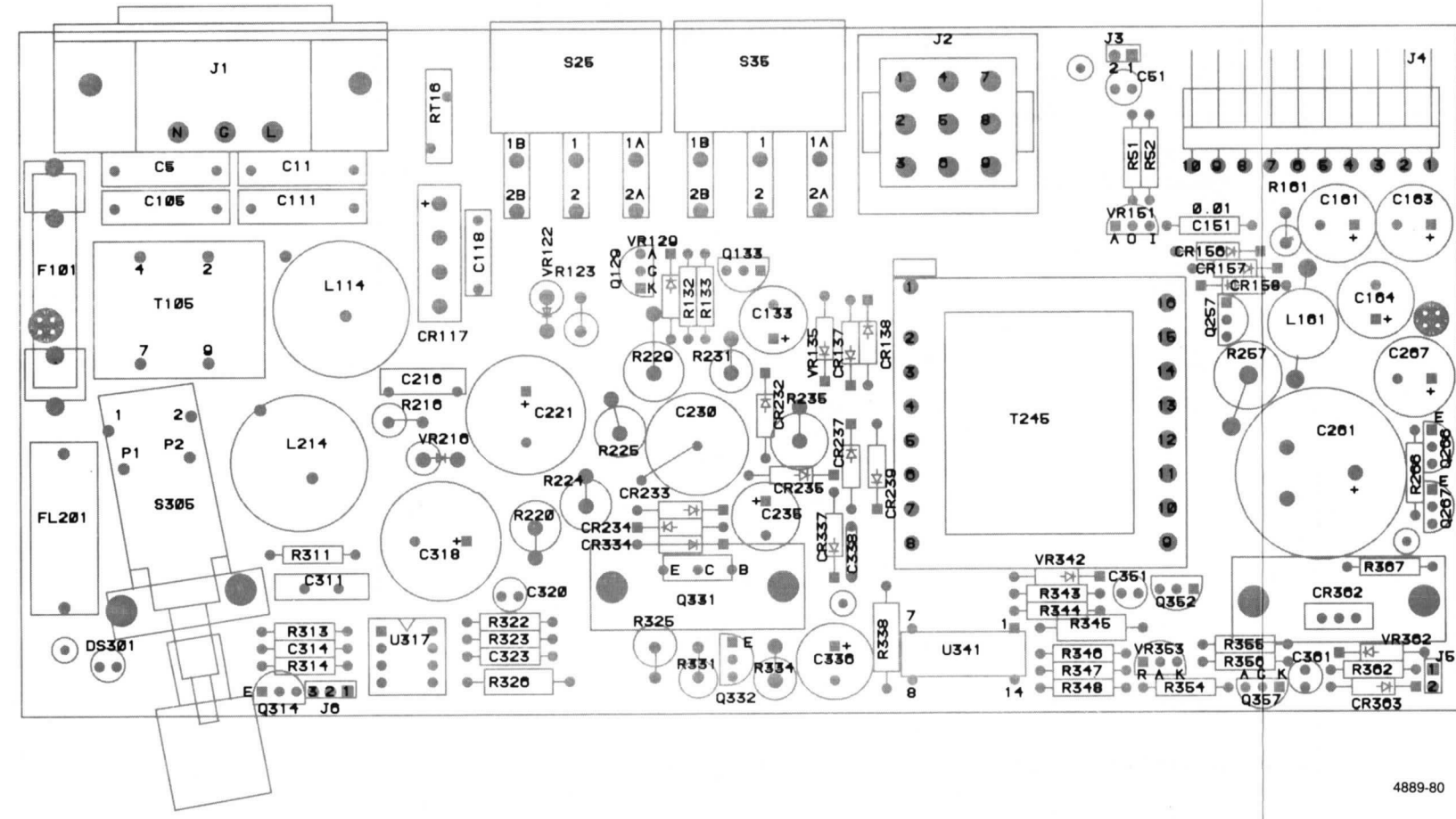
NOTES:

KEYTRONIC CORPORATION
4889-S20

BOARD:
KEYBOARD

ASSEMBLY-SHEET:
A4-1
(1 OF 1)

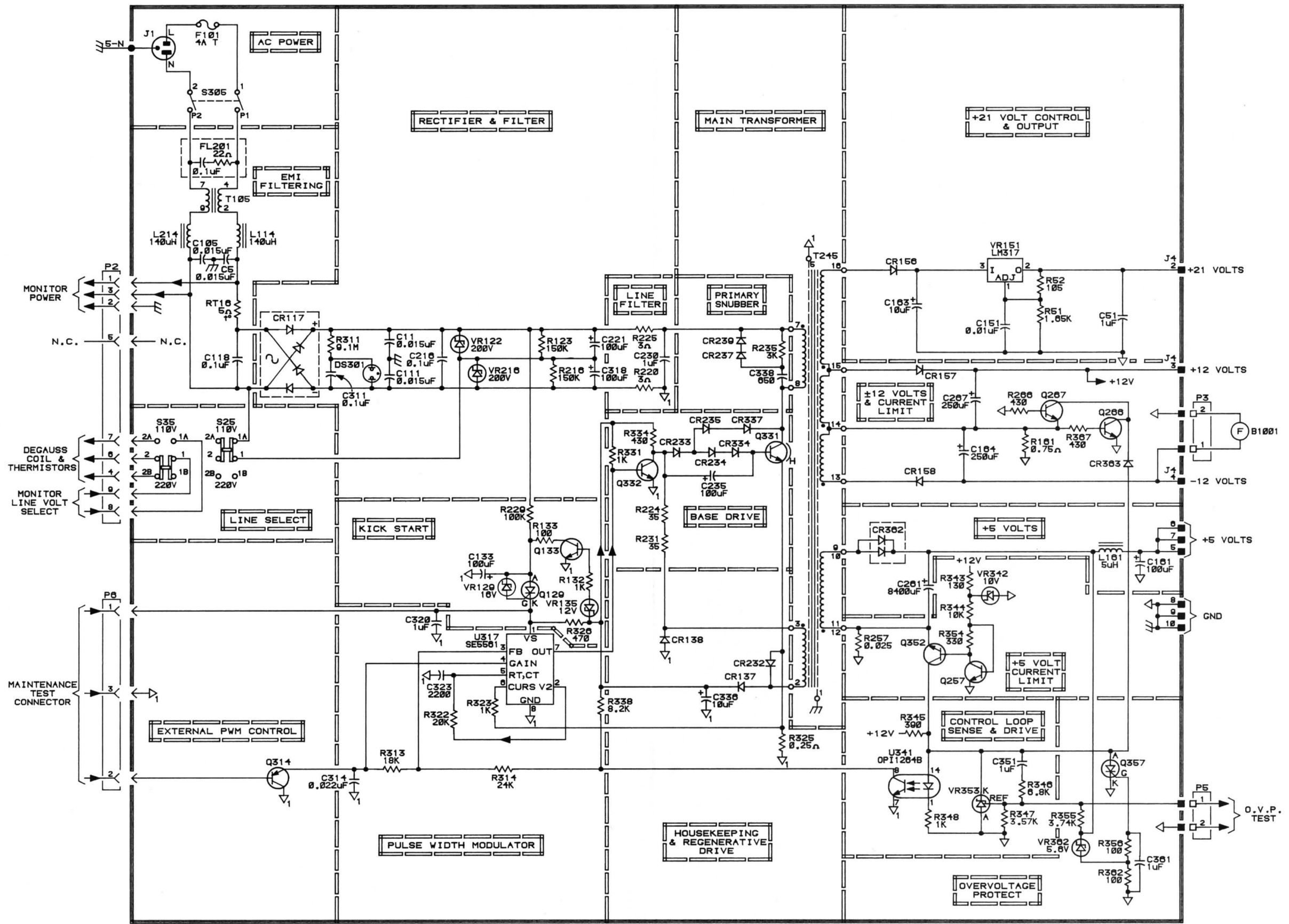
LOGIC POWER SUPPLY
COMPONENT LOCATIONS



Logic Power Supply (620-0005-00) Component Locations.

4889-80

4107 SERVICE



INSTRUMENT:
620-0005-00
(FOR USE WITH 4107)

NOTES:

4889-S21

BOARD: 670-8318-00
LOGIC POWER SUPPLY BOARD

ASSEMBLY-SHEET:
A5-1
(1 OF 1)

LOGIC POWER SUPPLY
620-0005-00
A5A1-1

Section 12

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```

1 2 3 4 5           Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
    --- * ---
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
    --- * ---
Parts of Detail Part
Attaching parts for Parts of Detail Part
    --- * ---
  
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol --- * --- indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

..	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OB	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

REPLACEABLE MECHANICAL PARTS

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
000FF	LEWIS SCREW	4114 SOUTH PEORIA AVE.	CHICAGO, IL 60609
000HQ	MC GUIRE BEARING CO.	947 S.E. MARKET	PORTLAND, OR 97214
000JA	J. PHILLIP INDUSTRIES INC.	5713 NORTHWEST HIGHWAY	CHICAGO, ILL 60646
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01536	CAMCAR DIV OF TEXTRON INC. SEMS PRODUCTS UNIT	1818 CHRISTINA ST.	ROCKFORD, IL 61108
02768	ILLINOIS TOOL WORKS, INC., FASTEX DIV.	195 ALGONQUIN ROAD	DES PLAINES, IL 60016
04919	COMPONENT MANUFACTURING SERVICE, INC.	1 COMPONENT PARK WEST	BRIDGEWATER, MA 02379
06915	RICHCO PLASTIC CO.	5825 N. TRIPP AVE.	CHICAGO, IL 60646
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
13103	THERMALLOY COMPANY, INC.	2021 W VALLEY VIEW LANE P O BOX 34829	DALLAS, TX 75234
19613	TEXTTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
19738	AUDEL CORP.	50 LACKAWANNA AVE.	PARSIPPANY, NJ 07054
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
30817	INSTRUMENT SPECIALTIES COMPANY, INC.	BROAD ST., BOX A	DELAWARE WATER GAP, PA 18327
46384	PENN ENGINEERING AND MFG. CORP.	P O BOX 311	DOYLESTOWN, PA 18901
52152	MINNESOTA MINING AND MFG CO.	INDUSTRIAL SPECIALTIES DIV. 3M CENTER	ST. PAUL, MN 55144
52833	KEYTRONIC CORP., OCR DIV.	SPOKANE INDUSTRIAL PK., P. O. BOX 14687	SPOKANE, WA 99214
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD P O BOX 500	ELGIN, IL 60120
80009	TEKTRONIX, INC.	2530 CRESCENT DR.	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	701 SONORA AVENUE	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	P.O. BOX 6626	GLENDALE, CA 91201
S3109	C/O PANEL COMPONENTS CORP.	5713 NORTHWEST HIGHWAY	SANTA ROSA, CA 95406
T1105	J PHILLIP INDUSTRIES INC	312 E. MAIN ST.	CHICAGO, IL 60646
T1372	ELECTRI-CORD MFG CO INC		WESTFIELD, PA 16950

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1 2 3 4 5	Name & Description	Mfr	
		Eff	Dscont				Code	Mfr Part Number
1-1	200-2841-02			1		COVER,TERMINAL:TOP *****ATTACHING PARTS)*****		
-2	212-0115-00			2		SCREW ASSY,WASHER:8-3 X 0.75,PNH,STL	000FF	OBD
-3	354-0411-00			2		PACKING,PREFMD:0.125 ID X 0.062 XSECT *****END ATTACHING PARTS)*****	000HQ	8006-366Y
-4	200-2864-00			1		COVER CIRCUIT BD:		
-5	131-0132-00			AR		CONTACT,ELEC:FINGER STRIP	30817	97-135-X-3.75 IN
-6	366-1833-00			1		KNOB:GRAY,0.25 ID X 0.392 X 0.39	80009	366-1833-00
-7	366-0534-00			1		PUSHBUTTON:BLK/BLK/GRN,0.335 SQ X 0.39		
-8	334-5153-00			1		PLATE,IDENT:MKD POWER ON/OFF,BRIGHTNESS		
-9	334-5262-00			1		MARKER,IDENT:MKD 4107	80009	334-5152-00
-10	333-3040-02			1		FRONT PANEL: *****ATTACHING PARTS)*****	80009	333-3040-00
-11	212-0115-00			2		SCREW ASSY,WASHER:8-32 X 0.75,PNH,STL *****END ATTACHING PARTS)*****	000FF	OBD
-12	331-0567-00			1		MASK,CRT:	80009	331-0567-00
-13	384-1665-00			1		EXTENSION SHAFT:14.16L,PLASTIC	80009	384-1665-00
-14	377-0570-00			1		INSERT KNOB:0.055 ID X 1.32L,NYLON,0.456 O	80009	377-0570-00
-15	----			1		MONITOR ASSY:4107(SEE 4107 DISPLAY SERVICE *****ATTACHING PARTS)*****		
-16	212-0114-00			6		SCREW ASSY,WASHER:8-32 X 0.375,PNH,STL *****END ATTACHING PARTS)*****	000FF	OBD
-17	337-3176-00			1		SHIELD ELEC:MONITOR EMI *****ATTACHING PARTS)*****		
-18	213-0144-00			2		SCREW,TPG,TF:8-18 X 0.5 INCH,TRH,STL *****END ATTACHING PARTS)*****	83385	ORD BY DESCR
-19	----			1		POWER SUPPLY ASSY:(SEE A5 REPL) *****ATTACHING PARTS)*****		
-20	212-0114-00			6		SCREW ASSY,WASHER:8-32 X 0.375,PNH,STL *****END ATTACHING PARTS)*****	000FF	OBD
-21	380-0707-00			1		POWER SUPPLY INCLUDES .HOUSING HALF CKT BD:TOP	80009	380-0707-00
-22	213-0931-00			1		.SCREW,TPG TF:6-20X0.312,TYPE B,PNH,STL		
-23	348-0141-00			1		.GROMMET,PLASTIC:U-SHP,0.625 X 0.658 INCH	80009	348-0141-00
-24	343-0775-00			1		.CLIP,SPR TNSN:	52152	3484-1000
-25	----			1		.CKT BOARD ASSY:PWR SUPPLY (NOT REPLACEABL *****ATTACHING PARTS)*****		
-26	211-0121-00			1		.SCR,ASSEM WSHR:4-40 X 0.438 INCH,PNH BRS *****END ATTACHING PARTS)*****	83385	ORD BY DESCR
-27	214-1815-00			2		.HEAT SINK,XSTR:TO-220 ALUMINIUM	13103	6034B-TT
-28	----			1		.DIODE:(SEE A5CR362 REPL) *****ATTACHING PARTS)*****		
-29	211-0008-00			2		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-30	210-0586-00			2		.NUT,PL,ASSEM WA:4-40 X 0.25,STL *****END ATTACHING PARTS)*****	83385	ORD BY DESCR
-31	----			1		.CONN,RCPT,ELEC:(SEE A5J1 REPL) *****ATTACHING PARTS)*****		
-32	210-3100-00			3		.RIVET,SOLID:0.26L X 0.136 OD,RND,PLSTC *****END ATTACHING PARTS)*****	02768	201-090751-00
-33	----			1		.SWITCH:(SEE A5S305 REPL) *****ATTACHING PARTS)*****		
-34	211-0008-00			2		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-35	210-0406-00			2		.NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS *****END ATTACHING PARTS)*****	73743	12161-50
-36	344-0326-00			2		.CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-37	361-0067-00			4		.SPACER,CKT BD:0.187,NYLON	06915	LCBS-3M
-38	334-3379-01			1		.MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-01
-39	334-5212-00			1		.MARKER,IDENT:MARKED CAUTION	80009	334-5212-00
-40	----			1		.FAN:(SEE A5B1001 REPL) *****ATTACHING PARTS)*****		
-41	213-0932-00			2		.SCREW,TPG,TF:12-16X0.375L,SEMS,PNH,STL *****END ATTACHING PARTS)*****	01536	OBD

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	----		-		.FAN INCLUDES:		
-42	352-0169-00		1		..HLDR,TERM CONN:2 WIRE BLACK	80009	352-0169-00
-43	131-0707-00		2		..CONNECTOR,TERM:22-26 AWG,BRS & CU BE GOL	22526	47439
-44	251-3076-00		1		.WIRE,FABRIC:14 X 14 MESH,SST		
-45	361-1281-00		1		.SPACER,FAN:0.062 X 3.988 X 3.613 PLSTC		
-46	131-1688-00		1		.TERM, QIK DISC:MALE,0.032 X 0.25 BL,45 DEG	00779	42577-4
					***** (ATTACHING PARTS) *****		
-47	210-0407-00		1		.NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
					***** (END ATTACHING PARTS) *****		
-48	214-3472-00		1		.DAMPER,SHIMMY:CAPACITOR,BLK VINYL/NITRILE		
-49	380-0706-01		1		.HOUSING,HALF:CKT BD BOTTOM	80009	380-0706-01
-50	195-1040-00		1		.LEAD,ELECTRICAL:18 AWG,4.0 L,5-4	80009	195-1040-00
-51	210-0202-00		1		..TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-52	----		1		CKT BOARD ASSY:DISPLAY CONT(SEE A2 REPL)		
-53	386-5031-00		1		.STIFFENER,CKT BD:9.1 L,ALUMINUM	80009	386-5031-00
					***** (ATTACHING PARTS) *****		
-54	210-3099-00		1		.RIVET SOLID:0.187 L X 0.116 OD, DOME HD,AL	19738	75021-0406
					***** (END ATTACHING PARTS) *****		
-55	136-0755-00		1		.SKT,PL-IN ELEC:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-55	195-0147-00		1		.LEAD,ELECTRICAL:18 AWG,3.75 L W/GROUNDING		
-56	----		2		.CONNECTOR ELEC:(SEE REPL A2P35,39)		
					***** (ATTACHING PARTS) *****		
-57	210-3102-00		4		.RIVET,SOLID:0.25 L X 0.156,ALUMINUM	19738	1131-0308
					***** (END ATTACHING PARTS) *****		
-58	----		1		CKT BOARD ASSY:TERMINAL CONT(SEE A1 REPL)		
-59	136-0797-00		8		.SKT PLUG-IN,ELEC:MICROCKT,28 CONTACT	27264	15-29-2285
-60	136-0813-00		1		.SKT,PL-IN ELEC:CHIP CARRIER,68 CONTACTS	19613	268-5400-00-1102
-61	129-1017-00		4		.SPACER,POST:0.219 L,4-40 INT THD ONE END	46384	KFB3-440-7ET
-62	----		2		.CONN,RCPT,ELEC:(SEE A1J13,J28 REPL)		
					***** (ATTACHING PARTS) *****		
-63	211-0340-00		4		.SCREW,MACHINE:2-56 X 0.375 ROUND NYLON		
-64	210-0405-00		4		.NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	12157-50
					***** (END ATTACHING PARTS) *****		
-65	----		1		CKT BD ASSY:RAM 3 (SEE A3 REPL)		
-66	----		2		CONNECTOR ELEC:(SEE REPL A3J49,P48)		
					***** (ATTACHING PARTS) *****		
-67	211-0340-00		4		.SCREW,MACHINE:2-56 X 0.375 ROUND NYLON		
-68	210-0405-00		4		.NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	12157-50
					***** (END ATTACHING PARTS) *****		
-69	366-1559-01		2		.PUSH BUTTON:GRAY,0.43 L X 0.18 W X 0.18	80009	366-1559-01
-70	386-5104-00		1		PLATE CONNECTOR MTG:ALUMINUM		
					***** (ATTACHING PARTS) *****		
-71	131-0890-01		2		LOCK,CONNECTOR:4-40 X 0.312L,HEX HD,STL	71468	D20418-2
-72	210-0054-00		2		WASHER,LOCK:SPLIT,0.118 ID X 0.212"OD S	83385	ORD BY DESCR
-73	211-0008-00		2		SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
					***** (END ATTACHING PARTS) *****		
-74	131-1369-00		1		TERM,QUICK DISC:0.615 L X 0.25 W/BLADE	00779	42506-2
					***** (ATTACHING PARTS) *****		
-75	210-0406-00		1		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
					***** (END ATTACHING PARTS) *****		
-76	196-2280-00		1		LEAD,ELECTRICAL:12 AWG,6.967 L		
-77	348-0513-00		2		FOOT,CABINET:POLYURETHANE,BLACK	80009	348-0513-00
-78	200-2842-02		1		COVER,TERMINAL BTM:		

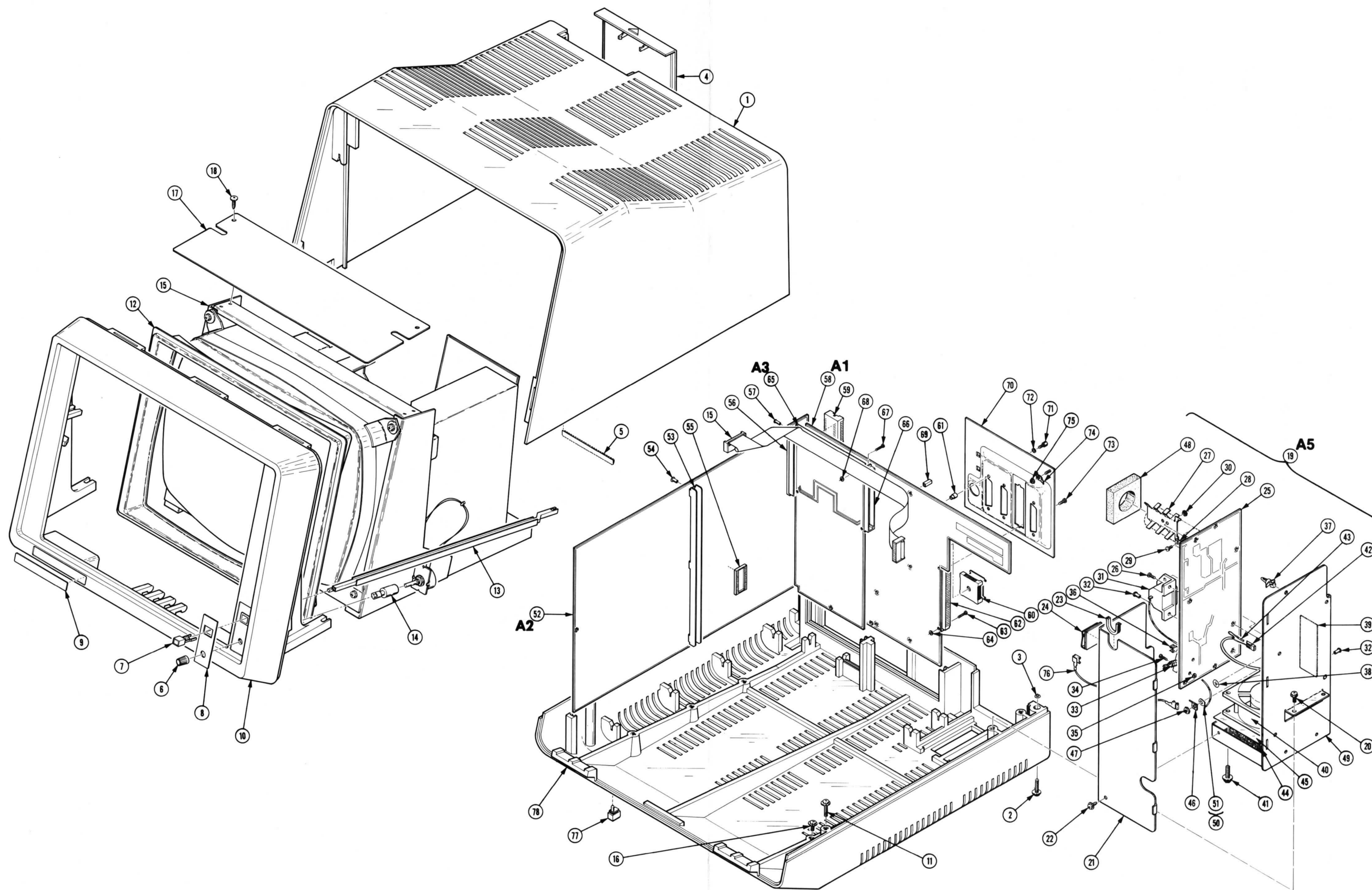
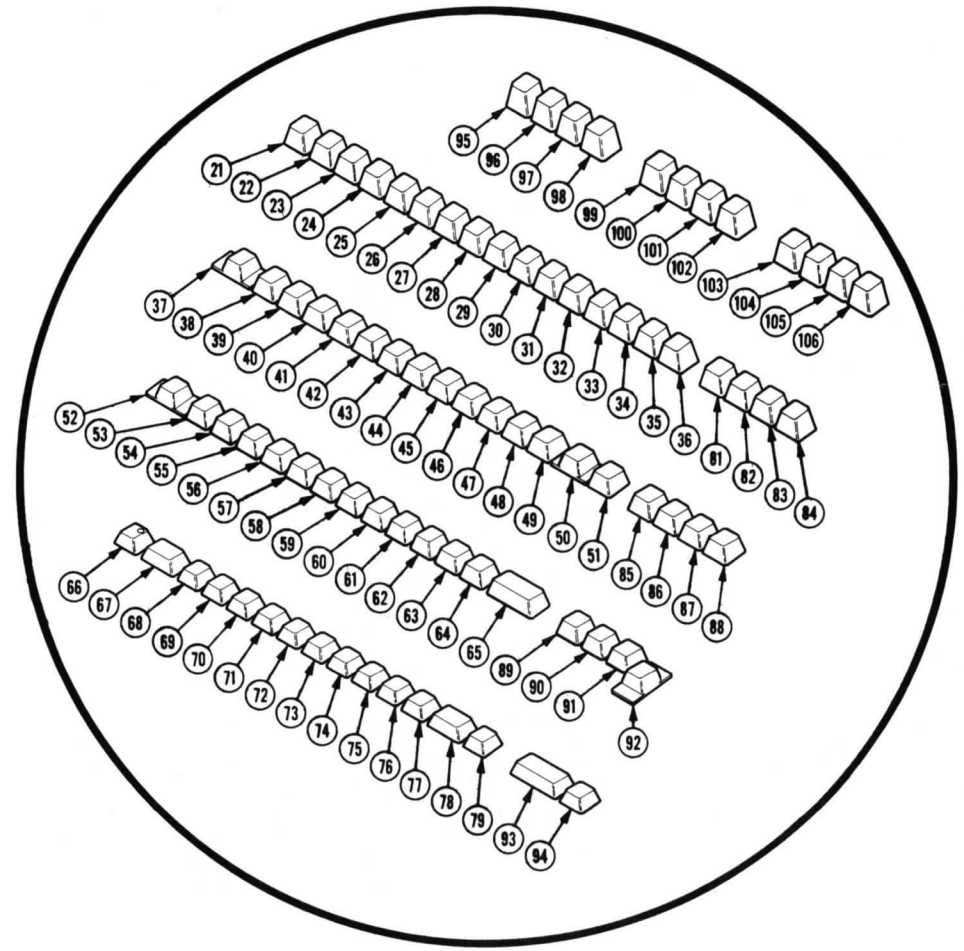
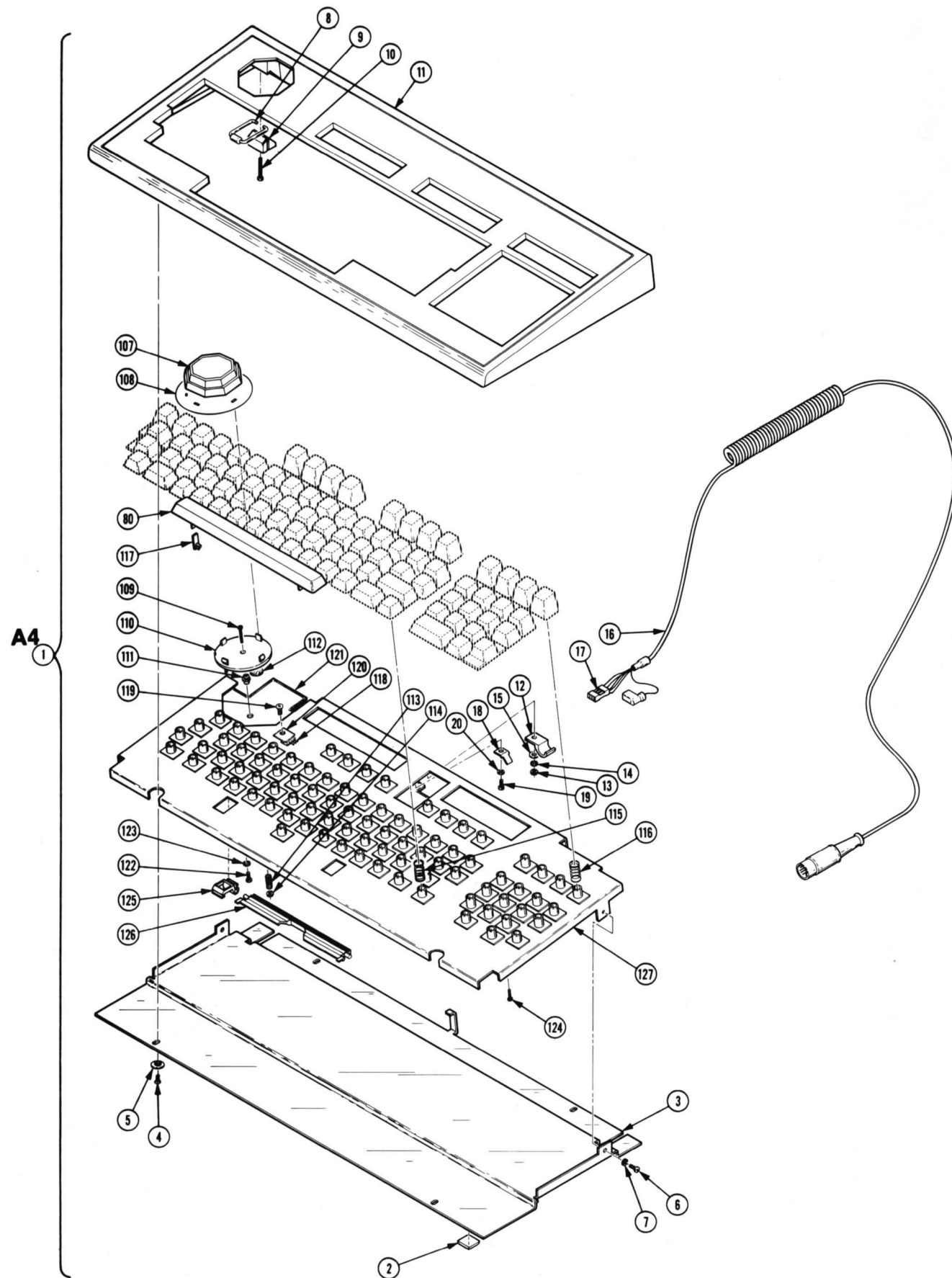


FIG. 2 KEYBOARD



REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont									
2-1	----			1						KEYBOARD ASSY:(SEE A4 REPL)		
-2	118-3014-00			4						.FOOT,RUBBER:	52833	48-00559-000
-3	118-3013-00			1						.PLATE,BASE: ***** (ATTACHING PARTS)*****	52833	49-01307-000
-4	211-0101-00			4						.SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	ORD BY DESCR
-5	118-3190-00			4						.WASHER:SHOULDER		
-6	211-0008-00			2						.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-7	210-0004-00			2						.WASHER,LOCK:#4 INTL,0.015 THK,STL CD PL ***** (END ATTACHING PARTS)*****	000BK	ORD BY DESCR
-8	118-3020-00			2						.LEG:	52833	45-00057-000
-9	118-3021-00			2						.BLOCK,BAIL: ***** (ATTACHING PARTS)*****	52833	44-00193-000
-10	118-3022-00			2						.SCREW: ***** (END ATTACHING PARTS)*****	52833	47-00290-000
-11	118-3023-00			1						.HOUSING,KEYBOARD:	52833	44-00205-000
-12	118-3006-00			1						.STRAP,TIEDOWN: ***** (ATTACHING PARTS)*****	52833	48-00646-000
-13	210-0551-00			1						.NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	ORD BY DESCR
-14	210-0004-00			1						.WASHER,LOCK:#4 INTL,0.015 THK,STL CD PL	000BK	ORD BY DESCR
-15	210-0994-00			1						.WASHER,FLAT:0.125 ID X 0.25" OD,STL ***** (END ATTACHING PARTS)*****	86928	5702-201-20
-16	118-3026-00			1						.CABLE ASSY,SP ELEC:	52833	48-00626-000
-17	118-3025-00			1						.CONN,PLUG,ELEC:	52833	48-00501-000
-18	118-3032-00			1						.STANDOFF: ***** (ATTACHING PARTS)*****	52833	47-00351-032
-19	211-0008-00			1						.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-20	210-0004-00			1						.WASHER,LOCK:#4 INTL,0.015 THK,STL CD PL ***** (END ATTACHING PARTS)*****	000BK	ORD BY DESCR
-21	118-3173-00			1						.PUSHBUTTON:DERAS/SERAS	52833	
	----			-						(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY)		
	118-3291-00			1						.PUSHBUTTON:DL DIRSOO/BL DIRSO (OPTION 4G ONLY)		
-22	118-3245-00			1						.PUSHBUTTON:LBR/LBRKT	52833	
	----			-						(STANDARD AND OPTION 4A ONLY)		
	118-3143-00			1						.PUSHBUTTON:*/DLR (OPTION 4B ONLY)	52833	
	----			-						(OPTION 4B ONLY)		
	118-3260-00			1						.PUSHBUTTON:CARET/OVERLINE	52833	
	----			-						(OPTIONS 4C, 4F ONLY)		
	118-3285-00			1						.PUSHBUTTON:CARET/# (OPTION 4G ONLY)		
	----			-						(OPTION 4G ONLY)		
	118-3392-00			1						.PUSHBUTTON:LEFT BRACKET/LEFT BRACE (OPTION 4K ONLY)		
	----			-						(OPTION 4K ONLY)		
-23	118-3249-00			1						.PUSHBUTTON:EP/1	52833	
	----			-						(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3133-00			1						.PUSHBUTTON:1/& (OPTION 4B ONLY)	52833	
	----			-						(OPTION 4B ONLY)		
	118-3396-00			1						.PUSHBUTTON:1/— (OPTION 4K ONLY)		
	----			-						(OPTION 4K ONLY)		
-24	118-3254-00			1						.PUSHBUTTON:@/2	52833	
	----			-						(STANDARD AND OPTION 4A ONLY)		
	118-3152-00			1						.PUSHBUTTON:2/ACUT ACNT E (OPTION 4B ONLY)	52833	
	----			-						(OPTION 4B ONLY)		
	118-3256-00			1						.PUSHBUTTON:QUOTES/2 (OPTIONS 4C, 4F, 4G ONLY)	52833	
	----			-						(OPTIONS 4C, 4F, 4G ONLY)		
	118-3402-00			1						.PUSHBUTTON:2/@ (OPTION 4K ONLY)		
	----			-						(OPTION 4K ONLY)		
-25	118-3250-00			1						.PUSHBUTTON:#/3	52833	
	----			-						(STANDARD AND OPTIONS 4C, 4F ONLY)		
	118-3144-00			1						.PUSHBUTTON:3/VER QUOTES (OPTION 4B ONLY)	52833	
	----			-						(OPTION 4B ONLY)		
	366-0536-00			1						.PUSHBUTTON:MOKE TAN,POUNDS OVER 3 UK (OPTION 4A ONLY)		
	----			-						(OPTION 4A ONLY)		
	118-3286-00			1						.PUSHBUTTON:SECTION/3 (OPTION 4G ONLY)		
	----			-						(OPTION 4G ONLY)		
	118-3393-00			1						.PUSHBUTTON:3/# (OPTION 4K ONLY)		
	----			-						(OPTION 4K ONLY)		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont									
2-26	118-3251-00			1						.PUSHBUTTON:DLR/4	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3141-00			1						.PUSHBUTTON:4/FWD SLASH	52833	
-27	118-3394-00			1						.(OPTION 4B ONLY)		
	-----			-						.PUSHBUTTON:4/DLR		
	-----			-						.(OPTION 4K ONLY)		
-27	118-3252-00			1						.PUSHBUTTON:%/5	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3145-00			1						.PUSHBUTTON:5/(52833	
-28	118-3395-00			1						.(OPTION 4B ONLY)		
	-----			-						.PUSHBUTTON:5/%		
	-----			-						.(OPTION 4K ONLY)		
-28	118-3248-00			1						.PUSHBUTTON:CARET/6	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3257-00			1						.PUSHBUTTON:&/6	52833	
-29	118-3136-00			1						.(OPTIONS 4C, 4F, 4G ONLY)		
	-----			-						.PUSHBUTTON:6/SECTION	52833	
	-----			-						.(OPTION 4B ONLY)		
-29	118-3401-00			1						.PUSHBUTTON:6/CAROT		
	-----			-						.(OPTION 4K ONLY)		
	118-3188-00			1						.PUSHBUTTON:&/7	52833	
-29	118-3135-00			1						.(STANDARD AND OPTION 4A ONLY)		
	-----			-						.PUSHBUTTON:7/GRV APOST E	52833	
	-----			-						.(OPTION 4B ONLY)		
-30	118-3255-00			1						.PUSHBUTTON:;/7	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
	118-3400-00			1						.PUSHBUTTON:7/&		
-30	118-3253-00			1						.(OPTION 4K ONLY)		
	-----			-						.PUSHBUTTON:ASTERISK/8	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
-30	118-3146-00			1						.PUSHBUTTON:8/EP	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3258-00			1						.PUSHBUTTON:;/8	52833	
-30	118-3399-00			1						.(OPTIONS 4C, 4F, 4G ONLY)		
	-----			-						.PUSHBUTTON:8/*		
	-----			-						.(OPTION 4K ONLY)		
-31	118-3183-00			1						.PUSHBUTTON:;/9	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3142-00			1						.PUSHBUTTON:9/CEDILLIA	52833	
-31	118-3259-00			1						.(OPTION 4B ONLY)		
	-----			-						.PUSHBUTTON:)/9	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
-32	118-3398-00			1						.PUSHBUTTON:9/(
	-----			-						.(OPTION 4K ONLY)		
	118-3184-00			1						.PUSHBUTTON:)/PHASE	52833	
-32	118-3572-00			1						.(STANDARD AND OPTION 4A ONLY)		
	-----			-						.PUSHBUTTON:Q/GRV ACNT		
	-----			-						.(OPTION 4B ONLY)		
-32	118-3265-00			1						.PUSHBUTTON:=/BULLSEYE	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
	118-3403-00			1						.PUSHBUTTON:0/)		
-33	118-3185-00			1						.(OPTION 4K ONLY)		
	-----			-						.PUSHBUTTON:HORIZONTAL/HYPHEN		
	-----			-						.(STANDARD AND OPTIONS 4A)		
-33	118-3134-00			1						.PUSHBUTTON:DEGREE/)	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3263-00			1						.PUSHBUTTON:~/+	52833	
-33	118-3288-00			1						.(OPTIONS 4C, 4F ONLY)		
	-----			-						.PUSHBUTTON:~/SHARPS		
	-----			-						.(OPTION 4G ONLY)		
-33	118-3405-00			1						.PUSHBUTTON:-/UNDERScore		
	-----			-						.(OPTION 4K ONLY)		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont					
2-34	118-3247-00			1		.PUSHBUTTON: +/=	52833	
	-----			-		.(STANDARD AND OPTION 4A ONLY)		
	118-3185-00			1		.PUSHBUTTON:HORIZONTAL/HYPHEN		
	-----			-		.(OPTION 4B ONLY)		
	118-3266-00			1		.PUSHBUTTON:GRV ACNT/ACUT ACNT		52833
-----			-		.(OPTIONS 4C, 4F, 4G ONLY)			
118-3284-00			1		.PUSHBUTTON:GRV A POST/ACUT A POST			
-----			-		.(OPTION 4G ONLY)			
118-3404-00			1		.PUSHBUTTON: +/=			
-35	-----			-		.(OPTION 4K ONLY)		
	118-3246-00			1		.PUSHBUTTON:RBR/RBRKT	52833	
	-----			-		.(STANDARD AND OPTION 4A ONLY)		
	118-3573-00			1		.PUSHBUTTON:MILRON/ENGLISH POUND)		
	-----			-		.(OPTION 4B ONLY)		
	118-3264-00			1		.PUSHBUTTON:LESS THAN/GREATER THAN	52833	
	-----			-		.(OPTION 4C ONLY)		
	118-3149-00			1		.PUSHBUTTON:LESS THAN/GREATER THAN	52833	
	-----			-		.(OPTION 4F ONLY)		
	118-3283-00			1		.PUSHBUTTON:*/+		
-----			-		.(OPTION 4G ONLY)			
118-3397-00			1		.PUSHBUTTON:RIGHT BRACKET/RIGHT BRACE			
-----			-		.(OPTION 4K ONLY)			
-36	118-3172-00			1		.PUSHBUTTON:RUB OUT	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3574-00			1		.PUSHBUTTON:RUB OUT/BACK SPACE)		
-----			-		.(OPTIONS 4B, 4G ONLY)			
-37	118-3182-00			1		.PUSHBUTTON:ESC		
	-----			-		.(STANDARD & OPTIONS 4A, 4C, 4F, 4G)		
118-3179-00			1		.PUSHBUTTON:TAB			
-----			-		.(OPTION 4B)			
-38	118-3228-00			1		.PUSHBUTTON:TILDE/VERT LINE	52833	
	-----			-		.(STANDARD AND OPTION 4A ONLY)		
	118-3149-00			1		.PUSHBUTTON:LESS THAN/GREATER THAN	52833	
	-----			-		.(OPTION 4B, 4G ONLY)		
	118-3262-00			1		.PUSHBUTTON:ASTERISK/@		52833
-----			-		.(OPTIONS 4C, 4F ONLY)			
118-3390-00			1		.PUSHBUTTON:VERT BAR			
-----			-		.(OPTION 4K ONLY)			
-39	118-3234-00			1		.PUSHBUTTON:Q	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3151-00			1		.PUSHBUTTON:A	52833	
	-----			-		.(OPTION 4B ONLY)		
118-3384-00			1		.PUSHBUTTON:Q			
-----			-		.(OPTION 4K ONLY)			
-40	118-3238-00			1		.PUSHBUTTON:W	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3191-00			1		.PUSHBUTTON:Z	52833	
	-----			-		.(OPTION 4B ONLY)		
118-3388-00			1		.PUSHBUTTON:W			
-----			-		.(OPTION 4K ONLY)			
-41	118-3230-00			1		.PUSHBUTTON:E	52833	
	118-3382-00			1		.PUSHBUTTON:E		
-----			-		.(OPTION 4K ONLY)			
-42	118-3235-00			1		.PUSHBUTTON:R	52833	
	118-3385-00			1		.PUSHBUTTON:R		
-----			-		.(OPTION 4K ONLY)			
-43	118-3236-00			1		.PUSHBUTTON:T	52833	
	118-3386-00			1		.PUSHBUTTON:T		
-----			-		.(OPTION 4K ONLY)			
-44	118-3239-00			1		.PUSHBUTTON:Y	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY)		
	118-3209-00			1		.PUSHBUTTON:Z		
	-----			-		.(OPTION 4G ONLY)		
118-3389-00			1		.PUSHBUTTON:Y			
-----			-		.(OPTION 4K ONLY)			

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty						Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont		1	2	3	4	5			
2-45	118-3237-00			1						.PUSHBUTTON:U	52833	
	118-3387-00			1						.PUSHBUTTON:U		
	-----			-						.(OPTION 4K ONLY)		
-46	118-3231-00			1						.PUSHBUTTON:I	52833	
	118-3383-00			1						.PUSHBUTTON:I		
	-----			-						.(OPTION 4K ONLY)		
-47	118-3232-00			1						.PUSHBUTTON:O	52833	
	118-3380-00			1						.PUSHBUTTON:O		
	-----			-						.(OPTION 4K ONLY)		
-48	118-3233-00			1						.PUSHBUTTON:P	52833	
	118-3381-00			1						.PUSHBUTTON:P		
	-----			1						.(OPTION 4K ONLY)		
-49	118-3229-00			1						.PUSHBUTTON:GRAVE ACCENT/BKWD SLASH	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3150-00			1						.PUSHBUTTON:DIRS/CARET	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3261-00			1						.PUSHBUTTON:DEGREE/A	52833	
	-----			-						.(OPTIONS 4C, 4F ONLY)		
	118-3282-00			1						.PUSHBUTTON:DIRESIS/U		
	-----			-						.(OPTION 4G)		
	118-3391-00			1						.PUSHBUTTON:/'		
	-----			-						.(OPTION 4K ONLY)		
-50	118-3171-00			1						.PUSHBUTTON:BACK SPACE	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3182-00			1						.PUSHBUTTON:ESC		
	-----			-						.(OPTION 4B)		
	118-3140-00			1						.PUSHBUTTON:LEFT ARROW		
	-----			-						.(OPTION 4G ONLY)		
-51	118-3181-00			1						.PUSHBUTTON:LINE FEED	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3140-00			1						.PUSHBUTTON:LEFT ARROW		
	-----			-						.(OPTION 4B ONLY)		
	118-3290-00			1						.PUSHBUTTON:DOWN ARROW		
	-----			-						.(OPTION 4G ONLY)		
-52	118-3179-00			1						.PUSHBUTTON:TAB	52833	
	-----			-						.(STANDARD & OPTIONS 4A,4C,4F,4G)		
	118-3138-00			1						.PUSHBUTTON:DWN OPEN FAT ARROW		
	-----			-						.(OPTION 4B ONLY)		
-53	118-3178-00			1						.PUSHBUTTON:CTRL	52833	
-54	118-3215-00			1						.PUSHBUTTON:A	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F,4G ONLY)		
	118-3148-00			1						.PUSHBUTTON:Q	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3363-00			1						.PUSHBUTTON:A		
	-----			-						.(OPTION 4K ONLY)		
-55	118-3223-00			1						.PUSHBUTTON:S	52833	
	118-3377-00			1						.PUSHBUTTON:S		
	-----			-						.(OPTION 4K ONLY)		
-56	118-3216-00			1						.PUSHBUTTON:D	52833	
	118-3373-00			1						.PUSHBUTTON:D		
	-----			-						.(OPTION 4K ONLY)		
-57	118-3217-00			1						.PUSHBUTTON:F	52833	
	118-3370-00			1						.PUSHBUTTON:F		
	-----			-						.(OPTION 4K ONLY)		
-58	118-3218-00			1						.PUSHBUTTON:G	52833	
	118-3374-00			1						.PUSHBUTTON:G		
	-----			-						.(OPTION 4K ONLY)		
-59	118-3219-00			1						.PUSHBUTTON:H	52833	
	118-3375-00			1						.PUSHBUTTON:H		
	-----			-						.(OPTION 4K ONLY)		
-60	118-3220-00			1						.PUSHBUTTON:J	52833	
	118-3371-00			1						.PUSHBUTTON:J		
	-----			-						.(OPTION 4K ONLY)		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1 2 3 4 5					Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont									
2-61	118-3221-00			1						.PUSHBUTTON:K	52833	
	118-3376-00			1						.PUSHBUTTON:K		
	-----			-						.(OPTION 4K ONLY)		
-62	118-3222-00			1						.PUSHBUTTON:L	52833	
	118-3372-00			1						.PUSHBUTTON:L		
	-----			-						.(OPTION 4K ONLY)		
-63	118-3214-00			1						.PUSHBUTTON::/;	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3147-00			1						.PUSHBUTTON:M	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3271-00			1						.PUSHBUTTON:DIRESIS O	52833	
	-----			-						.(OPTION 4C, 4G ONLY)		
	366-0537-00			1						.PUSH BUTTON:SMOKE TAN,NULL		
	-----			-						.(OPTION 4F ONLY)		
	118-3379-00			1						.PUSHBUTTON::/:		
	-----			-						.(OPTION 4K ONLY)		
-64	118-3224-00			1						.PUSHBUTTON:QUOTES/ACUTE ACNT	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3158-00			1						.PUSHBUTTON:%/GRV ACNT U	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3272-00			1						.PUSHBUTTON:DIRESIS A	52833	
	-----			-						.(OPTION 4C, 4G ONLY)		
	366-0538-00			1						.PUSH BUTTON:SMOKE TAN,AE RUN TOGETHER		
	-----			-						.(OPTION 4F ONLY)		
	118-3378-00			1						.PUSHBUTTON:/'		
	-----			-						.(OPTION 4K ONLY)		
-65	118-3180-00			1						.PUSHBUTTON:RETURN	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3139-00			1						.PUSHBUTTON:RETURN ARROW	52833	
	-----			-						.(OPTION 4B, 4G ONLY)		
-66	118-3164-00			1						.PUSHBUTTON:CAPS/LOCK	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY)		
	118-3431-00			1						.PUSHBUTTON:SPERR		
	-----			-						.(OPTION 4G ONLY)		
	118-3571-00			1						.PUSHBUTTON:ENGLISH/KATAKANA		
	-----			-						.(OPTION 4K ONLY)		
-67	118-3177-00			1						.PUSHBUTTON:SHIFT	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3137-00			1						.PUSHBUTTON:MAJ/UNDRLN MIN	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3289-00			1						.PUSHBUTTON:UP OPEN FAT ARROW		
	-----			-						.(OPTION 4G ONLY)		
-68	118-3209-00			1						.PUSHBUTTON:Z	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3157-00			1						.PUSHBUTTON:W	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3430-00			1						.PUSHBUTTON:Y		
	-----			-						.(OPTION 4G ONLY)		
	118-3361-00			1						.PUSHBUTTON:Z		
	-----			-						.(OPTION 4K ONLY)		
-69	118-3208-00			1						.PUSHBUTTON:X	52833	
	118-3360-00			1						.PUSHBUTTON:X		
	-----			-						.(OPTION 4K ONLY)		
-70	118-3204-00			1						.PUSHBUTTON:C	52833	
	118-3368-00			1						.PUSHBUTTON:C		
	-----			-						.(OPTION 4K ONLY)		
-71	118-3207-00			1						.PUSHBUTTON:V	52833	
	118-3359-00			1						.PUSHBUTTON:V		
	-----			-						.(OPTION 4K ONLY)		
-72	118-3203-00			1						.PUSHBUTTON:B	52833	
	118-3367-00			1						.PUSHBUTTON:B		
	-----			-						.(OPTION 4K ONLY)		
-73	118-3206-00			1						.PUSHBUTTON:N	52833	
	118-3358-00			1						.PUSHBUTTON:N		
	-----			-						.(OPTION 4K ONLY)		

REPLACEABLE MECHANICAL PARTS

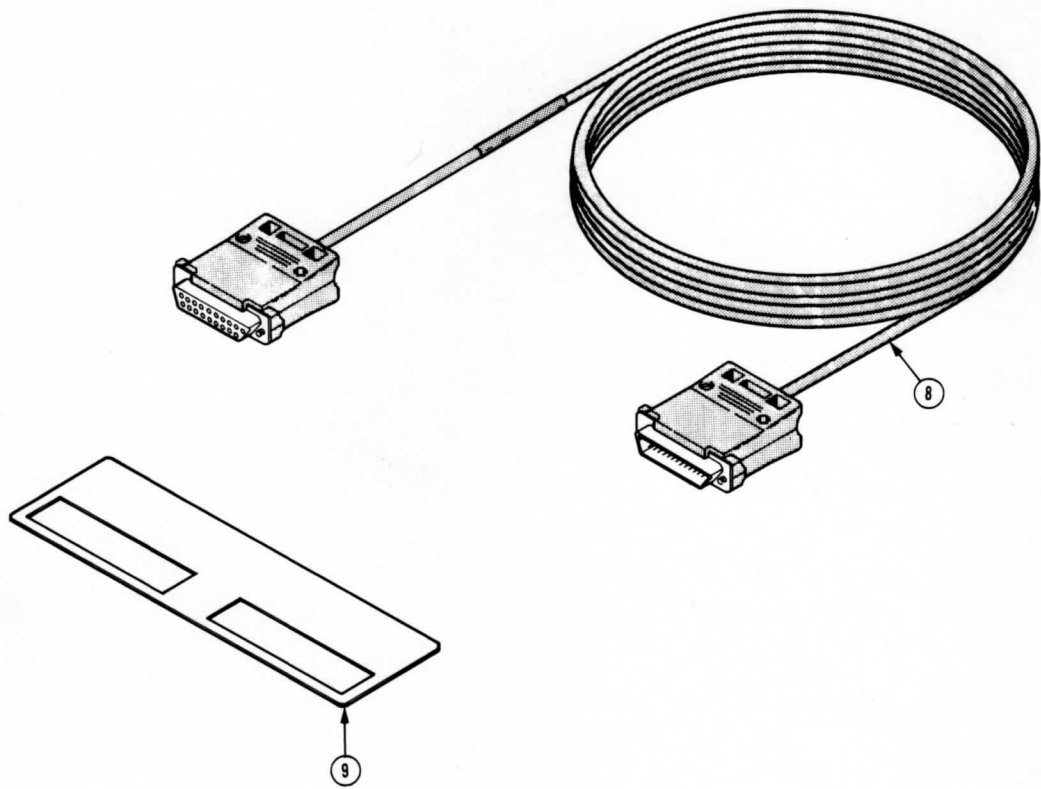
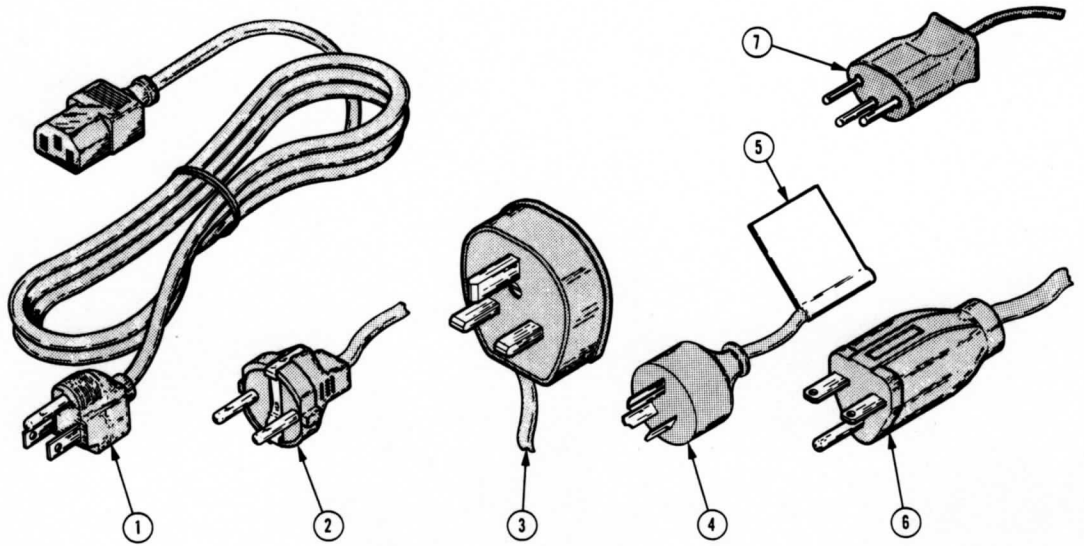
Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont									
2-74	118-3205-00			1						.PUSHBUTTON:M	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F, 4G ONLY)		
	118-3154-00			1						.PUSHBUTTON:?,	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3369-00			1						.PUSHBUTTON:M		
	-----			-						.(OPTION 4K ONLY)		
-75	118-3200-00			1						.PUSHBUTTON:LESS THAN/.	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3155-00			1						.PUSHBUTTON:PERIOD/;	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3268-00			1						.PUSHBUTTON:SEMICOLON/COMMA	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
	118-3362-00			1						.PUSHBUTTON:./</.		
	-----			-						.(OPTION 4K ONLY)		
-76	118-3201-00			1						.PUSHBUTTON:GREATER THAN/.	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3156-00			1						.PUSHBUTTON://:	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3267-00			1						.PUSHBUTTON:COLON/PERIOD	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
	118-3366-00			1						.PUSHBUTTON:./>		
	-----			-						.(OPTION 4K ONLY)		
-77	118-3202-00			1						.PUSHBUTTON:?!/	52833	
	-----			-						.(STANDARD AND OPTION 4A ONLY)		
	118-3153-00			1						.PUSHBUTTON:+/=	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3269-00			1						.PUSHBUTTON:HORIZONTAL/HYPHEN	52833	
	-----			-						.(OPTIONS 4C, 4F, 4G ONLY)		
	118-3365-00			1						.PUSHBUTTON://?/.		
	-----			-						.(OPTION 4K ONLY)		
-78	118-3177-00			1						.PUSHBUTTON:SHIFT	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4C, 4F ONLY)		
	118-3137-00			1						.PUSHBUTTON:MAJ/UNDRN MIN	52833	
	-----			-						.(OPTION 4B ONLY)		
	118-3289-00			1						.PUSHBUTTON:UP OPEN FAT ARROW		
	-----			-						.(OPTION 4G ONLY)		
-79	118-3187-00			1						.PUSHBUTTON:BREAK	52833	
-80	118-3186-00			1						.PUSHBUTTON:SPACE BAR	52833	
-81	118-3241-00			1						.PUSHBUTTON:7	52833	
-82	118-3242-00			1						.PUSHBUTTON:8	52833	
-83	118-3243-00			1						.PUSHBUTTON:9	52833	
-84	118-3244-00			1						.PUSHBUTTON:MINUS	52833	
-85	118-3225-00			1						.PUSHBUTTON:4	52833	
-86	118-3240-00			1						.PUSHBUTTON:5	52833	
-87	118-3226-00			1						.PUSHBUTTON:6	52833	
-88	118-3227-00			1						.PUSHBUTTON:COMMA	52833	
-89	118-3211-00			1						.PUSHBUTTON:1	52833	
-90	118-3212-00			1						.PUSHBUTTON:2	52833	
-91	118-3213-00			1						.PUSHBUTTON:3	52833	
-92	118-3161-00			1						.PUSHBUTTON:ENTER	52833	
-93	118-3210-00			1						.PUSHBUTTON:PHASE	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4B, 4G ONLY)		
	118-3270-00			1						.PUSHBUTTON:BULLSEYE	52833	
	-----			-						.(OPTIONS 4C, 4F ONLY)		
	118-3287-00			1						.PUSHBUTTON:=/PHASE		
	-----			-						.(OPTION 4G ONLY)		
-94	118-3199-00			1						.PUSHBUTTON:PERIOD	52833	
-95	118-3160-00			1						.PUSHBUTTON:GERAS DIALOG	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY)		
	118-3300-00			1						.PUSHBUTTON:GL DIRSO/DIA LOG		
	-----			-						.(OPTION 4G ONLY)		
-96	118-3174-00			1						.PUSHBUTTON:CANCEL/SETUP	52833	
	-----			-						.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY)		
	118-3299-00			1						.PUSHBUTTON:STOP/PARAM		
	-----			-						.(OPTION 4G ONLY)		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No.		Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
		Eff	Dscont					
2-97	118-3167-00			1		.PUSHBUTTON:DCOPY/SCOPY	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3298-00			1		.PUSHBUTTON:DKOP/BKOP		
	-----			-		.(OPTION 4G ONLY)		
-98	118-3163-00			1		.PUSHBUTTON:SET COLOR	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3295-00			1		.PUSHBUTTON:MENU		
	-----			-		.(OPTION 4G ONLY)		
	118-3621-00			1		.PUSHBUTTON:MENU CAP LOCK		
	-----			-		.(OPTION 4K ONLY)		
-99	118-3175-00			1		.PUSHBUTTON:F1/HUE	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3293-00			1		.PUSHBUTTON:F1/FWERT		
	-----			-		.(OPTION 4G ONLY)		
-100	118-3176-00			1		.PUSHBUTTON:F2/LIT	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3292-00			1		.PUSHBUTTON:F2/FHELL		
	-----			-		.(OPTION 4G ONLY)		
-101	118-3165-00			1		.PUSHBUTTON:F3/SAT	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3294-00			1		.PUSHBUTTON:F3/FS DIRS A TT		
	-----			-		.(OPTION 4G ONLY)		
-102	118-3166-00			1		.PUSHBUTTON:F4/RST	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3296-00			1		.PUSHBUTTON:F4/FORIG		
	-----			-		.(OPTION 4G ONLY)		
-103	118-3168-00			1		.PUSHBUTTON:F5/CMENU	52833	
	-----			-		.(STANDARD AND OPTIONS 4A, 4B, 4C, 4F ONLY		
	118-3297-00			1		.PUSHBUTTON:F5/FMEN DIRSU		
	-----			-		.(OPTION 4G ONLY)		
-104	118-3169-00			1		.PUSHBUTTON:F6	52833	
-105	118-3170-00			1		.PUSHBUTTON:F7	52833	
-106	118-3159-00			1		.PUSHBUTTON:F8	52833	
-107	118-3162-00			1		.PUSHBUTTON:JOY SWITCH CAP	52833	
	-----			-		.JOYSTICK:(SEE JS1)		
-108	118-3192-00			1		..SHIELD,DUST:JOY SWITCH	52833	
-109	118-3198-00			1		..SCREW:BINDER HEAD,0-80		
-110	118-3194-00			1		..CAP,DISC:JOY SWITCH	52833	
-111	118-3197-00			1		..PIVOT:BRASS,JOY SWITCH	52833	
-112	118-3193-00			4		..PAD,CARRIER:JOY SWITCH	52833	
-113	118-3195-00			1		..SPRING:JOY SWITCH	52833	
-114	118-3196-00			1		..RETAINER,SPRING:JOY SWITCH	52833	
-115	118-3017-00			1		.SPRING:	52833	45-00053-090
	-----			-		.(S59 ONLY)		
	118-3007-00			2		.SPRING:	52833	45-00053-030
	-----			-		.(S46 AND S60 ONLY)		
	118-3007-00			3		.SPRING:	52833	45-00053-030
	-----			-		..S46,60,78 OPTION 4K ONLY)		
-116	118-3016-00			83		.SPRING:		
	118-3016-00			82		.SPRING:		
	-----			-		.(OPTION 4K ONLY)		
-117	118-3009-00			2		.LEG:	52833	44-00174-000
-118	-----			1		.MICROCIRCUIT:(SEE A4A1 REPL)		
					(ATTACHING PARTS).....		
-119	118-3031-00			1		.SCREW:	52833	47-00402-001
-120	118-3030-00			1		.INSULATOR:	52833	48-00651-000
					(END ATTACHING PARTS).....		
-121	-----			1		.CIRCUIT BOARD (NOT REPLACEABLE SEE A4A1)		
					(ATTACHING PARTS).....		
-122	211-0008-00			2		.SCREW,MACHINE:4-40 X 0.250,PNH,STL,POZ	83385	ORD BY DESCR
-123	210-0004-00			2		.WASHER,LOCK:#4 INTL,0.015 THK,STL CD PL	000BK	ORD BY DESCR
-124	118-3015-00			13		.SCREW:	52833	47-0368-00
					(END ATTACHING PARTS).....		
-125	118-3010-00			2		.BRACKET,MTG:SPACER BAR	52833	44-00102-000
-126	118-3008-00			1		.SPACER,BAR:	52833	44-00173-000
-127	118-3028-00			1		.PLATE,MTG:	52833	49-01306-000

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1	2	3	4	5	Name & Description	Mfr Code	Mfr Part Number
STANDARD ACCESSORIES												
3-1	161-0066-00			1						CABLE ASSY,PWR.:3,18 AWG,115V,98.0 L	T1372	OBD
-2	161-0066-09			1						CABLE ASSY,PWR:3,0.75MM SQ,220V,96.0 L	S3109	OBD
	-----			-						(OPTION A1 EUROPEAN ONLY)		
-3	161-0066-10			1						CABLE ASSY,PWR:3,0.75MM SQ,240V,96.0 L	S3109	OBD
	-----			-						(OPTION A2 UNITED KINGDOM ONLY)		
-4	161-0066-11			1						CABLE ASSY,PWR:3,0.75MM,240V,96.0L	S3109	1600
	-----			-						(OPTION A3 AUSTRALIAN ONLY)		
-5	334-3995-00			1						MARKER,IDENT:MARKED CAUTION	80009	334-3995-00
	-----			-						(OPTION A3 AUSTRALIAN ONLY)		
-6	161-0066-12			1						CABLE ASSY,PWR:3,18 AWG,240V,96.0 L	T1105	OBD
	-----			-						(OPTION A4 NORTH AMERICAN ONLY)		
-7	161-0154-00			1						CABLE ASSY,PWR:3,0.75MM SQ,240V,6A,2.5M L	000JA	A25SW
	-----			-						(OPTION A5 SWISS ONLY)		
-8	012-0911-00			1						CABLE,INTCON:144.0 L	04919	OBD
-9	334-5164-00			1						OVERLAY KEYBOARD:MARKED USER DEFINABLE		
	070-4981-00			1						MANUAL,TECH:OPERATORS	80009	070-4527-00
	070-4893-00			1						MANUAL,TECH:REFERENCE	80009	070-4893-00
	070-4892-00			1						MANUAL,TECH:REFERENCE	80009	070-4892-00
OPTIONAL ACCESSORIES												
	070-4889-00			1						MANUAL,TECH:SERVICE	80009	070-4525-00
	067-1150-00			1						FIXTURE,CAL:CABLIBRATION GRATICULE	80009	067-1150-00
	067-1043-00			1						FIXTURE,CAL:HOST PORT LOOP BACK CONN	80009	067-1043-00
	013-0214-00			1						ADAPTER ASSY:COPIER LOOPBACK TEST FIXTURE	80009	013-0214-00
	070-4891-00			1						MANUAL,TECH:SERVICE DISPLAY MODULE	80009	070-4689-00



Option	Order No.	Qty.	Name & Description
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OPTIONS

A1			EUROPEAN:POWER OPTION
A2			UNITED KINGDOM:POWER OPTION
A3			AUSTALIAN:POWER OPTION
A4			NORTH AMERICAN:POWER OPTION
A5			SWISS:POWER OPTION
4A			UNITED KINGDOM KEYBOARD
4B			FRENCH KEYBOARD
4C			SWEDISH KEYBOARD
4F			DANISH/NORWEGIAN KEYBOARD
4G			GERMAN KEYBOARD
4K			KATAKANA KEYBOARD

Section 13

ACCESSORIES

These accessories are listed in the mechanical parts list (Section 12) where part numbers are given for each item. Standard accessories are supplied with each 4107, and optional accessories may be ordered separately, and in addition to, standard accessories.

STANDARD ACCESSORIES

- *4107/4109 Reference Guide*
- *4107/4109 Programmers Reference Manual*
- *4107/4109 Operators Manual*
- Keyboard (detached item with connecting cable)
- Keyboard overlays
- Power cord set
- RS-232 Host port cable

OPTIONAL ACCESSORIES

- *4107 Service Manual*
- *Display Module for the 4107, Service Manual*
- RS-232 loop-back connector
- Copier port loop-back connector
- Centronics-type copier cable
- Alignment graticule (for display image)

AUXILIARY EQUIPMENT

The ADS01 Adjustable Display Stand provides an adjustable base for the display unit of the terminal. This Adjustable Display Stand sets on a table or desk and allows the user to adjust the display for optimum viewing height and angle.

Appendix A

STRAP INFORMATION

The 4107 terminal has straps on the Terminal Control board and the Display Module. These straps provide flexibility in its operating parameters. The two general types of straps are: cut straps, and jumper straps. In cases where a terminal was designed to function in one way, but provisions were made for future design enhancements, cut straps are often used. Jumper straps are used for most strap options, which allows:

- More than one kind of chip to be used in a given socket
- A change in timing or other operating parameters

TERMINAL CONTROL BOARD STRAPS

Table A-1 lists the straps on the Terminal Control board. Straps labeled "Jxxx" (on the circuit board) have square pins with movable jumpers. Straps labeled "Wxxx" are cut straps; they consist of circuit runs on layer 1 of the ECB (and no square pins).

Table A-1

TERMINAL CONTROL BOARD STRAPS

Strap Label	Definition and Function
EEPROM Type Straps: (W30 two straps)	These two straps are related to the type of EEPROM used (2817, or 2817A). One strap changes pin 1 (Vpp) for 2817, to READY/BUSY for a 2817A. The other strap changes the 2817 READY/BUSY to an extra address line for a 2817A.
Keyboard/Host-Port Timing (W295 & W294)	These straps allow clock input X2 to be used instead of X1. The appropriate components must be inserted, then cut both straps.
RS-232A vs. RS-232C (W493)	This cut strap provides a means for converting from RS-232A to RS-232C. This strap moves the driver for 'secondary request to send' from pin 11 to pin 19 (on output connection).
2PPI-related Straps: (see Special Clock Provisions)	
Processor Clock, W137	When connected, runs the processor on the Display Control Board's 14.7456 MHz clock.
DUART Clock, W280	When connected, runs the DUART's divide-by-four network on the 14.7456 MHz Display Control Board clock.
W294, W295	These cut-straps allow the DUARTs to run on 3.6864 MHz crystals.

STRAP INFORMATION

SPECIAL CLOCK PROVISIONS

There are four possible clock sources, other than the normal source on the Terminal Control Board. The normal source (with no straps cut or oscillators on the TCB) is the 14.7456 MHz oscillator on the Display Control Board. In this mode, the DUARTs and 80186 all run on the same clock. If the processor or DUARTs are to be run on different clocks, then one or more of the following changes must be implemented:

- Run the DUARTs on their own oscillator module (14.7456 MHz). To do this, cut the strap in the DISP CLK line (W280) and let the oscillator chip, Y485, provide the 14.7456 MHz clock.
- Run the DUARTs on 3.6864 MHz crystals. To do this, cut the straps at both DUARTs: W294 and W295 for U290, and also the two cut-straps for U437. Then install the crystals and two 20 pF capacitors in the spaces marked "not used" (on the schematic).
- Run the processor on an oscillator module. To do this, cut the strap that connects the terminal clock to the processor (W137). Now insert an oscillator module of the desired frequency into the spot labeled "186 clock." The DUARTs can still be run on the display clock.
- Run the processor on a crystal. To do this, cut strap, W135, and install a crystal in the spot for Y135. Install 20 pF capacitors in the spaces marked "not used", and strap the other side of W135.

DISPLAY MODULE STRAPS

The separate *Display Module for the 4107, Service Manual* contains strap information for the 119-1594-00 Display Module. The present version of the module contains no straps, but the Display Module service manual will provide the latest strap information.

Appendix B

REPLACING ROMS

CAUTION

Before removing the ROM Access Door, or before touching any ROMs, read the following "Electrostatic Discharge Awareness" information.

ELECTROSTATIC DISCHARGE AWARENESS

This product contains components that are highly sensitive to electrostatic discharge. To prevent damage to such components and to maintain product reliability, do NOT touch or remove the circuit boards or components in the 4107 until the following conditions are met.

Handling of Static-Sensitive Components

Handle all static sensitive components (such as ROMs, EEROMs, custom logic arrays, etc.) in a static-safeguarded work area. A static-safe area is any area that is capable of controlling static charge on conductive materials, people, and non-conductive materials.

The following equipment is recommended to create a static-safe area:

- Conductive floor mats,
- Conductive table mat,
- Wrist strap (conducts acquired body charge to ground),
- Ground cord (to suitable ground connection),
- Ionized air blower (for certain applications where climate or other conditions create excessive static build-up).

Transportation of Static-Sensitive Components

Transport all static-sensitive components in static-shielded containers/packages.

A "static shield" container must be capable of protecting from static discharge as well as static fields. The following is a list of suitable static-shield containers:

- Plastic bags (10,000 ohms/sq-cm insulation value),
- Insulated tote boxes,
- Dip Tubes (constructed especially for transporting Dual In-line Package components: RAMs, ROMs, etc.).

REPLACING ROMS

ROM REPLACEMENT PROCEDURE

The terminal contains replaceable ROMs (Read Only Memories, used to host programs that control the terminal, provide command-set instructions, etc.) This allows you to update firmware as new versions become available. The only tool required for this procedure is a small flat-bladed screwdriver.

Replace the ROMs by doing the following:

1. **Remove the ROM access door.** This door is located at the rear of the terminal (see Figure B-1) and may be removed by pulling it out from the top. Once the door is free, set it aside. The eight banks of ROMs are now exposed (see Figure B-2).

NOTE

If this is the first time a set of ROMs has been replaced, the ROM may be difficult to remove from the socket. With gentle pressure, however, the ROM should come free.

2. **Remove each ROM to be replaced.** Do this by using the screwdriver to pry the top and bottom of the ROM from its holder (see Figure B-2). Place the old ROMs in a safe location until operation of the new ROMs has been verified. Then you may wish to discard the old ROMs.

CAUTION

Make sure that the new ROMs are installed in the proper sockets. If the ROMs are installed in the wrong locations, the terminal will not operate properly. If this happens, remove the ROM and install it in its proper socket.

3. **Install the new ROMs.** Place each ROM into the proper socket (each ROM is labeled by a component number; match this number to the number on the circuit board). The ROMs are keyed so they cannot be installed upside down. Lock each ROM in place by pushing firmly in.

4. **Reinstall the ROM access door.** Place the bottom of the door in the chassis first, then lock it in place by pressing in firmly on the top of the door.

This completes the ROM replacement procedure. Your terminal is now ready for use with its new firmware.

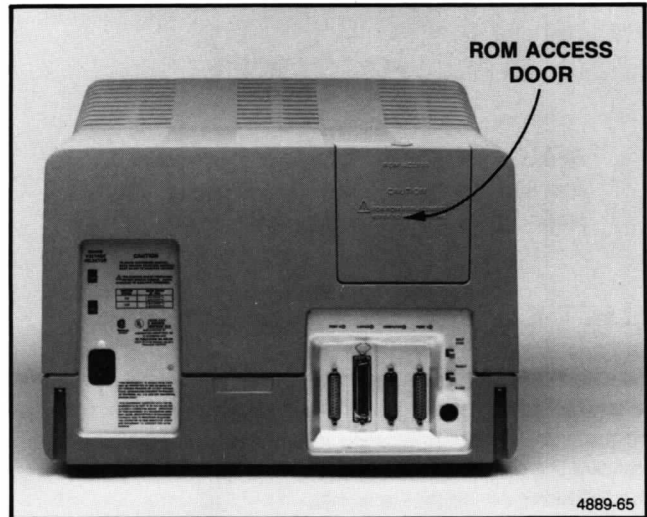


Figure B-1. ROM Access Door.

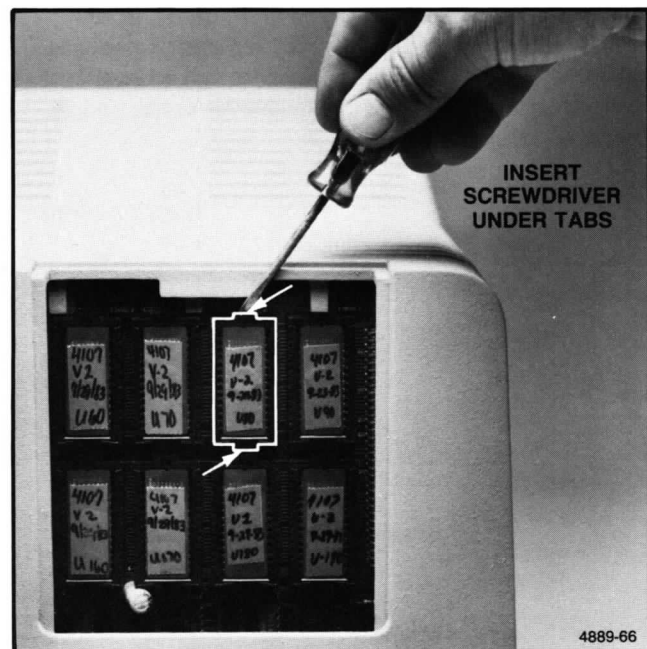


Figure B-2. Replacing the ROMs.

Appendix C

SELF TEST DIAGNOSTIC PROGRAM

INTRODUCTION

The primary troubleshooting aid for the terminal is the Self Test diagnostic program. This program resides in firmware and is arranged to test most of the hardware of the terminal (see NOTE). For the most part, Self Test does not depend on any portion of the hardware until it has tested it; it may then use this hardware to aid in other tests.

This appendix covers the levels of Self Test, how errors are reported, how to start and run the different levels of Self Test, descriptions of the tests that are performed, and how to select and run menu items.

NOTE

The Self Test program does not test the power supply or Display Module. Power supply problems are relatively easy to isolate. For more information on the power supply, consult the theory of operation section.

The Display Module is not automatically checked during Power Up or Extended Self Test. However, you may check the basic parts of the Display Module by running Adjustment Self Test. The adjustment patterns listed in the display menu may be used to determine what part of the Display Module is malfunctioning. Also, a green LED on the top of the Display Control board is on if the Display Module circuitry is generating a +5 volt supply.

SELF TEST OVERVIEW

LEVELS OF SELF TEST

There are three levels of the Self Test diagnostic program. These are: Power Up Self Test, Extended Self Test, and Adjustment Self Test. Figure C-1 shows how these levels relate to one another.

Power Up Self Test

Power Up Self Test runs automatically every time the terminal is turned on, or the RESET button is pushed. It performs a quick check of the various hardware modules. This check takes less than 15 seconds to run, and occurs during the time between turning on (or resetting) the terminal and when the cursor appears.

To do more extensive testing of the terminal, use Extended Self Test or Adjustment Self Test.

Extended Self Test

Extended Self Test includes all the tests run during Power Up Self Test as well as much more extensive testing of circuitry. Extended Self Test may take up to four minutes to complete. It is initiated by pressing the SELF TEST and RESET buttons (located on the rear of the terminal) in the proper sequence. The procedure for starting Extended Self Test is covered later in this appendix.

During Extended Self Test, a menu appears that allows you to enter Adjustment Self Test.

Adjustment Self Test

Adjustment Self Test is used primarily for making adjustments and performance checks. However, this version of Self Test may also be used as a troubleshooting tool for certain parts of the terminal, such as the host port and copier port. Detailed information about Adjustment Self Test is located near the end of this appendix.

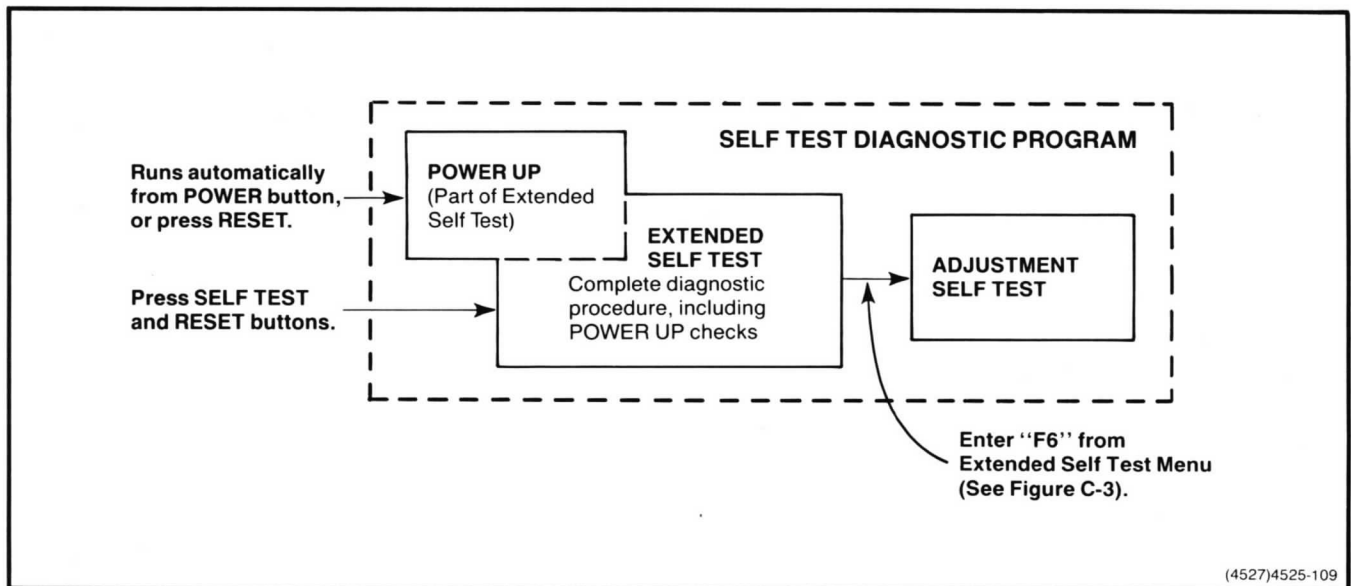


Figure C-1. Self Test Functional Diagram.

ERROR REPORTING

If the terminal finds a problem with itself while running Self Test, it reports this fact in the form of a message. Error messages may occur in one or more forms. These are: a printed message, the terminal bell, the light on the CAPS LOCK key, and internal indicator LEDs.

Printed Message

Anytime Self Test finds a problem, it tries to write a message on the screen. The message relates to what failed when Self Test tried to test it. A printed error message begins with the words "Self Test Error -".

The possible printed error messages are:

Processor System Failure [xx.zzzz] (see NOTE)

Uxxx ROM Checksum Failure (Uxxx is the component number of the defective ROM)

Uxxx ROM is Wrong Part (Uxxx is the component number of the defective ROM)

RAM System Failure [xx.zzzz]

Nonvolatile Parameters Failure - Defaults Reset [xx.zzzz]

Keyboard Failure or Not Attached [xx.zzzz]

Keyboard Interface Failure [xx.zzzz]

Host Port Failure [xx.zzzz]

Printer Port Failure [xx.zzzz]

Dialog Display System Failure [xx.zzzz]

Graphics Display System Failure [xx.zzzz]

The bracketted part of the message is a code that provides more detailed information; xx is the test number, and zzzz is the actual error code. A list of definitions for these many codes, is located at the end of this appendix under the heading, Error Codes.

NOTE

The Processor System Failure test has no unique test number. It may locate system errors during any of the other tests. This message displays the number of the test where the system error occurred. The error code is also borrowed from that test.

Terminal Bell

The terminal bell rings twice when Self Test encounters a problem. The only exception to this is if the keyboard is not connected.

CAPS LOCK Key Light

When Self Test checks the keyboard, the light on the CAPS LOCK key flashes quickly. If Self Test finds a problem with the keyboard, this light stays on.

SELF TEST

Additional Indicators

On the rear panel of the terminal, there is a pop-off cover that protects the Terminal Control board ROMs. With this cover removed, three red LEDs are visible (see Figure C-2).

- The left LED represents the Terminal Control board
- The middle LED represents the RAM3 board
- the right LED represents the Display Control board

When a test is running for circuitry on one of the boards, the corresponding LED flashes. If a problem is found with that circuit board, its LED remains lit. This way, for certain messages printed on the screen, you can further isolate the problem to one of the two main boards. Take the cover off, and observe which LED is lit, to determine which of the three circuit boards failed.

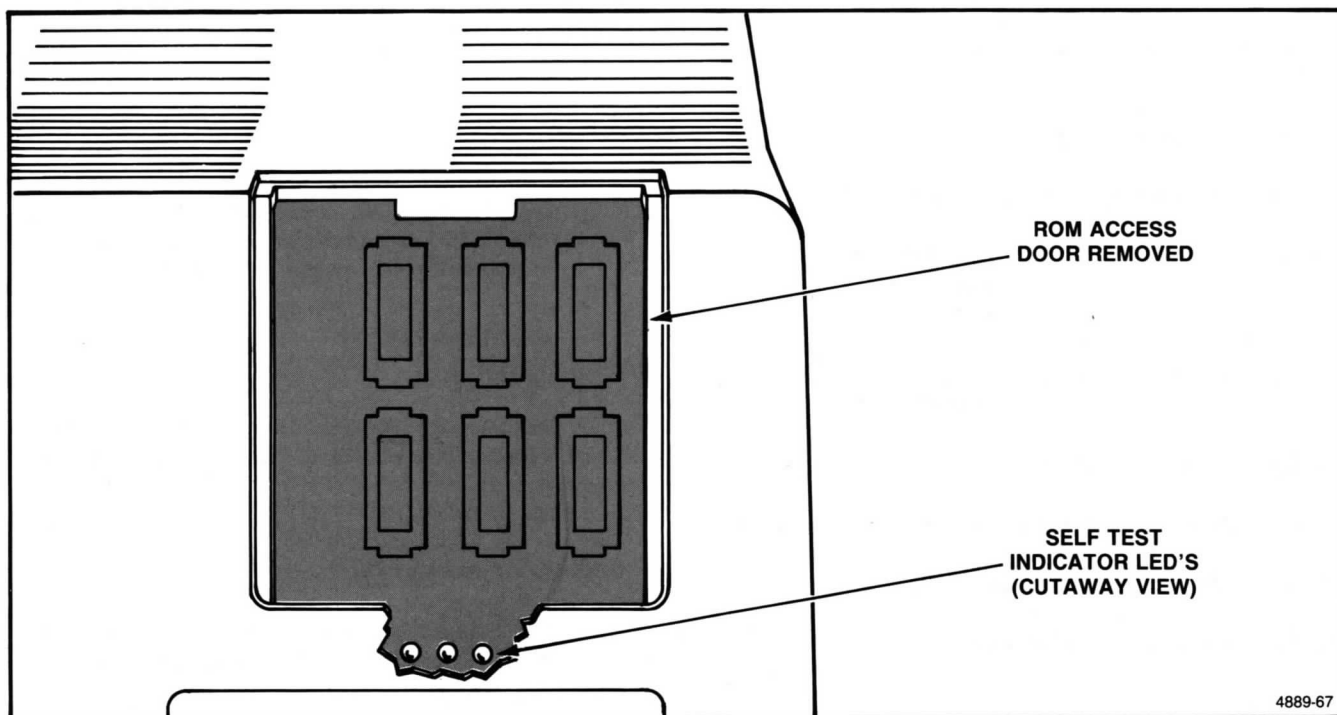


Figure C-2 . Indicator LEDs.

RUNNING SELF TEST

STARTING EXTENDED SELF TEST

Perform the following steps when starting Extended Self Test or Adjustment Self Test:

1. Press the SELF TEST button (located on the rear of the terminal) and hold it in.
2. Press the RESET button (also located on the rear of the terminal; below the SELF TEST button) and release it.
3. Hold the SELF TEST button for another two seconds, then release it.

A graphics crosshair cursor appears on the screen to indicate that Extended Self Test is running. The crosshairs blink alternately between black and white.

After about 30 seconds, the crosshairs disappear, a menu appears on the screen (see Figure C-3), and the bell rings once (one bell is a prompt for user input).

When this menu appears, you have three choices: you can press the F6 key (which displays the Adjustment Self Test menu), you can press F7 to continue Extended Self Test, or you may exit Extended Self Test by pressing F8.

If you do nothing at all, the terminal waits for 20 seconds. After this amount of time, if it has received no keyboard input, it goes ahead and continues with Extended Self Test.

```

F5    Continuous Self Test
F6    Adjustment Procedures Menu
F7    Continue Self Test
F8    Exit Self Test

Selection:
    
```

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Figure C-3. Extended Self Test Menu.

CONTINUING EXTENDED SELF TEST

When Extended Self Test continues, the crosshair cursor is placed back on the screen. It continues to blink between white and black as long as everything is proceeding normally. When Extended Self Test has finished testing (after about four minutes), the bell rings once, the menu shown in Figure C-4 is placed on the screen, and Extended Self Test halts.

You must select an item from this menu. The test does not "time out" and continue if nothing is done. Pressing either the F7 or F8 keys ends Extended Self Test and returns the cursor to the screen. Pressing any of the other keys in the menu enters Adjustment Self Test and performs the tests or displays the menus indicated.

```

Adjustment Procedures Menu

F1    Reset Nonvolatile Parameters
F2    Keyboard Switch Test
F3    RS-232 Interface Menu
F4    Hard Copy Menu
F5    Display Pattern Menu
F6    Graphics Tablet Menu
F7    Exit Current Menu
F8    Exit Self Test

Selection:
    
```

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Figure C-4. Adjustment Test Menu.

CONTROL FLOW OF SELF TEST

Table C-1 shows the order in which the various hardware modules are tested. During Power Up Self Test, only the tests marked PUP are performed. During Extended Self Test, all of the tests are performed. Figure C-5 is flow chart of Self Test.

Table C-1
POWER UP/EXTENDED SELF TEST SEQUENCE

Test Name	When Executed ^a	Board Tested
ROM checksum and position	PUP/EST	TCB
TCB Short RAM memory	PUP/EST	TCB
TCB Long RAM memory	EST	TCB
Keyboard	PUP/EST	KBD & TCB
Host port (internal loopback)	PUP/EST	TCB
Host port interrupt check	PUP/EST	TCB
RS-232 peripheral ports check	PUP/EST	TCB
RS-232 peripheral ports interrupt check	PUP/EST	TCB
Printer/copier port check	PUP/EST	TCB
Printer/copier port interrupt check	PUP/EST	TCB
RAM3 Short memory test	PUP/EST	RAM3
RAM3 Long memory test	EST	RAM3
Display I/O handshake	PUP/EST	DCB/TCB
Display Read/Write ports	PUP/EST	
CRT Controller timing	PUP/EST	DCB
Color map	PUP/EST	DCB
Graphics Control	PUP/EST	DCB
Graphics memory (short test)	PUP/EST	DCB
Graphics memory (long test)	EST	DCB/RAM3
Dialog memory (short test)	PUP/EST	DCB
Dialog memory (long test)	EST	DCB/RAM3
Character ROM	PUP/EST	DCB
Video paths	PUP/EST	DCB
Dialog attributes	PUP/EST	DCB
Display interrupt check	PUP/EST	DCB

^a EST means the test is performed during Extended Self Test.
PUP means the test is performed during Power Up Self Test.

Once a test has passed, the components tested can be ruled out as being good. So, as an example, if Extended Self Test failed during the Color Map test, all components associated with the tests before the color map are good. The problem is likely in the Color Map circuitry itself, but it could also be caused by one of the areas not yet tested.

TEST DESCRIPTIONS

Following are descriptions of all the tests listed in Table C-1 (the interrupt checks are described under one title). The test descriptions tell what area of the terminal each test checks and what each test does.

ROM Checksum and Position

This test performs a checksum on all ROMs in the terminal. A position test is also performed to make sure that the ROMs are plugged in the correct sockets and are residing at the right address space.

RAM Memory Test

This test is done on all system RAM. The various tests that are done are:

- A walking ones check. All system RAM is set to zero. A one bit is then "walked through" the field of zeros for all memory space. If a bit is not able to be raised to a logical one, an error results.
- A walking zeros check. Similar to the walking ones check. All system RAM space is set to one. A zero bit is then walked through memory space. If a bit is not able to be set to zero, an error results.
- A March II check. Data is written into a memory location and then immediately read back. If the data is correct, the test moves to the next memory location.
- Refresh Test. A bit pattern is written in RAM. Self Test then waits 15 seconds and checks the RAM to make sure the bit pattern is still there. Because of the time required for the refresh memory test, it is only done during Extended Self Test.

Keyboard Test

This test verifies that all hardware within the keyboard is functional. During this test, the terminal holds the keyboard inactive (this allows testing to be done while preventing input to the terminal). A loopback test of the keyboard interface on the Terminal Control board is then performed (keyboard output is looped back to become keyboard input). At the same time, the keyboard microprocessor performs its own test. At the end of this test, the keyboard sends a status byte to the terminal. If the keyboard passes the test, this status byte is F0 (hex). If the keyboard does not pass; either no status byte, or a value of FF (hex) is returned.

During the keyboard test, the light on the CAPS LOCK key flashes briefly. If a problem occurs, this light stays on.

To test the keyboard keys and their mechanical connections, use the keyboard key switch test, available in Adjustment Self Test.

Host Port Test

This test checks the RS-232 host interface by placing the Dual Universal Asynchronous Receiver-Transmitter (DUART) chip in internal loopback mode. Characters are then transmitted and received internally without affecting the external lines going to the host computer or modem.

A more thorough test of the RS-232 port may be performed using Adjustment Self Test. This requires use of the RS-232 loopback connector and checks the connections to the host connector itself.

2-Port Peripheral Interface Test

This test checks the other half of the DUART. The test is the same as the Host Port Test, but checks the 2PPI input and output paths and the related part of the DUART.

Copier Port Test

The Programmable Peripheral Interface (PPI) chip is checked by reading and writing to registers in the chip. However, no data is output to the copier port to be read back.

A more thorough test of the copier port may be performed using Adjustment Self Test. This requires use of the copier port loopback connector and checks connectors to the copier port connector itself.

Interrupt Tests

The interrupt inputs and masks are tested by generating interrupts and then checking that the interrupts are recognized and serviced correctly. This is accomplished in the following manner:

1. Interrupts are generated and serviced from the sources HOSTDAV, MISCCOMINT, PRINTERINT, and DISPINT (see the schematics, Section 11, for the location of these signals).
2. The interrupts are again generated from the same sources, this time with the masks on. Self Test checks to make sure that the processor is not interrupted.
3. HOSTDAV and MISCCOMINT are again generated to make sure that the interrupts are nested properly.

Display I/O Handshake Test

This test makes sure that the processor can communicate with the Display Control board (DCB) and that the board responds with the appropriate acknowledge. Both, the dialog and graphics, handshake circuitries are verified.

Display Read/Write Ports Test

This test exercises the read/write ports to make sure that no lines are stuck to a logic high or low.

SELF TEST

Graphics Control

This test verifies operation of the programmable array logic chips that control the graphics display section of the DCB.

Dialog Controller Timing Test

This test verifies the horizontal and vertical sync timing of the DCB's 9007 CRT Controller, within the limits of the microprocessor.

Dialog Memory Test

This test checks the RAM memory for the dialog area. The same four tests are performed on this RAM as is performed on the system RAM. For more information, see the description of the RAM memory tests.

Graphics Memory Test

This test checks the the RAM memory for the graphics area. The same four tests are performed on this RAM as is performed on the system RAM. There is one difference, however, in that unused data bits are masked off. For more information, see the description of the RAM memory tests.

Character ROM Test

The character ROM is checked by forcing the ROM to output each character. The character dot information is then captured from the processor and compared to character data in system firmware. If these do not match, an error is generated.

Color Map Test

The Color Map RAM is checked using a "walking 0" and a "walking 1" test. For information on these tests, see the descriptions under RAM Memory Tests.

Dialog Attributes Test

The dialog attributes are tested by setting and clearing attribute bits in the dialog RAM. Whether the appropriate attributes were tested, is determined by reading attribute status from the processor.

Video Paths Test

Using special Self Test modes, the video data is selected from an alpha foreground, alpha background, alpha cursor, graphics, graphics cursor, and blanking. By programming the appropriate data on a scan line from the selected source, the video data path can be verified by reading the color map address. Each data bit, from each video source, is set high and low. The color map address is then checked to make certain the data path is functioning correctly.

ADJUSTMENT SELF TEST

Adjustment Self Test is used to perform adjustment procedures on the Display Module or to perform validation checks on the terminal's interfacing ports.

Adjustment Self Test is entered after starting Extended Self Test. The Adjustment Self Test menu may be displayed by pressing the F6 key, when the first menu appears (see Figure C-3), or by waiting until Extended Self Test is finished. The Adjustment Procedures Menu is shown in Figure C-6.

A test or pattern may be selected by pressing the key associated with that test or pattern. The remainder of this appendix describes these menu items.

F1 RESET NONVOLATILE PARAMETERS

CAUTION

Pressing the F1 key, changes any communication parameters that are not set to the default value. Unless this is desired, do NOT press this key.

Pressing the F1 key causes all nonvolatile parameters to be set to the default value. This may take up to a minute, depending on how many parameters must be reset. When the parameters have been reset, the following message appears on the screen:

Nonvolatile Parameters Reset

Once this message has appeared, you may select any of the other items from the Adjustment Procedures Menu.

F2 KEYBOARD SWITCH TEST

After pressing the F2 key, a message appears telling you what type of keyboard is installed ("North American" or "French" for example). Following this message, another message appears:

Press keyboard keys. Press F7 twice to exit.

As each key is pressed, its unshifted nomenclature is displayed. For instance, if the A, S, D, F, F1, TAB, and ESC keys are pressed, this appears on the screen:

A S D F F1 TAB ESC

While the key is pressed, the key identifier (nomenclature) displayed on the screen blinks. When the key is released, the nomenclature stops blinking. This test is useful for verifying that all keys make contact and display the proper code.

F7 must be pressed twice to exit this test. The first time F7 is pressed, F7 is displayed.

```

Adjustment Procedures Menu

F1  Reset Nonvolatile Parameters
F2  Keyboard Switch Test
F3  RS-232 Interface Menu
F4  Hard Copy Menu
F5  Display Pattern Menu
F6  Graphics Tablet Menu
F7  Exit Current Menu
F8  Exit Self Test

Selection:
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```

Figure C-6. Adjustment Procedures Menu.

SELF TEST

F3 RS-232 INTERFACE MENU

Pressing the F3 key causes the RS-232 ports menu to be displayed. This menu is shown in Figure C-7.

NOTE

These tests require that the RS-232 loopback connector be used. This connector is an optional accessory to the terminal and may be ordered if one is not available. There is no way to perform this test without this loopback connector.

You may select any item from this menu. Each test is similar, but checks a different data path (from connector to DUART and back).

F1 - Host Port Test

Pressing the F1 key causes the following message to be displayed:

**Install RS-232 Loopback. Press
Space Bar.**

If a cable is connected to the host port, disconnect this cable and connect the RS-232 loopback connector to the host port. Once the connector is in place, press the Space Bar. This causes the terminal to do three checks:

- Hex characters 00, 55, AA, and FF are transmitted at the highest baud rate and then looped back to be received. This test checks to make sure that transmitted characters match the received characters. Status bit timing is also checked.
- The timing of user-selectable baud rates is checked.
- RS-232 status and control lines (RTS and CTS for example) are checked for proper flagging.

After these checks are completed (about 2 seconds) the following message is printed on the screen:

**RS-232 Interface Test Completed.
Selection:**

If an error occurs during the test, the bell rings twice, and this message appears:

**Self Test Error - Host Port Failure
RS-232 Interface Test Completed
Selection:**

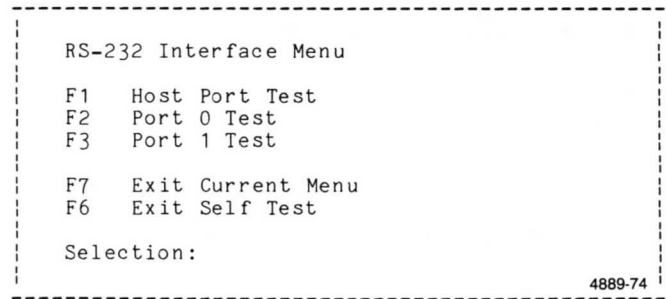


Figure C-7. RS-232 Interfaces Menu.

F2 and F3 - Peripheral Port Tests

Pressing the F2 or F3 key causes the following message to be displayed:

**Connect Host Port cable to Port x. Press Space
Bar.**

If a cable is connected to the peripheral port (to be checked), unplug it. Connect one end of the host RS-232 cable to the host port. Then connect the other end of that cable to the peripheral port to be checked (port 0 for F2, port 1 for F3). The terminal sends/receives data from the host connector to the respective peripheral port. This verifies the operation of the internal send and receive paths.

After these checks are successfully completed (about 2 seconds), the following message appears:

**Peripheral Port Test Completed
Selection:**

If a fault occurs during the test, the bell rings twice, and the following message appears:

**Self Test Error - Port x Failure
Peripheral Port Test Completed.
Selection:**

F4 HARD COPY MENU

Pressing the F4 key causes the hard copy menu to be displayed. This menu is shown in figure C-8. You may now select one of the items from this menu.

Pressing the F7 key returns to the Adjustment Procedures Menu. Pressing the F8 key exits Self Test.

F1 - Loopback Test

NOTE

Selecting the Loopback test from the Hard Copy menu requires that the hard copy loopback connector be used. This connector is an optional accessory to the terminal and may be ordered if one is not available. The loopback test can not be performed without the loopback connector.

The hard copy loopback test is similar to the RS-232 loopback test just described. After selecting the hard copy loopback test, the following message appears:

Install Copier port loopback. Press Space Bar.

After space is typed, the test will run and then return to the hard copy menu when finished. The following message is displayed when the test has finished with no errors detected:

**Copier Loopback Test Completed
Selection:**

If an error is detected by this test, the bell rings twice, and the following message is displayed on the screen:

**Self Test Error - Printer Port Failure
Copier Loopback Test Completed.
Selection:**

F2 - Color Copier Pattern

This test outputs a color pattern to a color copier connected to the copier port; this checks the interface connection between the terminal and the copier/printer. This pattern may be used to verify that the pattern displayed on the screen is accurately reproduced by the copier.

From the Hard Copy Menu, press F2. This displays the following message:

Connect Copier. Check that the copier READY light is on. Press Space Bar.

If the copier is not connected or not functioning, when the Space Bar is pressed, the following message is displayed on the screen (and it exits back to the hard copy menu):

***** Copier not ready *****

If the copier is functioning, the pattern shows up, and this message appears on the screen:

This pattern should be on the Copier and display:

The pattern consists of eight adjacent vertical bars (each is 10 character-cells wide). The bars are painted these colors: black, blue, red, magenta, green, cyan, yellow, and white. The test then prints a message, and exits back to the Hard Copy Menu.

Test Completed.

```

Hard Copy Menu

F1  Loopback Test
F2  Color Copier Pattern

F7  Exit Current Menu
F8  Exit Self Test

Selection:
  
```

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Figure C-8. Hard Copy Menu.

SELF TEST

F5 DISPLAY PATTERN MENU

Pressing the F5 key causes the Display Pattern Menu to be displayed. This menu is shown in Figure C-9.

These display patterns are used primarily for adjustment of the terminal, before being shipped from the factory. Some of these patterns, however, may be useful for on-site adjustment of the terminal. To find out which patterns are used, consult the adjustment section (5) in this manual.

The crosshairs test displays the cross hair cursor. The cursor begins in the upper left corner of the screen and moves to the lower right corner. The cursor may be stopped by pressing a keyboard key. If no key is pressed, the process is repeated.

On any of the patterns, the red, green, and blue components of the display may be controlled. Each color may be turned on or off, or may be increased in intensity by pressing the designated key. There are four levels of intensity for each color component; after selecting the highest level, the color goes back to the lowest level on the next select. When a new display pattern is selected, or the Display Menu Pattern is exited, the color map is reset to the default values.

The Set Color key toggles between a visible and invisible menu.

```
-----  
Display Pattern Menu  
  
F1      Grid Pattern Menu  
F2      Gray Scale Pattern  
F3      White Screen Pattern  
F4      Color Pattern  
F5      H Pattern  
F6      Crosshairs Test  
  
F7      Exit Current Menu  
F8      Exit Self Test  
Sh F1   Video Amp Zero Level  
Sh F2   Video Amp Maximum Level  
Sh F3   Dot Pattern  
  
Dialog   Toggle red video on and off  
Setup    Toggle green video on and off  
S Copy   Toggle blue video on and off  
Sh Dialog Increment red intensity  
Sh Setup  Increment green intensity  
Sh S Copy Increment blue intensity  
Menu     Turn the menu on and off  
  
Selection:  
  
-----  
4889-76
```

Figure C-9. Display Pattern Menu.

F6 GRAPHICS TABLET TEST

After selecting the graphics tablet test, this message appears on the screen:

Connect Table to Port 1. Press Space Bar.

Upon pressing the space bar, the test begins, and the screen displays one or the other of these messages (depending on whether the tablet pen is in presence or not):

Tablet Self Test Passed - Cursor on Tablet.

or

Tablet Self Test Passed - Cursor off Tablet.

If the tablet test fails, the following message is displayed:

Tablet Self Test Failed.

Furthermore, if the tablet does not respond to the query from Self Test, the following message is displayed:

No Response from Tablet.

All of these messages are followed by the prompt message (which lets you return to the Adjustment Menu):

Selection:

ERROR CODES

Each error message displayed by the main part of Self Test (not Adjustment Self Test) contains a text message followed by a numeric error code, such as:

Display System Failure [20.000F]

This part of the Self Test appendix lists these error codes and explains how to read them.

The English part of the message is self-explanatory, such as "Display System Failure." This means that a failure occurred on the Display Control board (not the Display Module). The error code is more involved and requires some study in the following error code tables to determine the meaning. The first part of the code (the two digits in front of the decimal) stand for the test name where the fault occurred. In the case above, "20" stands for the test named "Graphics Memory Bank Select test;" see Error Codes List.

The second part of the code is a four-bit Hex code. Each test has its own unique error codes, so you need to first look up the test description and then read the error code description under that test name. There are two basic types of error codes:

- One is a simple Hex number that stands for an area of memory that failed, etc.
- The other type of code is also a Hex number; but you must convert it to a binary number and look up the active binary bits, to see what the error code stands for.

The following explanation tells you how to convert these Hex numbers into code definitions.

INTERPRETING HEX ERROR CODES

Many of the error codes listed in this appendix are listed as Bit 0 thru Bit 9 set. However, the displayed error code is a Hex number. Use the following steps to convert these Hex codes to meaningful information.

1. First, read the last four digits of the code as a four-digit Hex number.
2. Then, look up the Hex number in Table C-2. Convert each Hex digit into a corresponding binary number.

3. Write down each binary group in order.
4. Write the numbers 0 through 9 (bit numbers) over these binary digits.
5. See which of the ten bits are active, and look for the corresponding bit-descriptions under the test name.

EXAMPLE 1 --

The following error message is reported:

"Dialog Display System Failure [2A.00FF]"

The 2A represents the "Dialog foreground index test." The error code is "00FF". We look up each Hex number in Table C-2, and record the binary groups as follows:

0	0	F	F
0000	0000	1111	1111

Now number these bits right to left:

10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	1	1	1	1

This means that bits 0 through 7 are all active. Looking under the description of the 2A test, we find bits 0 through 7 indicate which background indices (0 to 7) have failed. In this case all eight background indices failed, which seems to indicate a problem common to the entire dialog background display. You would look for a part of the circuitry that affects all of the dialog background.

Table C-2

HEX-TO-BINARY CONVERSION

Hex	Binary	Hex	Binary
0	0000	8	1000
1	0001	9	1001
2	0010	A	1010
3	0011	B	1011
4	0100	C	1100
5	0101	D	1101
6	0110	E	1110
7	0111	F	1111

SELF TEST

EXAMPLE 2 --

Let's try another error code, just to be sure we have the picture. Suppose this error message appears:

"Display Timing Fault [1D.001A]"

Apparently there is some type of timing problem on the Display Control board. The "1D" test is called "CRT Controller Timing test". Now we know that the problem is related to the 9007 CRT controller chip.

Looking up the 001A Hex code in Table C-2, we find the following bit pattern:

0	0	1	A
0000	0000	0001	1010

Setting these binary groups against the bit numbers yields:

10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	1	0

This means that bits 1, 3, and 4 are active (high).

Under the error code explanation for test 1A, we find these errors correspond to the bits listed in the error message.

Bit 0 – (ignore)

Bit 1 – VS bit was never set low.

Bit 2 – (ignore)

Bit 3 – On the first visible line, one or more of the following status bits was set incorrectly: VS should be high, HS should be high, VLT should be low, and DRB should be high.

Bit 4 – On the second visible line, DRB was not low.

Bit 5 – (ignore)

etc.

This points to problems with VLT and DRB signals in the CRT Controller chip.

SELF TEST ERROR CODES LIST

The following error codes may appear while the main part of Self Test is running. (The second group of codes in this section only appear during the Adjustments part of Self Test.) Each test is listed here (by name and test number), and the error code(s) for that test are explained in brief terms.

Test 1 – RAM Memory Walking Ones

Error code indicates a bad memory block. Error code (nnnn) indicates the location (between 0 and 7FFF) of a 32K block of faulty memory.

Test 2 – RAM Memory Walking Zeroes

This code (nnnn) indicates the location of a bad 32K memory block, between 0 and 7FFF.

Test 3 – RAM Memory March

This code (nnnn) indicates the location of a memory problem, between 0 and 7FFF.

Test 4 – RAM Memory Ones

Error code points to location of memory fault (as in Tests 1 thru 5).

Test 5 – RAM Memory Zeroes

Error code points to location of memory fault (as in Tests 1 thru 4).

Test 8 – Nonvolatile parameters test and load

Bit 0 = EEROM Ready line did not go true.

Bit 1 = EEROM checksum bad.

Bit 2 = EEROM system version number incorrect.

Bit 3 = EEROM byte cannot be written correctly.

Test 9 – DUART Timer Test

Bit 0 = Timer finished counting too quickly.

Bit 1 = Timer did not finish counting in the time allowed.

Test A – Keyboard interface loopback test

- Bit 0 = TxRDYA not set after transmitting the first character.
- Bit 1 = TxRDYA was set after the second character was sent.
- Bit 2 = TxEMTA, RxRDYA, and/or FFULLA were set after the first character finished transmission.
- Bit 3 = RxRDYA not set, or FFULLA set, after first character finished transmission.
- Bit 4 = TxRDYA, RxRDYA, and/or FFULLA not set after waiting for the third character.
- Bit 5 = TxEMTA not set after fourth character finishes transmission.
- Bit 6 = First character received is not 00 (H).
- Bit 7 = Second character received is not 0FF (H).
- Bit 8 = Third character received is not 5 (H).
- Bit 9 = Fourth character received was not 0AA (H).

Test B – Keyboard Self Test results

- Bit 0 = Data was received from the keyboard before the data clamp was released.
- Bit 1 = No status code was received from the keyboard.
- Bit 2 = Keyboard Self Test failed.

Test D – Host Port Transmit/Receive Test (internal loopback)

- Bit 0 = TxRDYB not set after transmitting first character.
- Bit 1 = TxRDYB was set after the second character was sent.
- Bit 2 = TxEMTB, RxRDYB, and/or FFULLB was set after the first character finished transmission.
- Bit 3 = RxRDYB not set or FFULLB set after first character finished transmission.
- Bit 4 = TxRDYB, RxRDYB, and/or FFULLB not set after waiting for the third character.
- Bit 5 = TxEMTB was not set after the fourth character finished transmission.

- Bit 6 = The first character received was not 00 (H).
- Bit 7 = The second character received was not 0FF (H).
- Bit 8 = The third character received was not 55 (H).
- Bit 9 = The fourth character received was not 0AA (H).

Test E – Test of Host Port baud rates (internal loopback).

If bit is set, its baud rate failed the test.

- Bit 0 = 19.2 Kbaud
- Bit 1 = 9600 Baud
- Bit 2 = 4800 Baud
- Bit 3 = 2400 Baud
- Bit 4 = 1800 Baud
- Bit 5 = 1200 Baud
- Bit 6 = 600 Baud
- Bit 7 = 300 Baud
- Bit 8 = 150 Baud
- Bit 9 = 110 Baud

Test F – Host port HOSTDAV interrupt test

- Bit 0 = HOSTDAV did not generate an NMI interrupt.
- Bit 1 = NMI interrupt was detected while it was disabled.

Test 10 – Host port MISCCOMINT interrupt test

- Bit 0 = MISCCOMINT did not generate an interrupt.
- Bit 1 = MISCCOMINT was detected while masked off at the processor.

Test 11 – PPI DUART timer test

- Bit 0 = Timer finished counting too quickly.
- Bit 1 = Timer did not finish counting in the time allowed.

SELF TEST

Test 12 – Port 0 transmit/receive test (internal loopback)

Error Bit definitions are same as for Test D.

Test 13 – Port 1 transmit/receive test (internal loopback)

Error Bit definitions are same as for Tests D and 12.

Test 14 – PPI Interrupt test

Bit 0 = PPI interrupt did not generate an interrupt.

Bit 1 = PPI interrupt was detected while masked of by the processor.

Test 15 – Hard Copy port internal data test

Bit 0 = The data written to hard copy output port was not same as the corresponding data when read back over this port.

Test 16 – Hard Copy port PRINTERINT interrupt test

Bit 0 = PRINTERINT did not generate an interrupt.

Bit 1 = PRINTERINT was detected while masked off by the processor.

Test 17 – RAM Memory walking ones check

Error codes indicate bad memory location as follows:

2000 = 32K memory block from 20,000 (H) to 27,FFF (H).

2800 = 32K memory block from 28,000 (H) to 2F,FFF (H).

3000 = 32K memory block from 30,000 (H) to 37,FFF (H).

3800 = 32K memory block from 38,000 (H) to 3F,FFF (H).

C000 = 32K memory block from C0,000 (H) to C7,FFF (H).

C800 = 32K memory block from C8,000 (H) to CF,FFF (H).

D000 = 32K memory block from D0,000 (H) to D7,FFF (H).

D800 = 32K memory block from D8,000 (H) to DF,FFF (H).

Test 18 – RAM Memory Walking Zeroes check

Same error codes as for Test 17

Test 19 – RAM Memory March

Same error codes as for Test 17.

Test 1A – RAM Memory Ones check

Same error codes as for Test 17.

Test 1B – RAM Memory Zeroes test

Same error codes as for Test 17.

Test 1C – Display I/O Handshake test

Bit 0 = DISPRDY line stayed in not-ready condition after writing the Graphics Control Register.

Bit 1 = DISPRDY line stayed in not-ready condition after reading the Graphics Control Register.

Test 1D – CRT Controller Timing test

Bit 0 = VS bit (Vertical Sync) was never set high.

Bit 1 = VS bit was never set low.

Bit 2 = Vertical sync ended too soon.

Bit 3 = On the first visible line, one or more of the following status bits was set incorrectly: VS should be high, HS should be high, VLT should be low, and DRB should be high.

Bit 4 = On the second visible line, DRB was not low.

Test 1E – Display Read/Write Registers test

Bit 0 = Graphics Control Register failed.

Bit 1 = Alpha Control Register failed.

Bit 2 = 9007 Vertical Cursor Register failed.

Bit 3 = 9007 Horizontal Cursor Register failed.

Test 1F – Color Map RAM test

The error code indicates the color map bad address offset. The bad address is reported as the four digit code <nnnn> in this message:

1F00: <nnnn>

Test 20 – Graphics Memory Bank Select test

- Bit 0 = Writing data to graphics memory Bank 1 caused the data in memory Bank 0 to be modified instead.
- Bit 1 = Incorrect data was written to graphics memory Bank 1.
- Bit 2 = Writing both pages did not write the correct data to Bank 0.
- Bit 3 = Writing both pages did not write the correct data to Bank 1.

Test 21 – Graphics Memory test

The error code represents the 64K segment of graphics memory that failed, as follows:

- 4000 = failure in memory between locations 40,000 and 4F,FFF.
- 5000 = memory problem between 50,000 and 5F,FFF.
- 6000 = memory problem between 60,000 and 6F,FFF.
- 7000 = memory problem between 70,000 and 7F,FFF.

Test 22 – Graphics 16-byte Write test

- Bit 0 = Writing even words to 16 locations failed to write 16 bytes at a time.

Test 23 – Graphics Plane Write Enable test

- Bit 0 = Plane 0 write-disabling failed.
- Bit 1 = Plane 1 write-disabling failed.
- Bit 2 = Plane 2 write-disabling failed.
- Bit 3 = Plane 3 write-disabling failed.

Test 24 – Graphics ALU Modes test

- Bit 0 = ALU Replace-mode failed.
- Bit 1 = ALU XOR-mode failed.
- Bit 2 = ALU OR-mode failed.
- Bit 3 = ALU AND-mode failed.

Test 25 – Graphics Data Shift test

- Bit 0 = Failed to shift ALU data 0 space left (no shift).
- Bit 1 = Failed to shift ALU data 1 space to left.
- Bit 2 = Failed to shift ALU data 2 spaces to left.
- Bit 3 = Failed to shift ALU data 3 spaces to left.
- Bit 4 = Failed to shift ALU data 0 space to right (no shift).
- Bit 5 = Failed to shift ALU data 1 space to right.
- Bit 6 = Failed to shift ALU data 2 spaces to right.
- Bit 7 = Failed to shift ALU data 3 spaces to right.

Test 26 – Dialog Handshake test

- Bit 0 = DISPRDY line stayed in not-ready condition after writing the Dialog Memory base address.
- Bit 1 = DISPRDY line stayed in not-ready condition after reading the Dialog Memory base address.

Test 27 – Dialog Memory test

Error code represents the 8K segment of dialog memory that failed, as follows:

- 1800 = Memory failure located between 18000 and 19FFF.

Test 28 – Dialog Character ROM test

The error code represents the address of the first byte in the ROM that had an error.

Test 29 – Graphics Index (0 thru 15) test

- Bit 0 = Graphics Index 0 failed.
- Bit 1 = Graphics Index 1 failed.
- Bit 2 = Graphics Index 2 failed.
- etc., through
- Bit 15 = Graphics Index 15 failed.

SELF TEST

Test 2A – Dialog Foreground Index test

- Bit 0 = Dialog foreground index 0 failed.
- Bit 1 = Dialog foreground index 1 failed.
- Bit 2 = Dialog foreground index 2 failed.
etc., through
- Bit 7 = Dialog foreground index 7 failed.

Test 2B – Dialog Background Index test

- Bit 0 = Dialog background index 1 failed.
- Bit 1 = Dialog background index 1 failed.
etc., through
- Bit 7 = Dialog background index 7 failed.

Test 2C – Dialog Cursor Index test

- Bit 0 = Dialog cursor foreground index failed.
- Bit 1 = Dialog cursor background index failed.

Test 2D – Graphics Cursor Index test

- Bit 0 = Graphics cursor foreground index failed.
- Bit 1 = Graphics cursor background index failed.

Test 2E – Retrace Blanking Index test

- Bit 0 = Blanking index failed.

Test 2F – Dialog Windowshade test

- Bit 0 = Top windowshade control failed.
- Bit 1 = Bottom windowshade control failed.

Test 30 – Dialog Transparent Control test

- Bit 0 = Dialog index 0 was not transparent with transparency enabled.
- Bit 1 = Dialog index 1 was transparent.
- Bit 2 = Dialog index 2 was transparent.
- Bit 3 = Dialog index 4 was transparent.
- Bit 4 = Dialog index 0 was transparent with transparency Disabled.

Test 31 – Dialog Blink Attribute test

- Bit 0 = With solid-block character, and character blink clock low, the dialog foreground index was not enabled.
- Bit 1 = With solid-block character, and character blink clock high, the dialog background index was not enabled.

Test 32 – Dialog Underline Attribute test

- Bit 0 = The underline row (14th row in character cell) was enabled in a line of space-characters, with the underline attribute disabled.
- Bit 1 = The underline row was not enabled in a line of space-characters, with the underline attribute enabled.

Test 33 – Display DISPINT test

- Bit 0 = Enabling a vertical sync interrupt did not create a processor interrupt.
- Bit 1 = A processor interrupt occurred after disabling the vertical sync interrupt.

ADJUSTMENT PROCEDURE ERROR CODES

The following error codes are only displayed while running the Adjustment part of Self Test. The explanation of these codes follows the same format as used to describe the main codes (preceding discussion). The test name, as printed on the display screen, appears first. Then, the error codes are listed and described for each test.

Host Port Test Error Codes

Test A1 – Host port transmit/receive test (external loopback)

- Bit 0 = TxRDYB not set after transmitting first character.
- Bit 1 = TxRDYB set after transmitting second character.
- Bit 2 = TxEMPTB, RxRDYB, and/or FFULLB was set before the first character was finished transmitting.
- Bit 3 = RxRDYB not set or FFULLB set after first character finished transmission.
- Bit 4 = TxRDYB, RxRDYB, and/or FFULLB not set after waiting for third character.
- Bit 5 = TxEMTB not set after fourth character finishes transmission.
- Bit 6 = First character received is not 00 (H).
- Bit 7 = Second character received is not 0FF (H).
- Bit 8 = Third character received is not 55 (H).
- Bit 9 = Fourth character received is not 0AA (H).

Test A2 – Host Port Baud Rates test (with external loopback)

The bits tell which tests failed.

- Bit 0 = 19.2 Kbaud
- Bit 1 = 9600 Baud
- Bit 2 = 4800 Baud
- Bit 3 = 2400 Baud
- Bit 4 = 1800 Baud
- Bit 5 = 1200 Baud

Bit 6 = 600 Baud

Bit 7 = 300 Baud

Bit 8 = 150 Baud

Bit 9 = 110 Baud

Test A3 – RTS and CTS test

- Bit 0 = CTS not high, or Delta CTS bit not set, after setting RTS high.
- Bit 1 = Delta CTS bit not cleared by reading the Input Port.
- Bit 2 = CTS not low, or Delta CTS not set, after setting RTS low.

Test A4 – DTR and DSR test

- Bit 0 = DSR not high, or Delta DSR bit not set, after setting DTR high with OP2 = low, OP5 = low, and OP6 = low.
- Bit 1 = Delta DSR bit not cleared by reading the Input Port.
- Bit 2 = DSR not low, or Delta DSR bit not set, after setting DTR low with OP2 = low, OP5 = low, and OP6 = high.
- Bit 3 = DSR not high after setting DTR high with OP2 = high, OP5 = high, and OP6 = high.
- Bit 4 = DSR not low, after setting DTR low with OP2 = low, OP5 = high, and OP6 = high.
- Bit 5 = DSR not low, after setting DTR low with OP2 = high, OP5 = low, and OP6 = high.

Test A5 – SRTS, DCD, and SDCD test

- Bit 0 = DCD not high, or Delta DCD not set, after setting SRTS high.
- Bit 1 = SDCD not high, or Delta SDCD not set, after setting SRTS high.
- Bit 2 = Delta DCD, or Delta SDCD, not cleared by reading the input port.
- Bit 3 = DCD not low, or Delta DCD not set, after setting SRTS low.
- Bit 4 = SDCD not low, or Delta SDCD not set, after setting SRTS low.

SELF TEST

Peripheral Port 0 Tests

Test A1 – Port 0 Baud Rates test (external loopback)

Same error codes as for Test A2, Host Port Baud Rates test.

(Bit 0 = 19.2 Kbaud, thru Bit 9 = 110 Baud.)

Test A2 – Port 0 Status Lines test

Bit 0 = RTS not high, or Delta RTS not set, when driven high by Host RTS.

Bit 1 = Delta RTS not cleared by reading input port.

Bit 2 = RTS not low, or Delta RTS not set, when driven low by Host RTS.

Bit 3 = DTR not high, or Delta DTR not set, when driven high by Host DTR.

Bit 4 = Delta DTR not cleared by reading Input Port.

Bit 5 = DTR not low, or Delta DTR not set, when driven low by Host DTR.

Bit 6 = SRTS not set high when driven high by SRTS from host.

Bit 7 = SRTS not set low when driven low by SRTS from host.

Test A3 – Port 0 Control Lines test

Bit 0 = Host CTS not driven high by a high on Port CTS.

Bit 1 = Host CTS not driven low by a low on Port CTS.

Bit 3 = Host DSR not driven high by a high on port DSR.

Bit 4 = Host DSR not driven low by a low on port DSR.

Bit 5 = Host DCD not driven high by a high on port DCD.

Bit 6 = Host DCD not driven low by a low on port DCD.

Peripheral Port 1 Tests

These tests and error codes (for Peripheral Port 1) are identical to those for Port 0. The only exception is that the screen message says "Port 1 Test" (instead of "Port 0 Test").

Hard Copy Loopback Test

This error message deals with the 4107's Printer port.

Test A1 – Hard Copy Loopback test

Bit 0 = Data or status bit failure on Hard Copy port.

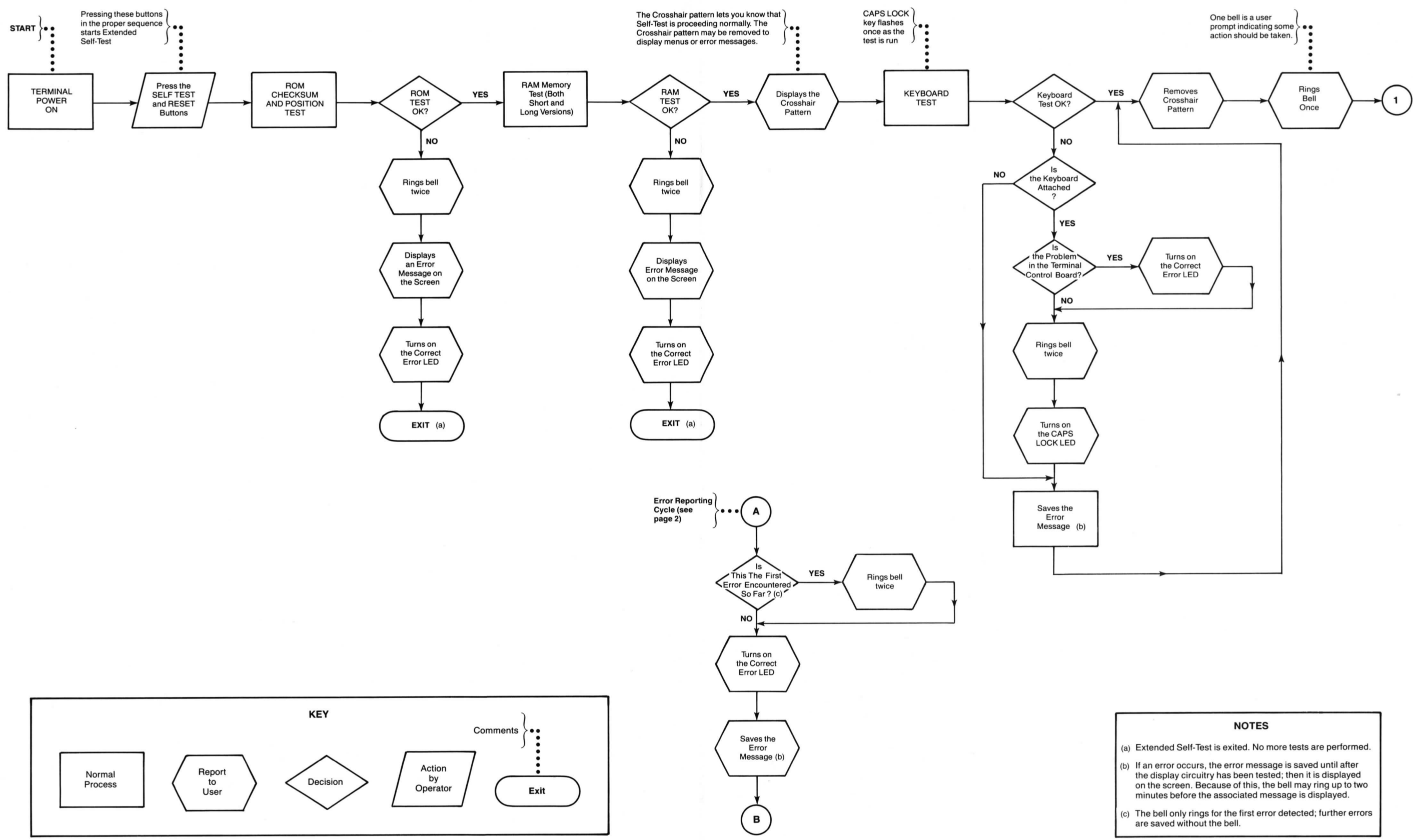


Figure C-5A. Self Test Control Flow.

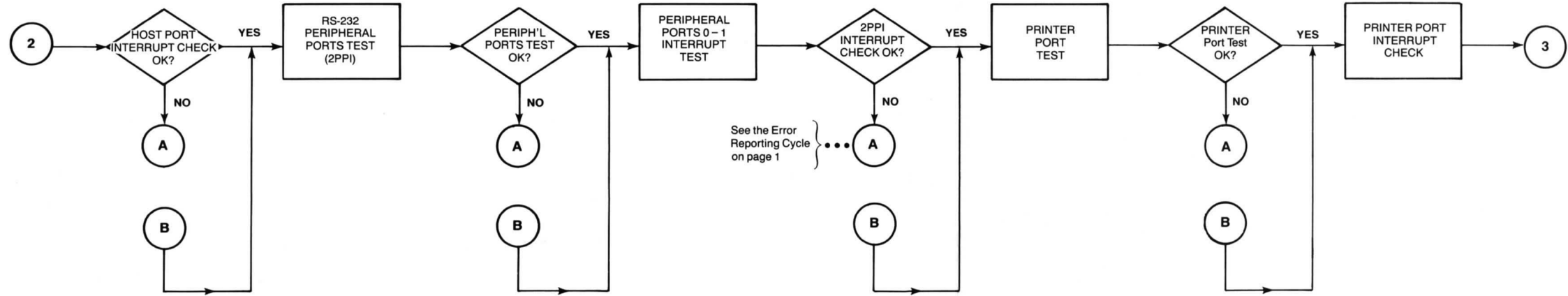
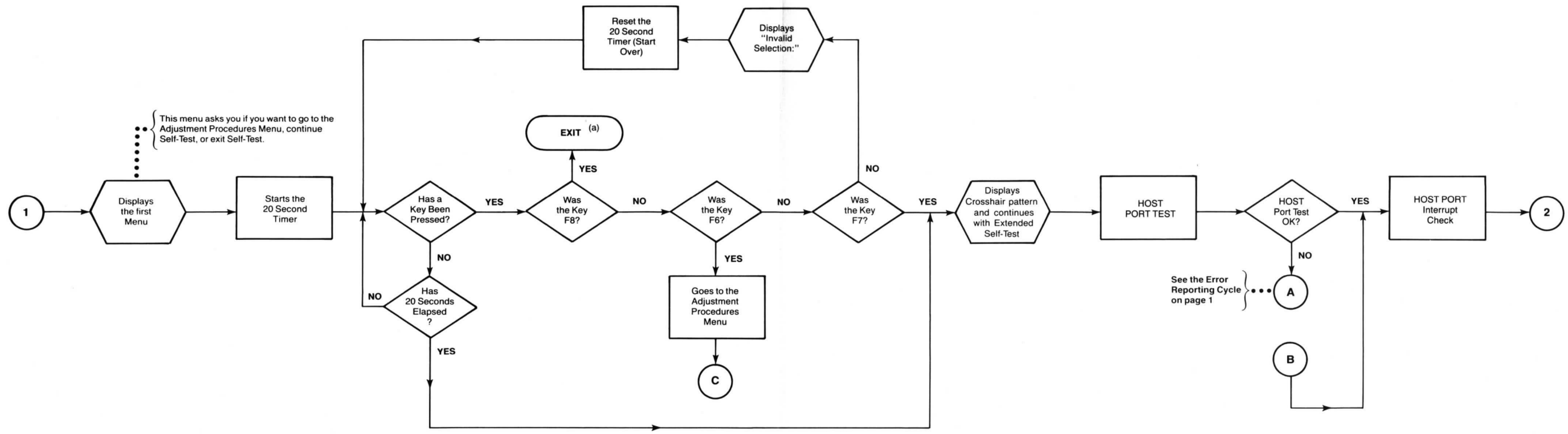


FIGURE C-5B
SELF-TEST CONTROL FLOW

Figure C-5B. Self Test Control Flow.

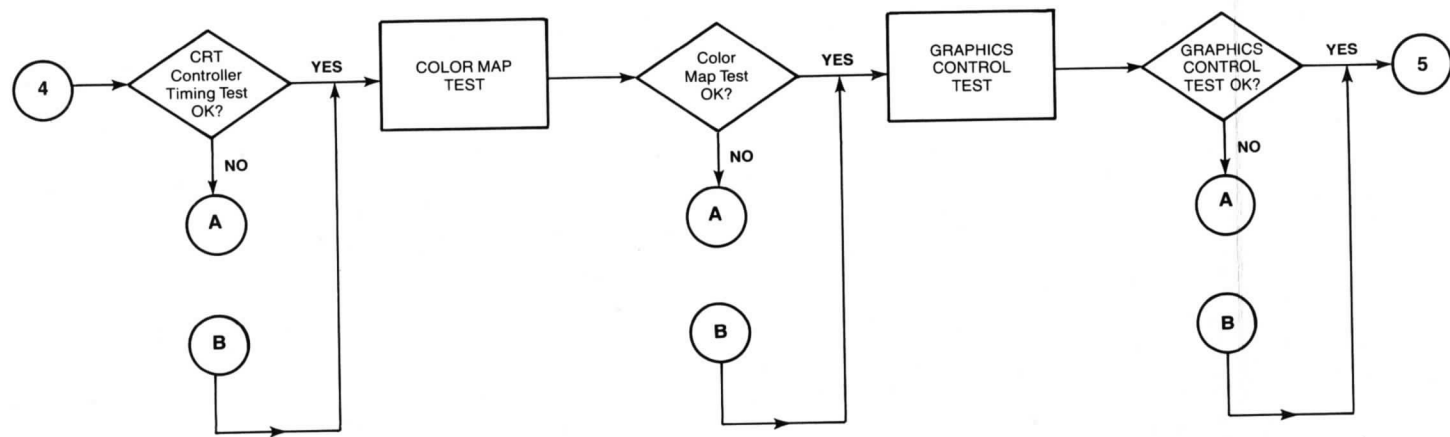
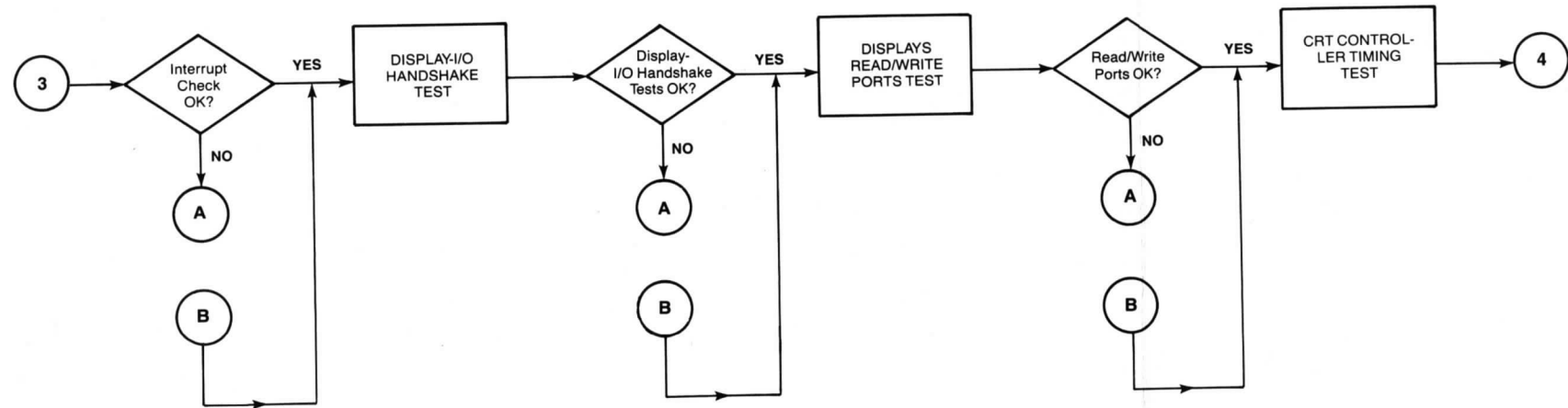
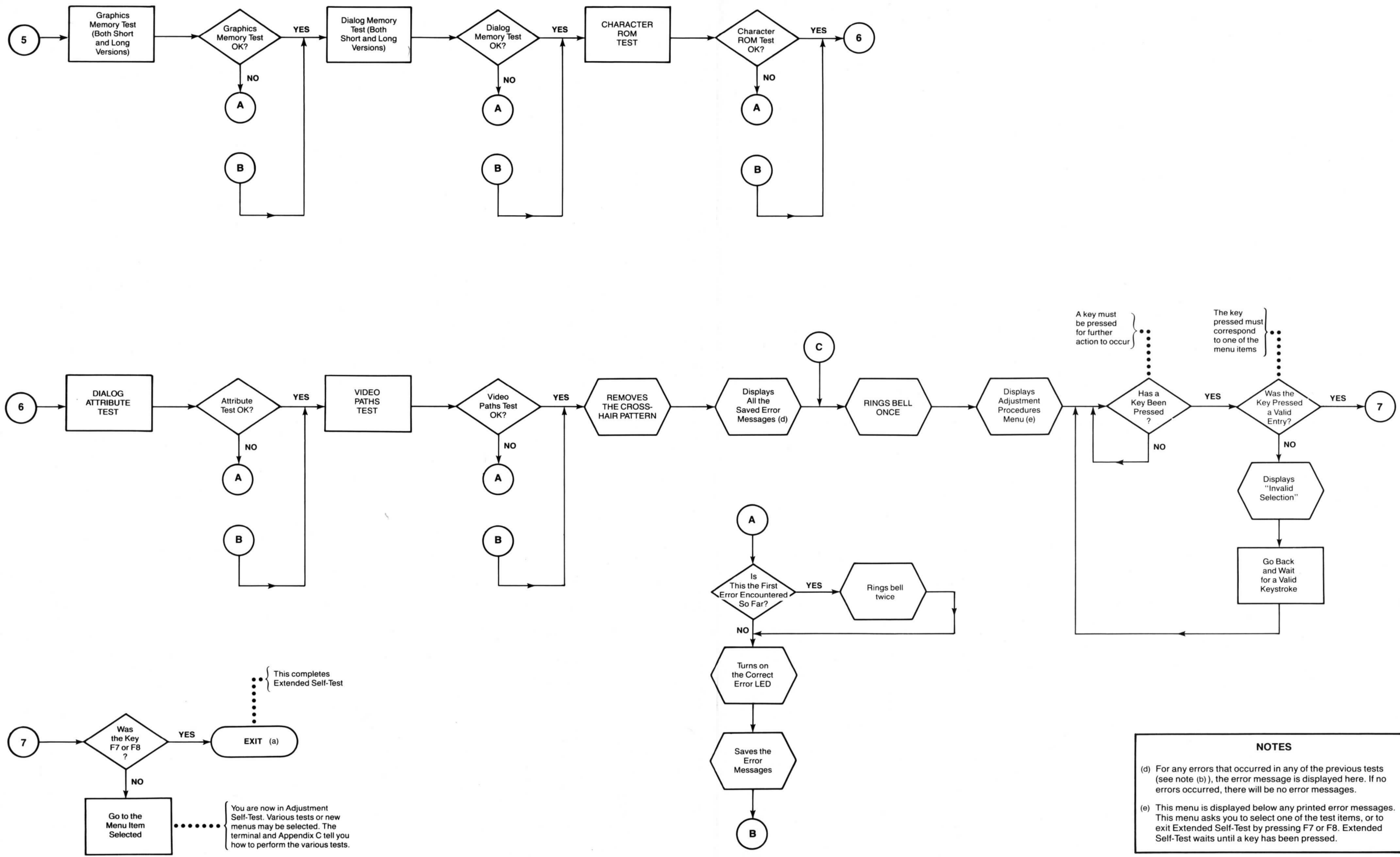


Figure C-5C. Self Test Control Flow.



NOTES

(d) For any errors that occurred in any of the previous tests (see note (b)), the error message is displayed here. If no errors occurred, there will be no error messages.

(e) This menu is displayed below any printed error messages. This menu asks you to select one of the test items, or to exit Extended Self-Test by pressing F7 or F8. Extended Self-Test waits until a key has been pressed.

Figure C-5D. Self Test Control Flow.

FIGURE C-5D
SELF TEST CONTROL FLOW

Appendix D

4107 SIGNAL LIST

The following table contains a list of all signals that appear on the edges of the schematic sheets in Section 11. The number in parenthesis (immediately following a signal name) is the number of the times that signal appears on the schematics. The right column contains a short definition/description of each signal.

Table D-1
SIGNAL NAMES

Name	Definition
+ 21 VOLTS	Required to read or write the 2817 EEPROMs.
+ 21 VOLT CONTROL	Same as 21 VOLTSON-0.
+ 5V LIMITED	+ 5 volts supplied for device at Copier port.
21 VOLTSON-0	Turns on the + 21 V supply for 2817 read or write.
2817CS-0	2817 chip select line.
2817RDY-1	Indicates to the processor that the 2817 is ready for a read or a write.
4109-0	Tells DCB that it is installed in a 4109.
5V ON-1	Confirms that the + 5V supply is working; and sends + 5V to Display Module.
9007CS-0	9007 dialog controller chip select — enabled so the 80186 may set this controller's internal registers.
A0-1 to A13-1, A9-1	Latched processor address lines.
ABUSY-0	Alpha controller busy, status line.
ACK-0	Acknowledge — input from copier port.
ACNTLRD-0	Alpha controller read enable.
ACNTLWR-0	Alpha controller write enable.
AD0-1 to AD15-1	Address/Data bus — multiplexed processor address and data bus.
ADREN-0	Enable line for 9007 I/O address buffer.
AHIWR-0	Dialog List RAM high bank write strobe.
ALE-1	Address Latch Enable — processor externally latches an address via this enable line.

Table D-1 (cont)
SIGNAL NAMES

Name	Definition
ALOWR-0	Dialog List RAM low bank write strobe.
ALPHACS-0	Alpha Chip Select — enables a data transfer between the processor data bus and the DCB dialog data bus.
ALPREQ-1	Alpha System Request — caused by VIDIO or ALPHACS.
ALU0-1 to ALU2-1	ALU Mode select lines.
ALUD0-1 to ALUD3-1	ALU Data — to RAM data write buffers on DCB.
APAGE0-1 to APAGE2-1	Alpha Font Selector — Selects one of three fonts in the Font ROM (default is 0).
ARAMWR-0	Alpha Memory (RAM) write strobe.
ARDY-1	Asynchronous Ready — a processor input from an addressed device; indicates its need for wait state(s).
ATTRTEST-1	Attribute PAL test line.
BG0-1 to BG2-1	Background — indicates the background color index.
BG0D-1 to BG2D-1	Background Delayed — delays the background color index by 1 dot-clock cycle.
BHE-0	Byte High Enable — this processor input selects either a word transfer or a byte transfer (on the upper half of the data bus).
BLA0-1 to BLA17-1 ^a	Latched address lines 0 through 17.
BLANK-0 ^a	Blanking signal to the Display Module.
BLBHE-0 ^a	Latched Byte High Enable (see BHE-0).
BLD0-1 to BLD12-1 ^a	Latched data lines 1 through 12.
BLERCY-0 ^a	Latched Early Write Cycle.
BLINKENB-1 ^a	Blink Enable — enables blink attributes for dialog characters.
BLOCKCUR-1 ^a	Dialog area rectangular block cursor enable line.
BLPAGE1-0 ^a	Latched "page 1" memory bank enable signal.

^a "BL" refers to Big Latch (I/O between DCB and TCB busses).

SIGNAL LIST

Table D-1 (cont)
SIGNAL NAMES

Name	Definition
BLWRCY-1 (-0) ^a	Latched Write Cycle — indicates the processor is doing an I/O write to DCB.
BRD-0	Buffered Read — processor read command buffered.
BRW-1	Buffered Read/Write — indicates a read or write by the processor.
BUSY-1	Busy — input from Copier port.
BWR-0	Buffered Write — processor write command (buffered).
C0-1 to C7-1	Character Code — represents the current character in the lower byte of the dialog list character word.
CAS0-0 to CAS3-0	Column Address Strobe 0 thru 3 — multiplexed CAS signals to graphics RAMs.
CBLANK-1	Composite Blanking request (from 9007) — provides blanking for retrace.
CCLK-0	Character Clock — clocks the dialog RAM output pipeline.
CHARBG-0	Character Background — background image enable.
CHARBLNKCLK-1	Character Blink Clock.
CHARFG-0	Character Foreground — foreground image enable.
CLKOUT-1	Clock Out — clock output from processor, is half the frequency of the system clock.
CLKTST-1	Clock Test — test input to DCB timing generator.
CLRPIX-0	Clears the pixel output latches.
COMPOSITE BLANK-1	Composite Blanking signal (V and H) to the Display Module.
COMPOSITE SYNC-0	Composite Sync (V and H) signal to the Display Module.
CSYNC-0	Composite Sync Request — from 9007 to Display Module.
CTS	Clear-to-Send — RS-232 signal from host (see RS-232 specifications).
CTSA	Clear-to-Send Channel A — Port 0 CTS signal.

^a "BL" refers to Big Latch (I/O between DCB and TCB busses).

Table D-1 (cont)
SIGNAL NAMES

Name	Definition
CTSB	Clear-to-Send Channel B — Port 1 CTS signal.
CURBLKCLK-1	Alpha Cursor Blink Clock.
CURS-1	Alpha Cursor — cursor request signal from 9007.
D0-1 to D15-1	Data Bus lines on TCB.
DATA0 RETURN to DATA7 RETURN	Data Return — ground lines for Copier port data.
DCD (J22)	Data Carrier Direct — Host port RS-232 signal.
DCDA	DCD channel A — Port 0, DCD RS-232 signal.
DCDB	DCD channel B — Port 1, DCD RS-232 signal.
DCLK	Dot Clock — pixel rate clock signal.
DEN-0	Data Enable — processor output to indicate valid data on the bus.
DIALOGENB-0	Dialog display enable signal.
DISPINT-1	Display Interrupt — interrupt from 9007 controller to the processor.
DISPRDY-1	Display Ready — indicates to the processor whether or not the DCB is ready to receive a data transfer.
DOTCLK0-0 to DOTCLK5-0	Dot Clocks — six clocks that run at pixel rate, with varying phases.
DRQ1-1	DMA Request — to processor from test connector.
DRB-0	Data Row Boundary — indicates the top raster line of a character row/cell on the screen.
DSRA	Data Set Ready (channel A) — RS-232 signal from peripheral Port 0.
DSRB	Data Set Ready (channel B) — RS-232 signal from peripheral Port 1.
DT-1	Data Transmit — indicates the data flow direction on the processor data bus.
DTR	Data Terminal Ready — RS-232 host signal.
DTRA	DTR (channel A) — RS-232 peripheral Port 0 signal.

Table D-1 (cont)
SIGNAL NAMES

Name	Definition
DTRB	DTR (channel B) — RS-232 peripheral Port 1 signal.
ENBPIPE-0	Enable Pipeline — clocks the Dialog List row buffer (and pipeline) output.
EOLLOCK-1	End-of-Line Lock — controls the character output pipeline.
FAULT-0	Fault — error from fault indicator on copier/printer (on Copier port input).
FG0-1 to FG2-1	Foreground 0 to 2 — color index for the foreground of the display dialog area.
FONT0-1 to FONT7-1	Outputs from the character font ROM.
FONTRD-1	Read enable for the Self Test Font Read Latch.
G0-0 to G1-0	Graphics memory Output Enables — G0 enables high bank; G1 enables low bank.
GA0-1 to GA7-1	Graphics Memory Address lines.
GBUSY-0	Graphics front control PAL is busy (status line).
GCNTRD-0	Graphics Control Read Enable.
GCNTLWR-0	Graphics Control Write Enable.
GLOAD-1 (-0)	Graphics Load — for X Position latch, and Graphics Shift Registers.
GRAMWR-0	Graphics Memory Write Command.
GRAPHCS-0	Chip Select for Graphics RAM front control PAL.
GRFREQ-0	Graphics Request — a read from 40000 — 7FFFF, or a write to 40000 — BFFFF, translates into this request for graphics controller operation.
GSRD0-1 to GSRD3-1	Graphics Shift Register data outputs.
GSYNC-1	Graphics Sync — timing signal from X Position counter.
GX0-1 to GX9-1	Graphics Cursor X Position address.
GY0-1 to GY8-1	Graphics Cursor Y Position address.
HCLK-0	Horizontal Clock — from timing generator.

Table D-1 (cont)
SIGNAL NAMES

Name	Definition
HIWR-0	High Write Enable — write enable for High Byte; this is the upper byte (D8 — D15) of the processor word.
HLDA-1	Hold Acknowledge — acknowledge availability of the bus following a HOLD bus request.
HOLD-0	Hold — input from test connector and from Display Control board requesting use of the processor bus.
HOSTDAV-1	Host Data Available — signal from the host port, requests processor DMA cycle.
HS-0	Horizontal Sync — used to reset the NOTEXT register.
HWSTB-0	Hardware Strobe — strobes the registers (hardware) on the DCB.
INPUT PRIME RETURN	Input Prime Return — ground return for INPUT PRIME-0.
INPUT PRIME-0	Input Prime — output from Copier port.
INT0-1 to INT3-1	Interrupts 0 to 3 — four separate processor interrupt request inputs.
INTERLACE-1	Requests interlaced mode from DCB timing generator.
KBGND	Keyboard Ground — ground line for keyboard.
KBRDATA-1	Keyboard Receive Data — data to keyboard from processor.
KBRESET-0	Keyboard Reset — resets and tests the keyboard (runs that part of Self Test).
KBTDATA-1	Keyboard Transmit Data — data and/or status from the keyboard to the processor.
KBVCC	Keyboard Power Supply Voltage — + 12 VDC (regulated down to + 5 VDC in the keyboard).
LATERW-0	Late Read/Write — delayed read or write control.
LCS-0	Lower Chip Select — this processor line selects chips in the lower address area.
LGSR-0	Load Graphics Shift Register.
LISTENB-0	List Enable — enables dialog list data to become video data.

SIGNAL LIST

**Table D-1 (cont)
SIGNAL NAMES**

Name	Definition
LOCK-0	Lock — indication by processor that other devices may not access the bus.
LOWR-0	Low Write Enable — allows only the low byte (B0–B7) to be written.
LRAMRDDAT-0	Latched RAM read data.
LS0-0 to LS2-0	Latched Status 0 to 2 — causes status bits 0 to 2 to be latched by the processor.
MAP0-1 to MAP4-1	Color Map address lines.
MAP4-0	Color Map Address line-4.
MAPIO-0	Color Map I/O — control line from “alpha system I/O control”.
MAPWR-0	Map Write — write enable to the Color Map.
MCS0-0 to MCS3-0	Middle Chip Select — chip select lines from the processor.
MDEN-0	Manual Data Enable — not used; may be used to control data on bus from a test fixture.
MEM-1	Memory Access — request line from processor to Proc/Display arbitration PAL.
MISCOMINT-1	Miscellaneous Communications Interrupt — an interrupt request from the DUART to the processor.
NAME	DEFINITION
NMI-0	Non-maskable inter causes it to perform an interrupt routine.
ODD-1	Odd condition — for double-wide characters.
P0-1 to P63-1	Pixel data bus — from RAMs to Graphics Shift Registers.
PCS0-0 to PCS6-0	Port Chip Select — indicates which 128 byte section of I/O space has been selected.
PE-1	Printer Enable — printer acknowledges it is enabled.
PIPECBLANK-1	Pipelined composite blanking signal.
PIPEDRB-0	Pipelined Data Row Boundery — piped DRB signal from the Alpha Controller.

**Table D-1 (cont)
SIGNAL NAMES**

Name	Definition
PIPEHS-0	Pipelined Horizontal Sync signal.
PIPEVS-0	Pipelined Vertical Sync signal.
PLSTENB-0	Pipeline Strobe Enable — enables double-wide character PAL.
PRINTERINT-1	Printer Interrupt — interrupt output from processor to Printer Port.
PROCESSOR-0	Allows processor to write to graphics memories (via MUX).
QS0-1 and QS3-1	Queue Status — status outputs from processor.
QSMD-0	Queue Status Mode Disable (to processor).
RAMCS0-0 to RAMCS3-0	RAM Chip Select — processor memory (RAM) chip select.
RAMD0-1 to RAMD3-1	RAM Data — Graphics RAM data from RAM chips to processor.
RAMRDCLK-0	RAM Read Clock — for Graphics RAM chips.
RAMRDY-1	RAM Ready — RAMs send ready signal to processor.
RAS0-0 to RAS3-0	Row Address Strobe A to D — Row address strobelines for graphics memory.
RC	Receive Clock — RS-232 standard.
RD-0/QSMD-0	Selects Read or Queue Status Mode for processor.
RDATA (J22)	Receive Data — RS-232 data to terminal.
RDYAND-1	Ready AND — test connector input ANDed with the terminal's internal ready signal.
RDYOR-0	Ready OR — test connector input ORed with the terminal's internal ready signal.
RENB-0	Refresh Enable — refreshes the Dialog List RAMs.
RESET-0	Reset — signal from the Reset switch.
RESET	Reset — an input to the processor.
RESETOUT-1	Reset Out — reset signal from the processor to the rest of the system.
RTS (J22)	Request to Send — RS-232 signal, host port.

Table D-1 (cont)

SIGNAL NAMES

Name	Definition
RTSA (J20)	Request to Send — peripheral port 0 RS-232 signal.
RTSB (J23)	Request to Send — peripheral port 1 RS-232 signal.
SDCD (J22)	Secondary Data Carrier Detect — RS-232 signal.
SELECT-1	Select — signal from printer port to processor.
SHIFT0-1 to SHIFT3-1	Shift mode selector — Shifts processor/RAM data to ALU (via Shift PAL).
SL0-1 to SL3-1	Scan Line 0 to 3 — binary count for character generator; character line information from alpha CRT controller.
SMRESET-0	System Reset — processor reset to Display Control board.
SRDY-1	Synchronous Ready — processor input.
SRMODE0-0	Shift Register Mode 0 select line.
SRMODE1-0	Shift Register Mode 1 select line.
SRTS (J22)	Secondary Request to Send — RS-232 host signal.
SRTSA (J20)	Secondary Request to Send — RS-232 port 0 signal.
SRTSB (J23)	Secondary Request to Send — RS-232 port 1 signal.
STB RETURN	Standby Ground Return — ground for standby signal to printer (from printer port).
STB-0	Standby — standby signal from processor to printer.
STCLK-0	Self Test Clock signal.
STEST-0	Self Test — from Self test switch (unbuffered and unlatched).
STOPPIX-1	Stop Pixels — disables the Pixel Output-to-Display latches.
SYSRES-0	System Reset — same as SYSRESET, but originating on the Display Control board.
SYSRESET-0 and SYSRESET-1	System Reset — these complementart outputs are controlled by the processor.

Table D-1 (cont)

SIGNAL NAMES

Name	Definition
TBWIN-0	Top/Bottom Window Shade — dialog window shade enable.
TC (J22)	Transmit Clock — RS-232 signal.
TDATA (J22)	Transmit Data — RS-232 signal.
TERMCLK-1	Terminal Clock — main clock, from keyboard port oscillator.
TESTCS-0	Test Chip Select — outputs the test results from system memory decoder (custom gate array).
TESTNMI-0	Test Non-Maskable Interrupt — an input from the test connector that allows manual or external NMI.
TESTRD-0	Test Read — allows data read via test connector.
TMRIN0-1 and TMRIN1-1	Timer In — these inputs control the processor's timer outputs.
TMROUT0-1 and TMROUT1-1	Timer Out — output signals from the processor's timers.
TSC-0	Tri-State Control — from processor to alpha CRT controller.
UCS-0	Upper Chip Select — processor line selects chip in upper address area.
UNDERLINE-1	Unerline — indicates that a character is to be underlined.
VA0-1	Video Address 0 — represents the address of the first pixel in the dialog area.
VCLK-1	Vertical Clock — from DCB timing generator.
VD0-1 to VD7-1	Video Data 0 to 7 — latched list data for display.
VIDIO-0	Video Input/Output — this processor output is the master control line for all I/O between the terminal Control board and the Display Control board.
VIDOFF-1	Video Off — turns off the video Display Module.
VLT-0	Visible Line Time — indicates the visible portion of the scan line.

SIGNAL LIST

Table D-1 (cont)

SIGNAL NAMES

Name	Definition
VRESET-0	Video system Reset — from processor to Display Control board.
VS-0	Vertical Sync — vertical sync signal from the alpha CRT controller.
WEHI-0	Write Enable for High RAM on RAM3 board.
WELO-0	Write Enable for Low RAMs on RAM3 board.
WINCLK-1	Dialog Window-Shade Clock.
WR-0/QS1-1	Write (or Queue Status) signal from the processor to the system.
WR0-0	Write High RAM Bank — p/o bit map on DCB.
WR1-0	Write Low RAM Bank — p/o bit map on DCB.
WRBOTH-1	Enable write to both banks of DCB bit map RAM.
WRCY-0	Write Cycle — indicates that the processor is performing an I/O write.
WRDIS0-1 to WRDIS3-1	Write Disable lines — prevents ALU from operating on all but selected graphics data lines.
XCUR-0	X Cursor signal — part of crosshair cursor.
XHAIR-1	Crosshair — cursor enable signal.
XPOS-0	X-Position counter clock pulse.
XPRNTENB-1	Transparent Mode Enable — request to pixel decoder PAL.
YCUR-0	Y Cursor signal — part of crosshair cursor.
YDCGY0-1	Y Down-Counter for Graphics Y Position.
YEP3-0	"Yes, the RAM3 board is installed."
YPOS-0	Y-Position counter clock pulse.

Appendix E

ASCII CHARTS

This appendix includes the standard ASCII code chart and additional ASCII code charts which define the specific characters used as parameters.

The code charts are:

NOTE
ASCII stands for "American Standard Code for Information Interchange."

Table	Description
E-1	ASCII Standard Code Chart
E-2	United Kingdom Character Set
E-3	French Character Set
E-4	Swedish Character Set
E-5	Danish/Norwegian Character Set
E-6	German Character Set
E-7	Supplementary Character Set
E-8	Rulings Character Set

Table E-1
ASCII STANDARD CODE CHART

BITS				CONTROL		FIGURES		UPPERCASE		LOWERCASE		
B7	B6	B5	B4	B3	B2	B1						
0	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	1	0	1	0	0	1	0	1	0	
0	0	1	0	0	1	1	0	0	1	0	1	
0	0	1	1	0	0	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	0	0	0	0	
0	1	0	0	1	0	0	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	0	0	0	0	0	0	0	
1	0	1	0	0	0	0	0	0	0	0	0	
1	0	1	1	0	0	0	0	0	0	0	0	
1	1	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	1	0	0	0	0	0	0	0	
1	1	1	0	0	0	0	0	0	0	0	0	
1	1	1	1	0	0	0	0	0	0	0	0	
1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	1	1	1	0	0	0	0	0	0	
					NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
					SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
					SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
					EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
					ET ₄	D4 ₂₀	\$ ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
					EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
					AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
					BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
					BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
					HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
					LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
					VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	[₉₁	k ₁₀₇	{ ₁₂₃
					FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	\ ₉₂	l ₁₀₈	₁₂₄
					CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇] ₉₃	m ₁₀₉	} ₁₂₅
					SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	~ ₁₂₆
					SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	_ ₉₅	o ₁₁₁	DT ₁₂₇

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Table E-2
UNITED KINGDOM CHARACTER SET

BITS				0 0		0 1		1 0		1 1	
B7	B6	B5		CONTROL		FIGURES		UPPERCASE		LOWERCASE	
B4	B3	B2	B1								
0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
0	0	0	1	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
0	0	1	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
0	0	1	1	EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
0	1	0	0	ET ₄	D4 ₂₀	£ ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
0	1	0	1	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
0	1	1	0	AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
0	1	1	1	BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
1	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
1	0	0	1	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
1	0	1	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
1	0	1	1	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	[₉₁	k ₁₀₇	{ ₁₂₃
1	1	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	\ ₉₂	l ₁₀₈	₁₂₄
1	1	0	1	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇] ₉₃	m ₁₀₉	} ₁₂₅
1	1	1	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	— ₁₂₆
1	1	1	1	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	_ ₉₅	o ₁₁₁	DT ₁₂₇

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Table E-3
FRENCH CHARACTER SET

BITS				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
B7	B6	B5		CONTROL		FIGURES		UPPERCASE		LOWERCASE	
B4	B3	B2	B1								
0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
0	0	0	1	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
0	0	1	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
0	0	1	1	EX ₃	D3 ₁₉	£ ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
0	1	0	0	ET ₄	D4 ₂₀	\$ ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
0	1	0	1	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
0	1	1	0	AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
0	1	1	1	BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
1	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
1	0	0	1	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
1	0	1	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
1	0	1	1	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	° ₉₁	k ₁₀₇	é ₁₂₃
1	1	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	ç ₉₂	l ₁₀₈	ù ₁₂₄
1	1	0	1	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇	§ ₉₃	m ₁₀₉	è ₁₂₅
1	1	1	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	'' ₁₂₆
1	1	1	1	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	— ₉₅	o ₁₁₁	D _T ₁₂₇

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Table E-4
SWEDISH CHARACTER SET

BITS				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
B7	B6	B5		CONTROL		FIGURES		UPPERCASE		LOWERCASE	
B4	B3	B2	B1								
0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
0	0	0	1	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
0	0	1	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
0	0	1	1	EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
0	1	0	0	ET ₄	D4 ₂₀	α ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
0	1	0	1	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
0	1	1	0	AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
0	1	1	1	BL ₇	EB ₂₃	' ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
1	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
1	0	0	1	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
1	0	1	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
1	0	1	1	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	Ä ₉₁	k ₁₀₇	ä ₁₂₃
1	1	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	Ö ₉₂	l ₁₀₈	ö ₁₂₄
1	1	0	1	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇	Å ₉₃	m ₁₀₉	å ₁₂₅
1	1	1	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	- ₁₂₆
1	1	1	1	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	_ ₉₅	o ₁₁₁	D _T ₁₂₇

(4526)4893-24

Table E-5
DANISH/NORWEGIAN CHARACTER SET

BITS				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
B7	B6	B5		CONTROL		FIGURES		UPPERCASE		LOWERCASE	
B4	B3	B2	B1								
0	0	0	0	NJ ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
0	0	0	1	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
0	0	1	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
0	0	1	1	EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
0	1	0	0	ET ₄	D4 ₂₀	\$ ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
0	1	0	1	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
0	1	1	0	AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
0	1	1	1	BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
1	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
1	0	0	1	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
1	0	1	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
1	0	1	1	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	Æ ₉₁	k ₁₀₇	æ ₁₂₃
1	1	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	Ø ₉₂	l ₁₀₈	ø ₁₂₄
1	1	0	1	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇	Å ₉₃	m ₁₀₉	å ₁₂₅
1	1	1	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	— ₁₂₆
1	1	1	1	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	— ₉₅	o ₁₁₁	D _T ₁₂₇

(4526)4893-26

Table E-6
GERMAN CHARACTER SET

BITS				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
B7	B6	B5		CONTROL		FIGURES		UPPERCASE		LOWERCASE	
B4	B3	B2	B1								
0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	§ ₆₄	P ₈₀	\ ₉₆	p ₁₁₂
0	0	0	1	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	a ₉₇	q ₁₁₃
0	0	1	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	b ₉₈	r ₁₁₄
0	0	1	1	EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	c ₉₉	s ₁₁₅
0	1	0	0	ET ₄	D4 ₂₀	\$ ₃₆	4 ₅₂	D ₆₈	T ₈₄	d ₁₀₀	t ₁₁₆
0	1	0	1	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	e ₁₀₁	u ₁₁₇
0	1	1	0	AK ₆	Sy ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	f ₁₀₂	v ₁₁₈
0	1	1	1	BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	g ₁₀₃	w ₁₁₉
1	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	h ₁₀₄	x ₁₂₀
1	0	0	1	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	i ₁₀₅	y ₁₂₁
1	0	1	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀	j ₁₀₆	z ₁₂₂
1	0	1	1	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	Ä ₉₁	k ₁₀₇	ä ₁₂₃
1	1	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	Ö ₉₂	l ₁₀₈	ö ₁₂₄
1	1	0	1	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇	Ü ₉₃	m ₁₀₉	ü ₁₂₅
1	1	1	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄	n ₁₁₀	ß ₁₂₆
1	1	1	1	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉	— ₉₅	o ₁₁₁	D _T ₁₂₇






































































































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Table E-7
SUPPLEMENTARY CHARACTER SET

BITS				0 0		0 1		1 0		1 1					
B7	B6	B5	B4	B3	B2	B1	CONTROL		FIGURES		UPPERCASE		LOWERCASE		
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1
0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	— ₆₄	Ñ ₈₀	◆ ₉₆	☐ ₁₁₂				
0	0	0	1	SH ₁	D1 ₁₇	Ä ₃₃	1 ₄₉	¢ ₆₅	ñ ₈₁	■ ₉₇	☐ ₁₁₃				
0	0	1	0	SX ₂	D2 ₁₈	ä ₃₄	2 ₅₀	₆₆	ı ₈₂	HT ₉₈	☐ ₁₁₄				
0	0	1	1	EX ₃	D3 ₁₉	Å ₃₅	3 ₅₁	† ₆₇	ı ₈₃	FF ₉₉	☐ ₁₁₅				
0	1	0	0	ET ₄	D4 ₂₀	å ₃₆	4 ₅₂	□ ₆₈	α ₈₄	CR ₁₀₀	☐ ₁₁₆				
0	1	0	1	EQ ₅	NK ₂₁	Æ ₃₇	5 ₅₃	■ ₆₉	σ ₈₅	LF ₁₀₁	☐ ₁₁₇				
0	1	1	0	AK ₆	SY ₂₂	æ ₃₈	6 ₅₄	● ₇₀	τ ₈₆	° ₁₀₂	☐ ₁₁₈				
0	1	1	1	BL ₇	EB ₂₃	à ₃₉	7 ₅₅	Δ ₇₁	ρ ₈₇	± ₁₀₃	☐ ₁₁₉				
1	0	0	0	BS ₈	CN ₂₄	ç ₄₀	8 ₅₆	δ ₇₂	μ ₈₈	NL ₁₀₄	☐ ₁₂₀				
1	0	0	1	HT ₉	EM ₂₅	é ₄₁	9 ₅₇	λ ₇₃	Σ ₈₉	VT ₁₀₅	≤ ₁₂₁				
1	0	1	0	LF ₁₀	SB ₂₆	è ₄₂	ù ₅₈	⌋ ₇₄	Ω ₉₀	☐ ₁₀₆	≥ ₁₂₂				
1	0	1	1	VT ₁₁	EC ₂₇	ö ₄₃	β ₅₉	L ₇₅	∫ ₉₁	☐ ₁₀₇	π ₁₂₃				
1	1	0	0	FF ₁₂	FS ₂₈	ö ₄₄	<0 ₆₀	⌈ ₇₆	∫ ₉₂	☐ ₁₀₈	≠ ₁₂₄				
1	1	0	1	CR ₁₃	GS ₂₉	φ ₄₅	α ₆₁	⌋ ₇₇	÷ ₉₃	☐ ₁₀₉	£ ₁₂₅				
1	1	1	0	SO ₁₄	RS ₃₀	ü ₄₆	§ ₆₂	⌋ ₇₈	≈ ₉₄	☐ ₁₁₀	• ₁₂₆				
1	1	1	1	SI ₁₅	US ₃₁	ü ₄₇	•• ₆₃	∞ ₇₉	⌈ ₉₅	☐ ₁₁₁	DT ₁₂₇				

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Table E-8
RULINGS CHARACTER SET

BITS				0 0		0 0 1		0 1 0		0 1 1		1 0 0		1 0 1		1 1 0		1 1 1				
B7	B6	B5	B4	B3	B2	B1	CONTROL				FIGURES				UPPERCASE				LOWERCASE			
0	0	0	0	0	0	0	NU ₀	DL ₁₆	Sp ₃₂	0 ₄₈	@ ₆₄	P ₈₀	◆ ₉₆									
0	0	0	0	1	0	0	SH ₁	D1 ₁₇	! ₃₃	1 ₄₉	A ₆₅	Q ₈₁	■ ₉₇									
0	0	1	0	0	0	0	SX ₂	D2 ₁₈	" ₃₄	2 ₅₀	B ₆₆	R ₈₂	HT ₉₈									
0	0	1	1	0	0	0	EX ₃	D3 ₁₉	# ₃₅	3 ₅₁	C ₆₇	S ₈₃	FF ₉₉									
0	1	0	0	0	0	0	ET ₄	D4 ₂₀	\$ ₃₆	4 ₅₂	D ₆₈	T ₈₄	CR ₁₀₀									
0	1	0	1	0	0	0	EQ ₅	NK ₂₁	% ₃₇	5 ₅₃	E ₆₉	U ₈₅	LF ₁₀₁									
0	1	1	0	0	0	0	AK ₆	SY ₂₂	& ₃₈	6 ₅₄	F ₇₀	V ₈₆	° ₁₀₂									
0	1	1	1	0	0	0	BL ₇	EB ₂₃	/ ₃₉	7 ₅₅	G ₇₁	W ₈₇	± ₁₀₃									
1	0	0	0	0	0	0	BS ₈	CN ₂₄	(₄₀	8 ₅₆	H ₇₂	X ₈₈	NL ₁₀₄									
1	0	0	1	0	0	0	HT ₉	EM ₂₅) ₄₁	9 ₅₇	I ₇₃	Y ₈₉	VT ₁₀₅									
1	0	1	0	0	0	0	LF ₁₀	SB ₂₆	* ₄₂	: ₅₈	J ₇₄	Z ₉₀										
1	0	1	1	0	0	0	VT ₁₁	EC ₂₇	+ ₄₃	; ₅₉	K ₇₅	[₉₁										
1	1	0	0	0	0	0	FF ₁₂	FS ₂₈	, ₄₄	< ₆₀	L ₇₆	\ ₉₂										
1	1	0	1	0	0	0	CR ₁₃	GS ₂₉	- ₄₅	= ₆₁	M ₇₇] ₉₃										
1	1	1	0	0	0	0	SO ₁₄	RS ₃₀	. ₄₆	> ₆₂	N ₇₈	^ ₉₄										
1	1	1	1	0	0	0	SI ₁₅	US ₃₁	/ ₄₇	? ₆₃	O ₇₉											

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