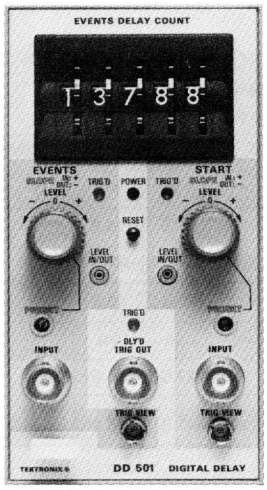
DD 501



Digital Delay

DD 501

- Digital Events Delay
- Delay to 99,999 Events
- Divide by N up to 20 MHz
- Pulse Counting to 65 MHz
- Time Delay with Ext Clock
- Compatible with Most Attenuator Probes

The DD 501 is an events count or count down plug-in unit. The unit counts a predetermined number of events, from 0 to 99,999, selected by the front-panel thumb-wheel switches. The DD 501 can also function as a frequency divider, or it can be used in a "counted burst' mode with pulse or function generators that can be synchronously gated. Tektronix generators capable of being gated by the DD 501 are the FG 501, FG 502, FG 504, and the PG 508.

EVENTS DELAY

Count — 1 to 99,999 events.
Max Count Rate — 65 MHz.
Insertion Delay — 30 ns or less from final event to trigger output pulse.
Recycle Time — 50 ns or less.
Reset — Manually resets delay counter.

INPUT CHARACTERISTICS

(All characteristics apply to both events and start inputs).
Input Impedance — 1 MΩ, 20 pF.
Slope — Either + or −, selectable.
Sensitivity — 85 mV p-p @ 30 MHz.
Frequency Response — Up to 65 MHz at 120 mV sensitivity.
Minimum Detectable Pulse Width — 5 ns.
Threshold Level Range — From −1.5 V to +1.5 V (−15 V to +15 V with 10X probe). Can be externally programmed or monitored at front panel jacks.
Trigger View Out — Threshold detector output, at least 0.5 V (200 Ω or less source impedance).
Events Triggered Light — Visual indication that events are being detected.
Start Triggered Light — Visual indication that delay is in progress.

TRIGGER OUTPUT

Pulse Width — Width of events pulse plus 6 ns or less.
Voltage Swing — + 0.8 V or less to at least + 2.0 V with 3 TTL loads (≃5 mA).
Light — Indicates output trigger.

GENERAL

Temperature — Operating: 0°C to +50°C. Non-operating: −40°C to +75°C.
Altitude — Operating: to 15,000 ft; Non-operating: to 50,000 ft.

Order DD 501 Digital Delay

DL 502

Digital Latch

DL 502

- 16 Channel Latching Capability
- Captures Glitches as Narrow as 5 ns at Probe Tips
- Allows Expansion of Information Time Frame
- TM 500 Compatibility

The TEKTRONIX DL 502 Digital Latch extends the logic analyzer's measurement capabilities. The Digital Latch aids in detecting narrow pulses in a data stream that cannot be captured by a logic analyzer alone. The 16 channel latch captures asynchronous glitches of less than one sample interval or as narrow as 5 ns.

In asynchronous measurements without latching capability, high speed data anomalies go undetected if they do not appear on a clock edge. The DL 502 Digital Latch captures the glitch and holds it until the next clock edge, then expands and displays it for one sample interval.

SPECIFICATIONS

Minimum pulse width to initiate latch — 5 ns.

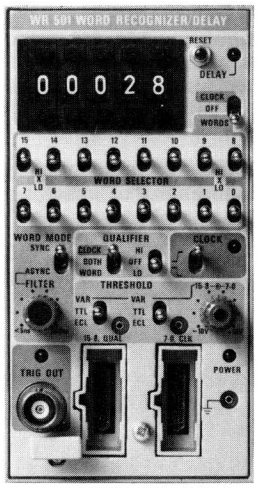
Minimum amplitude to initiate latch — 500 mV centered at threshold.

Minimum sample interval asynchronous clock — 50 ns.

Order DL 502 Digital Latch

Standard accessories include instruction manual, 6 inch BNC cable.

WR 501



Word Recognizer with Digital Delay

WR 501

The WR 501 is a 16 bit parallel Word Recognizer with digital delay that produces trigger pulses when a preselected word occurs. It occupies one plug-in position in any TM 500 Series Power Module Mainframe.

The WR 501 may also be used separately as a word recognizer to generate triggers for oscilloscopes or other measurement instruments. It gives you fast access to any unique word in the data stream.

WORD RECOGNIZER (WR 501)

Inputs — 16 data inputs plus a clock and qualifier.

Word Selection — Made using sixteen three-position toggle switches. Positions are HI, (don't care), and LO.

Qualifier — Can expand the word recognizer to 17 bits, act as a gate for the external clock or do both.

Clock — Selects positive- or negative-going edge of clock input signal. Used for synchronous operation.

Modes — Front panel selection of snychronous word recognition (a trigger is produced only when the operator selected word occurs at a clock edge; either position, positive or negative edge, may be selected), or asynchronous word recognition (a trigger is produced anytime the recognized word occurs).

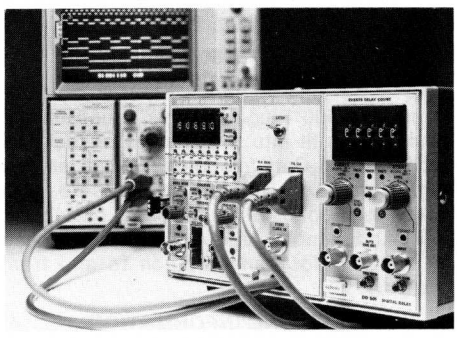
Synchronous Mode —

Minimum Set-up time	18 ns
Minimum Hold time	0 ns

(Filter is automatically disabled)

Asynchronous Mode and Filter —
Minimum coincidence time is variable from 15 ns or less to 200 ns or more.

Order WR 501 Word Recognizer



The DL 502 Digital Latch and WR 501 Word Recognizer are TM 500 Plug-ins compatible with all Tektronix Logic Analyzers (page 39-40).