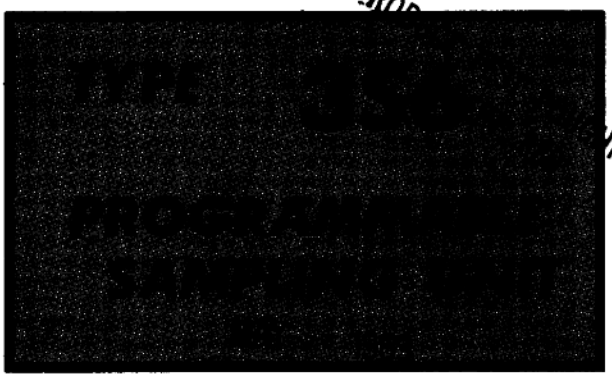
INSTRUCTION MANUAL

Serial Number B030187



Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon 97005 ● Phone 644-0161 ● Cables: Tektronix

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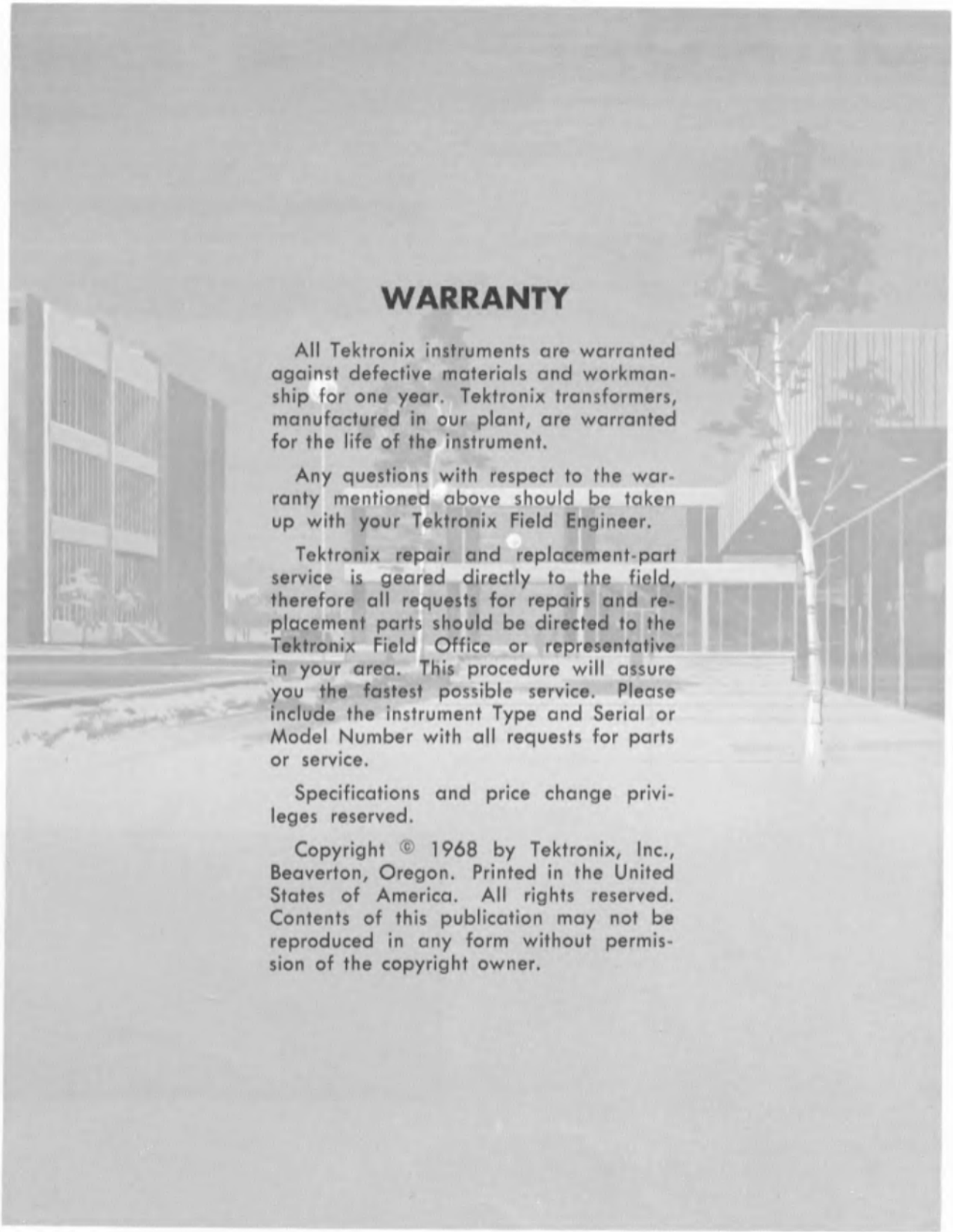


WARRANTY

All Tektronix instruments are warranted against defective materials and workmanship for one year. Tektronix transformers, manufactured in our plant, are warranted for the life of the instrument.

Any questions with respect to the warranty mentioned above should be taken up with your Tektronix Field Engineer.

Tektronix repair and replacement-part service is geared directly to the field, therefore all requests for repairs and replacement parts should be directed to the Tektronix Field Office or representative in your area. This procedure will assure you the fastest possible service. Please include the instrument Type and Serial or Model Number with all requests for parts or service.

Specifications and price change privileges reserved.

CONTENTS

Abbreviations and symbols used in this manual are based on or taken directly from IEEE Standard 260 "Standard Symbols for Units" MIL-STD-12B and other standards of the electronics industry. Change information, if any, is located at the rear of this manual.

Fig. 1-1. Type 3S6 Programmable Sampling Unit.

SECTION 1
SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Type 3S6 Programmable Sampling Unit is a dual-channel vertical amplifier plug-in unit designed for operation in the Tektronix Type 568 Oscilloscope. The Type 3S6 accepts S-series sampling heads. The sampling heads determine the input characteristics of the sampling unit and the availability of trigger pickoff for internal triggering from Channel A.

The Type 3S6 will operate with any Tektronix 3T-series sampling unit. It is recommended that it normally be used with 3T6 Programmable Sampling Sweep. Both the Type 3S6 and the Type 3T6 can be externally programmed through a rear panel connector that is accessible through J214 of a Type 568 or R568 Oscilloscope. (Conventional or real-time time-base plug-in units do not operate with the Type 3S6.) The Type 3S6 provides the vertical signal information for amplitude measurements by a Tektronix digital readout system (Type 568-Type 230). Decimal and units control of the digital unit readout is also provided by the 3S6 including a sampling head deflection factor multiplier for sampling heads with sensitivities requiring the numbers around the Type 3S6 Units/Div control to have a decimal shift.

One or two S-series sampling heads can be used remotely on an interconnecting cable provided with the Type 3S6. This cable connects the sampling heads to J113 on the rear panel of the Type 568 Oscilloscope. Interconnecting wiring within the Type 568 connects J113 to J13 at the rear of the Type 3S6. The Type 3S6 provides the power for the sampling heads.

NOTE

Earlier models of the Type 568 Oscilloscope require installation of Field Modification Kit Tektronix Part No. 040-0492-00, to provide an interconnecting path from the sampling heads to the Type 3S6 input circuits.

Sampled signals are presented to the oscilloscope CRT vertical deflection plates. The two Type 3S6 channels may be displayed either individually, simultaneously, or in a combined mode, A + B, producing algebraic addition of two input signals. External programming of the Type 3S6 produces only simultaneous displays (Dual Trace) of the two channels. Individual channel displays are possible by offsetting the unused channel just outside the graticule area by external programming of DC Offset to the unused channel. A + B displays are not possible when externally programming the Type 3S6.

ELECTRICAL CHARACTERISTICS

Digital Unit Compatibility

The Type 3S6 is compatible for operation with all Type 230 (or R230) Digital Units.

Characteristics

The following characteristics apply over an ambient temperature range of 0° C to +50° C and after a five minute warmup, providing the instrument was calibrated at a temperature between +20° C and +30° C.

Characteristics listed below apply for either front panel operation or external programming only after the Type 3S6 front panel GAIN control has been properly adjusted for the particular oscilloscope in which the unit is operating.

For particular system warmup requirements, refer to the Type 568 instruction manual.

A procedure for mating the Type 3S6 to the oscilloscope can be found in the Operating Instruction section.

ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirement
Deflection Factor	
UNITS/DIV Range	2 to 200 in seven steps in a 1-2-5 sequence with Units/Div labeled on the sampling head.
Accuracy	Within 3%, when NORMAL-SMOOTH function is NORMAL, including sequential and random sampling. Within 4% when NORMAL-SMOOTH function is SMOOTH. (Not used with random sampling.)
Units/Div VARIABLE Range	Increases any display deflection at least 2.5 times when control is turned fully CW from CAL position. (Control also alters signal sent to digital unit. Control is inoperative when Vertical Mode switch is at EXT PROG.)
B DELAY Range	$\geq$ 10 ns
Interchannel Delay Range	At least +5 to −5 ns, with two of same type sampling heads; either both in Type 3S6 or both on identical length extender cables, and only when using time-coincident signals.

ELECTRICAL CHARACTERISTICS Cont'd

Characteristics	Performance Requirement
Loop Gain At NORMAL	Can be set to be < 0.90 to > 1.10 using the DOT RESPONSE control.
At SMOOTH	0.3 X Unity Loop Gain (DOT RESPONSE control inoperative).
Low Frequency Trigger Rate Dot Slash	Vertical dot drift is 50.1 div when sampling sweep unit is triggered at 20 Hz.
Vertical GAIN control	Adjusts a post Memory amplifier gain so all deflection factors match the oscilloscope CRT deflection factor.
DC OFFSET External Program controlled: Range	—995 mV to +995 mV in 5 mV steps, programmed by a modified BCD code.
Accuracy	Within 2% of the programmed value, or 5 mV, whichever is greater.
Front Panel (Internal) Dial control: Range	+1 V to —1 V.
Accuracy, expressed as relationship between dial number and the same voltage when externally programmed	Within 10 mV of the same offset voltage obtained in the external program mode.
Source resistance	10 kΩ, within 1%.
Accuracy (referred to Input)	Within 2%.
Deflection Factor (Referred to CRT)	200 mV per display division, within 3% at both positions of INVERT switch.
Source resistance	10 kΩ, within 0.5%.
Accuracy of Vertical Signal to Digital Unit	Within 2% at NORMAL (typically 1%). Within 3% at SMOOTH. When Units/Div VARIABLE is at its CAL detent position.
CENTERING control Range	Control can move free-run trace at least +2 to —2 divisions from graticule centerline.
Position Indicator Lamps	One indicator lamp will be on and the other off when CRT dot is more than 4 divisions away from graticule centerline.
Programmable Functions	Both Channel Units/Div, DC Offset, and Smoothing.
Units/Div Multiplier	A digital unit readout decimal and units multiplier (milli) automatically responds to any sampling head multiplier of ×0.1, ×1, or ×10 that may require the numbers around the Units/Div switches to have a decimal shift.
Type of Units	The Type 3S6 automatically controls a digital unit readout to indicate the Volts and Amps units of either channel sampling head.
External Programming Logic	Negative
Logical 1 (True)	Ground, or a voltage from 0 V to +2 V. See the operating instructions for current value required of the external closure circuit (Fig. 2-10).
Logical 0 (False)	Open circuit, or a voltage from +6 V to +15 V. See the Operating Instructions for leakage current values allowable when external closure circuit is a cut-off transistor (Fig. 2-10).

ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature— —40° C to +65° C.

Altitude—to 50,000 feet.

Operating

Temperature—As stated above Electrical Characteristics table.

Altitude—to 15,000 feet.

MECHANICAL CHARACTERISTICS

Dimensions—Height 6¼ inches

Width 4¼ inches

Length 14½ inches

Approximate dimensions including knobs and connectors.

Construction—Aluminum alloy chassis with epoxy laminated circuit boards. All circuit boards are removable without using a soldering iron. Two center-located circuit cards are of the plug-in type. The front panel is anodized aluminum.

Accessories—An illustrated list of the accessories supplied with the Type 3S6 is at the end of the Mechanical Parts list pullout pages.

SECTION 2
OPERATING INSTRUCTIONS

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

This section covers installation, first time operation, function of front panel controls and connectors, general operation and applications of the Type 3S6 Programmable Sampling Unit. If you are unfamiliar with sampling, it may be helpful to read Section 3, Basic Tektronix Sampling Principles, before proceeding with this section.

The Type 3S6 is a special purpose dual-channel sampling unit designed to operate with a Type 568 Oscilloscope. The Type 3S6 uses S-series sampling heads which determine the input characteristics of the sampling system.

The Type 3S6 has no provisions on the front panel for applying input signals. Sampling heads for either or both of the Type 3S6 channels are connected through a cable, supplied with the Type 3S6, to J113 on the rear panel of the Type 568 Oscilloscope. See Fig. 2-1.

NOTE

Earlier models of the Type 568 Oscilloscope require installation of Field Modification Kit, Tektronix Part No. 040-0492-00, to provide an interconnecting path from the sampling heads to the Type 3S6 input circuits. This modification consists of installation of J113 on the Type 568 rear panel and J13 at the rear of the vertical plug-in compartment. Kit No. 040-0492-00 provides these connectors already wired, together with necessary mounting hardware.

Input signals of both channels are routed from J113 on the Type 568 rear panel to J13 at the rear of the vertical plug-in compartment. Be sure that the adapter (Connector, Circuit Board, Tektronix Part No. 012-0149-00) is inserted in J13 of the Type 3S6. See Fig. 2-2. This part provides continuity from pins J13 of the Type 3S6 to corresponding pins of J13 of the Type 568. The same type connector must be inserted in J14 of the Type 3S6 for external programming.

For equivalent time sampling, the sampling system consists of a Type 568 Oscilloscope, Type 3S6 Sampling Unit, S-series sampling head (or heads), an interconnecting cable for connecting sampling heads to the rear of the Type 568, and a sampling sweep unit. The Type 3S6 is not intended for use with real-time time-base units. The Type 3S6 may be externally programmed through the Type 568 rear panel connector J214 by a Tektronix Type 240 Program Control Unit or Type 241 Programmer.

The Type 3S6 vertical deflection factors of 2 to 200 are calibrated to the units labeled on the sampling head.

Installing the Type 3S6 in the Oscilloscope

The Type 3S6 is designed to drive the vertical deflection plates of the oscilloscope CRT, and therefore is installed in the left-hand compartment of the oscilloscope.

Install the supplied small circuit board connectors (Tektronix Part No. 012-0149-00), one into the Type 3S6 rear panel connector J13, and the other into the rear panel connector J14. See Fig. 2-2. J13 completes the circuits for operation of the remote sampling heads and J14 completes the circuits for external programming of the Type 3S6.

To insert the Type 3S6 into the oscilloscope compartment, turn the knob (at the front panel bottom center) counterclockwise several turns until it stops. Then slide the Type 3S6 completely into the compartment using the handle at the bottom of the front panel. Once the plug-in is seated, turn the knob a few turns clockwise until it is hand-tight.

The Type 3S6 requires at least one sampling head in order to operate. Connect an S-series sampling head to the input cable (Fig. 2-1) as follows:

1. Pull the latch knob outward from the sampling head front panel (this knob will normally be pushed out during the connecting process if the knob is free to move).

2. Slowly insert the two plastic guides at the end of the CH A or CH B portions of the input cable completely into the sampling head.

3. Push in the latch knob to lock the sampling head to the cable.

4. To remove a sampling head from the cable, pull the latch knob outward from the sampling head front panel and remove the unit from the cable.

Fig. 2-1. Interconnecting cable for connecting sampling heads to J113 of Type 568 Oscilloscope.

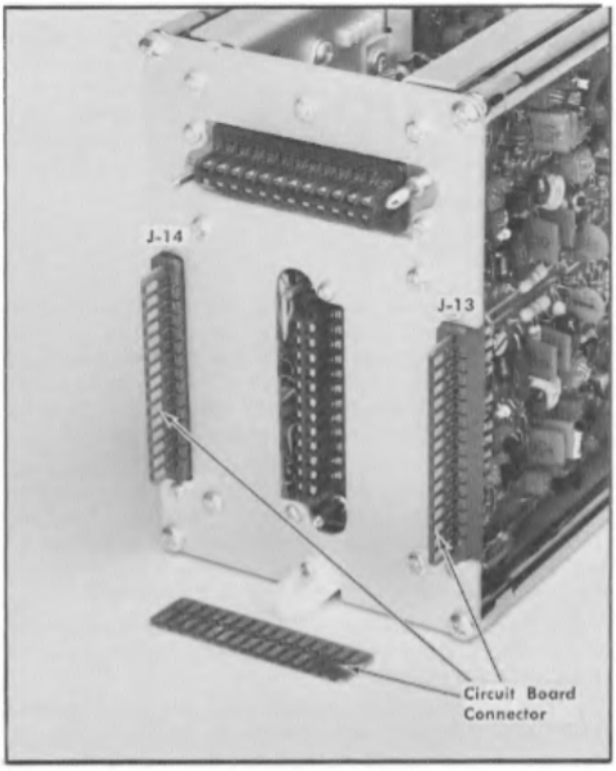


Fig. 2-2. Installation of Circuit Board Connector.

Mating

The Type 3S6 Output Amplifier gain must be matched to the indicator oscilloscope CRT deflection factor for accurate signal amplitude measurements. The GAIN control, a screwdriver adjustment on the front panel, adjusts the Output Amplifier gain of the Type 3S6. The Type 284 Pulse Generator is used as a signal source when adjusting the GAIN control in the Equivalent-Time Sampling operation which follows. Changing the GAIN control setting doesn't affect the amplitude of the signal sent to the digital unit. For further gain-setting information, refer to the Gain Adjustment instructions later in this section.

FIRST TIME OPERATION

Equivalent-time Sampling Operation

Equivalent-time sampling operation of the Type 3S6 requires a sampling sweep unit in the right hand compartment of the indicator oscilloscope. In this First Time Operation procedure, a Type 3T6 Programmable Sampling Sweep Unit, Type 568 Oscilloscope, Type 230 Digital Unit, and a Type 284 Pulse Generator are used (see Fig. 2-3). Any S-series sampling head can be used. If you are not already familiar with the operation of the oscilloscope and sampling sweep unit, read the manuals for these instruments before proceeding. Two Type S-2 Sampling Heads were used when making the waveform photographs for the following procedure. Set the controls as follows:

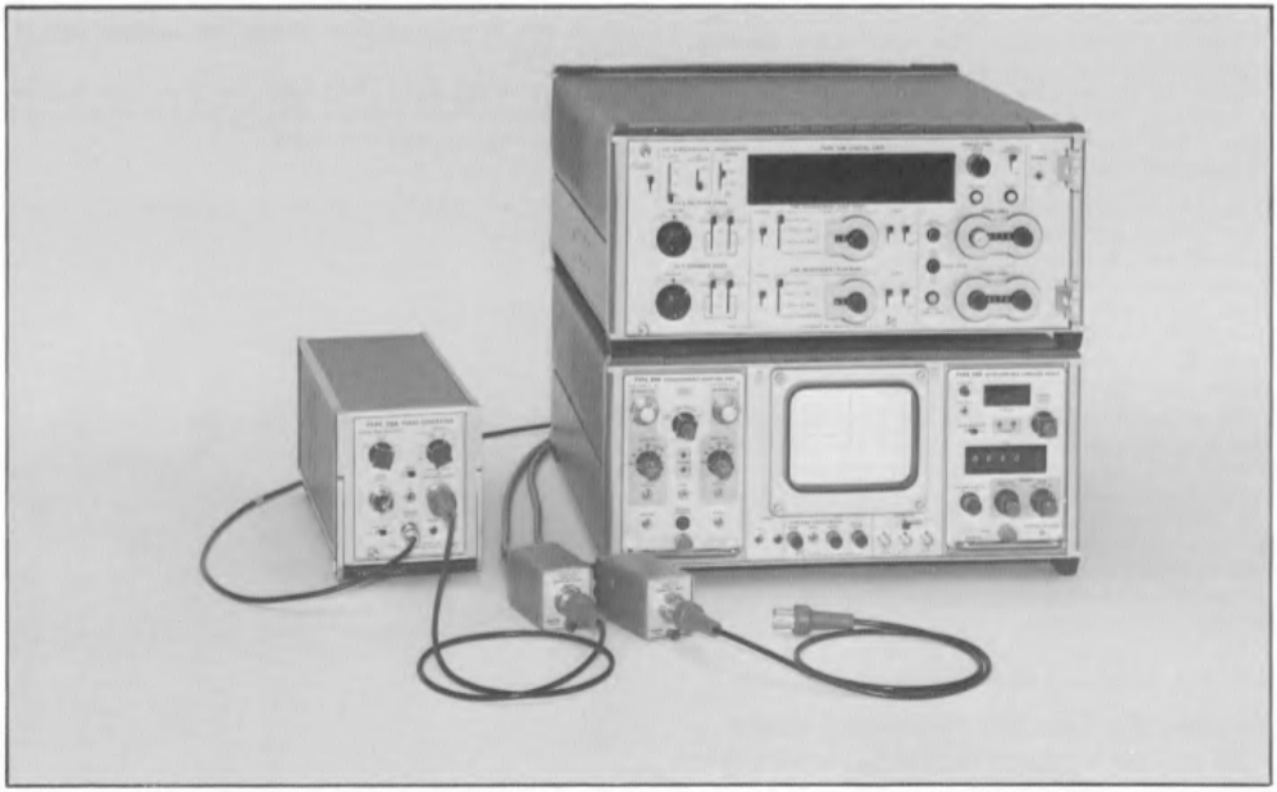


Fig. 2-3. Setup used during First Time Operation.

Type 3S6

Display Mode	CH A
NORMAL-SMOOTH	NORMAL
DC OFFSET (both channels)	0.00 (locked)
Units/Div (both channels)	200
VARIABLE (both channels)	CAL (detent)
INVERT (both channels)	Push in

Type 3T6

Horiz Position	Midrange
Samples/Sweep	1000
Time/Div Decade Time/Div Multiplier	7 5 } 500 ns/Div
Delay	0000
Program Selector	Internal
Trigger Sensitivity	Fully clockwise (free-run)
Recovery Time	Optional
Trigger Source	External

Type 230

Measurement Averaging	8
CRT Intensification	Ref Zones to OFF Time Measurement to OFF
Measurement Mode	A volts
CH A Reference Zones	Both at Average
Channel switches	Both at A
Time Measurement Start Point	Optional
Time Measurement Stop Point	Optional
Slope	Both at + and 1st
Display Time	Midrange
Triggered Measurement	Off
Limits	Optional

Type 284

Square Wave Amplitude	1.0 V
Period	1 μs
Mode	Square Wave Output
Lead Time	[1]75 ns

[1]Type 284 instruments having serial numbers prior to SN B030236 require installation of Field Modification Kit, Tektronix Part No. 040-0487-00 in order to obtain a 75 ns trigger lead time.

NOTE

Operating sampling heads having a 50 Ω input without the input connector terminated by a 50 Ω resistor or coaxial cable will cause a few millivolts vertical shift to the zero signal baseline. This occurs because the strobe kickout signal is reflected from the open input connector. The kickout signal arrives back at the sampling bridge during sampling time, while the bridge is still conducting. To avoid this, set the display zero reference point with the sampling head input circuit terminated. Also use at least 20 cm of airline between the sampling head input and a fast generator or circuit that is sensitive to the fast strobe kickout signal.

Operating Adjustments. Turn on power and allow the equipment to warm up for 5 minutes. Connect a 50 Ω coaxial cable with a 5 ns signal delay and GR 874 connectors to the input connectors of the sampling heads for Channel A and Channel B. Do not connect the opposite ends of these cables at this time.

Operating adjustments should be checked periodically, and must be adjusted when the Type 3S6 is used in a different oscilloscope. The Type 3S6 CENTERING, sampling head Bridge Balance, and the Type 3S6 GAIN controls are explained below.

With DC OFFSET controls for both channels locked at the 0 mV positions (0.00), adjust the screwdriver-adjust CENTERING control until the trace is at the graticule centerline. Position the trace start to the graticule left edge using the Type 3T6 horizontal Position control. The sampling head Bridge Balance control (accessible through hole in case left side) is checked next.

Set the CH A UNITS/DIV switch to 200. Turn the UNITS/DIV control clockwise. Adjust the sampling head control until the trace remains stationary near the graticule center as the UNITS/DIV control is turned throughout its range. Set the Display Mode switch to CH B. Adjust the CH B sampling head Bridge Balance using the same procedure. Return the display Mode switch to CH A. Check the setting of the GAIN control next.

Connect the Square Wave Output signal from the Type 284 to the coaxial cable leading to the Channel A sampling head. Any applied signal (to sampling head) should be 1 volt or less. See the Specification section of the sampling head manual (bound in this Type 3S6 manual) for further information. Connect the Trigger Output connector of the Type 284 to the Type 3S6 external trigger input connector J123 located on the Type 568 rear panel through a 50 Ω coaxial cable with a 5 ns signal delay and BNC connectors.

Adjust the Type 3T6 Trigger Sensitivity control counterclockwise, then clockwise for a stable display. Center the display vertically using the DC OFFSET control. The square wave displayed will have a vertical amplitude of 5 major divisions if the GAIN control on the Type 3S6 front panel is properly set. If the vertical amplitude is not 5 divisions, adjust the amplitude by setting the GAIN control with a small screwdriver.

Check Channel B gain by applying the square wave output of the Type 284 to the coaxial cable leading to the Channel B sampling head. Change the Display Mode switch to CH B. A square wave having a vertical amplitude of 5 major divisions should be displayed. If not, see the Performance Check and Calibration section of this manual. Return Type 3S6 Display Mode to CH A.

Digital readout of the amplitude of the vertical input signal applied to either Channel of the Type 3S6 can be displayed on the Type 230 Digital Unit. Set Type 230 Ref Zones switch to 0%. Use the CH A 0% Position control (outer knob) to set the intensified region about one-half centimeter to the left of the rising portion of the displayed signal. Set Ref Zones switch to BOTH. Use the CH A 100% Position control to set the second intensified region about one-half centimeter to the right of completion of the rising portion of the signal displayed. Pulse amplitude is read in the Type 230 readout window.

Change the following control settings of the Type 230.

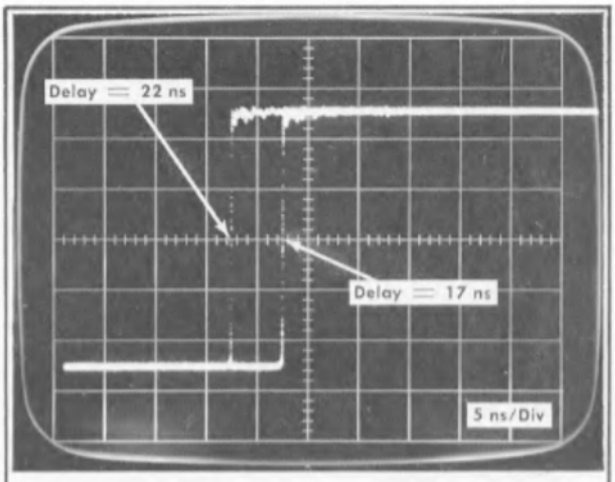
Ref Zones	OFF
Measurement Mode	Time
Time Measurement Start	10% between zones
Time Measurement Stop	90% between zones

Measuring a Step Signal 10% to 90% Risetime. Connect the coaxial cable from Channel A input to the Pulse Output connector of the Type 284. Set the Type 284 Mode switch for Pulse operation. Set the Type 3S6 CH A Units/Div switch to 50 and the Display Mode switch to CH A. Vertically position the display to midscreen using the CH A DC OFFSET control. Set the Type 3T6 Time/Div Decade to 9 and the Multiplier to 5 for a sweep rate of 5 ns/Div.

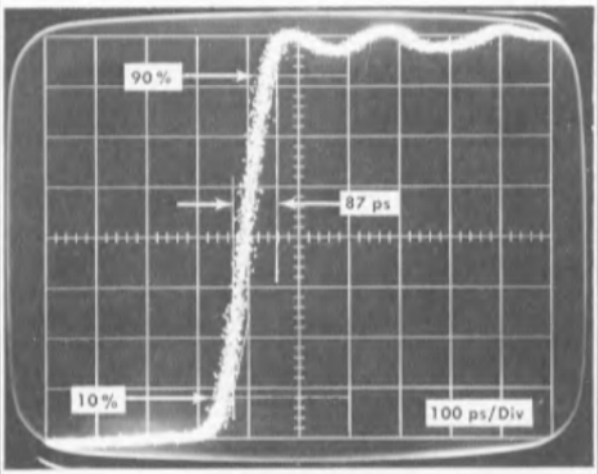
Adjust the Type 3T6 Trigger Sensitivity for a stable display. Position the display start to the graticule left edge using the Type 3T6 Horizontal Position control. Delay the time window start by adding delay in 1 ns increments, while noting the effect on the display. See Fig. 2-4A. Continue to add delay until the pulse start is less than 1 division from the graticule left edge. Note delay reading and set the Time/Div Decade switch to 0 (fully clockwise). The sweep rate is now 500 ps/div. It should be noted that when the Time/Div Decade was turned to the fully cw position a decimal appeared in the Delay readout area, indicating the delay to be one-tenth of the previous value. Reset the Delay dials to equal the previous value. Change the Delay to again position the rising portion of the pulse near the graticule left edge. Set the sweep rate to 100 ps by placing the Time/Div Multiplier to 1. Position the display to the position shown in Fig. 2-4B using the Type 3T6 Horizontal Position control, the Type 3S6 DC OFFSET, and the Type 3S6 VARIABLE control. Read the pulse 10% to 90% risetime from the CRT graticule markings by determining the horizontal distance in divisions between the 10% and 90% amplitude levels of the pulse. Multiply the number of divisions times the sweep rate to determine the pulse risetime. See Fig. 2-4B. Inaccurate measurement of risetime will result if a nonlinear portion of the sweep is used. Refer to linearity specifications for your sampling sweep unit to determine whether a portion of the sweep must be excluded.

To measure pulse risetime using a digital unit, set the Type 230 Time Measurement switch to ON and Ref Zones switch to BOTH. Set the intensified reference zones to the positions shown in Fig. 2-4C by turning the 0% and 100% Position controls. Read the pulse risetime in the Type 230 readout window.

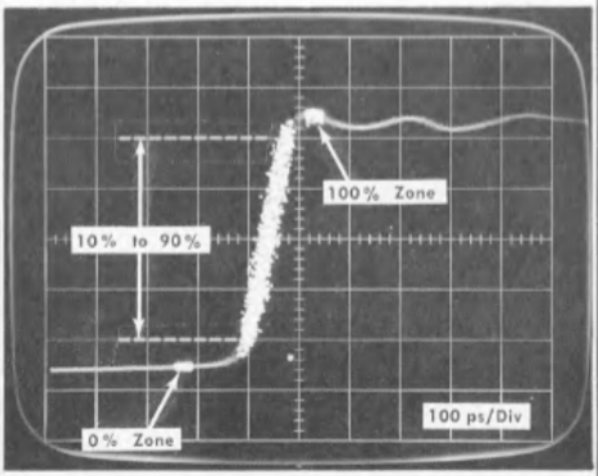
The function of the Type 3S6 front panel controls and connectors is explained below. See Fig. 2-5.



(A) Effect of increasing sampling sweep delay by 5 ns.



(B) Determining risetime from the CRT display.



(C) Determining risetime from the digitial readout unit.

Fig. 2-4. Fast-rise pulse displays.


TYPE 3S6 PROGRAMMABLE SAMPLING UNIT
CHANNEL A
CHANNEL B
DC OFFSET ±1V
DC OFFSET ±1V
INTERNAL TRIGGER CH A ONLY
DUAL-TRACE
CH A
CH B
EXT PROG
A+B
NORMAL
SMOOTH
UNITS/DIV
UNITS/DIV
CAL
VARIABLE
50
20
10
100
5
200
2
INVERT PULL
POSITION
DOT RESPONSE
GAIN
DOT RESPONSE
CENTERING
EXTERNAL PROGRAM
B DELAY
SERIAL

FUNCTIONS OF FRONT PANEL CONTROLS AND CONNECTORS

Display Mode Switch — Selects one of the five following display modes.

- **CH A** — The Channel A signal is displayed.
- **CH B** — The Channel B signal is displayed.
- **DUAL-TRACE** — Both channel signals are displayed. The display switches from CH A to CH B after each CH A dot, and vice versa.
- **A + B** — The algebraic sum (±A, ±B as selected with the INVERT switches) of the two channels is displayed.
- **EXT PROG** — Selecting EXT PROG with the Display Mode Switch causes the Type 3S6 to operate in the Dual-Trace Mode. Programming logic is supplied through connector J214 on the Type 568 rear panel when using EXT PROG Mode. Deflection factor, DC Offset amplitude, Offset polarity, and NORMAL/SMOOTH functions are externally programmable. The front panel Units/Div VARIABLE is inoperative when using EXT PROG and therefore has no effect on displayed signal amplitude. Front panel screwdriver adjustments, position indicators, and the INVERT switches operate in their normal manner when using EXT PROG.

DOT RESPONSE (screwdriver adjustment) — Allows the loop gain of each Channel to be adjusted to unity when the NORMAL/SMOOTH switch is in the NORMAL position. DOT RESPONSE controls are inoperative in SMOOTH position.

NORMAL/SMOOTH (red knob concentric with the Display Mode switch) — Selects unity loop gain at NORMAL and reduces the loop gain to 0.3 or less at SMOOTH. Smoothing reduces the effect of random noise on the display while requiring high sampling dot density for the correct displayed risetime.

DC OFFSET ±1 V Controls — These controls apply internal signal offset voltages of +1 V to −1 V to the sampling head (unless otherwise stated on the sampling head front panel). The input signal zero reference (related to the CRT) is the DC Offset voltage instead of ground. This permits all portions of a maximum ±1 V input signal to be positioned through the CRT vertical window even at a deflection factor of 2 Units/Div (2 mV/Div for sampling heads such as the Types S-1, S-2, and S-3). The vertical window is a total of 16 mV when the deflection factor is 2 mV/Div, and 1.6 volts when the deflection factor is 200 mV/Div. The calibrated offset dial is marked with 100 minor divisions each of which represents 2 mV. Each complete turn changes the offset 200 mV. The dial may be rotated 5 complete turns in either direction, from the 0.00 mV setting. The offset control provides a range of offset voltage from −1 V to +1 V. Negative offset voltage is indicated by the black numbers on the dial and positive offset voltage by the red numbers. The number appearing below the index marker is added to the number above the index marker and their sum is multiplied by 10 to determine the DC Offset voltage. Be sure to read numbers from the dial below the index marker having the same color as the numbers above the index marker. When starting from the 0.00 mV position, turning the control clockwise moves the display up and provides increasing values of negative offset voltage. Counterclockwise rotation of the control has the opposite effect.

Units/Div Switches — Selects calibrated deflection factor for each Channel. The units are selected and named on the panel. S-series sampling head For example, with a Type S-2 sampling head in Channel A, the Channel A Units/Div switch set at 100 and the VARIABLE control in the CAL position, each major division of deflection corresponds to 100 millivolts of applied signal at the Type S-2 input connector.

VARIABLE controls (Same control knob used for INVERT) — Provides uncalibrated variation of the deflection factor between labeled values of the Units/Div switches. Display size increases at least 2.5 times as the control is rotated clockwise from the CAL (detent) position. This control is inoperative during external programming.

INVERT Switches — In the Normal (pushed in) position, a positive input signal deflects the CRT beam upward. In the pulled position the displayed signal is inverted. When the Display Mode switch is set to A + B, algebraic addition of Channel A and B is obtained. The position of the INVERT switches determines the polarity of each channel before algebraic addition. Allows differential displays at full frequency response of the sampling heads in use. These switches do not affect the signals sent to the digital unit.

B DELAY — Varies the time position of CH B display over a range of at least 10 ns. Time coincidence with Channel A depends upon the time difference of sampling heads and sampling head cable lengths.

GAIN — Matches the vertical output amplifier gain to the oscilloscope CRT deflection factor. (Does not affect the internal Digital Gain accuracy).

CENTERING Control (screwdriver adjust) — Adjusts the vertical position of the A and B displays. See page 2-14 for adjustment limits.

EXTERNAL PROGRAM Indicator — Lights when the Display Mode switch is set to EXT PROG as a reminder that DC Offset voltage, Offset voltage polarity, Units/Div, and Smooth/Normal functions are being externally programmed.

OPERATING INFORMATION

Gain Adjustment Using Oscilloscope Calibrator

NOTE

It is recommended that 60 Hz oscilloscope calibrators be used as a signal source for setting the Type 3S6 GAIN adjustment only when no other source is available, and then only after verifying the signal amplitude with accurate measuring equipment. The following procedure uses the Type 568 20 kHz Calibrator (500 mV into 50 Ω, ±2%), producing a Type 3S6 deflection factor accuracy of ±5%.

1. Allow the equipment to warm up for at least 5 minutes.

2. Set the controls as follows:

Type 3S6

Display Mode	CH B
NORMAL/SMOOTH	NORMAL
DC OFFSET (both Channels)	0.00
Units/Div (both Channels)	100
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Push in

Type 3T6

Horiz Position	Midrange
Samples/Sweep	1000
Time/Div Decade Time/Div Multiplier	5 1 } 100 μs/Div
Delay	Optional
Program Selector	Internal
Trigger Sensitivity	For triggered display
Recovery Time	Clockwise
Trigger Polarity	+
Trigger Source	External

3. Apply the signal from the indicator oscilloscope calibrator (500 mV into 50 Ω) connector to the 50 Ω input connector of the Channel B sampling head. Use a coaxial cable and a BNC to GR adapter at the calibrator. Connect a coaxial cable with BNC connectors from the Type 568 Pretrigger connector to the external trigger connector on the Type 568 rear panel (J123).

4. With the DC OFFSET control, align the display with the graticule lines and check for exactly 5 divisions of vertical deflection. If the vertical deflection is not 5 divisions, adjust the GAIN control.

5. Check Channel A by connecting the signal into the 50 Ω input connector of the Channel A sampling head. If the amplitude is not 5 vertical divisions refer to Section 7, Performance Check/Calibration.

Triggering

Internal triggering of the sampling sweep unit from the signal applied to CH A can be used when the signal is a repetitive square or sine wave.

When observing a fast risetime pulse using the Type 3T6, an external pretrigger such as supplied by the Type 284 is required. The amount of pretrigger time required is dependent upon the type of sampling head, sampling head cable length, delay in the Type 3S6, and the type of oscilloscope used. See the Type 3T5 or Type 3T6 Instruction Manual for detailed information on pretrigger requirements.

Dual Trace

The dual-trace feature of the Type 3S6 provides for observing Channels A and B simultaneously. This is useful for determining the time relationship of two signals. The sweep may be triggered from an external source or by the signal applied to CH A input if the sampling head provides a trigger pickoff. Internal triggering is available only from Channel A. No trigger output circuit is provided for the Channel B signal. If the time relationship of two signals is to be displayed, use input cables with equal signal delays.

The B DELAY control adds a variable to the time coincidence of Channel B in relation to Channel A sampling time. The B DELAY range of 10 ns will accommodate small time differences in cables or sampling heads, so that both signals can be displayed in time coincidence.

For dual-trace operation, set the controls as follows:

Type 3S6

Display Mode	DUAL-TRACE
NORMAL-SMOOTH	NORMAL
DC OFFSET (both Channels)	0.00
Units/Div (both Channels)	100
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Push in

Type 3T6

Horiz Position	Midrange
Samples/Sweep	1000
Time/Div Decade Time/Div Multiplier	7 1 } 100 ns/Div
Program Selector	Internal
Delay	0000
Trigger Sensitivity	For Triggered Display
Recovery Time	Counterclockwise
Trigger Polarity	+
Trigger Source	External

Type 284

Square Wave Amplitude	1.0 V
Period	1 μs
Mode	Square Wave Output
Lead Time	Optional

Connect the Square Wave Output signal to the inputs of Channel A and Channel B sampling heads through a power divider and two 5 ns coaxial cables. See Fig. 2-6. Connect the Type 284 Trigger Output signal to the Type 3T6 50 Ω external trigger input connector through a 50 Ω coaxial cable (J213, Type 568 rear panel).

Adjust the Type 3T6 Trigger Sensitivity control for a stable display. Center both traces on the graticule with the DC OFFSET controls. One half of the Type 284 output signal is applied to each input. A properly triggered dual-trace display will be similar to Fig. 2-7A.

Dot Response. A convenient method of setting the DOT RESPONSE controls for unity loop gain is to cause double or multiple triggering of the sweep so that some samples must respond to the full 0.5 volt signal amplitude.

NOTE

The maximum allowable amplitude of the signal into the sampling head input for unity loop gain depends upon the sampling head used. (For example, 0.5 V with the Type S-1, 0.2 V with the Type S-2, 1 V with the Type S-3).

For adjusting the loop gain using the Type S-2, the output of the Type 284 may be set at 100 mV (providing 50 mV at each output of the power divider) or a 50 Ω attenuator may be inserted between the power divider and the input of the Type S-2.

Turn the Type 3T6 Trigger Sensitivity control clockwise into the free-run region, and adjust the Recovery Time control until the display is similar to Fig. 2-7B. In the double triggered display of Fig. 2-7B, Channel A is operating at less than unity loop gain and Channel B is operating at unity loop gain. Clockwise rotation of the Channel A DOT RESPONSE control will produce unity loop gain as shown for Channel B. Adjust the DOT RESPONSE controls for the best flat upper or lower portions of the square-wave display.

Double or multiple triggering is useful in setting the DOT RESPONSE controls for unity loop gain. However, this type of display should be avoided in normal operation, since it is a false display.

B Delay. To show the action of the B DELAY control change the following control settings:

Type 284

Mode Switch	Pulse Output

Type 3S6

Units/Div (both Channels)	50

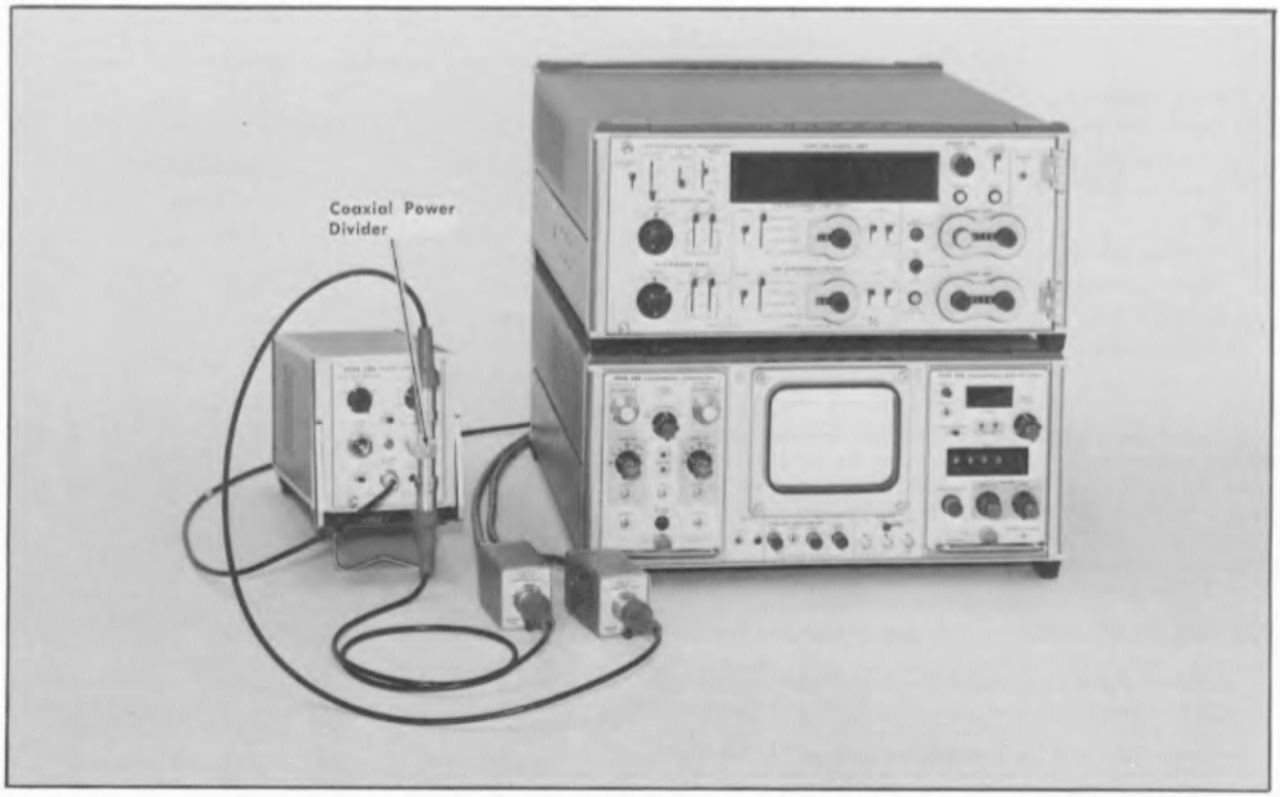


Fig. 2-6. Initial Power Divider connections.

Type 3T6

Time/Div Decade	9 (1 ns/Div)

Connect the Power Divider to the Type 284 Pulse Output connector.

Adjust the Type 3T6 Trigger Sensitivity and Delay controls so the Channel A step signal is at the center vertical line of the graticule (see Fig. 2-7C).

Turn the B DELAY control to show the variable time window relationship between operation of the A and B Channels. Fig. 2-7C is a double exposure showing the display for the clockwise and counterclockwise positions of the B DELAY control.

Adjust the B DELAY control to move the Channel B step display to the same horizontal position as that of the Channel A step display. This coincidence of the two channel displays shows that the B Delay circuit has compensated for the small delay differences in the two signal paths. The time coincidence of two signals fed into the two 50 Ω cables can now be checked on the CRT display.

A + B

The algebraic addition of two signals can be obtained with the Display Mode switch set to the A + B position. The B DELAY control can be useful in compensating for small time delay differences in the setup before making accurate algebraic addition of two signals. For accurate algebraic addition, the sampling heads for Channel A and B should be of the same type.

The following example uses a single test signal to both Channels through identical length cables or probes.

For A + B operation, set the controls as follows:

Type 356

Display Mode	A + B
NORMAL/SMOOTH	NORMAL
DC OFFSET (both Channels)	0.00
Units/Div (both Channels)	50
VARIABLE (both Channels)	CAL
INVERT	Push in
B DELAY	As in procedure below

Type 3T6

Horiz Position	Midrange
Samples/Sweep	1000
Time/Div Decade Time/Div Multiplier	9 1 } 1 ns/Div
Delay	0000
Program Selector	Internal
Trig Sensitivity	Fully clockwise
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	External

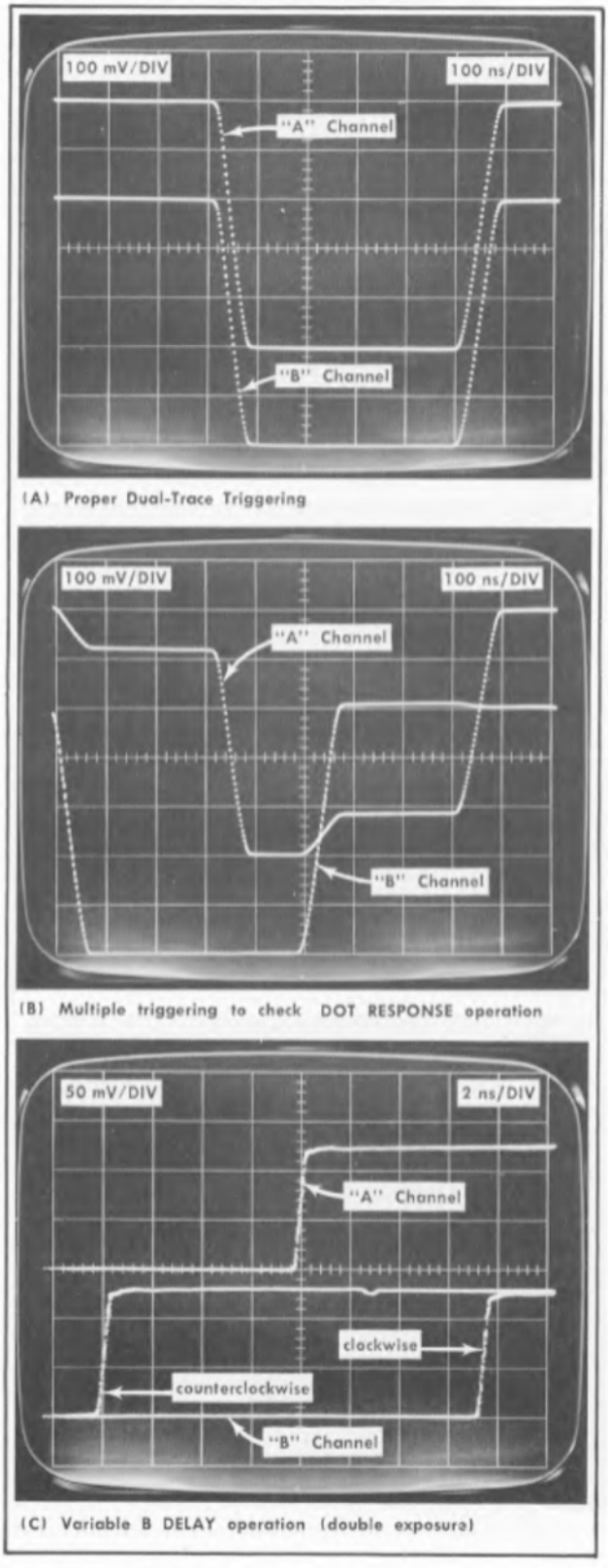
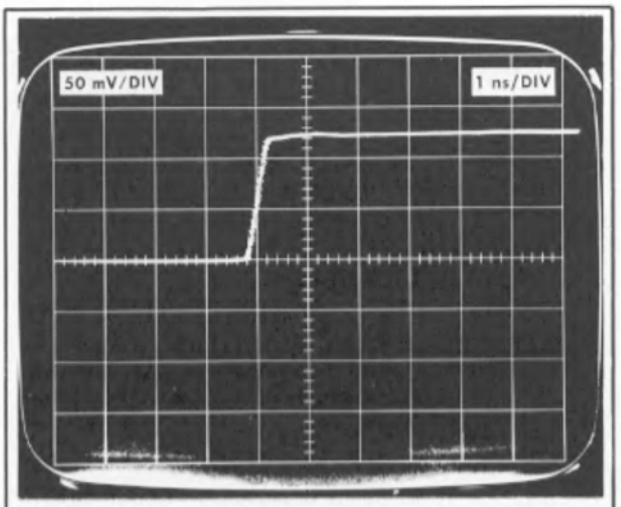
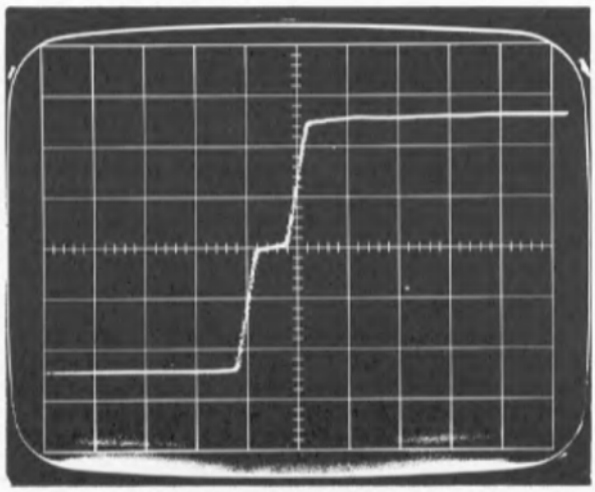


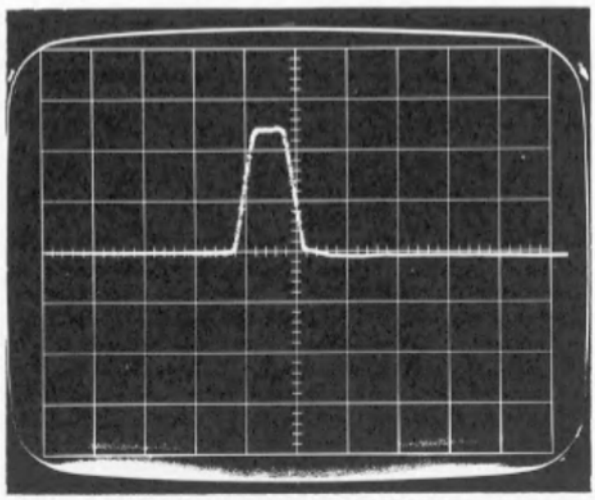
Fig. 2-7. Typical displays to show dual trace operation.



(A) A or B Channel display



(B) A + B both INVERT switches in the same position



(C) A + B one INVERT switch in the out position

Fig. 2-8. Displays used to show A + B operation.

Type 284

Mode	Pulse Output
Lead Time	75 ns

Connect the Pulse Output signal from the Type 284 to the input of Channel A and B sampling heads. Use a power divider and two 5 ns coaxial cables in the arrangement of Fig. 2-6.

Connect the Trigger Output signal of the Type 284 to the External Trigger input 50 Ω connector on the Type 3T6 through a 5 ns signal delay 50 Ω coaxial cable.

Initially set the Display Mode switch to CH A or CH B set the Type 3T6 for an externally triggered 2 ns/Div stable sweep. Set the Type 3T6 Delay as necessary to obtain a display similar to Fig. 2-8A.

Set the Type 3S6 Display Mode switch to DUAL-TRACE and adjust the B DELAY control until the two displays are in time coincidence. Set the Display Mode switch to A + B. Addition of the two signals will be displayed. Again adjust the Type 3S6 B DELAY and notice its effect upon the composite display. Fig. 2-8B shows the composite A + B display with the B DELAY adjusted about 1 ns away from time coincidence of the two signals.

Pull one of the INVERT switches, inverting one of the Channel displays. Any time difference of the two signals will be displayed as a pulse, while those portions of the two signals that are equal and opposite will display a straight line. Adjust the B DELAY control and notice the change in polarity of the pulse as Channel B passes through time coincidence with Channel A. See Fig. 2-8C.

Adjust the B DELAY control for minimum time difference. The display will approach a single trace with no vertical deflection (if the two sampling heads and cable delays are identical). When the composite A + B display is a straight line, the Channel B display is at time coincidence with the Channel A display.

When using the Type 3S6 with the Display Mode switch set to A + B and the INVERT switch of one channel pulled, the display is proportional to the difference in the applied signals. This differential operation can be useful for canceling undesired in-phase (common-mode) signals. Input voltage limitation of the sampling head must be observed (±1 V for the Type S-2 sampling head).

Calibrated DC OFFSET Controls

The DC Offset control can be rotated five complete turns clockwise or counterclockwise from the 0 mV position. Since five turns result in a 1 V change, each revolution of the dial results in a 200 mV change. Each of the 100 minor divisions on the inner dial represents 2 mV of offset voltage. Numbers indicated directly above and below the index marker are added together and then multiplied by 10 to determine offset voltage in millivolts.

The DC OFFSET dials provide a convenient way of determining DC OFFSET voltage values for external programming. These dials can be used to make a direct reading of the offset voltage provided the no-signal free-run trace position is known with the OFFSET control at 0.00. Accurate measurements of either the offset voltage or of a signal's

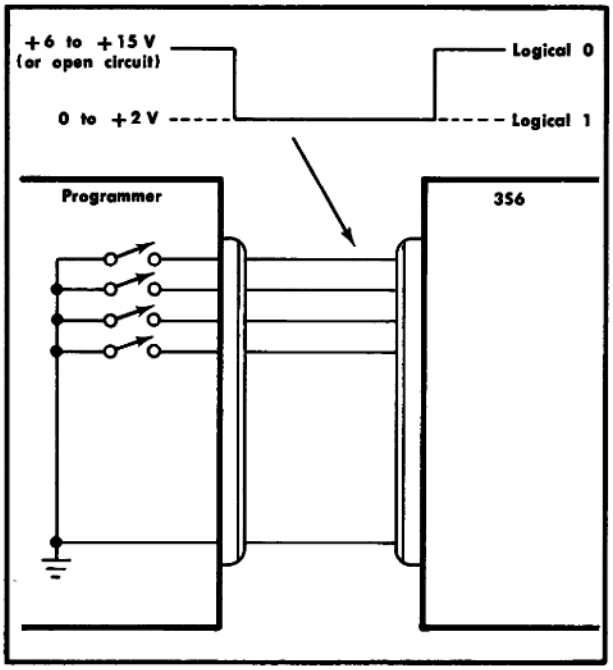


Fig. 2-9. Potentials required from programmer for proper input logic to Type 3S6 programmable functions.

amplitude can be obtained using the slideback technique. Use the OFFSET control to position the display bottom to a graticule line. Read the control dial. Use the OFFSET control to position the display top to the same graticule line. Read the control dial. The difference between the two readings is the signal amplitude.

Unless otherwise stated on the sampling head front panel, the DC Offset voltage cancels the effects of an applied DC voltage of up to ±1 V at the sampling head input.

External Programming

Deflection factor, DC offset amplitude and polarity, and either Normal or Smooth loop gain can be programmed. Terminals for connecting an automatic calibrator are also provided by the External Program connector (J14). For external programming, the Type 3S6 Display Mode switch must be set to EXT PROG and an interconnecting cable run from the programming unit to J214 on the rear panel of the Type 568 Oscilloscope. Be sure that an adapter (Connector, Circuit Board, Tektronix Part No. 012-0149-00) is inserted in J14 at the rear of the Type 3S6 (see Fig. 2-2). This connector provides continuity from pins of J14 on the Type 3S6 to corresponding pins of J14 on the Type 568. Wiring within the Type 568 connects pins of J14 to J214 on the Type 568 rear panel.

The two logic levels required to program the 3S6 can be provided in a number of ways, depending upon the type of programmer used. Each logic line can be controlled using a switch, transistor, or other closure type programmer. With the negative logic system used by the Type 3S6, a logical ONE results when the voltage of a program line is at its less positive level. See Fig. 2-9. A voltage of 0 V to +2 V applied to a program line of the Type 3S6 will provide a logical ONE, while a potential of +6 V to +15 V results

TABLE 2-1

Offset Programming (Voltages in mV)

		Hundreds lines					Tens Lines					Fives	Ground Return Lines
Offset	mV	800	400	200	100	mV	80	40	20	10	mV	5	
	000	0	0	0	0	00	0	0	0	0	0	0	
	100	0	0	0	1	10	0	0	0	1	5	1	
	200	0	0	1	0	20	0	0	1	0			
	300	0	0	1	1	30	0	0	1	1			
	400	0	1	0	0	40	0	1	0	0			
	500	0	1	0	1	50	0	1	0	1			
	600	0	1	1	0	60	0	1	1	0			
	700	0	1	1	1	70	0	1	1	1			
	800	1	0	0	0	80	1	0	0	0			
	900	1	0	0	1	90	1	0	0	1			
		Program Connector Terminals											
Channel	J14[2]	5	6	7	8		9	10	11	12		13	A
A	J214[3]	5	6	7	8		9	10	11	12		13	16
Channel	J14	J	K	L	M		N	P	R	S		14	A
B	J214	23	24	25	26		27	28	29	30		14	16

[2]J14 is connector at rear of Type 3S6 and in Type 568 Vertical plug-in compartment.
[3]J214 is on rear panel of Type 568 Oscilloscope.

in a logical ZERO. Leaving a programming line open also provides a logical ZERO, while shorting the line to ground produces a logical ONE input.

Truth tables showing logic values required by the programmable functions are presented during the following discussion.

Programming DC Offset

Refer to Table 2-1 in the following example of using a truth table while programming a DC offset voltage.

1. Assume that a test display has been properly positioned on the CRT by use of the DC OFFSET control while operating the Type 3S6 from its front panel.

2. The number appearing above the DC OFFSET control index marker is a black 40. The number directly below the index marker, of the same color, is 12.5. Adding the two numbers together and multiplying by 10 gives: 10 (40 + 12.5) or 525 mV of negative DC Offset voltage. The polarity is negative and black numbers are used since the DC OFFSET control has been rotated clockwise from the 0.00 mV position. Thus the amount and polarity of offset voltage required from the external programmer to properly display this signal is —525 mV.

3. Table 2-1 shows four logical ONE states are needed to program 525 mV of Offset voltage; in the HUNDREDS columns, a ONE is found in the 400 and 100 columns to the right of 500 mV; in the TENS columns, a ONE is found in the 20 column to the right of 20 mV; and in the FIVES column, a ONE is found to the right of 5 mV.

4. The programming connectors and pin numbers are found at the bottom of Table 2-1 and are in vertical alignment with columns of the truth table. To program CH A for 525 mV of offset voltage, apply a logical ONE at pins 6, 8, 11 and 13 of J214.

5. Table 2-2 shows logic required for selecting Offset Voltage Polarity. A negative offset voltage polarity requires a logical ZERO (+6 V to +15 V or an open circuit). To program CH A for a positive offset voltage polarity requires a logical ONE (0 V to +2 V) at terminal 1 of J214.

TABLE 2-2

Programming DC Offset Polarity

	Channel A	Channel B
J14	Pin 1	Pin 19
J214	Pin 1	Pin D

Logical ONE required for (+) polarity.
Logical ZERO required for (—) polarity.

Table 2-3 is a truth table for programming Units/Div. The truth table and terminals for programming Smoothing are given in Table 2-4. These functions are programmed in the same manner as DC Offset. Do not ground program lines to anything other than the Common Ground Return Lines shown in Table 2-1.

TABLE 2-3

Programming Units/Div

	Units/Div	A-4 B-4	A-2 B-2	A-1 B-1
	200	0	0	0
	100	0	0	1
	50	0	1	0
	20	0	1	1
	10	1	0	1
	5	1	1	0
	2	1	1	1
	Program Connector Terminals			
Ch. A	J14	2	3	4
	J214	2	3	4
Ch. B	J14	E	F	H
	J214	20	21	22

TABLE 2-4

Programming Smoothing

	Both Channels	
	Normal	Smooth
J14 Pin 15	0	1
J214 Pin 15	0	1

DC Offset Corrections

A difference in offset voltage may be noted at high sensitivities when interchanging plug-ins (3S6's) used in a system in which DC Offset is programmed.

The setting of the +15 V of the replacement Type 3S6 Power Supply may be changed slightly to return the programmed DC Offset Voltage to its former value. Changing the +15 V supply will change other adjustments slightly, such as Bridge Balance and Smoothing Balance.

Using this method of correcting for a difference in programmed DC Offset Voltage between plug-ins makes changes unnecessary in the programming system.

Programmer Current Requirements

In order that the Type 3S6 will see the proper input logic when externally programmed, certain current requirements must be met by the programmer supplying the logic.

A logical ONE is present on a 3S6 logic line if a potential of 0 to +2 volts appears on the logic line. In order to meet this requirement, the programmer must be capable of supplying a certain minimum current. The minimum current required depends upon the logic lines considered.

A worst-case example (one requiring the most current) is shown in Fig. 2-11A. This circuit is used to provide 800 mV of DC Offset. To obtain 800 mV of offset a logical ONE (0 to +2 V) is required on the programming line. A logical ONE on the programming line will reverse bias Q602 and

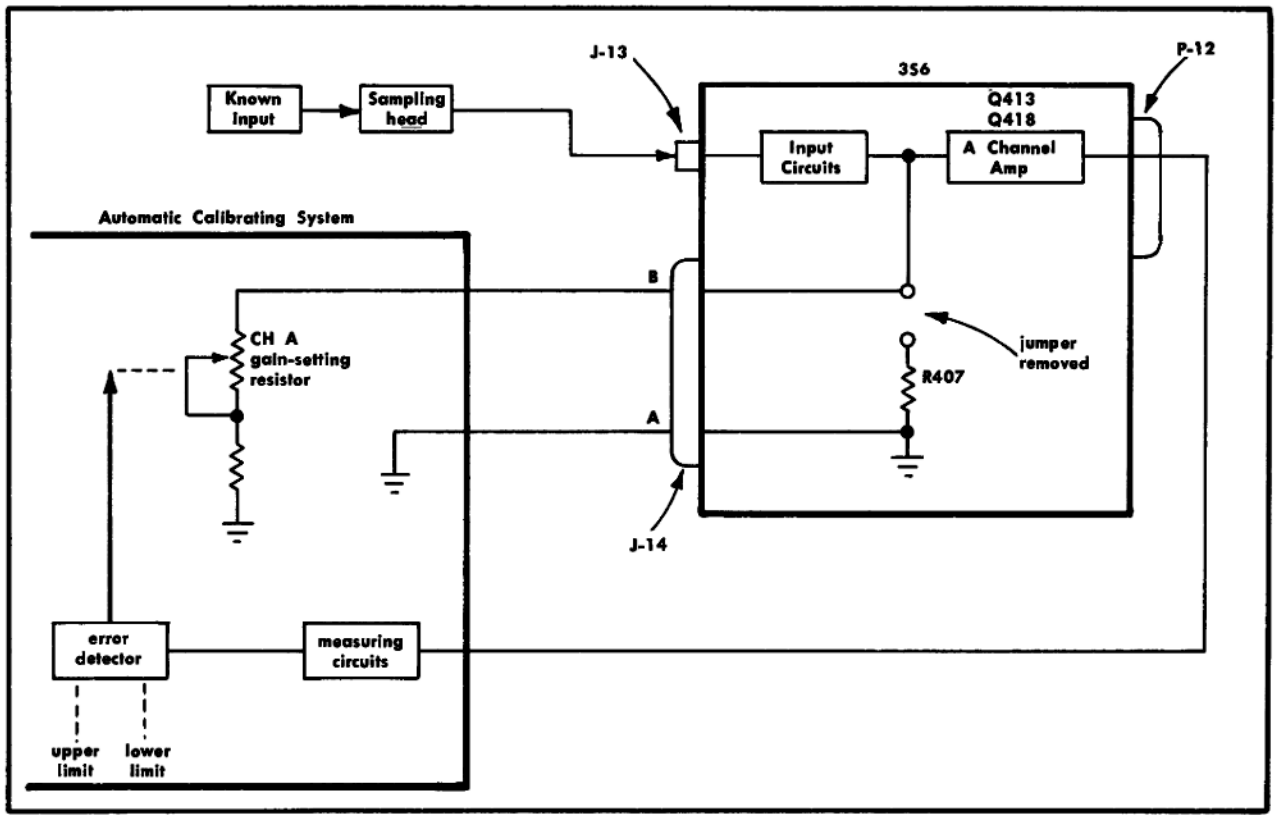


Fig. 2-10. Block diagram of a system for automatic calibration of digital readout.

keep it cut off. Fig. 2-11B illustrates that the resistance of the closed switch contacts cannot exceed 575 Ω, or more than 2 volts will appear on the programming line. Logic level ONE requires 0 to +2 V on the Type 3S6 programming line. The switch, or device used as a switch, must be able to pass at least 3.5 mA with not more than a 2 volt drop across it. This will insure that Q602 remains cut off as required.

When programming the opposite logic level (logical ZERO), the worst case condition occurs in the circuit having the highest internal resistance. This is the circuit used for programming 5 mV of DC Offset. See Fig. 2-11C.

Since the 5 mV of offset is not wanted, a logical ZERO (+6 to +15 V) is required on the programming line. Fig. 2-11C shows that leakage current through the open switch, or device used as a switch, must not exceed 16.5 μA. Keeping leakage current below this value insures that Q626 will be forward biased and will conduct sufficient current to perform its function.

The Programmer must be capable of delivering at least 3.6 mA for a logical ONE input, and must not permit more than 16.5 μA of current in the programming line for a logical ZERO input.

GENERAL APPLICATIONS

Automatic Calibration

Terminals are provided at J214 for connecting to circuits providing automatic deflection factor calibration. See Table 2-5.

TABLE 2-5

Automatic Calibration Connections

	Channel A	Channel B	Ground Return
J14	Pin B	Pin C	Pin A
J214	Pin 17	Pin 18	Pin 16

The automatic or (self-cal) feature is intended primarily for use in systems employing digital readout and requiring close tolerance accuracy. An automatic or self-calibrating system can be made that will check the reading of the digital unit against a known value of input signal (when programmed to do so). See Fig. 2-10. If the measured value is not within selected limits of the known value the Type 3S6 gain will be automatically changed. A reading above the upper limit selected results in a reduction in amplitude gain. A reading below limit will cause amplifier gain to increase. Although only Channel A is shown in Fig. 2-10, both channels can be controlled.

In systems using the automatic calibration feature, internal jumpers at the input circuits of Q413 and Q433 must be removed. It is not necessary for the Type 3S6 Display Mode switch to be in the EXT PROG position.

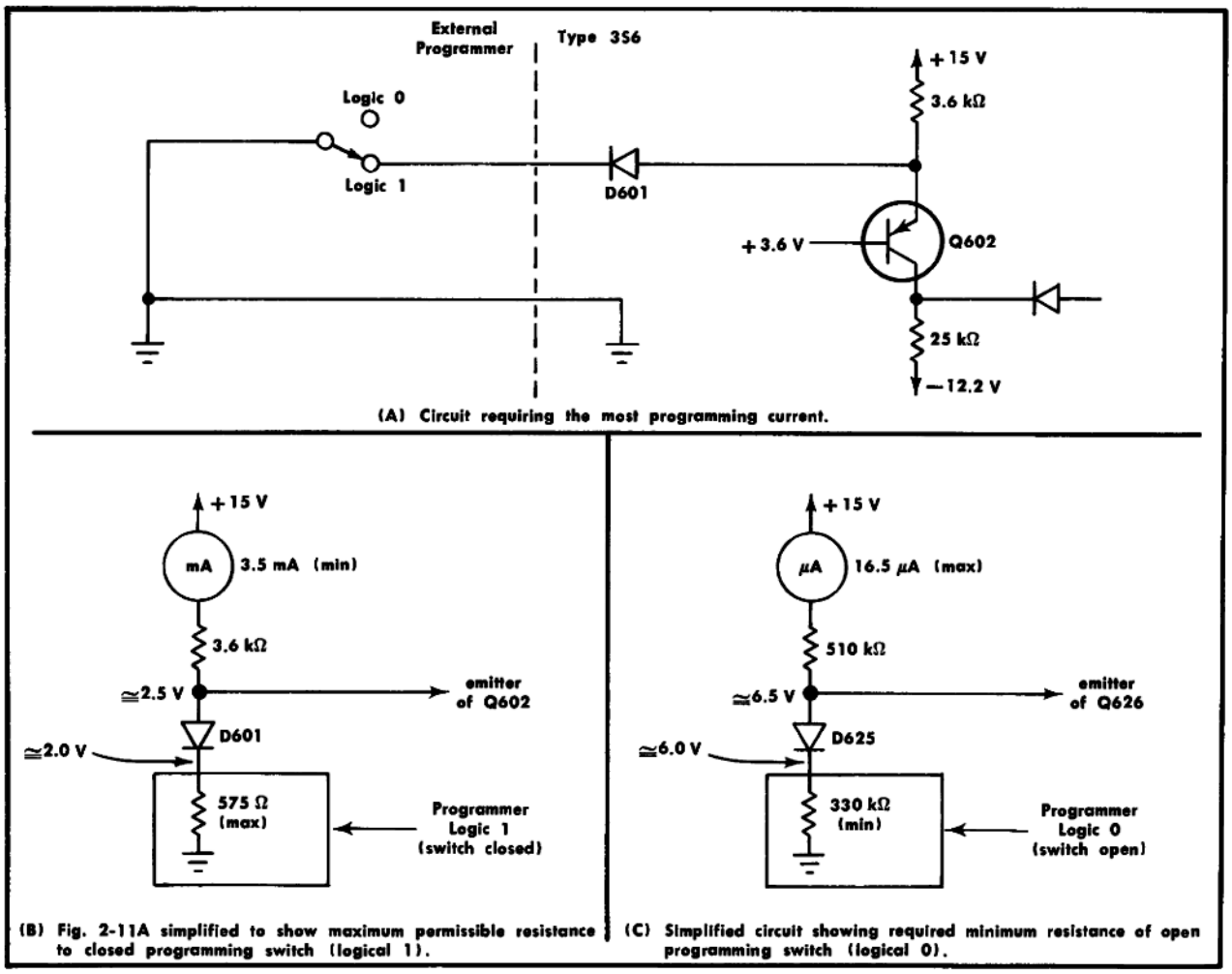


Fig. 2-11. External programmer current and resistance requirements.

Digital Readout

The Type 3S6 will provide vertical information for use with the Type 568/Type 230 Digital Readout System. A sampling sweep unit is needed along with the Type 3S6. The screwdriver adjusted CENTERING control must be properly set when making amplitude measurements with a digital unit. Set the sampling unit DC Offset control for zero volts. Without a signal applied, free run the sampling sweep unit and adjust the CENTERING control so the no-signal trace is within ±½ major division of the graticule centerline. Now all on-screen displays, regardless of DC Offset value, will properly drive the digital unit for amplitude measurements.

NOTE

Moving the Type 3S6 VARIABLE control from the CAL (detent) position affects the unit-of-measure lamp and the decimal neon of the digital unit. With the Type 230, the unit-of-measure lamp goes out, and the decimal shifts position. This will not happen when the Type 3S6 is operating from external programming.

Use of Smoothing

Time and amplitude noise may sometimes be objectionable when operating at minimum deflection factors or maximum sweep rates. For smoothing, turn the NORMAL/SMOOTH switch on the Type 3S6 to the SMOOTH position. This will reduce the random noise to about one-half the former value by decreasing the gain of the sampling feedback loop. Fig. 2-12 shows the advantage of using smoothing when observing a low-amplitude signal.

Dot Density. Normally the SMOOTH position of the NORMAL-SMOOTH switch will not significantly affect the rise-time of the display if the dot density is sufficient. If, however, the display wave shape is affected when the switch is changed from the NORMAL to the SMOOTH position, a compromise must be made between smoothing and dot density. Fig. 2-13 illustrates the effect produced by using smoothing when the dot density is low. This effect can be compared to the high dot density of the same input signal as shown in Fig. 2-12B.

Coaxial Cables

Signal cables that connect the vertical signal from the source to a 50 Ω input connector should have a characteris-

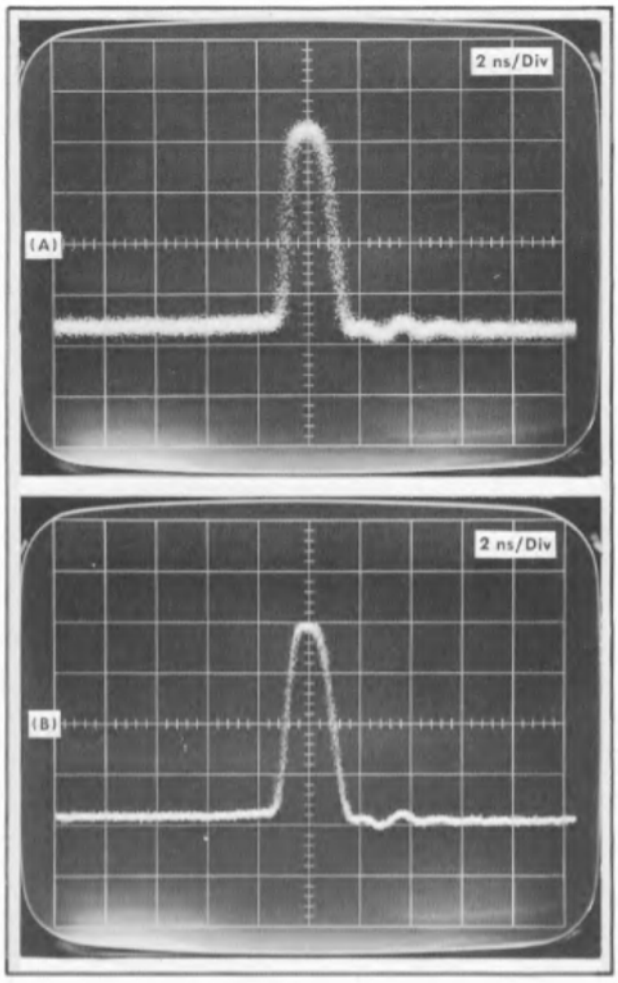


Fig. 2-12. Use the SMOOTH-NORMAL switch in normal process sampling for decreasing display noise when viewing a low-amplitude signal. (A) NORMAL-SMOOTH switch at NORMAL; (B) NORMAL-SMOOTH switch at SMOOTH.

tic impedance of 50 ohms. Impedance other than 50 ohms will cause reflections that may make it difficult to interpret the display. High-quality low-loss coaxial cable should be used to ensure that all the information obtained at the source will be delivered to the input. If it is necessary to use cables with a characteristic impedance other than 50 ohms, suitable impedance-matching devices will aid in obtaining meaningful displays.

The characteristic impedance, velocity of propagation and nature of signal losses in a coaxial cable are determined by the physical and electrical characteristics of the cable. Common coaxial cables, such as RG-213/U, have skin effect and with increasing dielectric losses which increase signal frequency. Some small diameter cables (1/8 inch) lose much of the high-frequency information of a fast risetime pulse in a very few feet of cable.

Losses of high frequency information can be shown with a fast-rise pulse generator and sampling system. Using a 5 ns delay RG-58/U coaxial cable as connecting cable, a display similar to Fig. 2-14A can be shown. Adding an additional 10 ns delay RG-58/U coaxial cable in the signal path results

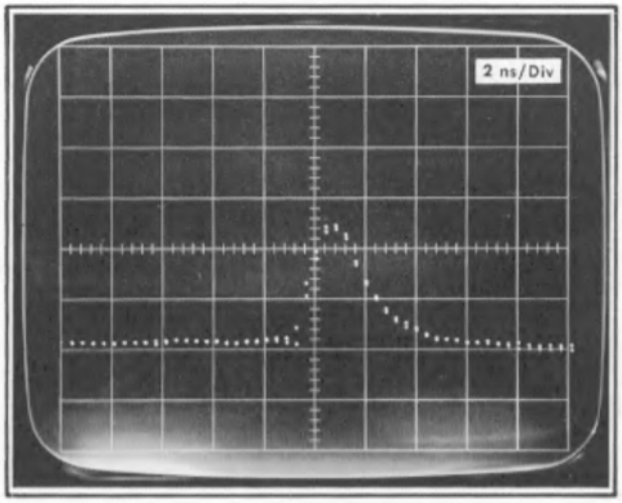


Fig. 2-13. Degraded display of signal shown in Fig. 2-12B, caused by use of smoothing with sampling sweep unit set for low dot density normal process sampling.

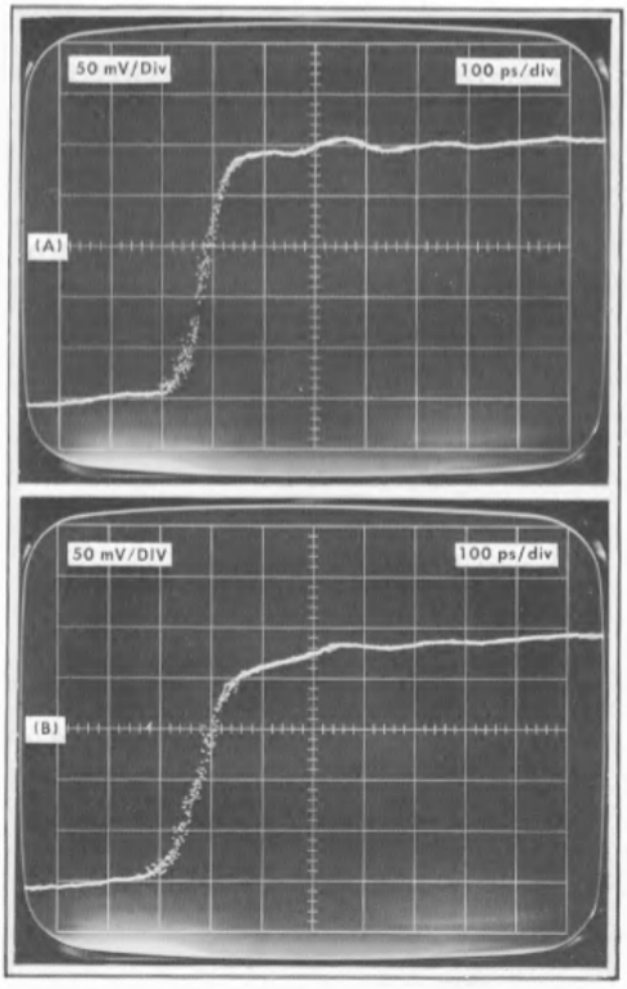


Fig. 2-14. Coaxial cable in a fast-rise system (A) using 5 ns-delay and (B) 15 ns-delay cable.

in a display similar to that of Fig. 2-14B. By using larger diameter, higher quality cable such as RG-213/U in the same system, less loss is shown with the same length of connecting cable. Tektronix Type 113 Delay Cable is a high quality, low loss cable with 60 ns signal delay.

Attenuating the Input Signal. The maximum signal amplitude that should be applied to the input connector of the sampling head will depend upon the sampling head installed in the Type 3S6. To attenuate the signals to 50 Ω input sampling heads, use an attenuator probe and/or external coaxial attenuators. The attenuators must have good frequency response beyond the frequency response of the sampling head to avoid reducing system performance. High quality coaxial attenuators are available through your Tektronix Field Office or Representative with attenuation factors such as 10×, 5× and 2×. When the attenuators are stacked their attenuation factors multiply; i.e., two 10× attenuators produce 100× attenuation. The 50 Ω attenuators must be matched to 50 Ω input and output impedance to provide their stated attenuation factor.

To divide a signal into two equal parts, and maintain a good 50 Ω impedance match, use a power divider such as GR 874—TPD, Tektronix Part No. 017-0082-00. The loss between any two of the power divider connectors is 6 dB (half voltage) when each connector has a 50 Ω circuit connected.

Passive Probes. The Tektronix P6034 10× Probe and the P6035 100× Probe are moderate-resistance passive probes designed for use with 50-ohm systems. They are small in size, permitting measurements to be made in miniaturized circuitry. Power rating is 0.5 watt up to a frequency of 500 MHz. Momentary voltage peaks up to 500 volts can be permitted at low frequencies, but voltage derating is required at higher frequencies. Characteristic data is given in the probe instruction manuals.

The P6034 10× Probe places 500 ohms resistance and less than 0.8 pF capacitance in parallel with the signal source at low frequencies. The probe bandwidth is DC to approximately 3.5 GHz, and risetime is 100 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 300 ohms and the capacitive reactance is about 400 ohms.

The P6035 100× Probe places 5 kΩ resistance and less than 0.7 pF capacitance in parallel with the signal source at low frequincies. Bandwidth of the probe is DC to approximately 1.5 GHz, and risetime is 200 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 2 kΩ and the capacitive reactance is about 450 ohms.

Built-in Probes. Another satisfactory method of coupling fractional nanosecond signals from within a circuit is to design the circuit with a built-in 50-ohm output terminal. With this built-in probe, the circuit can be monitored without being disturbed. When the circuit is not being tested, a 50-ohm terminating resistor can be substituted for the test cable. If it is not convenient to build in a permanent 50-ohm test point, an external coupling circuit, which may be considered a probe, can be attached to the circuit.

Several factors must be considered when constructing such a built-in signal probe. A probe is designed to transfer energy from a source to a load, with controlled fidelity and attenuation. Both internal and external characteristics affect its operation. It must be able to carry a given energy level, be mechanically adaptable to the circuit to be measured, and be equally responsive to all frequencies within the limits of the system. The probe must not load the circuit significantly or the display may not present a true representation of the circuit operation. Loading many even disrupt the operation of the circuit. When it is necessary to AC-couple the probe, the capacitor should be placed between the series attenuator resistance and the 50-ohm probe cable to minimize differences between the input characteristics with and without the capacitor. In a 50-ohm environment, stray capacitance to ground has a shorter and more uniform time constant than if the capacitor were placed at the signal source where the impedance is usually higher and sometimes of unknown value.

Fig. 2-15A shows the parallel method of coupling to a circuit under test. Resistor R_s is connected in series with the 50-ohm input cable to the sampling unit, placing R_s + 50 ohms across the impedance in the circuit. This method usually requires the use of an amplitude correction factor. In order to avoid overloading the circuit, the total resistance of R_s + 50 ohms should not be less than 5 times the impedance of the device (R_L in parallel with Z_o) requiring a 20% correction. The physical position of R_s will affect the fidelity of the coupling.

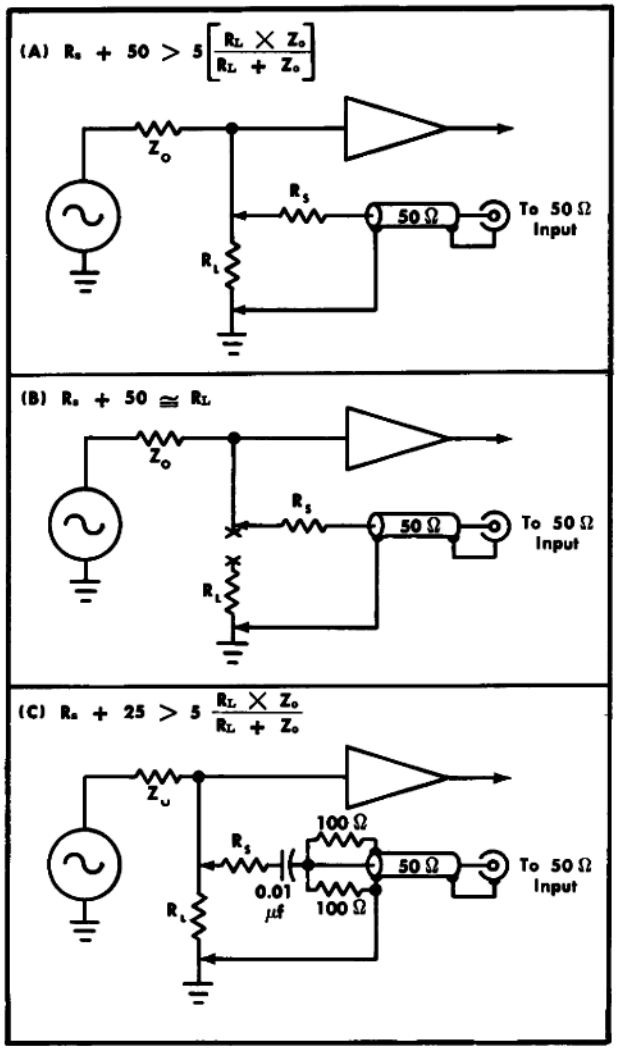


Fig. 2-15. Built-in probes for coupling to a test circuit. (A) parallel method; (B) series method; (C) reverse-terminated parallel method.

Fig. 2-15B shows the series method of coupling to a circuit. Resistor R_s plus the 50 ohm sampling head input resistance replaces the impedance of the circuit under test. If R_L is 50 ohms, simply substitute the 50-ohm test cable without R_s. It is best to locate R_s in the original position of R_L and to ground the coaxial cable where R_L was grounded.

A variation of the parallel method is the reverse-terminated network shown in Fig. 2-15C. This system may be used across any impedance up to about 200 ohms. At higher source impedances, circuit loading would require more than 20% correction. The two 100-ohm resistors across the cable input serve to reverse-terminate any small reflections due to connectors, attenuator, etc. The series capacitor, which is optional, blocks DC components and protects the resistors.

NOTES

SECTION 3
TEKTRONIX BASIC SAMPLING PRINCIPLES

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section provides a basic functional description of the vertical channels of sampling oscilloscopes. A discussion of equivalent-time sampling process is included. Operating instructions, including first time operation, are given in Section 2.

BASIC SAMPLING TECHNIQUES

The current state of the electronic art does not permit direct cathode-ray tube display of fractional-nanosecond risetime low-level signals. Risetimes in the order of 0.35 ns can be displayed on a CRT if the signal is at least several volts in amplitude.

An inherent limitation in linear amplifiers is the compromise necessary between bandpass and gain. A high gain amplifier is a low bandpass amplifier; and conversely, wideband amplifiers are necessarily low gain amplifiers. For any particular configuration, gain times bandpass is nearly a constant, so anything done to increase the gain will proportionately reduce the bandpass and vice versa. The gain-bandpass product limitation of linear amplifiers restricts the display of millivolt signals on a CRT to the 50 to 200 MHz region.

The sampling technique permits the quantitative display (on a CRT) of a facsimile of fractional-nanosecond risetime low-level signals. In sampling, many cycles of an input signal are translated into one cycle of low-frequency information. The change takes place at the input, or sampling bridge. Since only the sampling bridge is subjected to the input signal high frequencies, the performance of a sampling system is not dependent on the gain-bandpass limitations of conventional amplifiers.

However, the sampling technique introduces some limitations of its own. The sampling process being described is restricted to repetitive signals of low amplitude (typically 1 or 2 volts peak to peak), from low impedance sources. Fortunately, most fractional-nanosecond risetime signals exist in low impedance environments and are generally low amplitude. Piping the signal from the circuit under test to the input of the sampling oscilloscope vertical channel requires a more sophisticated technique than lower bandpass systems. In spite of its limitations, sampling can measure fast signals that otherwise defy observation.

A sampling system looks at the instantaneous amplitude of a signal during a specific small time period, remembers the amplitude, and displays a single dot on the CRT corresponding to the amplitude. After a dot is displayed for a fixed amount of time, the system again looks at the instantaneous amplitude of a different cycle of the input signal. Each successive look, or sample, is at a slightly later time in relation to a fixed point of each signal cycle. Each sample is displayed as a spot on the CRT. Generally the vertical position of the dot represents the equivalent time when the sample was taken. After many cycles of the input signal, the sampling system has reconstructed and displayed a single facsimile made up of many samples, each sample taken from a different cycle of the input signal.

Fig. 3-1 illustrates the equivalent time reconstruction of a repetitive square wave. The CRT display is a series of dots rather than the conventional oscilloscope continuous presentation. In the illustration, a series of samples is taken of the

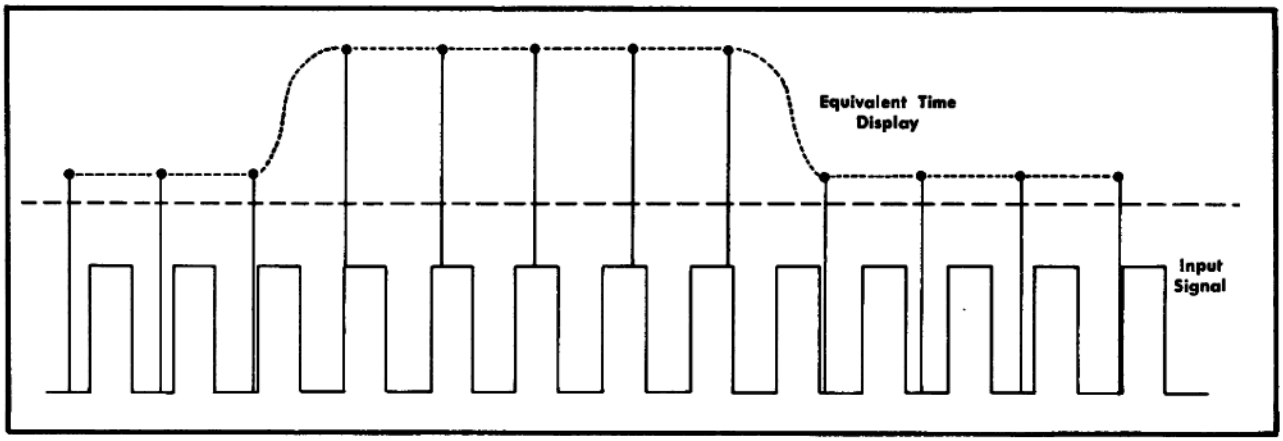


Fig. 3-1. Equivalent time display of repetitive real time signal by means of the sampling technique.

input signal. After each sample, when memory has been established and stabilized, the CRT is unblanked and a dot appears. A large number of such dots form the display.

The number of dots per horizontal unit of display is called dot density. The dot density of a display is controlled by the operator to provide the best compromise between resolution and repetition rate of the display. Since only one sample is taken from any particular input cycle, the time required to reconstruct a display is a function of the dot density selected and the repetition rate of the signal. The higher the dot density selected (for high resolution), the longer the time required to construct the equivalent time display. (The higher the repetition rate of the signal, the less time required to reconstruct the waveform limited by a maximum repetition rate of the system.)

Sampling requires repetitive input signals, though not necessarily signals with constant repetition rate. The equivalent time between dots is determined by the time delay between the fixed point on the signal at which triggering occurs, and the point at which the sample is taken. Since both time references (triggering-time and sample-time) are taken from the same cycle of the signal, the signal repetitions do not have to be identical in amplitude, time duration, and shape. Any differences in the individual cycles show as noise or jitter in the reconstructed display.

Sampling systems have maximum signal repetition rates at which samples can be taken and accurately displayed. The primary limit is the time required for the preamp and the AC amplifier to stabilize after a sample has been taken.

Signals below 100 kHz may have considerable repetition rate jitter and still the sampling oscilloscope will present a sample of each cycle, without display jitter. For signals with a repetition rate higher than 100 kHz, the timing unit holds off retriggering for a maximum of about 10 μs. This means that a sample will not be taken from every cycle of a high repetition rate signal. Only those cycles are sampled which occur after the end of the holdoff. If the signal is truly repetitive and each cycle is identical, these "missed" cycles are of little significance.

The circuits in the vertical channel of a Tektronix sampling oscilloscope comprise an error-sampled feedback system with ratchet memory. The memory output is not reset to zero after a displayed dot. The memory output remains at the displayed amplitude of each dot in succession until it is corrected by the next sample. The amplitude difference between the two samples is then the error between the memory output and the new sampled amplitude.

Fig. 3-2 shows a simplified block diagram of an error-sampled feedback system with ratchet memory. The output signal from the sampling bridges is the difference, or error, between the instantaneous amplitude of the signal at sample time and the previously memorized amplitude. A change is made to the memory output only when the instantaneous amplitude of the signal at sample time is different from the memory output. The memory output "ratchets" up or down at sample time as a result of the error signal sampled. The transition of memory from one output voltage to another occurs between displayed dots, and is therefore not seen on the CRT.

The error-sampled ratchet-memory technique has the advantage of allowing display noise to be "smoothed". Smoothing is discussed later in this section. The error-sampled approach also minimizes signal kickout into the input cable by the sampling bridge interrogate pulse (hereafter called "strobe" pulse). Since the sample is always the difference between the signal and the memory output, the error-signal and kickout are much smaller in amplitude than they would be if the memory output reverted to zero and the entire signal was sampled after each dot.

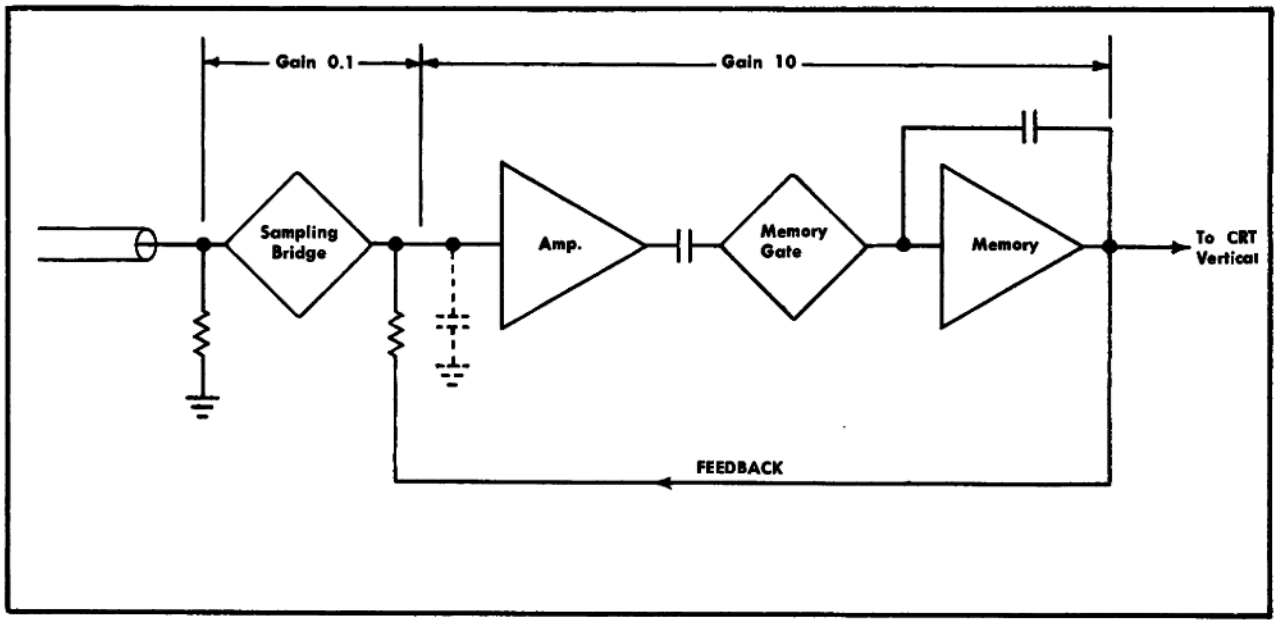


Fig. 3-2. Simplified block diagram of an error-sampled feedback system with a ratchet memory.

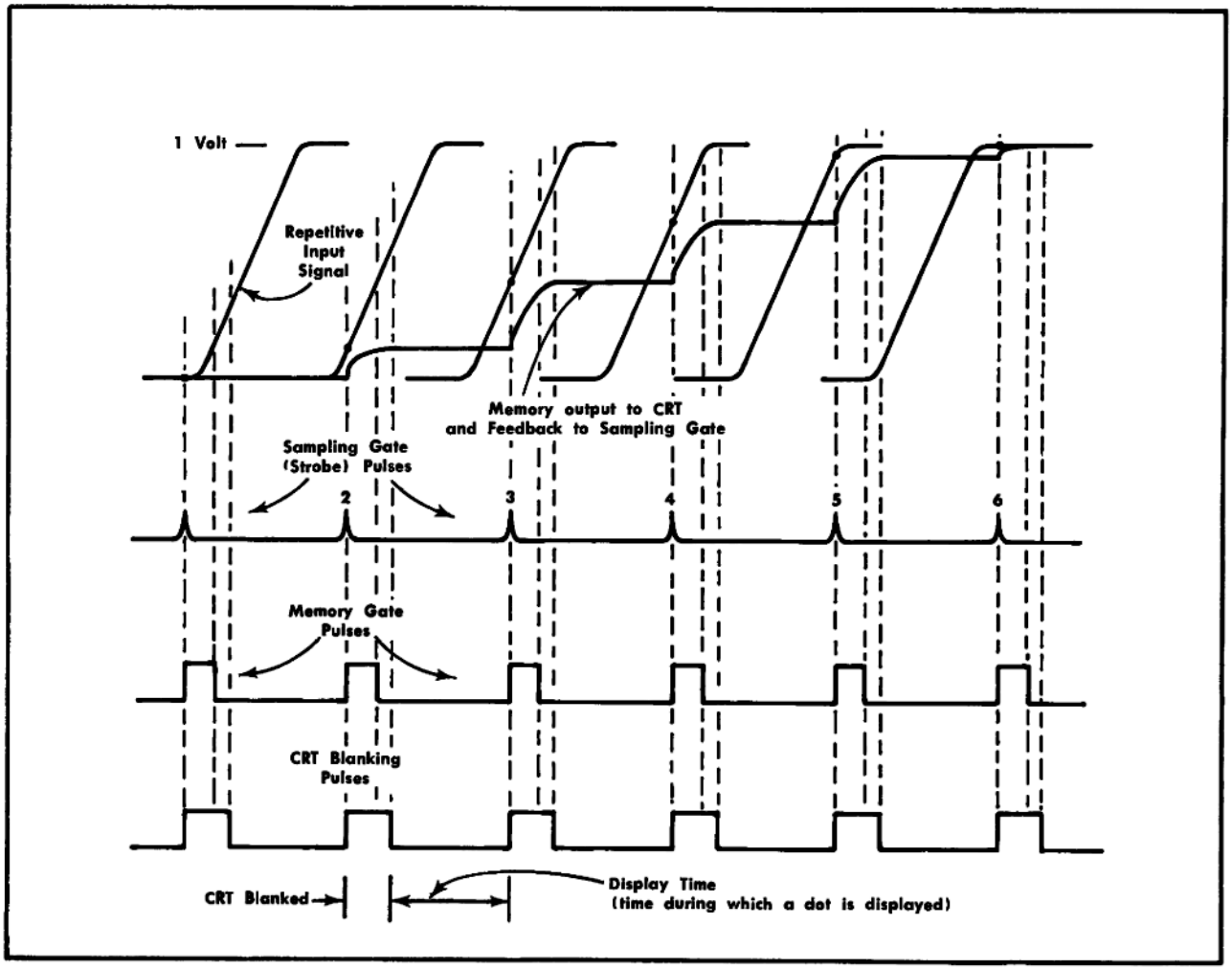


Fig. 3-3. Simplified representation of an error-sampled ratchet-memory waveform.

The output from the sampling bridge at sampling time is about 2% of the difference between the signal voltage and the memory output. The 2% signal is the input to the first amplifier. The output of the amplifier is AC-coupled to a memory gate. The memory gate couples the signal to the memory amplifier during the time it is gated on. The memory amplifier changes the memory feedback voltage to equal the signal voltage at the instant of sampling. These changes in memory output occur while the CRT is blanked, and do not revert to zero, but remain at a fixed voltage until corrected by the next error signal. (The signal to the amplifier of a typical sampling system is only about 2% of the error signal sampled by the bridge. The percentage of response, or attenuation through the sampling bridge, is the sampling efficiency.)

At each sample time the difference between the memory feedback and the 2% signal value is amplified and applied to the memory circuit via the memory gate, to correct the memory output to follow a rising signal in a series of steps as shown in Fig. 3-3. This figure shows the input signal and memory feedback voltages for six samples along the rise of a step waveform.

At the time of Sample 1, the input signal and feedback are equal. There is no error voltage, so the memory output is not changed. The CRT is blanked until the circuit stabilizes after the memory gate pulse ends.

At the time of sample 2, the input signal is (for example) 0.1 volt. The memory output is 0. Assuming a sampling efficiency of 10%, the input of the amplifier receives 10% of the error signal, or 0.01 volt. The 0.01 volt, times the gain of the amplifiers (×10) corrects the memory output and feedback to equal the 0.1 volt signal at sample time. Again, the CRT is blanked during this change until the circuit is stabilized.

At the time of sample 3, the difference between the input signal and the feedback is 0.35 volt. The amplifier input responds to 10% or 0.035 volt. The gain of the amplifier and memory changes the feedback 0.35 volt to the new value of 0.45 volt (equal to the signal at number three sampling time). The CRT is again blanked during this change until the circuit is stabilized.

This process continues until sample 7 (not shown). Here again, there is no difference between the input signal and the

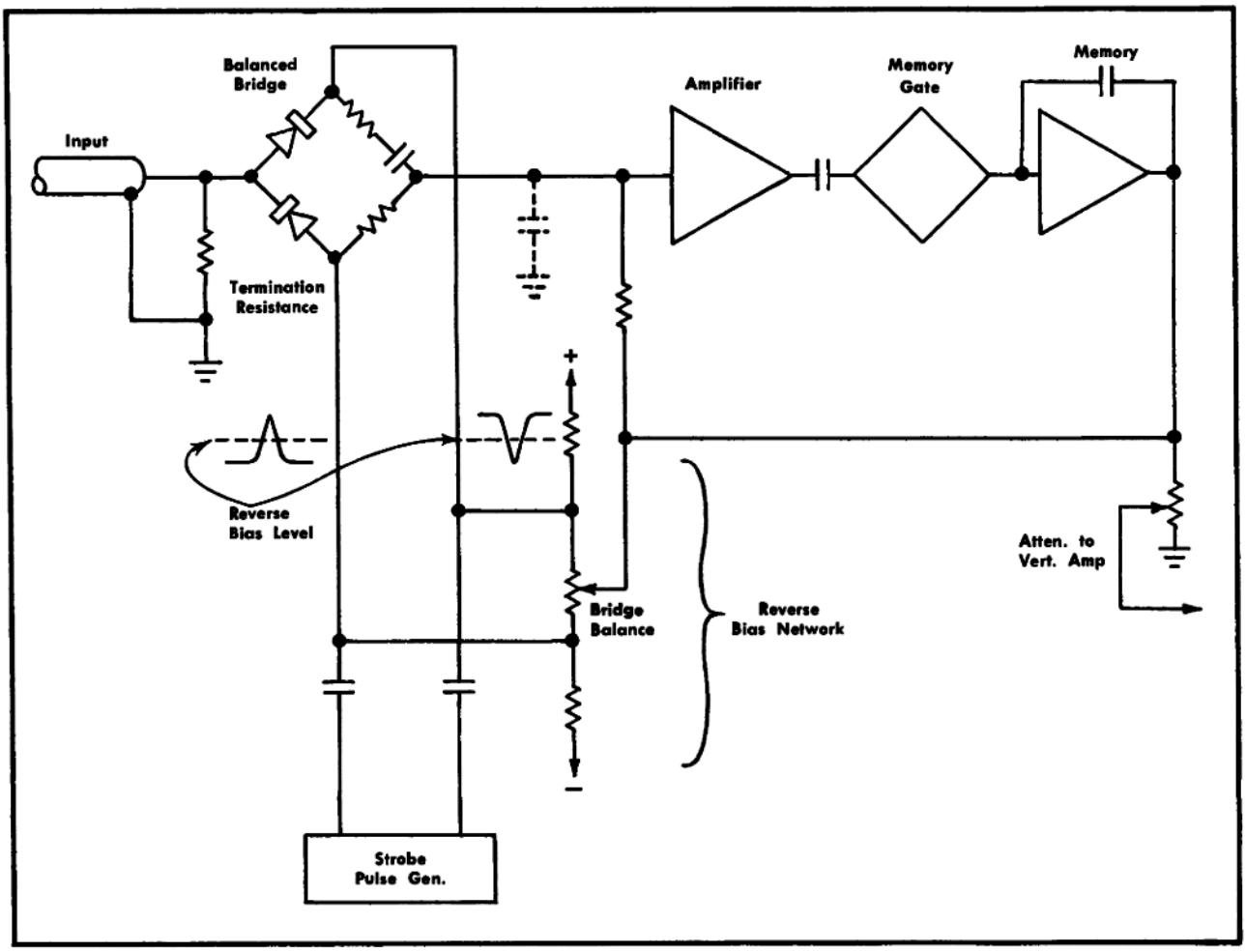


Fig. 3-4. Simplified diagram, showing how the strobe pulse causes the sampling bridge to conduct.

feedback. There is no error signal, and the memory output and feedback is not changed. The system will remain at this voltage until the input changes, or until system drift has caused an error in the memory output (if there is a long period of time between successive samples).

Effective Sampling Time

The minimum risetime a sampling system can display is controlled by the time interval during which the strobe pulse applies forward bias to the sampling bridge diodes. The duration of the bridge forward bias is controlled by the time the strobe pulse exceeds a fixed reverse bias. Special circuitry is used to make the strobe duration as short as possible consistent with noise and diode recovery time. The strobe pulse is generated by a snap-off diode and a short section of shorted transmission line called a clipping line. The effective bridge conduction time is adjusted primarily by controlling the amplitude and duration of the strobe pulse, thus controlling the time during which the strobe pulse exceeds the reverse bias. Adjusting the reverse bias is a secondary means of controlling the sampling bridge conduction time.

Fig 3-4 shows how the strobe pulse breaks through the reverse bias on the sampling bridge. The reverse bias is shown by dashed lines through the strobe pulses.

Dot Response (Loop Gain)

Dot response is a visual display of the ability of a system to reduce the error voltage to zero after each sample. When the gain of the memory feedback loop is equal to (and compensates for) the attenuation across the sampling bridge, the loop gain is unity or 1. In this case, the memory feedback voltage equals the value of sampling-time signal voltage.

If the loop gain is less than unity, the memory output signal and feedback to the first amplifier is less than necessary to reduce the error voltage to zero. The memory output and the feedback will then approach the signal asymptotically after several samples have been taken. The error voltage thus approaches zero (for a steady state signal) after several samples, being reduced by the same factor after each sample. In the case of a loop gain of less than unity, the feedback voltage is effectively a moving average of several preceding samples.

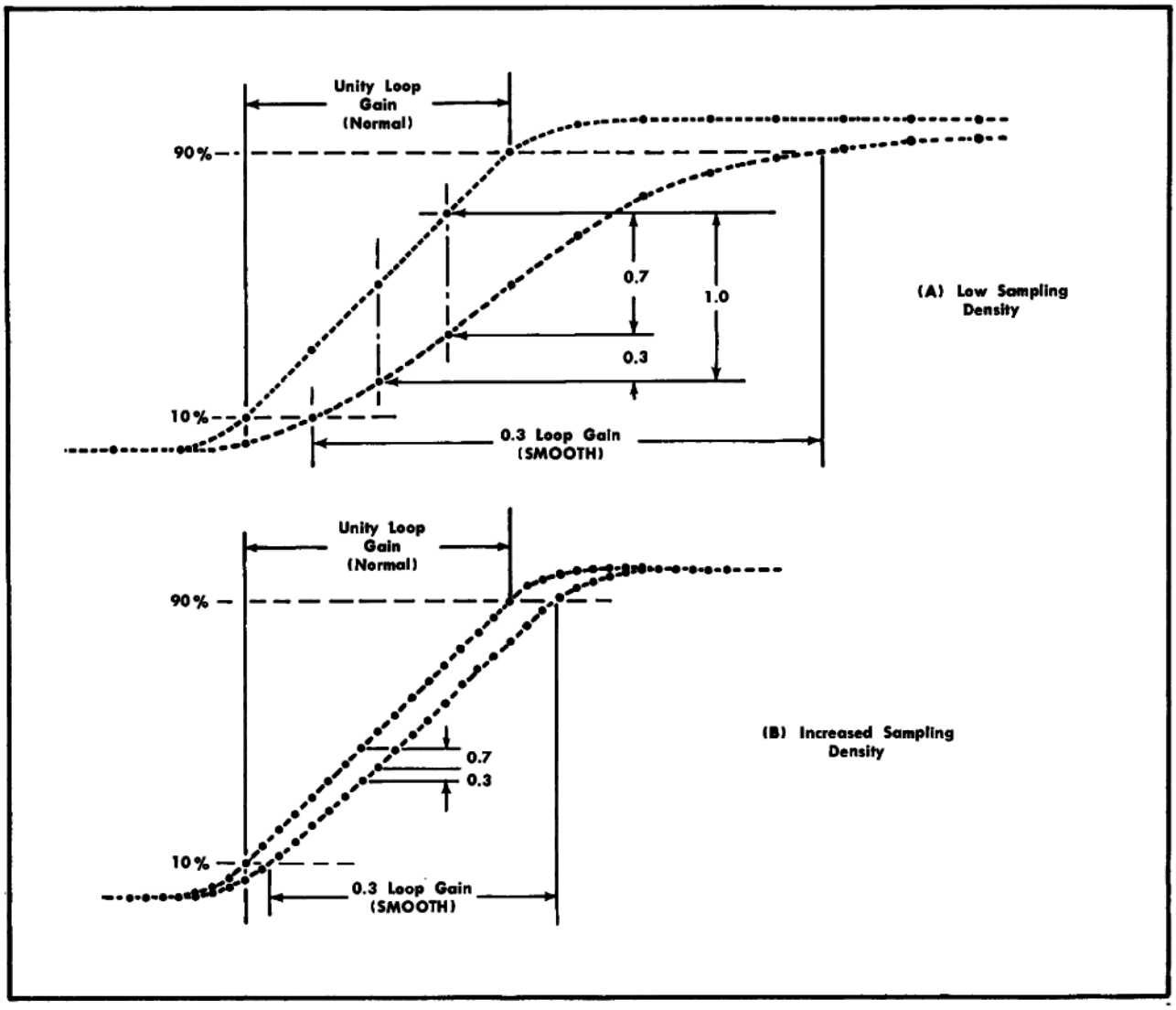


Fig. 3-5. Equivalent-time display with and without smoothing for two different sampling densities.

If the loop gain is greater than unity, the feedback voltage will be greater than the error signal after each sample. The displayed dot sequence of a step signal will then alternately overshoot and undershoot for a few samples.

For least displayed waveform distortion the loop gain must be unity, allowing the system to track the input signal as closely as possible.

Smoothing

A loop gain of less than unity can be useful, if the resulting compromise is understood and the system is operated properly. Random noise in the display is reduced when loop gain is less than unity, since several consecutive samples are averaged. The averaging may also slow down the fastest display risetime capability, depending upon the number of dots contained in the step transition and/or the loop gain. By increasing the number of dots in a step transition, the display will follow the actual step transition more closely.

Fig. 3-5 shows the usual effects on a step display when smoothing is used for two different sampling densities (sampling density or dot density is the number of samples or dots per horizontal division). In the Type 3S6 the operational choice of loop gain is either 1.0 (NORMAL) or 0.3 (SMOOTH). In Fig. 3-5A the actual risetime (between the 10% and 90% points) for unity loop gain displays 4 dots. When operating at 0.3 loop gain, 7 dots are shown. There is a significant difference between the 0.3 loop gain (SMOOTH) and the unity loop gain (NORMAL) displays.

In Fig. 3-5B the sampling density is increased, showing a difference of one sample in the SMOOTH and NORMAL positions between the 10% and 90% points of this step transition.

When the smoothed mode has a loop gain of 0.3, as in the Type 3S6, 15 or more samples between the 10% and 90% points of a risetime will result in the smoothed and unsmoothed displays having essentially the same risetime. When the smoothed display contains 12 samples between

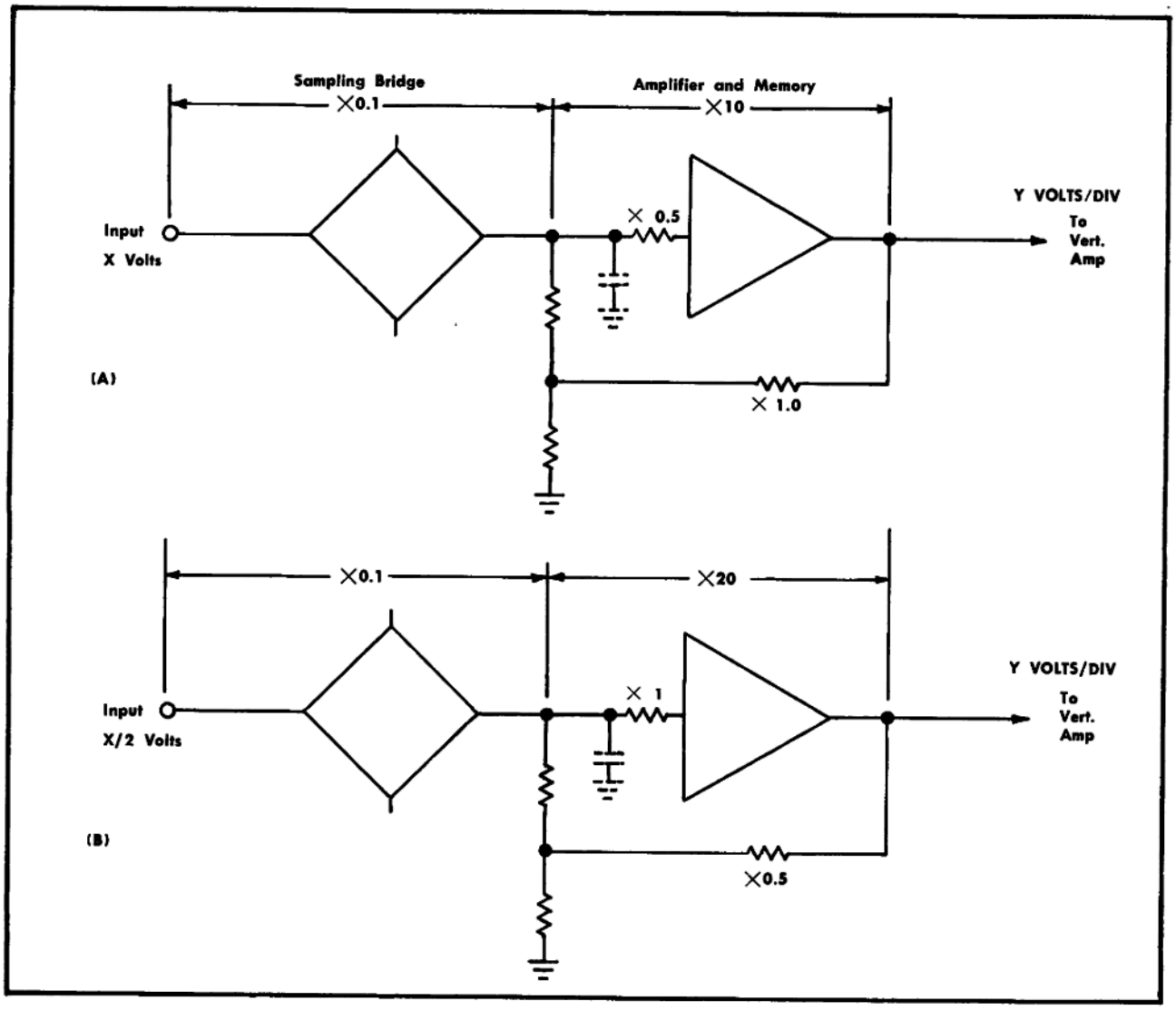


Fig. 3-6. Method of decreasing the vertical deflection factor while maintaining unity loop gain.

the 10% and 90% points, the smoothed risetime will be about 6% longer than for the unsmoothed display. As the number of samples contained in the risetime is reduced below 12, the difference between smoothed and unsmoothed displays goes up rapidly.

Smoothing of Random Noise

When the loop gain is reduced to 0.3, the displayed dots represent the average of several consecutive samples. Noise of a random nature will be materially reduced in the display at the possible expense of introducing an error in the displayed risetime. Therefore, if random noise is apparent, reducing loop gain may improve the display. Note that this is only true for random noise. Systematic noise (noise with its repetition rate harmonically related to the signal) is treated as part of the signal.

The Type 3S6 has a loop gain control labeled NORMAL-SMOOTH. In the SMOOTH mode, loop gain is reduced to 0.3. Always check that there is sufficient sampling density to warrant smoothing. This can be done by changing the dots/division (or samples/division) control on the timing unit and observing the effect of sampling density on the displayed risetime.

Smoothing cannot be applied where the full amplitude of each sample is required. When using the random sampling process of a sampling sweep unit like the Type 3T2, each sample requires unity loop gain. The display dots are not presented in time sequence, and therefore cannot be averaged.

Tangential Noise

Traditionally the amplitude of random noise in an amplifier is qualified by stating the equivalent RMS value of the noise referred to the input of the amplifier. In the case of a CRT sampling display, qualifiying the noise amplitude by

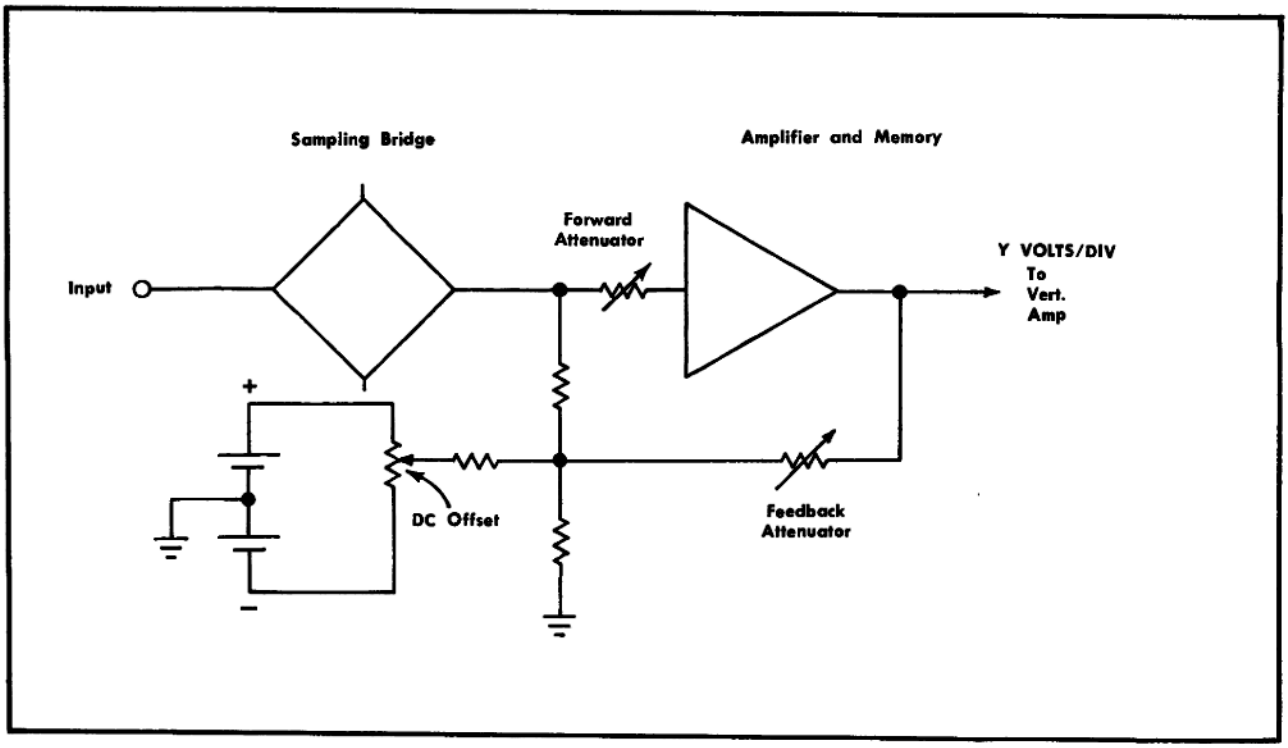


Fig. 3-7. Method of adding a DC Offset voltage to the memory feedback.

stating its RMS value is somewhat unsatisfactory. The visible effect of the random noise is more nearly 3 times the RMS value of the noise. Peak-to-peak limits of truly random noise would have to be stated as — infinity to + infinity. Obviously these broad limits would reveal nothing about the amount of significant noise to expect in a display. It has been determined empirically that 90% of the dispersion caused by random noise closely approximates the visible widening of the trace. The noise can be described as existing between two horizontal tangents representing the significant upper and lower limits of the trace width. Hence, the term TANGENTIAL NOISE. Tangential noise is defined as an equivalent peak-to-peak voltage at the input of a sampling system that will cause the same trace widening as 90% of the random noise. 5% of the dots can be expected to fall above the trace width and 5% below it. This method of stating the noise figure of a sampling system is considered to be more meaningful than the RMS value, in that it more closely approximates the actual observed trace widening. Measurement of Tangential Noise is described in Section 6.

Display Sensitivity—Deflection Factor

The two terms display sensitivity and deflection factor are often mistakenly interchanged. Deflection factor is defined as the ratio of the input signal amplitude to the resultant displacement of the indicating spot. When the oscilloscope vertical gain control is calibrated in volts per division, it is indicating deflection factor. Deflection sensitivity is the reciprocal of deflection factor. Sensitivity is indicated by a vertical gain control calibrated in divisions per volt.

There is always some point within the oscilloscope vertical amplifier after which the signal remains at a fixed deflection factor. The signal out of the vertical memory amplifier of a sampling oscilloscope is usually the first point at which the standard vertical deflection signal exists. Thus, the memory and feedback voltages previously mentioned always deflect the CRT spot vertically with a fixed deflection factor.

Fig. 3-6A shows a simplified block diagram of a bridge and amplifier combination where the gain of the amplifier just compensatets for the attenuation of the sampling bridge. In Fig. 3-6B the amplifier has twice as much gain as is necessary to compensate for the low sampling efficiency. By introducing a 2:1 attenuator in the feedback path between the memory output and the bridge output, the loop gain is still maintained at unity. Now, only half as much input signal produces the same memory output as in Fig. 3-6A.

Fig. 3-6 shows two fixed attenuators in each example. The usual method of changing amplifier and memory gain in a sampling unit is to attenuate the signal through (or to) it. The attenuator in series with the amplifier and memory is called the forward attenuator, in contrast to the feedback attenuator.

The attenuators in Fig. 3-6 and Fig. 3-7 show that both the "forward gain" and the "feedback attenuation" are altered when changing a sampling system vertical deflection factor.

The system deflection factor can be altered two ways: 1) by changing both the forward and the feedback attenuation and thereby maintaining the same loop gain, and 2) by

changing only the feedback attenuation, at the expense of varying the loop gain. If loop gain is not greater than unity, and many samples are included in a signal transition, the memory feedback to the sampling bridge always approaches the signal amplitude, regardless of the forward attenuator attenuation ratio.

Since loop gain is determined by the combined forward and feedback attenuation ratios, the loop gain can be altered without altering the deflection factor by changing the forward attenuation only. Increasing the forward attenuation ratio (decreasing the amplifier and memory gain) "smooths" the display by making the loop gain less than unity.

DC Offset

Since the sampling bridge can operate over a range of +2 to —2 volts of input signal, and the system has resolution capability of 2 mV/div, it is advantageous to be able to display a small vertical "window" of the input signal. Fig. 3-7 shows the method of adding a DC offset voltage to the memory feedback. The error signal produced at sampling time is no longer referenced to ground. Instead, it is referenced to the DC offset voltage.

A DC Offset voltage is recognized as a signal by the sampling bridge, algebraically adding it to the error signal. Therefore, the memory feedback signal in a system with DC Offset includes a DC value to cancel the DC Offset voltage at the output side of the sampling bridge. The deflection factor of a system with DC Offset is centered around the DC Offset voltage instead of ground. This permits portions of the signal (other than ground) to be positioned to the CRT center, without altering the deflection factor.

SECTION 4
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains a block diagram description and circuit description of the Type 3S6 Sampling Unit. The block diagram description is an expansion of Section 3, Basic Sampling Principles. The circuit description follows the sequence of diagrams at the back of this manual.

The Digital Unit Control circuits are described in Section 5, Digital Unit Control Description.

BLOCK DIAGRAM

Refer to Fig. 4-1 and the complete block diagram at the back of this manual during the following description. Since most of Channel A and Channel B are identical, no reference is made to either channel except where they differ. Channel A occupies the top half of the block diagram.

Fig. 4-1 includes a simplified block diagram of a typical sampling head. The Type 3S6 Sampling Unit serves no useful purpose by itself, but functions as part of a sampling system only when a sampling head is connected. Therefore, the sampling head simplified blocks are included.

Feedback Loop and Pulse Amplifier Chain

Fig. 4-1 relates to Fig. 3-4 and Fig. 3-7. The reconstructed signal of the Memory block (Fig. 4-1) is the first point in the Type 3S6 at which the amplitude is always a standard value of 0.5 volt per CRT vertical division. The signal between the sampling head output and the Memory output bears no similarity to the signal at the Memory output. Under ideal conditions, there is no signal between those two points whenever the sampling head input signal is at a steady value. The Post Amplifier, AC Amplifier and Memory Gate all are part of a pulse amplifier chain that amplifies the sampling head output signal just after each sample is taken. The pulse chain signals are greatest in amplitude when the sampled signal is at its full amplitude difference from the last sample (as in using the random sampling process in the Type 3T2 Random Sampling Sweep unit).

The smoothing, DC Offset, and the Units/Div circuit can be externally programmed when the Vertical Mode Switch is in the EXT PROG position. Programming is accomplished by connecting the program lines to ground at Pin A (rear panel) through saturated transistors or other closure types of programmers described in the Operating Instructions, Section 2.

Type 3S6 provides connections at J13 rear connector for all connections to the sampling head. From J13, connections are made to the logic control circuits to select the Units/Div Multiplier and the units of measure (Volts or Amps). These connections provide information to an external digital unit as described in Section 5, Digital Unit Control Description.

To complete the association in Fig. 4-1 with Section 3, the following describes the operating cycle:

a. The sampling head bridge applies an error signal to the head preamp whenever there is a voltage difference at the bridge input and output terminals at sampling time. The error-signal voltage amplitude is just a few per cent of the difference (sampling efficiency), and the pulse duration out of the bridge is equal to the bridge conduction time. A small storage capacitance at the head preamp input time-stretches the pulse so the pulse chain can amplify the error signal pulses at moderate rates of rise.

b. The time-stretched signal is amplified by the Type 3S6 Post Amplifier. Its gain is affected by the Smoothing circuit which operates in either the smooth or normal modes. The SMOOTH or NORMAL operation can be programmed externally in the EXT PROG position of the vertical Mode switch, or controlled from the front panel by the SMOOTH-NORMAL switch. In the Normal mode, the DOT RESPONSE control allows a small adjustment of the Post Amplifier gain to obtain unity loop gain. In the Smooth mode, the DOT RESPONSE control is disconnected. This reduces the Post Amplifier gain so that the sampling loop operates at about 0.3 of the gain in the Normal mode. The output of the Post Amplifier is capacitively coupled to the AC Amplifier and Forward Attenuator.

c. The AC Amplifier and Forward Attenuator block is an AC amplifier with its gain determined by the ratio of the feedback resistance to the selected input resistance. The Units/Div switch or external program, (through the Attenuator Decoder block) selects the input resistance and feedback circuit of the AC Amplifier. The attenuated or amplified pulse is applied to the Memory circuit during conduction time of the Memory Gate.

d. The Memory circuit applies its output voltage to both the vertical amplifier and the Feedback Attenuator block.

e. The Feedback Attenuator block attenuates the standard 0.5 Volt/Div signal from the Memory circuit and feeds it to the sampling head. Here the feedback voltage is combined with the DC Offset voltage and applied to the output side of the sampling bridge through the bridge balance circuit. The Units/Div switch or external program (through the Attenuator Decoder block) selects the attenuation of the Feedback Attenuator. The forward Attenuator operates concurrently with the Feedback Attenuator to maintain constant loop gain.

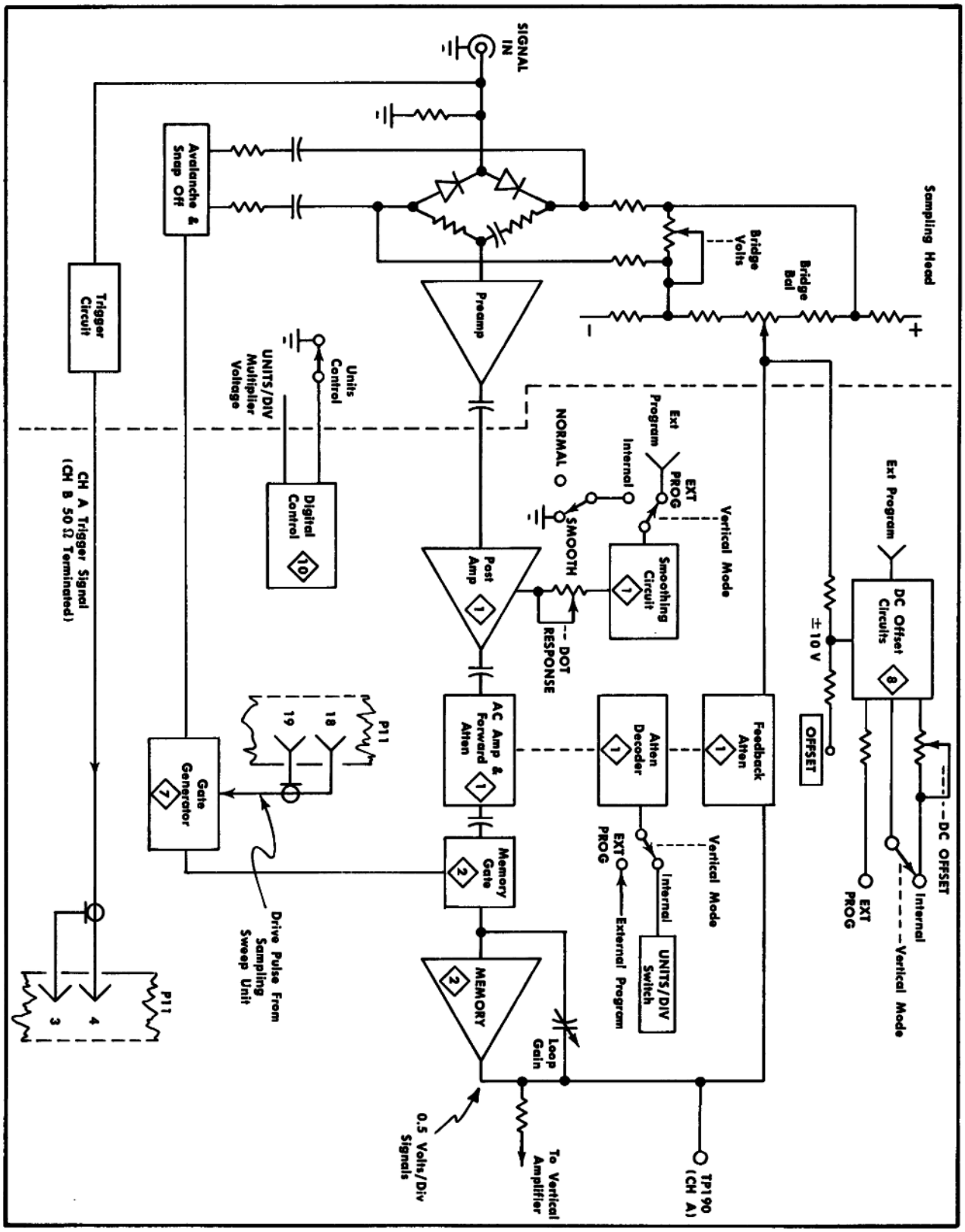


Fig. 4-1. Type 3S6 and sampling head feedback loop diagram.

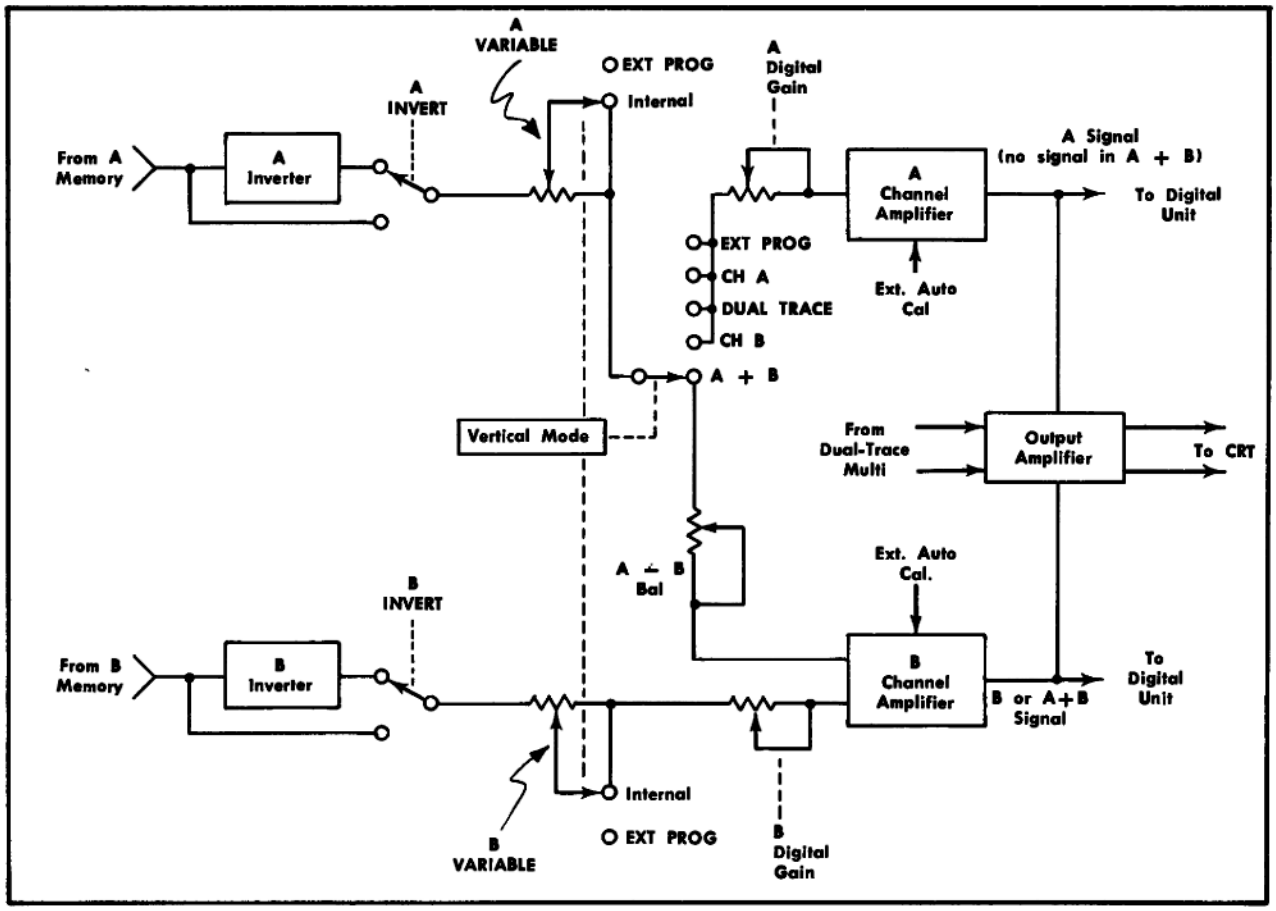


Fig. 4-2. A and B Vertical Channel block diagrams following the Memory showing A + B mode signal connections.

Vertical Channel Following Memory

Blocks between the Memory and the CRT (see Fig. 4-2) include the inverter and the INVERT switch, the Units/Div VARIABLE control and internal Digital Gain control, the Channel Amplifier and the Output Amplifier with its input controlled by the Dual-Trace Multi. The Output Amplifier drives the indicator oscilloscope CRT vertical deflection plates directly.

The Inverter is a ×1 gain inverting amplifier that is normally in the circuit. The Inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Channel Amplifier is a ×2 gain inverting amplifier with both the Units/Div VARIABLE and Digital Gain controls in series with the signal input.

During external program operation, the Units/Div VARIABLE control center arm is disconnected and does not operate. With external automatic calibration equipment connected to the proper pins of the external program connectors, the Channel Amplifier gain can be changed over a small range for calibration to a standard input signal. Except in A+B operation, the A and B Digital Gain controls allow the gain to be adjusted for a digital readout unit. (Channel A signal is disconnected in A+B operation.)

In the A+B position of the Vertical Mode switch, the B Channel Amplifier is driven by both Channel A and Channel B signals, providing algebraic addition displays. The A-B Bal control allows the Channel A signal to be balanced with the B signal in the A+B position.

NOTE

The Channel Amplifiers drive the Output Amplifier and provide a signal output for a digital readout amplitude measurement.

The Output Amplifier is a high gain inverting amplifier that drives the CRT vertical deflection plates directly. The input is from either Channel A or Channel B, selected by the Dual-Trace multi. The multi control circuit selects one channel continuously (CH A or CH B), alternates between channels after each sample (Dual-Trace and EXT PROG), or selects Channel B for algebraic addition (A+B).

The Position Lamp Driver circuit (not shown on the block diagram) monitors the DC voltage of the Output Amplifier lines and turns on the appropriate neon lamp to indicate whether the deflection voltage has placed the trace above or below the graticule center.

Gate Generators

The Type 3S6 Gate Generator blocks consist of a Blocking Oscillator, Dual-Trace Driver, and two Strobe and Memory Gate Drivers. The Sampling Drive pulse from the sweep unit drives the Blocking Oscillator, which then drives the Dual-Trace Driver and both Strobe and Memory Gate Driver blocks.

Since the Type 3S6 will operate with several different sampling sweep units, the Gate Generator is designed to operate from slightly different Sampling Drive pulses. The Blocking Oscillator converts the normal variations in amplitude, risetime and duration of the Sampling Drive pulses to a standardized drive pulse with always the same amplitude, risetime and duration.

The Blocking Oscillator output pulse is converted to an RC ramp signal at both Delay circuits, and the (internal) A Delay and (front-panel) B Delay controls select a point along each ramp at which the Strobe Drive is generated. As the individual channel Strobe Drive is generated, the Memory Gate Driver causes the same channel Memory Gate to conduct. The duration of Memory Gate conduction is controlled by the Memory Gate Width control. Thus, a few nanoseconds after the arrival of the Sampling Drive pulse, a Strobe Pulse is sent to the sampling head, and the Memory Gate is driven into conduction. The instrument is calibrated so the B DELAY control alters the time of the Channel B Strobe Drive pulse approximately ±5 ns with respect to the Channel A Strobe Drive pulse (when both sampling heads are the same type).

The Dual-Trace Driver circuit drives both the CRT blanking circuit (to extinguish the CRT beam while the dot is being moved between samples) and the Dual-Trace Multi. If the Vertical Mode switch is at DUAL-TRACE or at EXT PROG, the Dual-Trace Driver causes the Dual-Trace Multi to change state at the time each sample is taken.

Internal Trigger

The Type 3S6 couples a Channel A sampling head internal trigger pickoff signal directly from J13 (rear panel sampling head interconnector) to P11 (indicator oscilloscope horizontally mounted interconnector) through a short section of coaxial cable. P11 couples the Channel A internal trigger signal through the indicator oscilloscope J11 directly to the sampling sweep unit rear panel interconnector. The Channel B sampling head trigger pickoff circuit is terminated in 51 Ω at the Type 3S6 rear panel J13 connector. Internal triggering is thus possible only from Channel A sampling heads that contain trigger pickoff circuitry.

CIRCUIT DESCRIPTION

The following circuit description sequence follows the order of the diagrams in Section 10.

Programmed Amplifiers and Attenuators

The Programmed Amplifiers and Attenuators diagram for each channel includes the Post Amplifier, Smoothing, AC Amplifier, Forward and Feedback Attenuators, and Attenuator Decoder circuits. The Forward Attenuator is described as part of the AC Amplifier. The Feedback Attenuator circuits include a ×2 gain operational amplifier. Where the two channels are identical, the operation of only one is described. Differences between the channels are discussed in detail.

The Post Amplifier is a two-stage non-inverting operational amplifier with complementary emitter followers at the output. Low output impedance drives the Forward Attenuator resistors of the AC Amplifier. The input resistance of R13 (CH A) terminates the coaxial cable feed from the sampling head preamplifier. The coaxial cable shield is DC isolated from ground to provide a Units/Div Multiplier control connection from the sampling head to the Digital Unit Control circuits. The gain of the Post Amplifier is changed by varying the resistance of R9 or disconnecting R9 to change the feedback. The Smoothing circuit has two modes of operation, Normal and Smooth. In the Normal mode Q8 is saturated, allowing the DOT RESPONSE control to adjust the gain of the Amplifier. In the Smooth mode, the DOT RESPONSE control is disconnected by cutting off Q8. This increases the feedback and decreases the gain of the Post Amplifier. Total Post Amplifier AC gain (in Normal mode) with unity loop gain is approximately 11, producing a 2.2 volt output signal at TP25 for a 0.2 volt input signal at Q15 base. DC gain is about two, and DC feedback keeps the Amplifier within its proper dynamic range.

Q15 and Q16 provide voltage gain while Q19 and Q22 are the output emitter followers. Q19 assures low output impedance for positive output signals, and Q22 provides low output impedance for negative output signals. Each emitter follower has a resistor in the collector for parasitic oscillation suppression. C20 permits the output emitters to be at different DC voltages.

The Smoothing function is either internally or externally controlled, depending upon the position of the Vertical Mode switch. For front-panel operation of the NORMAL/SMOOTH switch, the switch is an open circuit at NORMAL and grounds the Smoothing circuit input at SMOOTH.

At NORMAL, R3, R4 and R5 bias Q6 to cutoff and R7 biases Q8 on to saturation. The low saturation resistance of Q8 connects one end of the DOT RESPONSE control (R9) to ground. This connects R9 in parallel with R10 in the Post Amplifier AC feedback circuit. C11 is allowed to bypass more signal, thereby reducing the AC feedback. Thus, the Post Amplifier gain can be adjusted over a small range by the DOT RESPONSE control.

When the NORMAL/SMOOTH switch is at SMOOTH, D3 conducts and R4 biases Q6 to saturation. Q6 collector voltage turns Q8 off, disconnecting the DOT RESPONSE control from ground. With R9 disconnected, R10 resistance in series with R11 and C11 increases the Post Amplifier AC feedback voltage and thus decreases the gain. This reduces the sampling loop gain of the Type 3S6 to 0.3 or less compared to the loop gain at NORMAL.

External programming of the Smoothing circuit merely duplicates the NORMAL/SMOOTH switch functions when the Vertical Mode switch is at EXT PROG. A logical ONE or a ground closure programs the SMOOTH mode and a logical ZERO or an open circuit programs the NORMAL mode.

The AC Amplifier and Forward Attenuators consist of an inverting operational amplifier with complementary emitter follower output circuit. The AC Amplifier gain is changed whenever the Units/Div switch (or external program) is changed. Control is by FET switched input resistors together with a transistor-switched feedback circuit.

The gain change function of the amplifier is called the Forward Attenuator because it affects the signal amplitude

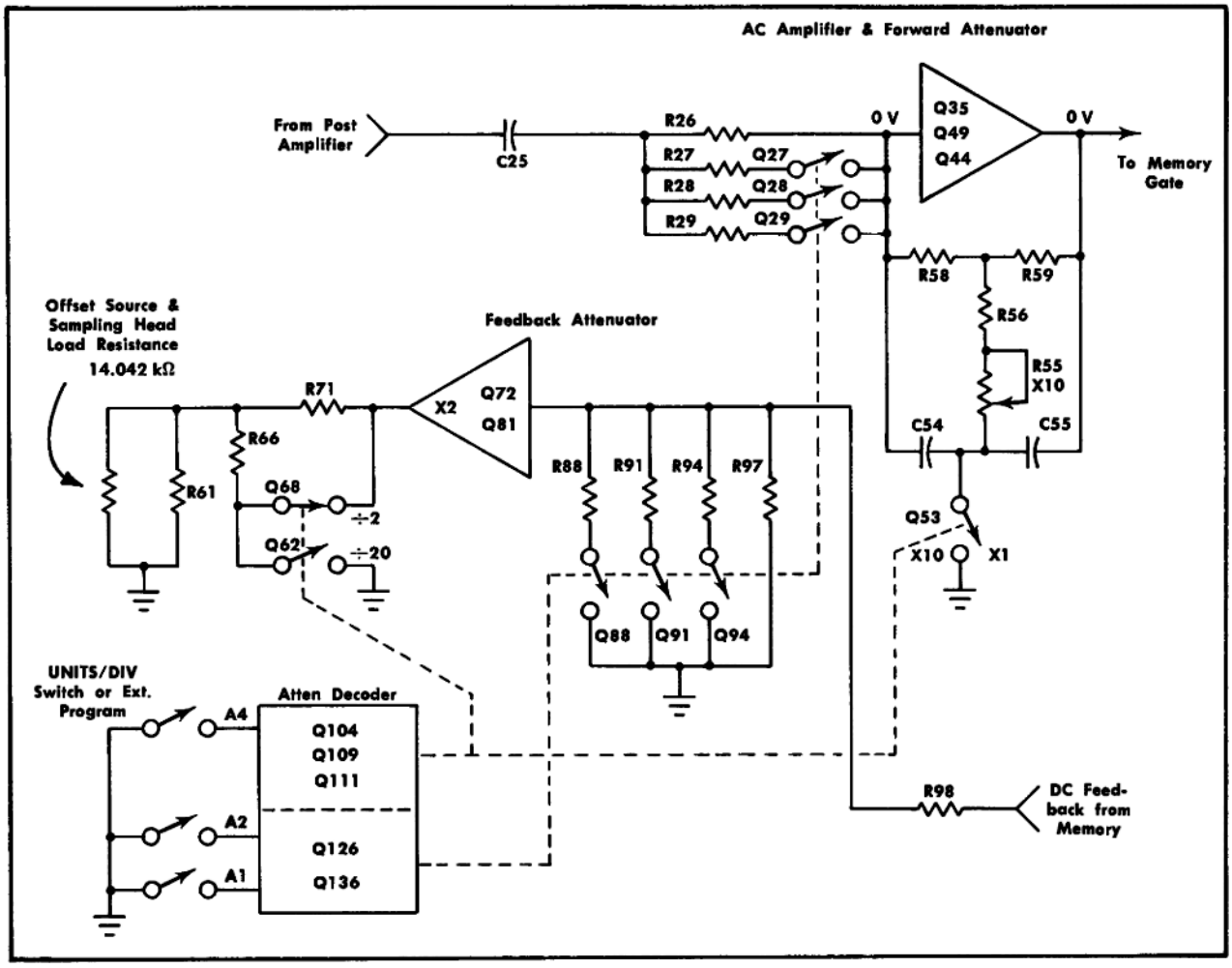


Fig. 4-3. Simplified Programmed Amplifiers and Attenuator diagram.

through the circuitry from the Post Amplifier to the Memory input. Fig. 4-3 shows the AC Amplifier input resistors R26 through R29. R27, R28 and R29 are connected into the circuit by Q27, Q28 and Q29 (shown as switches in Fig. 4-3) to change the input resistance and thereby the gain. These FET's are held at low resistance conduction (less than 30 Ω) or at cutoff by the Attenuator Decoder circuit (from logic lines A1 and A2). The A4 line (through the Attenuator Decoder block) controls the AC Amplifier feedback network by turning Q53 on or off. Q53 saturation increases the gain of the amplifier ten times by reducing the feedback to 0.1 its normal value. The feedback circuit consists of R59-C55, R58-C54 and R55-R56. The Decoder circuits operate the Feedback Attenuator circuits simultaneously so that the sampling loop gain is maintained constant. (See Section 3 for loop gain relationship between forward and feedback attenuators).

Schematic diagram 1 has truth tables in the AC Amplifier section showing the relationship between the lines A1, A2 and A4, and the transistors' on-off states.

At quiescence, the base of Q35 in the AC Amplifier is at 0 volts. Temperature compensation for Q35 is provided by D37. Q35 collector voltage is about +10 volts, and Q49 emitter follower output is slightly negative (between —0.25 V and ground). 0 volts input (at Q35 base) allows Q27, Q28 and Q29 to be biased off or on by the Attenuator Decoder circuits. When Q53 is turned on to change the gain of the AC Amplifier, Q53 connects the center of the feedback circuit to ground with about 125 Ω (R55 and R56). This causes only about 0.2 volt shift in the output quiescent voltage. R55 is adjusted for a gain increase of exactly ×10 when Q53 is saturated.

Two possible Q111 collector voltages of —24 or +7 V control Q52 and turn Q53 on or off. Operation is as follows: When the collector of Q111 is at +7 volts, R51 and D51 back bias Q52 by about 0.5 volt. With Q52 off, R53 turns Q53 on. The —24 volts from Q111 collector saturates Q52. This sets Q53 base positive and turns off Q53.

The summing input of the AC Amplifier (at Q35 base) receives both the input signal from the Post Amplifier (through C25 and the FET-selected input resistors) and the feedback signal from the feedback network. Q35 amplifies the signal and drives the bases of emitter followers Q49

and Q44. Q49 provides a low output impedance for positive signals and Q44 provides a low output impedance for negative signals. Q44 is AC-coupled to the output by C47. R48-C48 and R45-C45 are power supply decoupling networks in the collector circuits of Q44 and Q49. D42 protects Q44 base-emitter junction if Q35 is removed from its socket. The low output impedance of the AC Amplifier is required to drive the Memory Gate circuit for full screen transitions.

The Feedback Attenuator circuit consists of a selectable attenuator network at the input of a non-inverting ×2 gain operational amplifier (Q81-Q72) and a divide-by-two or divide-by-twenty divider network between Q72 and the sampling head. See Fig. 4-3. Attenuator resistors are changed by special low resistance FET transistors, drawn as switches in Fig. 4-3. The ×2 amplifier low output impedance drives the divider network R71, R66, R61 and 14.042 kΩ. The 14.042 kΩ consists of the Offset circuit output resistance in parallel with the sampling head bridge volts circuit resistance.

The CH A (CH B) Programmed Amplifier and Attenuators diagram shows truth tables listing the feedback attenuation as a percentage of the Memory DC output voltage. The input to the Feedback Attenuator at point (A) is the Memory signal at the standard deflection factor of 0.5 volt per displayed division. The truth table shows the percentage of memory output signal that reaches Q81 base at point (B). Q88-Q91 and Q94 turn on and ground appropriate attenuator resistors as a function of the program applied to the A1 and A2 lines, altering the signal at point (B). The output signal at point (C) is also included in the truth tables as a percentage of the voltage at (A). Q62 and Q68 turn on alternately and ground appropriate attenuator resistors as a function of the program applied to the A4 line. Point (C) voltage provides current through R71 and/or R66 to the DC Offset and sampling head circuits so that the voltage across R61 is held at about zero with no sampling head input signal.

Q72 and Q81 operate as a ×2 gain, non-inverting operational amplifier between the two attenuator networks. R75 and R79 (both 0.1% tolerance resistors) set the gain at ×2. The amplifier has high input resistance at Q81 base, and very low output impedance at Q72 collector. This low output impedance drives the 2×/20× divider network.

The collector signal of Q81B drives Q72 base. Q72 collector drives the output and provides a feedback signal to Q81A base through R75 and R79. The common emitters of Q81 complete the feedback path and provide temperature compensation. All quiescent base current of Q81B passes through R85, and all quiescent base current of Q81A passes through R78. Base currents from both halves of Q81 pass through Attenuator Zero control, R86. R86 is adjusted during calibration so that Q81 base currents do not offset the Memory output signal as it passes through the Feedback Attenuator networks. The Attenuator Zero control requires adjustment only if Q81 or Q72 is replaced. The adjustment assures that when the Memory output voltage is zero, the output voltage at Q72 collector is nearly zero. R73 and C73 comprise a power supply decoupling network. C72 slows the amplifier risetime, preventing self oscillations.

The Attenuator Decoder circuit has two sections; 1) Q104, Q109 and Q111 controlled by the condition at the A4 line and 2) Q126, Q136, D129 and D136 controlled by the conditions at the A1 and A2 lines. The circuits work together to turn on or cut off field effect transistors (FET) in the Feedback Attenuator and the Forward Attenuator circuits according to the Units/Div (deflection factor) programmed. The Units/Div can be controlled from the front panel, or externally programmed depending on the setting of the Vertical Mode switch. Conditions required at the A1, A2 and A4 lines are identical for either internal or external control. A "true" logic state ONE must place A1, A2 or A4 between 0 V and +2 V or at ground. A "false" logic state ZERO must place A1, A2 or A4 between +6 V and +15 V or be an open circuit. The Programmed Amplifier and Attenuator diagrams show truth tables listing the correct circuit voltages for both logic states of the input lines.

The A4 decoder circuit controls Q62 and Q68 in the Feedback Attenuator and Q53 in the AC Amplifier circuit. When the A4 line is grounded the decoder and the attenuator respond as follows:

When A4 = ONE: D101 conducts by current in R101 permitting R102 and R103 to forward bias Q104. Q104 positive collector voltage forward biases Q109, setting Q109 collector voltage at approximately —25 volts. This voltage forward biases D110 and D69. D69 conduction couples the —25 volts to Q68 gate, causing Q68 to cut off. At the same time D110 conduction couples the —25 volts to Q111 base, reverse biasing Q111. With Q111 off, its collector voltage is set at +7 volts (caused by conduction through R111, R51 and D51) reverse biasing D64. Q62 gate is zero biased by R63. Zero bias to Q62 sets its channel resistance to less than 30 Ω, in effect grounding one end of R66. Conduction of D51 in the AC Amplifier reverse biases Q52 and protects Q52 from excessive reverse bias. With Q52 off, R53 turns on Q53. Therefore, with a logical ONE at A4, Q62 and Q53 are on and Q68 is OFF. If A4 condition is a logical ZERO, Q62 and Q53 will be off and Q68 will be on.

The A1, A2 decoder circuit controls six attenuator FET's. Q136 is controlled by the A1 line and Q126 is controlled by the A2 line. Both transistors drive attenuator FET's and the OR gate, D129-D136. Q136 controls both Q94 in the Feedback Attenuator and Q27 in the Forward Attenuator. Q126 controls Q88 in the Feedback Attenuator and Q29 in the Forward Attenuator. The OR gate circuit controls Q91 in the Feedback Attenuator and Q28 in the Forward Attenuator.

When either or both of the Units/Div logic lines A1 and A2 are grounded (for a logical ONE), the decoder and attenuator networks respond as follows:

1. When A1 = ONE: D131 conducts, causing R132 and R133 to forward bias Q136. With Q136 saturated, its collector voltage of +3.4 to +3.5 volts back biases D139. This causes R139 to zero bias both Q94 and Q27.

2. When A2 = ONE: D121 conducts, causing R122 and R123 to forward bias Q126. With Q126 saturated, its collector voltage of +3.4 to +3.5 volts back biases D128, which causes R128 to zero bias both Q88 and Q29.

3. When A1 and A2 both = ONE: the +3.4 volts at the OR gate inputs (D129 and D136 cathodes) reverse biases both gate diodes so their common anode voltage is held at zero by R137. R137 applies zero bias to both Q91 and Q28.

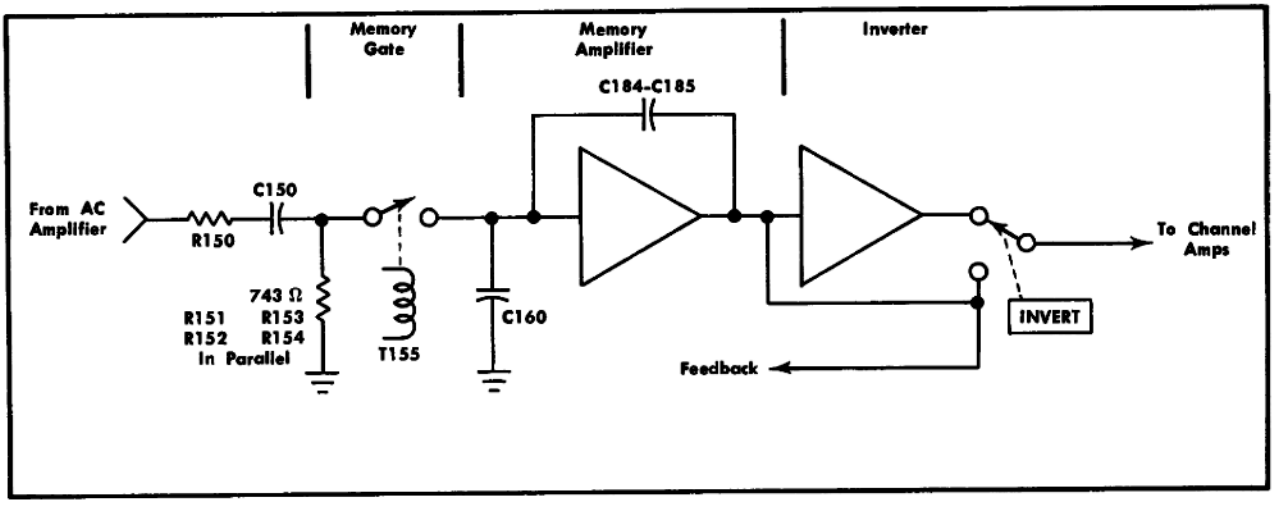


Fig. 4-4. Detailed block of Memory diagram showing basic Memory Gate circuit.

If only A1 or only A2 is grounded, the OR gate holds both Q91 and Q28 in heavy reverse bias (by conduction of D137), and they are both open circuits. Only two positions of the Units/Div switch (or two externally programmed deflection factors) 20 and 2, cause all three feedback attenuator input sections and all three AC Amplifier input sections to be active.

D137 conduction limits the negative voltage to —26 volts and thus protects both Q126-Q136 and the FET's from the —100 volts supply when Q126 and/or Q136 are at cutoff.

Memory Diagram

The Memory diagram of each channel includes the Memory Gate, the Memory Amplifier and the Inverter. The AC Amplifier signal pulse is applied to the Memory circuit during the conduction time of the Memory Gate. The resulting DC signal from the Memory circuit output drives the Feedback Attenuator, the Inverter and the INVERT switch. The Inverter is normally in the circuit to drive the Channel Amplifier circuits through the INVERT switch. The Inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Memory Gate is a pulse-driven diode gate that assures a very high input resistance to the Memory Amplifier except for about 0.15 to 0.2 μs at the time of each sample. During conduction time, the Memory Gate is a low impedance that allows the AC Amplifier to introduce charge to the Memory input through R150, C150 and the gate diodes' conduction resistance.

Fig. 4-4 is a detailed block diagram of the circuits on the Memory diagram. The Memory Gate is represented by a resistor, a coil and a relay switch. The resistor is the parallel value of the four biasing resistors which assure that the four gating diodes are normally not conducting. This equivalent circuit shows that the Memory Amplifier input is zero volts when there is no error signal at sample time.

Looking from the Memory Gate toward its input, the four gating diodes are normally reverse biased by the voltage of Zener diode D151. (Two of the four diodes provide very high reverse biased leakage resistance, although they don't turn off very fast. The other two turn off fast at the end of the gating pulse, although they don't provide high resistance when reverse biased). D151 voltage is balanced to ground by R153 and R154 so D156 cathode rests at +2.5 volts and D158 anode rests at —2.5 volts. C151 assures that the AC Amplifier output signal drives both sides of the Memory Gate diodes.

The gate diodes are forward biased into conduction by T155 at the time of each sample due to the drive pulse from the Memory Gate Driver. T155 is a toroidal transformer specially wound to balance capacitive and inductive coupling to the two secondary windings. The winding with only one end connected provides the capacitive balance. The magnetic toroid core provides the inductive balance. Thus, the drive pulse is converted to identical drive signals to assure that the output junction of the four diodes accurately divides the 5 volts of D151-C151. This places the junction of D157-D159 at ground when no error signal is applied from the AC Amplifier. The functions of the two limiting diodes D153-D154, and the Memory Gate, are discussed in the Memory Amplifier description next. R156, R158 and D155 are shunt damping loads to T155 which minimize self inductance ringing when the memory gate drive pulse ends.

The Memory Amplifier is an integrating operational amplifier with special low leakage (high DC resistance) input circuit. The input and feedback components are capacitors, making the AC input impedance very low. The internal high gain assures a very low output resistance, so that as long as there is no change at the input, the output DC voltage remains stable. The input low leakage circuit has no DC connection to ground except during the time the Memory Gate conducts.

The Memory Amplifier is specially decoupled from the power supplies because the output stage (Q181 and Q182) can require a current pulse as great as 30 mA for a 20 volt output change at sample time. The decoupling networks are: R161-C161, R180-C180 and R183-C183. L197 in the output lead to the INVERT switch, presents a high impedance to the Memory output for high frequency (fast change) sig-

nals. The inductor assures that the output amplifier does not have to provide high current to the output load. L197 slows the output signal response, but at a time when the CRT is blanked.

A dual junction FET (Q162) is the input stage. It is biased for essentially no leakage at the input gate, and the stage has high voltage gain at the in-phase output drain lead. Any voltage change at Q162 gate lead is amplified and applied to the inverting amplifier Q174. Q174 collector circuit applies proper bias to both bases of the output complementary emitter follower pair Q181-Q182, and restores the DC level so a zero input signal (at Q162A) causes a zero output signal. Q174 collector and Q181-Q182 outputs operate linearly through the range of +10 to —10 volts.

Positive feedback is supplied through R178 to Q162B gate to increase the open-loop gain and thereby reduce the input resistance of the Memory Amplifier. The Memory Amplifier has a slower risetime than the Post and AC Amplifiers. C160 and Q162 input gate lead accepts some of the charge from the AC Amplifier, temporarily storing it until the Memory Amplifier can respond.

A cycle of operation at sample time takes the following sequence:

a. The Memory Gate drive pulse arrives at essentially the same time the Sampling Bridge is strobed into conduction. Propagation delay through the three AC coupled amplifiers is quite short. The CRT is blanked at the same time. The fact that the Memory Amplifier input is always at zero volts, and the Memory Gate is balanced around zero volts, prevents any false changes in C184-C185 charge. Therefore, there is no change in the Memory Amplifier output voltage during the time the Memory Gate conducts ahead of the arrival of the AC Amplifier output signal.

b. The AC Amplifier applies a pulse signal through R150-C150 and the Memory Gate to the Memory Amplifier input. C160 accepts some of the charge until the amplifier begins to respond, driving an equal and opposite current back to the input through the feedback capacitors.

c. Since the AC Amplifier output signal is applied to the Memory Amplifier "virtual signal ground" input, C150 receives about 10% of the total error signal charge before the Memory Gate stops conducting. Thus, as the AC Amplifier output returns to its quiescent voltage, the output side of C150 overshoots. The 743 Ω (resistance of R151, R152, R153, R154 in parallel) of the Memory Gate discharges C150 well in advance of the next error signal.

If the Type 3S6 is displaying a single transition step over the full graticule with the display starting at the lower left and ending at the upper right, the error signal is very large during retrace. Such large error signals (even during random process sampling) apply a significant charge to C150. Then the overshoot at the end of the error signal pulse is large enough to cause one side of the Memory Gate to conduct, and remove some of the intended charge in the feedback capacitors. Two normally non-conducting clamp diodes prevent such undesired removal of memory charge. D153 and D154 help to discharge C150 if it receives too large a charge during the Memory Gate conduction time, thus preventing false amplitude displays. These two diodes do not conduct at any other time.

d. As the Memory Gate drive pulse ends, C160 charge is removed by the Memory Amplifier feedback. This causes the Memory output voltage to continue changing toward proper amplitude for a short period after the Memory Gate stops conducting. As soon as C160 charge is returned to normal, the output voltage remains fixed until the next sample.

The actual resting voltage at Q162A gate may not be precisely zero, but it is within a few millivolts of zero. Any deviation from zero can be due to several things: slight differences in conduction of the Memory Gating diodes; slight differences in resistance of the four Memory Gate biasing resistors; some small error signal being generated at each sample time even when the sampling head input signal is zero. Q162B gate voltage is adjusted over a small range to allow the above normal variations. Adjustment of Q162B gate voltage is called the Smoothing Balance adjustment, because it is set so there is no change in Memery Amplifier output when the forward attenuation or gain is changed. The Post Amplifier gain is changed (through the smoothing circuit) by changing the NORMAL/SMOOTH switch from because it is set so there is no change in Memory Amplifier output when the forward attenuation or loop gain is changed. one position to the other or doing the equivalent by external programming. Whatever small zero-input error signal may exist in the system, it always has an average value that will not alter the memory stored charge. Changing the forward attenuation or loop gain changes the peak amplitude of the residual error signal, but not its average voltage zero value. Therefore, Q162B gate voltage is adjusted to equal the average voltage zero value of the residual error signal, and the trace does not move when changing the NORMAL-SMOOTH switch position.

Memory output voltage limits of about +10 and —10 are set by two diodes in parallel with the feedback capacitors. The diodes, D187 and D188 are reverse biased by 9 volts each. If the output tries to go more positive than about +10 volts, D188 conducts (9 + 0.6 = 9.6 volts) reducing the amplifier gain to much less than 1. If the output tries to go more negative than about —10 volts D187 conducts, reducing the amplifier gain to much less than 1. The clamping diodes prevent the amplifier output transistors from saturating at the time of an overdrive signal, and thus assure fast response away from the clamped voltage at the next sample.

The amplifier contains two protective diodes that conduct only when a transistor is removed from its socket. D163 prevents Q162 source leads from having to withstand —100 volts when it is plugged into its socket while the power is on. D173 protects Q174 base-emitter junction in the event Q162 is removed from its socket while the power is on.

Temperature compensation of the amplifier is accomplished effectively by the source-coupled FET input amplifier and D176 and D177. The two identical halves of Q162 compensate each other so their total current does not change with temperature change. D176 and D177 have junction-drop temperature coefficients similar to Q181 and Q182 base-emitter junctions, and thus stabilize the output circuit.

The Memory Amplifier output signal drives the feedback attenuator circuit. The signal is the standard deflection signal mentioned in Section 3, 0.5 volt/CRT division. The memory also drives a X1 gain inverting amplifier (the Inverter) because the rest of the vertical amplifier stages (Channel Amplifier and Output Amplifier) invert the signal to the CRT.

NOTE

The Memory output limit of +10 volts at 0.5 V/div equals 40 CRT divisions of displayed area, required to keep amplitude limiting off screen. The whole pulse amplifier chain is designed for full response and fast recovery so that on-screen displays have accurate deflection factors and DC offset reference.

The Inverter Amplifier is a temperature compensated DC coupled operational amplifier with a gain of 1. R194 and R190 (0.1% tolerance resistors) set the gain. Q190 and Q192 emitter-coupled stage provides both the temperature compensation and high internal gain. Q195 provides the inversion and negative signal offset so the input and output can both be at zero volts at the same time. Q195 collector has the same +10 volt operating range as the Memory output. L195 raises the load resistance during fast changes at sample time to limit the pulse current amplitude required of the —12.2 volt supply at Q195 emitter.

Protective components are D190, which conducts when Q195 is removed from its socket and protects Q190 base emitter junction from excessive reverse bias; D195, which conducts when Q192 is removed from its socket and protects Q195 base-emitter junction from excessive reverse bias; and C195, which stabilizes the amplifier against self-oscillation.

The Inverter drives the Channel Amplifier through the INVERT switch and the VARIABLE and Digital Gain controls.

A and B Channel Amps

The two Channel Amplifiers are ×2 gain inverting operational amplifiers. The input circuit switching by the Vertical Mode Switch disconnects the Units/Div VARIABLE controls, so that they are at maximum resistance at EXT PROG. The switch also connects the A signal into the B Channel Amplifier in the A+B position. The gain is adjusted by the Digital Gain control (with the Units/Div VARIABLE control at maximum resistance, and the Vertical Mode switch not in the A+B position) so that the output to the Digital Unit is the required 1 V/Div. A center-screen zero signal input produces an output of about +10 volts. The output voltage can swing through approximately a 20-volt range, corresponding to ±10 CRT divisions.

The input summing point of both amplifiers is referenced at zero volts at the base of Q413 (Q433). Q413 biasing is set by D414. D414 also provides temperature compensation. The input signal divider network R401 (Units/Div VARIABLE control), R404 (Digital Gain control) and R405 in series with R407 to ground, divide the signal before it feeds through R408 (499 Ω input resistor) to the summing input point at Q413 base.

The Digital Gain control varies the series resistance of the divider network as does the Units/Div VARIABLE control. To use **Auto Cal** disconnect R407 by removing the strap diagrammed directly above R407, and provide a remote resistor that substitutes for R407. Varying the external resistance above and below the value of R407 (from 7.9 kΩ to open circuit) changes the amplifier input current division and the amplifier gain is changed accordingly. A similar arrangement using R427 is provided in Channel B. See the Operating Instructions for additional information on Auto Cal.

Placing the Vertical Mode switch at A+B disconnects the A signal from the A Channel Amplifier input and feeds it to the B Channel Amplifier through the A-B Bal control R430 and R431. Thus the A and B signal currents are combined at the B Channel Amplifier input current summing point, Q433 base. The B Channel Amplifier then provides the algebraic sum of the two signals at its output to the Output Amplifier and the Digital Unit.

Q413 is the inverting amplifier and Q418 is the current gain emitter follower output. When a positive signal overdrives the amplifier, both Q413 and Q418 turn on hard, and both transistors may saturate. When a negative drive signal overdrives the amplifier, Zener diode D417 and D416 limit Q418 emitter voltage to about +20.7 volts, stopping any increase in feedback current. Once the feedback current stops following the input current, the summing input point becomes a higher impedance and starts negative. Q413 is completely cut off. D418 catches its collector at +21.3 volts, and D405 catches its base at less than —1 volt. The amplifier remains in this condition until the negative overdrive ceases.

D405 and D406 limit the input signal drive to the amplifier. C413 slows the amplifier risetime, preventing high frequency oscillations. D416 disconnects Zener diode D417 until the diode is required to clamp a positive excursion at approximately +20 V.

Output Amplifier

The Output Amplifier diagram contains circuits for three blocks of the complete block diagram: The Dual-Trace Multi, the Output Amp and the Position Lamp Driver.

The Dual-Trace Multi selects which Channel Amplifier drives the Output Amplifier. Dual-Trace Multi operation is programmed by the Vertical Mode switch on the front panel. The Dual-Trace Multi is actually a multivibrator when the Vertical Mode switch is placed in the DUAL-TRACE or EXT PROG position. At the other modes of operation, the Dual-Trace Driver signal is diode-disconnected, and only one of the two transistors may conduct. A conducting transistor takes the signal current of the channel not displayed, and a non-conducting transistor permits its associated channel to be displayed. Multi transistor Q450 controls Channel B, and Q455 controls Channel A.

The signals of the Channel Amplifiers are coupled to the digital output connector (P12) by L465 and L460. L465 and L460 prevent oscillation in the A and B Channel Amplifiers by isolating the capacitance load of the digital unit. The Channel Amplifier signals are also coupled into two grounded base amplifiers. These amplifiers share the collector load resistance of R463, R467 and R470 in parallel. Only one of the common base amplifiers (either Q461 or Q466) is connected to the collector load resistance at a time. The Output Amplifier diagram lists DC voltages for displaying Channel A.

Q450 conduction (controlled by the Vertical Mode switch set to CH A) forward-biases D461 so that Q461 collector volt-

age reverse-biases D462. This disconnects the Channel B signal from the Output Amplifier. Q455 non-conduction permits R459 to reverse bias D466. Thus Q466 collector current path is through D467 and the Channel A signal reaches the Output Amplifier input.

Dual-Trace operation forward biases D441 so the —50 V to 0 V Dual-Trace Driver signal can reach the Dual-Trace Multi and switch it at each sample time. Each time a sample is taken, the Dual-Trace Multi changes on the positive portion of the drive pulse. Each time the multi changes states, the Output Amplifier is driven by the other channel. The multi divides the sampling rate by two and delivers a Digital Intensified Zone Enable signal (up = logical ZERO at about +1 volt = CH A; down = logical ONE at about —1 volt = CH B) to the digital unit from Q450 collector.

The Output Amplifier consists of the high gain stage Q477 and Q478, and a ×1 inverting amplifier Q487 and Q488. The high gain stage drives the inverter. Both circuits are DC coupled operational amplifiers with a common negative point at Zener diode D480.

Signals arrive from the common-base stages Q461 and/or Q466 and pass through the front panel GAIN control to the summing input at the base of Q477. The front panel CENTERING control also applies a DC signal to the same summing point, permitting positioning of the trace on the screen.

Signals are amplified by Q477 and given current gain by emitter follower Q478. (All four Output Amplifier transistors have BV_{CBO} ratings of 300 volts). D479 connects Q477 collector to the output if Q478 base falls faster than its emitter for fast full screen positive-going changes. Q478 emitter also drives the ×1 inverter input.

The inverter amplifier is identical to that just described, except that the gain is 1. D489 connects Q487 collector to the output if Q488 base falls faster than its emitter for fast full screen negative-going changes. Both sides of the Output Amplifier drive the Position Lamp Driver stage.

The Position Lamp Driver is a floating current switch that operates the two position-indicating neons on the front panel.

The average voltage at the CRT deflection plates is about +180 volts, which sets the total emitter current of Q495 and Q496 at 0.3 mA. When the two deflection plate voltages are equal, the two transistors share the 0.3 mA and both neons are lighted. If either deflection plate goes more positive than the other, the transistor on that side takes all the 0.3 mA and the other transistor cuts off. Each transistor has a BV_{CBO} rating of 85 volts, so R497 prevents the turned off-transistor collector from going all the way to +300 volts. The dark neon has some voltage across it, but not enough to cause it to glow. D492 and D493 assure that the two transistor base voltages are never more than 0.6 volt apart.

Gate Generators

The Gate Generators diagram contains circuits for the Blocking Oscillator, Dual-Trace Driver, both Delay and Strobe Drivers and both Memory Gate Drivers. The Blocking oscillator starts the sampling process when driven by the sampling sweep unit.

The Blocking Oscillator output drives the two Delay and Strobe Driver circuits, and the Dual-Trace Driver circuit. The Dual-Trace Driver circuit drives the Dual-Trace Multivibrator and CRT cathode circuit for interdot blanking of the display.

The Blocking Oscillator can be thought of as a risetime improving circuit. When driven by the sampling sweep unit drive pulse, Q503 always delivers a signal of the same amplitude and same risetime at its output. The stage is a simple amplifier until T503 builds up enough positive feedback for regeneration. After regeneration, the circuit ignores the drive pulse shape, amplitude and energy content. Q503 is normally biased to cutoff, causing the output signal to go from +15 volts to ground each time it is driven. D502 disconnects T503 backswing pulse from Q503 base and also makes certain T503 does not load the drive pulse.

The Dual-Trace Driver is a monostable multivibrator Neither transistor conducts until driven. —12 volts is applied through L516 to R515 and R518, placing Q515 at zero bias. Q522 is reverse biased by the junction drop of D520 and current in R520. Normally, neither transistor is conducting.

A negative drive pulse from the Blocking oscillator is coupled through R505, C505 and C513 to Q522 base. (D506 is reverse-biased 15 volts while Q515 is off, so it doesn't stop the drive pulse from reaching Q522.) Q522 turns on hard and D519-C519 couples the drive to Q515 base. Q515 turns on and applies more drive to Q522. D506 turns on and keeps Q515 from saturating. Thus a heavy regeneration causes a 50 volt output pulse to drive both the Dual-Trace Multi and the CRT blanking circuit. C513 charges very rapidly, but C511 does not. C511 holds base drive current applied to Q522 for a longer period. When C511 is charged, Q522 cuts off and its falling collector signal is AC coupled by C519 alone to Q515 base, turning it off. The turn-off is also regenerative, with D520 limiting the reverse bias on Q522 and helping to recharge C513 for the next cycle.

The Delay and Strobe Driver and the Memory Gate Driver circuits are unusual multivibrators. The A and B Channel circuits are identical except for R530, a power supply isolation resistor located between +15 volts and the B DELAY control. The Channel B circuit is explained below.

The complete circuit, from Blocking Oscillator output to the two pulse outputs, consists of: A two-diode comporator that compares a negative-going ramp with a fixed DC voltage variable by the Delay control; a very low-current amplifier that follows the Delay control voltage without affecting its output to the next stage; and a monostable multivibrator with two output terminals.

Quiescent circuit conditions are: Q538 base voltage rests between +15 and +11 volts, as set by the B DELAY control. Q538 current is limited to about 1 mA by R537 which leaves the collector clamped by D539 at —12.8 volts, assuring that there is no change in output voltage when the Delay control position is changed. Q541 is reverse biased 0.6 volt by D539, and Q555 is reverse biased 0.6 volt by current in D555, D552, R551 and the Memory Gate Width control. Q555 collector voltage is at —12.2 volts through T355.

As the Blocking Oscillator fires, R536-C536 form a negative-going ramp signal that soon causes D536 to conduct. When D536 conducts, the ramp turns on Q538. C537 contains enough charge for Q538 collector to clear D539 of carriers, and to forward bias Q541. As Q541 conducts, the negative signal is coupled through C541 and C543 back to Q538 base in a regenerative turn-on. The feedback signal also reverse

biases D534 and D536 so as not to disturb the other channel Delay circuit.

The —27 volt signal from Q541 collector drives Q555 through C547 and C548. C548 couples a fast turn-on pulse to Q555 while C547 signal current reverse biases D552, allowing R553 to keep Q555 turned on. Q555 collector signal is coupled through R549 back to Q541 base and holds Q541 in steady conduction. R557 applies a steady 40 mA current to the Memory Gate transformer primary (T355) for the pulse duration of about 180 ns.

C543 regenerative turn-on to Q538 does not last as long as Q555 turn-on to Q541, but since Q541 is saturated, Q538 is not disturbed. The duration of Q555 conduction is therefore controlled only by the position of the Memory Gate Width control which adjusts C547 charge rate. The smaller the resistance, the shorter the gate duration. As C547 charges toward +15 volts, D552 again conducts and turns Q555 off, stopping the Memory Gate pulse and the drive to Q541 base. However, Q541 was in saturation, so it does not stop conducting immediately. Q541 collector signal rises positive about 350 ns after it is driven negative. This RC rise is slow and does not couple much energy through either C541 or C543. Q541 total negative step is coupled by C541 as a Strobe Drive pulse to the sampling head.

The sampling drive pulse from the sampling sweep unit is slewed in time from the initial trigger event to each sample. An additional time positioning is accomplished in the two Delay (ramp comparator) circuits. The additional time slewing of the strobe drive pulses require an identical time slewing of the Memory Gate drive pulses in order to maintain proper processing of the error signals into the Memory Amplifier. This is accomplished since the Memory Gate Driver is driven by the Delay and Strobe Driver.

Programmed Offset

The Programmed Offset diagrams for each channel include the Offset Current Selector, Offset Amplifier, Offset Inverter, Electronic Switch and Polarity Decoder circuits. The offset circuits provide a DC voltage which is combined with the signal feedback voltage in the sampling head and applied to the sampling bridge. The circuit operates in two modes; external, with the Vertical Mode switch in the EXT PROG position; and internal, with the Vertical Mode switch in any position other than the EXT PROG position.

In the external mode, the DC Offset voltage is externally programmed by external voltages or connections made to the proper pins at the rear program connector. The program operates the Offset Current Selector block and the Polarity Decoder block. The Offset Current Selector circuit provides a programmed current to the Offset Amplifier. This current causes the Offset Amplifier to produce an output voltage from 0 to +9.95 volts in 0.05 volt increments. The voltage is fed to the Offset Inverter (a ×1 inverting amplifier) and the Electronic Switch circuits. The Electronic Switch circuit, operated by the Polarity Decoder circuit, selects the positive (or the inverted negative) offset voltage which is coupled through J13 (rear panel) to the sampling head.

In the internal mode, the Offset Amplifier block provides an analog voltage output with a range of —10 to +10 volts as set by the DC OFFSET control. The Polarity Decoder circuit operates the Electronic Switch circuit (Q677 conducting) to couple the output voltage to the sampling head. The Offset Inverter circuit is not used in the internal mode. Also the Offset Current Selector is not programmable in this mode, but does supply input current to the Offset Amplifier.

When the DC OFFSET is front-panel controlled, the Vertical Mode switch connects emitter return resistors of Q602, Q610, Q616, Q620 and Q622 to ground. This reverse biases these transistors, since their bases are connected to decoupled +3.6 volts. With these transistors off, a current path is provided from the —50 V supply through each collector resistor and coupling diode to Q633A base. This supplies a total of 2 mA to the Offset Amplifier summing point at Q633A base.

The Offset Current Selector circuit supplies a programmed current in the external mode to the Offset Amplifier. Each of the nine current selector transistor circuits supplies a different amount of current. The output currents are added through diodes to the Offset Amplifier summing input at Q633A base. In the external mode, each transistor can be turned on or off by the external program.

The mV of Offset voltage controlled by each input line is labeled at the left of diagram 8. For further programming information see the Operating Instructions, Section 2.

In external program, the Offset Current Selector circuit operates as follows (since both Channels are the same, only Channel A is described):

1. +15 volts is connected by the Vertical Mode switch to the emitter return resistors of Q602, Q610, Q616, Q620 and Q622. +3.6 volts is connected to the bases of Q604, Q608, Q614 and Q626 through decoupling resistor R628. Each transistor collector is connected to the Offset Amplifier summing input through a diode. Each transistor circuit can provide current for the Offset Amplifier circuit, but only when externally programmed to do so.

2. (Using the Q626 circuit as an example). With a logical ONE at connector A of the logic card, D625 is forward biased by current in R625. This sets Q626 emitter at about +0.6 volt, cutting off Q626 (because its base voltage is at +3.6 volts). With Q626 off, R626 current forward biases D626. This applies the current into the Offset Amplifier summing input at Q633A base.

3. When connector A of the logic card is left on open circuit (logical ZERO), D625 cannot conduct R625 current. Instead, Q626 is forward biased and its collector takes all of the R626 current away from D626 and the Offset Amplifier input.

4. The other transistors in the Offset Current Selector circuit operate as just described for Q626, except that the output current path is from the —50 volt supply, and the current values are different due to different resistance values for the collector resistors. It is the sum of all currents out of the Offset Current Selector circuits that sets the final programmed DC OFFSET voltage. The accuracy of the current for the Offset Amplifier is affected by the collector resistors and the —50-volt supply voltage.

Offset Amplifier. The Offset Amplifier is a DC coupled inverting (operational) amplifier consisting of Q633, Q642 and Q645. Both the input and feedback components differ in internal operation as compared to external programming

of the DC OFFSET voltage. The input summing terminal is at the base of dual transistor Q633A. The output terminal is at the emitter of emitter follower Q645. Internal gain is very high due to large collector load resistors for both Q633B and Q642. The high gain assures that the variable current input is converted to a variable voltage output with very low output resistance.

Internal operation connects R648 and the Offset Zero control as one of the input elements to the amplifier, and the DC OFFSET control (R647) is a variable resistance feedback element.

Externally programmed control of the Offset output voltage connects various resistors of the Offset Current Selector circuits as the input elements, and R646 as the fixed resistance feedback element.

Output voltage swing is from —10 to +10 volts when internally controlled, and from 0 V to +9.95 V when externally programmed. The two different voltage ranges require that the high gain input comparator amplifier, Q633, operate at different reference voltages for the two modes of operation. The reference voltage is applied to the base of Q633B, and is —10 V for internal operation, and ground for externally programmed operation. The large emitter return voltage, —100 V, prevents the stage static current from changing very much between the two conditions.

Internal operation produces an output voltage as a function of Ohm's law. The voltage varies based upon the fixed 2 mA input and feedback current and the resistance value of the variable DC OFFSET control R647. Assume R647 is zero ohms (fully clockwise at Black scale = —10 V Offset). Whatever the current value through R647, zero ohms causes zero volts difference between the amplifier summing input and the output at Q645 emitter. Since Q633B base is at —10 V, the output is also at —10 V. Turning the DC OFFSET control so it introduces resistance in the feedback path causes the output voltage to change in a positive direction. By the time the control is fully counterclockwise, the feedback current and the resistance cause the output at Q645 emitter to be at +10 V.

Externally programmed operation uses a fixed feedback resistor and different amounts of input current as selected by the Offset Current Selector circuits and the external program. R646 is the fixed feedback resistor, and even through the front panel DC OFFSET control is not completely disconnected, its current load on the output does not alter the output voltage as controlled by the feedback amplifier. The reference voltage for external control at Q633B base is ground. With all the input resistors connected to a negative voltage, it is not possible to program an output voltage that passes through zero and changes polarity. Thus, the Offset Inverter ×1 gain amplifier is used when a negative Offset output voltage is required. Protection diodes are D634, D641, D643 and D645.

C647 connected across the DC OFFSET control minimized the effect of wiper contact noise on the output voltage when the control setting is changed. C634 prevents AC pickup in the Vertical Mode switch lead by providing low impedance to any AC signals at Q633B base.

The Offset Inverter Amplifier is a temperature-compensated DC coupled amplifier with a gain of 1. Feedback resistor R660 and input resistor R650, both 0.1% tolerance resistors, set the gain. Q653 dual-transistor is an emitter-coupled stage providing both temperature compensation and high internal gain. Q658 operates as an inverting amplifier feeding Q660 emitter follower output circuit.

Any input voltage other than zero causes a current in the input resistor R650. Any change in Q653A base voltage changes Q653B collector voltage to Q658 base in the same direction. Q658 amplifies and inverts the signal, applying it to Q660 emitter follower. Q660 voltage output produces an equal and opposite current to Q653A base, making the output voltage equal and opposite to the amplifier input voltage.

Two diodes provide protection when transistors are removed from their sockets. D658 conducts when Q658 is removed. D657 conducts when Q653 is removed. R657 and C657 comprise a decoupling network in Q658 emitter circuit.

The Electronic Switch circuit operates during external programming as a single pole double throw switch consisting of field effect transistors Q663 and Q677. One transistor is on while the other is off as set by the Polarity Decoder circuit. The transistor drain leads are connected together (TP663) to provide whichever polarity output voltage is desired by the external program. When Q677 is on, it connects the Offset Amplifier output voltage (0 to +10 V) to the output circuits. When Q633 is on, it connects the Inverter Amplifier output voltage (0 to —10 V) to the output circuits. Conduction of either transistor is set by the Polarity Decoder circuit. R678 connected at TP663 is not used, but is in the circuit to make the Offset card usable in a Type 3S5.

The Polarity Decoder circuit operates the two transistors Q663 and Q677 in the Electronic Switch circuit, turning one transistor on while holding the other off.

The circuit holds Q677 on (exclusively) during internal operation. Q670, Q673 and Q675 are the decoder transistors. An external program that places a logical ONE at the front panel connector J15 pin 4 will cause the Decoder circuit to turn Q663 off and Q677 on. See the Operating Instructions for programming this circuit through the rear panel connector.

An external program of a logical ONE to the Decoder input causes D667 to conduct R667 current. Then R668 and R669 forward bias Q70 into saturation. R670 turns Q673 on to saturation, placing Q663 gate lead at about —25 V and assuring that it remains cut off. Q673 collector voltage also reverse biases Q675, causing R675 to reverse bias D676 and set Q677 gate lead at zero bias, turning Q677 on. D675 in Q675 emitter circuit provides an equal junction drop to that of D674, assuring that Q675 can be placed at cutoff when the external program is a logical ONE.

An external program of a logical ZERO to the Decoder input reverses the conditions, causing Q663 to conduct and Q677 to be at cut off. At that time, D674 reverse biases, and prevents Q673 high collector voltage from overdriving Q675 base circuit.

Power Supplies

The Power Supply diagram contains the internal power supplies power connections from the indicator oscilloscope and power connections to J13 (rear connector) for the sampling heads. Power from the indicator oscilloscope enters through P11 at the left edge of the diagram. P11 and J13 also show pin connections to other circuits within the Type 3S6.

Internal power supplies obtain power from the indicator oscilloscope at 6.3 VAC and from the —12.2-volt, +125-volt, and —100-volt supplies. The 6.3 VAC is fed to T950 primary. T950 secondary windings feed the +15 and +3.6 volt supplies.

The +15-volt Supply is fed from T950 secondary winding at terminals 5, 6 and 7. The secondary voltage of approximately 52 VAC is rectified by D951-D953, filtered by C950, and regulated by D955, Q957, Q959, Q966 and Q969. The regulator circuit is of the series type, with Q969 the series pass (variable resistance) transistor. Q957 and Q959 form a temperature compensated comparator circuit, and Q966 inverts and amplifies the comparator output which controls Q969. The output voltage is compared with the reference Zener diode D955. Assume a positive change in the output voltage. The correcting action that follows causes Q969 series resistance to increase, restoring the output voltage to its correct value. The positive change at the output is directly coupled to Q957 base, and attenuator-coupled to Q959 base. Q959 emitter is driven by Q957 emitter and follows the change all the way. Q959 base does not follow the change 100%, and therefore the transistor receives a forward bias signal. Q959 increases its current, and applies a positive signal to Q966 base, causing Q966 to reduce its collector current. Current reduction in Q966 causes Q969 base and emitter to go more negative. Or more properly stated, Q969 increases the voltage across it, restoring the output to its proper value.

If the +15 volt supply is accidentally shorted to ground, excessive current through R951 and R953 will cause these resistors to overheat and open up, protecting Q969 and rectifiers, and the transformer.

The —50-Volt Supply consists of the comparator, Q901-Q907 and shunt regulator Q903. (The —50 volt supply is one of two voltage references for the +50 V supply.)

The circuit changes the resistance of Q903 to take more current when the load current reduces, and to take less current when the load current increases. D905 protects Q903 from damage in the event the output is shorted to a voltage more positive than —12.2 volts.

Comparator transistors Q901-Q907 compare a voltage near ground at the junction of R908-R909 with zero volts at ground. If the output load current increases (output voltage goes positive), Q907 base and emitter follow the change. Q907 emitter drives Q901 emitter positively, which is an increase in forward bias and turns Q901 on harder. Q901 collector voltage change decreases Q903 turn-on bias increasing Q903 resistance and permitting a negative return in voltage at the supply output.

The +50-volt Supply uses one transistor as an emitter follower and the other transistor as both a comparator and as the shunt regulating element. R917-R918 presents a voltage near +15 volts to the base of emitter follower Q911. Q911 provides current gain to the signal and applies it to the base of comparator-regulator transistor Q915.

If the output load current increases (voltage goes negative), Q911 emitter takes Q915 base negative, reducing Q915 current. As Q915 current reduces, the output voltage rises back to its proper value.

A short circuit that places the +50-volt line less positive than +15 volts will reverse-bias D915 and protect Q915 from damage. The large resistance value of R917 and R918 protects Q911 from damage. A short circuit on the +50-volt line will cause the +50-volt output to be a few volts low. Again, no transistors will be damaged.

The +3.6-volt Supply is fed from T950 secondary connections 3 and 4. The secondary voltage of approximately 6.7 VAC is rectified by the bridge rectifier D930A-B-C-D, filtered by C931 and fed to the output through Q938. Q936 emitter follower controls Q938. R933 and R934 set Q936 base at +3.6 volts. Through equal and opposite base-emitter junction drops of Q936 and Q938, the output voltage is +3.6 volts. The circuit transforms the input impedance at Q936 base to less than one ohm at Q938 emitter, so load changes do not significantly affect the output voltage.

The —25-Volt Supply is fed from the —100-volt Supply from the indicator oscilloscope through R946 and Q944 emitter follower. R941 and R942 set Q944 base at about —25.6 V, which provides a low impedance —25 volts output at Q944 emitter. R946 limits the current from the —100-volt supply and limits power dissipation in Q944.

Card Connectors and Decoupling Networks

The Card Connectors and Decoupling Networks diagram contains the Offset and Logic Card connectors, and the power supply decoupling networks on the Output and Vertical boards.

The Offset card connector J600 and the Logic Card connector J800 show the signal contained at each pin, and the number of the schematic where it can be found.

Decoupling networks are drawn within outlined areas that represent particular diagrams already described.

Vertical Mode Switch and Program Connectors

The Vertical Mode Switch and Program Connectors diagram contains information on the Vertical Mode Switch, the rear external program connectors and the digital readout connector.

All of the Vertical Mode Switch connections are shown with references to the other schematic diagrams where sections of the switch are shown. Each section or wafer of the switches is coded to indicate its position in the switch assembly. The numbered portion of the code refers to the wafer number counting from the front (the mounting end of the switch) toward the rear. The letters F and R indicate whether the front or rear of the wafer performs the particular switching function.

When the Vertical Mode switch is in the EXT PROG position, the front panel EXTERNAL PROGRAM light, B999 is lighted. B999 is then connected to —12.2-Volt supply and ground through R999.

NOTES

SECTION 5
DIGITAL UNIT CONTROL DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

General Definition

This section of the manual describes the circuits and logic of the Type 3S6 Digital Unit Control diagram. A logic diagram titled Digital Unit Control Logic is included at the back of the manual following the Digital Unit Control diagram.

The Digital Unit Control circuits operate exclusively to program the readout logic circuits of a Tektronix Type 230 Digital Unit. The Type 3S6 controls the digital unit only when it is programmed by the digital unit. The type of units (either volts or amperes) programmed into the digital unit is controlled by the type of sampling head operated with the Type 3S6.

Description of the Digital Unit Control circuits is separate from the description of other Type 3S6 circuits. This is because the Digital Unit Control circuits do not contribute to the Type 3S6 operation. Only the Type 230 Digital Unit uses the Digital Unit Control outputs. All outputs pass out the rear of the Type 3S6, through P12, through the Type 568 ocilloscope, and into the associated digital unit.

Three types of signal sources control the circuit functions: (1) the deflection factor selected by either the front panel Units/Div switch or an external program, (2) the sampling head units (Volts or Amps) and its units decade (multiplier: X0.1, X1 or X10) and (3) the digital unit amplitude measurement program. If the digital unit is programmed to make a time measurement, all of the Digital Unit Control outputs are inhibited. If the digital unit is programmed to make an amplitude measurement, the Digital Unit Control circuits function as instructed by the other two sources.

NOTE

Both the Digital Unit Control circuit diagram and its Digital Unit Control diagram include logic symbols. Logic symbols used are based on the ASA Y32.14-1962 Standards, and are drawn using negative logic symbols only.

Three types of outputs control the digital unit: (1) the type of units, Volts or Amps, (2) the readout number decimal point, including an "M" for mV or mA and (3) the digital unit counter circuit divide command (see the digital unit instruction manual for use of the counter divide outputs).

All input and output lines are considered to be a logical ONE when grounded, and a logical ZERO when left open circuit. (Grounding is accomplished in both cases by saturating transistors in the digital unit, saturating transistors at the Digital Unit Control output leads, and by solid ground connections by the Units/Div switches.)

Block Diagram

The main Block diagram includes the Digital Unit Control blocks at the lower left corner. Each block name agrees with areas outlined on both the Digital Unit Control diagram and the Digital Unit Control Logic diagram. The general layout of all blocks on all three diagrams is the same, with input lines at the left and output lines at the right.

Comparing the block diagram to the Digital Unit Control Logic diagram during the following block description may prove useful in understanding the Digital Unit Control circuits.

The eight blocks of the Digital Unit Control circuits show that the input lines from both CH A and CH B are always connected, but that only one set of output lines drives the digital unit circuits. Two pairs of channel selection lines from the digital unit tell the Digital Unit Control circuits which channel is being used. One pair carries the channel selection instructions for the decimal and units output, and the other pair carries the channel selection instructions for the digital unit counter divide output. When the digital unit is programmed to make an amplitude measurement, one of each pair of channel select lines is grounded. If the measurement is being made on Channel A, the three input sources from Channel B are inhibited by the digital unit grounding the "A D, U, GND" and "A ÷ GND" lines. When the digital unit is programmed to make a time measurement, none of the channel select lines is grounded, and all outputs are inhibited.

NOTE

This description does not indicate the point from which digital unit programming originates. The circuits in the Type 3S6 operate the same whether the digital unit is externally programmed or controlled from its own front panel. However, externally programming the Type 3S6 does make the plug-in's circuits operate in a slightly different manner than controlling it from the Type 3S6 front panel. Front panel control of the Type 3S6 permits the VARIABLE control CAL switches to inhibit the decimal and units section of the Digital Unit Control circuits; externally programming the Type 3S6 causes both the VARIABLE control and its CAL switch to be removed from operation, so that turning the control will neither affect the CRT deflection factor, nor inhibit the decimal and units outputs.

Input lines from the Units/Div switches are labeled A1, A2 and A4, and B1, B2 and B4. The Units/Div lines are grounded according to Truth Table 5-1. The 1's digit and the 2's digit lines go to both the 200 UNITS/DIV DECODER block and the COUNTER DIVIDE CONTROL block. The 4's digit lines go to only the 10, 5, 2 UNITS/DIV DECODER block. Output from the 200 UNITS/DIV DECODER block is a logical ONE only when 200 Units/Div is programmed. Output from the 10, 5, 2 UNITS/DIV DECODER block is a logical ONE only when the 10, 5 and 2 Units/Div deflection factor is programmed. Outputs from the COUNTER DIVIDE

CONTROL block are logical ONE according to Table 5-1; only one output line is a logical ONE at any particular time and the other two lines are then a logical ZERO.

TABLE 5-1

Units/Div Truth Table

Units/ Div	A4 B4	A2 B2	A1 B1	÷[1]
200	0	0	0	5
100	0	0	1	1
50	0	1	0	2
20	0	1	1	5
10	1	0	1	1
5	1	1	0	2
2	1	1	1	5

[1] ÷ = **Output line at Logical 1.**

NOTE

Logical 1 means the line is grounded, Logical 0 means an open circuit; not grounded.

Two other input line pairs (to the Digital Unit Control circuits) come from the sampling heads. One pair, to the UNITS CONTROL block gives instructions to the digital unit to indicate that the readout units are either Volts or Amperes. The other pair, to the UNITS/DIV MULTIPLIER DECODE block gives instructions regarding the sampling head deflection factor in relation to the Type 3S6 Units/Div control. The sampling head may require that the numbers around the Units/Div switch be multiplied by X0.1, X1 or X10, indicating the need for a decimal shift in the digital unit readout. The Units/Div multiplier instructions are ternary (three levels) rather than binary (two levels) as are all the other instructions given.

Both the UNITS CONTROL and the UNITS/DIV MULITPLIER DECODER blocks receive information from both Channel A and Channel B. These blocks use the Channel Select lines from the digital unit to inhibit information from the channel not in use.

Included in the UNITS/DIV MULTIPLIER DECODER block is a Ternary to Binary decoder that converts one-line ternary information to three-line binary information at the lines labeled X0.1, X1 and X10.

Outputs from all four of the Units/Div Decoder blocks feed the DECIMAL CONTROL block. The DECIMAL CONTROL block decodes both the Units/Div number programmed and the sampling head Units/Div multiplier to operate the digital unit decimal neons and the "milli" readout lamp. The M lamp control line is part of the Decimal Control block because lighting the M (for "milli") affects the location of the readout decimal.

Logic Voltages

Negative logic is used throughout this manual to describe the operation of the Type 3S6 circuits. By the standards of negative logic, a TRUE state, or logical ONE (1) exists at a lead which is at or very near ground. A FALSE state or logical ZERO (0) is present at a lead which is either open-circuit or more positive with respect to ground. External control line voltage limits are stated in Section 1, Specification, to be logical ONE (TRUE) 0 V to +2 V; logical ZERO (FALSE) +6 V to +15 V, or open circuit. Externally controlled logic lines can be operated either by saturating transistors that do not completely ground the line, or by using cut off transistors that exhibit some I_{CBO} leakage and do not really leave the line open.

Voltage levels of logic states produced within the Type 3S6 are different than the voltage levels of logical ONES or ZEROS in externally controlled logic. This results because the principal voltage supply for integrated circuits in the Type 3S6 is 3.6 volts rather than 15 volts.

Output voltage limits for a logical ONE or ZERO may also vary because those limits are set by the digital unit in use. However, it can be noted that a logical ONE is always accomplished by a saturated transistor.

Internal logic voltages that relate to the integrated circuits are stated at the bottom of Fig. 5-1. Other voltage values, such as the ternary voltages out of the Units/Div Multiplier Decoder are given later on in this section.

Logic states throughout the Digital Unit Control Logic diagram (without giving the voltage values) are included in the four truth Tables 5-2, 5-3, 5-4 and 5-5. The first three truth tables give the output logic states of all significant gates for three conditions of a sampling head Units/Div multiplier, X0.1, X1 and X10. The truth tables are of primary value when searching for a failure.

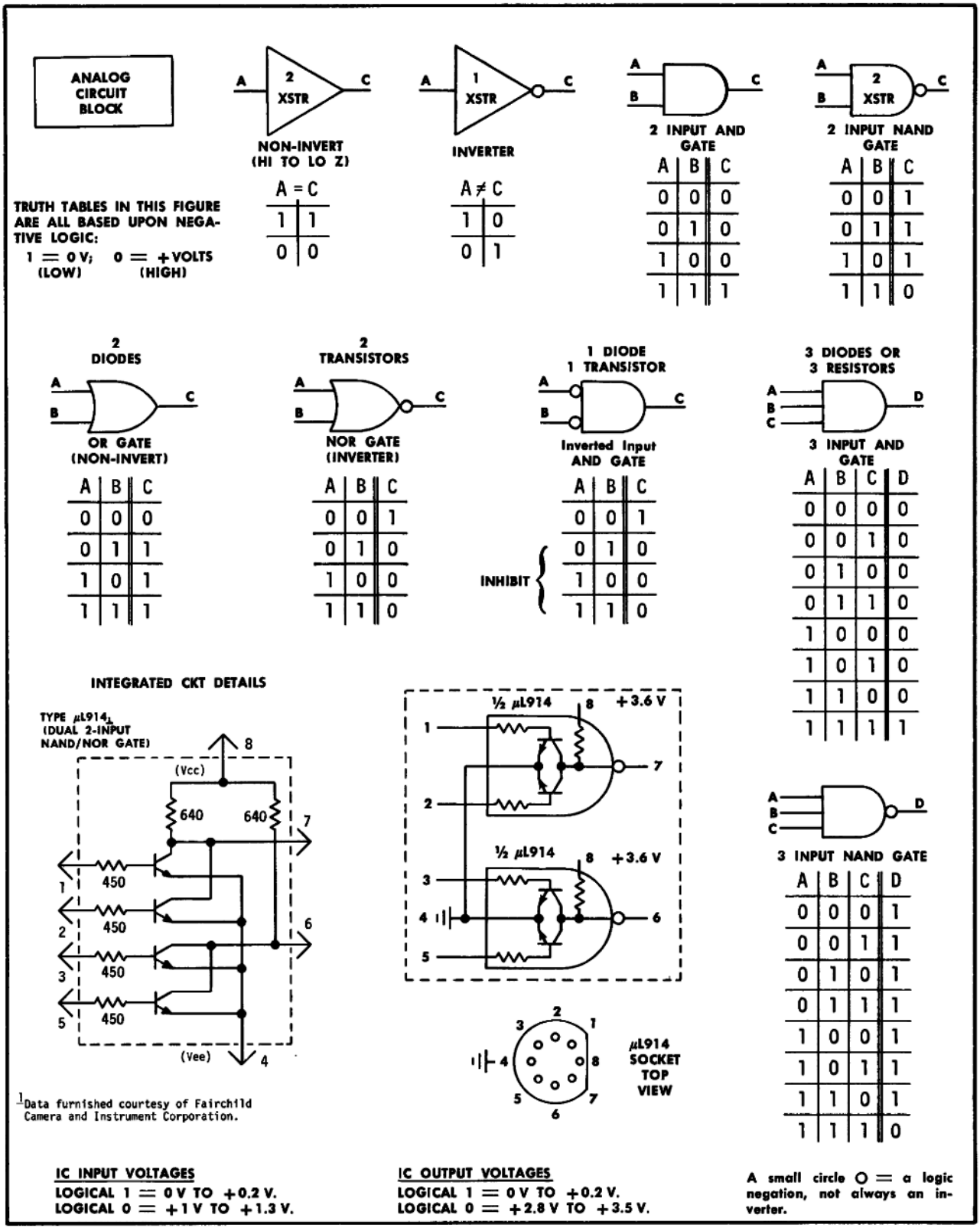
Control settings for using the first three truth tables are: the digital unit operating to make a Channel A amplitude measurement; the sampling head multiplier as stated at the top of the Table; the Units/Div as stated at the left of the Table; and if not externally programming the Type 3S6, the Units/Div VARIABLE control at CAL. The tables also apply to Channel B if all controls are properly set for an amplitude measurement on Channel B.

Table 5-5 applies to the circuits of the Counter Divide Control block, and is altered only by the Units/Div switch(es). If not externally programming the Type 3S6, the Units/Div VARIABLE control must be at CAL.

Digital Unit Control Logic Diagram

Fig. 5-1 is a key to the logic symbols used in the Digital Unit Control Logic Diagram. If you are not experienced with logic symbols, it is recommended that this area on the Logic Diagram be read after reading the circuit description later in this section.

Symbols in the lower portions of Tables 5-2, 5-3, 5-4 and 5-5 differ slightly from the symbols on the Logic Diagram. Specifically, the column headed "M Q806" has a 3 input NAND gate symbol with a logic negation at one input. This symbol is equivalent to a group of symbols on the Logic Diagram; U805B inverter; R804, R805 and R806 3 input AND gate; and the (non-inhibited) 2 input NOR gate Q806, D806. The logical ONE in this column indicates that Q806 is saturated and the digital unit M lamp will be lighted. A second symbol difference includes the logic symbols leading to and including the DEC 3 column. Q839 is shown in a manner that ignores D839. This is justified by the fact htat there will be an output only when the last gate is not inhibited. The truth tables, and the symbols used, do not apply when the digital unit inhibits the outputs.



[1]Data furnished courtesy of Fairchild Camera and Instrument Corporation.

Fig. 5-1. Digital Unit Control Logic diagram symbols and truth tables.

TABLE 5-2

Decimal & M Output Logic States When Units/Div Multiplier = X0.1

Units/ Div	Input Logic A4 B4	A2 B2	A1 B1	Q814 Coll	Q826 Coll	Q816 Q828	Ternary Decoder X10	X1	X0.1	U805A	U834A	U834B	U835A	U835B	U833A	U833B	U838B	M Q806	DEC4 Q836	DEC5 Q843	D833 D834 D835	D840 D841 D842	U838A	DEC3 Q839
200	0	0	0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	0	1	0
100	0	0	1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	0
50	0	1	0	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	0
20	0	1	1	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1	0	0	1	1	0
10	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	1
5	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	1	1	0	1
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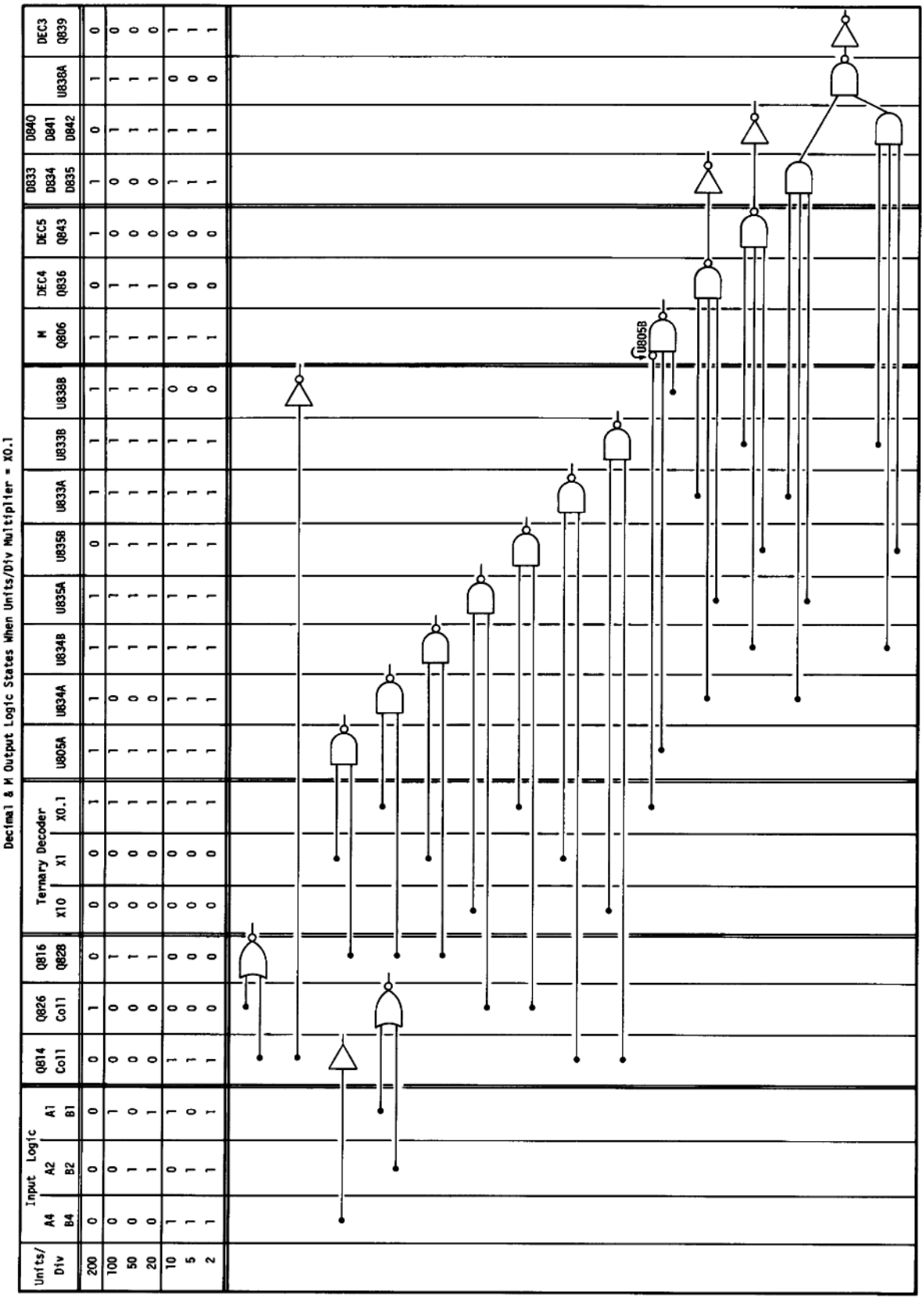


TABLE 5-3

Decimal & M Output Logic States When Units/Div Multiplier = X1

Units/ Div	Input Logic A4 B4	A2 B2	A1 B1	Q814 Coll	Q826 Coll	Q816 Q828	Ternary Decoder X10	X1	X0.1	U805A	U834A	U834B	U835A	U835B	U833A	U833B	U838B	M Q806	DEC4 Q836	DEC5 Q843	D833 D834 D835	D840 D841 D842	U838A	DEC3 Q839
200	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
100	0	0	1	0	0	1	0	1	0	0	1	0	1	1	1	1	1	1	0	1	1	0	1	0
50	0	1	0	0	0	1	0	1	0	0	1	0	1	1	1	1	1	1	0	1	1	0	1	0
20	0	1	1	0	0	1	0	1	0	0	1	0	1	1	1	1	1	1	0	1	1	0	1	0
10	1	0	1	1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0
5	1	1	0	1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0
2	1	1	1	1	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1	0	0	1	1	0

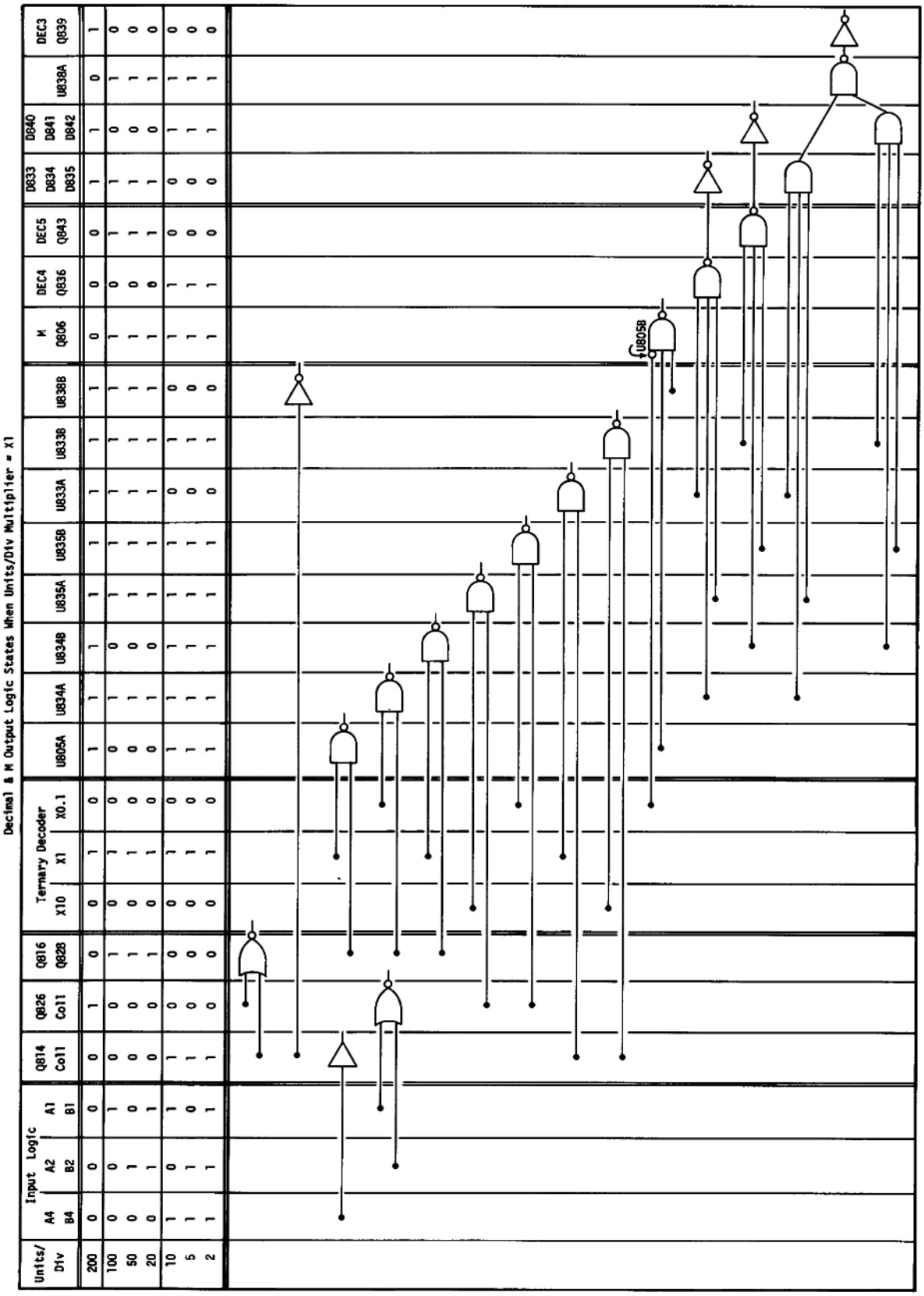
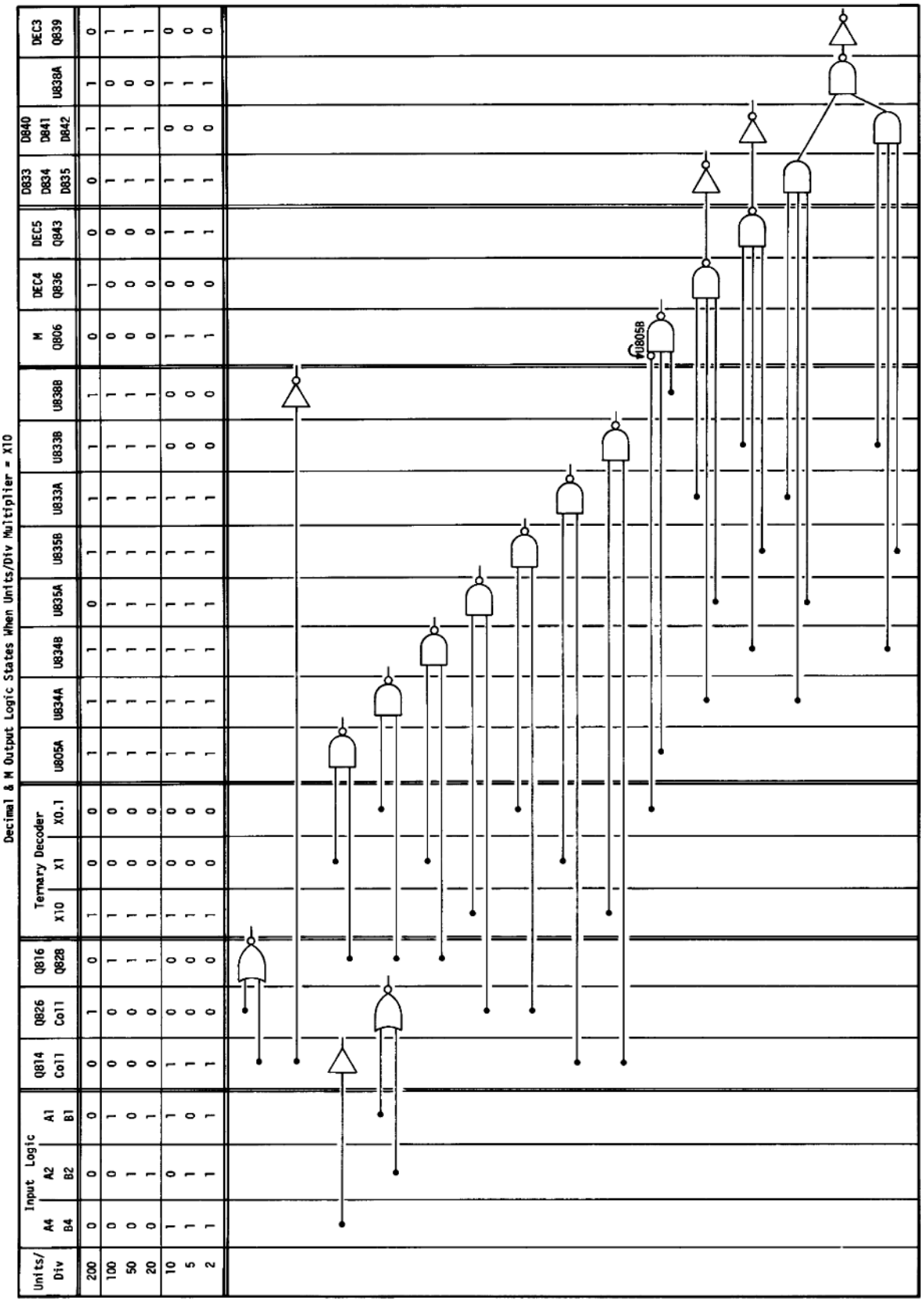


TABLE 5-4

Decimal & M Output Logic States When Units/Div Multiplier = X10

Units/ Div	Input Logic A4 B4	A2 B2	A1 B1	Q814 Coil	Q826 Coil	Q816 Q828	Ternary Decoder X10	X1	X0.1	U805A	U834A	U834B	U835A	U835B	U833A	U833B	U838B	M Q806	DEC4 Q836	DEC5 Q843	D833 D834 D835	D840 D841 D842	U838A	DEC3 Q839
200	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	1	1	0	1	0	0	1	1	0
100	0	0	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
50	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
20	0	1	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
10	1	0	1	1	0	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	0
5	1	1	0	1	0	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	0
2	1	1	1	1	0	0	1	0	0	1	1	1	1	1	1	0	0	1	0	1	1	0	1	0



All symbols used in this manual are negative logic symbols, regardless of the "active" state of the input or output lines. This applies even to the logic symbols on the circuit diagram. Thus, the function of any gate can be defined independently of the circuit's intended function, and all symbols on the circuit diagram or Logic diagram have truth tables found in Fig. 5-1.

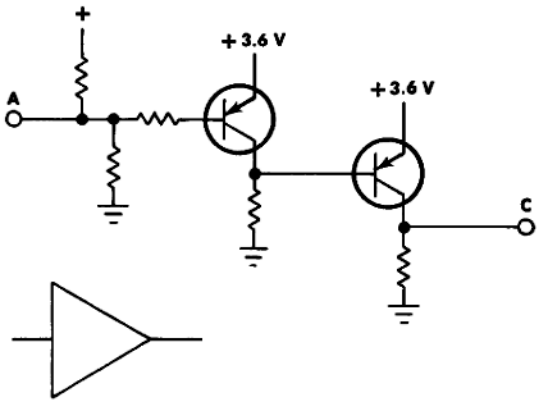
Abbreviations on the Logic Diagram include D for Decimal; U signifying Unit; GND, ground; A, Not A; and CH, channel.

Basic Logic Symbols

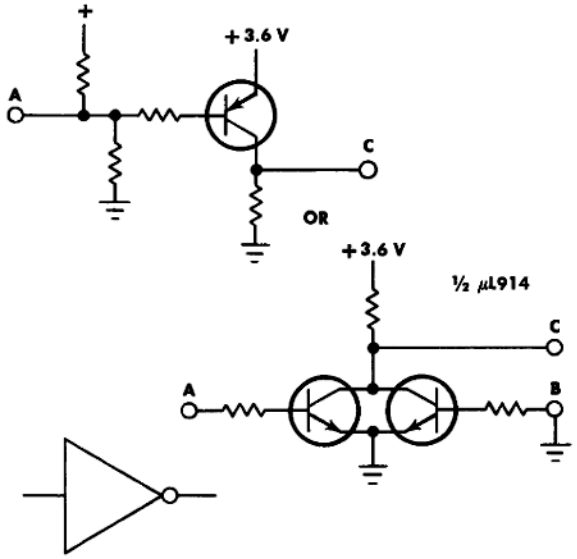
The logic symbols used in the Type 3S6 are presented in diagram form below. The sequence relates to Fig. 5-1 in a right-to-left and top-to-bottom sequence.

1 Input, 1 Output Non-Inverter

(High Z to Low Z, or voltage changing)

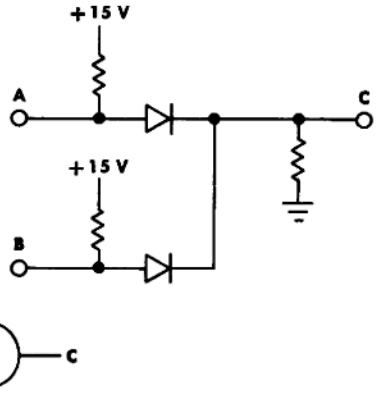


1 Input, 1 Output Inverter



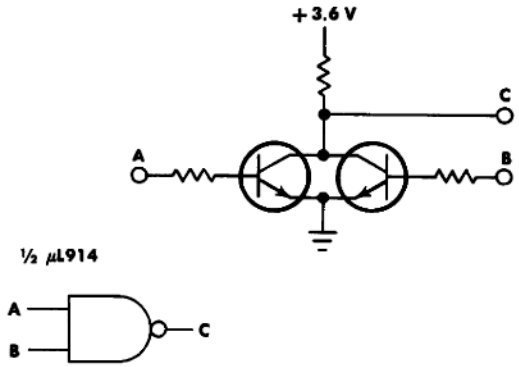
2 Input AND Gate

Both input leads must be grounded for the output to be at a logical 1.



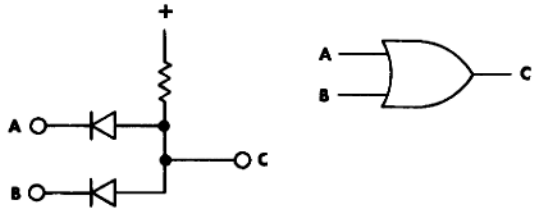
2 Input NAND Gate

If either input is pulled up to a logical ZERO, the output will be at a logical ONE. Both inputs must be at ONE for the output to be at ZERO.



2 Diode OR Gate

Either input at ONE makes the output at ONE.



2 Transistor NOR Gate (Inverting)

Neither input at ONE; output is at ONE.

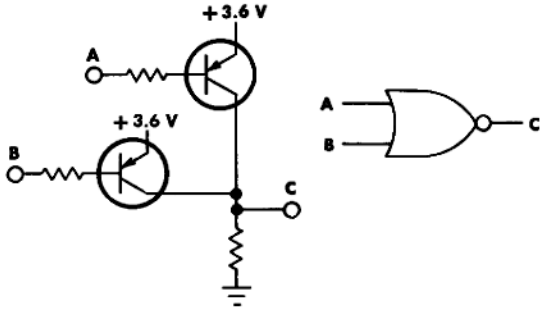
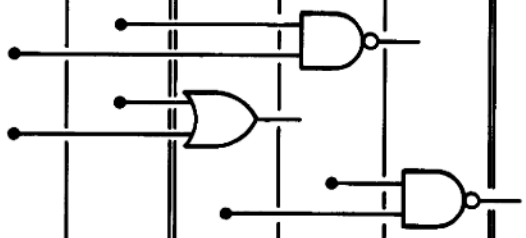


TABLE 5-5

Digital ÷ GND Output Logic States

Units/ Div	INPUT A2	LOGIC A1	Q884 Coll	Q874 Coll	D886 D885	U887A	U887B	Q891 Coll	Q892 Coll	Q893 Coll	÷
200	0	0	1	0	1	1	0	0	1	0	5
100	0	1	1	1	1	0	1	0	0	1	1
50	1	0	0	0	0	1	1	1	0	0	2
20	1	1	0	1	1	1	0	0	1	0	5
10	0	1	1	1	1	0	1	0	0	1	1
5	1	0	0	0	0	1	1	1	0	0	2
2	1	1	0	1	1	1	0	0	1	0	5



Q899 Out = 0

NOTES

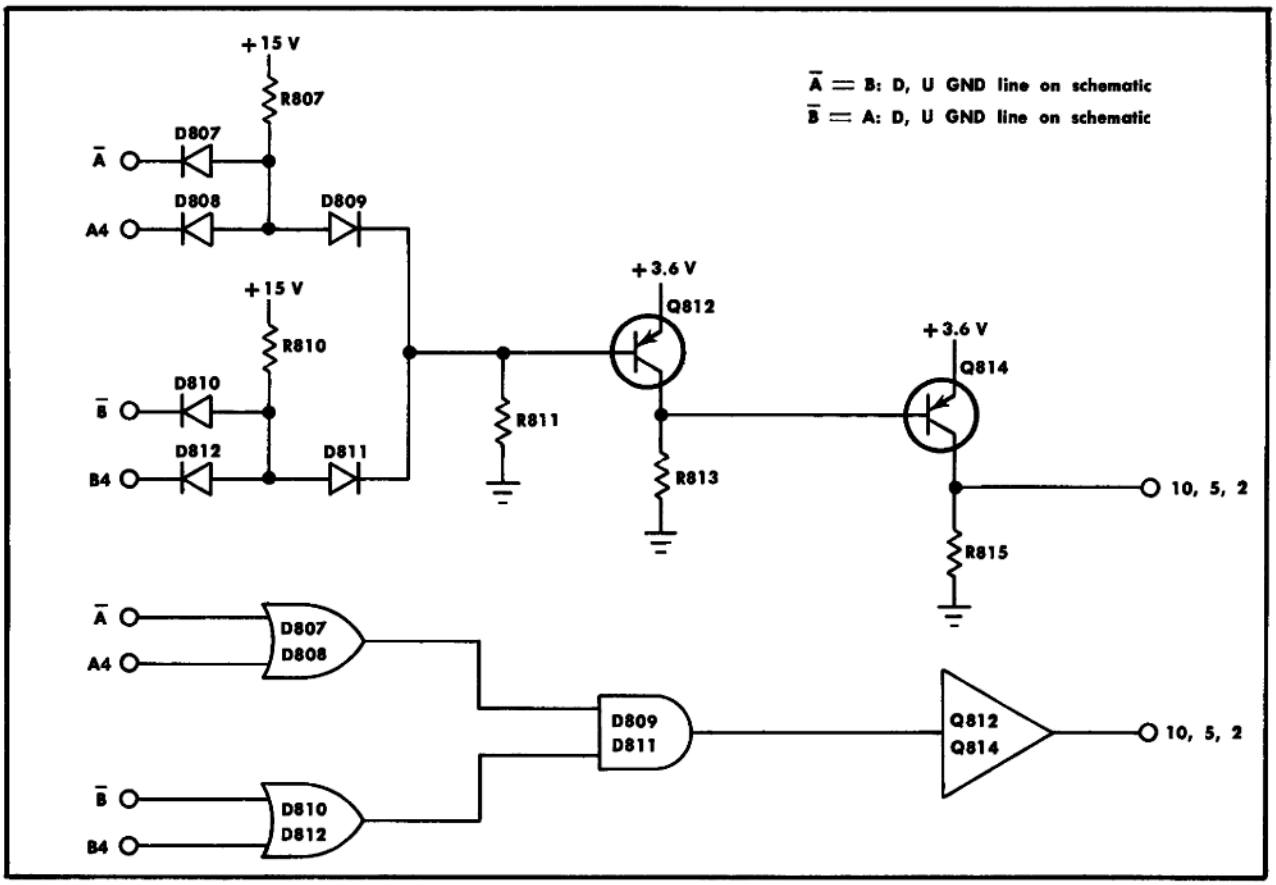
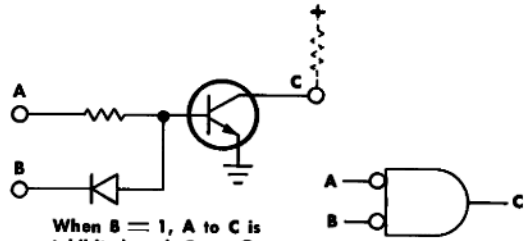


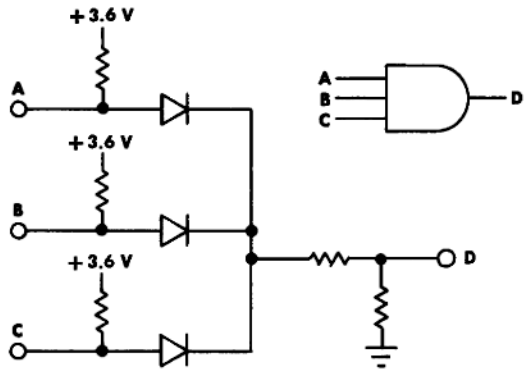
Fig. 5-2. Circuit and Logic diagrams of the 10, 5, 2 UNITS/DIV DECODER block.

1 Diode, 1 Transistor Inverted Input AND Gate



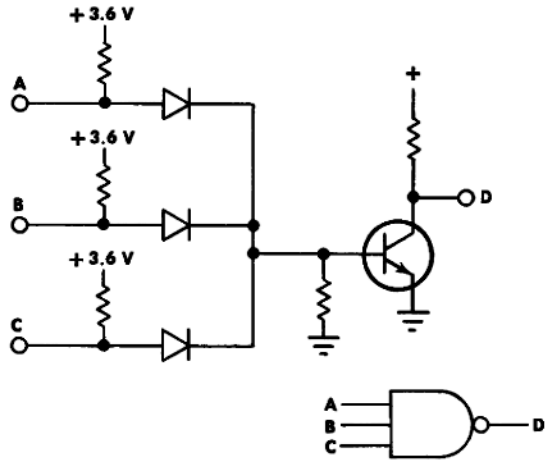
3 Input AND Gate

If all three inputs are at ONE, the output will be at ONE.



3 Input NAND Gate

The above gate with an inverter before terminal D. Only if all three inputs are at ONE, will the output be at ZERO.



CIRCUIT DESCRIPTION

One block from the Digital Unit Control portion of the complete Block Diagram is drawn in detailed schematic and basic logic form in Fig. 5-2. Fig. 5-2 should be useful

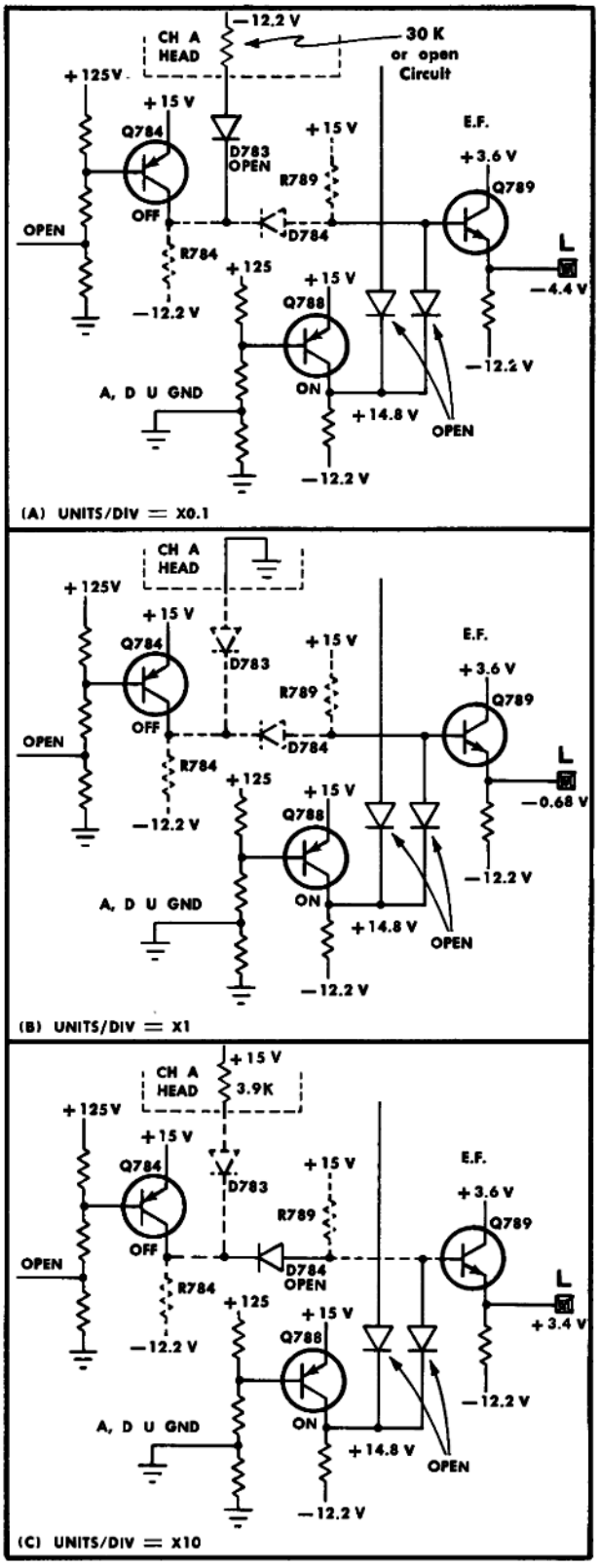


Fig. 5-3. Units/Div Multiplier Decoder circuit showing the ternary voltages for ×0.1, ×1 and ×10 Units/Div multipliers of the sampling head.

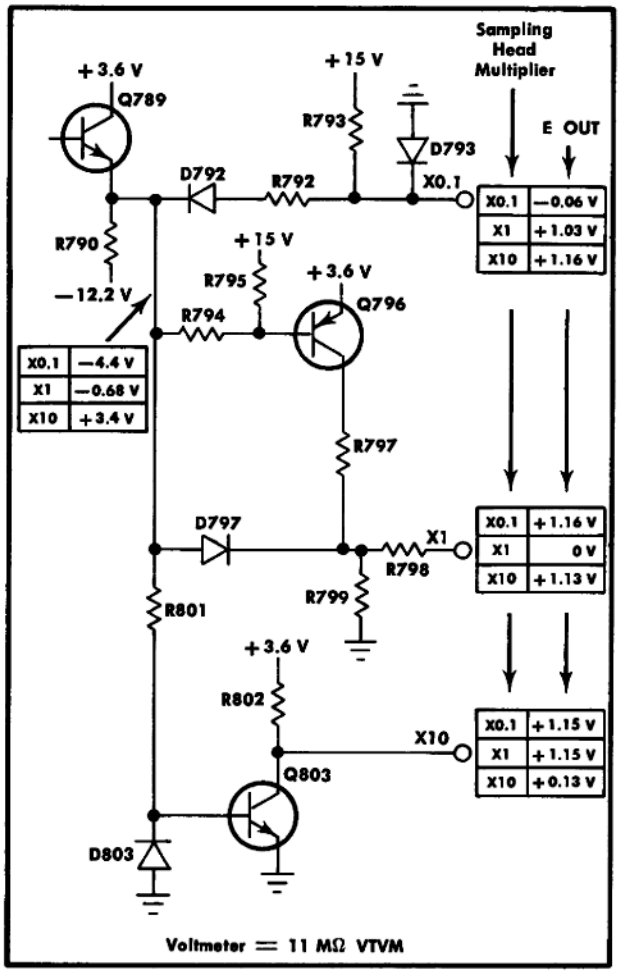


Fig. 5-4. Ternary to Binary Decoder circuit voltages.

in understanding the relationship between formal block diagram, circuit diagram and logic diagram. The block shown in Fig. 5-2 is the 10, 5, 2 UNITS/DIV DECODER.

To program the 10, 5, 2 UNITS/DIV Decoder circuit for a Channel A measurement, B is grounded. (B is the line labeled on the schematic diagram as A: D, U, GND.) At the same time, the A (not A = B: D, U, GND) line must be at a logical ZERO. This leaves only one line into the decoder circuit, the A4 line, which can affect the output at Q814 collector.

If A4 is a logical ZERO, R807 reverse-biases Q812. Q812 at cutoff lets R813 apply forward bias to Q814, saturating Q814. The circuit output is then a logical ZERO in agreement with the logical ZERO at the A4 input. This operation then agrees with the statement earlier in the block diagram description, that the 10, 5 or 2 Units/Div is programmed. Table 5-1 shows that the A4 (or B4) is a logical ONE at only 10, 5 and 2 Units/Div.

No other logic circuits will be detailed, but the simple principles stated for Fig. 5-2 apply through the rest of the Decimal Unit Control circuits that can be diagrammed into logic symbols.

Analog circuits of the Type 3S6 Digital Unit Control circuit are in the UNITS/DIV MULTIPLIER DECODER block. These are described in detail.

Units/Div Multiplier Decoder

The Units/Div Multiplier Decoder circuits (outlined on both the schematic and logic diagrams) consist of a Channel Select circuit and a Ternary to Binary Decoder. A secondary function of the Channel Select circuit is to limit the amplitude of the X0.1 and X10 Units/Div multiplier signals from the sampling head to voltage values usable at the Ternary To Binary Decoder. The multiplier signal for X1 Units/Div is not limited, but is instead a ground connection in the sampling head.

Fig. 5-3 shows the circuit changes to the input circuits of the Units/Div Multiplier Decoder for the three sampling head multiplier settings. The Channel Select portion is shown, including the current paths and output voltages for X0.1, X1 and X10 multiplier conditions. Output voltage is controlled within the Channel Select circuit for both the X0.1 and X10 condition. For the X1 condition, output voltage is determined by the ground connection in the sampling head. Thus, the circuit does not depend upon a stable current source from the sampling head except at the 1 condition.

Ternary to Binary Decoder

Fig. 5-4 shows the Ternary to Binary Decoder circuit with input and output voltages. This part of the circuit is similar to the Channel Select section, in that they both translate certain input voltage values to other output voltage values. Component conduction conditions that generate (translate) the output voltages are listed in Table 5-6.

TABLE 5-6

Ternary to Binary Conduction Paths

MULTI Units/Div	Electron Path
X0.1	Logical 1 —4.4 V at Q789 emitter, through D792, R792 and D793 to give —0.06 V at X0.1 out.
	Logical 0 —4.4 V at Q789 emitter saturates Q796. R797-R798 current into load drops Q796 collector voltage to +1.6 V at X1.
	Logical 0 Q803 is at cutoff. Current in R802 and load gives +1.15 V at X10 out.
X1	Logical 0 —0.68 V at Q789 emitter causes electron current in D792-R792-R793 to set +1.03 V at X0.1 out.
	Logical 1 R794-R795 reverse-bias Q796. No current in R797-R798 gives 0 V at X1 out.
	Logical 0 Q803 still at cutoff. Current in R802 and load gives +1.15 V at X10 out.
X10	Logical 0 +3.4 V at Q798 emitter reverse biases D792. R793 current into load gives +1.15 V at X0.1 out.
	Logical 0 D797 conducts. Current in R798 and load gives +1.13 V at X1 out.
	Logical 1 Q803 saturates to give +0.13 V at X10 out.

OUTPUTS TO DIGITAL UNIT

Decimal Control

All Units/Div Decoder and Units Multiplier Decoder signals are processed by the Decimal Control circuits as two-level binary logic. The 10, 5, 2 Units/Div Decoder, the 100, 50, 20 Units/Div Decoder, and the 200 Units/Div Decoder each feed two dual-input NAND gates of the Decimal Decoder. The X0.1, X1 and X10 input lines inhibit one gate of each pair of gates, allowing each Units/Div decoder to control only one decimal. Actually, only Decimal 4 and Decimal 5 are controlled by the decoders because the 200 Units/Div Decoder is combined with the 100, 50, 20 Units/Div Decoder output. Thus there are only two Units/Div categories controlling Decimal 4 or Decimal 5 (200, 100-50-20 and 10-5-2). Decimal 3 is programmed only when Decimal 4 or Decimal 5 are not asked for (by the combination of Units/Div decoders and Units multiplier). Table 5-7 identifies each Units/Div category control (200, 100-50-20, and 10-5-2) in the columns marked with an "X"; the Type 230 modifies the Decimal Control outputs when it receives a ÷5 command from the Counter Divide Control circuits.

Use Tables 5-2, 5-3 and 5-4 if the circuits require maintenance. Set the digital unit controls for an amplitude measurement and use an 11 MΩ VTVM to check for proper gate voltages. Voltage values for the truth tables are given at the bottom of Fig. 5-1.

Units Control

The Units Control block contains logic-type circuits that cause Q855 to conduct (for Volts) when the sampling head input logic line is at a logical ONE. Q857 conducts (for Amps) when the sampling head input line is at a logical ZERO (+15 volts through 30 kΩ). This simple mode of operation is possible whenever one of the digital unit D, U, GND lines is at a logical ONE. If both D, U, GND lines are at a logical ZERO, the output tries to program Volts, but the D, U INHIBIT signal from Q859 makes both outputs a logical ZERO. Both D, U, GND lines will be at logical ZERO when the digital unit is programmed to take a time measurement.

Counter Divide Control

All states of the Counter Divide Control block are shown in Table 5-5. The circuits are not described. Use the truth table of Table 5-5, and the voltages at the bottom of Fig. 5-1 when servicing the circuits.

Outputs Summary

Table 5-8 lists all the Digital Unit Control circuit inputs and outputs (except the V or A units) in summary form related to the digital unit readout display. The Type 230 interprets the outputs internally. On a decimal output line that is a logical ZERO, a 230 will place the output voltage at about +6 or +8 volts. The Units Mult column of Table 5-8 indicates whether the digital unit "M" lamp is lighted.

TABLE 5-7

Digital Unit Decimal Numbering

Type 230:	0 . 0 . 0 . 0 . 0 . 0
DEC:	1 2 3 4 5

TABLE 5-8

Digital Unit Control circuit outputs related to Digital Unit readout display

	Sampling Head Units/Div Multiplier														
	X0.1 20/Div to 0.2/Div					X1 200/Div to 2/Div					X10 2000/Div to 20/Div				
Units/ Div	Dec 2	Dec 3	Dec 4	Dec 5	Units Mult	Dec 2	Dec 3	Dec 4	Dec 5	Units Mult	Dec 2	Dec 3	Dec 4	Dec 5	Units Mult
200			230		m	230				None		230			None
100			230		m				230	m		230			None
50			230		m				230	m		230			None
20		230			m			230	6R1A	m	230				None
10		230			m			230		m				230	m
5		230			m			230		m				230	m
2	230				m		230			m			230		m

The Type 230 contains 5 number readout lamps and one polarity readout lamp. Table 5-7 identifies the lighted decimal neon.

When the Type 3S6 is front panel controlled and the VARIABLE control is turned from its CAL detent position the units lamps of the Type 230 go out, and the decimal neons shift around in a random manner, dependent upon the position of the Units/Div switches. This is normal.

SECTION 6
MAINTENANCE

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains maintenance information for use in preventive maintenance, corrective maintenance or troubleshooting of the Type 3S6.

PREVENTIVE MAINTENANCE

General

Preventive maintenance consists of cleaning, visual inspection, lubrication, etc. Preventive maintenance performed on a regular basis will help prevent instrument failure and will improve reliability of this instrument. The severity of the environment to which the Type 3S6 is subjected will determine the frequency of maintenance.

Cleaning

The Type 3S6 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path.

The covers of the Type 568 in which the Type 3S6 operates, provide protection against dust in the interior of the instrument. Operating without the covers in place will require more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastic used in this instrument. Some chemicals to avoid are benzene, toluene, xylene, acetone or similar solvents.

Exterior. Loose dust accumulated on the outside of the Type 3S6 can be removed with a soft cloth or small paint brush. The paint brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild solution of water and detergent. Abrasive cleaners should not be used.

Interior. Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air. Remove any dirt which remains with a soft paint brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces on circuit boards.

Lubrication

The reliability of potentiometers, rotary switches and other moving parts can be increased if they are kept properly lubricated. Use a cleaning-type lubricant (such as Tektronix Part No. 006-0218-00) on switch contacts. Lubricate switch detents with a heavier grease (such as Tektronix Part No. 006-0219-00). Potentiometers should be lubricated with a lubricant which will not affect electrical characteristics (such as Tektronix Part No. 006-0220-00). Do not over-lubricate. A lubrication kit containing the necessary lubricant and instructions is available from Tektronix. Order Tektronix Part No. 003-0342-00.

Visual Inspection

The Type 3S6 should be inspected occasionally for such defects as broken connections, improperly seated transistors, damaged circuit boards and heat-damaged parts.

The remedy for most visible defects is obvious; however, care must be taken if heat-damaged parts are located. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged parts are replaced; otherwise, the damage may be repeated.

Recalibration

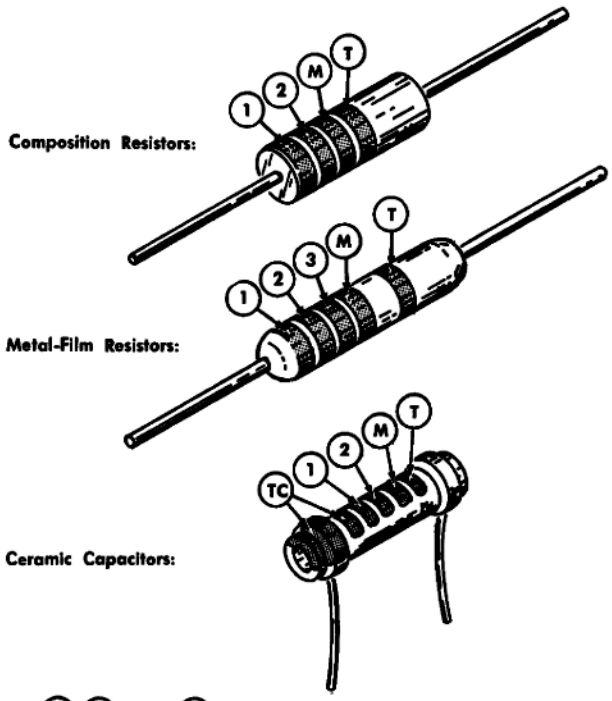
To assure accurate meaurements, check the calibration of this instrument after each 500 hours of operation or once every six months.

Parts Identification

Identification of Switch Wafers. Wafers of switches shown on the circuit diagram are numbered from the first wafer located behind the detent section of the switch to the last wafer. The letters F and R indicate whether the front or the rear of the wafer is used to perform the particular switching function. For example, the designation 2R printed by a switch section on a schematic identifies the switch section as being on the rear side of the second wafer when counting back from the front panel.

Wiring Color Code. The wiring in the Type 3S6 is color coded to facilitate circuit tracing. In the case of power-supply leads, the color code indicates the voltage carried, with the widest stripe denoting the first significant figure. Table 6-1 lists the color combinations and the voltages indicated by the colors.

Resistor Coding. The Type 3S6 uses a number of very stable metal film resistors identified by their gray background color and color coding.



Resistor and Capacitor Color Code

Color	Significant Figures	Multiplier: Resistors	Multiplier: Capacitors	Tolerance: Resistors	Tolerance: Capacitors
Silver	---	10^{-2}	---	±10%	---
Gold	---	10^{-1}	---	±5%	---
Black	0	1	1	---	±20% or 2 pF*
Brown	1	10	10	±1%	±1% or 0.1 pF*
Red	2	10^2	10^2	±2%	±2%
Orange	3	10^3	10^3	±3%	±3%
Yellow	4	10^4	10^4	±4%	+100% —0%
Green	5	10^5	10^5	±0.5%	±5% or 0.5 pF*
Blue	6	10^6	10^6	---	---
Violet	7	---	---	---	---
Gray	8	---	10^{-2}	---	+80% —20% or 0.25 pF*
White	9	---	10^{-1}	---	±10% or 1 pF*
(none)	---	---	---	±20%	±10% or 1 pF*

*For capacitance of 10 pF or less.

(1) (2) and (3) —1st, 2nd and 3rd significant figures;
(M) —multiplier; (T) —tolerance;
(TC) —temperature coefficient.

NOTE: (T) and/or (TC) color code for capacitors depends upon manufacturer and capacitor type. May not be present in some cases.

Fig. 6-1. Resistor and ceramic capacitor color codes.

If the resistor has three significant figures with a multiplier, the resistor will be EIA color coded. If it has four signficant figures with a multiplier, the value will be printed on the resistor. For example, a 333 kΩ resistor will be color coded, but a 333.5 kΩ resistor will have its value printed on the resistor body.

The color-coding sequence is shown in Fig. 6-1.

TABLE 6-1

Power Supplies Wire Color Coding

Supply	Color Code
—100 V	Brown-Black-Brown on Tan
—50 V	Green-Black-Black on Tan
—25 V	Blue-Black-Black on Tan
—12.2 V	Brown-Red-Black on Tan
+3.6 V	Orange-Violet-Black on White
+15 V	Brown-Green-Black on White
+50 V	Green-Black-Black on White
+125 V	Brown-Red-Brown on White
+300 V	Orange-Black-Brown on White

Capacitor Marking. The capacitance values of common disc capacitors and small electrolytics are marked in microfarads on the side of the component body. The white ceramic capacitors used in the Type 3S6 are color coded in picofarads using a modified EIA code (see Fig. 6-1).

Diode Color Code. The cathode end of each glass enclosed diode is indicated by a stripe, a dot or a series of stripes. For normal silicon or germanium diodes the stripes also indicate the type of diode, using the resistor color-code system (e.g., 6165 indicates the type of diode with Tektronix Part No. 152-0165-00). The cathode and anode ends of metal-encased diodes can be distinguished by the diode symbol marked on the body or by the flared end of the anode.

Parts Replacement

All parts used in the Type 3S6 can be purchased directly through your Tektronix Field Office or Representative. However, replacements for standard electronic items can generally be obtained locally in less time than is required to obtain them from Tektronix. Replacements for the special parts used in the assembly of the Type 3S6 should be ordered from Tektronix since these parts are either manufactured or selected by Tektronix to satisfy a particular requirement. Before purchasing or ordering, consult the Electrical Parts List to determine the value, tolerance and rating required.

NOTE

When selecting the replacement parts, it is important to remember that the physical size and shape

of a component may affect its performance at high frequencies. Parts orientation and lead dress should duplicate those of the original part since many of the components are mounted in a particular way to reduce or control stray capacitance and inductance. After repair, portions of the instrument may require recalibration.

Rotary Switches. Individual wafers or mechanical parts of rotary switches are normally not replaced. If a switch is defective, replace the entire assembly. The availability of replacement switches, either wired or unwired, is detailed in the Electrical Parts List.

Circuit Boards. Use ordinary 60/40 solder and a 15- to 40-watt pencil type soldering iron on the circuit boards. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the etched wiring from the base material.

Most of the components mounted on the Vertical and Output circuit boards can be replaced without removing the boards from the instrument. Observe soldering precautions given under Soldering Techniques in this section. However, if the underside of the board must be reached, refer to the directions for Circuit Board Replacement.

NOTE

Cleaning of the circuit board hole is not recommended while the board is mounted in the instrument. Solder pushed through the hole toward the back side cannot always be cleared away unless the back side is accessible. Thus, clear the mounting hole only when the board is out of the instrument.

Power Supply Capacitors, C931 and C950. Unsolder the leads and pull the capacitor from the clamp towards the top of the unit. Unsolder the bottom lead of C931. Install the replacement capacitor, solder the leads and resistor.

Power Transistor, Q969. Remove the Output Circuit Board following directions for replacement of circuit boards. Lift the insulation for the circuit board, unsolder the leads, then remove the nuts holding the transistor with a $^5/_{16}$ wrench and remove the transistor. Install the replacement transistor, resolder the leads, then replace the insulation sheet and circuit board.

Power Transformer, T950. Remove the Output Circuit Board or the Vertical Circuit Board following directions for replacement of circuit boards. Lift the circuit board insulation. Unsolder the leads and remove the screws on each side of the transformer and remove it through the opening. Install the replacement transformer, resolder the leads, then replace the insulation sheet and circuit board.

Replacement of soldered-in diodes. Grasp the diode lead between the body of the diode and the circuit board with a small pair of tweezers.

Touch the tip of the soldering iron to the lead where it enters the circuit board. Gently but firmly pull the diode lead from the hole in the circuit board. If removal of the lead does not leave a clean hole, apply a sharp object such as a toothpick or pointed tool while reheating the solder. Avoid using too much heat. Access to the rear of the circuit board is desirable.

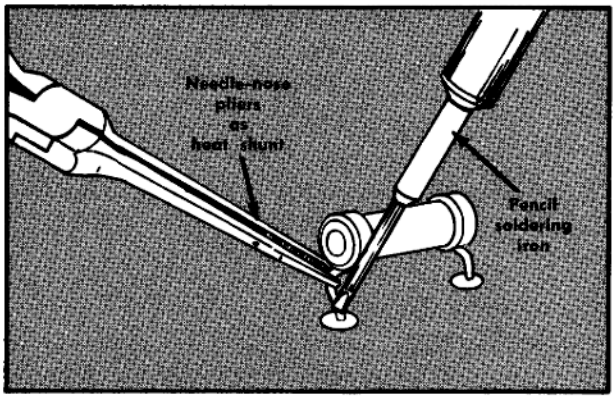


Fig. 6-2. Apply the soldering iron to the heat-shunted lead when removing a component from a circuit card.

To place the new diode, bend the leads and trim to fit just through the board. Tin each lead while using the tweezers as a heat sink. Place the diode leads in the holes. Apply a small amount of solder, if necessary, to assure a good bond. Use the tweezers as a heat sink and use only enough heat for a good connection.

Replacement of other soldered-in components. Grip the component lead with long-nose pliers. Touch the soldering iron to the lead at the solder connection. Refer to Fig. 6-2. When the solder begins to melt, pull the lead out gently.

The hole can be cleaned by reheating the solder and placing a sharp object such as a toothpick or pointed tool into the hole to clean it out.

Bend the leads of the new component to fit the holes in the board. If the component is replaced while the board is mounted in the instrument, cut the leads so they will just protrude through the board.

Pre-tin the leads of the component by applying the soldering iron and a small amount of solder to each (heat-shunted) lead. Insert the leads into the board until the component is firmly seated against the board. If it does not seat properly, heat the solder and gently press the component into place.

Apply the iron and a small amount of solder to the connection to make a firm solder joint. To protect heat-sensitive components, hold the lead between the component body and the solder joint with a pair of long-nose pliers or other heat sink.

Clip the excess leads that protrude through the board.

Clean the area around the solder connection with a flux-remover solvent to maintain good environmental characteristics. Be careful not to remove information printed on the board.

Metal Terminals. When soldering metal terminals (e.g., switch terminals, potentiometers, etc.), ordinary 60/40 solder can be used. The soldering iron should have a 40- to 75-watt rating with a $^1/_8$ inch wide chisel-shaped tip.

Observe the following precautions when soldering metal terminals:

1. Apply only enough heat to make the solder flow freely.

2. Apply only enough solder to form a solid connection. Excess solder may impair the function of the part.

3. If a wire extends beyond the solder point, clip off the excess.

4. Clean the flux from the solder joint with a flux-remover solvent to maintain good environmental characteristics.

Subassembly Removal

Circuit Board Replacement. If a circuit board is damaged and cannot be repaired, the entire assembly including all soldered-on components should be replaced. The part number given in the Mechanical Parts List is for the completely wired board.

Procedure for replacing circuit boards follows:

The center circuit boards, Offset and Logic, are removed by a steady pulling at the white plastic handle, either with thumb and forefinger, pliers or by a wire looped around the handle so the entire hand can be used. To replace the circuit boards, keep the bottom parallel to the chassis as the circuit board is placed in the side holders and push down on the handle until it is firmly in place.

The Vertical and Output circuit board assemblies are held to the Type 3S6 chassis by screws connecting to spring mountings. Be certain that the screws are gradually loosened so the circuit board assembly does not spring up at one end and cause damage. Loosen the screws one turn at a time to equalize stress caused by the springs. Check that the pins are straight before replacement. Replace the circuit board with careful alignment of the holes over the pins and with pressure on the area around the screws to overcome spring resistance for the initial screw tightening, then tighten all the screws gradually, (as in the removal), one turn at a time. If difficulty is encountered because of bent pins, remove the plastic insulating sheet, then re-install it at a position near the tops of the pins for better alignment of the pins. Install the board as above. As the board is tightened down, it will push the plastic sheet into proper position.

TROUBLESHOOTING

Introduction

The following information is provided to facilitate troubleshooting of the Type 3S6 if trouble develops. Information contained in other sections should be used along with the following information to aid in locating the defective component.

Diagrams. Circuit diagrams are given on foldout pages in Section 10. The circuit number and electrical value of each component in this instrument are shown on the diagram. Important voltages and waveforms are also shown on the diagrams.

Component Numbering. The circuit number of each electrical part is shown on the circuit diagram. Each main circuit is assigned a series of circuit numbers. Table 6-2 lists the main circuits in the Type 3S6 and the series of circuit numbers assigned to each. For example, using Table 6-2, a resistor numbered R615 is identified as being located in the CH A Programmed Offset.

TABLE 6-2

Circuit Numbers On Schematics	Circuit
1-149	CH A Programmed Amp & Attenuators
150-199	CH A Memory
200-349	CH B Programmed Amp & Attenuators
350-399	CH B Memory
400-439	A & B Channel Amps
440-499	Output Amplifier
500-599	Gate Generators
600-699	CH A Programmed Offset
700-779	CH B Programmed Offset
780-899	Digital Unit Control Logic
900-969	Power Supply
970-999	Card Connectors & Decoupling Networks

Troubleshooting Techniques

This troubleshooting procedure is arranged in an order which checks the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks assure proper connection, operation and calibration. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, it should be replaced following the replacement procedures given in this section.

1. Check Associated Equipment. Before proceeding with troubleshooting of the Type 3S6 check that the equipment used with the Type 3S6 is operating correctly. Check that the signal is properly connected and that the interconnecting cables are not defective. Also, check the power source.

2. Check Control Settings. Incorrect control settings can indicate a trouble that does not exist. For example, incorrect setting of the VARIABLE control appears as incorrect gain, etc. If there is any question about the correct function or operation of any control, see the Operation Instructions section of this manual.

3. Check Instrument Calibration. Check the calibration of the instrument, or the affected circuit if the trouble exists in one circuit. The indicated trouble may only be a result of misadjustment or may be corrected by calibration. Complete instructions are given in the Calibration section of this manual.

4. Isolate the Trouble to a Circuit. If the trouble has not been corrected or isolated to a particular circuit with the preceding steps, make the following checks if possible.

a. Check for the correct resistance readings at the interconnecting plug terminals, as indicated in Table 6-3.

If the resistance values at the horizontal interconnecting plug are equal to or higher than stated in Table 6-3, proceed with the next step.

TABLE 6-3

Interconnecting Plug Resistance Checks

Type 3S6 disconnected from Osilloscope (pin numbers omitted are unconnected)

Pin Number	Resistance to Ground	With Ohmmeter Leads Reversed
1	infinite	infinite
2	infinite	infinite
3	0	0
4	infinite	infinite
9	0	0
10	37 kΩ	12 kΩ
11	0	0
12	45 kΩ	47 kΩ
15	4.5 kΩ	4.4 kΩ
16	600 Ω	330 Ω
17	37 kΩ	12 kΩ
18	300 Ω	300 Ω
19	0	0
20	5.6 Ω	5.5 kΩ
21	37 kΩ	13.5 kΩ
22	0	0
23	3 kΩ	3 kΩ
24	5 kΩ	9.5 Ω

b. Connect the sampling head to the interconnecting cable and connect the Type 3S6 to the oscilloscope in which it will normally operate. Use the rigid extender, Tektronix Part No. 067-0590-00. Turn on the instrument and allow at least 5 minutes warmup time.

Check the power supply voltages. Convenient test points are shown in Table 6-4.

Incorrect operation of all circuits often indicates trouble in the power supplies. Check first for correct adjustment of the individual supplies. However, a defective component elsewhere in the instrument can appear as a power-supply trouble and may also affect the operation of other circuits.

Table 6-4 shows the tolerance of the internal power supply voltages, and the normal voltages supplied by the oscilloscope. If a power supply voltage is within the listed tolerances, the supply can be assumed to be working correctly. If outside the tolerances, the +15 volt adjustment may be incorrect, or a component may be defective.

Power Supply voltage checks may be made at the points indicated in Table 6-4.

Servicing the Feedback Loop

Problems that are caused by the sampling feedback loop can usually be isoluated using a calibrated signal amplitude at various deflection factors.

Errors in deflection factor, when the display does not require unity loop gain, are caused only by an attenuation error in the feedback attenuator circuits. For displays that require unity loop gain, if both the deflection factor and dot response are significantly in error at one setting of the UNITS/DIV switch, the feedback attenuator circuit is probably at fault. For displays that have a significant dot response error, without a deflection factor error, the fault is in the AC Amplifier gain changing circuit.

TABLE 6-4

Power Supply	Tolerance	Test Point Number and Location
−100 V		Pin AD, Output circuit board Pin AH, Vertical circuit board
−50 V	±0.5 V	Pin AI, Output circuit board
−25 V	±1.25 V	Pin AS, Output circuit board
−12.2 V		Pin AM, Vertical circuit board
+3.6 V	±0.18 V	Pin AR, Output circuit board Pin X, Vertical circuit board
−15 V[1]	±0.15 V	Pin AE, AF, Output circuit board Pin AJ, Vertical circuit board
+50 V (DCPL)	±1 V	Pin AK, AL, Output circuit board
+125 V		Pin AG, Output circuit board Pin AG, Vertical circuit board
+300 V		Pin V, Output circuit board

[1]Adjusted by R962.

Truth tables located on both Programmed Amp and Attenuators diagrams list the attenuator (FET) transistors which saturate at each deflection factor. These tables are valuable when troubleshooting the AC Amplifier and Feedback Attenuator circuits.

The faulty display may occur at only two positions of the Units/Div switch that are a decade apart. When this occurs, the fault is either one of the three FETs at the AC Amplifier input, or one of the three FETs at the Feedback Attenuator input.

If the fault occurs over the UNITS/DIV ranges of 200, 100, 50 and 20, the fault is either Q68/R66 or a shorted Q53, or an open Q52. If the fault occurs over the UNITS/DIV ranges of 10, 5 and 2, the fault is either Q62/R66, misadjustment of the AC Amplifier ×10 gain control, shorted Q52 or an open Q53.

Two of the truth tables list the feedback attenuation in percentage of the Memory DC output voltage. The AC Amplifier truth table does not list gain changes because neither the DC nor the instantaneous AC gain figures apply to proper circuit operation. The DC gain figures are higher than the AC gain figures, and neither apply to actual circuit operation. Correct operation of the AC Amplifier at each position of the UNITS/DIV switch can be determined only by using a calibrated amplitude signal and the CRT display. (Proper gain changes are charge quantity changes, not AC peak or DC gain changes that can be monitored on a test oscilloscope.)

What may appear as feedback loop problems can actually be attenuator control transistors Q104 through Q136. These transistors function the same for both internal control and external programming control of the deflection factor. One AND gate, D129/D136 must also be considered when the problem includes several ranges of the UNITS/DIV switch.

Once the problem has been isolated to an area of the loop, start solving the problem by transistor substitution. If that does not lead to correction, then it may be necessary to check attenuator resistor values with an accurate DC resistance bridge.

Transistor Checks

Transistors should not be replaced unless they are actually defective. Transistor defects usually take the form of the

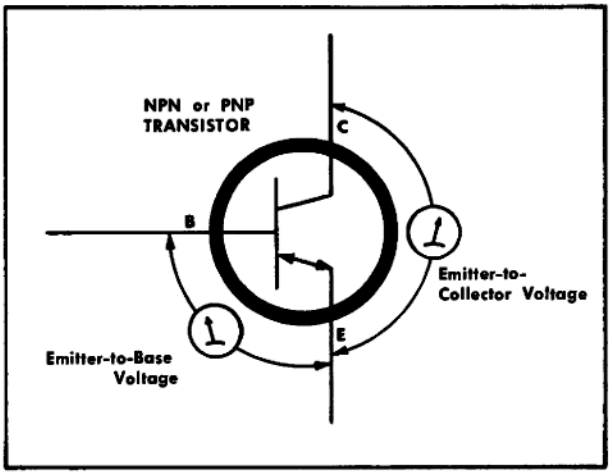


Fig. 6-3. In-circuit voltage checks NPN or PNP transistors.

transistor opening, shorting or developing excessive leakage. To check a transistor for these and other defects, use a transistor curve display instrument such as a Tektronix Type 575. However, a defective transistor can be found by signal-tracing, by making in-circuit voltage checks, or by using the substitution method. The location of all transistors is shown in the parts location figures later in this section.

To check transistors using a voltmeter, measure the emitter-to-base and emitter-to-collector voltages and determine whether the voltages are consistent with the normal resistances and currents in the circuit (see Fig. 6-3). Note the lead configuration in Fig. 6-4.

When checking transistors by substitution, be sure that the voltages on the transistor are normal before making the substitution. If a transistor is substituted without first checking out the circuit, the new transistor may immediately be damaged by some defect in the circuit.

CAUTION

Be careful when making measurements on live circuits. The small size and high density of components used in this instrument result in close spacing. An inadvertent movement of the test probes, or the use of oversized probes may short between circuits.

Diode Checks

A diode can be checked for an open or shorted condition by measuring the resistance between terminals. With an ohmmeter scale having an internal source of about 1.5 volts, the resistance should be very high in one direction and very low when the leads are reversed.

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diode. Do not measure tunnel diodes with an ohmmeter; use a dynamic tester (such as Tektronix Type 575 Transistor-Curve Tracer).

Field Effect Transistors (FET)

Field effect transistors in the Type 3S6 should not be tested with an ohmmeter. Rather, if you suspect trouble in a dual FET, pull the unit out of the socket, rotate it 180° and re-insert it. The leads are arranged in a manner to permit the unit to be installed with the guide pin either straight up or straight down. If there is no change in current or circuit operation, both sections of the dual FET are probably good.

Actual condition of either half of an FET can be checked using a Tektronix Type 575 Transistor Curve Tracer. The Gate corresponds to the Base, Drain to the Collector, and Source to the Emitter of an ordinary transistor at the curve tracer sockets.

Set the curve tracer controls:

COLLECTOR SWEEP Controls	
PEAK VOLTS RANGE	20.0
POLARITY	+ (NPN)
PEAK VOLT Control	Fully counterclockwise
DISSIPATION LIMITING RESISTOR	2 K
VERTICAL Controls	
CURRENT OR VOLTAGE	1 COLLECTOR MA
POSITION	Spot at lower left corner of graticule
HORIZONTAL Controls	
VOLTS/DIV	10 COLLECTOR VOLTS
POSITION	Spot at lower left corner of graticule
BASE STEP GENERATOR Controls	
REPETITIVE/OFF/SINGLE FAMILY	REPETITIVE
STEPS/FAMILY	Fully counterclockwise
POLARITY	—
STEPS/SEC	120 (up)
SERIES RESISTOR	Optional
STEP SELECTOR	.2 MA PER STEP
Slope Panel Controls	
Center rotary switch	EMITTER GROUNDED

Connect a 1000 Ω (1% or 5%) ½ watt resistor between the B and E binding posts on whichever side of the sloping panel you plan to test the FET. This resistor develops a voltage bias for the GATE lead at 1 volt per mA base step current.

Since the leads of the FET are short, you can avoid bending them (with a chance of breakage) by building an adapter out of a spare transistor socket and wire leads to the sloping panel binding posts.

Integrated Circuit Checks. Integrated circuits are best checked by direct substitution. Where a replacement is not available, use any of the test methods listed for transistors that can be safely used for integrated circuits.

Major Circuit and Parts Location

The remainder of this section includes photographs of sections of the Type 3S6. Major circuit areas are identified. All components mounted on circuit boards are identified by circuit numbers. All circuit board connections are identified by pin letters.

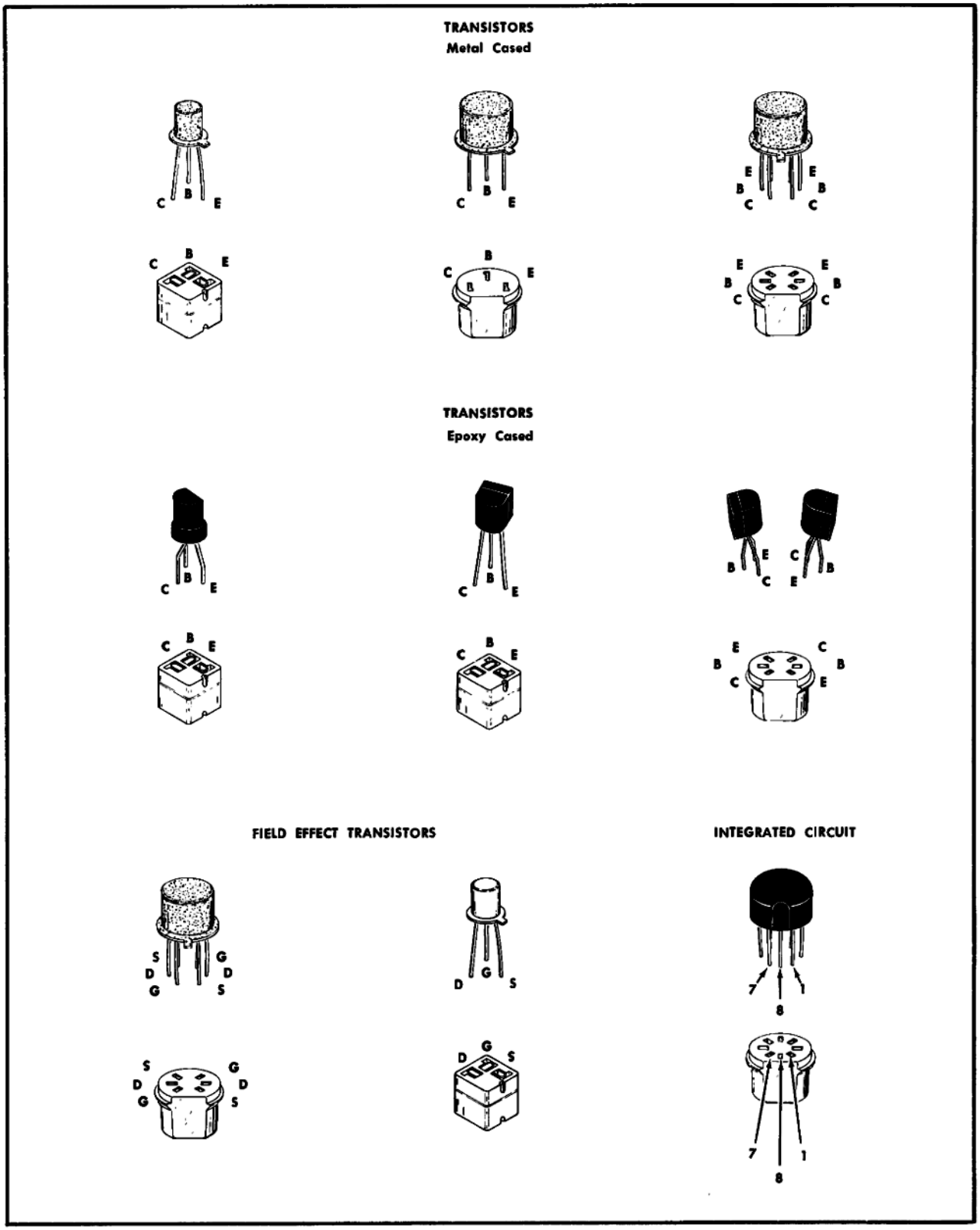


Fig. 6-4. Lead configuration for socket-mounted transistors and integrated circuits, top view.

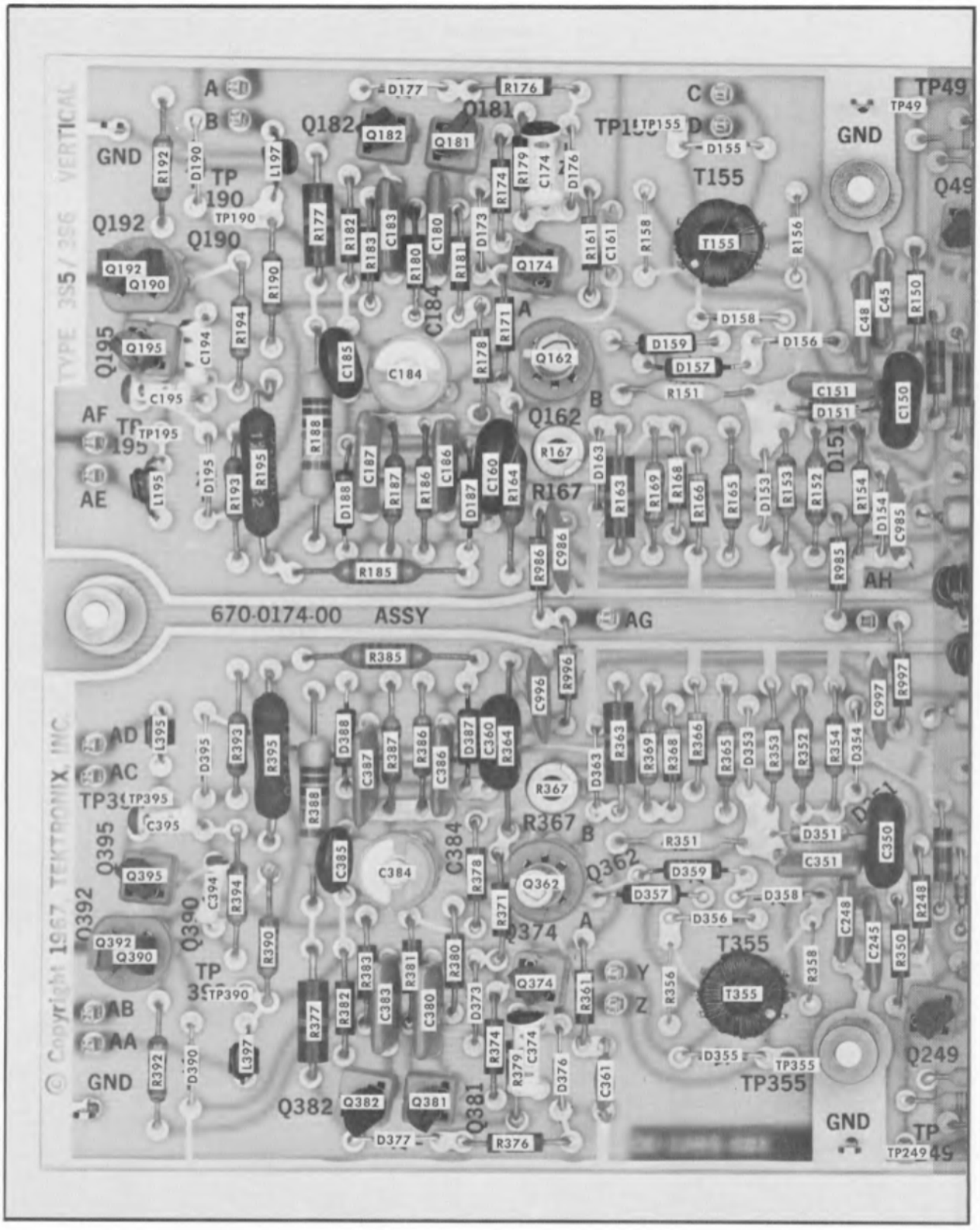


Fig. 6-5A. Vertical Circuit Board component locations.

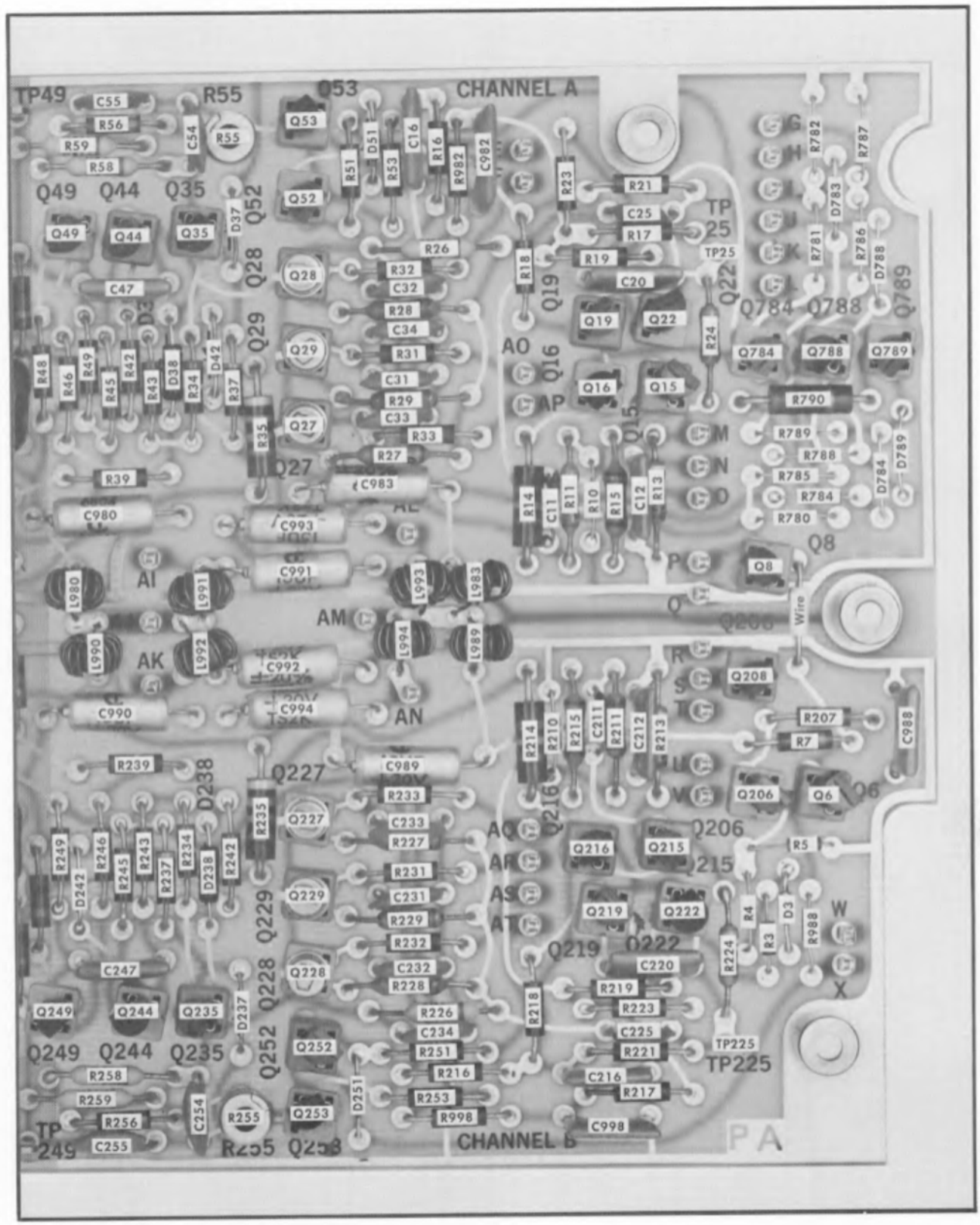


Fig. 6-5B. Vertical Circuit Board component locations.

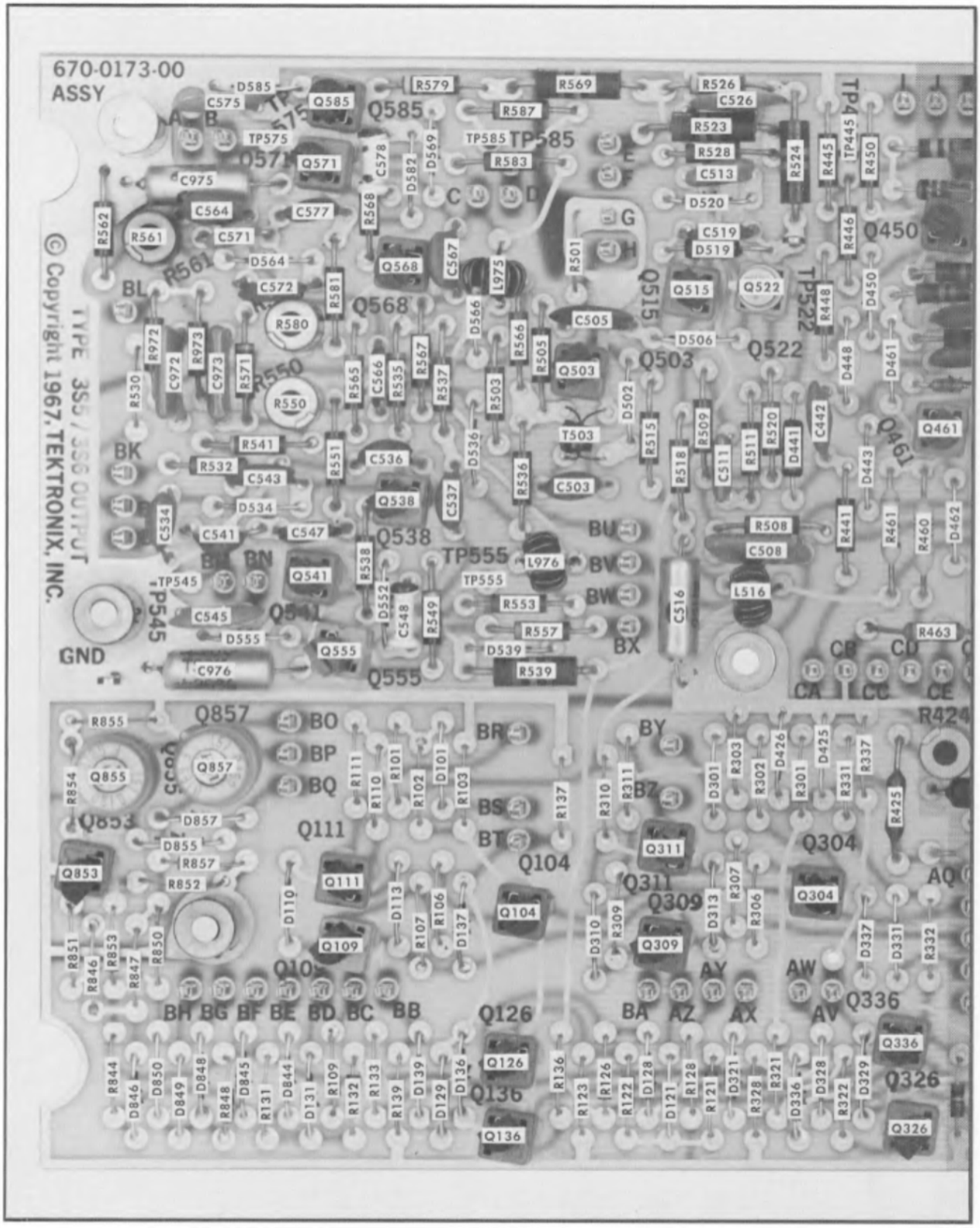


Fig. 6-6A. Output Circuit Board Assembly component locations.

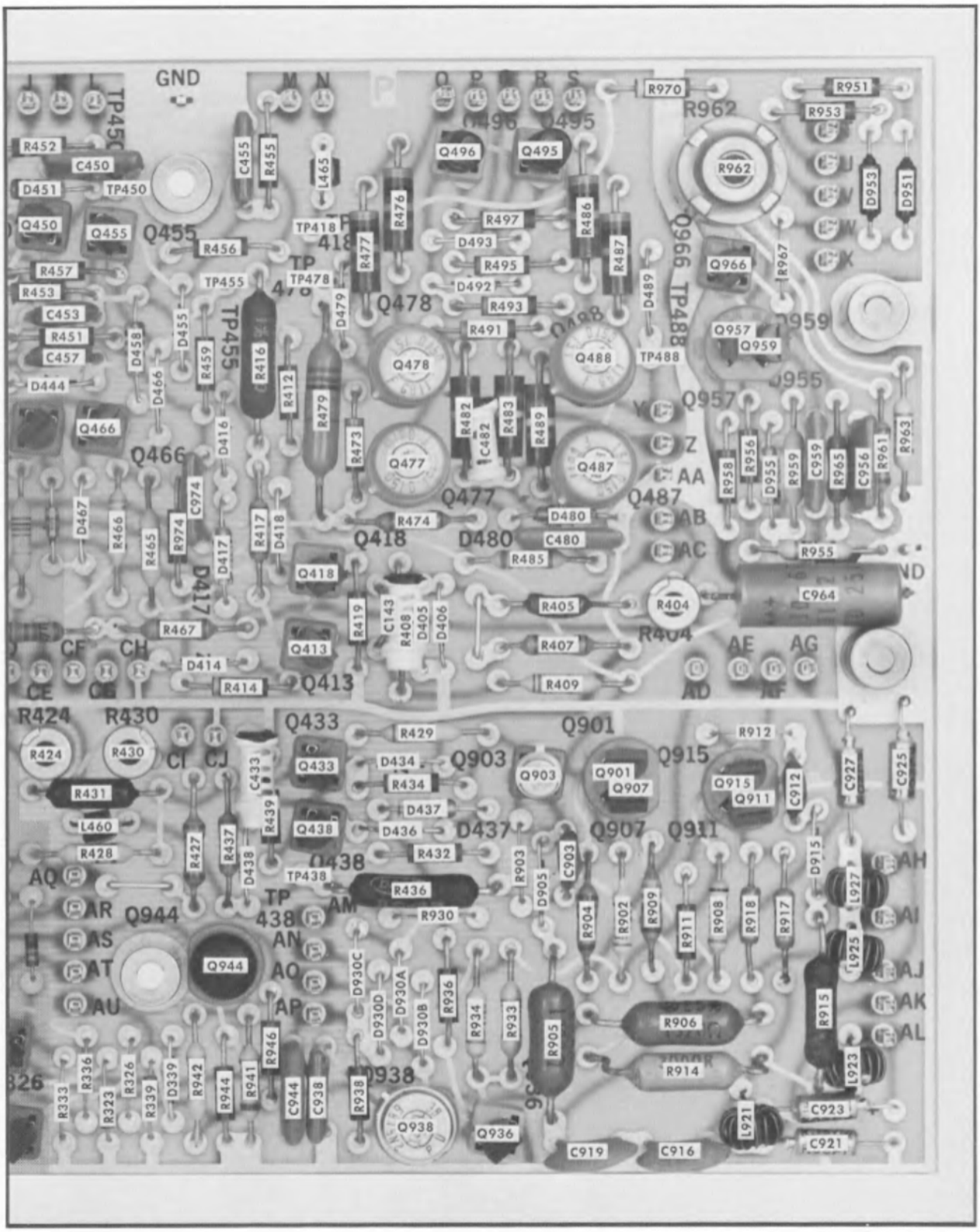


Fig. 6-6B. Output Circuit Board Assembly component locations.

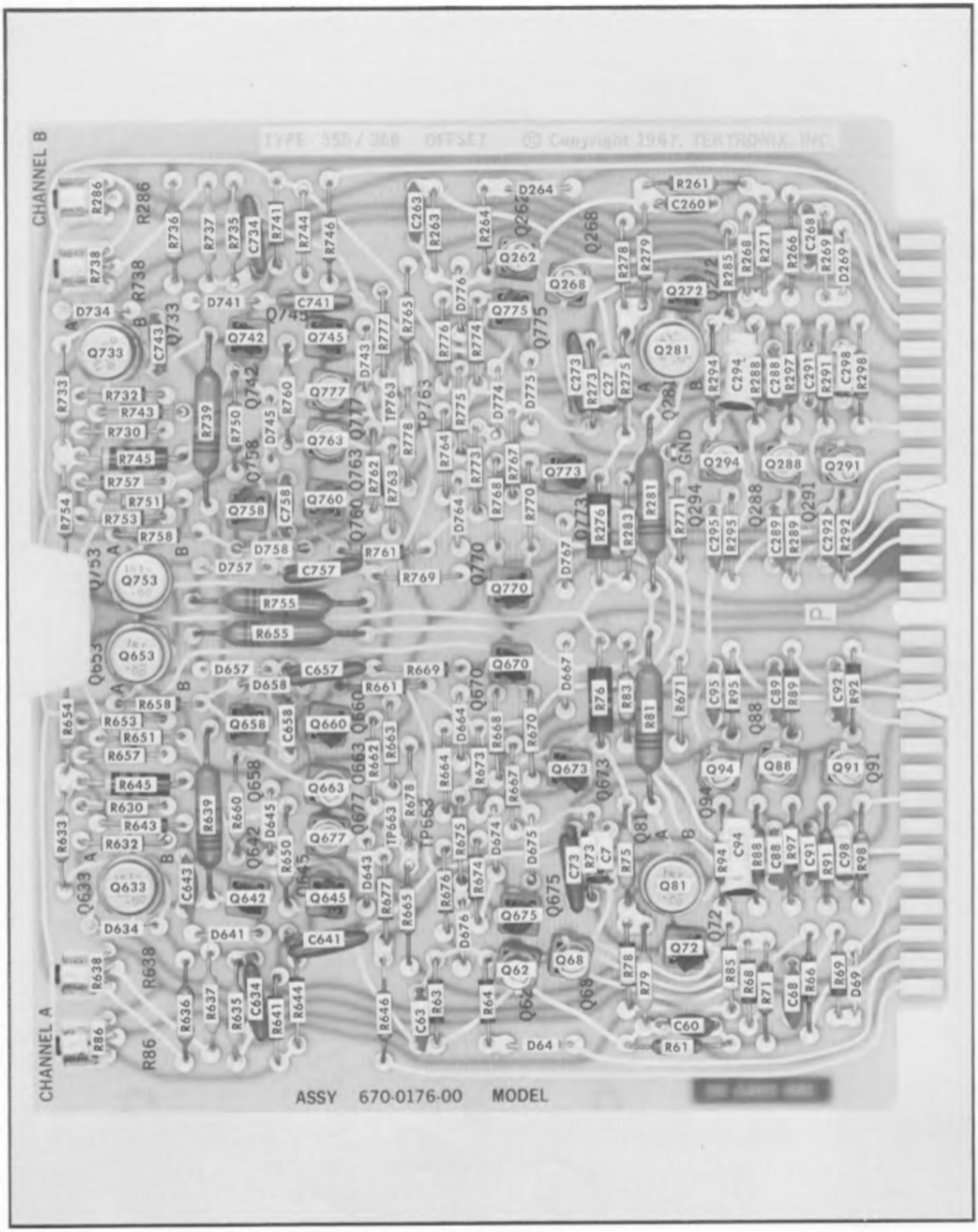


Fig. 6-7. Offset Circuit Board Assembly.

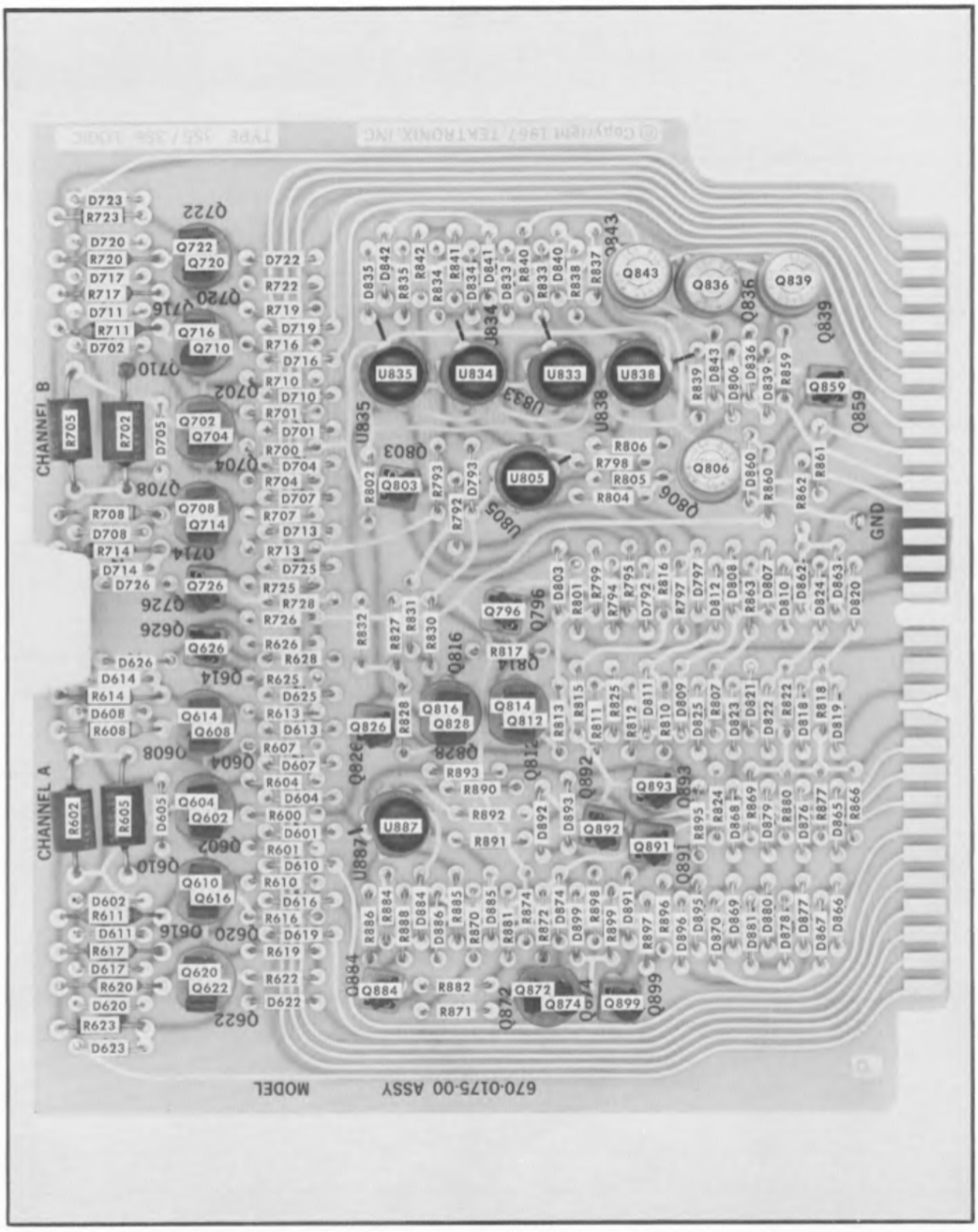


Fig. 6-8. Logic Circuit Board Assembly.

NOTES

SECTION 7
PERFORMANCE CHECK / CALIBRATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Performance Check is a method of checking the instrument's performance without internal adjustments. Failure to meet the requirements given in any check indicates the need for calibration. Performance Check steps are those identified in the type style used in the sub-heading for this paragraph. Calibration steps are headlined in the style of the next sub-heading.

Any needed maintenance should be performed before proceeding with calibration. The Calibration steps restore the instrument to original performance standards stated in Section 1.

Completing the calibration steps of this procedure matches the performance of one channel to the other, and enables both channels to operate with any S-series sampling head. It assures that the DOT RESPONSE controls and B DELAY control have sufficient electrical range for all heads. Either a Type S-1 or Type S-2 is used, with the Type S-1 recommended.

Equipment Required

The equipment list following, or its equivalent, is required for calibrating or checking the performance of the Type 3S6. To assure accuracy, all test equipment must be calibrated. If other equipment is substituted, it must meet or exceed the limits stated in the description. The first group of times includes those used in both the Performance Check and Calibration procedures. Following are additional items used only for one or the other of the two procedures.

1. Type 568 indicator oscilloscope and Type 230 Digital Unit (optional) in which to operate the Type 3S6. Also required is an interconnecting cable, Type 568 to sampling heads, Tektronix Part No. 012-0130-00.

2. Type S-1 or S-2 Sampling Head; two Type S-1 sampling heads are recommended.

3. 3T-series sampling sweep unit; Type 3T6 Programmable Sampling Sweep recommended.

4. Test Oscilloscope with vertical risetime of 20 ns or less, minimum deflection factor of 5 mV/div or less, and a comparator. For example, Tektronix Type 545B with Type W plug-in unit.

5. 1× Probe, Tektronix Part No. 010-0193-00.

6. Square wave and pulse generator that produces 1 μs and 10 μs period square waves with 1.0 volt peak amplitude into 50 Ω; 0.5 volt peak amplitude into S-1, or 0.2 volt peak amplitude into S-2. Also required is a pulse of approximately 0.25 volt with $\leq$ 70 ps risetime. The Tektronix Type 284 will meet the above requirements, with attenuators, items 7 and 8. (If your Type 284 leadtime switch is labeled 5 ns — 50 ns, order modification Kit, Tektronix Part No. 040-0487-00.)

7. 50 Ω 2× attenuator with GR 874 connectors, such as GR874-G6. Tektronix Part No. 017-0080-00.

8. 50 Ω 5× attenuator with GR 874 connectors, such as GR874-G14. Tektronix Part No. 017-0079-00.

9. 50 Ω coaxial cable with GR 874 connector such as 5 ns signal delay RG58C/U cable, Tektronix Part No. 017-0512-00.

10. 50 Ω cable, approximately 4 feet long with BNC connectors, for example, RG58C/U, Tektronix Part No. 012-0057-00. (This cable is supplied with the Type 284.)

11. Small-bit screwdriver for making adjustments.

12. If calibrating with a Type S-3, a 50 Ω Voltage Pickoff unit, Tektronix Part No. 017-0077-01 and a 50 Ω end-line termination, GR 874-W50B, Tektronix Part No. 017-0081-00.

Calibration Aids

Items in the list below are required for complete calibration, but not for Performance Check.

13. Flexible interconnecting cable, Tektronix Part No. 012-0066-00, and rigid plug-in extender, Tektronix Part No. 067-0590-00 Calibration Fixture, to operate the Type 3S6 outside the indicator oscilloscope.

14. 10× Probe, P6010. Tektronix Part No. 010-0188-00.

15. If a Type W Plug-in Unit is not available, a precision voltmeter is needed that can measure up to +50 or —50 volts with an accuracy of +0.25%. John Fluke Model 801B meets the requirements.

16. Bench multimeter such as Triplett Model 630-NA.

17. Normalizer Head, optional for Loop Gain adjustment and to check Digital logic; Tektronix Calibration Fixture 067-0572-00.

18. Patch cord with insulated alligator clips (not shown).

19. Circuit card extender. Tektronix Part No. 012-0149-00.

Performance Check Equipment

The items listed below are needed to complete the Performance Check, but are not required for calibration.

20. 50 Ω Amplitude Calibrator. Output impedance 50 Ω; voltage range 0.012 to 1.2 volt square wave; accuracy within ±0.25%. Tektronix Calibration Fixture 067-0508-00.

21. Patch cord, BNC to banana plug. Tektronix Part No. 012-0090-00. A 10 kΩ resistor (not shown) is required with a Type 3T6 Sampling Sweep Unit.

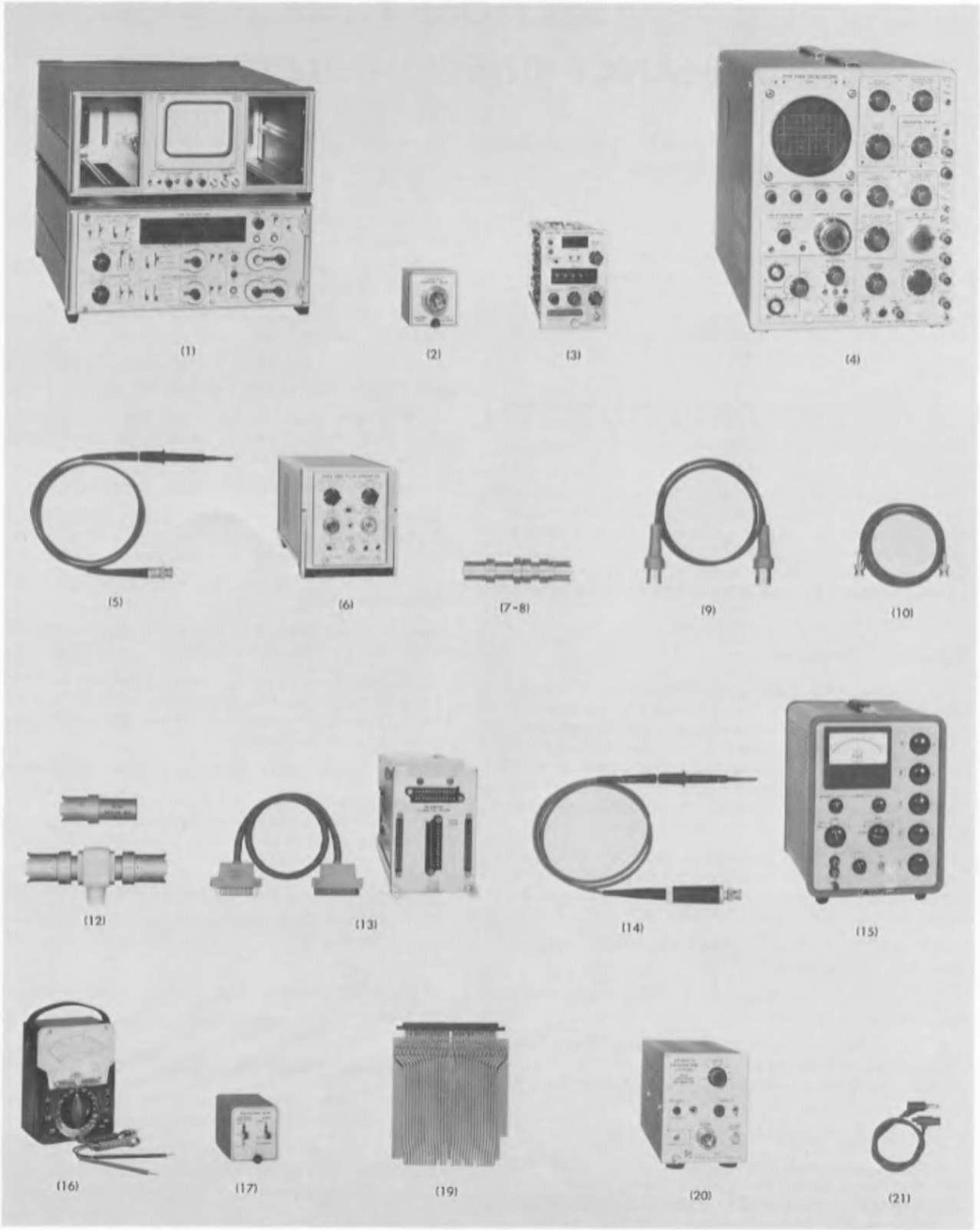


Fig. 7-1. Equipment required for recalibration or performance check.

PERFORMANCE CHECK AND CALIBRATION RECORD INDEX

The following abridged procedure may be used as a performance check or caibration procedure guide by the experienced calibrator, or it may be used as a record. (Tektronix Inc. authorizes reproduction of the abridged procedure by any user of the equipment). The step numbers and titles are identical to those used in the complete procedure. When the instrument meets the requirements in the Performance Check steps, the Type 3S6 will meet all Characteristics listed in Section 1.

Type 3S6 Serial No. _____

Performance/Calibration Date _____

Performed by _____

☐ 1. Check and Adjust Power Supplies (Page 7-6)

+3.6 Volt value _____

+15 Volt value _____

+50 Volt value _____

−25 Volt value _____

−50 Volt value _____

☐ 2. Check Gate Generator and Sampling Head Avalanche Operation (Page 7-6)

Blanking pulse width at 50% amplitude points _____ (2 μs to 4 μs)

☐ 3. Check Dot Response and Smoothing (Page 7-6)

DOT RESPONSE control can be set for a unity dot response display. Change of NORMAL-SMOOTH switch from NORMAL to SMOOTH changes dot response from unity to $\leq$0.3.

☐ 4. Adjust Memory Gate Width Controls (Page 7-7)

Maximum dot response

☐ 5. Adjust Sampling Head Snap Off and Avalanche Volts Controls (page 7-7)

Near maximum dot response

☐ 6. Adjust Sampling Head Bridge Balance Controls (Page 7-8)

No trace movement with Units/Div switch change.

☐ 7. Adjust Smoothing Balance Controls (Page 7-8)

No trace shift as NORMAL-SMOOTH switch is changed.

☐ 8. Check Vertical Digital Accuracy (with Readout System) (Page 7-9)

Accuracy within 2%.

☐ 9. Check Digital Intensified Zone Enable Square Wave ±0.7 V or more at TP445 (Page 7-10)

☐ 10. Adjust Digital Gain Controls (Page 7-10)

Correct Digital Unit reading

☐ 11. Check Deflection Factor Accuracies Over Range of Units/Div Switch and Variable Control (Page 7-10)

Variable control at CAL; accuracy within 3% at NORMAL and 4% at SMOOTH settings of NORMAL-SMOOTH switch; Variable control increases deflection 2.5 times or more when control is turned clockwise from CAL position.

☐ 12. Adjust GAIN and A-B Bal Controls (Page 7-11)

Correct operation

☐ 13. Check DC Offset (EXT PROG and Front Panel Controls) (Page 7-11)

EXT PROG Accuracy within 2% of programmed value, or 5 mV whichever is greater, Front Panel control, range of +1 to −1 V, accuracy within 10 mV of same offset voltage in EXT PROG mode.

☐ 14. Check Position Indicators and Adjust Centering Control (Page 7-13)

Indicator neon will light showing direction trace is off graticule.

☐ 15. Adjust Loop Gain Using Normalizer Head Calibration Fixture (Page 7-13)

2.5 volt peak to peak amplitude of signal at TP190 (Channel A) or TP 390 (Channel B) with mid-range (electrical center) setting of DOT RESPONSE control.

☐ 16. Adjust Loop Gain (Page 7-14)

Correct balance between sampling head Gain control and Type 3S6 Loop Gain controls.

☐ 17. Check Interchannel Delay Range (Page 7-15)

B DELAY control range is 10 ns and can match the B display to the A display.

☐ 18. Adjust A Delay Control (Page 7-15)

B DELAY control range is within +5 ns and −5 ns of A display.

☐ 19. Check Memory Slash (Page 7-15)

Vertical dot drift is $\leq$0.1 div when sampling sweep unit is triggered at 20 Hz.

☐ 20. Adjust Offset Cal and Zero (Page 7-16)

Correct Offset Voltage.

☐ 21. Adjust Attenuator Zero (Page 7-16)

Correct operation, see procedure.

☐ 22. Check Digital Control Logic with Normalizer Head (Page 7-17)

Units and Decimal Lamps to be lit with setting of Units/Div Multiplier and Units/Div switches; see Table 7-5.

PRELIMINARY PROCEDURE

Performance Check

Install the two supplied small interconnecting circuit cards into the two 30 pin connectors, J13 and J14, located on the Type 3S6 rear panel. Install the Type 3S6 into the Type 568 Oscilloscope left side plug-in compartment. Connect a calibrated sampling head to the Channel A connector of the dual flexible sampling head interconnecting cable (Tektronix Part No. 012-0130-00, supplied with the Type 3S6). Connect the other end of the sampling head interconnecting cable to J113 at the rear panel of the Type 568 Oscilloscope.

Calibration Procedure

a. Place the Type 3S6 center-mounted Offset circuit card on an extender (item 18 of equipment required) and insert the extender and Offset card in place. The Offset circuit card is now fully above the instrument top and properly connected through the extender.

Install the rigid plug-in extender (item 12 of equipment required) first to the rear of the Type 3S6, and then into the Type 568 left plug-in compartment. The extender clips over the Type 3S6 rear panel, and then is firmly held in place by pressure from the top of the Type 568 opening.

NOTE

Four small interconnecting circuit cards are required for the extender connections of the Type 3S6 to the Type 568. Two are supplied with the Type 3S6 and two are supplied with the extender (item 12 of equipment required). If the sampling head is a Type S-3, use a VP-2 and 50 Ω termination at the end of the coaxial cable. Insert the probe tip into the VP-2.

b. Install the Type 3T6 (or other sampling sweep unit) into the indicator oscilloscope right side compartment.

c. Remove the case from the sampling head to be used in this procedure. Connect the sampling head to the Channel A connector of interconnecting cable 012-0130-00. Make certain that both the coaxial (trigger) connector and the Sampler Board Multi-terminal contacts are properly mated. Leave the Type 3S6 Channel B cable disconnected.

CAUTION

When the sampling head cover is off, always turn off the oscilloscope power before connecting the head or changing channel installation. Component damage (to Type S-1, S-2 blow-by compensating transistors) can be caused by irregular contact sequence when the head is installed with no cover.

PERFORMANCE CHECK/CALIBRATION PROCEDURE

Both procedures

Make all power connections. Turn on the power to all equipment. Allow five minutes warmup time before proceeding. Set the controls as listed following Fig. 7-2.

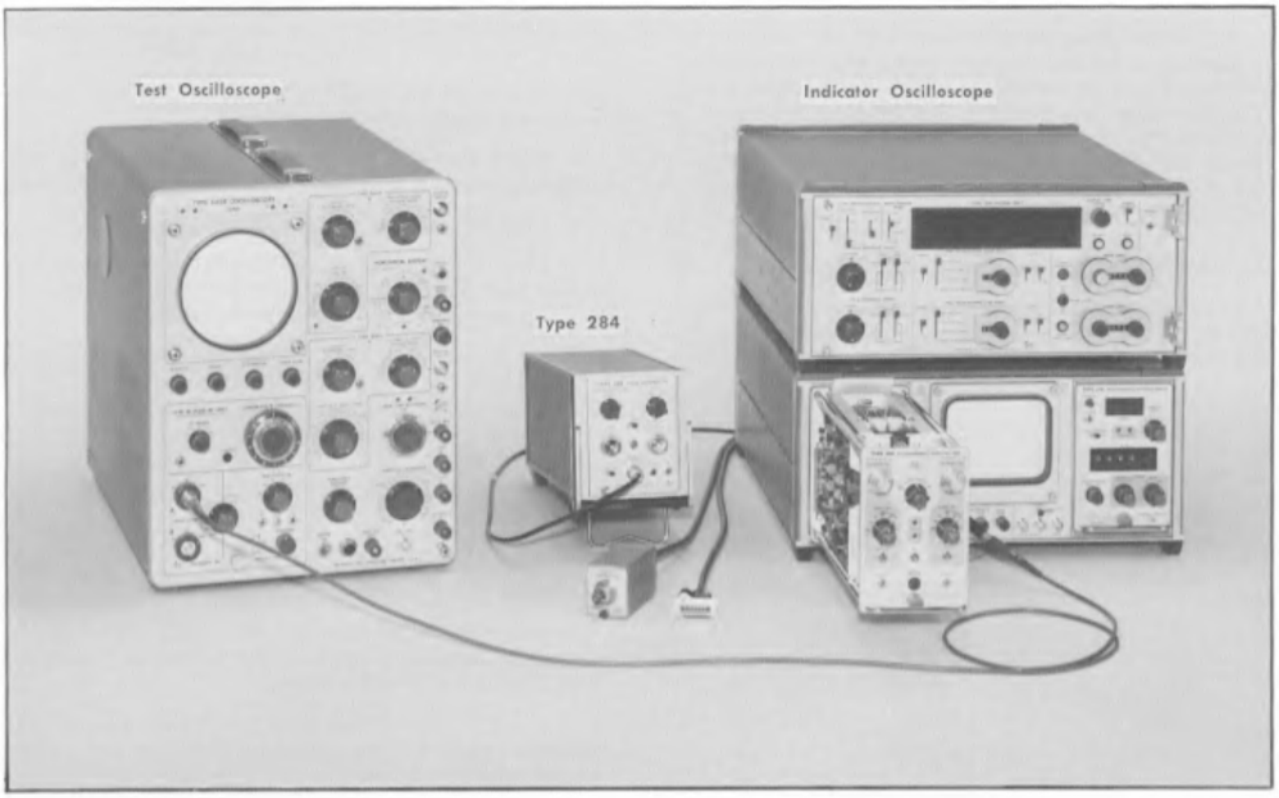


Fig. 7-2. Initial test equipment setup for step 1.

Control Settings

Type 3S6 (Both Channels)

Mode Switch	CH A
UNITS/DIV	100
VARIABLE	CAL
INVERT	Pushed in
DC OFFSET	0

Type 3T6

Horiz Pos	Midrange
Horiz Gain	As set
Samples/Sweep	1000
Decade	7 } 500 ns/div
Multiplier	5 }
Delay	0000
Program Selector	Int
Triggering	
Sensitivity	Fully clockwise
Recovery Time	Midrange
Mode	Ext
Polarity	+

Type 284

Mode	Square Wave
Period	1 μs
Square Wave Amplitude	1.0 V
Lead Time	75 ns

Test Oscilloscope

Sweep Rate	5 ms/div
Vertical	
With 1× Probe	10 mV/div, AC coupled
Triggering	+ line

NOTE

If the sampling head being used is known to operate correctly, do not adjust any controls at this time. If the sampling head is being calibrated at the same time the Type 3S6 is being calibrated, preset the Bridge Volts control fully clockwise; see Fig. 7-8. (The control will probably remain full clockwise in a Type S-1, and may be readjusted in the Type S-2.)

1. Check and Adjust Power Supplies

a. Refer to Fig. 7-3 to locate the power supply test points and the +15 Volt adjustment control. Location is on the Output circuit board, instrument right side.

Use the Type W Unit with a 1× probe or a precision voltmeter. Connect the probe to the test points in succession. Set the Type W mV/cm switch to 5 mV to check the ripple on the test oscilloscope.

c. CHECK—Power supply voltages within tolerances listed as follows:

Voltage	Tolerance	Ripple
+3.6 V	5%, ±0.18 V	20 mV
+15 V	1%, ±0.15 V	2 mV
+50 V	2%, ±1.0 V	7 mV
−25 V	5%, ±1.25 V	10 mV
−50 V	1%, ±0.5 V	7 mV

NOTE

Power supply voltage and ripple tolerances are guides to correct instrument operation, not instrument performance requirements. Actual values may exceed listed tolerances with no loss in measurement accuracy, if the instrument meets the performance requirements. Actual values may exceed listed tolerances with no loss in measurement accuracy, if the instrument meets the performance requirements in Section 1 as tested in this procedure.

d. ADJUST—+15 Volts control, R962, for +15 volts if part C showed the +15 volt supply to be out of tolerance.

2. Check Gate Generator and Sampling Head Avalanche Operation

a. Change the test oscilloscope probe from 1× to 10× and reset the test oscilloscope controls for:

Sweep Rate	20 μs/div
Vertical	
With 10× Probe	20 V/div, AC coupled
Triggering	+ Internal

b. Connect the test oscilloscope 10× Probe ground clip to a ground test point so the tip can reach (Test Point) TP522, should be similar to that shown in Fig. 7-4C.

c. Center the test oscilloscope display vertically and increase the sweep rate to 1 μs/div.

d. Check that the banking pulse duration at the 50% amplitude points is between 2 μs and 4 μs (2 to 4 divisions).

e. Reset the test oscilloscope sweep rate to 20 μs/cm.

f. Connect the probe ground clip so the tip can be connected to Q69 emitter (Sampling Head); see Fig. 7-4B. The signal should be similar to that shown in Fig. 7-4D.

NOTE

The test points checked in Step 2 are of particular value if you cannot obtain a free-run trace. If there is no signal to TP522, check that the sampling sweep unit is actually free running.

3. Check Dot Response (Loop Gain) and Smoothing

Requirements—NORMAL: DOT RESPONSE control can be set for a unity loop gain display when the NORMAL-SMOOTH switch is at NORMAL.

SMOOTH: Loop gain is displayed as ≤ 0.3 when the sampling sweep unit operates in a normal sequential dot sampling process.

a. Set the UNITS/DIV switch to 100 with a Type S-1; to 50 with a Type S-2; 200 with a Type S-3. Set the Type 284 to deliver 1 μs square waves at 1.0 volt. Install the appropriate 50 Ω attenuator listed in Table 7-1 between the signal cable and the Type 284 output connector.

b. Set the sampling sweep unit for 500 ns/div (0.5 μs/div). Obtain a double-triggered display on the indicator oscilloscope by free running the time base and adjusting the Recovery Time control. The display should be similar to any one in Fig. 7-5.

c. Set the DOT RESPONSE control to unity loop gain as in Fig. 7-5A.

d. Change the NORMAL-SMOOTH switch from NORMAL to SMOOTH.

e. Check that the display is less than 1.5 divisions at the point indicated in Fig. 7-6A with the Type S-1 or S-3, or less than 1.2 divisions at the same point with the Type S-2.

f. Reset the switch to NORMAL.

g. Move the sampling head to Channel B, (turn power off if Sampling head cover was removed) and repeat Part C of Channel B Dot Response.

TABLE 7-1

Attenuator To Be Used With Type 284

Sampling Head	Attenuator	P-P Signal Desired at Input	Type 284 Square Wave Amplitude
S-1	2×	0.5 V	1.0 V
S-2	5×	0.2 V	1.0 V
S-3	None	1.0 V	1.0 V

h. Return the sampling head to Channel A (turn power off if cover was removed).

4. Adjust Memory Gate Width Controls

a. Leave the 10× Probe on the test oscilloscope vertical input. Connect the 1× Probe to the test oscilloscope External Trigger input connector. Reset the test oscilloscope controls for:

Sweep Rate	0.1 μs/div
Vertical	
With 10× Probe	0.1 V/div
Triggering	+ External

b. Install a 50 Ω attenuator onto the Type 284 Square Wave and Sine Wave Output connector (see Table 7-1). Place a coaxial cable (with GR 874 connectors) between the attenuator and the sampling head input connector. If the sampling head is a Type S-3, use a VP-2 and 50 Ω termination at the end of the coaxial cable. Insert the probe tip into the VP-2.

c. Place the coaxial cable (with BNC connectors) between the Type 284 Trigger Out connector and the sampling sweep unit External Trigger input connector.

d. Refer to Fig. 7-7 for the Type 3S6 test points located on the instrument left side. Controls are shown in Fig. 7-4A. Connect the test oscilloscope external trigger 1× probe tip to TP155. Connect the vertical 10× probe tip to the Q15 base at R13.

e. Adjust the sampling sweep unit Trigger Sensitivity and Recovery Time controls for a double-triggered indicator oscilloscope display similar to any in Fig. 7-5. The test oscilloscope display should be similar to the waveform in Fig. 7-8A when the sampling head is Type S-1, to Fig. 7-8B or C if the sampling head is Type S-2, and similar to Fig. 7-8D if the sampling head is a Type S-3. (It is recommended that a Type S-3 be used if available.)

f. Locate R580, the A Memory Gate Width control (see Fig. 7-4) and adjust it for an indicator oscilloscope display of maximum loop gain. Adjust R580 while observing both the top and bottom flat portions of the display. The final position is when any plus or minus loop gain non-linearity is minimum, not just maximum loop gain at the display top. The test oscilloscope display is at maximum amplitude for maximum loop gain.

g. Move the sampling head to Channel B. (It is not necessary to turn the power off unless the sampling head cover has been removed.) Move the test oscilloscope 10× probe tip to Q215 base at R213. Change the Type 3S6 Mode switch to CH B and obtain a display. Locate R550, the B Memory Gate Width control (see Fig. 7-4) and adjust it for the maximum loop gain as in part f.

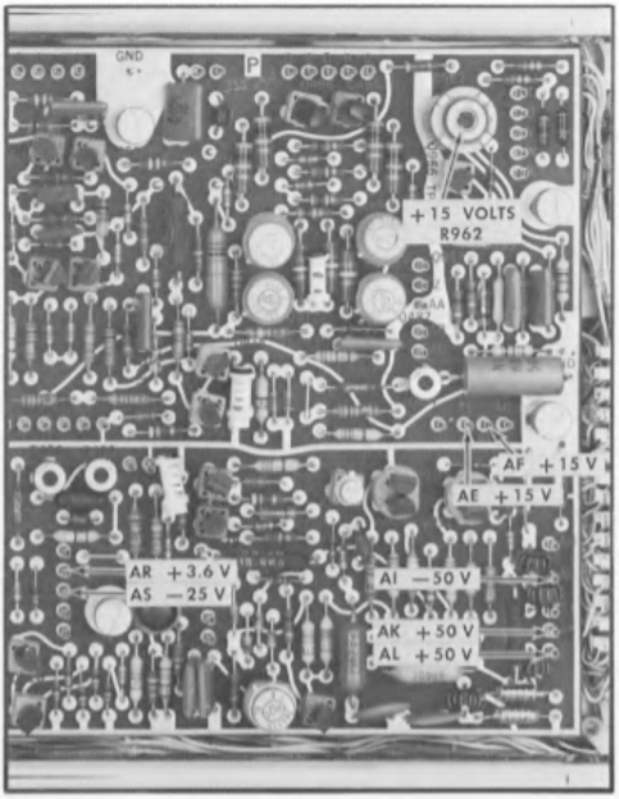


Fig. 7-3. Location of power supply test points and +15 Volt adjustment, instrument right side.

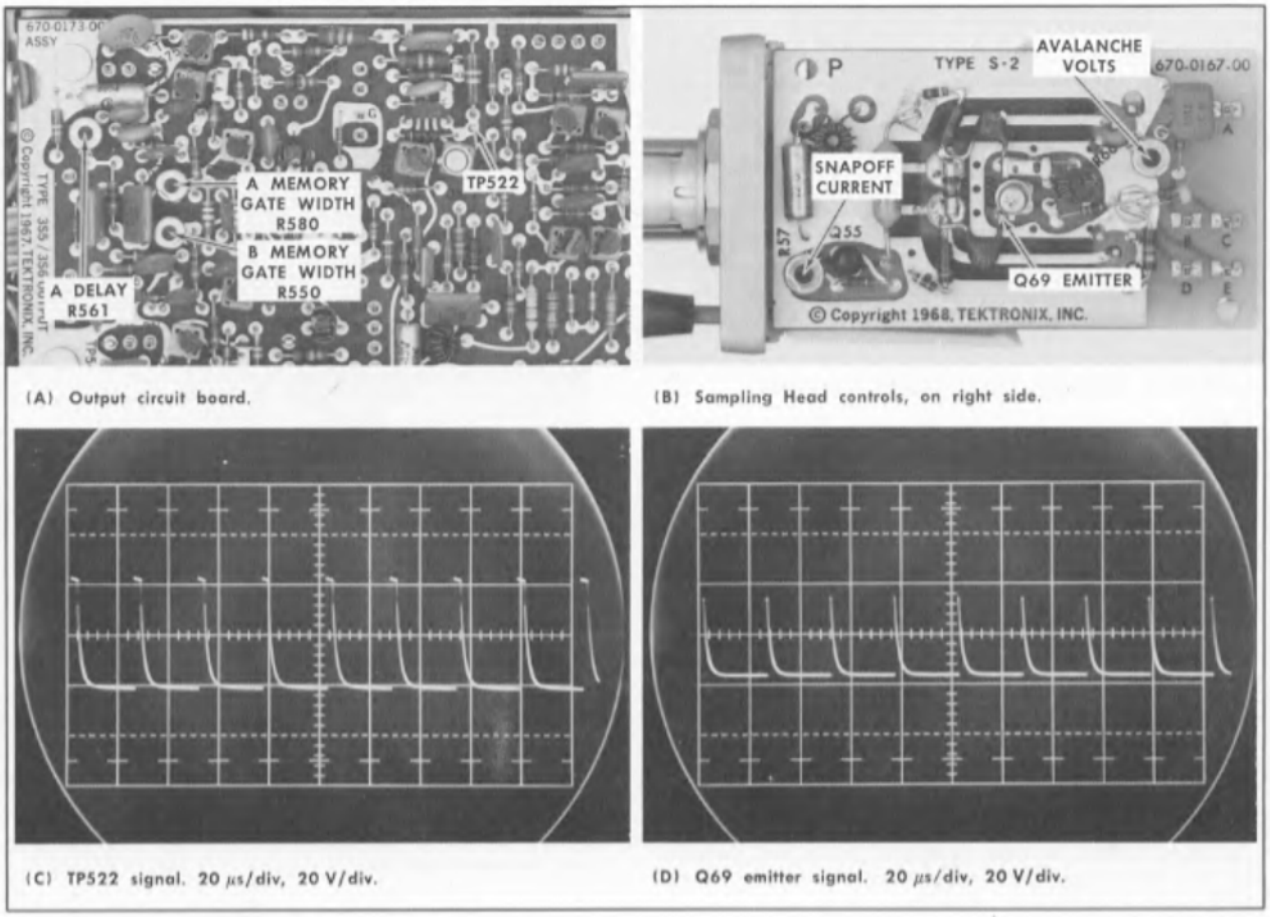
5. Adjust Sampling Head Snap Off and Avalanche Volts Controls

NOTE

If the sampling head used in this procedure is operating properly, and there is no intent to calibrate the head, disregard this step. This step is to be used only when the sampling head also needs calibration.

a. Continue with the double-triggered display obtained in Step 4, and leave the test oscilloscope on Q215 base at R213.

b. Refer to Fig. 7-4B for control locations. Adjust the Snap Off Current control, R57. The test oscilloscope display amplitude will change. Adjust R57 for a test oscilloscope display near the maximum amplitude obtainable (near maximum loop gain). The final position of R57 is decided thus: Note that the Type 3S6 display moves up and down when turning R57; if a maximum vertical up or down excursion occurs near a point where the test oscilloscope display amplitude is maximum, leave R57 at the Type 3S6 maximum excursion point.



(A) Output circuit board.

(B) Sampling Head controls, on right side.

(C) TP522 signal. 20 μs/div, 20 V/div.

(D) Q69 emitter signal. 20 μs/div, 20 V/div.

Fig. 7-4. Gate Generator and Sampling Head Avalanche operation.

c. Move the test oscilloscope probe to the emitter of the sampling head avalanche transistor, Q69 (shown in Fig. 7-4B). Adjust the Avalanche Volts control, R66, slightly clockwise and note that the avalanche circuit operation becomes unstable. Return R66 about 1/8 turn counterclockwise from the point of instability.

d. Interaction between the two controls may require that the above two adjustments be repeated.

NOTE

Step 5 adjustments do not assure proper sampling noise and risetime calibration. Those adjustments are described in the sampling head instruction manual calibration procedure.

6. Adjust Sampling Head Bridge balance Controls

a. Disconnect the signal cable from the Type 284. Leave the cable connected to the sampling head. Leave the sampling sweep unit triggered from the Type 284 for a displayed no-signal trace.

b. Set both DC OFFSET controls for zero volts at TP663 and TP763.

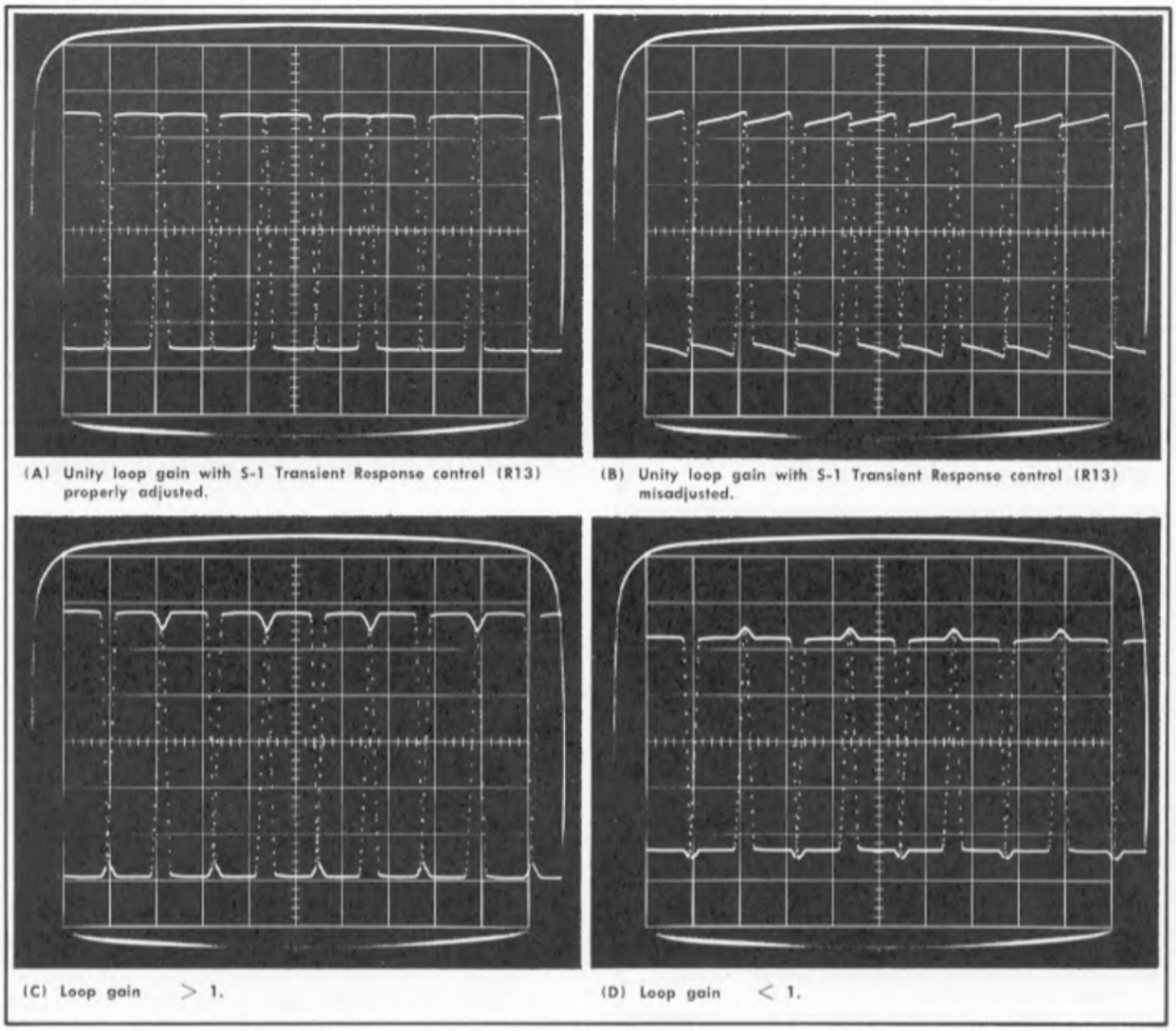
c. Change the UNITS/DIV switch from 200 to 2 and adjust Bridge Bal R22, (shown in Fig. 7-9) for no more than one division of trace movement as the switch is changed from 200 to 2.

7. Adjust Smoothing Balance Controls

a. Disconnect the cable from the Type 284. Leave the cable connected to the sampling head. Leave the sampling sweep triggered from the Type 284 for a displayed no-signal trace.

b. Set both Type 3S6 DC OFFSET controls to zero.

c. Turn the NORMAL-SMOOTH control to SMOOTH and note the trace shift. If the trace moves vertically, readjust the Channel B Smoothing Balance control R367, (shown in Fig. 7-10) until there is no trace movement as the NORMAL-SMOOTH control is switched between its two positions.



(A) Unity loop gain with S-1 Transient Response control (R13) properly adjusted.

(B) Unity loop gain with S-1 Transient Response control (R13) misadjusted.

(C) Loop gain > 1.

(D) Loop gain < 1.

Fig. 7-5. Type 3S6/S1 waveforms, 1 μs period square wave, sampling sweep double triggered at 500 ns/div.

d. Move the sampling head back to Channel A. (Turn oscilloscope power off if samping head cover was removed). Change the Type 3S6 Mode switch to CH A. Readjust the Channel A Smoothing Balance control R167, shown in Fig. 7-10, until there is no trace shift as the NORMAL-SMOOTH control is switched between its two positions.

8. Check Vertical Digital Accuracy (with Readout System)

Requirement—The Type 3S6 will permit a Tektronix digital readout system to make voltage measurement with an accuracy of ±2%. (±2.7% in set-up below.)

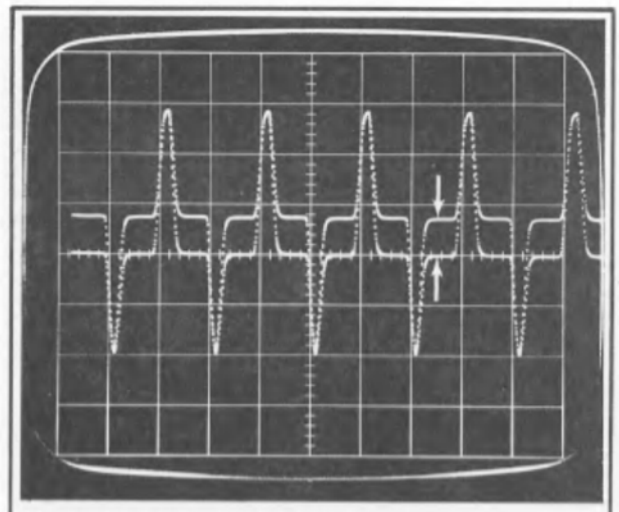
a. Connect the Type 284 Square Wave Output to the sampling head input through a 50 Ω coaxial cable. Set the Type 3S6 UNITS/DIV switches to 200 and check that the VARIABLE controls are at CAL. The input square wave amplitude is now 1.0 volts, ±0.5% when the sampling head input resistance is 50 Ω.

b. Set the Type 284 Period Switch for 10 μs square waves. Set the sampling sweep unit for a sweep rate of 2 μs/div.

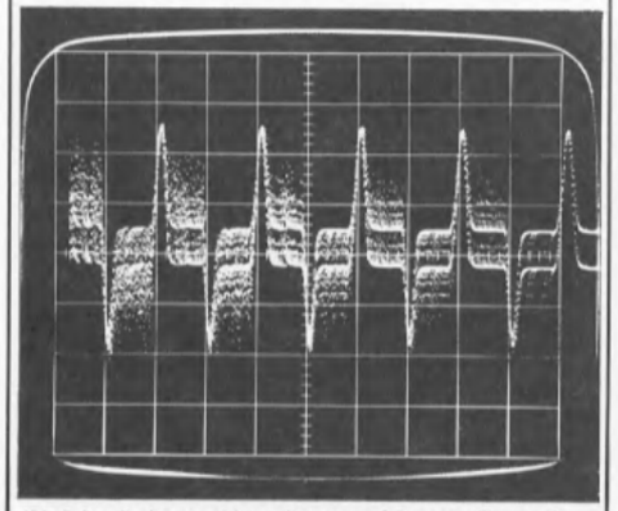
c. Set the digital unit controls to measure voltage from Channel A, along a rising slope waveform.

d. Check—Digital readout is between 0.973 V and 1.027 V.

e. Change the sampling head to Channel B and the Mode switch to CH B. Set the digital unit to read voltage from Channel B.



(A) Display with Type S-1 Sampling Head.



(B) False display requiring adjustment of Recovery Time and Trigger Sensitivity controls.

Fig. 7-6. Smoothed displays of 1 μs square wave, double triggered.

f. CHECK—Digital readout is between 0.973 V and 1.027 V. Refer to step 10 if not within tolerance.

9. Check Digital Intensified Zone Enable

NOTE

Disconnect the Type 3S6 plug-in extender and connect a flexible extension from the power (horizontal) connector only. (Turn power off before disconnecting an extension.)

a. Set the sampling sweep unit Time/Div to 100 ns (Decade to 7 and Multiplier to 1) and the Trigger Sensitivity control fully clockwise.

b. Set the Type 3S6 Mode switch to DUAL-TRACE.

c. Connect the 1× probe from the Type W Input A connector to TP445; see Fig. 7-12. Set the test oscilloscope sweep rate to 20 μs/div, and deflection factor to 1 V/div.

d. Check that the square wave levels above and below the zero volt reference line are ±0.7 V or more (at least 0.7 division above and below the zero reference line).

e. Disconnect the probe.

10. Adjust Digital Gain Controls ◐

NOTE

This step applies only if the Type 3S6 is used with a Type 230 Digital Unit and if R404 or R424 have been replaced or otherwise misadjusted. If this step does not apply, then DO NOT adjust R404 and R424 from the factory adjustment positions.

a. Turn off indicator oscilloscope power, remove the flexible interconnecting cable, re-install the Type 3S6 on the plug-in extender. Turn the instrument power on. Allow 5 minutes warmup time.

b. Remove any attenuator that is in the signal cable between the Type 284 and the sampling head input. The square wave amplitude is now 1.0 volt ±0.5% when the sampling head input resistance is 50 Ω. Set the Type 284 Period switch to deliver 10 μs square waves. Set both Type 3S6 UNITS/DIV switches to 200 and obtain a display similar to Fig. 7-11. Check that both VARIABLE controls are at CAL. Set the digital unit controls to measure voltage from Channel A, along a rising slope waveform. Set the sampling sweep unit for 2 μs/div.

c. Refer to Fig. 7-12 and locate the A Digital Gain control, R404. Adjust R404 until the digital unit reads 1.00 volt.

d. Move the sampling head to Channel B. (Turn oscilloscope power off if sampling head cover was removed.) Set the Type 3S6 Mode switch to CH B.

e. Locate the B Digital Gain control, R424. Change the digital unit to read voltage from Channel B. Adjust R424 until the digital unit reads 1.00 volt.

NOTE

Changing either Digital Gain control requires that the front panel GAIN control and the A-B Bal control be adjusted as described in step 12.

11. Check Deflection Factor Accuracies Over Range of Units/Div Switch and Variable Control Range

Requirement—All calibrated deflection factors will produce displays with amplitude accuracy of ±3% at NORMAL and ±4% at SMOOTH (when the VARIABLE control is at CAL). VARIABLE control increases display amplitude to 250% or more of calibrated amplitude.

a. Set the Type 3S6 UNITS/DIV switch to 200 and apply 1.2 volts from the 50 Ω Amplitude Calibrator (item 19, equipment required) to the Channel B input through a 50 Ω coaxial cable. Connect a coaxial cable from the Amplitude Calibrator Trigger Output connector to the sampling sweep unit External Trigger Input 50 Ω connector.

b. Set the sampling sweep unit for a sweep rate of 10 μs/div and obtain a stable triggered display.

c. Adjust the front panel GAIN control for a display amplitude of 6 divisions.

d. Check all position of the UNITS/DIV switch as listed in Table 7-2 for a 6 division display amplitude within a tolerance of ±0.18 div. Also check with the NORMAL-SMOOTH switch at SMOOTH within a tolerance of ±0.24 div.

TABLE 7-2

Units/Div	50 Ω Amplitude Calibrator
200	1.2 V
100	.6 V
50	.3 V
20	.12 V
10	.06 V
5	.03 V
2	.012 V

NOTE

Record deflection in each case. If one range is above tolerance, GAIN can be reduced to bring all ranges within tolerance without need for checking the attenuator circuits.

e. Set the UNITS/DIV switch to 200 and the 50 Ω Amplitude Calibrator to 0.6 volts. Display amplitude is 3 divisions.

f. Turn the VARIABLE control fully clockwise from the detent setting and check the display amplitude for 7.5 divisions or more.

g. Return the VARIABLE control to the detent (CAL position.

h. Change the sampling head to Channel A and the Mode switch to CH A. Repeat the check for Channel A.

12. Adjust GAIN and A-B Bal Controls

a. Move the sampling head to Channel B.

b. Connect the cable between the Type 284 and the sampling head input. Set the sampling sweep unit for a sweep rate of 0.5 μs/div (500 ns; Decade at 7, Multiplier at 5.) Set the Type 284 to deliver 10 μs square waves at 1.0 volt. Obtain a display similar to Fig. 7-11, normally triggered (not double triggered).

c. Adjust the front panel GAIN control for a 5 division display.

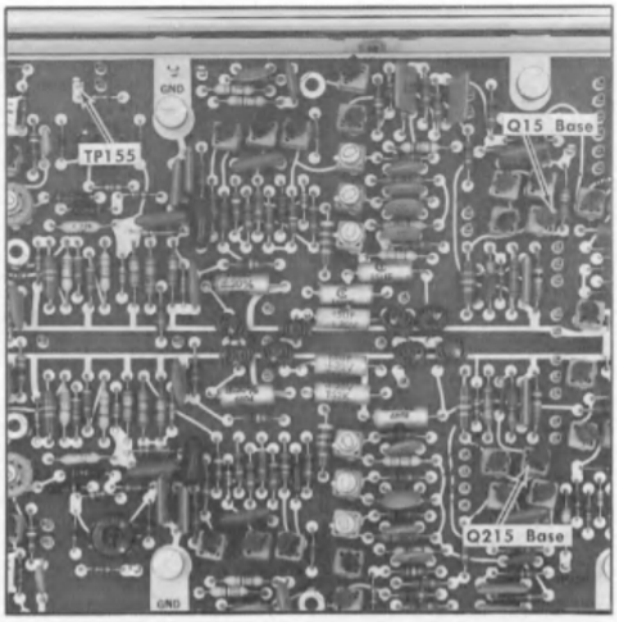


Fig. 7-7. Type 3S6 test points for adjustment of Memory Gate Width controls.

d. Disconnect the signal cable. Connect the bench multimeter between chassis and TP390. Set the B DC OFFSET control for zero volts on the meter.

e. Connect a second, calibrated head to Channel A and connect the signal cable to the Channel A sampling head input.

f. Set the Type 3S6 Mode switch to A+B and check for a 5 division display.

g. If the display amplitude is not 5 divisions, refer to Fig. 7-12 for location of the A-B Bal control, R430, and adjust R430 for a 5 division display.

13. Check DC Offset (Ext Prog and Front Panel Control)

Requirement—EXT PROG, range of —995 mV to +995 mV in 5 mV steps; accuracy within 2% of the programmed value, or 5 mV, whichever is greater.

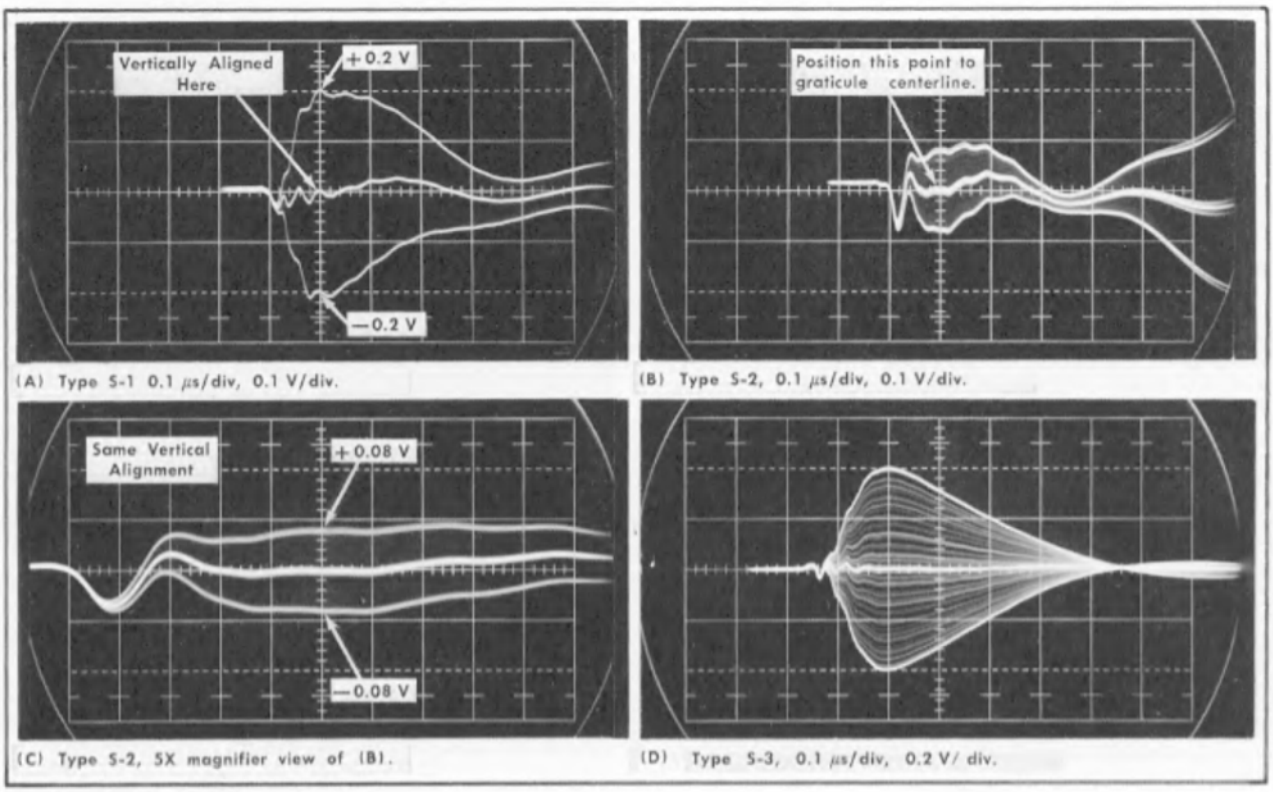
Front panel DC OFFSET control, range of +1 V to —1 V accuracy within 10 mV of same offset voltage in EXT PROG mode.

a. Connect the 1× probe from the Type W Input A to TP663. Set the Type W Input Atten to R = infinity.

b. Set the sampling sweep unit Trigger Sensitivity control fully counterclockwise.

c. Set the Mode switch to EXT PROG and externally program —995 mV of A Offset. Refer to Table 7-3 for Channel A DC Offset.

d. With the Type W Comparison Voltage, check that TP663 voltage is —995 mV ±2% (±19.9 mV).



(A) Type S-1 0.1 μs/div, 0.1 V/div.

(B) Type S-2, 0.1 μs/div, 0.1 V/div.

(C) Type S-2, 5X magnifier view of (B).

(D) Type S-3, 0.1 μs/div, 0.2 V/ div.

Fig. 7-8. Test oscilloscope displays of sampling head output signals at Q15 (Q215) base at R13 (R213), step 4, unity dot response.

e. Set the Mode switch to CH A and the DC OFFSET control to −995 mV (black numbers).

f. Check that the TP663 voltage is within 10 mV of the voltage measured in part d.

g. Repeat the comparisons for setting at 0 mV, +660 mV, and +995 mV. Tolerance at 0 mV is 5 mV. Set the Mode switch to EXT PROG and externally program B Offset −995 mV. Refer to Table 7-3 for Channel B DC Offset.

h. Connect the 1× probe from the Type W Input A to TP763.

i. Check with Type W Comparison Voltage that TP763 voltage is −995 mV ±2% (±19.9 mV).

j. Set the Mode switch to CH B and the DC OFFSET control to −995 mV (black numbers).

k. Check that TP763 voltage is within 10 mV of the voltage measured in part j.

l. Repeat the comparisons for settings at 0 mV, +660 mV and +995 mV. Tolerance at 0 mV is 5 mV. See Calibration step 20 if not within tolerance.

m. Connect the 50 Ω Amplitude Calibrator to the sampling head input connector, set the Volts switch to .6, aand set the Type 3S6 Mode switch to EXT PROG.

n. Externally program 10 UNITS/DIV and 0 mV offset. Refer to Tables 7-3 and 7-4. Set the sampling sweep unit sweep rate for 2 μs/div, obtain a display and note the position of the trace on the indicator oscilloscope.

TABLE 7-3

External Program DC Offset

DC Offset	Channel A		Channel B	
	Pin Number[1]	Logic State	Pin Number[1]	Logic State
+Polarity	4	1	H	1
−Polarity	4	0	H	0
800 mV	5		J	
400 mV	6		K	
200 mV	7		L	
100 mV	8		M	
80 mV	9		N	
40 mV	10		P	
20 mV	11		R	
10 mV	12		S	
5 mV	13		14	

[1]J214 of Type 568.

The logic state 1 is 0 to +2 V (True) and logic state 0 is +6 to +15 V (False) or an open circuit.

o. Externally program 660 mV, Table 7-3, and note the new position of the trace.

p. Check that new position is within 1.2 div, ÷12 mV (±2% of 600 mV) of the first position.

q. Repeat the check for the other channel.

TABLE 7-4

External Program Units/Div

UNITS/DIV	Channel A Pin Number[2] 1 2 3 Logic State	Channel B Pin Number[2] D E F Logic State
200	0 0 0	0 0 0
100	0 0 1	0 0 1
50	0 1 0	0 1 0
20	0 1 1	0 1 1
10	1 0 1	1 0 1
5	1 1 0	1 1 0
2	1 1 1	1 1 1

[2]J214 of Type 568.

Negative Logic; True (Logical 1): 0 to 2 V; False (Logical 0): +6 to 15 V or open circuit.

14. Check Position Indicators and Adjust Centering Control

Requirement—Up position indicator neon lights, and down position indicator neon is dark, when CRT beam is above the graticule. Down position indicator lights and up position indicator is dark when CRT beam is below the graticule.

a. Set the sampling sweep unit triggering controls for a free-running trace and the Type 3S6 A DC OFFSET control to place the trace above the top graticule line.

b. Check that the up indicator is on and the down indicator is off.

c. Offset the trace below the bottom graticule line.

d. Check that the down indicator is on and the up indicator is off.

e. Set the DC OFFSET control for zero volts offset. Terminate the sampling head input (Types S-1 or S-2) with 50 Ω or a 50 Ω coaxial cable (no signal input). (Types S-3, leave probe tip unconnected.)

f. Adjust the front panel CENTERING control to place the free run trace at the graticule centerline.

NOTE

The Type 230 may not give valid amplitude readout if the no-signal zero-offset trace position is more than ½ major division away from the graticule centerline.

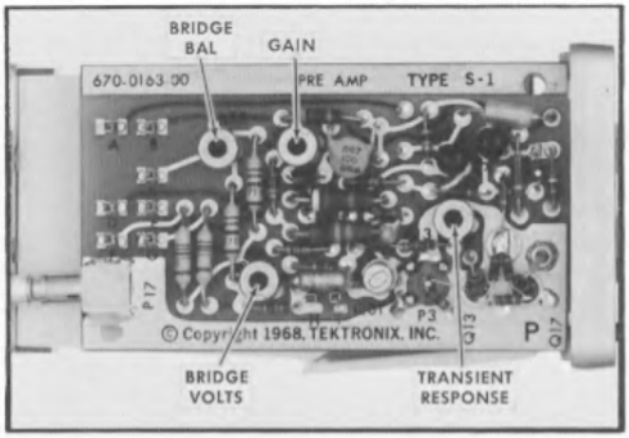


Fig. 7-9. Sampling Head left side control locations.

15. Adjust Loop Gain Using Normalizer Head ◐ Calibration Fixture

NOTE

Steps 15 and 16 (parts a through d) accomplish the proper Loop Gain (200, 100, 50, 20) capacitor adjustment. Step 15 uses a special Tektronix calibration fixture (item 16 of equipment required), and Step 16 uses a Type S-1 or S-2 Sampling Head. Both steps are included in this procedure to allow the Type 3S6 to be adjusted when a Normalizer is used, and Step 16 parts a through d, can be disregarded.

a. Connect the Normalizer Head to Channel B and set the UNITS/DIV switch to 100.

b. Free run the sampling sweep unit. Use a sweep rate that produces a continuous double trace display.

c. Set the NORMAL-SMOOTH switch to NORMAL. Use the DC OFFSET control so the sampling display is two traces, several divisions apart.

d. Connect the test oscilloscope 10× probe to TP390 (or TP190 for Channel A), see Fig. 7-10. Free run the test oscilloscope, sweep rate of 1 ms/div and vertical deflection factor of 1.0 V/div (including the probe 10× attenuation).

e. Set the DOT RESPONSE control fully clockwise, and note either the indicator or test oscilloscope display. Record the number of divisions of trace separation. Set the DOT RESPONSE control fully counterclockwise. Record the number of divisions of trace separation. Calculate the number of divisions by which the two traces should be separated when the DOT RESPONSE control is at its electrical midrange setting. Set the DOT RESPONSE control to its electrical midpoint as calculated.

f. Adjust the Loop Gain (200, 100, 50, 20) capacitor C384 (C184 for Channel A) until the two indicator oscilloscope traces are exactly 5 major divisions apart. See Fig. 7-10 for capacitor location. The test oscilloscope display should indicate exactly 2.5 volts difference between the two traces

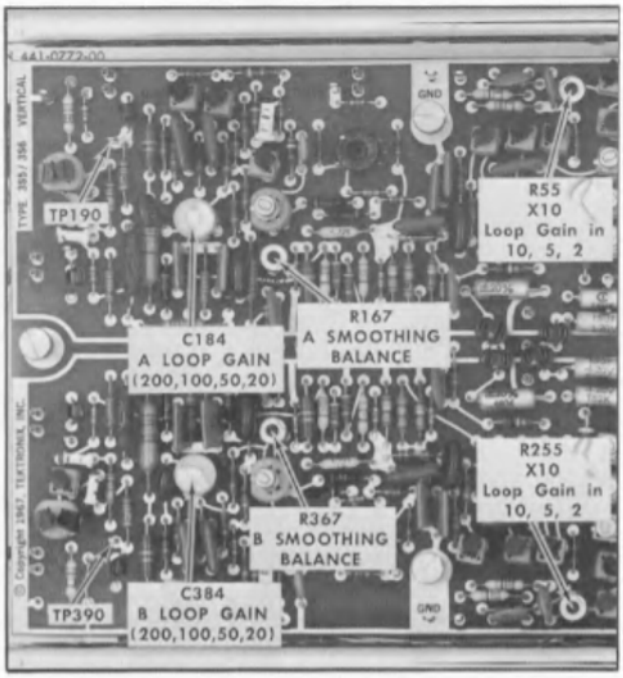


Fig. 7-10. Vertical circuit board control locations, left side.

(or square wave signal peak to peak value). The ±3% tolerance of both the test oscilloscope and indicator oscilloscope displays may show that they differ. This is of no consequence to the Type 3S6 calibration, because of the range of the DOT RESPONSE control. The real value of this adjustment is that if more than one Type 3S6 is calibrated in the same lab, they will all permit unity loop gain operation of any calibrated sampling head in any Type 3S6. This step or Step 16 (a through d) should be performed before attempting a sampling head calibration, particularly when adjusting the sampling head Preamplifier Gain control.

g. Repeat the above procedure for the other Type 3S6 channel.

16. Adjust Loop Gain ◐

NOTE

This step establishes the correct balance between the sampling head Preamplifier Gain control (R46 in Fig. 7-9) and the Type 3S6 Loop Gain (200, 100, 50, 20) controls C184 and C384. The procedure includes both the indicator oscilloscope and test oscilloscope displays.

a. Input signal amplitude to the sampling head must be the value stated earlier in Table 7-1. The test oscilloscope displays of the sampling head output signals (Fig. 7-8) are to be adjusted for ±0.2 volt when using a Type S-1, for ±0.08 volt when using a Type S-2, and for ±0.4 volt when using a Type S-3 (see Fig. 7-7D).

Set the Type 284 to deliver 1 μs square waves at 1.0 volt. Install the correct 50 Ω attenuator in the signal cable at the Type 284 output connector. Set the sampling sweep rate to 500 ns/div (0.5 μs/div). Set both Type 3S6 UNITS/DIV switches to 100.

b. Obtain a double-triggered display on the indicator oscilloscope by free running the samping sweep unit and adjusting the Recovery Time control. The display should be similar to any one in Fig. 7-5.

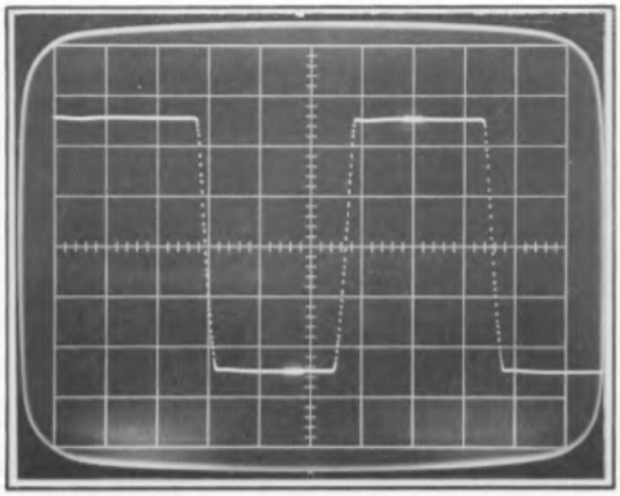


Fig. 7-11. Typical display for checking Vertical accuracy, 10 μs square wave at 2 μs/div.

Turn the Type 3S6 DOT RESPONSE control through its range. The double-triggered display amplitude should change over the control range in a manner similar to the triple exposure of Fig. 7-13. Set the DOT RESPONSE control to its electrical mid-point, not necessarily to unity loop gain.

c. Connect the test oscilloscope 10× probe to Q15 base (or Q215 base for Channel B) shown in Fig. 7-7.

CAUTION

Be very careful not to cause the probe tip to short between Q15 base and emitter leads, or the sampling head circuits may be damaged.

Externally trigger the test oscilloscope from TP155, using a sweep rate of 0.1 μs/div and vertical deflection factor of 0.1 V/div (including the probe 10× attenuation). (0.2 V/div when using a Type S-3.)

d. Decide whether the sampling display loop gain is greater or less than unity. Also note carefully the test oscilloscope display amplitude.

If the sampling head output signal is greater than that stated in part a at the beginning of this step, and at the same time the sampling display shows greater than unity loop gain, adjust the Type 3S6 Loop Gain control, C184 (C384 for Channel B), for unity loop gain. See Fig. 7-10 for locations.

If the sampling head output signal on the test oscilloscope is still greater than required, reduce the sampling head Preamplifier Gain (R46 shown in Fig. 7-9) a small amount, but not all the way to unity loop gain. Return the loop to unity gain with the Loop Gain capacitor.

If the sampling head output signal is less than required when the indicator oscilloscope displays unity loop gain, increase the sampling head Preamplifier Gain a small amount. Return the loop to unity gain with the Loop Gain capacitor.

Through such interacting adjustments, set the system loop gain to unity while the test oscilloscope reveals that the sampling head output signal is the correct amplitude listed in part a of this step.

e. Set the Type 284 Square Wave Amplitude switch to 100 mV. (Do not remove the attenuator). Set the Type 3S6 UNITS/DIV switch to 10.

f. If the indicator oscilloscope display is not unity loop gain, adjust ×10 Loop Gain (in 10, 5, 2) control, R55 (R255 for Channel B), for unity loop gain.

g. Repeat the above procedure for the other channel.

17. Check Interchannel Delay Range

Requirement—B DELAY control range is at least 10 ns.

a. Only one sampling head should be used, changing it from one channel to the other as necessary.

b. Connect the Type 284 fast pulse output to the Channel A sampling head input connector. Externally trigger the sampling sweep unit from the Type 284 Trigger Output connector. Set the sampling sweep rate to 2 ns/div. Set the Type 3S6 Mode switch to CH A.

c. Obtain a step display of the signal fed to Channel A. Adjust the sampling sweep unit Delay and Horiz Pos controls so the center of the rise passes through the center of the graticule.

d. Change the Mode switch to CH B, move sampling head to Channel B and apply the Type 284 fast pulse to the Channel B input connector.

e. Set the Type 3S6 B DELAY control fully counterclockwise and note the position of the step 50% amplitude point. It should be 2.5 divisions or more to the left of the graticule center (at least 5 ns to the left of center).

f. Turn the B DELAY control fully clockwise and check that the Channel B 50% amplitude point is to the right of the center graticule line, for a total range of at least 10 ns.

18. Adjust Type 3S6 A Delay Control ◐

a. Connect the Type 284 fast pulse output to the Channel B Sampling Head input connector. Set the sampling sweep unit to 2 ns/div. Set the Type 3S6 Mode switch to DUAL-TRACE.

b. Obtain a step display of the signal fed to Channel B. Set the B DELAY control fully counterclockwise and use the sampling sweep unit Time Position controls to move the step so the center of its rise passes to the left of the graticule 2.5 div point; see point no. 1, Fig. 7-14.

c. Turn the B DELAY control fully clockwise. The step display should now be to the right of the graticule 7.5 div point; see point no. 2, Fig. 7-14. Adjust the sampling sweep unit Time Position controls so the two points (no. 1 and no. 2 of Fig. 7-14) fall equal distances on the left and right of the graticule centerline.

d. Move the sampling head to Channel A with the signal cable. The step display should now be at the graticule centerline: see Fig. 7-14, point no. 3. If not, adjust the A DELAY control, R561 shown in Fig. 7-7, so that the step display half-amplitude point does cross at the graticule centerline.

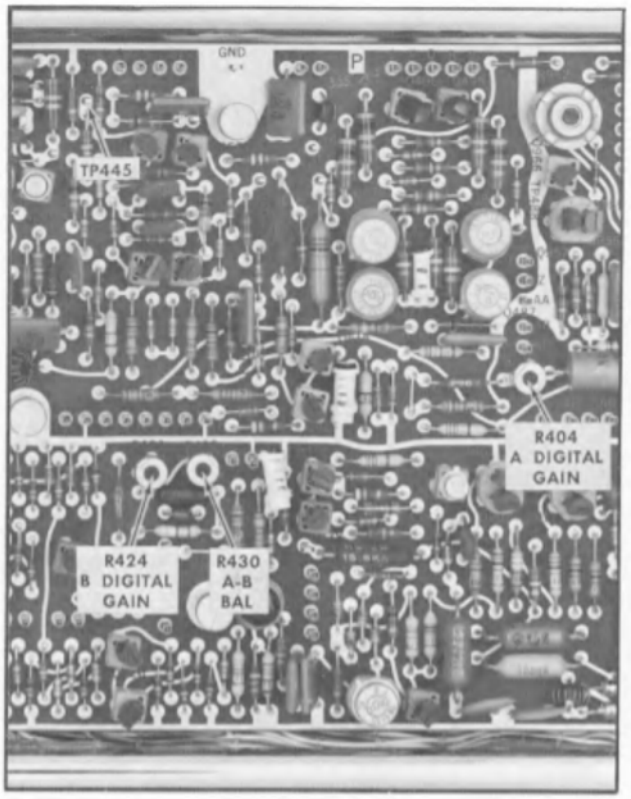


Fig. 7-12. Location of controls on Output circuit board, right side of instrument.

19. Check Memory Slash

Requirement—Vertical dot drift is ≤0.1 division when sampling sweep unit is triggered at 20 Hz.

a. Set the test oscilloscope Time/div to 5 ms/div, Triggering Mode to Auto and Level control fully clockwise.

b. Connect a BNC to banana patch cord from the +GATE jack to the sampling sweep unit External Trigger input connector through a 10 kΩ resistor.

c. Set the sampling sweep unit Trigger Sensitivity control fully clockwise, Time/Div to 500 ns (Decade to 7, Multiplier to 5) and adjust the indicator oscilloscope Focus and Astigmatism controls for the sharpest dot.

d. Turn the sampling sweep unit Trigger Mode switch to Ext Auto and observe the dot as it crosses the CRT.

e. Check that the vertical elongation of a displayed dot is 0.1 div or less.

f. Set the sampling sweep unit Trigger Mode to Ext.

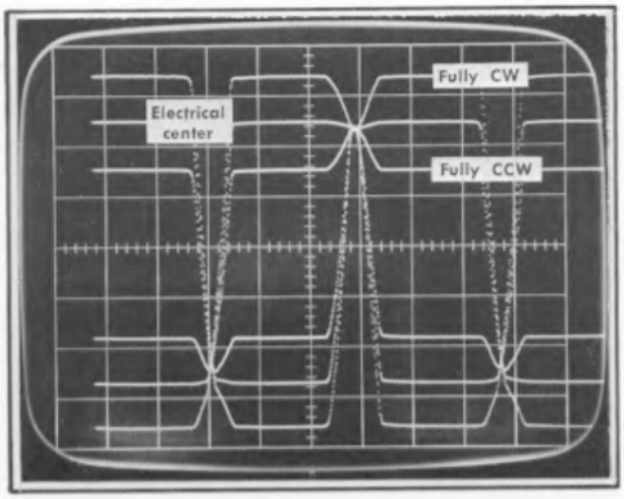


Fig. 7-13. Finding electrical center of Type 356 DOT RESPONSE control. Triple exposure; double triggered; 1 μs square wave; 200 ns/div; 100 mV/div.

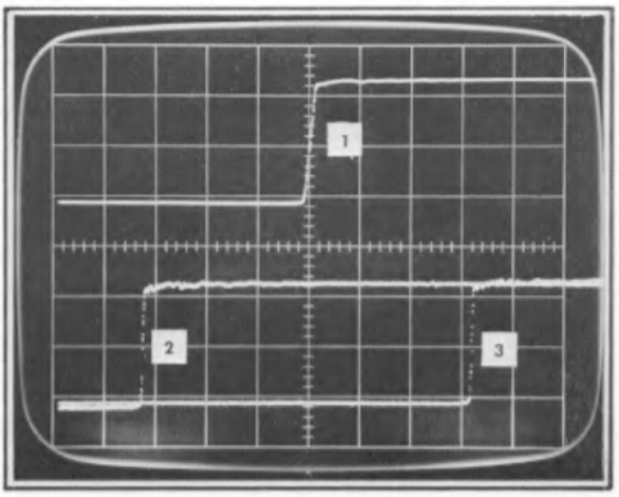


Fig. 7-14. Waveforms for steps 17 and 18, B DELAY control range.

20. Adjust Offset Cal and Offset Zero

a. Connect the 1× probe from the Type W Input to TP663 (Channel A). Set the Type W Input Selector to Ground and the Vc Range to 0. Position the test oscilloscope trace at the centerline and set the Comparison Voltage to 995.

b. Set the Type 356 A DC OFFSET control to +995 mV (black numbers). Set the Type W Input Selector to DC and the Vc Range switch to —1.1.

c. Check that the test oscilloscope trace is at the centerline, —995 mV at TP663. If trace is not at the centerline, adjust the A Offset Cal control, R638 shown in Fig. 7-15, for —995 mV, trace at test oscilloscope centerline.

d. Change the A DC OFFSET control to 0, set the Type W Vc Range switch to 0, and Comparison Voltage to 000.

e. Check that the test oscilloscope trace is at the graticule centerline, 0 mV at TP663. If not 0 mV, adjust the A Offset Zero control, R649, for 0 mV, trace at test oscilloscope centerline.

f. Repeat the check and/or adjustment for the B Channel, using TP763. Control locations are shown in Fig. 7-15.

g. Disconnect the probe.

21. Adjust Attenuator Zero

a. With the Offset circuit card on the extender, set both UNITS/DIV switches to 200 and the Mode switch to CH B.

b. Adjust the B DC OFFSET control for zero volts at TP390 as measured with the bench multimeter.

c. Connect Pin 21 of the Offset circuit card interconnector to ground using a patch cord with insulated alligator clips.

d. Connect the 1× probe from the Type W Input A to the base of Q281B.

e. Change the B UNITS/DIV switch to 2 and check that the test oscilloscope display shows not more than 4 mV, of change.

f. If the voltage change is more than 4 mV, adjust R286, the B Attenuator Zero control, for not more than 4 mV of change as the UNITS/DIV switch is changed from 200 to 2.

NOTE

Do not ground Pin 21 (or Pin 8) longer than necessary to make the adjustment.

g. Disconnect the patch cord Probe and meter lead, and move the sampling head to Channel A. Set the Mode Switch to CH A.

h. Adjust the A DC OFFSET control for zero volts at TP190 as measured with bench multimeter.

i. Connect Pin 8, Offset circuit board interconnector, to ground with the patch cord.

j. Connect the 1× probe to the base of Q81B.

k. Change the A UNITS/DIV switch to 2 and check for not more than 4 mV change.

l. If the voltage change is more than 4 mV, adjust R86, A Attenuator Zero control, for not more than 4 mV of change as the UNITS/DIV switch is changed from 200 to 2.

m. Disconnect the ground patch cord, probe and meter leads.

n. Turn the power off, remove the Offset circuit card assembly from the extender, replace the Offset circuit card without the extender, and turn on the power.

22. Check Digital Control Logic with Normalizer Head

In all positions of the vertical mode switch with the exception of EXT PROG, the digital unit units-of-measure lamp goes out when the VARIABLE control is moved from the CAL position. The V units lamp lights with a voltage-indicating sampling head and the A units lamp lights[3] with a current-indicating sampling head.

Table 7-5 lists the Units and Decimal lamps to be lit with the Type 3S6 UNITS/DIV and Normalizer Units/Div Multiplier switch settings. X indicates the lighted decimal.

[3]Some Type 230 Units are not connected for operation of the A lamp. See your Field Engineer for modification instructions.

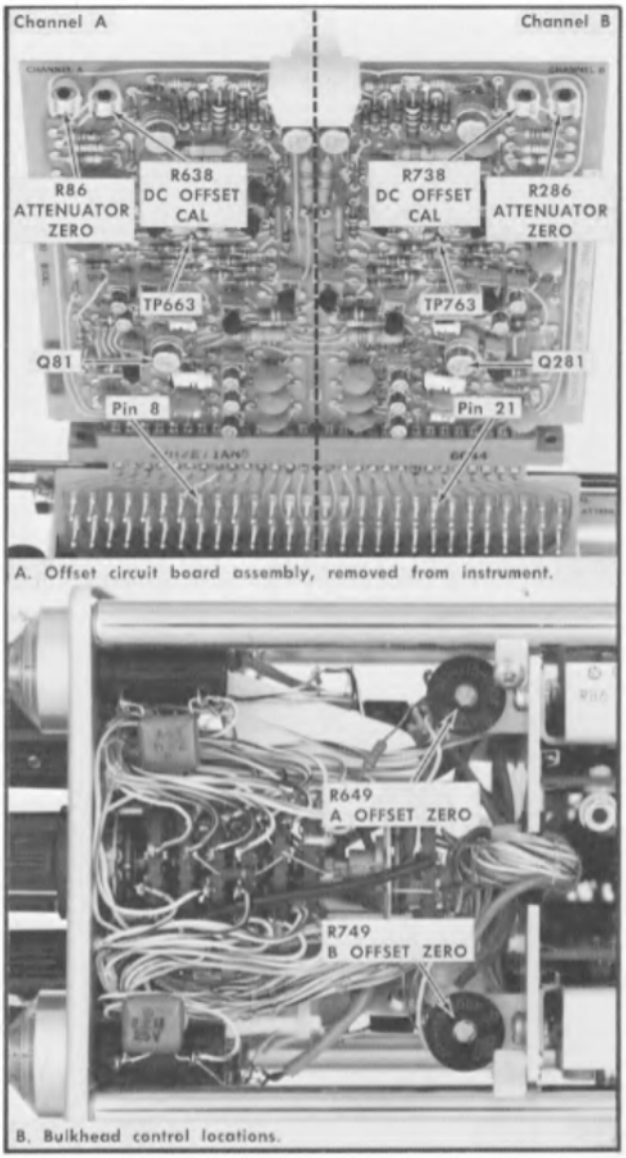


Fig. 7-15. Control locations, Type 3S6 top view.

TABLE 7-5

Units/Div Multipler	Type 3S6 UNITS/DIV	Decimal 1	2	3	4	5	Units Multiplier	÷ Output
×0.1	200	0	0	0	X	0	m	5
	100	0	0	0	X	0	m	1
	50	0	0	0	X	0	m	2
	20	0	0	X	0	0	m	5
	10	0	0	X	0	0	m	1
	5	0	0	X	0	0	m	2
	2	0	X	0	0	0	m	5
×1	200	0	X	0	0	0	none	5
	100	0	0	0	0	X	m	1
	50	0	0	0	0	X	m	2
	20	0	0	0	X	0	m	5
	10	0	0	0	X	0	m	1
	5	0	0	0	X	0	m	2
	2	0	0	X	0	0	m	5
×10	200	0	0	X	0	0	none	5
	100	0	0	X	0	0	none	1
	50	0	0	X	0	0	none	2
	20	0	X	0	0	0	none	5
	10	0	0	0	0	X	m	1
	5	0	0	0	0	X	m	2
	2	0	0	0	X	0	m	5

ABBREVIATIONS AND SYMBOLS

A or amp	amperes
AC or ac	alternating current
AF	audio frequency
α	alpha—common-base current amplification factor
AM	amplitude modulation
$\approx$	approximately equal to
β	beta—common-emitter current amplification factor
BHB	binding head brass
BHS	binding head steel
BNC	baby series "N" connector
$\times$	by or times
C	carbon
C	capacitance
cap.	capacitor
cer	ceramic
cm	centimeter
comp	composition
conn	connector
$\sim$	cycle
c/s or cps	cycles per second
CRT	cathode-ray tube
csk	countersunk
Δ	increment
dB	decibel
dBm	decibel referred to one milliwatt
DC or dc	direct current
DE	double end
°	degrees
°C	degrees Celsius (degrees centigrade)
°F	degrees Fahrenheit
°K	degrees Kelvin
dia	diameter
$\div$	divide by
div	division
EHF	extremely high frequency
elect.	electrolytic
EMC	electrolytic, metal cased
EMI	electromagnetic interference (see RFI)
EMT	electrolytic, metal tubular
ε	epsilon—2.71828 or % of error
$\geqslant$	equal to or greater than
$\leqslant$	equal to or less than
ext	external
F or f	farad
F & I	focus and intensity
FHB	flat head brass
FHS	flat head steel
Fil HB	fillister head brass
Fil HS	fillister head steel
FM	frequency modulation
ft	feet or foot
G	giga or 10^9
g	occeleration due to gravity
Ge	germanium
GHz	gigahertz
GMV	guaranteed minimum value
GR	General Radio
$>$	greater than
H or h	henry
h	height or high
hex.	hexagonal
HF	high frequency
HHB	hex head brass
HHS	hex head steel
HSB	hex socket brass
HSS	hex socket steel
HV	high voltage
Hz	hertz (cycles per second)
ID	inside diameter
IF	intermediate frequency
in.	inch or inches
incd	incandescent
∞	infinity
int	internal
$\int$	integral
k	kilohms or kilo (10^3)
k Ω	kilohm
kc	kilocycle
kHz	kilohertz
L	inductance
λ	lambda—wavelength
$\gg$	large compared with
$<$	less than
LF	low frequency
lg	length or long
LV	low voltage
M	mega or 10^6
m	milli or 10^{-3}
MΩ or meg	megohm
μ	micro or 10^{-6}
mc	megacycle
met.	metal
MHz	megahertz
mm	millimeter
ms	millisecond
—	minus
mtg hdw	mounting hardware
n	nano or 10^{-9}
no. or #	number
ns	nanosecond
OD	outside diameter
OHB	oval head brass
OHS	oval head steel
Ω	omega—ohms
ω	omega—angular frequency
p	pico or 10^{-12}
/	per
%	percent
PHB	pan head brass
ϕ	phi—phase angle
π	pi—3.1416
PHS	pan head steel
+	plus
$\pm$	plus or minus
PIV	peak inverse voltage
plstc	plastic
PMC	paper, metal cased
poly	polystyrene
prec	precision
PT	paper, tubular
PTM	paper or plastic, tubular, molded
pwr	power
Q	figure of merit
RC	resistance capacitance
RF	radio frequency
RFI	radio frequency interference (see EMI)
RHB	round head brass
ρ	rho—resistivity
RHS	round head steel
r/min or rpm	revolutions per minute
RMS	root mean square
s or sec.	second
SE	single end
Si	silicon
SN or S/N	serial number
$\ll$	small compared with
T	tera or 10^{12}
TC	temperature compensated
TD	tunnel diode
THB	truss head brass
θ	theta—angular phase displacement
thk	thick
THS	truss head steel
tub.	tubular
UHF	ultro high frequency
V	volt
VAC	volts, alternating current
var	variable
VDC	volts, direct current
VHF	very high frequency
VSWR	voltage standing wave ratio
W	watt
w	wide or width
w/	with
w/o	without
WW	wire-wound
xmfr	transformer

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number
*000-0000-00	Asterisk preceding Tektronix Part Number indicates manufactured by or for Tektronix, Inc., or reworked or checked components.
Use 000-0000-00	Part number indicated is direct replacement.
	Screwdriver adjustment.
	Control, adjustment or connector.

SECTION 8
ELECTRICAL PARTS LIST

Values are fixed unless marked Variable.

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Bulbs			
B498	150-0035-00			Neon A1D T2			
B499	150-0035-00			Neon A1D T2			
B999	150-0038-00			680 Lamp Assembly			
				Capacitors			
				Tolerance ±20% unless otherwise indicated.			
C11	283-0051-00			0.003 pF	Cer	100 V	5%
C12	283-0026-00			0.2 µF	Cer	25 V	
C16	283-0026-00			0.2 µF	Cer	25 V	
C20	283-0059-00			1 PF	Cer	25 V	+80%-20%
C25	283-0065-00			0.001 µF	Cer	100 V	5%
C31	283-0060-00			100 pF	Cer	200 V	5%
C32	283-0060-00			100 pF	Cer	200 V	5%
C33	283-0060-00			100 pF	Cer	200 V	5%
C34	283-0060-00			100 pF	Cer	200 V	5%
C45	283-0026-00			0.2 µF	Cer	25 V	
C47	283-0059-00			1 µF	Cer	25 V	+80%-20%
C48	283-0026-00			0.2 µF	Cer	25 V	
C54	283-0060-00			100 pF	Cer	200 V	5%
C55	283-0060-00			100 pF	Cer	200 V	5%
C150	283-0620-00			470 pF	Mica	300 V	1%
C151	283-0059-00			1 µF	Cer	25 V	+80%-20%
C160	283-0594-00			0.001 µF	Mica	100 V	1%
C161	283-0000-00			0.001 µF	Cer	500 V	
C174	281-0547-00			2.7 pF	Cer	500 V	10%
C180	283-0059-00			1 µF	Cer	25 V	+80%-20%
C183	283-0059-00			1 µF	Cer	25 V	+80%-20%
C184	281-0092-00			9-35 pF, Var	Cer		
C185	283-0600-00			43 pF	Cer	500 V	5%
C186	283-0026-00			0.2 µF	Cer	25 V	
C187	283-0026-00			0.2 µF	Cer	25 V	
C194	281-0619-00			1.2 pF	Cer	200 V	
C195	281-0611-00			2.7 pF	Cer	200 V	±0.25 pF
C211	283-0051-00			0.0033 pF	Cer	100 V	5%
C212	283-0026-00			0.2 µF	Cer	25 V	
C216	283-0026-00			0.2 µF	Cer	25 V	
C220	283-0059-00			1 µF	Cer	25 V	+80%-20%
C225	283-0065-00			0.001 µF	Cer	100 V	5%
C231	283-0060-00			100 pF	Cer	200 V	5%
C232	203-0060-00			100 pF	Cer	200 V	5%
C233	283-0060-00			100 pF	Cer	200 V	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION		
			Capacitors (cont)			
C234	283-0060-00		100 pF	Cer	200 V	5%
C245	283-0026-00		0.2 μF	Cer	25 V	
C247	283-0059-00		1 μF	Cer	25 V	+80%-20%
C248	283-0026-00		0.2 μF	Cer	25 V	
C254	283-0060-00		100 pF	Cer	200 V	5%
C255	283-0060-00		100 pF	Cer	200 V	5%
C350	283-0620-00		470 pF	Mica	300 V	1%
C351	283-0059-00		1 μF	Cer	25 V	+80%-20%
C360	283-0594-00		0.001 μF	Mica	100 V	1%
C361	283-0000-00		0.001 μF	Cer	500 V	
C374	281-0547-00		2.7 pF	Cer	500 V	10%
C380	283-0059-00		1 μF	Cer	25 V	+80%-20%
C383	283-0059-00		1 μF	Cer	25 V	+80%-20%
C384	281-0092-00		9-35 pF, Var	Cer		
C385	283-0600-00		43 pF	Cer	500 V	5%
C386	283-0026-00		0.2 μF	Cer	25 V	
C387	283-0026-00		0.2 μF	Cer	25 V	
C394	281-0619-00		1.2 pF	Cer	200 V	
C395	281-0611-00		2.7 pF	Cer	200 V	±0.25 pF
C413	281-0629-00		33 pF	Cer	600 V	5%
C433	281-0629-00		33 pF	Cer	600 V	5%
C442	283-0060-00		100 pF	Cer	200 V	5%
C450	283-0059-00		1 μF	Cer	25 V	+80%-20%
C453	283-0144-00		33 pF	Cer	500 V	2%
C455	283-0059-00		1 μF	Cer	25 V	+80%-20%
C457	283-0144-00		33 pF	Cer	500 V	2%
C480	283-0026-00		0.2 μF	Cer	25 V	
C482	281-0592-00		4.7 pF	Cer		±0.5 pF
C503	283-0032-00		470 pF	Cer	500 V	5%
C505	283-0113-00		56 pF	Cer	500 V	1%
C508	283-0059-00		1 μF	Cer	25 V	+80%-20%
C511	283-0108-00		220 pF	Cer	200 V	10%
C513	283-0084-00		270 pF	Cer	1000 V	5%
C516	290-0134-00		22 μF	Elect.	15 V	
C519	283-0094-00		27 pF	Cer	200 V	10%
C526	283-0004-00		0.02 μF	Cer	150 V	
C534	283-0032-00		470 pF	Cer	500 V	5%
C536	283-0094-00		27 pF	Cer	200 V	10%
C537	283-0032-00		470 pF	Cer	500 V	5%
C541	283-0103-00		180 pF	Cer	500 V	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Capacitors (cont)			
C543	283-0115-00			47 pF	Cer	200 V	5%
C545	283-0004-00			0.02 μF	Cer	150 V	
C547	283-0094-00			27 pF	Cer	200 V	10%
C548	281-0612-00			5.6 pF	Cer	200 V	±0.5 pF
C564	283-0032-00			470 pF	Cer	500 V	5%
C566	283-0094-00			27 pF	Cer	200 V	10%
C567	283-0032-00			470 pF	Cer	500 V	5%
C571	283-0103-00			180 pF	Cer	500 V	5%
C572	283-0115-00			47 pF	Cer	200 V	5%
C575	283-0004-00			0.02 μF	Cer	150 V	
C577	283-0094-00			27 pF	Cer	200 V	10%
C578	281-0612-00			5.6 pF	Cer	200 V	±0.5 pF
C647	283-0164-00			2.2 μF	Cer	25 V	
C747	283-0164-00			2.2 μF	Cer	25 V	
C903	283-0067-00			0.001 pF	Cer	200 V	10%
C912	283-0067-00			0.001 pF	Cer	200 V	10%
C916	283-0004-00			0.02 μF	Cer	150 V	
C919	283-0004-00			0.02 μF	Cer	150 V	
C921	290-0327-00			0.56 μF	Elect.	100 V	
C923	290-0327-00			0.56 μF	Elect.	100 V	
C925	290-0327-00			0.56 μF	Elect.	100 V	
C927	290-0327-00			0.56 μF	Elect.	100 V	
C931	290-0369-00			800 μF	Elect.	15 V	+75%-10%
C938	283-0059-00			1 μF	Cer	25 V	+80%-20%
C944	283-0134-00			0.47 pF	Cer	50 V	+80%-20%
C950	290-0317-00			1000 μF	Elect.	40 V	+100%-10%
C956	283-0059-00			1 μF	Cer	25 V	+80%-20%
C959	283-0026-00			0.2 μF	Cer	25 V	
C964	290-0158-00			50 μF	Elect.	25 V	+75%-15%
C972	283-0059-00			1 μF	Cer	25 V	+80%-20%
C973	283-0059-00			1 μF	Cer	25 V	+80%-20%
C974	283-0059-00			1 μF	Cer	25 V	+80%-20%
C975	290-0135-00			15 μF	Elect.	20 V	
C976	290-0135-00			15 μF	Elect.	20 V	
C980	290-0135-00			15 μF	Elect.	20 V	
C982	283-0026-00			0.2 μF	Cer	25 V	
C983	290-0135-00			15 μF	Elect.	20 V	
C985	283-0004-00			0.02 μF	Cer	150 V	
C986	283-0004-00			0.02 μF	Cer	150 V	
C988	283-0059-00			1 μF	Cer	25 V	+80%-20%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION
		Capacitors (cont)		
C989	290-0135-00			15 μF Elect. 20 V
C990	290-0135-00			15 μF Elect. 20 V
C991	290-0135-00			15 μF Elect. 20 V
C992	290-0135-00			15 μF Elect. 20 V
C993	290-0135-00			15 μF Elect. 20 V
C994	290-0135-00			15 μF Elect. 20 V
C996	283-0004-00			0.02 μF Cer 150 V
C997	283-0004-00			0.02 μF Cer 150 V
C998	283-0026-00			0.2 μF Cer 25 V
		Semiconductor Device, Diodes		
D3	*152-0185-00			Silicon Replaceable by 1N4152
D37	152-0141-02			Silicon 1N4152
D38	152-0149-00			Zener 1N961B 0.4 W, 10 V, 5%
D42	*152-0185-00			Silicon Replaceable by 1N4152
D51	*152-0185-00			Silicon Replaceable by 1N4152
D101	*152-0185-00			Silicon Replaceable by 1N4152
D110	*152-0185-00			Silicon Replaceable by 1N4152
D113	*152-0185-00			Silicon Replaceable by 1N4152
D121	*152-0185-00			Silicon Replaceable by 1N4152
D128	*152-0185-00			Silicon Replaceable by 1N4152
D129	*152-0185-00			Silicon Replaceable by 1N4152
D131	*152-0185-00			Silicon Replaceable by 1N4152
D136	*152-0185-00			Silicon Replaceable by 1N4152
D137	*152-0185-00			Silicon Replaceable by 1N4152
D139	*152-0185-00			Silicon Replaceable by 1N4152
D151	152-0195-00			Zener 1N751A 0.4 W, 5.1 V, 5%
D153	*152-0185-00			Silicon Replaceable by 1N4152
D154	*152-0185-00			Silicon Replaceable by 1N4152
D155	*152-0185-00			Silicon Replaceable by 1N4152
D156	*152-0185-00			Silicon Replaceable by 1N4152
D157	*152-0323-00			Silicon Tek Spec
D158	*152-0185-00			Silicon Replaceable by 1N4152
D159	*152-0323-00			Silicon Tek Spec
D163	*152-0185-00			Silicon Replaceable by 1N4152
D173	*152-0185-00			Silicon Replaceable by 1N4152
D176	*152-0185-00			Silicon Replaceable by 1N4152
D177	*152-0185-00			Silicon Replaceable by 1N4152
D187	*152-0323-00			Silicon Tek Spec
D188	*152-0323-00			Silicon Tek Spec
D190	*152-0185-00			Silicon Replaceable by 1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D195	*152-0185-00		Silicon	Replaceable by 1N4152
D237	152-0141-02		Silicon	1N4152
D238	152-0149-00		Zener	1N961B 0.4 W, 10 V, 5%
D242	*152-0185-00		Silicon	Replaceable by 1N4152
D251	*152-0185-00		Silicon	Replaceable by 1N4152
D301	*152-0185-00		Silicon	Replaceable by 1N4152
D310	*152-0185-00		Silicon	Replaceable by 1N4152
D313	*152-0185-00		Silicon	Replaceable by 1N4152
D321	*152-0185-00		Silicon	Replaceable by 1N4152
D328	*152-0185-00		Silicon	Replaceable by 1N4152
D329	*152-0185-00		Silicon	Replaceable by 1N4152
D331	*152-0185-00		Silicon	Replaceable by 1N4152
D336	*152-0185-00		Silicon	Replaceable by 1N4152
D337	*152-0185-00		Silicon	Replaceable by 1N4152
D339	*152-0185-00		Silicon	Replaceable by 1N4152
D351	152-0195-00		Zener	1N751A 0.4 W, 5.1 V, 5%
D353	*152-0185-00		Silicon	Replaceable by 1N4152
D354	*152-0185-00		Silicon	Replaceable by 1N4152
D355	*152-0185-00		Silicon	Replaceable by 1N4152
D356	*152-0185-00		Silicon	Replaceable by 1N4152
D357	*152-0323-00		Silicon	Tek Spec
D358	*152-0185-00		Silicon	Replaceable by 1N4152
D359	*152-0323-00		Silicon	Tek Spec
D363	*152-0185-00		Silicon	Replaceable by 1N4152
D373	*152-0185-00		Silicon	Replaceable by 1N4152
D376	*152-0185-00		Silicon	Replaceable by 1N4152
D377	*152-0185-00		Silicon	Replaceable by 1N4152
D387	*152-0323-00		Silicon	Tek Spec
D388	*152-0323-00		Silicon	Tek Spec
D390	*152-0185-00		Silicon	Replaceable by 1N4152
D395	*152-0185-00		Silicon	Replaceable by 1N4152
D405	152-0141-02		Silicon	1N4152
D406	152-0141-02		Silicon	1N4152
D414	152-0141-02		Silicon	1N4152
D416	*152-0185-00		Silicon	Replaceable by 1N4152
D417	152-0195-00		Zener	1N751A 0.4 W, 5.1 V, 5%
D418	*152-0185-00		Silicon	Replaceable by 1N4152
D425	152-0141-02		Silicon	1N4152
D426	152-0141-02		Silicon	1N4152
D434	152-0141-02		Silicon	1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D436	*152-0185-00		Silicon	Replaceable by 1N4152
D437	152-0195-00		Zener	1N751A 0.4 W, 5.1 V, 5%
D438	*152-0185-00		Silicon	Replaceable by 1N4152
D441	*152-0233-00		Silicon	Tek Spec
D443	*152-0185-00		Silicon	Replaceable by 1N4152
D444	*152-0185-00		Silicon	Replaceable by 1N4152
D448	*152-0185-00		Silicon	Replaceable by 1N4152
D450	*152-0185-00		Silicon	Replaceable by 1N4152
D451	152-0008-00		Germanium	
D455	*152-0185-00		Silicon	Replaceable by 1N4152
D458	152-0008-00		Germanium	
D461	*152-0185-00		Silicon	Replaceable by 1N4152
D462	*152-0185-00		Silicon	Replaceable by 1N4152
D466	*152-0185-00		Silicon	Replaceable by 1N4152
D467	*152-0185-00		Silicon	Replaceable by 1N4152
D479	*152-0185-00		Silicon	Replaceable by 1N4152
D480	152-0166-00		Zener	1N753A 0.4 W, 6.2 V, 5%
D489	*152-0185-00		Silicon	Replaceable by 1N4152
D492	*152-0185-00		Silicon	Replaceable by 1N4152
D493	*152-0185-00		Silicon	Replaceable by 1N4152
D502	*152-0185-00		Silicon	Replaceable by 1N4152
D506	*152-0185-00		Silicon	Replaceable by 1N4152
D519	*152-0233-00		Silicon	Tek Spec
D520	*152-0185-00		Silicon	Replaceable by 1N4152
D534	*152-0185-00		Silicon	Replaceable by 1N4152
D536	*152-0185-00		Silicon	Replaceable by 1N4152
D539	*152-0185-00		Silicon	Replaceable by 1N4152
D552	*152-0185-00		Silicon	Replaceable by 1N4152
D555	*152-0185-00		Silicon	Replaceable by 1N4152
D564	*152-0185-00		Silicon	Replaceable by 1N4152
D566	*152-0185-00		Silicon	Replaceable by 1N4152
D569	*152-0185-00		Silicon	Replaceable by 1N4152
D582	*152-0185-00		Silicon	Replaceable by 1N4152
D585	*152-0185-00		Silicon	Replaceable by 1N4152
D629	*152-0185-00		Silicon	Replaceable by 1N4152
D783	*152-0185-00		Silicon	Replaceable by 1N4152
D784	*152-0185-00		Silicon	Replaceable by 1N4152
D788	*152-0185-00		Silicon	Replaceable by 1N4152
D789	*152-0185-00		Silicon	Replaceable by 1N4152
D844	*152-0185-00		Silicon	Replaceable by 1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION	
				Semiconductor Device, Diodes (cont)	
D845	*152-0185-00			Silicon	Replaceable by 1N4152
D846	*152-0185-00			Silicon	Replaceable by 1N4152
D848	*152-0185-00			Silicon	Replaceable by 1N4152
D849	*152-0185-00			Silicon	Replaceable by 1N4152
D850	*152-0185-00			Silicon	Replaceable by 1N4152
D855	*152-0185-00			Silicon	Replaceable by 1N4152
D857	*152-0185-00			Silicon	Replaceable by 1N4152
D905	*152-0185-00			Silicon	Replaceable by 1N4152
D915	*152-0185-00			Silicon	Replaceable by 1N4152
D930A	*152-0333-00			Silicon	Tek Spec
D930B	*152-0333-00			Silicon	Tek Spec
D930C	*152-0333-00			Silicon	Tek Spec
D930D	*152-0333-00			Silicon	Tek Spec
D951	*152-0107-00			Silicon	Replacealbe by 1N647
D953	*152-0107-00			Silicon	Replaceable by 1N647
D955	152-0212-00			Zener	1N936 9 V, 5%, TC
				Connectors	
J31	131-0327-00			Receptacle, 30 contact, female	
J41	131-0327-00			Receptacle, 30 contact, female	
J600	131-0549-00			Receptacle, 56 pin, female	
J800	131-0549-00			Receptacle, 56 pin, female	
P11	131-0149-00			24 contact, male	
P12	131-0149-00			24 contact, male	
				Inductors	
L12	276-0581-00			Core 1 ferrite	
L195	*120-0402-00			Toroid, 3 turns single	
L197	*120-0402-00			Toroid, 3 turns single	
L212	276-0581-00			Core, ferrite	
L395	*120-0402-00			Toroid, 3 turns single	
L397	*120-0402-00			Toroid, 3 turns single	
L460	*120-0402-00			Toroid, 3 turns single	
L465	*120-0402-00			Toroid, 3 turns single	
L516	*120-0382-00			Toroid, 14 turns single	
L921	*120-0382-00			Toroid, 14 turns single	

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION	
				Inductors (cont)	
L923	*120-0382-00			Toroid, 14 turns single	
L925	*120-0382-00			Toroid, 14 turns single	
L927	*120-0382-00			Toroid, 14 turns single	
L975	*120-0382-00			Toroid, 14 turns single	
L976	*120-0382-00			Toroid, 14 turns single	
L980	*120-0382-00			Toroid, 14 turns single	
L983	*120-0382-00			Toroid, 14 turns single	
L989	*120-0382-00			Toroid, 14 turns single	
L990	*120-0382-00			Toroid, 14 turns single	
L991	*120-0382-00			Toroid, 14 turns single	
L992	*120-0382-00			Toroid, 14 turns single	
L993	*120-0382-00			Toroid, 14 turns single	
L994	*120-0382-00			Toroid, 14 turns single	
				Transistors	
Q6	151-0188-00			Silicon	2N3906
Q8	151-0188-00			Silicon	2N3906
Q15	*151-0192-00			Silicon	Replaceable by MPS-6521
Q16	151-0188-00			Silicon	2N3906
Q19	151-0190-00			Silicon	2N3904
Q22	151-0188-00			Silicon	2N3906
Q27	151-1021-00			Silicon	FET
Q28	151-1021-00			Silicon	FET
Q29	151-1021-00			Silicon	FET
Q35	151-0190-00			Silicon	2N3904
Q44	151-0188-00			Silicon	2N3906
Q49	151-0190-00			Silicon	2N3904
Q52	151-0188-00			Silicon	2N3906
Q53	151-0188-00			Silicon	2N3906
Q104	151-0188-00			Silicon	2N3906
Q109	151-0190-00			Silicon	2N3904
Q111	151-0190-00			Silicon	2N3904
Q126	151-0188-00			Silicon	2N3906
Q136	151-0188-00			Silicon	2N3906
Q162	151-1007-00			Silicon	Dual FET
Q174	151-0188-00			Silicon	2N3906
Q181	151-0190-00			Silicon	2N3904
Q182	151-0188-00			Silicon	2N3906
Q190	151-0188-00			Silicon	2N3906
Q192	151-0188-00			Silicon	2N3906

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION
		Transistors (cont)		
Q195	151-0190-00		Silicon	2N3904
Q206	151-0188-00		Silicon	2N3906
Q208	151-0188-00		Silicon	2N3906
Q215	*151-0192-00		Silicon	Replaceable by MPS-6521
Q216	151-0188-00		Silicon	2N3906
Q219	151-0190-00		Silicon	2N3904
Q222	151-0188-00		Silicon	2N3906
Q227	151-1021-00		Silicon	FET
Q228	151-1021-00		Silicon	FET
Q229	151-1021-00		Silicon	FET
Q235	151-0190-00		Silicon	2N3904
Q244	151-0188-00		Silicon	2N3906
Q249	151-0190-00		Silicon	2N3904
Q252	151-0188-00		Silicon	2N3906
Q253	151-0188-00		Silicon	2N3906
Q304	151-0188-00		Silicon	2N3906
Q309	151-0190-00		Silicon	2N3904
Q311	151-0190-00		Silicon	2N3904
Q326	151-0188-00		Silicon	2N3906
Q336	151-0188-00		Silicon	2N3906
Q362	151-1007-00		Silicon	Dual FET
Q374	151-0188-00		Silicon	2N3906
Q381	151-0190-00		Silicon	2N3904
Q382	151-0188-00		Silicon	2N3906
Q390	151-0188-00		Silicon	2N3906
Q392	151-0188-00		Silicon	2N3906
Q395	151-0190-00		Silicon	2N3904
Q413	151-0190-00		Silicon	2N3904
Q418	151-0188-00		Silicon	2N3906
Q433	151-0190-00		Silicon	2N3904
Q438	151-0188-00		Silicon	2N3906
Q450	151-0188-00		Silicon	2N3906
Q455	151-0188-00		Silicon	2N3906
Q461	151-0190-00		Silicon	2N3904
Q466	151-0190-00		Silicon	2N3904
Q477	*151-0150-00		Silicon	Selected from 2N3440
Q478	*151-0150-00		Silicon	Selected from 2N3440
Q487	*151-0150-00		Silicon	Selected from 2N3440
Q488	*151-0150-00		Silicon	Selected from 2N3440
Q495	151-0179-00		Silicon	2N3877A

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION
		Transistors (cont)		
Q496	151-0179-00			Silicon 2N3877A
Q503	151-0190-00			Silicon 2N3904
Q515	151-0190-00			Silicon 2N3904
Q522	*151-0133-00			Silicon Selected from 2N3251
Q538	151-0188-00			Silicon 2N3906
Q541	151-0190-00			Silicon 2N3904
Q555	151-0188-00			Silicon 2N3906
Q568	151-0188-00			Silicon 2N3906
Q571	151-0190-00			Silicon 2N3904
Q585	151-0188-00			Silicon 2N3906
Q784	151-0188-00			Silicon 2N3906
Q788	151-0188-00			Silicon 2N3906
Q789	151-0190-00			Silicon 2N3904
Q853	151-0190-00			Silicon 2N3904
Q855	*151-0150-00			Silicon Selected from 2N3440
Q857	*151-0150-00			Silicon Selected from 2N3440
Q901	151-0188-00			Silicon 2N3906
Q903	*151-0133-00			Silicon Selected from 2N3251
Q907	151-0188-00			Silicon 2N3906
Q911	151-0188-00			Silicon 2N3906
Q915	151-0190-00			Silicon 2N3904
Q936	*151-0216-00			Silicon Replaceable by MPS-6523
Q938	151-0260-00			Silicon 2N5189
Q944	*151-0228-00			Silicon Tek Spec
Q957	151-0188-00			Silicon 2N3906
Q959	151-0188-00			Silicon 2N3906
Q966	151-0188-00			Silicon 2N3906
Q969	*151-0148-00			Silicon Selected from 40250 (RCA)
		Resistors		
Resistors are fixed, composition, ±10% unless otherwise indicated.				
R3	317-0123-00	12 kΩ	1/8 W	5%
R4	317-0222-00	2.2 kΩ	1/8 W	5%
R5	317-0682-00	6.8 kΩ	1/8 W	5%
R7	315-0202-00	2 kΩ	1/4 W	5%
R9	311-0702-00	250 Ω, Var		
R10	317-0392-00	3.9 kΩ	1/8 W	5%
R11	321-0126-00	200 Ω	1/8 W Prec	1%
R13	321-0093-00	90.9 Ω	1/8 W Prec	1%
R14	301-0563-00	56 kΩ	1/2 W	5%
R15	321-0262-01	5.23 kΩ	1/8 W Prec	1%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION			
				Resistors (cont)			
R16	315-0101-00			100 Ω	1/4 W		5%
R17	315-0512-00			5.1 kΩ	1/4 W		5%
R18	315-0101-00			100 Ω	1/4 W		5%
R19	315-0123-00			12 kΩ	1/4 W		5%
R21	315-0153-00			15 kΩ	1/4 W		5%
R23	315-0101-00			100 Ω	1/4 W		5%
R24	321-0246-00			3.57 kΩ	1/8 W	Prec	1%
R26	321-0318-00			20.0 kΩ	1/8 W	Prec	1%
R27	321-0312-00			17.4 kΩ	1/8 W	Prec	1%
R28	321-0242-00			3.24 kΩ	1/8 W	Prec	1%
R29	321-0267-00			5.9 kΩ	1/8 W	Prec	1%
R31	315-0102-00			1 kΩ	1/4 W		5%
R32	315-0102-00			1 kΩ	1/4 W		5%
R33	315-0102-00			1 kΩ	1/4 W		5%
R34	315-0624-00			620 kΩ	1/4 W		5%
R35	301-0433-00			43 kΩ	1/2 W		5%
R37	315-0302-00			3 kΩ	1/4 W		5%
R39	315-0104-00			100 kΩ	1/4 W		5%
R42	315-0101-00			100 Ω	1/4 W		5%
R43	315-0752-00			7.5 kΩ	1/4 W		5%
R45	315-0101-00			100 Ω	1/4 W		5%
R46	315-0101-00			100 Ω	1/4 W		5%
R48	315-0101-00			100 Ω	1/4 W		5%
R49	315-0242-00			2.4 kΩ	1/4 W		5%
R51	315-0134-00			130 kΩ	1/4 W		5%
R53	315-0202-00			2 kΩ	1/4 W		5%
R55	311-0622-00			100 Ω, Var			
R56	315-0750-00			75 Ω	1/4 W		5%
R58	321-0210-00			1.5 kΩ	1/8 W	Prec	1%
R59	321-0210-00			1.5 kΩ	1/8 W	Prec	1%
R101	317-0184-00			180 kΩ	1/8 W		5%
R102	317-0203-00			20 kΩ	1/8 W		5%
R103	317-0104-00			100 kΩ	1/8 W		5%
R106	317-0564-00			560 kΩ	1/8 W		5%
R107	317-0473-00			47 kΩ	1/8 W		5%
R109	317-0364-00			360 kΩ	1/8 W		5%
R110	317-0105-00			1 MΩ	1/8 W		5%
R111	317-0364-00			360 kΩ	1/8 W		5%
R121	317-0184-00			180 kΩ	1/8 W		5%
R122	317-0203-00			20 kΩ	1/8 W		5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION			
				Resistors (cont)			
R123	317-0104-00			100 kΩ	1/8 W		5%
R126	317-0104-00			100 kΩ	1/8 W		5%
R128	317-0104-00			100 kΩ	1/8 W		5%
R131	317-0184-00			180 kΩ	1/8 W		5%
R132	317-0203-00			20 kΩ	1/8 W		5%
R133	317-0104-00			100 kΩ	1/8 W		5%
R136	317-0104-00			100 kΩ	1/8 W		5%
R137	317-0104-00			100 kΩ	1/8 W		5%
R139	317-0104-00			100 kΩ	1/8 W		5%
R150	315-0101-00			100 Ω	1/4 W		5%
R151	321-0253-00			4.33 kΩ	1/8 W	Prec	1%
R152	321-0242-00			3.24 kΩ	1/8 W	Prec	1%
R153	321-0231-00			2.49 kΩ	1/8 W	Prec	1%
R154	321-0231-00			2.49 kΩ	1/8 W	Prec	1%
R156	317-0102-00			1 kΩ	1/8 W		5%
R158	317-0102-00			1 kΩ	1/8 W		5%
R161	315-0392-00			3.9 kΩ	1/4 W		5%
R163	301-0513-00			51 kΩ	1/2 W		5%
R164	322-1389-01			111 kΩ	1/4 W	Prec	1/2%
R165	321-0304-00			14.3 kΩ	1/8 W	Prec	1%
R166	315-0471-00			470 Ω	1/4 W		5%
R167	311-0635-00			1 kΩ, Var			
R168	315-0471-00			470 Ω	1/4 W		5%
R169	321-0296-00			11.8 kΩ	1/8 W	Prec	1%
R171	315-0101-00			100 Ω	1/4 W		5%
R174	315-0102-00			1 kΩ	1/4 W		5%
R176	315-0241-00			240 Ω	1/4 W		5%
R177	301-0513-00			51 kΩ	1/2 W		5%
R178	315-0105-00			1 MΩ	1/4 W		5%
R179	315-0241-00			240 Ω	1/4 W		5%
R180	315-0101-00			100 Ω	1/4 W		5%
R181	315-0101-00			100 Ω	1/4 W		5%
R182	315-0101-00			100 Ω	1/4 W		5%
R183	315-0101-00			100 Ω	1/4 W		5%
R185	322-1389-01			111 kΩ	1/4 W	Prec	1/2%
R186	321-0283-00			8.66 kΩ	1/8 W	Prec	1%
R187	321-0292-00			10.7 kΩ	1/8 W	Prec	1%
R188	323-1389-01			111 kΩ	1/2 W	Prec	1/2%
R190	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R192	321-0303-00			14 kΩ	1/8 W	Prec	1%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Resistors (cont)			
R193	321-0409-00			178 kΩ	1/8 W	Prec	1%
R194	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R195	308-0320-00			15.6 kΩ	3 W	WW	
R207	315-0202-00			2 kΩ	1/4 W		5%
R209	311-0702-00			250 Ω, Var			
R210	317-0392-00			3.9 kΩ	1/8 W		5%
R211	321-0126-00			200 Ω	1/8 W	Prec	1%
R213	321-0093-00			90.9 Ω	1/8 W	Prec	1%
R214	301-0563-00			56 kΩ	1/2 W		5%
R215	321-0262-01			5.23 kΩ	1/8 W	Prec	1%
R216	315-0101-00			100 Ω	1/4 W		5%
R217	315-0512-00			5.1 kΩ	1/4 W		5%
R218	315-0101-00			100 Ω	1/4 W		5%
R219	315-0123-00			12 kΩ	1/4 W		5%
R221	315-0153-00			15 kΩ	1/4 W		5%
R223	315-0101-00			100 Ω	1/4 W		5%
R224	321-0246-00			3.57 kΩ	1/8 W	Prec	1%
R226	321-0318-00			20 kΩ	1/8 W	Prec	1%
R227	321-0312-00			17.4 kΩ	1/8 W	Prec	1%
R228	321-0242-00			3.24 kΩ	1/8 W	Prec	1%
R229	321-0267-00			5.9 kΩ	1/8 W	Prec	1%
R231	315-0102-00			1 kΩ	1/4 W		5%
R232	315-0102-00			1 kΩ	1/4 W		5%
R233	315-0102-00			1 kΩ	1/4 W		5%
R234	315-0624-00			620 kΩ	1/4 W		5%
R235	301-0433-00			43 kΩ	1/2 W		5%
R237	315-0302-00			3 kΩ	1/4 W		5%
R239	315-0104-00			100 kΩ	1/4 W		5%
R242	315-0101-00			100 Ω	1/4 W		5%
R243	315-0752-00			7.5 kΩ	1/4 W		5%
R245	315-0101-00			100 Ω	1/4 W		5%
R246	315-0101-00			100 Ω	1/4 W		5%
R248	315-0101-00			100 Ω	1/4 W		5%
R249	315-0242-00			2.4 kΩ	1/4 W		5%
R251	315-0134-00			130 kΩ	1/4 W		5%
R253	315-0202-00			2 kΩ	1/4 W		5%
R255	311-0622-00			100 Ω, Var			
R256	315-0750-00			75 Ω	1/4 W		5%
R258	321-0210-00			1.5 kΩ	1/8 W	Prec	1%
R259	321-0210-00			1.5 kΩ	1/8 W	Prec	1%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION		
				Resistors (cont)		
R301	317-0184-00			180 kΩ	1/8 W	5%
R302	317-0203-00			20 kΩ	1/8 W	5%
R303	317-0104-00			100 kΩ	1/8 W	5%
R306	317-0564-00			560 kΩ	1/8 W	5%
R307	317-0473-00			47 kΩ	1/8 W	5%
R309	317-0364-00			360 kΩ	1/8 W	5%
R310	317-0105-00			1 MΩ	1/8 W	5%
R311	317-0364-00			360 kΩ	1/8 W	5%
R321	317-0184-00			180 kΩ	1/8 W	5%
R322	317-0203-00			20 kΩ	1/8 W	5%
R323	317-0104-00			100 kΩ	1/8 W	5%
R326	317-0104-00			100 kΩ	1/8 W	5%
R328	317-0104-00			100 kΩ	1/8 W	5%
R331	317-0184-00			180 kΩ	1/8 W	5%
R332	317-0203-00			20 kΩ	1/8 W	5%
R333	317-0104-00			100 kΩ	1/8 W	5%
R336	317-0104-00			100 kΩ	1/8 W	5%
R337	317-0104-00			100 kΩ	1/8 W	5%
R339	317-0104-00			100 kΩ	1/8 W	5%
R350	315-0101-00			100 Ω	1/4 W	5%
R351	321-0253-00			4.22 kΩ	1/8 W Prec	1%
R352	321-0242-00			3.24 kΩ	1/8 W Prec	1%
R353	321-0231-00			2.49 kΩ	1/8 W Prec	1%
R354	321-0231-00			2.49 kΩ	1/8 W Prec	1%
R356	317-0102-00			1 kΩ	1/8 W	5%
R358	317-0102-00			1 kΩ	1/8 W	5%
R361	315-0392-00			3.9 kΩ	1/4 W	5%
R363	301-0513-00			51 kΩ	1/2 W	5%
R364	322-1389-01			111 kΩ	1/4 W Prec	1/2%
R365	321-0304-00			14.3 kΩ	1/8 W Prec	1%
R366	315-0471-00			470 Ω	1/4 W	5%
R367	311-0635-00			1 kΩ, Var		
R368	315-0471-00			470 Ω	1/4 W	5%
R369	321-0296-00			11.8 kΩ	1/8 W Prec	1%
R371	315-0101-00			100 Ω	1/4 W	5%
R374	315-0102-00			1 kΩ	1/4 W	5%
R376	315-0241-00			240 Ω	1/4 W	5%
R377	301-0513-00			51 kΩ	1/2 W	5%
R378	315-0105-00			1 MΩ	1/4 W	5%
R379	315-0241-00			240 Ω	1/4 W	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION			
				Resistors (cont)			
R380	315-0101-00			100 Ω	1/4 W		5%
R381	315-0101-00			100 Ω	1/4 W		5%
R382	315-0101-00			100 Ω	1/4 W		5%
R383	315-0101-00			100 Ω	1/4 W		5%
R385	322-1389-01			111 kΩ	1/4 W	Prec	1/2%
R386	321-0283-00			8.66 kΩ	1/8 W	Prec	1%
R387	321-0292-00			10.7 kΩ	1/8 W	Prec	1%
R388	323-1389-01			111 kΩ	1/2 W	Prec	1/2%
R390	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R392	321-0303-00			14 kΩ	1/8 W	Prec	1%
R393	321-0409-00			178 kΩ	1/8 W	Prec	1%
R394	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R395	308-0320-00			15.6 kΩ	3 W	WW	
R401	311-0701-00			5 kΩ, Var			
R404	311-0609-00			2 kΩ, Var			
R405	321-0185-00			825 Ω	1/8 W	Prec	1%
R407	321-0308-00			15.8 kΩ	1/8 W	Prec	1%
R408	321-0164-00			499 Ω	1/8 W	Prec	1%
R409	321-0314-00			18.2 kΩ	1/8 W	Prec	1%
R412	315-0124-00			120 kΩ	1/4 W		5%
R414	315-0432-00			4.3 kΩ	1/4 W		5%
R416	308-0320-00			15.6 kΩ	3 W	WW	1%
R417	321-0305-00			14.7 kΩ	1/8 W	Prec	1%
R419	315-0101-00			100 Ω	1/4 W		5%
R421	311-0701-00			5 kΩ, Var			
R424	311-0609-00			2 kΩ, Var			
R425	321-0185-00			825 Ω	1/8 W	Prec	1%
R427	321-0308-00			15.8 kΩ	1/8 W	Prec	1%
R428	321-0164-00			499 Ω	1/8 W	Prec	1%
R429	321-0314-00			18.2 kΩ	1/8 W	Prec	1%
R430	311-0609-00			2 kΩ, Var			
R431	321-0204-00			1.3 kΩ	1/8 W	Prec	1%
R432	315-0124-00			120 kΩ	1/4 W		5%
R434	315-0432-00			4.3 kΩ	1/4 W		5%
R436	308-0320-00			15.6 kΩ	3 W	WW	1%
R437	321-0305-00			14.7 kΩ	1/8 W	Prec	1%
R439	315-0101-00			100 Ω	1/4 W		5%
R441	315-0203-00			20 kΩ	1/4 W		5%
R445	315-0222-00			2.2 kΩ	1/4 W		5%
R446	315-0183-00			18 kΩ	1/4 W		5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Resistors (cont)			
R448	315-0103-00			10 kΩ	1/4 W		5%
R450	315-0101-00			100 Ω	1/4 W		5%
R451	315-0562-00			5.6 kΩ	1/4 W		5%
R452	315-0244-00			240 kΩ	1/4 W		5%
R453	315-0153-00			15 kΩ	1/4 W		5%
R455	315-0101-00			100 Ω	1/4 W		5%
R456	315-0244-00			240 kΩ	1/4 W		5%
R457	315-0153-00			15 kΩ	1/4 W		5%
R459	315-0562-00			5.6 kΩ	1/4 W		5%
R460	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R461	321-0248-00			3.74 kΩ	1/8 W	Prec	1%
R463	321-0278-00			7.68 kΩ	1/8 W	Prec	1%
R465	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R466	321-0248-00			3.74 kΩ	1/8 W	Prec	1%
R467	321-0237-00			2.87 kΩ	1/8 W	Prec	1%
R470	311-0608-00			2 kΩ, Var			
R472	311-0546-00			10 kΩ, Var			
R473	315-0333-00			33 kΩ	1/4 W		5%
R474	321-0317-00			19.6 kΩ	1/8 W	Prec	1%
R476	301-0303-00			30 kΩ	1/2 W		5%
R477	301-0303-00			30 kΩ	1/2 W		5%
R479	323-0402-00			150 kΩ	1/2 W	Prec	1%
R482	301-0164-00			160 kΩ	1/2 W		5%
R483	301-0164-00			160 kΩ	1/2 W		5%
R485	321-0284-00			8.87 kΩ	1/8 W	Prec	1%
R486	301-0303-00			30 kΩ	1/2 W		5%
R487	301-0303-00			30 kΩ	1/2 W		5%
R489	301-0164-00			160 kΩ	1/2 W		5%
R491	315-0304-00			300 kΩ	1/4 W		5%
R493	315-0304-00			300 kΩ	1/4 W		5%
R495	315-0624-00			620 kΩ	1/4 W		5%
R497	315-0106-00			10 MΩ	1/4 W		5%
R501	317-0511-00			510 Ω	1/8 W		5%
R503	315-0102-00			1 kΩ	1/4 W		5%
R505	315-0512-00			5.1 kΩ	1/4 W		5%
R508	315-0101-00			100 Ω	1/4 W		5%
R509	315-0222-00			2.2 kΩ	1/4 W		5%
R511	315-0512-00			5.1 kΩ	1/4 W		5%
R515	315-0241-00			240 Ω	1/4 W		5%
R518	315-0102-00			1 kΩ	1/4 W		5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION		
				Resistors (cont)		
R520	315-0363-00			36 kΩ	1/4 W	5%
R523	301-0153-00			15 kΩ	1/2 W	5%
R524	301-0153-00			15 kΩ	1/2 W	5%
R526	315-0471-00			470 Ω	1/4 W	5%
R528	315-0122-00			1.2 kΩ	1/4 W	5%
R530	317-0511-00			510 Ω	1/8 W	5%
R531	311-0310-00			5 kΩ, Var		
R532	315-0123-00			12 kΩ	1/4 W	5%
R535	315-0394-00			390 kΩ	1/4 W	5%
R536	315-0122-00			1.2 kΩ	1/4 W	5%
R537	315-0104-00			100 kΩ	1/4 W	5%
R538	315-0101-00			100 Ω	1/4 W	5%
R539	301-0563-00			56 kΩ	1/2 W	5%
R541	315-0472-00			4.7 kΩ	1/4 W	5%
R549	315-0432-00			4.3 kΩ	1/4 W	5%
R550	311-0607-00			10 kΩ, Var		
R551	315-0202-00			2 kΩ	1/4 W	5%
R553	315-0103-00			10 kΩ	1/4 W	5%
R557	315-0301-00			300 Ω	1/4 W	5%
R561	311-0633-00			5 kΩ, Var		
R562	315-0123-00			12 kΩ	1/4 W	5%
R565	315-0394-00			390 kΩ	1/4 W	5%
R566	315-0122-00			1.2 kΩ	1/4 W	5%
R567	315-0104-00			100 kΩ	1/4 W	5%
R568	315-0101-00			100 Ω	1/4 W	5%
R569	301-0563-00			56 kΩ	1/2 W	5%
R571	315-0472-00			4.7 kΩ	1/4 W	5%
R579	315-0432-00			4.3 kΩ	1/4 W	5%
R580	311-0607-00			10 kΩ, Var		
R581	315-0202-00			2 kΩ	1/4 W	5%
R583	315-0103-00			10 kΩ	1/4 W	5%
R587	315-0301-00			300 Ω	1/4 W	5%
R629	315-0222-00			2.2 kΩ	1/4 W	5%
R647	311-0838-00			10 kΩ, Var		
R648	321-0405-00			162 kΩ	1/8 W Prec	1%
R649	311-0115-00			100 kΩ, Var		
R747	311-0838-00			10 kΩ, Var		
R748	321-0405-00			162 kΩ	1/8 W Prec	1%
R749	311-0115-00			100 kΩ, Var		
R780	317-0105-00			1 MΩ	1/8 W	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION		
			Resistors (cont)			
R781	317-0563-00		56 kΩ	1/8 W		5%
R782	317-0124-00		120 kΩ	1/8 W		5%
R784	317-0123-00		12 kΩ	1/8 W		5%
R785	317-0105-00		1 MΩ	1/8 W		5%
R786	317-0563-00		56 kΩ	1/8 W		5%
R787	317-0124-00		120 kΩ	1/8 W		5%
R788	317-0123-00		12 kΩ	1/8 W		5%
R789	317-0273-00		27 kΩ	1/8 W		5%
R790	301-0122-00		1.2 kΩ	1/2 W		5%
R844	317-0303-00		30 kΩ	1/8 W		5%
R846	317-0224-00		220 kΩ	1/8 W		5%
R847	317-0303-00		30 kΩ	1/8 W		5%
R848	317-0303-00		30 kΩ	1/8 W		5%
R850	317-0303-00		30 kΩ	1/8 W		5%
R851	317-0224-00		220 kΩ	1/8 W		5%
R852	317-0473-00		47 kΩ	1/8 W		5%
R853	317-0303-00		30 kΩ	1/8 W		5%
R854	317-0303-00		30 kΩ	1/8 W		5%
R855	317-0103-00		10 kΩ	1/8 W		5%
R857	317-0103-00		10 kΩ	1/8 W		5%
R902	321-0603-00		15 kΩ	1/8 W	Prec	1/4%
R903	317-0102-00		1 kΩ	1/8 W		5%
R904	321-0406-00		165 kΩ	1/8 W	Prec	1%
R905	308-0253-00		1.32 kΩ	3 W	WW	1%
R906	308-0253-00		1.32 kΩ	3 W	WW	1%
R908	321-0603-00		15 kΩ	1/8 W	Prec	1/4%
R909	321-0692-00		49.9 kΩ	1/8 W	Prec	1/2%
R911	315-0114-00		110 kΩ	1/4 W		5%
R912	317-0102-00		1 kΩ	1/8 W		5%
R914	308-0421-00		3 kΩ	3 W	WW	5%
R915	308-0304-00		1.5 kΩ	3 W	WW	1%
R917	321-0761-03		35 kΩ	1/8 W	Prec	1/4%
R918	321-0755-03		65 kΩ	1/8 W	Prec	1/4%
R929	317-0510-00		51 Ω	1/8 W		5%
R930	317-0036-00		3.6 Ω	1/8 W		5%
R931	315-0562-00		5.6 kΩ	1/4 W		5%
R933	321-0289-00		10 kΩ	1/8 W	Prec	1%
R934	321-0241-00		3.16 kΩ	1/8 W	Prec	1%
R936	315-0202-00		2 kΩ	1/4 W		5%
R938	315-0751-00		750 Ω	1/4 W		5%
R941	321-0328-00		25.5 kΩ	1/8 W	Prec	1%
R942	321-0372-00		73.2 kΩ	1/8 W	Prec	1%
R944	315-0243-00		24 kΩ	1/4 W		5%
R946	315-0183-00		18 kΩ	1/4 W		5%
R947	308-0077-00		1 kΩ	3 W	WW	1%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION			
				Resistors (cont)			
R948	301-0473-00			47 kΩ	1/2 W		5%
R950	315-0562-00			5.6 kΩ	1/4 W		5%
R951	307-0103-00			2.7 kΩ	1/4 W		5%
R953	307-0103-00			2.7 kΩ	1/4 W		5%
R955	321-0184-00			806 Ω	1/8 W	Prec	1%
R956	315-0101-00			100 Ω	1/4 W		5%
R958	315-0101-00			100 Ω	1/4 W		5%
R959	321-0253-00			4.22 kΩ	1/8 W	Prec	1%
R961	321-0203-00			1.27 kΩ	1/8 W	Prec	1%
R962	311-0442-00			250 Ω, Var			
R963	321-0184-00			806 Ω	1/8 W	Prec	1%
R965	321-0296-00			11.8 kΩ	1/8 W	Prec	1%
R967	317-0102-00			1 kΩ	1/8 W		5%
R970	315-0471-00			470 Ω	1/4 W		5%
R972	315-0100-00			10 Ω	1/4 W		5%
R973	315-0100-00			10 Ω	1/4 W		5%
R974	315-0101-00			100 Ω	1/4 W		5%
R982	315-0101-00			100 Ω	1/4 W		5%
R985	315-0101-00			100 Ω	1/4 W		5%
R986	315-0330-00			33 Ω	1/4 W		5%
R988	317-0100-00			10 Ω	1/8 W		5%
R996	315-0330-00			33 Ω	1/4 W		5%
R997	315-0101-00			100 Ω	1/4 W		5%
R998	315-0101-00			100 Ω	1/4 W		5%
R999	308-0387-00			178 Ω	3 W	WW	
				Switches			
Unwired or Wired							
SW197	260-0516-00			Pull	INVERT (Ch. A)		
SW397	260-0516-00			Pull	INVERT (Ch. B)		
SW400	Wired *262-0838-00			Rotary	UNITS/DIV (Ch. A)		
SW400	260-0921-00			Rotary	UNITS/DIV (Ch. A)		
SW420	Wired *262-0838-00			Rotary	UNITS/DIV (Ch. B)		
SW420	260-0921-00			Rotary	UNITS/DIV (Ch. B)		
SW450A SW450B	Wired *262-0837-00			Rotary	MODE		
SW450A SW450B	260-0922-00			Rotary	MODE		

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION	
				Transformers	
T155	*120-0547-00			Toroid, 15 turns, quadfilar	
T355	*120-0547-00			Toroid, 15 turns, quadfilar	
T503	*120-0546-00			Toroid, 4 turns, bifilar	
T950	*120-0561-00			Power	
				Test Points	
TP25	*214-0579-00			Pin, Test Point	
TP49	*214-0579-00			Pin, Test Point	
TP155	*214-0579-00			Pin, Test Point	
TP190	*214-0579-00			Pin, Test Point	
TP195	*214-0579-00			Pin, Test Point	
TP225	*214-0579-00			Pin, Test Point	
TP249	*214-0579-00			Pin, Test Point	
TP355	*214-0579-00			Pin, Test Point	
TP390	*214-0579-00			Pin, Test Point	
TP395	*214-0579-00			Pin, Test Point	
TP418	*214-0579-00			Pin, Test Point	
TP438	*214-0579-00			Pin, Test Point	
TP445	*214-0579-00			Pin, Test Point	
TP450	*214-0579-00			Pin, Test Point	
TP455	*214-0579-00			Pin, Test Point	
TP478	*214-0579-00			Pin, Test Point	
TP488	*214-0579-00			Pin, Test Point	
TP522	*214-0579-00			Pin, Test Point	
TP545	*214-0579-00			Pin, Test Point	
TP555	*214-0579-00			Pin, Test Point	
TP575	*214-0579-00			Pin, Test Point	
TP585	*214-0585-00			Pin, Test Point	
				Logic Card	
	*670-0175-00			Complete Card	
				Semiconductor Device, Diodes	
D601	*152-0185-00			Silicon	Replaceable by 1N4152
D602	152-0141-02			Silicon	1N4152
D604	*152-0185-00			Silicon	Replaceable by 1N4152
D605	152-0141-02			Silicon	1N4152
D607	*152-0185-00			Silicon	Replaceable by 1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D608	152-0141-02			Silicon 1N4152
D610	*152-0185-00			Silicon Replaceable by 1N4152
D611	152-0141-02			Silicon 1N4152
D613	*152-0185-00			Silicon Replaceable by 1N4152
D614	152-0141-02			Silicon 1N4152
D616	*152-0185-00			Silicon Replaceable by 1N4152
D617	152-0141-02			Silicon 1N4152
D619	*152-0185-00			Silicon Replaceable by 1N4152
D620	152-0141-02			Silicon 1N4152
D622	*152-0185-00			Silicon Replaceable by 1N4152
D623	151-0141-02			Silicon 1N4152
D625	*152-0185-00			Silicon Replaceable by 1N4152
D626	152-0141-02			Silicon 1N4152
D701	*152-0185-00			Silicon Replaceable by 1N4152
D702	152-0141-02			Silicon 1N4152
D704	*152-0185-00			Silicon Replaceable by 1N4152
D705	152-0141-02			Silicon 1N4152
D707	*152-0185-00			Silicon Replaceable by 1N4152
D708	152-0141-02			Silicon 1N4152
D710	*152-0185-00			Silicon Replaceable by 1N4152
D711	152-0141-02			Silicon 1N4152
D713	*152-0185-00			Silicon Replaceable by 1N4152
D714	152-0141-02			Silicon 1N4152
D716	*152-0185-00			Silicon Replaceable by 1N4152
D717	152-0141-02			Silicon 1N4152
D719	*152-0185-00			Silicon Replaceable by 1N4152
D720	152-0141-02			Silicon 1N4152
D722	*152-0185-00			Silicon Replaceable by 1N4152
D723	152-0141-02			Silicon 1N4152
D725	*152-0185-00			Silicon Replaceable by 1N4152
D726	152-0141-02			Silicon 1N4152
D792	*152-0185-00			Silicon Replaceable by 1N4152
D793	*152-0185-00			Silicon Replaceable by 1N4152
D797	*152-0185-00			Silicon Replaceable by 1N4152
D803	*152-0185-00			Silicon Replaceable by 1N4152
D806	*152-0185-00			Silicon Replaceable by 1N4152
D807	*152-0185-00			Silicon Replaceable by 1N4152
D808	*152-0185-00			Silicon Replaceable by 1N4152
D809	*152-0185-00			Silicon Replaceable by 1N4152
D810	*152-0185-00			Silicon Replaceable by 1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D811	*152-0185-00		Silicon	Replaceable by 1N4152
D812	*152-0185-00		Silicon	Replaceable by 1N4152
D818	*152-0185-00		Silicon	Replaceable by 1N4152
D819	*152-0185-00		Silicon	Replaceable by 1N4152
D820	*152-0185-00		Silicon	Replaceable by 1N4152
D821	*152-0185-00		Silicon	Replaceable by 1N4152
D822	*152-0185-00		Silicon	Replaceable by 1N4152
D823	*152-0185-00		Silicon	Replaceable by 1N4152
D824	*152-0185-00		Silicon	Replaceable by 1N4152
D825	*152-0185-00		Silicon	Replaceable by 1N4152
D833	*152-0185-00		Silicon	Replaceable by 1N4152
D834	*152-0185-00		Silicon	Replaceable by 1N4152
D835	*152-0185-00		Silicon	Replaceable by 1N4152
D836	*152-0185-00		Silicon	Replaceable by 1N4152
D839	*152-0185-00		Silicon	Replaceable by 1N4152
D840	*152-0185-00		Silicon	Replaceable by 1N4152
D841	*152-0185-00		Silicon	Replaceable by 1N4152
D842	*152-0185-00		Silicon	Replaceable by 1N4152
D843	*152-0185-00		Silicon	Replaceable by 1N4152
D860	*152-0185-00		Silicon	Replaceable by 1N4152
D862	*152-0185-00		Silicon	Replaceable by 1N4152
D863	*152-0185-00		Silicon	Replaceable by 1N4152
D865	*152-0185-00		Silicon	Replaceable by 1N4152
D866	*152-0185-00		Silicon	Replaceable by 1N4152
D867	*152-0185-00		Silicon	Replaceable by 1N4152
D868	*152-0185-00		Silicon	Replaceable by 1N4152
D869	*152-0185-00		Silicon	Replaceable by 1N4152
D870	*152-0185-00		Silicon	Replaceable by 1N4152
D874	*152-0185-00		Silicon	Replaceable by 1N4152
D876	*152-0185-00		Silicon	Replaceable by 1N4152
D877	*152-0185-00		Silicon	Replaceable by 1N4152
D878	*152-0185-00		Silicon	Replaceable by 1N4152
D879	*152-0185-00		Silicon	Replaceable by 1N4152
D880	*152-0185-00		Silicon	Replaceable by 1N4152
D881	*152-0185-00		Silicon	Replaceable by 1N4152
D884	*152-0185-00		Silicon	Replaceable by 1N4152
D885	*152-0185-00		Silicon	Replaceable by 1N4152
D886	*152-0185-00		Silicon	Replaceable by 1N4152
D891	*152-0185-00		Silicon	Replaceable by 1N4152
D892	*152-0185-00		Silicon	Replaceable by 1N4152

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D893	*152-0185-00		Silicon	Replaceable by 1N4152
D895	*152-0185-00		Silicon	Replaceable by 1N4152
D896	*152-0185-00		Silicon	Replaceable by 1N4152
D899	*152-0185-00		Silicon	Replaceable by 1N4152
		Transistors		
Q602	151-0188-00		Silicon	2N3906
Q604	151-0188-00		Silicon	2N3906
Q608	151-0188-00		Silicon	2N3906
Q610	151-0188-00		Silicon	2N3906
Q614	151-0188-00		Silicon	2N3906
Q616	151-0188-00		Silicon	2N3906
Q620	151-0188-00		Silicon	2N3906
Q622	151-0188-00		Silicon	2N3906
Q626	151-0188-00		Silicon	2N3906
Q702	151-0188-00		Silicon	2N3906
Q704	151-0188-00		Silicon	2N3906
Q708	151-0188-00		Silicon	2N3906
Q710	151-0188-00		Silicon	2N3906
Q714	151-0188-00		Silicon	2N3906
Q716	151-0188-00		Silicon	2N3906
Q720	151-0188-00		Silicon	2N3906
Q722	151-0188-00		Silicon	2N3906
Q726	151-0188-00		Silicon	2N3906
Q796	151-0188-00		Silicon	2N3906
Q803	151-0190-00		Silicon	2N3904
Q806	*151-0150-00		Silicon	Selected from 2N3440
Q812	151-0188-00		Silicon	2N3906
Q814	151-0188-00		Silicon	2N3906
Q816	151-0188-00		Silicon	2N3906
Q826	151-0188-00		Silicon	2N3906
Q828	151-0188-00		Silicon	2N3906
Q836	*151-0150-00		Silicon	Selected from 2N3440
Q839	*151-0150-00		Silicon	Selected from 2N3440
Q843	*151-0150-00		Silicon	Selected from 2N3440
Q859	151-0190-00		Silicon	2N3904
Q872	151-0188-00		Silicon	2N3906
Q874	151-0188-00		Silicon	2N3906
Q884	151-0188-00		Silicon	2N3906
Q891	151-0190-00		Silicon	2N3904
Q892	151-0190-00		Silicon	2N3904

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION		
			Transistors (cont)			
Q893	151-0190-00		Silicon	2N3904		
Q899	151-0190-00		Silicon	2N3904		
			Resistors			
Resistors are fixed, composition, ±10% unless otherwise indicated.						
R600	317-0101-00		100 Ω	1/8 W		5%
R601	317-0362-00		3.6 kΩ	1/8 W		5%
R602	308-0472-00		25 kΩ	1/4 W	WW	1/20%
R604	317-0752-00		7.5 kΩ	1/8 W		5%
R605	308-0475-00		50 kΩ	1/4 W	WW	1/10%
R607	317-0153-00		15 kΩ	1/8 W		5%
R608	321-0644-00		100 kΩ	1/8 W	Prec	1/4%
R610	317-0303-00		30 kΩ	1/8 W		5%
R611	321-0646-00		200 kΩ	1/8 W	Prec	1/2%
R613	317-0363-00		36 kΩ	1/8 W		5%
R614	321-0733-01		250 kΩ	1/8 W	Prec	1/2%
R616	317-0753-00		75 kΩ	1/8 W		5%
R617	321-0648-00		500 kΩ	1/8 W	Prec	1/2%
R619	317-0154-00		150 kΩ	1/8 W		5%
R620	321-0481-00		1 MΩ	1/8 W	Prec	1%
R622	317-0304-00		300 kΩ	1/8 W		5%
R623	315-0205-00		2 MΩ	1/4 W		5%
R625	317-0514-00		510 kΩ	1/8 W		5%
R626	317-0105-00		1 MΩ	1/8 W		5%
R628	317-0101-00		100 Ω	1/8 W		5%
R700	317-0101-00		100 Ω	1/8 W		5%
R701	317-0362-00		3.6 kΩ	1/8 W		5%
R702	308-0472-00		25 kΩ	1/4 W	WW	1/20%
R704	317-0752-00		7.5 kΩ	1/8 W		5%
R705	308-0475-00		50 kΩ	1/4 W	WW	1/10%
R707	317-0153-00		15 kΩ	1/8 W		5%
R708	321-0644-00		100 kΩ	1/8 W	Prec	1/4%
R710	317-0303-00		30 kΩ	1/8 W		5%
R711	321-0646-00		200 kΩ	1/8 W	Prec	1/2%
R713	317-0363-00		36 kΩ	1/8 W		5%
R714	321-0733-01		250 kΩ	1/8 W	Prec	1/2%
R716	317-0753-00		75 kΩ	1/8 W		5%
R717	321-0648-00		500 kΩ	1/8 W	Prec	1/2%
R719	317-0154-00		150 kΩ	1/8 W		5%
R720	321-0481-00		1 MΩ	1/8 W	Prec	1%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION		
				Resistors (cont)		
R722	317-0304-00			300 kΩ	1/8 W	5%
R723	315-0205-00			2 MΩ	1/4 W	5%
R725	317-0514-00			510 kΩ	1/8 W	5%
R726	317-0105-00			1 MΩ	1/8 W	5%
R728	317-0101-00			100 Ω	1/8 W	5%
R792	317-0122-00			1.2 kΩ	1/8 W	5%
R793	317-0472-00			4.7 kΩ	1/8 W	5%
R794	317-0203-00			20 kΩ	1/8 W	5%
R795	317-0563-00			56 kΩ	1/8 W	5%
R797	317-0181-00			180 Ω	1/8 W	5%
R798	317-0621-00			620 Ω	1/8 W	5%
R799	317-0203-00			20 kΩ	1/8 W	5%
R801	317-0273-00			27 kΩ	1/8 W	5%
R802	317-0132-00			1.3 kΩ	1/8 W	5%
R804	317-0153-00			15 kΩ	1/8 W	5%
R805	317-0153-00			15 kΩ	1/8 W	5%
R806	317-0153-00			15 kΩ	1/8 W	5%
R807	317-0164-00			160 kΩ	1/8 W	5%
R810	317-0164-00			160 kΩ	1/8 W	5%
R811	317-0104-00			100 kΩ	1/8 W	5%
R812	317-0102-00			1 kΩ	1/8 W	5%
R813	317-0183-00			18 kΩ	1/8 W	5%
R815	317-0202-00			2 kΩ	1/8 W	5%
R816	317-0681-00			680 Ω	1/8 W	5%
R817	317-0273-00			27 kΩ	1/8 W	5%
R818	317-0513-00			51 kΩ	1/8 W	5%
R822	317-0513-00			51 kΩ	1/8 W	5%
R824	317-0303-00			30 kΩ	1/8 W	5%
R825	317-0102-00			1 kΩ	1/8 W	5%
R827	317-0202-00			2 kΩ	1/8 W	5%
R828	317-0273-00			27 kΩ	1/8 W	5%
R830	317-0682-00			6.8 kΩ	1/8 W	5%
R831	317-0681-00			680 Ω	1/8 W	5%
R832	317-0122-00			1.2 kΩ	1/8 W	5%
R833	317-0153-00			15 kΩ	1/8 W	5%
R834	317-0153-00			15 kΩ	1/8 W	5%
R835	317-0153-00			15 kΩ	1/8 W	5%
R837	317-0132-00			1.3 kΩ	1/8 W	5%
R838	317-0132-00			1.3 kΩ	1/8 W	5%
R839	317-0153-00			15 kΩ	1/8 W	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION		
				Resistors (cont)		
R840	317-0153-00			15 kΩ	1/8 W	5%
R841	317-0153-00			15 kΩ	1/8 W	5%
R842	317-0153-00			15 kΩ	1/8 W	5%
R859	317-0822-00			8.2 kΩ	1/8 W	5%
R860	317-0272-00			2.7 kΩ	1/8 W	5%
R861	317-0623-00			62 kΩ	1/8 W	5%
R862	317-0912-00			9.1 kΩ	1/8 W	5%
R863	317-0273-00			27 kΩ	1/8 W	5%
R866	317-0164-00			160 kΩ	1/8 W	5%
R869	317-0164-00			160 kΩ	1/8 W	5%
R870	317-0104-00			100 kΩ	1/8 W	5%
R871	317-0102-00			1 kΩ	1/8 W	5%
R872	317-0183-00			18 kΩ	1/8 W	5%
R874	317-0562-00			5.6 kΩ	1/8 W	5%
R877	317-0513-00			51 kΩ	1/8 W	5%
R880	317-0513-00			51 kΩ	1/8 W	5%
R881	317-0303-00			30 kΩ	1/8 W	5%
R882	317-0102-00			1 kΩ	1/8 W	5%
R884	317-0562-00			5.6 kΩ	1/8 W	5%
R885	317-0242-00			2.4 kΩ	1/8 W	5%
R886	317-0242-00			2.4 kΩ	1/8 W	5%
R888	317-0242-00			2.4 kΩ	1/8 W	5%
R890	317-0182-00			1.8 kΩ	1/8 W	5%
R891	317-0362-00			3.6 kΩ	1/8 W	5%
R892	317-0303-00			30 kΩ	1/8 W	5%
R893	317-0243-00			24 kΩ	1/8 W	5%
R895	317-0273-00			27 kΩ	1/8 W	5%
R896	317-0912-00			9.1 kΩ	1/8 W	5%
R897	317-0623-00			62 kΩ	1/8 W	5%
R898	317-0822-00			8.2 kΩ	1/8 W	5%
R899	317-0272-00			2.7 kΩ	1/8 W	5%
				Integrated Circuits		
U805A U805B	156-0011-00			Dual 2-Input NAND/ NOR Gate		Replaceable by Fairchild μL914
U833A U833B	156-0011-00			Dual 2-Input NAND/ NOR Gate		Replaceable by Fairchild μL914
U834A U834B	156-0011-00			Dual 2-Input NAND/ NOR Gate		Replaceable by Fairchild μL914
U835A U835B	156-0011-00			Dual 2-Input NAND/ NOR Gate		Replaceable by Fairchild μL914
U838A U838B	156-0011-00			Dual 2-Input NAND/ NOR Gate		Replaceable by Fairchild μL914
U887A U887B	156-0011-00			Dual 2-Input NAND/ NOT Gate		Replaceable by Fairchild μL914

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION		
				Offset Card		
	*670-0176-00			Complete Card		
				Capacitors		
Tolerance ±20% unless otherwise indicated.						
C60	283-0032-00			470 pF	Cer	500 V 5%
C63	283-0060-00			100 pF	Cer	200 V 5%
C68	382-0060-00			100 pF	Cer	200 V 5%
C72	281-0617-00			15 pF	Cer	200 V
C73	283-0059-00			1 μF	Cer	25 V +80%-20%
C88	283-0060-00			100 pF	Cer	200 V 5%
C89	283-0060-00			100 pF	Cer	200 V 5%
C91	283-0103-00			180 pF	Cer	500 V 5%
C92	283-0060-00			100 pF	Cer	200 V 5%
C94	281-0603-00			39 pF	Cer	500 V 5%
C95	283-0060-00			100 pF	Cer	200 V 5%
C98	281-0657-00			13 pF	Cer	500 V 5%
C260	283-0032-00			470 pF	Cer	500 V 5%
C263	283-0060-00			100 pF	Cer	200 V 5%
C268	283-0060-00			100 pF	Cer	200 V 5%
C272	281-0617-00			15 pF	Cer	200 V
C273	283-0059-00			1 μF	Cer	25 V +80%-20%
C288	283-0060-00			100 pF	Cer	200 V 5%
C289	283-0060-00			100 pF	Cer	200 V 5%
C291	283-0103-00			180 pF	Cer	500 V 5%
C292	283-0060-00			100 pF	Cer	200 V 5%
C294	281-0603-00			39 pF	Cer	500 V 5%
C295	283-0060-00			100 pF	Cer	200 V 5%
C298	281-0657-00			13 pF	Cer	500 V 5%
C634	283-0059-00			1 μF	Cer	25 V +80%-20%
C641	283-0059-00			1 μF	Cer	25 V +80%-20%
C643	283-0060-00			100 pF	Cer	200 V 5%
C657	283-0059-00			1 μF	Cer	25 V +80%-20%
C658	283-0060-00			100 pF	Cer	200 V 5%
C734	283-0059-00			1 μF	Cer	25 V +80%-20%
C741	283-0059-00			1 μF	Cer	25 V +80%-20%
C743	283-0060-00			100 pF	Cer	200 V 5%
C757	283-0059-00			1 μF	Cer	25 V +80%-20%
C758	283-0060-00			100 pF	Cer	200 V 5%
				Semiconductor Device, Diodes		
D64	*152-0185-00			Silicon	Replaceable by 1N4152	
D69	*152-0185-00			Silicon	Replaceable by 1N4152	
D264	*152-0185-00			Silicon	Replaceable by 1N4152	
D269	*152-0185-00			Silicon	Replaceable by 1N4152	
D634	*152-0185-00			Silicon	Replaceable by 1N4152	

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION
		Semiconductor Device, Diodes (cont)		
D641	*152-0185-00		Silicon	Replaceable by 1N4152
D643	*152-0185-00		Silicon	Replaceable by 1N4152
D645	*152-0185-00		Silicon	Replaceable by 1N4152
D657	*152-0185-00		Silicon	Replaceable by 1N4152
D658	*152-0185-00		Silicon	Replaceable by 1N4152
D664	*152-0185-00		Silicon	Replaceable by 1N4152
D667	*152-0185-00		Silicon	Replaceable by 1N4152
D674	*152-0185-00		Silicon	Replaceable by 1N4152
D675	*152-0185-00		Silicon	Replaceable by 1N4152
D676	*152-0185-00		Silicon	Replaceable by 1N4152
D734	*152-0185-00		Silicon	Replaceable by 1N4152
D741	*152-0185-00		Silicon	Replaceable by 1N4152
D743	*152-0185-00		Silicon	Replaceable by 1N4152
D745	*152-0185-00		Silicon	Replaceable by 1N4152
D757	*152-0185-00		Silicon	Replaceable by 1N4152
D758	*152-0185-00		Silicon	Replaceable by 1N4152
D764	*152-0185-00		Silicon	Replaceable by 1N4152
D767	*152-0185-00		Silicon	Replaceable by 1N4152
D774	*152-0185-00		Silicon	Replaceable by 1N4152
D775	*152-0185-00		Silicon	Replaceable by 1N4152
D776	*152-0185-00		Silicon	Replaceable by 1N4152
		Transistors		
Q62	151-1021-00		Silicon	FET
Q68	151-1021-00		Silicon	FET
Q72	*151-0216-00		Silicon	Replaceable by MPS-6543
Q81	*151-0236-00		Silicon	Dual, Tek Spec
Q88	151-1021-00		Silicon	FET
Q91	151-1021-00		Silicon	FET
Q94	151-1021-00		Silicon	FET
Q262	151-1021-00		Silicon	FET
Q268	151-1021-00		Silicon	FET
Q272	*151-0216-00		Silicon	Replaceable by MPS-6543
Q281	*151-0236-00		Silicon	Dual, Tek Spec
Q288	151-1021-00		Silicon	FET
Q291	151-1021-00		Silicon	FET
Q294	151-1021-00		Silicon	FET
Q633	*151-0236-00		Silicon	Dual, Tek Spec
Q642	151-0188-00		Silicon	2N3906
Q645	151-0190-00		Silicon	2N3904
Q653	*151-0236-00		Silicon	Dual, Tek Spec
Q658	151-0188-00		Silicon	2N3906
Q660	151-0188-00		Silicon	2N3906

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION
		Transistors (cont)		
Q663	151-1021-00		Silicon	FET
Q670	151-0188-00		Silicon	2N3906
Q673	151-0190-00		Silicon	2N3904
Q675	151-0190-00		Silicon	2N3904
Q677	151-1021-00		Silicon	FET
Q733	*151-0236-00		Silicon	Dual, Tek Spec
Q742	151-0188-00		Silicon	2N3906
Q745	151-0190-00		Silicon	2N3904
Q753	*151-0236-00		Silicon	Dual, Tek Spec
Q758	151-0188-00		Silicon	2N3906
Q760	151-0188-00		Silicon	2N3906
Q763	151-1021-00		Silicon	FET
Q770	151-0188-00		Silicon	2N3906
Q773	151-0190-00		Silicon	2N3904
Q775	151-0190-00		Silicon	2N3904
Q777	151-1021-00		Silicon	FET
		Resistors		
Resistors are fixed, composition, ±10% unless otherwise indicated.				
R61	321-0268-03	6.04 kΩ	1/8 W	Prec 1/4%
R63	315-0104-00	100 kΩ	1/4 W	5%
R64	315-0102-00	1 kΩ	1/4 W	5%
R66	321-0770-03	4.204 kΩ	1/8 W	Prec 1/4%
R68	315-0104-00	100 kΩ	1/4 W	5%
R69	315-0102-00	1 kΩ	1/4 W	5%
R71	321-0767-03	38.02 kΩ	1/8 W	Prec 1/4%
R73	315-0100-00	10 Ω	1/4 W	5%
R75	321-1289-07	10.1 kΩ	1/8 W	Prec 1/10%
R76	301-0753-00	75 kΩ	1/2 W	5%
R78	315-0915-00	9.1 MΩ	1/4 W	5%
R79	321-1289-07	10.1 kΩ	1/8 W	Prec 1/10%
R81	323-0489-00	1.21 MΩ	1/2 W	1%
R83	321-0452-00	499 kΩ	1/8 W	Prec 1%
R85	315-0915-00	9.1 MΩ	1/4 W	5%
R86	311-0613-00	100 kΩ, Var		
R88	321-0289-03	10 kΩ	1/8 W	Prec 1/4%
R89	315-0102-00	1 kΩ	1/4 W	5%
R91	321-1267-03	5.97 kΩ	1/8 W	Prec 1/4%
R92	315-0102-00	1 kΩ	1/4 W	5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Resistors (cont)			
R94	321-0604-00			30 kΩ	1/8 W	Prec	1/4%
R95	315-0102-00			1 kΩ	1/4 W		5%
R97	321-0769-03			50.33 kΩ	1/8 W	Prec	1/4%
R98	321-0373-03			75 kΩ	1/8 W	Prec	1/4%
R261	321-0268-03			6.04 kΩ	1/8 W	Prec	1/4%
R263	315-0104-00			100 kΩ	1/4 W		5%
R264	315-0102-00			1 kΩ	1/4 W		5%
R266	321-0770-03			4.204 kΩ	1/8 W	Prec	1/4%
R268	315-0104-00			100 kΩ	1/4 W		5%
R269	315-0102-00			1 kΩ	1/4 W		5%
R271	321-0767-03			38.02 kΩ	1/8 W	Prec	1/4%
R273	315-0100-00			10 Ω	1/4 W		5%
R275	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R276	301-0753-00			75 kΩ	1/2 W		5%
R278	315-0915-00			9.1 MΩ	1/4 W		5%
R279	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R281	323-0489-00			1.21 MΩ	1/2 W	Prec	1%
R283	321-0452-00			499 kΩ	1/8 W	Prec	1%
R285	315-0915-00			9.1 MΩ	1/4 W		5%
R286	311-0613-00			100 kΩ, Var			
R288	321-0289-03			10 kΩ	1/8 W	Prec	1/4%
R289	315-0102-00			1 kΩ	1/4 W		5%
R291	321-1267-03			5.97 kΩ	1/8 W	Prec	1/4%
R292	315-0102-00			1 kΩ	1/4 W		5%
R294	321-0604-00			30 kΩ	1/8 W	Prec	1/4%
R295	315-0102-00			1 kΩ	1/4 W		5%
R297	321-0769-03			50.33 kΩ	1/8 W	Prec	1/4%
R298	321-0373-03			75 kΩ	1/8 W	Prec	1/4%
R630	315-0106-00			10 MΩ	1/4 W		5%
R632	315-0101-00			100 Ω	1/4 W		5%
R633	321-0452-00			499 kΩ	1/8 W	Prec	1%
R635	321-0289-00			10 kΩ	1/8 W	Prec	1%
R636	321-0348-00			41.2 kΩ	1/8 W	Prec	1%
R637	321-0451-00			487 kΩ	1/8 W	Prec	1%
R638	311-0613-00			100 kΩ, Var			
R639	323-0488-00			1.18 MΩ	1/2 W	Prec	1%
R641	315-0101-00			100 Ω	1/4 W		5%
R643	315-0184-00			180 kΩ	1/4 W		5%
R644	315-0101-00			100 Ω	1/4 W		5%
R645	301-0433-00			43 kΩ	1/2 W		5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	DESCRIPTION			
				Resistors (cont)			
R646	321-0766-06			4.053 kΩ	1/8 W	Prec	1/4%
R650	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R651	315-0106-00			10 MΩ	1/4 W		5%
R653	315-0101-00			100 Ω	1/4 W		5%
R654	321-0452-00			499 kΩ	1/8 W	Prec	1%
R655	323-0488-00			1.18 MΩ	1/2 W	Prec	1%
R657	315-0101-00			100 Ω	1/4 W		5%
R658	315-0184-00			180 kΩ	1/4 W		5%
R660	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R661	315-0432-00			4.3 kΩ	1/4 W		5%
R662	315-0101-00			100 Ω	1/4 W		5%
R663	315-0104-00			100 kΩ	1/4 W		5%
R664	315-0102-00			1 kΩ	1/4 W		5%
R665	321-0768-03			18.99 kΩ	1/8 W	Prec	1/4%
R667	315-0184-00			180 kΩ	1/4 W		5%
R668	315-0203-00			20 kΩ	1/4 W		5%
R669	315-0104-00			100 kΩ	1/4 W		5%
R670	315-0564-00			560 kΩ	1/4 W		5%
R671	315-0473-00			47 kΩ	1/4 W		5%
R673	315-0364-00			360 kΩ	1/4 W		5%
R674	315-0105-00			1 MΩ	1/4 W		5%
R675	315-0364-00			360 kΩ	1/4 W		5%
R676	315-0102-00			1 kΩ	1/4 W		5%
R677	315-0104-00			100 kΩ	1/4 W		5%
R678	321-0289-00			10 kΩ	1/8 W	Prec	1%
R730	315-0106-00			10 MΩ	1/4 W		5%
R732	315-0101-00			100 Ω	1/4 W		5%
R733	321-0452-00			499 kΩ	1/8 W	Prec	1%
R735	321-0289-00			10 kΩ	1/8 W	Prec	1%
R736	321-0348-00			41.2 kΩ	1/8 W	Prec	1%
R737	321-0451-00			487 kΩ	1/8 W	Prec	1%
R738	311-0613-00			100 kΩ, Var			
R739	323-0488-00			1.18 MΩ	1/2 W	Prec	1%
R741	315-0101-00			100 Ω	1/4 W		5%
R743	315-0184-00			180 kΩ	1/4 W		5%
R744	315-0101-00			100 Ω	1/4 W		5%
R745	301-0433-00			43 kΩ	1/2 W		5%
R746	321-0766-06			4.053 kΩ	1/8 W	Prec	1/4%
R750	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R751	315-0106-00			10 MΩ	1/4 W		5%

CKT. NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	DISC	DESCRIPTION			
				Resistors (cont)			
R753	315-0101-00			100 Ω	1/4 W		5%
R754	321-0452-00			499 kΩ	1/8 W	Prec	1%
R755	323-0488-00			1.18 MΩ	1/2 W	Prec	1%
R757	315-0101-00			100 Ω	1/4 W		5%
R758	315-0184-00			180 kΩ	1/4 W		5%
R760	321-1289-07			10.1 kΩ	1/8 W	Prec	1/10%
R761	315-0432-00			4.3 kΩ	1/4 W		5%
R762	315-0101-00			100 Ω	1/4 W		5%
R763	315-0104-00			100 kΩ	1/4 W		5%
R764	315-0102-00			1 kΩ	1/4 W		5%
R765	321-0768-03			18.99 kΩ	1/8 W	Prec	1/4%
R767	315-0184-00			180 kΩ	1/4 W		5%
R768	315-0203-00			20 kΩ	1/4 W		5%
R769	315-0104-00			100 kΩ	1/4 W		5%
R770	315-0564-00			560 kΩ	1/4 W		5%
R771	315-0473-00			47 kΩ	1/4 W		5%
R773	315-0364-00			360 kΩ	1/4 W		5%
R774	315-0105-00			1 MΩ	1/4 W		5%
R775	315-0364-00			360 kΩ	1/4 W		5%
R776	315-0102-00			1 kΩ	1/4 W		5%
R777	315-0104-00			100 kΩ	1/4 W		5%
R778	321-0289-00			10 kΩ	1/8 W	Prec	1%
				Test Points			
TP663	*214-0579-00			Pin, Test Point			
TP763	*214-0579-00			Pin, Test Point			

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations which appear on the pullout pages immediately following the Diagrams section of this instruction manual.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the Description column.

Assembly and/or Component
Detail Part of Assembly and/or Component
mounting hardware for Detail Part
Parts of Detail Part
mounting hardware for Parts of Detail Part
mounting hardware for Assembly and/or Component

Mounting hardware always appears in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Mounting hardware must be purchased separately, unless otherwise specified.

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ABBREVIATIONS AND SYMBOLS

For an explanation of the abbreviations and symbols used in this section, please refer to the page immediately preceding the Electrical Parts List in this instruction manual.

INDEX OF MECHANICAL PARTS LIST ILLUSTRATIONS

(Located behind diagrams)

SECTION 9
MECHANICAL PARTS LIST

FIG. 1 EXPLODED VIEW

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	QTY	1 2 3 4 5	DESCRIPTION
1-1	311-0195-00			1		DIAL, w/brakes (CH A)
	- - - - - -			-		dial includes:
	213-0048-00			1		SCREW, set, 4-40 x 1/8 inch, HSS
-2	366-0365-00			1		KNOB, red--CAL VARIABLE (CH A)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-3	366-0322-00			1		KNOB, charcoal--UNITS/DIV (CH A)
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-4	262-0838-00			1		SWITCH, wired--UNITS/DIV (CH A)
	- - - - - -			-		switch includes:
	260-0921-00			1		SWITCH, unwired
-5	260-0516-00			1		SWITCH, push
	- - - - - -			-		mounting hardware: (not included w/switch)
-6	211-0089-00			2		SCREW, 2-56 x 3/8 inch, PHS
-7	210-0405-00			2		NUT, hex., 2-56 x 3/16 inch
-8	407-0428-00			1		BRACKET
-9	- - - - - -			1		RESISTOR, variable
	- - - - - -			-		resistor includes:
	213-0022-00			1		SCREW, set, 4-40 x 3/16 inch, HSS
	- - - - - -			-		mounting hardware: (not included w/resistor)
-10	214-0749-00			1		SPRING, detent
-11	384-0689-00			1		SHAFT, extension
-12	351-0107-00			1		GUIDE, mounting
	- - - - - -			-		mounting hardware: (not included w/guide)
	210-0001-00			2		LOCKWASHER, internal, #2
-13	210-0405-00			2		NUT, hex., 2-56 x 3/16 inch
	- - - - - -			-		mounting hardware: (not included w/switch)
-14	210-0255-00			1		LUG, solder, 3/8 inch ID
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
-15	366-0189-00			1		KNOB, red--NORMAL SMOOTH
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-16	366-0322-00			1		KNOB, charcoal--MODE
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-17	262-0837-00			1		SWITCH, wired--MODE
	- - - - - -			-		switch includes:
	260-0992-00			1		SWITCH, unwired
	- - - - - -			-		mounting hardware: (not included w/switch)
-18	210-0255-00			1		LUG, solder, 3/8 inch diameter
-19	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch

FIG. 1 EXPLODED VIEW (cont)

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	DESCRIPTION 1 2 3 4 5
1-20	331-0195-00			1	DIAL, w/brakes (CH B)
	- - - - - -			-	dial includes:
	213-0048-00			1	SCREW, set, 4-40 x 1/8 inch, HSS
-21	366-0365-00			1	KNOB, red--CAL VARIABLE (CH B)
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-22	366-0322-00			1	KNOB, charcoal--UNITS/DIV (CH B)
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-23	262-0838-00			1	SWITCH, wired--UNITS/DIV (CH B)
	- - - - - -			-	switch includes:
	260-0921-00			1	SWITCH, unwired
-24	260-0516-00			1	SWITCH, push
	- - - - - -			-	mounting hardware: (not included w/switch)
-25	211-0089-00			2	SCREW, 2-56 x 3/8 inch, PHS
-26	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
-27	407-0428-00			1	BRACKET
-28	- - - - - -			1	RESISTOR, variable
	- - - - - -			-	resistor includes:
	213-0022-00			1	SCREW, set, 4-40 x 3/16 inch, HSS
	- - - - - -			-	mounting hardware: (not included w/resistor)
-29	214-0749-00			1	SPRING, detent
-30	384-0689-00			1	SHAFT, extension
-31	351-0107-00			1	GUIDE, mounting
	- - - - - -			-	mounting hardware: (not included w/guide)
	210-0001-00			2	LOCKWASHER, internal, #2
-32	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
	- - - - - -			-	mounting hardware: (not included w/switch)
-33	210-0255-00			1	LUG, solder, 3/8 inch ID
	210-0978-00			1	WASHER, flat, 3/8 ID x 1/2 inch OD
	210-0590-00			1	NUT, hex., 3/8-32 x 7/16 inch
-34	- - - - - -			4	RESISTOR, variable
	- - - - - -			-	mounting hardware for each: (not included w/resistor)
-35	210-0471-00			1	NUT, hex., 1/4-32 x 5/16 x 19/32 inch long
-36	358-0054-00			1	BUSHING, front panel
-37	- - - - - -			1	RESISTOR, variable
	- - - - - -			-	mounting hardware: (not included w/resistor)
-38	210-0471-00			1	NUT, hex., 1/4-32 x 5/16 x 19/32 inch long
	210-0223-00			1	LUG, solder, 1/4 ID x 7/16 inch OD, SE
-39	358-0054-00			1	BUSHING, front panel
-40	366-0061-00			1	KNOB, gray, plug-in securing
	- - - - - -			-	knob includes:
	213-0020-00			1	SCREW, set, 6-32 x 1/8 inch, HSS
-41	214-0052-00			1	FASTENER, pawl right, w/stop
	- - - - - -			-	mounting hardware: (not included w/fastener)
	210-0004-00			2	LOCKWASHER, internal, #4
-42	210-0406-00			2	NUT, hex., 4-40 x 3/16 inch

FIG. 1 EXPLODED VIEW (cont)

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF	SERIAL/MODEL NO. DISC	QTY	DESCRIPTION 1 2 3 4 5
1-43	- - - - - -			1	LIGHT, w/hardware--EXTERNAL PROGRAM (see Elect Parts List)
-44	333-1054-01			1	PANEL, front
-45	386-1377-00			1	SUB-PANEL, front
-46	367-0075-00			1	HANDLE, carrying
	- - - - - -			-	mounting hardware: (not included w/handle)
-47	213-0187-00			2	SCREW, set, 8-32 x 7/16 inch, HSS
-48	352-0084-00			2	HOLDER, plastic, neon
-49	378-0541-00			2	FILTER, lens, neon
-50	200-0609-00			2	COVER, neon holder
-51	386-1355-00			1	PLATE, chassis support
	- - - - - -			-	plate includes:
-52	211-0094-00			4	SCREW, 4-40 x 1/2 inch, THS
-53	358-0215-00			2	BUSHING, plastic, horseshoe
-54	348-0149-00			3	GROMMET, plastic, "U" shaped
-55	406-0635-00			2	BRACKET, plastic
	- - - - - -			-	mounting hardware for each: (not included w/bracket)
	213-0088-00			2	SCREW, thread forming, 4-40 x 1/4 inch, PHS
-56	- - - - - -			2	RESISTOR, variable
	- - - - - -			-	mounting hardware for each: (not included w/resistor)
-57	210-0438-00			2	NUT, hex., 1-72 x 5/32 inch
-58	343-0089-00			3	CLAMP, cable, plastic, large
-59	441-0772-00			1	CHASSIS, vertical
	- - - - - -			-	mounting hardware: (not included w/chassis)
-60	211-0504-00			5	SCREW, 6-32 x 1/4 inch, PHS
-61	210-0202-00			1	LUG, solder, SE #6
-62	441-0771-00			1	CHASSIS, output
	- - - - - -			-	mounting hardware: (not included w/chassis)
-63	211-0504-00			6	SCREW, 6-32 x 1/4 inch, PHS
-64	214-1042-00			14	SPRING, helical compression
-65	344-0152-00			2	CLIP, circuit board
	- - - - - -			-	mounting hardware for each: (not included w/clip)
-66	211-0503-00			2	SCREW, 6-32 x 3/16 inch, PHS

FIG. 1 EXPLODED VIEW (cont)

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	DESCRIPTION 1 2 3 4 5
1-67	346-0054-00			4	STRAP, retainer
-68	129-0162-00			2	POST, metal
	- - - - - -			-	mounting hardware for each: (not included w/post)
-69	211-0007-00			2	SCREW, 4-40 x 3/16 inch, PHS
-70	131-0549-00			2	CONNECTOR, 56 pin
	- - - - - -			-	mounting hardware for each: (not included w/connector)
-71	211-0014-00			2	SCREW, 4-40 x 1/2 inch, PHS
-72	214-0702-00			3	KEY, polarizing
-73	344-0116-00			1	CLIP, capacitor mounting
	- - - - - -			-	mounting hardware: (not included w/clip)
	213-0044-00			1	SCREW, thread forming, 5-32 x 3/16 inch, PHS
-74	344-0118-00			1	CLIP, capacitor mounting
	- - - - - -			-	mounting hardware: (not included w/clip)
	213-0044-00			1	SCREW, thread forming, 5-32 x 3/16 inch, PHS
-75	200-0256-00			1	COVER, capacitor, plastic, 1 ID x 2 1/32 inches long
-76	131-0433-00			1	CONNECTOR, terminal
	358-0241-00			1	BUSHING, plastic
-77	129-0152-00			2	POST, metal
	- - - - - -			-	mounting hardware for each: (not included w/post)
-78	211-0504-00			2	SCREW, 6-32 x 1/4 inch, PHS
-79	- - - - - -			1	TRANSFORMER
	- - - - - -			-	mounting hardware: (not included w/transformer)
	210-0004-00			2	LOCKWASHER, internal, #4
-80	211-0020-00			2	SCREW, 4-40 x 1 1/8 inches, RHS
-81	670-0175-00			1	ASSEMBLY, circuit card--LOGIC
	- - - - - -			-	assembly includes:
	388-0964-00			1	CARD, circuit
-82	136-0183-00			4	SOCKET, transistor, 3 pin
-83	136-0220-00			11	SOCKET, transistor, 3 pin
-84	136-0235-00			11	SOCKET, transistor, 6 pin
-85	136-0237-00			6	SOCKET, transistor, 8 pin
-86	200-0385-00			4	COVER, transistor
-87	214-0579-00			1	PIN, test point
-88	367-0090-00			1	GRIP, plastic
-89	210-1062-00			1	WASHER, recessed, plastic
-90	213-0082-00			1	SCREW, 4-40 x 1/2 inch, PHS

FIG. 1 EXPLODED VIEW (cont)

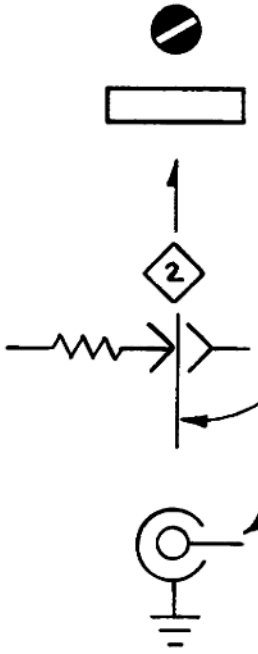
FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	DESCRIPTION 1 2 3 4 5
1-91	670-0176-00			1	ASSEMBLY, circuit card--OFFSET
	- - - - - -			-	assembly includes:
	388-0965-00			1	CARD, circuit
-92	136-0220-00			30	SOCKET, transistor, 3 pin
-93	136-0235-00			6	SOCKET, transistor, 6 pin
-94	214-0579-00			3	PIN, test point
-95	352-0100-00			4	HOLDER, variable resistor
-96	358-0214-00			4	BUSHING, plastic
-97	367-0090-00			1	GRIP, plastic
-98	210-1062-00			1	WASHER, recessed, plastic
-99	213-0082-00			1	SCREW, 4-40 x 1/2 inch, PHS
-100	214-1036-00			1	INSULATOR, plate
-101	670-0174-00			1	ASSEMBLY, circuit board--VERTICAL
	- - - - - -			-	assembly includes:
	388-0963-00			1	BOARD, circuit
-102	136-0220-00			39	SOCKET, transistor, 3 pin
-103	136-0235-00			4	SOCKET, transistor, 6 pin
-104	136-0263-00			42	SOCKET, connector pin
-105	214-0579-00			14	PIN, test point
-106	361-0182-00			6	SPACER, sleeve
	- - - - - -			-	mounting hardware: (not included w/assembly)
-107	211-0610-00			6	SCREW, 6-32 x 3/8 inch, PHB
-108	214-1037-00			1	INSULATOR, plate
-109	670-0173-00			1	ASSEMBLY, circuit board--OUTPUT
	- - - - - -			-	assembly includes:
	388-0962-00			1	BOARD, circuit
-110	136-0183-00			8	SOCKET, transistor, 3 pin
-111	136-0220-00			33	SOCKET, transistor, 3 pin
-112	136-0235-00			3	SOCKET, transistor, 6 pin
-113	136-0263-00			87	SOCKET, connector pin
-114	200-0385-00			6	COVER, transistor
-115	214-0579-00			15	PIN, test point
-116	361-0182-00			8	SPACER, sleeve
	- - - - - -			-	mounting hardware: (not included w/assembly)
-117	211-0610-00			8	SCREW, 6-32 x 3/8 inch, PHB
-118	- - - - - -			1	TRANSISTOR
	- - - - - -			-	mounting hardware: (not included w/transistor)
	211-0507-00			2	SCREW, 6-32 x 5/16 inch, PHS
-119	210-0457-00			2	NUT, keps, 6-32 x 5/16 inch
-120	131-0513-02			134	CONNECTOR, feed thru
	- - - - - -			-	mounting hardware for each: (not included w/connector)
-121	358-0329-00			1	BUSHING, plastic

FIG. 1 EXPLODED VIEW (cont)

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	DESCRIPTION 1 2 3 4 5
1-122	384-0615-00			4	ROD, spacing
-123	131-0149-00			1	CONNECTOR, 24 contact, male
	- - - - - -			-	mounting hardware: (not included w/connector)
-124	211-0016-00			2	SCREW, 4-40 x 5/8 inch, RHS
	166-0032-00			2	SPACER, 5/16 inch long
-125	210-0586-00			2	NUT, keps, 4-40 x 1/4 inch
-126	131-0149-00			1	CONNECTOR, 24 contact, male
	- - - - - -			-	mounting hardware: (not included w/connector)
	211-0008-00			2	SCREW, 4-40 x 1/4 inch, PHS
-127	210-0586-00			2	NUT, keps, 4-40 x 1/4 inch
-128	131-0327-00			2	CONNECTOR, 30 contact, female
	- - - - - -			-	mounting hardware: (not included w/connector)
	211-0014-00			2	SCREW, 4-40 x 1/2 inch, PHS
-129	210-0586-00			2	NUT, keps, 4-40 x 1/4 inch
-130	351-0037-00			1	GUIDE, plug-in, plastic
	- - - - - -			-	mounting hardware: (not included w/guide)
	211-0013-00			1	SCREW, 4-40 x 3/8 inch, RHS
	210-0586-00			1	NUT, keps, 4-40 x 1/4 inch
-131	210-0202-00			1	LUG, solder, SE #6
	- - - - - -			-	mounting hardware: (not included w/lug)
	211-0504-00			1	SCREW, 6-32 x 1/4 inch, PHS
	210-0457-00			1	NUT, keps, 6-32 x 5/16 inch
-132	386-1354-00			1	PLATE, rear
	- - - - - -			-	mounting hardware: (not included w/plate)
-133	212-0023-00			4	SCREW, 8-32 x 3/8 inch, PHS
-134	179-1284-00			1	CABLE HARNESS, chassis
	- - - - - -			-	cable harness includes:
	131-0512-00			110	CONNECTOR, terminal
-135	179-1285-00			1	CABLE HARNESS, logic & switch
	- - - - - -			-	cable harness includes:
	131-0512-00			7	CONNECTOR, terminal
-136	179-1287-00			1	CABLE HARNESS, vertical
	- - - - - -			-	cable harness includes:
	131-0512-00			12	CONNECTOR, terminal
-137	179-1288-00			1	CABLE HARNESS, output
	- - - - - -			-	cable harness includes:
	131-0512-00			13	CONNECTOR, terminal

SECTION 10
DIAGRAMS

The following symbols are used on the diagrams:



Screwdriver adjustment

Front panel control or connector

Clockwise control rotation in direction of arrow

Refer to indicated diagram

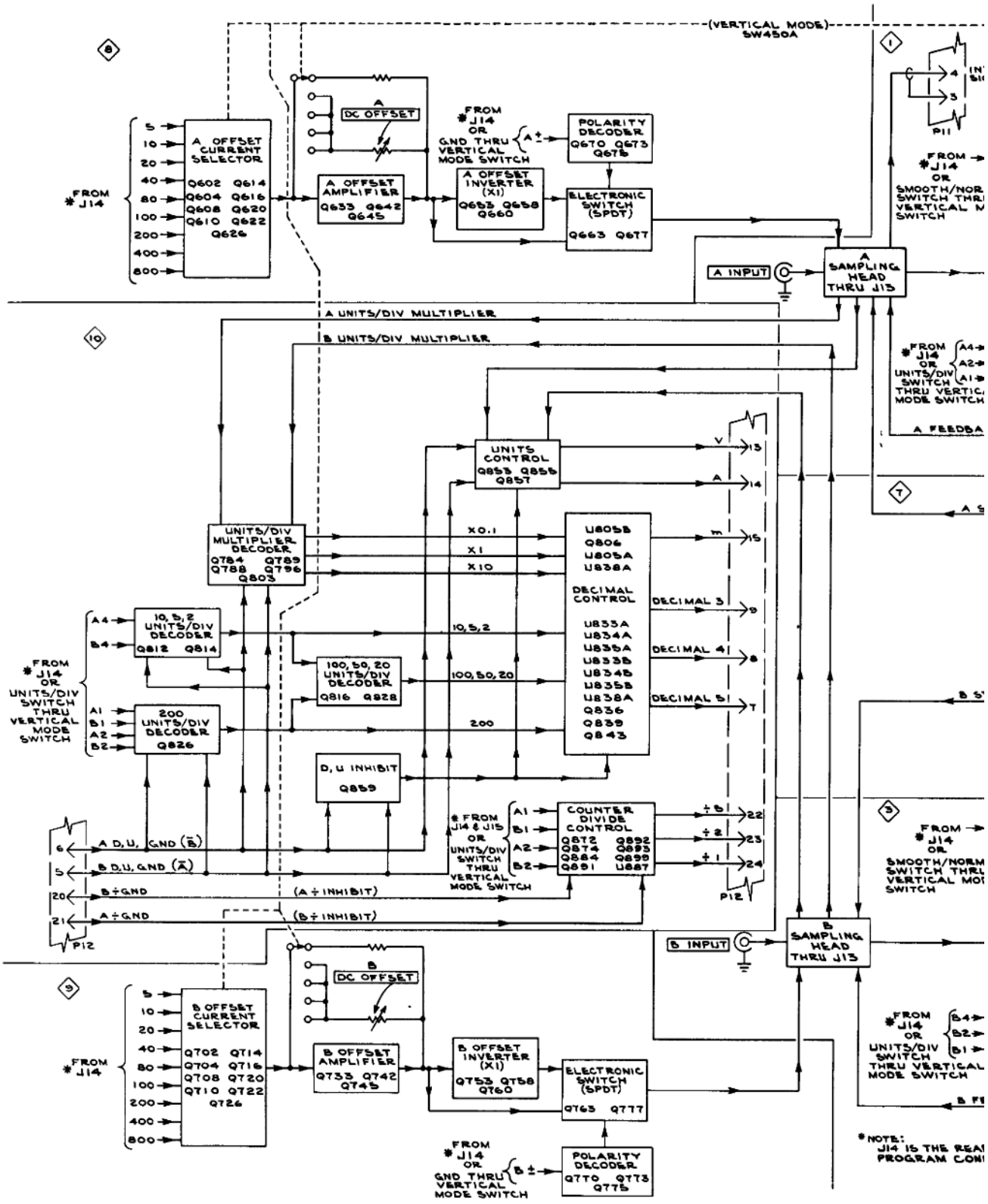
Blue line encloses components located on circuit board

Sampling Head
50 Ω Input Conn.

VOLTAGES AND WAVEFORMS TEST CONDITIONS

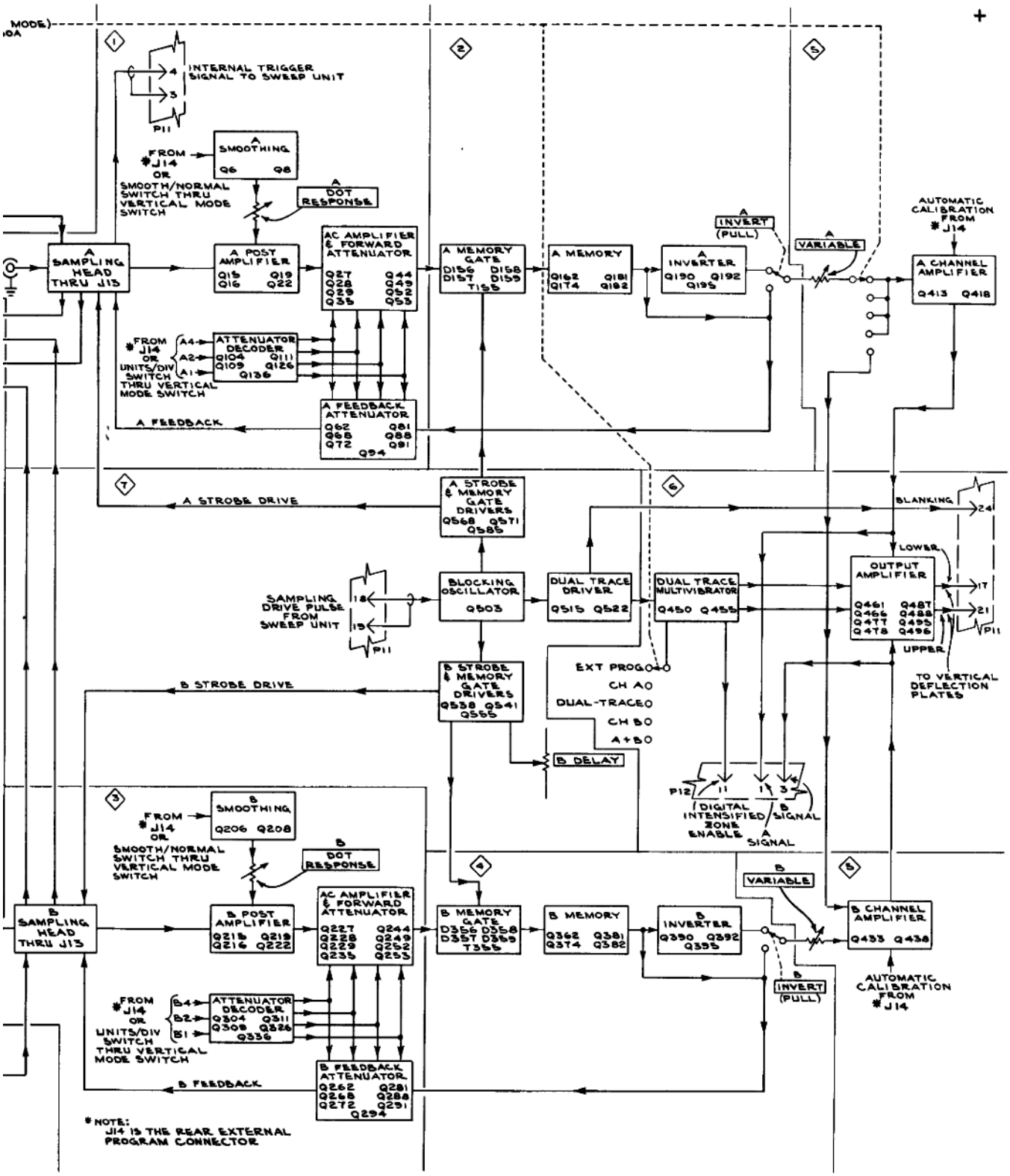
Typical voltage measurements and waveform photographs (shown in blue) were obtained under the following conditions unless noted otherwise on the individual diagrams:

Test Oscilloscope	
Bandwidth	DC to at least 50 MHz
Probe Input Impedance	10 Megohms, 7 picofarads
Probe Ground Lead	Clipped to Type 3S6 chassis
Triggering	Internal unless indicated otherwise
DC Voltmeter	
Type	Volt-Ohmmeter
Sensitivity	20,000 Ω/Volt
Type 3S6 Conditions	A calibrated sampling head connected to Channel A (or B) being tested. Connected to Oscilloscope through Type 3S6 plug-in extender (Tektronix Part No. 067-0590-00). Termination or coaxial cable connected. (Refer to sampling head instruction manual) No input signal. Extend the offset circuit board with an extender board (Tektronix Part No. 012-0149-00).
Type 3S6 Control Settings (both channels)	
Mode switch	CH A (CH B)
UNITS/DIV	200
VARIABLE	CAL
INVERT	Pushed in
DC OFFSET	Midrange, 0 Volts at test point TP663 for channel A, (TP763 for channel B).
Sampling Sweep Unit	
Sweep rate 100 ns/div or faster, Trigger Sensitivity control fully clockwise (free run).	


(VERTICAL MODE) SW450A
A OFFSET CURRENT SELECTOR
Q602 Q614 Q604 Q616 Q608 Q620 Q610 Q622 Q626
A DC OFFSET
A OFFSET AMPLIFIER Q633 Q642 Q645
A OFFSET INVERTER (X1) Q653 Q658 Q660
POLARITY DECODER Q670 Q673 Q675
ELECTRONIC SWITCH (5PDT) Q663 Q677
A INPUT
A SAMPLING HEAD THRU J13
A UNITS/DIV MULTIPLIER
B UNITS/DIV MULTIPLIER
UNITS CONTROL Q853 Q855 Q857
UNITS/DIV MULTIPLIER DECODER Q784 Q789 Q788 Q796 Q803
X0.1
X1
X10
U805B Q806 U805A U838A
DECIMAL CONTROL
U835A U834A U835A U833B U834B U835B U838A Q836 Q839 Q843
DECIMAL 3
DECIMAL 4
DECIMAL 5
10,5,2 UNITS/DIV DECODER Q812 Q814
100,50,20 UNITS/DIV DECODER Q816 Q828
200 UNITS/DIV DECODER Q826
D, U INHIBIT Q859
COUNTER DIVIDE CONTROL Q872 Q892 Q874 Q893 Q884 Q890 Q891 Q887
A D,U, GND
B D,U, GND
B÷GND
A÷GND
(A÷INHIBIT)
(B÷INHIBIT)
B OFFSET CURRENT SELECTOR
Q702 Q714 Q704 Q716 Q708 Q720 Q710 Q722 Q726
B DC OFFSET
B OFFSET AMPLIFIER Q733 Q742 Q745
B OFFSET INVERTER (X1) Q753 Q758 Q760
ELECTRONIC SWITCH (5PDT) Q763 Q777
POLARITY DECODER Q770 Q773 Q775
B INPUT
B SAMPLING HEAD THRU J13
FROM *J14 OR GND THRU VERTICAL MODE SWITCH
FROM *J14 OR UNITS/DIV SWITCH THRU VERTICAL MODE SWITCH
FROM *J14 & J15 OR UNITS/DIV SWITCH THRU VERTICAL MODE SWITCH
P11
P12
*NOTE:
J14 IS THE REAR PROGRAM CONN

TYPE 356

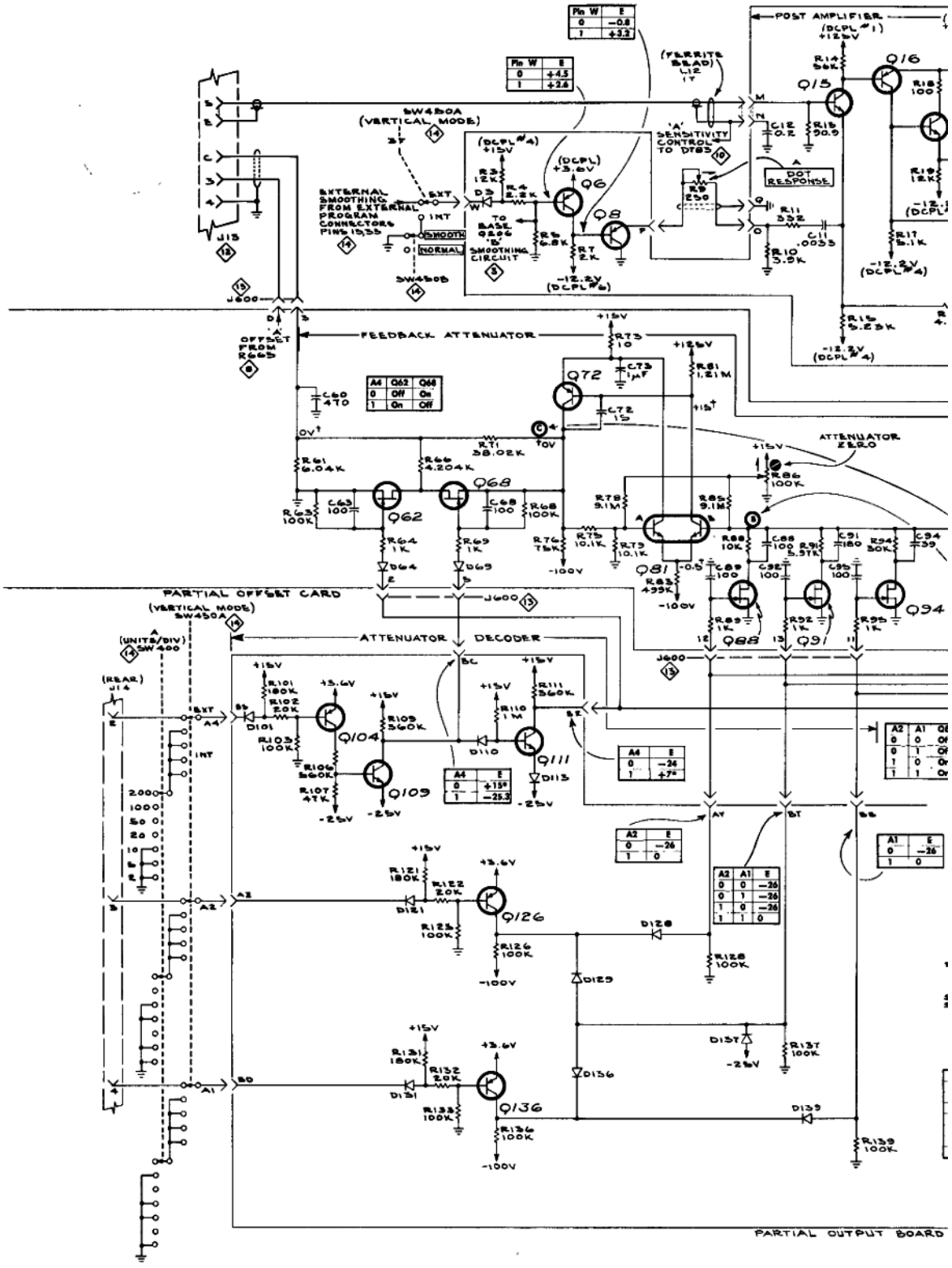
A

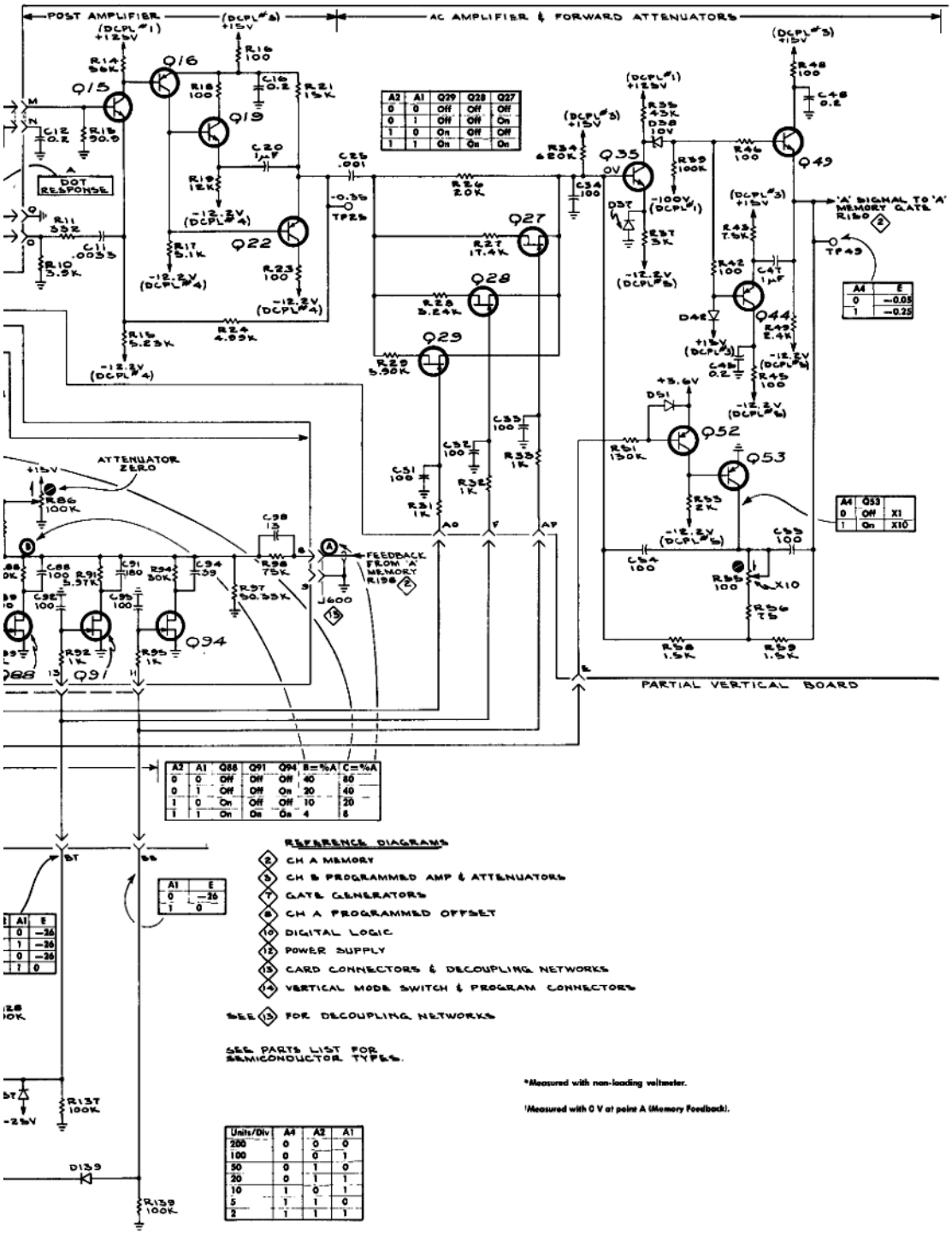


A

BLOCK DIAGRAM

PLM 868


POST AMPLIFIER
FEEDBACK ATTENUATOR
PARTIAL OFFSET CARD
ATTENUATOR DECODER
PARTIAL OUTPUT BOARD
SW450A (VERTICAL MODE)
ATTENUATOR ZERO
DOT RESPONSE
EXTERNAL SMOOTHING FROM EXTERNAL PROGRAM CONNECTORS PINS 15,35
TO BASE Q82C 'B' SMOOTHING CIRCUIT
(FERRITE BEAD) L12
'A' SENSITIVITY CONTROL TO DT85
'A' OFFSET FROM R665
(UNITS/DIV) SW400
(REAR) J14
J600
J615
SW450B
Q15
Q16
Q6
Q8
Q62
Q68
Q72
Q81
Q88
Q91
Q94
Q104
Q109
Q111
Q126
Q136
TYPE 356



A2	A1	Q29	Q28	Q27
0	0	Off	Off	Off
0	1	Off	Off	On
1	0	On	Off	Off
1	1	On	On	On

A4	E
0	−0.05
1	−0.25

A4	Q53	
0	Off	X1
1	On	X10

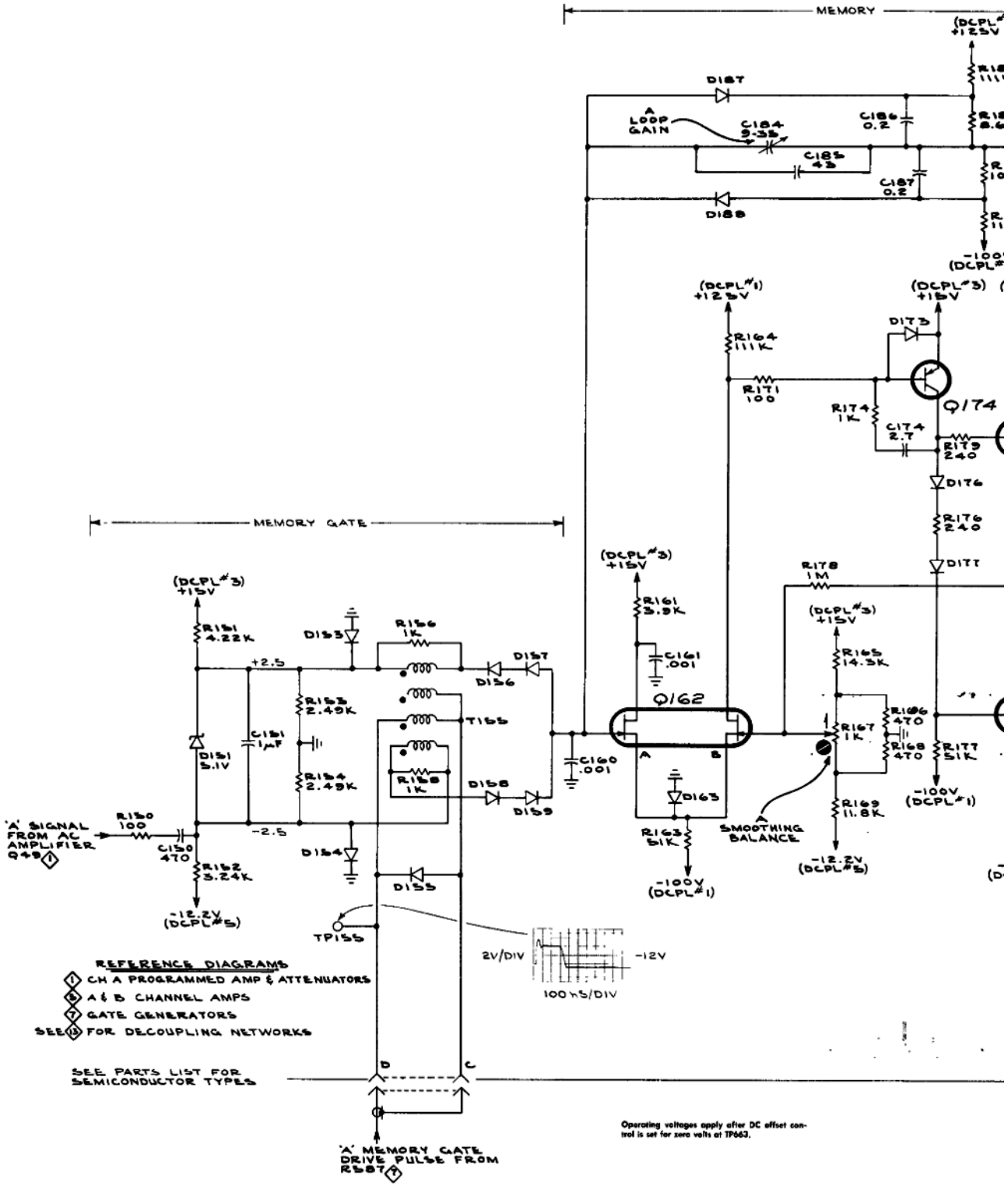
A3	A1	Q86	Q91	Q94	B=%A	C=%A
0	0	Off	Off	Off	40	80
0	1	Off	Off	On	20	40
1	0	On	Off	Off	10	20
1	1	On	On	On	4	8

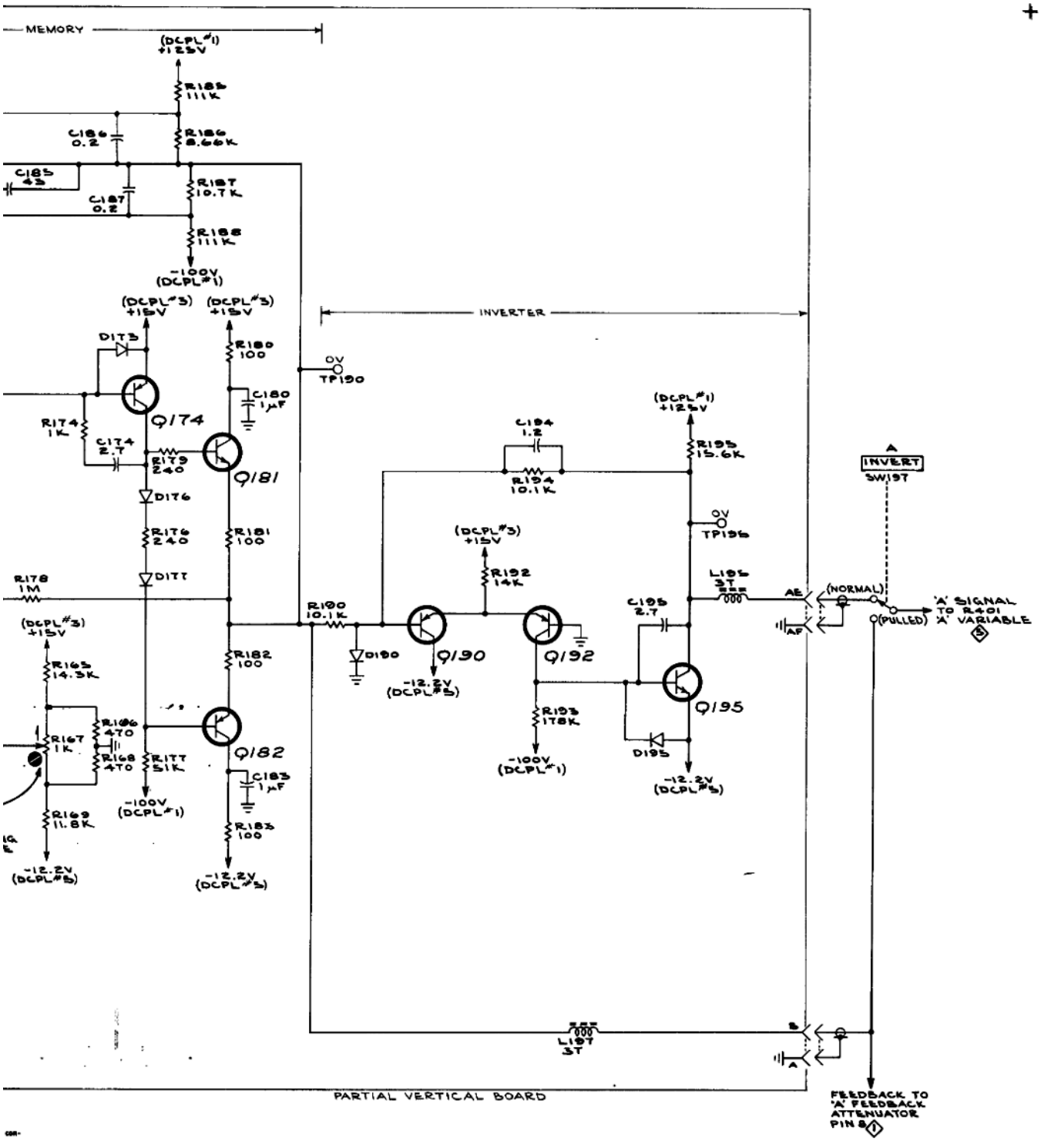
A1	E
0	−26
1	0

Units/Div	A4	A2	A1
200	0	0	0
100	0	0	1
50	0	1	0
20	0	1	1
10	1	0	1
5	1	1	0
2	1	1	1

PLN 868

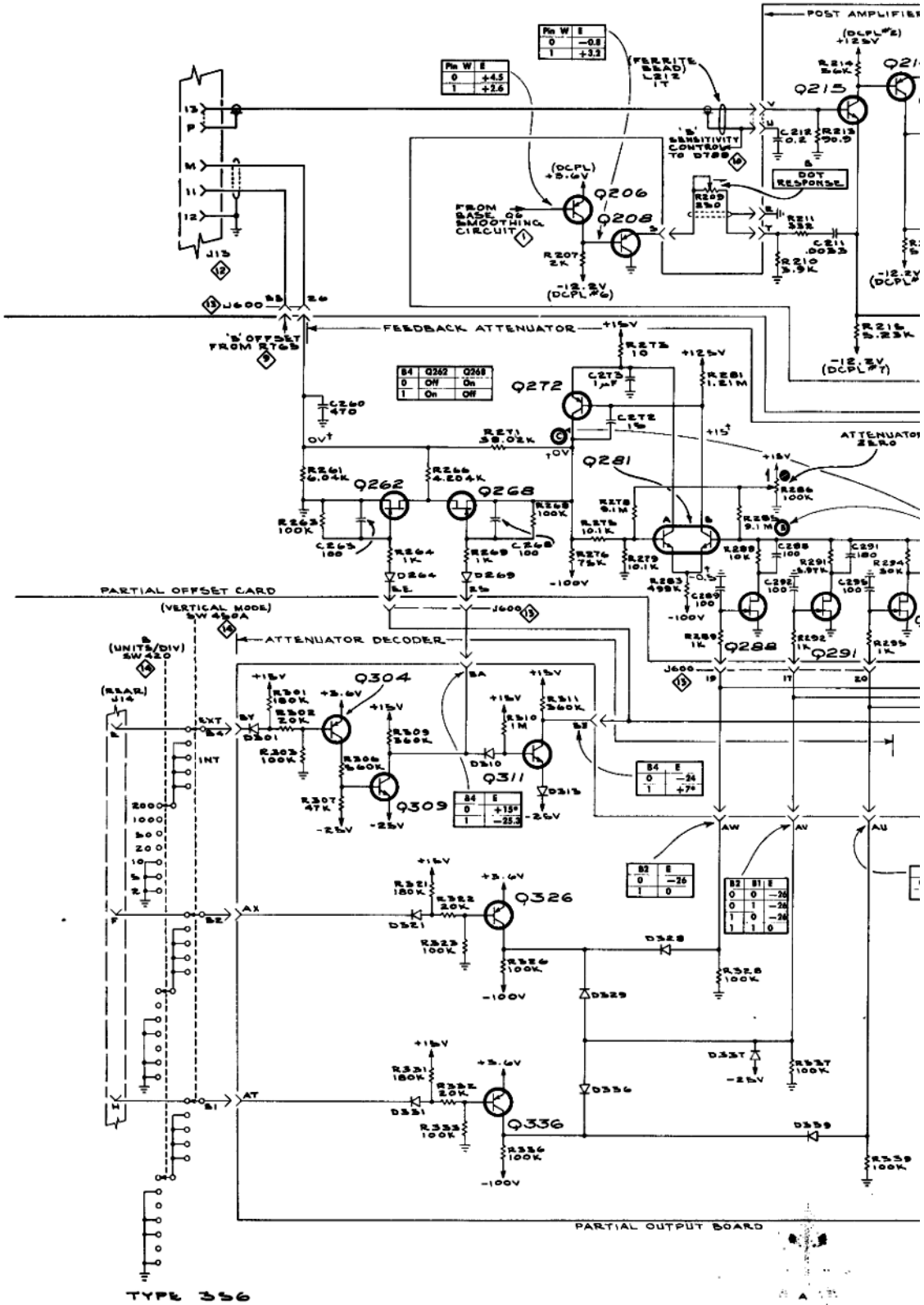
CH A PROGRAMMED AMP & ATTENUATORS 1

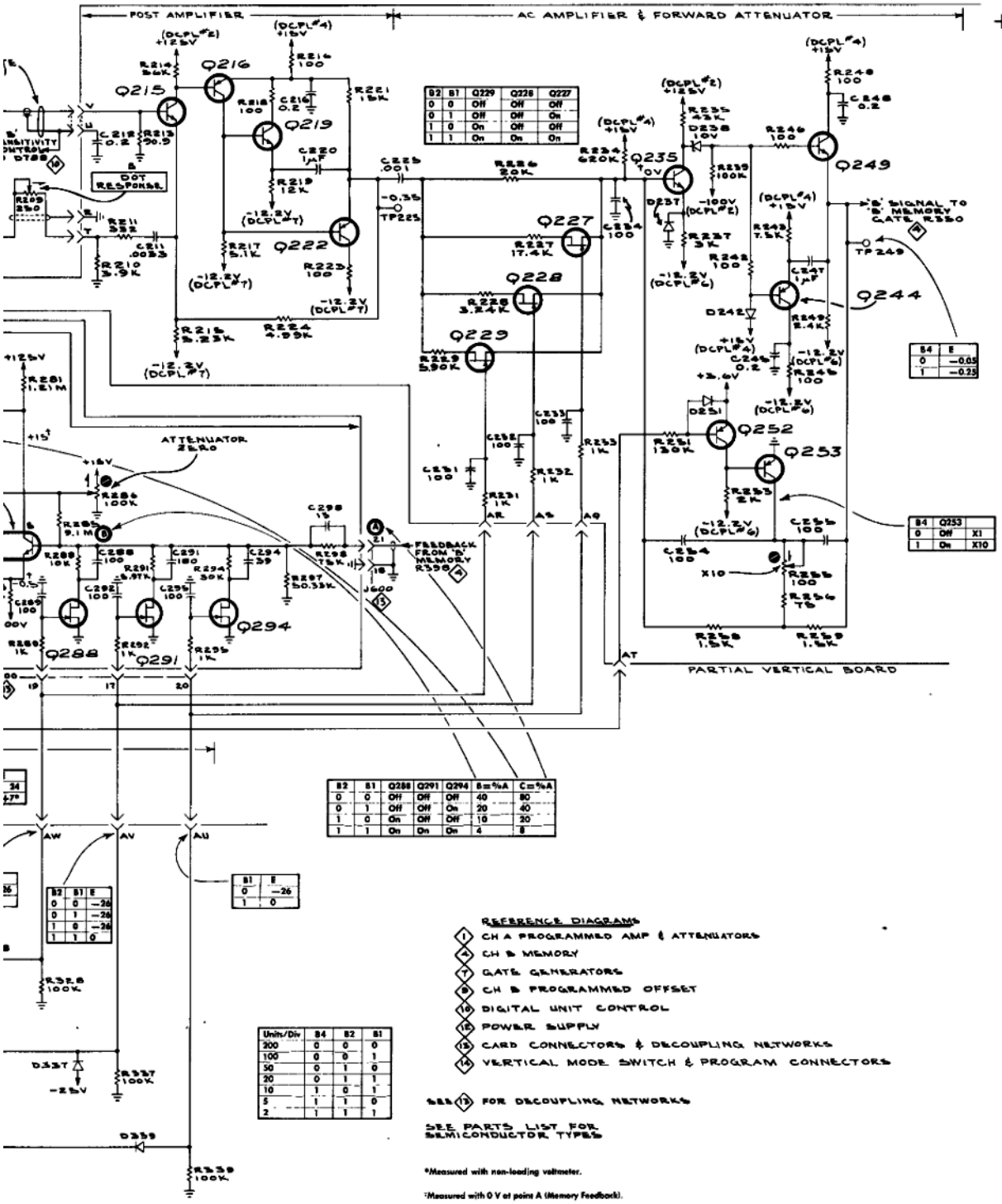

MEMORY
MEMORY GATE
D187
A LOOP GAIN
C184 5-35
C186 0.2
C185 43
C187 0.2
D188
(DCPL#1) +12.5V
(DCPL#3) +15V
R164 111K
D173
R171 100
Q174
R174 1K
C174 2.7
R179 240
D176
R176 240
D177
R178 1M
R161 3.9K
C161 .001
Q162
R165 14.3K
R166 470
R167 1K
R168 470
R177 51K
D163
R163 51K
SMOOTHING BALANCE
R169 11.8K
-100V (DCPL#1)
-12.2V (DCPL#5)
R151 4.22K
D153
R156 1K
D157
D156
+2.5
R153 2.49K
T155
C151 1μF
D151 5.1V
R154 2.49K
R158 1K
D158
D159
C160 .001
'A' SIGNAL FROM AC AMPLIFIER Q49 ◇1
R150 100
C150 470
-2.5
D164
D155
R152 3.24K
TP155
2V/DIV
-12V
100 nS/DIV
REFERENCE DIAGRAMS
◇1 CH A PROGRAMMED AMP & ATTENUATORS
◇6 A & B CHANNEL AMPS
◇7 GATE GENERATORS
SEE ◇8 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
D
C
'A' MEMORY GATE DRIVE PULSE FROM R587 ◇7
Operating voltages apply after DC offset control is set for zero volts at TP663.



CH A MEMORY 2

PLM 868


POST AMPLIFIER
FEEDBACK ATTENUATOR
ATTENUATOR DECODER
PARTIAL OFFSET CARD
PARTIAL OUTPUT BOARD
(VERTICAL MODE) SW 420A
(UNITS/DIV) SW 420
(REAR) J14
FERRITE BEAD L212
'B' SENSITIVITY CONTROL TO D788
DOT RESPONSE
FROM BASE OF SMOOTHING CIRCUIT
'B' OFFSET FROM D765
ATTENUATOR ZERO
Q206
Q208
Q215
Q272
Q281
Q262
Q268
Q282
Q291
Q304
Q309
Q311
Q326
Q336
J600
J13
D264
D269
D301
D310
D312
D321
D328
D329
D331
D336
D337
D339
INT
EXT
AX
AT
AW
AV
AU
TYPE 356



B2	B1	Q229	Q228	Q227
0	0	Off	Off	Off
0	1	Off	Off	On
1	0	On	Off	Off
1	1	On	On	On

B4	E
0	−0.05
1	−0.25

B4	Q253	
0	Off	X1
1	On	X10

B2	B1	Q288	Q291	Q294	B=%A	C=%A
0	0	Off	Off	Off	40	80
0	1	Off	Off	On	20	40
1	0	On	Off	Off	10	20
1	1	On	On	On	4	8

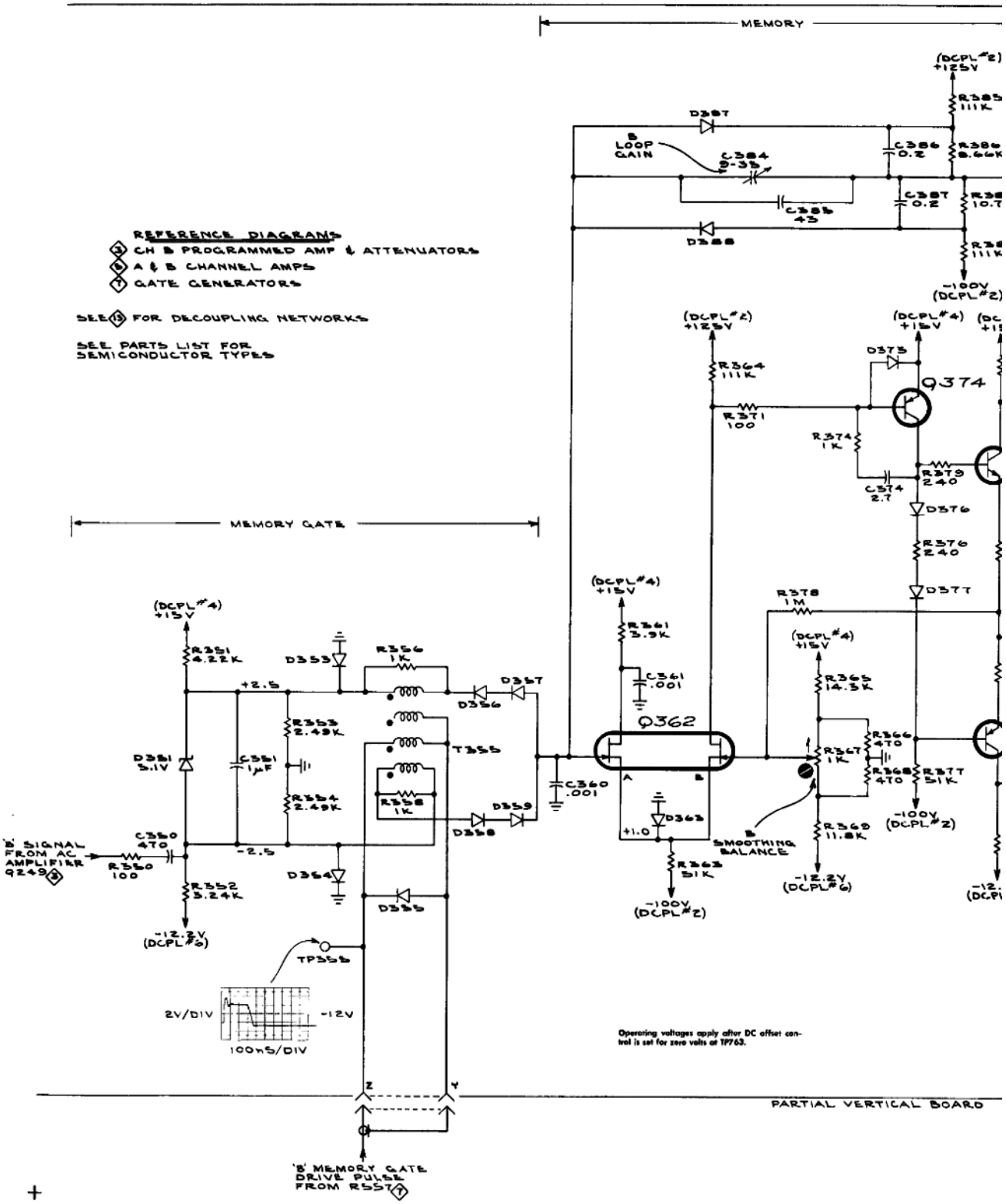
B2	B1	E
0	0	−26
0	1	−26
1	0	−26
1	1	0

B1	E
0	−26
1	0

Units/Div	B4	B2	B1
200	0	0	0
100	0	0	1
50	0	1	0
20	0	1	1
10	1	0	1
5	1	1	0
2	1	1	1

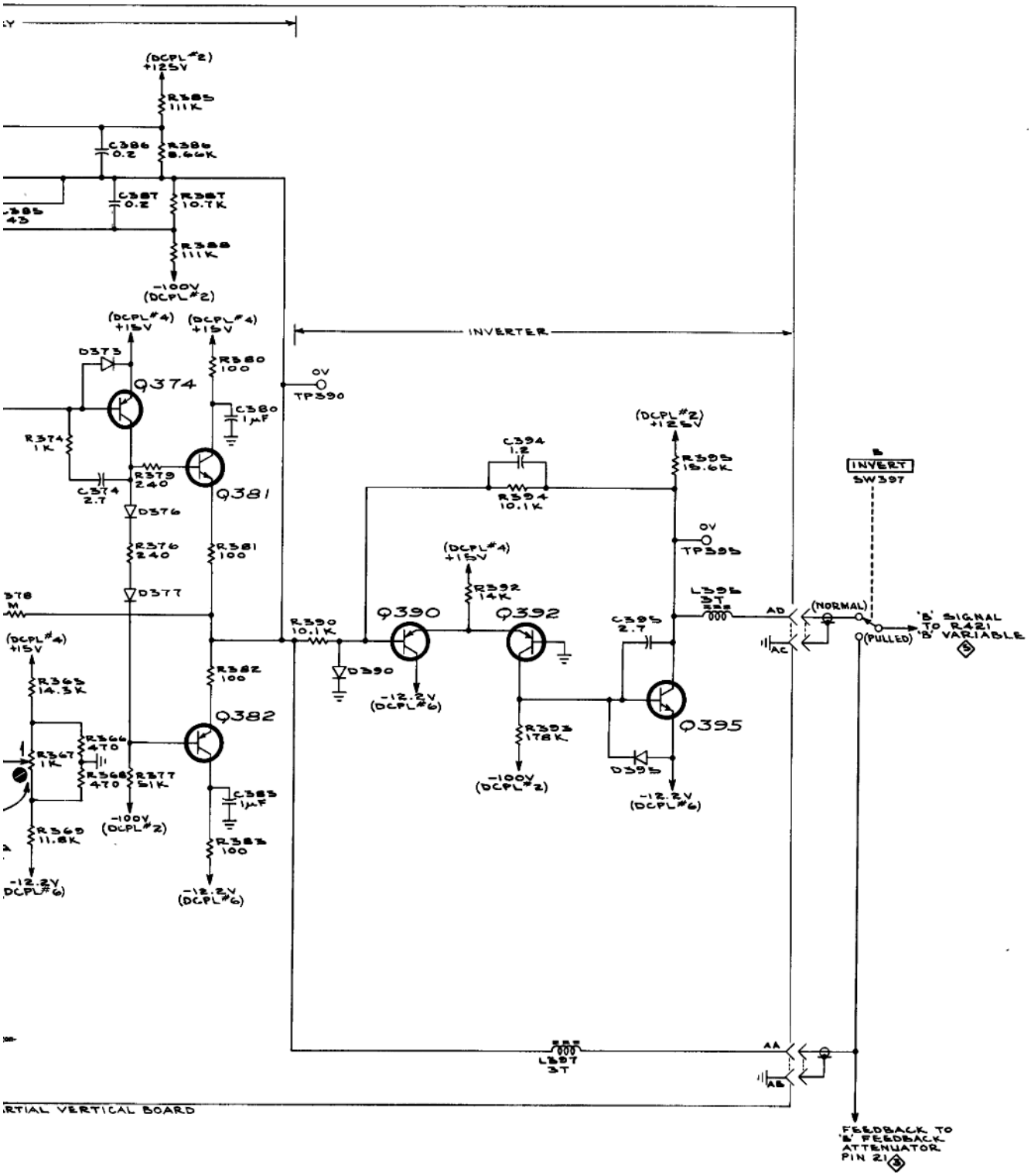
PLM 868

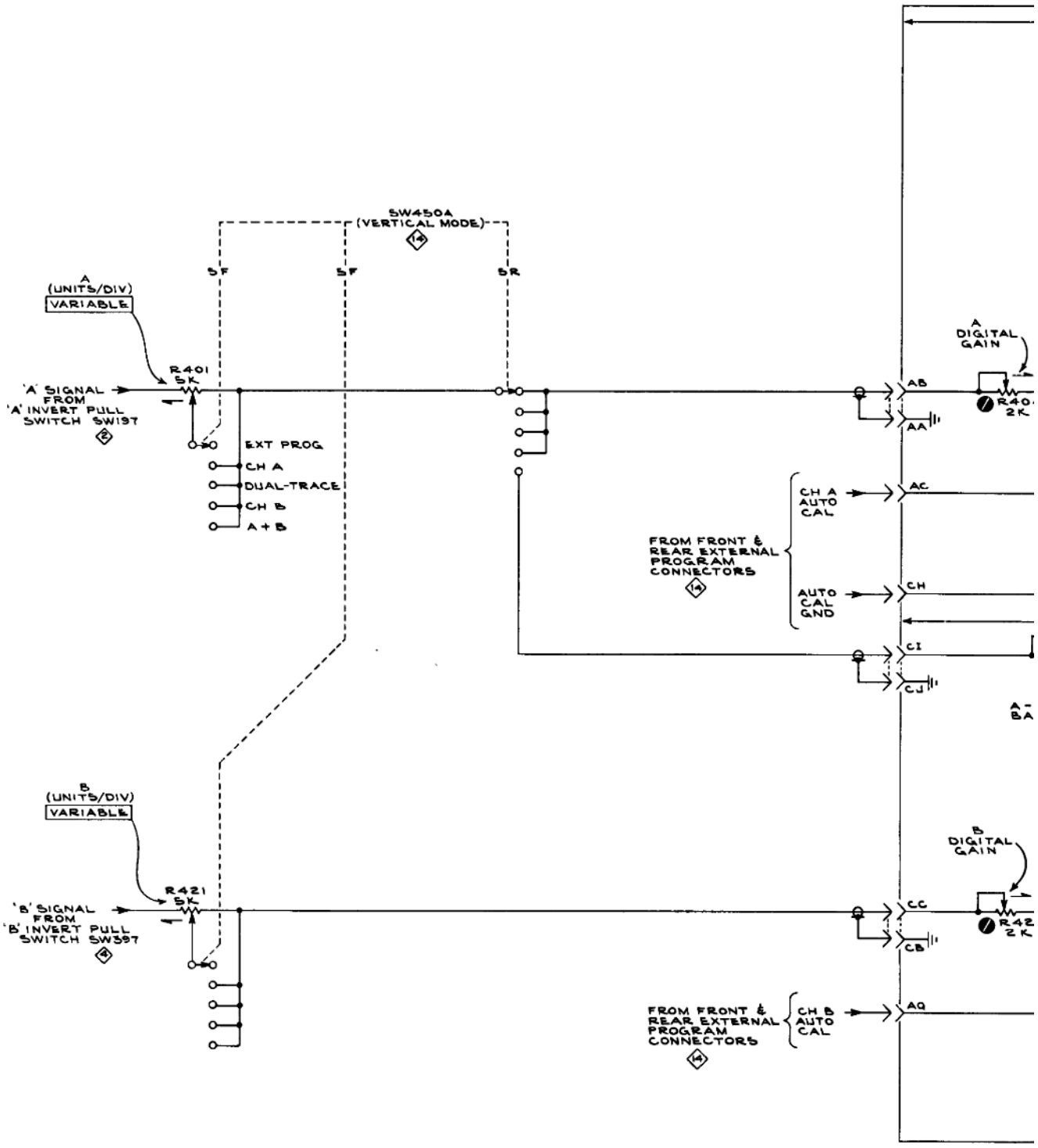
CH B PROGRAMMED AMP & ATTENUATORS 3

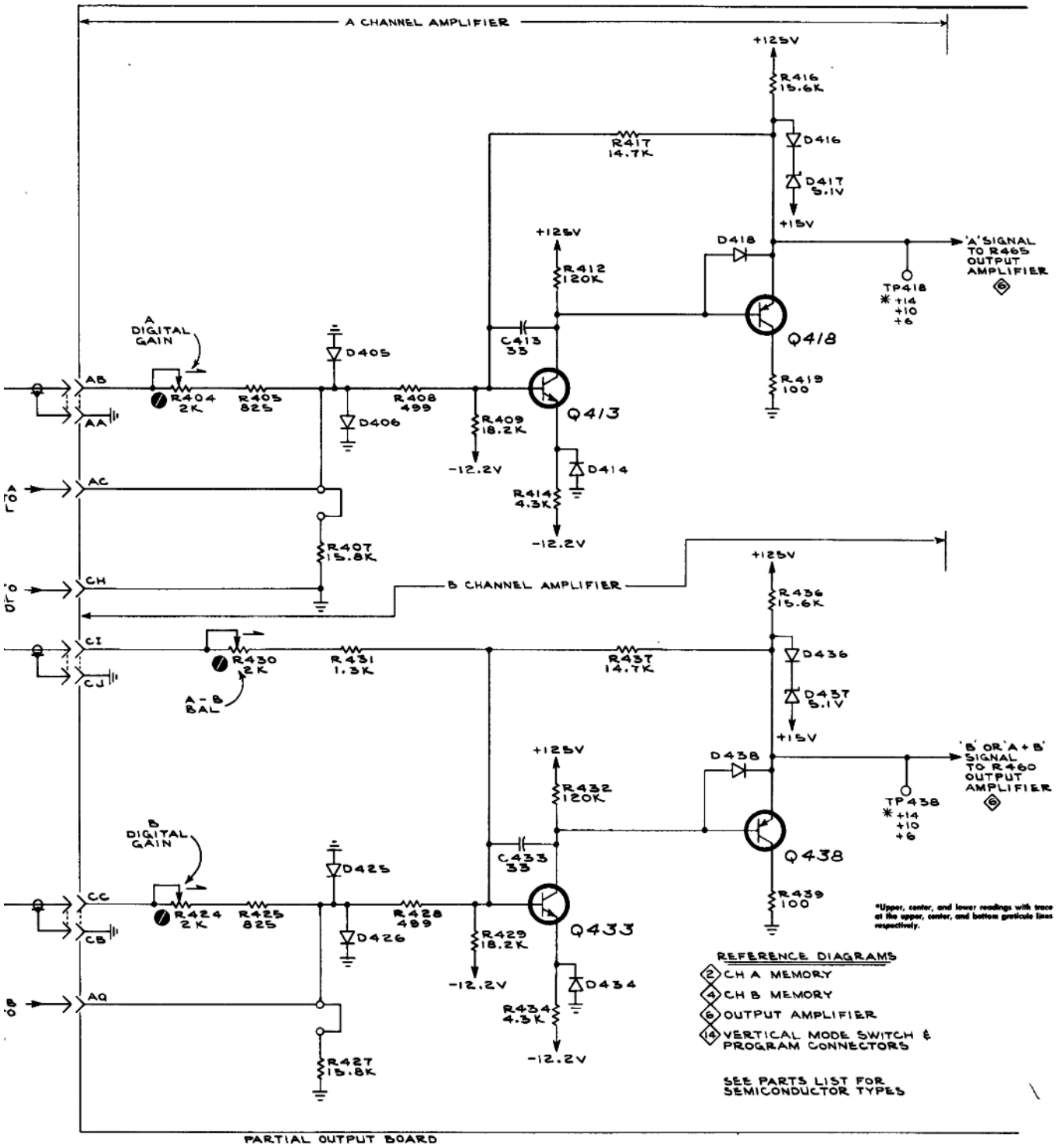

MEMORY
MEMORY GATE
REFERENCE DIAGRAMS
3 CH B PROGRAMMED AMP & ATTENUATORS
6 A & B CHANNEL AMPS
7 GATE GENERATORS
SEE 13 FOR DECOUPLING NETWORKS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
B LOOP GAIN
C384 9-35
C385 43
C386 0.2
C387 0.2
D387
D388
R385 111K
R386 8.66K
R388 10.7
R389 111K
-100V (DCPL#2)
(DCPL#2) +125V
(DCPL#4) +15V
R364 111K
D373
Q374
R371 100
R374 1K
R379 240
C374 2.7
D376
R376 240
D377
R378 1M
R361 3.9K
C361 .001
Q362
R365 14.5K
R366 470
R367 1K
R368 470
R377 51K
-100V (DCPL#2)
D363
+1.0
R369 11.8K
-12.2V (DCPL#6)
R363 51K
-100V (DCPL#2)
B SMOOTHING BALANCE
R351 4.22K
D353
R356 1K
D357
D356
+2.5
R353 2.49K
T355
D351 5.1V
C351 1μF
R354 2.49K
R358 1K
D359
D358
C360 .001
'B' SIGNAL FROM AC AMPLIFIER 9249 3
C350 470
R350 100
-2.5
D364
D355
R352 3.24K
-12.2V (DCPL#6)
TP356
2V/DIV
-12V
100nS/DIV
Z
Y
'B' MEMORY GATE DRIVE PULSE FROM R557 7
Operating voltages apply after DC offset control is set for zero volts at TP763.
PARTIAL VERTICAL BOARD

TYPE 356

A


(DCPL #2) +125V
R385 111K
C386 0.2
R386 8.66K
C387 0.2
R387 10.7K
R388 111K
-100V (DCPL #2)
(DCPL #4) +15V
(DCPL #4) +15V
INVERTER
D373
R380 100
Q374
0V
TP390
C380 1μF
R374 1K
R379 240
C374 2.7
Q381
D376
R376 240
R381 100
D377
R390 10.1K
Q390
Q392
D390
-12.2V (DCPL #6)
C394 1.2
R394 10.1K
(DCPL #2) +125V
R395 15.6K
0V
TP395
(DCPL #4) +15V
R392 14K
L395 3T
C395 2.7
AD
AC
(NORMAL)
(PULLED)
B INVERT SW397
'B' SIGNAL TO R421 'B' VARIABLE
5
(DCPL #4) +15V
R365 14.3K
R382 100
Q382
R366 470
R367 1K
R368 470
R377 51K
C383 1μF
R369 11.8K
-100V (DCPL #2)
R383 100
-12.2V (DCPL #6)
-12.2V (DCPL #6)
R393 178K
-100V (DCPL #2)
Q395
D395
-12.2V (DCPL #6)
L397 3T
AA
AB
FEEDBACK TO 'B' FEEDBACK ATTENUATOR PIN 21
3
RTIAL VERTICAL BOARD
A
CH B MEMORY
4
PLM 868

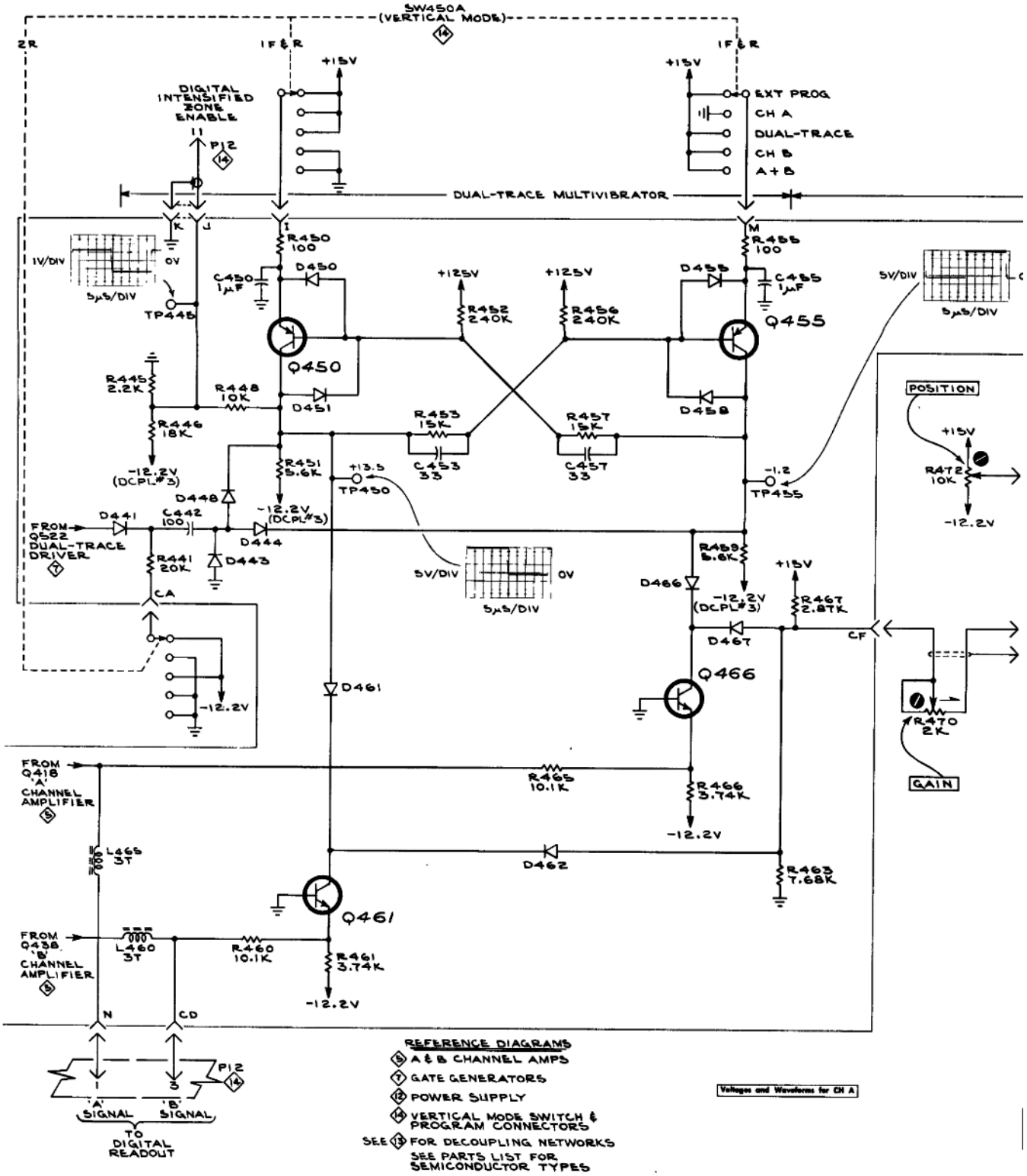

SW450A
(VERTICAL MODE)
14
5F
5F
5R
A
(UNITS/DIV)
VARIABLE
R401
5K
'A' SIGNAL
FROM
'A' INVERT PULL
SWITCH SW197
2
EXT PROG
CH A
DUAL-TRACE
CH B
A+B
A
DIGITAL
GAIN
AB
AA
R40
2K
CH A
AUTO
CAL
AC
FROM FRONT &
REAR EXTERNAL
PROGRAM
CONNECTORS
14
AUTO
CAL
GND
CH
CI
CJ
A-
BA
B
(UNITS/DIV)
VARIABLE
R421
5K
'B' SIGNAL
FROM
'B' INVERT PULL
SWITCH SW397
4
B
DIGITAL
GAIN
CC
CB
R42
2K
FROM FRONT &
REAR EXTERNAL
PROGRAM
CONNECTORS
14
CH B
AUTO
CAL
AQ



A

A & B CHANNEL AMPS ⑤

PLM 868



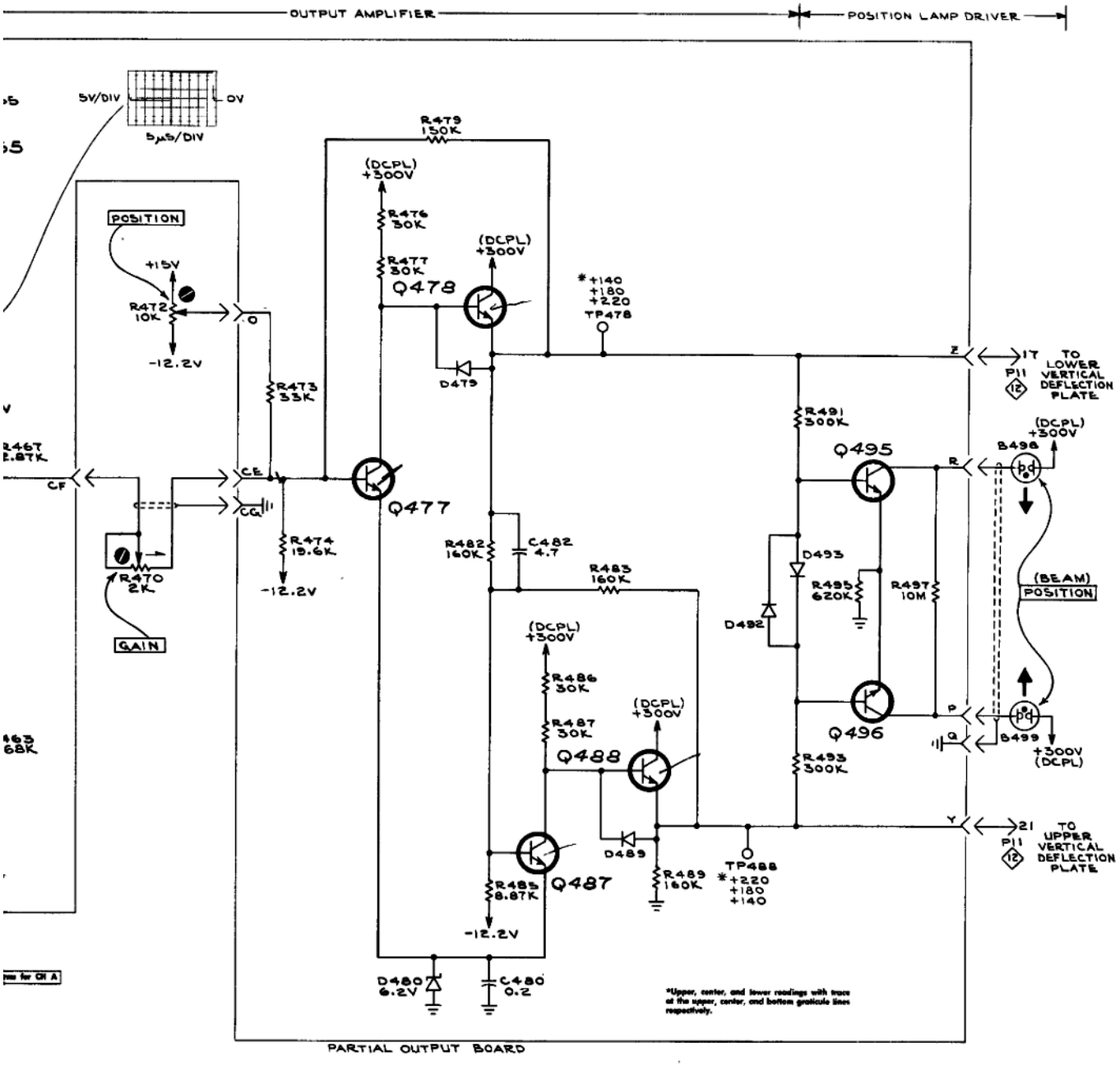
REFERENCE DIAGRAMS

- 5 A & B CHANNEL AMPS
- 7 GATE GENERATORS
- 12 POWER SUPPLY
- 14 VERTICAL MODE SWITCH & PROGRAM CONNECTORS

SEE 13 FOR DECOUPLING NETWORKS

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

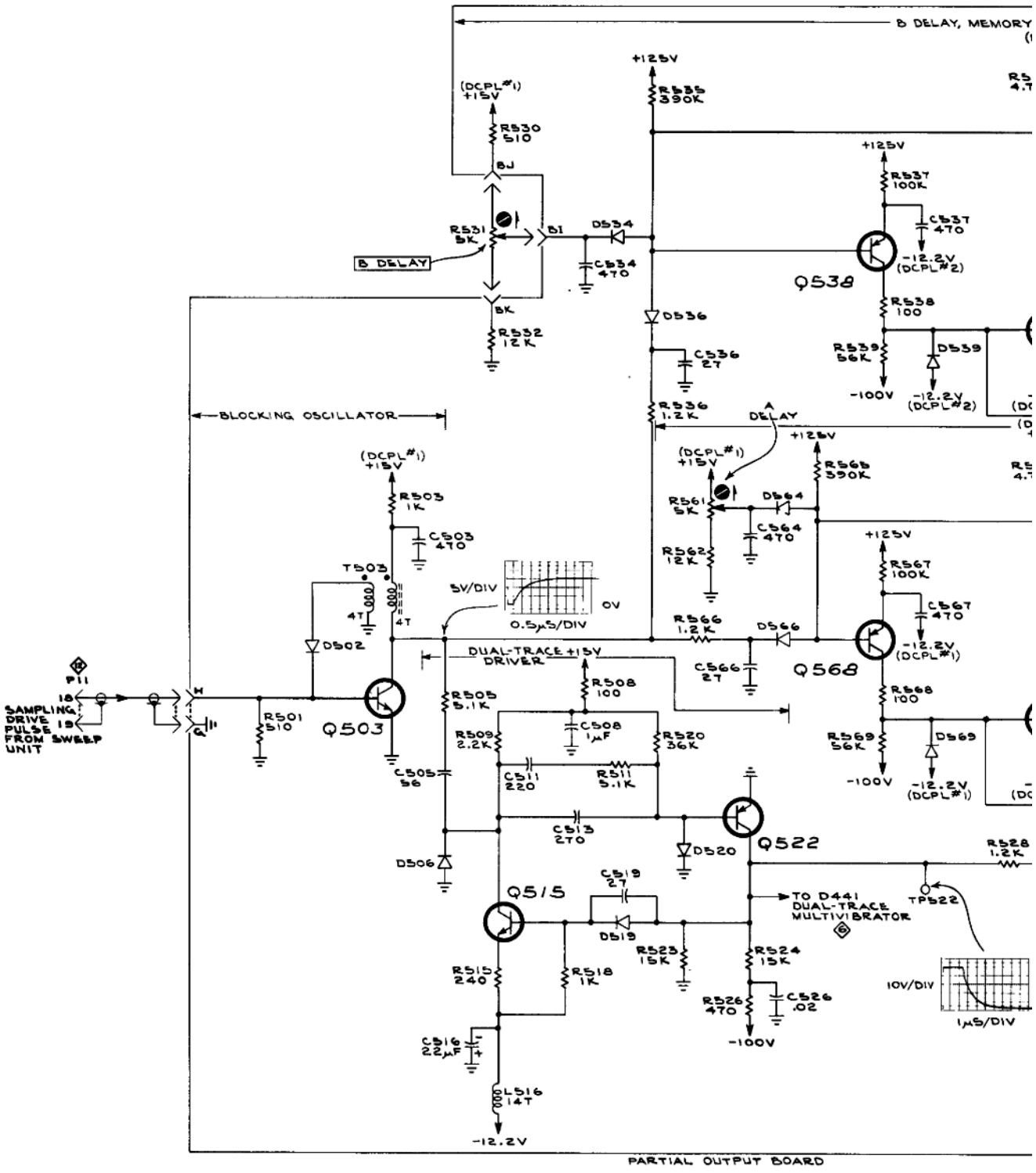
Voltages and Waveforms for CH A

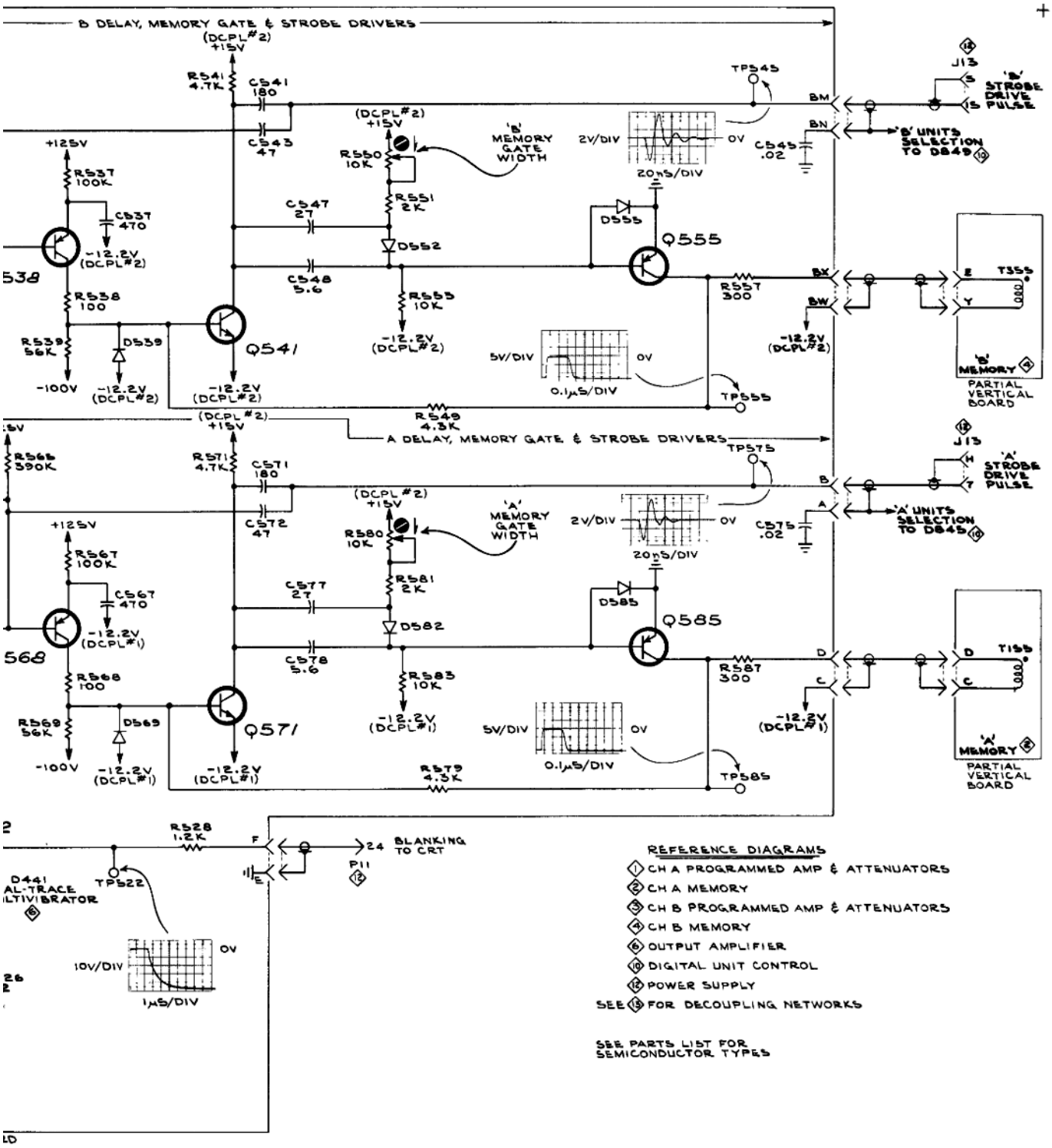


A

OUTPUT AMPLIFIER ⑥

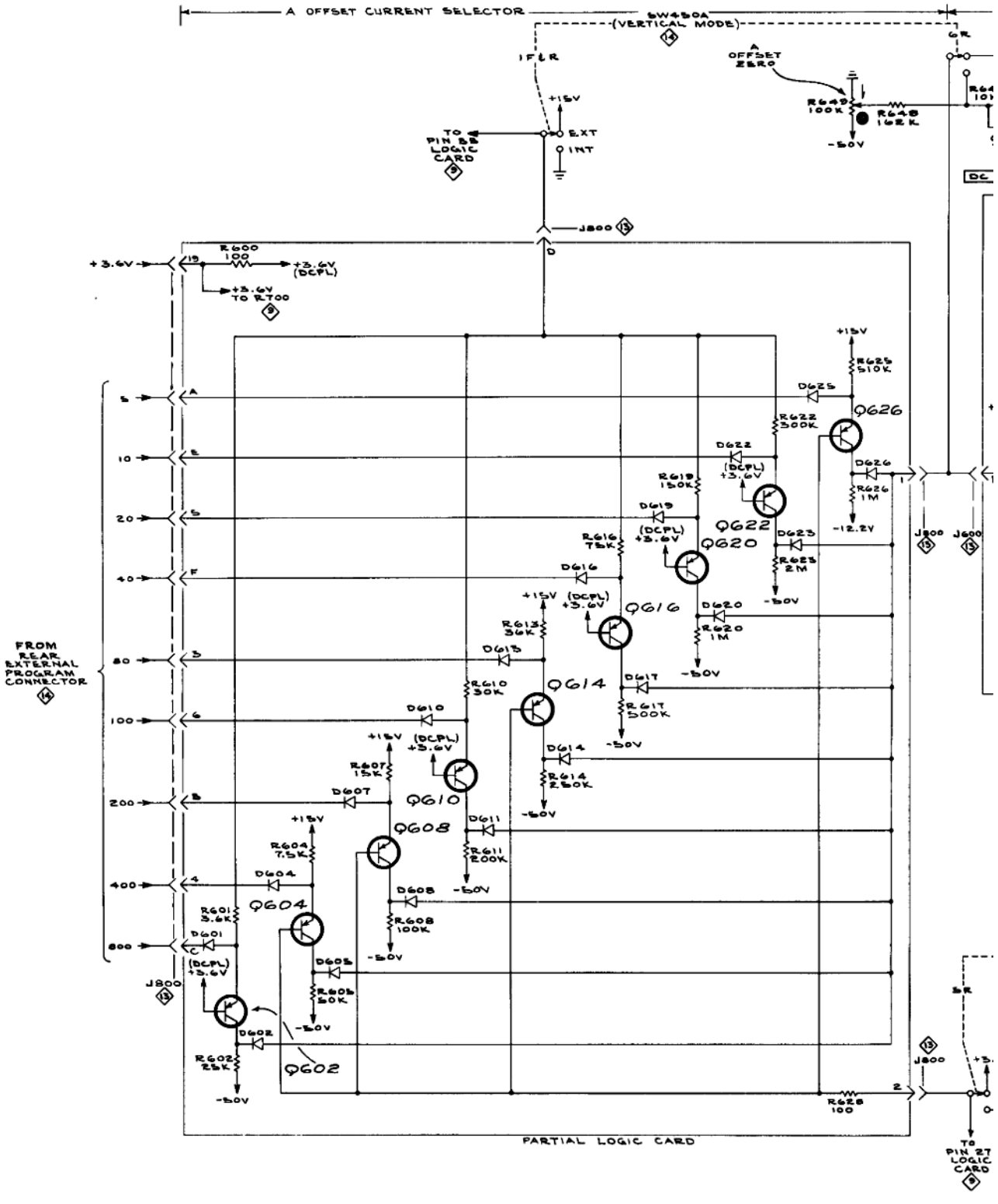
PLM 868

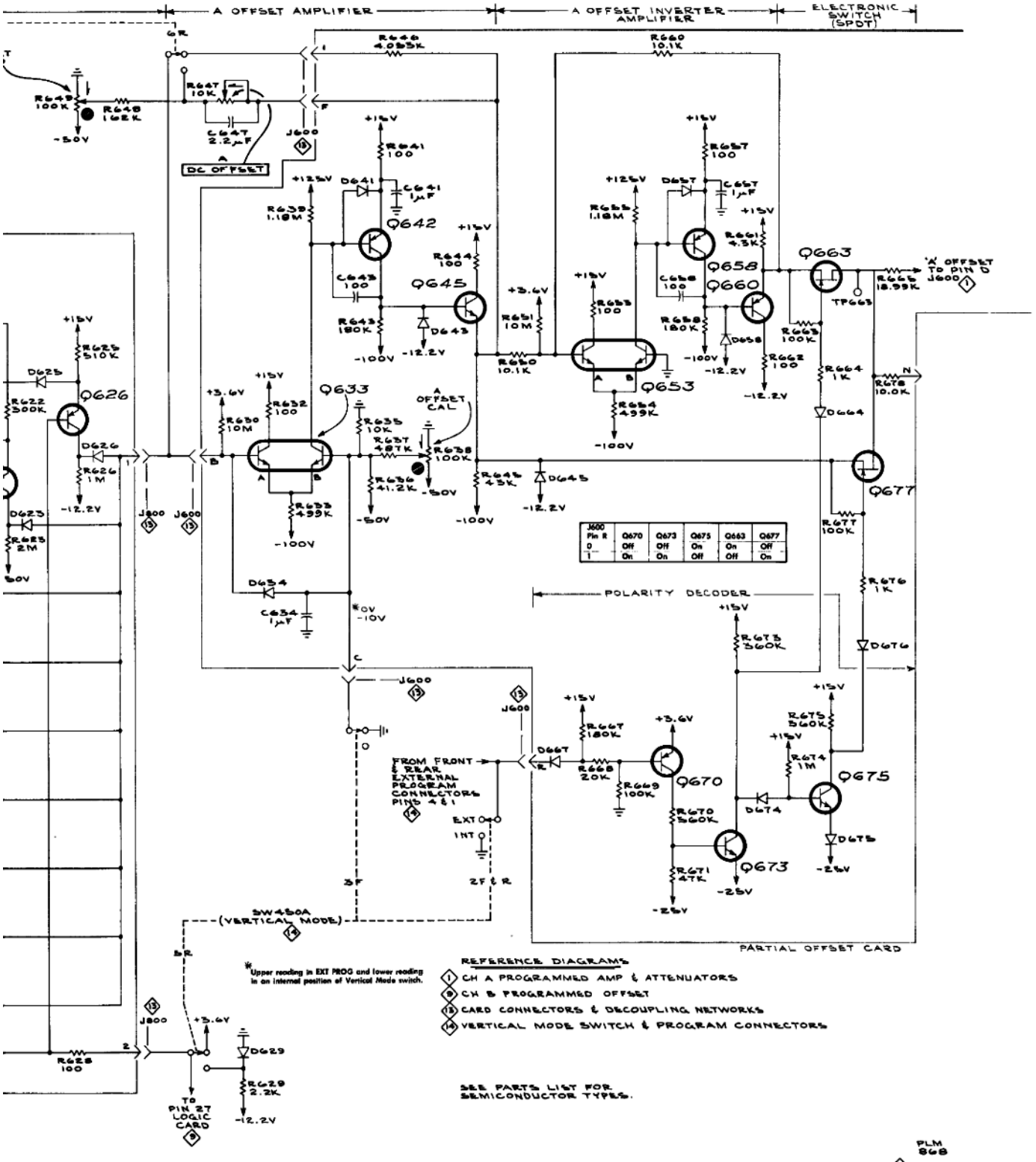

B DELAY, MEMORY
+125V
R535 390K
(DCPL#1) +15V
R530 510
BJ
R531 5K
B1
D534
B DELAY
C534 470
BK
R532 12K
D536
C536 27
R536 1.2K
Q538
R537 100K
C537 470
-12.2V (DCPL#2)
R538 100
R539 56K
D539
-100V
-12.2V (DCPL#2)
BLOCKING OSCILLATOR
A DELAY
(DCPL#1) +15V
R503 1K
C503 470
T503
4T
4T
D502
5V/DIV
0V
0.5μS/DIV
R561 5K
D564
C564 470
R562 12K
R565 390K
R567 100K
C567 470
R566 1.2K
D566
C566 27
Q568
R568 100
R569 56K
D569
-100V
-12.2V (DCPL#1)
DUAL-TRACE +15V DRIVER
P11
18
19
SAMPLING DRIVE PULSE FROM SWEEP UNIT
H
G
R501 510
Q503
R505 5.1K
R508 100
C508 1μF
R509 2.2K
R520 36K
C505 56
C511 220
R511 5.1K
C513 270
D506
Q522
D520
R528 1.2K
C519 27
Q515
D519
TO D441 DUAL-TRACE MULTIVIBRATOR
TP522
10V/DIV
1μS/DIV
R523 15K
R524 15K
R515 240
R518 1K
R526 470
C526 .02
-100V
C516 22μF
L516 14T
-12.2V
PARTIAL OUTPUT BOARD



PLM 868

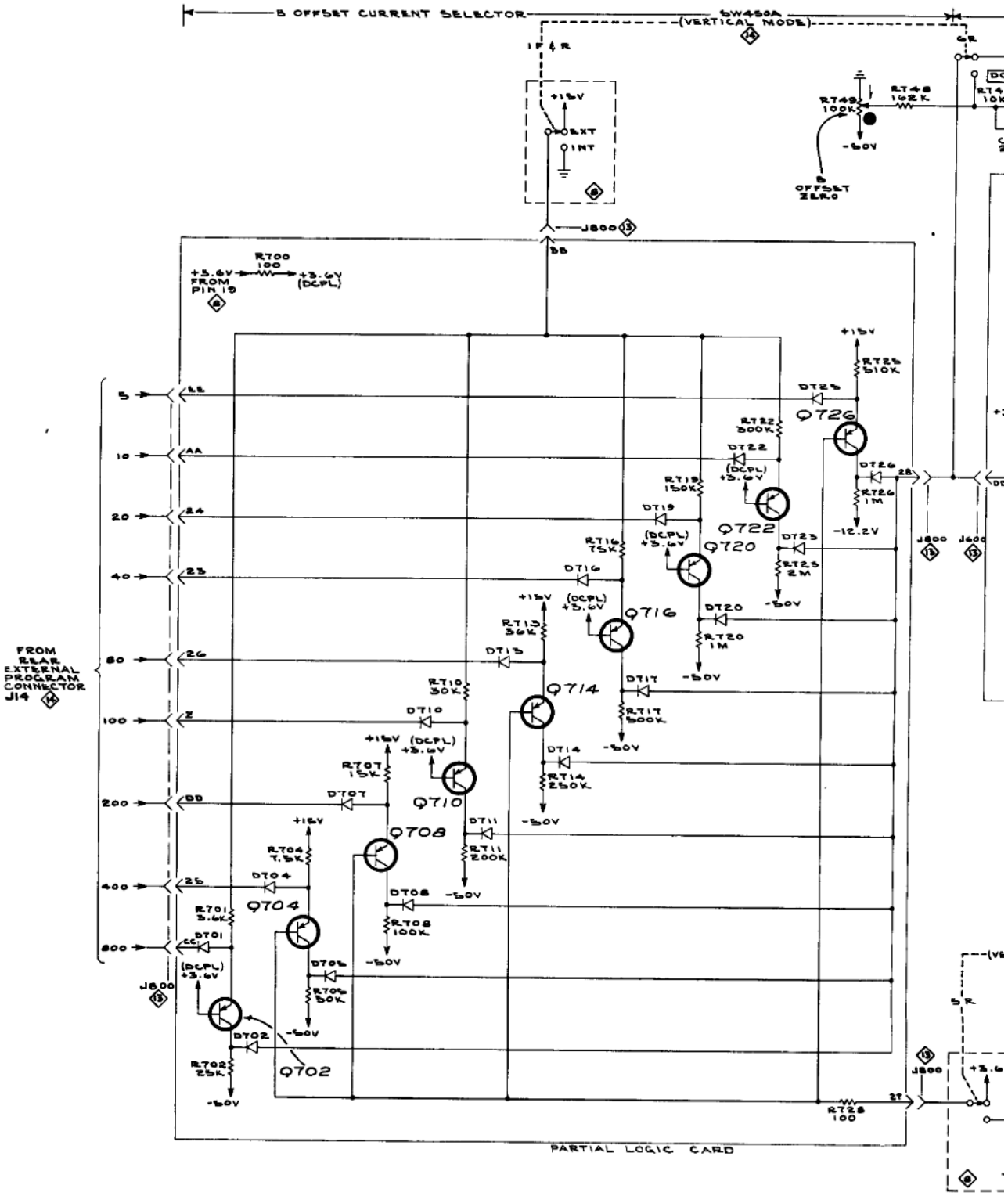
GATE GENERATORS 7


A OFFSET CURRENT SELECTOR
SW450A (VERTICAL MODE)
A OFFSET ZERO
R649 100K
R648 162K
-50V
IF & R
+15V
EXT
INT
TO PIN 58 LOGIC CARD
J800
+3.6V
R600 100
+3.6V (DCPL)
+3.6V TO RT00
FROM REAR EXTERNAL PROGRAM CONNECTOR
PARTIAL LOGIC CARD
Q626
Q622
Q620
Q616
Q614
Q610
Q608
Q604
Q602
D625
D622
D619
D616
D613
D610
D607
D604
D601
D602
D605
D608
D611
D614
D617
D620
D623
D626
R625 510K
R622 500K
R619 150K
R616 75K
R613 36K
R610 30K
R607 15K
R604 7.5K
R601 3.6K
R602 25K
R605 50K
R608 100K
R611 200K
R614 250K
R617 500K
R620 1M
R623 2M
R626 1M
R628 100
-12.2V
TO PIN 27 LOGIC CARD
TYPE 356

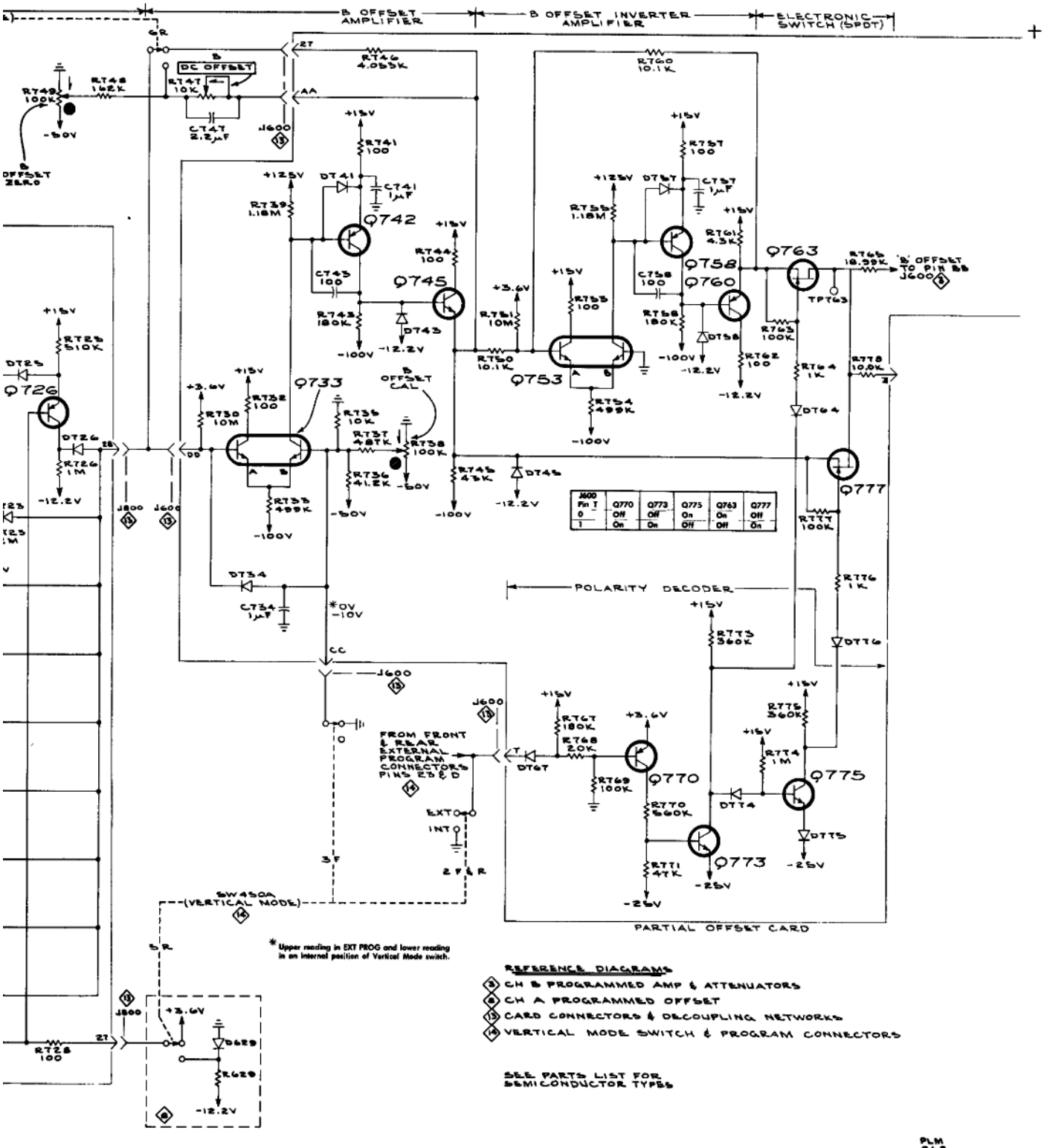


PLM 868

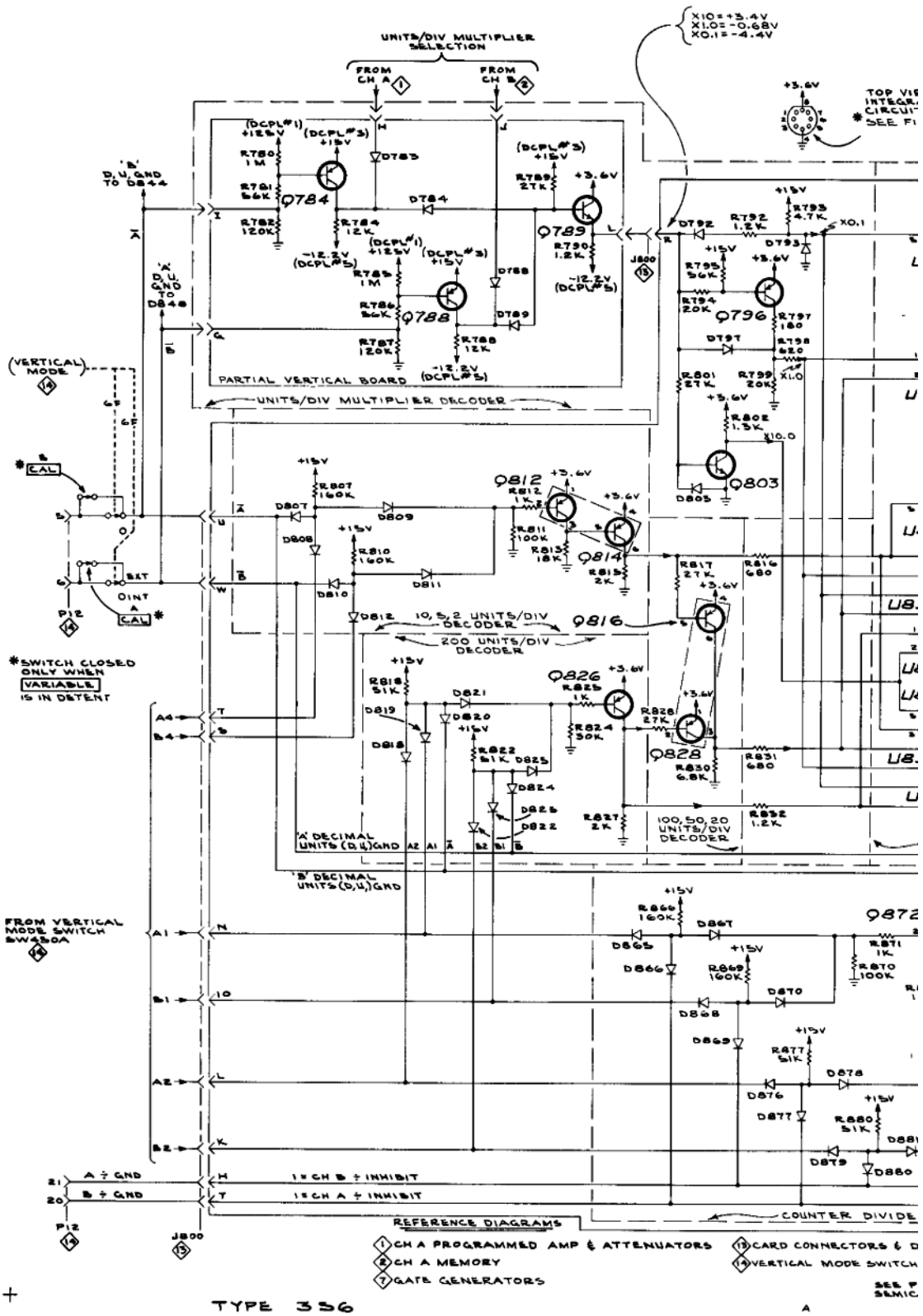
CH A PROGRAMMED OFFSET 8


B OFFSET CURRENT SELECTOR
SW450A
(VERTICAL MODE)
1 F & R
+15V
EXT
INT
R749 100K
-50V
B OFFSET ZERO
R748 1.02K
J800
+3.6V FROM PIN 19
R700 100
+3.6V (DCPL)
FROM REAR EXTERNAL PROGRAM CONNECTOR J14
5
10
20
40
80
100
200
400
800
Q726
Q722
Q720
Q716
Q714
Q710
Q708
Q704
Q702
R725 510K
R722 500K
R719 150K
R716 75K
R713 36K
R710 30K
R707 15K
R704 7.5K
R701 3.6K
R726 1M
R723 2M
R720 1M
R717 500K
R714 250K
R711 200K
R708 100K
R705 50K
R702 25K
-12.2V
(DCPL) +3.6V
R728 100
PARTIAL LOGIC CARD

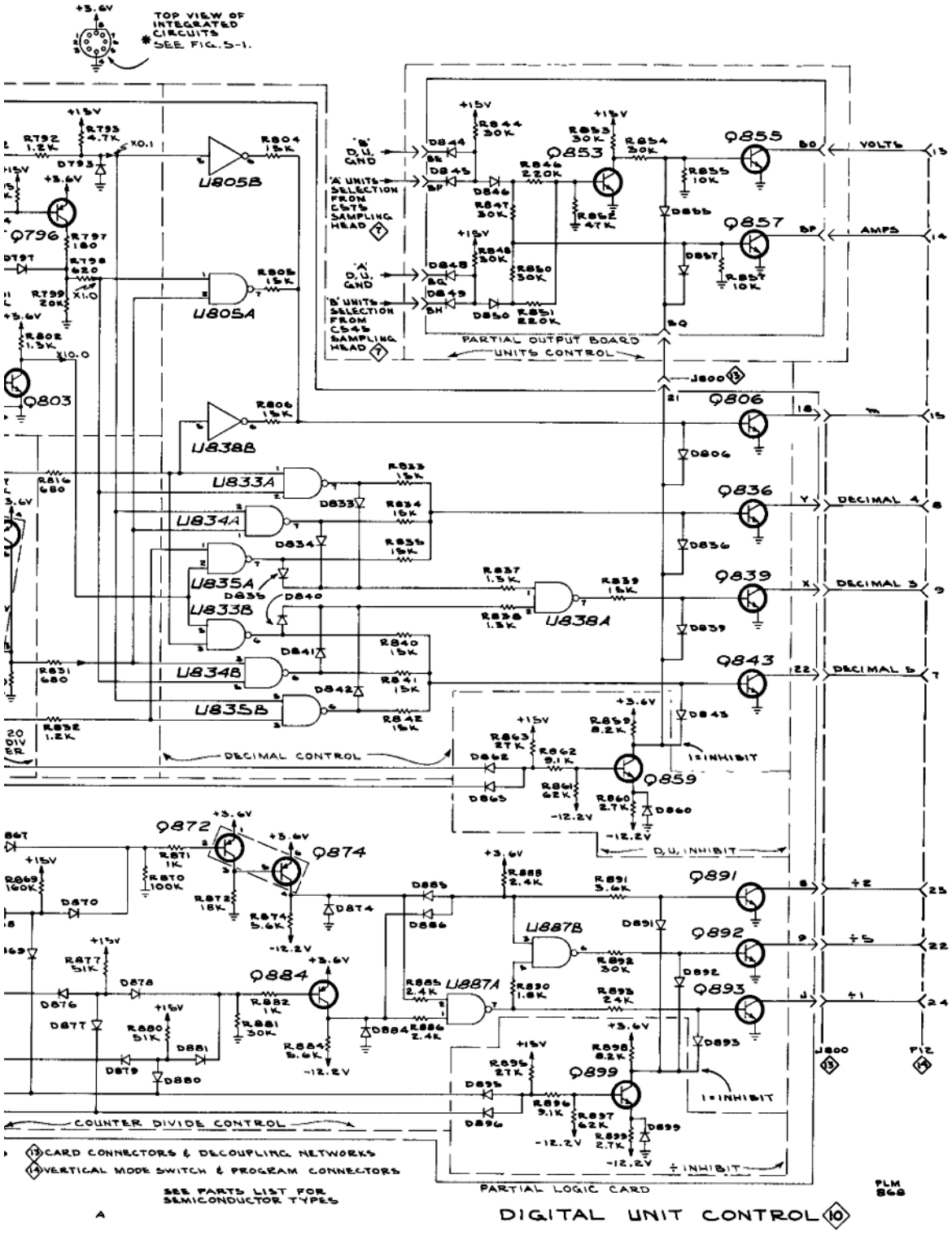
TYPE 356



CH B PROGRAMMED OFFSET 9


UNITS/DIV MULTIPLIER SELECTION
FROM CH A
FROM CH B
X10 = +3.4V
X1.0 = -0.68V
X0.1 = -4.4V
PARTIAL VERTICAL BOARD
UNITS/DIV MULTIPLIER DECODER
(VERTICAL) MODE
*SWITCH CLOSED ONLY WHEN VARIABLE IS IN DETENT
10, 5, 2 UNITS/DIV DECODER
200 UNITS/DIV DECODER
100, 50, 20 UNITS/DIV DECODER
'A' DECIMAL UNITS (D,U) GND
'B' DECIMAL UNITS (D,U) GND
FROM VERTICAL MODE SWITCH SW450A
A ÷ GND
B ÷ GND
1 = CH B ÷ INHIBIT
1 = CH A ÷ INHIBIT
COUNTER DIVIDE
REFERENCE DIAGRAMS
CH A PROGRAMMED AMP & ATTENUATORS
CH A MEMORY
GATE GENERATORS
CARD CONNECTORS & D
VERTICAL MODE SWITCH

TYPE 356



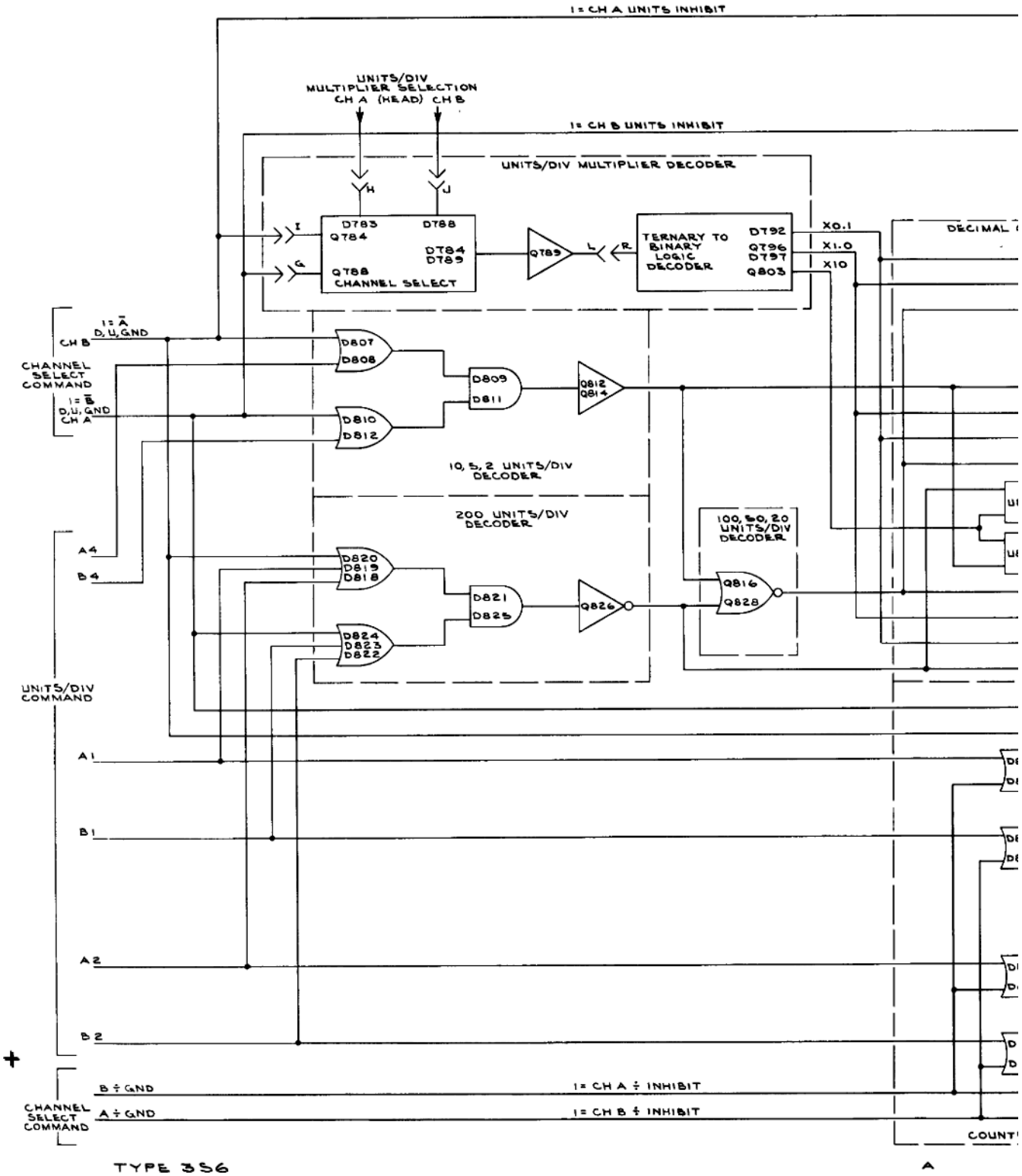
(13) CARD CONNECTORS & DECOUPLING NETWORKS

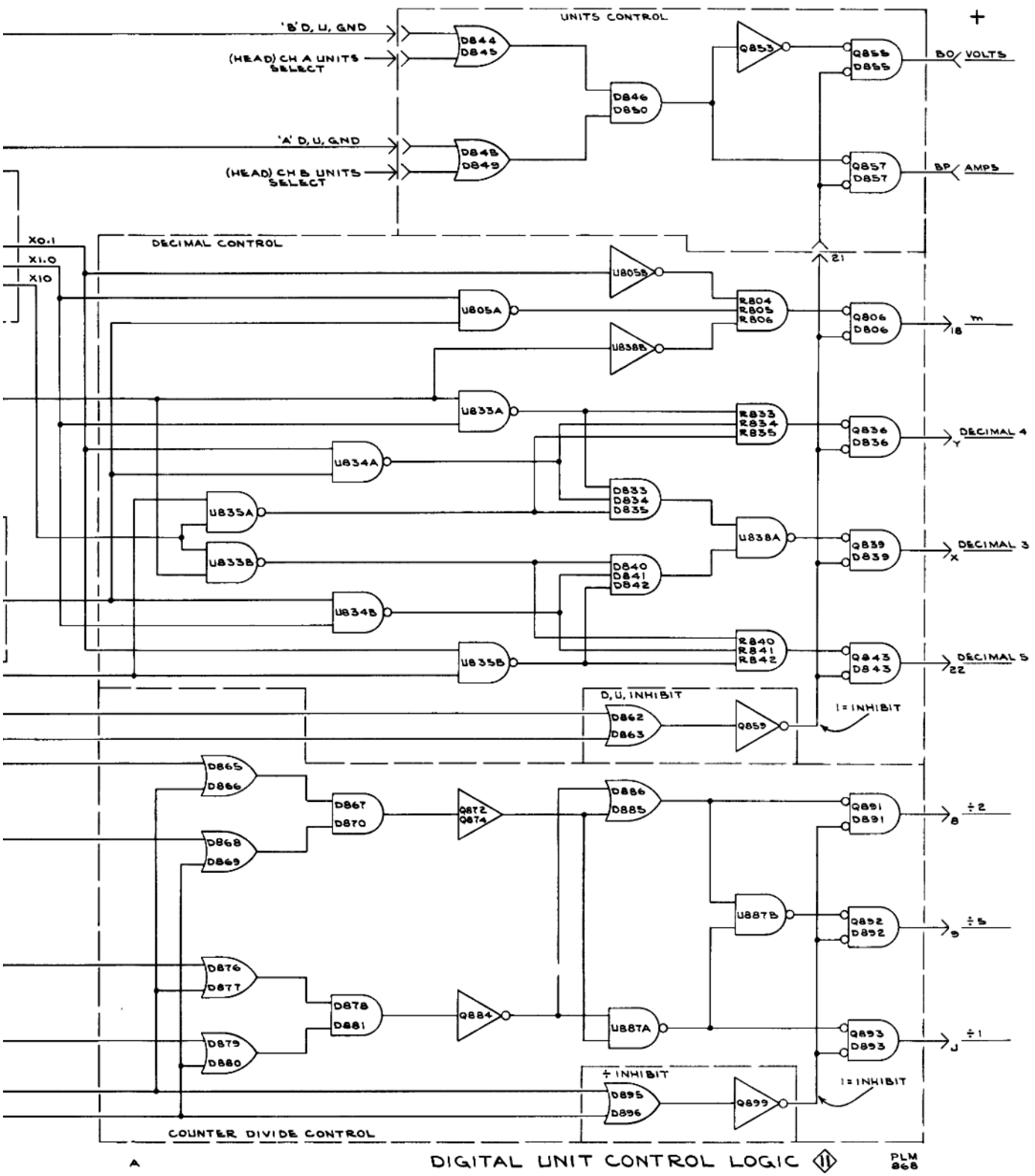
(14) VERTICAL MODE SWITCH & PROGRAM CONNECTORS

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

PLM 868

DIGITAL UNIT CONTROL (10)

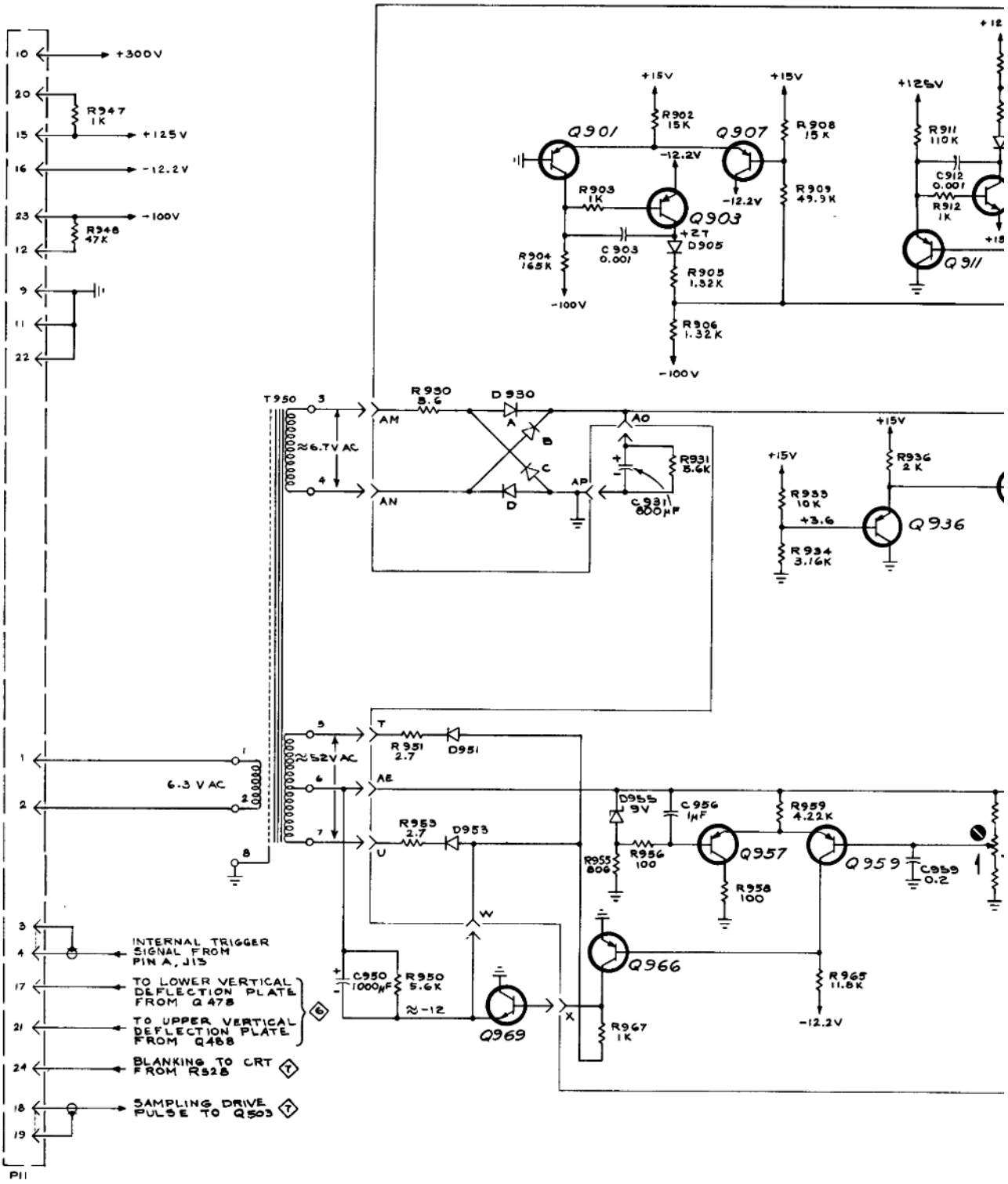

1 = CH A UNITS INHIBIT
UNITS/DIV MULTIPLIER SELECTION CH A (HEAD) CH B
1 = CH B UNITS INHIBIT
UNITS/DIV MULTIPLIER DECODER
H
J
I
G
D783
Q784
D788
D784
D789
Q788 CHANNEL SELECT
Q789
L
R
TERNARY TO BINARY LOGIC DECODER
D792
Q796
D797
Q803
X0.1
X1.0
X10
DECIMAL
1 = Ā D, U, GND CH B
CHANNEL SELECT COMMAND
1 = B̄ D, U, GND CH A
D807
D808
D809
D811
Q812
Q814
D810
D812
10, 5, 2 UNITS/DIV DECODER
200 UNITS/DIV DECODER
100, 50, 20 UNITS/DIV DECODER
A4
B4
D820
D819
D818
D821
D825
Q826
Q816
Q828
D824
D823
D822
UNITS/DIV COMMAND
A1
B1
A2
B2
+
B ÷ GND
A ÷ GND
CHANNEL SELECT COMMAND
1 = CH A ÷ INHIBIT
1 = CH B ÷ INHIBIT
COUNT
TYPE 356
A



A

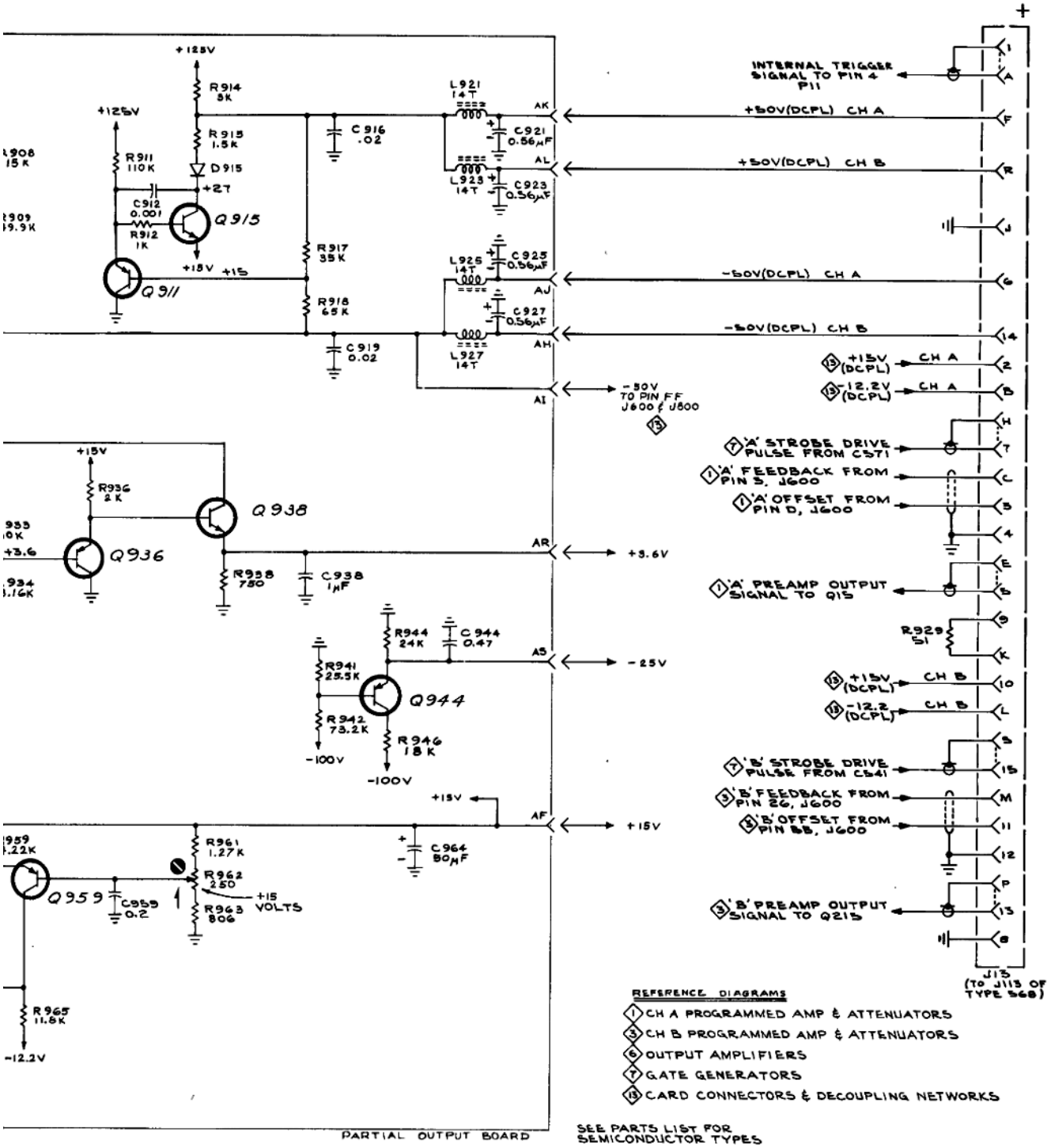
DIGITAL UNIT CONTROL LOGIC (11)

PLM 868


+300V
R947 1K
+125V
-12.2V
-100V
R948 47K
+15V
R902 15K
Q901
Q907
R908 15K
-12.2V
R903 1K
Q903
R909 49.9K
C903 0.001
+2.7
D905
R904 165K
R905 1.32K
R906 1.32K
-100V
R911 110K
C912 0.001
R912 1K
Q911
T950
R930 8.6
D930
AM
AN
AO
AP
≈6.7V AC
R931 8.6K
C931 800MF
R936 2K
R933 10K
+3.6
R934 3.16K
Q936
6.3 V AC
≈52V AC
R951 2.7
D951
AE
R953 2.7
D953
U
D955 9V
C956 1MF
R959 4.22K
R955 806
R956 100
Q957
Q959
R958 100
C959 0.2
W
X
Q966
Q969
C950 1000MF
R950 5.6K
≈-12
R967 1K
R965 11.8K
INTERNAL TRIGGER SIGNAL FROM PIN A, J15
TO LOWER VERTICAL DEFLECTION PLATE FROM Q478
TO UPPER VERTICAL DEFLECTION PLATE FROM Q488
BLANKING TO CRT FROM R528
SAMPLING DRIVE PULSE TO Q503
P11

TYPE 356

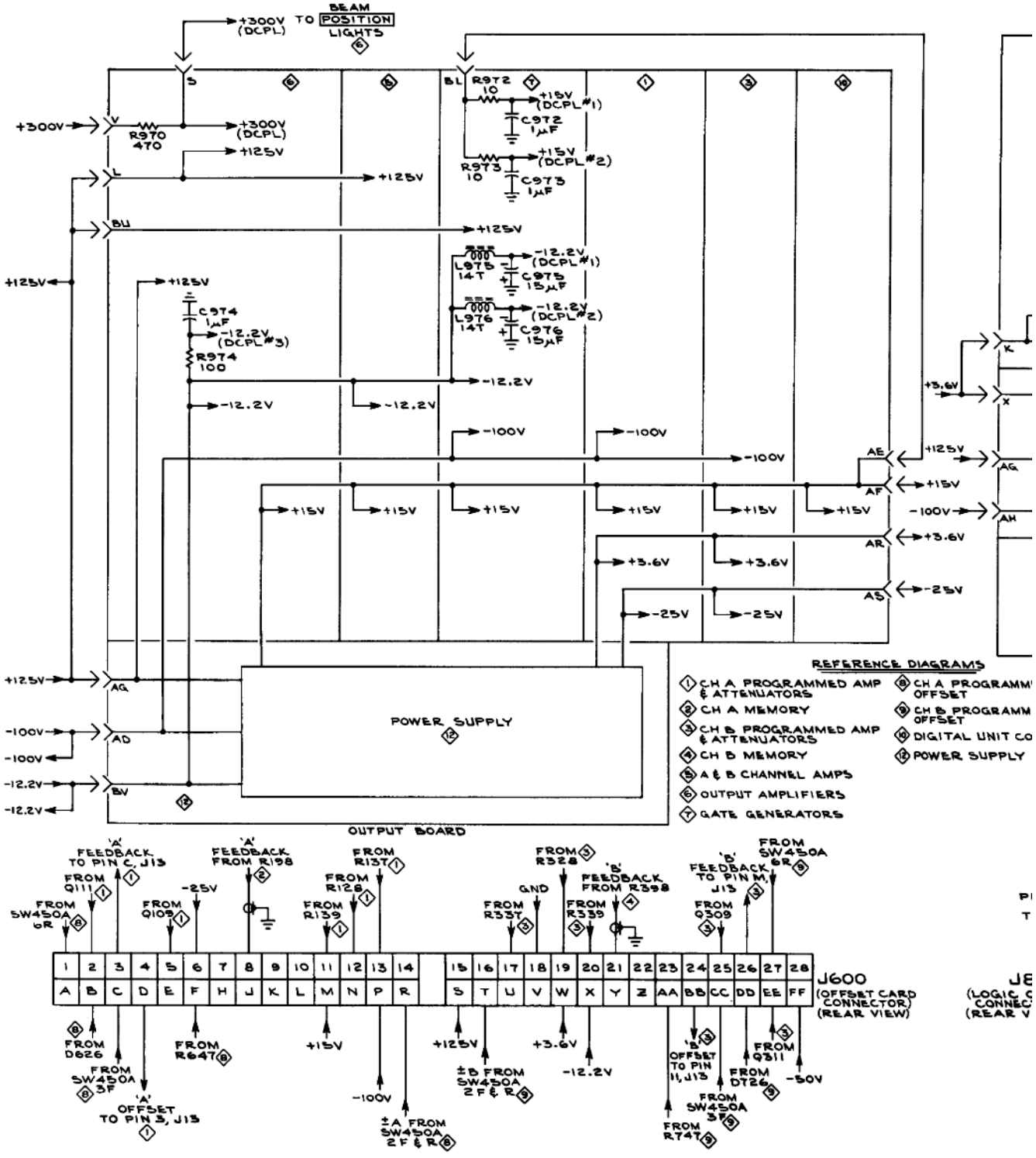
A

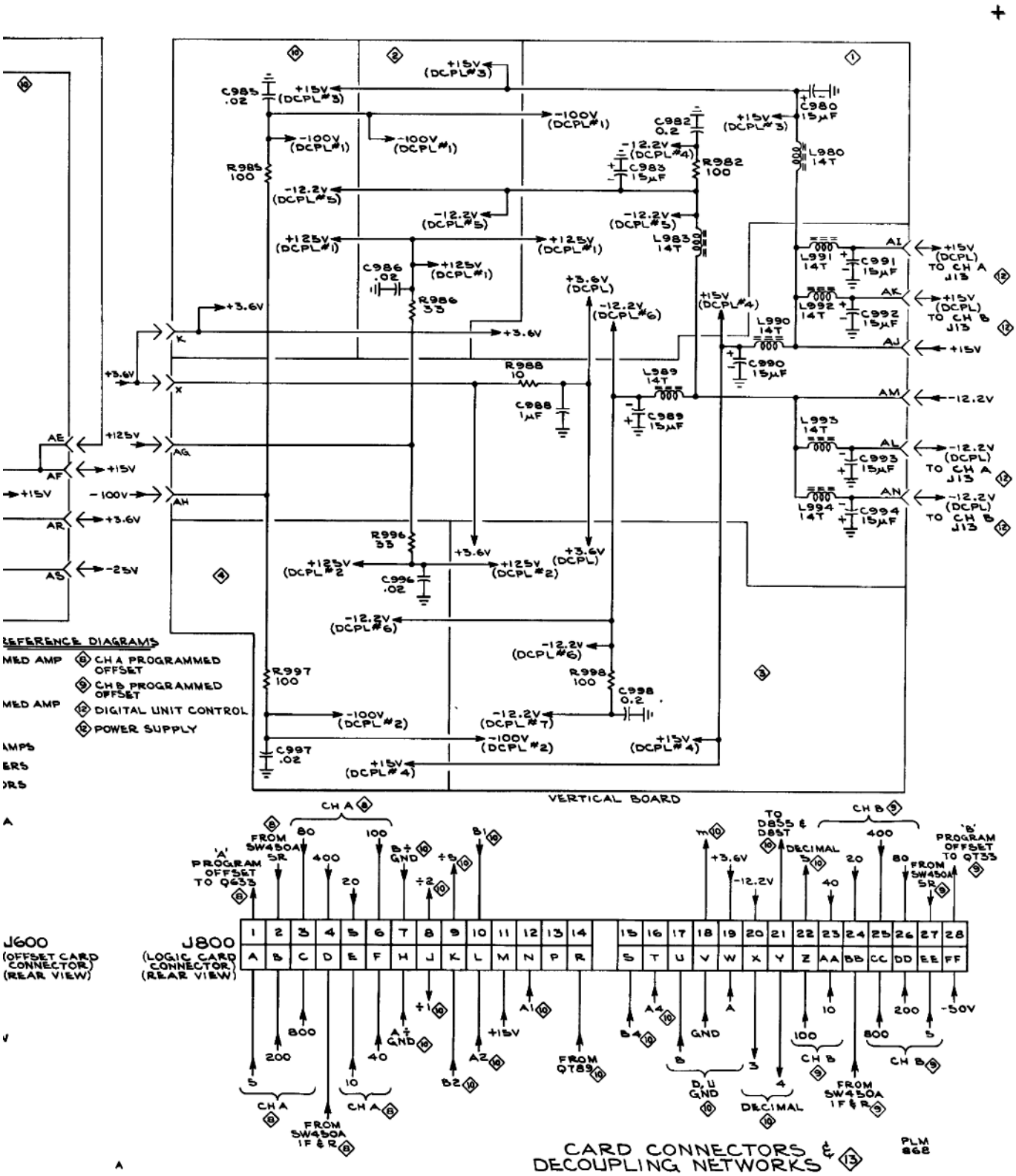


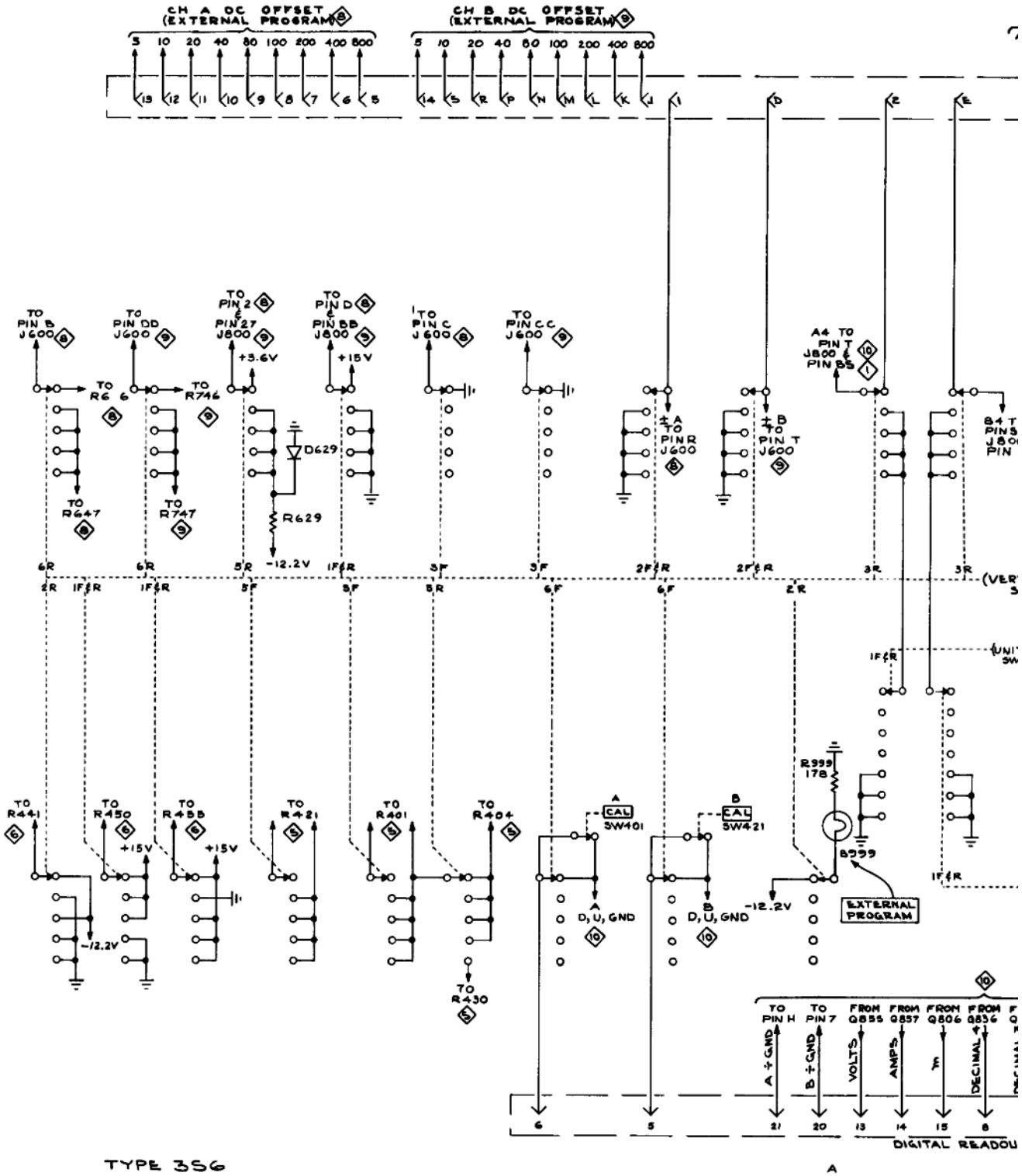
hq
868

A

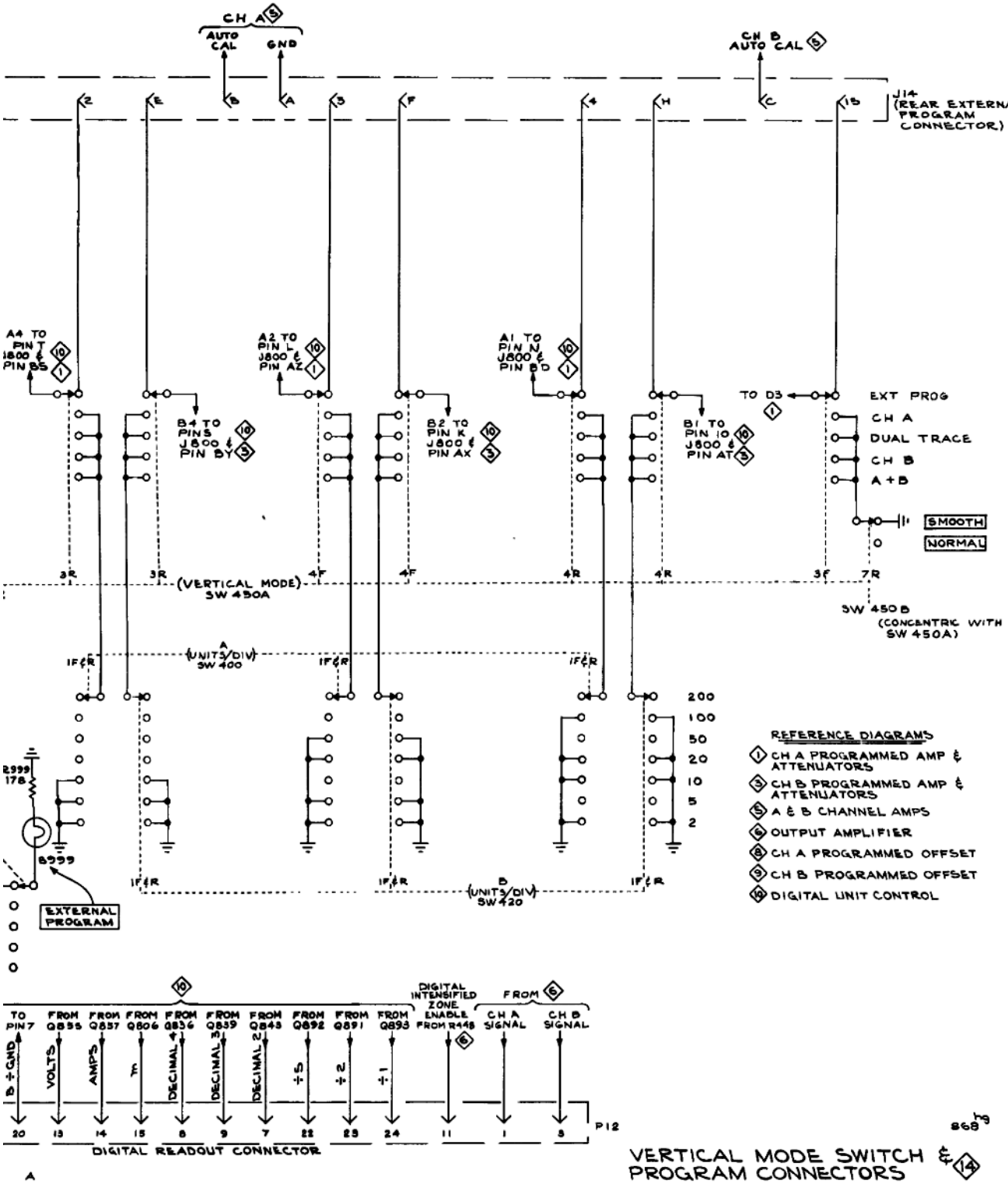
POWER SUPPLY 12


BEAM POSITION LIGHTS
+300V (DCPL)
TO
+300V
R970 470
+125V
R972 10
+15V (DCPL#1)
C972 1μF
R973 10
+15V (DCPL#2)
C973 1μF
L975 14T
C975 15μF
-12.2V (DCPL#1)
L976 14T
C976 15μF
-12.2V (DCPL#2)
C974 1μF
-12.2V (DCPL#3)
R974 100
-12.2V
-100V
+15V
+3.6V
-25V
+12.5V
-100V
-12.2V
POWER SUPPLY
OUTPUT BOARD
REFERENCE DIAGRAMS
1 CH A PROGRAMMED AMP & ATTENUATORS
2 CH A MEMORY
3 CH B PROGRAMMED AMP & ATTENUATORS
4 CH B MEMORY
5 A & B CHANNEL AMPS
6 OUTPUT AMPLIFIERS
7 GATE GENERATORS
8 CH A PROGRAMM OFFSET
9 CH B PROGRAMM OFFSET
10 DIGITAL UNIT CO
12 POWER SUPPLY
'A' FEEDBACK TO PIN C, J13
FROM Q111
FROM SW450A 6R
FROM Q105
-25V
'A' FEEDBACK FROM R198
FROM R128
FROM R137
FROM R139
FROM R328
GND
FROM R337
'B' FEEDBACK FROM R398
FROM R339
FROM SW450A 6R
'B' FEEDBACK TO PIN M, J13
FROM Q309
J600 (OFFSET CARD CONNECTOR) (REAR VIEW)
FROM D626
FROM SW450A 3F
'A' OFFSET TO PIN 3, J13
FROM R647
+15V
-100V
±A FROM SW450A 2F & R
+125V
±B FROM SW450A 2F & R
+3.6V
-12.2V
'B' OFFSET TO PIN 11, J13
FROM R747
FROM SW450A 3F
FROM DT26
FROM Q311
-50V


VERTICAL BOARD
CARD CONNECTORS & DECOUPLING NETWORKS
J600 (OFFSET CARD CONNECTOR) (REAR VIEW)
J800 (LOGIC CARD CONNECTOR) (REAR VIEW)
REFERENCE DIAGRAMS
CH A PROGRAMMED OFFSET
CH B PROGRAMMED OFFSET
DIGITAL UNIT CONTROL
POWER SUPPLY
+15V (DCPL#3)
-100V (DCPL#1)
-12.2V (DCPL#4)
-12.2V (DCPL#5)
+125V (DCPL#1)
+3.6V (DCPL)
-12.2V (DCPL#6)
+125V (DCPL#2)
-100V (DCPL#2)
-12.2V (DCPL#7)
+15V (DCPL#4)
+15V (DCPL) TO CH A J13
+15V (DCPL) TO CH B J13
-12.2V (DCPL) TO CH A J13
-12.2V (DCPL) TO CH B J13
'A' PROGRAM OFFSET TO Q633
'B' PROGRAM OFFSET TO QT33
TO DB55 & DB5T
FROM SW450A SR
FROM SW450A IF & R
FROM QT89
B+ GND
A+ GND
D, U GND
DECIMAL
CH A
CH B
PLM 868


CH A DC OFFSET (EXTERNAL PROGRAM) 8
5 10 20 40 80 100 200 400 800
19 12 11 10 9 8 7 6 5
CH B DC OFFSET (EXTERNAL PROGRAM) 9
5 10 20 40 80 100 200 400 800
14 S R P N M L K J
TO PIN B J600 8
TO PIN DD J600 9
TO PIN 2 & PIN 27 J800 9
TO PIN D & PIN BB J800 5
TO PIN C J600 8
TO PIN CC J600 9
A4 TO PIN T J800 & PIN BS 10 1
+3.6V
+15V
TO R646 6
TO R746 9
TO R647 8
TO R747 9
D629
R629
-12.2V
±A TO PIN R J600 8
±B TO PIN T J600 9
6R 6R 5R 1F&R 3F 3F 2F&R 2F&R 3R 3R
2R 1F&R 1F&R 5F 3F 5R 6F 6F 2R
TO R441 6
TO R450 6
TO R455 6
TO R421 5
TO R401 5
TO R404 5
+15V
+15V
-12.2V
TO R430 5
A CAL SW401
B CAL SW421
A D, U, GND 10
B D, U, GND 10
R999 178
B999
-12.2V
EXTERNAL PROGRAM
1F&R
10
TO PIN H
TO PIN 7
FROM Q855
FROM Q857
FROM Q806
FROM Q856
A ÷GND
B ÷GND
VOLTS
AMPS
Ω
DECIMAL
6 5 21 20 13 14 15 8
DIGITAL READOU

TYPE 356



868 h9

VERTICAL MODE SWITCH & PROGRAM CONNECTORS ⑭

FIG. 1 EXPLODED VIE

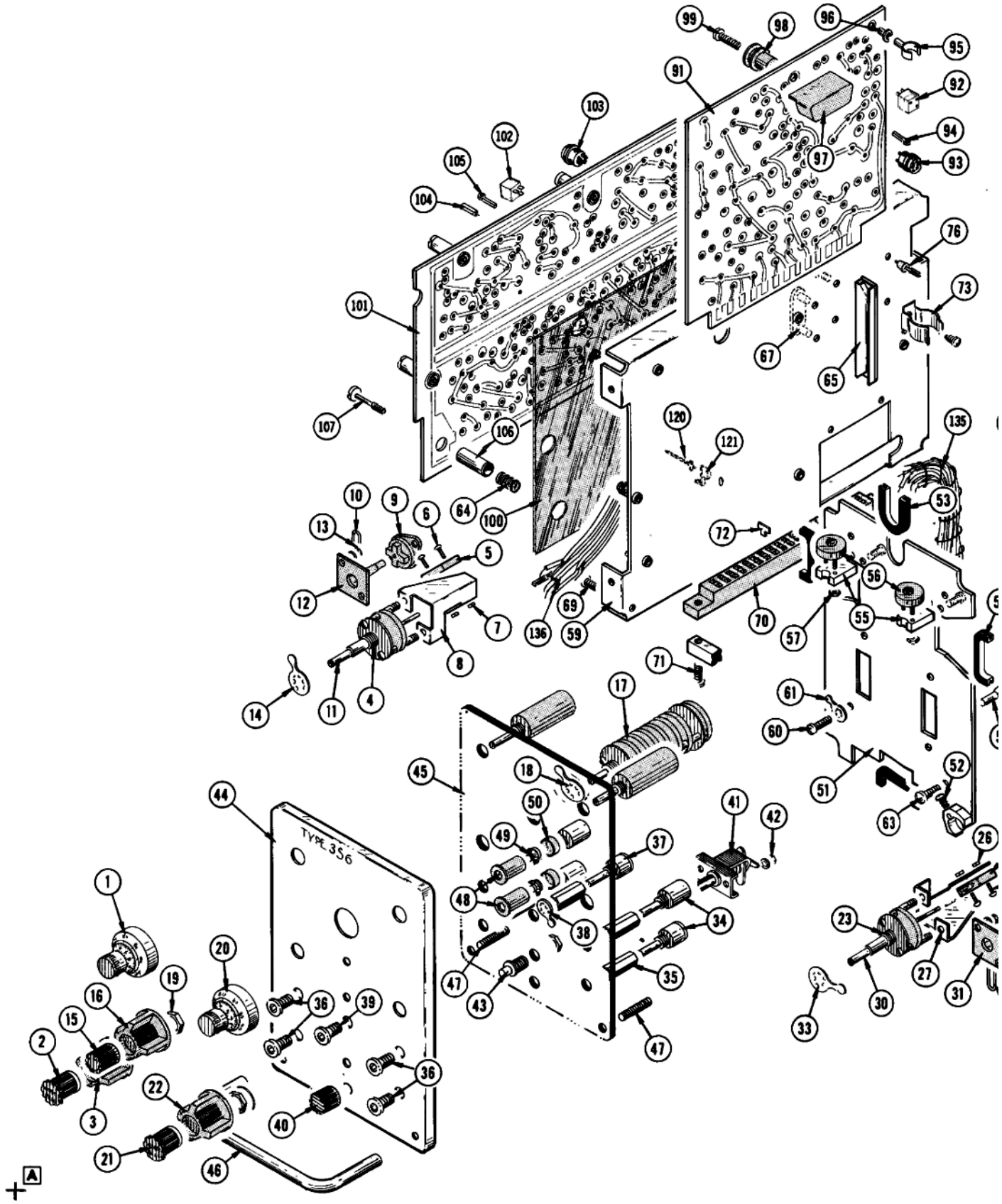
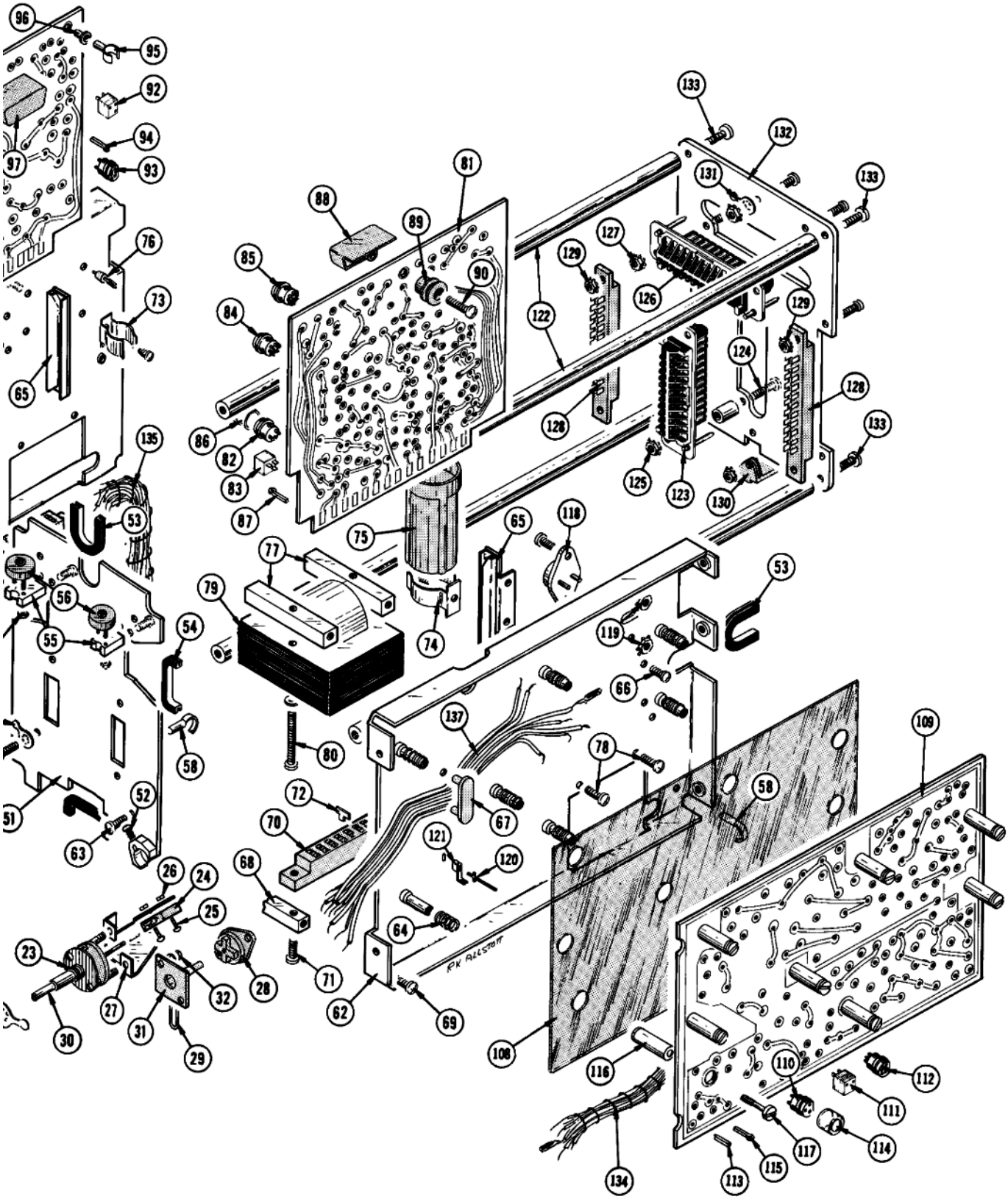


FIG. 1 EXPLODED VIEW



TYPE 3S6 PROGRAMMABLE SAMPLING UNIT

OPTIONAL ACCESSORIES (not shown)

Fig. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	1 2 3 4 5	DESCRIPTION
	012-0131-00			1		CABLE, interconnecting, 6 feet
	012-0149-00			1		ASSEMBLY, circuit card

A

FIG. & INDEX NO.	
2-1	(
-2	3
	(

FIG. 2 STANDARD ACCESSORIES

FIG. & INDEX NO.	TEKTRONIX PART NO.	SERIAL/MODEL NO. EFF.	SERIAL/MODEL NO. DISC.	QTY	DESCRIPTION 1 2 3 4 5
2-1	012-0130-00			1	CABLE, interconnecting, 6 feet
-2	388-0805-00			2	BOARD, circuit, connector
	070-0789-00			2	MANUAL, instruction (not shown)