91A24, 91AE24, AND P6460

OPERATOR'S MANUAL ADDENDUM

TO THE DAS 9100 SERIES OPERATOR'S MANUAL (PART NUMBER 070-03264-00, -01, AND UP)

This Tektronix Manual Addendum supports the following products:

91A24 Data Acquisition Module
91AE24 Data Acquisition Module
P6460 Data Acquisition Probe

This addendum is designed to be inserted into *DAS 9100 Series Operator's Manuals* that have part numbers 070-3264-00, -01, and up. You can find your manual part number in the bottom left corner of the manual title page. (Note: Some manuals may already have this addendum inserted in the back of their binders. Check your manual to see if there is a duplicate.)

This addendum contains operator's information specific to the 91A24 and 91AE24 Data Acquisition Modules and the P6460 Data Acquisition Probe. It adds information to the *DAS 9100 Series Operator's Manual*; it does not replace information.

Refer to the *DAS 9100 Series Operator's Manual* for information on other products, including mainframes, instrument modules, probes, and options.

How To Use This Addendum. This addendum is organized similarly to the *DAS 9100 Series Operator's Manual*. Information within the addendum corresponds to sections within the operator's manual. You can place the addendum at the back of the operator's manual binder, or you can insert the pages into their corresponding operator's manual sections.

This addendum affects only some of the operator's manual sections; it does not affect all of them.

PLEASE CHECK FOR CHANGE INFORMATION
AT THE REAR OF THIS MANUAL

Tektronix, Inc.
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Serial Number _____

070-4540-00
Product Group 57

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TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

LIST OF ILLUSTRATIONS

OPERATOR'S SAFETY SUMMARY

The general safety information in this part of the summary is for both operators and service personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols As Marked on Equipment


DANGER — High voltage.


Protective ground (earth) terminal.


ATTENTION — refer to manual.

Grounding the Product

This product is grounded through the mainframe in which it is operating. To avoid electrical shock, plug the power cord of the mainframe into a properly wired receptacle before connecting to the product. A protective-ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulated) can render an electric shock.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

GENERAL INFORMATION

DESCRIPTION

The 91A24 and 91AE24 Data Acquisition Modules are plug-in circuit board assemblies that are compatible with any DAS 9100 Series mainframe. They feature comprehensive clocking, data qualification, and triggering abilities. Acquisition rates of up to 10 MHz are possible, using either internal or external clocking. Each module acquires 24 data channels, using three data acqusition probes.

Clocking. The 91A24 can acquire data under the control of either asynchronous internal clocking or synchronous external clocking. For external clocking, three different clock expressions may be formed, each using as many as three clock and three qualifier signals. Data can be demultiplexed without double probing.

Data Qualification and Triggering. The 91A24 offers extensive word recognition for data qualification and triggering.

For qualifying blocks of data, you can use as many as two ORed word recognizers to begin data storage, and two more to end data storage. Alternatively, you can qualify data on a cycle-by-cycle basis using up to two ORed word recognizers.

For triggering, there is a 16-level sequential word recognizer, a word recognizer for resetting the sequential word recognizer, and a word recognizer which can trigger independently of the sequential word recognizer.

Module Configuration. Only one 91A24 module may be installed in a DAS mainframe. In addition, up to three 91AE24 modules can be installed, allowing acquisition of up to 96 channels. 91AE24s are expander modules and can only be used with a 91A24 module installed in the mainframe.

Modes of Operation. The 91A24 and 91AE24 modules may be operated alone in 91A24 ONLY mode, or they may be used with high-speed data acquisition modules in 91A24 ARMS mode.

In ARMS mode, the 91A24/91AE24 and high-speed modules act as linked logic analyzers. Both types of modules acquire data simultaneously; when the 91A24 trigger conditions are satisfied, the high-speed module is armed to look for its trigger event.

Data Display. Data acquired by 91A24/91AE24 modules, including ARMS acquisition, can be displayed in both state table and timing diagram format.

STANDARD AND OPTIONAL ACCESSORIES

91A24 DATA ACQUISITION MODULE

The following lists include the standard and optional accessories for the 91A24 Data Acquisition Module.

Standard Accessories

1	175-8165-00	External Sync Output Cable, 2 m (78 in.)
1	070-4672-00	*91A24 Instructions*
1	070-4540-00	*91A24, 91AE24, and P6460 Operator's Manual Addendum (to the DAS 9100 Series Operator's Manual)*

Optional Accessories

UPIK40	40-pin Universal Probe Interface Kit
070-4541-00	*91A24 and 91AE24 Service Manual Addendum (to the DAS 9100 Series Service Manual)*
175-8166-00	Interconnect Cable Assembly, 28 cm (11 in.), for service procedures; 7 required
DAS 9100 Series Mnemonics Tapes;	see your Tektronix Sales Engineer for ordering information

91AE24 DATA ACQUISITION MODULE

The following lists include the standard and optional accessories for the 91AE24 (Expander) Module.

Standard Accessories

7	175-8167-00	Interconnect Cable Assemblies, 7.6 cm (3 in.)
1	070-4671-00	*91AE24 Instructions*

Optional Accessories

UPIK40	40-pin Universal Probe Interface Kit
070-4541-00	*91A24 and 91AE24 Service Manual Addendum (to the DAS 9100 Series Service Manual)*
175-8166-00	Interconnect Cable Assembly, 28 cm (11 in.), for service procedures; 7 required
DAS 9100 Series Mnemonics Tapes;	see your Tektronix Sales Engineer for ordering information

P6460 DATA ACQUISITION PROBE

The following lists include the standard and optional accessories for the P6460 Data Acquisition Probe.

Standard Accessories

1	070-4345-00	*P6460 Instructions* (includes service information)
1	012-0747-00	Lead Set, 25 cm (10 in.)
1	020-0720-00	Package of 12 Probe Tips (each tip is a 206-0222-00)
2	012-0989-00	Ground (or VL) Sense Leads, 12.7 cm (5 in.) with Pomona Hook Tips (344-0267-00)
2	344-0046-00	Alligator Clips (substitute for hook tips above)

Optional Accessories

012-0987-00	Flying Lead Set, 12.7 cm (5 in.)
012-0800-00	Flying Lead Set, 25 cm (9.8 in.)
020-1041-00	40-pin Univ. Probe Interface Kit
012-1000-00	Diagnostic Lead Set, 25 cm (10 in.)
012-0989-01	Package of 10 Ground (or VL) Sense Lead Tips with Pomona Hook Tips (344-0267-00)
103-0209-01	GPIB Connector/Adapter
003-0709-00	IC Extractor, 16-pin
015-0330-00	Adapter, Test Clip, 16-DIP
015-0339-02	Adapter, Test Clip, 40-DIP, 10 cm (3.9 in.) cable (requires 380-0560-05 Adapter)
015-0339-00	Adapter, Test Clip, 40-DIP, 30 cm (11.8 in.) cable (requires 380-0560-05 Adapter)
380-0560-05	Adapter, required for use with 40-DIP Adapters
119-1474-00	Probe Holder

SPECIFICATIONS

Table 1
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: DATA ACQUISITION AND STORAGE

Characteristics	Performance Requirements	Supplemental Information
Maximum Sampling Rate	10 MHz (non-multiplexed)	Internal or External Clocking (multiplexed 20 MHz)
Acquisition Memory		
Memory Depth		1023 Words
Memory Width		24 Channels (one 91A24, 3 probes); expandable to 96 channels (one 91A24, three 91AE24s, 12 probes).
Data Setup (period data valid prior to clock edge)	25 ns min. (using P6460 probe)	Same requirement for multiplexed data.
Data Hold (period data valid beyond clock edge)	0 ns max. (using P6460 probe)	Same requirement for multiplexed data.
Trigger Position		Selectable for BEGIN, CENTER, END, DELAY. In DELAY mode, trigger sequence = 1015 − DELAY value.
External Trigger Enable		TTL LS input to mainframe BNC connector. Rising edge enables sequential word recognizer trigger on next clock cycle.
Setup Time	25 ns min.	
Hold Time	0 ns max.	
91A24 ARMS Modes		High-speed module is armed to look for trigger within ten 91A24 clock cycles after 91A24 trigger event.
Requirement for Time Alignment		1. No data qualifiers are used (91A24 clock qualifiers are permitted). 2. High-speed module operation must overlap 91A24 operation by at least 5 master clocks. 3. High-speed clock rate must be at least twice that of 91A24 master clocks. 4. Trigger words for both the high-speed and 91A24 modules must be in memory.

Table 2
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: CLOCKING

Characteristic	Performance Requirements	Supplemental Information
Internal Clock		Interval is selectable from 100 ns to 5 ms in a 1-2-5 sequence. May be qualified using 91A24's pod C qualifier.
External Clocks & Qualifiers		3 clocks, 3 qualifiers
Source		Via acquisition probes connected to 91A24
Selection		Boolean combinations used to form 3 POD CLOCK expressions.
Raw Clock Rate	20 MHz max.	Time between *qualified* master clocks may be no less than 100 ns. Other POD CLOCKs must occur ⩾ 20 ns before next cycle's master clock.
Clock Pulse Width	25 ns min., high and low (using P6460 probe)	
Qualifier Setup Time	25 ns min. (using P6460 probe)	
Qualifier Hold Time	0 ns max. (using P6460 probe)	

Table 3
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: WORD RECOGNIZER FUNCTIONS

Characteristic	Performance Requirements	Supplemental Information
Word Recognizer Width		Same as channel width
BEGIN STORE IF		Up to 2 ORed word recognizers
END STORE IF		Up to 2 ORed word recognizers
STORE ONLY IF		Up to 2 ORed word recognizers
RESET Word Recognizer		Resets sequential word recognizer to Level 1, and resets timer.
Independent Trigger		Parallel word recognizer ORed to sequential word recognizer. Not affected by trigger input signal.
Sequential Word Recognizer		Up to 16 levels of word recognition
OCCURS Counter		Number of event occurrences (1-4096) may be specified at each level.
Intermediate Level Actions		THEN, RUN TIMER, STOP TIMER, SYNC OUT selections
Final Level Actions		TRIGGER, INCR CNTR (12 decimal digits), SYNC & TRG, NEVER TRG selections

Table 3 (cont.)
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: WORD RECOGNIZER FUNCTIONS

Characteristic	Performance Requirements	Supplemental Information
Timer Accuracy	Indicated value ± 2%, ± 100 ns each time started	Times to over 27 hours.
Sync Output Signal	TTL output level, terminated into 1 MΩ	Remains high until completion of a subsequent word recognizer level with no sync-output specified.
Sync Output Delay	3 master clocks + 45 ns ± 10 ns between event occurrence and rising edge of sync-output	Measured from master clock's active edge to connector output.
Word Recognizer Output		TTL-level signal output by mainframe BNC connector. 4 Master clock cycles after trigger event, signal goes and remains high.

Table 4
91A24 AND 91AE24 ELECTRICAL SPECIFICATIONS: PROBE INTERFACE AND SUPPORT

Characteristic	Performance Requirements	Supplemental Information
Probe-to-Module Signals		8 data (91A24 & 91AE24), 1 clock, 1 qualifier (91A24 only)
Module-to-Probe Signals		
Threshold Reference Voltage		
Fixed (TTL)		+1.40 V
Variable (VAR)		−6.40 V to +6.35 V in 50 mV steps. Default is −1.30 V.
TTL and VAR Threshold Accuracy (to input of attached probe)	Indicated value ± 0.5%, ± 65 mV	

91A24 AND 91AE24 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications for the operation of this instrument meet or exceed those specified for the operation of the DAS9109 Mainframe and the DAS9129 Mainframe. For details, refer to the *DAS 9100 Series Operator's Manual.*

Table 5
P6460 ELECTRICAL SPECIFICATIONS

Characteristic	Description
User's Ground Sense	<100 Ω to user's ground
Input Impedance	1 MΩ ± 1%, 5 pF nominal; lead set adds approx 5 pF
Max. Non-Destructive Input Voltage Range	±40 V (DC + peak AC)
Max. Voltage Between Any Two Inputs	±60 V (DC + peak AC)
Operating Input Voltage Range	From −40 V to input threshold's voltage + 10 V (+30 V for RS-232 only)
Threshold Offset and Accuracy	±0.25% of threshold ±50 mV
Minimum Input Swing	0.5 V p-p centered on the threshold
Minimum Pulse Width (with input 250 mV over the threshold from +0.5 V and −0.5 V)	4 ns at threshold

Table 6
P6460 ENVIRONMENTAL SPECIFICATIONS

Characteristic	Description
Temperature	
Operating	−15°C to +55°C
Storage	−62°C to +75°C
Humidity	95% to 97% relative humidity
Altitude	
Operating	4.5 km (15,000 ft.)
Non-operating	15 km (50,000 ft.)
Electrical Discharge	5 kV maximum from 200 pF with 2 kΩ series resistance

Table 7
P6460 PHYSICAL SPECIFICATIONS

Characteristic	Description
Weight	340 g (12 oz.)
Overall Dimensions	
Pod	11.4 cm (4.5 in.) long, 5.6 cm (2.2 in.) wide, 2.2 cm (0.85 in.) deep
Cable	2 m (78.8 in.) ±10%

OPERATING INSTRUCTIONS

This section describes installation requirements for the 91A24 and 91AE24 modules and their probes. It also provides operator's checkout procedures for the modules and probes.

Repackaging Information. All DAS 9100 Series products are shipped in specially designed transportation packaging. Keep this packaging for use whenever you ship DAS products. If the original packaging is no longer fit for use, contact your nearest Tektronix Field Office and obtain new DAS packaging.

If you need to ship any part of your 91A24/91AE24 system to a Tektronix Service Center, please send all parts of your 91A24 system: the 91A24 module, any 91AE24 modules, and their probes.

When you ship a product to a Tektronix Service Center, be sure to attach an identifying tag to the product (inside the packaging). On this tag include your name, the name of your company, the name and serial number of the enclosed product, and a description of the service requested.

MODULE INSTALLATION

It is assumed that you are already familiar with the procedures for removing the mainframe top panel and cover, and with the procedures for installing modules into the mainframe bus slots. If you are not familiar with these procedures, refer to the *Operating Instructions* section of the *DAS 9100 Series Operator's Manual.*

Do not remove or install a 91A24 or 91AE24 module until you have read the following warnings, cautions, and configuration requirements.

WARNING

When installing or removing instrument modules, the operator may gain access to the mainframe's module compartment only. Unless you are a qualified service technician, do not open any other compartments within the mainframe because they contain hazardous voltages.

CAUTION

When modules are being installed, the mainframe should be turned off and unplugged from its power source. Damage to the module's circuitry may occur if the module is installed while the mainframe is receiving power.

CONFIGURATION AND UPDATE REQUIREMENTS

Configuration Requirements

The power and configuration requirements for the 91A24 and 91AE24 modules are as follows:

1. To operate 91AE24 modules, a 91A24 module must be installed in the mainframe.
2. The 91A24 module can only share a +5 V power supply with a 91AE24, 91A08, or 91P32 module.

CAUTION

If the 91A24 is installed in a bus slot sharing a power supply with any type of module other than a 91AE24, 91A08, or 91P32, the power supply may not function correctly due to current overload.

When positioning modules around the 91A24, be sure to allow for the power supply restriction. Table 1 shows bus slot positions recommended for 91A24 and 91AE24 modules.

You can see which power supplies are present in the mainframe by checking the chrome pins visible through the power supply area cover. DO NOT remove the power supply area cover.

3. Without violating the power supply requirement, the 91A24 and 91AE24 must be positioned in adjacent bus slots. All 91AE24 modules must be positioned to the same side (either all to the right or all to the left) of the 91A24 module. Table 1 shows bus slot positions recommended for 91A24 and 91AE24 modules.

Table 1
RECOMMENDED BUS-SLOT PLACEMENT

Bus Slot	Module
0	Controller
1	91A24 Data Acquisition Module
2	91AE24 Data Acquisition Module
3	91AE24 Data Acquisition Module
4	91AE24 Data Acquisition Module
5	Any module other than a 91A24 or 91AE24
6	Any module other than a 91A24 or 91AE24
7	Trigger/Timebase

Positioning modules as recommended ensures that Tektronix mnemonics tape files will restore. Also, if you use more than one DAS, consistent positioning of modules ensures that your setup files are transferable.

Firmware Update Requirements

To operate with 91A24/91AE24 modules your DAS must be equipped with firmware version 1.11 or higher. If your DAS has a lower firmware version, it will display the error message NEEDS FIRMWARE VERSION $>=$ 1.11 at powerup. You can determine your mainframe's firmware version by looking in the upper right corner of the power-up display.

Firmware version 1.11 requires that 91A04 modules be equipped with version 2 (or higher) firmware. You can determine if your 91A04 has the correct firmware by checking the 91A04 listing on the DAS powerup display: V2 (or higher) should appear at the right of this line.

To obtain Version 1.11 update kits for your mainframe and/or 91A04, contact your Tektronix representative.

Hardware Update Requirements

For use with 91A24/91AE24 modules, certain hardware updates are required. These updates can be performed by your Tektronix Service Center, or you can order the appropriate DAS hardware update kit. The following updates are necessary:

- DAS mainframes with serial numbers lower than B030100 require a controller board modification.
- 91A08 modules with serial numbers lower than B020100 require modification to operate in 91A24 ARMS 91A08 mode.
- PMA 100 Personality Module Adapters with serial numbers lower than B020100 require a new backpanel label.

Should any of your equipment require an update, contact your Tektronix representative.

WORD RECOGNIZER AND CLOCK INTERCONNECT PINS

When one or more 91AE24 expander modules are installed in the mainframe, interconnect pins on the top edge of the modules are used to communicate word recognizer and clock signals.

Each 91AE24 module comes equipped with seven 3-inch interconnect cable assemblies. These cables connect the 91A24 and 91AE24 modules' word recognizer and clock interconnect pins. In addition, some of the 91A24's square-pin jumpers move to interconnect pins on the 91AE24 furthest from the 91A24. Interconnect cables and square-pin jumpers must be correctly installed for the modules to operate properly.

Figure 1 illustrates how the interconnect cables and square-pin jumpers should be installed.

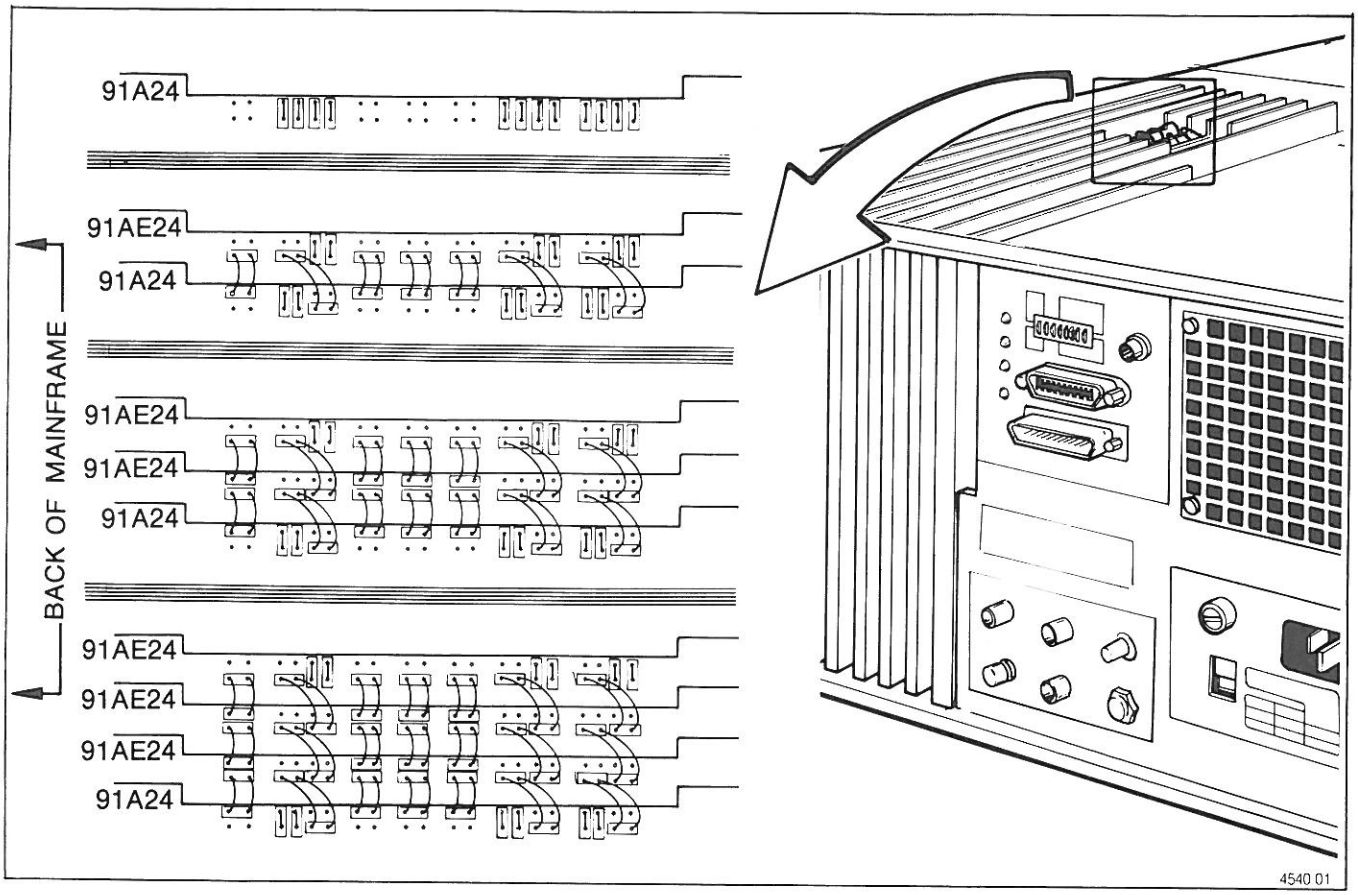


Figure 1. 91A24/91AE24 interconnect pins. This illustration shows correct configurations of interconnect cables and square-pin jumpers. Four possible cases are shown: a 91A24 without 91AE24s, and configurations when one, two, and three 91AE24s are installed.

SYNC-OUTPUT CABLE

The 91A24 module comes equipped with a 2-meter coaxial cable. This cable is used to carry a TTL-level sync-output signal. The sync-output signal can be synchronized with recognition of events defined in the Trigger Specification submenu's sequential word recognizer.

The sync-output cable is connected to the 91A24 through back-panel openings on the mainframe. The cable plug-in jack is located on the back edge of the 91A24 module, immediately below the pod C connector. Connection of the sync-output cable is shown in Figure 2.

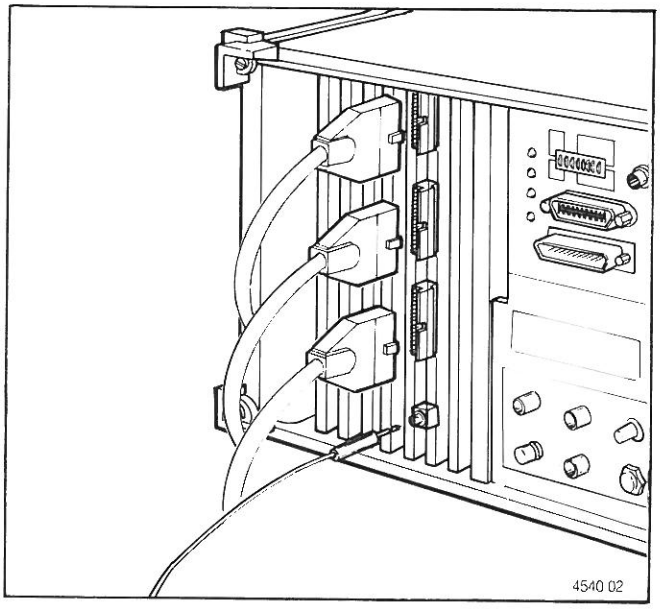


Figure 2. Connecting P6460 probes and sync-output cable.

CONNECTING ACQUISITION PROBES

Data acquistion probes are connected to the 91A24 and 91AE24 through back-panel openings on the mainframe. The probes attach to the modules' pod A, pod B, and pod C connectors.

To connect probes to modules (see Figure 2):

1. Grasp the probe by its cable holder.
2. Align the cable holder with the module's pod connector. Be sure the raised tab on the cable holder is facing towards bus slot 0, and is aligned with the opening on the module's pod connector.
3. Gently push the cable holder onto the connector. Do not force the connection.

To disconnect the probe, grasp the cable holder and pull gently.

CAUTION

You may damage the probe cable if you disconnect the probe by pulling on the cable rather than the cable holder.

P6460 CHARACTERISTICS

The P6460 is a 100 MHz data acquisition probe. Each P6460 provides the 91A24 module with eight data input channels, one qualifier channel, and one clock channel. When connected to a 91AE24 module, only the data channels are active. For P6460 specifications and signal characteristics, refer to *Specifications* in this manual.

Figure 3 illustrates the various elements and features of the P6460 probe. Refer to this figure when reading the following paragraphs.

Probe label for 91A24/91AE24. Each P6460 comes packaged with two gummed signal input labels. Find the label that has Q (qualifier) marked on the left and CK (clock) marked on the right. Place the label on the probe housing location shown in Figure 3.

Probe Leads and Tips. Each P6460 probe is supplied with a 10-inch lead set and a package of 12 probe tips (grabber-type). Figure 3 shows connection of the leads and tips.

Connect the lead set to the probe, making sure that the set's white lead is on the side of the probe housing labled CK (clock). Push the lead set's connector into the probe housing. To disconnect the lead set, pull on its connector; do not pull on the leads.

⚠**Ground Lead Connections.** Also provided with each P6460 are two 5-inch ground sense leads with Pomona Hook tips, and two alligator-clip lead tips. As shown in Figure 3, only one ground lead is required for use with the 91A24 and 91AE24 modules. Plug the lead into either of the probe housing's connectors labeled USERS GND.

Use the alligator-clip tips if necessary to ensure a secure ground connection. (Both types of lead tips make threaded connections to the ground lead.)

The middle GND connector, labeled ⚠, should only be used when the the diagnostic lead set is connected to the probe.

Maximum Non-destructive Input Voltage. The maximum input voltage which may be used with the P6460 probe is ±40 V peak.

CAUTION

Probe circuitry may be damaged if the P6460 is connected to a voltage source greater than ±40 V peak.

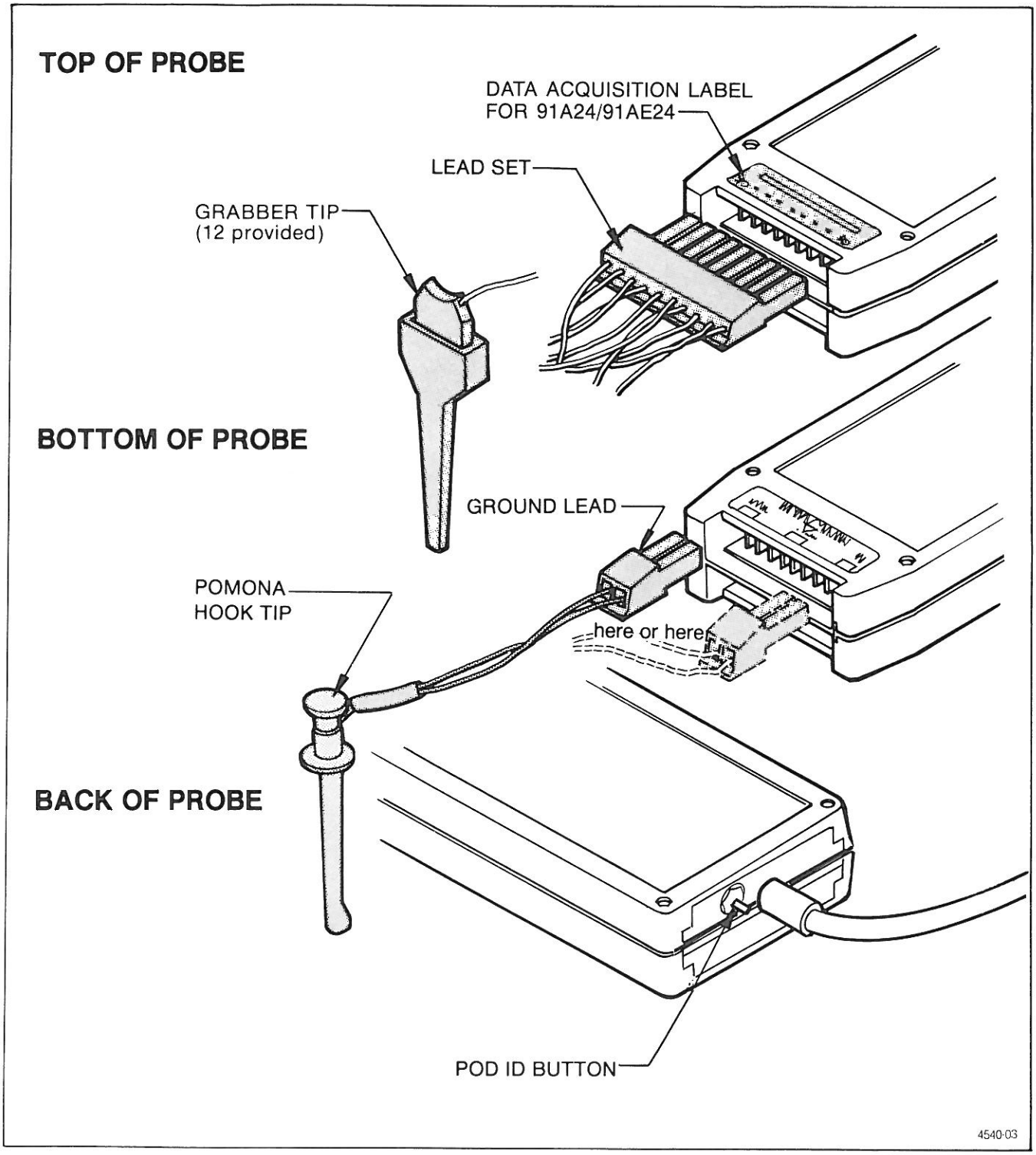


Figure 3. P6460 Data Acquisition Probe characteristics and lead connections.

OPERATOR'S CHECKOUT

When the DAS mainframe is powered up, all installed 91A24 or 91AE24 modules will appear on the power-up configuration display. PASS or FAIL notations appear next to each module to show the results of that module's power-up testing. Table 2 lists and defines the power-up error conditions for 91A24 and 91AE24 modules.

Table 2
POWER-UP ERROR CONDITIONS

Error Condition	Definition
91A24 Acquisition Module FAIL	The 91A24 module has failed the power-up test. The module will not operate properly. Refer the 91A24 module to qualified service personnel. This failure does not affect the operation of any installed pattern generator modules or other data acquisition modules, except for 91AE24s. 91AE24 modules will not operate without a working 91A24 module.
91AE24 Acquisition Module FAIL	The 91AE24 module has failed the power-up test. The module will not operate properly. This failure will occur if the clock and word recognizer interconnect pins are improperly connected by interconnect cables and square-pin jumpers. Power down the mainframe, check the interconnect pins, then power up the mainframe. If the failure continues, refer the 91AE24 module to qualified service personnel. This failure may affect operation of the 91A24 module and/or other 91AE24 modules.

CHANNEL SPECIFICATION MENU

For specific information on how to operate the Channel Specification menu, refer to *Channel Specification Menu* in the *DAS 9100 Series Operator's Manual*. The following paragraphs describe only special characteristics of the menu as they apply to the 91A24 module.

POWER-UP CHANNEL GROUPING

At power-up, the DAS organizes all 91A24 and 91AE24 pod A data in group A, pod B data in group B, and pod C data in group C. You may regroup channels as desired.

GROUPING DEMULTIPLEXED CHANNELS

When you have set up demultiplexing in the 91A24 Clock Specification sub-menu, multiplexed data is acquired by pod A. The data is demultiplexed and stored in both pod A and pod B memories (pod B data lines are not connected). In the Channel Specification menu's PROBE column, the data stored in pod B memory is listed as pod B data.

THRESHOLD SELECTION

The default THRESHOLD field value for 91A24/91AE24 pods is TTL +1.40 V. When you select VAR, you can specify a threshold in the range of −6.40 V to +6.35 V.

When you set one pod's threshold, the DAS automatically sets all other pods connected to that module with the same threshold value.

TRIGGER SPECIFICATION MENU

The 91A24 and 91AE24 modules may be used in either of two acquisition modes, selected in the Trigger Specification menu. They are:

- **91A24 ONLY Mode** - this mode uses one 91A24 and up to three 91AE24 modules for data acquisition.
- **91A24 ARMS Mode** - ARMS mode allows data acquisition using 91A24/91AE24 modules together with a high-speed data acquisition module. The two types of modules are set up with different clock rates to provide a time-aligned display. When the 91A24 recognizes its trigger event, it arms the high-speed module to look for a second trigger event.

In both 91A24 ONLY and 91A24 ARMS modes, there are two sub-menus for setting up the 91A24: the Trigger Specification and Clock Specification sub-menus. For ARMS mode you set up the high-speed module's trigger and clocking in its ONLY mode, then select the appropriate 91A24 ARMS mode before starting acquisition.

The remainder of this section describes the 91A24 Trigger Specification sub-menu, the 91A24 Clock Specification sub-menu, and specific information for using 91A24 ARMS mode.

91A24 TRIGGER SPECIFICATION SUB-MENU

When you press the TRIGGER SPEC key after power-up, the DAS displays the 91A24's Trigger Specification sub-menu. 91A24 ONLY is the default acquisition mode. In this mode the DAS acquires data using one 91A24 module and up to three 91AE24 modules.

Description of the 91A24 Trigger Specification sub-menu is divided into four topics:

- **MODE, SPECIFICATION, and Data Entry Fields** – describes general-purpose fields in the sub-menu.
- **Mnemonics Functions** – describes the use of recognition mnemonics in data entry fields.
- **Data Qualification Functions** – describes fields and functions which let you specify the kind of data to be stored.
- **Trigger Functions** – describes fields and functions which let you trigger on particular data, and actions which the 91A24 can perform before the trigger occurs.

MODE, SPECIFICATION, AND DATA ENTRY FIELDS

The following paragraphs explain the Trigger Specification sub-menu MODE, SPECIFICATION, and word recognizer fields. Refer to the numbered callouts in Figure 4 when reading the field descriptions.

Specific trigger, storage, and mnemonics functions are described later in this section.

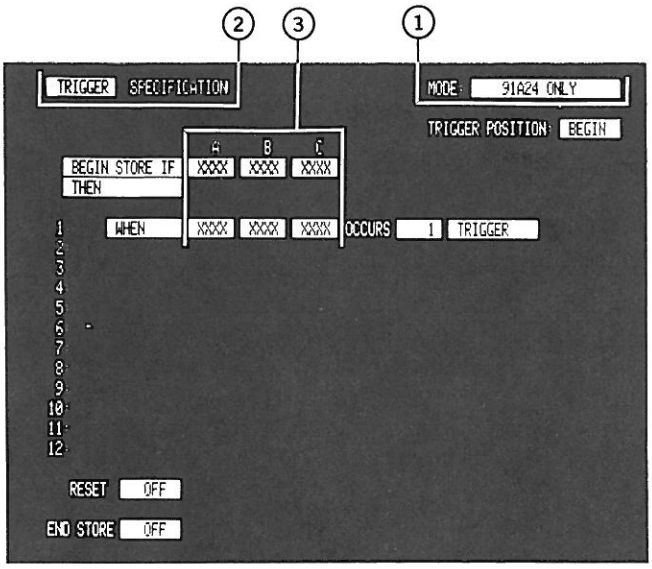


Figure 4. Default 91A24 Trigger Specification sub-menu.

① MODE Field
(see Figure 4)

The MODE field is used to select among the Trigger Specification menu's available trigger modes. Which modes are available depends on which acquisition modules are installed in the mainframe. The field only appears in reverse video if more than one type of acquisition module is installed in the mainframe. The default mode is 91A24 ONLY.

To change trigger modes:

Press SELECT.

② SPECIFICATION Field
(see Figure 4)

This field lets you select between the Trigger Specification and Clock Specification sub-menus.

To move from one sub-menu to the other:

Press SELECT.

For details of clock specification, refer to *91A24 Clock Specification Sub-menu.*

NOTE

If there is a MICRO NAME specified in the Define Mnemonics menu, the field's SPECIFICATION label changes to read SPECIFICATION FOR: [micro name]. Refer to the Define Mnemonics *section of this manual for details.*

③ Data Entry Fields
(see Figure 4)

The word recognizer data entry fields are organized in channel group columns. Channel group names are indicated above each group column.

NOTE

You can specify special group column headings in the Define Mnemonics menu. For details, refer to the Define Mnemonics Menu *section of this manual.*

To enter numeric data values:

Use the data entry keys.

Don't care (X) values are entered using the DON'T CARE key.

You can also use mnemonics in data entry fields. For details refer to the following *Mnemonics Functions* discussion and to the *Define Mnemonics Menu* section of this manual.

A channel group's data entry field will not be displayed if it's width exceeds 30 characters. The width of a group's field depends on the number of channels in the group and the group's display radix. You can alter channel grouping and display radix in the Channel Specification menu.

When the DAS cannot display all of the group columns on the display, it displays one or both of the messages <- MORE and MORE ->. The sub-menu allows you to scroll channel group columns sideways onto the display.

To scroll group columns:

Simultaneously press the SHIFT and ▷ or ◁ SCROLL keys.

The DAS scrolls group columns onto the display one at a time, and indicates the direction in which other columns are hidden.

MNEMONICS FUNCTIONS

Working with the Define Mnemonics menu, the 91A24 Trigger Specification sub-menu provides a special function which permits you to use mnemonics in data entry fields. This feature is enabled by setting up special tables in the Define Mnemonics menu.

In these tables, called [group]* tables, you list numeric values and their associated mnemonics. Each [group]* table corresponds to a particular channel group, and can provide mnemonics for that group's data entry fields in the 91A24 Trigger Specification sub-menu.

For details on setting up 91A24-compatible [group]* tables, refer to the *Define Mnemonics Menu* section of this manual.

Once you have set up [group]* tables, their mnemonics and associated data values are easily obtained in data entry fields.

To obtain table mnemonics in a data entry field:

Press SELECT.

The first mnemonic listed in the corresponding [group]* table will appear in the data entry field.

To choose from mnemonics listed in the table:

Press INCR to obtain the table's next mnemonic. Press DECR to obtain the previous mnemonic.

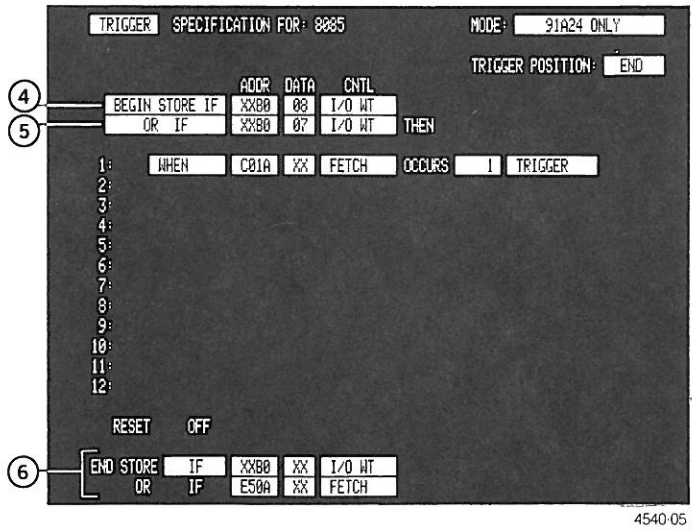
To return to numeric entry in a data entry field:

Press SELECT to obtain the numeric value associated with the mnemonic currently in the field, or press DON'T CARE to return the field to all don't cares (Xs).

DATA QUALIFICATION FUNCTIONS

The 91A24 offers special functions for qualifying data storage: BEGIN STORE IF, END STORE IF, and STORE ONLY IF. The following paragraphs describe how to use the Trigger Specification sub-menu to set up data qualification. They discuss each relevant field in the sub-menu and explain its optional values.

Figure 5 illustrates a typical 91A24 Trigger Specification sub-menu and its fields. Refer to the numbered callouts in Figure 5 when reading the following field descriptions.



4540-05

Figure 5. 91A24 Trigger Specification sub-menu and its data qualification functions. This example shows parallel BEGIN STORE and END STORE qualifiers.

④ BEGIN STORE/STORE ONLY IF Qualifier

(see Figure 5)

Press SELECT to choose between the following functions:

BEGIN STORE IF – the field's default function. When the event specified in the adjacent word recognizer fields is recognized, the DAS stores the BEGIN STORE and subsequent words until it recognizes an END STORE event. You can use the BEGIN STORE and END STORE functions to qualify specific blocks of data for storage.

NOTE

Data values entered in the sequential word recognizer, RESET word recognizer, and triggering parallel word recognizer are compared only to data that is qualified for storage. Therefore, values specified in these word recognizers must be a subset of qualified data.

STORE ONLY IF – directs the DAS to store a single cycle of data only if it meets the criteria you've specified in the adjacent word recognizer fields.

This function can be useful when you are interested in storing only a particular type of cycle, such as I/O reads.

⑤ Parallel Word Recognizer

(see Figure 5)

This field allows you to add a parallel ORed word recognizer for BEGIN STORE IF or STORE ONLY IF functions. It can also be used as a global ORed trigger word.

Press SELECT to obtain the following functions:

THEN – no operation is performed. The default value for this field. The DAS does not display data entry fields.

THEN WHEN...TRIGGER
THEN WHEN NOT...TRIGGER – both selections set up an ORed word recognizer for triggering. For details, refer to *Trigger Functions* in this section.

OR IF – provides a second word recognizer for the BEGIN STORE IF or STORE ONLY IF function (whichever is selected in the field directly above). The two word recognizers work in parallel and are logically ORed.

Using parallel word recognizers, you can specify two different recognition values for the same data qualification function.

⑥ END STORE Qualifier

(see Figure 5)

The END STORE function ends data storage until the DAS recognizes a BEGIN STORE data word. Up to two END STORE word recognizers are available.

Using BEGIN STORE and END STORE qualifiers, you can qualify specific blocks of data for storage and triggering. This allows you to avoid storing irrelevant data between occurrences of the target blocks.

NOTE

Data words which cause an END STORE to occur are not stored in the DAS acquisition memory.

In default, no data entry fields are displayed, and OFF is displayed in reverse video. When you select a value other than OFF, data entry fields appear to the right of the END STORE field.

NOTE

If you select the sub-menu's STORE ONLY IF function, the DAS turns the END STORE field OFF. Any END STORE values previously entered will be retained by the DAS, but are inactive.

Press SELECT to obtain the following END STORE options:

END STORE OFF – data storage is never disabled. This is the field's default value. No data entry fields are displayed.

END STORE IF – ends data storage if the value in the adjacent data entry fields is recognized.

BEGIN STORE has precedence over END STORE. For example, if you specify END STORE on all don't cares (Xs), the DAS stores only those words that match the BEGIN STORE value.

END STORE IF NOT – ends data storage if the data value is NOT recognized.

END STORE IF
OR IF – provides two parallel ORed word recognizers for the END STORE function. The DAS ends storage if it recognizes either of the data values.

TRIGGER FUNCTIONS

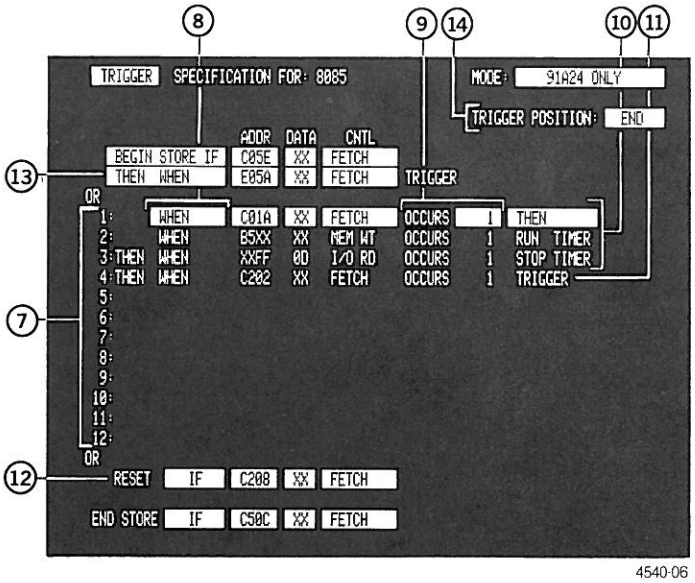
For triggering, the 91A24 offers a 16-level sequential word recognizer, a word recognizer which resets the sequential word recognizer, and a parallel word recognizer which can trigger independently of the sequential word recognizer.

NOTE

Data values entered in the sequential word recognizer, RESET word recognizer, and triggering parallel word recognizer are compared only to data that is qualified for storage. Therefore, values specified in these word recognizers must be a subset of qualified data.

The following paragraphs describe how to use the Trigger Specification sub-menu to set up trigger parameters. They discuss each relevant field in the sub-menu and explain its optional values.

Figure 6 illustrates a typical 91A24 Trigger Specification sub-menu and its fields. Refer to the numbered callouts in Figure 6 when reading the following trigger function descriptions.



4540-06

Figure 6. 91A24 Trigger Specification sub-menu and its trigger functions.

⑦ Sequential Word Recognizer

(see Figure 6)

The sequential word recognizer lets you build up to 16 levels of word recognition. You can use the sequential word recognizer for triggering and a variety of other actions.

The sub-menu also provides a RESET word recognizer which can return the sequential word recognizer to its first level. Note that if a sequential word recognizer value and the RESET value are recognized during the same clock cycle, no reset occurs.

At power-up there is one sequential word recognizer level. You can add and delete new word recognizer levels as you define the recognition sequence. You can display up to 12 levels on the screen at one time. If you are setting up more

than 12 levels, use the SCROLL keys to access the additional levels.

To add a level:

With the cursor placed in a sequential word recognizer level, press the ADD LINE key. (Note that a level may not be added while 12 levels are displayed and the cursor is positioned on the last one. Press the ∧ SCROLL key, then press ADD LINE.)

The DAS adds the new level below the current cursor position, then moves the cursor to the new level's far left data entry field.

To delete a level:

With the cursor on the level you wish to remove, press the DEL LINE key.

The DAS deletes the level and moves following levels up one. When there is only one level it cannot be deleted.

When data acquisition has begun and a sequential word recognizer level has not yet been satisfied, the message WAITING FOR LEVEL: [level#] appears on the second line of the display.

Individual fields of the sequential word recognizer are explained in the following paragraphs.

⑧ WHEN/WHEN NOT Field
(see Figure 6)

This is the first field in each level of the sequential word recognizer. It determines whether the DAS will look for the value in the word recognizer, or any value other than the one in the word recognizer.

Press SELECT to obtain the following options:

WHEN – the OCCURS count increments when data matches the value in the adjacent data entry fields. WHEN is the field's default value.

If you use the WHEN statement and don't use a RESET word, WHEN means that data values on this level will *eventually follow* those specified on the previous level.

If the WHEN statement is used in conjunction with a don't cared (Xed) RESET word, a new interpretation results: the values specified on this level must *immediately follow* the ones specified on the previous level, or the sequential word recognizer will be reset to the first level.

WHEN NOT – the OCCURS count increments when data does NOT match values in the data entry fields. Note that if the data value is all don't care's (Xs), the level will never be satisfied.

The WHEN NOT statement is most useful on the final level of the sequential word recognizer with a trigger action (TRIGGER or SYNC & TRG), and with a don't cared (Xed) RESET word. This setup allows you to trigger on intermittent problems. You set up the sequential word recognizer to match correct program flow, cycle-for-cycle. The don't cared RESET word will reset the sequential word recognizer after each correct execution of the sequence. The trigger occurs only if the data value in the WHEN NOT...TRIGGER level is not recognized.

⑨ OCCURS Field
(see Figure 6)

This field lets you specify the number of times an event must occur before the DAS performs the level's action and moves to the next level.

The field's default value is 1. You may specify a minimum of 1 and a maximum of 4096 occurrences.

To enter a value in the OCCURS field:

Use the DATA ENTRY keys.

To delete an OCCURS field value:

Press DON'T CARE. The field value changes to zero. Enter a value of at least one.

⑩ Intermediate Level Action Field
(see Figure 6)

When the OCCURS counter is satisfied on an intermediate level of the sequential word recognizer, this field tells the DAS what action to take before moving to the next level.

On the final level of the sequential word recognizer (or whenever there is only one level), the action field offers a different set of actions than for intermediate levels. For details, refer to *Final Level Action Field.*

Press SELECT to obtain the following intermediate level actions:

THEN – the field's default value. No action is performed. The DAS simply advances to the next level of the sequence.

RUN TIMER – starts a timer that measures 100 ns increments. The timer continues until a subsequent level with STOP TIMER is satisfied, a trigger occurs, or the STOP key is pressed.

If the timer is stopped and restarted on subsequent levels of the sequence, it counts accumulated time. If a RESET event is recognized while the timer is running, the timer stops and resets to 0 ns. Over 27 hours total elapsed time may be measured.

During an acquisition that uses the timer, elapsed time appears on the second line of any menu being displayed. When acquisition is completed, the DAS displays total elapsed time on the third line of the State Table menu.

NOTE

RUN TIMER and STOP TIMER will not appear in this field if you have selected INCR CNTR in the final level's action field. The counter and timer actions are mutually exclusive.

STOP TIMER – stops the timer. You can restart the timer by specifying RUN TIMER on a subsequent level.

SYNC OUT – directs the 91A24 to output a high TTL signal. The signal will remain high until a subsequent word recognizer level causes a different action.

NOTE

A delay of three master clock cycles + 45ns ±10ns exists between event occurrence in the system under test and the time that the signal is output by the 91A24's sync-out connector.

You could use this signal to trigger an oscilloscope.

⑪ Final Level Action Field

(see Figure 6)

On the final level of the sequential word recognizer (or when there is only one level), the actions available in this field are different from those on an intermediate level.

Press SELECT to choose from the following final level actions:

TRIGGER – triggers the 91A24. TRIGGER is the default value for this field.

When a trigger occurs, the DAS stops the timer and outputs a high TTL signal at the backpanel BNC connector labeled WORD RECOGNIZER OUTPUT.

INCR CNTR – increments the 91A24's counter each time the level is satisfied. The total count can consist of up to 12 decimal digits. During an acquisition that uses the counter, the current count appears on the second line of any menu being displayed. When the acquisition is completed, the total count appears on the third line of the State Table menu.

You can use INCR CNTR with the RESET word recognizer to count occurrences of a sequence. When the final sequence level is satisfied, the counter increments. Then, when the RESET value is recognized, the sequential word recognizer returns to level 1. You can use this setup to determine how many times the sequence occurred.

NOTE

INCR CNTR will not appear in this field if you have selected RUN TIMER in a preliminary level's action field. The counter and timer actions are mutually exclusive.

SYNC & TRG – causes the DAS to trigger and output a high-level TTL signal. (See *SYNC OUT*, described previously.)

NEVER TRG – causes the DAS to continue acquiring data without triggering. When the DAS encounters the NEVER TRG action, the message WAITING FOR MANUAL STOP appears on the second line of the display. (NEVER TRG does not reset or stop the timer.)

NOTE

If the independent trigger (specified in the parallel ORed word recognizer) recognizes a trigger event, it overrides NEVER TRG and the 91A24 triggers.

The NEVER TRG action could be used, for example, with SYNC OUT specified on another level of the sequential word recognizer, and with a RESET word. Using this setup you could repeatedly output the sync signal to an oscilloscope.

⑫ RESET Field

(see Figure 6)

The RESET word recognizer lets you specify an event that resets the sequential word recognizer. The reset occurs only if:

- the reset value and a sequential word recognizer value are not recognized simultaneously.
- a trigger has not already occurred.

Press SELECT to choose from the following RESET options:

OFF – the default value for this field. No data entry fields are displayed, and the sequential word recognizer is never reset.

NOTE

If you select any OR IF word recognizers, the DAS turns the RESET field OFF. The RESET and OR IF functions are mutually exclusive. Any RESET values previously entered will be retained by the DAS, but are inactive.

IF – data entry fields appear to the right. If the specified data value is recognized, the sequential word recognizer can be reset to its first level.

IF NOT – can reset the sequential word recognizer if the specified data value is NOT recognized.

If the sequential word recognizer's RUN TIMER action has started before a reset occurs, the timer stops and resets to 0 ns. If the INCR COUNTER action is used and a reset occurs, the counter is not reset.

⑬ Parallel Word Recognizer

(see Figure 6)

This field lets you set up a word recognizer for triggering that is independent of the sequential word recognizer.

Press SELECT to choose from the following options:

THEN – the field's default value. No data entry fields are displayed, and there is no operation performed.

THEN WHEN...TRIGGER – data entry fields appear to the right, followed by the statement TRIGGER. If the data value is recognized, the 91A24 triggers regardless of the sequential word recognizer state.

When a trigger occurs, the DAS stops the timer, and outputs a high TTL signal at the backpanel BNC connector labeled WORD RECOGNIZER OUTPUT.

NOTE

If you select the parallel OR IF word recognizer for the END STORE qualifier, the DAS removes the THEN WHEN and THEN WHEN NOT trigger selections and their data entry fields. Any data values previously entered will be retained by the DAS, but are inactive.

THEN WHEN NOT...TRIGGER– when the data value is NOT recognized, the 91A24 triggers.

OR IF – provides an ORed word recognizer for data qualification. For details, refer to *Data Qualification Functions* in this section.

You can use the independent trigger as the sole triggering word recognizer, and reserve the sequential word recognizer for other actions. Or, you can set up both as triggers to recognize different events. The independent trigger is ORed with the sequential word recognizer, so that the first one to recognize its trigger condition causes the 91A24 to trigger.

⑭ TRIGGER POSITION Field

(see Figure 6)

Once a trigger has occurred, the TRIGGER POSITION field determines when the resulting stop store is generated. The value you specify in this field establishes the trigger sequence's position relative to acquisition memory.

Press SELECT to choose from the following options:

BEGIN – positions the trigger as sequence 14, at the beginning of memory. Words 0-13 are data which preceded the trigger sequence.

CENTER – positions the trigger as sequence 510, at the center of memory. Words 0-509 are data which preceded the trigger sequence.

END – positions the trigger as sequence 1010, at the end of memory.

DELAY – when selected, an extra field appears directly below for entering a trigger delay value. The trigger sequence equals 1015 – DELAY value specified.

The default DELAY value is 1. You can delay the trigger from a minimum of 1 to a maximum of 32,767 clock cycles.

WORD RECOGNIZER OUTPUT

In addition to the sync-output signal described previously, the 91A24 generates a word recognizer output signal when the 91A24 triggers. Four master clock cycles after the trigger event occurs in the system under test, a high TTL signal is output through the BNC connector on the the mainframe backpanel labeled WORD RECOGNIZER OUTPUT.

TRIGGER INPUT

The DAS allows you to enable the sequential word recognizer using the rising edge of an external TTL-level signal. The parallel word recognizer trigger is enabled regardless of the trigger input signal.

As long as the trigger input signal remains low, the sequential word recognizer is disabled. When the input signal level goes high, triggering is enabled on the next clock cycle. The signal input location is the BNC connector on the mainframe backpanel labeled TRIGGER INPUT.

91A24 CLOCK SPECIFICATION SUB-MENU

To access the Clock Specification sub-menu, press SELECT in the Trigger Specification sub-menu's SPECIFICATION field.

This sub-menu is used to set up clocking for data acquisition. You can choose between internal and external clocking.

- **Internal Clock Configuration.** This is the default configuration for the Clock Specification sub-menu. You use it to set up an asynchronous internal clock rate for data acquisition.

  Use a fast internal clock to observe system-under-test timing.

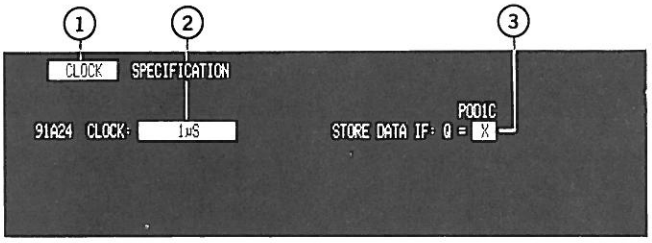
- **External Clock Configuration.** This sub-menu configuration lets you set up synchronous data acquisition. Its features let you set up clocking for complex systems, including those with multiplexed buses.

  Use external clocking to synchronize acquisition with the system-under-test's operation.

Details of the two clock configurations and their fields follow.

INTERNAL CLOCKING

The following paragraphs describe how to use the Clock Specification sub-menu to set up internal clocking. Figure 7 illustrates the default Clock Specification sub-menu and its fields. Refer to the numbered callouts in Figure 7 when reading the following field descriptions.



4540-07

Figure 7. Default Clock Specification sub-menu. The default sub-menu sets up the 91A24 with an asynchronous internal clock.

① SPECIFICATION Field
(see Figure 7)

This field lets you select between the Clock Specification and Trigger Specification sub-menus.

To move from one sub-menu to the other:

Press SELECT.

② 91A24 CLOCK Field
(see Figure 7)

This field has two functions: it allows you to select between internal and external clock specifications, and to set the internal clock rate. The field's default value is a 1 µs internal clock.

To set the internal clock rate:

Press the INCR key to increase the clock interval. Press the DECR key to decrease the interval.

The DAS displays increasing and decreasing interval values in a 1-2-5 sequence, ranging from 100 ns minimum to 5 ms maximum.

To select the external clock configuration:

Press the SELECT key.

The DAS displays the value EXTERNAL, and new fields appear in the sub-menu. Values previously specified for internal clocking are retained but inactive.

For details of the external clock configuration and its use, refer to the following *External Clocking* discussion.

③ STORE DATA IF Field
(see Figure 7)

The STORE DATA IF field lets you set up qualification of the DAS internal clock using the 91A24's pod C qualifier (Q) line. (POD identification over this field indicates which mainframe slot holds the 91A24 module.) When the qualifer line is connected to a signal in your system under test, that signal's state can be ANDed to the internal clock. In this way the DAS acquires data only when the qualifier is true.

You can assert the qualifier as positive true (1) or negative true (0). In default, the STORE DATA IF field is set to don't care (X), so that the qualifier signal is not asserted.

To assert the clock qualifier:

Enter a 1 or a 0, using the data entry keys.

NOTE

Only data which is qualified for storage can be compared for word recognition. When using the clock qualifier, make sure that the Trigger Specification sub-menu's recognition values are a subset of qualified data.

EXTERNAL CLOCKING

In its external clock configuration, the Clock Specification sub-menu lets you synchronize data acquisition with operation of the system under test. It also offers a simple setup for demultiplexing data.

The following paragraphs describe how to use the Clock Specification sub-menu to set up external clocking. Figure 8 illustrates the Clock Specification sub-menu and its fields configured for external clocking. Refer to the numbered callouts in Figure 8 when reading the following field descriptions.

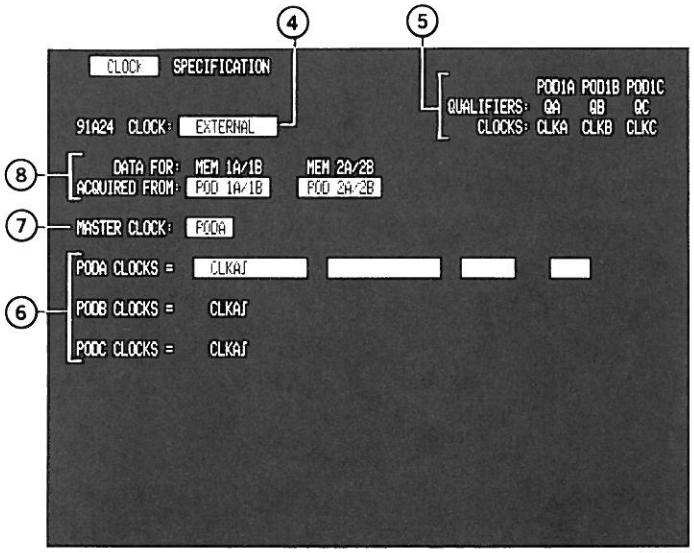


Figure 8. Clock Specification sub-menu configured for external clocking.

④ 91A24 CLOCK Field

(see Figure 8)

By pressing SELECT, this field lets you choose between the internal clock and external clock configurations. Any values entered for the previous clocking configuration are retained but inactive.

⑤ Clocks and Qualifiers Index

(see Figure 8)

The clocks and qualifers index indicates which mainframe slot holds the 91A24 module, and therefore which probes' clock and qualifier lines are available. The 91A24 is the only module that receives clock and qualifier signals; 91AE24 expander modules do not.

If the 91A24 is installed in mainframe slot 2, for example, its probes will be indexed as POD2A, POD2B, and POD2C. These will be the pods you can use to input clock and qualifier signals.

⑥ POD CLOCK Expressions

(see Figure 8)

The PODA CLOCK, PODB CLOCK, and PODC CLOCK expressions specify when each pod's data is clocked for storage. With one or more 91AE24s installed, each module's pod A data is clocked by PODA CLOCKS, each module's pod B data is clocked by PODB CLOCKS, and each module's pod C data is clocked by the PODC CLOCKS expression.

To form each pod clock expression, you can use all three clock signals (CLKA, CLKB, and CLKC) and all three qualifier signals (QA, QB, and QC). Pods attached to the 91A24 input clock and qualifier signals; 91AE24 expander module pods do not. Figure 10 shows how the pod clock expressions are related to data acquisition.

As shown in Figure 10, there are four fields available to form each pod clock expression. These fields represent terms in a logic equation. In each pod clock field, you can choose from a set of optional terms.

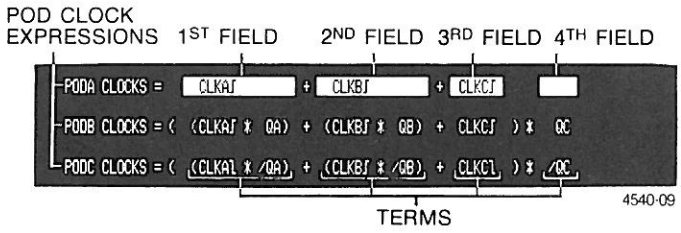


Figure 9. Pod clock expressions and their fields.

The following list defines symbolic characters used within and between terms of the pod clock expressions:

*	=	AND
+	=	OR
/	=	NOT - electrical low level of signal
∫	=	rising edge of signal
⌊	=	falling edge of signal
( )	=	indicate precedence of operators

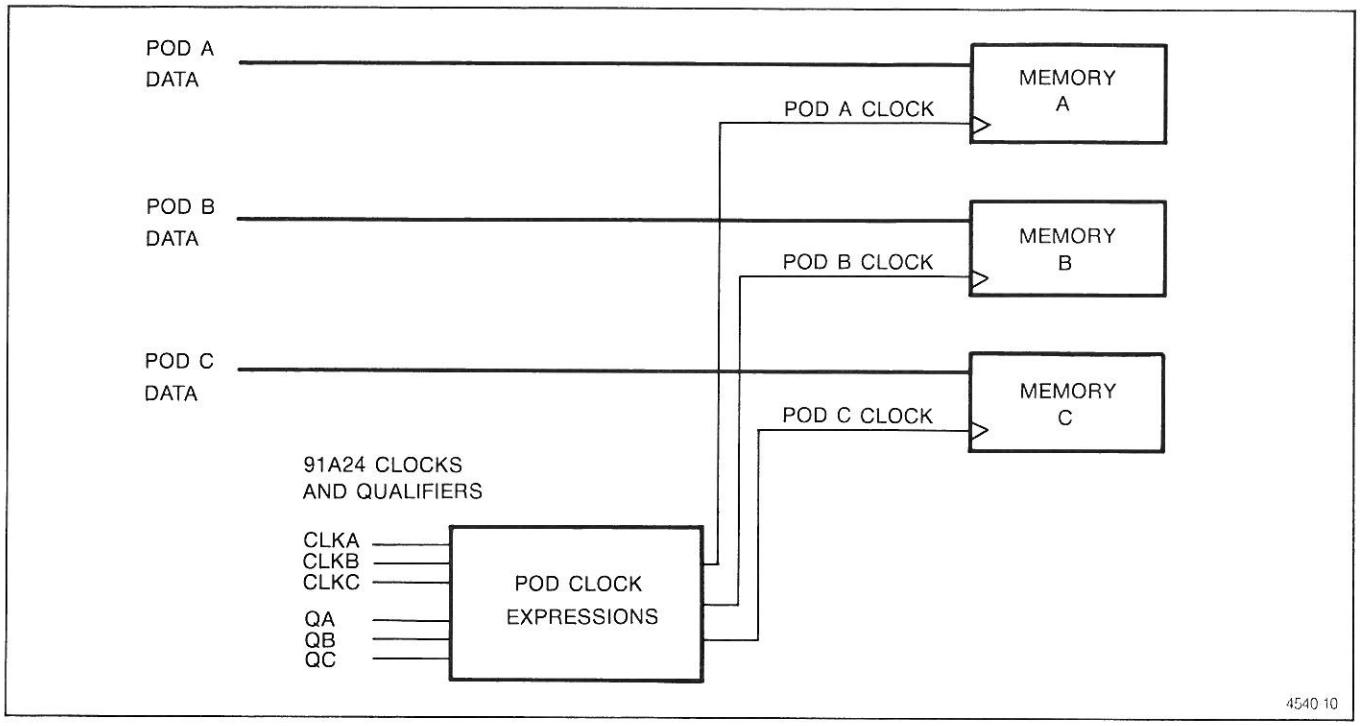


Figure 10. External clocking and acquisition. This illustration shows how clocks, qualifiers, and data are collected. All three clocks and all three qualifiers are available to form each pod clock expression.

In default, the first field of each pod clock expression is set to the rising edge of CLKA. Fields following the first terms are empty, so that the clock and qualifier lines corresponding to these fields are not used. Therefore, each pod's data will be clocked on the rising edge of CLKA.

Pod clock expressions must have at least one term. If you leave all fields in an expression empty and attempt to leave the sub-menu, the DAS displays the message MUST ASSIGN AT LEAST ONE CLK TO POD.

To select optional terms in a clock expression (see Figure 9):

Press the SELECT key in a pod clock field.

In the PODA CLOCK, PODB CLOCK, and PODC CLOCK fields, optional terms are rotated in the following order:

1st field:
- CLKA ⎍ — *default*
- CLKA ⎏
- (CLKA ⎍ * QA)
- (CLKA ⎏ * QA)
- (CLKA ⎍ * /QA)
- (CLKA ⎏ * /QA)
- Empty

2nd field:
- Empty — *default*
- CLKB ⎍
- CLKB ⎏
- (CLKB ⎍ * QB)
- (CLKB ⎏ * QB)
- (CLKB ⎍ * /QB)
- (CLKB ⎏ * /QB)

3rd field:
- Empty — *default*
- CLKC ⎍
- CLKC ⎏

4th field:
- Empty — *default*
- QC
- /QC

To remove a term from a clock expression:

Press the DON'T CARE key in the field whose term you want to delete.

Terms in pod clock expressions are linked in a specific way. Any of the first three terms used are ORed together. The fourth term, if used, is always ANDed to the quantity of the first three terms. The DAS displays +, *, and ( ) symbols between terms accordingly.

When using clock and qualifier lines, keep the following points in mind:

- Clock lines are edge-sensitive.
- Qualifier lines are level-sensitive.
- CLKA, CLKB, and CLKC, whichever are used, are ORed together.
- QA, when used, is ANDed to CLKA.
- QB, when used, is ANDed to CLKB.
- QC, when used, is ANDed to the quantity of all other terms used in the clock expression.

Clocking Constraints. The following guidelines must be observed when setting up external clocking for 91A24/91AE24 modules:

- The active edge of each clock signal (CLKA, CLKB, and CLKC) must be separated from the other signals' active edges by at least 20 ns.
- Clock signals must have a pulse width (high and low) of at least 25 ns.
- One or more pod clock expressions can come true simultaneously, provided this results from using the same clock (CLKA, CLKB, or CLKC) signal.
- One pod clock expression must come true first during each system-under-test bus cycle. This clock expression, defined as the master clock, must come true only once per bus cycle, and can occur at a rate no greater than 10 MHz. (See the *Master Clock Field* discussion.)
- Other pod clock expressions may come true more than once during a master clock cycle, but at a rate no greater than 10 MHz. Only the last data clocked before the next master clock occurs is stored in acquisition memory.

⑦ MASTER CLOCK Field
(see Figure 8)

This field tells the DAS which pod clock expression comes true first during each system-under-test bus cycle. The DAS uses the master clock definition to align data on a cycle-by-cycle basis.

When the master clock expression comes true, data last clocked by the PODA, PODB, and PODC CLOCK expressions is stored in memory. To ensure that data is properly aligned in memory, the master clock should occur only once per bus cycle.

The master clock expression can come true simultaneously with other clock expressions, provided this results from using the same clock signal (CLKA, CLKB, or CLKC).

In default, the pod A clock expression is defined as the MASTER CLOCK.

To specify the MASTER CLOCK:

Press the SELECT key. You can specify the PODA, PODB, or PODC clock expression as the master clock.

Data clocked by the master clock expression, and data from the pods clocked simultaneously or following will be aligned as parts of the same acquisition memory sequence.

⑧ DATA FOR / ACQUIRED FROM Field
(see Figure 8)

This field lets you demultiplex data without double probing. As shown in Figure 11, data is demultiplexed by setting up two different pod clock expressions for the same pod. The demultiplexed data is stored in two memories.

91A24 and 91AE24 modules can demultiplex eight channels each. An additional field appears for each 91AE24 installed, so that you can select demultiplexing on a module-by-module basis.

Only pod A of each module may demultiplex data. When a module's pod A is set up for demultiplexing, that module's pod B data lines are not connected. If the 91A24 module is used for demultiplexing, its pod B clock (CLKB) and qualifier (QB) lines are still active.

Pod A and pod B clock expressions demultiplex pod A data. The pod A clock expression determines when one piece of data (a data byte, for example) is stored in a module's memory A. The pod B clock expression clocks the other piece of data (perhaps the high-order address byte) at a different time into that module's memory B.

NOTE

In the Channel Specification menu, data that is acquired by pod A and stored in memory B is listed in the PROBE column as POD B.

To set up POD A demultiplexing:

Press the SELECT key.

The default value POD A/POD B changes to POD A. (The letters A and B are preceded by the module's slot number.) Data for memories A and B will now be acquired by pod A, and clocked by the PODA CLOCK and PODB CLOCK expressions.

To return to normal acquisition:

Press the SELECT key.

The value POD A/POD B will be displayed.

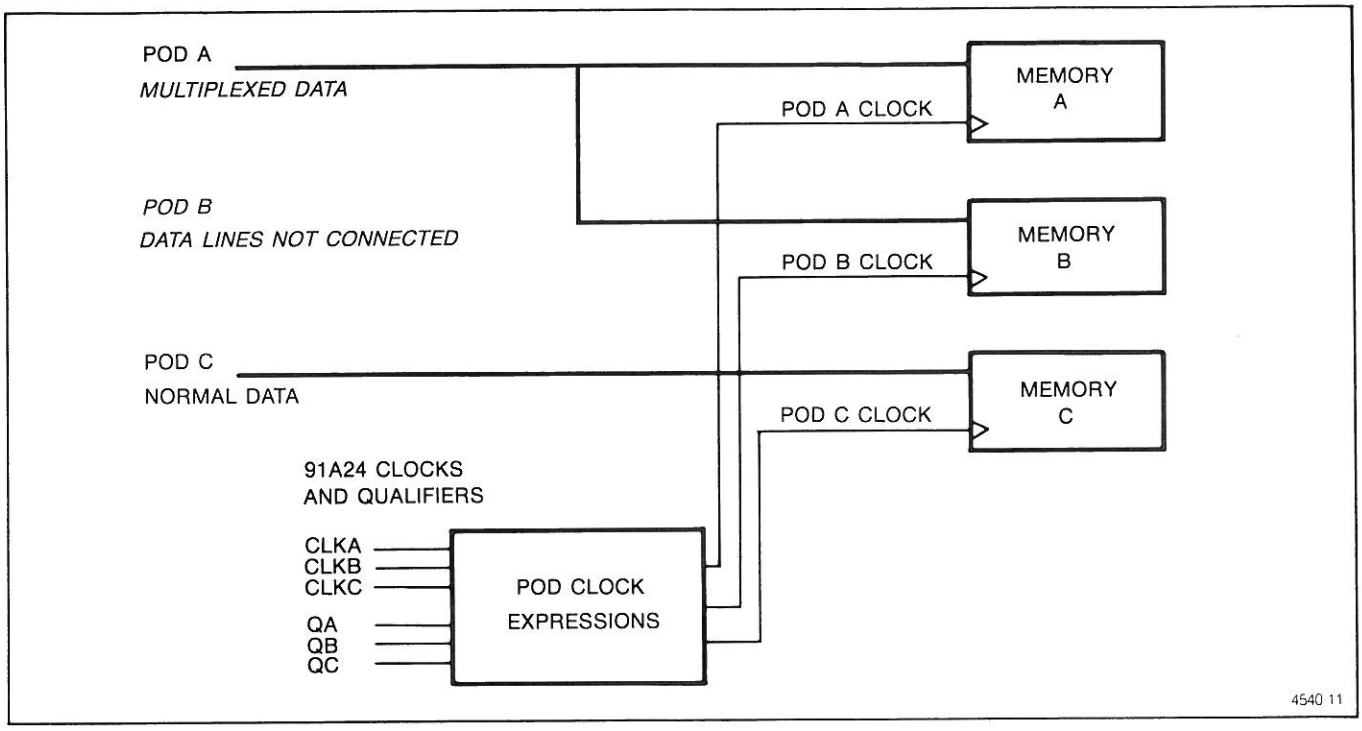


Figure 11. Demultiplexed acquisition.

91A24 ARMS MODE

The 91A24 can be used in ARMS mode with high-speed data acquisition modules, such as the 91A04. In ARMS mode, the 91A24 and the high-speed module act as linked logic analyzers. While both modules start acquiring data at the same time, their triggers occur separately. The 91A24 triggers first, then arms the high-speed module to look for its trigger.

ARMS mode supports any combination of 91A24/91AE24 and high-speed modules, so long as they do not exceed their individual limits or the maximum of 104 channels.

NOTE

The 91A24 does not operate in ARMS mode with 91A32 modules.

SUB-MENU ORGANIZATION

In 91A24 ARMS mode, the Trigger Specification and Clock Specification sub-menus operate as described previously in this section.

NOTE

When in ARMS mode, selections in the 91A24's TRIGGER POSITION field place the trigger sequence differently: BEGIN=14, CENTER=254, END=494, and DELAY=504–[delay value].

To set up ARMS mode:

Set up the high-speed module's clocking and triggering in its Trigger Specification ONLY mode. (High-speed modules' ONLY mode fields and values are described in the *DAS 9100 Series Operator's Manual*.)

Set up 91A24 triggering in the 91A24 Trigger Specification sub-menu.

Set up 91A24 clocking in the 91A24 Clock Specification sub-menu.

Before starting acquisition, select 91A24 ARMS [high-speed module].

CONDITIONS FOR TIME-ALIGNMENT

You can set up the 91A24 and high-speed modules' clocking and triggering any way you wish. However, to acquire and display time-aligned ARMS data, the following requirements must be met:

- The high-speed module must acquire data at a rate that is at least twice as fast as the 91A24 module.
- Both the 91A24 and high-speed module triggers must be positioned within the first 512 memory sequences. The 91A24 trigger can be delayed, but the DELAY value must be no greater 500.
- The 91A24 and high-speed module's triggers must occur so that at least five 91A24 clock cycles are overlapped by high-speed clock cycles.
- High-speed module clock qualifiers are not used.
- 91A24 data qualification is not used. (Use of 91A24 clock qualifiers is permitted.)

ARMS ACQUISITION DISPLAY

If all time-alignment conditions are met, the State Table and Timing Diagram menus will display the ARMS acquisition in its proper time relationship.

If any time-alignment conditions are not met, the State Table and Timing Diagram menus will display ARMS acquisition in a fence display format. The fence separates slow- and fast-clocked data stored in the two memories.

For additional information, refer to *State Table Menu* and *Timing Diagram Menu* in this manual.

STATE TABLE MENU

ADDITIONS WITH FIRMWARE VERSION 1.11

The following paragraphs describe only special display considerations as they apply to Version 1.11 and to 91A24/91AE24 data. For specific information on how to operate the State Table, refer to *State Table Menu* in the *DAS 9100 Series Operator's Manual.*

PAGE SCROLLING

Version 1.11 provides a page scrolling feature for the State Table menu.

To display an adjacent page of memory:

With the cursor in a sequence (SEQ) field, press the SHIFT and Δ or ∇ SCROLL keys simultaneously.

The DAS displays the adjacent page of memory starting at the cursor location. You can page at high speed by holding the keys down.

COUNTER/TIMER DISPLAY

If you have selected either the RUN TIMER or INCR CNTR actions in the 91A24 Trigger Specification sub-menu's sequential word recognizer, the total count will be displayed on the third line of the State Table menu.

For details of counter/timer operation, refer to *Trigger Functions* in the *Trigger Specification* section of this manual.

ACQUISITION MEMORY DISPLAY

The State Table's acquisition memory display shows up to 1023 sequential data words (numbered 0—1022) acquired by 91A24/91AE24 modules.

ARMS ACQUISITION DISPLAY

In 91A24 ARMS mode, only the first 512 sequences of 91A24 memory are displayed.

If the conditions listed for time-alignment (see *91A24 ARMS Mode*) are met, the State Table displays 91A24 data and high-speed module data with the proper time relationship.

If time-alignment conditions are not met, a horizontal fence separates the 91A24 and high-speed modules' data display.

REFERENCE MEMORY DISPLAY

The reference memory can be used to store a maximum of 1023 sequences. This number decreases depending on channel width, the amount of data acquired by a high-speed module (when using ARMS mode), and the number and length of mnemonics tables (which share this memory space in the DAS).

For example, if you are acquiring 48 channels of 91A24 data, you can store 1023 sequential data words in the reference memory. If you are acquiring 96 channels of data, you can store at least 512 sequential data words. As you add mnemonics tables and acquisition channels, the number of sequences you can store in reference memory decreases.

For details of reference memory use, refer to *State Table Menu* in the *DAS 9100 Series Operator's Manual*, and to the *Define Mnemonics Addendum.*

TIMING DIAGRAM MENU

For specific information on how to operate the Timing Diagram menu, refer to *Timing Diagram Menu* in the *DAS 9100 Series Operator's Manual*. The following paragraphs describe only those aspects of the display that apply specifically to 91A24/91AE24 data.

ACQUISITION DISPLAY

The Timing Diagram menu displays memory data in 512-word blocks. To see which 512 words are being displayed, set the MAG (magnification) field to 1 and look at the memory window. Memory search functions operate on the 512-word block currently being displayed.

To view a new block of memory:

Scroll the cursor (C) line to the left to see data towards the beginning of memory, or to the right to see data towards the end of memory. When the cursor reaches the end of the 256-sequence block, the menu shifts the cursor back to the center of the screen and shows the next block.

An alternative method for viewing another block of memory is to enter the State Table menu, specify the desired memory sequence (SEQ) number, and then return to the Timing Diagram menu.

ARMS ACQUISITION DISPLAY

In 91A24 ARMS mode, only the first 512 sequences of 91A24 memory are displayed.

If the conditions listed for time-alignment are met (see *91A24 ARMS Mode*), the Timing Diagram menu displays the fast-clocked data and slow-clocked 91A24 data in the proper time relationship.

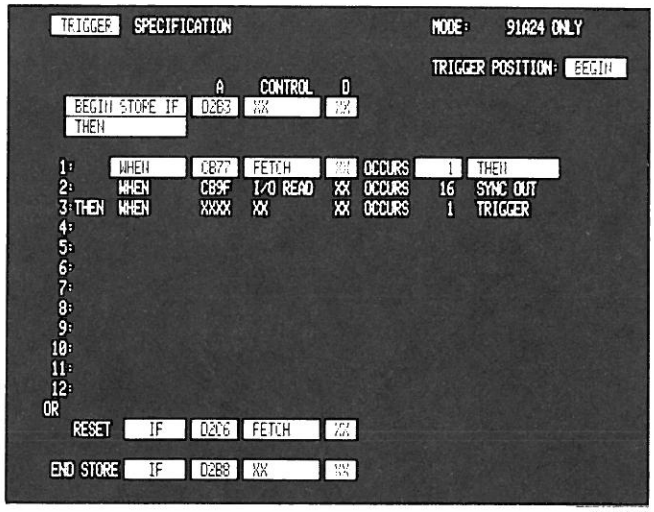
If the time-alignment conditions are not met, a vertical fence separates fast- and slow-clocked data.

DEFINE MNEMONICS MENU
ADDITIONS WITH FIRMWARE VERSION 1.11

Firmware Version 1.11 adds three mnemonics features for the 91A24 Trigger Specification sub-menu controlled through the Define Mnemonics menu, and also adds a new system call.

WORD RECOGNIZER MNEMONICS

Word recognizer data entry fields in the 91A24 Trigger Specification sub-menu allow you to enter mnemonics and their associated numeric values. The mnemonics and their values are obtained from special tables that you set up in the Define Mnemonics menu. Figure 12 shows the appearance of the 91A24 Trigger Specification sub-menu when mnemonics are used to denote data values.



4540 12

Figure 12. Using mnemonics for word recognition in the 91A24 Trigger Specification sub-menu.

Mnemonics for the 91A24 Trigger Specification sub-menu must be defined in tables named [group]*, where [group] is the name of a channel group (A - F, 0 - 9) for which the mnemonics are defined. For example, if you want to specify recognition mnemonics for channel group C, you create a table named C*. If you also want mnemonics for channel group A values, you create another table named A*. An example of a [group]* table is shown in Figure 13.

In order to obtain mnemonics in the 91A24 Trigger Specification sub-menu, the [group]* table must meet the following conditions:

- The [group]* table must be a DEFAULT table as controlled from the Table Definition sub-menu.
- The [group]* table must only receive passed bits. The number of bits passed to the [group]* table must equal the number of channels in the corresponding channel group.
- Mnemonics in [group]* tables should be no longer than eight characters. In the data entry fields, additional characters are truncated.

Once you have listed mnemonics and associated data values in a [group]* table, you can use its mnemonics to replace numeric data entry in the 91A24 Trigger Specification sub-menu.

For details on specifying mnemonics in data entry fields, refer to *Mnemonics Functions* in the *Trigger Specification* section of this manual.

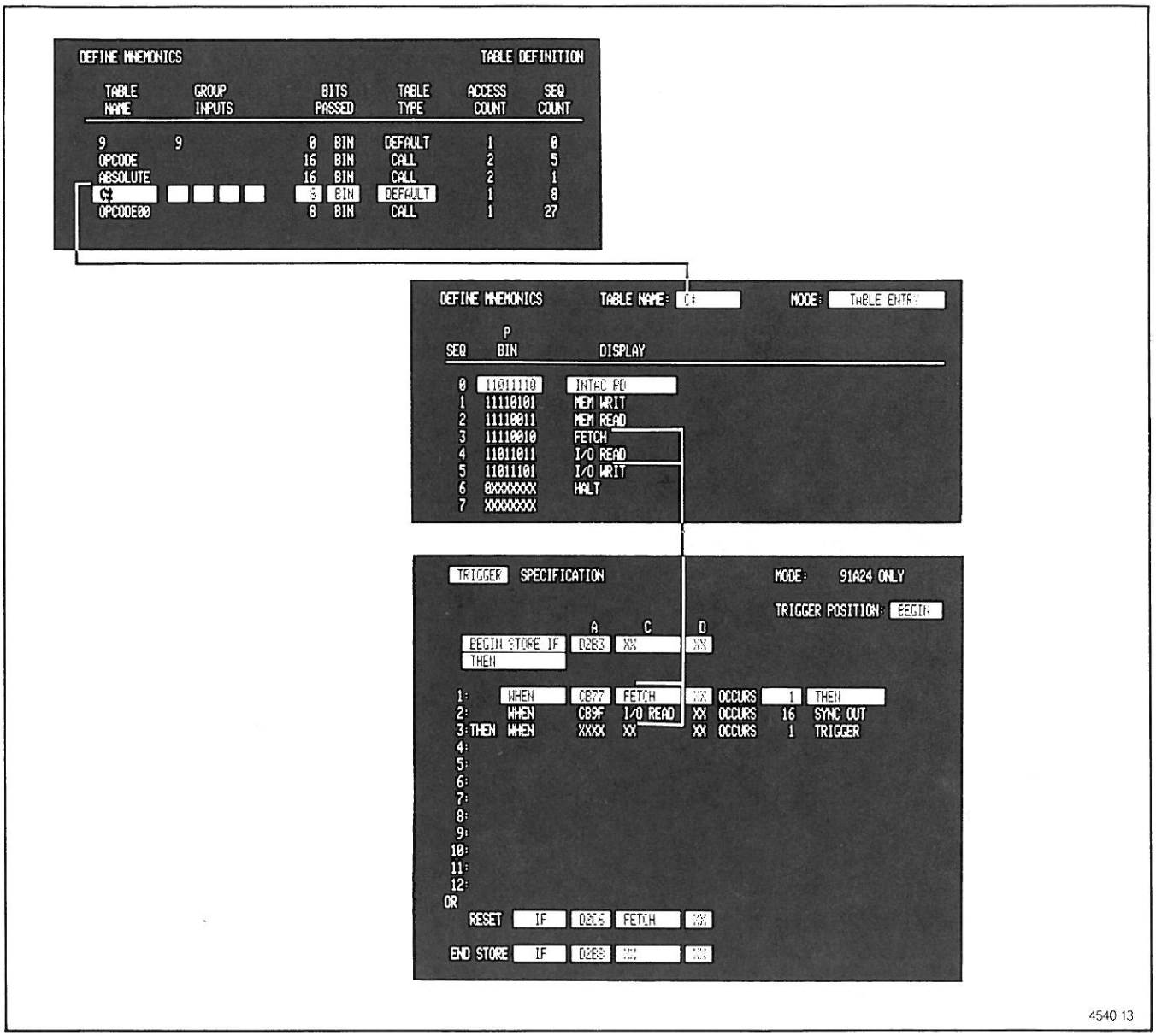


Figure 13. How creating a [group]* table provides word recognizer mnemonics for the 91A24 Trigger Specification sub-menu. The table C* provides mnemonics (in this case, bus cycle types) for channel group C data entry fields.

GROUP HEADINGS FOR THE 91A24 TRIGGER SPECIFICATION SUB-MENU

There are two ways to change group column headings in the 91A24 Trigger Specification sub-menu:

- When you enter a GROUP HEADING in the Define Mnemonics Display Setup sub-menu, that heading appears over the channel group's data entry column.
- When you specify a MICRO NAME in the Define Mnemonics Table Definition sub-menu, the A, C and D group column headings are automatically labeled ADDR, CNTL, and DATA. No other group column headings are affected by the MICRO NAME field.

DISPLAYING MICRO NAMES

As shown in Figure 14, when you enter a name in the MICRO NAME field of the Define Mnemonics Table Definition sub-menu, that name appears in the State Table menu, and in the 91A24 Trigger and Clock Specification sub-menus.

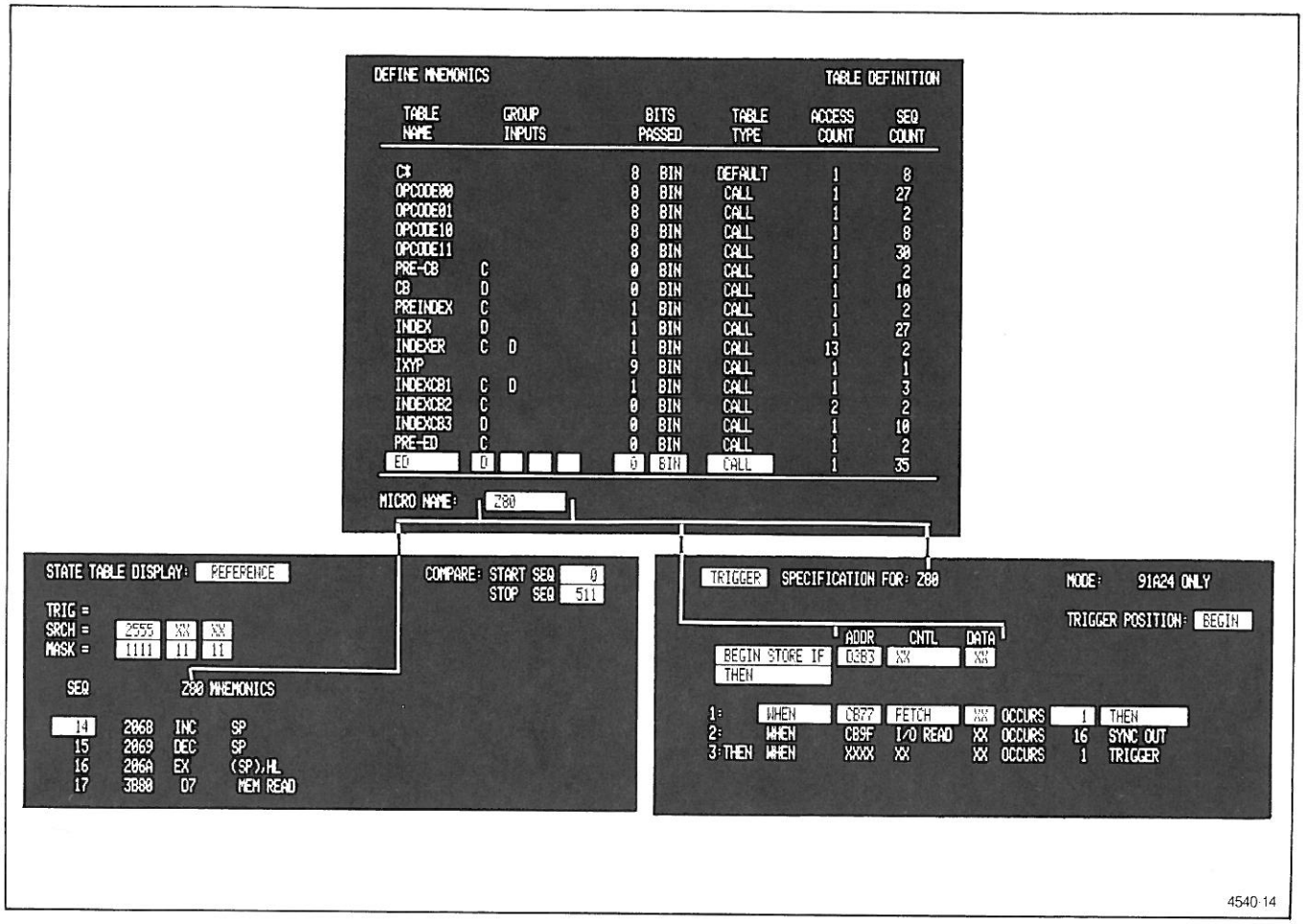


Figure 14. Changes in the State Table menu and 91A24 Trigger Specification menu caused by the MICRO NAME field. The name in the MICRO NAME field is displayed by both the 91A24 Clock and Trigger Specification sub-menus. ADDR, CNTL, and DATA headings appear over data entry columns for groups A, C, and D in the 91A24 Trigger Specification sub-menu.

NEW SYSTEM CALL

***TSTMARK.** This system call tests the acquisition sequence currently being disassembled to determine whether it was previously marked by the *MARK system call. If the acquisition sequence was not *MARKed, disassembly continues uninterrupted. If the acquisition sequence was *MARKed, *TSTMARK calls a user-defined table named MARK*. Pass bits to table MARK* through the *TSTMARK system call.

For details of the *MARK system call, refer to the *Define Mnemonics Addendum.*

APPLICATION EXAMPLES

These application examples are provided to demonstrate the use of 91A24/91AE24 modules. The examples are based on the 8085 microprocessor, but can be generalized to apply to systems based on other processors. The application examples show:

- connections to the system under test
- external clock setup, demultiplexing
- triggering techniques
- storage qualification
- use of the timer and counter

SYSTEM SETUP

The DAS equipment setup used for these application examples is as follows:

91A24 Data Acquisition Module, installed in mainframe slot 1.

91AE24 Data Acquisition Module, installed in mainframe slot 2.

Four data acquisition probes, connected to 91A24 pod connectors 1A, 1B, 1C, and to 91AE24 pod connector 2A.

Universal Probe Interface Kit. (Optional. Connection of leads is detailed under *Connections to the 8085*, which follows.)

91TM02 — 8085 Mnemonics Tape. (Optional. This tape programs the DAS acquisition and mnemonics setups for 8085 acquisition and disassembly. You can also enter these setups manually. The DAS 9100 Series Mnemonics Tapes cover a range of microprocessors, buses, and communication codes.)

For details of module installation and probe connection, refer to the *Operating Instructions* sections of this manual and of the *DAS 9100 Series Operator's Manual.*

CONNECTIONS TO THE 8085

The lead connections shown in Figure 15 can be made with or without the Universal Probe Interface Kit. However, the kit is recommended because it allows you to create a fast, dedicated lead setup for connections to your microprocessor. Refer to instructions included with the kit for details of its use. Figure 15 is a pinout of the 8085 microprocessor showing 91A24/91AE24 probe connections. The pod numbers shown in the diagram assume that the 91A24 is installed in slot 1 of the mainframe, and that the 91AE24 is installed in slot 2.

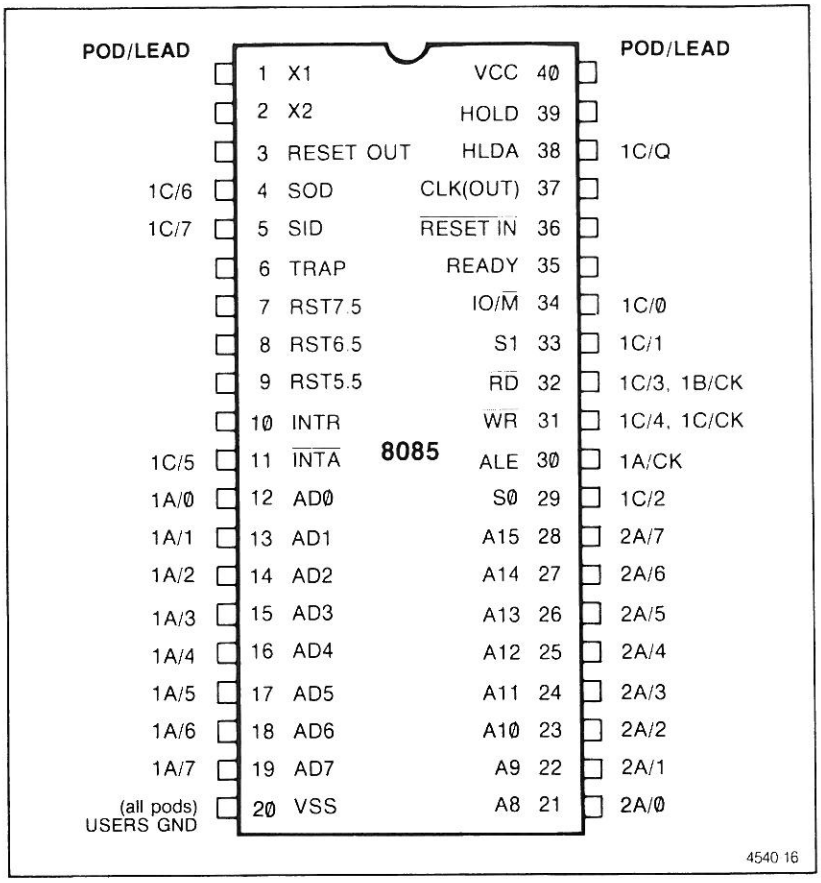


Figure 15. Connections to the 8085 microprocessor.

CLOCKING

In this application example, the 91A24 and 91AE24 modules use external clocking to acquire bus information from the 8085. In this way, acquisition is synchronized with the 8085 system's operation.

SETTING UP DEMULTIPLEXING

91A24 and 91AE24 modules allow you to demultiplex data without double probing. Data acquired by a module's pod A is clocked at two different times in the bus cycle, and stored in two memories. When a module is not set up for demultiplexing, the second memory is used for pod B data; when demultiplexing is set up, memory B stores demultiplexed data from pod A, and pod B is not connected.

In this application example, pod 1A leads are connected to the 8085's multiplexed address/data lines AD0-AD7. Pod 1B's data lines are not connected. As will be shown when setting up clock expressions, A0-A7 are clocked early in the bus cycle and stored in pod 1A memory. D7-D0 are clocked later in the bus cycle and stored in pod 1B memory.

As shown in Figure 17, this pod/memory arrangement is specified in the Clock Specification sub-menu's ACQUIRED FROM field. The field's default value POD 1A/1B is changed to POD 1A.

SETTING UP CLOCK EXPRESSIONS

The quickest way to choose signals for clocking is to examine a system timing diagram. Figure 16 shows general system timing for the 8085 microprocessor, and the desired 91A24 acquisition times.

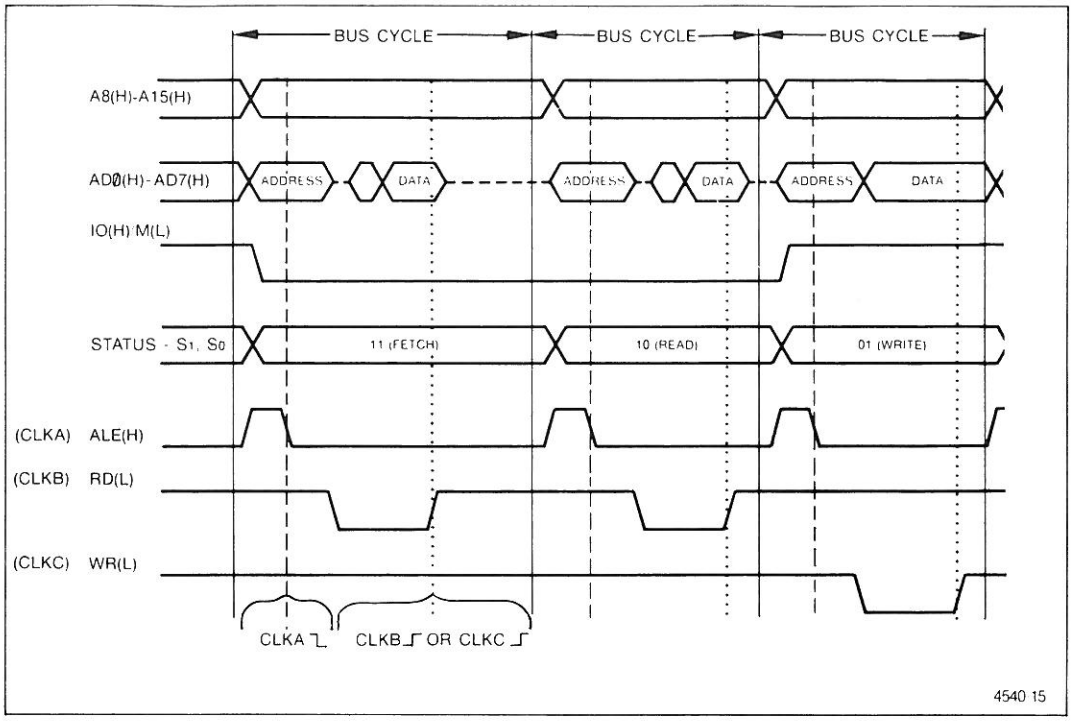


Figure 16. 8085 bus timing and 91A24 clocking. The falling edge of ALE(H) clocks the high- and low-order address bytes. Either the rising edge of RD(L) or the rising edge of WR(L), whichever is true on the bus cycle, clocks the data byte, control signals, and status signals.

The 8085 signals ALE(H), RD(L), and WR(L) are suitable clocking signals. Address information is valid on the falling edge of ALE(H), Address Latch Enable. Data and control lines are valid on the rising edge of either RD(L) or WR(L), whichever is true on the bus cycle. As shown in Figure 17, the Clock Specification sub-menu is set up with the appropriate clock expressions.

PODA CLOCKS — clocks pods 1A and 2A, which carry the low- and high-order address bytes. Because ALE(H) is acquired by the 91A24's pod A clock lead, the sub-menu labels it CLKA.

PODB CLOCKS — clocks the data byte. Recall that pod 1A acquires multiplexed address and data. Because demultiplexing is set up in the ACQUIRED FROM field, the pod B clock expression clocks pod 1A data into pod 1B memory.

Because RD(H) and WR(H) are acquired by the 91A24's pod B and pod C clock leads, the sub-menu labels the signals as CLKB and CLKC.

PODC CLOCKS — clocks pod 1C, which carries control signals. This clock expression is the same as PODB CLOCKS.

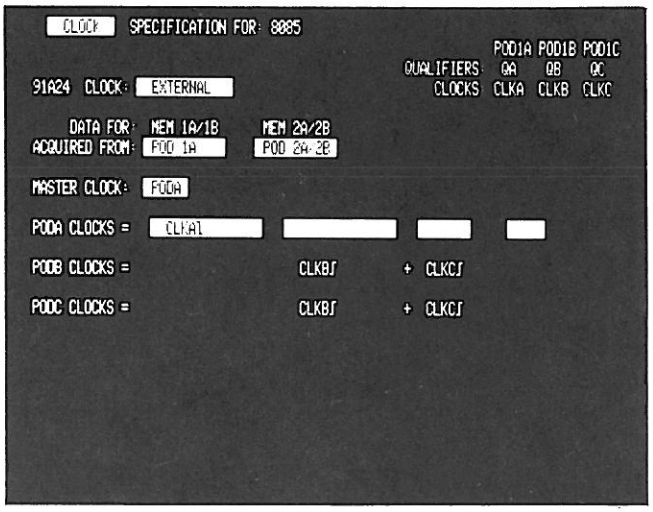


Figure 17. Clock Specification sub-menu setup for 8085.

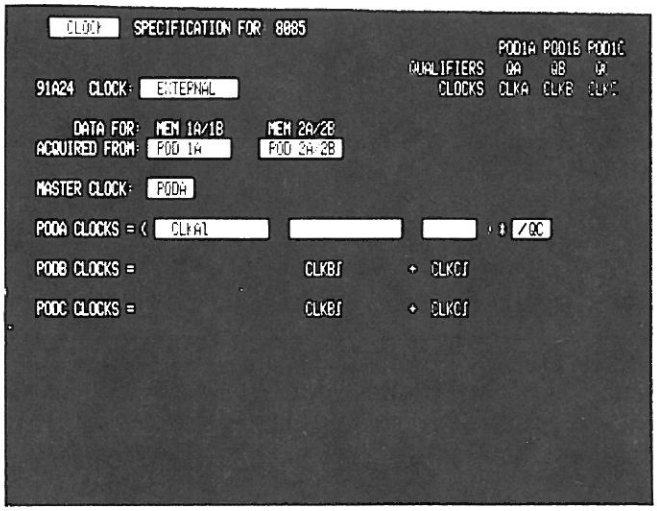
DEFINING THE MASTER CLOCK

Note that in Figure 16, the pod A clock expression is the first to come true during each 8085 bus cycle. Therefore, the MASTER CLOCK field is set to PODA. This ensures that each bus cycle's address, data, control, and status information are aligned in acquisition memory.

SETTING UP A DMA QUALIFIER

The 91A24's qualifier lines allow you to prevent acquisition of unwanted or invalid data. For instance, the 8085 can release control of the system bus for direct memory access (DMA) operations. When the 8085 Hold Acknowledge (HLDA(H)) signal is high, the 8085 no longer has control of the bus.

It is possible to prevent acquisition of these cycles by connecting the 91A24's pod C qualifier lead to HLDA(H). In the clock specification sub-menu, this qualifier signal can be logically ANDed to each clock expression. Alternatively, it can be ANDed just to the master clock expression (PODA CLOCKS) with the same result. (If the master clock expression doesn't come true, no other data clocked in that bus cycle will be stored in memory). The sub-menu labels the signal as QC.



4540 17

Figure 18. Using /QC to eliminate acquisition of DMA cycles.

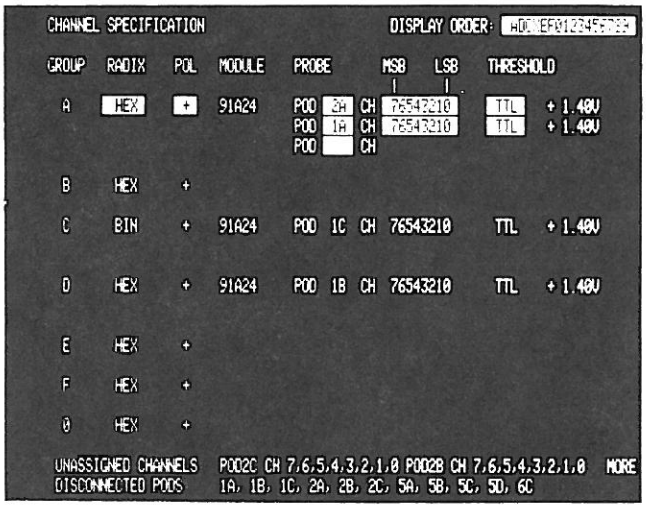
By specifying /QC, bus cycles will be acquired only when HLDA(H) is low. The qualified master clock expression is shown in Figure 18.

CHANNEL GROUPING

Figure 19 shows the Channel Specification menu as it is set up by the 8085 Mnemonics Tape (91TM02).

There are three special items to note in this Channel Specification menu setup:

- Address lines are placed in group A, control lines are placed in group C, and data lines are placed in group D. As explained in the *Define Mnemonics Menu* section of this manual, this channel grouping must be used to obtain the word recognizer headings ADDR, CNTRL, and DATA. The headings appear when a MICRO NAME is entered in the Table Definition sub-menu of the Define Mnemonics menu.
- In Group D's POD field, POD 1B is specified. Although data is actually acquired from the 8085's multiplexed address/data lines by pod 1A, it is demultiplexed into pod 1B's memory, and labeled by the Channel Specification menu as POD 1B.
- The DISPLAY ORDER field is changed so that groups A, C, and D are displayed in the order A, D, and C. This is done so that address and data will be adjacent in the Trigger Specification sub-menu and State Table menu.



4540 18

Figure 19. 8085 Channel Specification setup.

TRIGGERING AND DATA QUALIFICATION

This portion shows how you could examine some typical problems using the Trigger Specification sub-menu. There are usually several ways to approach such problems. These examples are designed to demonstrate the 91A24's capabilities.

TIMING WORST-CASE EXECUTION

Problem: Need to determine the time efficiency of a proposed sorting algorithm (listed in Figure 20).

Objective: Time each pass through the compare/swap loop, since this is where the routine spends the most time.

```
;Sub-routine for sorting 256-byte array into non-increasing order

C000   06 00            SORT:    MVI    B,0          ;set up loop counter for 256
C002   21 01 BC                  LXI    H,0BC00H     ;set up pointer to array
C005   4E                        MOV    C,M          ;pick up array length
C006   0D                        DCR    C
C007   23                        INX    H
C008   73              LOOP:    MOV    A,M          ;pick up first byte
C009   23                        INX    H            ;advance array pointer
C00A   BE                        CMP    M            ;compare to second byte
C00B   D2 15 C0                  JNC    NO SWAP      ;jump if no swap needed
C00E   56                        MOV    D,M          ;swap bytes
C00F   77                        MOV    M,A
C010   2B                        DCX    H
C011   72                        MOV    M,D
C012   23                        INX    H
C013   06 01                     MOV    B,1
C015   0D              NO SWAP: DCR    C            ;decrement array length pointer
C016   C2 08 C0                  JNZ    LOOP         ;repeat until end of array
C019   05                        DCR    B            ;decrement outer loop counter
C01A   CA 00 C0                  JZ     SORT
C01D   C9                        RET
```

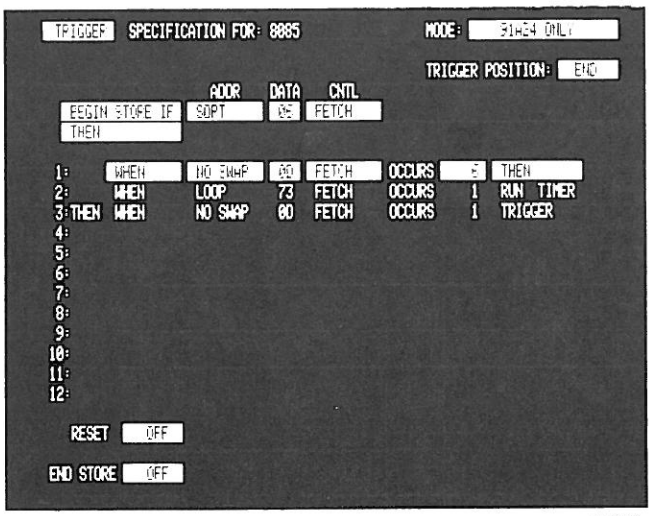
4540 19

Figure 20. A proposed sorting algorithm. This routine sorts a 256-byte array of unsigned 8-bit numbers into an array of non-increasing order. The array length is stored at address BC00; the array's elements are stored starting at address BC01.

Method: Set up the 91A24 Trigger Specification submenu (as shown in Figure 21) to identify and time the compare/swap loop:

- The BEGIN STORE qualifier's data value makes sure that the DAS stores only the sort routine.
- Vary level 1's OCCURS value to specify which pass through the compare/swap loop will be timed. After each acquisition, increment the OCCURS value to time execution of the next pass, then rerun the routine using the original unsorted array.
- Level 2 tells the DAS to begin timing when the compare/swap loop is entered.
- The trigger action on level 3 turns the timer off when the compare/swap loop is completed.

Expect: When acquisition is completed the TIME= value appears appears on the third line of the State Table display.



4540 20

Figure 21. 91A24 Trigger Specification setup for timing worst-case execution.

COUNTING OCCURRENCES OF A REPETITIVE EVENT

Problem: Getting bad output to peripheral devices using RS-232 interface. Suspect that not all of the output buffer is getting sent.

Objective: Observe the RS-232 UART interrupt service routine (listed in Figure 22), and count the number of I/O writes to the output port before line-feed occurs.

```
;RS-232 UART Interrupt Service Routine
;Outputs characters in output buffer until a line-feed is found.

A000   F5              INTRPT:   PUSH   PSW          ;save registers
A001   E5                        PUSH   H
A002   21 00 B6                  LXI    H,BUFPTR    ;get output buffer pointer
A005   7E                        MOV    A,M         ;get next character
A006   D3 F0                     OUT    IOPORT      ;send char to UART
A008   FE 0A                     CPI    LF          ;was it a line-feed?
A00A   CA 10 A0                  JZ     DONE        ;yes, all done
A00D   34                        INR    M           ;point at next character
A00E   C3 14 A0                  JMP    EXIT
A010   3E 01            DONE:    MVI    A,01        ;disable further UART interrupts
A012   D3 F1                     OUT    IO STAT
A014   E1              EXIT:     POP    H           ;restore registers
A015   F1                        POP    PSW
A016   FB                        EI
A017   C9                        RET
```

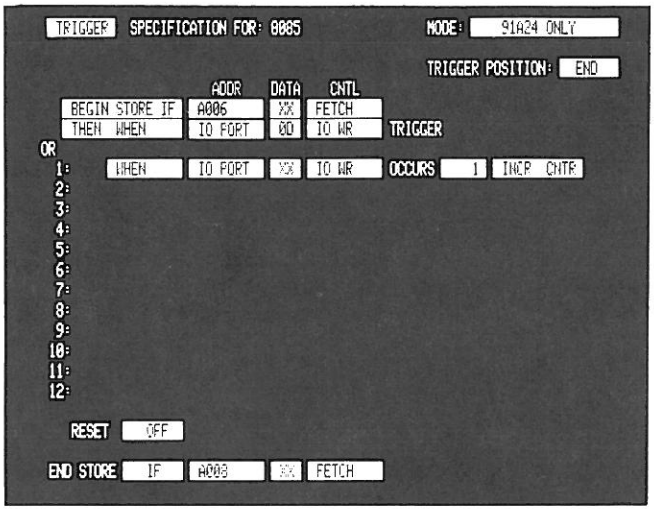
4540 21

Figure 22. An interrupt service routine which outputs characters to an I/O port. The routine continues in a character-output loop until it detects a line-feed.

Method: Set up the 91A24 to identify and store the character-output loop, count I/O writes to the output port, and trigger when the line-feed occurs.

- BEGIN STORE on the instruction fetch which sends the output buffer's contents to the UART.
- INCR CNTR each time an I/O write to IO-PORT occurs.
- END STORE *after* the OUT instruction and its associated I/O write. (END STORE words are not stored.)
- TRIGGER on the line-feed I/O write.

Expect: When acquisition is completed, the State Table displays the CNTR = value (showing total number of characters output), and displays a listing of all OUT instructions and their associated I/O writes.



4540 22

Figure 23. 91A24 Trigger Specification sub-menu set up to count output of characters to an I/O port.

ERROR AND PROMPTER MESSAGES: Additions with Firmware Version 1.11

ACQUISITION STARTED -- CONTINUOUS	If you hold down the START ACQ or START SYSTEM keys for an extended period, the DAS continuously acquires and displays data until you press the STOP key. Holding down START SYSTEM also begins automatic restart of the Pattern Generator.
ALL LEVELS USED	You are attempting to add levels to the stack even though all 16 levels have been allocated.
MUST ASSIGN 1 CLOCK TO POD [X]	You must specify at least one clock term in the POD[X] CLOCK expression, where [X] equals A, B or C.
MUST BE A SUBSET OF STORE ONLY IF	You have specified a word recognizer value that is not a subset of your STORE ONLY IF value. You may not exit the menu while this condition exists. Each incorrect sequence is marked with a highlighted question mark (if it is visible on the screen) or indicated by a highlighted M (if you need to scroll it onto the screen).
NEEDS FIRMWARE VERSION >= 1.11	You must have firmware version 1.11 or higher.
NOT AN ACQ POD	You have attempted to specify a non-acquisition pod ID in a Channel Specification menu POD field. Specify an acquisition pod.
UNDISPLAYABLE GROUP	The data entry field for the channel group requires more than 30 characters for display, and therefore cannot fit on the screen. In the Channel Specification menu, change the group's display radix and/or reduce the number of channels in the group.
WAITING FOR LEVEL: [1-16]	The sequential word recognizer's current level [1-16] is not yet satisfied.
WAITING FOR LEVEL: [1-16] TIME = [value]	If you have specified RUN TIMER in the sequential word recognizer, and the DAS is waiting to trigger, the TIME = message shows you the timer's current total.
WAITING FOR LEVEL: [1-16] CNTR = [value]	If you have specified INCR CNTR in the sequential word recognizer, and the DAS is waiting to trigger, the CNTR = message gives you the counter current total.
WAITING FOR MANUAL STOP	Either the NEVER TRG level or the CNTR level has been satisfied. Press STOP to end acquisition.

INDEX

INDEX (cont.)

INDEX (cont.)