Page 5-24, Figure 5-7. Change part of the timing as shown below:

FROM

TO
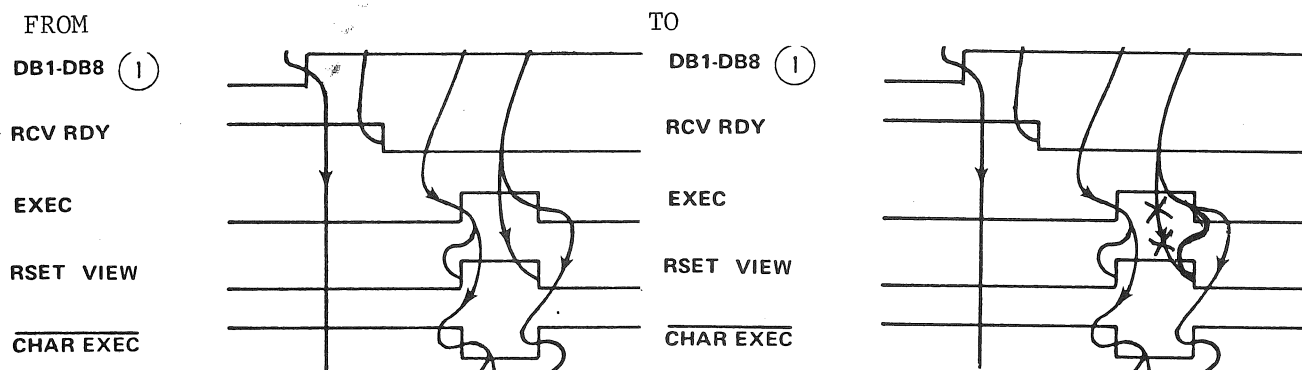
Page 5-25, Figure 5-10.   Near middle of the schematic, reverse the arrow direction on the SCAN CLK line between TC-15 and TC-16.

Page 5-27, Figure 5-12.   At left-middle, in the TC-19 block. Add "19" to the RCV RDY line.

Page 5-31, Figure 5-16.   Near left-middle, in the TC-19 block. Add "L" to the GWA line.

Page 5-44, Figure 5-36.   Near the middle of the schematic. Delete R68 and the associated ground symbol.

Page 5-49, Figure 5-46.   Near bottom-right. Add a circle at pin 6 of U17B.

Page 5-61, Figure 5-65.   At right-top, edge connector pin 23. Change TC10-17 to TC10-N.

Change entered _____.
                       Date

File this change notice in the back of the manual.

Permanent File Copy

This modification modernizes TC-2 circuitry.

SECTION 2:   Replace pages 2-3/2-4 with the enclosed pages

2-3 through 2-4A.

SECTION 4:   Replace pages 4-5/4-6 with the enclosed pages 4-5, 4-5A, 4-5B & 4-6.

SECTION 5:   Page 5-45 - Change Tab label to read   TC-2
670-1436-00

Change Fig. 5-37 title to "Fig. 5-37A. KB STROBE

timing (TC-2 circuit card 670-1436-00)."

Change Fig. 5-38 title to "Fig. 5-38A. Clock timing

(TC-2 circuit card 670-1436-00)."

Change Fig. 5-39 title to "Fig. 5-39A. OUTPUT DATA

SELECTOR. TC-2 CIRCUIT CARD 670-1436-00."

Change page number to 5-45A.

Insert the enclosed page 5-45 between page 5-44 and 5-45A.

Modification entered in manual _____.
                                    Date

Insert this instruction page in the back of the manual.

M18,108/1171

viewing level, thus prolonging tube life. Whenever data is processed by the Terminal or whenever appropriate keys are pressed, the $\overline{\text{HOLD}}$ signal is removed and a $\overline{\text{VIEW}}$ signal is generated to permit another 60 to 120 second viewing period. Just before the $\overline{\text{HOLD}}$ signal is generated, the View Lamp pulsates to warn of the impending Hold Mode. This permits the operator to reset the circuit for another 60 to 120 seconds before it drops into the Hold Mode.

Operation is as follows: Assume that either a $\overline{\text{VIEW KY}}$ or a $\overline{\text{RSET VIEW}}$ signal has just been received. It is applied to U95, where it generates a positive 60 to 120 second output pulse. This pulse is applied to U87 to reset that counter circuit, and is also applied to Q93 to hold it in conduction. With Q93 in conduction, its collector holds the gate of Q91 low to keep that device turned off. When the delay period has elapsed, the output of U95 returns low, releasing U87 and turning Q93 off. With Q93 turned off, C20 charges until it places Q91 in conduction momentarily. C20 then discharges through R24 and the gate junction of Q91. Q91 then again turns off, permitting C20 to go into another charge cycle.

Each time Q91 turns on, it applies a positive pulse to U87. The trailing edge of this pulse advances the U87 count by one. The $\overline{\text{VIEW LMP}}$ signal is caused by the $\div 2$ output of U87, and causes the lamp to blink 7 times until all four outputs from U87 go high. The output of U85B then goes low, and applies a high through R12 to Q93. Q93 conducts and shorts out C20, holding Q91 cut off. The low out of U85B becomes the $\overline{\text{HOLD}}$ signal. It is inverted by Q71 to place a high on the $\overline{\text{VIEW}}$ line. The $\overline{\text{VIEW LMP}}$ output is held low until another viewing cycle is commanded.

The Strobe and Repeat circuit operates to provide an RKB STROB signal each time a keyboard character is actuated. If the Repeat key is held down while a key is held down, the circuit causes repetitive RKB STROB signals to be generated at a 20 Hz rate.

When a RAW STROB is received, it is applied to U85A, whose other outputs are normally held high. The low from U85A passes through U1B and becomes RKB STROB. Under this circumstance, the RKB STROB duplicates the RAW STROB. If a Keyboard key is held down continuously, the RAW STROB remains high and holds the RKB STROB high. However, if the Repeat key is held down, the $\overline{\text{RPT KY}}$ input turns Q1 off, placing a high at the Q3 gate. C33 charges through R33 until Q3 goes into conduction. This permits C33 to discharge through L37 and the Q3 gate junction. When C33 discharges sufficiently, Q3 again turns off and C33 starts another charge cycle. The positive pulse that occurs when Q3 goes into conduction is applied to U23A, where its trailing edge causes U23A to change states.

The U23A configuration is such that its pin 5 output changes state for each input pulse from Q3. This results in the pin 1 input of U85A going alternately low and high at a 10 Hz rate. This causes the RKB STROB output to be interrupted ten times a second, even though the RAW STROB input signal remains high.

KB Click Circuit. The outputs from U85A are also applied to the input of U5. Each negative input into U5 causes it to deliver a 200 μs (approximate) positive pulse through R5 and R42 to the Bell circuit. This causes the output speaker to emit a short pulse, or "click".

Bell Circuit. The Bell circuit can be separated into three sub-circuits . . . . the Multivibrator, the Gating section and the Amplifier. The Multivibrator is a unijunction diode controlling a D latch to generate push-pull output signals. The pulses from Q45 causes the U23B outputs to continuously change state. The push-pull outputs of U23B are applied to opposite sides of output transistors Q47 and Q49. Except when a Bell signal has been commanded, Q47 and Q49 are without current, and the push-pull outputs from U23B can go no further. However, when a $\overline{\text{BEL X}}$ or a $\overline{\text{RING}}$ signal is received, it causes the U83A output to go low, turning Q53 on. This provides drive to Q51, supplying current to Q47 and Q49. Q47 and Q49 alternately turn on and off, supplying the Bell signal to the operational amplifier circuit. The operational amplifier drives the BELL SPKR line, producing an audible output.

When the $\overline{\text{BEL X}}$ or $\overline{\text{RING}}$ signal is made available to U83B, it not only turns Q53 and Q51 on, it also provides drive to Q63. When Q63 turns on, its low output provides a low to U83A. This causes U83A to produce a high output, which turns Q53 off. During the time that Q53 was turned on, C96 accumulated a charge. With Q53 turned off, the long time constant of C96-R96 holds Q51 in conduction for about one-half second. Then Q51 turns off, ending the audible output.

Initial and Home Circuit. The object of this circuit is to provide an $\overline{\text{INITIAL}}$ signal at turn-on, and to generate a $\overline{\text{HOME}}$ signal whenever a $\overline{\text{HOME KY}}$ signal is received. At turn-on, the +5 V supply builds up, applying a positive voltage to the base of Q41. Until C101 charges, it holds Q41 cut off. This holds Q43 cut off, applying a high to U1C and a low to U81A and U81B. While this condition exists, a $\overline{\text{HOME}}$ and an $\overline{\text{INITIAL}}$ signal occur. Approximately 100 ms later, C101 is charged sufficiently to place Q41 in conduction, causing Q43 to conduct. This removes the high from U1C, ending the output pulses.

Output Data Selector TC-2 (Circuit Card 670-1436-01)

The Output Data Selector circuit card performs several functions. It provides clock signals, develops a KB STROB, a FUNC COMP signal, a DATA STRB signal, and makes data bits available to the rest of the Terminal. The circuits that perform these functions are the Clock circuit, the KB Strobe circuit, the Function Complete circuit, Multiplexer Control circuit, Data Multiplexers, the Data Strobe circuit, and the TTY DEL and Closing Bracket Control circuit.

Clock Circuit. The 4 MHz signal developed by the crystal-controlled multivibrator is applied to U13E, which provides a square wave through U13D to clock the U15A and U15B flip-flops. U15A divides the 4 MHz by 2 to provide a symmetrical 2 MHz clock for the rest of the Terminal. The output of U15A is also sent to U15B, where it is again divided by 2 to provide a 1 MHz clock.

Keyboard Strobe Circuit. When a keyboard character is struck, the RKB STROB line goes high. The low from U11C one-sets U37B. The next negative transition of the 1 MHz clock one-sets U39A, generating KB STROBE. The next 1 MHz negative transition one-sets U39B, causing it to zero-set U37B. The next 1 MHz negative transition zero-sets U39A, placing a low on the J input of U39B. U39B then has lows on the J and K inputs and remains in the one-set condition until zero-set (via U7A) by the Function Complete circuit.

Function Complete Circuit. The Function Complete circuit consists of several negative input OR gates which respond to any one of a number of low input signals. Two outputs are derived from this circuit; one is the FUNC COMP signal, and the other is a signal for resetting the KB Strobe circuit. Any one of the six input signals can cause a reset signal to be sent to the KB Strobe circuit. All except the $\overline{\text{XMIT COMP}}$ signal cause a FUNC COMP signal to be generated.

Multiplexers. These devices are provided with A and B control signals to determine which input data (C0, C1, C2) will control the output of its respective section. BA combinations of 00, 01, 10 will engage C0, C1, C2 respectively.

Multiplexer Control Circuit. This circuit provides two signals to each of the multiplexers, determining which input will control the outputs. When a keyboard signal is entered, the KB STROBE causes a low from U35C, which causes a low from U5B. The U5A output remains high. This combination permits keyboard input data (KB1, etc) to appear at the output of the multiplexers.

During Scratch Pad Send operation, SEND goes high and applies lows to the A and B inputs of the multiplexers, causing Scratch Pad data (SP1, etc) to leave the multiplexers.

In auxiliary operation, $\overline{\text{IN AUX}}$ is low. AUX STROB generates a low from U35A, which places a low on the B inputs while the A inputs remains high. Auxiliary data (A1, etc) then passes through the multiplexers.

Data Strobe Circuit. The Data Strobe Circuit provides a DATA STRB whenever Keyboard or Auxiliary data is being passed through the multiplexers. During Scratch Pad transmission, $\overline{\text{SP XMT STR}}$ must go low to cause DATA STRB.

TTY DEL and Closing Bracket Control Circuit. The purpose of this circuit is to limit the output during TTY operation so that output bit B6 remains low at all times except when the character DEL or Closing Bracket is being transmitted. In essence, the circuit has no effect when TTY is low. Notice that TTY is applied to U35B. If it is low, it causes U35B to have a high output, causing the U5C output to follow the KB6 input. Since the U5C output is applied to the 2C2 input of U27, it has the effect of applying KB6 directly to the multiplexer.

When Teletype Mode is selected, TTY is high. Now U35B is controlled either by the KB7 input or by the U31A output. The B6 output follows the KB6 input as long as KB7 is low. When KB7 is high, the U35B output can only go high when the KB1, KB3, KB4, KB5, and KB6 combination indicates that a DEL or Closing Bracket is being generated. During those times, the U31A output goes low, causing U35B to place a high on U5C, permitting KB6 to again control the B6 output via U5C and U27.

Output Data Selector TC-2 (Circuit Card 670-1436-00)

The Output Data Selector circuit card performs several functions. It provides clock signals, develops a KB STROB, a FUNC COMP signal, a DATA STRB signal, and makes data bits available to the rest of the Terminal. The circuits that perform these functions are the Clock circuit, the KB Strobe circuit, the Function Complete circuit, Gate Enabling circuit, Keyboard Input Gates, AUX Input Gates, Scratch Pad Send Gates, the Data Strobe circuit and the TTY DEL and Closing Bracket Control circuit.

Clock Circuit. The 4 MHz signal developed by the crystal-controlled multivibrator is applied to Q7, which provides a square wave through U7A to clock the U35A and U35B flip-flops. U35A divides the 4 MHz by 2 to provide a symmetrical 2 MHz clock for the rest of the Terminal. The output of U35A is also sent to U35B, where it is again divided by 2 to provide a 1 MHz clock.

KB Strobe Circuit. When a keyboard character is struck, the RKB STROB line goes high and combines with the other three highs on U55 to provide a low output. This causes U13A to become one-set. The next negative-going excursion of the 1 MHz clock pulse causes U15 to become one-set, causing the KB STROB line to go high. The next negative transition of the 1 MHz clock pulse zero-sets U15 and one-sets U13B. The zero output from U13B goes to U15, where it disables U15 in the zero-set condition. U13B now has two low inputs and remains in its one-set condition. The next positive excursion of the 1 MHz clock causes U33D to provide a low output, which zero-sets U13A to prepare it for the next input signal. U13B remains in its one-set condition until such time as the Function Complete circuit provides it with a zero-setting signal.

Function Complete Circuit. The Function Complete circuit consists of several negative input OR gates which respond to any one of a number of low input signals. Two outputs are derived from this circuit; one is the FUNC COMP signal, and the other is a signal for resetting the KB Strobe circuit. Any one of the six input signals can cause a reset signal to be sent to the KB Strobe circuit. All except the $\overline{\text{XMIT COMP}}$ signal cause a FUNC COMP signal to be generated.

Gate Enabling Circuit. The Gate Enabling circuit permits one of the three sets of gates to be enabled at a given time. The SEND input signal takes precedence. Whenever it exists, it enables the Scratch Pad Send Gates and disables the KB Input Gates and the Aux Input Gates.

When the SEND signal is low and IN KB AUX signal exists, U9A has two high inputs. Just before a KB STROB is developed in response to an RKB STROB, U13A applies another high signal to U9A. This sends a high to the KB Input Gates, permitting KB Data bits to pass through the input gates.

Two highs exist on U9C if SEND and $\overline{\text{IN AUX}}$ are low. When an AUX STROB arrives at the circuit, U9C provides a low output, causing U11C to place a high on the Aux Input Gates. The auxiliary data bits are then permitted to pass through.

Data Strobe Circuit. The Data Strobe Circuit provides a DATA STRB whenever data is being passed through any one of the three input gate circuits. When keyboard data is being input, highs are applied to U33A during KB STROB time, sending a low to U51A to generate the DATA STRB signal. When auxiliary inputs are being provided, the AUX STROB causes U33B to generate the DATA STRB. During Scratch Pad transmission, the low SP XMT STR signal causes the DATA STRB.

TTY DEL and Closing Bracket Control Circuit. The purpose of this circuit is to limit the output during TTY operation so that output bit B6 remains low at all times except when the character DEL or Closing Bracket is being transmitted. In essence, the circuit has no effect when TTY is low. Notice that TTY is applied to U9B. If it is low, it causes U9B to have a high output, causing the U7C output to follow the KB6 input. Since the U7C output is applied to U27D, it has the effect of applying KB6 directly to U27D.

When Teletype Mode is selected, TTY is high. Now U9B is controlled either by the KB7 input or by the U1 output. The B6 output follows the KB6 input as long as KB7 is low. When KB7 is high, the U9B output can only go high when the KB1, KB3, KB4, KB5, and KB6 combination indicates that a DEL or Closing Bracket is being generated. During those times, the U1 output goes low, causing U9B to place a high on U7D, permitting KB6 to again control the B6 output via U7D, U7C, and U27D.

Scratch Pad Control TC-4

This circuit card contains most of the circuitry for controlling the Scratch Pad features of the Terminal. When the Scratch Pad has not been selected at the keyboard or by program control, it is essentially a bypass card, and can be represented by the Scratch Pad Bypass drawing which appears on the schematic.

When in Compose Mode, most of the circuitry on the card is interactive, and therefore will be explained as part of an operating sequence rather than an individual circuits.

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
RESISTORS (cont)				
R154	317-0272-00			2.7 kΩ, 1/8 W, 5%
R156	317-0272-00			2.7 kΩ, 1/8 W, 5%
R158	317-0473-00			47 kΩ, 1/8 W, 5%
R159	317-0473-00			47 kΩ, 1/8 W, 5%
R161	317-0123-00			12 kΩ, 1/8 W, 5%
R163	317-0473-00			47 kΩ, 1/8 W, 5%
R165	317-0102-00			1 kΩ, 1/8 W, 5%
R166	317-0123-00			12 kΩ, 1/8 W, 5%
R168	317-0223-00			22 kΩ, 1/8 W, 5%
R171	317-0123-00			12 kΩ, 1/8 W, 5%
R173	317-0104-00			100 kΩ, 1/8 W, 5%
R175	317-0474-00			470 kΩ, 1/8 W, 5%
R177	317-0471-00			470 Ω, 1/8 W, 5%
R178	317-0101-00			100 Ω, 1/8 W, 5%
R179	317-0123-00			12 kΩ, 1/8 W, 5%
INTEGRATED CIRCUITS				
U1	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U5	156-0072-00			Monostable multi, replaceable by T.I. SN74121N
U7	156-0049-00			Op ampl, replaceable by Fairchild µA741C
U9	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U19	155-0031-00			Quad timing logic
U23	156-0041-00			Dual D flip-flop, replaceable by T.I. SN7474N,
U29	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U39	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U51	156-0043-00			Quad 2-input NOR gate, replaceable by T.I. SN7402N
U57	155-0031-00			Quad timing logic
U59	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U81	156-0094-00			Dual peripheral driver, replaceable by T.I. SN75451P
U83	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U85	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U87	156-0032-00			4-bit binary counter, replaceable by T.I. SN7493N
U95	156-0081-00			Retriggerable monostable multivibrator, replaceable by Fairchild 9601

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Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
ASSEMBLY,	670-1436-01			**OUTPUT DATA SELECTOR TC#2 Circuit Card**
A2				
CAPACITORS				
C1	281-0546-00			330 pF, 500 V, ±10%
C3	283-0602-00			53 pF, 300 V, ±3%
C5	283-0602-00			53 pF, 300 V, ±3%
C30	290-0530-00			68 μF, 6 V, ±20%
C31	283-0177-00			1 μF, 25 V, +80%-20%
C32	283-0177-00			1 μF, 25 V, +80%-20%
C33	283-0177-00			1 μF, 25 V, +80%-20%
C34	283-0177-00			1 μF, 25 V, +80%-20%
C37	290-0530-00			68 μF, 6 V, ±20%
C38	283-0177-00			1 μF, 25 V, +80%-20%
INDUCTORS				
L30	108-0395-00			64 μH
L34	108-0395-00			64 μH
L37	108-0395-00			64 μH
L50	108-0551-00			14 μH
L51	108-0551-00			14 μH
L54	108-0551-00			14 μH
L56	108-0551-00			14 μH
L58	108-0551-00			14 μH
L60	108-0551-00			14 μH
L62	108-0551-00			14 μH
L64	108-0551-00			14 μH
L66	108-0551-00			14 μH
L68	108-0551-00			14 μH
L70	108-0551-00			14 μH
RESISTORS				
R1	315-0681-00			680 Ω, 1/4 W, 5%
R3	321-0147-00			332 Ω, 1/8 W, 1%
R5	321-0147-00			332 Ω, 1/8 W, 1%
R7	315-0681-00			680 Ω, 1/4 W, 5%
R10	321-0097-00			100 Ω, 1/8 W, 1%
R20	315-0472-00			4.7 kΩ, 1/4 W, 5%
R25	315-0472-00			4.7 kΩ, 1/4 W, 5%
INTEGRATED CIRCUITS				
U5	156-0129-00			Quad 2-input positive & gate, replaceable by T.I. SN7408N
U7	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U11	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U13	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U15	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U19	156-0156-00			Dual 4-input positive or/nor clock driver, replaceable by MC1023L
U21	156-0098-00			Dual 4-line to 1-line, data select multiplex, replaceable by T.I. SN74153N
U23	156-0098-00			Dual 4-line to 1-line, data select multiplex, replaceable by T.I. SN74153N
U27	156-0098-00			Dual 4-line to 1-line, data select multiplex, replaceable by T.I. SN74153N
U29	156-0098-00			Dual 4-line to 1-line, data select multiplex, replaceable by T.I. SN74153N
U31	156-0034-00			Dual 4-input gate, replaceable by T.I. SN7420N
U35	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
INTEGRATED CIRCUITS (cont)				
U37	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U39	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
CRYSTAL				
Y10	158-0056-00			4 MHz

ASSEMBLY A2

	670-1436-00			**OUTPUT DATA SELECTOR TC#2 Circuit Card**
CAPACITORS				
C12	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C13	281-0510-00			22 pF, Cer, 500 V, 20%
C18	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C20	283-0187-00			0.047 µF, Cer, 400 V, 10%
C36	281-0510-00			22 pF, Cer, 500 V, 20%
C52	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C53	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C54	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C55	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C56	283-0177-00			1 µF, Cer, 25 V, +80%-20%
C57	283-0177-00			1 µF, Cer, 25 V, +80%-20%

| Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
SCD, DIODE				
CR20	152-0185-00			Silicon, replaceable by 1N4152
INDUCTORS				
L13	108-0395-00			64 μH
L50	108-0551-00			14 μH
L52	108-0551-00			14 μH
L54	108-0551-00			14 μH
L56	108-0551-00			14 μH
L58	108-0551-00			14 μH
L60	108-0551-00			14 μH
L62	108-0551-00			14 μH
L64	108-0551-00			14 μH
L66	108-0551-00			14 μH
L68	108-0551-00			14 μH
L70	108-0551-00			14 μH
TRANSISTOR				
Q7	151-0223-00			Silicon, NPN, 2N4275
RESISTORS				
R10	317-0102-00			1 kΩ, 1/8 W, 5%
R11	317-0202-00			2 kΩ, 1/8 W, 5%
R13	317-0431-00			430 Ω, 1/8 W, 5%
R15	317-0621-00			620 Ω, 1/8 W, 5%
R16	317-0182-00			1.8 kΩ, 1/8 W, 5%
R17	317-0102-00			1 kΩ, 1/8 W, 5%
R18	317-0682-00			6.8 kΩ, 1/8 W, 5%
R20	317-0222-00			2.2 kΩ, 1/8 W, 5%
R22	317-0222-00			2.2 kΩ, 1/8 W, 5%
R30	317-0472-00			4.7 kΩ, 1/8 W, 5%
R34	317-0472-00			4.7 kΩ, 1/8 W, 5%
R40	317-0472-00			4.7 kΩ, 1/8 W, 5%
R52	317-0102-00			1 kΩ, 1/8 W, 5%
R53	317-0102-00			1 kΩ, 1/8 W, 5%
R54	317-0102-00			1 kΩ, 1/8 W, 5%
INTEGRATED CIRCUITS				
U1	156-0035-00			8-input gate, replaceable by T.I. SN7430N
U5	156-0033-00			Linear, RF/IF ampl, replaceable by RCA CA3028A
U7	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U9	156-0047-00			Triple 3-input gate, replaceable by T.I. SN7410N
U11	156-0058-00			Hex. invert, replaceable by T.I. SN7404N
U13	156-0039-00			Dual J-K flip-flop, replaceable by T.I. SN7473N
U15	156-0038-00			J-K flip-flop, replaceable by T.I. SN7472N
U23	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U25	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U27	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
U29	156-0030-00			Quad 2-input gate, replaceable by T.I. SN7400N
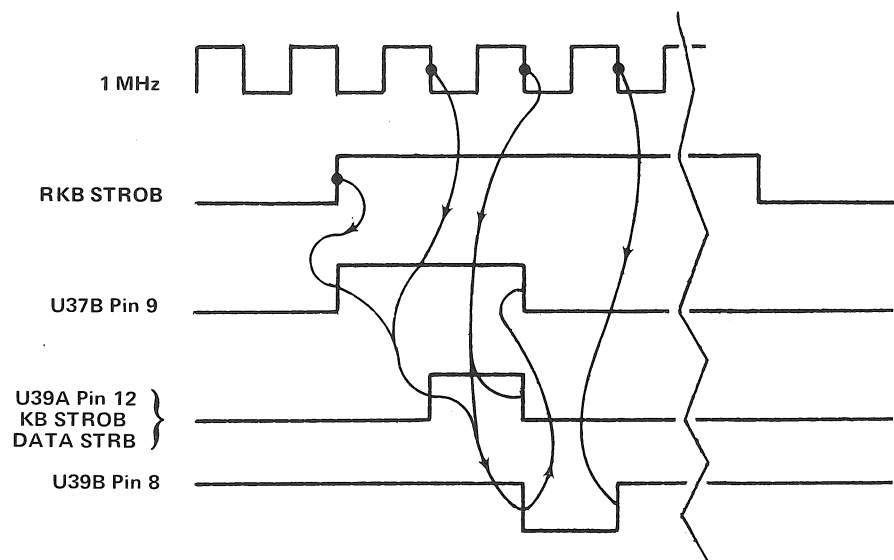
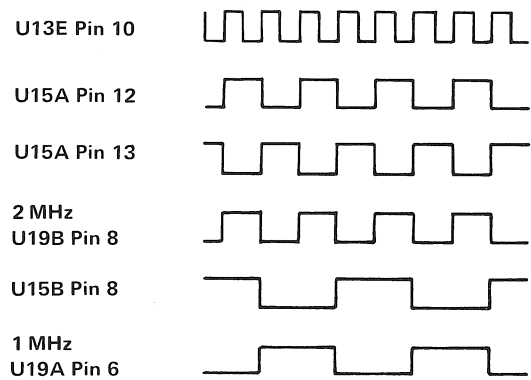Fig. 5-37. KB STROBE timing. (TC-2 Circuit card 670-1436-01).

Fig. 5-38. Clock timing (TC-2). Circuit card (670-1436-01).

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OUTPUT DATA SELECTOR TC-2
FIG. 5-39 CKT CARD NO. 670-1436-01 AND ABOVE

4002A

Page 5-45

TC-2
670-1436-01

4002A DRAWER UNIT AND KEYBOARD MAINTENANCE MANUAL

MOD INSERT FOR M18,158 EFFECTIVE AT SN B070630

This modification provides initialization for the Edit circuit.

Page 5-46, Fig. 5-41   Near the center of the schematic, remove

+5 V from pin 1 of U43A and add a line from

pin 1 of U43A to pin 6 of U7B (bottom, near center).

Place an X near each extreme of this line and

put a ① adjacent to the line, as shown below.
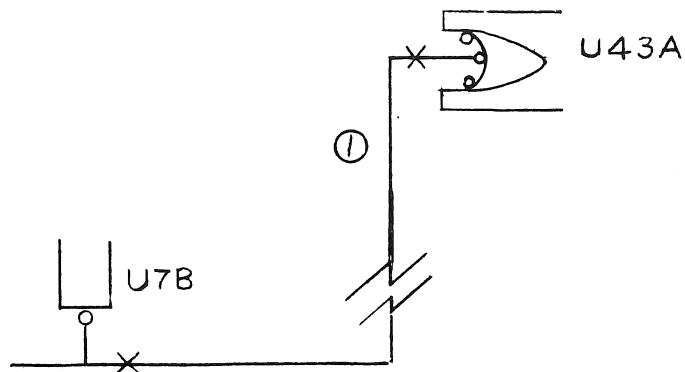
Add a note to the schematic as follows:

① This wire added in later board versions. Pin

1 of U43A was previously connected to +5 V.

MOD INSERT FOR M18,161   Effective at SN B080000-up

INCORPORATES NEW CIRCUIT BOARD AND CARDS AS FOLLOWS:

     TC-0   670-1522-01

     TC-5   670-1438-02

     TC-10 670-1443-02

     TC-12 670-1445-01

This modification improves Local Edit Send, Page Full operation, and

bell operation. It also permits use with scan converters and enables

refreshed Scratch Pad operation with synchronous interface units.

MAKE THE FOLLOWING CHANGES:

SECTION 2:   Replace pages 2-7 through 2-14 with the enclosed pages
               2-7 through 2-14A.

SECTION 4:   Change Electrical Parts List as follows:
Page 4-9
ASSEMBLY
  A4   670-1438-00   B010100 - B079999   SCRATCH PAD COUNTER TC#5 Circuit Card
        670-1438-01   B080000

ADD:

  R12   315-0472-00   XB080000   4.7 kΩ, 1/4 W, 5%

  U19   156-0131-00   XB080000   Single 25 MHz, 8-bit, replaceable by
                                           SN74164N

Page 4-16

ASSEMBLY
  A9   670-1443-00   B010100 - B079999   Y DATA REGISTER TC#10 Circuit Card
        670-1443-01   B080000 - B089999
        670-1443-02   B090000
Page 4-18

ASSEMBLY
  A11   670-1445-00   B010100 - B079999   X DATA REGISTER TC#12 Circuit Card
        670-1445-01   XB080000

REMOVE:

  C36   283-0220-00   B010100 - B079999X 0.01 µF, Cer, 50 V, 20%

  R36   315-0201-00   B010100 - B079999X 200 Ω, 1/4 W, 5%

MOD INSERT FOR M18,161 Effective at SN B080000-up

SECTION 5:   Page 5-5 - Add DO PAUSE *P   TC5-28 Initiating command for $\overline{\text{PAUSE}}$

Page 5-8 - Add SP STRIP *L   TC5-2 Sets Y register to Scratch Pad position

Page 5-14 Change J121 pin 19 as follows:

19   REFRSH   L   TC04   27 ①

Add the following note below the J121 listing:

"①Not connected on TC-0 number 670-1522-00."

Page 5-21/5-22 Remove and replace with the enclosed page 5-21/5-22

Pages 5-33 through 5-39. Remove and replace with the enclosed pages 5-33 through 5-39.

Page 5-44, Fig. 5-36 Add ①TC17-1 to list of destinations for the HOME signal on pin 5

Add note to the schematic:

①Not applicable if the Terminal contains TC-0 number 670-1522-00

Page 5-46, Fig. 5-41 Add ①TC17-8, ①J121-19 to list of destinations for the REFRSH signal on pin 27

Add note to the schematic:

①Not applicable if the Terminal contains TC-0 number 670-1522-00

Page 5-47, Fig. 5-42 Change figure number to 5-42A.
         Fig. 5-43 Near right middle of schematic, change U51A name from SEND INITIATE FF to SEND ENABLE FF. Change figure number and title of schematic to "Fig. 5-43A. SCRATCH PAD COUNTER. TC-5 CIRCUIT CARD #670-1438-00". Change the page number to 5-47

Insert the enclosed page 5-47 between 5-46 and 5-47A.

Page 5-49. Fig. 5-46. Add ①TC17-3 to list of destinations for the DC4 signal on pin U.
Add note to the schematic:
①Not applicable if the Terminal contains TC-0 number 670-1522-00.

Page 5-52, Fig. 5-50. Change figure number to 5-50A.

MOD INSERT FOR M18,161 Effective at SN B080000-up

Page 5-52, Fig. 5-51 At the top-left of the schematic, change the circuit as follows:

$\overline{\text{SP STRIP}}$
From TC5-2

Compose
From TC4-20

U29D
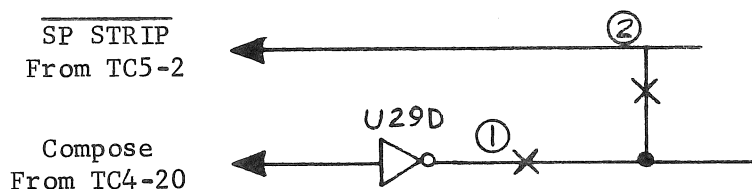
Near top left, add signal destinations as follows:

③ TC17-2 to $\overline{1Y}$ on pin B

③ TC17-4 to $\overline{2Y}$ on pin 2

③ TC17-5 to $\overline{4Y}$ on pin 5

Add the following notes near the changes:

① ② Circuit ① exists on circuit card 670-1443-00 only;
      circuit ② exists on circuit card 670-1443-01 only.

③ Not applicable if the Terminal contains TC-0 number 670-1522-00.

Change the figure number and title to "Fig. 5-51A. Y DATA REGISTER. TC-10 CIRCUIT CARD #670-1443-00 and 670-1443-01."
Change page number to 5-52A.
Insert the enclosed page 5-52 between pages 5-51 and 5-52A.

Page 5-54. Replace with the enclosed page 5-54.

Page 5-59, Fig. 5-61. Add ① TC17-28 to list of destinations for the CHAR PROC signal on pin 28.
Add the following note to the schematic:
① Not applicable if the Terminal contains TC-0 number 670-1522-00.

Page 5-61, Fig. 5-65. Add ① TC17-6 to list of destinations for the GRAF Z signal on pin 8.
Add ① TC17-7 to list of destinations for the LI BUSY signal on pin 19.
Add the following note to the schematic:
① Not applicable if the Terminal contains TC-0 number 670-1522-00.

SECTION 6: Change the Mechanical Parts List as follows:
Page 6-9
Fig. 3-24

670-1438-00	B010100 - B079999	1	CIRCUIT CARD ASSEMBLY-SCRATCH PAD
670-1438-01	B080000		LOGIC-A4
- - - - - -		-	circuit card assembly includes:
388-1987-00	B010100 - B079999	1	CIRCUIT CARD
388-1987-01	B080000	1	CIRCUIT CARD

SECTION 6:

Fig. -32   670-1443-00   B010100 - B079999   1   CIRCUIT CARD ASSEMBLY-Y DATA
              670-1443-01   B080000 - B089999   REGISTER A9
              670-1443-02   B090000
              - - - - - -   -   circuit card assembly includes:
              388-1992-00   B010100 - B089999   1   CIRCUIT CARD
              388-1992-01   B090000   1   CIRCUIT CARD

Fig. -34   670-1445-00   B010100 - B079999   1   CIRCUIT CARD ASSEMBLY-X DATA
              670-1445-01   B080000   REGISTER A11
              - - - - - -   -   circuit card assembly includes:
              388-1994-00   B010100 - B079999   1   CIRCUIT CARD
              388-1994-01   B080000   1   CIRCUIT CARD

Modification entered in manual_____.
                                  Date

Insert these instructions pages in the back of the manual.

If it is desired to shift from Unrefreshed Scratch Pad operation to Edit Mode under program control, the characters ESC ? must be sent to Terminal. The ESC character arms the U47B FF as previously explained and the ? character causes a signal to be routed through U2, U53D, and U51F to set the U33A output high. The high is blocked from U29A by CR22. After the ? is loaded into the memory, eight MOS CLK pulses occur and U7A develops a low output which goes to U43A to set the U33A output low. This low is felt at U29A, sending a signal through U45C, U51E and U53A to one-set Refresh FF U27A. The U33A output is also routed through U53D and U51F to the Edit Control circuit to one-set EDIT FF U7B. Edit operation is then as previously explained.

Program command sequence ESC C clears the Scratch Pad memory if in Unrefreshed Mode. ESC arms the U47B FF and the C causes a signal to pass through U23, Clear Select gate U53C, U14A and into U31 where it generates a 1 ms pulse. This 1 ms pulse affects the circuit in the same manner as previously explained.

Certain Interface Units are capable of causing the Unrefreshed Scratch Pad contents to be sent directly to the Terminal screen. This is accomplished by sending a $\overline{\text{SEND}}$ $\overline{\text{SCRN}}$ signal to TC-4 and TC-5. The $\overline{\text{SEND SCRN}}$ signal into TC-4 causes Send Screen FF U27B to one-set, enabling U15B and turning Q5 on. U15B sends out an $\overline{\text{INHIBIT X}}$ signal. Q5 disables U5A and enables U5C. $\overline{\text{SEND SCRN}}$ is also routed through U29A, U45C, U51E, and U53A to one-set Refresh FF U27A. As soon as the first character in memory is contained in the Shift Register, an $\overline{\text{SP SEND}}$ signal is received from TC-5. The $\overline{\text{SP SEND}}$ signal goes through U45A and U25F to zero-set U27A. $\overline{\text{SP SEND}}$ also goes through U59F to place an enabling voltage on U9D.

TC-2 sends a FUNC COMP signal to TC-4 to acknowledge receipt of the data transmitted by the Scratch Pad. This is applied to U5C. The output from U5C is routed through U9A and U9D to place a low pulse on MOS CLK Enable gate U11A. This results in eight MOS CLK pulses, which advance the next character into the Shift Register. An SP STROB and an SP EXEC signal follow the MOS CLK pulses. Another character is transmitted to the SCREEN and the operation is repeated until all characters are transmitted. The $\overline{\text{SP SEND}}$ signal then goes high, causing SEND SCREEN FF U27B to return to its zero-set condition. Q5 cuts off and U5C becomes disabled.

The Terminal can also be switched from the Unrefreshed Scratch Pad Mode to the Direct Mode by pressing the Home button. The $\overline{\text{HOME}}$ signal is applied to U14C. As soon as the Position Counter agrees with the Cursor Counter (on TC-5), $\overline{\text{AGREE}}$ is received by TC-4, causing a signal from U14C and U59E. This is routed to both the Refresh SP FF and the Unrefreshed SP FF, resetting them for Direct Mode operation.

Scratch Pad Counter TC-5

The Scratch Pad Counter circuit contains the Position Counter Registers, the Cursor Counter Registers, and the Cursor Storage Registers which are used in conjunction with the Scratch Pad Memory circuit. Other circuitry dependent upon these counters is also included on this diagram. When the Scratch Pad circuit is not in use, the card can be represented as the Scratch Pad Counter Bypass card, which is also shown on the schematic diagram.

As soon as the Terminal has been initialized, the $\overline{\text{INITIAL}}$ signal received on TC-5 resets the circuitry. When the Terminal is placed in Refreshed Compose Mode, $\overline{\text{SP}}$ $\overline{\text{EXEC}}$ signals are received continuously every 256 microseconds. Each one of these is routed through U43E and U45A to the Position Counter circuit.

The purpose of the Position Counters is to count the Scratch Pad Memory character position which is contained in the Shift Register on TC-14, and it is incremented every time that an $\overline{\text{SP EXEC}}$ signal is received. The Cursor Counter is incremented each time a character is inserted into the Scratch Pad Memory circuit. The $\overline{\text{CC CNT UP}}$ signal is passed through Cursor Count Up Disable gate U47B and through U29C to increment the counter. Assume that thirty characters have been stored in the Scratch Pad Memory. The Cursor Counter would contain the digital equivalent of thirty. Each time the Position Counter reaches that value, the A=B output of comparator U5 would cause U49D to generate the $\overline{\text{AGREE}}$ signal.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-01 and above. If an insert condition does not exist, low pulses are generated by U55B and U13B each time the Position Counters reach one hundred. (If insert conditions exists, U13B generates a low output when the Position Counter reaches 101. This accounts for the added Insert shift register on TC-14.) The U53B output forms the $\overline{\text{RSET INS}}$ signal, while the U13B output is processed through the TC-5 circuit as an "end of memory" signal. This signal causes a high to be applied to the J input of U35A. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal causes U35A to one-set. This causes several things to happen. The one output provides enabling voltage to U55A and U59D. The low from the zero output goes to U55B to disable it, and goes to U13A to reset the position counters to zero. The low from U35A also goes to U5 during this time to inhibit $\overline{\text{AGREE}}$ signals. (With pin 1 high and pin 15 low, the comparator cannot generate an $\overline{\text{AGREE}}$ output.) When $\overline{\text{SP EXEC}}$ returns high, it generates an $\overline{\text{SP RSET X}}$ from U55A and a $\overline{\text{DC PAUSE}}$ from U59D. $\overline{\text{SP RSET X}}$ goes to TC-12 to reset the X registers. $\overline{\text{DO PAUSE}}$ goes to TC-4 to inhibit MOS CLK pulses. It is also used in TC-5 circuitry

to zero-set U35B (to inhibit SP EXEC X pulses) and to one-set U17A if the $\overline{\text{SEND}}$ signal is low. (Send operation is discussed later.) U17A is normally zero-set, supplying enabling voltages to U37D and U55B. The U37D output is thus held low, supplying an $\overline{\text{SP STRIP}}$ signal to hold the display in the scratch pad area of the display. The next $\overline{\text{SP}}$ $\overline{\text{EXEC}}$ pulse ends the $\overline{\text{DO PAUSE}}$ signal from U59D, ends the $\overline{\text{SP RSET X}}$ pulse from U55A, and zero-sets U35A. When $\overline{\text{DO PAUSE}}$ ends, it releases U35B. When U35A zero-sets, its zero output puts a high on U55B. The one output from U35A one sets U51A to permit Send operation, if it had been ordered by a $\overline{\text{SEND}}$ signal. Each subsequent SP EXEC pulse causes a low out of U55B. This low appears at the output of U19 eight 1 MHZ pulses later, generating an EXEC signal to permit writing the character in the Scratch Pad strip.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-00. If an insert condition does not exist, low pulses are generated by U55B and U13B each time the Position Counters reach one hundred. (If insert conditions exists, U13B generates a low output when the Position Counter reaches 101. This accounts for the added Insert shift register on TC-14.) The U55B output forms the $\overline{\text{RSET INS}}$ signal, while the U13B output is processed through the TC-5 circuit as an "end of memory" signal. This signal causes a high to be applied to the J input of U35A. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal causes U35A to one-set. This causes several things to happen. The first of these is that the zero output is applied to U13A to zero-set the Position Counters. This removes the highs from the output gates of the counters and removes the enabling high from pin J or U35A. With U35A one-set, U55A receives enabling voltage and generates an $\overline{\text{SP RSET X}}$ signal which goes to the X-Register to return it to zero position. The trailing edge of the next $\overline{\text{SP EXEC}}$ signal returns U35A to its zero-set condition. This places an enabling voltage on U53B, permitting SP EXEC signals to control the output of that device. It also causes the Send Enable FF U51A to become one-set, thus initiating Send operation with the first character in Scratch Pad memory.

When Edit Mode is selected, a $\overline{\text{CS LOAD}}$ signal causes the Cursor Counter output to be loaded into the Cursor Storage circuit. This records the cursor count at the point where Edit Mode was selected, so that if Edit Send is to be accomplished, it can start from that position. It also occurs when the Terminal is shifted out of Scratch Pad Mode, so that the Cursor Counter can return to this value when the Terminal is switched back to Scratch Pad Mode.

If a character is inserted while the Terminal is in Edit Mode, a COUNT UP signal is applied to the Cursor Storage Register and $\overline{\text{CC CNT UP}}$ is applied to the Cursor Counter,

permitting both counters to increment by one. If a character is deleted from memory while in Edit Mode, a COUNT DWN signal is received to decrement the Cursor Storage Register at the same time a $\overline{\text{CC CNT DWN}}$ signal is decrementing the Cursor Counter. Thus the Cursor Storage Registers are compensated for additions or deletions of characters. When the Terminal is switched from Edit to Compose Mode, a $\overline{\text{CC LOAD}}$ signal is applied to the Cursor Counters, causing them to change their values to that contained in the Cursor Storage circuit.

Notice that the Cursor Counter is provided with a Cursor Count Up Disable gate and a Cursor Count Dwn Disable gate. Count up is disabled when the registers contain a digital equivalent of 98, causing a FULL LITE signal to exist as well as the disabling feedback signal. Count down disabling occurs when the Cursor Zero-Position Detect Diodes all have low inputs, indicating that the Cursor Counter has reached a value of zero.

One other circuit associated with insertion of characters into memory is the Clear Set circuit. When a character is to be inserted, the CL SET ARM line goes high, enabling U51B. The next negative transition of the 1 MHz line causes U51B to become one-set, placing enabling voltages on Set and Clear gates U45C and U45D. With the 1 MHz line low, U45D generates a low output, causing the CLEAR signal to be sent to the Shift Registers. (The CLEAR signal insures that the Shift Register contains all zeros before the SET signal loads the new character data.) The next half microsecond finds the 1 MHz line high; U45C generates a low output, causing the SET line to go high.

This paragraph pertains only to TC-5 circuit cards 670-1438-01 and above. When the Position Counter passes through one hundred and reaches the first character position, Send Enable FF U51A becomes one-set. The next low input on the 1 MHz line causes a low pulse out of U53C. This is applied through U49B and U37B to Send FF U17B. If a $\overline{\text{SEND}}$ had previously caused U17A to one-set, U17B would become one-set, causing $\overline{\text{SP SEND}}$ and SEND signals to be sent out. In addition, the pin 9 output of U17B puts an enabling voltage on U33C and U59C. U59C permits SP XMT STR signals to be generated. When an $\overline{\text{AGREE}}$ signal occurs (indicating that the last character has been transmitted), U33C generates a low output and causes U15B to send a reset signal through U57F to the Send Initiate and the Send flip-flops, restoring them to their zero-set condition.

This paragraph pertains only to TC-5 circuit cards numbered 670-1438-00. When the Position Counter passes through one hundred and reaches the first character

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position, Send Enable FF U51A becomes one-set. The next low input on the 1 MHz line causes a low pulse out of U53C. This is applied to Send Initiate gate U47D. If a SEND signal is present, U47D generates a high output pulse, the leading edge of which one-sets Send Initiate FF U17A, applying a high to the D input of U17B. The low pulse from U53C is also applied to U49B. When it ends, the U49B output goes low, causing a high to appear at the U37B output. This one-sets SEND FF U17B, causing SP SEND and SEND signals to be sent out. In addition, the pin 9 output of U17B puts an enabling voltage on U33C and U59C. U59C permits SP XMT STR signals to be generated. When an AGREE signal occurs (indicating that the last character has been transmitted), U33C generates a low output and causes U15B to send a reset signal through U57F to the Send Initiate and the Send flip-flops, restoring them to their zero-set condition.

If the Terminal is in the Edit Mode when the SEND command is executed, the EDIT FF signal disables U49B and enables Edit Send Execute device U37A. At the time that Edit was selected, the Cursor Counter loaded its contents into the Cursor Storage Register. When the Position Counter reached the first character position, it indirectly caused Send Initiate FF U17A to become one-set. This removed the low from the U37C pin 10 input, permitting that device to come under control of the SP STROB signal. Now each time the Position Counter increments one count, an SP STROB signal and a COUNT DWN signal are received by TC-5, causing the output of U45B to go low. This sends a high COUNT DWN signal into U21. When the Position Counter reaches the value that had been in Cursor Storage, the Cursor Storage contains the complement of 1. (Complement of 0 for TC-5 circuit cards numbered 670-1438-00.) All inputs to U9 are high. This causes the Edit Send Execute gate U9 to send a low to U41A, causing U37A and U37B to deliver a high pulse to U17B, one-setting that device and initiating transmission. Transmission continues until the Cursor Counter and the Position Counter values agree, at which time transmission is terminated and the Scratch Pad Send circuits become reset.

Horizontal Tab TC-6

The purpose of this circuit card is to permit insertion of tab positions, removal of tab positions, and the shifting of beam writing position to pre-determined tab positions. Circuitry consists of the following sections: Control Signal Decoder, Disarming Circuit, Tab Arm flip-flop, Set flip-flop, Clear flip-flop, Master Clear Control Circuit, Read/Write flip-flop, Reset flip-flop, Tab Pulse Control, Random Access Memory, and Master Clear Counters.

Assume that no tab positions have been established, and that it is desired to insert a tab at the position occupied by

the beam. The eight most significant bits are routed through Master Clear Counters U55 and U57 and applied to the Random Access Memory U35. There they call up a specific memory location which is coincident with the content of these lines. Upon receipt of a coded character (normally ESC), the Terminal provides an SP ARM signal into the circuit. The trailing edge of this pulse one-sets flip-flop U9B, applying enabling voltages to Set flip-flop U9A, Clear flip-flop U29A and Master Clear Control flip-flop U29B. In order to set a tab, the next input data must provide a low output from U1 in the Control Signal Decoder. As configured on the schematic, the number 1 provides all highs into U1. When the TC IN STRB pulse arrives, it causes a low pulse out of U1 which passes through U27A, is inverted and causes Set flip-flop U9A to become one-set. This applies a low to U31A, causing that device to remove the clear signal from Read/Write flip-flop U11A, at the same time sending a TAB BSY signal out through U53B. The TAB BSY signal is routed back to U51D to reset U9B to its zero-set condition. With the clear voltage removed from Read/Write flip-flop U11A, the next 1 MHz clock pulse one-sets U11A; U11A then applies a high to U51C and a low to U53A. The high at pin 9 of U51C has no effect, since the second input to U51C remains low. U51C therefore maintains a high into pin 12 of U35, holding that input in its tab setting condition. Read/Write gate U53A has coincidence between the low signal from the 1 MHz line and the low from the 0 output of U11A, and therefore provides a high into the R/W input of U35. This high at the R/W input of U35 causes the high at pin 12 to set a tab. Simultaneously, the U35 Data Out signal goes low, indicating that a tab position is contained at the existing address. A tab position has been written and the Tab Arm flip-flop has been reset. The next 1 MHz clock pulse one-sets U11B, resetting Set and Clear flip-flops U9A and U29A.

Let's now consider how the beam can be ordered to the tab position which was just inserted. This is accomplished by receiving an HT signal, which comes in and is applied to U51B to generate a TAB signal which goes to TC-12, the X Data Register. In TC-12, this tab signal causes the register to increment by 12 points, which is the spacing between character positions. As the X Register increments, the bit information coming into U55 and U57 changes, continuously calling up new addresses in the U35 Random Access Memory. The HT signal is also applied through U49B, where its trailing edge causes flip-flop U13A to become one-set. When this one-sets, it provides a TAB BSY signal to inform the Terminal that the circuitry is busy providing tab functions. At the same time, U13A releases the clear signal from U33B, U33A, and U13B. This permits that circuit to start counting from 0 to 8 in response to the 1 MHz input signals.

The X Register is incremented through its 12 points at a 2 MHz rate. Therefore, after 6 microseconds, the X Register completes incrementing to its new position. By this time,

the divide by 8 counter is providing a low to U53C. If the Random Access Memory has not arrived at a tab position, the Data Out connection remains high and U53C continues to provide a low output to U53D. This permits U53D to continue applying a high to the Clear input of U13A. U13A remains one-set and permits the divide by 8 counter to continue counting.

When the divide by 8 counter reaches 8, it applies three highs to U31B. The next time the 1 MHz clock goes high, U31B applies a low to U51B which causes another $\overline{TAB}$ signal to be sent to the X Register. The X Register increments through another 12 points and again the Random Access Memory indicates whether or not a tab position exists. If none exists, the divide by 8 counter causes another $\overline{TAB}$ signal to be sent out. This continues until either a tab position is arrived at, or the end of the line is reached and an $\overline{EOL}$ signal arrives. $\overline{EOL}$ is processed through U7A and U53D to apply a low to U13A, zero-setting that device. This places a clear signal onto the three flip-flops in the divide by 8 circuit, causing them to become zero-set. They are thus prevented from generating any more $\overline{TAB}$ signals.

Assume that the circuit is generating $\overline{TAB}$ signals and the X Register comes to rest in the position that addresses a tab in U35. The U35 Data Out line goes low. This low is joined in U53C by a low from U13B. The high from U53C causes U53D to zero-set U13A. When U13A becomes zero-set, the divide by 8 counter is again locked in a cleared condition, preventing additional $\overline{TAB}$ signals. It should be noted that at the same time U13A becomes zero-set, the $\overline{TAB\ BSY}$ is ended.

Assume now that the X Register is resting in a position that calls up a tab indication from U35, and that it is desired to clear this tab position. It can be done as follows: First, the $\overline{SP\ ARM}$ signal must be received to one-set Tab Arm flip-flop U9B. This provides enabling voltages to the Set flip-flop, Clear flip-flop, and the Master Clear flip-flop. The next character input must cause gate U3 to provide a low output. In the configuration shown on the schematic, the number 0 will perform this function. Assuming that a 0 has been received, the low output from U3 causes a high pulse to appear on the Clear flip-flop. The trailing edge of this causes the Clear flip-flop to become one-set, with the zero output causing a $\overline{TAB\ BSY}$ signal to be generated. At the same time, U51A applies a high to the Clear Set gate U51C.

Note that in addition to causing $\overline{TAB\ BSY}$ signal to be generated, U31A releases U11A from its cleared condition. The next 1 MHz pulse causes U11A to become one-set, applying a high to U51C, and a low to U53A. U51C now has two high inputs, and applies a low to the Data In connection of U35. The next time the 1 MHz clock goes

low, two lows are in effect at the input of U53A, causing it to apply a high signal to the R/W input of U35. This high signal writes the low at pin 12 into the RAM, removing the tab indication from that address and the Data Out at pin 14 goes low. It should be noted that the low $\overline{TAB\ BSY}$ signal again was fed back to clear U9B, causing it to become zero-set; thus the Set flip-flop, Clear flip-flop and the Master Clear Control flip-flops become disarmed.

Assume now that a number of tabs exist in the Random/Access Memory, and that all these tabs are to be cleared. Again, we must first receive an $\overline{SP\ ARM}$ signal which causes Tab Arm flip-flop U9B to become one-set, applying an enabling voltage to Master Clear Control flip-flop U29B. If the next character is an M, it causes the U5 output to pulse low, causing U29B to become one-set. The low transition into U37 causes it to generate a pulse of approximately 1.5 milliseconds duration. The zero output from U37 goes to U51A to place a high on U51C. The zero output from U37 also is processed by U31A to release the clear signal from R/W flip-flop U11A and to generate the $\overline{TAB\ BSY}$ signal. As before, the $\overline{TAB\ BSY}$ signal goes back to reset the TAB ARM flip-flop to its cleared condition.

The next 1 MHz CLOCK signal to arrive causes R/W flip-flop U11A to become one-set. This cause a high into U51C and a low into U53A. U51C now has two high inputs, causing a low output to be applied to the Data In terminal of U35. While the zero output from U37 is controlling U51A and U31A, the one output from U37 is applying a positive pulse to the Cnt/Load inputs of U55 and U57. This high signal permits U55 and U57 to be disconnected from the X Registered input lines and allows U55 and U57 to advance through one count for each input of the 1 MHz clock signal. The positive excursion of the 1 MHz clock advances the U55 and U57 count by one position. The negative level of the 1 MHz clock is then applied to R/W Gate U53A. The high pulse from U53A writes the low Data In signal into the Random Access Memory. A low is written into each address as the 1 MHz clock carries the U55 and U57 circuits through their entire range.

The U37 output pulse ends at the end of 1.5 ms. Notice that during pulse time, the 0 output from U37 was being fed back to U29B, locking U29B in a cleared condition. When the pulse ends, U29B remains in that condition until it again becomes enabled by the Tab Arm flip-flop and receives another input signal from U5. It should be noted that throughout the clearing of the tabs, the X Register was permitted to remain stationary. The U55, U57 outputs were clocked serially through their entire range by the combination of the high into pin 9 and the repetitive application of 1 MHz pulses.

One more point should be considered—receipt of a character other than those recognizable by U1, U3, or U5

while the SP ARM flip-flop is armed. In such a case, U1, U3, and U5 apply highs to U7B, causing U7B's output to remain low. This causes U49A to apply a high to U7C. When the $\overline{\text{SP ARM}}$ signal elapses, it applies a high to a second input of U7C. When the TC IN STRB signal arrives, this third high causes a low output of U7C, which results in U9B disarming.

Control Function Decoder TC-7

TC-7 is the control character and special function decoder for the Terminal. It consists principally of two Character Decoders, a Control Function Completes Delay circuit, and the special function output circuitry.

The inputs to the decoders consist of data lines DR1 through DR5. DR5 selects the decoder, and DR1 through DR4 determine its outputs. The CF EXEC signal is applied through an inverter to the decoders as an enabling voltage. Inputs 18 and 19 must both be low in order for the device to decode the DR1 through DR4 information. Therefore, when DR5 is low, U7 is enabled by the CF EXEC signal. When DR5 is high, U11 is enabled by the CF EXEC signal. Thus, if DR1 through DR5 were all high, U11 would be selected; when CF EXEC occurred, a low would appear on output pin 17, resulting in a high US control character signal out of the card.

The special function signals are generated whenever appropriate control characters are decoded by U7 or U11. These are then processed by the applicable circuitry and made available as outputs. It should be noted that although standard factory-wired connections are shown to indicate which signals control the special functions, these resistive straps can be moved to connect any of the control characters to any one of the special function control lines.

CF Comp Delay Circuit. The purpose of this circuit is to provide a 64 μs time delay between receipt of the CF EXEC signal and the CF COMP output signal. This 64 μs permits adequate time for any special function or control character to be executed by the Terminal. The details regarding this special function complete delay circuit can be determined from the timing diagram associated with the TC-7 schematic.

Character Rotator TC-8

TC-8 is the character rotator card, and is optional in the Terminal. When the card is not in use, a bypass card must be in its place. With the bypass card in use, the A, B, C, and D signals appear at the output as KR5, KR6, KR7, and KR8, respectively, and the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ signals appear at the output as KR2, KR3, and KR4, respectively. The KR1 output is held low and the $\overline{\text{KR SHIFT}}$ output is held high.

Assume that the Character Rotator card is in use and that U15A and U15B are in their zero-set condition. (This condition could occur as a result of a $\overline{\text{HOME}}$ signal, an $\overline{\text{INITIAL}}$ signal, or a US signal; it could also occur by having a successive number of NAK signals sufficient to leave the two flip-flops in their zero-set condition.) With the flip-flops zero-set, U13B receives two high signals and U13A, U13D, and U13C receive at least one low signal. Under this condition U35C has all high signals applied, causing a high output on the $\overline{\text{KR SHIFT}}$ line. U11D has a low input, causing it to place highs on 2 section input gates U3A, U5, U25, U7, U27, U9, and U31. Notice that the second input to these sections is provided by the A, B, C, D, $\overline{\text{E}}$, $\overline{\text{F}}$, $\overline{\text{G}}$, inputs as follows: U3A is driven by A, U5 is driven by $\overline{\text{E}}$, U25 is driven by B, U7 is driven by $\overline{\text{F}}$, U27 is driven by C, U9 is driven by $\overline{\text{G}}$, and U31 is driven by D. When row 1 is selected by the Character Generator matrix in TC-16, A, B, C, and D are low. By following these signals to the respective 0° gates, it can be seen that they control the KR5, KR6, KR7, and KR8 outputs—which would also be low at this time. When column 1 is selected, $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ are high. Following them through their 0° gates will result in KR2, KR3, and KR4 being high.

Now assume that an NAK has been received. U15A becomes one-set, causing U13C to receive two highs while the other three NAND gates each receive at least one low. The output of U13C goes low, causing a low $\overline{\text{KR SHIFT}}$ signal to be developed. At the same time, highs are received by one input of the 90° AND gates. The second input to these 90° gates is controlled by their respective A, B, C, D, $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ inputs. Now an interchange of functions has been accomplished. Note that KR1 is now put into use to control the X-axis, because the interchange has caused the 10 rows to be applied to the X Registers instead of the usual 8 columns. It should also be noticed that during 90° operation, the KR5 output is disabled, and is held in a low condition. This occurs because the KR6, KR7, and KR8 lines now are handling the column selection and three lines are sufficient. With 90° character rotation selected, the A, B, C, and D input lines control the KR1, KR2, KR3, and KR4 output lines respectively, while the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines control the KR6, KR7, and KR8 lines, respectively.

Receipt of another NAK signal causes 180° character rotation to be selected. At this time, U15A becomes zero-set and U15B becomes one-set. This condition results in U13D providing a low output to cause the $\overline{\text{KR SHIFT}}$ signal. U13D and U11A provide highs to appropriate AND gates. KR1 is now disabled and is held low, while KR5 is put back into use. Operation is similar to 0° condition except that the A, B, C, and D lines control KR8, KR7, KR6, and KR5, respectively. This causes the inverse of that which existed at 0° character rotation. Under these same circumstances, the $\overline{\text{E}}$, $\overline{\text{F}}$, and $\overline{\text{G}}$ lines control the KR4, KR3, and KR2 lines, respectively.

One more NAK signal causes U13A to receive two highs, with its low output causing a low $\overline{\text{KR SHIFT}}$ signal and

causing highs to be applied to appropriate AND gates. The operation now is similar to that described for 90° operation except that A, B, C, and D now control KR4, KR3, KR2, and KR1, respectively, while $\overline{E}$, $\overline{F}$, and $\overline{G}$ control KR8, KR7, and KR6, respectively.

Y D/A TC-9

The TC-9 circuit description is essentially the same as that for TC-13. Only the differences will be discussed here.

TC-9 does not contain an Italics circuit. Another difference is that TC-9 does contain a Compose circuit. When the Terminal is not in Compose Mode, the input to pin 6 of U87C is high; Q57 and Q77 are turned on. If S99 is set at BTM, CR84 is back-biased and prevents Q77 from affecting U55.

When Compose is selected, the input to pin 6 of U87C goes low, turning Q77 off and placing a high on the anode of CR84. This high passes through S99 to the negative input of U55, causing the output of U55 to hold the CRT beam in the Scratch Pad strip at the bottom of the display area. The D/A circuits now have no effect upon the vertical position of the beam. However, the beam can still be influenced by the character generator matrix signal coming in through the KR5 through KR8 lines at the bottom of the schematic.

If the tube had been rotated so that the Scratch Pad strip were at the top of the CRT, S99 would be in the Top position. Compose Mode would cause Q57 to turn off, placing a low signal through CR88 to the U55 circuit. This low into the negative input of U55 would result in a positive output, holding the display at the top of the CRT in the Scratch Pad area.

Y Data Register TC-10

The Y register contains the following circuits:
        5 Least Significant Bit (LSB) control
        5 Most Significant Bit (MSB) control
        16 Y Parallel control
        512 Y Parallel control
        Step control
        Line Feed Enable
        Line Feed ÷19
        Double Size Character Line Feed control
        Reset Circuit
        Cursor Up
        Page Full

These circuits will be discussed in that order.

5 LSB Control. The 5 LSB control circuit can be driven either parallel or serial. Under initial or reset conditions it is driven in parallel manner. Parallel input gates U41D, U41C,

and U45D are inhibited by the high signal from U57B. The resulting lows from these gates are applied to U41A, U41B, and U45A. When a horizontally oriented display tube is installed, a low is applied to the second inputs of each of these three OR gates, causing their outputs to be high, applying lows to U21 inputs A, B, and D. U21 pin C is receiving a high from U24C because of the effect of U57B on U45B. The high pulse from U57B also passes through U9B to apply a low to the load input of U21, causing the low-low-high-low at A, B, C, and D respectively, to be felt at outputs 3, 2, 6, and 7. These are inverted to cause $\overline{1Y}$, $\overline{2Y}$, and $\overline{8Y}$ to be high, and $\overline{4Y}$ to be low.

The $\overline{16Y}$ line is controlled by U7A. During resetting, the high signal from U57B is coupled through U9B to U3E, where it causes a high output to be applied to U23D. At this time, U24A is also applying a high to U23D, causing a low from U23D to zero-set U7A. This causes the 1 output to be low, causing the 16Y line to be high.

The condition of the just-described five lines is determined by whether a vertical or horizontal format is in use. The description given was for a horizontally oriented CRT. When a vertically oriented CRT is in use, the inputs to U41A, U41B, and U45A are high during the time that the pulse from U57B is high; this results in highs into U21 A, B, and D, causing the $\overline{1Y}$, $\overline{2Y}$, and $\overline{8Y}$ lines to be low. In addition, the high from U57B is inverted by U29E, applying a low through the strap link to U27A, putting a low on U23D, disabling it. Simultaneously, the low is applied to the preset connection of U7A, causing U7A to one-set. With U7A one-set, the one output is high, putting a low on the $\overline{16Y}$ line. It may be noted that U5B serves no function during this resetting action.

5 MSB Control. This circuit can be analyzed in a manner comparable to that used for the 5 LSB control circuit. It should be noted that during horizontal format reset conditions, the low which was applied to U21 is also applied to U25 pin D. This causes the $\overline{256Y}$ line to be high. When vertical format is selected, $\overline{32Y}$, $\overline{64Y}$, $\overline{128Y}$, $\overline{256Y}$, and 512Y lines are all held low during reset. During reset, U1D, U1C and U5C have no effect on the 5 MSB control circuit.

The two circuits described in the preceding paragraphs are normally reset under one of several conditions; one of these is upon receipt of the $\overline{HOME}$ signal; another is when $\overline{ALFA\ ORG}$ is received by way of U9A and U37B into U57B. A third situation causing reset to occur is when Page Full happens. At that time the $\overline{PF\ PULSE}$ from U35D is coupled back through U57B to cause reset to occur.

While in Graphic Mode, a high on the GRAF 2 line disables the $\overline{ALFA\ ORG}$ input and also disables the Page Full circuit. During this time data can be parallel-loaded

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into U21, U7A and their counterparts in the 5 MSB control circuit. The routes for DR1, DR2, DR3, and DR4 can be determined quite easily—they pass through gates and are applied to the inputs of the up-down counters. They are latched into only one counter at a time, the counter being determined by whether a high pulse is applied to the LO Y EN (low Y enable) line or the HI Y EN line. If applied to the LO Y EN line, it causes a low out of U9B, applying a low to the load input of U21. If the high is applied to the HI Y EN input line, it passes through U9D to apply a low to the load input of the 5 MSB counter.

The $\overline{16Y}$ and $\overline{512Y}$ lines are controlled in graphics by the combination of the enable pulse and DR5. If a LO Y EN pulse and a DR5 exist, U23C applies a low to U27A, placing a low at the preset input of U7A, causing U7A to one-set. This applies a low to the $\overline{16Y}$ line. If DR5 and HI Y EN signals exist at the same time, the ANDing is performed by U27B putting a low into U27D, applying a low to the preset input of U7B. This one-sets U7B, applying a low to the $\overline{512Y}$ line.

16Y Parallel Control and 512Y Parallel Control. Although these two are indicated as separate circuits on the schematic, their function was explained with the 5 LSB control and 5 MSB control circuits.

Step Control Circuit. The Step control circuit provides the drive pulse to increment or decrement the 5 LSB control circuit. The direction is determined by U51C, which responds to an $\overline{AUX +Y}$ signal from auxiliary units, a $\overline{+Y}$ signal from the Plot control circuit, and a Cursor Up signal from Cursor Up flip-flop U33B. Normally, these three lines are high, providing a low from U51C, disabling U57C and providing an enabling voltage to U5A. Under the described condition, a low pulse at any one of the three inputs to U51B will cause a low pulse out of U5A; this low pulse is accepted by U21, causing it to decrement one count at a time. When U21 decrements through 0, a low pulse appears on the pin 13 Borrow line. If U7A is one-set, it is an indication that a $\overline{16Y}$ exists and the Borrow is taken from this device. With U7A one-set, its 1 output disables U1D, preventing the Borrow pulse from passing through. The Borrow pulse goes through U5B to clock U7A into a zero-set condition, putting a high on the $\overline{16Y}$ line. The next time U21 clocks through 0 position, another Borrow pulse occurs at pin 13. This time it finds U7A zero-set and U1D is enabled. The Borrow pulse ANDs with the low from U7A in U1D to provide a high out of U1D and a low into the count-down input of the 5 MSB control counter, causing it to decrement by one point or one count. The Borrow pulse from U21 again causes U7A to toggle, this time one-setting it. Subsequent Borrow pulses will repeat the described action.

If U51C in the Step Control circuit is receiving a low from any one of its inputs, it will enable U57C and disable U5A. Now, pulses into U51B will cause U57C to generate low output pulses, and U21 will count up. Subsequent action is very similar to that described for counting down, except that a Carry pulse will be provided by U21 and will be acted on by U5B and U1C in a manner very similar to that described for Borrow.

Line Feed Enable Circuit. The Line Feed Enable circuit permits 2 MHz clock pulses to pass through U31A into the Step Control circuit to cause the counter circuit to increment or decrement according to the existing signals. U31A is normally disabled and becomes enabled in response to one of several signals into U59. One of these is a $\overline{LINE\ FEED}$ through U9C and U37C into U59. Another one is an $\overline{EOL}$ signal through the AUTO LF strap into U59. A third is a $\overline{Y\ CUR\ PULS}$ into U59. And a fourth is a $\overline{DBL\ SZ\ CHR}$ command through U37D, U35B, and U39 into U59. Regardless of which signal arrives at U59, it generates a high output into U57A. As long as Page Full condition does not exist, the 2 MHz signal through U37F clocks a pulse out of U57A which one-sets LF Clock Enable flip-flop U33A. U33A applies a high to U31A, enabling that gate. 2 MHz pulses are then permitted to pass through U31A to clock the counter circuit. The number of 2 MHz clock pulses permitted to pass through U31A is limited to either 19 or 38. Limiting to 19 is done by the Line Feed ÷ 19 circuit U11, U13A, U15, U17, U19B, U37A and the U13B flip-flop. When 19 pulses have passed through this countdown circuit, U33A zero-sets, putting a disabling voltage onto U31A.

Line Feed ÷ 19 Circuit. This circuit consists essentially of a divide-by-19 counter which is best explained through a timing diagram, which is provided opposite from the schematic.

Double Size Character Line Feed Control. If a $\overline{DBL\ SZ\ CHR}$ signal is in effect, U35B has an enabling voltage applied. When a $\overline{LINE\ FEED}$ pulse, or an $\overline{EOL}$ pulse is processed through U35A, it causes the U35B output to go low, thus one-setting U39. The low from the 0 output of U39 holds the U59 output high, resulting in a low from U57A. This holds U33A in a one-set condition. Therefore, when the first pulse from U13B reaches U33A, it is overridden by the low on the preset input. However, the pulse from U13B is routed back to U39, causing it to zero-set. Now the 0 output of U39 is high. This permits the U59 output to go low, providing a high output from U57A. The next U13B pulse to reach U33A resets it to a zero-set condition and disables U31A. In this manner, the counter is caused to step 38 counts in response to a $\overline{LINE\ FEED}$ command instead of stopping after the usual 19.

Reset Circuit. The reset circuit was basically discussed in conjunction with the 5 LSB control and the 5 MSB control circuits at the beginning of this discussion and will not be discussed further.

Cursor Up flip-flop Circuit. Cursor Up flip-flop U33B is one-set upon initialization, and remains in this condition until such a time as a $\overline{\text{CUR UP}}$ signal is commanded by the switch on the keyboard. At this time, U33B becomes zero-set, causing count-up pulses to be delivered by the Step Control circuit. Since the $\overline{\text{CUR UP}}$ is accompanied by a $\overline{\text{Y CUR PULS}}$, the U31A NAND gate and the Line Feed Enable circuit becomes enabled at the same time U33B becomes zero-set. Upon completion of the divide-by-19 countdown, U33A becomes zero-set, and its 0 output applies a high to U33B. The next 2 MHz clock pulse one-sets U33B, removing the low from the Step Control circuit.

One more comment. A $\overline{\text{PRNT BSY}}$ signal can be applied to the Page Full circuit to create a pseudo $\overline{\text{PAGE FULL}}$ signal to prevent Terminal operation until hard copy printing has been accomplished.

Page Full. TC-10 circuit cards 670-1443-01 and above. The page Full circuit will be described next. If not in Scratch Pad mode, Page Full is indicated when $\overline{512Y}$ and $\overline{256Y}$ are high and another Borrow pulse is applied to the input of U7B. This Borrow-during-zero condition indicates that the counters have decremented to zero and that the beam is at the bottom of the CRT, the Page Full position. In Alpha Mode, the other three inputs to U49 are high, causing it to generate a low output pulse, placing a low on U27C. This places a low on the K input of U55B. A simultaneous high from U27C goes to U55B. The next 2 MHZ pulse causes U55B to one-set, generating a PF LITE out of U55B. The low from the zero output of U55B passes through U35C and U53D to generate $\overline{\text{PAGE FULL}}$. The PF LITE signal is applied to U55A, permitting the next 2 MHZ pulse to one-set it. When the 2 MHZ pulse ends, U55A zero-sets and disables U35D. The $\overline{\text{PF PULSE}}$ goes to the interface unit and may be returned to TC-10 as a $\overline{\text{PF RESET}}$ signal. This goes into U31C and is applied to U51A to reset the flip-flop circuit. The $\overline{\text{PF PULSE}}$ from U35D is also looped back to U57B to generate a high output signal which resets the 5 LSB and 5 MSB circuits.

It should be noted that U7B disables PF Gate U49 immediately after the just-described action. This occurs when the trailing edge of the pulse from U5C one-sets U7B.

Removing the U49 low from U27C permits the $\overline{\text{PF RESET}}$ pulse to reset the U27C-U51A flip-flop. With U27C and U51A reset, U55B zero-sets in response to the next 2 MHZ pulse. The $\overline{\text{PAGE FULL}}$ line goes high and PF LITE goes low. The input to U55A goes low, disabling U55A in the zero-set state.

During Scratch Pad modes, $\overline{\text{SP STRIP}}$ inhibits U24D. It also holds U55B zero-set, preventing page full signals from being generated.

Page Full. TC-10 circuit cards 670-1443-00 only. The Page Full circuit will be described next. Page Full is indicated when $\overline{512Y}$ and $\overline{256Y}$ are high and another Borrow pulse is applied to the input of U7B. This Borrow during 0 condition indicates that the counters have decremented to 0 and that the beam is at the bottom of the CRT, the Page Full position. In Alpha Mode the other three inputs to U49 are high, causing it to generate a low output pulse, placing a low on U27C. This generates a low $\overline{\text{PAGE FULL}}$ pulse. A simultaneous high from U27C goes to U55B and U55A. The next 2 MHz pulse to occur causes U55B and U55A to one-set, generating a PF LITE out of U55B and a high out of U55A into U35D. When the 2 MHz pulse again goes high, U35D generates a low $\overline{\text{PF PULSE}}$. When the 2 MHz pulse ends, U55A 0-sets and disables U35D. The $\overline{\text{PF PULSE}}$ goes to the interface unit and may be returned to TC-10 as a $\overline{\text{PF RESET}}$ signal. This goes into U31C and is applied to U51A to reset the flip-flop circuit. The $\overline{\text{PF PULSE}}$ from U35D is also looped back to U57B to generate a high output signal which resets the 5 LSB and 5 MSB circuits.

It should be noted that U7B disables PF Gate U49 immediately after the just-described action. This occurs when the trailing edge of the pulse from U5C one-sets U7B.

Removing the U49 low from U27C permits the $\overline{\text{PF RESET}}$ pulse to reset the U27C-U51A flip-flop. With U27C and U51A reset, the $\overline{\text{PAGE FULL}}$ line goes high and the input to U55A goes low, disabling U55A in the zero-set state. Although the output of U27C returns low, the PF LITE flip-flop U55B remains one-set until such time as a $\overline{\text{FULL}}$ pulse is received, permitting the 2 MHz clock to zero-set U55B.

In/Out Data Routing TC-11

TC-11 is the input/output data routing board for the Terminal, and it contains the following principal circuits:

Output Latches

Input Latches

Local Control

Output Latch Clear

Graphic Word Assembler

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The output latches accept B1 through B8 data from the keyboard, scratch pad, or auxiliary inputs. Upon receipt of a DATA STRB, the data is latched through, making it available on the interface output lines TB1 through TB8. If LOCAL ECHO exists or if ON LINE is low, U27C sends a high through U5B to provide a low to U29D. With AUX PLOT low, this places a high on U3B and on the Local Control gates U23C through U37C. Then when a DATA STRB occurs, U3B sends a DROP FLG signal to the interface to prevent data from going to the computer. At the same time, gates U23C through U37C AND with data from the output latches to make the data bits available on the DR1 through DR8 lines. The output latches are cleared upon completion of character processing. For example, if On Line condition exists and data is being transmitted through the interface to the computer, it is followed by an LE COMP. This is applied to U5C in the Output Latch Clear circuit, is processed through U27D, U27B, and U45A to clear both Output Latches.

Input Latch Circuit. When data is received from the computer and interface, it appears on the RB1 through RB8 lines and is accompanied by RCV STROB. The strobe latches the data bits into U47 and U51, making them available at the output of the latches. From there these bits are routed through U25B through inverters and OR gates and are made available to the Terminal circuits on the DR1 through DR8 lines.

Graphic Word Assembler. The purpose of this circuit is to accept bytes of input information during Graphics Mode and route these bytes to the appropriate data registers in five-bit bytes. The sequence in which these bytes is routed is determined by straps R7, R13, and R5. Standard factory connection for these straps requires that bytes be supplied to the Terminal in the following sequence: high Y, low Y, high X, and low X. This discussion will assume that these straps are as shown on the schematics and the given sequence is being presented.

When Linear Interpolate or Point Plot Mode is selected, GS+FS goes low, causing the Graf FF to change states. U3C provides a low to U29C. The accompanying high from U27A serves several purposes—it provides enabling voltage to Byte Decoder U7, and enabling voltage to NAND gate U13A. It also removes the low which had been holding Hi byte flip-flop U11 zero-set. When graphic bytes are clocked into the TC-11 circuitry, the bit 7 and bit 6 configuration is determined by the byte being received. For example, high X byte has bit 7 low and bit 6 high; the low X byte has them high, low; the high Y byte has them low, high; and the low Y byte has them high, high. Upon receipt, these bits are applied to byte decoder U7 along with SYNC STRB, which is applied through U5F. The leading edge of the SYNC STRB clocks bit 7 and 6 through U7, placing a low on either the 4, 6, 5, or 7 output lines. If the high X byte is being received, it causes U7 pin 6 to go low, placing

enabling voltages on U29B and A. The high on Pin 4 of U7 holds the LOW Y EN line low and maintains a disabling voltage on the J input of HI BYTE FF U11. Pin 5 of U7 is also high, putting a low disabling voltage on the K input of U11, and on the LO X EN line. In addition, it places a low on U13A, disabling that gate. The high from pin 7 of U7 places a low on U29C to AND with the low from the GRAF flip-flop. The high output from U29C causes a low GWA output command, indicating that the Graphic Word Assembler is being employed.

Go back to Hi Byte flip-flop U11. Prior to the time that the GRAF flip-flop had been put into Graphics Mode, a low from U27A had held U11 zero-set. The low from U11 pin 8 held a low on U29B. When the high Y byte is decoded by U7, the low from pin 6 ANDs with the low from U11 pin 8, causing a HI Y EN pulse from U29B. The HI Y EN also goes through U33D to cause a high out of U13C, placing an enabling voltage on U15A. U15A is negative-edge conscious and when the SYNC STRB input ends, it causes the high at the J input of U15A to clock through and apply a high to the J input of U15B. The next 1 MHz clock pulse finds its negative transition one-setting U15B, causing the GWA COMP signal to go low. This GWA COMP signal is fed back through U13D and U13B to zero-set U15A, causing the U15B J input to go low. The next 1 MHz clock pulse has its negative edge zero-setting U15B, causing GWA COMP to end. This signal is an indication to the Interface Unit that the Graphic Word Assembler has loaded the byte into the appropriate register.

The next byte to arrive is a low Y byte and it contains a high bit 7 and a high bit 6. With pins 3 and 13 of byte decoder U7 high, its pin 4 output goes low when the SYNC STRB pulse arrives. This places a high on the LO Y EN line, at the same time holding lows on the HI Y EN, HI X EN, and LO X EN lines. The high on the LO Y EN line is applied to the J input of U11 and is also applied through U33A and U13C to the J input of U15A. When the SYNC STRB ends, U11 and U15A both become one-set. U11's change of state is a preparatory step towards having the next high byte enabling the HI X EN line. When U15A changed state, it caused a high to be applied to U15B, so that the GWA COMP pulse can be generated by the next 1 MHz pulse just as it did when the high Y byte was loaded.

When the GWA COMP pulse ends and the interface supplies the TC-11 with the high X byte, it is accompanied by a low bit 7 and a high bit 6. This causes a low on pin 6 of U7, providing enabling voltage to U29B and U29A. Since U11 is one-set, U29A now has two lows and generates a HI X EN output pulse. Incidentally, this pulse is of the same width as the Sync Strobe that caused it. This HI X EN pulse passes through U33A, U13C and is applied to the J input of U15A. The end of the SYNC STRB clocks U15A and causes U15B to generate another GWA COMP pulse as before. When the fourth byte (low X) is applied to the

CONNECTOR WIRE LIST (cont)

J342 AUXILIARY CONNECTOR

PIN		NAME	T	CONN	
1		SEND	*P	TC01	02
2	S	INTENS 2	*L	J144	14
				J251	8
				J256	3
				TC19	8
3		DR1	P	TC11	10
4		HCU PRNT	*P	TC07	28
5		XMITCOMP	*P	J121	27
6	S	AG	*L	J144	32
				TC19	28
7					
8	S	AUX PLT	*L	J144	31
9		ERAS INTV	*P	J251	07
10					
11		VIEW	*P	TC01	16
12	S	AUX PLOT	*L	J144	29
				TC14	20
13		ON LINE	L	J101	17
14					
15		ERASE	*P	TC01	0V
16		GWA	L	TC11	13
17					
18		DATA STRB	P	TC02	21
19		SP ERASE	*P	TC07	24
20		DR7	P	TC11	25
21		DR4	P	TC11	12
22		DR3	P	TC11	11
23		DR2	P	TC11	09
24					
25		DR6	P	TC11	23
26		DR5	P	TC11	26
27		XMIT RDY	L	TC19	13
28		RCV RDY	L	TC19	19
29		DR8	P	TC11	24
30		LOAD DATA	*P	J121	26
31					
32					
33					
34					
35	S	TC INHIB	*L	J144	18
				TC14	2
36					
37					

J343 AUXILIARY CONNECTOR

PIN		NAME	T	CONN	
1		HC GND	L	PWR SUP	
2		H COPY	L	J251	13
3	S	AUX −X	*P	J144	27
				TC12	U
4		2X	*P	TC12	02
5		1X	*P	TC12	03
6					
7					
8		PRGM GND	L	PWR SUP	
9	S	INTENS 3	*L	J251	9
				J254	2
10		4X	*P	TC12	04
11	S	AUX +Y	*P	J144	22
				TC10	V
12		32X	*P	TC12	09
13		64X	*P	TC12	06
14		128X	*P	TC12	08
15		256X	*P	TC12	07
16		512X	*P	TC12	11
17		16X	*P	TC12	10
18		8X	*P	TC12	05
19	S	AUXPLOTX	*P	J143	15
				TC12	16
20		REFRSH	L	TC04	27
21	S	AUXPLOTY	*P	J142	27
				TC10	7
22		ALFA	L	TC18	09
23		FULL	*P	TC01	22
24					
25		4Y	*P	TC10	05
26					
27		LE	*L	J121	10
28		2Y	*P	TC10	02
29		16Y	*P	TC10	06
30		1Y	*P	TC10	08
31		FUNC COMP	P	TC02	00
32		32Y	*P	TC10	07
33		64Y	*P	TC10	09
34		8Y	*P	TC10	00
35		128Y	*P	TC10	0H
36		256Y	*P	TC10	0L
37		512Y	*P	TC10	0M

CONNECTOR WIRE LIST (cont)

J344 AUXILIARY CONNECTOR

PIN	NAME	T	CONN
1	ACK	*P	TC07 20
2	SUB	*P	TC07 06
3	CAN	*P	TC07 08
4	LF	*P	TC07 05
5	FS	P	TC07 0F
6	NAK	P	TC07 0X
7	BS	*P	TC07 09
8	US	P	TC07 0E
9	SYN	*P	TC07 0P
10	FF	*P	TC07 0H
11	EM	*P	TC07 0N
12	VT	*P	TC07 0K
13	BEL	*P	TC07 19
14	ESC	*P	TC07 0L
15	HT	*P	TC07 0M
16	ETB	*P	TC07 0T
17	EOT	P	TC07 0V
18	DC4	*P	TC07 0U
19	ENQ	P	TC07 0W
20	GS	P	TC07 0J
21	DC2	P	TC07 0Y
22	STX	*P	TC07 0Z
23	ETX	*P	TC07 AA
24	DC3	P	PWR SUP
25	SOH	*P	TC07 25
26	DLE	P	TC07 DD
27	NUL	*P	TC07 EE
28	DC1	P	TC07 FF
29	CR	P	TC07 02
30	SI	*P	TC07 0D
31	RS	P	TC07 0B
32	SO	*P	TC07 0C
33	−15V	L	PWR SUP
34	+15V	L	PWR SUP
35	GND	L	PWR SUP
36	+5V	L	PWR SUP
37	CLR TO SND	L	J121 22

TC-3 CONNECTOR (J3)

PIN		NAME	T	CONN
A		MOS DATA	P	TC14 0W
R		GND	L	PWR SUP
S		+5V	L	PWR SUP
Y		MOS CLK	P	TC04 CC
14		+15V	L	PWR SUP
15		−15 V	L	PWR SUP
27	S	MOS DATA	*P	J144 30
				J341 37
				TC14 FF

TC-17 CONNECTOR (J17)

PIN	NAME	T	CONN	
EE	CHAR EXEC	*P	TC14 0Y	
H	DB1	P	TC14 0B	
J	DB2	P	TC14 0C	
K	DB3	P	TC14 0D	
L	DB4	P	TC14 03	
M	DB5	P	TC14 04	
R	GND	L	PWR SUP	
S	+5V	L	PWR SUP	
T	DB7	P	TC14 08	
U	DB6	P	TC14 0P	
V	DB8	P	TC14 09	
X	SCAN CLK	P	TC15 21	
1	HOME	*L	TC01 05	①
2	1Y	*P	TC10 0B	①
3	DC4	*P	TC07 0U	①
4	2Y	*P	TC10 02	①
5	4Y	*P	TC10 05	①
6	GRAF Z	P	TC18 08	①
7	L1 BUSY	*P	TC18 19	①
8	REFRSH	L	TC04 27	①
14	+15V	L	PWR SUP	
15	−15 V	L	PWR SUP	
20	CG RESET	P	TC15 DD	
22	E	*P	TC16 22	
23	F	*P	TC16 23	
24	G	*P	TC16 24	
25	AGREE	*P	TC05 0V	
26	ALFA 2	L	TC18 10	
28	CHAR PROC	*P	TC16 28	①

NOTE 1 : Not connected on TC-0 number 670-1522-00.

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BLOCK DIAGRAM DESCRIPTION

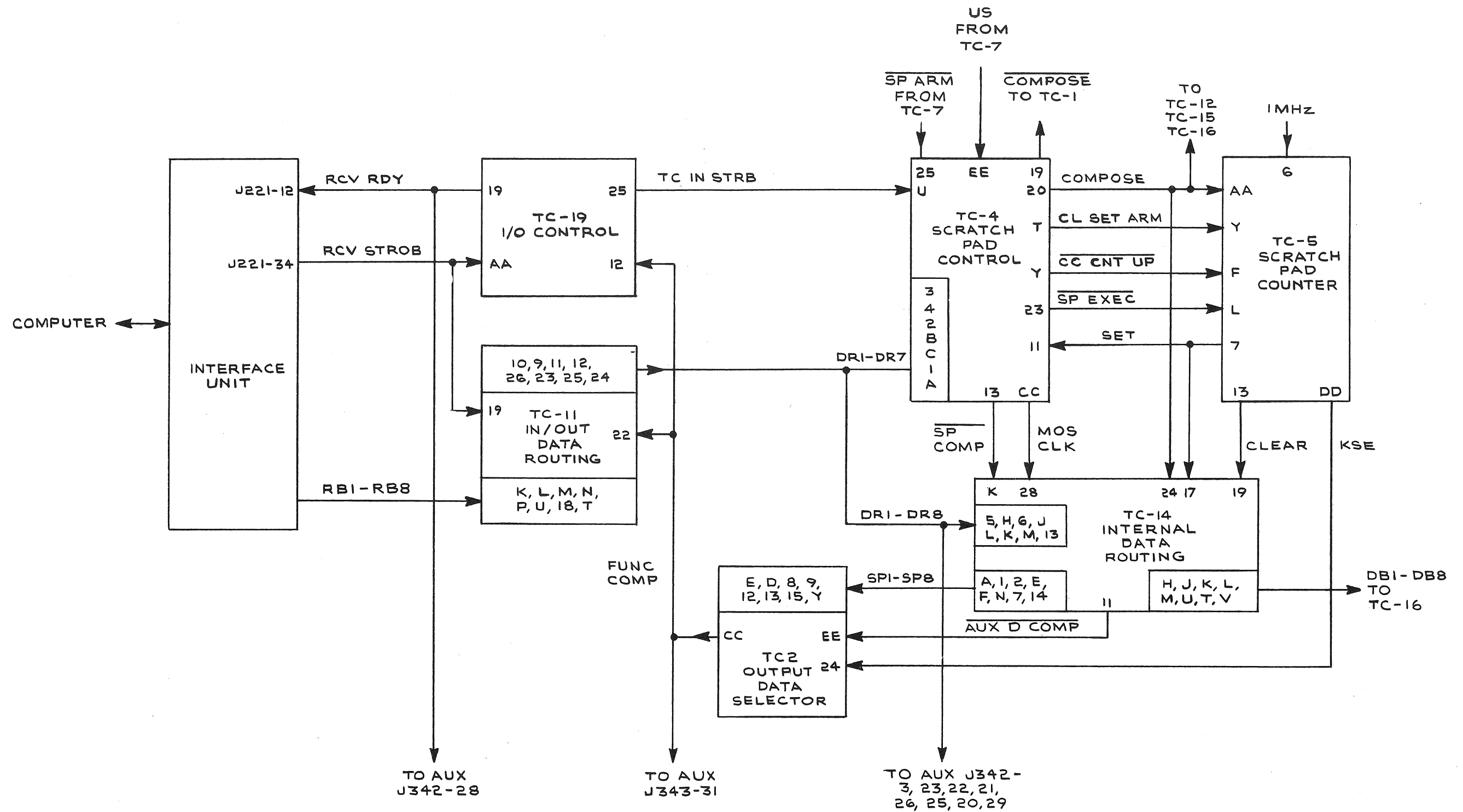### Receiving—On Line-Direct-Unrefreshed Scratch Pad Mode

General. In this mode, the Scratch Pad Memory circuit is loaded from the Interface Unit, without displaying the characters on the screen. This permits more rapid reception of a block which can be checked before being displayed. Checking is done by circuitry in the Interface Unit.

Description. When a RCV STROB brings in data bits containing Escape character, the DR1 through DR7 bits are decoded in TC-4 where they arm the Scratch Pad control circuitry. (The same effect can be obtained by sending $\overline{\text{SP ARM}}$ in from TC-7. $\overline{\text{SP ARM}}$ is strappable in TC-7 so that it can be controlled by any control character.) If the next character sent to the Terminal is a US, TC-7 decodes it and sends it to TC-4 where it puts the Terminal in Unrefreshed Scratch Pad Mode. COMPOSE goes high and $\overline{\text{COMPOSE}}$ goes low. $\overline{\text{COMPOSE}}$ goes to TC-1 to disable the bell. COMPOSE goes to numerous circuit cards to establish Scratch Pad operation.

The next character is strobed into TC-11 by the RCV STROB, and the DR bits are routed to TC-4. The RCV STROB also causes TC-19 to put a low on the RCV RDY line, and to generate the TC IN STRB signal for TC-4. TC-4 produces a CL SET ARM signal, and presets the CC CNT UP circuit. The CL SET ARM signal causes TC-5 to produce a 1/2 μs CLEAR signal followed by a 1/2 μs SET signal. CLEAR goes to TC-14 to insure that the shift register is empty, and then SET loads the DR bits. (The bits become available on the DV lines to TC-16 and the SP lines to TC-2, but are not used at this time.)

SET also goes to TC-4. When it ends, TC-4 sends a 1 μs $\overline{\text{SP COMP}}$ pulse and 8 MOS CLK pulses to TC-14. The $\overline{\text{SP COMP}}$ generates an $\overline{\text{AUX D COMP}}$ signal which goes to TC-2 to generate FUNC COMP, which goes to TC-11 to clear the latches and to TC-19 to reset RCV RDY high. The eight MOS CLK pulses serially shift the inserted character into the memory, removing them from the DB and SP lines. TC-4 also sends a $\overline{\text{CC CNT UP}}$ to TC-5 to increment the cursor counter register, and an $\overline{\text{SP EXEC}}$ to TC-5 to increment the position counter. When the Scratch Pad memory is fully loaded, KSE goes low to inhibit KB entry, although no such restraint is put on inputs from the computer.

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FIG 5-18
BLOCK DIAGRAM
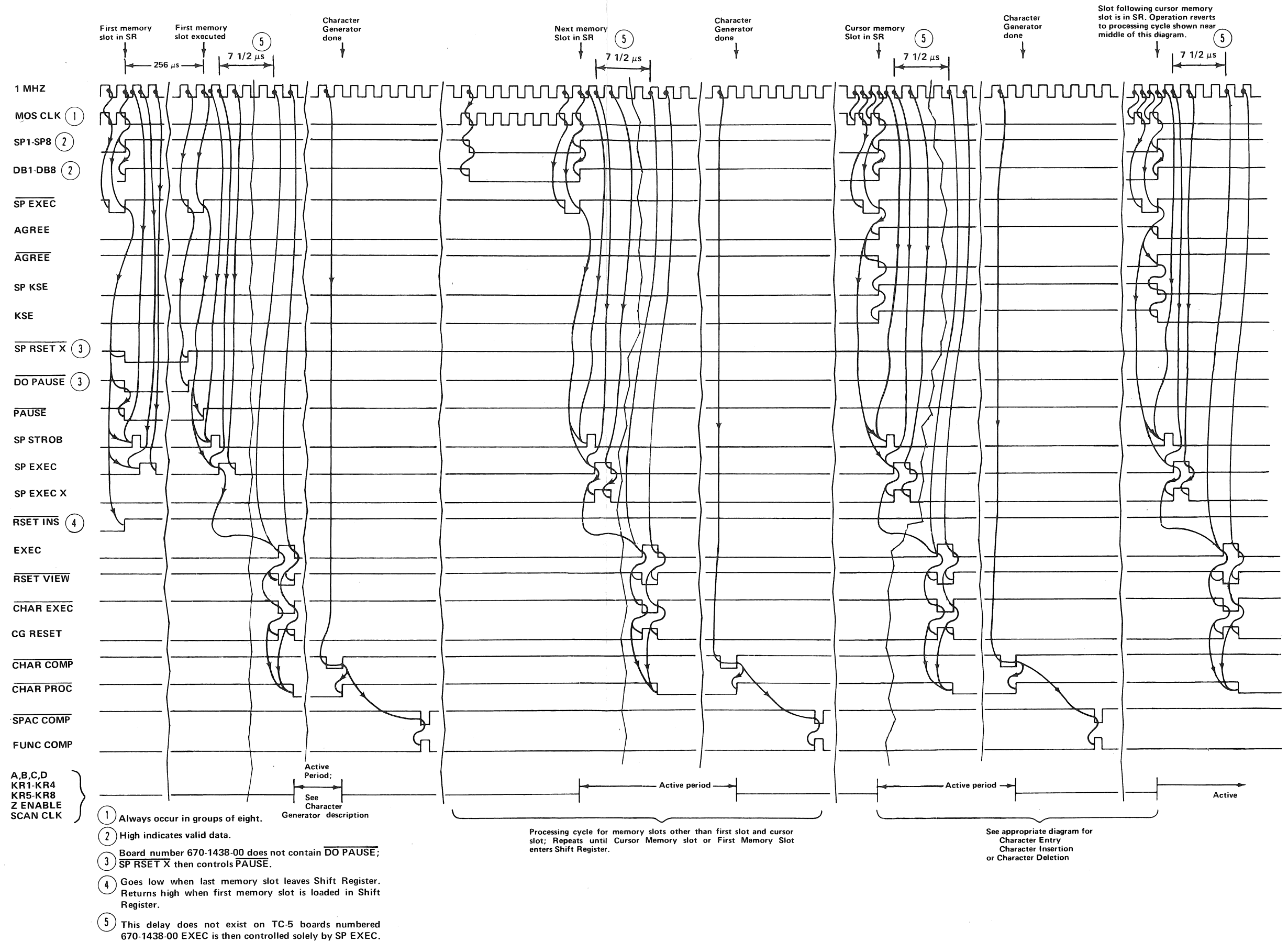RECEIVING IN UNREFRESHED
SCRATCH PAD MODE   1171 EKP

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Notes:

1. Always occur in groups of eight.

2. High indicates valid data.

3. Board number 670-1438-00 does not contain DO PAUSE; SP RSET X then controls PAUSE.

4. Goes low when last memory slot leaves Shift Register. Returns high when first memory slot is loaded in Shift Register.

5. This delay does not exist on TC-5 boards numbered 670-1438-00 EXEC is then controlled solely by SP EXEC.

Processing cycle for memory slots other than first slot and cursor slot; Repeats until Cursor Memory slot or First Memory Slot enters Shift Register.

See appropriate diagram for Character Entry Character Insertion or Character Deletion

Fig. 5-19. Refreshed Scratch Pad timing.

Character
key pressed

≥ 1 ms | 264 µs | 264 µs

1 MHZ

KB1-KB7 ①

KB8 ①

BIT 8 ①

RAW STROB ①

RKB STROB ①

MOS CLK ②

$\overline{\text{SP EXEC}}$ ③

SP KSE

KSE ③

KB STROB

DATA STRB

B1-B8

DR1-DR8

TC IN STRB

CL SET ARM

CLEAR

SET

SP1-SP8

DB1-DB8

$\overline{\text{CC CNT UP}}$

① Ends when key is released

② Always occur in groups of eight

③ Referenced to Fig. 5-19.
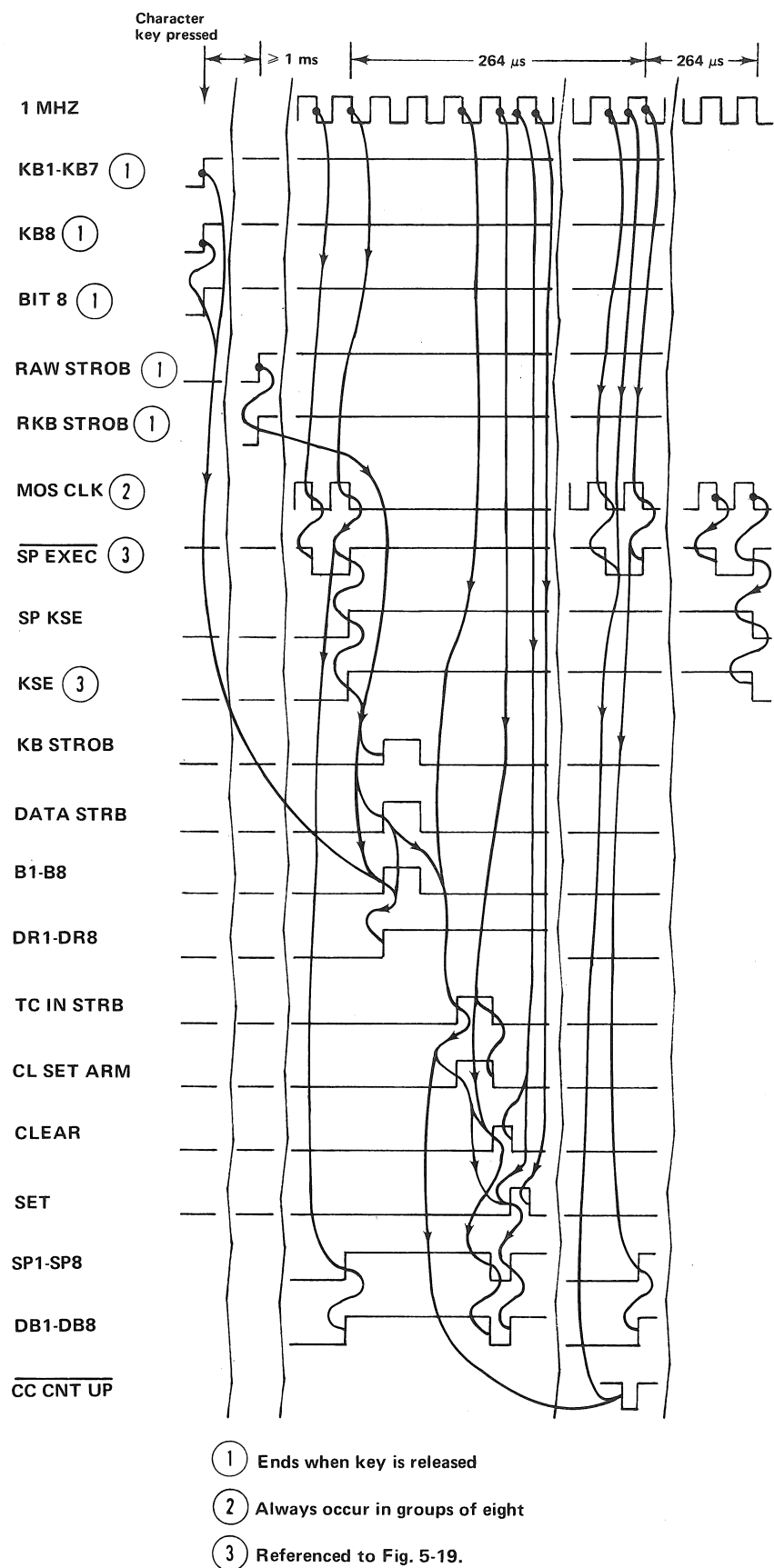
Fig. 5-20. Character Entry variation to Refreshed Scratch Pad timing. Events are additions to or variations of events in area designated on Fig. 5-19.

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Left diagram signal labels (top to bottom):
1 MHZ
EDIT KY
EDIT
CS LOAD
EDIT FF (1)
EDIT LMP (1)
KB1-KB7
KB8
BIT 8
RAW STROB
RKB STROB
MOS CLK (2)
SP EXEC
AGREE
SP KSE
KSE
KB STROB
DATA STRB
B1-B8
TC IN STRB
CL SET ARM
CLEAR
SET
COUNT DWN
CC CNT DWN
SP STROB
SP EXEC
CC CNT UP
EXEC
DR1-DR8
DELETE
AUX D COMP
FUNC COMP

Column markers: Edit Key Pressed, Edit Key Released, Delete Key Pressed

10 ms, 1 ms
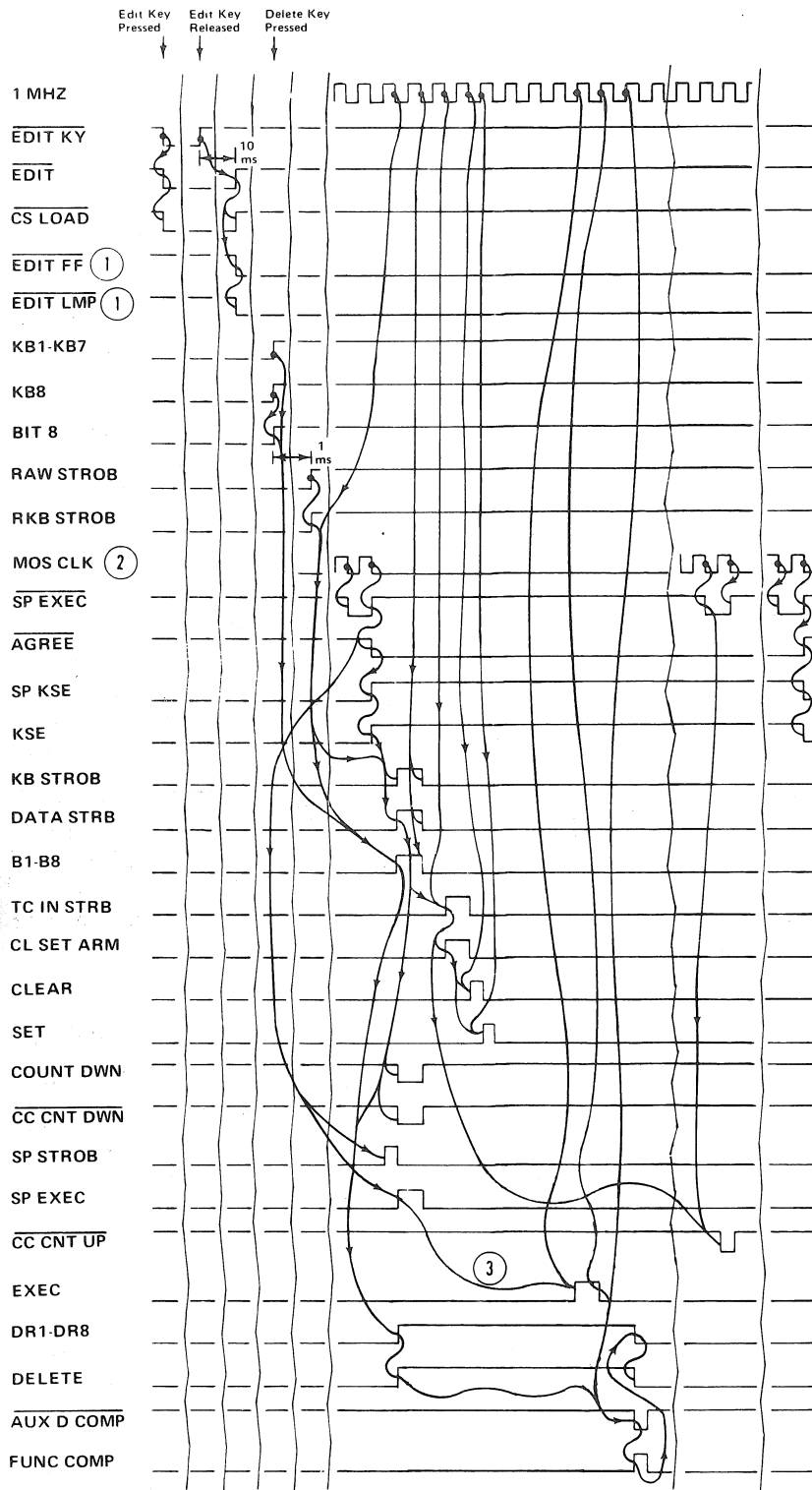
Fig. 5-21. Edit Mode, Delete operation. Timing is a variation of Refreshed Scratch Pad timing. Events are additions to or variations of events shown in Fig. 5-19.

Right diagram signal labels:
EDIT KY
EDIT
CS LOAD
EDIT FF
EDIT LMP
INSERT (1)
SP EXEC (2)
AGREE
INSERT FF
DATA STRB (2)
COUNT UP

Column markers: Edit Key pressed, Edit Key released, Insert Key pressed

10 ms
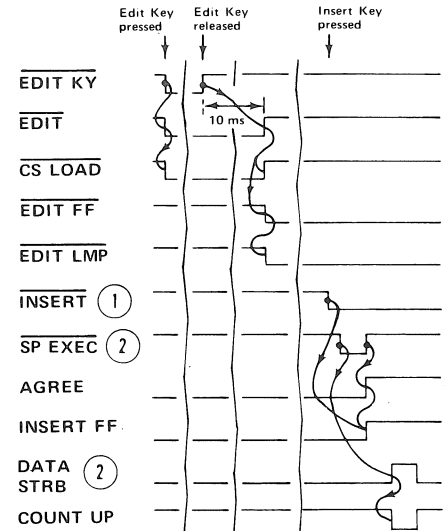
(1) Key must be held down during character insertion. Signal ends when key is released.

(2) Referenced to Fig. 5-20.

Fig. 5-22. Edit Mode, Insert operation. Timing shown is in addition to Character Entry timing shown in Fig. 5-20.

(1) Ends when Edit key again pressed or upon exiting from Scratch Pad Mode.

(2) Referenced to Fig. 5-19.

(3) This 7 1/2 µs delay does not exist on TC-5 boards numbered 670-1438-00. EXEC is then controlled solely by SP EXEC, and AUX D COMP follows the trailing edge of EXEC by 1 1/2 µs.

BLOCK DIAGRAM DESCRIPTION

Refreshed Scratch Pad Modes

The Refreshed Scratch Pad Block Diagram contains the signal lines (and pin numbers) which are incidental to the various modes of Refreshed Scratch Pad operation. The modes are explained separately in the following paragraphs under these titles: Entering Into Compose Mode; Quiescent Compose Operation; Character Entry; Edit Mode; Delete Operation; and Insert Operation.

Entering Into Compose Mode. If the Keyboard switch is at Scratch Pad, a $\overline{\text{COMP SW}}$ goes to TC-4. When a character is entered at the Keyboard, a RAW STROB signal goes to TC-1 to generate RKB STROB. This goes to TC-2 to generate KB STROB which combines with $\overline{\text{COMP SW}}$ in TC-4 to generate COMPOSE, $\overline{\text{COMPOSE}}$, and REFRSH, putting the Terminal into Compose Mode. If the TC-5 card is numbered 670-1433-01 or above, compose into TC-5 generates $\overline{\text{ST STRIP}}$ which goes to TC-9 to hold the X Register in the Scratch Pad area of the CRT. REFRSH into TC-19 causes RCV RDY to go low and sends $\overline{\text{LOC ECHO}}$ to TC-11 to permit the B1 through B8 bits to go to TC-14 as DR1 through DR8.

Quiescent Compose Operation. In Refreshed Mode, the Scratch Pad continually circulates characters through its memory and shift register. If the memory is empty, a succession of NUL characters (all low bits) is circulated. Circuit effect is as follows: Every 256 μs a series of eight MOS CLK pulses is generated in TC-4 and goes to TC-14 to shift eight bits from memory into the shift register. They are made available to the Character Generator on the DB1 through DB8 lines. They are also made available to TC-2 on the SP1 through SP8 lines, although only used there during Send operation.

After the eight MOS CLK pulses, an $\overline{\text{SP EXEC}}$ goes from TC-4 to TC-5 to increment the position counter. (The position counter keeps count of which Scratch Pad memory character slot is in the TC-14 shift register.) Then an SP STROB goes to TC-5, followed by an SP EXEC. The SP EXEC causes TC-5 to generate an SP EXEC X pulse for TC-12 and an EXEC pulse for TC-14.

TC-12 uses the SP EXEC X pulse to increment the X register to the next character position, after which it sends a $\overline{\text{SPAC COMP}}$ to TC-2. This generates a FUNC COMP from TC-2, which goes to TC-4, TC-11, and TC-19. (FUNC COMP signals are not instrumental in quiescent Compose operation.)

TC-14 uses the EXEC pulse to generate $\overline{\text{RSET VIEW}}$ and $\overline{\text{CHAR EXEC}}$. $\overline{\text{CHAR EXEC}}$ goes to the Character Generator circuit to cause it to scan through its matrix. The Char-

acter Generator sends $\overline{\text{CHAR PROC}}$ to TC-14 and TC-19. During matrix scanning, the Character Generator and Rotator circuits send out A, B, C, D, and KR1 through KR4 signals to TC-13, and KR5 through KR8 signals to TC-9 to move the beam position through the character-writing matrix. It also examines the DB1 through DB8 coding and sends out Z ENABLE pulses when dots are to be written. TC-9, TC-13, and TC-18 route the position and unblanking information to the Display Unit. (See the Receiving—On Line-Alphanumeric Mode Block diagram description, or individual circuit card descriptions, if a more detailed description of the Character Generator operation is required.) When through with the matrix, the Character Generator sends $\overline{\text{CHAR COMP}}$ to TC-12 and ends $\overline{\text{CHAR PROC}}$ into TC-14 and TC-19. ($\overline{\text{CHAR COMP}}$ into TC-12 serves no function in Compose Mode.)

The preceding sequence repeats itself every 256 μs, until the last memory character slot is in the shift register in TC-14. Then the Position Counter in TC-5 sends out a $\overline{\text{RSET INS}}$ to TC-14. ($\overline{\text{RSET INS}}$ is not used except during Edit Mode.) After the first character slot is shifted into the TC-14 shift register, the $\overline{\text{SP EXEC}}$ pulse (which follows the eight MOS CLK pulses) ends the $\overline{\text{RSET INS}}$ pulse and causes $\overline{\text{SP RSET X}}$ and $\overline{\text{DO PAUSE}}$, during which time EXEC and SP EXEC X are inhibited. ($\overline{\text{DO PAUSE}}$ occurs only in TC-5 cards number 670-1438-01 and above. In lower numbered cards its function is performed by $\overline{\text{SP RSET X}}$.)

$\overline{\text{SP RSET X}}$ goes to TC-12. TC-4 responds with a $\overline{\text{PAUSE}}$ signal for TC-5, while TC-12 zeroes the X register (sets beam to left edge of screen). 256 μs later, another $\overline{\text{SP EXEC}}$ pulse is emitted by TC-4, after which $\overline{\text{PAUSE}}$ ends. $\overline{\text{PAUSE}}$ is not generated again until 100 MOS CLK groups later, when the first character slot is again in the shift register.

TC-5 contains a Cursor Counter which maintains a record of the cursor position. Whenever that memory slot is in the shift register, TC-5 generates an $\overline{\text{AGREE}}$ signal which causes the Character Generator to print the cursor. If a character is also in that memory slot, both the character and the cursor are written. The $\overline{\text{AGREE}}$ signal also causes TC-4 to produce an SP KSE pulse, which causes TC-5 to generate a KSE pulse for TC-2. This permits character entry into the Scratch Pad through TC-2.

Character Entry. When a character is entered at the Keyboard, KB1 through KB7 go from the Keyboard to TC-2, while KB8 goes to TC-1 and BIT 8 goes from TC-1 to TC-2. The RKB STROB is applied to TC-2. When the Scratch Pad cursor memory slot is in the TC-11 shift register, TC-5 sends an $\overline{\text{AGREE}}$ signal to TC-4. TC-4 sends an SP KSE to TC-5, which sends a KSE to TC-2, permitting it to

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generate a KB STROB and a DATA STRB, and permitting the KB1 through KB8 data to go to TC-11 as B1 through B8. The KB STROB goes from TC-2 to TC-4, and DATA STRB goes to TC-11, TC-4, and TC-19. The KB STROB has no effect in TC-4 unless the Terminal is in Direct Mode with the rocker switch at Scratch Pad position. (Under that circumstance, the Terminal switches to Compose Mode as previously described.) The DATA STRB into TC-4 is used in Edit Mode only.

DATA STRB into TC-19 generates the TC IN STRB, while DATA STRB into TC-11 loads the B1 through B8 bits into latches, making them available on the DR1 through DR8 lines to TC-4 and TC-14. The TC IN STRB goes to TC-4 to generate a CL SET ARM signal for TC-5. TC-5 then sends a CLEAR signal to TC-14 to clear the shift register. This is followed by a SET signal from TC-5 to TC-4 and TC-14. (SET affects TC-4 only in Unrefreshed Mode.) In TC-14, SET loads the DR1 through DR8 bits into the shift register. The next set of MOS CLK pulses is followed by a $\overline{\text{CC CNT UP}}$ from TC-4 to TC-5, which increments the cursor counter in TC-5 by one, advancing the cursor to the next character slot in the memory circuit. Subsequent MOS CLK pulses cycle them through the memory circuit as explained for Quiescent Compose operation.

Edit Mode. When the Edit key is pushed at the Keyboard, an $\overline{\text{EDIT KY}}$ signal goes to TC-1, which sends an $\overline{\text{EDIT}}$ signal to TC-4. If in Compose Mode, a $\overline{\text{CS LOAD}}$ goes from TC-4 to TC-5 to load the cursor counter register contents into the cursor storage register. When $\overline{\text{EDIT}}$ ends, TC-4 sends an $\overline{\text{EDIT FF}}$ signal to TC-1, TC-5, and TC-14; TC-1 sends an $\overline{\text{EDIT LMP}}$ signal to the Keyboard to light the Edit lamp; TC-5 uses the $\overline{\text{EDIT FF}}$ signal during Send operation only; TC-14 uses the signal as enabling voltage for Insert and Delete operation.

A Quiescent Edit Operation now exists, which is the same as Quiescent Compose Operation except for the added signals and the lighted Edit lamp.

If the Edit key is pushed again, $\overline{\text{EDIT KY}}$ again causes $\overline{\text{EDIT}}$, which causes TC-4 to generate $\overline{\text{CC LOAD}}$. This causes TC-5 to load the cursor storage contents into the cursor counter. When $\overline{\text{CC LOAD}}$ ends, $\overline{\text{EDIT FF}}$ goes high and $\overline{\text{EDIT LMP}}$ into the Keyboard goes high, extinguishing the Edit lamp.

Delete Operation. If the Delete key is pushed while in Edit Mode, the character under the cursor is removed from memory and a NUL is put in its place. This happens as follows: When Delete is entered at the Keyboard, KB1 through KB7, BIT 8, and RKB STROB go to TC-2. When the cursor memory slot is in the shift register, $\overline{\text{AGREE}}$ goes from TC-5 to TC-4, SP KSE from TC-4 to TC-5, KSE from TC-5 to TC-2. DATA STRB then goes to TC-11, TC-4, and TC-19, while B1 through B8 go to TC-11. DATA STRB into TC-11 causes the B1 through B8 bits to emerge from TC-11 as DR bits, which are used by TC-14. In TC-14 a

detector senses the DELETE character, which causes the shift register to be bypassed by the memory loop.

A DELETE signal is also sent from TC-14 to TC-4. DATA STRB and DELETE combine in TC-4 to generate a CC CNT DWN signal and a COUNT DWN signal to make TC-5 decrement the cursor counter and cursor storage registers. An $\overline{\text{AUX D COMP}}$ signal is generated in TC-14 after the DELETE signal ends. This goes to TC-2 to generate FUNC COMP which clears the data register in TC-11.

DATA STRB into TC-19 causes TC IN STRB to go to TC-4, where it causes a $\overline{\text{CC CNT UP}}$ signal to go to TC-5 after the next set of eight MOS CLK pulses. This increments the cursor counter by one, restoring it to its previous slot in the Scratch Pad memory.

The Terminal then returns to Quiescent Edit Operation except that the shift register is still bypassed by the memory loop in TC-14. This exists until the last memory slot is shifted past the shift register. Then the $\overline{\text{RSET INS}}$ pulse from TC-5 goes to TC-14 to re-insert the empty shift register into the memory loop. The Terminal then returns to Quiescent Edit Operation, functioning as previously described.

Insert Operation. If a character is to be inserted, the Terminal must be in Edit Mode, the Insert key held down, and a character key pressed. The Insert key generates an $\overline{\text{INSERT}}$ signal for TC-4 and TC-14. It provides TC-4 with an enabling voltage, and causes TC-14 to place an empty "Insert Shift Register" in the memory loop. TC-14 sends an INSERT FF signal to TC-5 to account for the character slot added to the Scratch Pad memory loop. The empty shift register is inserted when the cursor slot is in the shift register, causing a NUL to be inserted in memory immediately following the cursor slot. In addition, parallel entry into the shift register is blocked and parallel entry into the insert shift register is enabled.

When a character is entered at the Keyboard, it waits until an $\overline{\text{AGREE}}$ signal occurs, indicating that the cursor slot is in the shift register. This also indicates that the NUL slot is in the insert shift register. The character being entered is then accepted into the insert shift register in a manner identical to that previously described for Character Entry, except that the DATA STRB which accompanies character entry also causes TC-4 to emit a COUNT UP signal. This causes the cursor storage register in TC-5 to increment to account for the added character.

There is one additional character slot in memory when the insert shift register is in the loop, and it must be removed to return to quiescent operation. Therefore, when the last character slot is in the insert shift register, the $\overline{\text{RSET INS}}$ signal goes from TC-5 to TC-14 to remove the insert shift register from the memory loop, restoring Quiescent Edit Operation.
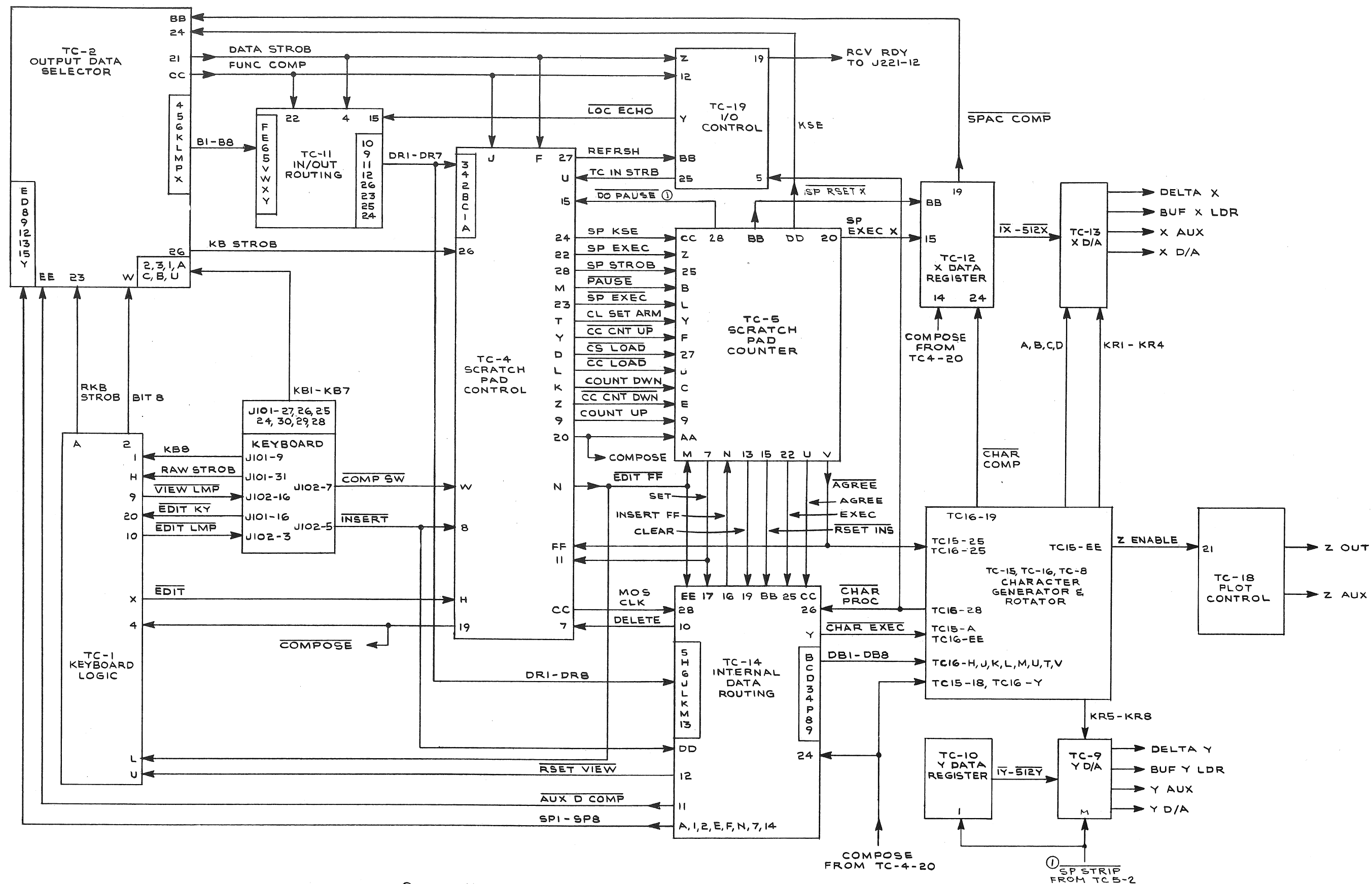
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① IF TERMINAL CONTAINS TC-5 BOARD NUMBERED 670-1438-00, THE DO PAUSE FUNCTION IS PERFORMED BY SP RSET X. THE SP STRIP FUNCTION IS PERFORMED BY COMPOSE INTO TC-10 AND BY COMPOSE INTO TC-9.

4002A DRAWER

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FIG 5-23
BLOCK DIAGRAM
REFRESHED SCRATCH PAD   1171 EKP

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SEND TIMING
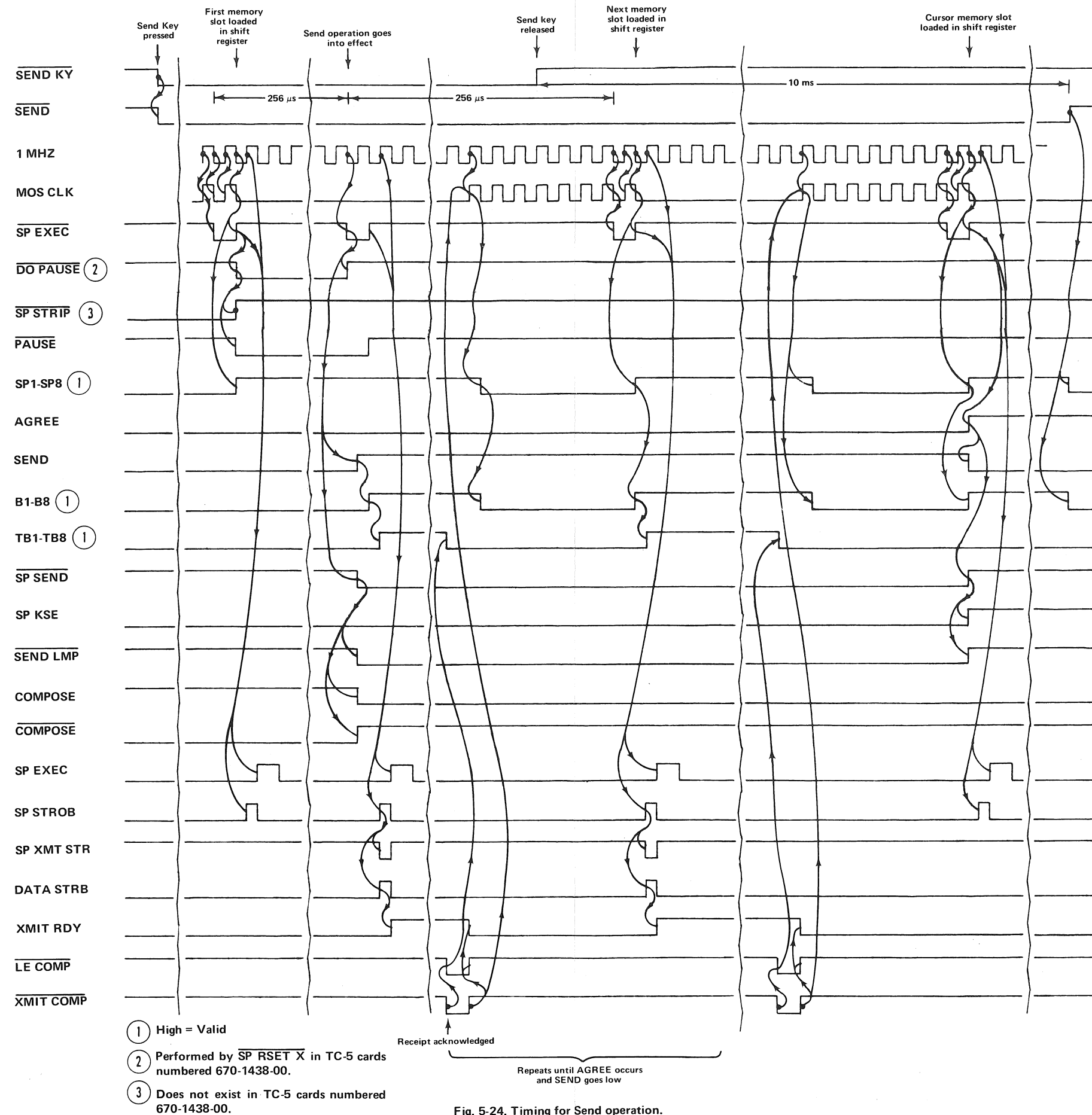
Fig. 5-24. Timing for Send operation.

Signal labels (left axis):
SEND KY
SEND
1 MHZ
MOS CLK
SP EXEC
DO PAUSE (2)
SP STRIP (3)
PAUSE
SP1-SP8 (1)
AGREE
SEND
B1-B8 (1)
TB1-TB8 (1)
SP SEND
SP KSE
SEND LMP
COMPOSE
COMPOSE
SP EXEC
SP STROB
SP XMT STR
DATA STRB
XMIT RDY
LE COMP
XMIT COMP

Annotations:
Send Key pressed
First memory slot loaded in shift register
Send operation goes into effect
Send key released
Next memory slot loaded in shift register
Cursor memory slot loaded in shift register

256 µs   256 µs   10 ms

Receipt acknowledged

Repeats until AGREE occurs and SEND goes low

(1) High = Valid

(2) Performed by SP RSET X in TC-5 cards numbered 670-1438-00.

(3) Does not exist in TC-5 cards numbered 670-1438-00.

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BLOCK DIAGRAM DESCRIPTION

Transmitting—On Line-Send; Echoing Not In Effect

General. Send can be initiated in Unrefreshed Mode, in Compose Mode (Send Operation), or in Edit Mode (Edit Send Operation). Send Operation causes the Scratch Pad memory contents from the first memory slot to the cursor position to be sent. Edit Send Operation sends the data between cursor memory position (the position occupied by the cursor when Edit Mode is selected) and the actual position of the cursor. The basic Send Operation is explained in detail, and the Edit Send Operation is explained as a variation of Send.

Send Operation. This is initiated by pressing the Send key while in Compose Mode. SEND KY then goes to TC-1. SEND goes from TC-1 to TC-, to TC-5, to the Interface Unit, and to the Display Unit. If in Unrefreshed Mode, SEND into TC-4 puts the Terminal into Compose Mode, putting a high on the REFRSH line. When the Scratch Pad memory first character slot is in the shift register in TC-14, TC-5 routes an SP SEND signal to TC-1, TC-4, the Interface Unit, and TC-19. TC-5 also provides a SEND signal to TC-2 and the Interface Unit. TC-1 routes a SEND LMP signal to the Keyboard to light the Send key. SP SEND into TC-4 ends the COMPOSE, COMPOSE, REFRSH, and MOS CLK signals, thus causing TC-14 to hold the first character on the SP1 through SP8 lines to TC-2. TC-2 uses the SEND signal to route the SP1 through SP8 bits to TC-11 as B1 through B8.

1 μs after TC-4 generates the SP EXEC pulse (which caused TC-5 to emit SP SEND), TC-4 sends an SP STROB to TC-5. TC-5 routes this to TC-2 as SP XMT STR. TC-2 then creates a DATA STRB signal for TC-11 and TC-19. This latches the B1 through B8 bits into TC-11, emitting them from there as TB1 through TB8. The DATA STRB into TC-19 causes XMIT RDY to go high.

When the computer accepts the data bits, the Interface Unit sends XMIT COMP to TC-2, TC-4, and TC-19. TC-19 ends the XMIT RDY signal and sends an LE COMP signal to TC-11 to clear the data latches. TC-2 responds to the XMIT COMP signal by routing a FUNC COMP (not shown) to TC-4, TC-11, and TC-19, although none of these have any effect in this mode. TC-4 uses the XMIT COMP signal to initiate another series of MOS CLK pulses to put the next character in the shift register in TC-14, again putting the bits on the SP1 through SP8 lines. These are followed by the usual SP EXEC and SP STROB signals from TC-4 to TC-5. SP EXEC increments the position counter. SP STROB causes a repeat of the transmission as previously described.

This continues until the cursor slot is in the TC-14 shift register, TC-5 then puts SP SEND high, SEND low, and inhibits future SP XMT STR signals, ending transmission. TC-5 also generates an AGREE signal for TC-4, which restores SP KSE to a high level. TC-5 then sends KSE to TC-2 and the Terminal reverts to Direct-On Line operation.

Edit Send Operation. If in Edit Mode when the Send button is pushed, operation is approximately the same as described for Send Operation. The exception is that the EDIT FF signal from TC-4 to TC-5 causes TC-5 to wait until the cursor memory position slot (slot indicative of the position occupied by the cursor when Edit Mode is selected) before the SP SEND and SEND signals are generated in TC-5. Then the EDIT FF signal ends. The EDIT light goes out and transmission occurs as in Send Operation.

Ⓐ
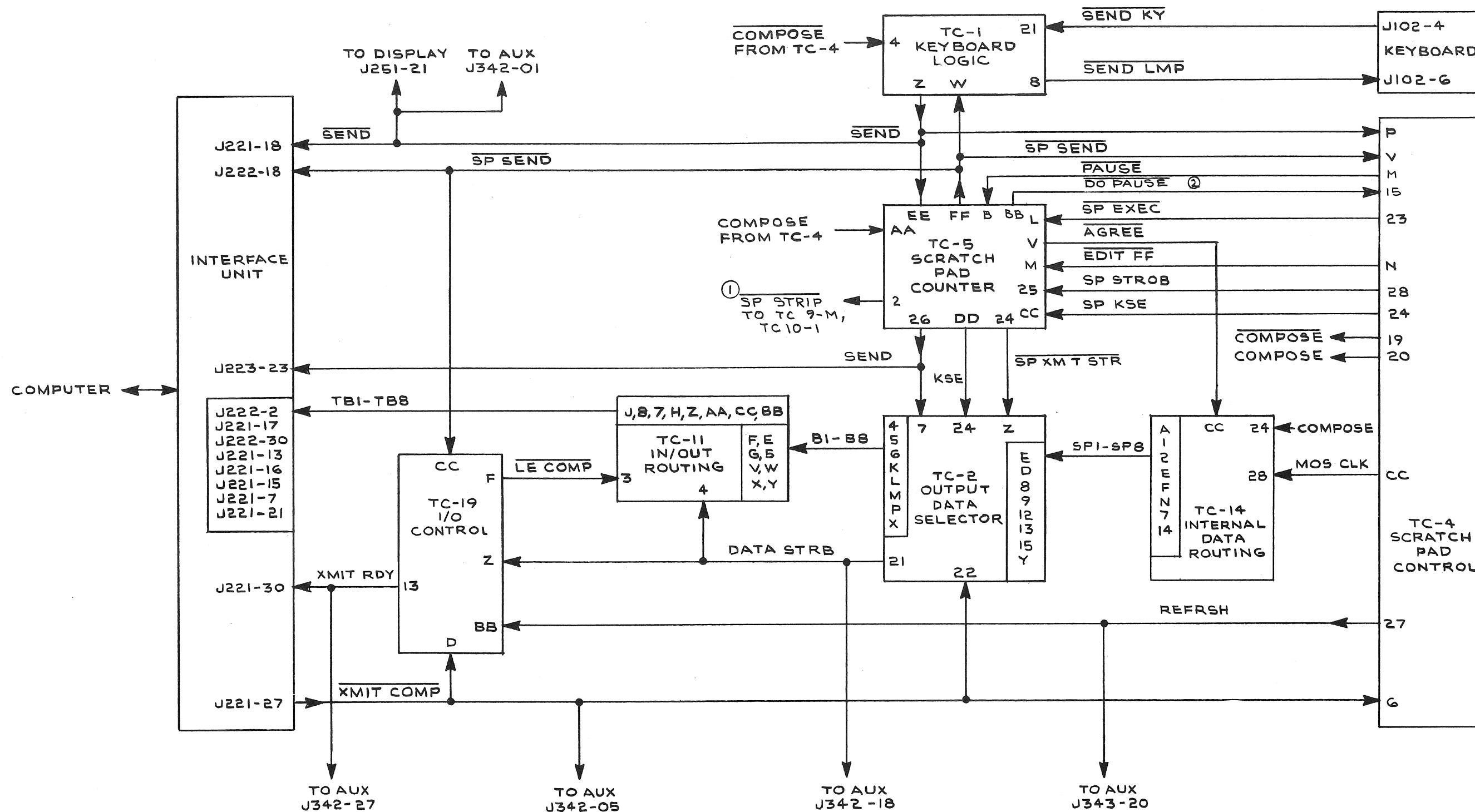
① SP STRIP DOES NOT EXIST IN TC-5 CARDS NUMBERED 670-1438-00.
ITS FUNCTION IS THEN PERFORMED BY COMPOSE IN TC-9 AND BY
COMPOSE IN TC-10

② DO PAUSE DOES NOT EXIST IN TC-5 CARDS NUMBERED 670-1438-00.
ITS FUNCTION IS THEN PERFORMED BY SP RSET X.

4002A DRAWER
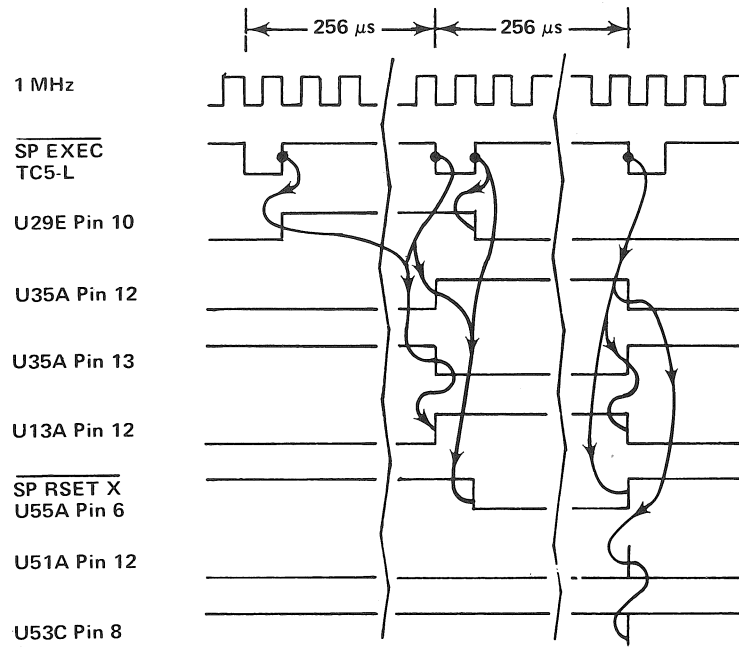
Ⓑ

FIG 5-25
BLOCK DIAGRAM
TRANSMITTING — ON LINE — SEND   1171 EKP

256 µs — 256 µs

1 MHz

$\overline{\text{SP EXEC}}$
TC5-L

U29E Pin 10

U35A Pin 12

U35A Pin 13

U13A Pin 12

$\overline{\text{SP RSET X}}$
U55A Pin 6

U51A Pin 12

U53C Pin 8

Fig. 5-42. $\overline{\text{SP RSET X}}$ circuit timing (TC-5).

Ⓐ

FIG 5-43 SCRATCH PAD COUNTER TC-5
CIRCUIT CARD #670-1438-01

4002A DRAWER

TC-5
670-1438-01

A4

1171   Page 5-47
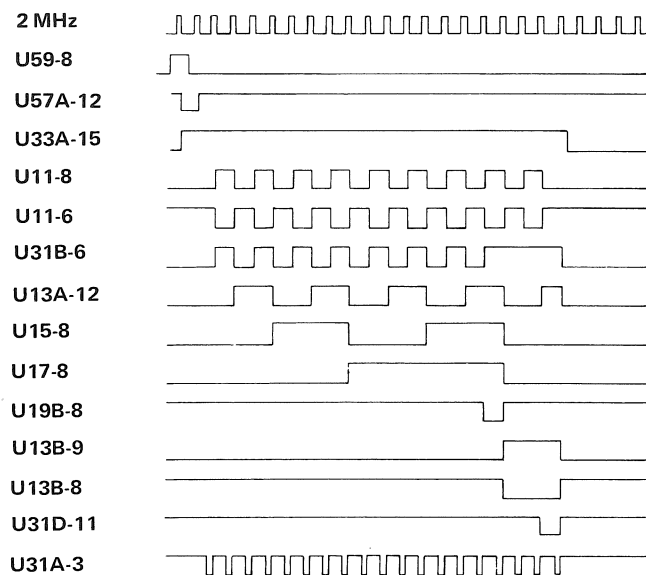
Fig. 5-50. Divide-by-19 counter timing diagram (TC-10).
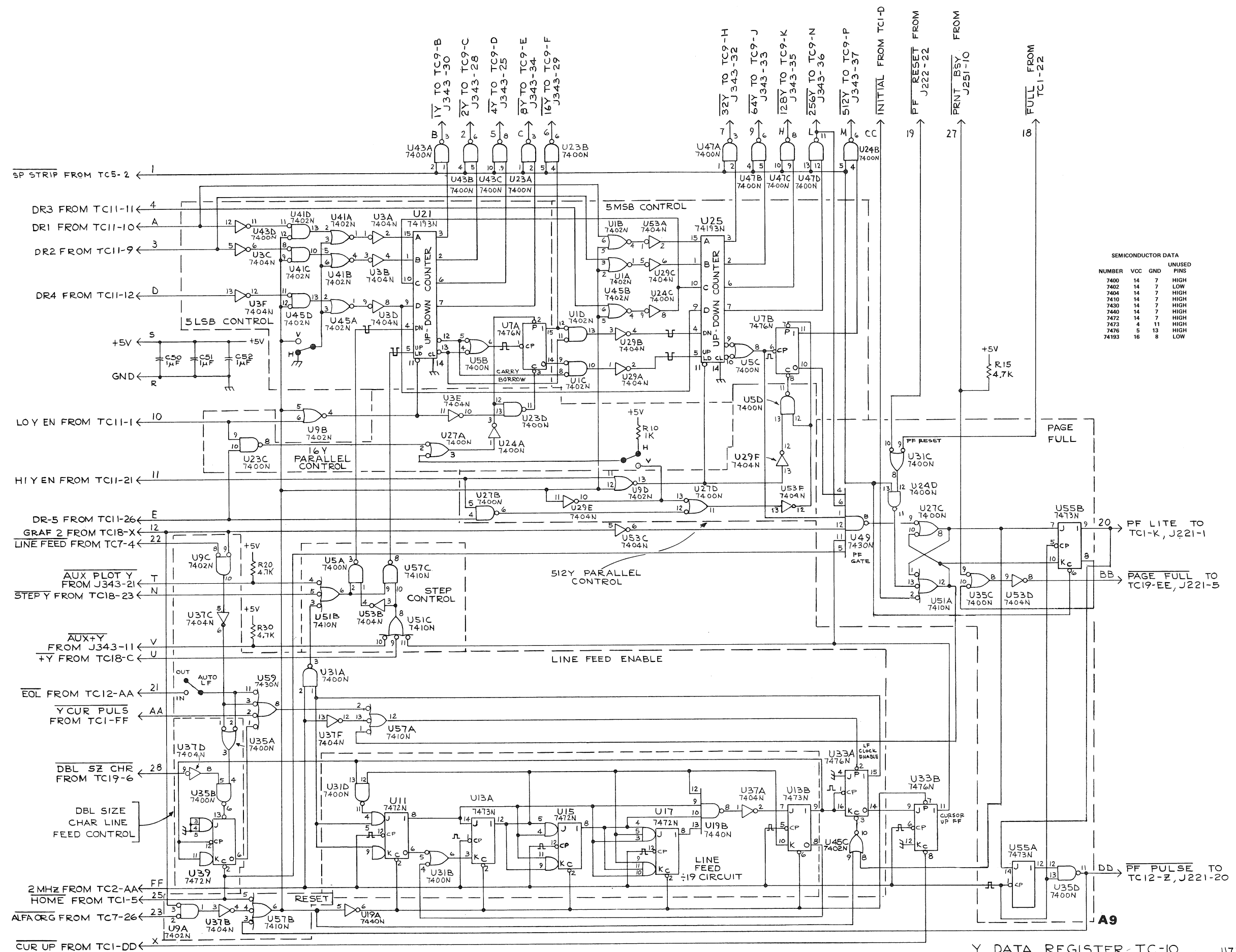
Y DATA REGISTER-TC-10

FIG. 5-51 CIRCUIT CARD # 670-1443-02

4002A DRAWER

Page 5-52

2 MHz

U11D Pin 13
(Starting Pulse)

U37C Pin 8

U17A Pin 15

U17A Pin 14

U15C Pin 8

U15D Pin 11

U13 Pin 8

U16B Pin 9

SPAC COMP
U16A Pin 13
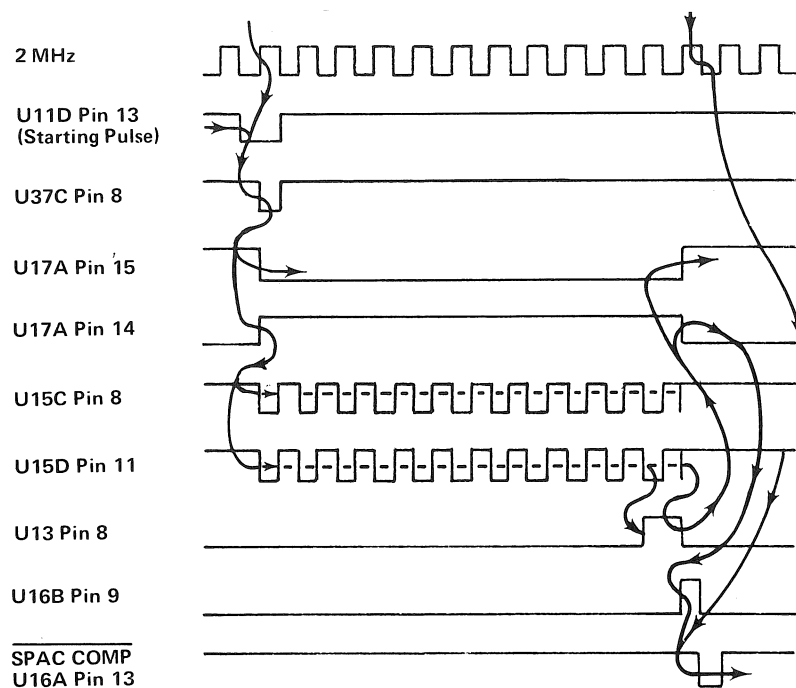
Fig. 5-53. Space circuit timing (TC-12).
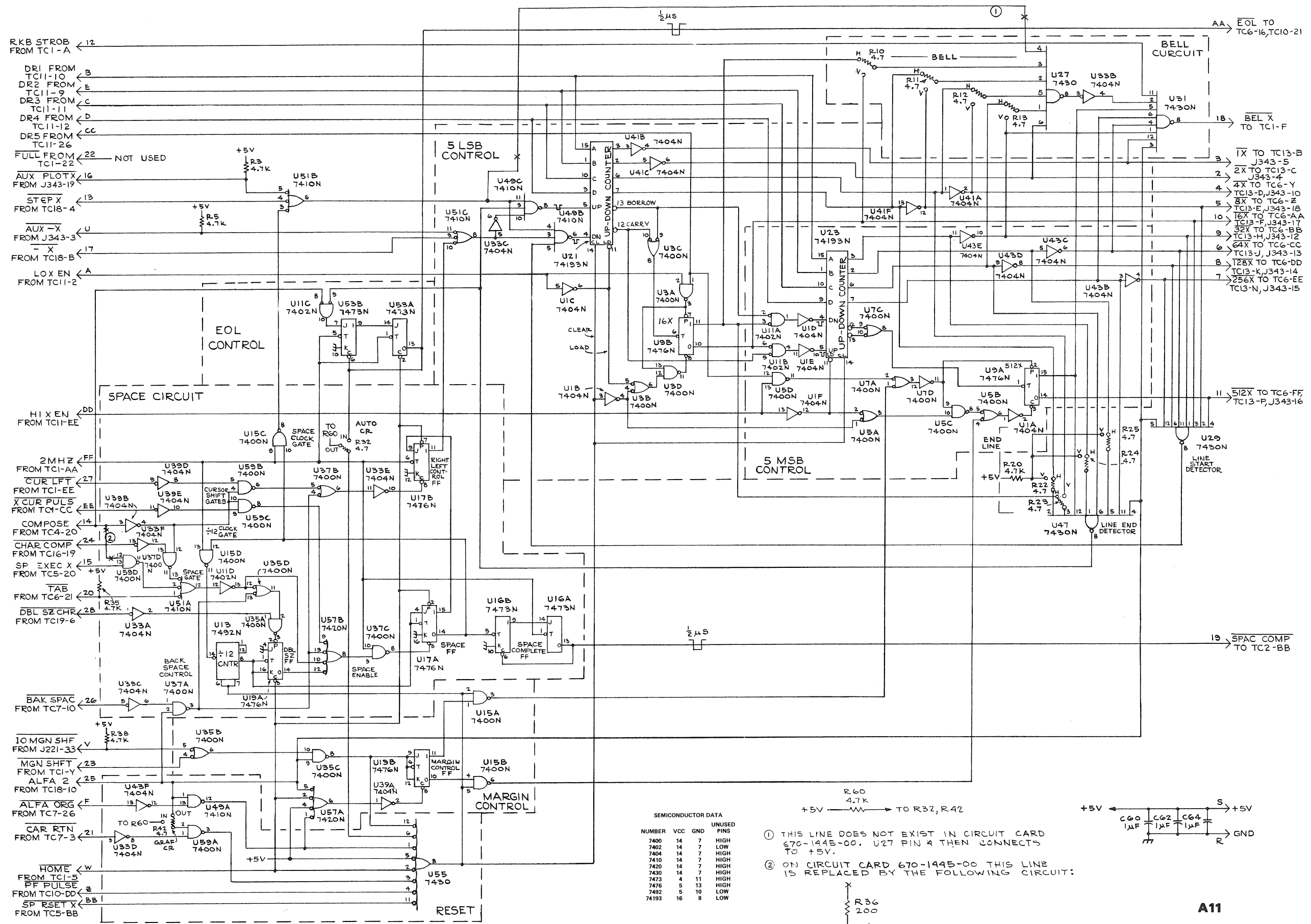
Ⓐ
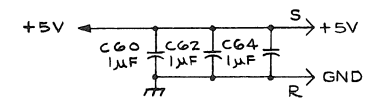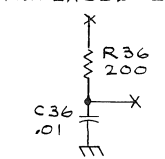
FIG. 5-54 X DATA REGISTER TC-12

4002A DRAWER UNIT AND KEYBOARD MAINTENANCE MANUAL

Modification Insert for M18,184   Effective SN B070630

Page 5-47 (Page 5-47A if M18,161 has been entered)

Change TC-5 Schematic as follows:
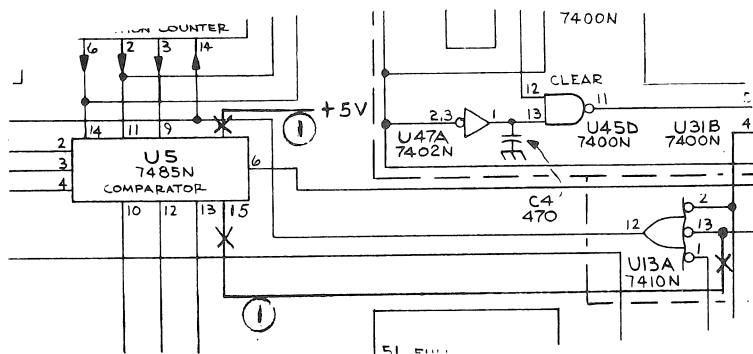
Add the following note to the schematic:

①These wires not contained on early circuit cards.

Modification entered in manual   _____.
                                           Date

Insert this instruction page in the back of the manual.

4002A DRAWER UNIT AND KEYBOARD MAINTENANCE MANUAL

MOD INSERT FOR M18,230 EFFECTIVE SN B070000-up

Change TC-1 (Part 2) Schematic, Page 5-44, as follows:

SECTION 5

At right-center change R73 and R79 from 51 Ω to 390 Ω.

SECTION 4

Change electrical parts list for TC-1 as follows:

CHANGE TO:

| R73 | 302-0391-00 | 390 Ω 1/2 W | 10% |
| R79 | 302-0391-00 | 390 Ω 1/2 W | 10% |

ASSEMBLY
   A1   670-1435-01   KEYBOARD LOGIC TC#1 Circuit Card

SECTION 6   Page 6-8

Change mechanical parts list for TC-1 as follows:

Fig. -15   670-1435-01   CIRCUIT CARD ASSEMBLY - KEYBOARD LOGIC A1

Modification entered in manual _____ .
                                            Date
Insert this instruction page in the back of the manual.

4002A DRAWER UNIT AND KEYBOARD MAINTENANCE MANUAL

MOD INSERT FOR M18,259   EFFECTIVE SN B090000-up

This modification provides initialization for the Shift Lock circuit.

CHANGE: Electrical Parts List as follows:

ASSEMBLY
  A1   670-1435-00   KEYBOARD LOGIC TC#1 Circuit Card

ADD:

  C7   290-0286-00   50 μF, Elect., 25V, -10% +75%

  CR1   152-0141-02   Silicon, replaceable by 1N4152

  R2   317-0103-00   10 kΩ, 1/8 W, 5%

  R10   317-0472-00   4.7 kΩ, 1/8 W, 5%

  R11   317-0103-00   10 kΩ, 1/8 W, 5%

SECTION 5:   Replace the keyboard schematic on page 5-41 with the enclosed
             page 5-41.

Modification entered in manual _____.
                                      Date

Insert this instruction page in the back of the manual.

4002A DRAWER   Ⓑ   FIG. 5-29 A19 KEYBOARD   1171
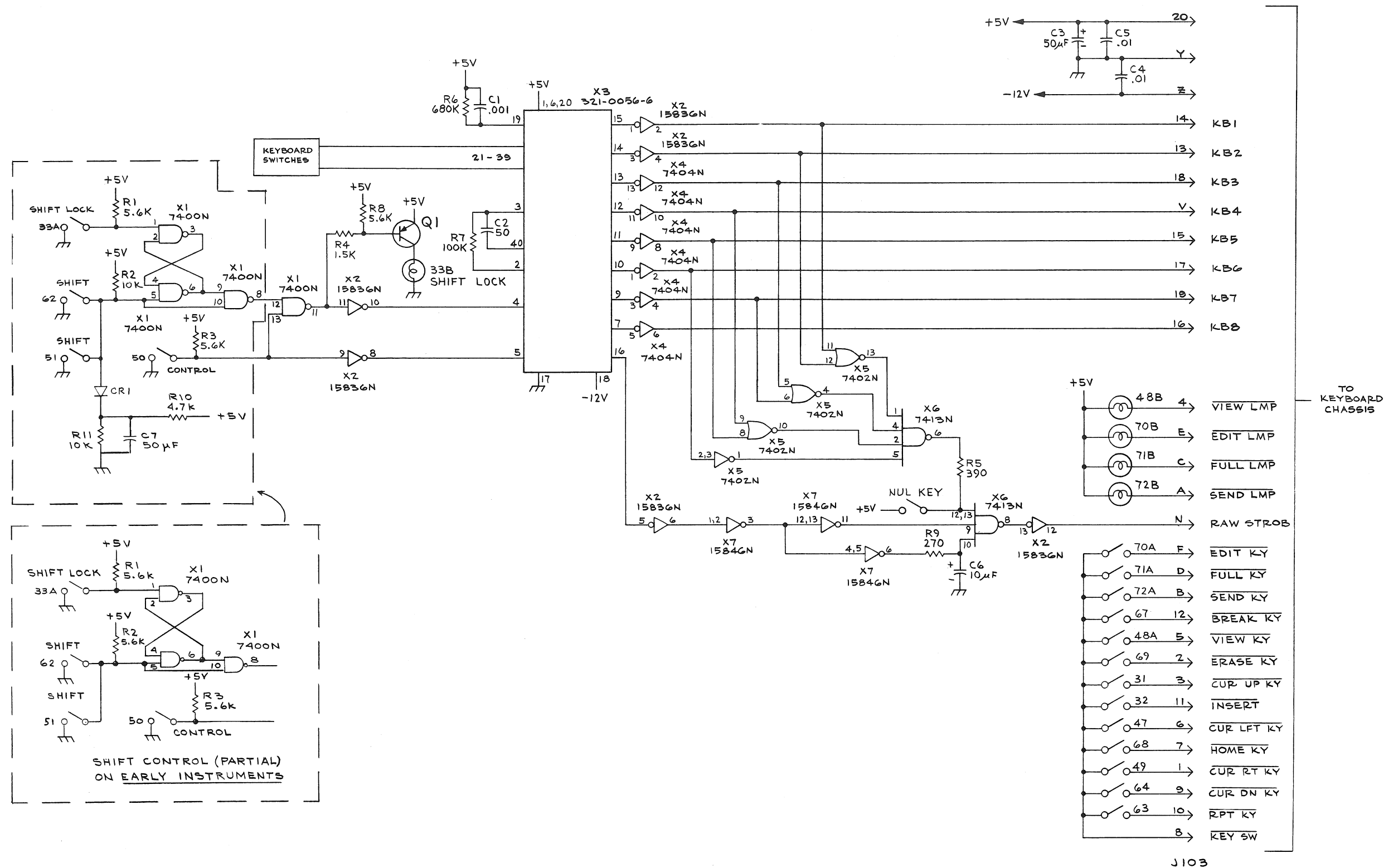
4002A DRAWER UNIT AND KEYBOARD MAINTENANCE MANUAL

MODIFICATION INSERT FOR M18,260   EFFECTIVE SN B080000-up

This modification provides initialization for the Scratch Pad Memory.

SECTION 2: Replace pages 2-19/2-20 with the enclosed pages 2-19/2-20.

SECTION 5: Page 5-56 - replace with the enclosed page 5-56.

Modification entered in manual _____.
                                      Date

Insert this instruction page in the back of the manual.

GDIV Control Circuit. Whenever linear interpolate is not in effect, the output from amplifier U3 is felt almost instantaneously through R71 at the positive input of U33. However, when linear interpolate is commanded, the first vector after linear interpolate is selected finds a GDIV signal coming in to turn Q13 on. This causes CR62 to be back biased, and permits Q29 to be turned on quite hard. This permits changes in U3 output voltage to appear directly on the positive input of U33. However, after the first vector has been written, GDIV goes low and GDLI goes high. With GDIV low, CR62 is conducting and the effect of the 15 V being applied to R62 holds Q29 cut off. However, the high GDLI signal turns Q57 on, back biasing CR67. Q59 turns on. Now, any changes in U5 output voltage must charge C69 through R71 and Q59 before the effect can be felt at the positive input of U33. This integration of U3 output signals permits relatively constant vector brightness.

Delta X Control Circuit. The DELTA X output is used on another card in conjunction with beam intensity during vector writing. Its purpose is to permit the Z axis to be turned on as a function of the X or Y vector length, depending upon which is longer. When changes in X Register outputs occur, the U33 output is applied to integrating amplifier U37. The current necessary to charge C52 causes an output voltage proportional to the change of input signal. VR52 and VR53 limit DELTA X output signals to approximately 12 V.

Internal Data Routing TC-14

TC-14 is the Internal Data Routing circuit card for the Terminal. Several functions are performed on this card. One of them is the routing of data directly to the Character Generator in Alphamuneric Mode; another is the routing of data to the Scratch Pad Memory circuit, and the subsequent release of this data from the memory circuit to the Character Generator. In addition, the Internal Data Routing card contains the circuitry for insertion and deletion of data in the Scratch Pad Memory circuit. An Execute circuit is also contained on this card.

The circuitry will be discussed in the following order: Data Select Gates, Execute Circuit, Scratch Pad Memory, Scratch Pad Input/Output, Scratch Pad Delete Circuit, Delete Comp Circuit, Scratch Pad Insert Circuit.

Data Select Gates. When in Direct Mode, the COMPOSE line is low, causing the Data Select Gates to route DR1 through DR8 data directly through this card and out on the DB1 through DB8 lines. When Compose Mode is selected, the DR1 through DR8 bits are blocked from the Data Select Gates; outputs are then taken from scratch pad shift registers U1 and U5. The output lines are sampled by a series of inverters which detect NUL signals. Whenever a character is in process, detected NUL signals and inverted CHAR PROC signals combine in U35B to produce a low NUL DET signal.

Execute Circuit. When in Direct Mode, U35A is inhibited by a low at its pin 1 input. It therefore presents a constant high output, disabling U51A and providing U55B with an enabling voltage. If the TC INHIB line is high and no delete character is present, U55B is permitted to respond to the pin 9 input. If in Alphanumeric Mode and no character is in process, U55A produces a low output in response to an EXEC signal input. If an AUX PLOT condition does not exist, U51C responds to the U55A output, causing U55B to develop a CHAR EXEC signal.

When in Compose Mode, U35A pin 1 goes high. At any time a control character is received into the circuit, it is detected by control character Detector U51B and causes the U35A output to go low. This disables U55B and provides U51A with an enabling voltage. Subsequent EXEC pulses then cause CF EXEC signals to be generated, rather than CHAR EXEC signals.

Scratch Pad Memory Circuit. This consists of two 4000 bit memory devices and a negative 6 volt power supply circuit. Data bits are applied to pin 1 of U37 and are clocked into the device by the MOS CLK signal. Each MOS CLK signal advances the data one position through the memory circuits while clocking in the next data bit. Data moves out of U37 pin 8 and is accepted in U57 on pin 1. The output from U57 pin 8 is applied to U9E for processing by the Scratch Pad Input/Output circuit. An initializing circuit is included on later versions of the circuit card. At turn-on, INITIAL goes low and permits 1 MHz clock pulses to cycle the Memory Circuit. Since INITIAL is also applied to U17C, the memory circuit becomes completely loaded with high bits. Data in the Memory Circuit is the inverse of true data, and its contents thus represent a succession of NUL characters.

Scratch Pad Input/Output Circuit. Assume that Compose Mode exists and a character is to be entered into the Scratch Pad circuit. The data bits appear on the DR1 through DR8 lines, and are applied to the parallel inputs of U1 and U5. Compose Clear gate U13A and Compose Set gate U13C each have two high inputs. A CLEAR signal is received from TC-5 and causes U13A to produce a low output, clearing the U1 and U5 Shift registers. One-half microsecond later a SET signal is received from TC-5 and causes U13C to generate a low output. This applies a high to the preset inputs of U1 and U5. This preset signal permits the content of the parallel input lines to appear at the output lines of U1 and U5. The least significant data bit appears at U1 pin 15, while the most significant data bit appears at pin 13 of U5. This signal at pin 13 of U5 is applied to the Compose Serial Output Gate U31D. The signal at pin 13 of U31D remains high under all except for delete conditions. Therefore, the U31D output is an inverted representation of the bit data at U5 pin 13. U13B and U17C cause the U31D output to be applied to the serial input of U37 in the Scratch Pad Memory circuit. After the data has been loaded into the Scratch Pad Shift Registers, a series of 8 MOS CLK pulse is received by the

circuit. These cause the data bits in U1 and U5 to be sequentially clocked out on pin 13 of U5, with the most significant bit leaving first and the least significant bit leaving last. These data bits are applied to the input of U37 and are sequentially accepted by the memory circuit.

Now assume that the Scratch Pad Memory has data in it and that a character bit 8 is present at U57 pin 8. The effect of this data bit is felt through U9E, U11C, and U29D, making it present at the pin 9 input of U1. The next MOS CLK pulse to arrive causes this bit to be clocked through U1 and appear at the pin 15 output. The MOS CLK pulse also causes the Scratch Pad Memory to make the next data bit (in this case bit 7) available at the U57 pin 8 output. The following MOS CLK pulse will then clock bit 7 in through pin 9 of U1, at the same time advancing the pin 15 output data to pin 14. Bit 7 now appears on pin 15 of U1 and pin 8 appears on pin 14. After six more clock pulses, bit 8 has advanced to pin 13 of U5 and bit 1 appears on pin 15 of U1. The Shift Register has now been loaded with the next character. The bits are felt through the Data Select Gates and appear on the DB1 through DB8 lines. The Scratch Pad Shift Register outputs are also available to the output data selector circuit on TC-2 via the SP1 through SP8 lines. This permits the Scratch Pad to transmit data to the computer in On Line-Send Mode or to the screen in Local Send Mode.

Scratch Pad Delete Circuit. If a character is to be deleted from the Scratch Pad Memory, the Scratch Pad Cursor is placed above this character. Edit Mode is selected and the delete key is pressed. The EDIT FF signal and the output of Delete Detector U45 causes U15D to produce a high output. When the Scratch Pad Shift Register contains the character over which the cursor is placed, an AGREE signal is developed by TC-5. This is applied to U17D, causing it to generate a low output. This one-sets the delete flip-flop U33A. The pin 13 output of U33A disables the Compose Serial Output Gate U31D. It is also applied to U31A to send a disabling voltage to the Compose Serial Gate U11A. The high from the pin 12 output of U33A is applied to the Delete Mode Shunt U31C.

Note the condition that exists. With Compose Serial Output Gate U31D disabled, serial data from U5 is prevented from going to the input of the Scratch Pad Memory circuit. Serial output data from the Scratch Pad Memory circuit is prevented from reaching the serial input of U1 because Compose Serial Input Gate U11A is disabled. With the Delete Mode Shunt Gate U31C enabled, the output from pin 8 of U57 loops through U9E, U31C, U13B, and U17C directly back to the input of the memory circuit. Under this condition, the data to be deleted is contained in the Scratch Pad Shift Register and is isolated from the Scratch Pad Memory circuit. When the next set of eight MOS CLK pulses is received, the data being clocked out of U57 is clocked directly back into U37. The data

which is contained in the Scratch Pad Shift Registers is clocked out of pin 13 of U5, but is not received by any circuit and therefore disappears from the Scratch Pad Memory.

At the same time that the character bits are being clocked out of U1 and U5, zeros are being clocked in at U1 pin 9. After the last character in memory has been clocked out of U57 and back into U37, a RSET INS signal is received. U35C and U31B cause delete flip-flop U33A to zero-set. The circuit then returns to normal operation. Note that the character has been removed and that no gap exists in its previous position. Also note that all data in the Scratch Pad Memory which follows the deletion point has been moved one position to the left as viewed on the Scratch Pad display.

Delete Complete Circuit. When the delete signal is received and detected by U45, it disables U55A in the execute circuit and prevents CHAR EXEC or CF EXEC signals from being generated. The Delete Detector output is also inverted by U47F and applied to the J input of U19A. The EXEC signal which accompanies the delete character causes U19A to become one-set. The negative transition of a subsequent 1 MHz clock pulse causes U19B to become one-set, applying a high to U17B. When the 1 MHz signal again goes positive, U17B develops a low output to cause an AUX D COMP signal to leave the circuit. In addition, the output from U17B is fed back to U19A to zero-set that device. This removes the high from J input of U19B. When the 1 MHz again goes low, U19B zero-sets and disables U17B.

Scratch Pad Insert Circuit. When a character is to be inserted, the Insert Shift Registers are brought into use to permit inserting the new character at the desired point in the string of characters in memory. To insert the character, an EDIT FF signal is applied to the circuit. When the Insert button is pushed, the INSERT signal arrives. This causes U15C to generate a high output. When the character over which the cursor appears is present in the Scratch Pad Shift Register, an AGREE signal is received from TC-5. This causes U35D to generate a low output, causing insert flip-flop U33B to become one-set. This causes several things to happen. The low output from pin 8 of U33B is applied through U31A to place an enabling voltage on U11B. U31A also places a high on U9D to send a low to disable the Compose Serial Input Gate U11C. The low from pin 8 of U33B also disables the Compose Set and Compose Clear gates U13C and U13A. At the same time, the high from U33B pin 9 is applied to the Insert Serial Gate U11A to enable it. The high from U33B pin 9 is also sent to U29A and U29B to enable those two devices.

When the character to be inserted is entered at the keyboard, the data bits appear on the DR1 through DR8

Ⓐ
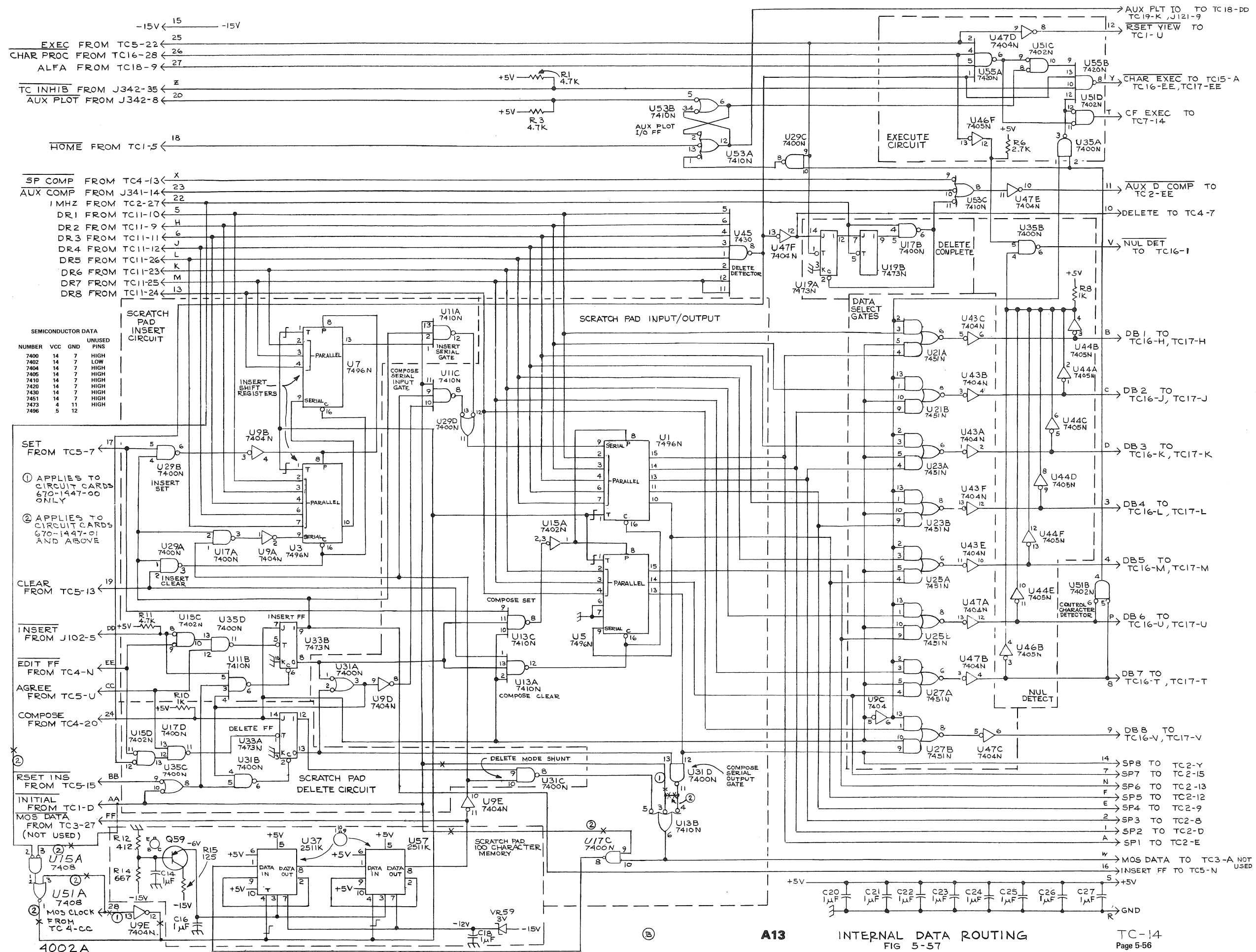
INTERNAL DATA ROUTING
FIG 5-57

MOD INSERT FOR M18,274

This modification improves graphic operation.

SECTION 2:   Replace pages 2-14A through 2-16 with the enclosed pages 2-14A
                through 2-16

SECTION 4:   Change the Electrical Parts List as follows:

Page 4-17

ASSEMBLY
  A10   670-1444-00 B010100 - B079999 IN/OUT DATA ROUTING TC#11 Circuit Card
              670-1444-01 B080000 - B089999
              670-1444-02 B090000 - B089999

ADD:

  C21   283-0000-00 XB080000 - B089999   0.001 µF, Cer, 500 V, +100%-0%

  R20   317-0202-00 XB080000 - B089999   2 kΩ, 1/8 W, 5%

  R21   315-0102-00 XB080000 - B089999   1 kΩ, 1/8 W, 5%

  U17   156-0039-00 XB090000   Dual J-K flip-flop, replaceable by T.I.
                                                 SN7473N

SECTION 5:   Page 5-28 - Write "SUPERCEDED - SEE PAGE 5-28A" across Fig. 5-13.
             Insert the enclosed page 5-28A between page 5-28 and 5-29.
             Remove page 5-29/5-30 and replace it with the enclosed page 5-29/5-30.

             Page 5-53 - Change the figure number and title to:
             "FIG. 5-52B. IN/OUT DATA ROUTING.
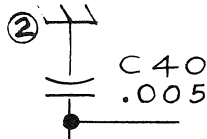   TC-11 CIRCUIT CARD #670-1444-00."
             Change the page number to 5-53B
             Change the Tab to "TC-11 670-1444-00"
             Insert the enclosed page 5-53/5-53A between page 5-52 and 5-53B.

             Page 5-61, Fig. 5-65. Near the bottom left of the schematic, change
                       the C40 circuit as shown below:

             Add the following note to the schematic:

             ② Changed from +5 V to ground connection by M18,274.
             Circuit card then changed from 670-1451-00 to 670-1451-01.

SECTION 6:   Change the Mechanical Parts List as follows:

Page 6-9

    Fig.   -33   670-1444-0Q   B010100 - B079999   CIRCUIT CARD ASSEMBLY-IN/OUT DATA
                                                                     ROUTING A10

                670-1444-01   B080000 - B089999

    Fig.   -33   670-1444-02   B090000   CIRCUIT CARD ASSEMBLY-IN/OUT DATA
                                                                        ROUTING A10

Modification entered in manual   _____.
                                          Date

Insert this instruction page in the back of the manual.

The output latches accept B1 through B8 data from the keyboard, scratch pad, or auxiliary inputs. Upon receipt of a DATA STRB, the data is latched through, making it available on the interface output lines TB1 through TB8. If LOCAL ECHO exists or if ON LINE is low, U27C sends a high to U3B and the Local Control gates U23C through U37C. When a DATA STRB occurs, U3B sends a DROP FLG signal to the interface to prevent data from going to the computer. At the same time, the high on gates U23C through U37C AND with data from the output latches to make the data bits available on the DR1 through DR8 lines. The output latches are cleared upon completion of character processing. For example, if On Line condition exists and data is being transmitted through the interface to the computer, it is followed by an LE COMP. This is applied to U5C in the Output Latch Clear circuit, is processed through U27D, U27B, and U45A to clear both Output Latches. If LOCAL Mode exists, ON LINE is low and completion signals are routed through U3A to do the clearing.

Input Latch Circuit. When data is received from the computer and interface, it appears on the RB1 through RB8 lines and is accompanied by RCV STROB. The strobe latches the data bits into U47 and U51, making them available at the output of the latches. From there these bits are routed through inverters and OR gates and are made available to the Terminal circuits on the DR1 through DR8 lines.

Graphic Word Assembler. The purpose of this circuit is to accept bytes of input information during Graphics Mode and route these bytes to the appropriate data registers in five-bit bytes. The sequence in which these bytes is routed is determined by straps R7, R13, and R5. Standard factory connection for these straps requires that bytes be supplied to the Terminal in the following sequence: high Y, low Y, high X, and low X. This discussion will assume that these straps are as shown on the schematics and the given sequence is being presented.

When Linear Interpolate or Point Plot Mode is selected, GS+FS goes low, causing the Graf FF to change states. U3C provides a low to U29C. The accompanying high from U27A serves several purposes—it provides enabling voltage to Byte Decoder U7, and enabling voltage to NAND gate U13A. It also removes the low which had been holding Hi byte flip-flop U11 zero-set. When graphic bytes are clocked into the TC-11 circuitry, the bit 7 and bit 6 configuration is determined by the byte being received. For example, high X byte has bit 7 low and bit 6 high; the low X byte has them high, low; the high Y byte has them low, high; and the low Y byte has them high, high. Upon receipt, these bits are applied to byte decoder U7 along with SYNC STRB, which is applied through U5F. The leading edge of the SYNC STRB clocks bit 7 and 6 through U7, placing a low on either the 4, 6, 5, or 7 output lines. If the high X byte is being received, it causes U7 pin 6 to go low, placing

enabling voltages on U29B and A. The high on Pin 4 of U7 holds the LOW Y EN line low and maintains a disabling voltage on the J input of HI BYTE FF U11. Pin 5 of U7 is also high, putting a low disabling voltage on the K input of U11, and on the LO X EN line. In addition, it places a low on U13A, disabling that gate. The high from pin 7 of U7 places a low on U29C to AND with the low from the GRAF flip-flop. The high output from U29C causes a low GWA output command, indicating that the Graphic Word Assembler is being employed.

Go back to Hi Byte flip-flop U11. Prior to the time that the GRAF flip-flop had been put into Graphics Mode, a low from U27A had held U11 zero-set. The low from U11 pin 8 held a low on U29B. When the high Y byte is decoded by U7, the low from pin 6 ANDs with the low from U11 pin 8, causing a HI Y EN pulse from U29B. The HI Y EN also goes through U33D to cause a high out of U13C, placing an enabling voltage on U15A. U15A is negative-edge conscious and when the SYNC STRB input ends, it causes the high at the J input of U15A to clock through and apply a high to the J input of U15B. The next 1 MHz clock pulse finds its negative transition one-setting U15B, causing the GWA COMP signal to go low. This GWA COMP signal is fed back through U13D and U13B to zero-set U15A, causing the U15B J input to go low. The next 1 MHz clock pulse has its negative edge zero-setting U15B, causing GWA COMP to end. This signal is an indication to the Interface Unit that the Graphic Word Assembler has loaded the byte into the appropriate register.

The next byte to arrive is a low Y byte and it contains a high bit 7 and a high bit 6. With pins 3 and 13 of byte decoder U7 high, its pin 4 output goes low when the SYNC STRB pulse arrives. This places a high on the LO Y EN line, at the same time holding lows on the HI Y EN, HI X EN, and LO X EN lines. The high on the LO Y EN line is applied to the J input of U11 and is also applied through U33A and U13C to the J input of U15A. When the SYNC STRB ends, U11 and U15A both become one-set. U11's change of state is a preparatory step towards having the next high byte enabling the HI X EN line. When U15A changed state, it caused a high to be applied to U15B, so that the GWA COMP pulse can be generated by the next 1 MHz pulse just as it did when the high Y byte was loaded.

When the GWA COMP pulse ends and the interface supplies the TC-11 with the high X byte, it is accompanied by a low bit 7 and a high bit 6. This causes a low on pin 6 of U7, providing enabling voltage to U29B and U29A. Since U11 is one-set, U29A now has two lows and generates a HI X EN output pulse. Incidentally, this pulse is of the same width as the Sync Strobe that caused it. This HI X EN pulse passes through U33A, U13C and is applied to the J input of U15A. The end of the SYNC STRB clocks U15A and causes U15B to generate another GWA COMP pulse as before. When the fourth byte (low X) is applied to the

TC-11 circuitry, it has a high bit 7 and a low bit 6. This causes a low on pin 5 of U7 when SYNC STRB occurs. This puts a high on the K input of U11, a high on the LO X EN line, and a high into U13A. The high into U13A ANDs with the high from U27A and causes a low into U31 to generate a low $\overline{\text{STROB DLY}}$ output pulse, which permits the point to be written. When SYNC STRB ends, LO X EN also ends, zero-setting U11. This permits receipt of the high Y byte of the next point to be written. Note that the fourth byte does not enable the GWA Comp flip-flops and no $\overline{\text{GWA}}$ $\overline{\text{COMP}}$ signal is generated. On TC-11 circuit cards 670-1444-01 and above, the end of the fourth pulse (at U13A pin 2) is felt through a network which causes U29D to clear the data latches.

One other item. It should be noted that throughout the loading of these four bytes, pin 7 of U7, the byte decoder, remained high to maintain a low into U29C. Since $\overline{\text{GS+FS}}$ remains low while in Linear Interpolate or Point Plot, U3C also provided a low into U29C. The high output from U29C was inverted by U53F and maintained a $\overline{\text{GWA}}$ signal to indicate that the Graphic Word Assembler is in its active state. If a control character is received, the bits strobed through U7 cause pin 7 to go low, putting a high on U29C. This causes $\overline{\text{GWA}}$ to go high, permitting the control character to be processed.

X Data Register TC-12

TC-12 is the X Data Register for the Terminal. Its purpose is to control the Terminal's horizontal address. The principal parts of TC-12 are the 5 LSB Control circuit, the 5 MSB Control circuit, the Reset circuit, Bell circuit, Line Start Detector, Line End Detector, EOL Control, Margin Control, and Space Control circuit. These circuits will be discussed in that order.

5 LSB Control. This circuit controls and stores the five least significant bits of the 10-bit X register. Bits $\overline{\text{1X}}$, $\overline{\text{2X}}$, $\overline{\text{4X}}$ and $\overline{\text{8X}}$ are controlled by Up-Down Counter U21; bit $\overline{\text{16X}}$ is controlled by flip-flop U9B. These devices can be controlled in either serial or parallel fashion. In addition, they can be cleared to zero upon command. Clearing the registers is accomplished by placing a high signal on the pin 14 Clear input of U21 and simultaneously applying a low to pin 8 (Clear input) of U9B. This clearing signal is received from U55 in the Reset circuit.

Serial control of the circuit is accomplished by applying a pulse to either the Up or Down input of the Counter circuit. Under normal left to right operation, count up gate U49C is enabled and pulses are applied to the Up input of the counter. These pulses can be the result of $\overline{\text{AUX PLOT X}}$ or $\overline{\text{STEP X}}$ input signals, or of the clock signal from U15C in the Space circuit. Each time a pulse is received, the Up-Down Counter increments its digital output by 1. For example, pin 3 represents bit 1 and pin 2 represents bit 2. When the counter is cleared, both of these outputs are low. After the first pulse arrives, pin 3 goes high. The second

pulse causes pin 3 to go low and pin 2 to go high. After 15 pulses have been received, pins 3, 2, 6, and 7 are all high. The next pulse causes them to go low and causes a low pulse to appear on pin 12, the Carry line. This low causes U3C to apply a high pulse to U9B, the 16X flip-flop. This flip-flop had initially been zero-set by the action of the U55 Clear pulse through U1B, U3B, and U3D. When this Carry pulse ends, U9B becomes one-set and applies a low on the $\overline{\text{16X}}$ line.

It should be noted that the 5 MSB Control circuit operates essentially the same as the 5 LSB Control circuit, differing only in its manner of receipt of input pulses. Notice that the zero output of U9B is applied through U11B and U1E to the Up pulse input of U23. Initially, U9B was in its one-set condition and its zero output held U11B disabled. Therefore, when the first Carry pulse from the U21 Up-Down Counter arrives at U11B, it is prevented from affecting the output of that device. However, after U9B has received its first Carry pulse, it becomes one-set. A low is applied from the U9B zero output to U11B, providing that device with an enabling voltage. The next time a carry pulse is received from U21, it causes U11B to develop a high output, which applies a low pulse to pin 5 of the Up-Down Counter. This causes that device to increment by one count. The trailing edge of the pulse which causes this incrementing, causes 16X flip-flop U9B to again become zero-set, removing the enabling voltage from U11B.

Decrementing or down-counting is accomplished in much the same manner. Whenever U51C in the 5 LSB Control circuit is receiving a low input, it provides a high to U33C and U49B. U33C disables U49C, preventing the count up input from receiving any further signals. The stepping commands from U51B are then applied to pin 4 of U49B, causing a low output to be applied to the count down input of Up-Down Counter U21.

Assume that the pin 3, 2, 6, and 7 outputs of the Up-down Counter all contain lows at the time that a count down pulse is received. The 3, 2, 6, and 7 outputs of the Up-Down Counter go high and a low pulse appears on pin 13, the Borrow output. Assume also that the 16X flip-flop U9B has been zero-set prior to the arrival of that count down pulse. Pin 11 of U9B is low, providing U11A with an enabling voltage. When the low borrow pulse arrives at U11A, it causes a high output from U11A, applying a low to the count down input of Up-Down Counter U23. This counter then decrements by 1. The Borrow pulse that causes the U23 Up-Down Counter to decrement is also applied to 16X flip-flop U9B, causing it to become one-set. This applies a disabling voltage to U11A. The next Borrow pulse to be sent from U21 is prevented from passing through U11A but causes U9B to again change states. Essentially, U21 is then borrowing 1 from U9B, the 16X flip-flop.

Parallel control of the register is accomplished simply by applying data bit information on the DR1 through DR5

lines, making it available to both the 5 LSB and the 5 MSB Control circuits. The data is not accepted by the registers until such time as an enabling pulse is applied to the devices. When the 5 LSB Control circuit is to be controlled in parallel fashion, the data bit information is accompanied by a LO X EN input pulse. This is applied through U1C to pin 11, the load input of U21. Whenever this input goes low, the bit information at inputs A, B, C, and D is made available at output pins 3, 2, 6, and 7, supplying the four least significant X bits. The fifth input bit is applied to U3A. If it is high, the LO X EN pulse causes U3A to develop a low output to one-set U9B. At the same time, the low output from U3A disables U3D. However, if the bit 5 input is low, it disables U3A. The LO X EN pulse is then routed through U1C to apply a low to U3B, putting a high on U3D. U3D develops a low output, zero-setting 16X flip-flop U9B. The 5 MSB circuit is parallel loaded in the same fashion, except that a signal must be present on the HI X EN line to cause loading.

Reset Circuit. The Reset circuit causes the register to be set to left or center margin position, depending upon the selection made by the margin control circuit. This resetting is done is response to such signals as $\overline{\text{HOME}}$, $\overline{\text{PF PULSE}}$, $\overline{\text{SP RSET X}}$, $\overline{\text{CAR RTN}}$, $\overline{\text{ALFA ORG}}$, $\overline{\text{IO MGN SHF}}$, and $\overline{\text{MGN SHFT}}$. In addition, strap option AUTO CR permits resetting to occur each time that an END of Line condition is reached. The 5 LSB register and four bits of the 5 MSB register are reset to zero, regardless of the condition of the Margin Control. However, 512X bit flip-flop U9A is set to either of two states upon Reset, depending upon whether U15A or U15B is enabled. If the Left Margin has been selected, Margin Control flip-flop U19B is zero-set, putting an enabling voltage on U15B. When a high pulse is emitted by U55, U15B sends a low pulse to U5B, causing the 512X flip-flop to become one-set. This stores a register address of zero, the left edge of the screen.

If the Margin Control flip-flop had been one-set due to a $\overline{\text{MGN SHFT}}$ command, U15A would be enabled and U15B would be disabled. Reset pulses from U55 would then pass through U15A, applying a low to U7A; this would place a low on the Preset input of 512X flip-flop U9A, causing its zero output to go low, commanding the register to the 512X position. This places the CRT beam at mid-screen.

Bell Circuit. The Bell circuit generates a $\overline{\text{BEL X}}$ signal which causes the Terminal's bell to ring as the register approaches the end of the horizontal line. If the selector straps are set for a horizontal display format, this $\overline{\text{BEL X}}$ signal is generated when the register is in the 78th character writing position and an RKB STROB pulse is received. If the straps are in the vertical position, the $\overline{\text{BEL X}}$ command is generated when the register is in the 67th character position and an $\overline{\text{RKB STROB}}$ signal is received.

Line Start Detector. This circuit consists of NAND gate U29, whose output is used to prevent application of countdown pulses to Up-Down Counter U21 whenever the register is in the first character position while in Alpha-numeric Mode. At this time all highs are applied to U29, causing it to send a low to U49B, preventing countdown pulses from passing through that device to U21.
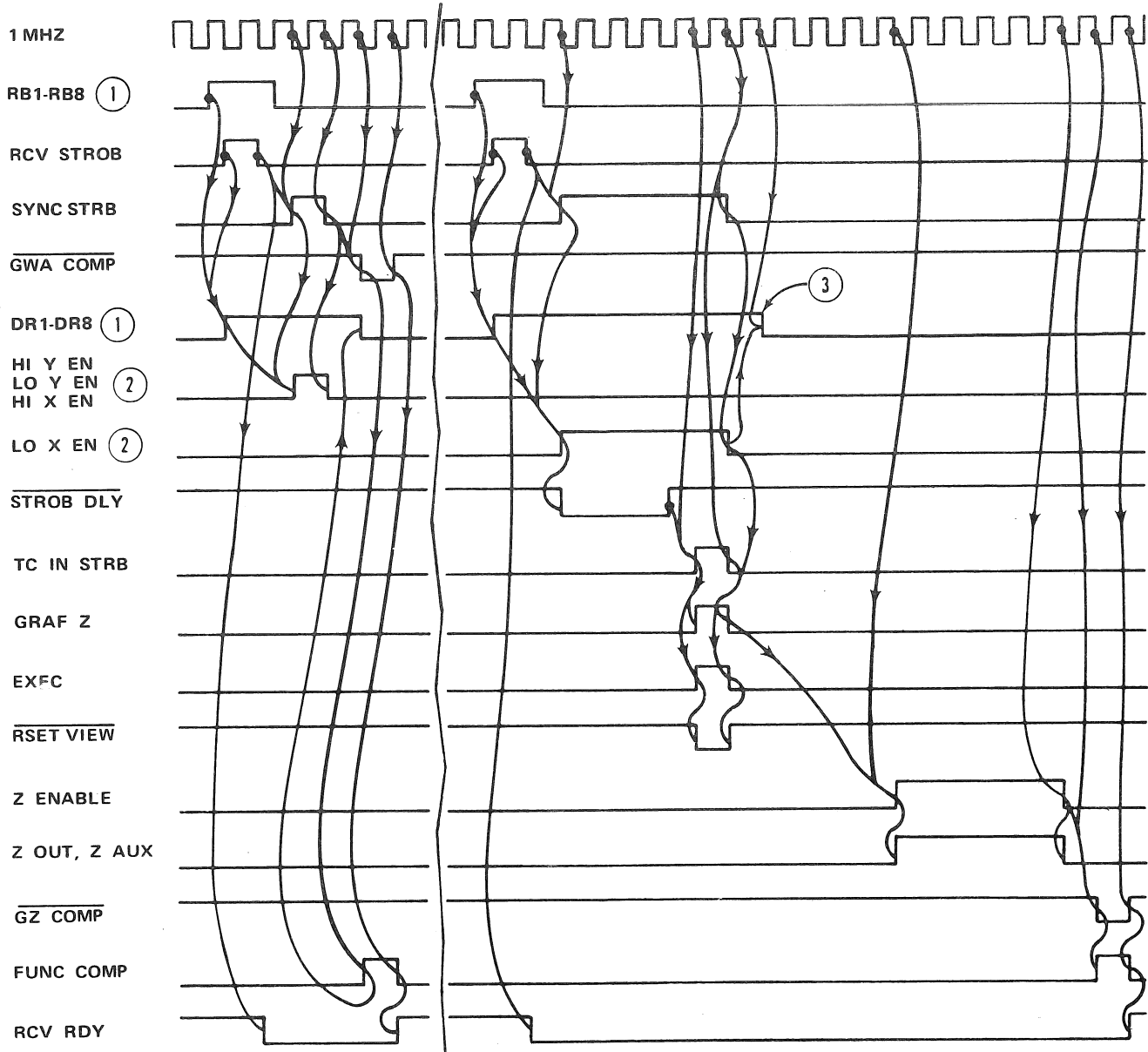
Line End Detect Circuit. This circuit consists of NAND gate U47. If the selector straps are in the horizontal position, the gate receives all high inputs after the 85th character has been written. The resultant low from U47 is applied to count up gate U49C, inhibiting that device. Additional input pulses are thereby prevented from incrementing the circuit.

The Line End pulse is also applied to U11C, causing a high to be placed on the J input of U53B. The next negative-going transition of the 2 MHz signal causes U53B to one-set, placing a high on the J input of U53A. The following negative transition of the 2 MHz clock causes U53A to one-set, putting a low on the $\overline{\text{EOL}}$ line. This low is also sent back to the clear input of U53B to zero-set it. This causes the J input to U53A to again go low. The next negative transition of the 2 MHz clock causes U53A to again zero-set, ending the $\overline{\text{EOL}}$ signal.

If the Auto CR strap is connected to the IN position, the $1/2 \mu s$ $\overline{\text{EOL}}$ pulse is also sent to U55, causing a reset pulse to be developed. This resets the X register to the Left or Center margin as determined by U19B in the Margin Control circuit.

Space Circuit. This circuit controls the movement of the register in 12 point increments as required by the character writing positions. It also controls the direction of movement and the $\overline{\text{SPAC COMP}}$ output signal. Assume that Alfa Mode exists and that the COMPOSE line is low. When the character generator finishes with character writing, a $\overline{\text{CHAR COMP}}$ signal is received, causing a high to be applied to U37D. U37D generates a low output and applies it to Space gate U51A. The resultant high produces a low from U11D which causes U57B to generate a high pulse output. This output zero-sets space FF U17A.

The low from pin 15 of U17A places a disabling low on Right Left Control flip-flop U17B. The high from U17A pin 14 is placed on the T input of U16B and also applies a high to U15C and U15D. The outputs of U15C and U15D pulse low for $1/2 \mu s$ each time the 2 MHz signal goes high. This causes the register to move one point, and also causes $\div 12$ Counter U13 to increment. Gates U15C and U15D are permitted to pass 12 clock pulses from the 2 MHz line. U13 emits a high pulse which ends when the 12th clock pulse is applied. This causes Space flip-flop U17A to become

1 MHZ

RB1-RB8 ①

RCV STROB

SYNC STRB

GWA COMP

DR1-DR8 ①

HI Y EN
LO Y EN ②
HI X EN

LO X EN ②

STROB DLY

TC IN STRB

GRAF Z

EXEC

RSET VIEW

Z ENABLE

Z OUT, Z AUX

GZ COMP

FUNC COMP

RCV RDY

① High = valid

② Only one of these occurs in response to a specific RCV STROB, determined by DR6 and DR7. Under standard strap configuration they occur in high Y, low Y, high X, low X sequence.

③ On TC-11 circuit cards 670-1444-00, DR1-DR8 go low at the beginning of FUNC COMP. On TC-11 circuit cards 670-1444-01, DR1-DR8 go low at end of LO X EN, without delay.

Fig. 5-13. Timing for Point Plot Mode. Straps set to write the point in response to a low X byte input.

BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Point Plot Mode

The Terminal goes into Point Plot Mode in response to receipt of Control Character FS. The five least significant incoming data bits can then be loaded directly into the X and Y registers to control register contents, thus controlling beam position. The registers are loaded by a four byte sequence in response to four input characters. The loading sequence is in accordance with the position of straps in TC-11 and TC-18. These straps are initially set for high Y, low Y, high X, and low X sequence. The Y bits are first loaded into the Y register to control the Y D/A output; then the X bits are loaded into the X register to control the X D/A output. After the last byte is received, the writing beam is unblanked and the point is written. After the point is written, the circuitry is reset to receive the next incoming character.

The Terminal must be in Alphanumeric Mode to receive the FS character which commands Point Plot Mode. Receipt of FS into TC-18 causes GS+FS to go to TC-11, where it enables the graphic word assembly circuitry. This causes GWA to go to TC-18 and $\overline{GWA}$ to go to TC-18 and TC-19. (Note: GWA and $\overline{GWA}$ are not direct complements of each other.) $\overline{GWA}$ into TC-19 presets the circuit for graphics.

When the 64 μs delay ends after receiving FS (see Alphanumeric Block Diagram Description), FUNC COMP goes from TC-2 to TC-19 to disable the TC IN STRB circuit.

In TC-18, the combination of GWA and $\overline{GWA}$ causes ALFA and ALFA 2 to go low and GRAF 2 to go high. (ALFA 2 and GRAF 2 are complements of each other.)

Now the circuit is set up for Point Plot operation. Assume that the sequence straps are as shown on the schematics, and that the computer will load the Terminal with four graphic bytes in the high Y, low Y, high X, low X sequence. The first byte arrives and is strobed into TC-11 by the RCV STROB. The resulting DR bits are sent to TC-10, TC-12, and TC-18. RCV STROB also goes to TC-19, where it causes RCV RDY to go low and generates a SYNC STRB for TC-11. In TC-11 the SYNC STRB causes HI Y EN to occur. HI Y EN goes to TC-10, where it loads the DR1 through DR5 bit information into the $\overline{32Y}$, $\overline{64Y}$, $\overline{128Y}$, $\overline{256Y}$, and $\overline{512Y}$ register positions, changing the Y D/A output. When SYNC STRB ends, so does the HI Y EN pulse. 1/2 μs later, a 1 μs $\overline{GWA\ COMP}$ pulse occurs and is sent to TC-2. The $\overline{GWA\ COMP}$ pulse causes TC-2 to generate a FUNC COMP pulse, which goes to TC-19 to reset the RCV RDY line high.

The next byte arrives and causes essentially the same action, except that TC-11 generates a LO Y EN pulse instead of a HI Y EN pulse. This causes the DR bits to load into the $\overline{1Y}$, $\overline{2Y}$, $\overline{4Y}$, $\overline{8Y}$, and $\overline{16Y}$ register positions. The third byte causes similar action, generating a HI X EN pulse in TC-11 to load the DR bits into the $\overline{32X}$, $\overline{64X}$, $\overline{128X}$, $\overline{256X}$, and $\overline{512X}$ register positions in TC-12. The fourth byte causes TC-11 to generate a LO X EN pulse to load $\overline{1X}$, $\overline{2X}$, $\overline{4X}$, $\overline{8X}$, and $\overline{16X}$ register positions in TC-12. The LO X EN pulse also goes to TC-18 to enable the GRAF Z circuit. On TC-11 circuit cards 670-1444-01 and above, the ending of the LO X EN pulse causes the data latches to clear, placing lows on the DR1-DR8 lines.

No $\overline{GWA\ COMP}$ pulse is generated by the fourth byte. Instead, a $\overline{STROB\ DLY}$ pulse goes to TC-19, where it causes the SYNC STRB to last about 100 μs. When STROB DLY ends, it causes a 1/2 μs TC IN STRB to be generated and ends the SYNC STRB. The TC IN STRB goes to TC-5 to generate an EXEC signal, and to TC-18 where it generates a GRAF Z signal. The EXEC signal from TC-5 goes to TC-14 to generate $\overline{RSET\ VIEW}$ for TC-1. TC-1 uses the signal to insure that $\overline{VIEW\ LMP}$ and $\overline{HOLD}$ are high and that $\overline{VIEW}$ is low. The GRAF Z signal from TC-18 goes to TC-15 to generate a Z ENABLE pulse. This goes to TC-18 to create a Z OUT pulse to write the point. When Z ENABLE ends, Z OUT ends and a 1 μs $\overline{GZ\ COMP}$ pulse goes from TC-18 to TC-2, where it generates FUNC COMP. As before, FUNC COMP resets the latches in TC-11 and resets the RCV RDY line in TC-19.

If the SSE CMD, GWA SEQ and GWA COMP CMD options in TC-11 and the GRAF WRITE option in TC-18 are set to accept a different byte sequence, essentially the same performance can be expected. Exceptions occur in the sequence in which the Y and X enable pulses (HI Y EN etc.) are generated.

Control Characters. If a control character is received by the Terminal, the low RB7 and RB6 cause $\overline{GWA}$ in TC-11 to go high. $\overline{GWA}$ goes to TC-18 to set ALFA high and to TC-19 to enable the TC IN STRB circuits. Subsequent action is essentially the same as explained in the Receiving—On Line-Direct-Alphanumeric Mode block diagram description. When the character is received and RCV RDY goes high, the Terminal returns to normal Point Plot Mode, with $\overline{GWA}$ low. RS cannot be executed while in Point Plot Mode. The Terminal must first be commanded into Alphanumeric Mode by a US (or a CR if strapped).

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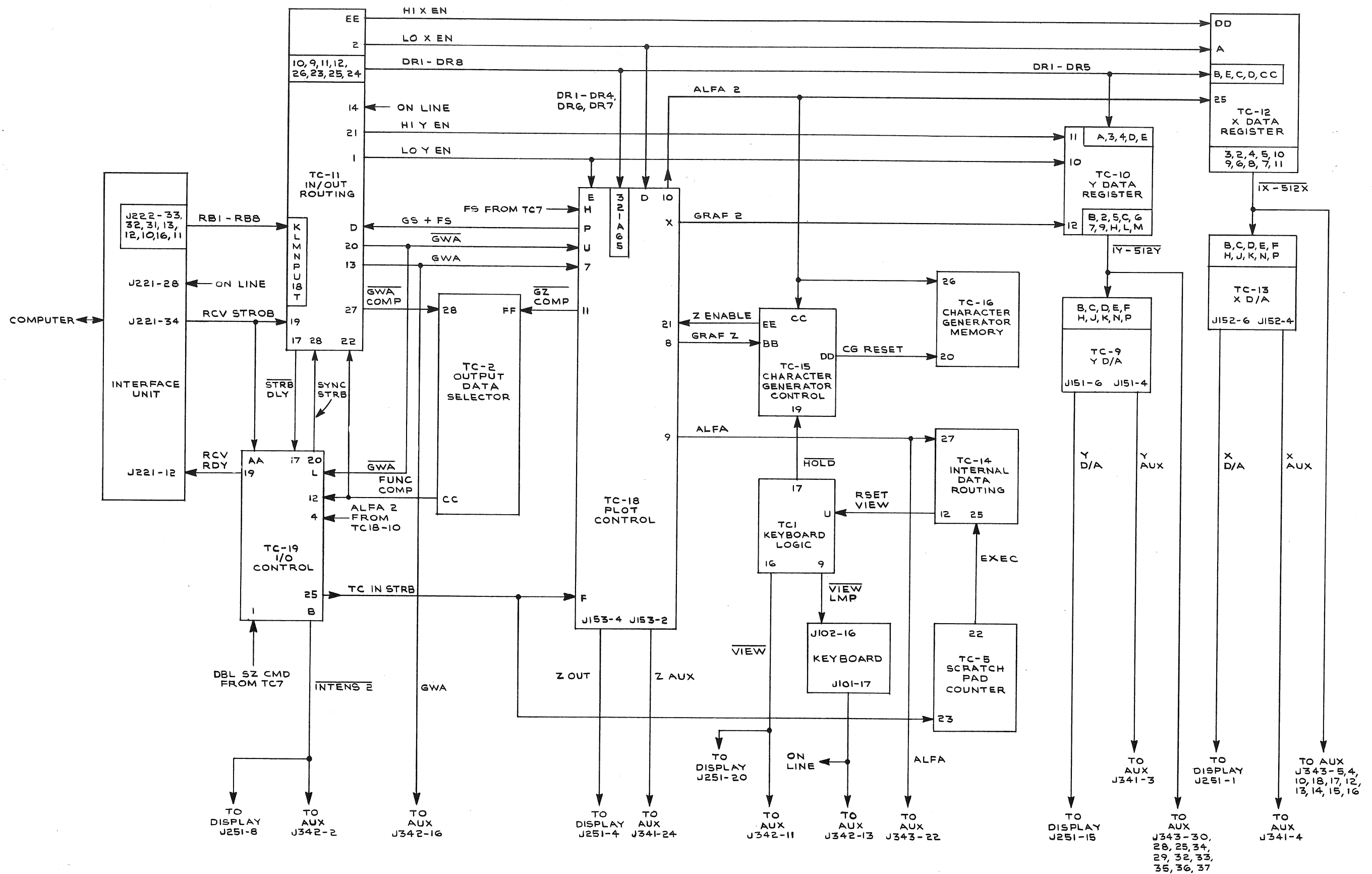
POINT PLOT BLOCK DIAGRAM

FIG 5-14
BLOCK DIAGRAM
RECEIVING IN ON LINE - DIRECT
POINT PLOT MODE

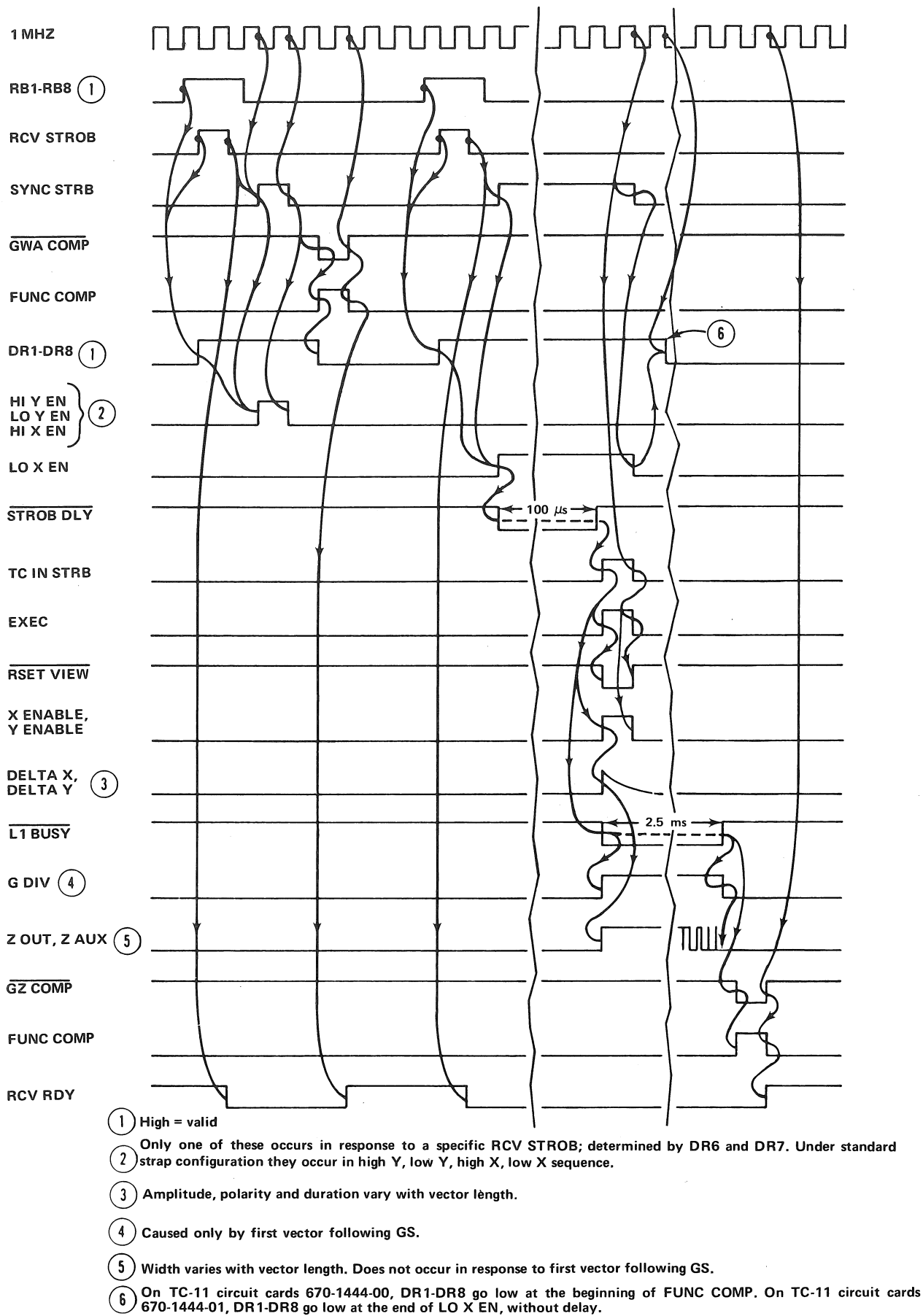4002A DRAWER

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971 EKP

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LINEAR INTERPOLATE TIMING

Signal		
1 MHZ		
RB1-RB8 ①		
RCV STROB		
SYNC STRB		
GWA COMP		
FUNC COMP		
DR1-DR8 ①		
HI Y EN / LO Y EN / HI X EN ②		
LO X EN		
STROB DLY		
TC IN STRB		
EXEC		
RSET VIEW		
X ENABLE, Y ENABLE		
DELTA X, DELTA Y ③		
L1 BUSY		
G DIV ④		
Z OUT, Z AUX ⑤		
GZ COMP		
FUNC COMP		
RCV RDY		

100 µs

2.5 ms

⑥

① High = valid

② Only one of these occurs in response to a specific RCV STROB; determined by DR6 and DR7. Under standard strap configuration they occur in high Y, low Y, high X, low X sequence.

③ Amplitude, polarity and duration vary with vector length.

④ Caused only by first vector following GS.

⑤ Width varies with vector length. Does not occur in response to first vector following GS.

⑥ On TC-11 circuit cards 670-1444-00, DR1-DR8 go low at the beginning of FUNC COMP. On TC-11 circuit cards 670-1444-01, DR1-DR8 go low at the end of LO X EN, without delay.

Fig. 5-15. Timing for Linear Interpolate Mode. Straps set to execute the vector in response to a low X byte input.

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BLOCK DIAGRAM DESCRIPTION

Receiving—On Line-Direct-Linear Interpolate Mode

General. The Terminal must be in Alphanumeric Mode to receive the initializing GS control character. The five least significant bits of subsequent characters can then be loaded directly into the X an; Y registers to control their contents, thus controlling beam position. The registers are loaded in a four byte sequence in accordance with the straps in TC-11 and TC-18. Unless otherwise requested, these straps are factory-set for high Y, low Y, high X, low X sequence.

The Y bits are first loaded into the Y Register. Then the X bits are loaded into the X Register. After the last byte is received, the beam is moved to the new position. If it is the first address to follow a GS command, no unblanking occurs. Subsequent addresses have the beam unblanked during movement, causing a line to be drawn between the points. After arriving at the new point, the circuitry automatically resets to receive the next incoming character.

If subsequent dark vectors are to be drawn, an additional GS character can be entered immediately preceding the address while in Linear Interpolate Mode. The Terminal will return to Alphanumeric Mode upon receipt of a US command, or upon receipt of a CR command if the circuitry is strapped to accept it.

Description. Receipt by TC-18 of control character GS puts highs on GS+FS, GDLI, and GDIV. It also puts lows on X ENABLE and Y ENABLE. GS+FS goes to TC-11, where it enables the Graphic Word Assembly circuit. This causes GWA to go to TC-18 and $\overline{\text{GWA}}$ to go to TC-18 and TC-19. (GWA and $\overline{\text{GWA}}$ are not direct complements of each other.) $\overline{\text{GWA}}$ into TC-19 presets the circuit for graphics. The X ENABLE and Y ENABLE lines going low prevent the X and Y registers from affecting the X and Y D/A outputs.

When the 64 μs delay ends after receiving GS (see Alphanumeric Block Diagram Description), FUNC COMP goes from TC-2 to TC-19 to disable the TC IN STRB circuit. In TC-18, the combination of GWA and $\overline{\text{GWA}}$ causes ALFA and ALFA 2 to go low and GRAF 2 to go high. (ALFA 2 and GRAF 2 are complements of each other.)

Now the circuit is set up for Linear Interpolate operation. Assume that the sequence straps are as shown on the schematics, and that the computer will load the Terminal with four graphic bytes in the high Y, low Y, high X, low X sequence. The first byte arrives and is strobed into TC-11 by the RCV STROB. The resulting DR bits are sent to TC-10, TC-12, and TC-18. RCV STROB also goes to TC-19, where it causes RCV RDY to go low and generates a SYNC STRB for TC-11. In TC-11, the SYNC STRB causes HI Y EN to occur. HI Y EN goes to TC-10, where it loads the DR1 through DR5 bit information into the $\overline{32Y}$, $\overline{64Y}$, $\overline{128Y}$, $\overline{256Y}$, and $\overline{512Y}$ register positions. No effect is felt on the Y D/A output, because Y ENABLE is low. When SYNC STRB ends, so does the HI Y EN pulse. 1/2 μs later, a 1 μs $\overline{\text{GWA COMP}}$ pulse causes TC-2 to generate a FUNC COMP pulse. FUNC COMP goes to TC-19 to reset the RCV RDY line high, and to TC-11 to clear the data latches.

The next byte arrives and causes essentially the same action, except that TC-11 generates a LO Y EN pulse instead of a HI Y EN pulse. This causes the DR bits to load into the $\overline{1Y}$, $\overline{2Y}$, $\overline{4Y}$, $\overline{8Y}$, and $\overline{16Y}$ register positions. The third byte causes similar action, generating a HI X EN pulse in TC-11 to load the DR bits into the $\overline{32X}$, $\overline{64X}$, $\overline{128X}$, $\overline{256X}$, and $\overline{512X}$ register positions in TC-12. The fourth byte causes TC-11 to generate a LO X EN pulse to load $\overline{1X}$, $\overline{2X}$, $\overline{4X}$, $\overline{8X}$, and $\overline{16X}$ register positions in TC-12. In TC-11 circuit cards 670-1444-01 and above, DR1-DR8 return low after LO X EN ends.

No $\overline{\text{GWA COMP}}$ pulse is generated by the fourth byte. Instead, a $\overline{\text{STROB DLY}}$ pulse goes to TC-19, where it causes the SYNC STRB to last about 100 μs. When $\overline{\text{STROB DLY}}$ ends, it causes a 1/2 μs TC IN STRB to be generated and ends the SYNC STRB. The TC IN STRB goes to TC-5 to generate an EXEC signal, and to TC-18 where it performs several functions. The EXEC signal from TC-5 goes to TC-14 to generate $\overline{\text{RSET VIEW}}$ for TC-1. TC-1 uses the signal to insure that $\overline{\text{VIEW LMP}}$ and $\overline{\text{HOLD}}$ are high, and that $\overline{\text{VIEW}}$ is low.

The TC IN STRB into TC-18 generates high X ENABLE and Y ENABLE pulses, and a low $\overline{\text{LI BUSY}}$ pulse. The X ENABLE and Y ENABLE pulses go to TC-13 and TC-9 respectively, to load the X and the Y Data Register information into the D/A circuits. With GDIV in effect (as occurs for the first address after each GS command), the D/A circuit outputs change rapidly.

When TC IN STRB ends, X ENABLE and Y ENABLE end. A brief time later $\overline{\text{LI BUSY}}$ goes high and GDIV goes low. GDIV then remains low until another GS command is received to command the vector to be dark. When $\overline{\text{LI BUSY}}$ goes high, it causes TC-18 to generate a 1 μs $\overline{\text{GZ COMP}}$ pulse. This goes to TC-2 to generate FUNC COMP, which goes to TC-11 to clear the latches and to TC-19 to reset the RCV RDY line.

When the first address after the GS is executed, the GDIV line goes low and remains there. The next address receives essentially the same treatment as just explained except that with GDIV low, the data latched into the Y and X D/A circuits (by X ENABLE and Y ENABLE) is confronted by an integrating time constant. The DELTA Y and DELTA X outputs are sent back to TC-18, where the larger of the two amplitudes controls the Z OUT pulse, which unblanks the writing beam. Therefore, the movement from the old to the new address occurs slower than the first (dark) one to follow GS, and the beam is unblanked to permit it to be written. With GDIV low, a 2.5 ms (nominal) timing circuit is put into effect in TC-18, causing the $\overline{\text{LI BUSY}}$ pulse to be of that duration.

If the SSE CMD, GWA SEQ, and GWA COMP CMD options in TC-11 and the GRAF WRITE option in TC-18 are set to accept a different byte sequence, essentially the same performance can be expected. Exceptions occur in the sequence in which the Y and X loading pulses (HI Y EN, etc.) are generated.
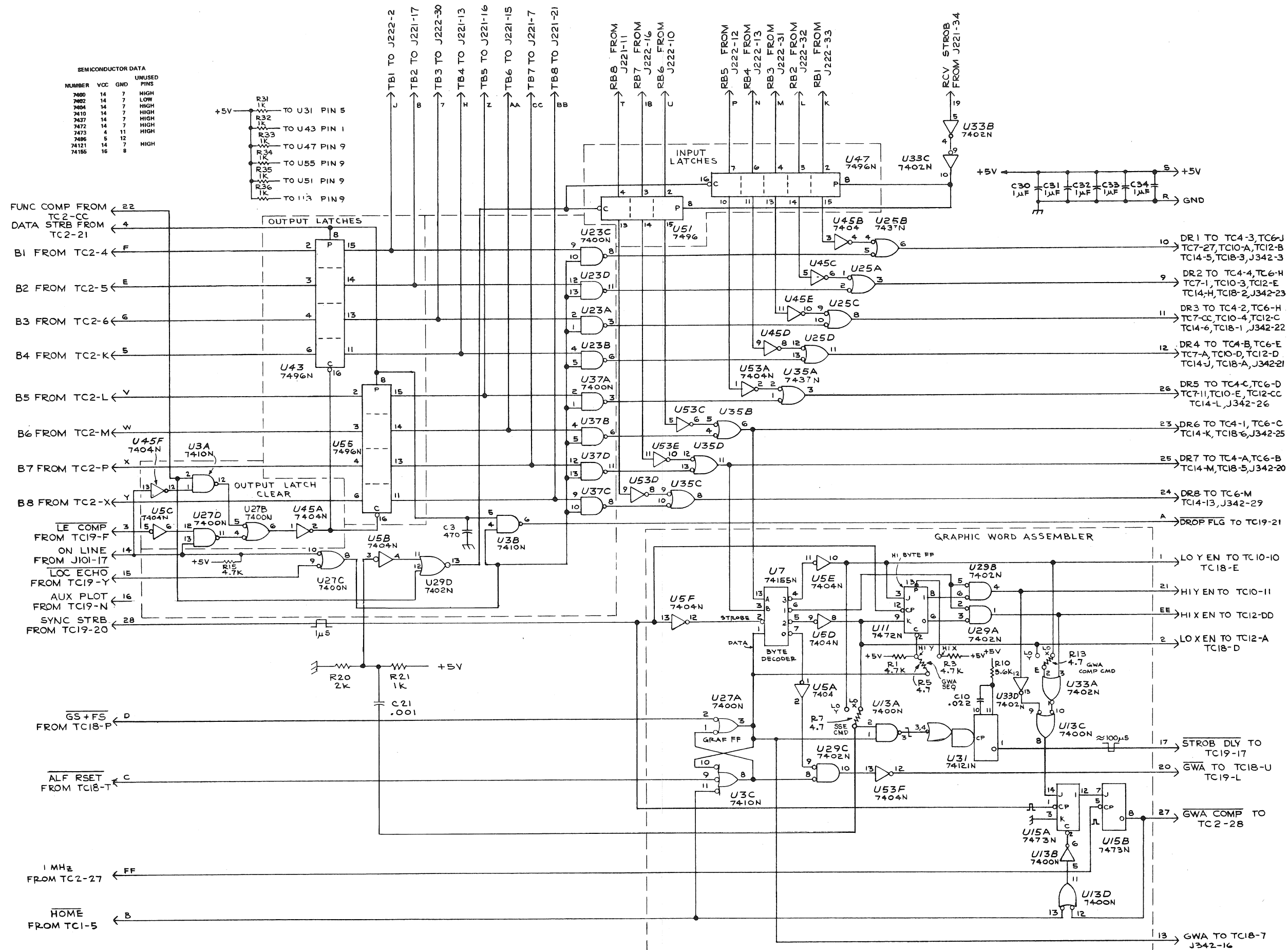
Control Characters. If a control character is received by the Terminal, the low RB7 and RB6 cause $\overline{\text{GWA}}$ in TC-11 to go high. $\overline{\text{GWA}}$ goes to TC-18 to set ALFA high and to TC-19 to enable the TC IN STRB circuits. Subsequent action is essentially the same as explained in the Receiving—On Line-Direct-Alphanumeric Mode block diagram description. When the character is received and RCV RDY goes high, the Terminal returns to normal Linear Interpolate Mode, with $\overline{\text{GWA}}$ low.

RS and FS cannot be executed while in Linear Interpolate Mode. The Terminal must first be commanded into Alphanumeric Mode by a US (or a CR, if strapped).

4002 A DRAWER

A10 IN/OUT DATA ROUTING TC-11

FIG 5-52 CIRCUIT CARD #670-1444-02 & ABOVE

Page 5-53

TC-11
670-1444-02

IN/OUT DATA ROUTING TC-11
FIG. 5-52A
CIRCUIT CARD #670-1444-01

A10

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TC-11
670-1444-01