MAY 4 1981

Tekscope

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Tekscope CONTENTS

Cover

The cover illustration conceptually demonstrates the multivendor capability of the new 8550 Microcomputer Lab. The 8550 supports a multiplicity of devices, 26 at present, and more in the near future. Illustration: Michael Satterwhite.

Tektronix is an equal opportunity employer.

A Microprocessor Development Lab with an Expandable Future

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Systems from Man-
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*Engineers. Bob gained extensive experience in
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After a time in Guernsey, he moved to EMC in
Amsterdam as European marketing product
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lyzers and communication testers. Bob moved
to Beaverton and assumed his present position
early in 1980. For recreation Bob enjoys racquet-
ball and outdoor activities including hiking and
camping.*

Designing with microprocessors is a dy-
namic activity. New applications of the
device appear daily. And tomorrow's pro-
cessors will perform even more complex
tasks. Microprocessor users must choose
their design tools wisely to be able to take
full advantage of the processors available
today and those coming along.

As microprocessor capabilities increase,
the size and make-up of design teams will
change. More extensive programming will
be needed to effectively put these new
capabilities to work. It is important that the
design tools you choose today be adaptable
to your design needs well into the future.
The new Tektronix 8500 Modular Microcom-
puter Development Lab Series is a design
tool with such flexibility.

Right now, there are three major ele-
ments in the series:

- The 8550 Microcomputer Development
  Lab (MDL), a self-contained, single-user
  system that supports 26 different chips,
  including the more popular 16-bit pro-
  cessors such as the Z8001, Z8002,
  68000, 8086, 8088, SBP9900, and
  TMS9900.
- The 8560 Multi-User Development Lab
  system, which contains a dedicated
  central computer and supports up to
  eight workstations.
- The 8540 Advanced Integration Unit for
  performing hardware/software integra-
  tion in host computer environments.

The 8560 can accommodate up to eight
users with any combination of 8550s, 8540s
or any RS232C terminals. Enhanced per-
formance is achieved with the Tektronix
CT8500 Terminal.

The 8550 is available now, with the 8560
and 8540 to follow within the year.

The 8550 single-user system

The 8550 Microcomputer Development Lab
(figure 1) consists of two basic units — the
8301 Microprocessor Development Unit and
the 8501 Data Management Unit. Working
together, these units support both software
development and hardware/software
integration.

The 8301 Microprocessor Development
Unit houses a system processor with 32K
bytes of static system memory, 32K bytes
of static program memory, a language pro-
cessor, and an emulator controller. There
is room for plug-in hardware options such
as emulator processors, an additional 32K
bytes of static program memory, a real-time
prototype analyzer (RTPA), and a PROM
programmer. The 8301 accommodates up
to 16 plug-in circuit boards.

Multiple processor architecture

The 8301 uses a multiple-processor archi-
tecture in a master-slave relationship (see
figure 2). The system's controller board,
serving as the master processor, runs the
operating system, directs the input/output
(I/O) activities for system peripherals, and
directs all of the other system elements
such as the emulator controller, language
processor, PROM programmer, and emu-
lator processors.

The language processor operates as a
slave to the system processor and trans-
lates assembly language or high level lan-
guage into machine language for the emu-
lator processor. In addition, it runs the edi-
tors including the high-performance ad-
vanced CRT editor.

The emulator processor, which is the
same type as that to be used in the proto-
type hardware under development, runs
user programs and interfaces with the pro-
totype hardware. Interaction between the
system and emulator processors is con-
trolled by the emulator controller under the
direction of the system processor. The emu-
lator controller ensures that only one pro-
cessor has control of the system buses at
any time.

Fig. 1. The 8550 Microcomputer Development Lab is a versatile software development and hard-
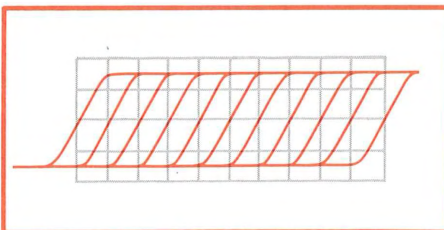ware/software integration system for microprocessor-based product design. The system supports
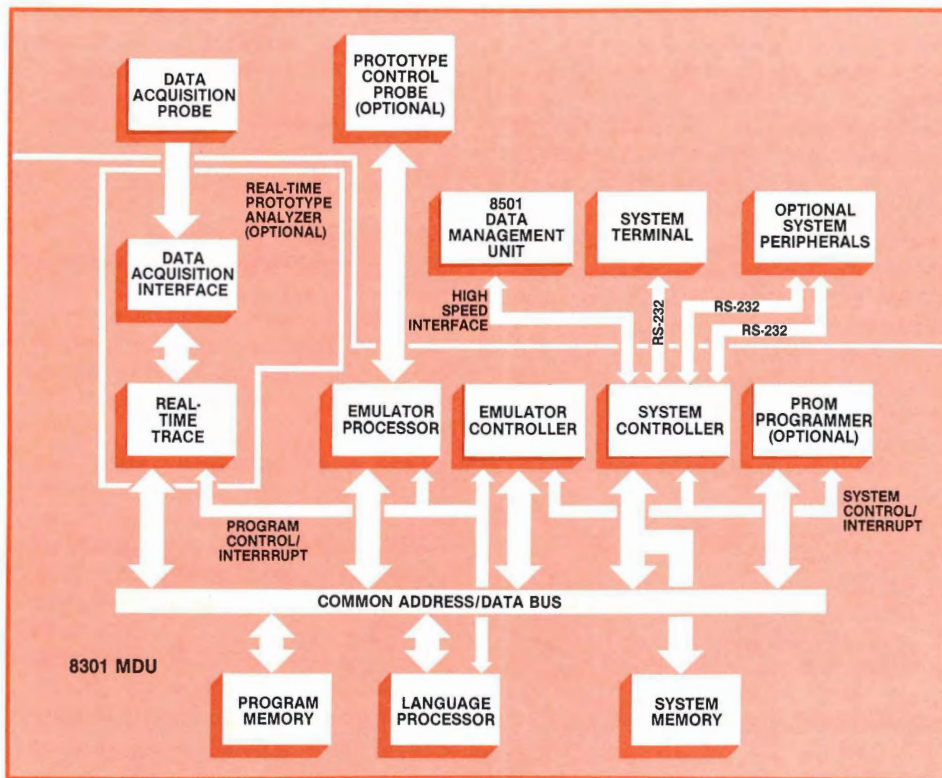many popular 8- and 16-bit microprocessors.

Fig. 2. Functional block diagram of the 8301 Microprocessor Development Unit. The system uses a multiprocessor architecture in a master/slave arrangement. The system processor (in the system controller) serves as the master, with the emulator and language processors serving as slaves. A high-speed interface provides rapid data transfer between the 8301 and 8501 Data Management Unit.

Management Unit (DMU) as needed. The system memory also provides buffer space for I/O activities.

The primary purpose of the program memory is to store the user program during execution by the emulator processor. The program memory also provides working space for the system and assembler processors, but only during program assembly and editing activities. During emulation, all program memory is available for the target microprocessor.

The system processor has access to both system and program memories. Several operating features are available to speed up the transfer of data between memories, including direct memory access (DMA), memory-to-memory data transfer, and bank switching of 16K-byte blocks of data. A special high-speed interface port permits data transfer between the 8301 and 8501 at a 153.6 kilobaud rate.

Several emulation modes are available: mode 0, mode 1, and mode 2 (see section on emulation capabilities). When operating in emulation mode 1, a memory map function is available that allows the operator to assign 128-byte blocks of memory address space to either the program memory in the 8301 or the memory in the prototype hardware. Assignments can be made throughout a total address space of

System bus structure

The system bus in the 8301 is a 100-line bus structure that is common to all 16 plug-in circuit boards. The bus is essentially universal in that data, address, and control lines are paralleled to all boards. The exceptions are the independent debug and interrupt lines and some control lines for the system and emulator processors (see figure 3). The separate lines result in a virtually uncrashable architecture.

The memory structure

In keeping with the multiprocessor concept of Tektronix systems, the 8301 memory is segmented. The system and program memories are identical 32K-byte static random-access memories (RAMs). The program memory is expandable to 64K bytes by adding a plug-in memory module.

The system memory is accessed only by the system processor and contains DOS/50, the operating system. The main resident part of DOS/50 is transferred into system memory at start-up, with subroutines loaded from the system disc in the 8501 Data
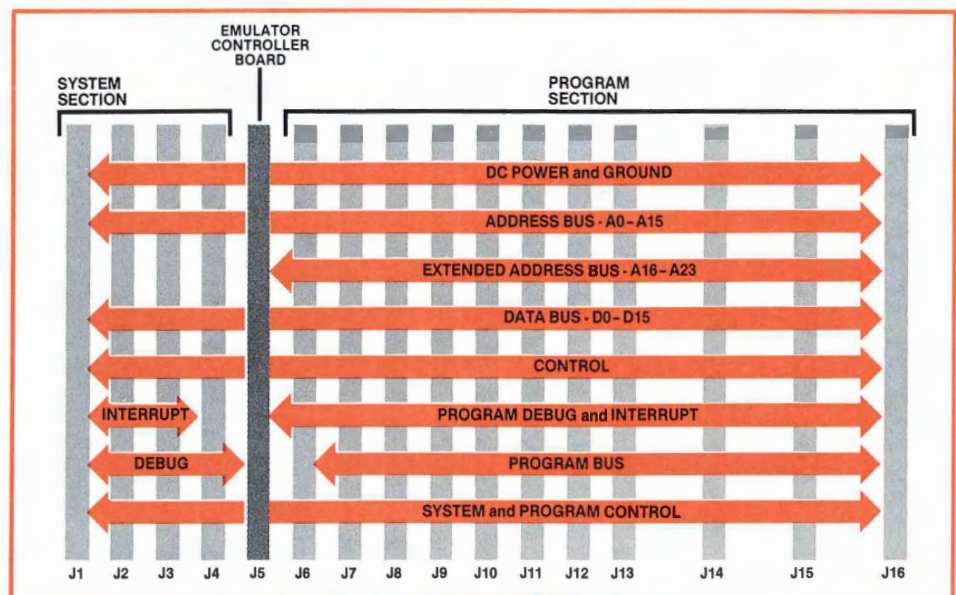

Fig. 3. The system bus consists of 100 lines that provide connection to the plug-in circuit boards in the 8301. The emulator controller board separates those control and signal lines that are dedicated either to the system section or to the program section.

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64K bytes. This function also allows write protection to segments of program memory, as selected by the user.

The 8501 provides high-volume bulk storage up to two megabytes on two double-density, double-sided-disc compatible drives with DMA data transfers. A 32K by 16-bit dynamic RAM board provides temporary storage space for the file manager, device interrupts, and other functions.

The 8501 also contains two 1K-byte read-only memories (ROMs). These ROMs contain a boot-up program for loading the operating system into system memory, and a set of self-test routines that are performed at start-up to ensure the 8550 is ready for use.

The disc operating system

The 8550 uses a new operating system called DOS/50 (for Disc Operating System, 8550). While similar to TEKDOS (the operating system for Tektronix 8001 and 8002 MDLs) in many respects, DOS/50 provides several new options for arranging, manipulating, and protecting files and a number of enhanced debugging commands.

DOS/50 supervises general input and output, file creation and maintenance, program assembly and compilation, program execution, monitoring and debugging, PROM programming, and communication.

Optional software (such as assemblers) can be easily combined with DOS/50 on a master disc (which can store up to 1 megabyte) giving you the convenience of having all of the assemblers, emulators, and compilers you would normally use, on one system disc.

DOS/50 includes several other operating conveniences, such as *spooling,* which allows DOS/50 to send output to a line printer while performing other tasks; and *type-ahead,* which allows you to enter additional commands while the previous command is executing.

File management

The 8501 Data Management Unit handles files for DOS/50 and manages the movement of user files between its flexible discs and program memory in the 8301.

Data management is simplified by using a tree-like file structure (see figure 4), which allows the user to specify one main system directory, one root directory for each disc, and any number of subdirectories under the root directory. Data files may be created and entered directly into the root directory.
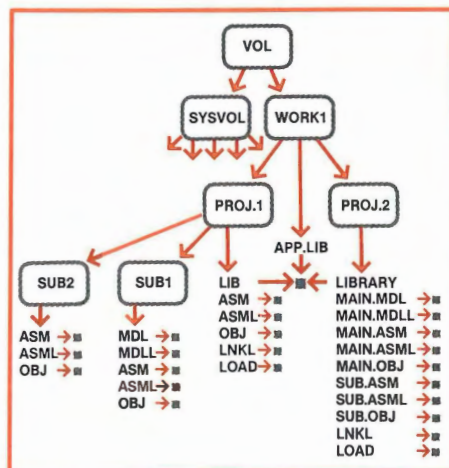

Fig. 4. An example of the DOS/50 tree-like file structure. The "root" of the tree is at the top. The rectangles represent directories, while the squares represent data files. Arrows indicate a logical connection, from which a path can be designated with a file specification.

As files are accumulated, the user may organize them into specific groups, each under its own specific directory. The user may create directories within directories to any level of nesting desired.

With extensive nesting, the file specification needed to access a specific file can be lengthy and cumbersome to use. DOS/50 includes a BRIEF command, which allows the user to specify a file by a single name. This greatly speeds up access to frequently used files.

DOS/50 also includes an extensive set of file attributes that allow the user to designate: the file owner, who can read from or write to that file, the date and time of file creation, when the file was last written to, when it was last accessed, and so forth. These attributes are especially helpful in keeping a file current when more than one user works with the file.

The assembler software packages for the 8550 offer powerful macros, library generators, linkers, and other capabilities designed to enhance the user's productivity.

Emulation capabilities

Integrating hardware and software is often the most time-consuming and frustrating task encountered in designing a microprocessor-based product. The 8550 emulator options allow integration in several stages, gradually transferring functions from the 8550 to the prototype.

Three levels of emulation are available:

- Mode 0, which uses the 8550's clock, program memory, and I/O signals to run the user's program. The prototype hardware is not needed in this mode, allowing software debugging to take place before the prototype is operational.

- Mode 1, (a partial emulation mode) uses the prototype's clock and I/O services. Some emulators also allow use of the 8550's I/O services in Mode 1. The program is run on the emulator, which may access both program memory and prototype memory. However, full control of the system is maintained by the system controller. A memory map function allows assignment of 128-byte blocks of memory address space as previously discussed in the memory structure section. The emulator can operate at full speed using either program or prototype memory.

- Mode 2, (the full emulation mode) uses only the prototype's memory, clock, and I/O facilities and runs the user program under the emulator processor's control. The user program can run at full speed, so any problems with functions involving critical timing relationships can be resolved.

In modes 1 and 2, the emulator takes the place of the microprocessor that eventually will reside in the prototype, using a prototype control probe to connect the prototype to the emulator.

The prototype control probe is a critical link in the emulation system. The ideal emulator would be transparent to the prototype hardware. That is, the prototype would function as though the microprocessor were plugged directly into its socket on the prototype hardware. In Tek emulators, the microprocessor is mounted in the prototype control probe pod, close to the prototype microprocessor socket, thus substantially reducing the loading and propagation-time effects normally associated with emulators.

The real-time prototype analyzer

The optional real-time prototype analyzer (RTPA) enables the designer to locate critical timing problems and hardware/software sequence problems in the prototype. The RTPA serves, in essence, as a logic analyzer for all data, addresses, and access control on the prototype's microprocessor socket. A logic probe provides an additional eight lines for viewing logic signals anywhere on the prototype board.

Two New Hard Copy Units Feature Low-Cost, High-Contrast Copies

The RTPA uses a 43-bit buffer to store program information captured from the address, data, and control busses. The user has a high degree of flexibility in selecting the data to be stored. Every transaction can be stored and displayed, or a specific window can be stored and analyzed while program execution continues at full speed.

For working with 16-bit designs, a trigger trace analyzer (TTA) option will soon be available. With a 62-bit wide, high-speed buffer, it will be capable of working with bus cycle speeds up to 8 MHz, and storing up to 16 data bits, 24 address bits, 14 emulator-dependent bits, and 8 bits from external hardware. Up to four independent events can be combined in both logical and sequential combinations to form a breakpoint or data storage trigger.

The PROM programmer

The user's final step in integrating the hardware and software is committing the program to PROM and evaluating its performance in the prototype. A PROM programmer option for the 8550 will soon be available that provides the capability to burn a PROM with data from program or prototype memory, read data from a PROM into program or prototype memory, or compare the PROM's contents with the contents of memory. The 8550 PROM programmer will support the Intel and Texas Instruments 2716, 2732, and Intel 8741, 8748, 8749, and 8755 PROMs.

Conclusion

As microprocessors become more numerous and their capabilities expand, the number of people involved in putting microprocessors to work will increase drastically. Software development and hardware/software integration will become a larger part of total project design time and expense.

The microprocessor development tools you choose today should meet your design needs tomorrow. The Tektronix 8500 Modular Microcomputer Development Lab Series will give you the flexibility to expand your design system as your needs expand. ■

Fig. 1. The 4611 Hard Copy Unit provides fast, clean, low-cost copies of direct-view-storage tube displays. The companion 4612 provides copies from raster-scan displays or other video signal sources.

Very early in its experience with computer graphic displays, Tektronix recognized the need for what is now commonly known as a "hard copy unit" — a device that connects to a terminal or monitor and reproduces, on paper, all of the graphic and alphanumeric information that appears on the screen. The concept is to reproduce information quickly (in less than 30 seconds) and conveniently, so that the operator need only press a button to obtain a copy. This gives the operator the freedom to request copies as often as needed, with a minimum of interruption in the work flow.

Quick hard copies of this kind are excellent working documents to annotate and edit as an aid to program development and debugging. They also serve as permanent records for the file — documenting, for example, intermediate steps of an important work session with the computer terminal. High-quality hard copies are often incorporated into reports and presentations. And when you require extremely high-quality (camera-ready) output; hard copies provide a quick preview and a chance to screen information for errors before sending it to a

plotter for final production. This capability becomes particularly important when the display is complex and final plotting can take several minutes.

A history of expertise in electrophotographics

Tektronix introduced its first hard copy unit in 1971, and has since developed a broad line of copiers (see figure 2). Prior to the introduction of the new 4611 and 4612, all of the Tektronix devices were based on electrophotographic technology. As the name implies, electrophotography is a photographic process, based on light-exposure techniques. Information to be copied from the display is brought into the hard copy unit and processed. Portions of the information are then displayed on a small cathode ray tube (CRT) located inside the hard copy unit. Light-sensitive paper containing a dry silver emulsion passes by the face of the hard-copy CRT, and thus is exposed to the same image as appears on the display to be copied. Bundles of tiny fiber-optic pipes keep the light from diffusing as it travels through the CRT faceplate

to the paper. The paper is heat-developed, with the end result being a very crisp, clear image of the original display.

The electrophotographic technique has several advantages over other hard-copy techniques. The process uses no toner, and image quality is very high. But the technique's most important advantage is its ability to produce true continuous-tone gray shades. Most other technologies must simulate gray shading by using half-toning methods — that is, by varying the dot sizes or spacing between dots to represent different shades of gray.

The ability of electrophotography to produce true gray shading makes the Tektronix devices using this technique excel in providing working copies from sophisticated image-processing systems with twelve or more shades of gray (the 4634 Imaging Hard Copy Unit), and for providing black and white copies of raster-scan color terminal displays (the 4632 Video Hard Copy Unit).

The expansion into electrostatic technology

The new Tektronix 4611 and 4612 Hard Copy Units are based on electrostatic technology — a technique involving the transfer of an electrical charge to paper. Incoming information about the image to be copied is processed and sent to a printing mechanism which "deposits" the image in its preliminary form as tiny points of electrical charge. The charged points on the

paper then attract particles of a black toner, making the image visible on the paper.

We have already discussed the advantages of electrophotographic light-exposure techniques. Why, then, expand into electrostatic technology and create the 4611 and 4612? Because electrostatic technology has some strong advantages of its own. The paper used in the process is excellent. Called "electrographic" or "dielectric," the paper has the look, feel, and handling characteristics of plain bond paper. The front side of the paper has an extremely thin plastic layer that aids in the charge-transfer process and is barely perceptible to the touch. Copies can be annotated with any kind of writing medium, including felt-tip and other liquid pens. Images are permanent with no tendency to age with exposure to heat or light.

Images made using electrostatic techniques are very high in contrast. That is, lines and characters are crisp and black on a very white background. And — perhaps the most significant advantage of electrostatics — the paper is very inexpensive, resulting in a copy cost less than one-third that of the dry silver paper used in electrophotographic copiers.

The 4611 and 4612 Hard Copy Units have all of these properties inherent to electrostatic technology. In addition, the 4611 and 4612 are based on an innovative implementation of the technology — one which brings advantages of its own. The imple-

mentation developed at Tektronix allows a lower base unit price than previously possible for an electrostatic hard-copy device. It also improves both image quality and operator convenience, and permits a very compact design. The 4611 and 4612 are only sixteen inches wide, seven inches high, and weigh just forty-five pounds.

A moving stylus for lower cost and better image

In most electrostatic copiers, charge transfer is achieved using a matrix of fixed-wire styli as wide as the paper being imaged. With up to 200 styli per inch, the manufacturing cost of this matrix and the electronics necessary to drive each stylus is high. The 4611 and 4612 use a novel approach — a moving stainless steel belt with raised styli in contact with the paper (see figure 3). This belt and the associated drive electronics are much less complex than the wire matrix and its drive circuitry, and thus less costly to manufacture. An added benefit of the moving styli is the ability to position adjacent dots with significant overlap to achieve smoother and darker lines and characters. This is illustrated in figure 4. As you can see, the line on the right is smoother and more easily integrated by the eye. This is due to high addressability (number of dots per inch) and significant dot overlap.

Dry toner for less mess and more consistent image density

Most electrostatic instruments use liquid-toning systems. Liquid toner consists of a suspension fluid (usually Isopar, a highly refined form of kerosene) containing suspended, black, charged particles that are attracted to imaged areas when this liquid is pumped against the paper. These systems have several disadvantages — the liquids are messy and inconvenient, and as copies are made, the black particles are used up resulting in a progressively lighter image. Copies can become faint and hard to read. Both concentrate and suspension fluid must be added periodically to maintain proper image density. Also, if the paper sits still for any length of time in contact with the liquid applicator, the toner seeps into the paper and leaves a gray smudge.

In contrast, the 4611 and 4612 are the first desktop terminal copiers to use dry, single-component, magnetic toner. This powder is inert and nontoxic and consists of particles that are a uniform mix of
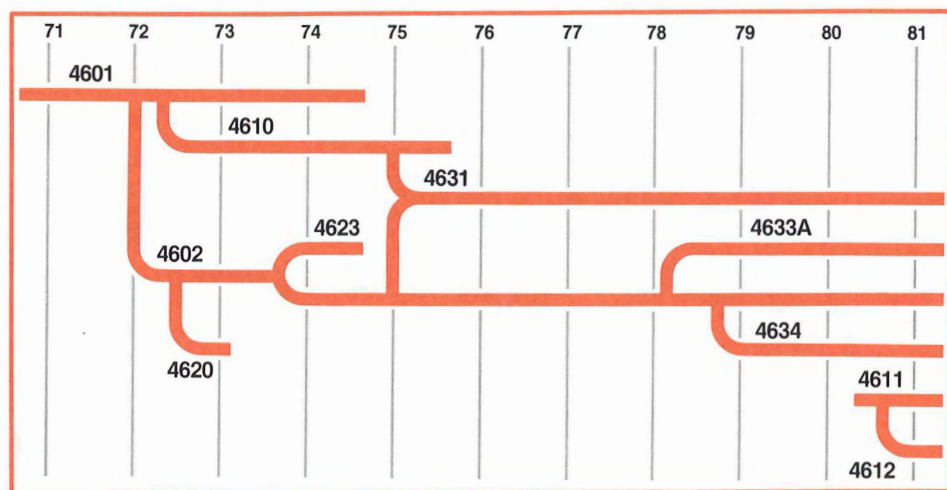

Fig. 2. The Tektronix family tree of copiers includes units that provide, in seconds, high image-quality copies of direct-view-storage tube and raster-scan displays. A line-scan recorder and a unit providing extensive gray scale (photographic) capabilities are also available. The 4611 and 4612 are the newest members of the family.
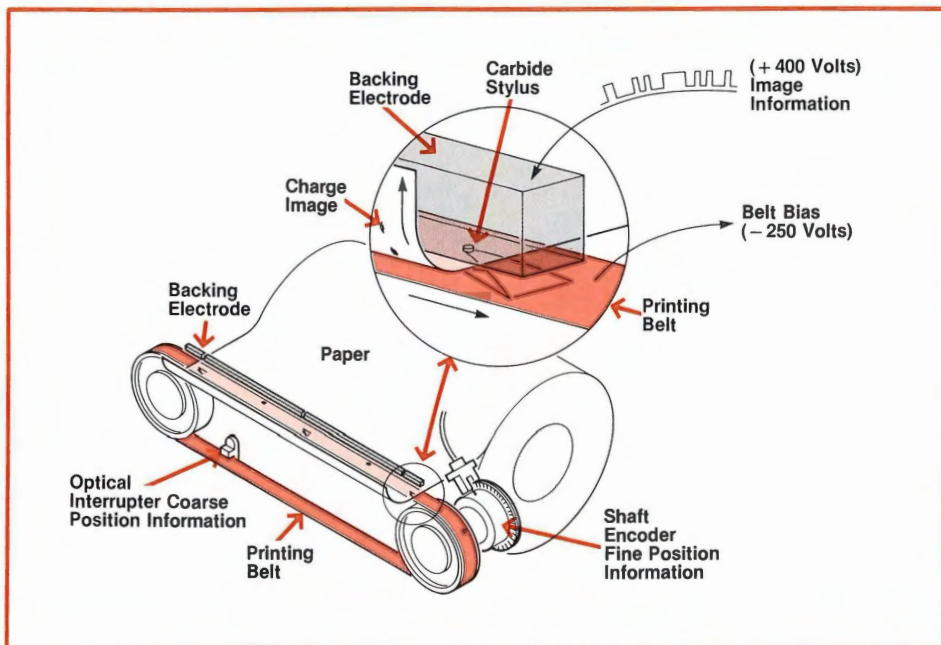
Fig. 3. The 4611 and 4612 employ a unique means of applying charge to the paper. A 0.001-inch thick stainless steel belt contains carbide styli attached to raised triangular portions of the belt. Two of the styli are in contact with the paper at any point in time.

carbon, wax, and magnetite. The most significant benefit of single-component toner is consistent image quality. As toner is used up in making copies, image density is consistent until the toner is almost completely gone. One loading of powder (about five ounces) will produce approximately 2,500 copies. Another important advantage is that there are no liquids or separate elements to mix, a major step in user convenience.

The inside story

A schematic of the 4611 and 4612 printing mechanism and charge-transfer process is shown in figure 3. A latent image is created on dielectric paper by charge transfer from a carbide stylus attached to a moving stainless steel belt. The belt scans across the paper as the paper is being pulled through the instrument, forming a raster-scan image. The 0.001-inch thick belt has raised triangular sections with a carbide writing stylus attached to the tip of each section. The belt also has square holes located in fixed relation to each stylus, to provide position-sensing by an optical detector. The belt runs on a set of 8-inch circumference crowned pulleys. One pulley is driven at approximately 2500 revolutions per minute by an induction motor, giving the belt a linear velocity of 330 inches per second. The total copy time for an 11-inch piece of paper is 24 seconds.

Two optical detectors provide position information to control image placement. One detector looks at holes in the belt, producing a signal each time a stylus starts at the left edge of the paper. The second detector looks at an encoder disc attached to the drive pulley. As the pulley rotates, output pulses from the detector provide belt linear motion and position information. The resolution of the encoder on the drive pulley gives 2048 imageable positions per eight inches of stylus travel (one revolution

of the drive pulley). This arrangement is how the high addressability (256 points per inch) and dot overlap are obtained to give the line quality shown in figure 4.

Charge is deposited on the very thin non-conductive coating on the surface of the paper. Charge transfer occurs via air-gap breakdown when a potential difference of 650 volts exists between the writing stylus and a backing electrode in contact with the conductive backside of the paper. The air gap is caused by paper-surface roughness. The stainless steel belt is biased at −250 volts and the backing electrode is driven from zero to +400 volts when an image is desired on the paper. Negligible charge transfer occurs with a voltage differential of less than 300 volts.

Two styli are on the page at any one time. Using two styli requires a segmented backing electrode and slightly more complex electronics, but produces approximately twice the printing speed possible with a single stylus. The controlling circuitry monitors position signals from the two optical detectors and applies voltage to the appropriate backing electrode(s) when either stylus is in a position where image information is desired.

After receiving the charge image, the paper moves past an applicator, where single-component magnetic toner is transferred to the charged areas on the paper (figure 5). Because the toner particles are magnetic, they form chains along the lines of flux from the magnet. As the magnet rotates, these chains are brushed against the surface of the paper. Because the toner
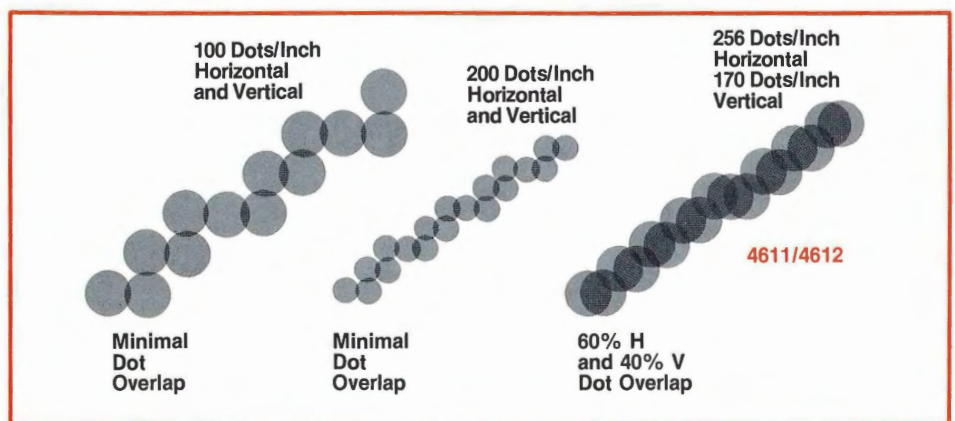

Fig. 4. Line quality is a function of dot overlap and the number of addressable points. The 4611 and 4612 have an addressability of 256 dots per inch horizontally and 170 dots per inch vertically. Dot overlap is greater than 60 percent in the horizontal direction and 40 percent in the vertical direction.

Obtaining a Hard Copy from a Cathode Ray Tube Display

It is often desirable to make a permanent copy of the information displayed on a cathode ray tube (CRT) screen. CRT hard copying is the process of transferring a temporary image from a CRT screen to a piece of paper. "Hard" refers to the ability to touch the results, and means that the image doesn't disappear when power is turned off. "Copy" means that what you see on the screen is what you want on the paper.

The first basic element of any hard-copy process is to acquire the image information.

In direct-view-storage tubes (DVSTs) the image is stored in the phosphor on the surface of the screen. This process means that we must scan the phosphor screen to obtain image information for making a copy. To determine whether any given point on the screen has stored information, we position the electron beam to that location and turn it on, but without the intensity required to store that point. A sense amplifier on the storage backplate can determine whether or not that point has stored information, because secondary emission is different for written and nonwritten areas of the phosphor. The image may be read by moving the electron beam

from point to point in a raster-scan fashion until the entire screen has been covered.

In a raster-scan terminal, the image is stored in semiconductor memory and constantly refreshed on a CRT screen. The image is commonly available as a composite video signal. This signal consists of timing pulses and picture data, repeating at the refresh rate of the terminal. RS-170[1] is commonly used in the television industry for specifying format, timing, and voltage requirements of a

monochrome composite video signal. The composite video provided by most CRT terminals follows the basic format of RS-170 but may vary somewhat in specific timing or voltage levels. Once you have a composite video signal and know its voltage and timing characteristics, it is fairly straightforward to sample the image information.

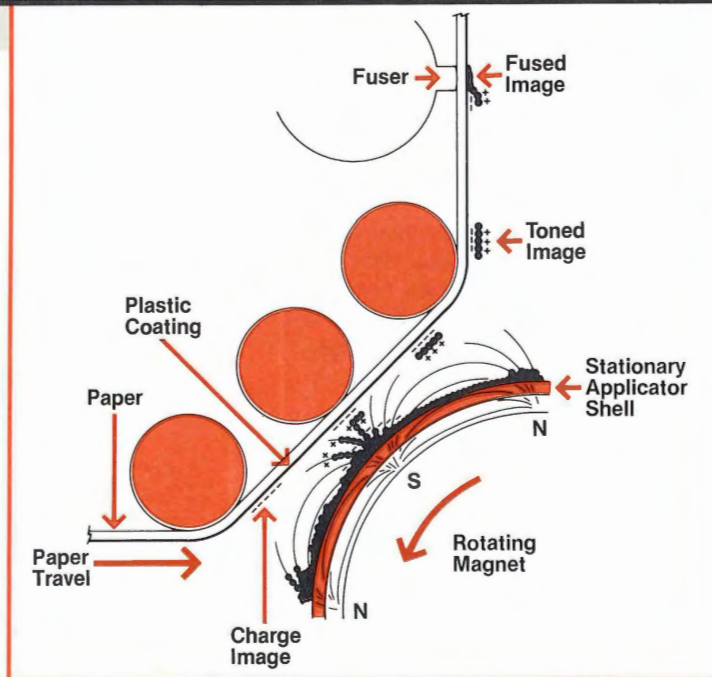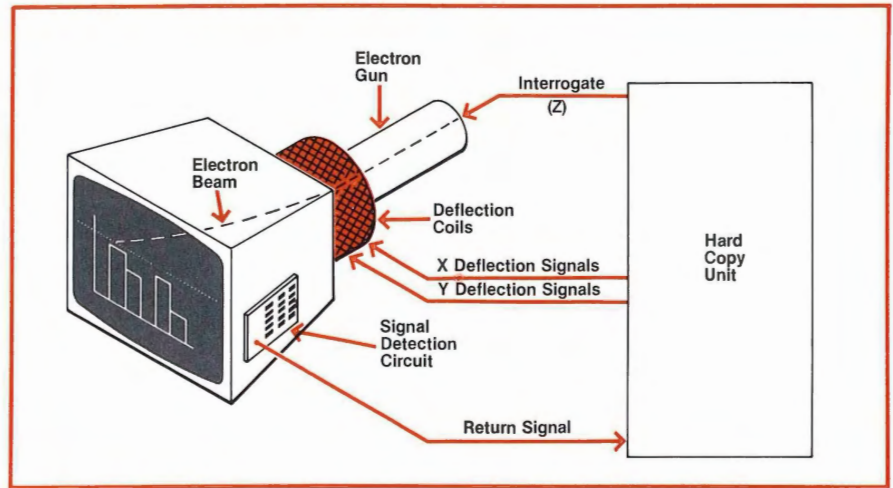[1]EIA RS-170: Electrical Performance Standard — Monochrome Television Studio Facilities

Fig. 5. A new dry toner overcomes the inconvenience and mess typical of liquid toners, and yields a uniform-density, high-contrast copy every time.

is also conductive, as the end of a chain approaches a charged area on the paper, like charges are repelled, giving the end of the chain an opposite charge that bonds toner to the charged areas. In nonimaged areas, magnetic force pulls the toner particles back to the applicator, leaving very little background. The toner particles are fused to the paper by heat from a metal fusing bar contacting the backside of the paper. This bar rotates downward when the copier is quiescent to prevent excessive heating of the paper. This action also prevents the operator from being able to accidentally touch the hot surface when loading paper.

The benefits of a modular design

An outline drawing of the assemblies in the 4611 and 4612 is shown in figure 6. All major sections of the instrument can be assembled and tested separately. This capability provides significant benefits for both field service and the manufacturing line. Repair time in the field is much shorter because almost any failure can be fixed by
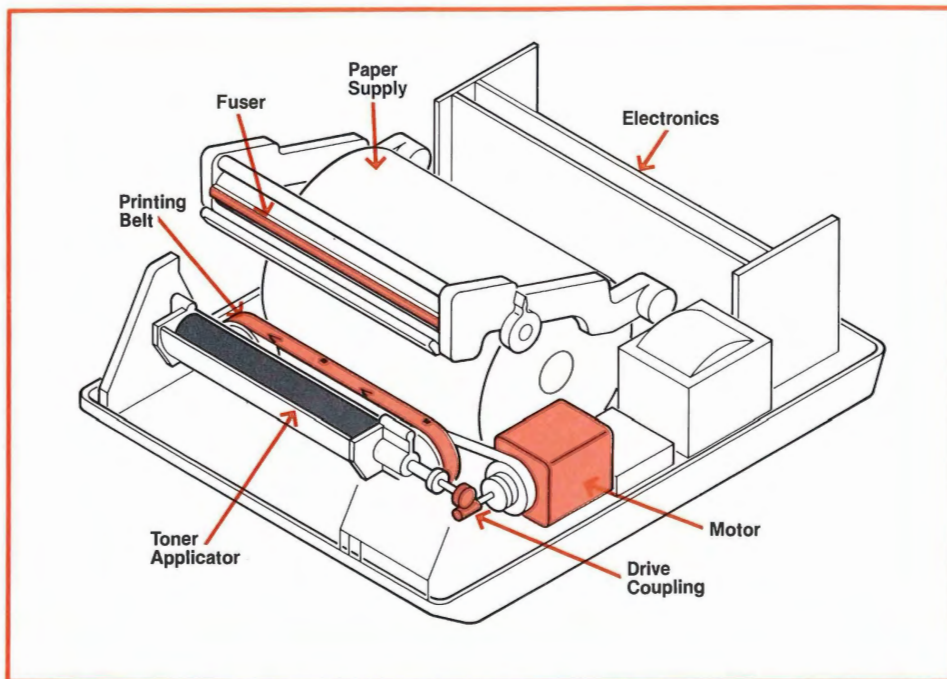
Fig. 6. The 4611 and 4612 consist of several subassemblies which are built and tested as individual modules. Modular design and construction simplifies both manufacture and service.

Cathy Cramer is the marketing product line manager for graphic hard-copy devices. She joined Tek following graduation from the University of California at Irvine with a B.A. in mathematics in 1975. Cathy wrote technical documentation for the 4051 Graphic System, then moved to graphic computing systems as a marketing product specialist working on the team that introduced the 4052 and 4054 Desktop Computers.

Tom Peekema is an engineering manager in the graphic hard-copy group and was project manager for the 4611 and 4612. He received his B.S.E.E. from Washington State University, joined Tek in 1974, and has worked in several areas of the Information Display Division. He leads a very busy personal life enjoying flying, soaring, puzzles, playing the piano, billiards, and racquetball.

merely exchanging assemblies. On the manufacturing line, modularity allows for an efficient division of labor. Those items that require precision assembly are produced at the module level, independent of the flow of final instrument assembly. This technique simplifies final assembly to mainly coupling together completed subassemblies.

An emphasis on reliability

Attention was given to reliability at every design phase of the 4611 and 4612. Steps taken included subjecting critical mechanical components to extensive life-tests to detect possible failure modes and correct them, implementing well-established procedures for elevated-temperature life testing of the electronic circuitry, and putting early production instruments through environmental and life tests to ensure that the 4611 and 4612 would meet or exceed all design goals prior to start of product shipment.

The aluminum die-cast top and bottom instrument covers used on the 4611 and 4612 are examples of the commitment to product reliability. Although more expensive than plastic or structural foam, the die castings offer several advantages that offset the extra cost. Internal heat rise is an important reliability factor. The power-supply heat-producing elements in the instruments are tied directly to the bottom casting. Because of the excellent heat conduction and radiation properties of aluminum, and the large area of the top and bottom covers, no cooling fan is required. Good electrical shielding, greater structural strength, and smaller size are other benefits derived from using aluminum castings.

Summary

The 4611 and 4612 Hard Copy Units employ unique electrostatic technology to produce sharp, high-contrast, permanent images of direct-view-storage tube, raster-scan, and other video displays. With their ease of operation and low copy cost, the 4611 and 4612 are ideal complements to the Tektronix 4630 Series of high image quality copiers.

Acknowledgements

Programmable Calibration Generator Speeds Instrument Checkout

Bob Oswald, project leader for the CG 551AP, joined Tek in 1974, feeling more at home with the lush greenery of western Oregon than with the desert beauty surrounding Scottsdale, Arizona. Bob received his B.S.E.E. from Michigan Technological University in 1964 and completed his M.S.E.E. in 1970 at Arizona State. He has worked on several TM 500 projects since joining Tek. In his leisure hours, Bob enjoys flying, woodworking, and silk-screen printing.

Electronic systems pervade our commercial, industrial and defense activities. Effective maintenance of these systems requires large numbers of skilled personnel and test equipment. However, the use of automated checkout procedures and equipment can substantially reduce the time required to maintain these electronic systems.

Programs are now underway in the armed services to extend automated checkout to maintenance of the test equipment, itself. The goal is to reduce the time and skill level required to verify calibration of test instruments used in large numbers.

The Tektronix CG 551AP Programmable Calibration Generator was developed to meet such a need. Designed primarily for oscilloscope calibration, it is also useful for checking other test instruments.

The CG 551AP packs all of the signals (except sine waves) needed to characterize oscilloscope performance, into one small, rugged package. Included are calibrated timing signals from five seconds to 0.4 nanoseconds, voltage amplitudes from 40 microvolts to 200 volts, current outputs from 1 milliamp to 100 milliamps, and fast, clean edges with risetimes of 200 picoseconds or less (using the Programmable Pulse Head accessory).

The CG 551AP is intended for use in a test system that uses the IEEE-488 General Purpose Interface Bus (GPIB) and a controller.

In a typical operation, the operator employs a program prepared for the particular oscilloscope under test. The program instructs the operator, via the controller display, how to set the oscilloscope controls. The controller then programs the CG 551AP (via the GPIB) to output the appropriate test signal to the oscilloscope. The CG 551AP display shows the parameters of the test signal selected. If the oscilloscope parameter being checked is not in perfect calibration, the operator manually adjusts a control on the CG 551AP's front panel so that the CG 551AP's output matches the oscilloscope's calibration. The percent of deviation from the standard, and whether the oscilloscope setting is slow, fast, low, or high, is displayed on the CG 551AP readout. The data from the CG 551AP's display and the CG 551AP's control settings can be sent (via the GPIB) to the controller and then to a hard copy unit to produce a permanent calibration record.

Microprocessor based control

The CG 551AP's system architecture is designed around the Motorola MC6800 microprocessor. The MC6800 was chosen because its capabilities best meet the requirements of the CG 551AP, and a family of support chips was available to handle the input/output, GPIB interface, and other elements of the design.

A block diagram of the central processing section of the CG 551AP is shown in figure 2. Firmware instructions for system operation occupy four kilobytes of read only memory (ROM). Eleven-bit addressability provides the capability of storing up to 8,192 instructions.

Temporary storage for programming operations is provided by one kilobyte of static random access memory (RAM). A smaller section of RAM (256 bytes) contains CG 551AP calibration constants, default values, and other data that need to be preserved when the instrument is powered down. A battery supplies power to this RAM during power down.

The microprocessor interfaces to the GPIB through an MC68488 general purpose interface adapter. Two kilobytes of ROM store instructions for the GPIB function.
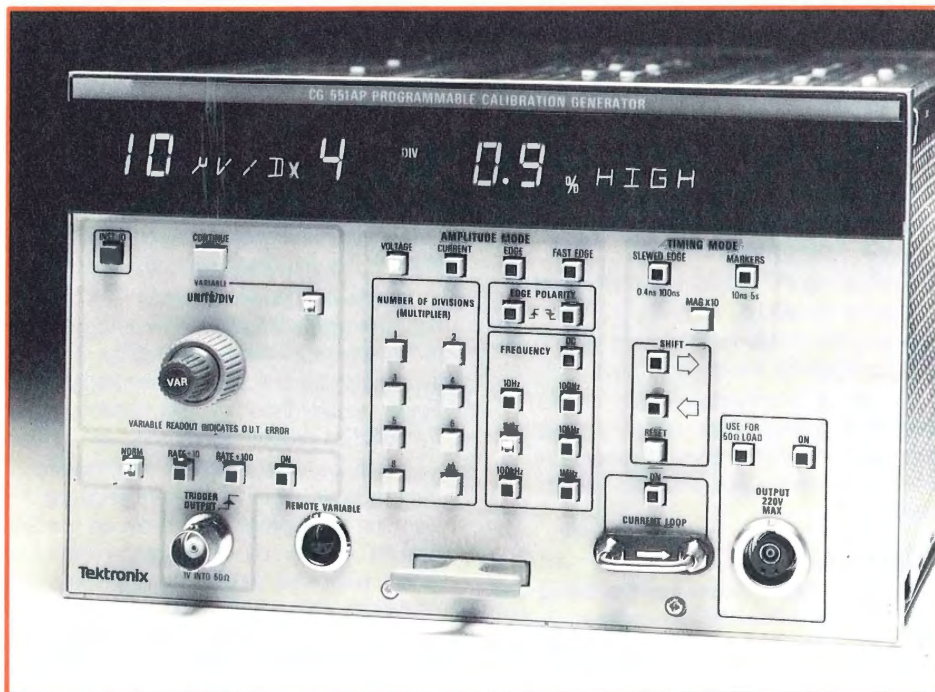

Fig. 1. The CG 551AP Programmable Calibration Generator provides six different types of signals useful in checking or calibrating oscilloscopes.
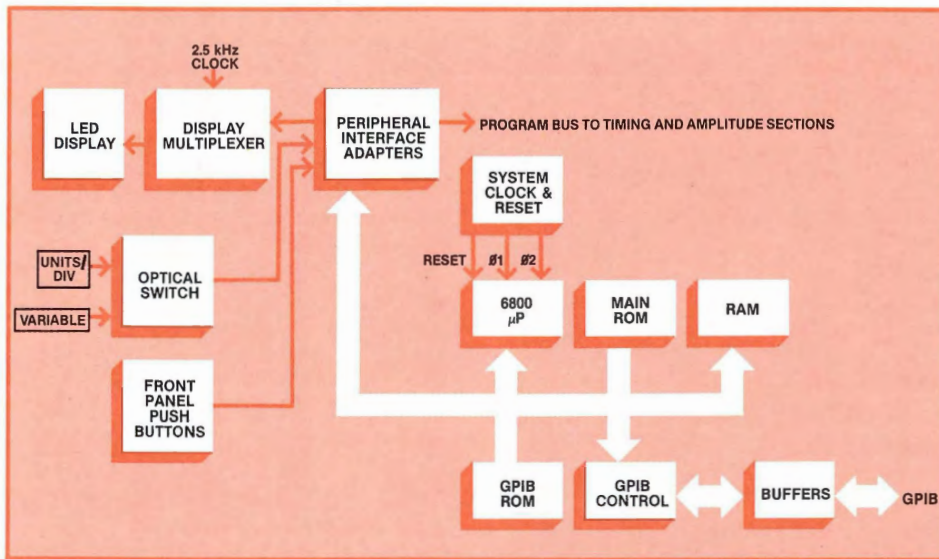
Fig. 2. Simplified block diagram of the central processor section of the CG 551AP. The CG 551AP is designed for use with a controller that communicates via the General Purpose Interface Bus.

Communication between the microprocessor and the CG 551AP front-panel controls is via an MC6821 peripheral interface adapter (PIA). Another MC6821 provides interface with the amplitude, edge, and timing circuits.

The front-panel TIME/DIV and VARIABLE controls use an optical switch to generate a Gray-code signal. (Gray-code is a binary code in which sequential numbers are represented by binary expressions, each of which differs from the preceding expression in one place only; for example, 0000, 0001, 0011, etc.). The optical switch contains two Gray-encoded discs. When the operator rotates either control, the slotted discs interrupt a light source that illuminates four photocells. Output from the photocells provide position information to the microprocessor, which thereby determines which control was turned and in which direction. As the control rotates, the microprocessor increments or decrements an internal firmware counter and programs the amplitude or timing section to produce the appropriate output.

When a front-panel control or push button is changed, or when a command is received via the GPIB to change the front-panel settings, the microprocessor responds by sending serial data from memory to control data registers in the timing and amplitude sections of the CG 551AP. The serial data in each data register is latched

to parallel output stages by high-level strobe signals. The latched data determines the characteristics of the output waveform to be generated by the CG 551AP.

Low noise generation a must

To produce clean, low-level amplitude signals and jitter-free high-speed timing signals requires a design that limits the extraneous noise coupled into the analog circuitry. Several CG 551AP design elements reflect this concern, specifically the use of:

- serial data transfer in the analog sections,
- a separate power supply for the central processing unit,
- shielding of amplitude section power supplies, and
- shielded, multicompartment, aluminum castings for the timing circuitry.

Powering up only the circuitry needed to perform a given function reduces power consumption, limits internal temperature rise, and eliminates potential sources of noise.

The timing circuitry

A simplified block diagram of the timing and amplitude circuitry is shown in figure 3. The main timing generator provides the timing signals for all modes of operation. The 100 MHz main VC0 output drives the time mark generator circuitry, while the 1-MHz reference oscillator serves the dual function of

reference frequency for the main VC0 and timing source for the chopping circuitry in the amplitude section.

The main VC0 operates at a nominal center frequency of 100 MHz and is phase-locked to the 1-MHz reference oscillator. The frequency of the main VC0 is changed in 100 kHz steps over a range of ± 9.9 percent by the front-panel VARIABLE control. The purpose of the main VC0 steering loop is to set the main VC0 to the correct harmonic of 100 kHz; once this is accomplished, the steering loop disconnects and the sampling loop takes over to keep the main VC0 on that harmonic.

Time markers covering the range from 10 ns to 5 seconds are derived from the 100 MHz main VC0 frequency by using countdown circuits. The markers are shaped to provide optimum resolution, with equal rise and fall times and a base width of about four percent of the period. When operating in the MAG X10 mode, every tenth marker is increased in amplitude for convenience in checking the timing and linearity of magnified sweeps. For checking fast sweeps, a technique called "slewed-edge" timing is used to generate timing signals from 0.4 nanoseconds to 100 nanoseconds. The slewed-edge technique is discussed in an article on page 14 .

The amplitude section

The standard amplitude calibrator (SAC) section of the CG 551AP provides voltage and current amplitude signals over a range of 40 microvolts to 200 volts and 1 milliamp to 100 milliamps, respectively. Pulses with clean, fast risetimes for checking oscilloscope vertical amplifier response also originate in the amplitude section.

Two floating power supplies — low voltage and high voltage — provide dc operating voltage for the SAC circuitry. Each supply can be enabled independently to power-up only those circuits needed for the function programmed.

A reference data register and floating data register accept and store serial data from the microprocessor, to set up the SAC circuits. A programmable voltage reference, which includes a multiplying digital-to-analog converter, converts a 10-bit digital signal to an equivalent dc analog voltage. This voltage is applied to a programmable precision resistive divider which provides a choice of eight voltage levels. The output of the divider goes to a level translator (not shown)
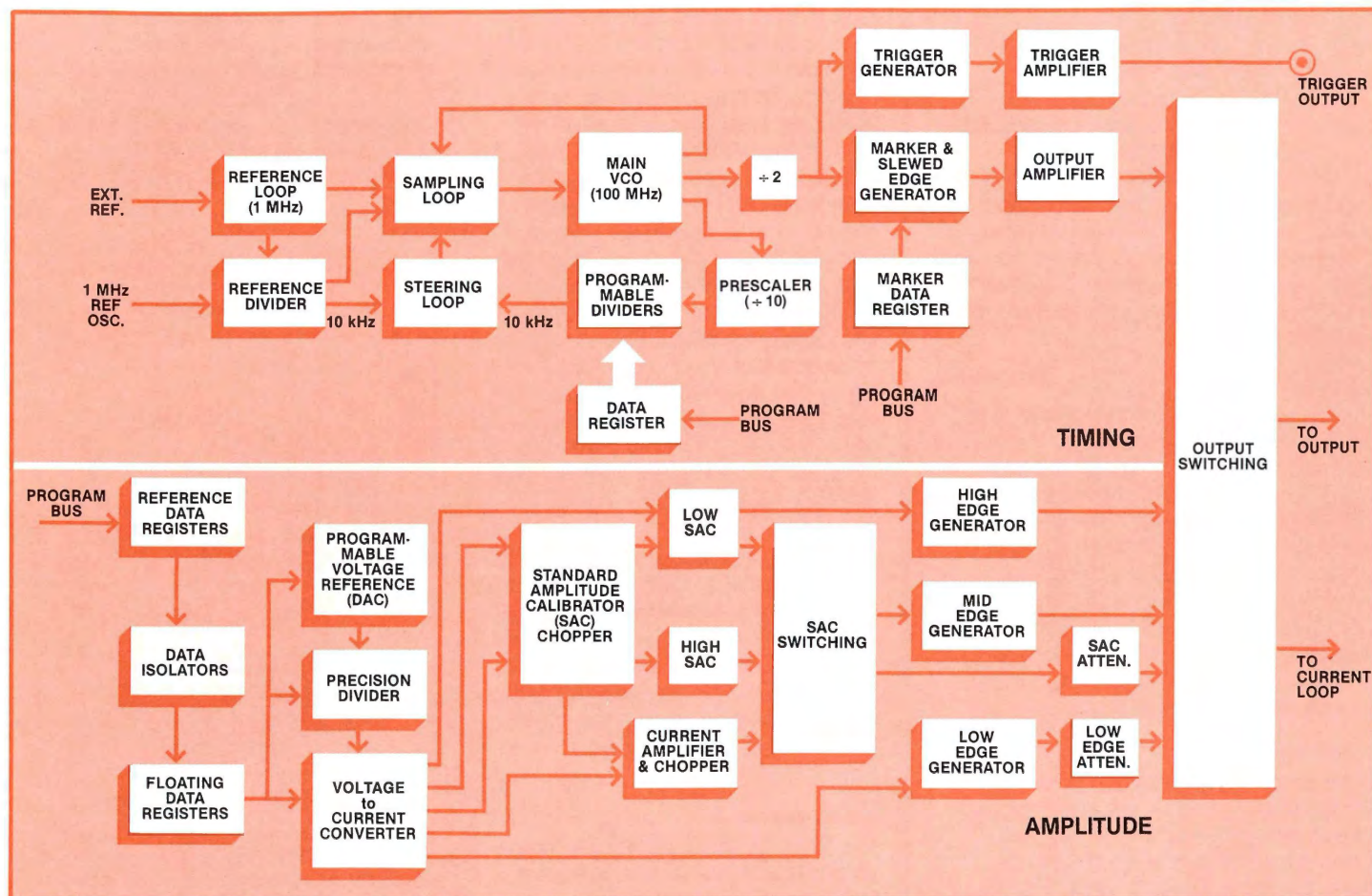
Fig. 3. Simplified block diagram of the timing and amplitude sections of the CG 551AP. Multiple output amplifiers maintain linearity and accuracy over a wide range of output amplitudes.

and a voltage-to-current converter, both programmed by the floating data registers. Two separate amplifiers — LOW SAC and HIGH SAC — are used to handle the wide range of output voltage available. The LOW SAC amplifier provides outputs in the 0.1 volt to 10 volt range, and the HIGH SAC covers the 10 volt to 200 volt range. A SAC attenuator provides precision attenuation of the signal to generate voltages from 80 millivolts to 40 microvolts.

Three separate amplifiers are used to cover the wide range of edge signals and maintain fast, clean outputs.

A single output connector

To make a programmable calibration system truly effective, all of the calibrated output signals from the calibration generator should be available at a single output connector. In the case of the CG 551AP, this task was no small undertaking. Output sig-

nal amplitudes range from 40 microvolts to 200 volts (necessitating a differential output and operator safeguards); timing signals range from 5 seconds to 0.4 nanoseconds; and aberration-free pulses with risetimes of 1.3 to 100 nanoseconds and amplitudes of 20 millivolts to 100 volts are available. (Pulse risetimes of less than 200 picoseconds are available using a programmable pulse head accessory that plugs into the output connector).

To handle this wide range of signals, a magnetic latching relay was designed which uses a contact structure similar to that developed for Tektronix cam switches. A matrix of these relays provide programmable switching of the various signals to the single output connector.

The output connector, itself, required considerable design effort. It provides a floating output for differential signals, supplies +10 volts and −10 volts for the

pulse head accessory, and meets safety requirements for the high-level signal outputs.

Programming the CG 551AP

Programming and remote control of the CG 551AP is accomplished via the GPIB. The CG 551AP can be both a talker and listener outputting data to, as well as receiving set-up instructions from, the GPIB controller.

All of the CG 551AP output functions are programmable using either high-level or low-level remote control messages. High-level messages are sent in ASCII and the CG 551AP responds in ASCII. Low-level messages begin with an ASCII control character followed by data in 8-bit binary bytes. Low-level commands require much less space in the controller's memory than do high-level commands. However, only the functions of changing the 13 basic settings and the setting query (SET?) are implemented in low-level language.

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Self test capabilities

To assure the operator that his calibration system is functioning properly, the CG 551AP performs extensive self-test routines. When power is applied, self-test routines check the internal memory, internal shift registers, conditions in the timing and amplitude sections, and calibration constants saved in the battery-maintained section of RAM. Almost eighty error codes are available for display on the CG 551AP's readout, to pinpoint circuit malfunctions or programming errors.

Summary

The CG 551AP can generate most of the signals needed to characterize an oscilloscope's performance. It is intended for use in a calibration system employing the IEEE-488 GPIB and a controller. The programmable signals are brought out to a single front-panel connector, greatly expediting the calibration function. The CG 551AP is designed to meet both commercial and military needs for a reliable, accurate, programmable calibration source for automated instrument checkout.

Slewed-Edge Signals Simplify Fast-Sweep Timing

Most modern oscilloscopes are designed for pulse-type applications. They are optimized to provide a clean transient response, solid triggering on pulse-type signals, and fast sweeps for resolving pulse timing relationships.

Typically, it is difficult to accurately calibrate the faster sweeps on oscilloscopes because of limitations imposed by the calibration signals available. Many calibration generators use a 1-megahertz, crystal-controlled oscillator as a reference frequency source. Frequency multipliers are then used to generate the higher frequency time marks, which are output as sine waves. Usually, the higher the output frequency, the lower the signal amplitude, and the more predominate the subharmonic content in the signal.

The vertical amplifier bandwidth of the oscilloscope being calibrated often can't pass these high-frequency sine waves, resulting in a very limited display amplitude of the calibration signal. The subharmonic distortion present in the test signal is magnified under these conditions, making accurate calibration even more difficult.

A new approach

The Tektronix CG 551AP Programmable Calibration Generator uses a different technique to generate fast timing signals. This slewed-edge technique uses the leading edges of fast-rise pulses as time markers.

The slewed-edge circuitry generates a series of paired pulses. The first pulse in each pair is the trigger pulse — the second is the slewed-edge pulse. The trigger pulse starts the oscilloscope's horizontal sweep. The circuitry then generates the slewed-edge pulse so that the leading edge of the pulse is displayed on the first vertical graticule line on the cathode ray tube (CRT). The pulse length is such that only the leading edge appears on screen.

After a period of time sufficient to let the sweep run and be reset, the circuit generates another trigger pulse. The next slewed-edge pulse is delayed so that it is displayed at the second vertical graticule line (one sweep division) on the CRT. On each subsequent sweep, the delay between the trigger and slewed-

edge pulse advances the displayed edge one sweep division. This procedure continues until a slewed edge is displayed for each sweep division (see figure 1). The slewed-edge pattern is repeated at a rate that produces a flicker-free display on the oscilloscope under test.
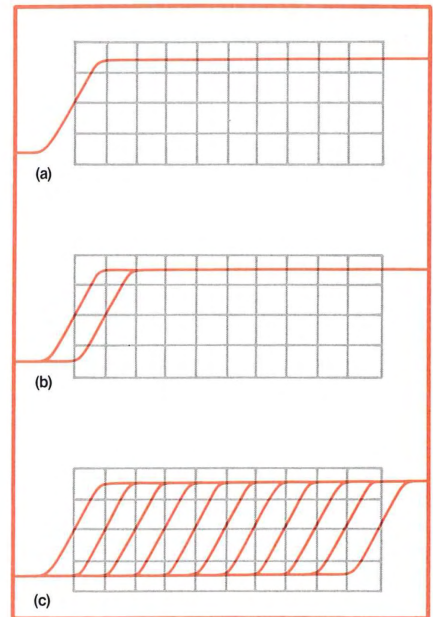

Fig. 1. A single slewed edge is displayed during each sweep. Subsequent slewed edges are delayed from the trigger pulse by linearly-increasing increments of time to produce a display similar to that shown in (c) above.

The slewed-edge circuits

A simplified block diagram of the slewed-edge circuit is shown at right. The generation of slewed edges requires two oscillators running at slightly different frequencies. A 100 MHz variable reference clock supplies timing for the circuit. The reference frequency is divided by two to obtain a trigger clock with a time period of 20 nanoseconds (50 MHz). An offset VCO, phase locked to the trigger clock timing source, generates a slewing clock with a time period of 20.5 nanoseconds (48.78 MHz).

The periods of both the trigger and slewing-edge clocks are divided further before the pulses are generated. The microprocessor calculates the divider values based on two requirements: the period between trigger pulses must be greater than the sum of the sweep run

and holdoff times (in the CG 551AP, maximum holdoff time is arbitrarily selected as 3500 nanoseconds); and the incremental delay time between the trigger and slewed-edge pulses must provide a spacing of one sweep division between each pair of displayed pulses. The time base setting to be calibrated determines what the delay between the trigger and slewed edge pulses should be. The trigger and slewed-edge dividers each contain two sets of values (or counts), referred to as initial and offset counts. The initial counts are used to generate only the first pair of trigger and slewed-edge pulses, and are usually calculated so the trigger and slewed-edge pulses are generated simultaneously.

The offset counts are used to generate all subsequent pairs of trigger and slewed-edge pulses, and are calculated to allow a delay of one sweep division between the displayed edges.

With a trigger clock period of 20 nanoseconds and a slewed-edge clock period of 20.5 nanoseconds, we have a 0.5 nanosecond time difference between the leading edges of the two clocks. If we count multiple cycles of both clocks we can select any multiple of 0.5 nanoseconds we desire. For example, four counts of the trigger clock equals 80 nanoseconds and four counts of the slewing clock equals 82 nanoseconds, for a difference of two nanoseconds. In selecting the initial counts, we must cal-

culate counts for the respective clocks that will result in a period of 3500 nanoseconds or longer and also result in time coincidence of the two clocks. Choosing an initial count of 205 for the trigger clock divider and 200 for the slewed clock divider results in coincident trigger and slewed pulses after 4100 nanoseconds (205 × 20 ns = 200 × 20.5 ns = 4100 ns).

If we want to generate a delay of two nanoseconds between the trigger and the slewed-edge pulses, the microprocessor must select offset counts of 209 for the trigger clock divider and 204 for the slewed-edge clock divider.

After the microprocessor selects the counts for the dividers, the sync signal starts the counters in the trigger and slewed-edge dividers at the instant when the trigger clock and slewing edge clock pulses are coincident. With the initial trigger divider count set at 205 and the slewed-edge divider count set at 200, the first trigger and slewed-edge pulses are generated simultaneously. Without stopping the counters, the control logic switches the dividers to the offset counts (209 and 204), which causes the second slewed edge to occur two nanoseconds after the second trigger pulse. Retaining the same offset counts increases the delay between the trigger and slewed-edge pulses by two nanoseconds on each sweep. That is, the third slewed edge is delayed four nano-

seconds after the third trigger pulse; the fourth slewed pulse is delayed six nanoseconds after the fourth trigger pulse, and so on.

The process continues until 15 slewed-edge markers have been generated. At this point, the edge counter directs the control logic to stop generating edges. When the control logic receives the next sync signal, the slewed-edge pattern is repeated, starting again with the initial counts of 205 and 200.

The shift feature

In an oscilloscope, there is an inherent delay between the trigger and the start of the sweep. A delay line is inserted in the vertical signal path to compensate for this delay. At the faster sweeps, the two delays usually do not match exactly. The result is that the slewed-edge pattern may appear to be shifted to the left or the right on the screen.

The CG 551AP has front-panel push buttons that allow you to shift the slewed-edge pattern to the left or right one sweep division at a time. Internally, the shift is accomplished by modifying the initial counts in the trigger and slewed-edge dividers to adjust the delay between the first trigger pulse and the first slewed-edge pulse. The shift capability is also useful when calibrating magnified sweeps.

Summary

The slewed-edge technique offers a convenient, precise method of calibrating the faster sweep speeds·typical of today's oscilloscopes. The slewed-edge signal may well become a standard feature on calibration generators of the future. ■
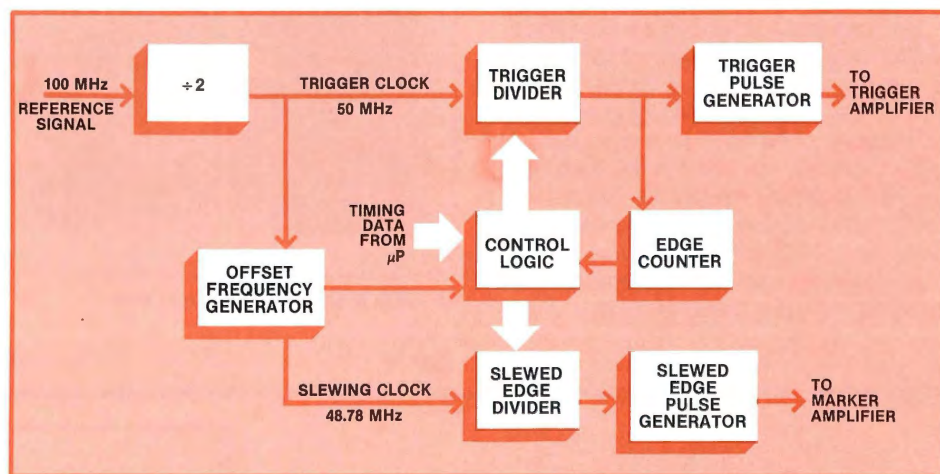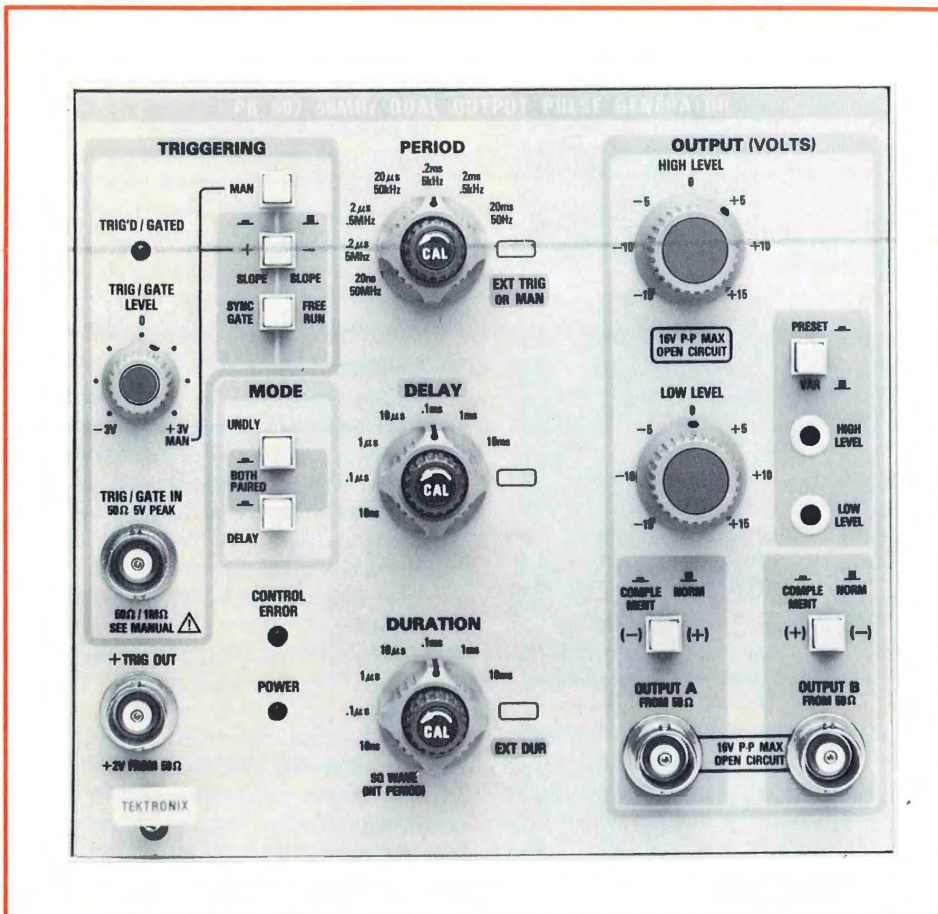

Fig. 2. Simplified block diagram of the slewed-edge circuitry. The outputs of two clocks running at slightly different frequencies are divided down to produce precise, short time intervals between the trigger and slewed-edge outputs.

New Products

A New Pulse Generator for the TM 500 Series

New High Performance Universal Counter/Timer

The new DC 509 Universal Counter/Timer is a microprocessor-based, dual-channel instrument that can perform single-shot time-interval measurements with 10-ns resolution. With measurement averaging, you can achieve 1-ps resolution.

The DC 509 performs eight measurement functions including frequency, period, ratio, width, time A to B, events B during A, time manual, and totalize.

Frequency measurements to 135 MHz are made on channel A using the powerful reciprocal counting technique, which provides high resolution measurement of low-frequency signals much more quickly than do conventional counting techniques. ■

PG 507 50-MHz Dual Output Pulse Generator

The PG 507 adds new capability to Tektronix' pulse generator line — simultaneous, normal or complementary dual pulse output at frequencies up to 50 MHz. Dual pulse outputs are useful in many applications, such as digital line driver simulation, control circuit testing, differential amplifier testing, and multiplexer design.

The PG 507 uses the versatile input and timing circuitry of the PG 508, and adds a second output in place of the variable rise/fall time capability. Output amplitude is adjustable up to 7.5 V p-p into 50 ohms and 15 V into an open circuit. High and low level output controls allow you to position the output pulses in ± 7.5 V and ± 15 V windows, respectively. Pulse risetime is 3.5 ns into 50 ohms.
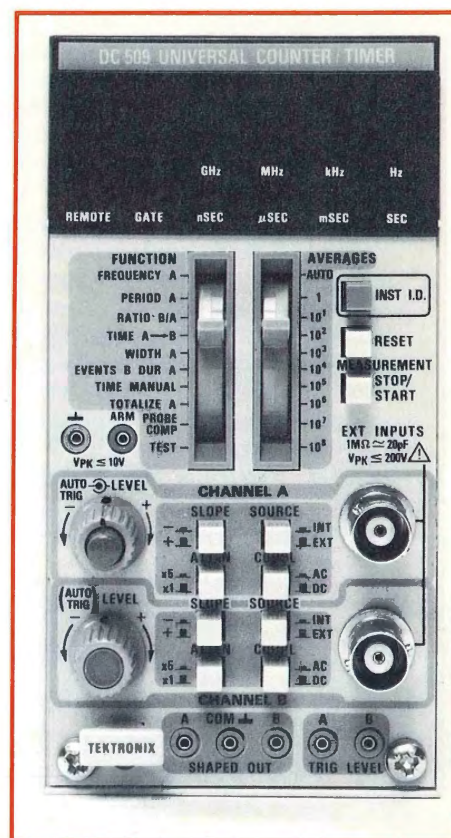
You can select pulse periods from 20 ns to 200 ms and pulse durations from 10 ns to 100 ms. Jitter is 0.1% + 50 ps. The PG 507 can be gated or triggered externally or manually, or be free run. A three-state trigger light tells you whether the input trigger level is above or below the TRIGGER/GATE LEVEL control setting, and flashes when the PG 507 is being triggered. It, thus, can serve as a logic probe as well as being an operating convenience. ■

DC 509 Universal Counter/Timer

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