



R6500 Microcomputer System DATA SHEET

ROM-RAM-I/O-COUNTER (RRIOC)

SYSTEM ABSTRACT

The ROM-RAM-I/O Counter (RRIOC), Part Number R6531, further enhances the cost-effectivity of the R6500 NMOS 8-bit microcomputer system by providing a powerful, flexible two-chip minimum system option. Produced with N-channel depletion load, silicon gate technology, the R6500 system employs advanced architecture, including 13 instruction addressing modes to achieve third generation performance speeds and smaller chips, the key to lower hardware and design costs. Included in the R6500 system are 10 software-compatible microprocessor (CPU) options, a growing number of memory and I/O devices, a very efficient, low-cost SYSTEM 65 development aid and complete documentation.

DESCRIPTION

The R6531 is primarily designed to provide innovative Equipment Designers with a wide span of two-chip minimum systems in combination with the R6500 family of 10 CPUs. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package — see Table 1. Both versions contain a 2048 x 8 mask-programmable ROM, a 128 x 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupt inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available to provide a RAM standby power pin and chip selects for multi-chip systems — see Figure 1.

Prototyping circuits are available in both the 40- and 52-pin packages, and in 1- and 2-MHz versions. They are offered as part numbers R6531-098 and R6531-098A for the 40-pin part, and as part numbers R6531-099 and R6531-099A for the 52-pin part.

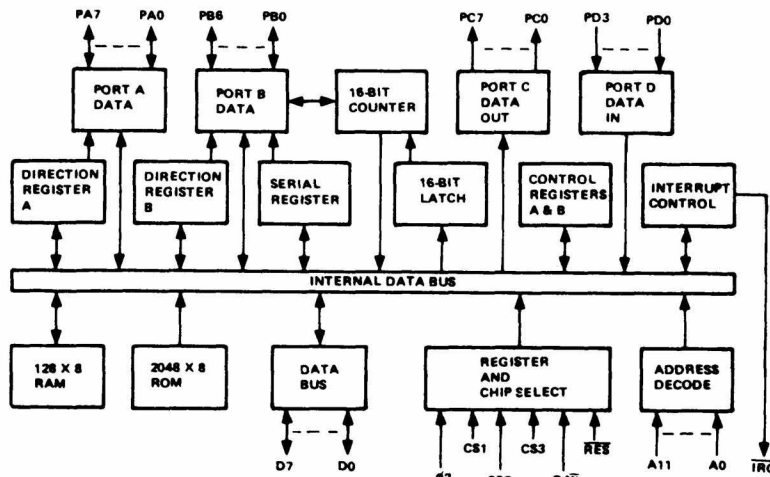
FEATURES

- 2048 x 8 mask programmable ROM
- 128 x 8 static RAM
- 16-bit multi-mode counter/latch
 - interval timer (one shot or free running)
 - pulse generator (one shot or free running)
 - event counter
 - external trigger
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports — 40 pin package)
- Expansion 8-bit output port and 4-bit input port (52 pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 2 MHz or 1 MHz operation
- Single +5V power supply

Table 1 Ordering Information

| | | |
|---------------------|--------------------|---------------------------------|
| Order Number: R6531 | Temperature Range: | No suffix = 0°C to +70°C |
| | | E = -40°C to +85°C (Industrial) |
| | Package: | C = 40-Pin DIP, Ceramic |
| | | P = 40-Pin DIP, Plastic |
| | | Q = 52-Pin QUIP, Plastic |
| | Frequency Range: | No suffix = 1 MHz |
| | | A = 2 MHz |

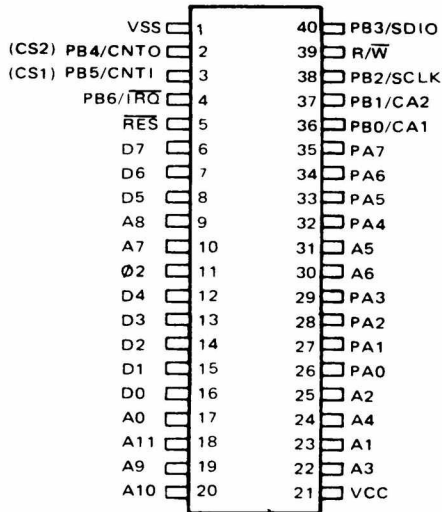
NOTE: Contact your local Rockwell representative for availability.



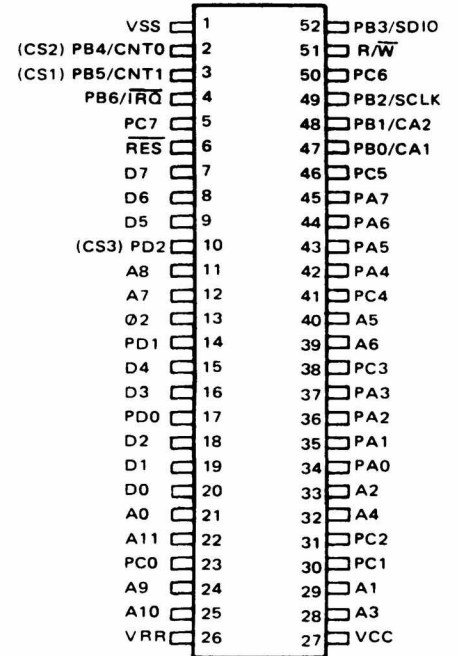
R6531 Block Diagram

R6500
MEMORY I/O
COMBOS

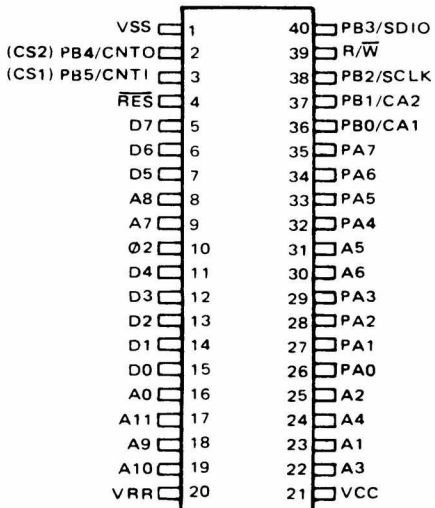
R6500
MEMORY I/O
COMBOS



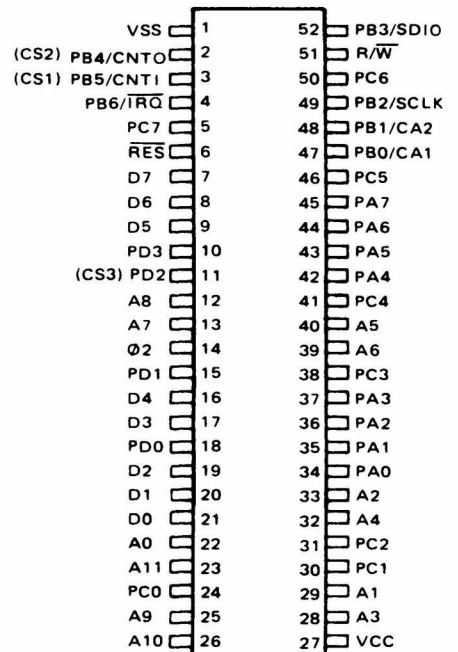
40-Pin Configuration
R6531, PB6 Option



52-Pin Configuration
R6531Q, VRR Option



40-Pin Configuration
R6531, VRR Option



52-Pin Configuration
R6531Q, PD3 Option

Figure 1. R6531 Pin Configuration Options

INTERFACE SIGNALS

RESET (RES)

This active low signal is used to initialize the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The RES signal must be low for at least four clock periods when reset is required.

ADDRESS BUS (A0-A11) AND CHIP SELECTS (CS1-CS3)

Memory and register selection is accomplished using the 12 address lines and, in multiple device systems, also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

DATA BUS (D0-D7)

The R6531 has eight data bus lines, which allow data to be transferred to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

READ/WRITE (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6531. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the R/W pin allows a write (with proper addressing) to the R6531.

PERIPHERAL DATA PORTS (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3)

Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 7-bit port, PB0-PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only port, PC0-PC7, and a 4-bit input only port, PD0-PD3. PD2 and PD3 may be assigned other functions as described herein.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the drivers float. If PB6 is programmed as the IRQ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of IRQ from other devices.

RAM RETENTION VOLTAGE (VRR)

A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselects RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.

INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531's, ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are:

| R6531 Function | Chip Selects | | | Address Inputs (A0-A11) | | | | | | | | | | | |
|----------------|--------------|-----|-----|-------------------------|---------------|---|---|---|----------------|---|---|---|---|------------|---|
| | CS3 | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROM | X | X | X | X | 2K ROM Decode | | | | | | | | | | |
| RAM | Y | Y | Y | Y | Y | Y | Y | Y | 128 RAM Decode | | | | | | |
| I/O | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | I/O Decode | |

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

ROM - 2K BYTES (16K BITS)

The 16K ROM is a 2048 x 8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

RAM - 128 BYTES (1024 BITS)

The 128 x 8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

R6531 40 PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-098 (1 MHz) and R6531-098A (2 MHz) are packaged in a 40-pin dual in-line package that has the same pinouts as the 40-pin R6531 with PB6 option. In this prototyping circuit, the ROM is disabled and there is no VRR option.

Access codes for this prototyping circuit are shown in the table below.

| R6531-098 Function | Chip Selects | | Address Inputs (A0 - A11) | | | | | | | | | | | |
|--------------------|--------------|-----|---------------------------|----|---|---|---|----------------|---|---|------------|---|---|---|
| | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM | N | N | L | L | L | N | L | 128 RAM Decode | | | | | | |
| I/O | N | N | L | H | H | H | L | L | L | L | I/O Decode | | | |

In the above table, N means No Effect, H means High (2.0 volts or greater) and L means Low (0.8 volt or less).

R6531 52-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-099 (1 MHz) and R6531-099A (2 MHz) are packaged in the 52-pin quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines.

Access codes for the prototyping circuit are shown in the table below.

| R6531-099 Function | Chip Selects | | | Address Inputs (A0-A11) | | | | | | | | | | | |
|--------------------|--------------|-----|-----|-------------------------|---------------|---|---|---|----------------|---|------------|---|---|---|---|
| | CS3 | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROM | H | N | N | H | 2K ROM Decode | | | | | | | | | | |
| RAM | L | N | N | L | L | L | N | L | 128 RAM Decode | | | | | | |
| I/O | L | N | N | L | H | H | H | L | L | L | I/O Decode | | | | |

The 128 words of RAM have been mapped into the first half of both Page 0 and Page 1, to accommodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

INPUT/OUTPUT

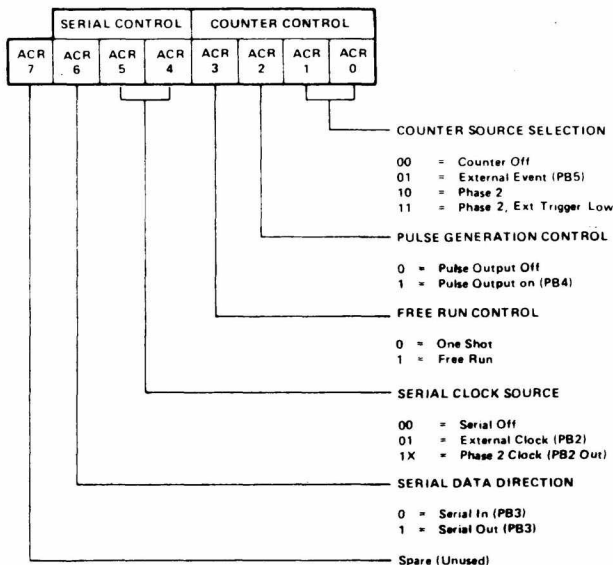
The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system. The addresses of the 15 internal peripheral registers are:

| A3 | A2 | A1 | A0 | Register |
|----|----|----|----|---|
| 0 | 0 | 0 | 0 | Port A |
| 0 | 0 | 0 | 1 | Port B |
| 0 | 0 | 1 | 0 | Port C (write only) |
| 0 | 0 | 1 | 1 | Port D (read only) |
| 0 | 1 | 0 | 0 | Read Lower Counter/Write Lower Latch |
| 0 | 1 | 0 | 1 | Read Upper Counter/Write Upper Latch and Download |
| 0 | 1 | 1 | 0 | Write Lower Latch |
| 0 | 1 | 1 | 1 | Write Upper Latch |
| 1 | 0 | 0 | 0 | Serial Data Register |
| 1 | 0 | 0 | 1 | Interrupt Flag Register |
| 1 | 0 | 1 | 0 | Interrupt Enable Register |
| 1 | 0 | 1 | 1 | Auxiliary Control Register |
| 1 | 1 | 0 | 0 | Peripheral Control Register |
| 1 | 1 | 0 | 1 | * Data Direction Register - Port A |
| 1 | 1 | 1 | 0 | * Data Direction Register - Port B |

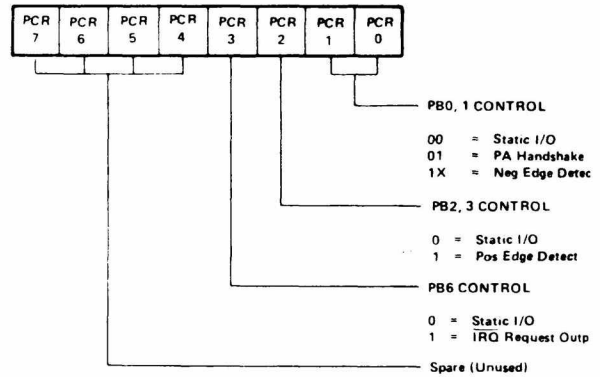
* Write Only

CONTROL REGISTERS

Two control registers, Peripheral Control and Auxiliary Control, are provided for software selection of various I/O functions. The Peripheral Control Register is primarily associated with Port B functions and the Auxiliary Control Register is associated with the counter and serial data functions which also affect Port B. The register bit assignments are:



Auxiliary Control Register (ACR)



Peripheral Control Register (PCR)

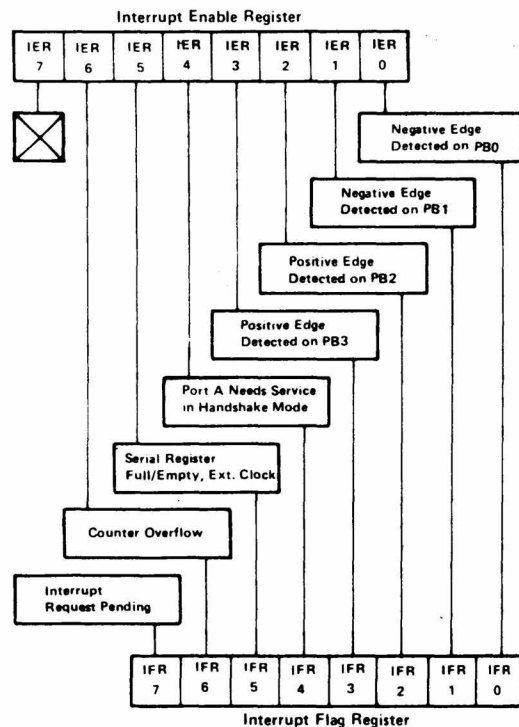
INTERRUPT ENABLE AND FLAG REGISTERS

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an IRQ Request Output, then PB6 will be set low to request the R6531 CPU to service IRQ.

The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in the bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 or writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are:



PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register – Port A (DDRA). Each line of the 7-bit data Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A “1” written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A “0” written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a “1” loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a “0” had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction – the Control Registers have no effect on data direction.

The 8-bit data Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

MULTI-MODE COUNTER/LATCH

The R6531 contains a 16-bit counter with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decremting counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 – Counter Off

Mode 1 – Event Counter – counts external event inputs (negative transitions) at PB5

Mode 2 – Interval Timer – counts \emptyset 2 system clock pulses.

Mode 3 – External Trigger – counts \emptyset 2 system clock pulses starting with a negative transition on PB5.

Mode Modifier A – Pulse Generation Control – causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B – Free Run Control – causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system \emptyset 2 clock rate. If the external clock is used, data may be shifted at any rate up to one half the system \emptyset 2 clock rate. In the external clock mode, the counter may be operated in the free run pulse generator mode using the CNT0 line externally connected to the SCLK line to provide the desired shift rate.

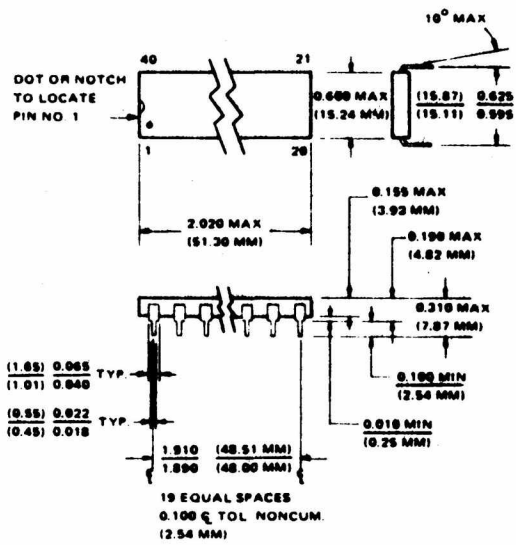
Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out, most significant bit first, under control of the shift clock

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.

HANDSHAKE OPERATIONS

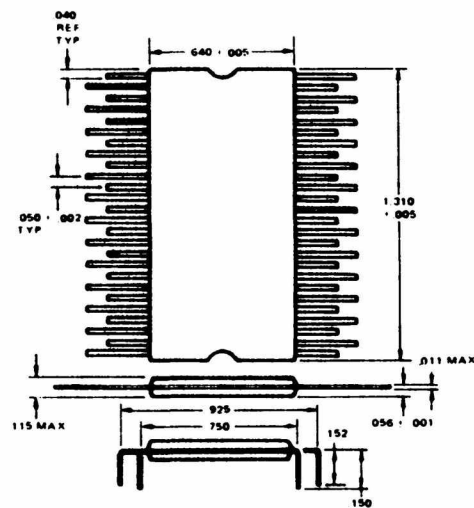
PB0 and PB1 may be used as handshake control lines for data transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.

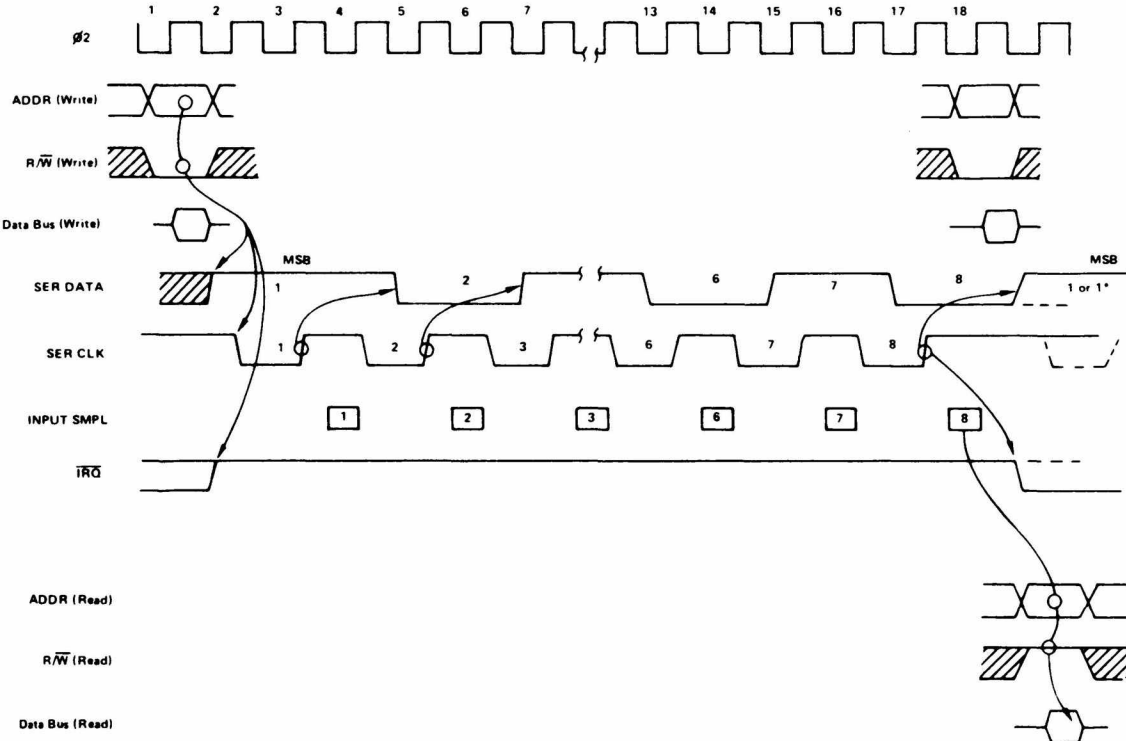


NOTE Pin No. 1 is in lower left corner when symbolization is in normal orientation

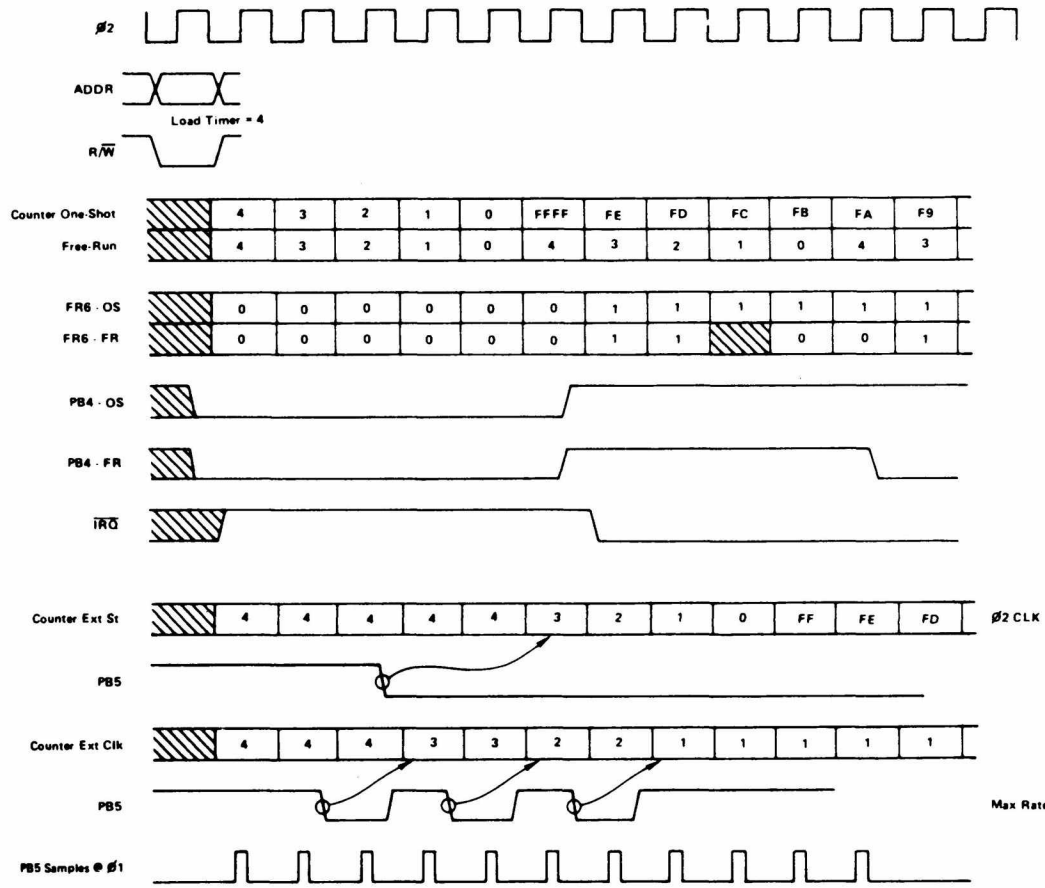
40-Pin Packaging Diagram



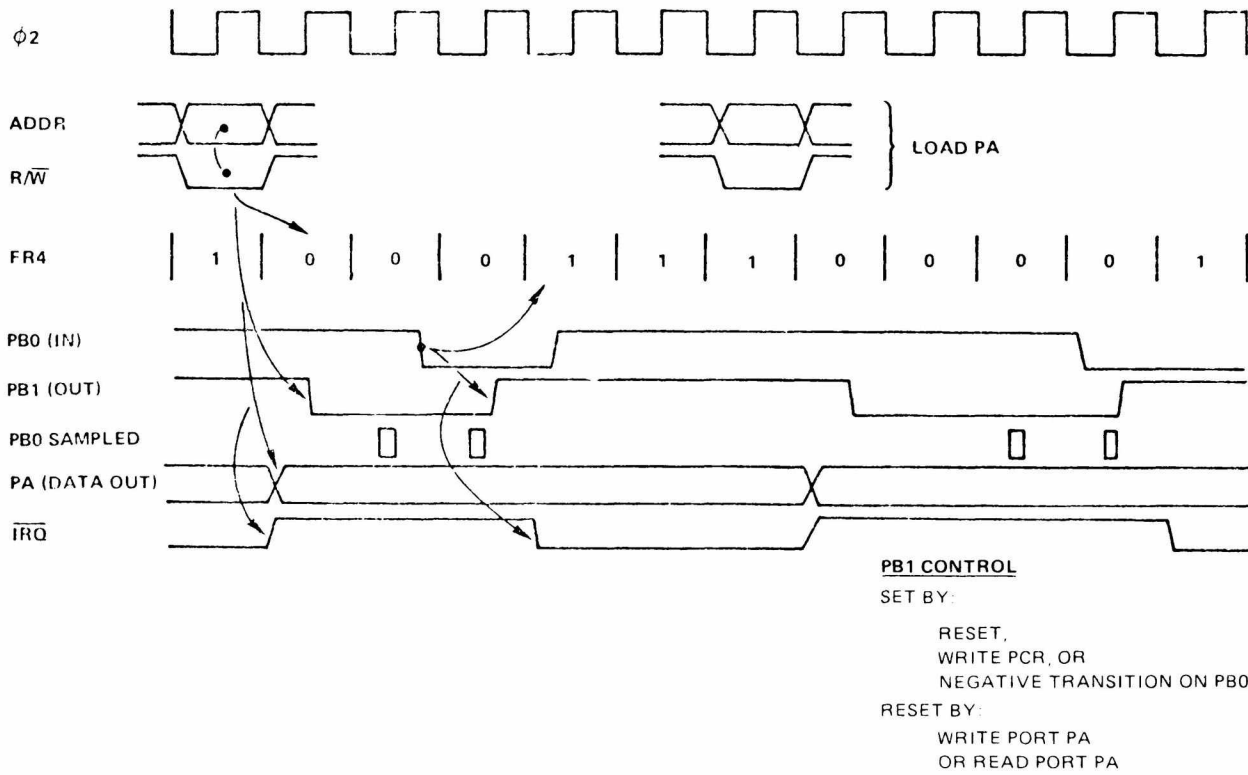
52-Pin Packaging Diagram



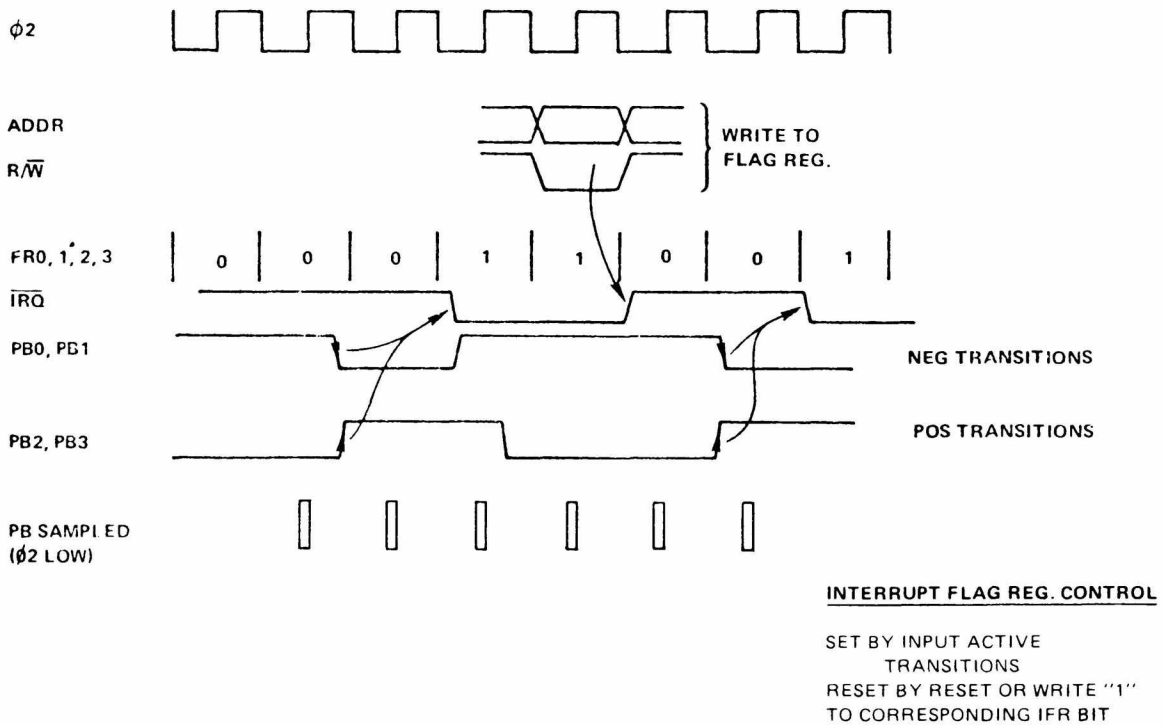
R6531 Serial Timing



R6531 Counter/Timer Timing



R6531 Timing for Handshake Mode



R6531 Timing for Interrupt Mode

Write Timing Characteristics

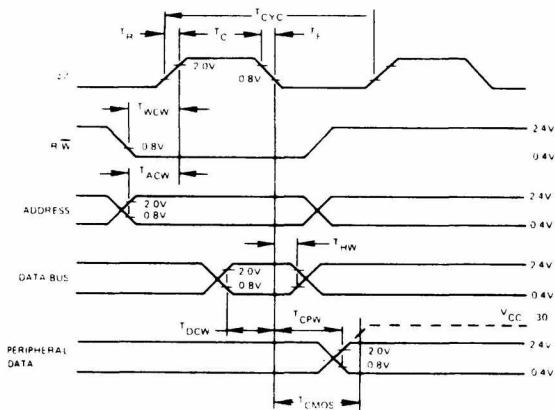
| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|--|------------|-------|-----|-------|-----|---------|
| | | Min | Max | Min | Max | |
| Clock Period | T_{CYC} | 1 | 10 | 0.5 | 10 | μs |
| Rise & Fall Times | T_R, T_F | | 25 | | 15 | ns |
| Clock Pulse Width | T_C | 470 | | 235 | | ns |
| R/\bar{W} valid before positive transition of clock | T_{WCW} | 180 | | 120 | | ns |
| Address valid before positive transition of clock | T_{ACW} | 180 | | 120 | | ns |
| Data Bus valid before negative transition of clock | T_{DCW} | 270 | | 135 | | ns |
| Data Bus Hold Time | T_{HW} | 10 | | 10 | | ns |
| Peripheral data valid after negative transition of clock | T_{CPW} | | 900 | | 450 | ns |



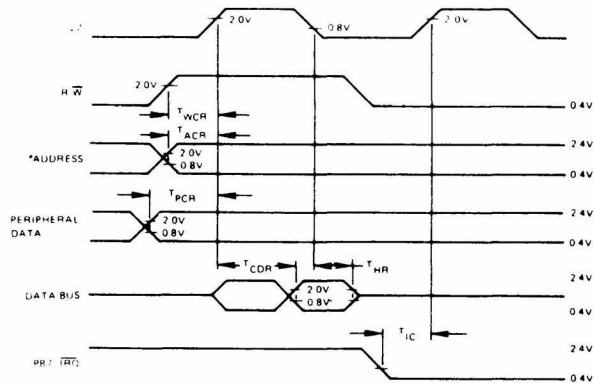
Read Timing Characteristics

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|-----------|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | |
| R/\bar{W} valid before positive transition of clock | T_{WCR} | 180 | | 120 | | ns |
| Address valid before positive transition of clock | T_{ACR} | 180 | | 120 | | ns |
| Peripheral data valid before positive transition of clock | T_{PCR} | 270 | | 135 | | ns |
| Data Bus valid after positive transition of clock | T_{CDR} | | 350 | | 180 | ns |
| Data Bus Hold Time | T_{HR} | 10 | | 10 | | ns |
| IRQ valid after negative transition of clock | T_{IC} | | 900 | | 450 | ns |

Loading = 100 pF + 1 TTL load for PA0-PA7, PB0-PB6, PC0-PC7
 = 100 pF + 1 TTL load for D0-D7 (R6531A)
 = 130 pF + 1 TTL load for D0-D7 (R6531)



Write Timing Characteristics



Read Timing Characteristics

SPECIFICATIONS

Maximum Ratings

| Rating | Symbol | Value | Unit |
|-----------------------------|-----------|--------------|-------------|
| Supply Voltage | V_{CC} | -0.3 to +7.0 | Vdc |
| Input Voltage | V_{in} | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | T | | $^{\circ}C$ |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Storage Temperature Range | T_{stg} | -55 to +150 | $^{\circ}C$ |

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

Electrical Characteristics

($V_{CC} = 5V \pm 10\%$ for R6531, $V_{CC} = 5V \pm 5\%$ for R6531A)

| Characteristic | Symbol | Min | Max | Unit |
|--|-----------|----------------|----------------|---------|
| Input High Voltage | V_{IH} | 2.0 | V_{CC} | V |
| Input Low Voltage | V_{IL} | -0.3 | +0.8 | V |
| Input Leakage Current; $V_{IN} = V_{SS} + 5V$, $V_{CC} = +5V$ A0-A11, CS1-CS3 R/W, RES, $\phi 2$, PD0-PD3 | I_{IN} | | 2.5 | μA |
| Leakage Current for High Impedance State, $V_{CC} = +5V$ (Three State); $V_{IN} = 0.4V$ to $2.4V$; D0-D7, PA0-PA7, PB0-PB6 | I_{TSI} | | ± 10.0 | μA |
| Output High Voltage $V_{CC} = MIN$, $I_{LOAD} \leq -200 \mu A$ (PA0-PA7, PB-PB6, D0-D7) | V_{OH} | $V_{SS} + 2.4$ | | V |
| Output Low Voltage $V_{CC} = MIN$, $I_{LOAD} \leq 2.1 mA$ | V_{OL} | | $V_{SS} + 0.4$ | V |
| Output High Current (Sourcing); $V_{OH} \geq 2.4V$ (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3, D0-D7) | I_{OH} | -200 | | μA |
| Output Low Current (Sinking); $V_{OL} \leq 0.4V$ (PA0-PA7) (PB0-PB6) (PC0-PC7) | I_{OL} | 2.1 | | mA |
| Clock Input Capacitance, $V_{CC} = 5V$ | C_{Clk} | | 20 | pF |
| Input Capacitance, $V_{CC} = 5V$ | C_{IN} | | 10 | pF |
| Output Capacitance, $V_{CC} = 5V$, chip deselected | C_{OUT} | | 10 | pF |
| Power Dissipation | P_D | | 1.0 | W |

*When programmed as address pins

All values are D.C. readings