NBSIR 73-309

RANDOM SAMPLING OSCILLOSCOPE TIME BASE

James R. Andrews

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Final Report

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U.S. DEPARTMENT OF COMMERCE, Frederick B. Dent, Secretary

NATIONAL BUREAU OF STANDARDS, Richard W. Roberts, Director

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ABSTRACT

With the advent of new miniaturized mercury (Hg) switches with reputed transition times of the order of 10 picoseconds, interest has been rekindled in their use in high speed pulse measurements. Since there is no pre-trigger signal available from a Hg switch, normal sequential sampling techniques are not usable to measure the fast Hg switch transition time. For this reason a new random sampling time base unit was designed to perform these measurements at the low repetition rate of Hg switches (< 100 Hz). The time base may be used with commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using its time magnifier, the fastest sweep rate is 10 ps/cm. A variable trigger lead time control is provided. The trigger sensitivity is 10 mV. The long term timing stability of the time base is excellent with less than 15 ps/h drift.

Key words: Mercury switch; oscilloscope; picosecond; pulse; random sampling; risetime; sampling; time base; transition time.

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1. INTRODUCTION

This is the final report on CCG project 72-67. The objective of this project was to construct a working model sampling system using a commercial 20 ps transition time, 50 ohm feed thru sampling head and NBS developed random sampling time base circuitry such that low repetition rate, fast risetime pulses can be sampled and displayed on a realtime oscilloscope. This final report provides engineering drawings, specifications, and operating instructions.

With the advent of new miniaturized mercury (Hg) switches with reputed transition times of the order of 10 picoseconds [1], interest has arisen in their use in high speed pulse measurements. However, it is not possible to directly observe the electrical closure of these miniature switches with the widest bandwidth (DC-18 GHz) sampling oscilloscope available. The problem is that due to the mechanical nature of the mercury switch there is no pre-trigger information available to initiate the oscilloscope timing circuits.

To observe signals that can not be triggered with precision or that do not furnish a pre-trigger, the classical technique [2] is to introduce a coaxial cable delay line in the oscilloscope vertical channel to obtain the necessary (35-70 ns) pre-trigger lead time, figure 1-1. Using ordinary high quality coaxial cable the delay line becomes the dominant band-limiting component in this measurement system. The

system 10%-90% transition time will be limited to 150 ps or slower. Thus, an ordinary signal delay line would not provide an acceptable solution as it would distort the closure waveform.

An alternative method is to use a different horizontal timing measurement method called random sampling [3]. In random sampling the vertical sampler is allowed to sample the input signal in a random fashion with no synchronization between the input signal and the sampling rate. The time base measures the time interval between the point of occurrence of the input trigger (usually the input signal of interest) and the point of occurrence of a vertical sample. This time interval may be positive or negative. If it is negative then the vertical sample was taken before the trigger occurred. With random sampling it is possible to make measurements ahead of the trigger. Thus the delay line in the vertical channel is no longer necessary. The major disadvantage of random sampling as compared to sequential sampling is the longer data acquistion time to obtain sufficient samples to adequately represent the input signal. This is due to the low probability of a vertical sample occurring within the narrow time window of interest that is centered on the trigger signal.

For the above reasons the new random sampling time base shown in figure 1-2 was designed to perform these measurements

at the low repetition rate of mercury switches (< 100 Hz). The time base may be used with commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using its time magnifier, the fastest sweep rate is 10 ps/cm. A variable lead time control is provided. The trigger sensitivity is 10 mV. It also includes a phase-locked oscillator to predict the point in time at which the next signal will occur. The long term timing stability of the time base is excellent (drift < 15 ps/h).

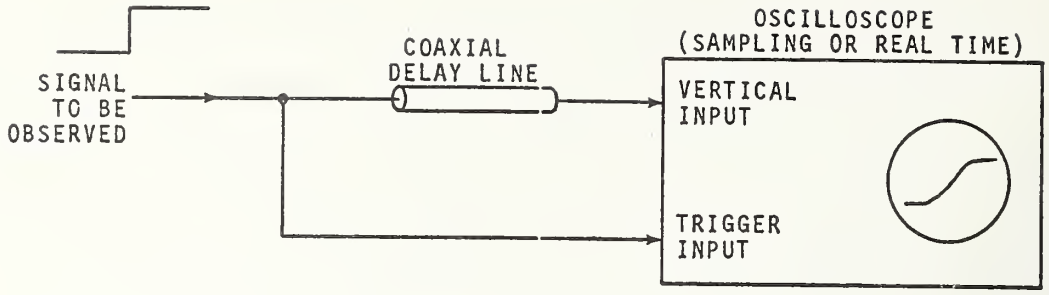


Figure 1-1. Classical technique to measure signals that do not furnish a pretrigger.

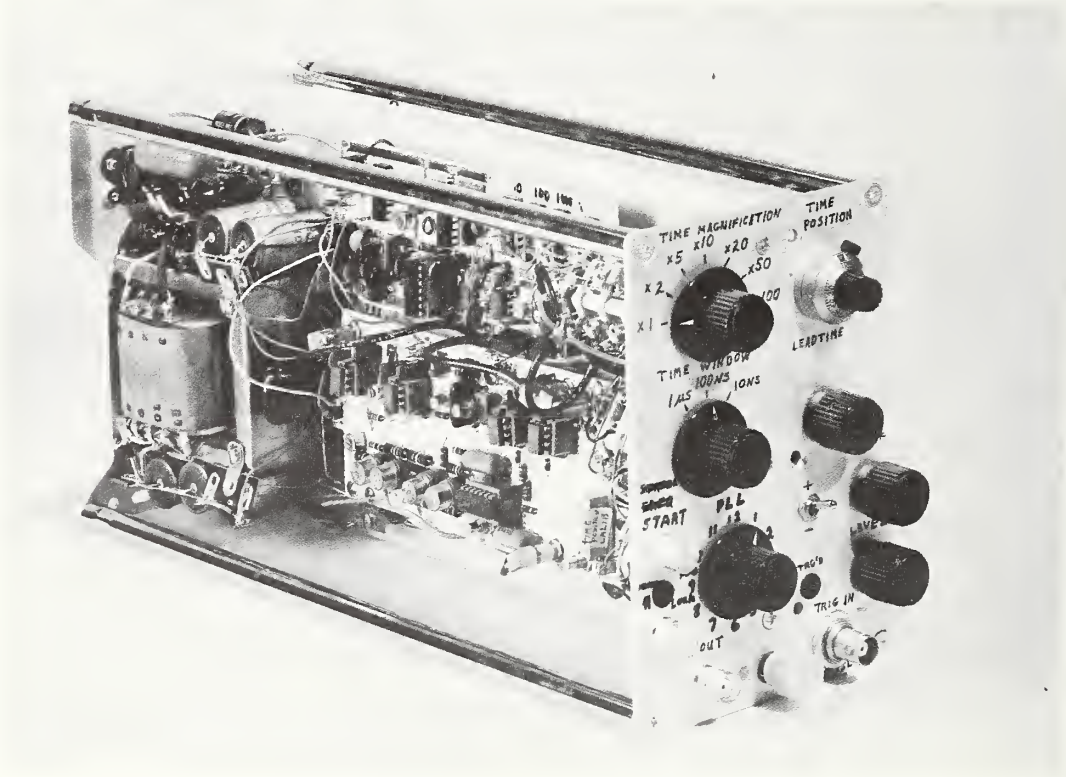


Figure 1-2. Random sampling oscilloscope time base plug-in.

2. PRINCIPLES OF RANDOM SAMPLING

The basic principle of random sampling is demonstrated in figures 2-1 and 2-2. Consider that we are interested in observing a time window t_w framed around an input signal. The point in time at which the input signal is of sufficient amplitude to cause a trigger recognition is at $t = t_o$. However we are interested in also observing the signal ahead of t_o for a time t_{LT}, the trigger lead time. The random sampling scheme provides a means of obtaining this lead time.

At the instant (t_o) a trigger is recognized, a step pulse called START is generated. The START pulse is applied to the linear timing ramp and it allows the RAMP voltage to begin its run-up. Meanwhile a free-running oscillator has been generating a train of STROBE pulses that are completely unsynchronized with the input signal repetition rate. Thus the occurrence of a STROBE pulse within the time window of interest (t_w) is a purely random coincidence. The STROBE pulse is the command to the vertical sampling gate to take a sample of the input signal. Assume now that indeed a STROBE has occurred at time t_1 within the time window and before the trigger recognition. The vertical channel now has a valid data point in the region of interest. Now introduce a fixed delay of length t_{LT} between the occurrence of the STROBE pulse and the generation of a STOP pulse. This delay is chosen to be sufficient to allow the STOP (t_1) pulse,

associated with the STROBE at t_1, to arrive at the timing RAMP after it has started its runup at t_o. The STOP pulse terminates the RAMP runup at whatever level it has achieved at the time of the occurrence of the STOP pulse. The stopped RAMP voltage level $V_R(t_i)$ is thus proportional to the instant in time (t_i) at which a vertical sample was taken. The timing ramp is thus a time to amplitude converter. The only item necessary after the ramp is a voltmeter to measure $V_R(t_i)$ and apply it after suitable low frequency amplification to the horizontal deflection plates of the display CRT. The cycle may now be repeated with another randomly occurring coincidence between the signal and the STROBE, say at t_2, again within the time window but after t_o. If for this event $t_2 > t_1$, the STOP (t_2) occurs later in time, but still a fixed delay t_{LT} after STROBE-signal coincidence at t_2. Thus the RAMP is allowed to run up to a much larger voltage $V_r(t_2)$. The process is allowed to repeat many times until sufficient data is obtained to permit a relatively complete representation of the input signal. Due to the randomness of the STROBE-signal coincidence, many data points will not be within the window of interest (such as t_3).

The major difference between the classical technique, figure 1-1, and the random sampling technique, figure 2-2, is the location of the time delay element. In the classical technique, the time delay element is inserted in the input

signal channel. It was shown earlier that this distorts the signal and restricts the system bandwidth.

With random sampling the delay element has been moved into the horizontal timing circuit (see fixed stop delay t_{LT}). This eliminates the signal distortion due to the delay line in the vertical channel and allows the full bandwidth capabilities of the sampling head to be utilized. The requirements on the delay element in the time base are much less stringent. The signals within the time base are digital logic signals. It is not necessary to preserve with fidelity their wave shape during transmission through the delay element. The only requirement is that the time delay introduced by the delay element be stable and free from any jitter. A coaxial delay line could be used. However an electronic circuit is used instead as this allows easy variation of the time delay (t_{LT}) with a dc control voltage.

However, there are some disadvantages. Random sampling is like everything else in actual practice, i.e. compromises and trade-offs must be made. The major disadvantage of random sampling as compared to sequential sampling is the longer data acquisition time to obtain sufficient samples to adequately represent the input signal. The probability of a coincidence within the time window of the free-running STROBE and the input signal is quite low particularly if the time window is narrow (for example, 100 ps) and the signal repetition rate is low (for example 50 Hz). For this reason a

prediction circuit is included in the time base. The function of this circuit is to measure the incoming signal frequency and then program the STROBE to occur within the time window (t_w) when the next input signal is predicted to occur.

However for mercury switches which have very large period jitters of typically 0.2 ms, random sampling data acquisition runs of several hours are not uncommon. This thus imposes very stringent long term stability requirements on the time base.

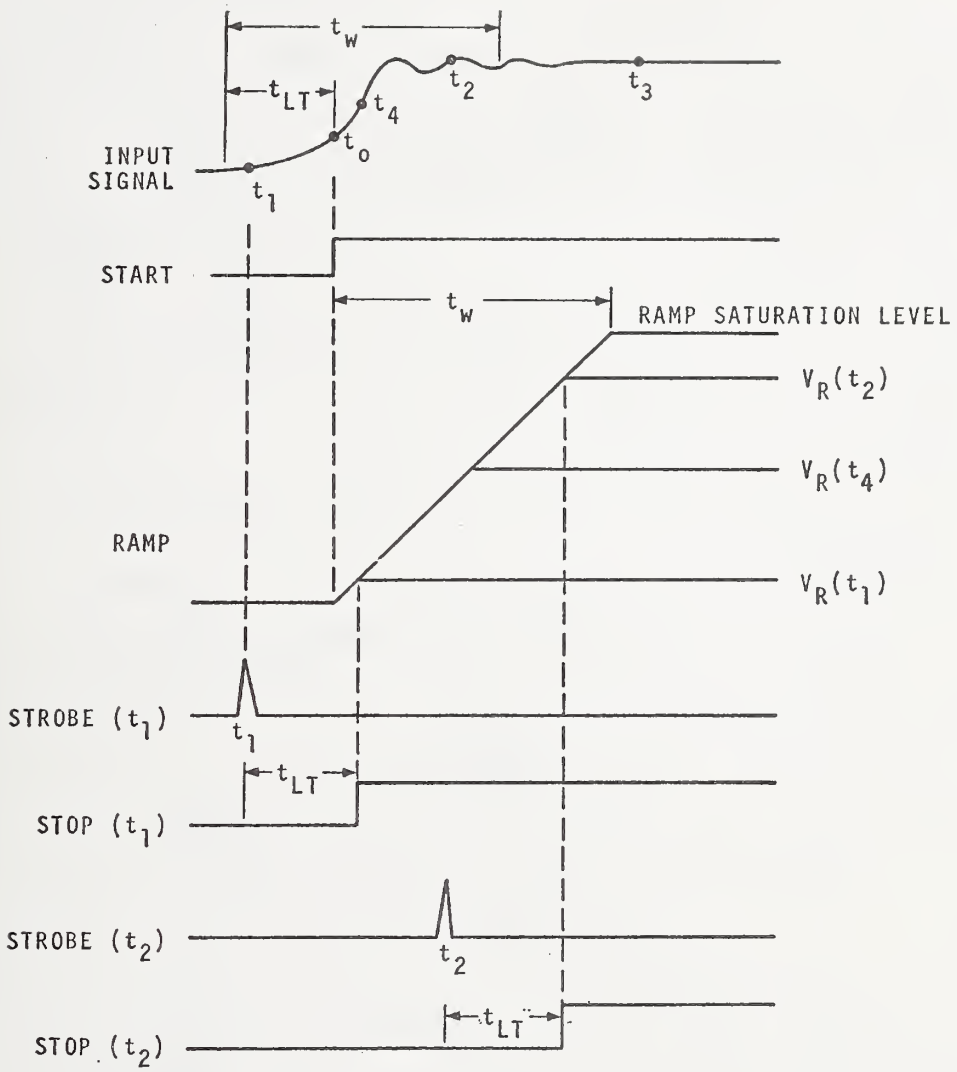


Figure 2-1. Basic random sampling timing diagram.

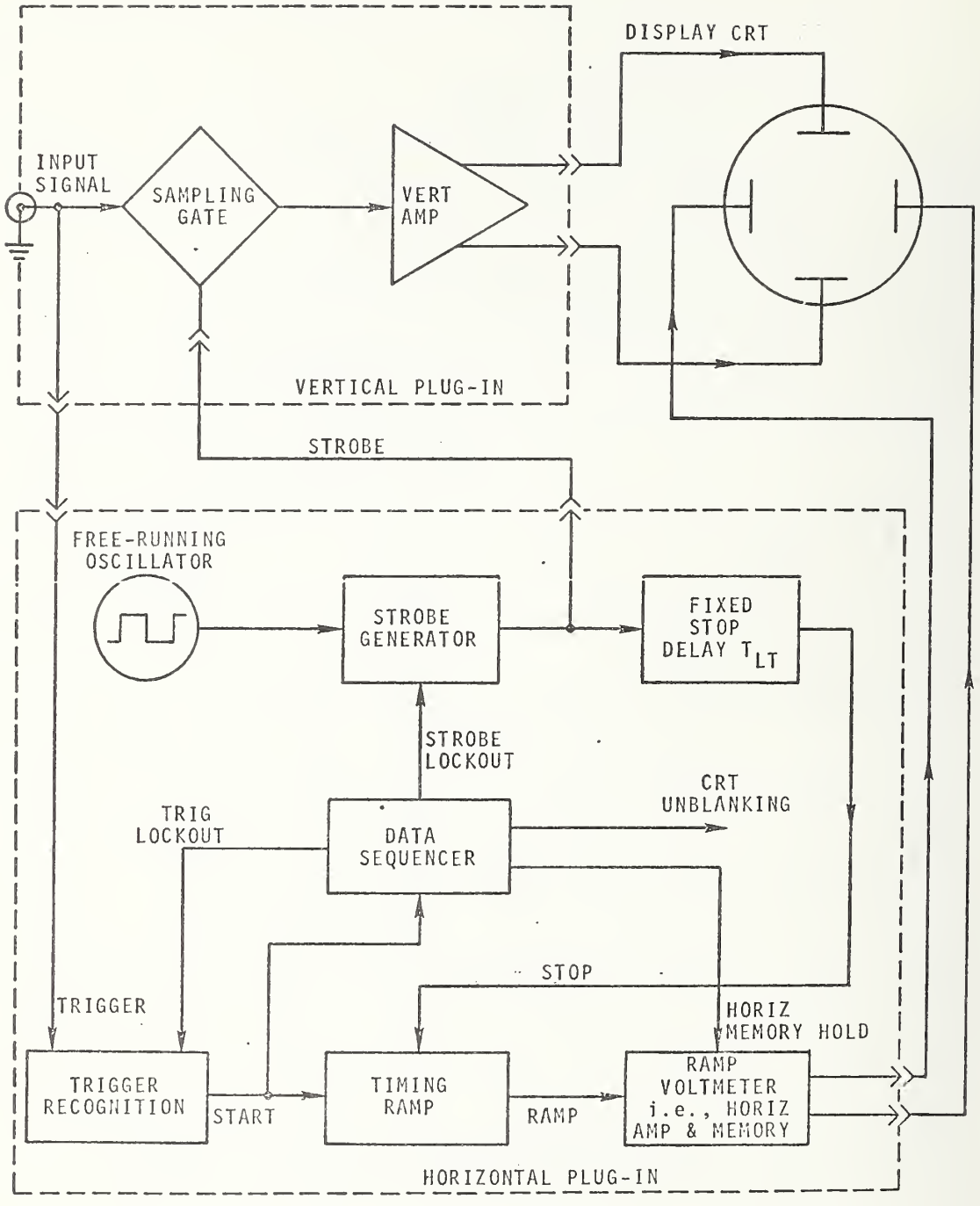


Figure 2-2. Basic random sampling block diagram.

3. SPECIFICATIONS

The instrument described in this report is a random sampling time base plug-in designed to be used in a commercial oscilloscope. It is used in the horizontal plug-in compartment of the oscilloscope main frame. The instrument is shown in the photograph, figure 1-2.

The reason for the choice of the particular oscilloscope is the availability of bistable storage display CRT's in this line. The extremely long persistence bistable storage CRT is essential when measuring mercury switch transitions. In this case the data acquisition time for a single waveform is several hours in duration.

The basic circuit design may be used with sampling oscilloscopes from other commercial manufacturers. Only minor circuit changes would be required to compensate for different power supply voltages and CRT requirements.

This instrument features three selectable time windows of 1 μs, 100 ns, and 10 ns. Time windows greater than 1 μs were not included as that is the time domain in which ordinary oscilloscopes excel. This instrument is specifically intended for high speed pulse measurements. A time magnifier is included to allow detailed examination of a small region within the basic time window. Using the time magnifier the fastest equivalent sweep rate is 10 ps/cm. A variable lead time control is provided to position the signal to be measured

within the time window. The trigger sensitivity is 10 mV. The instrument also includes an oscillator which is 0° phase-locked to the incoming trigger to predict the point in time at which the next signal will occur. This circuit increases the probability of obtaining valid data points. Table I lists the important electrical specifications.

TABLE I. ELECTRICAL CHARACTERISTICS

Characteristic	Performance
SWEEP RATES	
TIME/CM	Calibrated from 10 ps/cm to 100 ns/cm, selectable in a 1, 2, 5 sequence using the TIME WINDOW and TIME MAGNIFICATION controls.
TIME WINDOW	Three calibrated selectable windows of 1 μs, 100 ns, and 10 ns.
Time Window Accuracy	Within 1%
TIME MAGNIFICATION	Selectable from X1 to X100 in a 1, 2, 5 sequence.
Time Magnification Attenuator Accuracy	Within 3%
Timing Drift Long Term Stability	15 ps/h 10 ns window, X10 mag.
TIME POSITION	Ten turn control used to select position within basic time window for time magnification. Not used on X1.
Time Position Accuracy	Within 3%

TABLE I. CONTINUED

Characteristic	Performance
TRIGGERING	
Input Impedance	50 ohm nominal. +.3ρ, 1.4 ns TDR reflection.
Coupling	AC (.01 μF)
Polarity	Positive. Negative triggering is accomplished using external pulse inverting transformer.
Minimum Required Trigger Pulse	+10 mV, 1 ns duration
Maximum Trigger Pulse	+250 mV
Safe Overload	1 volt
Minimum Rate of Rise	5 V/μs
Sine Wave Sensitivity	1 mV RMS at 100 MHz
Bandwidth	400 MHz at 10 mV RMS
Holdoff Time	∿ 16 μs, i.e., countdown occurs for trigger frequencies greater than ∿ 60 kHz.
Display Jitter	
1 μs window, X1 mag.	< 5 ns
100 ns window, X1 mag.	< .4 ns
10 ns window, X1 mag.	< 40 ps
10 ns window, X100 mag.	20 ps
	Measured under optimum trigger conditions.

TABLE I. CONTINUED

Characteristic	Performance
Trigger Kickout	< .2 mV
	LEAD TIME
LEAD TIME	Variable control provided to position beginning of time window before (lead) or after (delay) trigger recognition.
Lead Time Range 1 µs window 100 ns window 10 ns window	 .5 µs lead to .9 µs delay 35 ns lead to 150 ns delay 15 ns lead to 80 ns delay
	STROBE
PLL	Phase locked loop (PLL) used to track incoming trigger frequency at 0° phase angle. PLL predicts occurence of next signal and fires STROBE to approximately coincide with signal.
PLL Capture Range	35 kHz to 100 kHz. Extended to 7-20 Hz by series of dividers in 1, 2, 5 sequence.
	OUTPUTS
START	Pulse occurs at instant of trigger recognition.

TABLE I. CONTINUED

Characteristic	Performance
Amplitude	+2 V into 50 Ω
10%-90% Transition Time	3.5 ns
Delay	40 ns after trigger
Z	TTL logic one pulse coincident with 7 μs unblanking pulse.
X	Voltage proportional to X deflection on CRT. 1 V/cm from -5 V to +5 V.

4. CIRCUIT DESCRIPTION

This section will discuss in detail the electrical design of the instrument. Block diagrams for the various circuits are found at the end of this section. Detailed circuit diagrams are located in chapter 5. Each block of the basic random sampling block diagram, figure 2-2, is described in more detail in this chapter.

4.1 Trigger

A more detailed block diagram for the trigger recognition circuit is presented in figure 4-1 with detailed circuit diagrams in figures 5-1, 5-2, and 5-3. The basic trigger recognition function is performed by a high speed (70 ps) tunnel diode. The adjustable bias voltage for this tunnel diode is furnished from a well regulated differential amplifier bias supply [4]. The importance of a highly stable, low noise bias for this tunnel diode to insure low jitter operation can not be ignored. The bias level can be adjusted for monostable operation with low frequency signals or astable operation to synchronize and count down high frequency signals. A buffer amplifier is used to provide isolation between external circuits and the very fast trigger recognition pulse.

Following the trigger recognition tunnel diode is the trigger lockout and anti-jitter circuit. The anti-jitter circuit [5] uses tunnel diode logic to prevent false

triggering during the rearming of the trigger circuit at the end of the trigger lockout period. A similar idea has been proposed by Nahman and Wigington [6] using coincidence circuits to detect the simultaneous presence of trigger and arming signals and then another gate to inhibit the passage of the delayed trigger. A modification of this has been proposed most recently by Bertolaccini and Cova [7].

A fast TTL flip-flop follows the trigger lockout circuit. The output of this flip-flop is the START pulse which is used to start the timing ramp and activate the data sequencer.

The pulse polarity for trigger recognition in this instrument is positive. To obtain triggering from a negative going signal, an external pulse inverting transformer is used.

Q101 is the input buffer amplifier. The voltage gain from the 50 ohm input to the collector is 0.9. The amplifier 10%-90% transition time is 400 ps.

TD1 is the trigger recognition diode. Constant voltage, low impedance bias for TD1 is furnished by Q102 and IC-100. The 1 μH choke L101 provides isolation between the bias supply and TD1 at high frequencies. The buffered input signal is fed to TD1 from Q101 by R101. When a trigger recognition occurs, TD1 switches from its low voltage state to its high voltage state generating a fast (< 100 ps)

transition. This voltage transition is differentiated and coupled out by R102 and C101 to the trigger lockout and anti-jitter circuit. TD1 is held in its high voltage state for several nanoseconds by the constant current action of L101. After the L/R decay of the current through L101, TD1 resets to its quiescent low voltage state. To synchronize with high frequency signals up to 400 MHz the TRIGGER LEVEL control is turned clockwise past 12 o'clock. This biases TD1 for astable operation.

The trigger lockout and anti-jitter circuit is shown in figure 5-2. Tunnel diodes TD2 and TD3 are used as logic gates. They are biased by the constant current transistors Q105 and Q106 respectively. They are triggered by the fast differentiated transition from TD1. The bias transistors form the output legs of differential pairs Q104-Q105 and Q106-Q107. These differential pairs are operated as ECL current switches to gate the bias currents for TD2 and TD3 on and off according to the state of the TRIG LOCKOUT signal.

Approximately 9 ma of bias current is furnished to TD2 by Q105. The additional current required to switch TD2 to its high voltage state is furnished by TD1 buffered by Q103. TD2 will only switch when its rearming current (9 ma) has reached 95% of its final value. Q106 furnishes approximately 6 ma of bias current to the output tunnel diode TD3. The fast transition from TD1 supplies a trigger pulse of 3 ma to

TD3 through the delay line DL1. The sum of the bias (6 ma) and the trigger (3 ma) currents is insufficient to switch the 10 ma tunnel diode to its high voltage state. However, if the arming tunnel diode TD2 was previously switched to its high voltage state, it would supply an additional arming bias current of 2 ma through R103 to TD3. TD3 would then be biased by 8 ma instead of 6 ma. Then the 3 ma trigger pulse would cause TD3 to switch states.

The timing sequence of events in this circuit is as follows. First assume TRIG LOCKOUT is a "1." Thus Q105 and Q106 are cutoff and as a result the arming tunnel diode TD2 and the output tunnel diode TD3 are also cutoff. When TRIG LOCKOUT switches to a "0," Q105 and Q106 turn on rapidly. However the bias currents for TD2 and TD3 do not build up as fast. This is due to the rearming delay action of C102 and C103 which momentarily divert the currents coming from Q105 and Q106. However C102 is much larger than C103 insuring that the bias for TD3 will have completely reached a stable steady state before the bias current in TD2 has reached a level sufficient to be triggered by a pulse from TD1. The arming tunnel diode TD2 may be triggered during the end of its rearming period. Thus the arming current transition may exhibit 1 or 2 ns of timing jitter.

The trigger pulse from TD1 arises at TD3 5 ns after it passed TD2 due to the delay line DL1. The bias current and arming current for TD3 are in a stable steady state condition when the trigger pulse arrives. Thus TD3 is able to make a jitter-free transition when it is triggered by TD1. The TD3 transition is amplified by the differential amplifier Q108-Q109.

The START and RAMP LOCK circuits are shown in figure 5-3. The START flip-flop is composed of two high speed TTL 74H00 gates. The flip-flop is set by the amplified TD3 transition from Q108.

The RAMP LOCK circuit's function is to prevent the timing ramp from functioning if it will produce invalid data. This can occur in the condition when a STOP pulse in the "1" state is present at the time of the arrival of the $\overline{\text{START}}$ pulse in the "0" state. An invalid time measurement would occur if the STOP went to "0" while the $\overline{\text{START}}$ was in the "0" state thus starting the ramp later than it should. To avoid this condition a fast TTL logic circuit is used to test for the presence of a STOP "1" at the instant of trigger recognition, t_o. If such a coincidence exists then the RAMP LOCK goes to the "1" state locking up the ramp for the duration of one trigger cycle.

4.2 Timing Ramp

The timing ramp block diagram is shown in figure 4-2 and in full detail in figure 5-4. The basic mechanism used here to obtain a linear timing ramp is a constant current source, I_T, (Q5, Q6, and the type 741 op amp) discharging a capacitor, C_T. The START-STOP switching action on the timing ramp is performed by the emitter coupled logic (ECL) gate (Q1-Q3) which is placed in the path connecting the constant timing current source I_T and the timing capacitor C_T. TTL logic signals drive transistors Q1 and Q2. A fixed logic state of "1/2," i.e., a voltage level intermediate between the defined levels of a TTL "0" and a TTL "1," is applied to the base of Q3. The collector of Q3 is connected to C_T. Q3 provides the only path for I_T to reach C_T. When the inputs to Q1 and Q2 are both "0's," these transistors are cutoff. Transistor Q3 is on and timing current I_T passes through it discharging C_T. When the input to either Q1 or Q2 is a "1" then that transistor is on and Q3 is off, thus diverting I_T to the +5 V supply.

The timing capacitor C_T was initially fully charged to +15 V through the ramp reset switch, JFET Q8. Q7 was off, thus applying +15 V to the gate of Q8. The use of a FET at Q8 to charge C_T to the stable, regulated +15 V supply is essential to the long term timing stability of this ramp. For low drain-source voltages, the FET behaves as a simple resistor whose V-I curve passes through the origin with no

offset. Saturated bi-polar transistors or diodes are not acceptable as the reset element Q8. This is because they introduce small, but nevertheless important, voltage offsets that are temperature dependent and will cause long term timing errors.

The timing sequence of events will now be described. Initially the START input to Q7 is a "0." The $\overline{\text{START}}$ input to Q1 is a "1." The STOP input to Q2 is a "0." When a trigger is recognized the START flip-flop sets the START signal to a "1." This turns on Q7 which in turn strongly reverse bias the gate of Q8, turning it off. The voltage on C_T remains essentially constant at +15 V as there are only very small leakage paths presently connected to C_T. The $\overline{\text{START}}$ signal, the negation of START and produced simultaneously with START, is passed through a 15 ns delay line, DL2. When it arrives at Q1 15 ns later, Q8 has already been disconnected from C_T. The "0" $\overline{\text{START}}$ now at Q1 turns it off. Now the inputs to Q1 and Q2 are both in the "0" state. Thus Q3 is now turned on and all of I_T now passes through it discharging C_T. If a STOP pulse going to the "1" state should occur during the discharge of C_T, it will turn on Q2. This immediately diverts I_T to Q2 turning off Q3 and stopping the run-down of the ramp.

The voltage on C_T is now proportional to the time interval between the occurrence of the delayed $\overline{\text{START}}$ and the STOP pulses

$$V_R(t_i) = +15\ V - \frac{1}{C_T} \int_{t\ (\overline{\text{START}}\ \text{dlyd.})}^{t(\text{STOP})} I_T\ dt$$

This stopped RAMP voltage $V_R(t_i)$ is read by a high impedance JFET source follower, Q9. The output of Q9 is fed to a ramp memory and subsequent horizontal amplifier.

The full excursion of the voltage ramp on C_T is from +15 V to +1.4 V the saturation voltage level of Q3. However only the center region of the ramp from +10 V to +5 V is actually used for timing measurements. This is done to avoid the nonlinear portions of the ramp. The nonlinearity from +15 to +10 V is particularly important for the 10 ns range (Δ V = -5 V in a Δt of 10 ns). The major factor here is the time required for the ECL gate to fully switch the current I_T into Q3 and C_T. The ramp voltage region from +5 V to +1.4 V is avoided due to the ramp nonlinearity introduced by the p-n junction capacitances of Q3 and Q8. These capacitances are inversely proportional to the reverse voltage across the junctions.

$$C_j \propto (1/V)^n$$

where n is typically 1/3 or 1/2 depending upon the construction of the transistor's junctions. For small voltages the value of C_j can become appreciable with respect to the 39 pF timing capacitor, C_T.

One additional input (RAMP LOCK) to the ECL gate is provided by Q4. It is the function of Q4 to prevent the timing ramp from functioning if it will produce invalid data.

4.3 Horizontal Amplifier

The block diagram for the horizontal amplifier is shown in figure 4-3. The gain and voltage level distribution is also included. With the exception of the discrete transistor final amplifier, fast slewing rate, integrated circuit, operational amplifiers are used throughout. The two memories use MOSFET sampling gates and JFET source followers. The detailed circuit diagrams are found on figures 5-5, 5-6, 5-7, 5-8, and 5-9.

The decay time of the stopped RAMP voltage, $V_R(t_i)$, on the 39 pF timing capacitor C_T is quite rapid. Therefore it is necessary to quickly transfer $V_R(t_i)$ to a larger ramp storage capacitor. This function is performed by a X1 follower amplifier IC-301 and the ramp memory, figure 5-5.

The valid data region of the RAMP voltage from 10 V to 5 V is inverted and level shifted by a X(-1) summing amplifier IC-302 to a -2.5 to +2.5 V signal, figure 5-6. In addition this amplifier also introduces an adjustable dc offset when the time magnifier is used in the X2 to the X100 positions. This offset allows the operator to select a particular time position within the basic time window around which he will use the time magnifier.

Following the summing amplifier is an adjustable attenuator, figure 5-7. It is used for the time magnifier function. The total gain in the amplifier chain is 2×10^3. The CRT requires a Δ V = 100 V for full scale deflection. With the time magnifier in the X1 position, an attenuation of 100 is inserted into the chain. For this case a change in the ramp voltage from 10 V to 5 V corresponds to a Δ V of 100 V at the CRT (i.e., full scale deflection). With the time magnifier in the X100 position, there is no attenuation inserted. In this situation, the Δ V of 5 V in the ramp voltage corresponds to a Δ V of 10^4 V at the output of the final amplifier. In actual practice an output of 10^4 V does not occur due to limiting within the amplifier chain. A particular small portion of the ramp voltage is actually linearly amplified by 2×10^3 to give an output Δ V of 100 V. This portion is chosen by adjustment of the time position control.

A horizontal memory is also included in the amplifier chain, figure 5-8. Its purpose is to stabilize the data applied to the CRT during the 7 μs unblanking period when a data point dot is being written on the bistable storage oscilloscope screen. There is a 7 μs delay after trigger recognition to allow for the horizontal and vertical amplifiers' settling time. At the end of this 7 μs delay this memory goes to a hold condition for the 7 μs unblanking period.

The signal level after the X10 driver amplifier IC-305, figure 5-9, varies from -5.00 V to +5.00 V. At this point a separate X1 buffer IC-306 provides a calibrated 1 V/div. X data output signal. The final amplifier is a pair of inverting, discrete transistor, operational amplifiers to provide push-pull drive to the CRT horizontal deflection plates. The gain and dc offset of this amplifier are adjustable to match the instrument to the CRT sensitivity.

For proper data handling transient response and long term stability it is imperative that the amplifiers never be allowed to limit or saturate. Separate fast diode limiters are included with each amplifier in the chain to carefully control the maximum signal levels.

4.4 Strobe Predictor

In the actual instrument the free-running oscillator, figure 2-2, is replaced by a strobe predictor. Figure 4-4 is the block diagram for this circuit. Its function was described earlier in the random sampling theory section. It is basically a phase locked oscillator [8]. The reference signal into the phase locked loop (PLL) is the $\overline{\text{START}}$ pulse from the trigger recognition circuit. Thus the PLL attempts to lock in frequency and phase with the incoming trigger signal.

The phase/frequency detector is a TTL integrated circuit, figure 5-10. The inputs to this detector are TTL logic pulses. This detector attempts to lock the loop with zero degree phase error between the negative going transitions of the reference and variable inputs.

The voltage controlled oscillator used is also a TTL integrated circuit and is a companion unit to the phase detector, figure 5-12. Its basic operating frequency range is 33 kHz to 100 kHz. This is compatible with the maximum data rate of 60 kHz of the instrument. For operation at lower frequencies, TTL frequency dividers are inserted to count down the voltage controlled oscillators basic frequency. The output of this divider chain is the variable input to the phase detector and also the VCO drive signal for the strobe generator and the stop delay circuit.

A low-pass filter is also in the loop. It is used to improve the PLL performance. A second-order active filter IC-401 is used, figure 5-10. The PLL natural frequency is 100 Hz or less depending upon the range in use. A damping factor of 0.7 is used to provide optimum damping.

With the PLL locked to an incoming signal, whose repetition rate is extremely stable (such as that derived from a quartz oscillator), no random sampling occurs. The PLL output occurs precisely at t_o (i.e., trigger recognition). The visual result on the CRT screen is the continuous display of

a single dot in the center of the CRT. Thus it is necessary to randomize the occurrence of the predicted STROBE on either side of t_o in a controlled manner. The technique used to accomplish this is the injection of a controlled amount of random noise onto the dc control voltage that is applied to the voltage controlled oscillator. The mean value of the noise voltage is zero and its lowest frequency component is at least 10X greater than the PLL bandwidth. Thus the injection of this noise into the PLL does not affect the lock characteristics of the PLL. The net result is a random phase jitter of the STROBE centered on t_o. The amount of phase jitter introduced is adjusted to coincide with the width of the time window used. The net result is a greatly increased probability of coincidence of the STROBE with the input signal in the time window as compared to the simple free-running oscillator.

The noise generator, figure 5-11, consists of the base-emitter junction of a transistor biased into its reverse breakdown region. The low level breakdown noise is amplified 80 dB by a low noise audio amplifier. The passband of the audio amplifier is from 2 kHz to 100 kHz.

One other addition is a simple circuit to turn on an LED on the front panel when the PLL is locked, figure 5-13. The U and D outputs from the phase detector are summed in IC-411. When the loop is locked the sum U-D is zero. This condition is detected by the dual comparator IC-412.

4.5 Strobe and Stop Delay

The strobe and stop delay block diagram is shown in figure 4-5. The TTL input to these circuits is the $\overline{VCO}$ signal from the strobe predictor circuit. To generate the STROBE signal, figure 5-14, the VCO signal is simply differentiated and passed through a high speed TTL gate and routed to the vertical plug-in. A strobe lockout gate is included to prevent the strobing of the vertical channel during the data display cycle.

The strobe delay circuit, figure 5-15, consists of a linear time ramp generator and a differential comparator. The ramp generator consists of a constant current source I_D (Q302) charging the delay capacitor C_D (C301, C302, or C303). Initially the $\overline{VCO}$ signal is in the "1" state. Thus the clamp transistor Q301 is turned on, clamping the delay ramp voltage V_D near zero volts. The clamp transistor is held just above saturation by the Schottky diode connected between the base and collector. When the $\overline{VCO}$ signal goes to the "0" state the clamp transistor Q301 is cutoff allowing C_D to be charged by I_D. $V_D(t)$ is thus a positive going ramp. When $V_D(t)$ reaches the voltage level, V_{LT}, set by the lead time control, the differential comparator changes states and produces the STOP pulse. The differential comparator consists of two high speed differential amplifiers Q303-Q304 and Q305-Q306 constructed of discrete fast NPN and PNP transistors.

Larger lead time ranges are obtained for the wider time windows (100 ns and 1 μs) by increasing the size of C_D. This is done by electronically switching into the circuit C302 and C303. This is accomplished by fully saturating transistors Q309 and Q310.

For minimum timing jitter and excellent long term stability, it is imperative that the delay current I_D and the lead time voltage V_{LT} be extremely well regulated and filtered from external transients (such as the START signal in particular). These filtering requirements also hold for the strobe generator. There must be a very precisely held time delay between the STROBE and STOP signals. Any jitter between these two signals will be seen as jitter on the CRT. Any crosstalk between the START pulse (and its other related data sequencing pulses) and the STOP and STROBE pulses must be avoided as this will also be a source of timing jitter. Thus proper component and wiring layout and power supply filtering is absolutely essential to minimizing timing jitter.

4.6 Data Sequencer

The last block diagram, figure 4-6, to complete the instrument is the data sequencer. The sequencer is composed entirely of TTL integrated circuits. Its purpose is to provide the proper time sequencing of the various data handling functions in the instrument after receipt of a START pulse

(i.e., trigger recognition). The detailed circuit diagrams are figures 5-16, 5-17 and 5-14.

When the START pulse goes to the "1" state it triggers a 2.5 μs monostable (IC-103). This 2.5 μs pulse is the RAMP SAMPLE command for the ramp memory. Simultaneous with the leading edge of the 2.5 μs pulse, a 7 μs monostable (IC-104) is triggered. The purpose of this monostable (IC-104) is to allow sufficient data settling time in the vertical and horizontal amplifiers. At the end of this 7 μs delay another 7 μs monostable (IC-105) is triggered. The output of IC-105 is the HORIZ HOLD pulse for the horizontal memory. This 7 μs pulse is also used as the CRT UNBLANKING pulse if the X data is valid, i.e., if the X voltage from the driver amplifier is between -5 V and +5 V. This check is performed by a dual comparator IC-110, figure 5-17. One additional monostable (IC-106) is used to give a 9 μs delay. It is triggered at the end of the 7 μs data delay. The outputs of IC-104 and IC-106 are combined in an OR gate to give the 16 μs TRIG LOCKOUT pulse. The STROBE LOCKOUT pulse is provided by a flip-flop IC-107, figure 5-14. The flip-flop is set to the "1" state at the end of the 2.5 μs RAMP SAMPLE pulse. It is then reset to "0" at the end of the data display period (CRT UNBLANKING). The START flip-flop IC-101, figure 5-3, is reset to "0" at the end of the 7 μs data delay pulse (IC-104). The resetting of START in turn resets the timing ramp via Q7 and Q8.

IC-109, figure 5-16, produces a single-shot pulse a few seconds after power is applied to the instrument. This pulse is used to set the flip-flops and other circuits to their proper state.

4.7 Power Supply

Figures 5-18 and 5-19 show the power supply and plug-in interconnections for use in the 564 oscilloscope mainframe. Many required voltages are directly available from the mainframe. The +5 V and +15 V are not available from the mainframe. These voltages are obtained from regulated power supplies driven by a built-in transformer. The transformer is powered by 6.3 V ac from the mainframe.

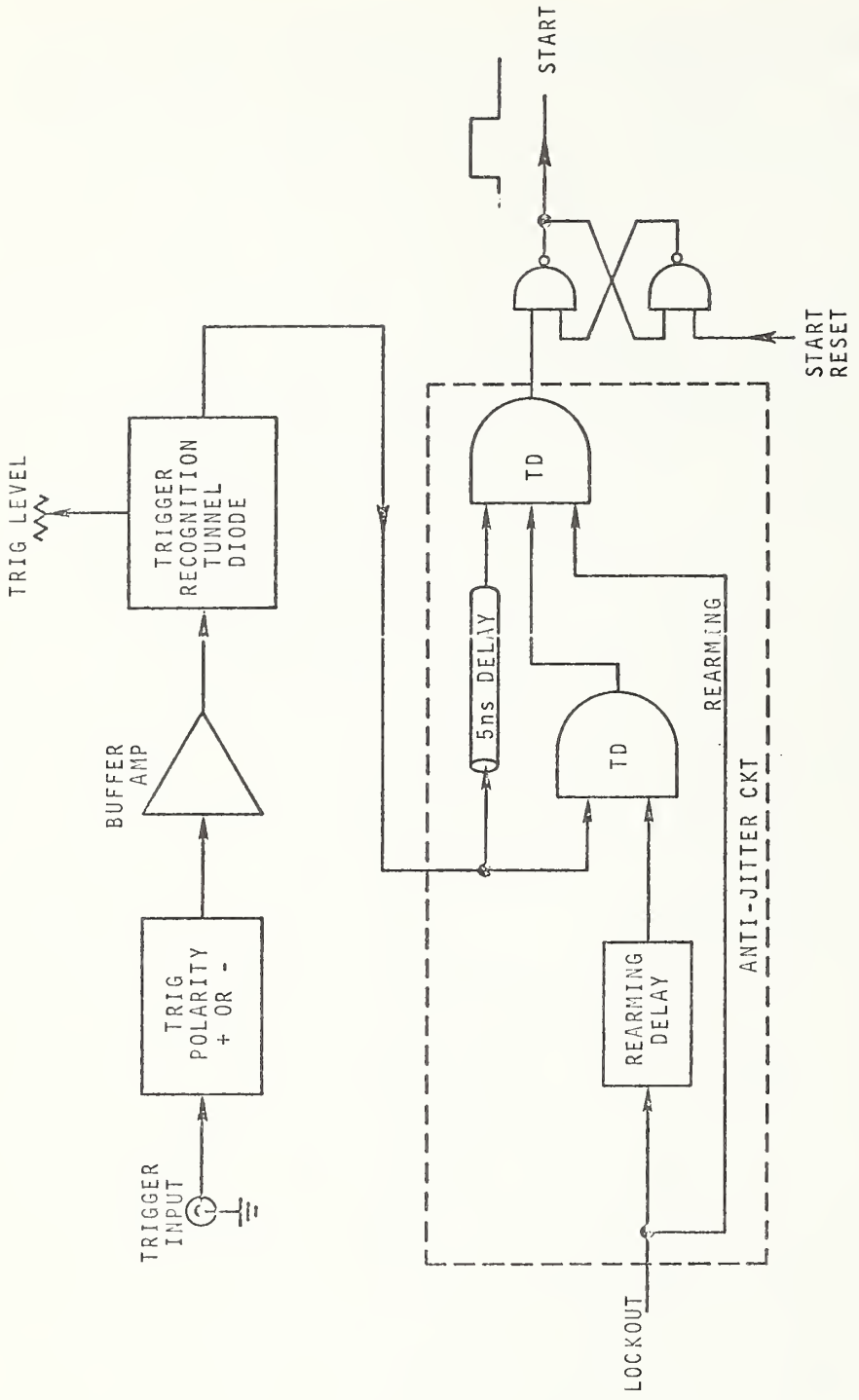


Figure 4-1. Trigger recognition block diagram.

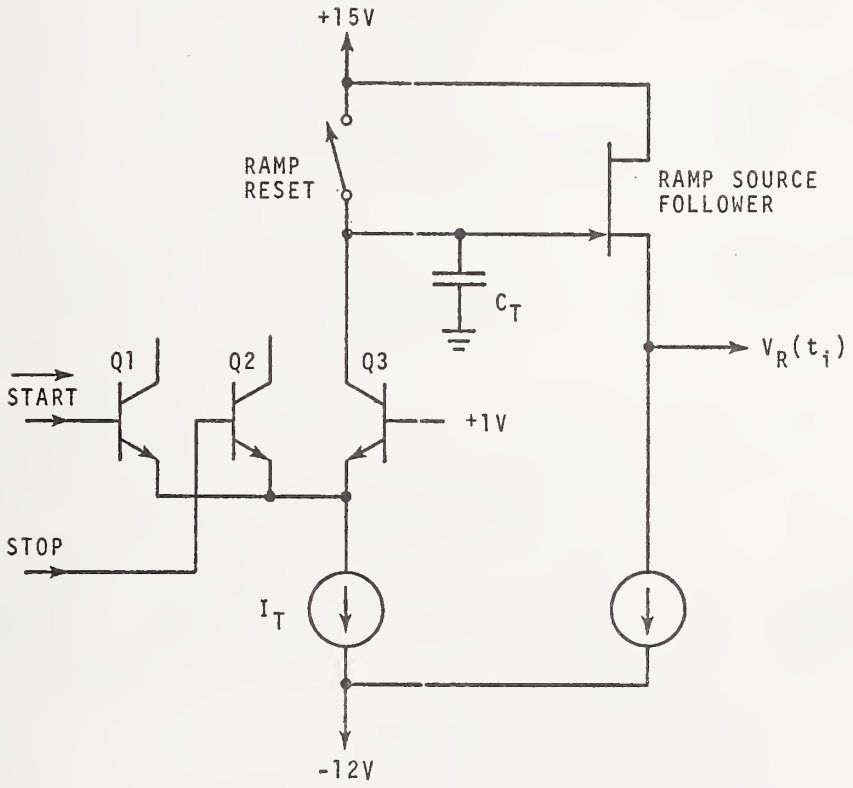


Figure 4-2. Timing ramp block diagram.

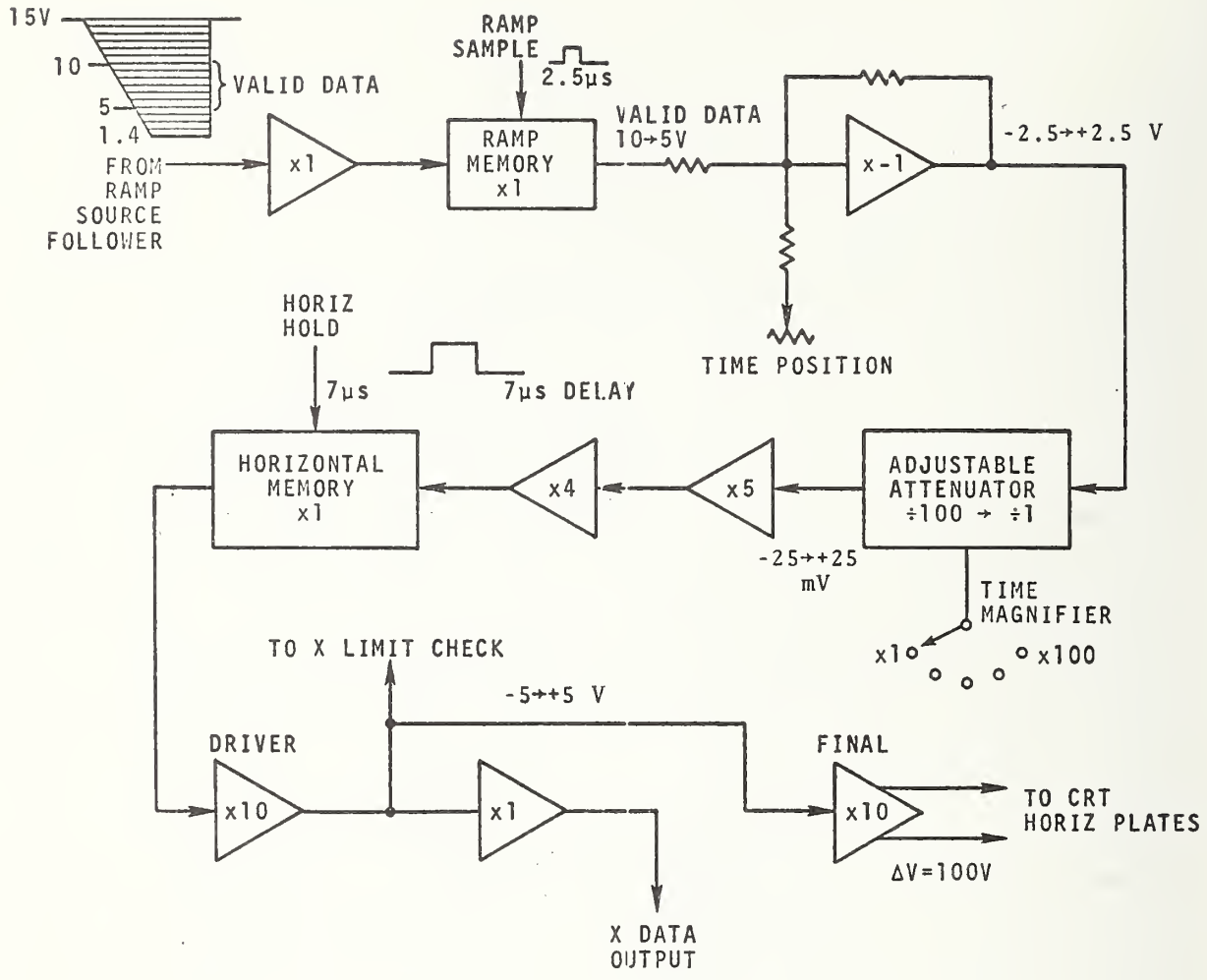


Figure 4-3. Horizontal amplifier block diagram.

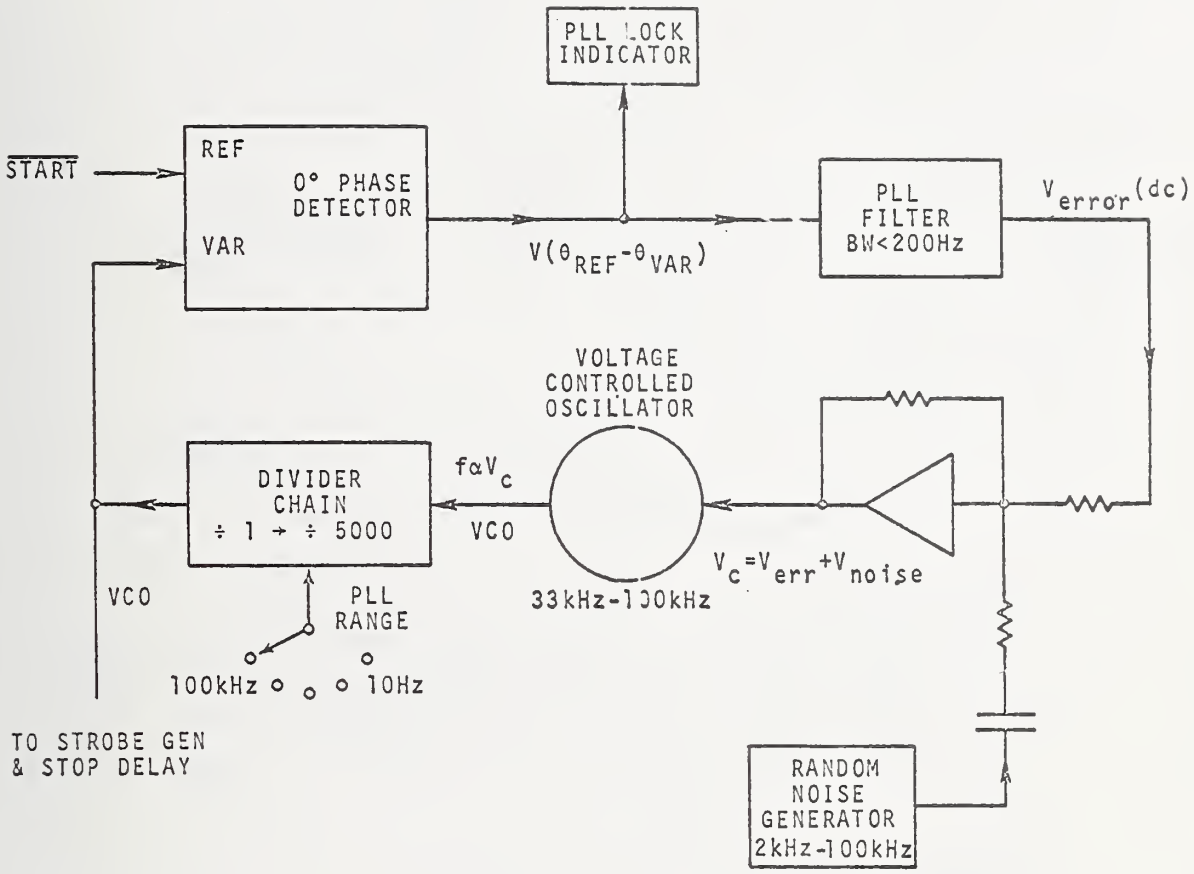


Figure 4-4. Strobe predictor block diagram.

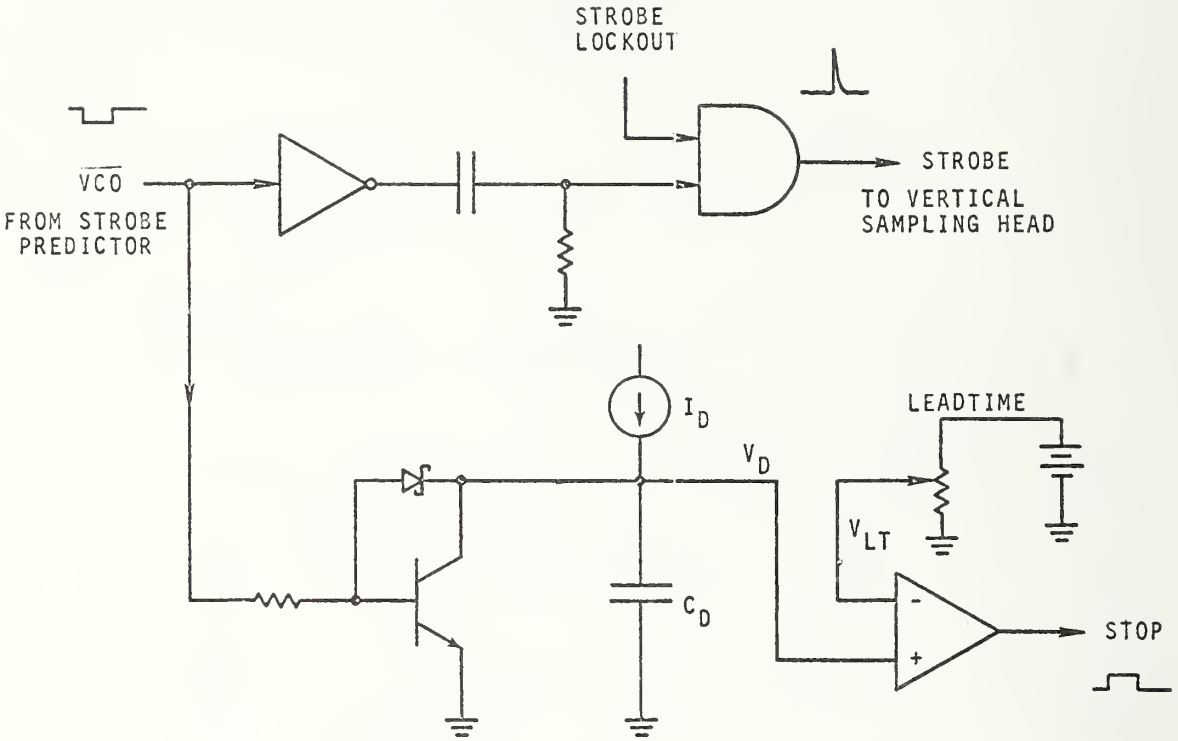


Figure 4-5. Strobe and stop delay block diagram.

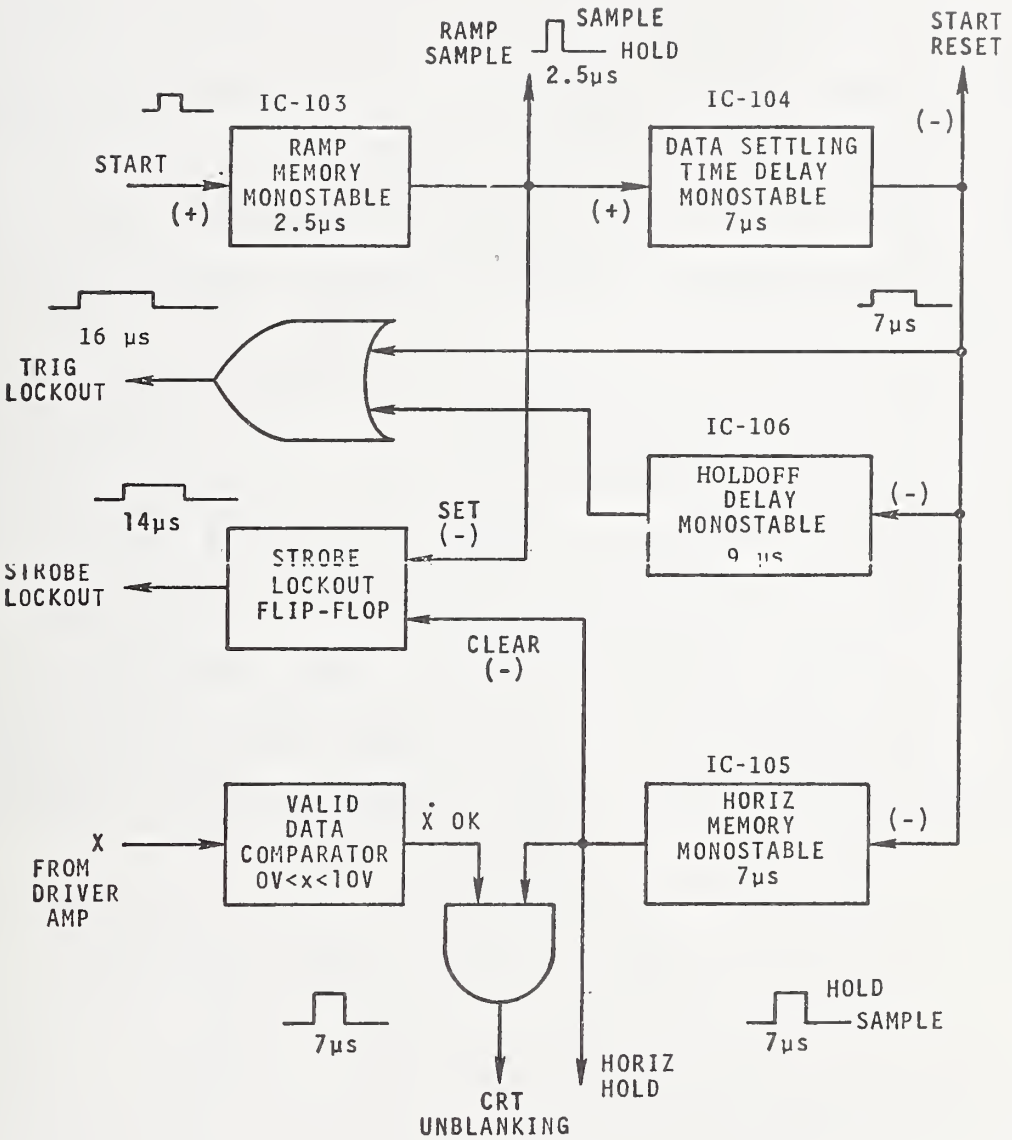


Figure 4-6. Data sequencer block diagram (+) denotes positive going edge triggering. (-) denotes negative going edge triggering.

5. CIRCUIT DIAGRAMS

This chapter consists of the detailed circuit diagrams for the random sampling time base. All component values are given directly on the circuit diagrams. Components referenced in the text are also given a number designation such as Q101. Unless noted otherwise, all resistors are 1/8 watt, 5% tolerance.

The instrument is constructed in a blank plug-in designed for the bistable storage oscilloscope. The actual circuit construction is as shown in figure 5-20. This view shows the power supply, horizontal amplifier, and strobe predictor. All other circuits are on a single circuit board on the other side. This prototype was built using perforated circuit board and quasi printed circuit, copper tape wiring techniques.

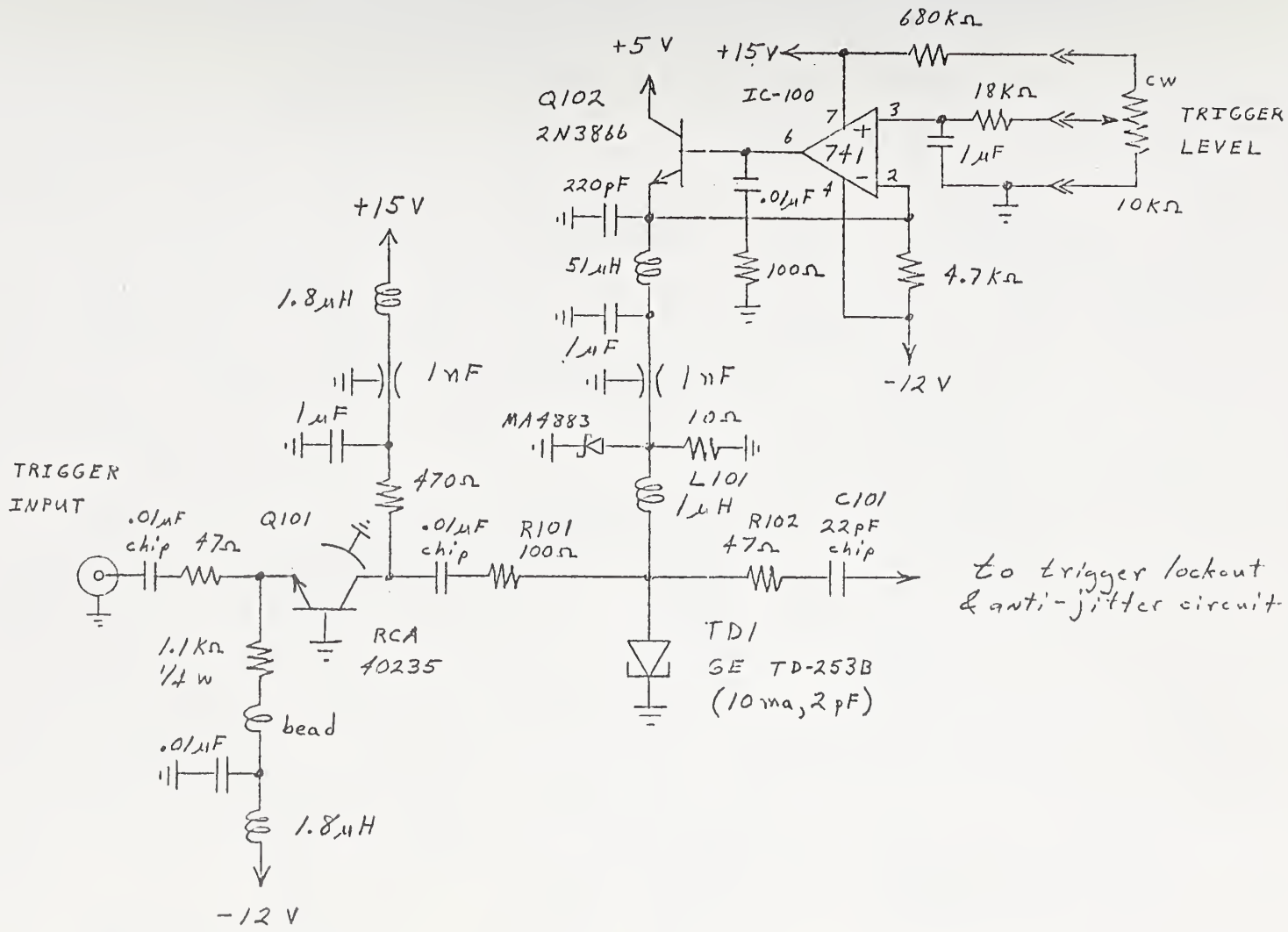


Figure 5-1. Input buffer amplifier and trigger recognition tunnel diode.

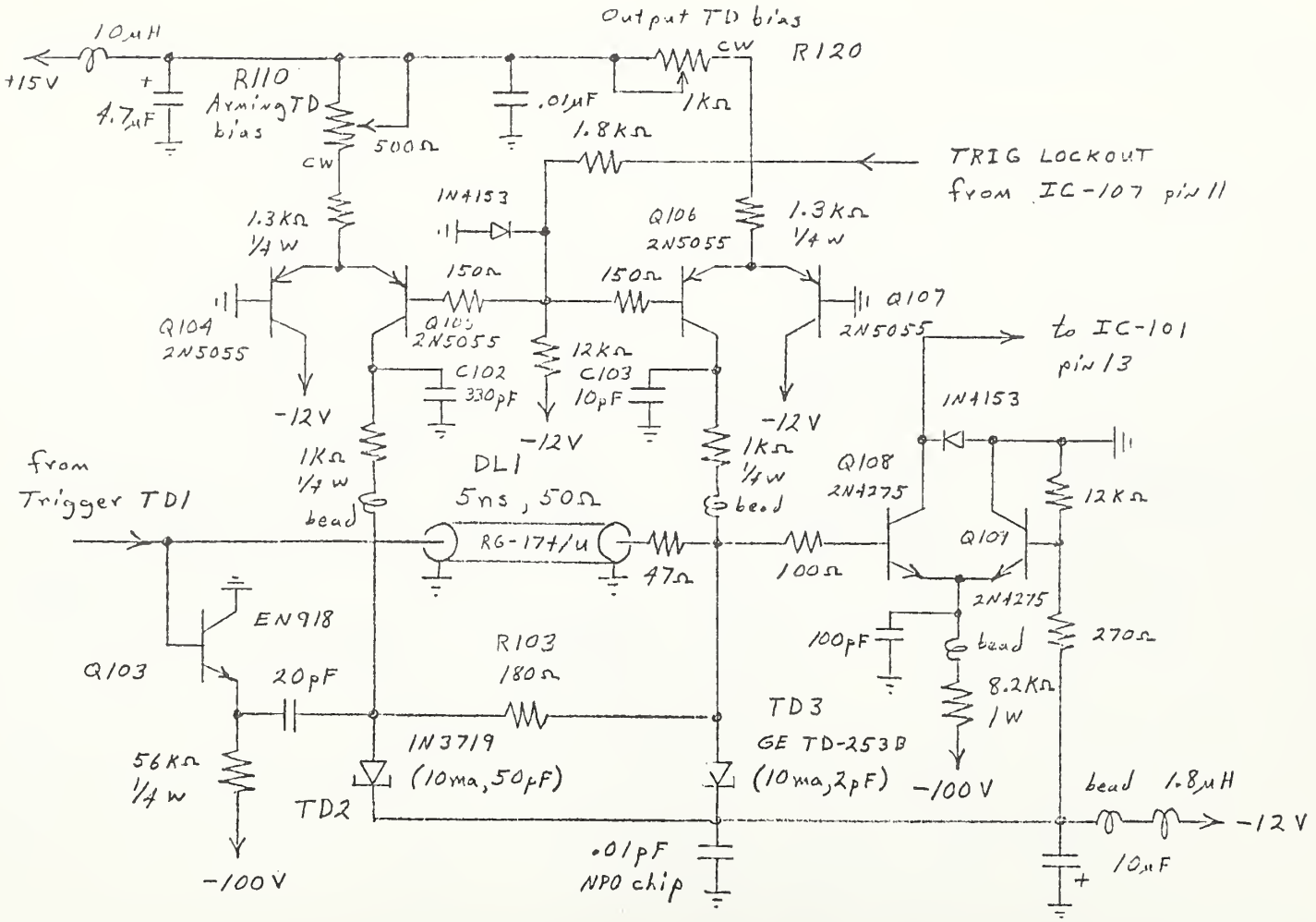


Figure 5-2. Trigger lockout and anti-jitter.

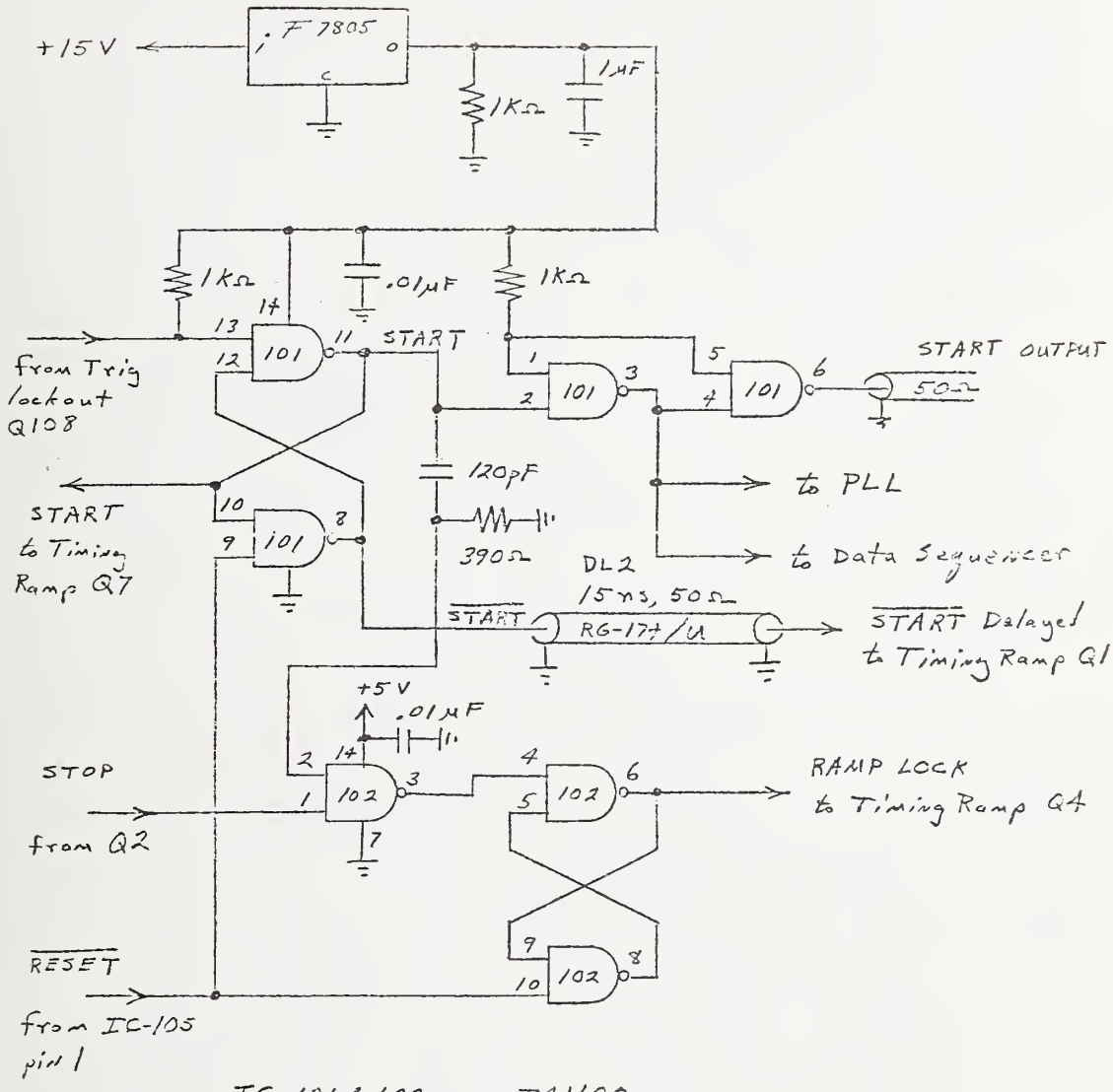


Figure 5-3. Start and ramp lock.

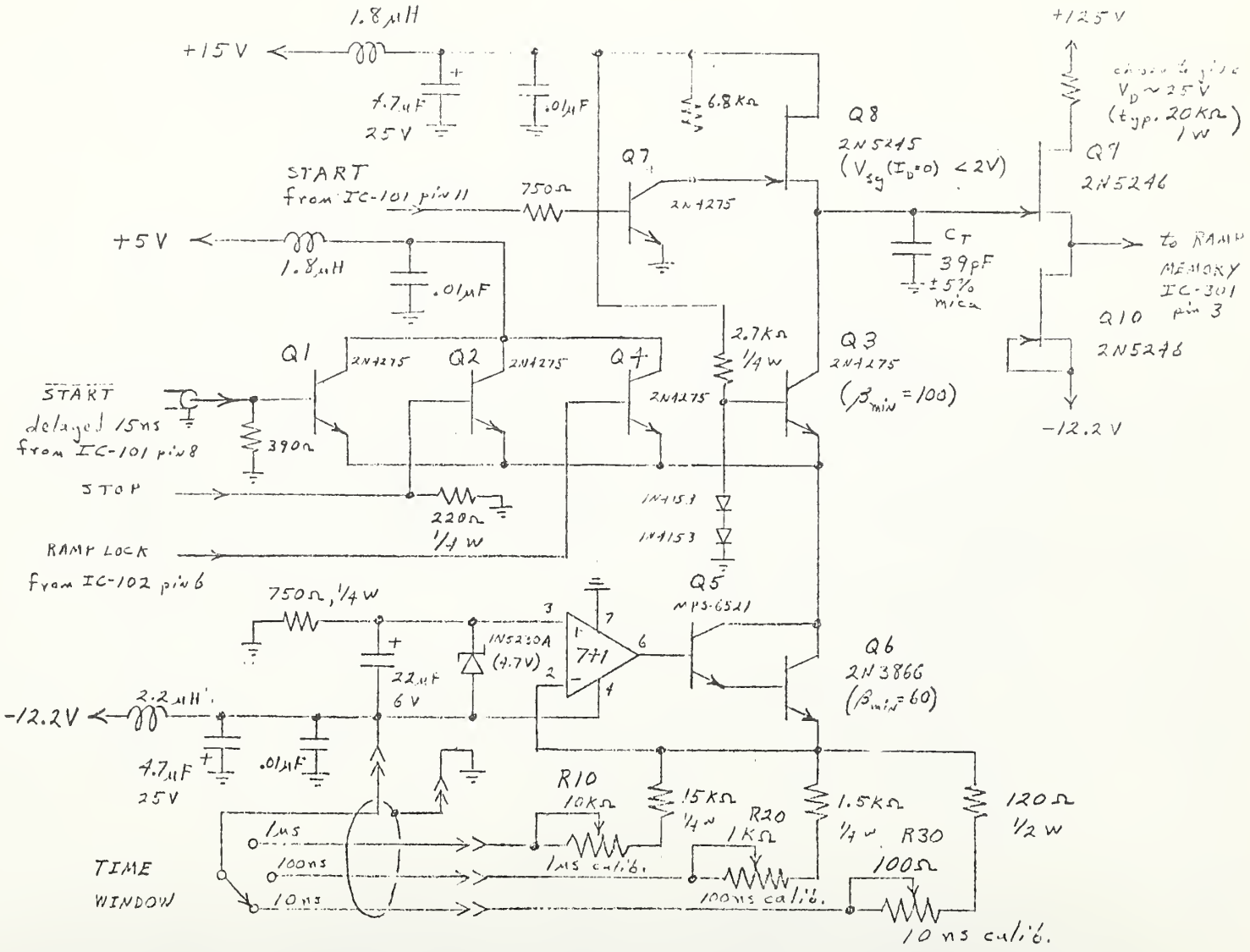


Figure 5-4. Timing ramp.

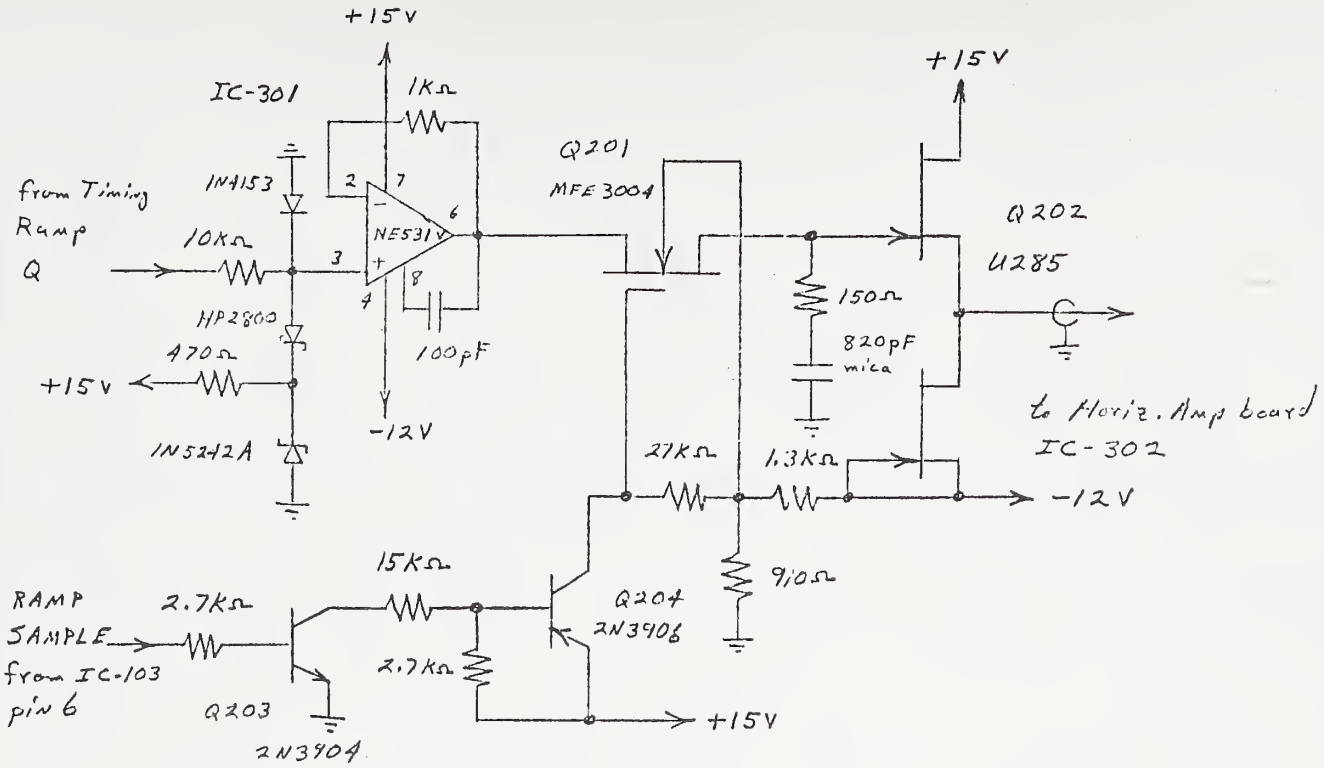


Figure 5-5. Ramp memory.

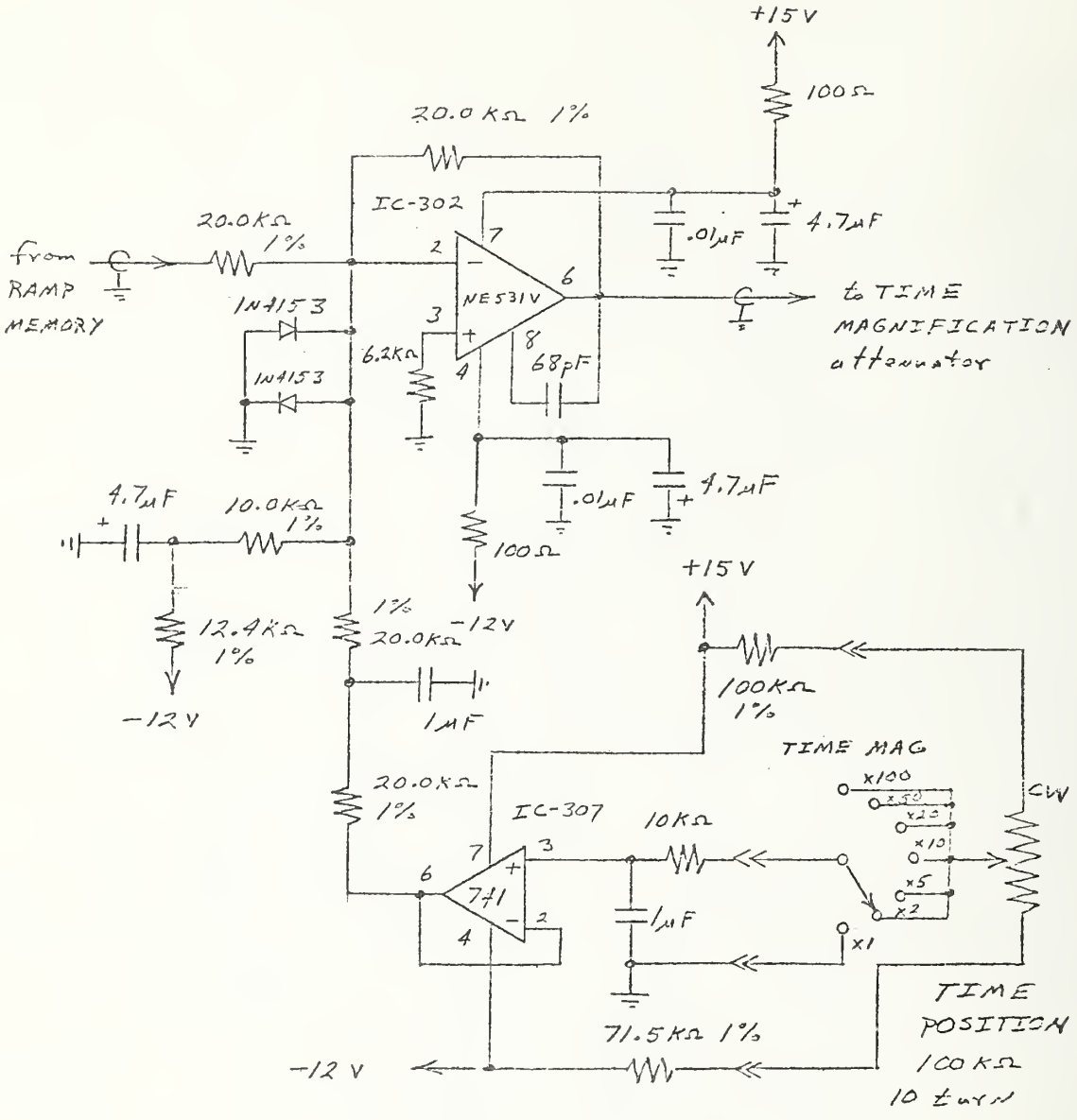


Figure 5-6. Time position summing amplifier.

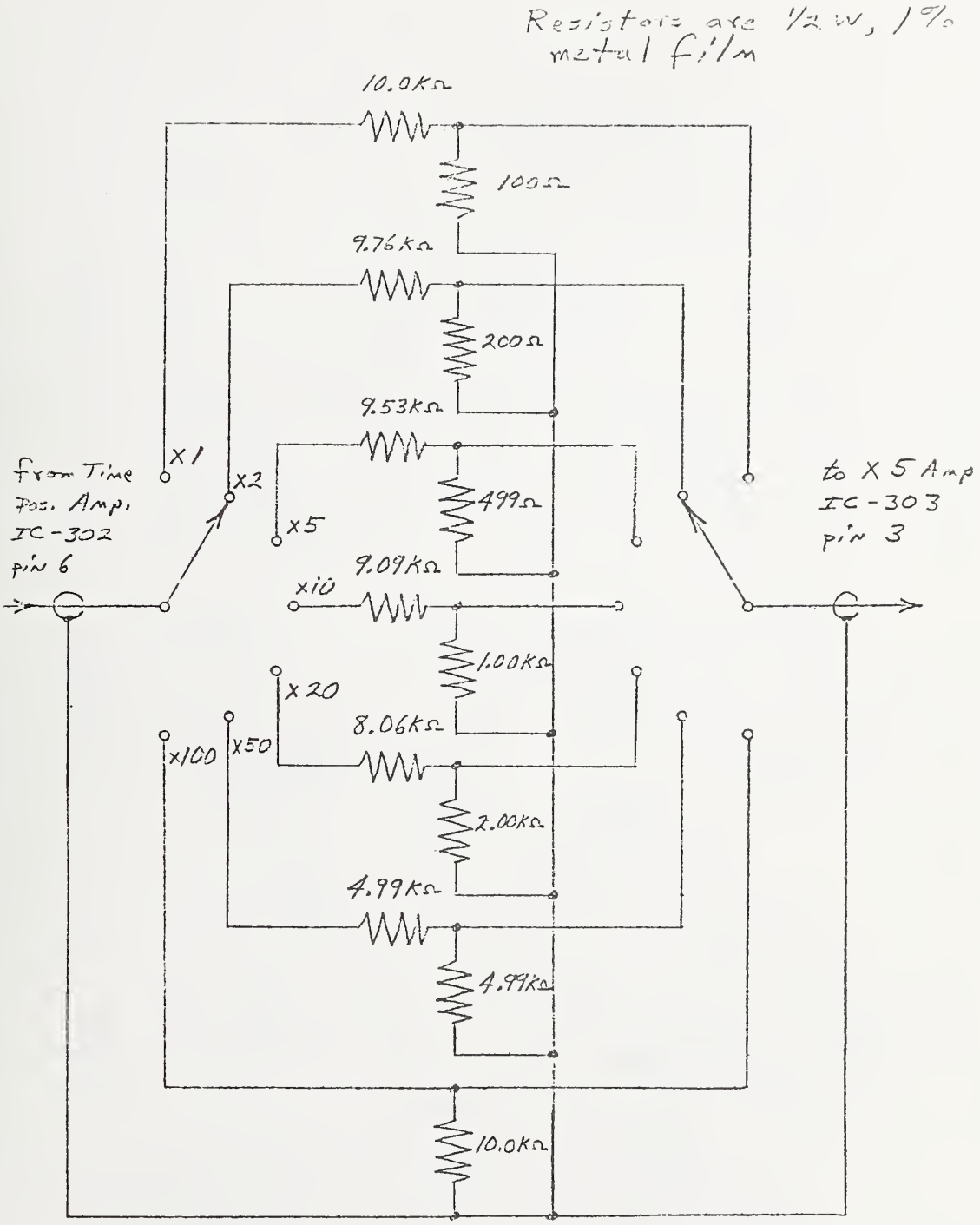


Figure 5-7. Time magnifier attenuator.

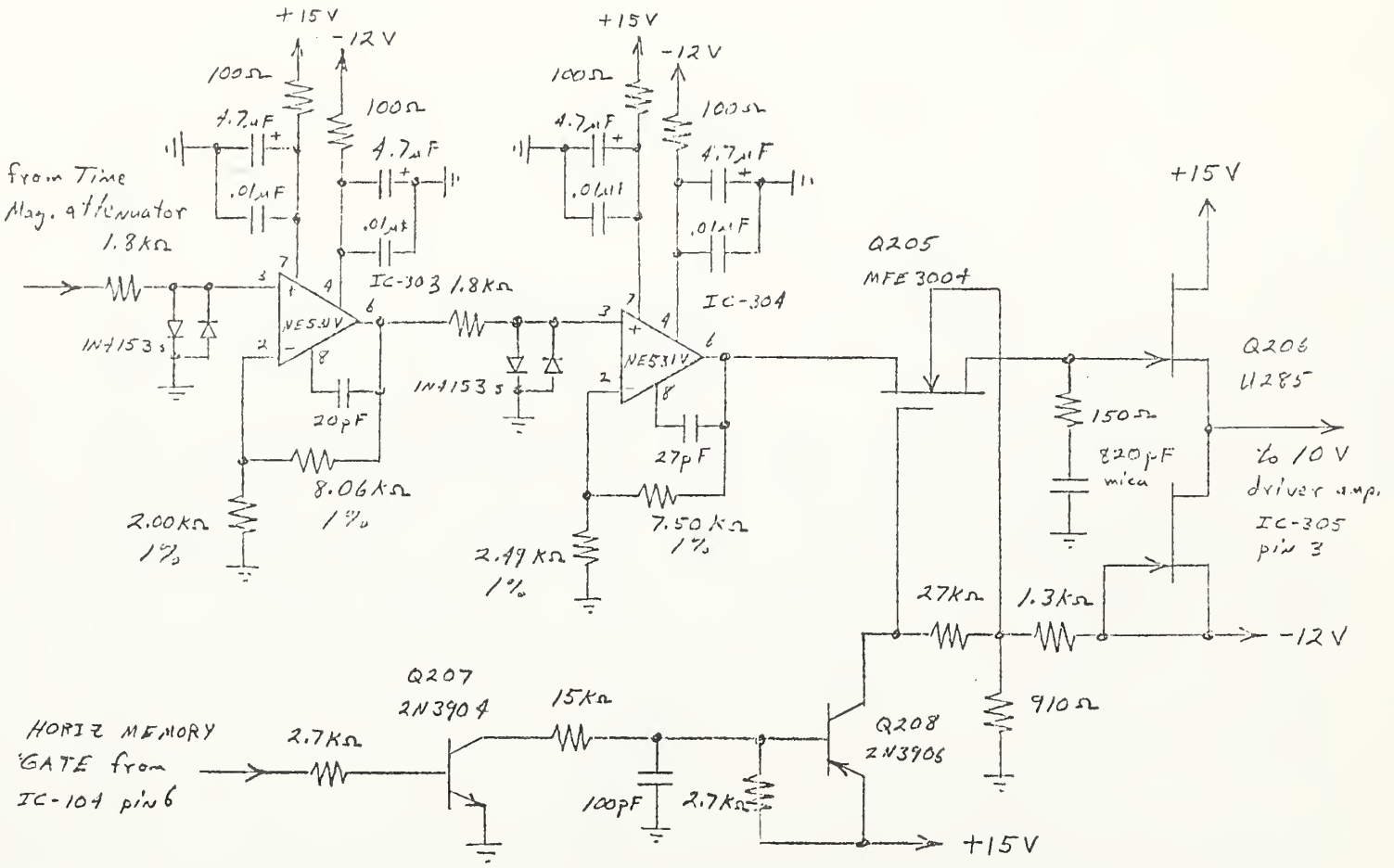


Figure 5-8. X5, X4 amplifiers and horizontal memory.

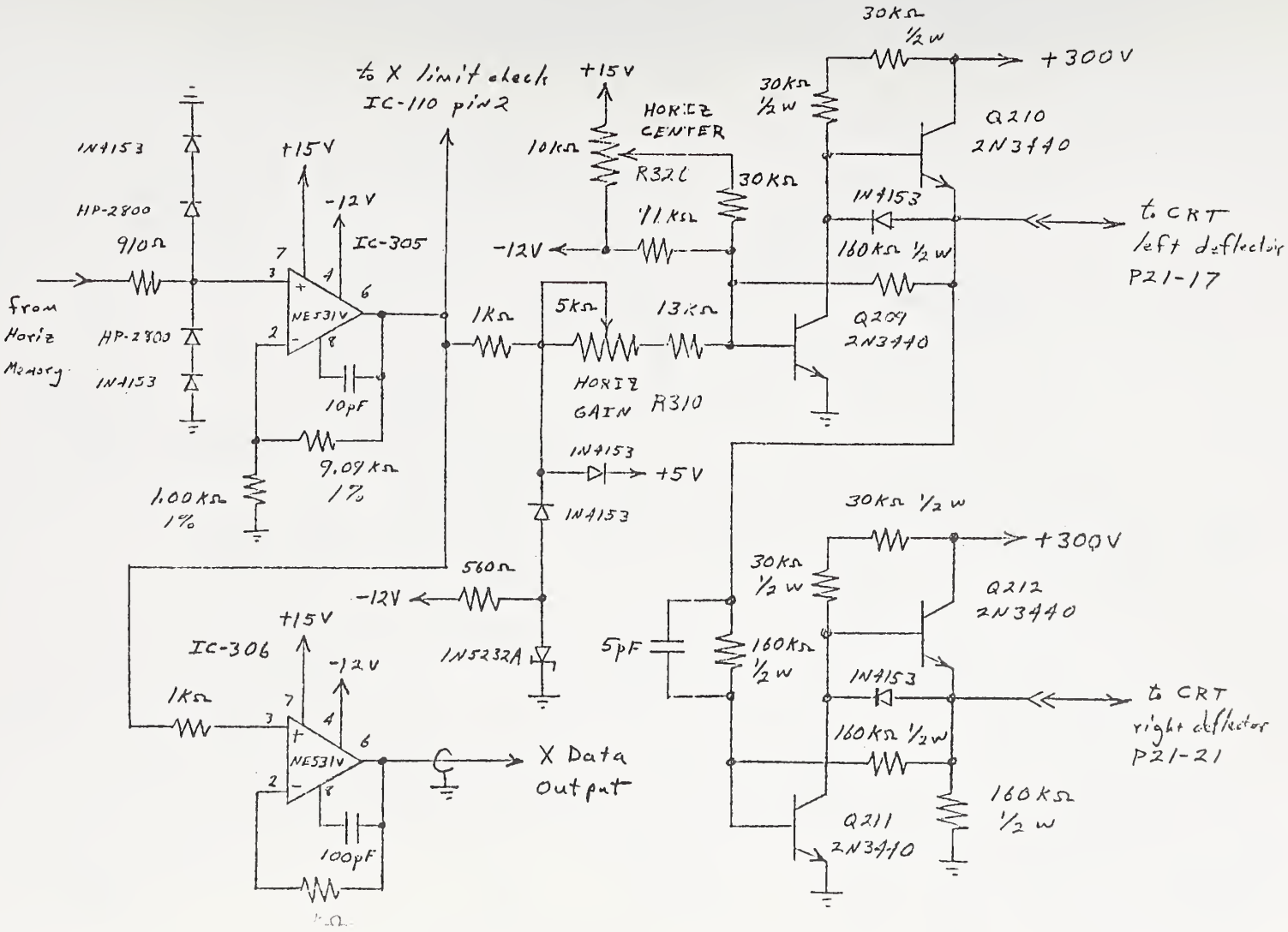


Figure 5-9. Driver and push-pull final amplifiers.

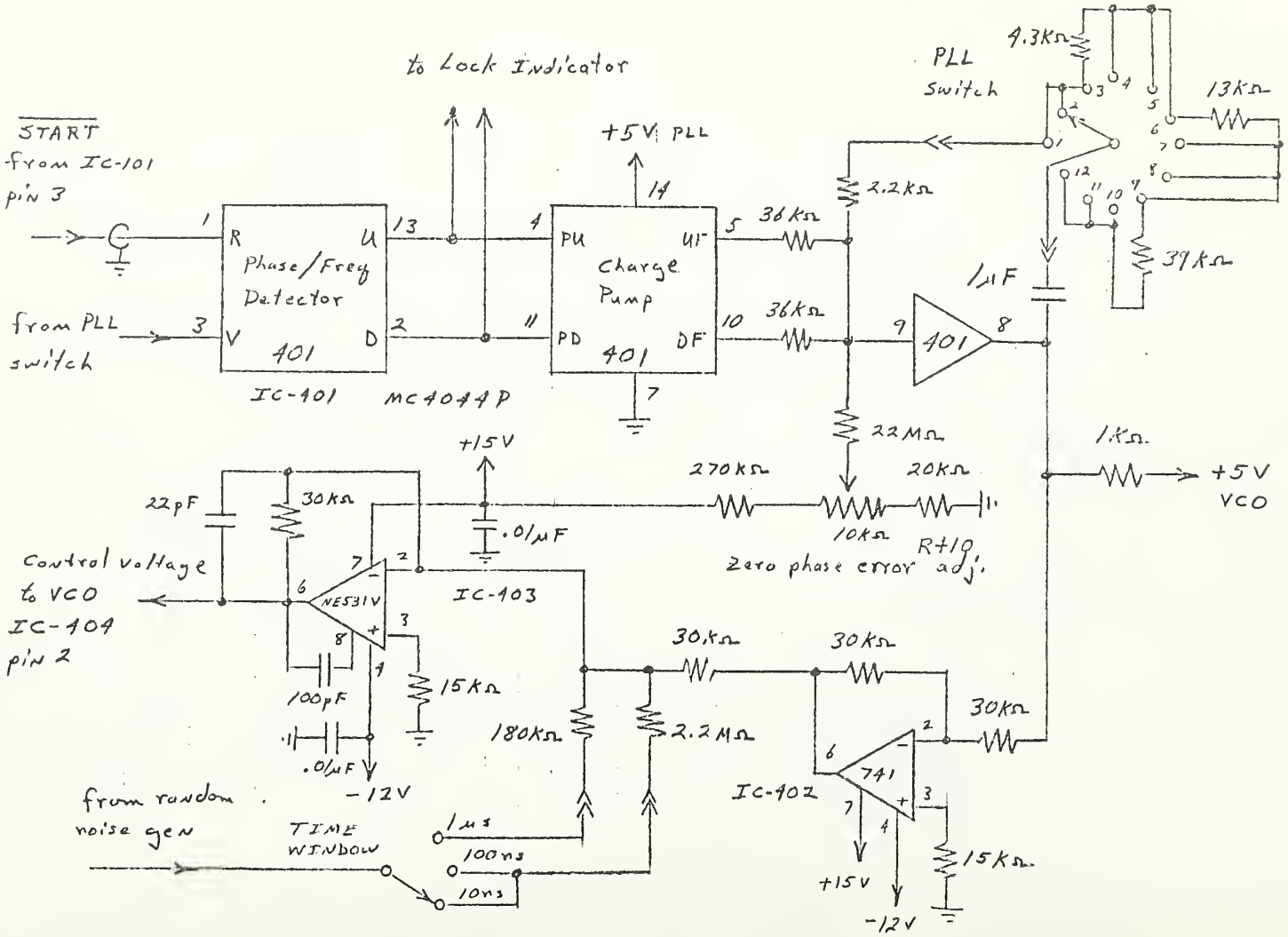
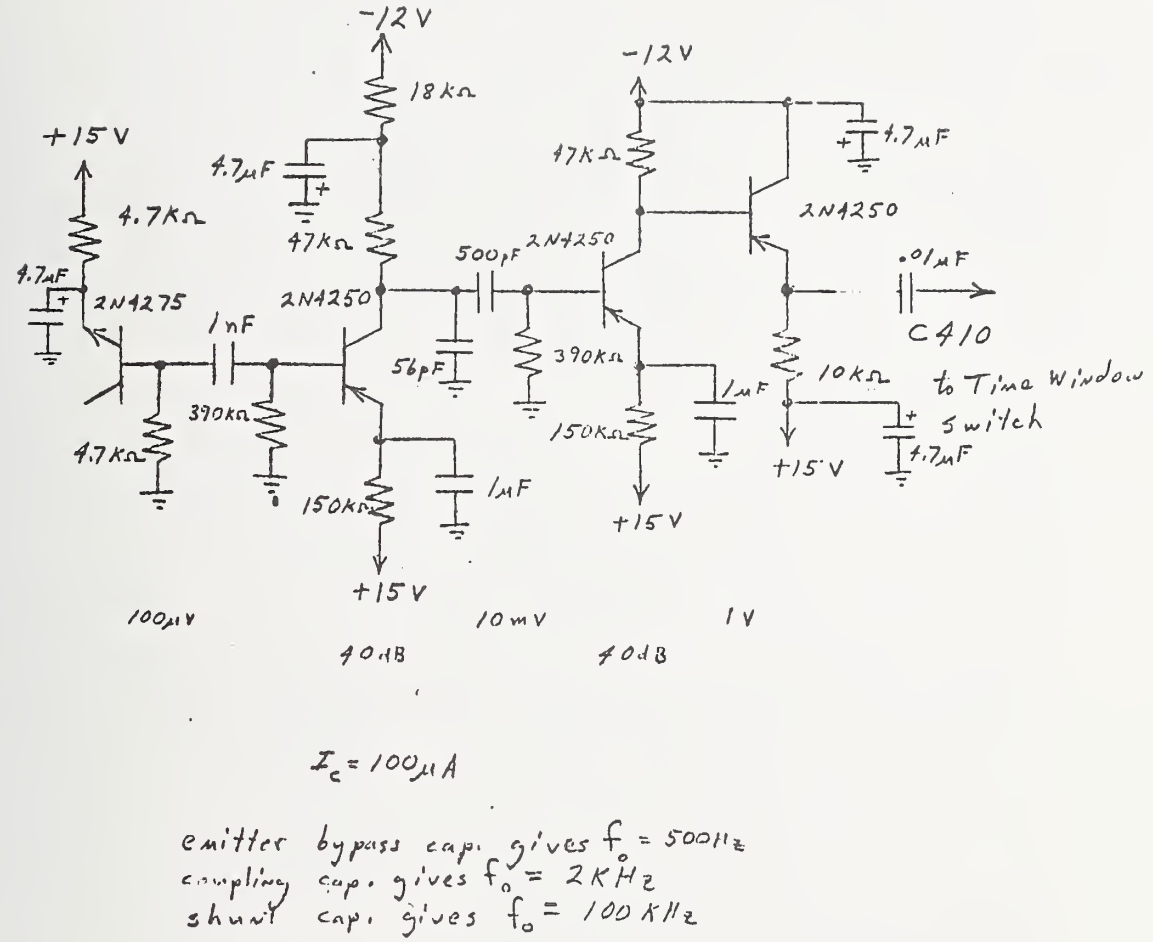


Figure 5-10. PLL phase/frequency detector and control loop.



$I_c = 100 \mu A$

emitter bypass cap. gives $f_o = 500 Hz$
coupling cap. gives $f_o = 2 KHz$
shunt cap. gives $f_o = 100 KHz$

Figure 5-11. Noise generator.

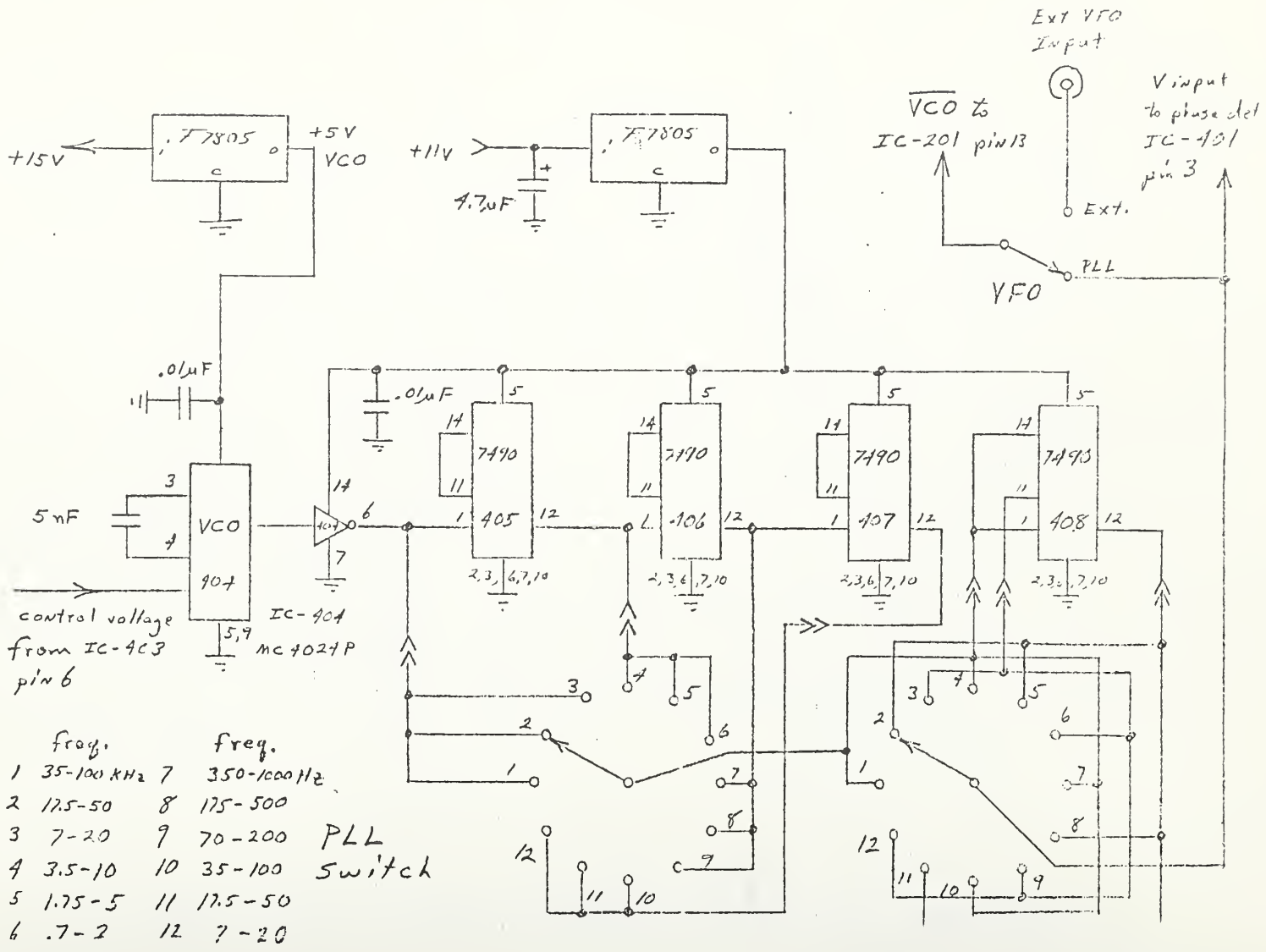


Figure 5-12. Voltage controlled oscillator (VCO) and frequency divider chain.

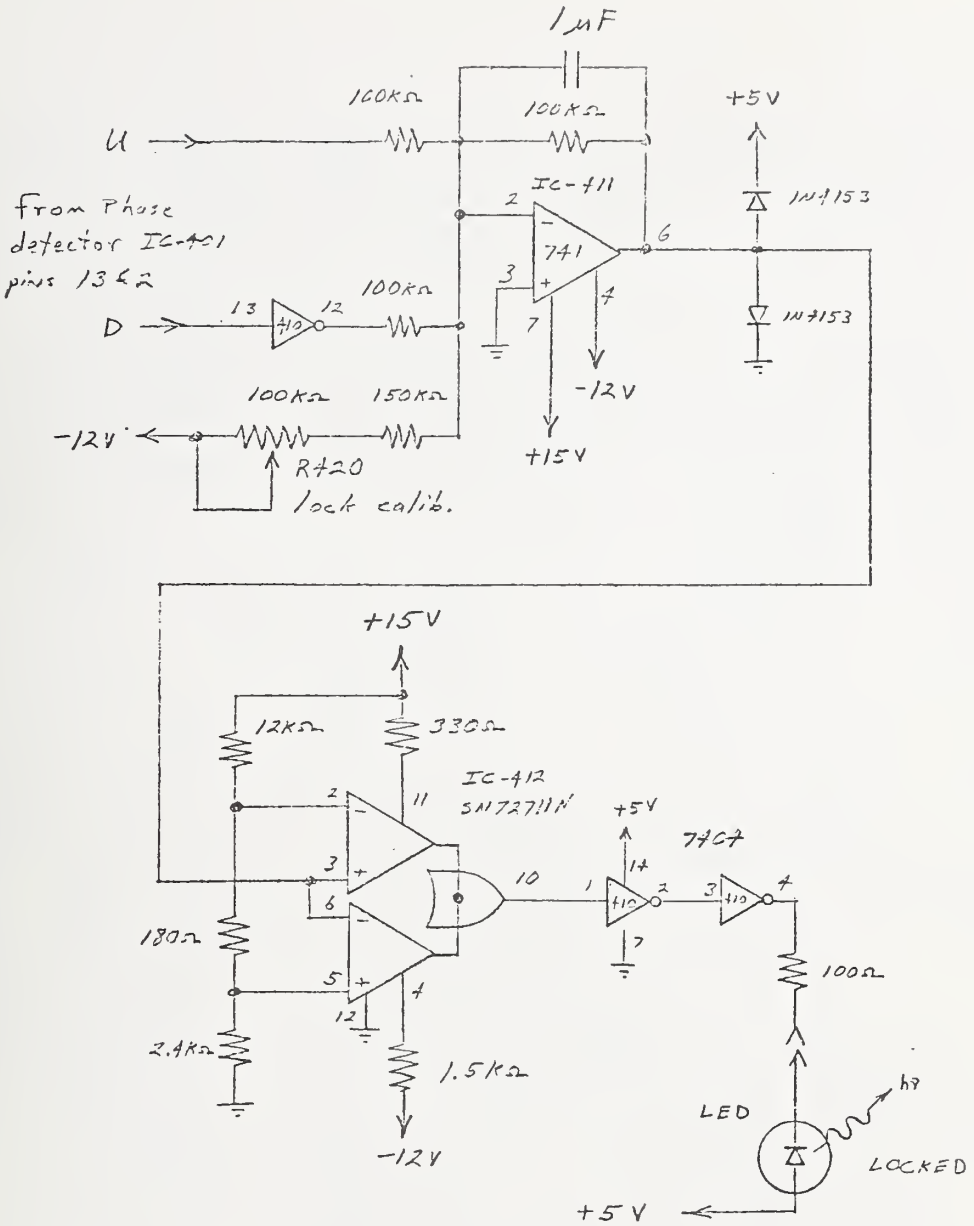


Figure 5-13. PLL lock indicator.

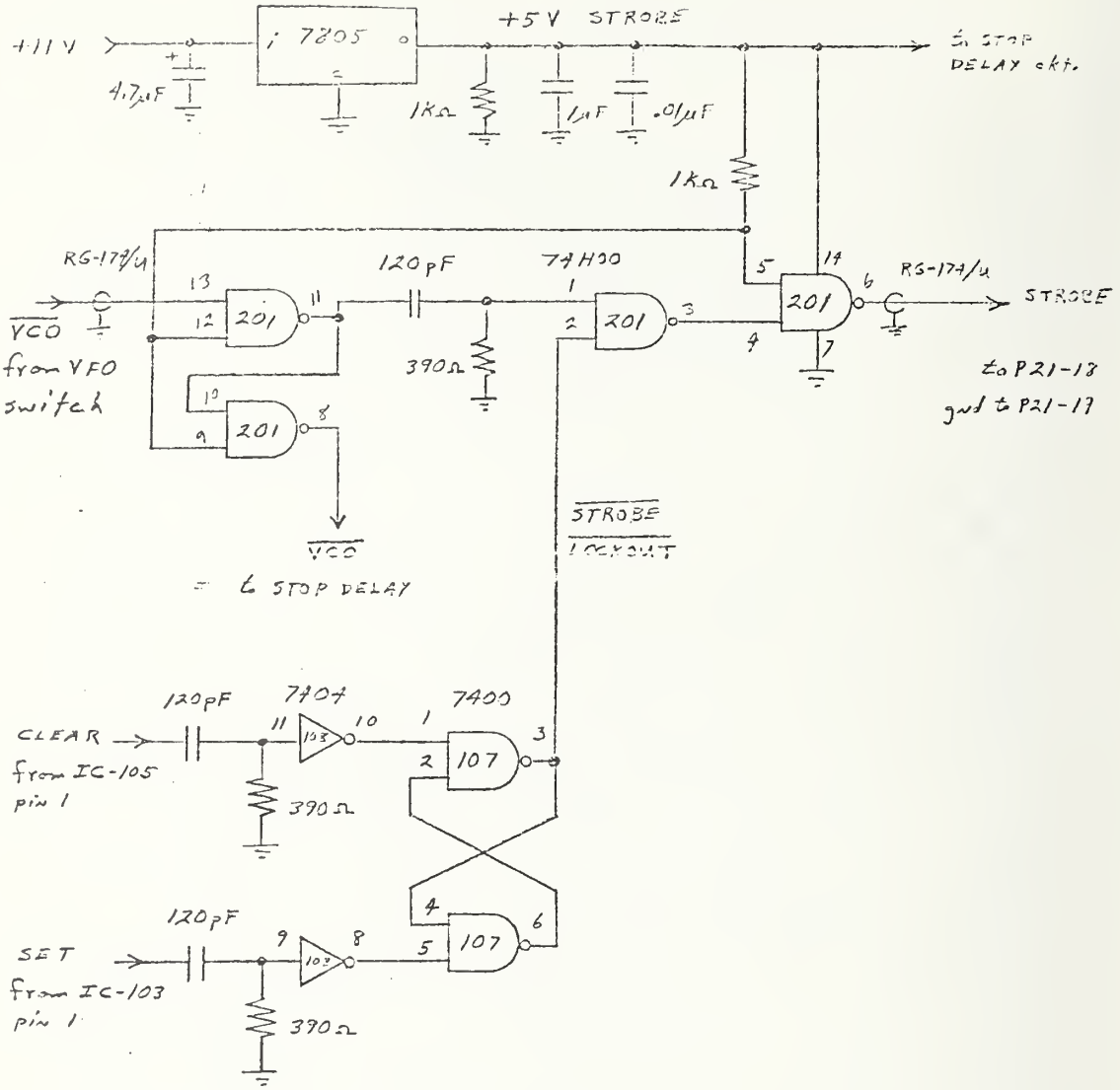


Figure 5-14. Strobe.

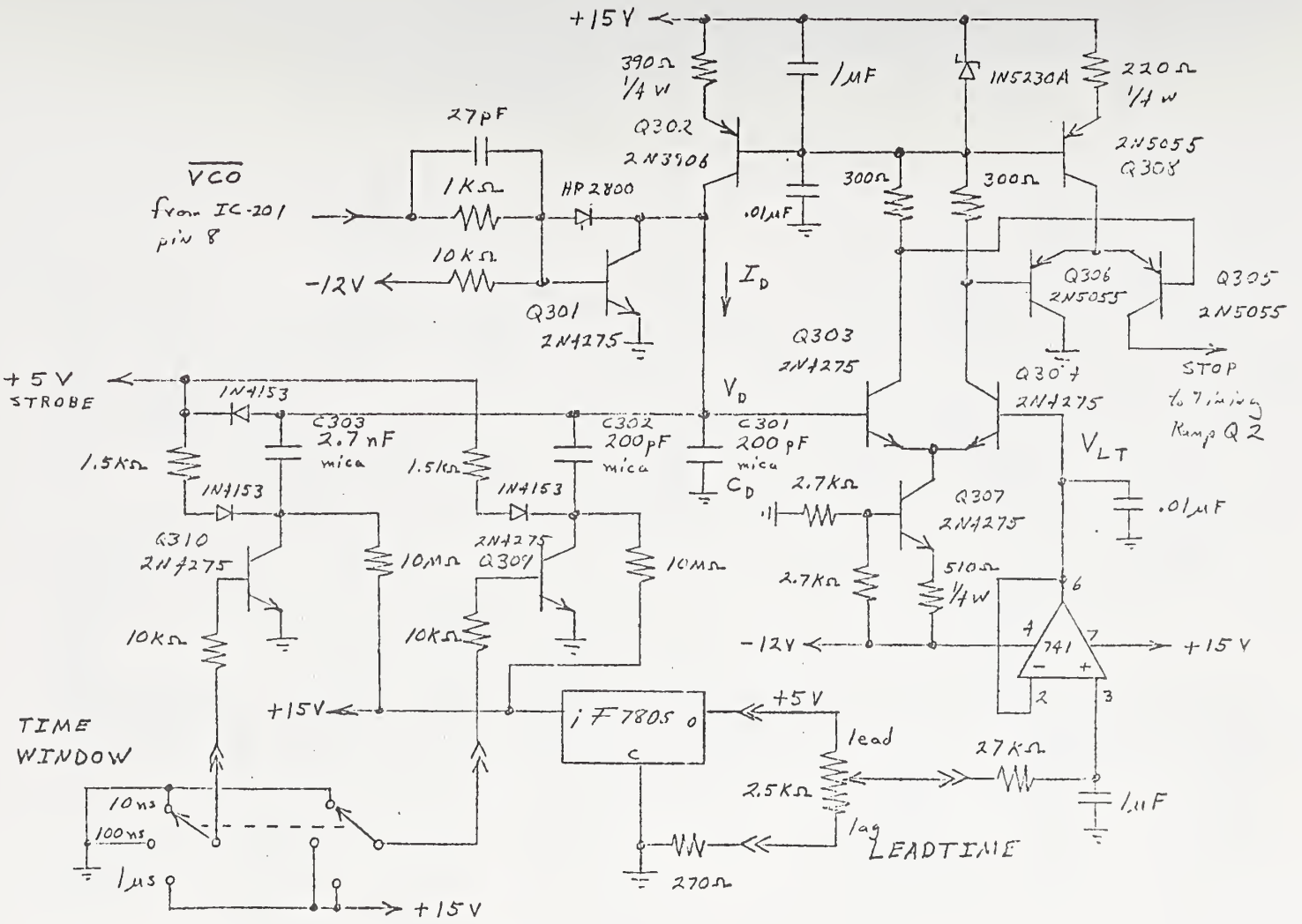


Figure 5-15. Stop delay.

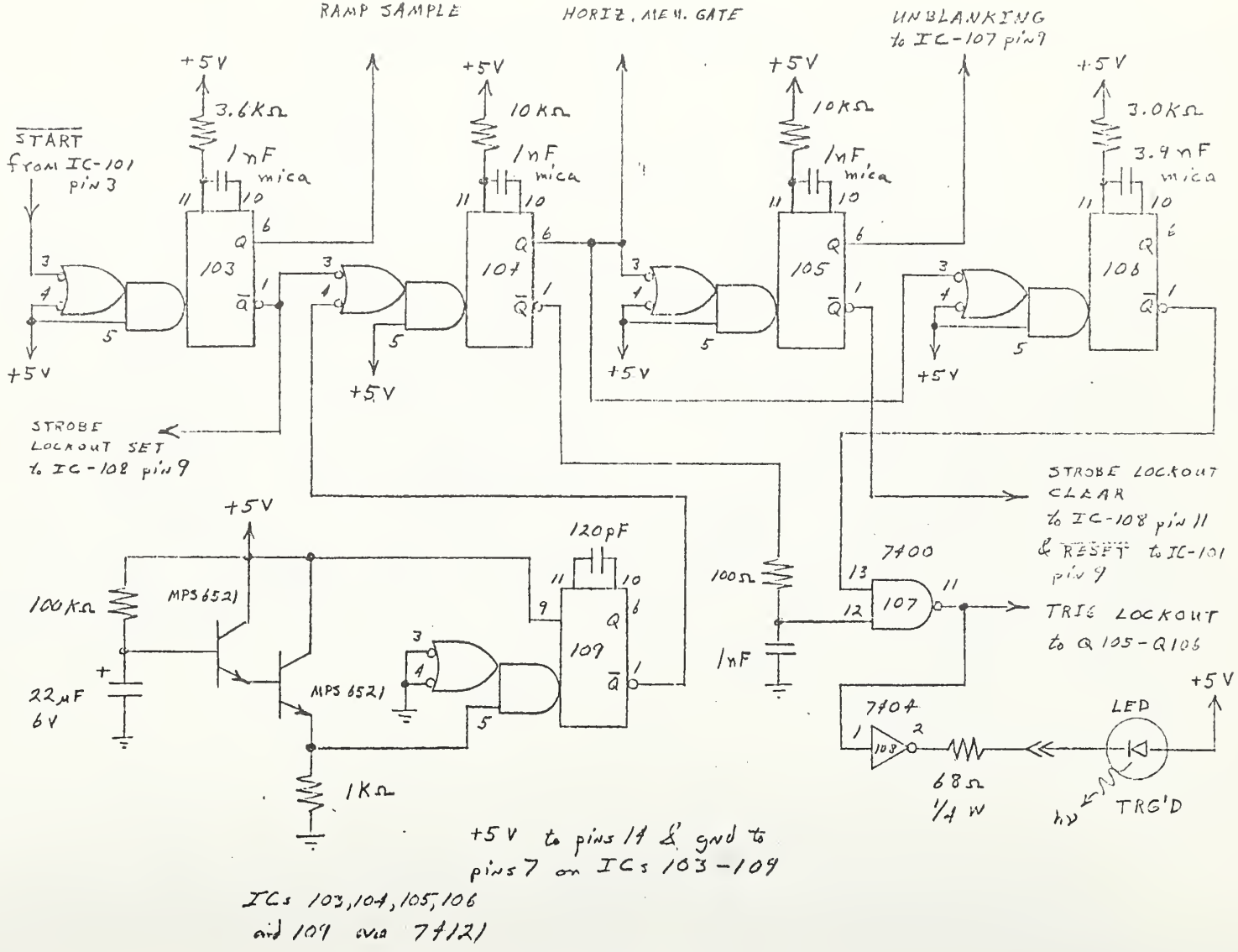


Figure 5-16. Data sequencer.

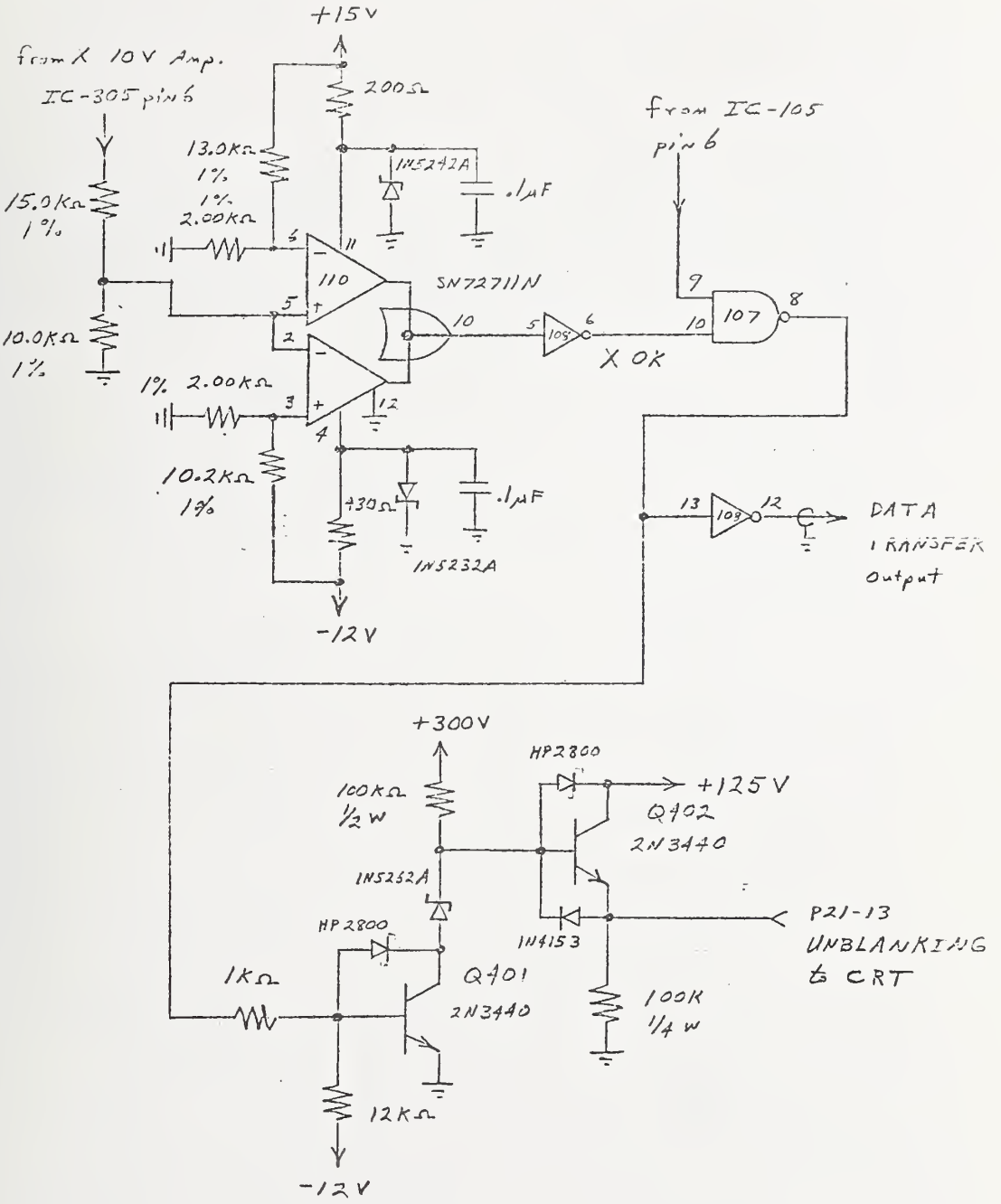


Figure 5-17. Unblanking.

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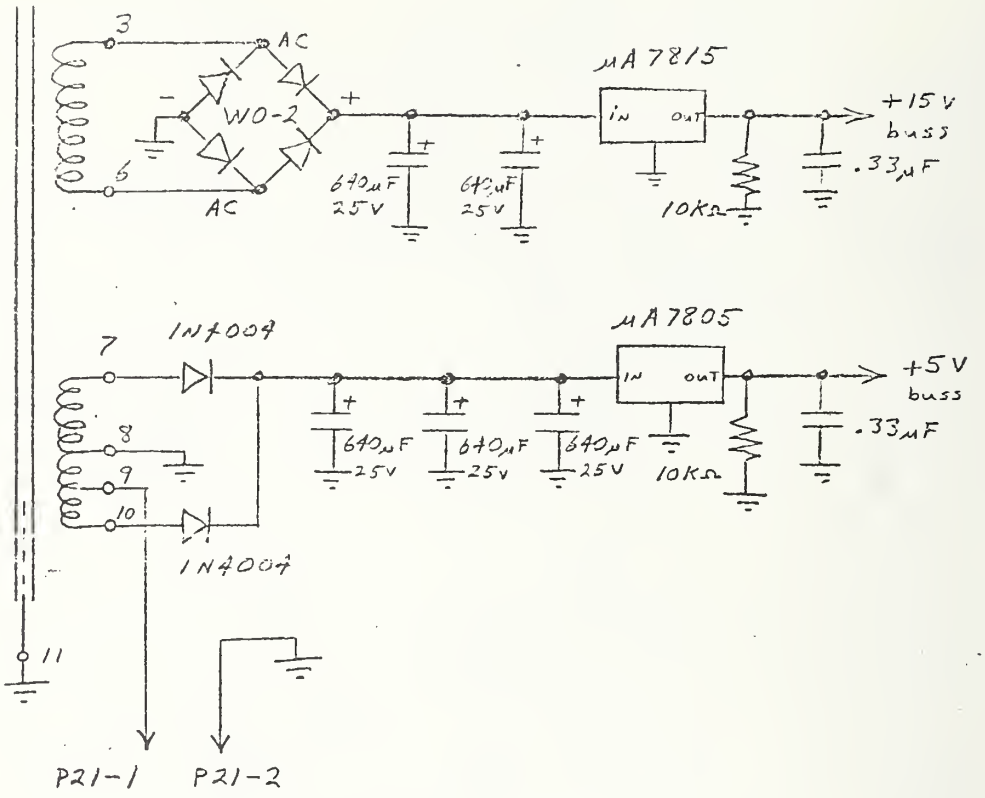
Company TEC – 0801-000



Note: The regulators (μA7805 & μA7815) are to be mounted on chassis using insulating washers.

Figure 5-18. +5 V and +15 V power supplies.

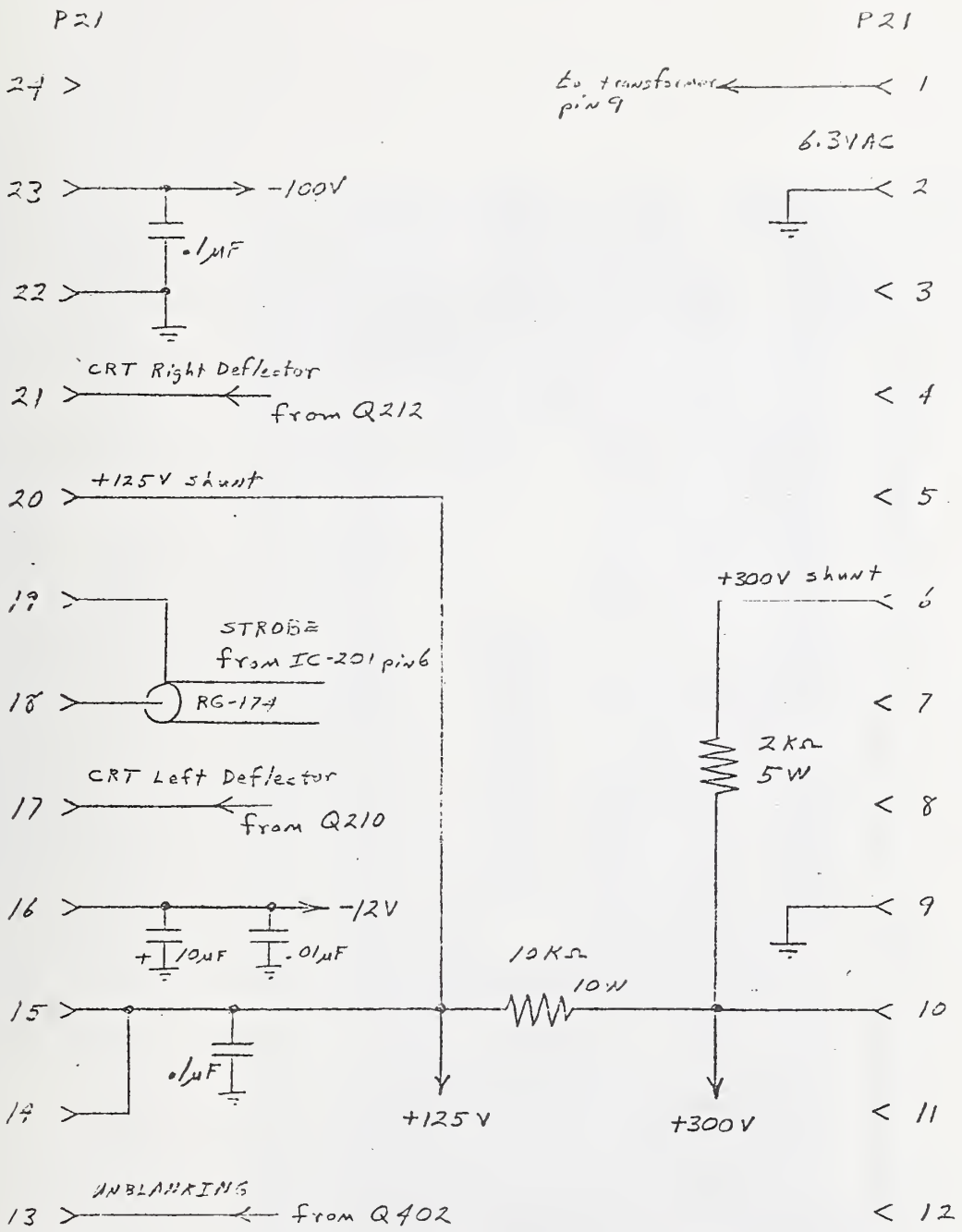


Figure 5-19. P21 plug-in connector.

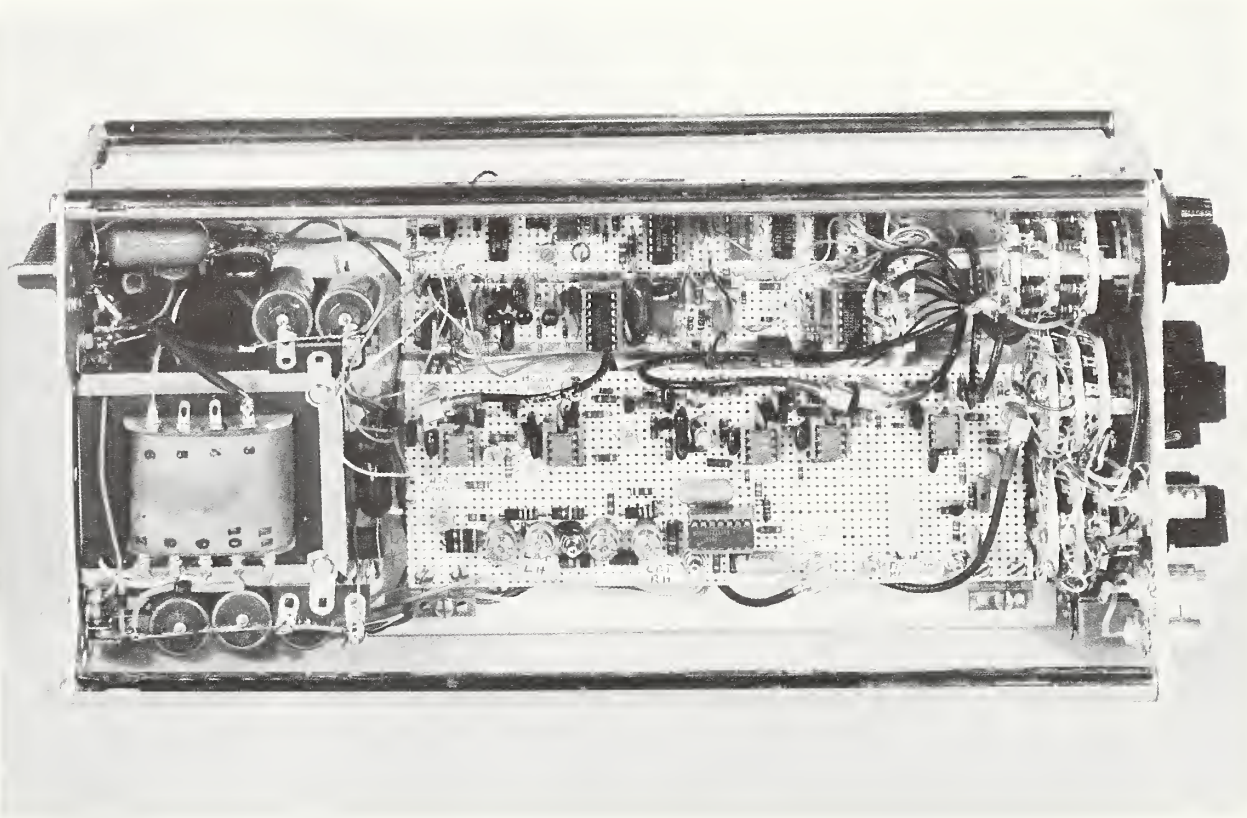


Figure 5-20. View of right side of plug-in. This view shows the power supply at the left. The board at the top is the strobe predictor circuit. The bottom board is the horizontal amplifier.

6. OPERATING INSTRUCTIONS

6.1 Oscilloscope System

The random sampling oscilloscope system is configured as shown in figure 6-1. A mainframe with a bistable storage CRT is used. The NBS random sampling time base is inserted in the horizontal plug-in compartment. A dual-trace sampling unit is inserted in the vertical plug-in compartment. Sampling heads are then mounted in the two smaller plug-in compartments within the sampling unit. Sampling heads may be inserted directly into the sampling unit. The 20 ps, 28 ps, and 90 ps feed thru sampling heads from another manufacturer require an additional interface unit to mate with the sampling unit. The design and construction of this interface is fully described in reference [9]. The signal to be measured is applied directly to the input of the sampling head. A short 50 ohm coaxial cable routes the signal from the output of the feedthrough sampler to the 50 ohm trigger input of the time base.

6.2 First Time Operation

1. Assemble the system configuration as shown in figure 6-1.
2. Set the sampling unit controls as follows:

   Display Mode: Ch A

   Position: Midposition

   DC offset: Midposition

   Trig Out: A

Dot Response: Midposition

Units/Div.: 50 mV/div

Variable: Calibrated

Invert: Pushed in

Smoothing: Normal

3. Set the NBS time base controls as follows:

   Time Window: 1 μs

   Time Magnification: X1

   Time Position: 500

   Lead Time: Clockwise

   VFO: Int.

   PLL: 1

   Trigger Level: Clockwise

4. Turn on power and allow the equipment to warm-up. Adjust the CRT controls (intensity, etc.) until a free-running horizontal trace is visable and focused.

5. Connect a short 50 ohm coaxial cable from the sampling unit Trig. Out connector to the NBS time base Trigger Input.

6. Set the TRIGGER LEVEL control to 11 o'clock position. The trace should stop free-running and the LOCK and TRG'D lights should extinguish.

7. Using a 50 ohm coaxial cable, connect a pulse generator to the ch A sampler input. The pulse generator should supply a pulse of the following characteristics:

Amplitude: 100 mV into 50 Ω

Polarity: Positive

Baseline: 0 V

Transition Time: $\leq$ 5 ns

Duration: $\leq$ 100 ns

Repetition Rate: 50 kHz

8. If the system is performing properly, the CRT should display a 100 mV pulse. The TRG'D and LOCK indicator lamps should be ON.
9. The various controls may now be adjusted to obtain familiarity with their functions.

6.3 Triggering Considerations

The trigger circuit is designed to provide a matched 50 ohm input. It will trigger on positive polarity pulses in the range of 10 mV to 250 mV. Optimum triggering is obtained with pulses of 50 mV or greater. For negative polarity triggering an external pulse inverting transformer is necessary. The TRIGGER LEVEL control range is designed to give monostable trigger operation for positions counterclockwise from 12 o'clock. The monostable mode is used for low frequency signals. Clockwise from the 12 o'clock position, the trigger circuit is in an astable mode and produces a free-running trace. The astable mode is used to synchronize

with high frequency signals. Due to the anti-jitter circuit, no HF stability or trigger holdoff controls are necessary. Figures 6-2, 6-3, and 6-4 show examples of the low jitter, stable triggering possible.

To obtain the minimum display jitter it is necessary to disable the internal strobe predictor circuit by throwing the VFO switch to EXT and using an external square wave generator free-running at ≃ 100 kHz as the VCO signal. With the internal strobe predictor there is some undesired interaction between various circuits. The result is an increase in the display jitter from 20 ps to 150 ps.

6.4 PLL Operation

The strobe predictor (PLL) circuitry is utilized to increase the probability of valid data measurement and thus reduce the time required to make a measurement. This circuit is a phase locked oscillator that locks in frequency and phase with the incoming trigger signal. It is very simple to use.

1. Set the VFO switch to INT.
2. Set the PLL range switch to 1 (i.e. PLL frequency range of 35 kHz to 100 kHz).
3. Observe the LOCK indicator, lamp. When it is on, the PLL is locked and functioning properly.
4. If the lamp is off, continue to change the PLL range switch position until the lamp lights.

5. Wait 1 to 2 seconds at each position of the PLL range switch to allow the PLL to search and acquire lock.
6. For astable trigger operation, i.e. high frequency synchronization, leave the PLL range switch at 1 as the time base free runs at approximately 60 kHz.

6.5 Sampling Efficiency

For random sampling to work properly, it is an absolute requirement that the sampling head be adjusted exactly for 100% sampling efficiency. Figure 6-5 shows the results obtained for various sampling efficiencies. The sampling efficiency is easily adjusted by obtaining a display such as figure 6-5 and adjusting the front panel DOT RESPONSE control on the sampling unit. It is necessary to check and readjust the sampling efficiency (DOT RESPONSE) when changing the voltage range switch. When adjusted for 100% on one range, the efficiency doesn't remain 100% when the range is changed as shown in figure 6-6. The SMOOTHING control must be left in the NORMAL position.

Due to the extreme randomness in which voltage samples are taken, the elaborate "last sample" feedback system incorporated in modern sampling oscilloscopes is of no value in pure random sampling. Thus the maximum dynamic range for valid sampled data measurements is considerably reduced from the

± 1 volt range for sequential sampling. The random sampling dynamic range is typically of the order of 200 mV. For valid measurements, the maximum signal excursions must be kept within these limits.

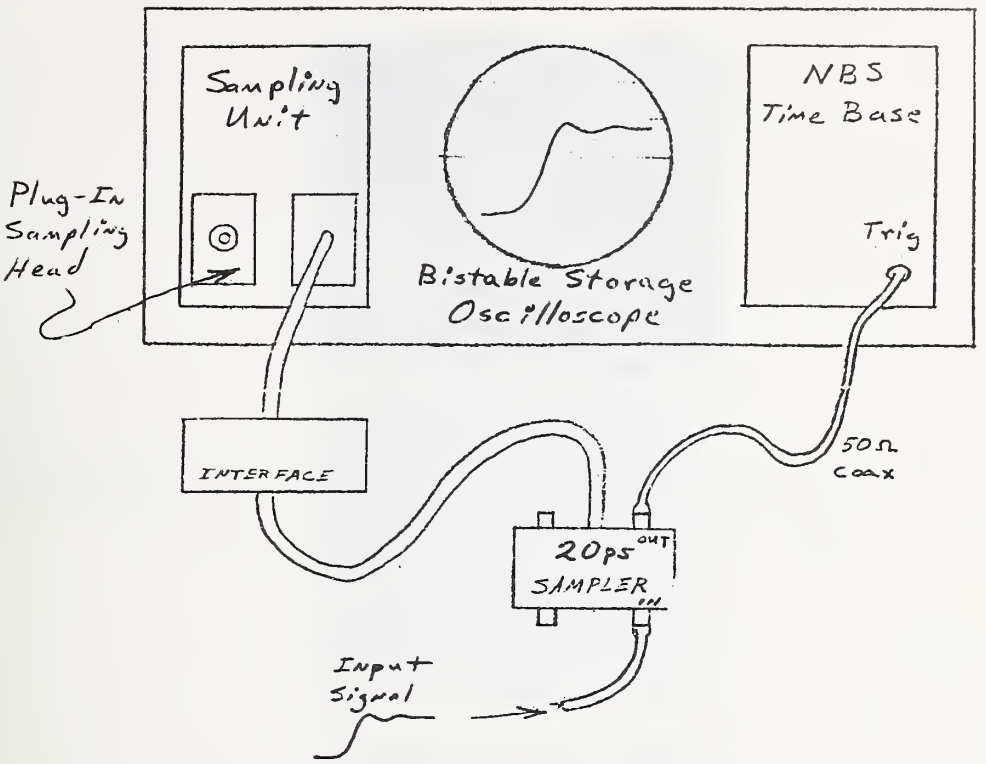
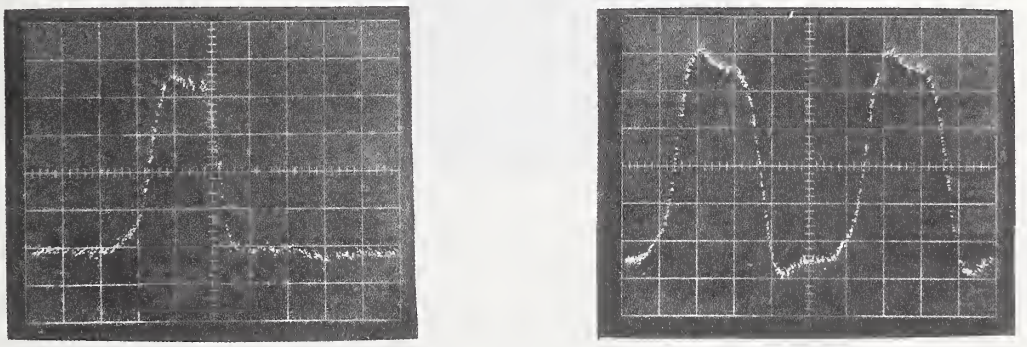


Figure 6-1. Random sampling oscilloscope system.



(a) (b)

Figure 6-2. Examples of trigger stability. 30ps sampling head. 20 mV/div. vertical, 1 ns/div. horizontal. 100 mV trigger pulse. (a) low frequency monostable operation, 50 kHz; (b) high frequency astable operation, 200 MHz.

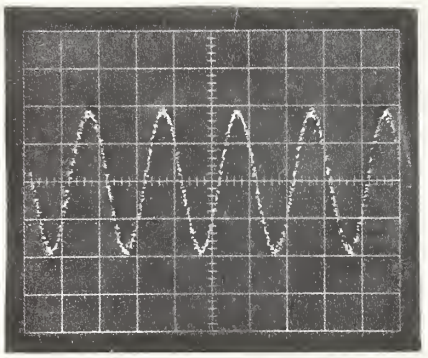


Figure 6-3. Example of trigger stability. 30ps sampling head. 20 mV/div. vertical, 5 ns/div. horizontal. 25 mV RMS, 100 MHz sine wave triggering.

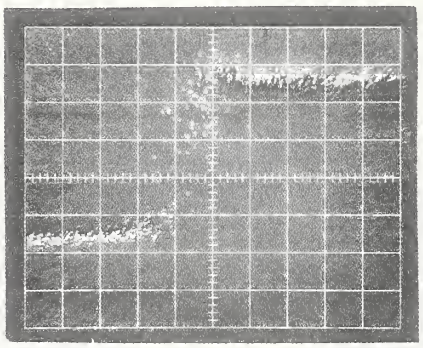
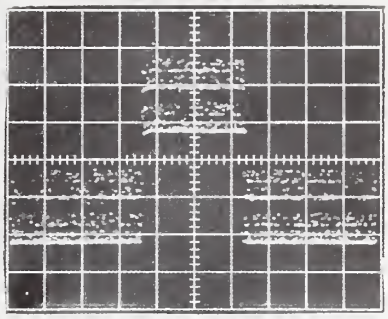
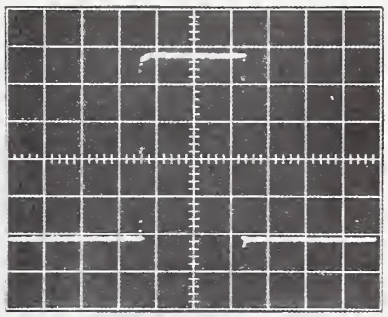


Figure 6-4. Example of trigger jitter. 20 ps sampling head. 20 mV/div. vertical, 20 ps/div. horizontal. The pulse from a very fast tunnel diode pulse generator is attenuated by a DC-18 GHz, 10 dB attenuator.

(a)



(b)



(c)

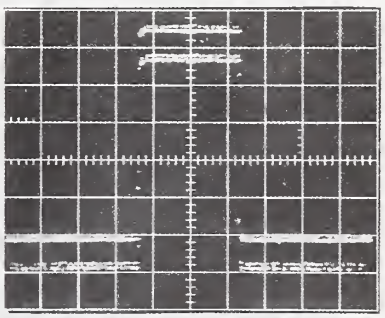
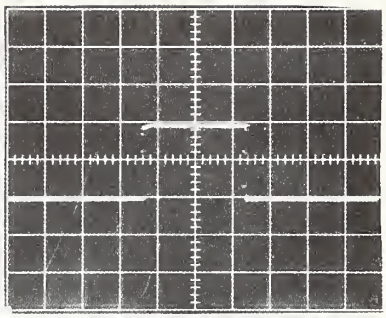
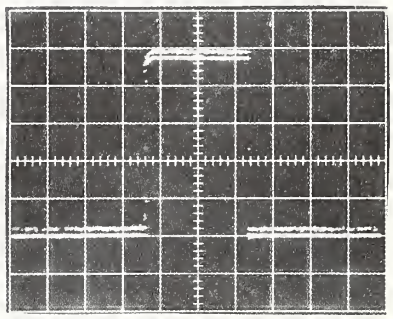


Figure 6-5. Random sampling measurements of a 100 mV, .3 μs pulse. 20 mV/div. vertical, .1 μs/div. horizontal. (a) sampling efficiency < 100%; (b) sampling efficiency = 100%; and (c) sampling efficiency > 100%.

(a)



(b)



(c)

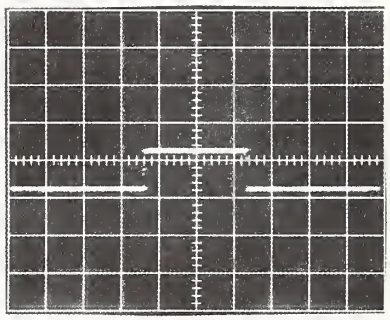


Figure 6-6. Effect of voltage range changes on sampling efficiency. .1 μs/div. horizontal. DOT RESPONSE adjusted for 100% sampling efficiency at 50 mV/div. (a) 50 mV/div.; (b) 20 mV/div.; (c) 100 mV/div.

7. CALIBRATION

Very few circuit adjustments are required for proper functioning of this instrument. This is due in large part to the use of precision 1% resistors in critical circuits. The circuits that must be adjusted and/or calibrated are the trigger anti-jitter circuit, strobe predictor, horizontal final amplifier, and the timing ramp.

7.1 General Setup

To perform all of these adjustments, assemble the system as shown in figure 6-1. For these adjustments the time base is connected to the oscilloscope mainframe by a plug-in extender cable. The time base remains outside of the mainframe cabinet to provide access to the adjustment controls. The equipment should be allowed to warm-up for at least twenty minutes before any adjustments are made. All front panel controls should be set as detailed under first time operation (see section 6.2).

7.2 Anti-Jitter Adjustment

1. Set all front panel controls as per section 6.2.
2. Connect a 100 mV peak-to-peak, 100 MHz signal to the 350 ps sampler input (ChA).
3. Set the TRIGGER LEVEL control fully counterclockwise to the 7 o'clock position.

4. Set the arming TD bias control R110 and the output TD bias control R120 completely clockwise (i.e. maximum bias current). The trace should now free-run.
5. Set the TIME WINDOW to 10 ns.
6. Set the TRIGGER LEVEL fully clockwise to the 5 o'clock position. The 100 MHz sine wave should now be approximately synchronized on the CRT.
7. Set the arming TD bias control R110 90 degrees counter-clockwise.
8. Slowly turn the output TD bias control R120 counter-clockwise. Note the setting of the control when a 3 ns jump of the position of the 100 MHz sine wave occurs, figure 7-1, continue to slowly turn the control until the trace stops. Note this new setting. Reset the control R120 to the midpoint between the two noted settings.
9. If the displayed sine wave is jittery, reset R110 ± 10 degrees. Repeat step 8. Continue this process of first resetting R110 and then R120 until a jitter free display is obtained.
10. Set TRIGGER LEVEL control to the 7 o'clock position and disconnect the trigger input signal. Check that the trace does not free-run. If it does, repeat steps 6, 7, 8, and 9.

7.3 Strobe Predictor Adjustment

1. Set up the front panel controls as detailed in section 6.2 under first time operation.
2. Connect a pulse generator to the 350 ps sampler (Ch A) supplying a pulse as detailed in section 6.2 step 7. The repetition rate of 50 kHz should be very stable such as that derived from a quartz oscillator. The TRG'D lamp should be on and a signal displayed on the CRT.
3. Connect the trigger output from the pulse generator to the external trigger input of the test oscilloscope. The test oscilloscope is a general purpose real-time oscilloscope with a 10 MHz or greater bandwidth. A 150 MHz oscilloscope was used to obtain the example shown later.
4. Connect one 10X probe from the test oscilloscope to the V input of the phase/frequency detector (IC-401, pin 3). Connect the other 10X probe to the R input (pin 1).
5. Set the test oscilloscope to 0.2 V/div vertical and 50 ns/div horizontal. Set the trigger to external.
6. With a clip-lead, ground the noise input to the PLL, i.e. between C410 and the TIME WINDOW switch.
7. If the PLL is functioning properly, waveforms similar to figure 7-2 will be obtained on the test oscilloscope. The broadening of the V waveform negative going transition is due to the inherent phase jitter of the PLL.

8. Adjust the zero phase error adjust R410 to center the V negative transition on the R negative transition.
9. With the PLL locked (fig. 7-2) adjust the PLL lock indicator R420 to turn on the LOCK lamp.
10. Disconnect the grounding clip lead from C410 and the 10X probes from V and R.

7.4 Horizontal Final Amplifier Calibration

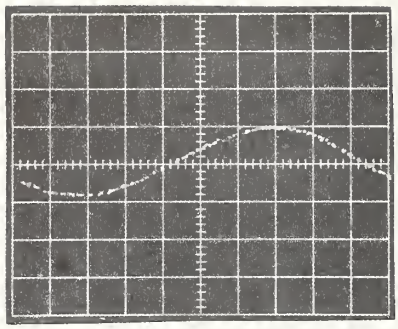
1. Set up the front panel controls as detailed in section 6.2.
2. Do not apply any signal to the sampler.
3. Set the TRIGGER LEVEL control to the 5 o'clock position to obtain a free-running horizontal trace.
4. Adjust the horizontal gain R310 to obtain a trace exactly 10 divisions long.
5. Adjust the horizontal centering R320 to center the trace on the CRT.

7.5 Timing Ramp Calibration

1. Set up the front panel controls as detailed in section 6.2.
2. Connect a 100 mV peak-to-peak, 10 MHz pulse or sine wave to the 350 ps sampler.
3. Adjust the TRIGGER LEVEL control for a stable display.
4. Adjust the 1 μs calibration R10 for 1 marker per division on the CRT.

5. Change the TIME WINDOW to 100 ns.
6. Change the 100 mV input signal to 100 MHz.
7. Adjust the TRIGGER LEVEL control for a stable display.
8. Adjust the 100 ns calibration R20 for 1 marker per division on the CRT.
9. Change the TIME WINDOW to 10 ns.
10. Change the 100 mV input signal to 200 MHz.
11. Adjust the TRIGGER LEVEL control for a stable display.
12. Adjust the 10 ns calibration R30 for 1 marker per 5 divisions on the CRT.

(a)



(b)

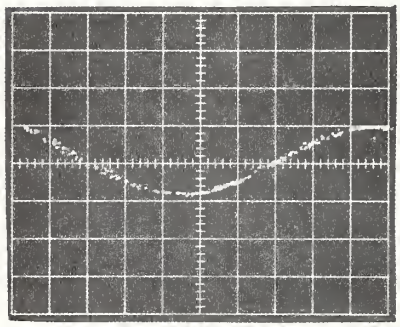


Figure 7-1. Output TD bias adjustment R120 effect. 100 MHz sine wave. 1 ns/div. horizontal. (a) R120 completely clockwise, i.e. free-running condition; (b) R120 slowly turned counterclockwise, point at which trace jumps 3 ns.

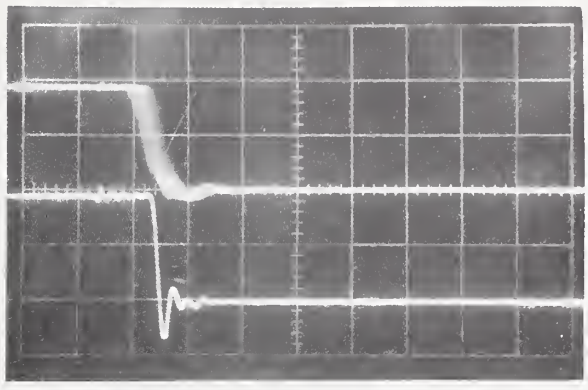


Figure 7-2. PLL locked condition. 2 V/div. vertical, 50 ns/div. horizontal. Top trace is V (VCO) input to phase/frequency detector. Bottom trace is R ($\overline{\text{START}}$) input. Oscilloscope was triggered by R.

8. CONCLUSIONS

This report has described in detail the design, operating instructions, and calibration procedures for a random sampling oscilloscope time base. The principal features of this instrument are its ability to function with very low repetition rate signals of 10 Hz or less and its excellent long term stability of 15 ps/hr. permitting single measurements of several hours in duration. The instrument may be used with various commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using a time magnifier, the fastest sweep rate is 10 ps/cm.

REFERENCES

[1] F. Meyer, "Impulsessplatz Mit Einer Zeitanflösung Von 18 ps" (Pulse Measurements with Resolution Time of 18 ps), in German, Electronics Letters, Vol. 6, Oct. 29, 1970, pp. 703-704.

[2] N.S. Nahman, "The Measurement of Baseband Pulse Risetimes of Less than 10^{-9} Second," Proc. IEEE, Vol. 55, No. 6, June 1967, pp. 855-864.

[3] G.J. Frye and N.S. Nahman, "Random Sampling Oscillography," IEEE Trans. on Instrumentation and Measurement, Vol. IM-13, No. 1, March 1964, pp. 8-13.

[4] James R. Andrews, "Improved Bias Supply for Tunnel-Diode Picosecond Pulse Generators," IEEE Trans. on Instrumentation and Measurement, Vol. IM-19, No. 3, Aug. 1970, pp. 171-175.

[5] J. Mulvey, A. Zimmerman, J. Weber, and J. Bookout, Sampling Oscilloscope Circuits, Tektronix, Inc., Beaverton, Oregon, 1st Ed. 1970, pp. 140-147.

[6] N.S. Nahman and R. L. Wigington, "A Technique for Synchronizing Oscilloscope Displays," Proc. IEEE, Vol. 51, No. 10, Oct. 1963, p. 1371.

[7] M. Bertolaccini and S. Cova, "Automatic Hold-Off Adjustment to Avoid False Triggering of Oscilloscope Time Base," IEEE Trans. on Instrumentation and Measurement, Vol. IM-22, No. 1, March 1973, pp. 92-94.

[8] Floyd M. Gardner, Phaselock Techniques, New York, John Wiley & Sons, Inc., 1966.

[9] James R. Andrews, "An Interfacing Unit for a 28 psec Feedthrough Sampling Head and a Random Sampling Oscilloscope," Review of Scientific Instruments, Vol. 42, No. 12, Dec. 1971, pp. 1882-1885.

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)

With the advent of new miniaturized mercury (Hg) switches with reputed transition times of the order of 10 picoseconds, interest has been rekindled in their use in high speed pulse measurements. Since there is no pre-trigger signal available from a Hg switch, normal sequential sampling techniques are not usable to measure the fast Hg switch transition time. For this reason a new random sampling time base unit was designed to perform these measurements at the low repetition rate of Hg switches (< 100 Hz). The time base may be used with commercial sampling oscilloscope systems through suitable interconnection terminals or possible interface equipment. It features three selectable time windows of 1 μs, 100 ns, and 10 ns. Using its time magnifier, the fastest sweep rate is 10 ps/cm. A variable trigger lead time control is provided. The trigger sensitivity is 10 mV. The long term timing stability of the time base is excellent with less than 15 ps/h drift.

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