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JOYCE LEKAS EDITOR 6601 50/462 DAVE K. MORTON ASSOCIATE EDITOR 6071

THE INSIDE STORY

THICK FILM PROCESSING

Just as people are given the labels thin and fat, hybrid circuits are similarly classified. Thin films are usually deposited through the vapor phase (i.e. evaporation, sputtering, chemical vapor deposition). Consequently, they are very thin, usually only a few hundred angstroms.

'Fat' films, (as friends in the thin film areas call them), or thick films, as the rest of the world knows them, are from 10 to 50 microns thick when dried. They are deposited from a collodial suspension of metal, resistive oxide, and/or glass particles. The particles are squeezed through photo etched holes in a film covered screen, and onto a substrate. These dried deposits are then fired to remove organics, to bond them to the substrate, and to solidify the particles into conductive or resistive films. Since the process, commonly called silk screening, dates back to Roman times, one would think that by now it would be a well defined science. The contrary is the case. Screen printing is still more of an art than a science.

We would like to describe some of the processing details of making thick film microcircuits.

To illustrate this processing, a hypothetical hybrid part will be defined and built, at least in the text. It will consist of 15 resistors requiring 2 different resistivity pastes, 3 thick film capacitors, 4 chip capacitors, and 2 IC's. Since the hybrid will be plugged into a circuit board using soldered pins, 2 different conductor materials will be necessary; gold for die and wire bonding, and platinum–gold or palladium–silver for soldering. For this many circuit elements, a 1 x 1½ x 0.025 inch substrate is about the minimum size practical for thick filming. If many more circuit elements were required, thin film circuits should be used.

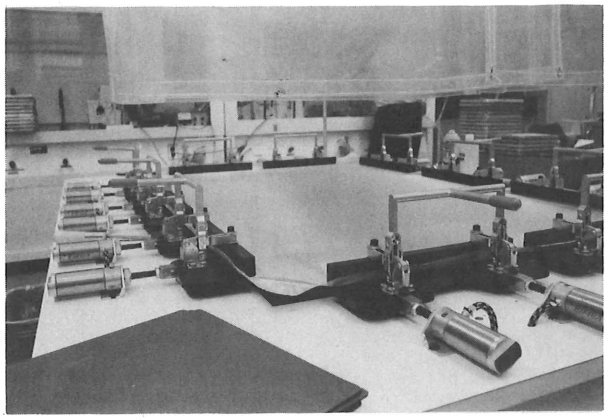


figure 1 Stretching the silk screen material. Screen shown is about four by six feet. Apparatus is all Tek-made.

Artwork

The first step in developing our hybrid circuit is to translate the circuit diagram into a layout of elements, drawn at 10x to 20x magnification. One of the 5 EE's in the Hybrids Design group would handle this task. This layout drawing is then used to cut a rubylith of each layer of the artwork. Conductor and resistor patterns are divided so that the desired materials are most efficiently used. These 'rubies' are then photo reduced to a 1x scale. This artwork is labeled and used to make master negatives and silk screen positives on an 8 x 10 inch mylar. New techniques for generating artwork being explored include both of the computer aided design systems available in engineering.

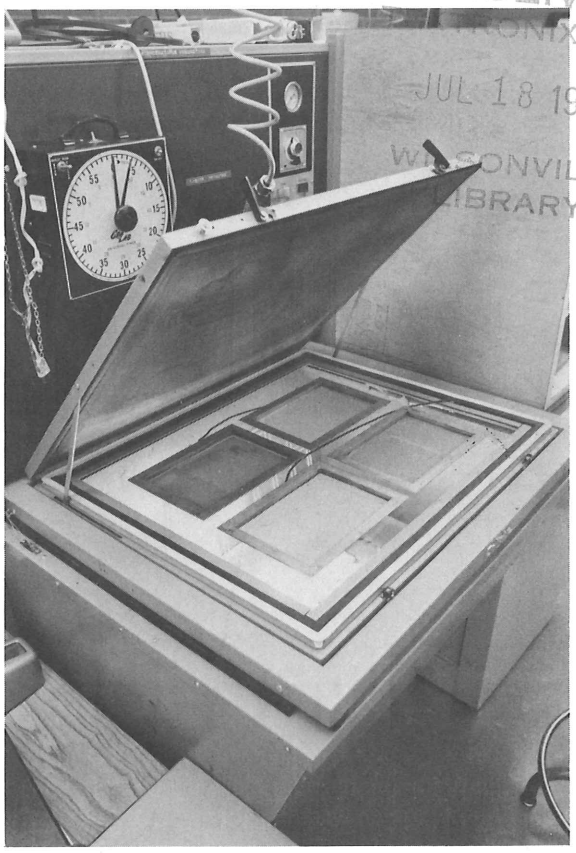


figure 2 Four individual screens (about 5 x 7 inches) ready for ultraviolet exposure. Normal exposure time is about 15 minutes.

Mask Making

After the artwork is thoroughly checked for errors of flaws, it is sent to the mask shop. The positive artwork is contact printed onto an ultraviolet (UV) curable emulsion to make screens. The areas not exposed are washed out of the screen, thus providing openings on which the paste will be deposited. (This same mask shop, run by Jim Parker, also stretches the screens and epoxies them to frames.) Now we have a set of screens for making our circuit. Let's examine the list.

1. No. 1 conductor (gold)
2. No. 2 conductor (solderable gold alloy conductor)
3. No. 1 resistor (low resistivity)
4. No. 2 resistor (high resistivity)
5. dielectric
6. resistor encapsulant

The resistor encapsulant is included so that our resistors will have higher stability, say 0.5 per cent end-of-life tolerance. This glass material can be cut by the laser or sand trimmed.

Printing

One rule that we presently cannot violate is that the resistors can only be fired once to their 850°C firing cycle. This means that the two resistors must be printed last, and co-fired. Any encapsulant must be fired to a much lower temperature. With this in mind, we start by printing, drying, and firing the gold conductor. Next we print, dry, print, and dry the dielectric. Depositing 2 layers greatly decreases the probability of shorts between the capacitor plates. The gold is used as the bottom plate. Now we print the top plates and solder pads with the solderable conductor. The dielectric and top conductors are co-fired again to decrease shorting, and increase yields.

Now comes the tricky part of 'fat' film processing; printing the resistors to the correct thickness (25 microns, dry) to obtain the correct sheet resistivity. To do this we use a surface profilometer (Talysurf 4) that accurately measures the dried film thickness. A few test parts are printed and fired before printing the entire run. These pieces are used to determine whether or not the resistivities are within a useful tolerance (trimming will increase resistivity). If they are too low, with not enough trim area available, or if they are too high, the resistors are rejected. The critical values vary with circuit design. Once the values are acceptable, the entire run is printed with the first resistor paste, and the parts are dried. The process is repeated for the second resistor paste. The entire run of parts is now fired through the standard 850°C, 50-minute cycle. It is imperative to maintain a constant firing cycle since the sheet resistivity of the paste is affected by both the firing temperature and the time at temperature.

Next we screen glass encapsulant over the resistors to protect them from the environment. This low temperature material (fired at 510°C) can be used as solder dams to prevent solder leaching of the gold, or excessive solder wicking.

figure 3 Printing the paste through the silk screen onto the substrate. Karen Sherwood controlling the process.

figure 4 Substrate with two-resistor printing ready for firing in 850°C oven for 50 minutes. Audrey Sinner loading substrates on the belt assembly.

Inspection

While inspection has not been mentioned until now, it is a routine part of the process. Any obvious flaws such as open or smeared conductor runs are immediately rejected. Alignment of the different layers is one of the most important parameters to watch while making parts. Entire runs have been rejected because of a poorly aligned encapsulant layer.

Trimming

Now the parts are either sand trimmed, or they leave the Thick Film area and go to Laser Trim. If active trimming is necessary (trimming to a desired level of circuit performance), the parts can be final-assembled in the Packaging group (Rod Chappel's), then sent for laser trimming. This Packaging group die and wire bond the IC's, place lids over them, solder the chip capacitors and other discretes, and attach pins for board insertion.

At last we have a hybrid circuit ready for an instrument. It should be noted that this was written from an engineer's point of view. Many times the initial design will be changed because of variations in resistivity caused by conductor-resistor interaction. Other times, new circuit requirements

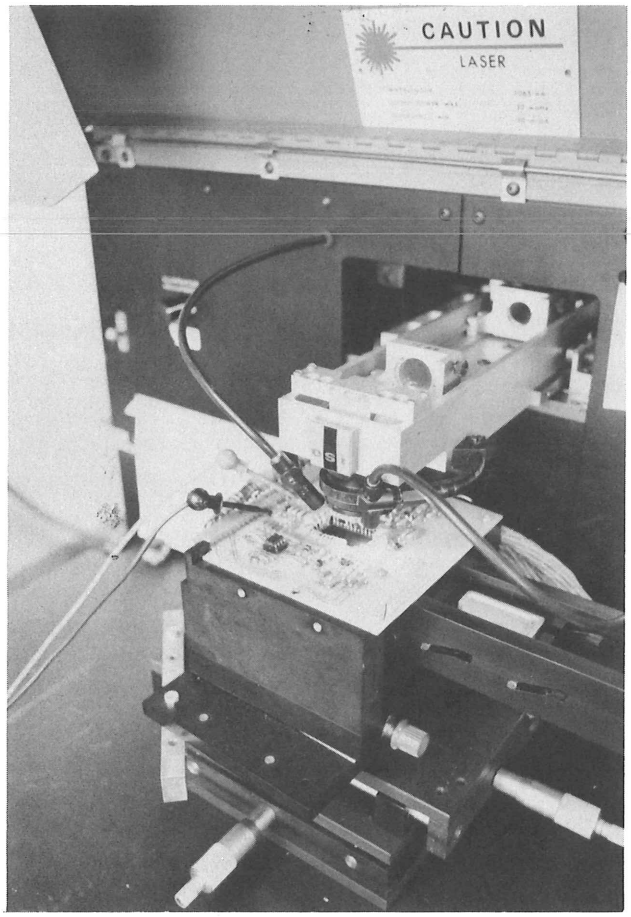


figure 5 Laser used in active resistor trimming.

will force change. Usually, parts are ready for packaging less than 10 days after receipt of artwork.

Cost

It is interesting to note that a part as described in this article would cost about $1.50 to $2 for the thick film, $8 to $20 for IC's (depending on their complexity), and about $2 for chip capacitors and pin attachments.

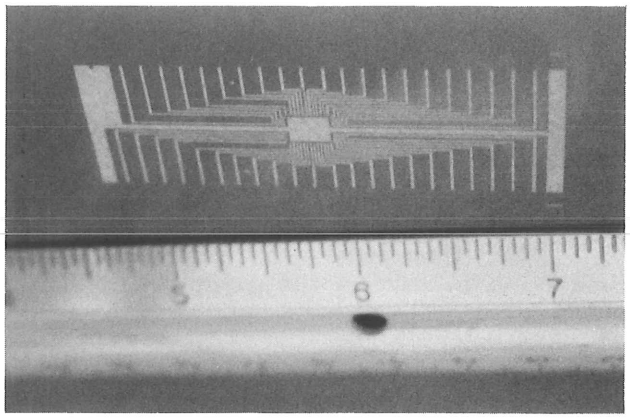
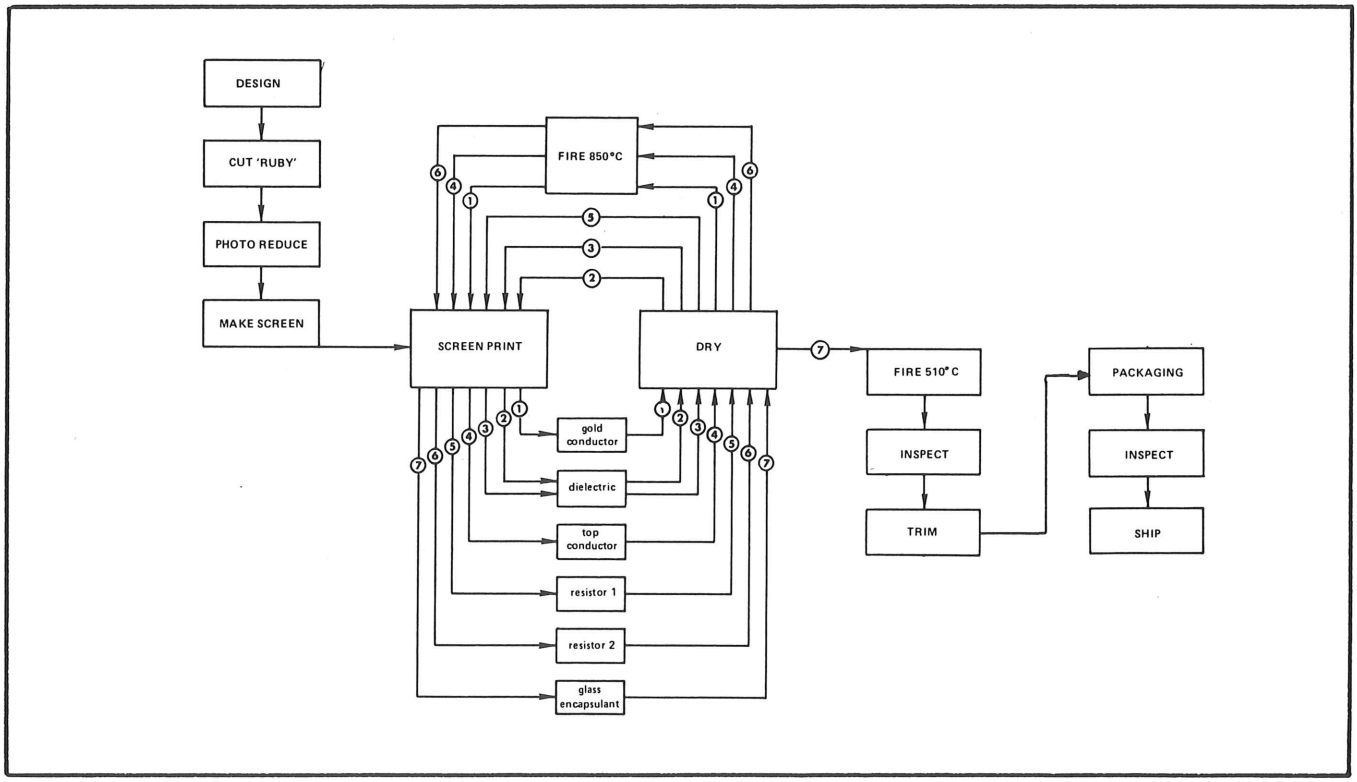


figure 6 Silk screen pattern showing fine resolution available with process.

This article has only described one type of 'fat' film part—a true hybrid. Several other classes of parts that are routinely made with thick films are high voltage dividers for CRT power supplies, attenuators for input selection, and thermal printers for alpha-numerical documentation. Resistor ladders, R-C networks, and potentiometers are also fabricated from thick films. The high voltage and power capabilities, coupled with reasonable production costs, make thick films an important part of Tek instrumentation.

If you have any questions of comments concerning thick films, please don't hesitate to contact me, Bob Burns, at ext. 6363, or any of the Hybrid Design group.

Editors Note: Consult issue 217 of COMPONENT NEWS for details on tolerances and values for Tek-made "fat films."



Williamson of MIT to talk

The Assistant Group Leader of MIT's Lincoln Labs Surface-wave Technology Group, Dr. Dick Williamson, will address IEEE's Portland Electronics Group at 7:30 p.m., May 15, in the auditorium of Building 50. He will speak on fabrication techniques for high resolution in surface acoustic wave and microelectronic devices. He will review advancements in photolithography techniques, lift off, electron lithography, X-ray lithography, ion-bombardment etching, and assess their advantages and disadvantages.

A dinner is scheduled for 5:30 p.m. at the Greenwood Inn in Beaverton before the meeting. For dinner reservations or further information, contact Gene Chao at ext. 7435.

Periodicals list available

Susan Steele of the library staff has compiled a revised list of the 322 periodicals regularly received by the library. Besides noting the earliest volume held of each major journal, the list includes a breakdown of titles into 15 separate subject categories. For example, one can see at a glance what periodicals deal with Optical Engineering, Material Science, Marketing, etc.

Copies are available in the library at 50-210, or call ext. 5388.

Here come the students

Once again this summer we will need places for out-of-town students to stay while they work here at Tek. There are fewer students than last year, but the need still exists. In particular, two young men from the Chalmers University of Technology in Gothenburg, Sweden will be with us for about eight weeks, and will need to know where they will be staying before they arrive. They will arrive on about the 5th of June and work for about eight weeks.

If you have a spare room and would be willing to rent it to one or more of these young engineers for the summer, call Dick Wells and give him your name, address, home phone and Tek extension. It may prove to be mutually educational. Dick is at ext. 7000.

How to break into print

ENGINEERING NEWS is always looking for information from engineers or engineering groups for publication. Have you something you'd like to see in print?

Write it down, and give us a call. (Often the best way to begin a story is to list all the basic facts and ideas in outline form.) One of our staff members will then help to arrange the material in its final form.

We have an available camera, as well as a fine graphic design service for making graphs, charts, diagrams, etc.

When you, or a member of your group of staff, want to see an article about your engineering operation, process, or product appear in ENGINEERING NEWS, call us at ext. 6071 or 6601.

Magnetics magnate to speak

Edward R. Cronk of Thomas & Skinner, Inc. will be at Tek on June 3 in the corporate council room, Building 50, from 10 a.m. to noon to talk about permanent magnets. His discussion will include basic magnetic theory, manufacturing methods, design considerations and limitations, and magnet testing.

Thomas & Skinner, Inc. is a manufacturer of permanent magnets, transformer laminations, magnetic tapes, and magnetic instruments.

For further information on this seminar, contact Bob Aguirre, ext. 7761.

A/D technology group formed

The Instrument Research Group of Tek Labs has been asked to coordinate the analog to digital converter needs of Tektronix. The purpose of this effort is to minimize duplication, yet to make sure that all real needs, both present and future, are being covered. In the coming weeks, the instrument research people will talk to groups at Tek about their needs, as well as catalog on-going A/D projects within the company.

If your group has specific questions or comments, please contact Gene Chao, ext. 7435 or 50-273.

The latest views on metrics

At the risk of being called 'visionary,' we continue to campaign for all-out conversion to the metric system in this country. Although we have met a few kindred souls who also abhor the disordered thinking that requires ordering 200 **feet** of 35 **millimeter** film, we usually find a large portion of the engineering profession growling, "We'll never do that."

China, popularly assumed to be a decadent nation, has outlawed the importation of machine tools calibrated in anything but the metric system. It's not illogical to assume that other countries will follow suit, avoiding the very confusion we are compelled to live with. Eventually, our machine tool manufacturers might be left holding their genuine antique foot-rules, wondering what happened to their foreign trade.

Obviously this change cannot be made overnight. However, we do feel that metric equivalents should be taught and stressed in our schools, from the primary grades up. We also feel that a good many engineers and production personnel should overcome the phobia that makes them resist this idea with the same unthinking fanaticism that greeted the establishment of time zones.

Editors note: This text was taken from an editorial in a 1949 issue of STANDARDS ENGINEERING.

Design Engineer Shares Circuit

by Bruce Campbell

In designing a power converter for charging an 8V battery from the line for the 230 miniscope series, I came upon a circuit that may be useful in a variety of applications.

I started with an inverter whose output power increased with frequency. In order to achieve regulation, I tried using a voltage-controlled pulse generator (VCP), to sense the output voltage and adjust the frequency of the inverter accordingly. Being an old unijunction transistor (UJT) fan, I figured I'd design a quick UJT relaxation oscillator and control it with an error amplifier, and I'd be home free.

Problems

Unfortunately, I'd overlooked a few details (as I often do). The relaxation oscillator had to have a frequency range of at least 30 to 1, which a UJT can do, but also needed a well defined upper frequency limit. Because it would always be connected to the batteries, it had to be a very low power circuit. If you're into UJTs, you know that the variance of intrinsic standoff ratio from device to device makes accurate predictability of the operating frequency of a UJT relaxation oscillator impossible. The final blow was power consumption, which was too large for me and not significantly alterable.

So how about programmable unijunction transistors (PUTs)? Well, these highly touted SCRs don't really have a decent turnoff mode, making a relaxation oscillator with the frequency range I needed impossible. The manufacturers suggest a modification for extending the frequency range, but I wasn't too excited about the extra two parts and frankly couldn't get the thing to work as they implied it would anyway.

So, with all these problems facing me, I set about trying to design a relaxation oscillator that would give me low power, predictable frequency of operation, and at least medium frequency range, which altogether, UJTs and PUTs can't offer. However, I did not wish to sacrifice the frequency vs supply voltage stability and circuit simplicity which UJT and PUT relaxation oscillators do offer.

Eureka

One morning the circuit came to me, and though the parts count went up, the circuit seems to solve all my problems and more.

I'll call it a bipolar relaxation oscillator for lack of a better name. It consists of eight 'everyday' components, and will generally be price competitive with UJT relaxation oscillators, in spite of the increased parts count. It is also generally cheaper than the PUT relaxation oscillators. The circuit's greatest usefulness lies in its versatility. It can be optimized to run at low frequencies, high frequencies, wide frequency ranges, low power consumption, or combinations of these.

As with UJT and PUT circuits, it can be used as a timer, pulse generator (perhaps voltage controlled as with my requirement), audio tone generator, or a crude ramp generator.

The heart of the circuit is its hysteresis or negative resistance element, which I will describe first.

HYSTERESIS ELEMENT

To describe its general function, we'll first ground the output and establish a 10V supply and a 5V reference level, as in figure #2.

Assume that $R_1 = R_2 = 1K$ ohms, and to start with, that $V_{in} = 0V$. Current flows from R_1 and R_2 through Q_1's emitter-base and collector-base junctions out the V_{in} node. The voltage across the emitter-base junction of Q_2 is approximately 0V, so Q_2 is off. If V_{in} is slowly increased, V_1 and V_2 will begin to track at about $V_{in} + 0.6V$. When V_{in} reaches and exceeds 4.4V, the current through R_2 reaches zero, then reverses direction as Q_1 begins to conduct. (see figure #3).

Q_1 becomes saturated because of plentiful base drive. Since V_1 nearly equals V_2, Q_2 is never biased on.

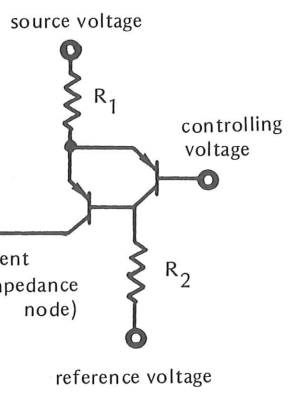


figure 1 Basic hysteresis element

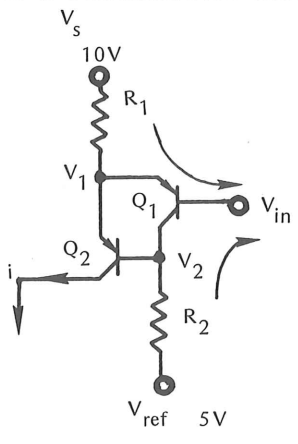


figure 2

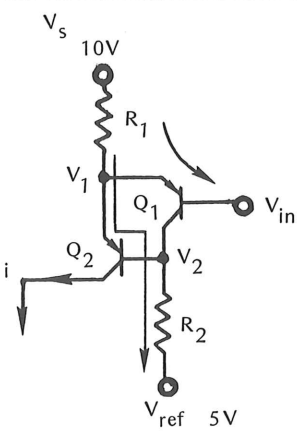


figure 3

If V_{in} continues to be increased, V_1 and V_2 will also rise; the current through R_1 decreases, and current through R_2 increases. When V_{in} exceeds approximately 6.9V, there is not enough current through R_1 to support enough voltage across R_2 to keep Q_1 saturated. If this process continues, $V_1 - V_2$ will become large enough to force Q_2 to begin to turn on.

When this occurs, extra current is drawn through R_1 by Q_2's emitter. This reduces V_1 and forces Q_1 towards the off state. Because of reduced Q_1 collector current, V_2 is also reduced. The small amount of Q_2 base current doesn't significantly counteract this effect. As V_2 is reduced, more base drive voltage is available to turn Q_2 on. In this way, each transistor's transition to another state aids the other transistor's transition, causing a quick, positive feedback enhanced switching action.

Now, $V_2 \approx 0V$, $V_1 \approx 0.6V$, $V_{in} \approx 7.2V$, and a state of output current exists. If V_{in} is slowly reduced, nothing happens until about 5V. Below this level, Q_1 begins to turn on and V_2 rises. When $V_1 - V_2$ becomes less than 0.6V, Q_1 turns off and Q_2 turns fully on. The action described previously is reversed, and positive feedback enhanced switching again occurs. The lower switching voltage is roughly determined by V_{ref}. The hysteresis width voltage depends on the values of R_1 and R_2, where:

$$V_{hyst} \approx \frac{(V_s - V_{ref} - 0.6)\, R_2}{R_1 + R_2}$$

As a practical point, be careful not to exceed Q_1 and Q_2's base-emitter reverse breakdown voltages. Consider using diode protection if higher source or hysteresis width voltages are involved. The circuit's NPN equivalent is shown in figure #4.

Relaxation oscillator

The basic hysteresis element is used for the relaxation oscillator shown in figure #5.

With this oscillator, the timing components R_0 and C_1 form the voltage control. Diode D_1 sets a reference voltage of approximately 0.6V. The peak point voltage, ($V_{C_{1max}}$), is a function of V_s, R_1, and R_2. As the cycle begins, Q_1 is saturated and C_1 charges towards the value of V_s, with current from R_1 and R_0. As C_1 charges, i_1 decreases and i_2 increases, until Q_1 can no longer remain saturated. Q_2 and Q_3 turn on, and V_1 falls rapidly. V_3 also falls, but it must fall at a slower rate than V_1. When V_3 reaches about 0.6V, Q_1 turns back on, Q_2 and Q_3 turn off, and the cycle repeats.

The operating frequency doesn't change much as V_s changes, because, as with UJT and PUT oscillator circuits, the peak point voltage and capacitor charging current both rise as a function of V_s. The i_3 component of the total charging current is well defined throughout the entire cycle, as it equals $i_1 - i_2$, (both of which are well defined). Therefore, the operating frequency is stable and predictable. The circuit can be optimized for low or high frequencies, or low power consumption. My experience has shown that the regenerative gain is high enough to insure switching without diode D_1, so the remainder of the discussion excludes this component. Also, adding Resistor R_4, (as shown in figure #6), will reduce the value of i_3 for lower frequency operation.

$R_{0MIN} > \dfrac{R_1}{B_{Q_3}}$ (to insure that capacitor C_1 discharges)

$R_{0MAX} \lesssim \dfrac{B_{Q_1} R_1}{10}$ (for obtaining minimum frequency predictability with varying B_{Q_1})

$R_4 \lesssim \dfrac{B_{Q_1} R_1}{10}$ (for obtaining frequency predictability over the entire frequency range with varying B_{Q_1})

The choices for R_1, R_2, and R_3 are less definable. For higher frequencies, they should be small enough to insure that Q_1 and Q_2's emitter voltages drop more quickly than Q_3's collector voltage for proper hysteresis. If R_3 is made too small though, there won't be sufficient base current for Q_3 at the minimum values of R_0 and V_s.

Without using the R_{0max} rule given previously, some maximum frequency readings are noted in figure #7. Note: Q_1 and Q_2 are both 151-0216-00 transistors,

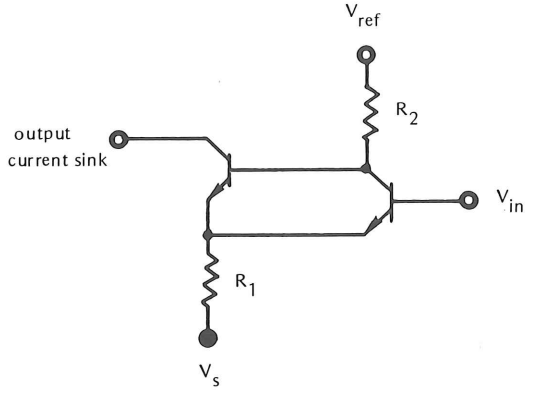


figure 4

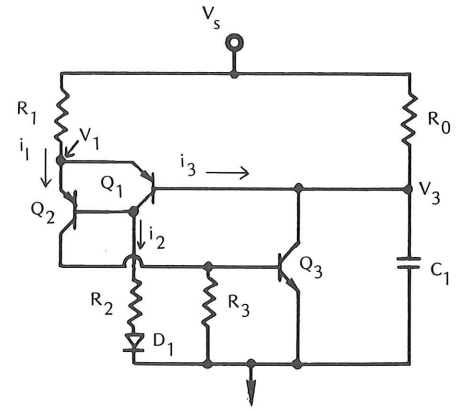


figure 5 Relaxation oscillator

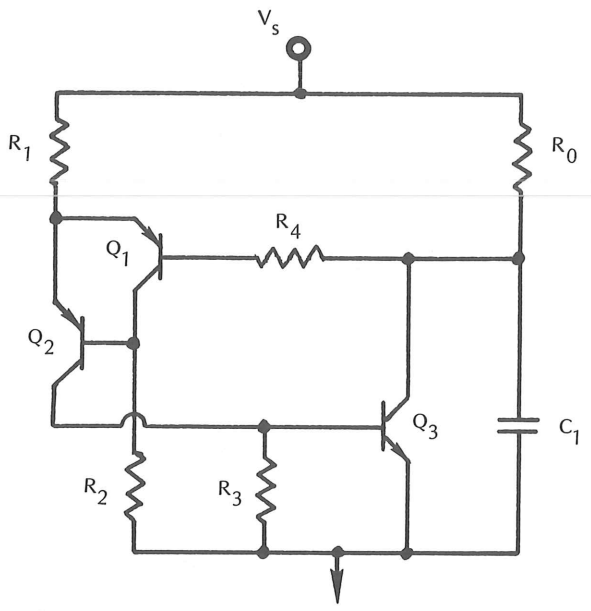


figure 6 Resistor added.

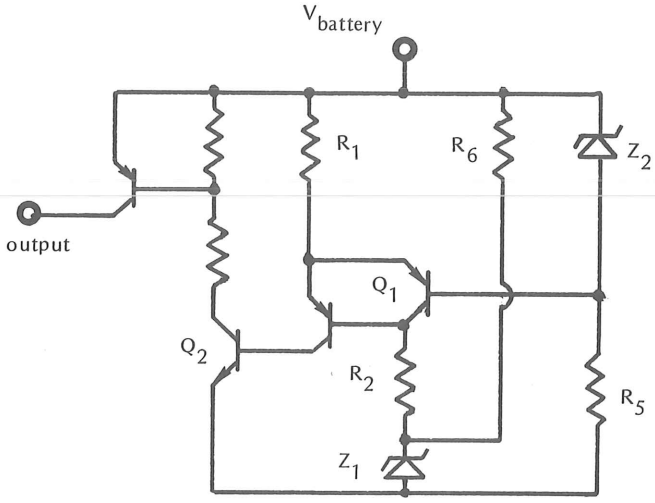


figure 8 Low Voltage Battery Shutdown Circuit

and Q_3 is a 151-0192-00. In my voltage controlled pulse generator application, (previously described), I set $R_1 = R_2 = 100K$ ohms, $R_3 = 51K$ ohms, and $R_4 = 0$ ohms. $C_1 = 1nf$, and R_0 was varied from 30K ohms to an infinite value.

Low voltage battery shutdown circuit

The hysteresis element can also be used in the low voltage battery shutdown circuit shown in figure #8.

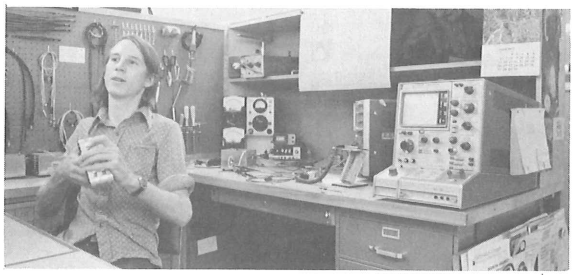
Z_1 generates a reference voltage. If Z_1 is a super zener, or the inaccuracy can be tolerated, one can omit the current stabilization resistor R_6.

The level of turn-on voltage is determined by the values of Z_1, Z_2, R_1, and R_2. Z_1 essentially sets the turn-off voltage point. For small hysteresis width voltages, one might choose to use two or three diodes to replace Z_2.

For comments, criticisms, or other applications, please contact me, Bruce Campbell, at ext. 6740.

Editor's Note:

Have you an original design you'd like to share? ENGINEERING NEWS would like to become a forum for idea swapping. If enough interest is shown, a regular design column will be run. (We will clear all material with the Patent Dept. first).



Bruce Campbell - circuit design genius at work

V_s 10V $Q_1 = Q_2 = 151\text{-}0216\text{-}00$ $Q_3 = 151\text{-}0192\text{-}00$

C	$*R_{0min}$	R_1	R_2	R_3	R_4	f_{max}	f_{min}	$f_{max/min}$
100uf	500	1K	1K	1K	0	3M	250K	12
1uf	1.1K	1K	1K	1K	30K	400K	16K	25
1uf	1.7K	10K	10K	10K	300K	100K	1.8K	55
10uf	630	10K	10K	10K	300K	66K	150	440
1uf	280	10K	10K	10K	300K	3.5K	1.34	2.6K
10uf	**150	10K	10K	10K	300K	666	.21	3.2K

$*R_{0max} = \infty$ for all tests **Dry lab number

figure 7 Table of resistor values and frequencies.

Scientific Computer Center

SINC DC with Monte Carlo

An initial version of SINC with DC Monte Carlo analysis is now available. To run it, enter -SINCMC(F=DATA) where DATA is your SINC input data.

The output is a voltage distribution plot and a local file named TAPE7. For statistical analysis of the output, use TAPE7 with the ISIS program.

Try it. If you have problems, type HELP,SINCMC. If you're still stumped, call Imants Golts at ext. 5127.

Logic minimization

Anyone who has tried to minimize a logic function of six or more variables knows there are better ways to spend one's time.

Well, now there's a computer program available to do this sort of stuff for you. To find out about it, trot down to your local neighborhood terminal and type HELP,LOGMIN.

TIDY cleans

Do you have trouble finding statement numbers in your Fortran code because they're out of sequence? Do you have trouble reading your code because all the information's packed to the left side?

Then consider using TIDY, a new Fortran program for renumbering and cleaning up old Fortran programs. For more information, simply type HELP,TIDY on your favorite terminal.

Carter reveals SCRIBE secrets

Attention SCRIBE and EDIT users! After May 19, a new version of the SCRIBE text editor will be available.

On Friday, May 16, at 10 a.m., I will start from ground and talk about the new SCRIBE program for about an hour in the Tech Center auditorium. Features of the new program and how it differs from the old one will be covered. For more information, contact me, Lynn Carter, at ext. 7446.

The Choice Is YOURS

In case anyone's failed to notice, each of the last 4 issues of ENGINEERING NEWS have flaunted a separate and individually gorgeous masthead. Now we have to make the BIG choice of which one to continue using. Want to help us?

Take a moment, reflect on it all, and indicate in the appropriate places the one most liked to the one least liked.....1 to 4. Grab the scissors, and mail the remains to our eager staff at 50-462.

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IN PRINT

Oliver Dalton, Laboratory Oscilloscope Products, and **Frank Elardo**, Product Marketing, collaborated on an article printed in the March 20 issue of **EDN** magazine called, *"Consider all the alternatives when choosing an oscilloscope."* Using an easy step-by-step method, the article helps the prospective buyer choose the proper instrument for any given application. In addition to explanations and descriptions of all supportive equipment, several photographs and diagrams are included.

Bill Walker, Group Vice President—Engineering, authored an article called, *"Test and measurement instruments, a look at the trends,"* in February's issue of **ELECTRONICS IN INDUSTRY** magazine. The material describes how instrument manufacturers are keeping pace with the requirements of a constantly expanding market, and what some of the resulting instrumentation will do.

Note: All articles IN PRINT are available in the Tek Library, ext. 5388.

Call for papers

The 12th Modulator Symposium will be held at the Statler Hilton Hotel, New York City, on February 4-5, 1976.

SPONSOR: The Advisory Group on Electron Divices, in conjunction with Palisades Institute for Research Services, Inc., and IEEE.

TOPICS: The scope of the symposium includes:

Lasers
Phased discharge devices
Electromagnetic pulsers
Vacuum tubes
Auxiliary devices
Linear accelerators
Nanosecond pulsers
Solid state devices
Magnetic devices
Modulator techniques
Transmitter reliability

ABSTRACT: Prospective speakers are asked to submit a comprehensive 200 word abstract by October 17, 1975. It should roughly approximate a 20-minute paper, including discussion. The heading should be by Title, Author(s), and Professional affiliation and location. An original and 10 copies should be sent to:

Program Chairman
Sol Schneider
Electronics Technology and Devices Laboratory (ECOM)
Ft. Monmouth, New Jersey 07703

OTHER: Authors: Remember to allow enough time for clearance by military sponsoring agencies and corporate editorial divisions.

1975 Mid-West Symposium on Circuits and Systems will be held at Sir George Williams University, (now known as Concordia University), Montreal, Canada, on August 11-12, 1975.

SPONSOR: Dept. of Electrical Engineering, Sir George Williams University.

TOPICS: Authors are invited to submit research or tutorial papers on any aspect of:

Circuit theory and design
Communications and control systems
Computer-aided analysis and design

ABSTRACT: A 300 word summary of the paper, headed by Title, Author(s), and Affiliations must be received in duplicate before May 15, 1975.

OTHER: Notification of acceptance and special sheets for the preparation of accepted papers for the conference will be sent before June 15, 1975. Send papers to:

Dr. M.N.S. Swamy
Dept. of Electrical Engineering
Sir George Williams Campus
Concordia University
1455 de Maisonneuve Blvd. West
Montreal, P.Q. H3G 1M8, Canada

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