

Caroline Downing

REV	REV	REF	DESCRIPTION OF CHANGE	CHK BY	DATE
D	OR		Initial Documentation		11-1-71
	A				5-7-73
	B		Major Revision, new format (14 pages).	Hakola	7-20-77
	C		Revision. (Pages 1,3,5,6,7,9,12,13,14).	Hakola	6-21-78
	D		Incorporate ECN's #1921 & #2777. All 14 pages changed. Minor format and typing changes.	Allen/ Steen	4-5-79

PART NUMBER 155-0065-00

Linda Boyer Writer Shel Allen Originator George Steen Originator

COMPANY CONFIDENTIAL

Tektronix, Inc.

H074

155-0065-00

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TEKTRONIX, INC.

P. O. BOX 500
BEAVERTON, OREGON U.S.A. 97077



DWN/
WR

COMP
ENGR

CHKR/
COORD

INSTR
DSGN

MATERIAL

FINISH

TITLE

High Frequency Differential Amplifier

DIMENSIONS ARE IN INCHES / MM
TOLERANCES: UNLESS OTHERWISE SPECIFIED

DEC ANLR

SCALE FIRST USED ON

SH 1 OF 14

CODE IDENT NO

80009

SIZE

A

PART NUMBER

155-0065-00

REV

D

1.0 DESCRIPTION

The H074 is a Monolithic Integrated Circuit/Transistor Hybrid. It was designed specifically as a Vertical Deflection Plate Driver in a CRT, enabling the 7900 Series to have a Bandwidth of DC to 500 MHz.

1.1 Features

- 1.1.1 DC to 500 MHz Bandwidth.
- 1.1.2 Discrete Transistor Outputs.
- 1.1.3 High Frequency Differential Amplifier.

2.0 ABSOLUTE MAXIMUM RATINGS

AN ABSOLUTE MAXIMUM RATING DEFINES A BIAS, MECHANICAL STRESS, OR ENVIRONMENTAL CONDITION BEYOND WHICH THE SERVICEABILITY OF AN INDIVIDUAL DEVICE MAY BE IMPAIRED. ANY COMBINATION OF ABSOLUTE MAXIMUM CONDITIONS MAY NOT NECESSARILY BE APPLICABLE CONCURRENTLY.

Symbols	Identifications	Notes	Values	Units
T_{Stg}	Storage Temperature, range		-55 to +125	°C
T_A	Operating Ambient Temperature, range		0 to 70	°C
P_{DMAX}	Total Device Power Dissipation		4	Watt
	Maximum voltage Pin 2 to Pin 8		40	Volt
	Maximum voltage Pin 3	Referred to Pin 12	5	Volt
	Maximum voltage substrate (case)	Referred to Pin 12	-20	Volt
	Maximum Current into Pin 2 and Pin 8		170	mA
	Maximum Current through Nichrome resistors		100	mA

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CODE IDENT NO
80009

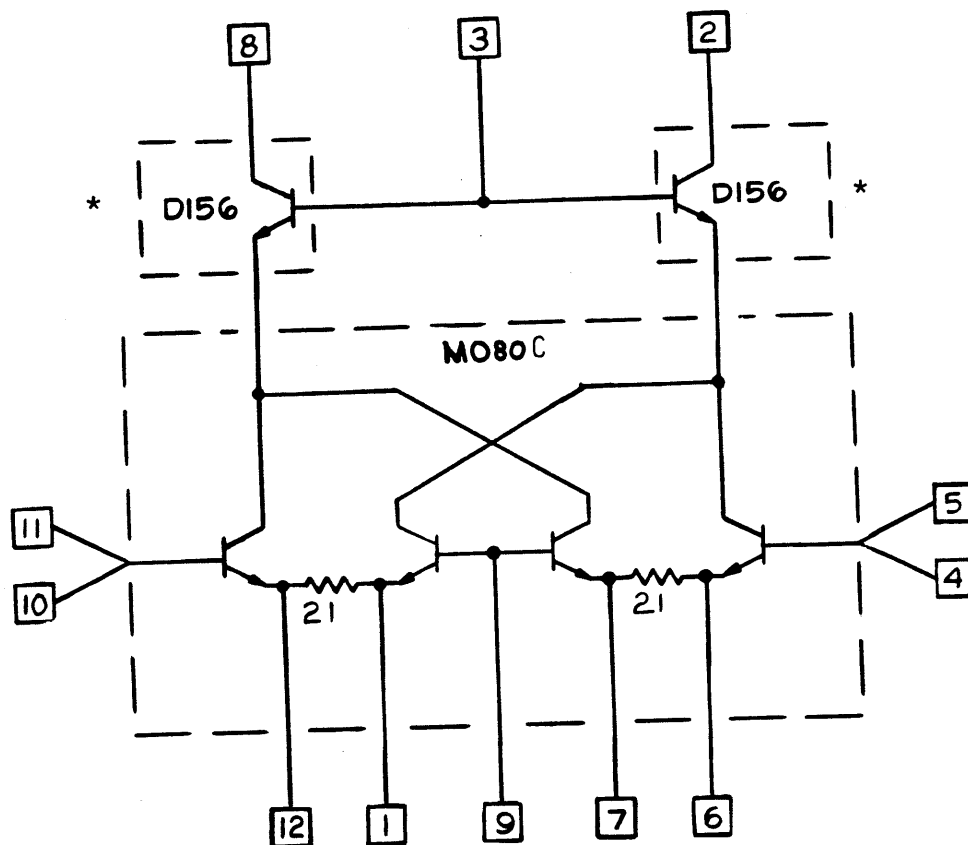
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Figure 1



*SELECTABLE TRANSISTORS
(153-0639-00)

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3.1 Layout Drawing

Refer to Bonding Diagram ICM-39-200.

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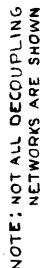
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REV

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4.0

PARAMETRIC DEFINITIONS, Figure 2



42074

155-0064, 155-0065, OC TEST FIXTURE
J. ADDIS 0125, 0186

PARAMETRIC DEFINITIONS, Table 1.

[illegible]

NAME _____

1	M80 BV CEO	5.0 & .5 mA
2	D78 BV CBO	50 V & .1 mA
3	BV SUB	30.0 V at .1 mA
4	NICHROME 1,12	
5	NICHROME 7, 6	Match within 1 Ω
6	INPUT I_b 9	2 mA
7	INPUT I_b 10,11	1 mA
8	INPUT I_b 4, 5	1 mA
9	DC OFFSET	.375 V R.T.O.
10	SET NULL	
11	GAIN	4.7 to 5.0
12	+DYN RANGE	27.5 V into 365 Ω
13	-DYN RANGE	-27.5 V into 365 Ω

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5.0

PARAMETRIC SUMMARY

No.	Symbols	Identifications	Notes and Test Conditions ¹	Values		Units
				Min	Max	
1	$R_1 - R_2$ MATCH	Nichrome Resistor Match	Subtract Resistance measured Pins 7 to 6 from resistance measured Pins 12 to 1.		1	Ω
2	I_{b9}	Input Current into Pin 9	Pins 12,1,7,6 ea carrying 40 mA. Pin 3 to +3 V. Pins 10 & 4 returned to ground through 50 Ω . Pin 9 to ground through 25 Ω . Pins 2 & 8 to +35 V through 182.5 Ω . Measure current in Pin 9. Case disconnected.		2	mA
3	$I_{b10 \& 11}$	Input Current into Pins 10 & 11.	Same as I_{b9} except measure current in Pins 10 & 11.		1	mA
4	$I_{b4 \& 5}$	Input Current into Pins 4 & 5.	Same as I_{b9} except measure current in Pins 4 & 5.		1	mA
5	BV_{CEO} at .5 mA M080	Collector-Emitter Break-down Voltage with bases open. Measurement includes base emitter drop of D-78	Pins 2,3 & 8 shorted and connected to .5 mA source. Pins 12,1,7 & 6 connected to Gnd. Pins 10,11,4 & 5 open. Substrate open. Measure Pin 3 to ground.	5.0		V

5.0

PARAMETRIC SUMMARY (continued)

No.	Symbols	Identifications	Notes and Test Conditions ¹	Values		Units
				Min	Max	
6	BV_{CBO} at .1 mA D-78	Collector-Base Break-down	Pin 3 to ground or negative source Pins 2 & 8 shorted and connected to .1 mA current source. Measure Pins 2 & 8 to Pin 3.	50		V
7	BV_{SUB} M080	Substrate (case) Breakdown Measurement includes base emitter drop of Output Transistor	Case to ground or negative source. Pin 3 to .1 mA current source. Measure Pin 3 to case.	30.0		V
8	V_{OUT}	D.C. OFFSET Voltage referred to Output.	Pins 12, 1, 7 & 6 each through 100 Ω to common point then to -15 V through 63.75 Ω . Pins 4 & 10 returned to ground through 50 Ω . Pin 3 to +3 V. Pin 9 to ground through 25 Ω . Pins 2 & 8 each through 182.5 Ω to +35 V. Measure Pin 2 to Pin 8. Case disconnected.		.375	V
9	GAIN	D.C. Current Gain With external shunt resistor from Pin 12 to Pin 1 and from Pin 7 to Pin 6 according to coding on case. CODE RESISTOR 1 110 2 130 3 160 4 220 5 300 6 510 7 1000	Same as V_{OUT} except add 5475 Ω Pin 11 to +15 V and 5475 Ω from Pin 5 to -15 V (5.479 mA input current). Measure Pin 2 to Pin 8 voltage. Connect proper coding resistor from Pin 1 to Pin 12 and from Pin 7 to Pin 6.	4.7	5.0	

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CODE IDENT NO
80009SIZE
APART NUMBER
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5.0

PARAMETRIC SUMMARY (continued)

No.	Symbols	Identifications	Notes and Test Conditions ¹	Values		Units
				Min	Max	
10	+ DYN. RNG.	Dynamic Range with + signal applied to Pin 11.	Same as V_{OUT} except Pins 4 & 5 are open and Pin 11 returned to +15 V through 590 Ω .	27.5		V
11	- DYN. RNG.	Dynamic Range with - signal applied to Pin 5.	Same as V_{OUT} except Pins 4 & 5 returned to +15 V through 590 Ω . Pins 10 & 11 are open.	-27.5		V
12	T_r	Risetime, measured from 10% to 90% of pulse where 0% is the baseline before pulse input and 100% is peak of the overshoot. Ringing, peak to peak	155-0065		470	pS
			Test system (sampler and pulser)		100	pS
			Displayed Rise-time		480	pS
					35	%

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6.0 PACKAGING

6.1 Terminal Identification

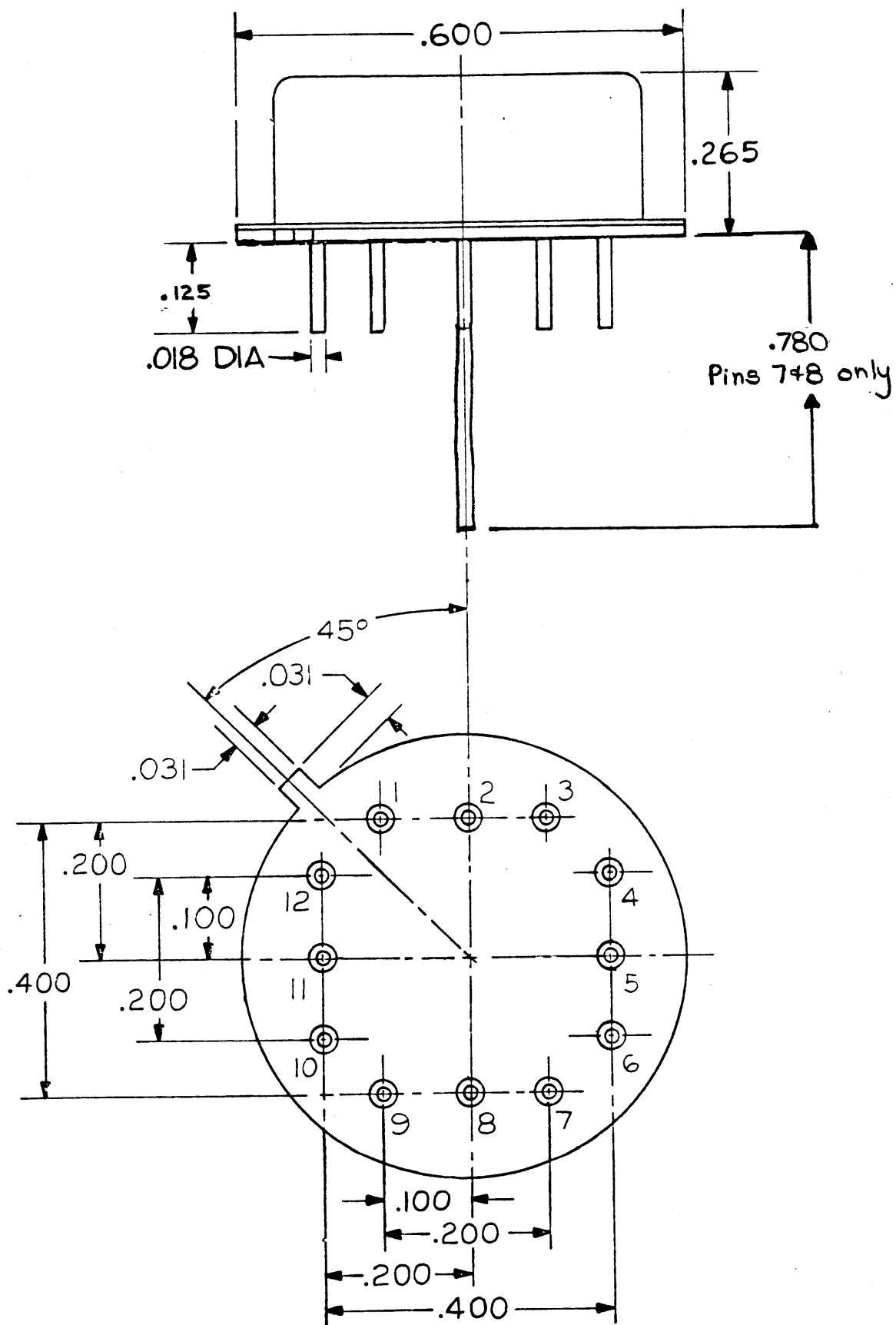
<u>Pin</u>	<u>Function</u>
1	Bias
2	Differential Output
3	Bias
4	Differential Input
5	Differential Input
6	Bias
7	Bias
8	Differential Output
9	Bias
10	Differential Input
11	Differential Input
12	Bias

Substrate connected to case.

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6.0 PACKAGING (continued)

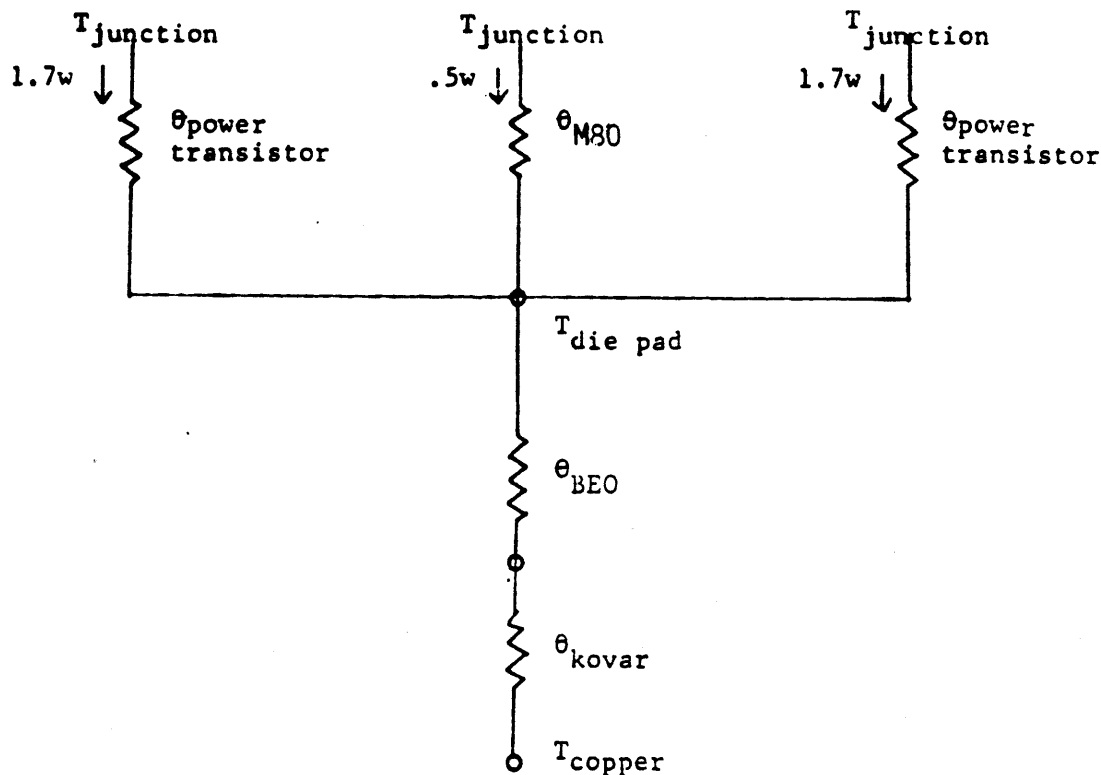
6.2 Outline Drawing



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6.0 PACKAGING (continued)

6.3 Thermal Characteristics



$\theta_{\text{power transistor}} = \text{from } 30^{\circ}\text{C/w to } 50^{\circ}\text{C/w depending on device and die bond (measured).}$

$\theta_{\text{BEO}} = 2^{\circ}\text{C/w (calculated)}$

$\theta_{\text{kovar}} = 1.8^{\circ}\text{C/w (calculated)}$

$$T_j - T_{\text{cu}} = \begin{cases} 30 * 1.7\text{w} + (3.8 * 3.9\text{w}) \\ 50 * 1.7\text{w} \end{cases}$$

For non studded package plugged into board with Cu heat sink;

$$T_{\text{pkg base}} - T_{\text{amb}} = (2.2 + 1.4 + 2.4) (3.9 \text{ W}) = 23.4$$



$$89^{\circ}\text{C} \leq T_j - T_{\text{amb}} \leq 123^{\circ}\text{C}$$

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7.0 RELIABILITY STATEMENT

Field failure rate (empirical) from Period 508 to
Period 703: 1.9%/1K hours.

8.0 APPLICATIONS INFORMATION

7844

9.0 REFERENCE LIST

153-0639-00

Bonding Diagram (ICM-39-200).

Test Book in Test Area (TSM-15-2065-00 - Fixture Test).

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