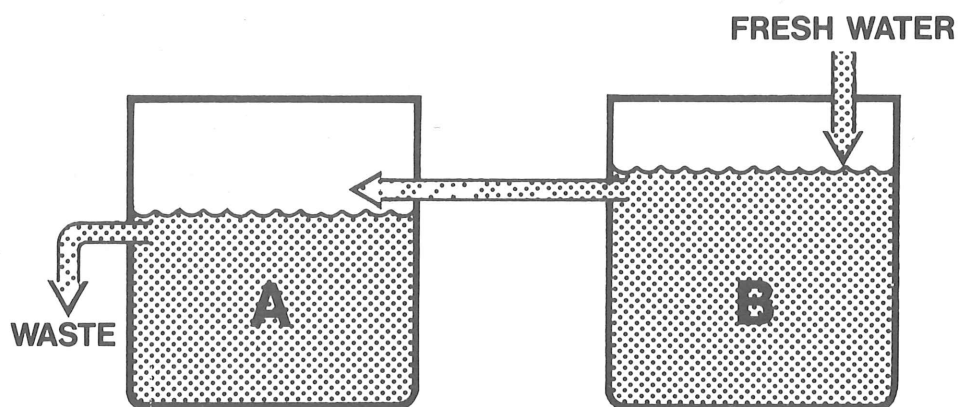


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Engineering News

VOLUME 3/ NUMBER 6 JUNE 1976 JOYCE LEKAS, EDITOR X6601 RHYS SCHROCK, ASSOCIATE EDITOR X6071 DS 50/462



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Water Use Cut Drastically in Electrochem

Electrochemical Engineering has developed water reuse systems for the Electrochem rinse tanks. In one process, water use has been reduced from 12,000 gallons per day to 30 gallons per day. Much of this is done by reusing rinse water. Most rinses don't require absolutely clean tap water.

Work started last September on a water conservation program. The 300,000 — 400,000 gallons of water used in Electrochem per day had to be reduced to one third to meet allowable contaminant standards by July, 1977. The major water savings has been a result of modifying rinse tanks into cascade systems. Previously parts were rinsed in a series of two or more tanks, each with its own water supply and drain. A simple two-cascade rinse consists of two tanks:

The parts to be rinsed are first placed in tank A. Here 90%—99% of the waste is rinsed from the parts. The final rinse is done in tank B, which has a fresh water supply. The waste water from tank B is pumped or flows into tank A, since pure water is not necessary for the first rinsing. This process re-

quires 10–100 fold less water than one-tank rinsing because the water in tank B gets very little contamination. In addition, the "waste" from tank B may be pumped to another cascade where the contaminants from tanks A and B are of no consequence. By applying this plan to the aluminum anodizing line, the number of fresh water inlets has been reduced from 8 to 3.

To determine when fresh water should be added to tank B, conductivity controllers have been installed in the rinse tanks. These Rinse Tank Controllers (RTC) measure the conductivity of the water, which is a measure of the contaminant level. When conductivity reaches a specified level, fresh water is automatically added to the system. This way, water is not used unless it is necessary.

In one etch process, by installing a four-cascade rinse, water usage was reduced from 12,000 gallons per day (GPD) to 30 GPD. They are now also recovering 100% of the copper in the system.

In some process baths a significant portion of chemicals is also conserved using a "drag-out-recovery" tank. For example, when parts are removed from a copper plating tank, they "drag-out" some of the copper plating solution. They are rinsed first in a tank of stagnant water ("drag-out-recovery" tank) where about 75% of the copper plating solution is removed and then they are rinsed in a cascade system as shown above. Contents of the "drag-out-recovery" tank are returned to the copper plating tank to replace the volume

lost by "drag-out" and evaporation. There are two benefits from this process; 1) conservation of valuable chemicals and 2) reduction of contaminants in the waste water.

Organic compounds (alcohols, wetting agents) are also a contamination problem in process waste. Plans are underway to segregate major sources for special treatment.

For more information, contact Jerry Jacky, ext. 7830.

papers . . . Call for papers . . . Call for papers

The 1977 Power Industry Computer Application Conference (PICA X) will be held in Toronto, Ontario, Canada May 24-27, 1977. PICA X is the tenth in a biannual series of conferences which deal with the application of analog and digital computers in the electric power industry.

SPONSER: IEEE Power Engineering group, Toronto Section.

TOPICS: Papers are invited which deal with any aspect of the application of computers to the solution of problems faced by the electric utility industry. Special consideration will be given to papers in the following general areas

Computers in Power Engineering Education
Nuclear Power Computations

Power Plant Performance and Control
Interactive Computer Graphics
Load and Economic Forecasting

ABSTRACTS: 150-200 word abstracts are due at IEEE Headquarters by October 8, 1976. Deadline for original manuscripts of accepted papers is January 3, 1977.

IEEE Headquarters
345 East 47th St.
New York, N.Y. 10017

OTHER: Prospective authors are urged to request a Power Author's Kit from:

IEEE, Technical Conference Services Office
345 East 47th. St.
New York, N.Y. 10017



► TELEPHONE PROBLEMS?

If you encounter any problems when dialing into the CYBER (busy signals, no response, etc.) please call ext. 5104. They have no other way of knowing that the computer is inaccessible.

► ENGINEERING IN GEORGIA

A copy of the booklet *A Brief History of Engineering in Georgia (and Guide to 76 Historic Engineering Sites)*, by James E. Brittain, Ph.D. is available for loan in the Technical Information Office, 50-462. This booklet, celebrating

"American Ingenuity-200 Years of Engineering" salutes the traditional role of the Engineer as innovator and problem solver. The contributions of Engineers in Colonial Georgia (1732) included surveying, roadworks, bridges, and forts. This engineering period progressed through the 1800s with railroads, canals, and dams, culminating in a spectacular system of 66 grist mills throughout the state. The booklet also covers engineering contributions in the 1900s which include hydroelectric power plants and real big railroad trestles.

► TECHNICAL STANDARDS

- There has been a revision to Tektronix Standard G-102, Drafting Standard for Circuit Boards. This revision removes the ambiguity about the application of .025 or .050 grid and makes the datum-to-grid note mandatory on all applicable circuit board drawings.
- Preliminary and rough draft versions of Atmospheric Test, Environmental Test, and a Cam Switch standard are under evaluation.
- Work is underway on Standards 062-2320-00, Circuit Board Switch Mounting; 062-1721-00, Circuit Board →

Drafting; and 062-1722-00, Circuit Board Design.

- The Institute of Printed Circuits (IPC) Technical Manual for Printed Circuits and Flexible Flat Cables is now available through Technical Standards.
- For information or copies of any of these standards, contact Technical Standards ext. 7976, del. sta. 58-187.

► MORE BIT PATTERN PER PUNCH CARD

A Fortran callable subroutine to punch any bit pattern desired into a punch card is now available on the CYBER computer. (A typical use would be to transfer data which contains negative values from the CYBER to the IBM 370. Negative values on the CYBER have the minus sign before the number; negative values in the IBM 370 have the minus sign superimposed over the units digit. This subroutine will allow the CYBER user to punch cards so that they can be used on the IBM 370.) The complete description on how to use it is contained in the source library. To get the source, type:

GET,PUNBIN/UN=LIBRARY

Then use SCRIBE to look at the description. If you have any questions, contact Dick Machlan, ext. 5714.

► COMPUTER NETWORKS SEMINAR

Leonard Kleinrock will teach an intensive 3-day seminar on Computer Networks. This is the first offering in which his latest authoritative text on computer networks, **Queueing Systems, Vol. II: Computer Applications**, Wiley Interscience 1976, will be used.

The basic objective of this in-depth seminar is to acquaint the participant with modern techniques of computer network design, both from the analytical as well as the practical point of view. Topics include packet switching, resource sharing, teleprocessing systems, and network evaluation and design. Experience with an existing international network (the ARPANET), its operational procedures, and the cost-effectiveness of large scale computer networks will be discussed. The advanced technology of satellite and ground radio packet switching will also be featured. The material represents the latest knowledge and experience with modern computer networks and provides fundamental understanding concerning their design, use and impact in the future.

The first seminar will be given in Dallas, Texas, July 19-21, 1976, followed by Washington, D.C., August 9-11, 1976, and Los Angeles, California, August 30-September 1, 1976. The fee of \$485 includes textbook, luncheons, and refreshments. For further information and registration contact:

Technology Transfer Institute
P. O. Box 35247
Los Angeles, California 90035
Phone: (213) 553-7397

- The following is a list of the committees in which the various members of the TV Engineering Group are involved:

Committee on Broadcast Television Systems (BTS)
C. W. Rhodes

Task Force on Standard Video Demodulator
C. W. Rhodes
Steve Roth

Joint Committee for Intersociety Coordination (JCIC)
C. W. Rhodes

Ad Hoc Committee on Color Television Study
C. W. Rhodes

Ad Hoc Committee on Television Broadcast
Ancillary Signals
C. W. Rhodes

IEEE

2.1.4—Video Signals Transmission Subcommittee
C. W. Rhodes

2.1.6—Subcommittee on Digital Technology
C. W. Rhodes
P. S. Crosby

ADCOM—Ad Committee of Broadcast Group
C. W. Rhodes

EIA (Electronic Industries Association)

TR-4.4 Subcommittee on Studio Facilities
C. W. Rhodes
Chairman

TR-4.4.2 Color Monitor Standard
J. Horn

R-4.4 Color Television Measurements Standards
Committee (Receivers)
C. W. Rhodes
Steve Roth

SMPTE

Northwest Section
C. W. Rhodes

Study Group of Digital Television
C. W. Rhodes

Television Technology Committee
C. W. Rhodes

STOC — TV (Satellite Technical and Operational
Committee — Television)
C. W. Rhodes

Graticule Subcommittee
C. W. Rhodes

OCCIR (International Radio Consultative Committee)
U.S. Study Groups 10 (Broadcasting Service — Sound)
And 11 (Broadcasting Service — Television)
C. W. Rhodes

CMTT (Transmission of Sound Broadcasting and
Television Signals Over Long Distances)
C. W. Rhodes

►MICROPROCESSOR DESIGN I

DESCRIPTION: Course is designed to introduce the student to the components of the 6800 microprocessor family, 6800 simulator and the Cyber 70 support software. Emphasis is going to be placed on use and programming of all the components used in design of the microprocessor based system. Course is being offered in cooperation with P.S.U. under ASE 410 for 4 credit hours.

RECOMMENDED BACKGROUND: Basic understanding of digital circuits and some programming background.

OBJECTIVES: Become familiar with hardware and software nomenclature. Learn how to use the presently available tools to help in the development of the microprocessor based system.

COURSE LENGTH: 11 weeks. One 2-½ hour lecture with one 2½ lab per week.

SCHEDULE: Monday and Wednesday from 2-4:30 p.m. and 4:30-7 p.m. starting June 21. At present there are not enough people to fill the 2-4:30 class. The 4:30-7 class has 5 openings.

PLACE: Building 47, Conference Room G.

CLASS SIZE: Limited to 20 per section.

INSTRUCTORS: Henry Joyoux (2-4:30) and Jack Riley (4:30-7).

REGISTRATION: Please call Lynne Buchanan or Steve Pataki, Ext. 6073.

Maureen Key 60-553