component news

Issue 265 COMPANY CONFIDENTIAL Nov. 29, 1978

RETs offer variety, large SOA

Fujitsu's new ring emitter transistor (RET) has generated a great deal of interest at Tek lately. This is probably due to the emphasis on switching parameters and performance, coupled with an abundance of ratings and package styles.

The RET design pays particular attention to both forward and reverse bias safe operating area (SOA). To obtain a greater forward bias SOA, the RET devices are emitter ballasted (see **Component News 262**) to promote current sharing between emitters. This is accomplished in a rather clever way.

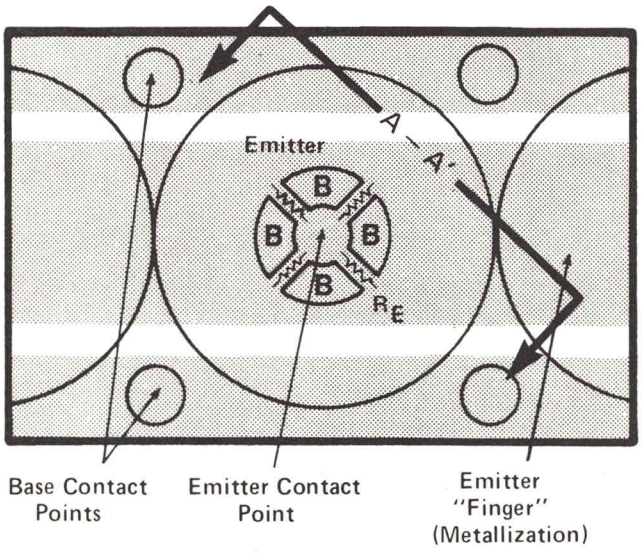


Figure 1 — Top view of RET

A top view of one RET device is akin to a four-spoke wheel with the hub as the emitter metal contact (see Figure 1). The spokes of this "wheel" are a very thin (~5000Å) layer of N++ material, which act as ballasting resistors. The conduction point is a much thicker (~2μm) ring, the "tire" on this hypothetical wheel. The P– base (~2.5μm) underneath the ring is designed to achieve a short transit time through the base, which means a high f_T. Using emitter ballasting allows bases to be made quite thin, because the base no longer has the main task of promoting SOA (see Figure 2).

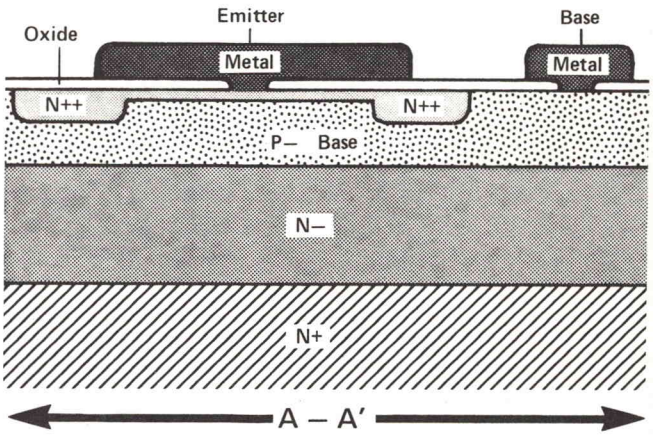


Figure 2 — RET cross-section

The RET structure simultaneously gives excellent reverse bias SOA, a necessity for inductive switching. The technique of using a thicker base center than base outside was pioneered by Unitrode in their UMT1009 series of high-voltage "Switchmode" type devices.

continued on page 2

Also in this issue

During turn-off, current is flowing out of the base and, due to de-biasing effects, collector-emitter conduction is forced toward the center of the emitter. A device with a thicker base has better SOA because charge dispersion tends to alleviate the formation of local "hot-spots." Also, because the base is thicker in this region, it has a lower gain than the outside region. This helps reduce storage time.

The table and graphs below summarize the performance data for the most promising RET devices (the NPN 2SC2527 and PNP 2SA1077). Notice that $V_{CE(SAT)}$ is not particularly spectacular, because this parameter is degraded by $I_E(R_E) - R_E$ is the emitter ballast resistance. R_E does obtain a very respectable SOA curve, though.

Initially, RETs were available in a TO-3 package only. Now Fujitsu is producing them in TO-220 plastic packages.

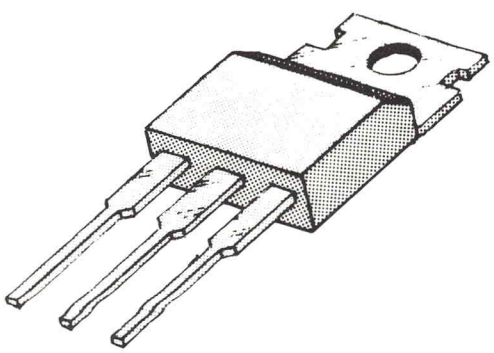
The 2SC2527 is currently under serious consideration by a design group at Tek. The part would be used to replace a fast, double-diffused device (151-0426-00) which has a poorer SOA and a high failure rate in this application.

If you're interested in the RET for your design, please contact me at 58-299, ext. 5345.

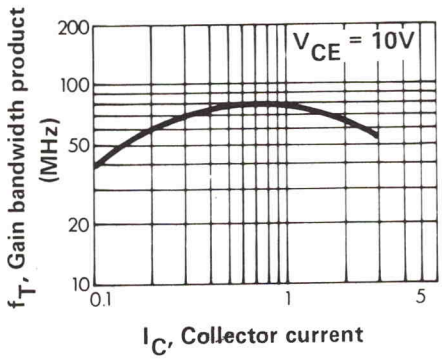
Jim Williamson

Performance characteristics – 2SC2527

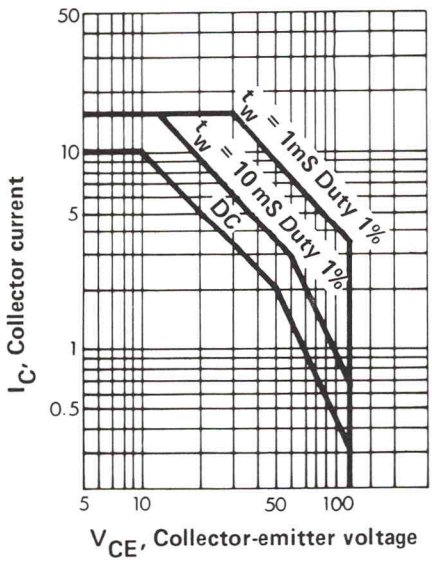
	Min.	Meas.(avg.)	Max.
BV_{CBO}	120V	230V	–
BV_{CEO}	120V	212V	–
h_{FE} (V_{CE}=5V)			
@1A	60	88	120
@5A	–	96	–
$V_{CE(SAT)}$ I_B=0.5A I_C=5A	–	0.73V	1.5V
C_{OB} V_{CB}=10V f=1MHz	–	200pF	–



Gain bandwidth product



Safe operating area



Use proper cable for crimped connections

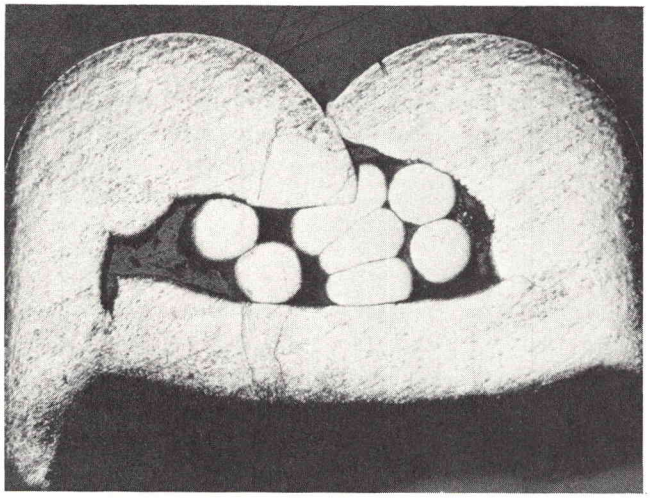
The mix of connectors in our products has increased greatly in the past few years, chiefly because of changing design requirements and different interconnection needs for OEM assemblies.

Therefore, this word of caution to new product designers: *Make sure the connector specified is designed to accommodate the cable size used.* For example, a connector designed for a 20 - 24 AWG (American Wire Gauge) cable should not be specified for a 30 AWG cable.

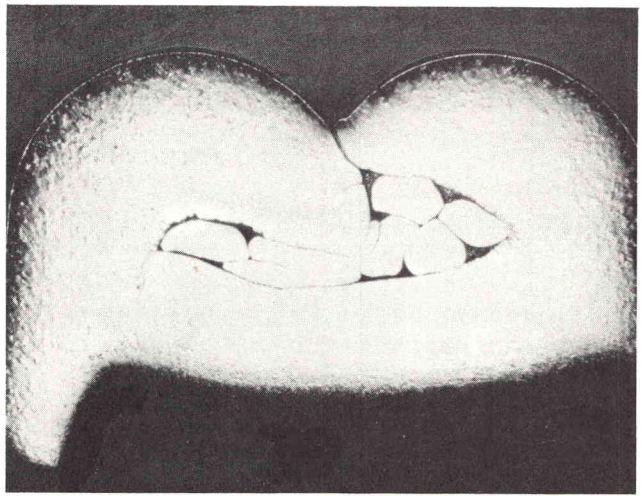
This may seem like an extreme example, but Wire Prep Pilot Assembly has had this combination appear in new designs in the past.

Remember that the purpose of a crimped connection is to form a gas-tight junction between cable and connector. Oversize connectors cannot provide reliable gas-tight connections, and trying to make them so by over-crimping compounds the problem. Then cable strands are crushed, often resulting in mechanical failure.

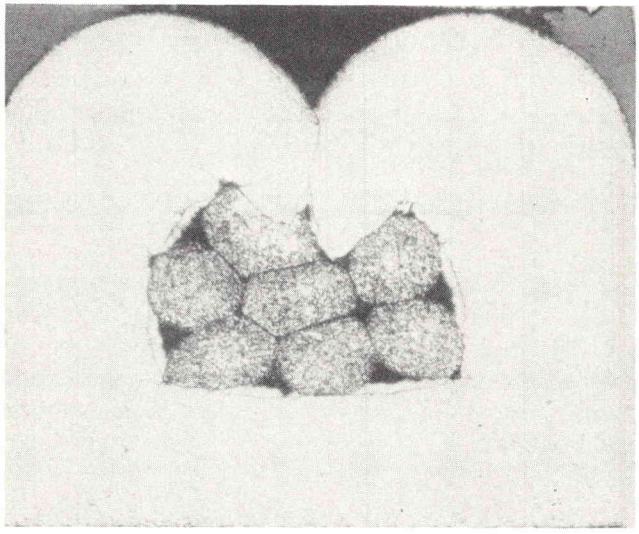
Wire Prep Pilot Assembly is attempting to catch misapplications as they appear by reviewing wire kits before they "Turn Regular." However, the problem can best be solved in the design stage, by calling out the proper size connector for your application.



Cross-section photograph (50X magnification) of an oversize connector which has crushed and separated the cable strands, resulting in a connection that is not gas-tight. A cold-flow metal spur, formed during over-crimping, further weakens the connection.



This oversize connector crushed and weakened these cable strands, making them vulnerable to breakage.



A proper size connector minimizes cable crushing and strand separation. The connector retains its form and thickness, lending optimum support to the connection.

For assistance in connector selection, call Larry Berry or Loren Spohn (ext. 6887), or Bud Siegel (ext. 5907).

Loren Spohn
Wire Prep, Engineering Support

Beryllium–nickel supply problem critical

Beryllium-nickel is a very useful material because of its strength and corrosion resistance. Two of its more undesirable features are high cost ($11 to $21 per pound) and supply problems.

The supply situation is a concern at all times because there is only one US vendor, no foreign vendors and no other vendors interested in producing this material. **This is a very serious single source problem,** because Purchasing has no options if the vendor has production difficulties.

Presently, this is what's happening. The vendor is taking nine months to deliver, with the possibility of missing even these long delivery times. As a consequence, several part numbers are out of stock, with stock levels dangerously low on the remaining part numbers.

Because of our present plight, it is becoming necessary to reduce, or eliminate, our use of beryllium-nickel. I would strongly suggest that this material **not** be used for new design, and that serious alternate material evaluation be done for existing applications.

If you need more information for alternate materials, call **Kwaku Mensah (ext. 7833).** If you need more information about vendor problems, call **Cal Bjerke (ext. 6603),** or if you need more details on material conversion plans for existing applications, call **Frank Javorsky (ext. 6391).**

Beryllium-copper, beryllium-nickel alloy guide

A guide for the selection and use of beryllium-copper and beryllium-nickel alloys is available from the Metallurgical Lab. These two alloys are among the most widely used at Tek for producing springs, contact switches, retainer clips and other similar components.

The guidelines were written by Kwaku Mensah, and describe the electrical and mechanical properties of the alloys, as well as the advantages and disadvantages associated with each. Selection factors are based on electrical and thermal conductivity, yield strength, corrosion and wear resistance, fatigue and impact strength and other criteria.

To make the best choice of materials, it is important that designers be aware of the unique properties of these alloys. If you would like a copy of the selection guidelines, send your request to the **Metallurgical Lab (38-314).**

SILKSCREENING RECESSED METAL PARTS

If you are designing parts which require silkscreened nomenclature and lines to be applied into a recessed area, you may be creating a problem for the metals marking group. Special screening frames must be designed and built to match each different part configuration. Because these screens are much more difficult to make and use, many hours are spent remaking the screens and reworking production parts.

As a parts designer, you can help most by eliminating recessed areas or the nomenclature in them, or by using decals wherever possible.

If you have no alternative to silkscreening in a recessed area, keep the following guidelines in mind:

The smallest standard frame we have is 7½" x 7½", and requires 1" of clearance from the bottom edge of the bend radius to any applied silkscreening. If the recessed area is smaller than 7½"x 7½", the following applies:

If the recessed area has a depth of **1" or less,** it requires ¼" of clearance from the bottom edge of the bend radius to the silkscreening.

If the recessed area has a depth of **over 1",** it requires 3/8" clearance from the bottom edge of the bend radius to the silkscreening.

These criteria will allow us to do an acceptable job with a minimum of problems.

Lee Bettelyoun
Metals Marking and Prepack Manager

"HMOS" A new generation of digital devices?

Intel's 2147 is a 4K x 1 static RAM with access times of 55 nS. The part is a major improvement in n-channel MOS technology and is rapidly becoming accepted by major users (IBM recently entered into a large contract for the 2147).

The improved performance of the device is attributed to new and better fabrication techniques, called "HMOS" or high-performance MOS by Intel. Other manufacturers are attempting to produce equivalent circuits, but it may take several months for similar devices to be available in large quantities.

the HMOS process

Although no formal definition of HMOS exists, we've defined it as an n-MOS device which: (1) is co-planar, (2) has polysilicon gates, and (3) uses arsenic for drain and source regions. The feature unique to Intel's HMOS is the use of arsenic for drain and source. Typically, phosphorus is used for these regions.

The use of arsenic produces much shallower junctions than phosphorus, resulting in less gate under diffusion and more control of the channel length. This allows narrower polysilicon lines for the gates and reduces capacitance, which increases both the density and speed of circuits.

It has been advertised that HMOS results in propagation delays of ~1nS/gate. Our measurements of clocks on the 2147 confirm this. The devices on the chip had polysilicon widths of approximately 3μm. As the polysilicon widths (thus channel length) are reduced to 2.5μm or less, propagation delays of sub-nanoseconds per gate appear likely. Many n-MOS circuits to be introduced next year are expected to have channel lengths of 2-2.5μm using an HMOS-type process.

This technology not only improves circuit performance using present production lithography techniques, but it is also easily adaptable to new improved lithography processes (such as electron-beam and x-ray lithography.

Nearly all MOS semiconductor manufacturers recognize the potential of this process and presently have programs to add the technique to their production lines.

circuit features

The basic memory cell of the 2147 is illustrated in Figure 1. This is a standard, static cell using depletion loads. (Other vendors are considering replacing the depletion load with a polysilicon resistor.) The circuit is a simple flip-flop which will retain its state until it is changed by applying new voltages to the bit lines while X_i line is high.

Externally, the 2147 uses only a 5-volt power supply. There is, however, a substrate generator on the chip that generates a substrate bias of approximately – 3 volts. The time constant for the substrate is about 35μS when +5 volts are applied to V_{CC}, see Figure 2. When V_{CC} changes from +5 volts to 0 volts, the substrate voltage drops to – 5 volts and slowly (~60 mS) rises to 0 volts, as illustrated in Figure 3.

continued on page 6

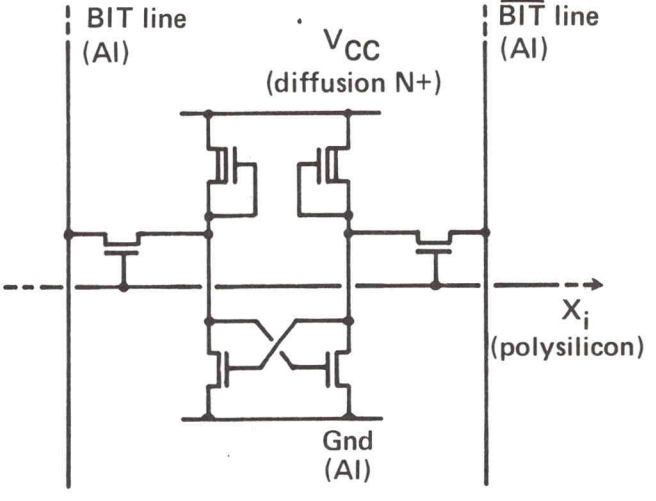


Figure 1 — Memory cell circuit

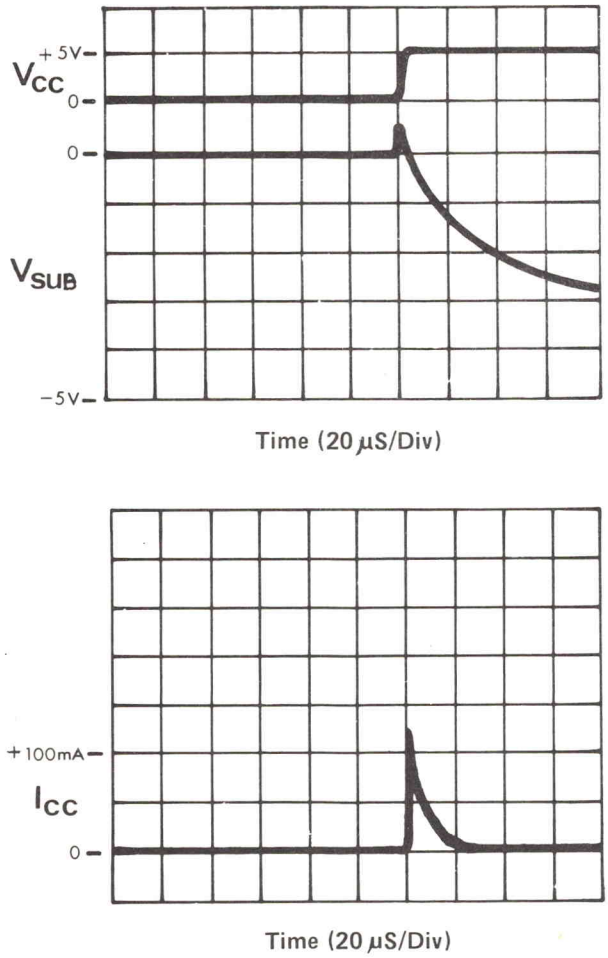


Figure 2 — Turn-on characteristics of substrate bias generator

In order to obtain the power/speed requirements, Intel has used four different threshold voltage transistors on the chip. The threshold voltage of the standard enhancement devices (~0.5V with V_{sub} = 0) is adjusted with only a boron implant, while the threshold voltage of standard depletion mode devices (~– 2V with V_{sub} = 0) is adjusted with only a phosphorus implant. The depletion devices in the cell area appear to be implanted with both boron and phosphorus. This will increase the threshold voltage of the device to about – 1.5 volts, which will in turn increase the resistance of the load and decrease the power consumed in the cell region.

For the power down feature, a transistor with no implants is used in series with some circuits, reducing the current of these circuits when the gate of this transistor is low. This transistor has a threshold voltage of approximately – 0.1 volts with V_{sub} = 0. Therefore, there is little voltage drop across the device under normal operation of the circuit (when gate is high).

processing techniques

The processing schedule of the 2147 is fairly conventional for today's n-MOS technology, with the exception of the arsenic and some other features unique to Intel. The following processing information and the threshold voltages noted previously, were obtained by analyzing chips received by Tek, and not from information supplied by Intel. Thus, there could be some errors and the processes may have changed since the parts we analyzed were produced.

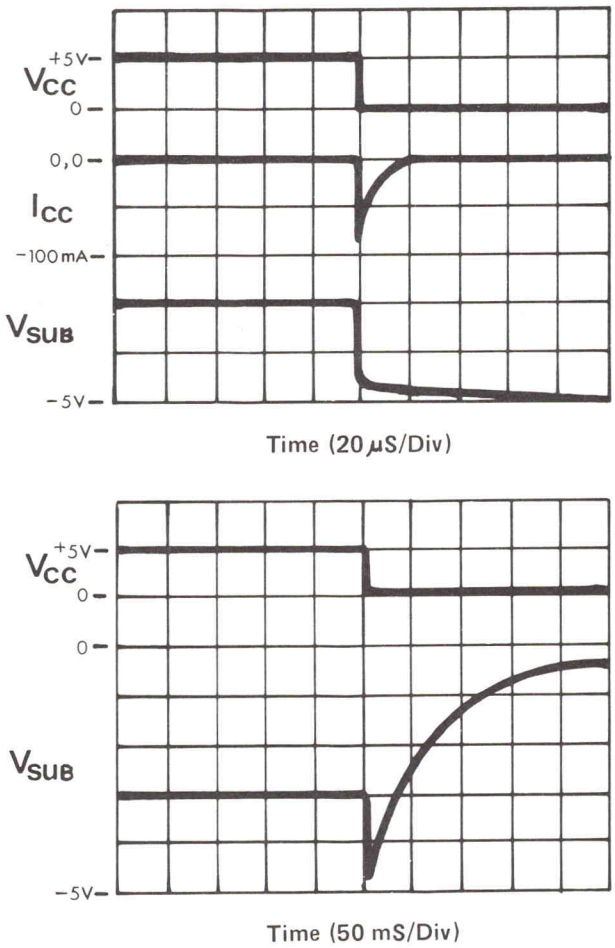


Figure 3 — Shut-down characteristics

A cross-section of a transistor on the 2147 chip is shown in Figure 4. The figure is approximately to scale with some of the measured dimensions included. Some special features to be noted are: (1) the arsenic diffusion may not overlap the boron field implant, (2) the thermo oxide grown on polysilicon consumes the polysilicon both vertically and horizontally, (3) the reflow glass gives very good aluminum step coverage, and (4) a very thick top glass layer is used.

continued on page 7

If the arsenic doesn't overlap the boron field implant, it implies that the breakdown voltage and capacitance of the arsenic-substrate junctions are more influenced by the substrate doping than deep phosphorus junctions. Therefore, it would be expected that the breakdown voltage would be larger and the capacitance would be smaller with the shallow arsenic diffusions than the deep phosphorus diffusions (~1.5μm). This effect has also been noted on the shallow phosphorus diffusions (~7000Å-8000Å) used by MOSTEK in their coplanar process.

The thermo oxide grown on the polysilicon can be used to control the diffusion of arsenic under the gate region. There is then the ability to reduce the under-diffusion to zero by controlling the thermo oxide thickness, which will in turn reduce capacitance and increase speed.

The reflow glass has a very high concentration of phosphorus. After reflowing and etching the contact hole, this glass produces very good aluminum step coverage. Intel deposits a thick layer of top glass, possibly to reduce the amount of moisture that penetrates to the reflow glass. This top layer does not have a high phosphorus concentration.

The arsenic junctions combined with the standard polysilicon-coplanar process appear to offer many advantages in digital circuits over other MOS processing techniques. As lithography techniques improve and circuit voltages are reduced, this process technique is expected to be used to produce denser and faster digital circuits.

Ron Burghard, ext. 6302

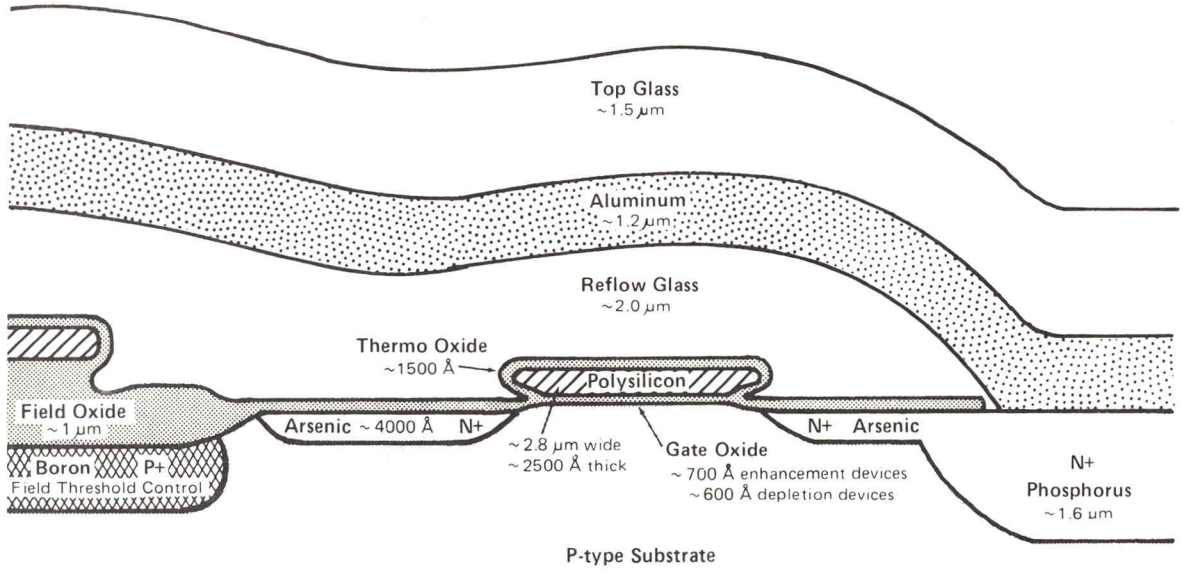


Figure 4 — Cross-section of MOS transistor

Probable Process Sequence (major steps)

1. Initial oxide/nitride (coplanar process)
2. Mask 1 — defines active area
3. Boron implant for field threshold control
4. Field oxidation and removal of initial oxide/nitride layers
5. First gate oxidation
6. Mask 2 — for boron implant
7. Boron implant for threshold control
8. Mask 3 — for phosphorus implant
9. Etch gate oxide for phosphorus implant
10. Phosphorus implant (depletion devices)
11. Second gate oxidation
12. Mask 4 — for buried contact cut (polysilicon to diffusion)
13. Etch oxide for buried contact
14. Deposit polysilicon
15. Phosphorus diffusion of polysilicon and buried contact
16. Mask 5 — defines polysilicon
17. Etch oxide for arsenic implant or diffusion
18. Arsenic implant or diffusion
19. Grow thermo oxide
20. Mask 6 — contact holes for aluminum (first cut)
21. Etch oxide for aluminum contacts
22. Deposit phosphosilicate glass
23. Reflow-deposited glass
24. Mask 7 — contact holes for aluminum (second cut)
15. Deposit aluminum and sinter
26. Mask 8 — define aluminum pattern
27. Mask 9 — define openings for bonding pads

The Kelvin Connection

Most engineers are familiar with the concept of Kelvin connections but not many have practical experience with it. A brief review of principles followed by an example will hopefully clarify when Kelvin contacts are appropriate, and what are the errors associated with Kelvin contacts used for measuring low resistances such as an electrical contact.

Kelvin connections consist of contact pairs with one pair per device terminal. One contact of a Kelvin pair supplies electrical stimulus to the terminal while the other contact senses the response to the stimulus. Another way of putting it is one contact supplies the current while the other contact senses the voltage at the terminal. Sensing the voltage with a separate contact assures that no errors occur due to sensing extraneous voltage drops across the current-supplying leads and contacts.

When are Kelvin contacts appropriate? They are appropriate when the errors due to other connection schemes exceed the desired accuracy of the measurement. Thus, an assessment of the relative errors must be made before a clear choice appears.

Figure 1a

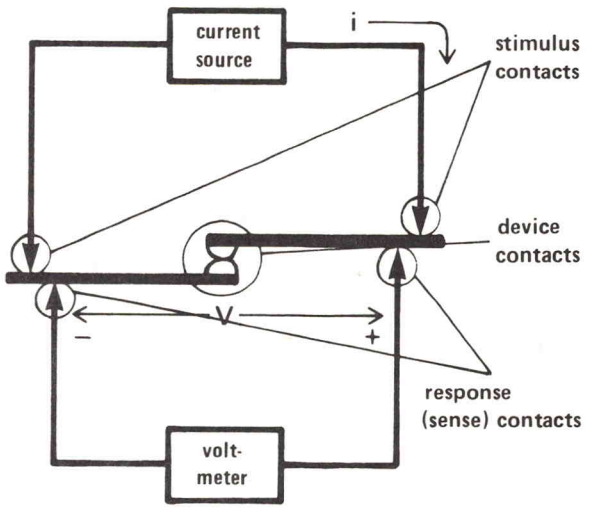
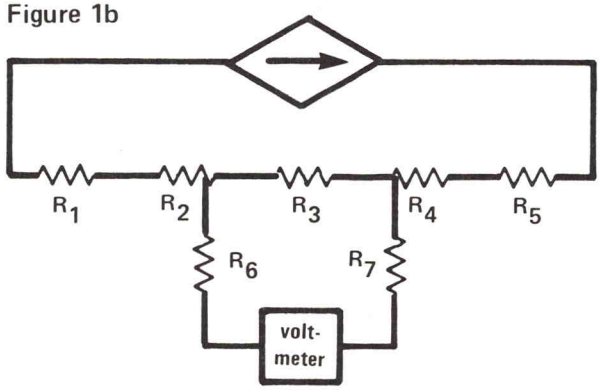


Figure 1b



R_1, R_5 – Current source lead bulk resistances

R_2, R_4 – Stimulus contact resistance

R_6, R_7 – Response contact resistance and voltmeter lead resistance

R_3 – Device contact resistance and device lead resistance

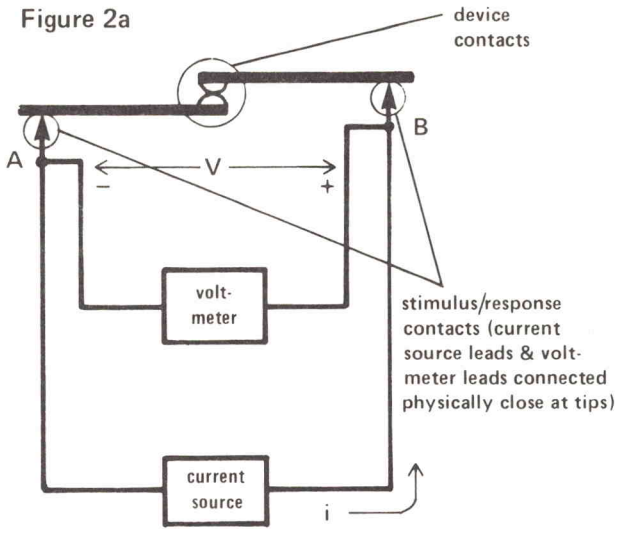
Suppose we want to measure the contact resistance of a power switch or power connector. Figures 1a and 2a show different ways of connecting a current source and voltmeter to the device for a standard force current–measure voltage arrangement.

In Figure 1a we see a four-terminal Kelvin connection for a contact resistance measurement. Figure 1b shows the schematic representation. If a high-impedance voltmeter is used, virtually no current flows through the response contact interfaces and voltmeter leads. Thus, the only voltage sensed by the voltmeter is voltage drop across the device contact resistance and device leads (R_3).

In Figure 2a we see a two-terminal connection similar to Figure 1a, which is Kelvin sensing to points A and B. This connection eliminates errors in measurement due to voltage drops across the current source leads but still has an error due to voltage drops across the stimulus-response contacts. This is the kind of error introduced into measurements when Kelvin sensing occurs up to a test socket or connector but the socket or connector itself is not Kelvin sensing. Figure 2b shows the schematic representation.

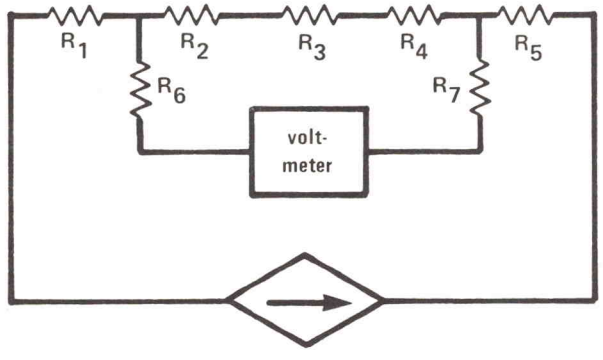
continued on page 9

Figure 2a



Which circuit should we use? The circuit in Figure 2 is simpler and more convenient, but will it be adequate for 10% accuracy? A typical clip contact used for measurement has a contact resistance plus bulk resistance of one to ten milliohms. A typical power switch has a contact plus lead resistance of two to twenty milliohms. Suppose we consider the extremes to determine the range of error.

Figure 2b



R_1, R_5 – Current source lead bulk resistances

R_2, R_4 – Stimulus contact resistance

R_6, R_7 – Response contact resistance and voltmeter lead resistance

R_3 – Device contact resistance and device lead resistance

Case 1. The resistance of each clip is one milliohm and the contact plus lead resistance is twenty milliohms.

$$\text{Error} = 100\% \times \frac{2m\Omega}{20m\Omega} = 10\%$$

Case 2. The resistance of each clip is ten milliohms and the contact plus lead resistance is two milliohms.

$$\text{Error} = 100\% \times \frac{20m\Omega}{2m\Omega} = 1000\%$$

All other cases would be between these extremes for this example. Clearly we cannot rely on 10% accuracy using the connection in Figure 2. We must use a full four-terminal Kelvin connection.

Whether or not you use Kelvin contacts is a matter of accuracy. If you must use a Kelvin connection, convenient contacts are available for axial lead devices and some Kelvin sockets also exist. Unusual pinouts will require custom built fixtures for Kelvin connection.

If you'd like more information on Kelvin connections, please contact me at 58-299, ext. 6365.

Paul Johnson
Electromechanical Component Engineering

Two gas displays given "01" P/Ns

Part numbers 150-1015-00 (2-digit, 0.3", 7 segment) and 150-1039-00 (1½ digit, 0.3", 7 segment) have both had -01 numbers set up. The -01 numbers are identical units to the -00's, except the -01 parts contain small amounts of Krypton gas which makes the initial ionization time a guaranteed five seconds or less.

All instruments that used the 150-1015-00 and most of the instruments that use the 150-1039-00 have been modified. Therefore, if you are considering these displays, the -01 numbers are the recommended devices.

For more information, contact **Betty Lise Anderson, ext. 5389.**

Calculating junction temperatures

In order to run reliability predictions using computer programs (such as MTBF) which require input of the part junction temperature, you must know the part power dissipation and thermal resistance.

Following is a list of thermal resistances of various IC package styles. The information was drawn from available vendor data (TI and Signetics). The junction temperature may then be calculated by:

$$T_J = T_A + \theta_{JA} \times P_D \text{ or } T_J = T_C + \theta_{JC} \times P_D$$

IC package pins	case style	θ_{JC} in °C/W	θ_{JA} in °C/W
8	metal can	40	120
8	plastic	45	125
8	cerdip	30	110
14/16	plastic	45	120
14/16	cerdip	35	100
20	plastic	37	88
20	cerdip	24	75
24	plastic	55	120
24	cerdip	26	60
40	plastic	50	110
40	cerdip	25	55

θ_{JC} = thermal resistance of junction to case

θ_{JA} = thermal resistance of junction to ambient air

submitted by Ron Schwartz, ext. 6511

Contact CE for evaluation information

You may not have noticed, but the Purchased Part Initiation Form (PPIF) has the following notation under supplier name and part number in the Component Evaluation section:

> This part (has) (has not) been evaluated

If the device you want part-numbered has **not** been evaluated, you are taking a company risk. To buy the best components for our dollars and equipment needs, always have samples evaluated **before** purchase. There may be a reason why that part has not been purchased before.

Keep in mind that good evaluations take time, but will save both dollars and time in the long run.

Contact the appropriate component evaluation engineer for information on specific components.

ATTENTION DESIGNERS:

We have identified problems with the following components. For further information, please contact **Bill Pfeifer, ext. 6303.**

8259 priority interrupt controller
8048 single chip microcomputer
8155 256-byte RAM, I/O and timer device
8253 16-bit timer
8257 quad DMA controller

TECHNICAL STANDARDS

The function of Technical Standards is to identify, describe, and document standard processes, procedures, and practices within the Tektronix complex, and to insure these standards are consistent with established national and international standards. Technical Standards also provides a central repository for standards and specifications required at Tektronix. *Chuck Sullivan, manager (58-187)*

new and revised standards available from Technical Standards

ABC-NAVY-STD-50 American-British-Canadian Naval Standardization Program — Surface Texture (24 June 1970)

ANSI C57.12.00—1973 General Requirements for Distribution, Power, and Regulating Transformers

ANSI C57.12.00a & b—1978 Thermal and Short-Circuit Requirements, Supplements to ANSI-C57.12.00—1973

ANSI C57.12.90—1973 Test Code for Distribution, Power, and Regulating Transformers

ANSI ExSC 435—April 1978 American National Standards Committees

ANSI Y14 Report—Number 2 Guidelines for Documenting of Computer Systems Used in Computer-Aided Preparation of Product Definition Data (December 1974)

ANSI Y14 Report—Number 3 Guidelines for Documenting of Computer Systems Used in Computer-Aided Preparation of Product Definition Data (December 1974)

AT&T Bell System Technical Reference Pub. 40000, Catalog, January 1978

1978 British Standards Institute Yearbook of British Standards

BSI BS 2754:1976 Memorandum—Construction of Electrical Equipment for Protection Against Electric Shock (Amend 1 slip incl)

BSI BS 3861:Part 3:1970 Specification for Electrical Safety of Office Machines: Part 3, General Requirements and Tests for Double-Insulated and All-Insulated Equipment

FCC Volume III of Rules and Regulations, August 1976 Edition, Transmittal Sheet No. 8

IEC C.I.S.P.R. Pub. 16 (1977) C.I.S.P.R. Specification for Radio Interference Measuring Apparatus and Measurement Methods

IEC Pub. 380 (1977) Safety of Electrically Energized Office Machines

ISO 3243 Keyboards for Countries Whose Languages Have Alphabetic Extenders—Guidelines for Harmonization (15 February 1973)

MIL-C-3885D Cable Assemblies and Cord Assemblies, Electrical, (18 July 1978)

MIL-C-28748/10C Connectors, Electrical, Rectangular, Rack and Panel, Polarized Center Jackscrew or Guidepin Style, Crimp Type Removable Socket Contacts, Size 16 (31 July 1978)

MIL-C-28840/4 Connectors, Electrical, Circular Threaded, High Shock, High Density, Shipboard, Metal Conduit for EMI Shielding (21 August 1978)

MIL-C-28840/27 Connector, Electrical, Circular Threaded, High Shock, High Density, Shipboard, Backshell, 45°, Metal Conduit for EMI Shielding (21 August 1978)

MIL-C-28840/30 Connectors, Electrical Circular Threaded, High Shock, High Density, Shipboard, Metal Conduit Coupling (21 August 1978)

MIL-C-39024/13A Connectors, Electrical, Test Point Type, Printed Wiring Type; Single Test Point (Right Angle, 2-Leg Mounting), Low Voltage, .080 (9 June 1978)

MIL-C-49142 Connector, Triaxial, Radiofrequency, General Specification for (17 April 1978)

MIL-C-49142/1 Connector, Triaxial, Radiofrequency (Series TRC-Cabled Plug, Socket Contact, Class 2) (17 April 1978)

MIL-C-49142/2 Connector, Triaxial, Radiofrequency (Series TRC-Receptacle, Pin Contacts, Jam Nut Mounted, Class 2) (17 April 1978)

MIL-C-49142/3 Connector, Triaxial, Radiofrequency (Series TRB-Plug, Pin Contact, Class 2) (17 April 1978)

MIL-C-49142/4 Connector, Triaxial, Radiofrequency (Series TRB-Receptacle, Socket Contact, Jam Nut Mounted, Class 2) (17 April 1978)

continued on page 12

TECHNICAL STANDARDS

CONTINUED

MIL-C-55302/113C Connectors, Printed Circuit Subassembly and Accessories: Plug, Straight-thru, 30 thru 110 Contact Positions, Crimp Removable Contacts (.100 Sq Grid) (4 August 1978)

MIL-M-28787/140A Modules, Standard Electronic Multiplexer, Digital, Key Code AGD (3 July 1978)

MIL-M-28787/186B Modules, Standard Electronic Generator, Function, MSB, Analog, Key Code SHY (30 June 1978)

MIL-M-28787/208 Modules, Standard Electronic Programmable Timer, Digital, Key Code HQE, (12 June 1978)

MIL-M-28787/246 Modules, Standard Electronic Optical Isolator, Digital, Key Code MUM, (7 July 1978)

MIL-M-28787/278 Modules, Standard Electronic Driver, Lamp/Relay, Digital, Key Code FQD, (12 June 1978)

MIL-M-38510/63 Microcircuits, Digital, ECL, and Quad Translator, Monolithic Silicon, (14 July 1978)

MIL-M-38510/110 Microcircuits, Linear, Quad Operational Amplifiers, Monolithic Silicon (25 May 1978)

MIL-M-38510/112 Microcircuits, Linear, Voltage Comparators, Monolithic Silicon (26 July 1978)

MIL-M-38510/172 Microcircuits, Digital, CMOS, AND-OR-INVERT, EXCLUSIVE-OR, EXCLUSIVE-NOR Gates, Monolithic Silicon, Positive Logic (9 June 1978)

MIL-S-8805/8E Switches, Sensitive, SPDT, Leaf Actuator, Low Level to 4 Amps, Hermetic Seal (24 August 1978)

MIL-S-24236/1F Switches, Thermostatic, (Bimetallic), Subminiature, Type I, Hermetically Sealed, Single-Pole, Single Throw (SPST), 5 Amperes, (27 June 1978)

MIL-S-24236/20D Switches, Thermostatic, (Bimetallic), Subminiature, Type I, Hermetically Sealed, Single-Pole, Single-Throw (SPST), 2 Amperes (8 June 1978)

MIL-S-24236/21A Switches, Thermostatic, (Bimetallic), Subminiature, Type I, Hermetically Sealed, Single-Pole, Single-Throw (SPST), 5 Amperes (10 July 1978)

MIL-S-81619/8B Switch, Solid State Transducer, 2-Axis Joystick (15 August 1978)

MIL-STD-870A Cadmium Plating, Low Embrittlement, Electrodeposition (22 August 1978)

MIL-STD-1504A Abrasive Blasting (23 August 1978)

NBS Spec. Pub. 400-44 Safe Operating Area Limits for Power Transistors (Sept. 1977)

NBS Tech. Note 976 International Trends and Developments of Importance to the Metrication Plans of the U. S. Construction Community (June 1978)

UL 62 Standard for Flexible Cord and Fixture Wire, Eleventh Edition, Revision October 11, 1978

cancelled military document

MIL-M-24198 Notice 1, 22 August 1978, Specification MIL-M-24198 (SHIPS), dated 18 August 1966, is hereby cancelled.

correction

Issue 264 of Component News gave an incorrect number for the Test Method Standard – Cables, Jacket Removal. The correct number for this standard is 062-3923-00.

for information on the above publications, please call Carol Whitmore, Technical Standards, ext. 7976.

ComponentNewsNewComponents

This column is designed to provide timely information regarding new components, vendors, availability and price. "New Components" can also be used as an informal update to the Common Design Parts Catalogs. Samples may or may not be available in Engineering Stock.

Vendor	No.	Description	When available	Tek P/N	Approx. cost	Engineer to contact
		analog devices				
Analog Devices	7524	D/A, 8-bit, CMOS, input latches, 100nS settling	now	no P/N	$ 3.00	Don Gladden, 6700
Analog Devices	7525	D/A, 3½ digit, BCD monolithic CMOS, 1-μS	now	no P/N	8.50	Don Gladden, 6700
Analog Devices	7533	D/A, 10-bit CMOS, 600nS maximum settling	now	no P/N	6.00	Don Gladden, 6700
Analog Devices	7541	D/A, 12-bit CMOS, 1-μS maximum settling	now	no P/N	12.00	Don Gladden, 6700
Analog Devices	565	D/A, 12-bit monolithic, internal ref., 400 nS maximum settling time	now	no P/N	14.00	Don Gladden, 6700
		electromechanical devices				
SAFT	--	Battery, 6V, 10AH lead acid	8 weeks	no P/N	--	Byron Witt, 5417
SAFT	--	Battery, 2V, 10AH lead acid	8 weeks	no P/N	--	Byron Witt, 5417
Capcon	LST-060	Tubing, EMI suppressant	now (sample)	no P/N	--	Byron Witt, 5417
ITT	--	Wire, #22AWG, 15 KV	now	176-0347-00	--	Rod Christiansen, 5953
Uniform Tube	--	Coax, 50Ω semi-rigid	--	175-2314-00	--	Rod Christiansen, 5953
Zephyr/3M	--	Cable assembly, flat ribbon, 40 cond., 28 AWG, 3.5" long, w/.025" sq. pin connectors	now	175-2353-00	--	Rod Christiansen, 5953
Gordos	761A0552-1	Reed relay, SPST, 5V coil	soon	148-0122-00	1.03	Paul Johnson, 6365
Gordos	NA	Reed relay, DPST, 12V coil	soon	148-0123-00	2.91	Paul Johnson, 6365
Gordos	NA	Reed relay, SPST, 6V coil	soon	148-0124-00	1.66	Paul Johnson, 6365
Gordos	NA	Reed relay, SPST, 12V coil	soon	148-0125-00	1.58	Paul Johnson, 6365
EAC	BEE-5	Reed relay, SPST, 5V coil	soon	148-0126-00	1.32	Paul Johnson, 6365
		optoelectronic and passive devices				
Monsanto	MAN73A	LED display, overflow and polarity indicator, 0.3" char., C.A.	soon	150-1069-00	1.30	Betty Anderson, 6389
Monsanto	MV57124	LED, rect., red, .125"x.220" 4 mcd, 2V	soon	no P/N	.50	Betty Anderson, 6389

COMPONENT CHECKLIST

The "Component Checklist" is intended to draw attention to problems or changes that affect circuit design. This listing includes: catalog and spec changes or discrepancies; availability and price changes; production problems; design recommendations; and notification of when and how problems were solved. For those problems of a continuing nature, periodic reminders with additional details will be included as needed.

	Tek P/N	Vendor	Description of Part	Who to Contact
✓	156-1257-00	Intel	8291 GPIB	Jim Howe, 6303

A problem has been found in the 8291 which appears to be an interaction between interrupt status bits. It is a problem which will cause confusion in any polled software or in an interrupt-driven software where the interrupt service routine is slower than the GPIB controller. The interrupt status bit SPASC will be **inverted,** rather than **set,** if there is a change in SPAS while ADSC bit is true.

The sequence for a serial poll will normally involve an Address State Change (ADSC) on receipt of My Talk Address (MTA), a Serial Poll Active State Change (SPASC) on ATN going false, a second SPASC on ATN going true following the transfer of the status byte, and a second ADSC on receipt of an Other Talk Address (OTA). In polled software, there will normally be two changes in SPAS between successive reads of the interrupt status register, with the first **setting** and the second **clearing** the SPASC bit; thus, the serial poll would go undetected.

It is obvious that no reasonable software design can accommodate this obscure state of affairs. Intel has been informed.

Dick Dunipace 94 344

component news

Published by Technical Communications
58-299 ext. 6867

Jacquie Calame, editor
Birdie Dalrymple, illustrator
Lola Janes, writer

To submit an article, call Jacquie on ext. 6867 or stop by 58-299.

For mailing list changes, contact Kelley Turner, (19-407), ext. 5835.

company confidential