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Instructions

12RM25
68000 MNEMONICS ROM PACK
with Option 02 or 04

The 68000 Mnemonics ROM Pack configures a 1240 Logic Analyzer to acquire and disassemble data from a 68000 microprocessor. The PM203 Personality Module monitors the contents of the 68000 pipeline, provides fetch and flush prediction, arranges the address and data lines, and generates some modified control lines for the use by the ROM Pack. (The PM203 is required for successful use of the 68000 Mnemonics ROM Pack. PM203s are ordered as options to this ROM Pack. Option 02 is for 64-pin DIP packages. Option 04 is for 68000s with a pin grid array package.)

The 12RM25 was developed using the GN7 mask of the 68000. Minor variations in operation may occur with other mask versions.

NOTE

To use this ROM Pack, your 1240 Logic Analyzer must be equipped with at least three 1240D2 cards.

Insert this manual at the back of your *1240 Logic Analyzer Operator's Manual*, or in the 1240 Optional Accessories binder.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL

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OVERVIEW

THIS MANUAL

This manual describes how the 68000 Mnemonics ROM Pack configures the 1240 Logic Analyzer for use with 68000 microprocessors, how to connect the 1240 to the 68000 using the PM203 Personality Module, and how to acquire, display, and interpret data. It also describes the four data display formats available when a 68000 Mnemonics ROM Pack is installed in your 1240 and how you can get a printout of these state table displays.

OTHER MANUALS

To use the 68000 Mnemonics ROM Pack, you should be familiar with the operation of the 1240 Logic Analyzer and the 68000 microprocessor. Refer to the *1240 Logic Analyzer Operator's Manual* and the operator's manuals for any communication packs that you may be using, as well as the *M68000 16/32-Bit Microprocessor Programmer's Reference Manual* (Fourth Edition, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632).

THE PM203

The PM203 Personality Module is designed to provide a convenient interface between the 1240 Logic Analyzer and your 68000-based system. The 68000 Mnemonics ROM Pack cannot be used to acquire data without a PM203. The PM203 also monitors the contents of the 68000 pipeline and provides fetch and flush prediction, clocking, and synthesis of control lines.

PM203s designed to support the 12RM25 68000 ROM Pack are the 12RM25 Option 02, and 12RM25 Option 04. The Option 02 supports the Motorola 68000 DIP package; the Option 04 supports the Motorola 68000 pin-grid array.

PM203 SERVICE

Servicing your own PM203 Personality Module is only recommended if you have a DAS 9100 from Tektronix, since full service of the PM203 requires the use of a DAS 9100 equipped with a 91A24 module, a 91P16 module, and a 91P32 module. If you have such a DAS and want to service your own PM203 Personality Module, you will also need a *PM203 Service Kit*.

CONNECTING TO THE 68000

CONNECTING THE PM203 TO THE 68000

Connect the PM203 Personality Module to your circuitry using one of the following procedures:

DIP-Adapter Socket:

1. Turn off the power to your 68000 system under test. If the PM203 is connected to the 1240, turn off the power to the 1240.

CAUTION

Only connect the PM203 to your 68000 system in a static-free environment and only after you have grounded yourself to drain static electricity.

2. Remove the 68000 from your system.
3. Put the flexible circuit's DIP-adapter into your 68000 system's socket. Refer to Figure 1a. Be sure to orient pin 1 of the adapter to pin 1 of the socket.
4. Insert your 68000 into the DIP-adapter. Again, be sure to orient pin 1 of the microprocessor to pin 1 of the adapter.

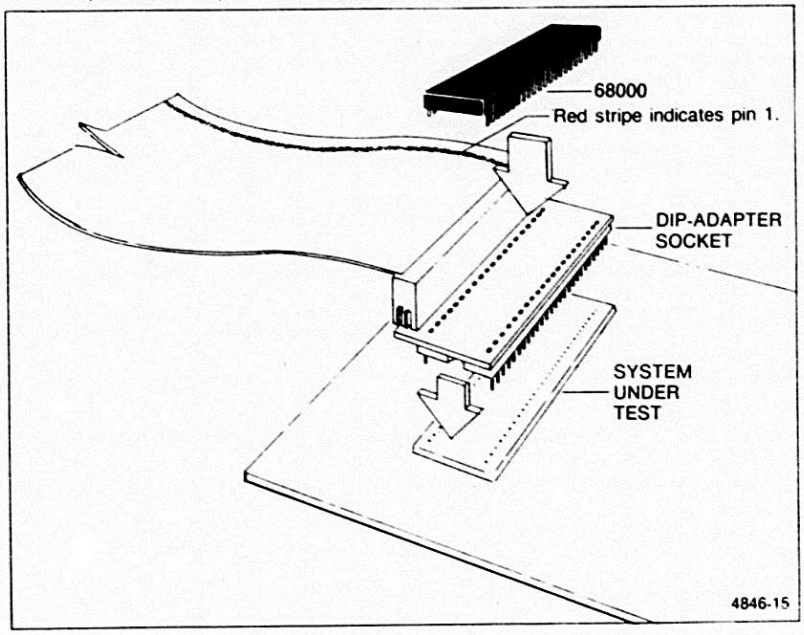


Figure 1a. Connecting Option 02 to the system under test (BO30100 and up).

DIP-Clip Connector:

1. Turn off the power to your 68000 system under test. If the PM203 is connected to the 1240, turn off the power to the 1240.

CAUTION

Only connect the PM203 to your 68000 system in a static-free environment and only after you have grounded yourself to drain static electricity.

2. Attach the DIP clip connector on your (Option 02) PM203 over the microprocessor in your test system. Refer to Figure 1. Be sure the clip is oriented so that pin 1 connects to pin 1. The brown wire on the edge of the ribbon cable should be nearest to the pin 1 end of the microprocessor.

CAUTION

Applying pressure to the ribbon cable where it connects to the DIP clip will cause the wires to age rapidly and eventually break. Avoid applying any pressure to the wires of the ribbon cable as you connect and disconnect the DIP clip.

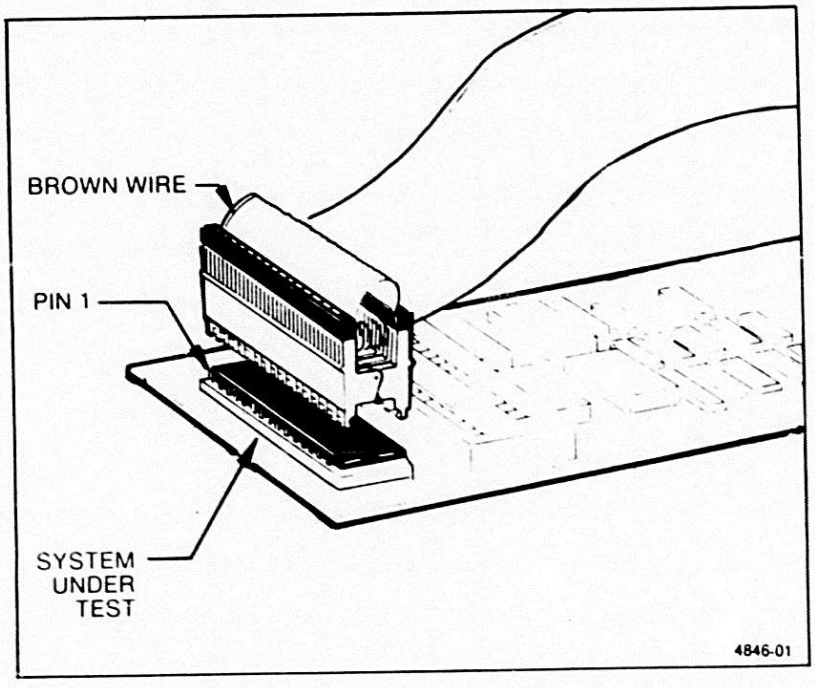


Figure 1. Connecting Option 02 to the system under test (BO20999 and down).

Pin Grid Array:

1. Turn off the power to your 68000 system under test. If the PM203 is connected to the 1240, turn off the power to the 1240.

WARNING

Only connect the PM203 to your 68000 system in a static-free environment and only after you have grounded yourself to drain static electricity.

2. Remove the 68000 from the pin grid array connector in your system under test.
3. Replace the 68000 with the (Option 04) PM203 pin grid array plug.
4. Put the 68000 into the top of the Option 04 plug. Make sure that pin A1 on the pin grid array, plug, and test system all match. Refer to Figure 2a or 2, depending on the serial number of your personality module.

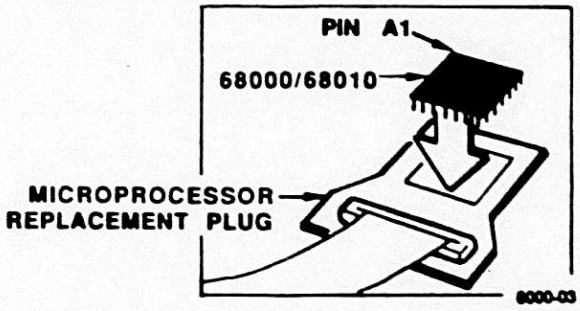


Figure 2a. Connecting Option 04 to the system under test (BO40100 and up).

CAUTION

Avoid nicking the edge of the flexible circuit of the PM203. It is very resistant to stretching and bending, as long as its surface is intact. But, if its edge is nicked, its resistance to tearing is greatly lowered.

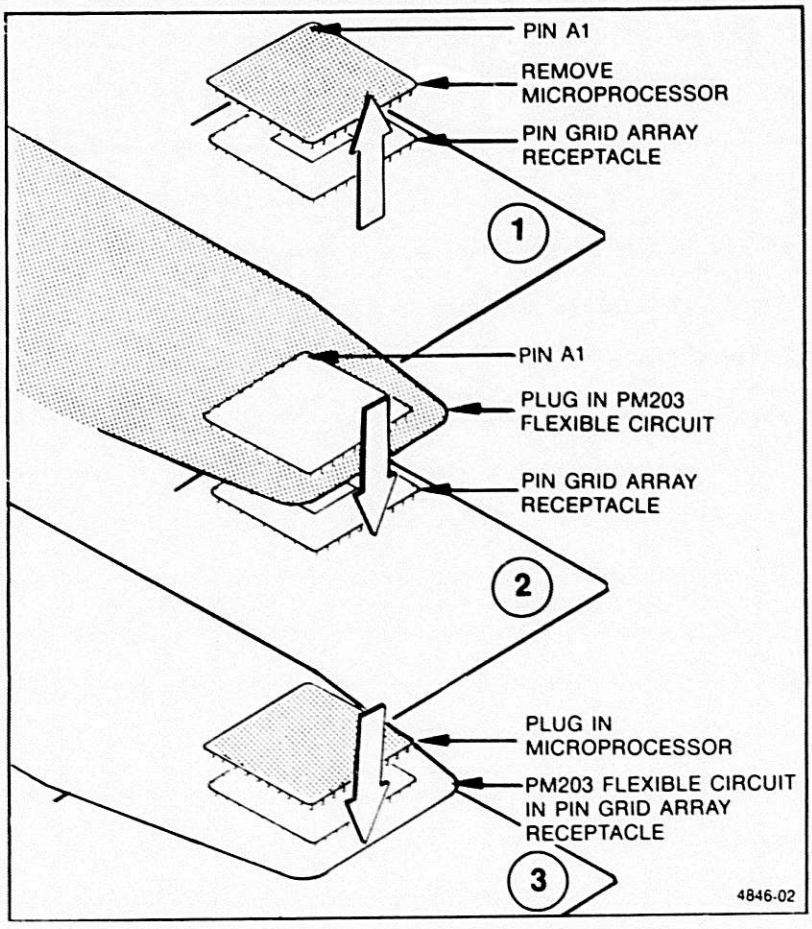


Figure 2. Connecting Option 04 to the system under test (BO30999 and down).

CONNECTING THE PM203 TO THE 1240

Remove any data acquisition probes from the three highest-numbered 1240D2 cards of the 1240. The ribbon cables from the PM203 connect directly to the 1240D2 18-channel acquisition cards of the 1240; no data acquisition probes are required. Connect the connectors on all six ribbon cables to the pods of the 1240 in accordance with Table 1.

Table 1
PM203 TO 1240 CONNECTIONS

PM203 Connector		1240 Pod I.D. Number for:	
1240	(DAS)	3 Acq. Cards	4 Acq. Cards
0	(1A)	0	2
1	(1B)	1	3
2	(1C)	2	4
3	(2A)	3	5
4	(2B)	4	6
5	(2C)	5	7

CONNECTION OVERVIEW

Table 2 provides an overview of the connections between the 1240 Logic Analyzer equipped with a 68000 Mnemonics ROM Pack and your 68000 microprocessor through the PM203 Personality Module.

Table 2
1240 TO PM203 AND 68000 SIGNAL MAP

1240 SCREEN			CONNECTION		68000 (OR PM203)	
GROUP	BIT	C/Q	POD*	CHAN	SIGNAL	PIN (DIP/PGA)
CNTL	7	-	2	7	$\overline{\text{RESET}}$	18/20
	6	-	2	6	$\overline{\text{UDS}}$	7/7
	5	-	2	5	$\overline{\text{BGACK}}$	12/12
	4	-	2	4	$\overline{\text{IRQ}}$	PM203
	3	-	2	3	SUP/$\overline{\text{USER}}$	PM203
	2	-	2	2	$\overline{\text{FETCH}}$	PM203
	1	-	2	1	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$)	PM203
	0	-	2	0	ENCODED	PM203
ADDR	23	-	5	7	A_{23}	52/55
	22	-	5	6	A_{22}	51/54
	21	-	5	5	A_{21}	50/53
	20	-	5	4	A_{20}	48/51
	19	-	5	3	A_{19}	47/50
	18	-	5	2	A_{18}	46/49
	17	-	5	1	A_{17}	45/48
	16	-	5	0	A_{16}	44/47
	15	-	4	7	A_{15}	43/46
	14	-	4	6	A_{14}	42/45
	13	-	4	5	A_{13}	41/44
	12	-	4	4	A_{12}	40/43
	11	-	4	3	A_{11}	39/42
	10	-	4	2	A_{10}	38/41
	9	-	4	1	A_9	37/40
	8	-	4	0	A_8	36/39
	7	-	1	7	A_7	35/38
	6	-	1	6	A_6	34/37
	5	-	1	5	A_5	33/36
	4	-	1	4	A_4	32/35
	3	-	1	3	A_3	31/34
	2	-	1	2	A_2	30/33
	1	-	1	1	A_1	29/32
	0	-	1	0	$\overline{\text{UDS}}$	7/7
DATA	15	-	3	7	D_{15}	54/58
	14	-	3	6	D_{14}	55/59
	13	-	3	5	D_{13}	56/60
	12	-	3	4	D_{12}	57/61
	11	-	3	3	D_{11}	58/62
	10	-	3	2	D_{10}	59/63
	9	-	3	1	D_9	60/64
	8	-	3	0	D_8	61/65
	7	-	0	7	D_7	62/66
	6	-	0	6	D_6	63/67
	5	-	0	5	D_5	64/68
	4	-	0	4	D_4	1/1
	3	-	0	3	D_3	2/2
	2	-	0	2	D_2	3/3
	1	-	0	1	D_1	4/4
	0	-	0	0	D_0	5/5
(none)		-	0	8	reserved for	rom pack
(none)		-	1	8	reserved for	rom pack
unused		P1	1	C/Q	CLK	15/15
(none)		P0	0	C/Q	DS	PM203

* Pod numbers are shown for a 1240 with three 1240D2 acquisition cards installed. If your 1240 has four acquisition cards, add 2 to the pod numbers given.

ROM PACK INSTALLATION

1240 CONFIGURATION

In order to acquire data from a 68000 microprocessor using the 68000 Mnemonics ROM Pack, you must have a 1240 Logic Analyzer equipped with at least three 1240D2 18-channel Data Acquisition Cards.

NOTE

The 68000 Mnemonics ROM Pack will not set up the 1240 or disassemble data when it is installed in a 1240 with less than three 1240D2 acquisition cards.

INSTALLING THE ROM PACK

CAUTION

Static discharge can damage the semiconductor devices in a Mnemonics ROM Pack. Discharge static from a pack before installing it by momentarily laying the pack, label side up, on the top of the 1240.

To install the 68000 Mnemonics ROM Pack in your 1240 Logic Analyzer, locate the slot on the right side of the instrument, beneath the probe connectors. Insert the connector end of the ROM Pack, with the label up, past the hinged slot cover and into the memory pack connector. (The mechanical design of the pack ensures that it cannot be installed incorrectly.) Refer to Figure 3.

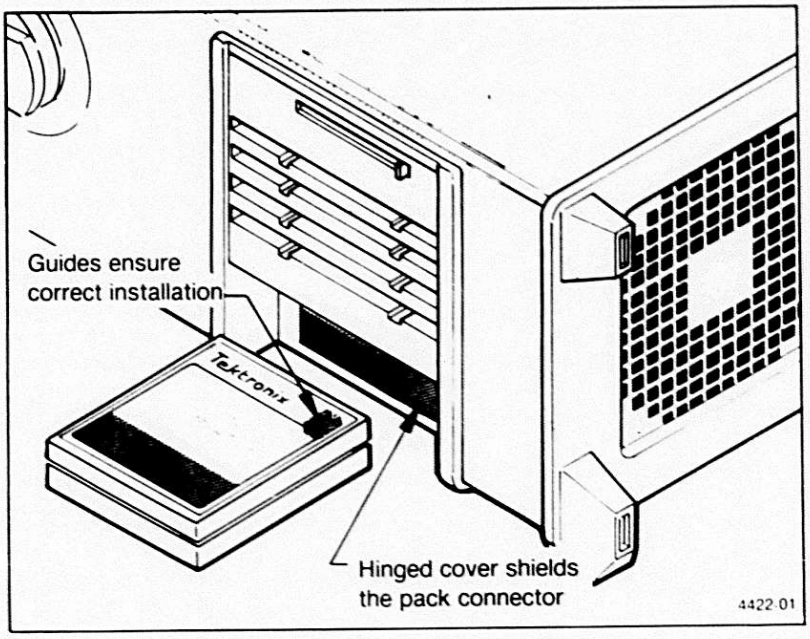


Figure 3. Installing the ROM Pack in a 1240.

NOTE

Power up the 1240 before powering up your system under test. Powering up your system first may result in a soft failure of your system.

Power up your 1240, then your system under test. The contents of the ROM Pack will be loaded automatically at power-up. If your 1240 is already on when the ROM Pack was installed, follow the next procedure, *Loading the ROM Pack Contents.*

NOTE

The 1240 should use the same power source as the system under test. Otherwise, differences between system grounds may cause inconsistent acquisition.

LOADING THE ROM PACK CONTENTS

Enter the Storage Memory Manager menu. Then press the LOAD NEW PACK soft key. The ROM Pack is now loaded.

CAUTION

Do not remove the ROM Pack while you are in any menu other than Storage Memory Manager. Removing it at any other time may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

REMOVING THE ROM PACK

To unload the ROM Pack from the 1240, enter the Storage Memory Manager menu, pull the ROM Pack straight out of the 1240 (it is not necessary to power down) and press LOAD NEW PACK.

CAUTION

After removing the ROM Pack, do not leave the Storage Memory Manager menu without pressing the LOAD NEW PACK soft key. Doing so may cause complete disruption of the 1240's internal memory. To restore the 1240, turn it off and back on.

THE SETUP SUPPLIED BY THE ROM PACK

When the 68000 Mnemonics ROM Pack is loaded into a 1240 with three or more 1240D2 cards, several things happen:

- The 1240 enters Operation Level 2, ADVANCED STATE ANALYSIS. If you manually leave level 2 for levels 0 or 1, you will ruin the setup supplied by the ROM Pack. Using level 3 (after you load the pack) will not cause a problem.
- All 1240D2 chaining is turned off.
- The thresholds are set to TTL on the pods used by this ROM Pack.
- All polarities are set to 1 (positive - true) on the pods used by this ROM Pack.
- T2 is defined as SYNC and used to clock the ADDR, DATA, and CNTL groups. See *Timebase Definitions* later in this manual.
- The input radix of the CNTL group is set to binary, while the output radix of the CNTL group and both radices of the ADDR and DATA groups are set to hexadecimal.

NOTE

If you attempt to use the 68000 Mnemonics ROM Pack in a 1240 that does not have at least three 1240D2 cards, the 1240 setup will not be modified.

Table 3 summarizes the way the 68000 Mnemonics ROM Pack sets up the last three 18-channel cards in the 1240.

Table 3
HOW THE 68000 ROM PACK SETS UP THE 1240

GROUP	TIME BASE	INPUT RADIX	DISPLAY RADIX	THRESHOLD, POLARITY	POD*: CHANNELS
CNTL	T2	BIN	HEX**	TTL, all +	2: 7-0
ADDR	T2	HEX	HEX	TTL, all +	5: 7-0
	T2	HEX	HEX	TTL, all +	4: 7-0
	T2	HEX	HEX	TTL, all +	1: 7-0
DATA	T2	HEX	HEX	TTL, all +	3: 7-0
	T2	HEX	HEX	TTL, all +	0: 7-0

* Pod numbers are shown for a 1240 with a total of three 1240D2 acquisition cards installed. If your 1240 has four acquisition cards, add 2 to the pod numbers given.

** The control lines are normally displayed in hexadecimal to conserve space in the state, absolute, hardware, and software formats. If you desire a different radix, you can enter the Channel Grouping menu and select it. The control line input radix default is binary to facilitate triggering.

MENU AND DATA DISPLAY DIFFERENCES

- The Timebase, Memory Config, and Channel Grouping menus are set up as shown in Table 3. Do not change these settings except as described in the subsection, *What You May Change*.
- Every menu that uses groups contains the CNTL, ADDR, and DATA groups set up by the ROM Pack.
- If a 1200C01 RS232C or a 1200C11 Parallel Printer COMM Pack is installed, the COMM PORT CONTROL menu is replaced by the LINE PRINTER OUTPUT menu. Line printer operation is described later in this manual.
- The STATE TABLE soft key label changes to 68000 STATE TABLE while you are in the State Table menu.
- Also in the State Table display, GLITCHES ON/OFF is replaced by a FORMAT select field. This is where you choose a data display format. The choices are STATE, ABSOLUTE, HARDWARE, and SOFTWARE. The differences between these formats are discussed in detail later in this manual. You can still make the choice of GLITCHES ON or GLITCHES OFF in the Timing Diagram menu; the State Table display will reflect that choice.
- In the Timing Diagram display, the active cursor value at the bottom of the display is shown in STATE, ABSOLUTE, or HARDWARE format depending on the selection made in the State Table menu. (If you select SOFTWARE disassembly in the State Table menu, readouts in the Timing Diagram will appear in HARDWARE format.)

TIMEBASE DEFINITIONS

The 68000 Mnemonics ROM Pack sets up the 1240 to use Timebase 2 in the SYNC mode. Timebase T2 is defined as the falling edge of a PM203-synthesized clock, DS, connected to the clock line of pod 0 (pod 2 if four acquisition cards are present). DS is a clock signal that the PM203 generates from the 68000's $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ (Upper and Lower Data Strobes). The falling edge of T2 is used to store the DATA, CNTL and ADDR groups. The 1240 will not disassemble correctly if you do not use this clock.

Processor Clock. The 68000 CLK signal from pin 15 of the 68000 is available on the clock line of pod 1 (pod 3 if four acquisition cards are present). You might wish to use this clock to monitor the activity on the bus during other parts of the bus cycle. However, the subtleties of PM203 timing may limit the usefulness of this approach.

Additional User Qualification. If your 1240 has four acquisition cards, you may use the extra clock/qualifier channel to further qualify Timebase 2. *However,* correct disassembly is not guaranteed when you do this.

WHAT YOU MAY CHANGE

Much of the setup provided by the 68000 Mnemonics ROM Pack cannot be disturbed without seriously impairing the disassembly of your data, but you can safely make the following modifications:

- You may change radices anywhere, but your choices will be ignored in some display formats.
- You may reorganize the CNTL group; the ROM Pack will retain its own internal grouping for processing purposes.
- You may change anything having to do with timebase T1; the 68000 Mnemonics ROM Pack only uses T2.
- You may change the configuration or grouping of any pod not used by the ROM Pack (as long as you do not chain the 1240D2s). The 68000 Mnemonics ROM Pack uses only the three highest-numbered 1240D2 (18-channel) acquisition cards.

NOTE

Do not chain your 18-channel cards. Doing so disrupts the setup supplied by the ROM Pack.

STORING AND USING A MODIFIED SETUP

When you have created and verified a modified setup for your 1240 that is compatible with the Mnemonics ROM Pack, you can store it and retrieve it using the following procedures:

Storing a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Remove the Mnemonics ROM Pack.
- Install a RAM Pack, press LOAD NEW PACK, and store your setup (FILETYPE: SETUP, STORED IN: PACK).

Using a Modified Setup

- Go to the Storage Memory Manager menu (UTILITY key).
- Install your RAM Pack, press LOAD NEW PACK, and load the file containing the modified setup.
- Store that setup in the 1240's internal RAM (FILETYPE: SETUP, STORED IN: RAM).
- Remove the RAM Pack, install the Mnemonics ROM Pack, and press LOAD NEW PACK.
- Retrieve your modified setup from the 1240's internal RAM and proceed.

DATA QUALIFICATION AND TRIGGERING

IDENTIFYING CYCLE TYPES

To use either the Global or Sequential Event Recognizers effectively, you need to be able to identify cycle types. Cycle types are decoded from the channels of the CNTL group according to the relationships shown in Table 6. Definitions of the individual control lines are provided in Tables 4 and 5.

Table 4
CONTROL LINE DEFINITIONS

CNTL CHAN.	NAME	DEFINITION
7	$\overline{\text{RESET}}$	buffered from the 68000 (DIP pin 18, PGA pin 20). A low indicates the occurence of a reset.
6	$\overline{\text{UDS}}$	latched version of Upper Data Strobe (pin 7). A low indicates that the high byte of the data bus is valid.
5	$\overline{\text{BGACK}}$	buffered version of Bus Grant Acknowledge (pin 12). A low indicates that control of the bus has been granted.
4	$\overline{\text{IRQ}}$	Interrupt Request, the OR'ed sum of $\overline{\text{IPL0}}$, $\overline{\text{IPL1}}$, and $\overline{\text{IPL2}}$; it goes low whenever any of them go low.
3	SUP/$\overline{\text{USER}}$	is high when the 68000 is in the Supervisor mode, low when it is in the User mode.
2	$\overline{\text{FETCH}}$	is low when any type of Fetch is occurring (either an opcode or extension word) and also when an Interrupt Acknowledge occurs; it is high during data transfers.
1	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$)	has two meanings depending on the status of $\overline{\text{FETCH}}$: While $\overline{\text{FETCH}}$ is low, a high on this line means an Opcode Fetch and a low indicates an Extension Fetch. While $\overline{\text{FETCH}}$ is high, a high on this line indicates a Read and a low means a Write.
0	ENCODED	has multiple meanings depending on the status of $\overline{\text{FETCH}}$ and OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$). Refer to Table 5.

Table 5
DECODING THE SIGNAL 'ENCODED'

	$\overline{\text{FETCH}}$ = 0		$\overline{\text{FETCH}}$ = 1	
	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$) = 0	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$) = 1	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$) = 0	OP/$\overline{\text{EXT}}$(R/$\overline{\text{W}}$) = 1
ENCODED = 0	Interrupt Acknowledge	Prior Opcode Flushed?	Valid Lower Byte Write	Valid Lower Byte Read
ENCODED = 1	Extension Word Read	Prior Opcode Not Flushed?	Not a Valid Lower Write	Not a Valid Lower Read

68000 CYCLE TYPE DEFINITIONS

Table 6 shows the cycle types marked by the 68000 ROM Pack and the control line conditions which correspond to each of them. It also contains a brief description of each cycle type.

Table 6
CYCLE TYPES LABELED BY THE 1240

CYCLE TYPE	CNTL GROUP 7654 3210	DESCRIPTION
(WRITE)	X0XX X100	Full 16-bit word write
(WRITE.L)	X1XX X100	Lower byte write
(WRITE.UP)	X0XX X101	Upper byte write
(READ)	X0XX X110	Full 16-bit word read
(READ.L)	X1XX X110	Lower byte read
(READ.UP)	X0XX X111	Upper byte read
(FETCH)	X0XX X011	Opcode fetch
(READ.EXT)	X0XX X001	Extension fetch
(INT ACK)	X0XX X000	Interrupt Acknowledge
(FETCH/FL)	X0XX X010	This cycle is an opcode fetch, and the previous fetch or extension fetch was probably flushed.
(XXXX.X) U	XXXX 0XXX	User mode
(XXXX.X) S	XXXX 1XXX	Supervisor mode
(FLUSH)	not appl.*	A fetch cycle that was probably flushed.

* You cannot trigger on this cycle type, since these labels are derived from post-acquisition processing.

TRIGGERING ON CYCLE TYPES

To specify a particular cycle type as a condition for data qualification or triggering, enter the values shown in Table 6 for that cycle type in the CNTL field of the event recognizer.

Table 7 contains some other useful control group patterns that may also be used for triggering, but are not labeled in the 1240 data display.

Table 7
OTHER USEFUL CONTROL GROUP PATTERNS

NAME	CNTL GROUP 7654 3210	DESCRIPTION
RESET	0XXX XXXX	Reset (DIP pin 18, PGA pin 20)
BGACK	XX0X XXXX	Bus Grant Acknowledge (pin 12), the bus has been relinquished to an external device.
IRQ	XXX0 XXXX	Interrupt request; the OR'ed sum of $\overline{IPL0}$, $\overline{IPL1}$, and $\overline{IPL2}$ (DIP pins 25, 24, & 23; PGA pins 27, 26, & 25)

CNTL Group Modification. You may split up the CNTL group, or rearrange its channels, or change its radix, without affecting disassembly. The ROM Pack maintains, for its internal use, a version of the group as it originally set it up. This allows you to take individual channels out of the CNTL group or create your own sub-groups with names that suggest the sub-set of channels you include or the way you are using them. (Of course, reorganization of the CNTL group means that you can no longer use the values given in Tables 6 and 7.)

The CNTL group is displayed in hexadecimal to conserve screen space.

BGACK. The default setup acquires data without regard to the status of $\overline{BGACK}$. If you want to be able to distinguish those cycles during which the bus is granted, look for a zero on channel 5 of pod 2. You may want to move this channel to a separate group for ease of viewing.

If you want to suppress data that occurs on cycles when the bus is granted, you can use data qualification and require $\overline{BGACK}$ to be high.

DISPLAYING DISASSEMBLED DATA

INSTRUCTION MNEMONICS

With the exceptions indicated in *Special Disassemblies* later in the manual, this ROM Pack disassembles in the Motorola 68000 mnemonics syntax used in the *M68000 16/32-Bit Microprocessor Programmer's Reference Manual,* Fourth Edition, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632.

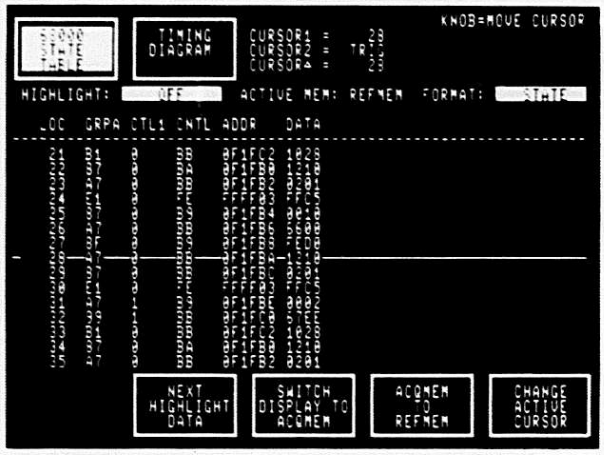
DISPLAY FORMATS

The mnemonics and cycle type information generated by the 68000 Mnemonics ROM Pack is available in the State Table display (accessed by pressing the DATA key). You have three choices of disassembly formats in addition to the standard state table display. You select the display format by placing the blinking field cursor in the FORMAT field and using the SELECT keys to indicate your choice.

NOTE

If you attempt to use the 68000 Mnemonics ROM Pack in a 1240 that does not have at least three 1240D2 cards, you will get an INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY message in the State Table menu and only the (standard) STATE display format will be available.

STATE. This is the standard 1240 State Table format that you get without the 68000 Mnemonics ROM Pack installed. This format is also the only one available in AUTO-RUN or when you have less than three 1240D2 cards installed (FORMAT field is not present). Look at Figure 4.



4846-04

Figure 4. STATE format is standard without the ROM Pack.

ABSOLUTE. This format is like the STATE format, but is enhanced by the addition of cycle type information. A FLUSH indicates cycles which were probably flushed (and a FETCH/FL indicates that the previous FETCH cycle was probably flushed). The Absolute format also adds an S/U character after the cycle type to note 68000 Supervisor or User mode. Look at Figure 5.

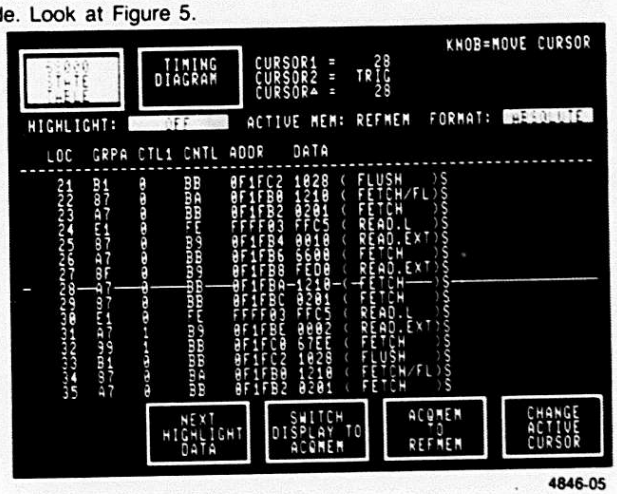


Figure 5. ABSOLUTE format adds cycle type information.

HARDWARE. In this format, instruction mnemonics are displayed in the DATA group on FETCH cycles, and cycle type information is provided on all other cycles. The mnemonics for cycles which may have been flushed are preceded by a question mark. Look at Figure 6.

NOTE

User choices of display radix are overridden in the HARDWARE display format. The ADDR and DATA groups are always displayed in the default radix of HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.

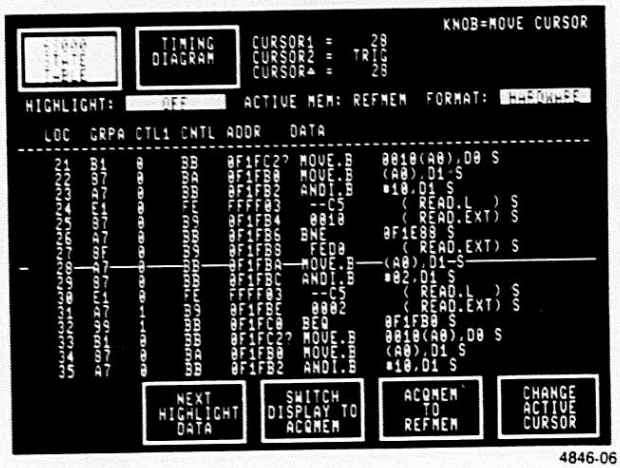


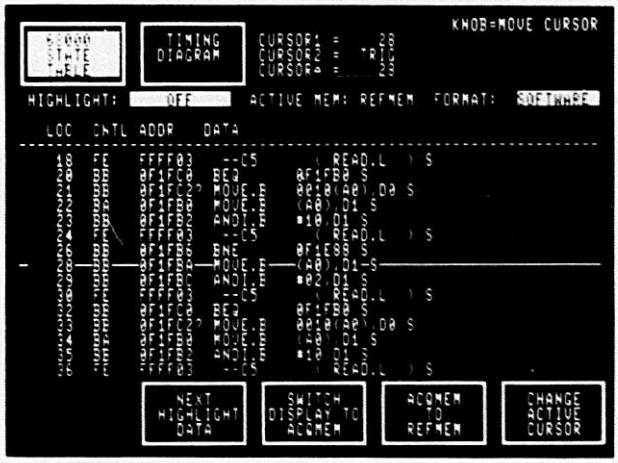
Figure 6. HARDWARE format shows instruction mnemonics.

SOFTWARE. This display format is designed to look like a source code listing and thus simplify analysis of the program flow. It is similar to HARDWARE except that READ.EXT cycles are not shown and all non-microprocessor data is suppressed (i.e. T1 data and T2 data from other groups, if there are any, is suppressed). Look at Figure 7.

The suppression of cycles resulting from the transition from any other format to SOFTWARE may cause the data cursors to move.

NOTE

User choices of display radix are overridden in the SOFTWARE display format. The ADDR and DATA groups are always displayed in the default radix of HEX. To see the data in these groups in your choice of radix, use the FORMAT select field to switch back and forth between this format and ABSOLUTE or STATE.



4846-07

Figure 7. SOFTWARE format suppresses READ.EXT cycles.

INTERLEAVING OF CODE AND DATA

Because the 68010 prefetches code into its pipeline, data transfers frequently will not be associated with the instruction immediately preceding them, but rather with a previous instruction. For example, in Figure 7 the data transfer at LOC 30 was caused by the execution of the instruction at LOC 28 rather than the one at 29.

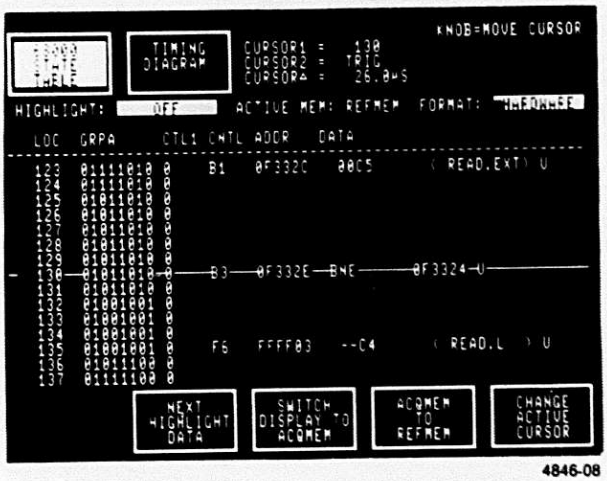
TIMING DISPLAYS

In the Timing Diagram menu, the active cursor value readout at the bottom of the data display reflects your choice of disassembly FORMAT in the State Table menu, with one exception: When you select SOFTWARE in the State Table menu, the readout in the Timing Diagram will be in HARDWARE format.

DUAL TIMEBASE DISPLAYS

If your 1240 has four data acquisition cards, you may use T1 with the first one.

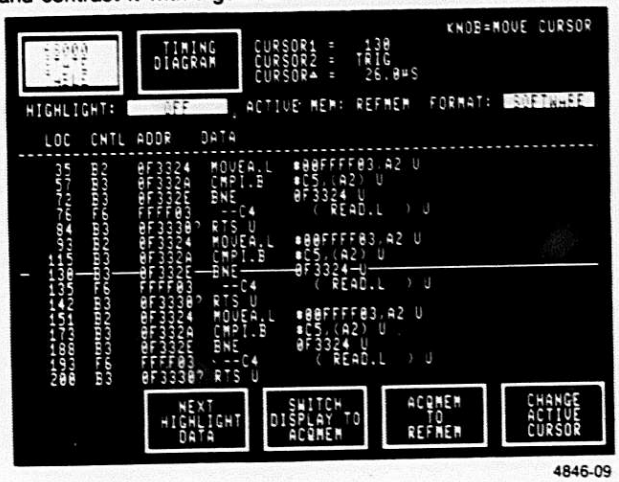
In the STATE, ABSOLUTE, and HARDWARE formats, the data acquired on T1 is correlated with the T2 data acquired from the 68000. However, due to delays inherent in the PM203 circuitry, this apparent correlation may be off by one, especially at higher speeds. Look at Figure 8 to see T1 data correlated with 68000 data.



4846-08

Figure 8. T1 data correlated with 68000 data.

When you select SOFTWARE as the data display format, T1 data is suppressed in the interest of giving you the best possible overview of the 68000 program flow. Refer to Figure 9 and contrast it with Figure 8.



4846-09

Figure 9. T1 data is suppressed in SOFTWARE format.

SPECIAL DISASSEMBLIES

The 68000 Mnemonics ROM Pack allows you to observe some of the more advanced capabilities of the 68000, but limitations imposed by the PM203 lead to some variations from standard Motorola disassembly. These special disassemblies are described in the following paragraphs and in Table 8 and Figure 10.

S and U suffixes indicate whether the 68000 is in the Supervisor or User mode.

.B, .W, and .L suffixes indicate byte, word, and long-word, respectively. No suffix is shown if the operation can only be performed on data of a particular length.

MOVEM registers are shown as D0-7, A0-7, or a subset of these. NO REG indicates that no registers were specified.

TAS, Test And Set, instructions will have both the read and write labeled as READ cycles. The second instruction labeled a READ is actually a WRITE; the data is correct, but the cycle type label will always be wrong.

FLUSH, FETCH/FL, and ? all refer to instruction fetches that were apparently flushed. In the Absolute format, FETCH/FL indicates that the preceding instruction was probably flushed, while FLUSH is used to mark the actual instruction that was probably flushed. In the Hardware and Software disassembly formats, **?** indicates the disassembled instruction was probably not executed.

The operands of instructions that are flushed may appear to be valid, when in fact they are not. (If READ.EXT cycles were associated with the flushed instruction but never appeared in the pipeline, the ROM Pack treats the next READ.EXT cycles that it finds as belonging to the flushed instruction, even though in fact they were supposed to be associated with some other instruction.)

The marking of flushes is imperfect; some flushes are not detected, some flush indications do not indicate a real flush. The PM203 monitors the consecutiveness of fetch addresses and informs the ROM Pack if they are not sequential. Consider flush indications as useful, but not infallible.

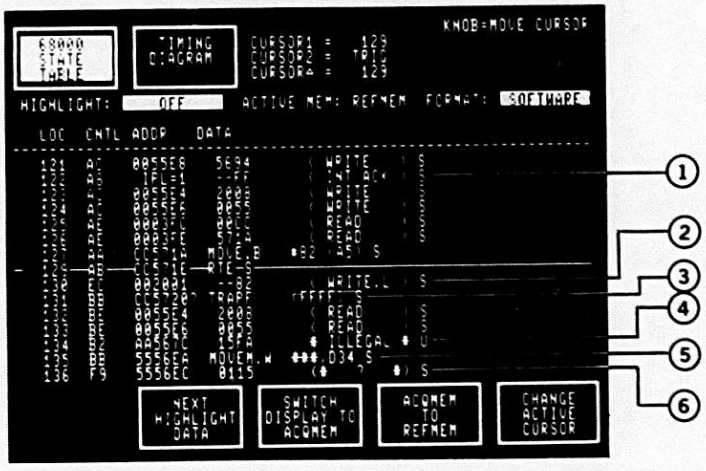
Address Displacement Integers. Some 68000 addressing modes use an 8- or 16-bit signed displacement integer. In the disassembly display, displacements are shown as unsigned 8- or 16-bit hexadecimal numbers, exactly as they are stored in the extension word. The only exception to this display convention is the program counter (PC), in which case, disassembly will show the signed, extended integer value.

Operand format differences between the standard Motorola format and the format used by Tektronix are shown in Table 8.

Table 8
OPERAND FORMAT DIFFERENCES

MODE	REGISTER	MOTOROLA	TEKTRONIX
111	010	d(PC)	addr-32-bit
111	011	d(PC,Xi)	offset(Xi)

Special disassemblies. When the 68000 Mnemonics ROM Pack encounters an unexpected combination of data, or when part of the data is missing, or other events occur, one of the indications shown in Figure 10 appears in the display.



1 ***Interrupt acknowledge*** cycles are shown with an IPL=X message replacing the address. X is the priority level decoded from address lines A1, A2, and A3.

2 ***Invalid data*** is replaced with dashes. In this example, the high byte is invalid and is replaced by dashes, while the lower data value is shown.

3 ***Unimplemented instructions*** are shown as TRAPA or TRAPF. These indicate that the 68000 has attempted to execute an opcode whose first hexadecimal digit is an **A** or an **F**, i.e., AXXX or FXXX. The standard 68000 exception processing will occur. Other unimplemented instructions are shown as (* ILLEGAL *).

4 ***Illegal opcode*** indications appear on opcode fetch cycles where the opcode is meaningless. This indication can result from a problem in your software causing an attempted execution at an erroneous address.

5 ***Missing Operand:*** signals that part of a multi-word instruction was not stored in the acquisition memory. This can arise at the end of memory or when some sort of data qualification has prevented the complete storage of an instruction. A single asterisk is displayed for each missing hexadecimal digit or register name.

6 ***Illegal cycle type:*** arises from an unexpected combination of control channel values. This indication can occur in every display format except STATE. It can be caused by a misconnected or defective PM203, a setup that has been modified and is no longer correct, or a problem with your system under test.

4846-10

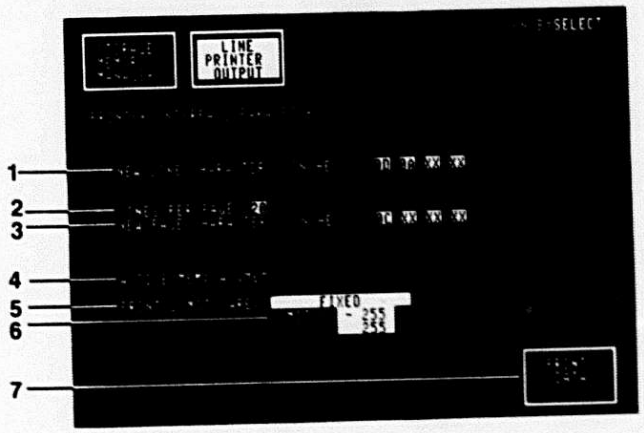
Figure 10. Special disassemblies.

EDITING THE REFERENCE MEMORY

If you edit a portion of your reference memory, you should also edit a reserved channel associated with that portion of memory to avoid disassembly anomalies. Two channels are reserved by the ROM Pack for post-acquisition processing of data, but only one is actually used. Channel 8 of pod 0 (pod 4 if four acquisition cards are present) is set to 1 for cycles which were identified by the PM203 as probably flushed.

LINE PRINTER OUTPUT

When the 68000 Mnemonics ROM Pack is installed in a 1240 that also has a 1200C01 RS232C or 1200C11 Parallel Printer COMM Pack installed, the UTILITY menu presents a soft key labeled LINE PRINTER OUTPUT replacing the COMM PORT CONTROL key. The menu accessed by this key allows you to send your state data displays to a line printer in the current format. Refer to Figures 11 and 12.



1 NEW LINE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will be appended to each line. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

2 LINES PER PAGE: Use this decimal field to specify the number of lines that will be printed on each page. Valid values range from 1 to 99.

3 NEW PAGE CHARACTERS: Use these hexadecimal fields to define a string of from one to four characters that will follow the end of every page. The first field must have an entry, but the last three fields can be filled with **X**s (don't cares).

4 ACTIVE MEM: This field is for information only. Change the active memory in the State Table or Timing Diagram menus.

5 PRINT LIMITS ARE: Use this field to indicate whether the area of active memory to be printed will be defined by FIXED LIMITS or BETWEEN CURSORS. When BETWEEN CURSORS is selected, the area of the active memory that will be printed is defined by the data cursors (inclusive).

6 LIMITS: This field becomes active when FIXED LIMITS is selected in the PRINT LIMITS ARE field. Entries here specify the first and last line of memory to be printed. When PRINT LIMITS ARE: BETWEEN CURSORS, this field displays the locations of the cursors.

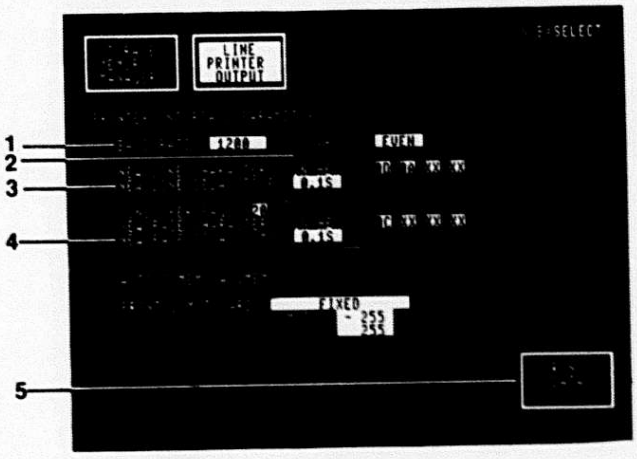
7 PRINT DATA: Touch this soft key to start the transmission of data. It will remain lighted during the transfer. Use the STOP key to interrupt the transmission, if necessary.

4846-11

Figure 11. LINE PRINTER OUTPUT menu when 1200C11 is installed.

NOTE

Do not attempt to control the 1240 remotely using an RS232C COMM Pack while any Mnemonics ROM Pack is installed.



1 BAUD RATE: Use this field to specify the baud rate at which the 1240 will supply data to the printer. The available choices are: 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600.

2 PARITY: Use this field to make parity choices of ODD, EVEN, and NONE. If your printer uses the 8th (parity) bit for something other than parity, set this field to NONE.

3 NEW LINE DELAY TIME: Use this field to specify the minimum time delay between the transmission of successive lines by the 1240. The choices range from NONE to 9.9 SEC in 100 ms steps.

4 NEW PAGE DELAY TIME: Use this field to specify the minimum amount of time delay between the transmission of the last line of one page and the first line of the next page. The choices range from NONE to 9.9 SEC in 100 ms steps.

5 PRINT DATA: Touch this soft key to start the transmission of data. Use the STOP key to interrupt the transmission, if necessary. This key places the 1240 ONLINE when the 1200C01 RS232C COMM Pack is installed. If the device being transmitted to is capable of transmitting back, spurious remote commands can affect the operation of the 1240. Also, during a PRINT DATA operation, the 1200C01 parameters are modified. Therefore, do not attempt to control the 1240 remotely while any Mnemonics ROM Pack is installed.

4846-12

Figure 12. LINE PRINTER OUTPUT menu when 1200C01 is installed. Refer to Figure 11 for a description of those fields that are the same in both menus. Refer to the *RS232C COMM Pack 1200C01 Operator's Manual* for information on handshaking protocols and the use of null modems.

ERROR MESSAGES

When used with a 68000 Mnemonics ROM Pack, the 1240 Logic Analyzer uses some error messages that are different from those it normally displays. Also, some of the normal error messages have additional meanings when they are used with this ROM Pack.

APPLYING SEARCH PATTERN - PLEASE WAIT — This message occurs briefly twice during a data acquisition with the 68000 Mnemonics ROM Pack installed, unless PATTERN SEARCH DISABLED is selected.

CONFIG ERROR — This message always appears in the State Table display after power-up with a 68000 Mnemonics ROM Pack installed. It indicates that the setup used to acquire the current acquisition memory and the current setup from the 68000 Mnemonics ROM Pack are inconsistent. Acquiring new data should make this message go away. (Refer to the *Reference Information* section of the *1240 Logic Analyzer Operator's Manual* for a complete discussion of this message.) This message also appears in the LINE PRINTER OUTPUT menu if the current configuration does not permit a PRINT DATA operation to be performed.

INSUFFICIENT 1240D2 CARDS TO SUPPORT DISASSEMBLY — This message indicates that your instrument does not have enough 18-channel cards to support the use of this Mnemonics ROM Pack.

MEMORY TIMEBASE ASSIGNMENTS WILL NOT SUPPORT DISASSEMBLY — The memory being displayed cannot be disassembled because it was acquired with a setup that does not support disassembly. Go to the Storage Memory Manager menu and press LOAD NEW PACK to get a setup that will support disassembly. Then, acquire new data using that setup.

NO VALID DATA ACQUIRED — This message indicates that either no T2 data was acquired or that the acquired data was so heavily qualified that what was left of it disappeared during (SOFTWARE) disassembly.

PRESS "STOP" TO TERMINATE OPERATION — This message indicates the correct way to stop a PRINT DATA operation. Since letting the printing operation finish or stopping it are your only choices once a printout is in progress, the 1240 assumes that you want to stop printing if you touch any key.

PM203 SPECIFICATIONS

Table 9 contains the environmental specifications for the PM203. Note that the environmental specifications for the PM203 are more restrictive than those for the 1240 Logic Analyzer itself.

The specifications shown in Table 10 refer to a 1240 Logic Analyzer system that includes a PM203 Personality Module.

Table 9
PM203 ENVIRONMENTAL SPECS

Characteristic	Description
Temperature	
Operating	0°C to 50°C
Storage	−55°C to 75°C
Humidity	0% to 95%
Altitude (max.)	
Operating	15,000 feet
Storage	50,000 feet

Table 10
PM203 – 1240 SYSTEM SPECS

Characteristic	Performance Requirement	Supplemental Information
Clock (DS) Freq.	12.5 MHz max.	
Input Capacitance		30 pF nominal
Threshold Voltage		1.3 V to 1.5 V
Max. Non-Destructive Input Voltage		−2 V to +7 V
Setup Time	10 ns min.	Measured from falling edge of S6
Hold Time	35 ns min.	Measured from falling edge of S6

REPLACEABLE PARTS LIST
68000 MNEMONICS ROM PACK — 12RM25

NUMBER	TEK. P/N	DESCRIPTION
ELECTRICAL	(REFER TO SCHEMATIC IN 1240 SERVICE MANUAL)	
A43	670-8172-00	CRT. BOARD ASSY: 32/64K MEMORY ROM PACK (U200, U300 EPROMs ARE NOT PART OF A43)
A43C100	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
A43C400	281-0775-00	CAP, FIXED, CER, DI: 0.1 uF, 20%, 50V
		CHASSIS PARTS
U200	160-2480-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
U300	160-2479-00	MICROCKT, DGTL: 16384 x 8 EPROM, PRGM
MECHANICAL	(REFER TO EXPLODED VIEW DRAWING)	
1	334-0164-00	1 MARKER, IDENT: MKD 68000 ROM PACK
2	200-2503-01	1 COVER, ROM PACK: TOP
		(ATTACHING PARTS)
3	211-0012-00	4 SCREW, MACHINE: 4.40 x 0.375, PHD, STL
		— — * — —
4	- - - - -	CKT BOARD ASSY: 32/64K MEMORY ROM PACK (SEE A43 REPL)
5	131-0993-00	2 • BUS CONDUCTOR: 2 WIRE, BLACK
6	131-0608-00	6 • TERMINAL, PIN: 0.365 L x 0.025 PH BRZ GOLD
7	136-0755-00	2 • SKT, PL-IN ELEC: MICROCIRCUIT, 28 DIP
8	337-3122-00	1 SHIELD, ELEC: STATIC
9	200-2504-01	1 COVER, ROM PACK: BOTTOM
10	334-4727-00	1 MARKER, IDENT: MKD PROM PROGRAM IDENT
		STANDARD ACCESSORIES
	070-4846-00	MANUAL, TECH: INSTRUCTION