7000-SERIES PLUG-IN/MAINFRAME INTERFACE MANUAL

(An Engineering Guideline)

COMPANY CONFIDENTIAL

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SPECIFICATION 704
March 1976

TOP

7000 SERIES PLUG-IN CONNECTOR

A38	CH 2	COLUMN ANALOG DATA	ROW ANALOG DATA	CH 2	B38
A37	CH 1			CH 1	B37
A35	FORCE READOUT			PLUG-IN MODE	B35
A33	2	TIMESLOT PULSE LINES GPIB*	TIMESLOT PULSE LINES GPIB*	1	B33
A32	4			3	B32
A31	6			5	B31
A30	8			7	B30
A29	10			9	B29
A27	–5 V POWER	GPIB*	GPIB*	+5.1 V POWER	B27
A26	LOGIC COMMON			$\overline{\text{SND}}$	B26
A25	$\overline{\text{NDAC}}$			$\overline{\text{NRFD}}$	B25
A24	$\overline{\text{IFC}}$			$\overline{\text{ATN}}$	B24
A23	$\overline{\text{DAV}}$			REN	B23
A22	$\overline{\text{EOI}}$			$\overline{\text{SRQ}}$	B22
A21					B21
A20	+ TRIGGER IN (H)			– TRIGGER IN (H)	B20
A19	+50 V POWER			–50 V POWER	B19
A18	+ 15 V POWER			–15 V POWER	B18
A17	AUX Z AXIS			AUX Z AXIS COM	B17
A16	MAIN FRAME MODE INFO			AUX Y AXIS	B16
A15	SINGLE-SWEEP LOGIC (H)			SINGLE-SWEEP RESET	B15
A14	LIGHTS COMMON			DUAL BEAM AUX Y AXIS	B14
A13	+ TRIGGER OUT (V)			– TRIGGER OUT (V)	B13
A12	GND			GND	B12
A11	SIGNAL (+)			SIGNAL (–)	B11
A10	SINGLE-SWEEP READY INDICATOR			X-Y COMPENSATION (H)	B10
A9	+ 5 V LIGHTS			DELAY GATE (H)	B9
A8	+5 V POWER			SWEEP LOCKOUT (H)	B8
A7	INTENSITY LIMIT			MAIN FRAME CHANNEL SWITCH SIGNAL	B7
A6	CHOP COMMON			ALTERNATE DRIVE	B6
A5	CHOP DRIVE			AUX SWEEP GATE (H)	B5
A4	LINE TRIGGER			HOLD OFF (H)	B4
A3	A SWEEP			B SWEEP	B3
A2	UTILITY COMMON			DELAY MODE CONTROL OUT (H)	B2
A1	SWEEP GATE			DELAY MODE CONTROL IN (H)	B1

*GPIB—(General Purpose Interface Bus) Refer to Readout and Programming sections for use.

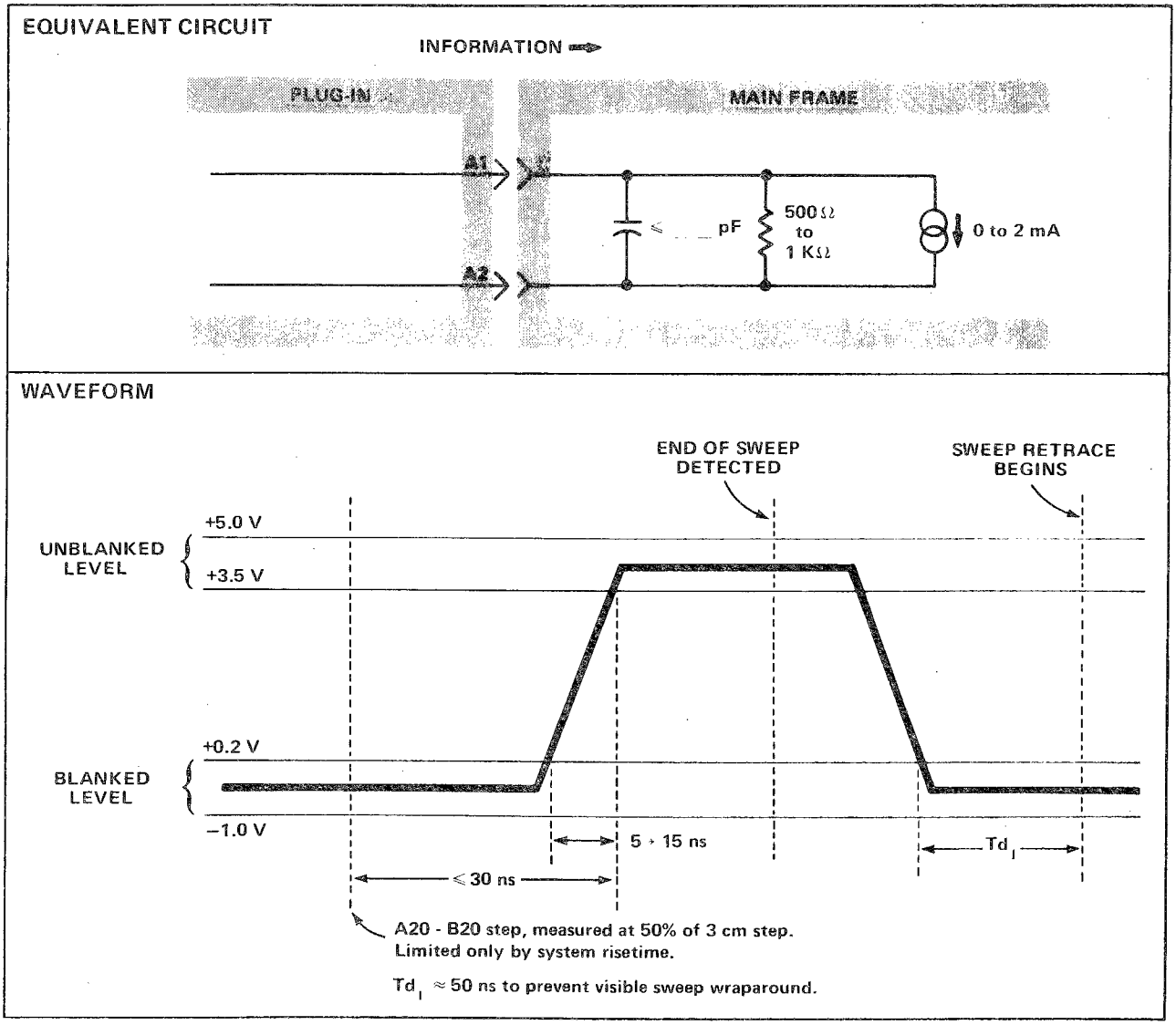
A1

SWEEP GATE

Sweep Gate, A1, is generated by the plug-in and used by the Main Frame to generate crt unblanking signals. The gate signal is required in all horizontal plug-in compartments.

Special Considerations:

1. When the time-base plug-in Lockout (B8) is in the HI state, A1 should be in the LO state.
2. Plug-ins that do not generate a gate should connect A1 to A8 (+5 V) to unblank the crt when the plug in is used in the horizontal compartments.



DELAY MODE CONTROL IN

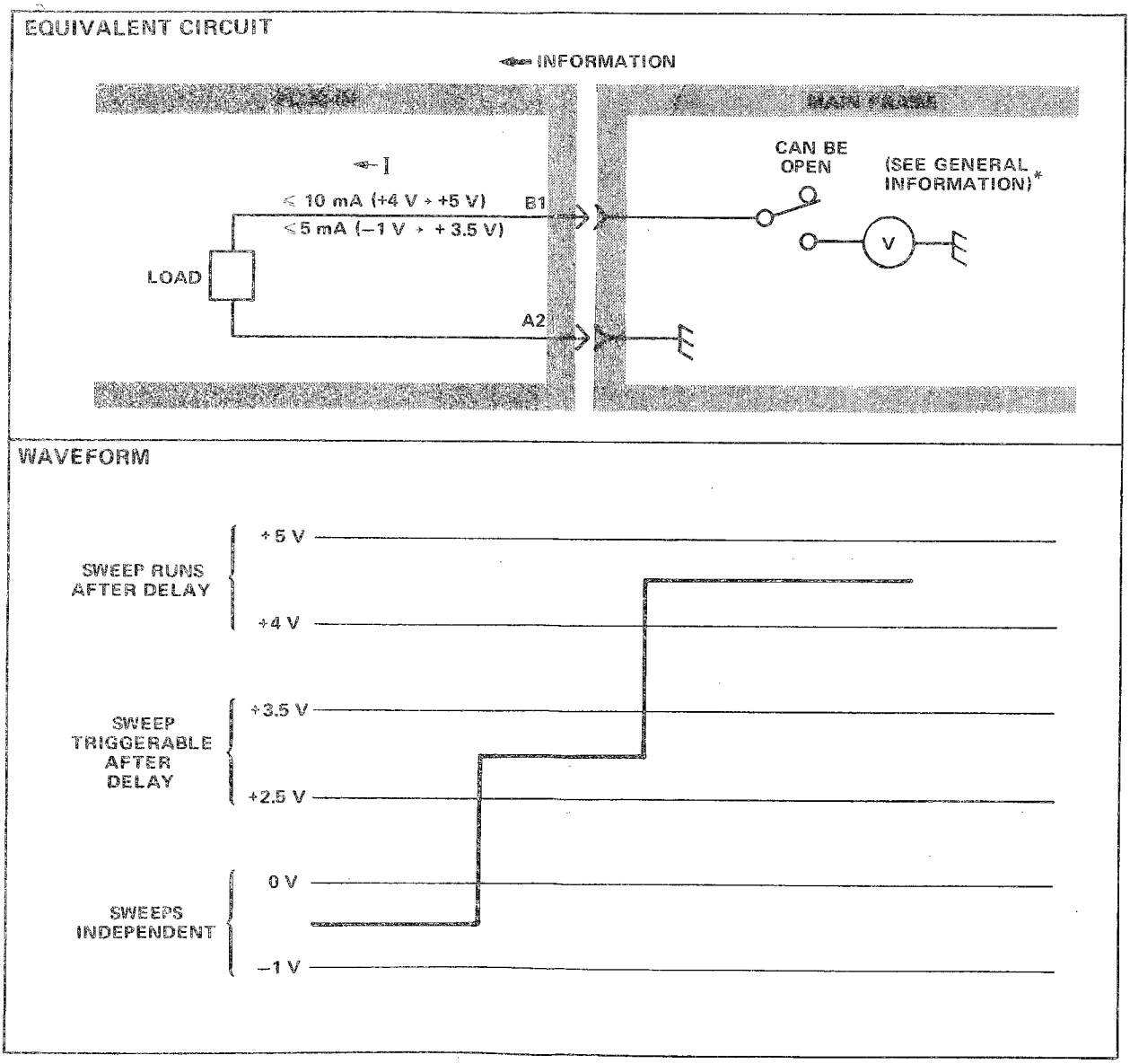
Delay Mode Control In, B1, is used by the delayed sweep plug-in with the Delay Gate, B9, to produce delayed sweep operation. B1, Delay Mode Control In, is used only in four-hole Main Frames. In three-hole Main Frames, this line is open.

* Typically, information goes into Main Frame A Horizontal, B2, through the Main Frame and out on B Horizontal, B1, to another plug-in.

For additional details on main frame switching, refer to section on Logic.

NOTE: *A 7A22 unit short circuits B1 (B2) to ground.* * *Instrument damage will occur under the following conditions: 7A22 installed in the B horizontal compartment; a 7B71, 7B51, or 7B85 installed in the A horizontal compartment and set for the "runs after delay time" mode.*

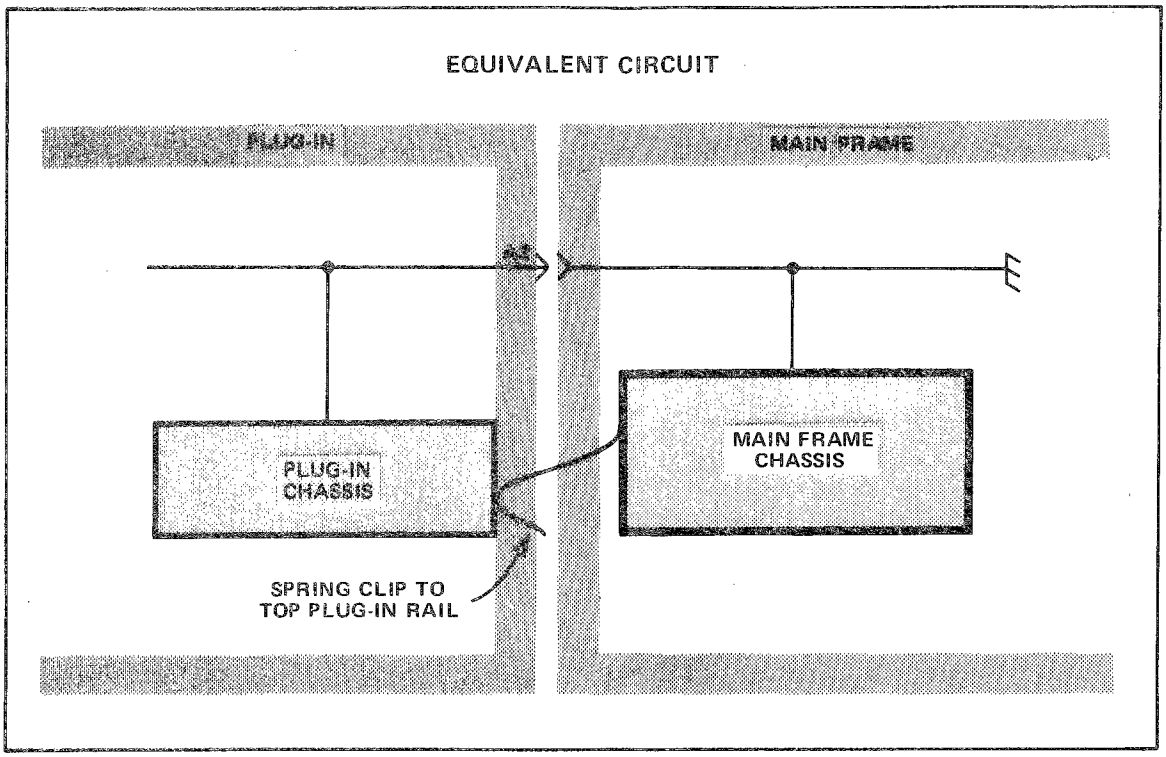
* MOD M30219 cuts B1 on 7A22 P 067-0587-01



A2

UTILITY COMMON

Utility Common, A2, was originally intended to be used exclusively as a ground return for the following pins: (A1) Sweep Gate; (B9) Delay Gate; (B8) Sweep Lockout; (B5) Auxiliary Sweep Gate; and (B4) Holdoff. It was not intended to be connected to the plug-in chassis. However, this was found to be unworkable and optimum performance was obtained when A2 was connected to the plug-in chassis ground.

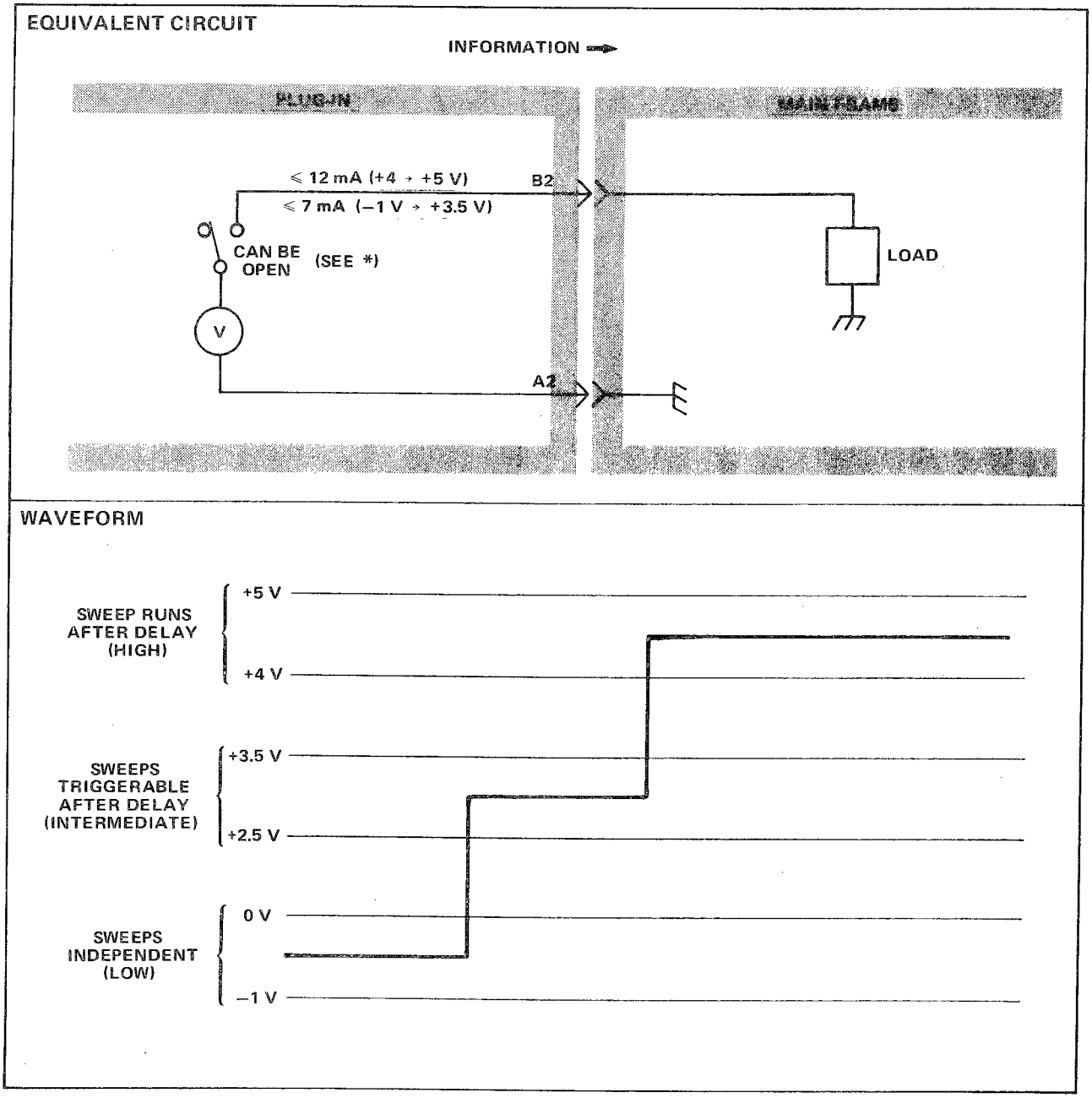


DELAY MODE CONTROL OUT

Delay Mode Control Out, B2, is generated by the delaying sweep plug-in. This information is used by the Main Frame and the delayed sweep plug-in when the delaying sweep plug-in is in the A Horizontal compartment. This signal is connected to B1 in the B Horizontal compartment.

Delay Mode Control Out, B2, is used only in four-hole Main Frames. In three-hole Main Frames, this pin is open.

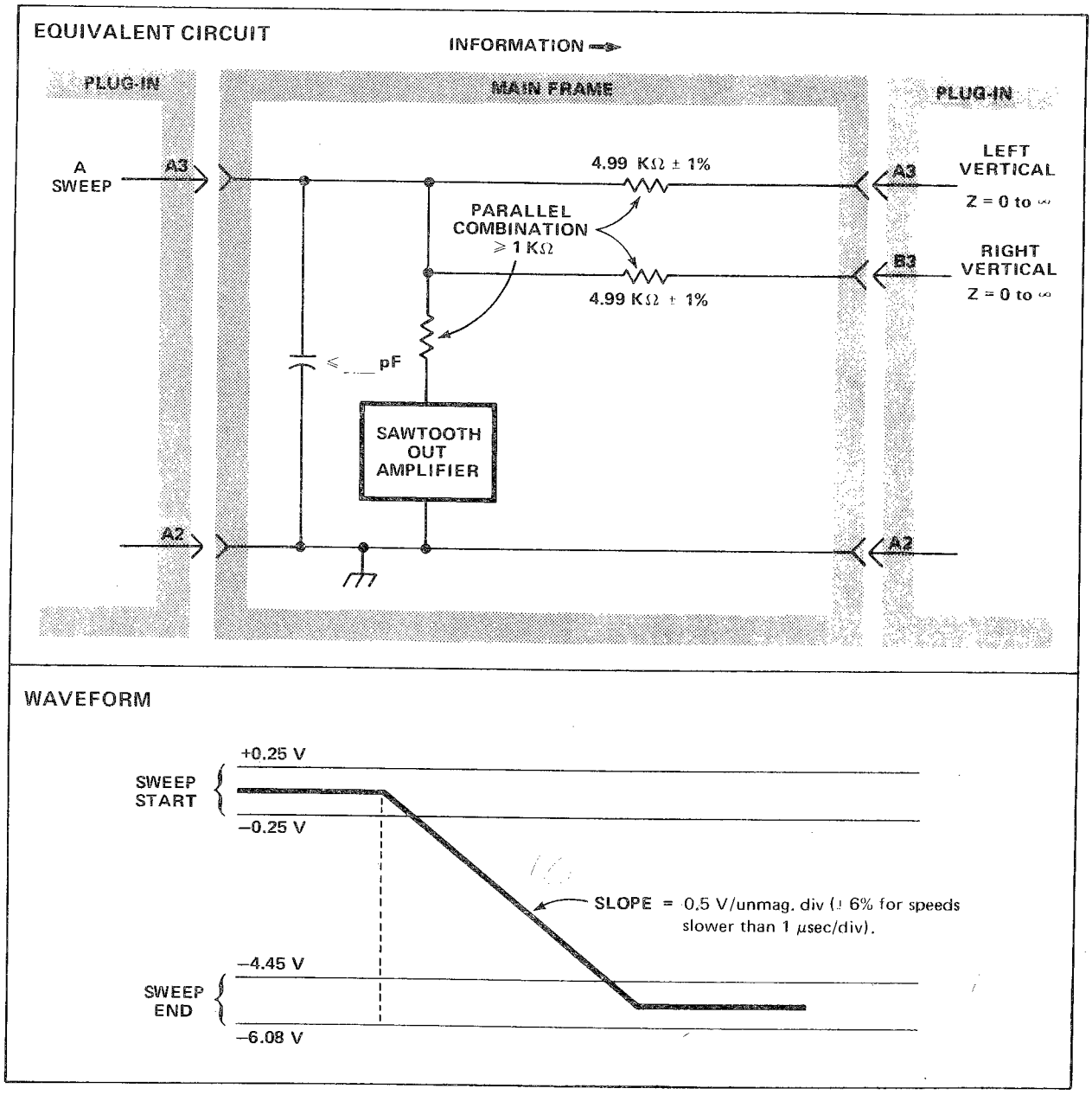
*Typically, information goes into the Main Frame A Horizontal, B2, through the Main Frame and out on B Horizontal, B1, to another plug-in.



A3

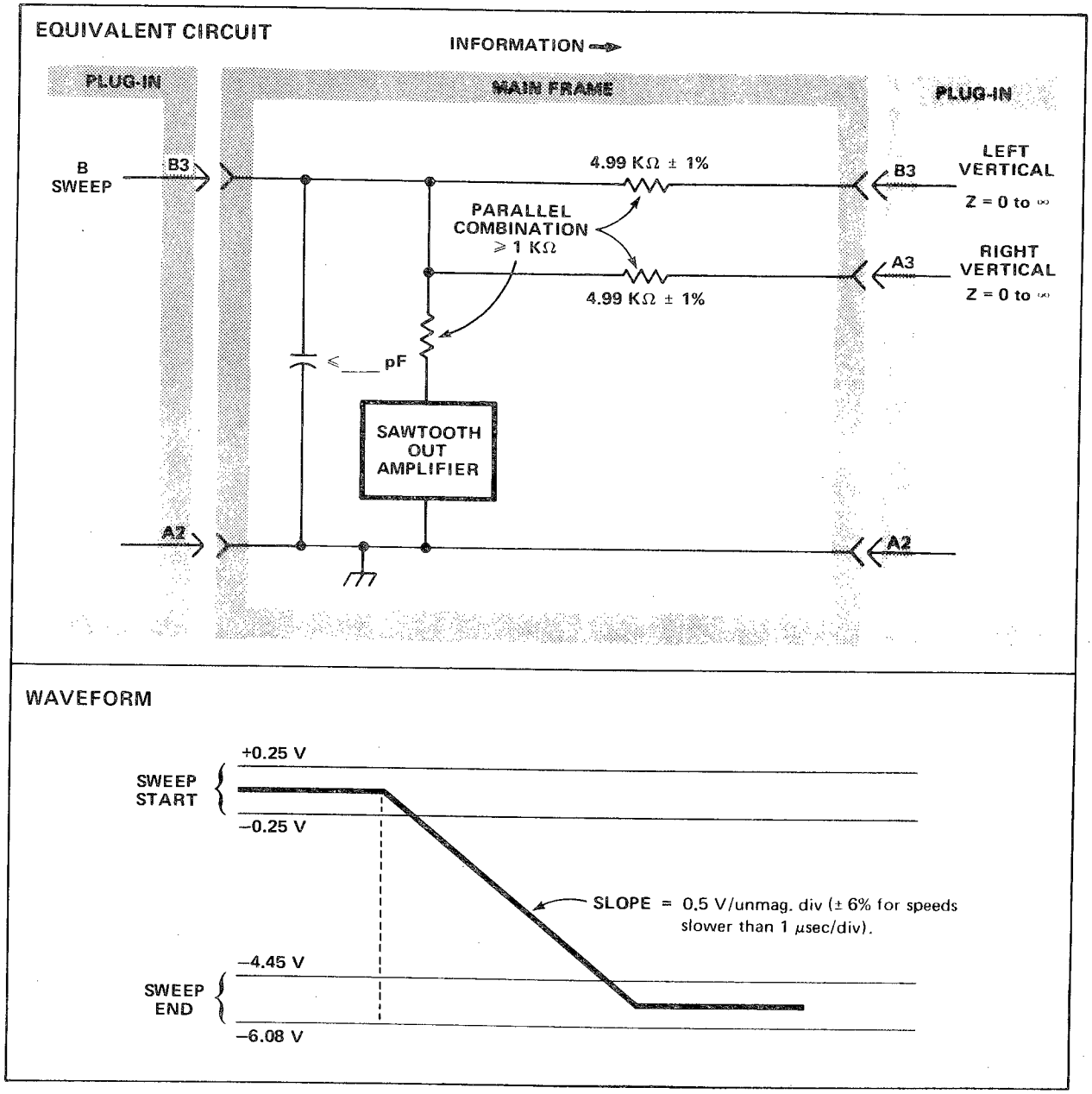
A SWEEP

A Sweep, A3, from "A" time-base plug-in supplies a negative-going sawtooth to the right and left vertical plug-in compartments and the Sawtooth Out amplifier.



B SWEEP

B Sweep, B3, is from time-base plug-ins. It supplies a negative-going sawtooth to the right and left vertical plug-in compartments and also to the sawtooth-out amplifier.



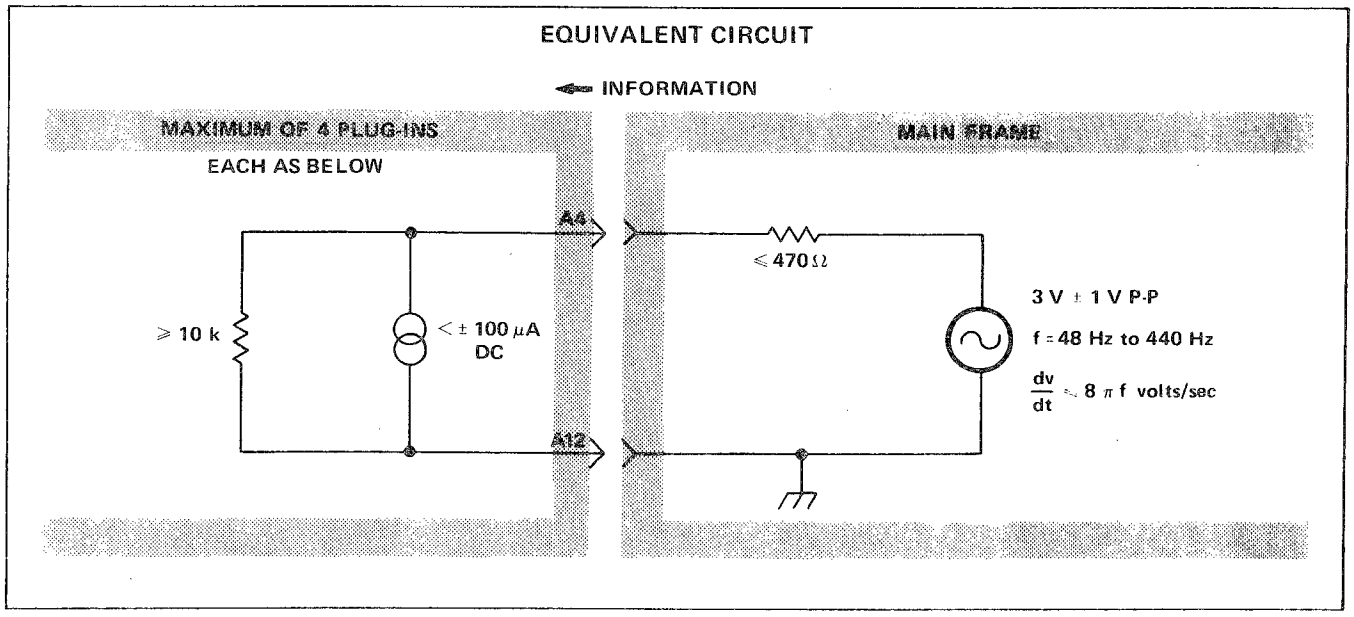
A4

LINE TRIGGER

Line Trigger A4 supplies a line trigger signal to the plug-ins.

Main Frame Considerations:

Phasing	A4 will be positive going when "hot" line conductor is positive going.
Maximum Noise	25 mV RMS (tangentially measured) 20 Hz to 1 KHz.
Power Line Isolation	2 kV RMS @ 60 Hz for 1 minute.

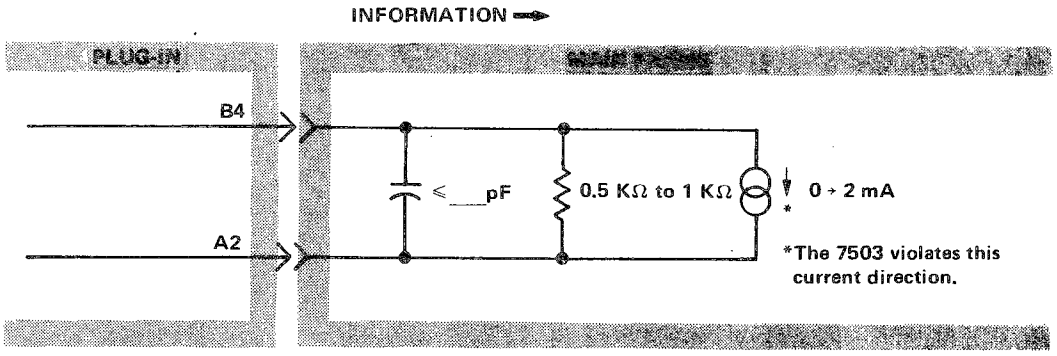


HOLDOFF

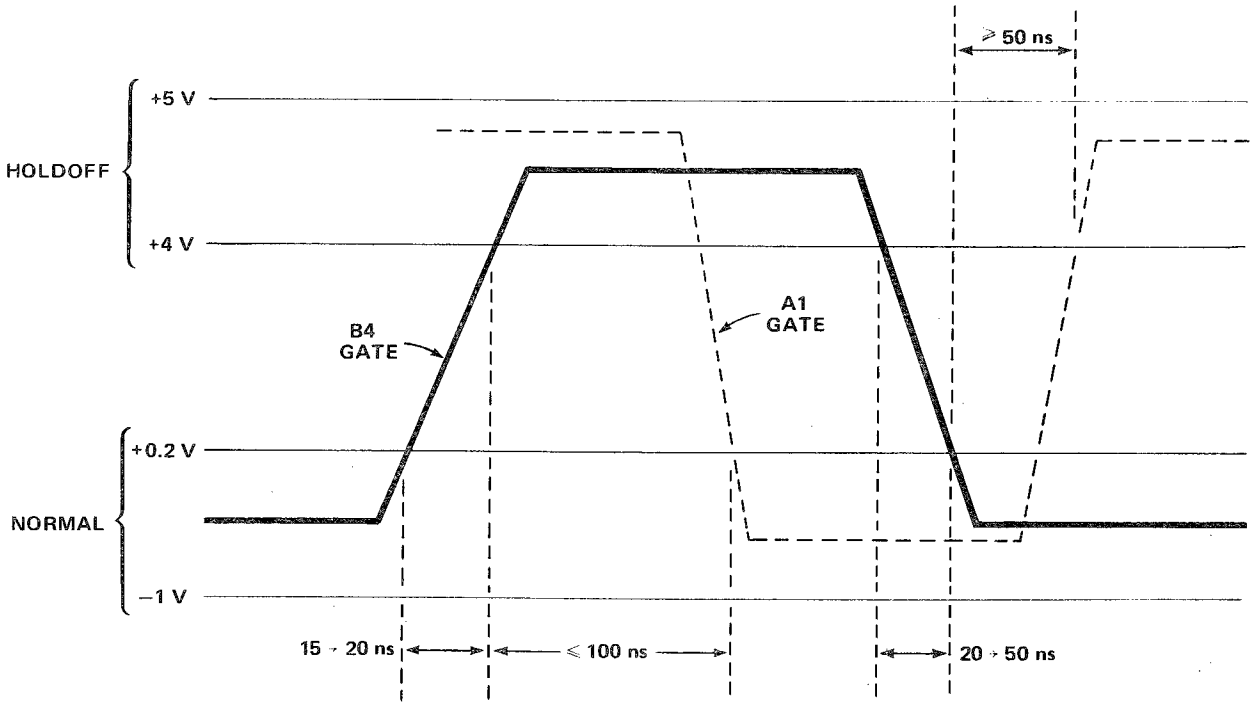
Holdoff, B4, is generated by the time-base plug-in and used by the Main Frame to derive switching information. Holdoff time is a function of the plug-in Time/Div setting.

For additional details on Main Frame Channel Switching signals, refer to Section on Logic.

EQUIVALENT CIRCUIT



WAVEFORM



A5

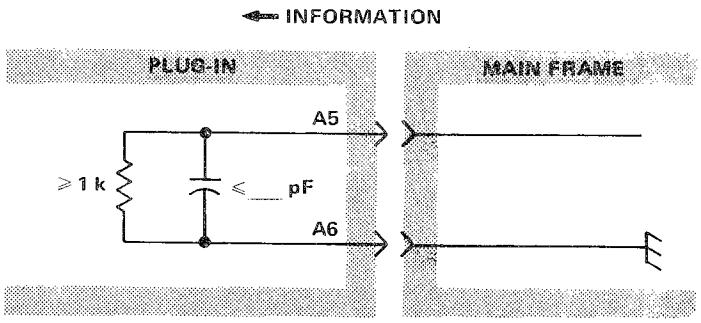
CHOP DRIVE

Chop Drive, A5, is generated by the Main Frame and used by dual-channel plug-ins to switch between Channel 1 and Channel 2 when the plug-in is in the Chop mode. The Chop Drive signal is always present.

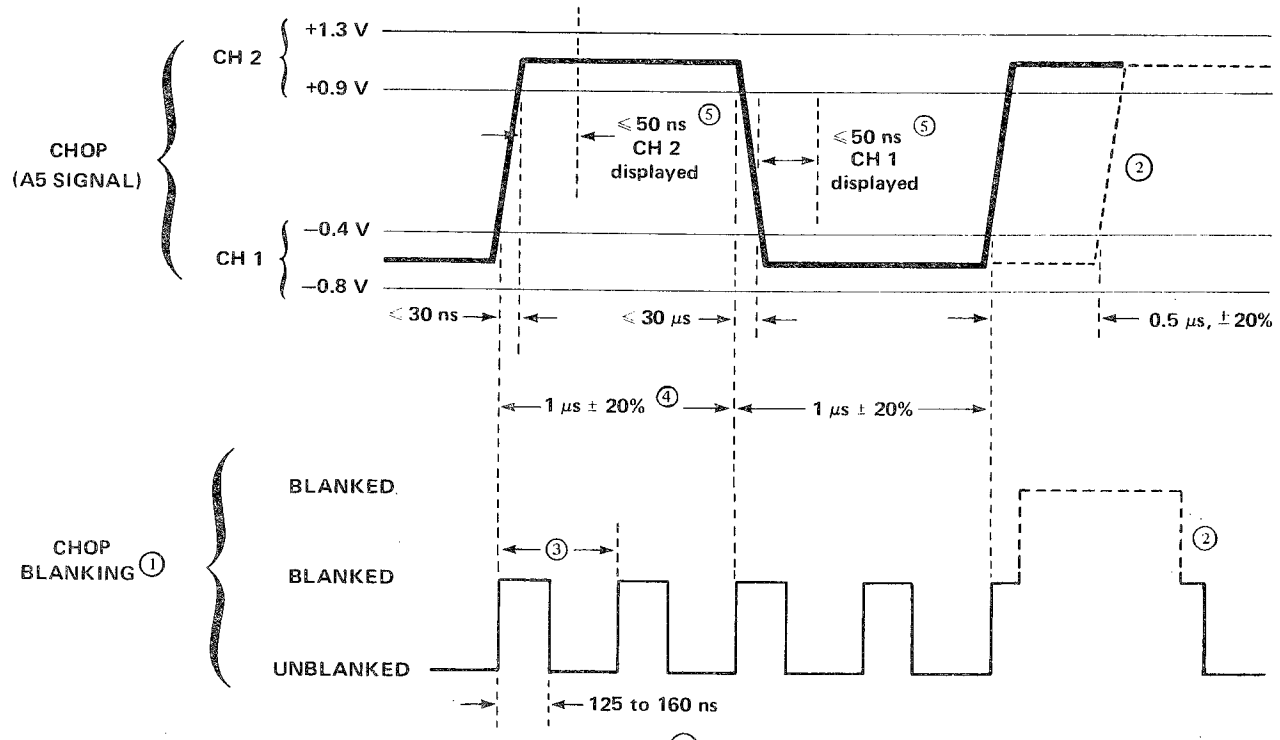
General Information:

For additional details on Main Frame Switching, refer to section on Logic.

EQUIVALENT CIRCUIT



WAVEFORMS



① Internal Main Frame Signal. Polarity and amplitude shown are for illustration only.

② Dotted waveform when Main Frame is in Horizontal Chop.

③ Left or right plug-in compartment display time.

④ 7704A has a selectable 10 μs time.

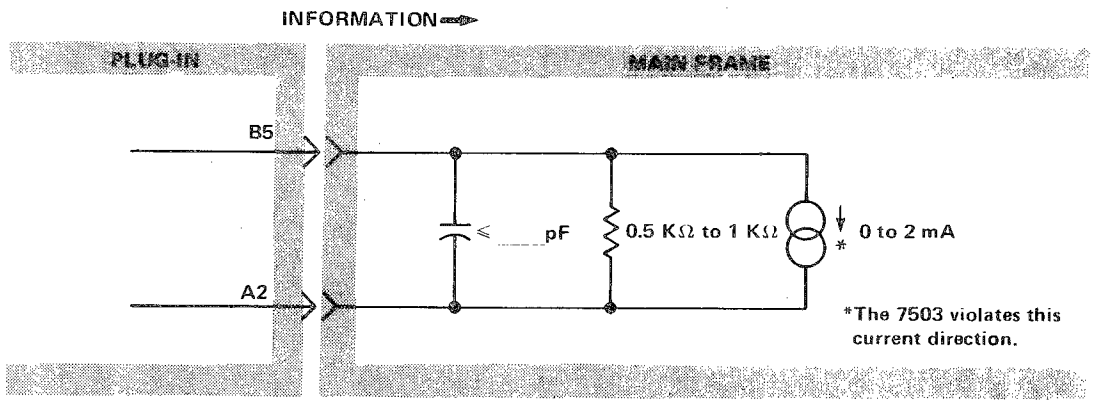
⑤ Some existing vertical plug-ins may not meet this specification.

AUXILIARY SWEEP GATE

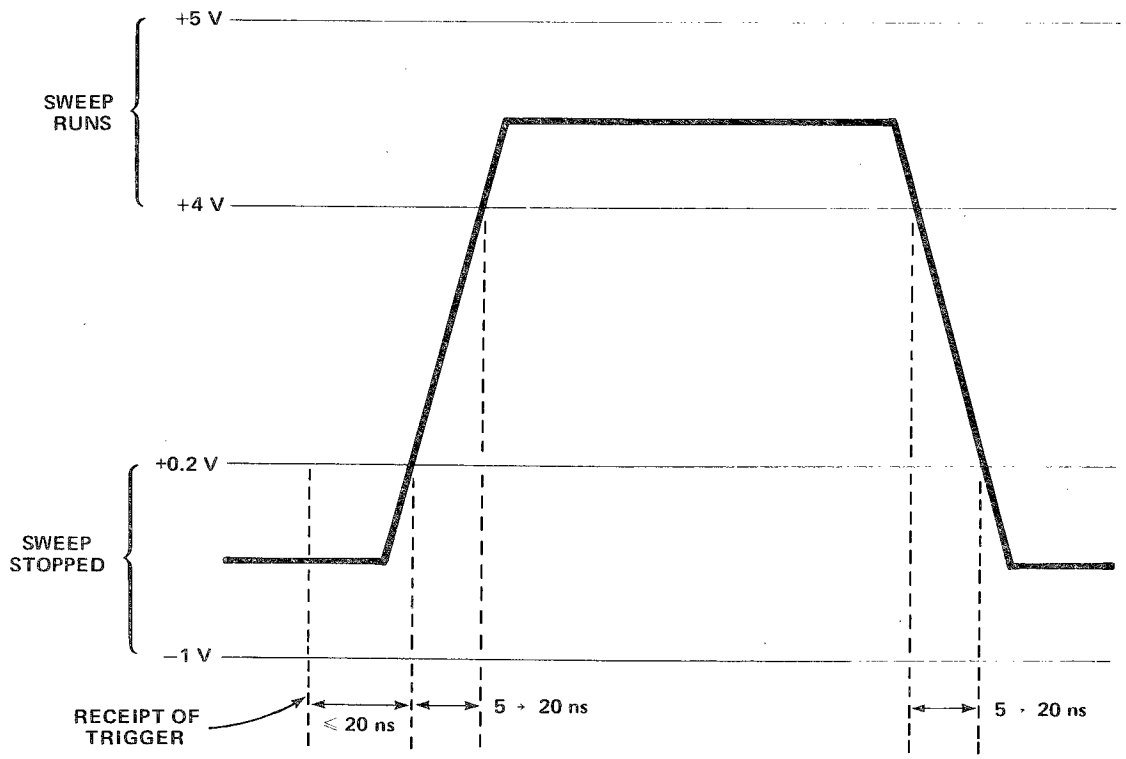
Auxiliary Sweep Gate, B5, is generated only by dual-sweep plug-ins. Usages are Gate Signal Out and Main Frame processing. It is not intended to be used as an unblanking signal.

See Miscellaneous Section—7000 Series Gate Nomenclature, for explanation of plug-in differences.

EQUIVALENT CIRCUIT



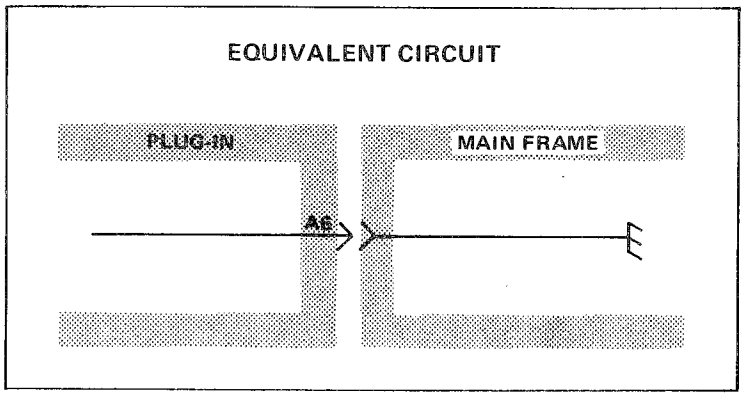
WAVEFORM



A6

CHOP COMMON

Chop Common, A6, is used to return to the Main Frame any current drawn from A5 (Chop Drive), B6 (Alternate Drive), and B7 (Main Frame Channel Switch signal). This line is grounded in the Main Frame and should not connect to ground in the plug-in unit.



ALTERNATE DRIVE

Alternate Drive, B6, is derived from horizontal plug-in or Main Frame information and used primarily by dual-channel plug-ins in the Alternate mode, to switch between channels.

General Information:

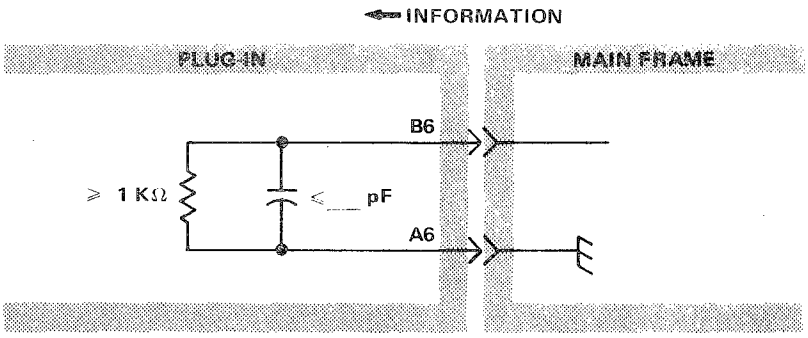
In a 4-hole Main Frame, CH 1 of a dual-channel plug-in is slaved to B Sweep and CH 2 is slaved to A Sweep during the following conditions:

(1) Main Frame horizontal is in ALT or CHOP.
(2) Main Frame vertical is NOT in ALT. (Clear Left, Right, Chop)
(3) A Sweep is NOT in Delaying mode.

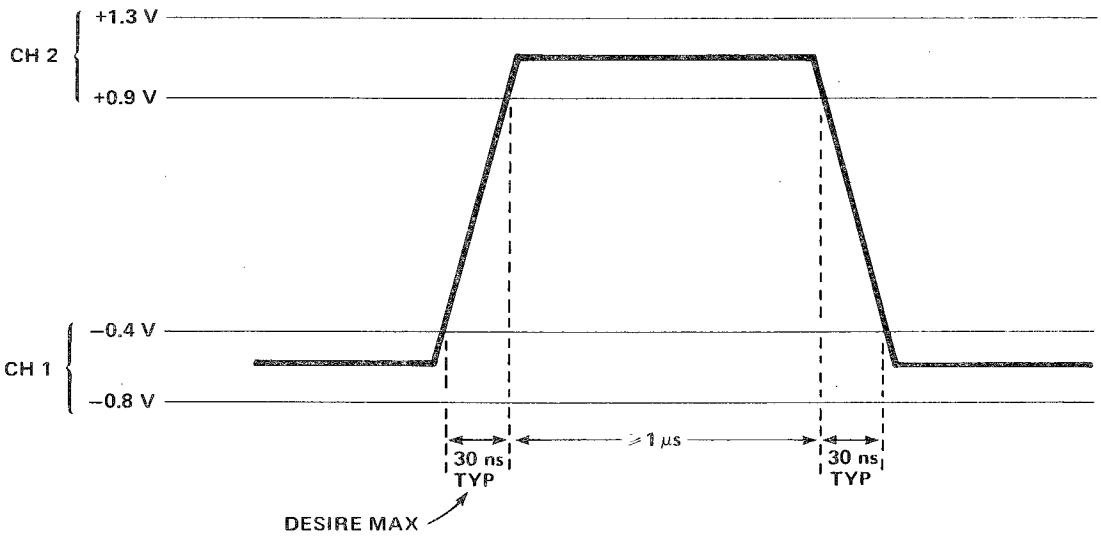
In a 3-hole Main Frame, vertical plug-ins are not slaved to the horizontal plug-in compartment.

For additional details of the Alternate Function, refer to the section on Logic.

EQUIVALENT CIRCUIT



WAVEFORM



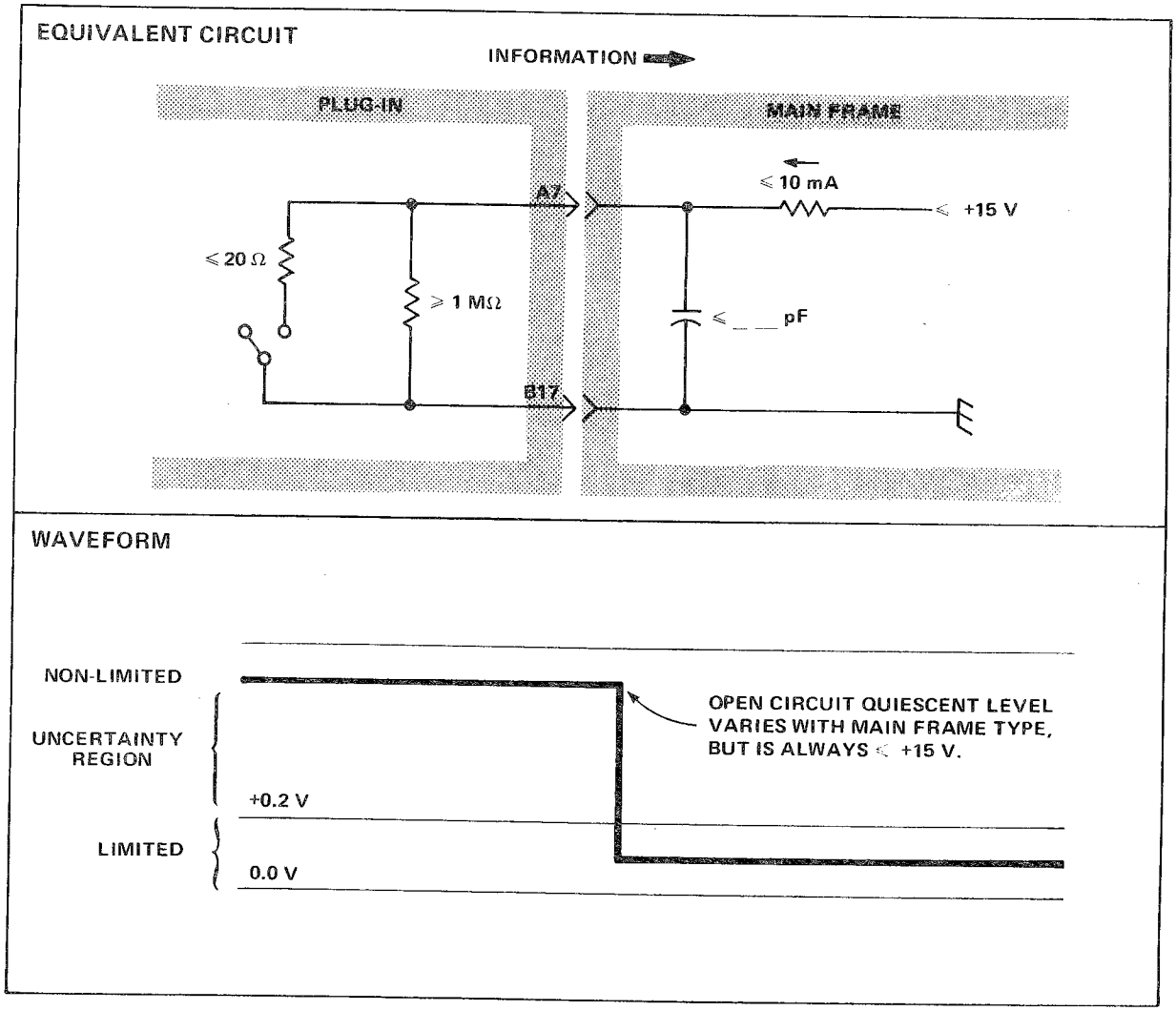
A7

INTENSITY LIMIT

Intensity Limit, A7, is used to reduce the possibility of burning the crt. Any time base sweep speed of 0.1 sec/div or slower will reduce the intensity to the limited value regardless of other time-base sweep speeds. The level of maximum intensity in the limited case is set by the Main Frame. For intensities below the limiting value, the intensity will not change when A7 is grounded.

General Information:

To assure optimum protection, the limit value should be set for the crt phosphor used.

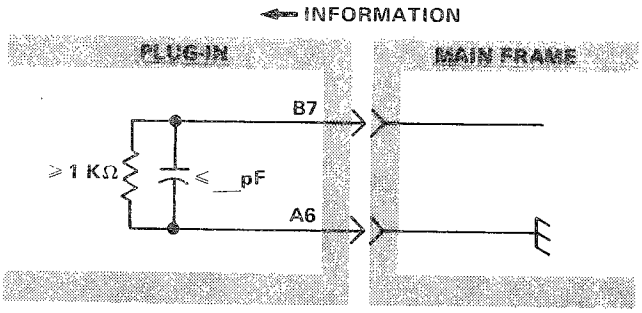


MAIN FRAME CHANNEL SWITCH SIGNAL

Main Frame Channel Switch Signal, B7 (with A16), is used by the plug-ins to determine when they are being displayed. This information is necessary when the Aux Z and/or Aux Y Axis are/is being used. This insures that only the displayed plug-in is controlling the Z and/or Y Axis. The Main Frame Delay Line's Time Delay must be considered when using these signals.

For additional details of Main Frame Channel Switching Signals, refer to section on Logic.

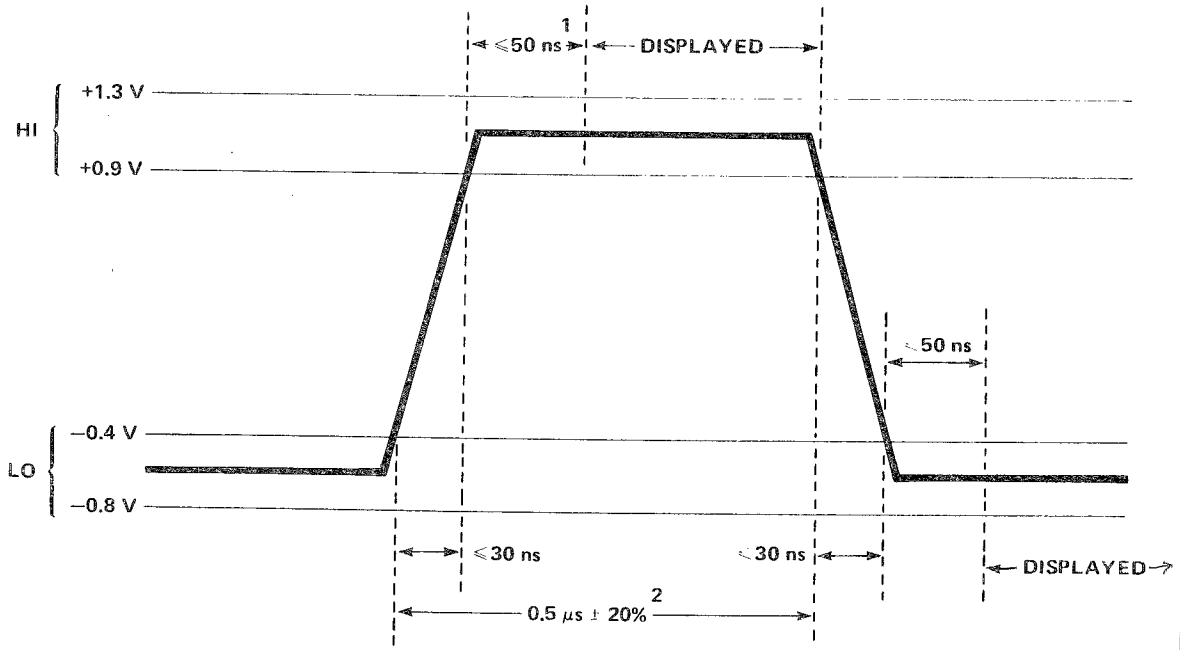
EQUIVALENT CIRCUIT



TRUTH TABLE

B7	A16	DISPLAY
LO	LO	NO
LO	HI	YES
HI	LO	YES
HI	HI	NO

WAVEFORM



[1] Some existing vertical plug-ins may not meet this specification.

[2] 7704A has a selectable 5 μs time.

A8

+5 V POWER

+5 V Power, A8, will provide up to 500 mA to each plug-in compartment. Each plug-in is limited to 16.5 W total power consumption.

General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

SWEEP LOCKOUT

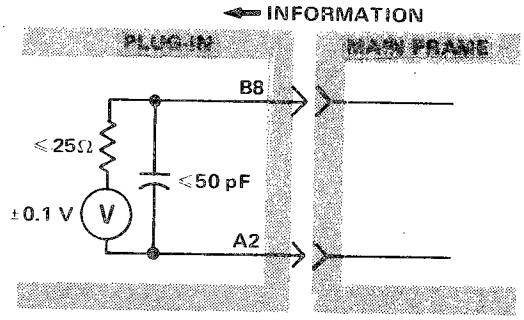
Sweep Lockout, B8, is derived from the time-base plug-in Delay Gate B9 or from main frame commands. This information is used to control when a sweep may operate.

B1 determines what the time base plug-in does when B8 goes to its LO state.

Special Considerations:

1. If B8 goes to the HI state when the sweep is running, the sweep must reset and perform its holdoff cycle.
2. The fast fall rate is necessary to assure proper time base plug-in sequencing. However, some commands may be much slower if sequencing is not of importance (i.e., storage commands).
3. A1 must be LO when B8 is HI.

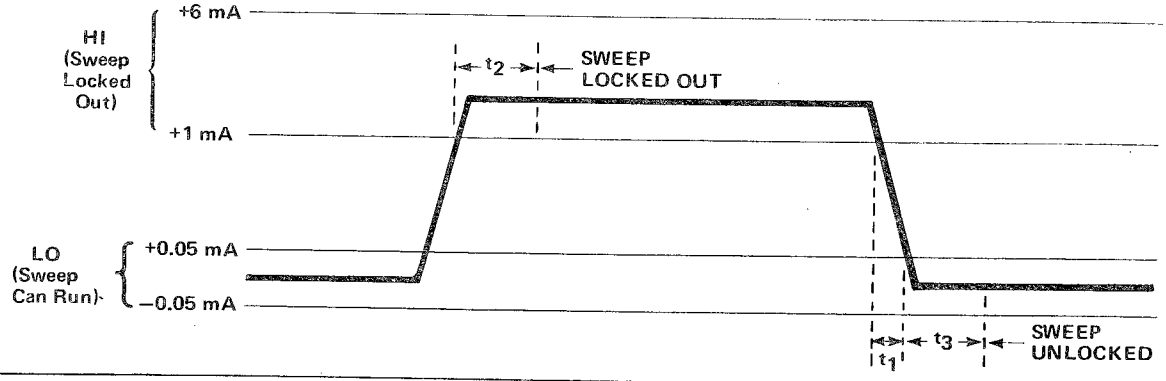
EQUIVALENT CIRCUIT



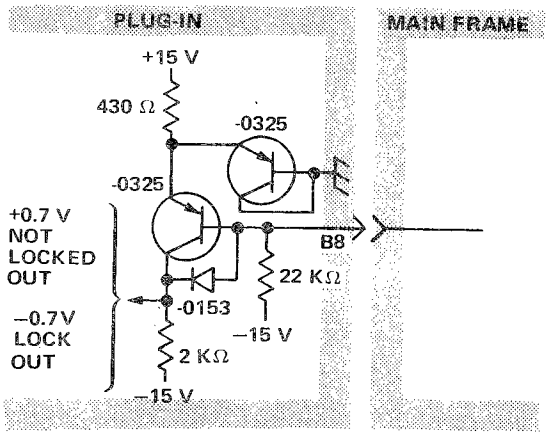
WAVEFORM

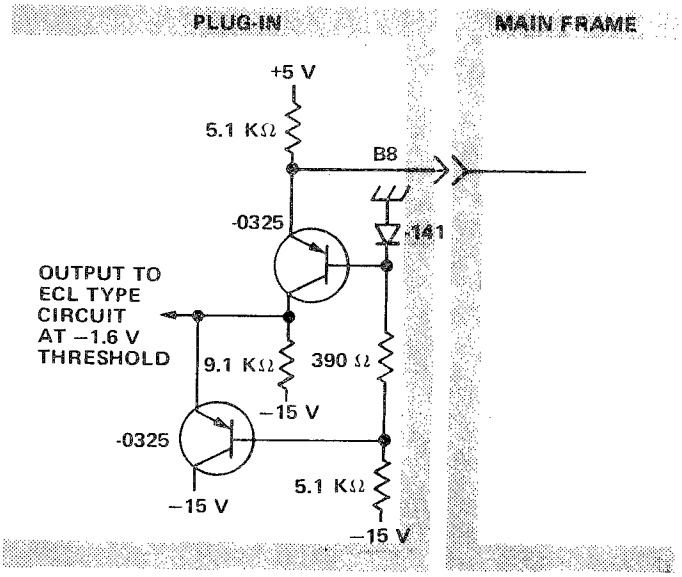
t_1 (10 - 15 ns) when generated from Delay Gate (B9).

t_2 and t_3 depends on plug-in—shorter is better, 10 - 20 ns is good.



POSSIBLE LOCKOUT CIRCUITS FOR PLUG-INS





A9

+5 V LIGHTS

+5 V Lights, A9, will provide up to 500 mA (previously 750 mA) to each plug-in compartment.

Each plug-in is limited to 16.5 W total power consumption.

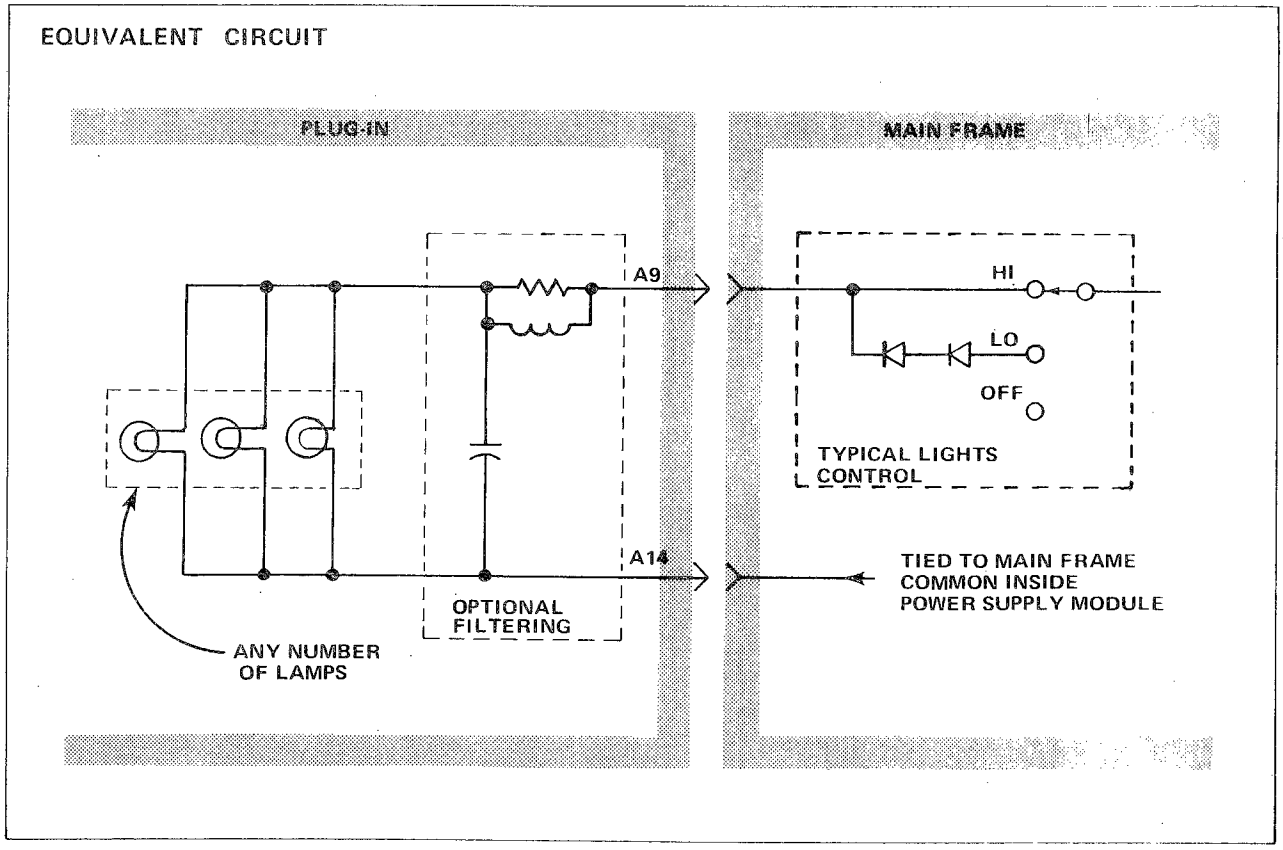
General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

Main Frames generally provide +5 V lights and control switching: HI (+5 V), LO (≈ +3.5 V), and OFF. The 7300, 7400, and 7600 Series do not provide +5 V Lights except as a conversion kit (040-0686-00).

Special Considerations:

1. When lights are used close to high sensitivity circuitry, i.e., vertical plug-in inputs, additional +5 V Lights filtering may be required.
2. A9, +5 V Lights, shall only be returned to A14.



DELAY GATE

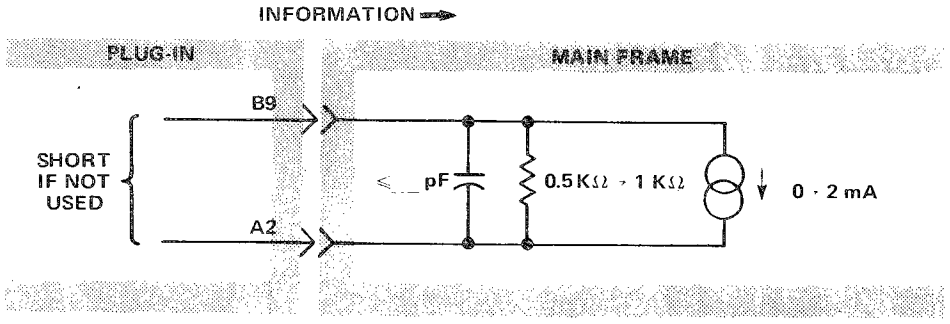
Delay Gate, B9, is generated by delaying sweep plug-ins (except dual-sweep plug-ins) when used in the Delaying mode. The Delaying mode is only usable when the Delayed Gate is generated by a sweep plug-in in the A compartment (B9 [A] drives B8 [B]). In some Main Frames, B9 information is used to generate Gate Out signals.

Special Considerations:

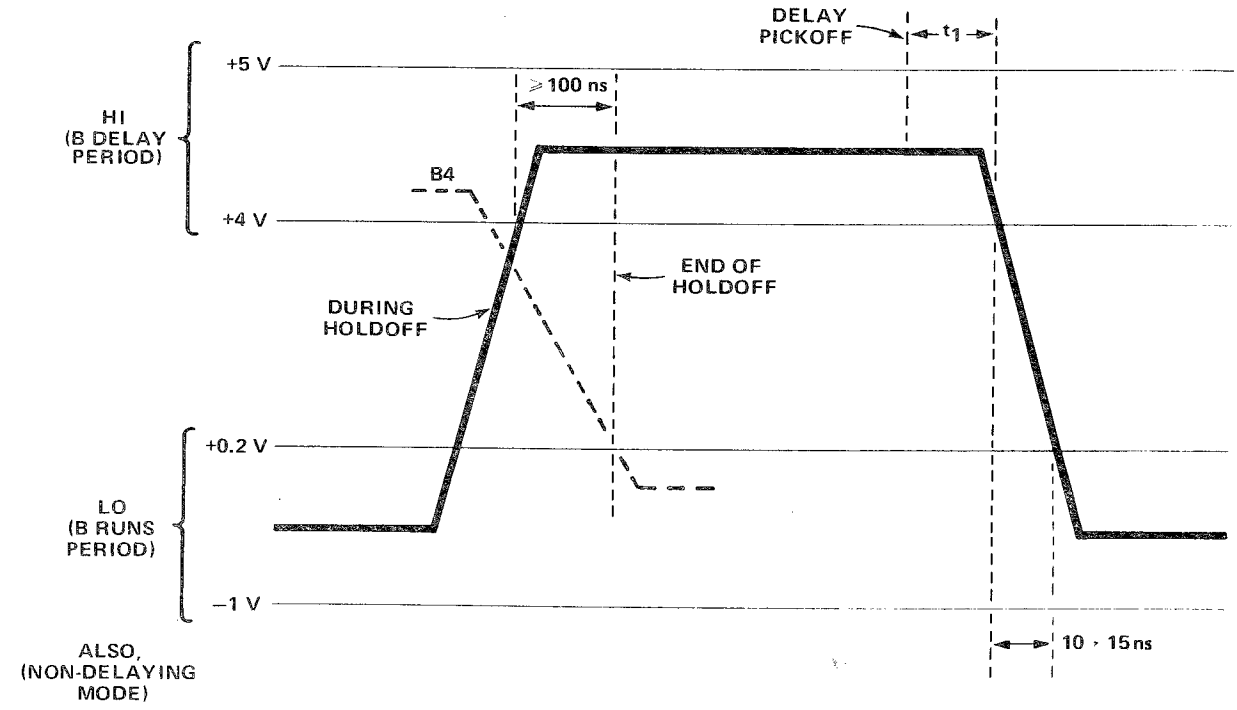
1. Following B9 transition from high to low, the sweep plug-in should run or be triggerable. The sweep must run only **ONCE** per B9 high to low transition.
2. B9 must stay low, if B2 is low.

B2 determines what the B compartment time-base plug-in does when B9 goes to its LO state.

EQUIVALENT CIRCUIT



WAVEFORM



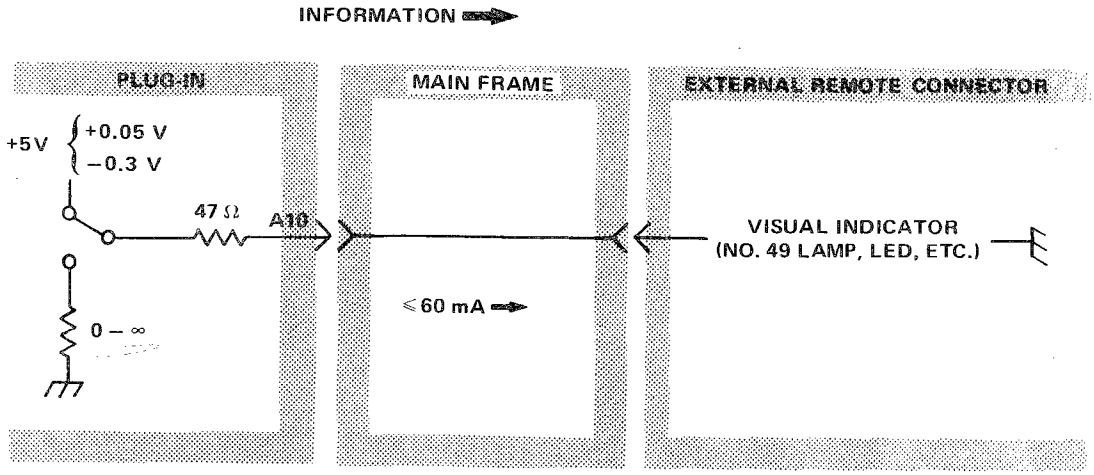
t_1 depends on plug-in. Shorter is better, 10 - 20 ns is good.

A10

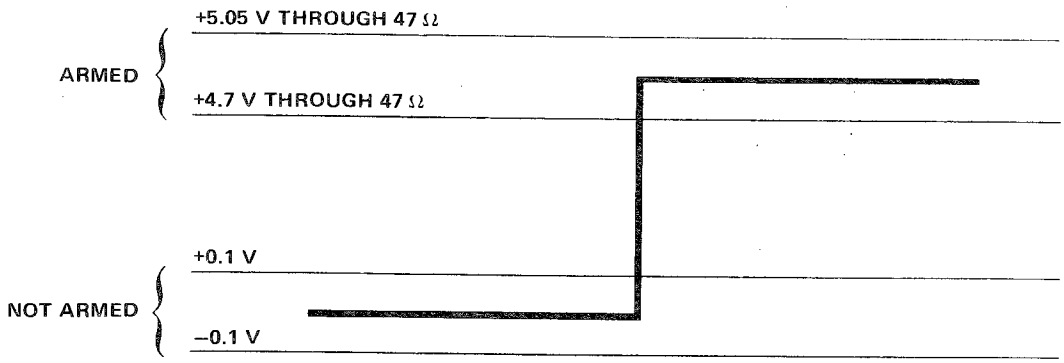
SINGLE SWEEP READY INDICATOR

Single Sweep Ready Indicator, A10, is used to determine if a sweep is armed when in the Single Sweep mode.

EQUIVALENT CIRCUIT



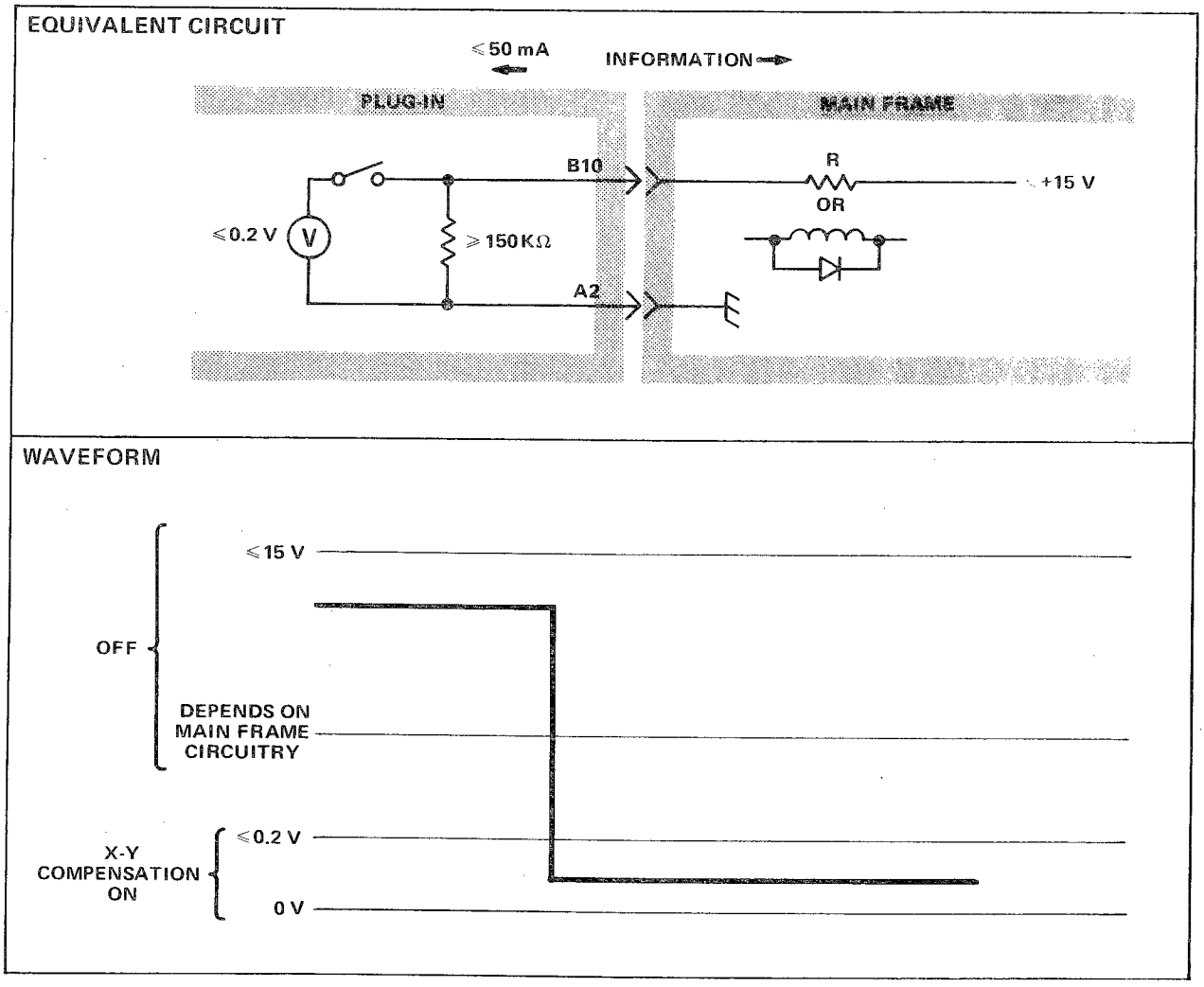
WAVEFORM



X-Y COMPENSATION

X-Y Compensation, B10, supplies the Main Frame with information to identify the presence of an amplifier plug-in (or sweep plug-in in Amplifier mode) in a horizontal plug-in compartment. This information can be used to switch in Horizontal signal path X-Y Compensation, Horizontal Alternate mode LOGIC and any other necessary control functions.

*Beware of 7B51 and 7T11, they connect B10 to +15 volts.



A11

SIGNAL +

Signal +, A11, provides signal input to the Main Frame. Positive signal on A11 deflects the trace up in the vertical compartments and to the right in the horizontal compartment(s).

DC Considerations:

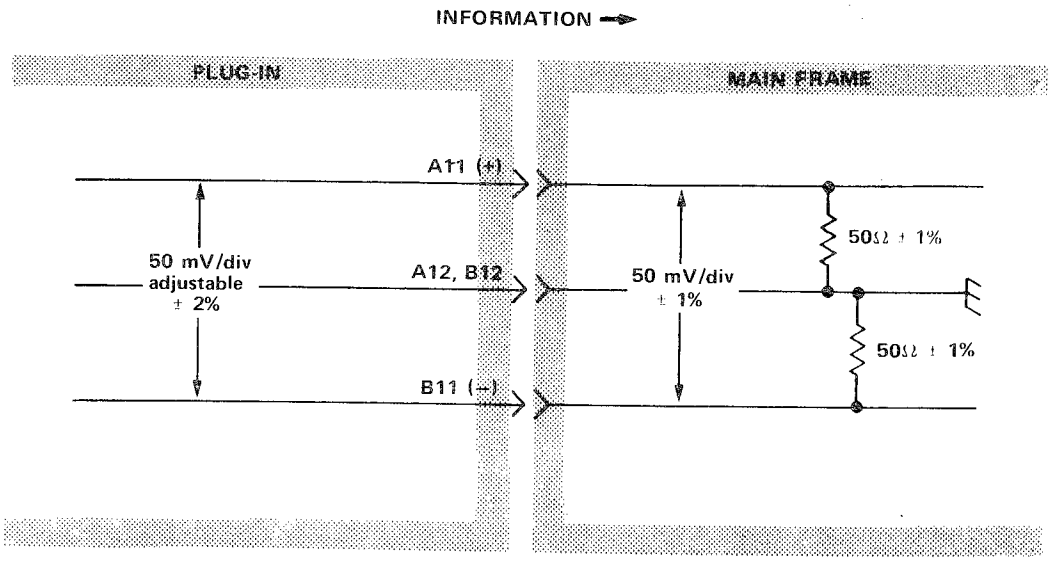
Deflection Factor	50 mV/div ± 1% differential
Input R	
A11 to A12, B12	50 Ω ± 1%
B11 to A12, B12	50 Ω ± 1%
A11 to B11	100 Ω ± 1%
A11 shorted to B11 to A12, B12	25 Ω ± 10%
Usable Signal Limits (all AC & DC specs apply)	± 9 divisions
Maximum Signal Limits	± 15 divisions
DC Centering	± 0.5 division of graticule center
Maximum Input DC Common Mode Component	150 mV or less

AC Considerations:

TDR (push-pull) [t_r equivalent to 0.35 ÷ 1.5 x Main Frame bandwidth]	2% ≤ 250 MHz 10% ≥ 250 MHz
CMRR to BW (for full screen signal)	≥ 100:1 ≤ 250 MHz ≥ 50:1 ≥ 250 MHz*

* Plug-in should be back-terminated.

EQUIVALENT CIRCUIT



SIGNAL –

Signal –, B11, provides signal input to the Main Frame. Negative signal on B11 deflects the trace up in the vertical compartments and to the right in the horizontal compartment(s).

DC Considerations:

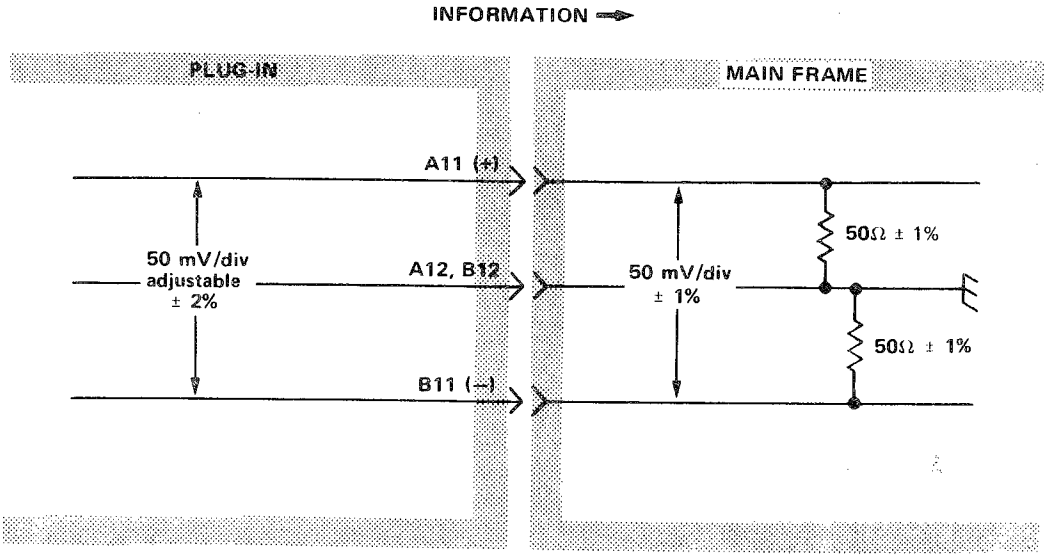
Deflection Factor	50 mV/div ± 1% differential
Input R	
A11 to A12, B12	50 Ω ± 1%
B11 to A12, B12	50 Ω ± 1%
A11 to B11	100 Ω ± 1%
A11 shorted to B11 to A12, B12	25 Ω ± 10%
Usable Signal Limits (all AC & DC specs apply)	± 9 divisions
Maximum Signal Limits	± 15 divisions
DC Centering	± 0.5 division of graticule center
Maximum Input DC Common Mode Component	150 mV or less

AC Considerations:

TDR (push-pull) [t_r equivalent to .35 ± 1.5 x Main Frame bandwidth]	2% ≤ 250 MHz 10% ≥ 250 MHz
CMRR to BW (for full screen signal)	≥ 100:1 ≤ 250 MHz ≥ 50:1 ≥ 250 MHz *

* Plug-in should be back-terminated.

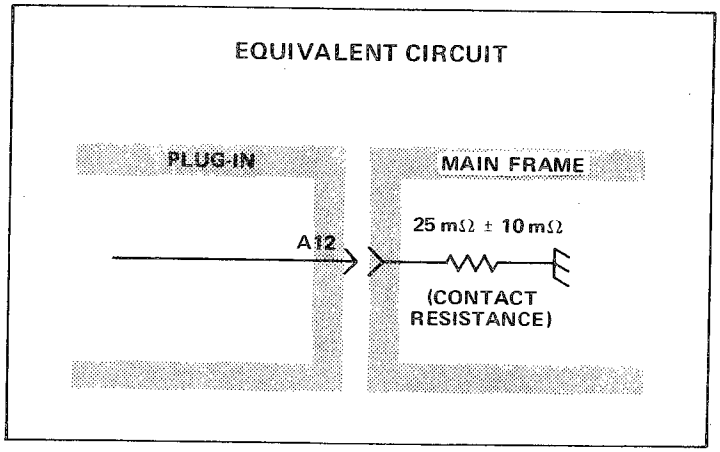
EQUIVALENT CIRCUIT



A12

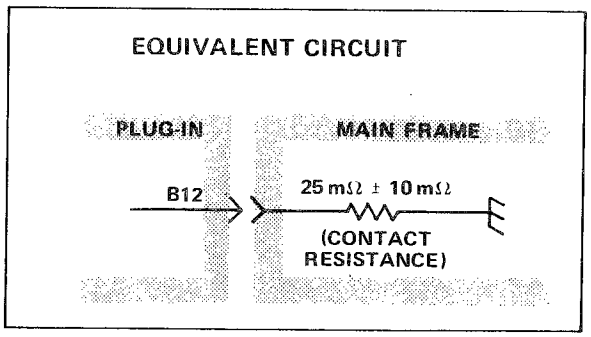
GROUND

Ground, A12, provides ground reference for A11 and A13. In addition, it is used as the plug-in power supply reference and return.



GROUND

Ground, B12, provides ground reference for B11 and B13. In addition, it is used as the plug-in power supply reference and return.



A13

+ TRIGGER OUT (V)

+ Trigger Out (V), A13, (differentially with B13) trigger input to the Main Frame. This trigger information is processed by the main frame and presented to the Horizontal MFI on pins A20 and B20. Positive-going trigger signal on A13 corresponds to a positive-going A11.

DC Considerations

MAIN FRAME (THROUGHPUT TO A20, B20)

Deflection Factor	50 mV/displayed signal division ± 5%.
Input R	
A13 to A12, B12	50 Ω ± 1%.
B13 to A12, B12	50 Ω ± 1%.
A13 to B13	100 Ω ± 1%.
A13 shorted to B13 to A12, B12	25 Ω ± 10%.
Usable Signal Limits	± 9 divisions (all ac & dc specifications apply)
Maximum Signal Limits	± 15 divisions.
Centering	± 0.20 division from A11, B11.
Maximum Input DC Common Mode Component	150 mV or less.

PLUG-IN

Deflection Factor	Within 2% of A11, B11 (50 mV/div).
Output R	See ac considerations.
Usable Signal Limits	± 9 divisions referred to A11, B11 (all ac and dc specifications apply)

PLUG-IN (cont.)

Maximum Signal Limits	± 15 divisions.
Centering	± 0.2 division from A11, B11.
Maximum Input Common Mode Component	150 mV or less.
Variable Volts/Div	Varies with signal channel.
Invert	Inverts with signal channel.

AC Considerations

MAIN FRAME (THROUGHPUT TO A20, B20)

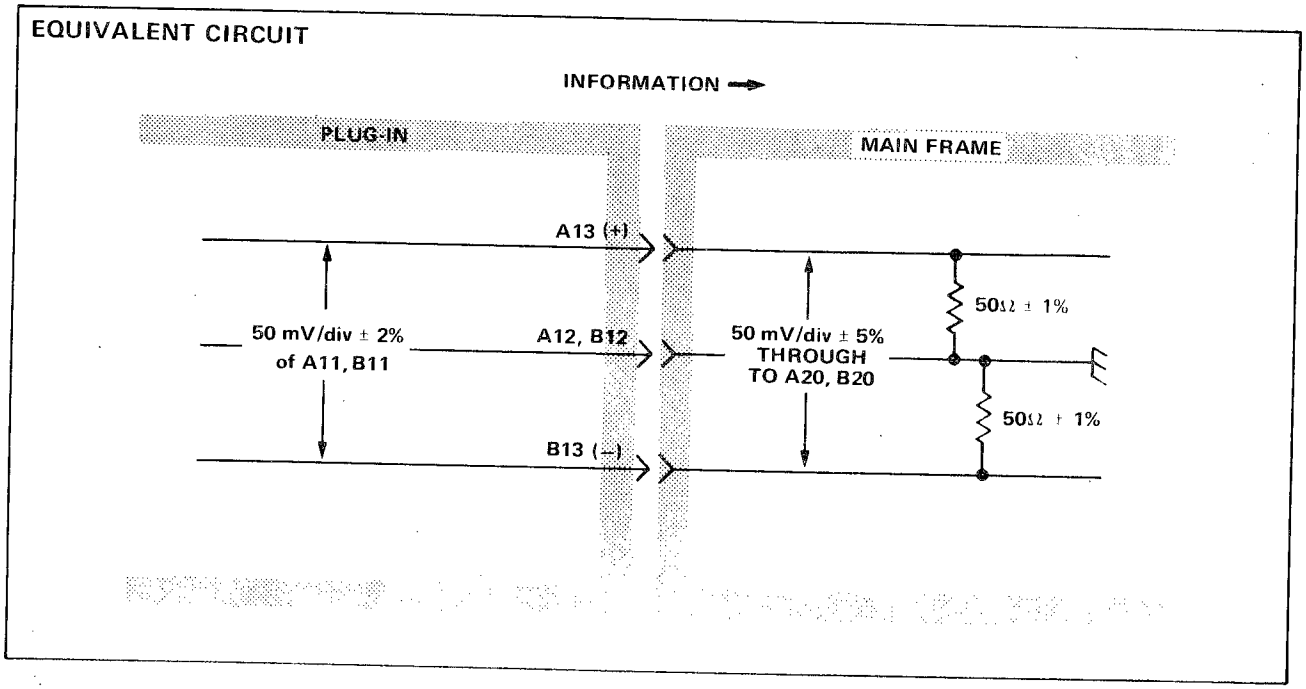
TDR (push-pull) (t_r equal to 0.35 ÷ 1.5 x BW)	2% ≤ 250 MHz. 10% ≥ 250 MHz.*
CMRR to BW (for full screen signal.	≥ 100:1 ≤ 250 MHz. ≥ 50:1 ≥ 250 MHz.*
Risetime	≤ displayed signal risetime (on screen).
Bandwidth	≥ displayed signal bandwidth (on screen).
Aberrations	+5%, –5% or less. Total 5% peak-to-peak or less.

PLUG-IN

Aberrations	+5%, –5% or less. Total 5% peak-to-peak or less.

*** Plug-in should be back terminated above 250 MHz.**

EQUIVALENT CIRCUIT



– TRIGGER OUT (V)

– Trigger Out (V), B13, trigger input to the Main Frame. This trigger information is processed by the main frame and presented to the Horizontal MFI on pins A20 and B20. Positive-going trigger signal on B13 corresponds to a negative-going B11.

DC Considerations

MAIN FRAME (THROUGHPUT TO A20, B20)

Deflection Factor	50 mV/displayed signal division ± 5%.
Input R	
A13 to A12, B12	50 Ω ± 1%.
B13 to A12, B12	50 Ω ± 1%.
A13 to B13	100 Ω ± 1%.
A13 shorted to B13 to A12, B12	25 Ω ± 10%.
Usable Signal Limits	± 9 divisions (all ac & dc specifications apply)
Maximum Signal Limits	± 15 divisions.
Centering	± 0.20 division from A11, B11.
Maximum Input DC Common Mode Component	150 mV or less.

PLUG-IN

Deflection Factor	Within 2% of A11, B11 (50 mV/div).
Output R	See ac considerations.
Usable Signal Limits	± 9 divisions referred to A11, B11 (all ac and dc specifications apply)

PLUG-IN (cont.)

Maximum Signal Limits	± 15 divisions.
Centering	± 0.2 division from A11, B11.
Maximum Input Common Mode Component	150 mV or less.
Variable Volts/Div	Varies with signal channel.
Invert	Inverts with signal channel.

AC Considerations

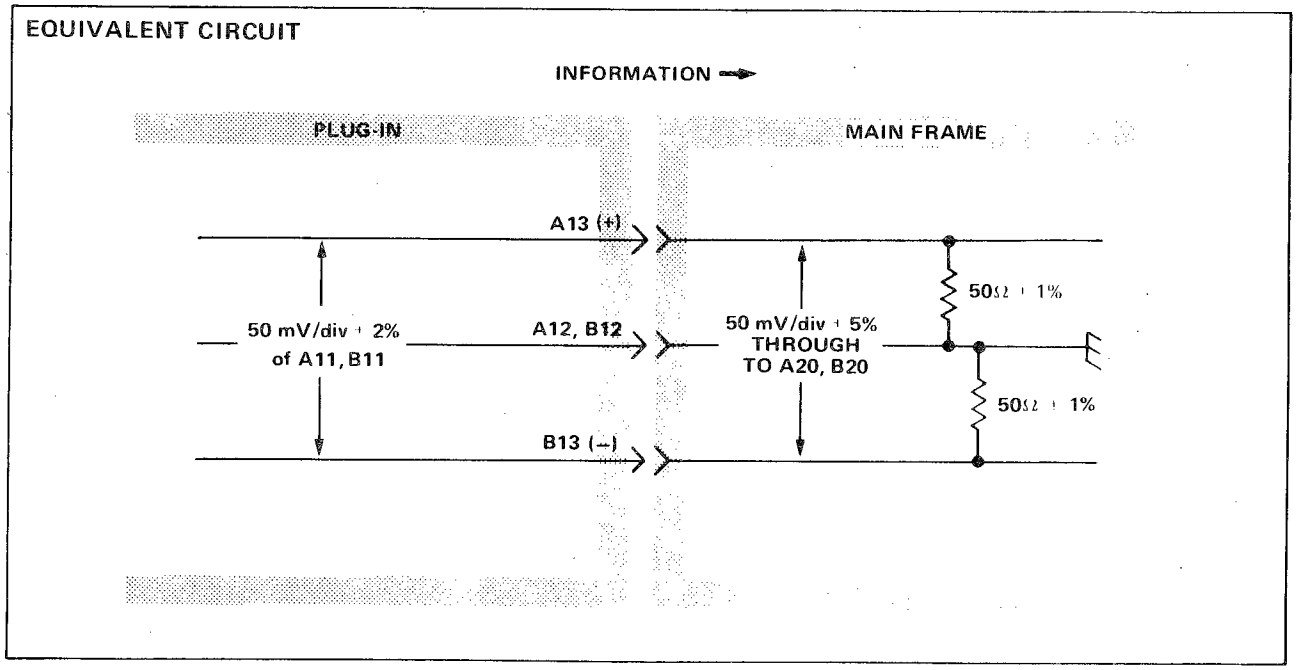
MAIN FRAME (THROUGHPUT TO A20, B20)

TDR (push-pull) (t_r equal to to 0.35 ÷ 1.5 x BW)	2% ≤ 250 MHz. 10% ≥ 250 MHz.*
CMRR to BW (for full screen signal.	≥ 100:1 ≤ 250 MHz. ≥ 50:1 ≥ 250 MHz.*
Risetime	≤ displayed signal risetime (on screen).
Bandwidth	≥ displayed signal bandwidth (on screen).
Aberrations	+5%, -5% or less. Total 5% peak-to-peak or less.

PLUG-IN

Aberrations	+5%, -5% or less. Total 5% peak-to-peak or less.

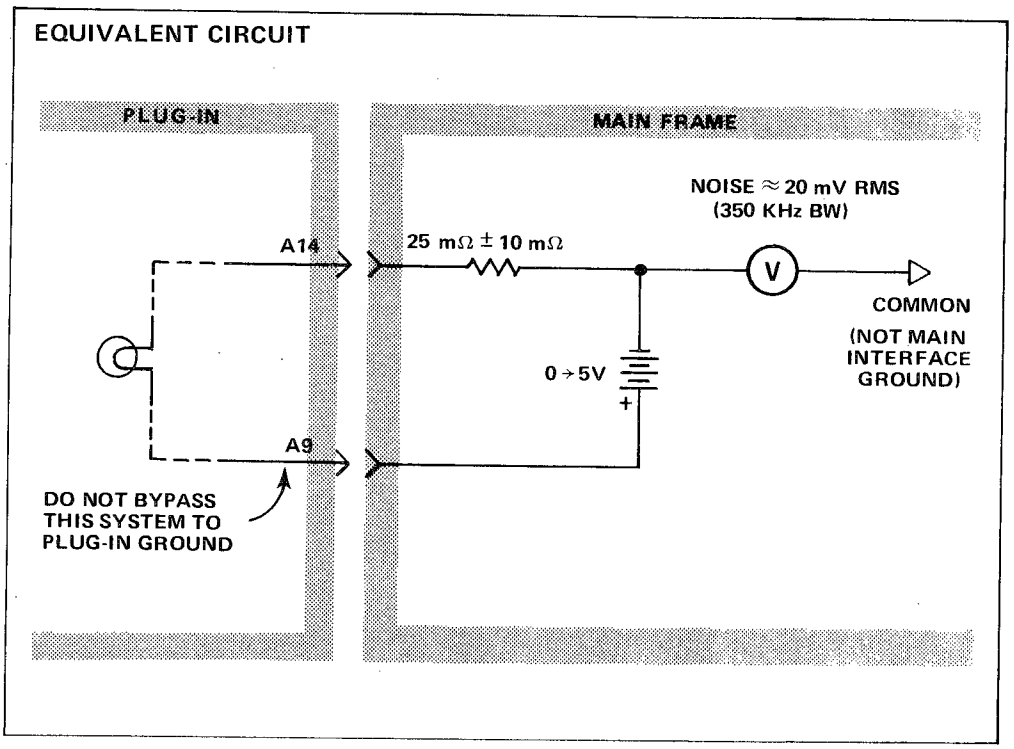
*** Plug-in should be back terminated above 250 MHz.**



A14

LIGHTS COMMON

Lights Common, A14, provides a return path for A9. Typically, A9 ties to MF ground inside the power supply.



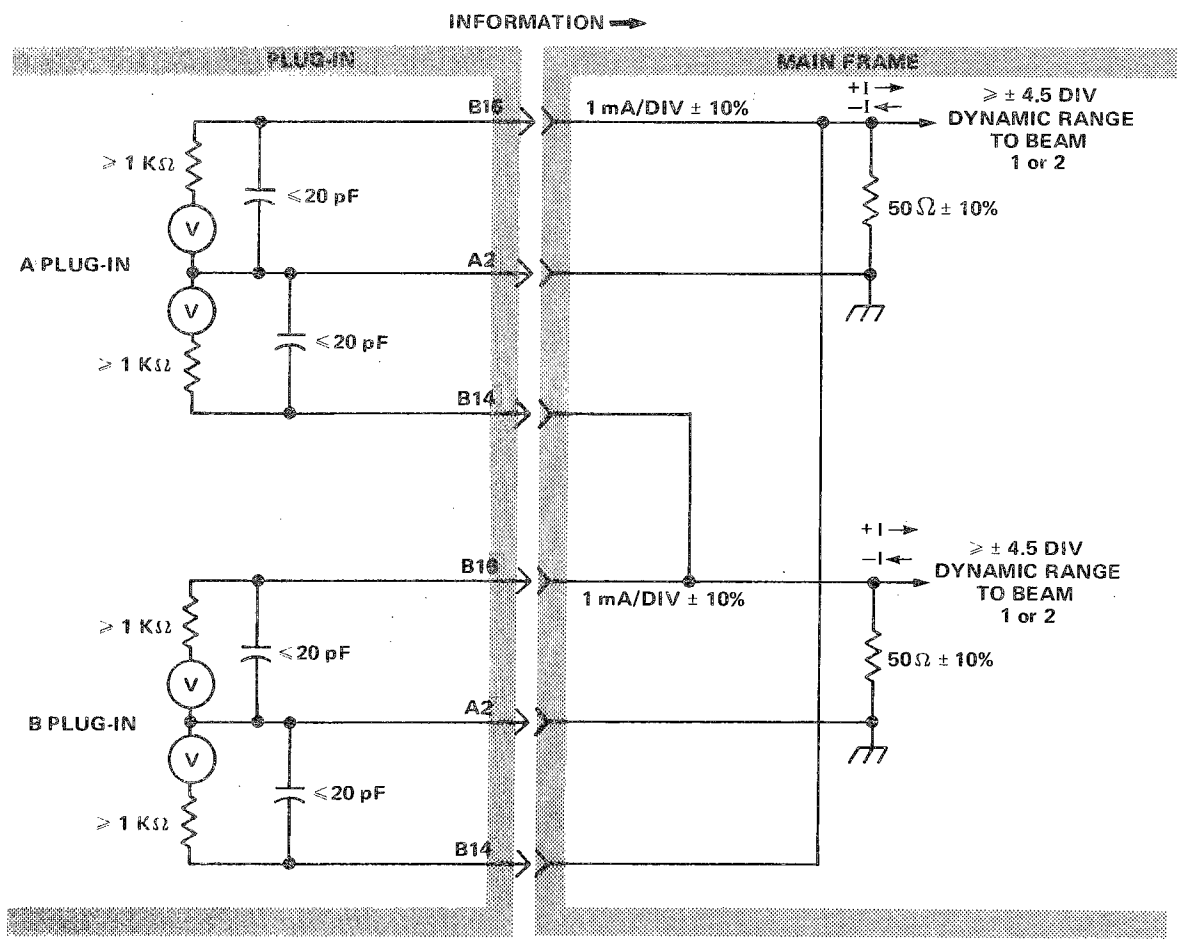
DUAL BEAM AUX Y AXIS

Dual Beam Aux Y Axis, B14, is used for vertical trace separation in Dual Beam Main Frame Sweep Switching applications. The analog signal originates in the time-base plug-in and is added to the Vertical Amplifier signal in the Main Frame. The displayed signal is deflected up with +I and is deflected down with −I.

Special Considerations:

The plug-in must obey A16 and B7.

EQUIVALENT CIRCUIT



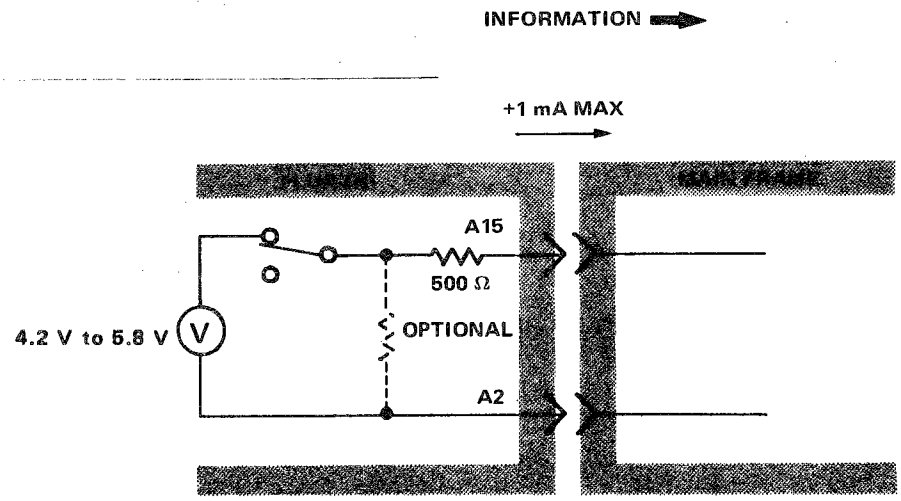
A15

SINGLE SWEEP LOGIC

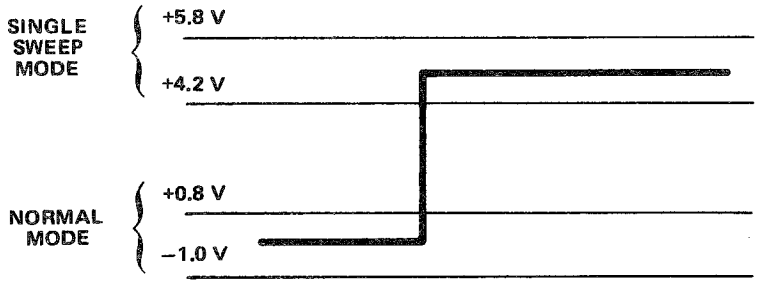
Single Sweep Logic, A15, provides the Main Frame with logic information from the sweep plug-in(s), indicating when the plug-in(s) is/is not in single sweep mode.

NOTE: *The 7B50, 7B51, 7B70, and 7B71 units do not meet this specification. They present a 4.7 kΩ series resistor when in the HI state.*

EQUIVALENT CIRCUIT



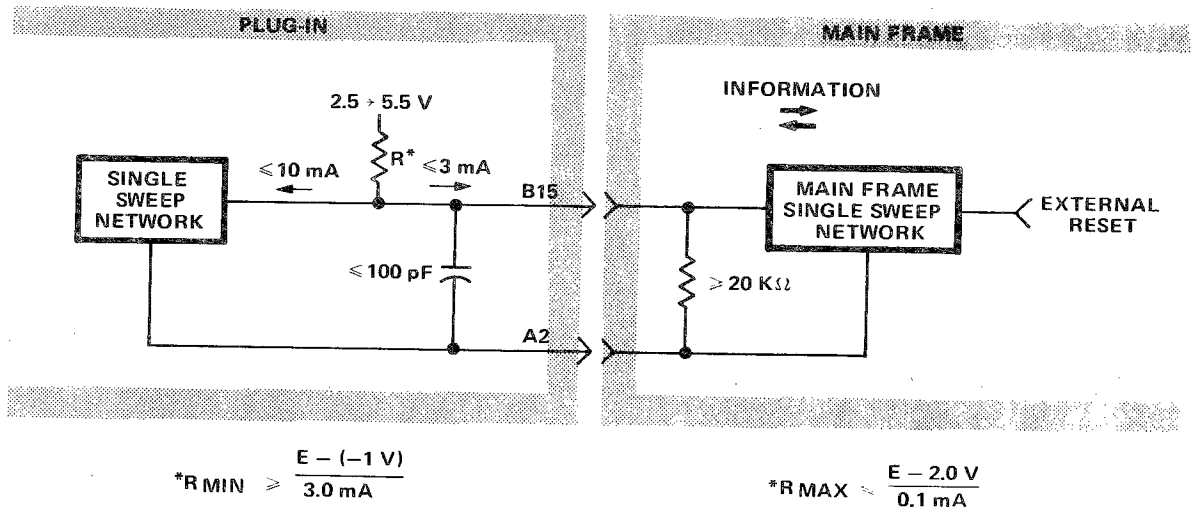
WAVEFORM (Plug-In Generated)



SINGLE SWEEP RESET

Single Sweep Reset, B15, is used to reset sweep plug-ins in the single-sweep mode. Some digital plug-ins use this pin as a strobe interrogation pulse.

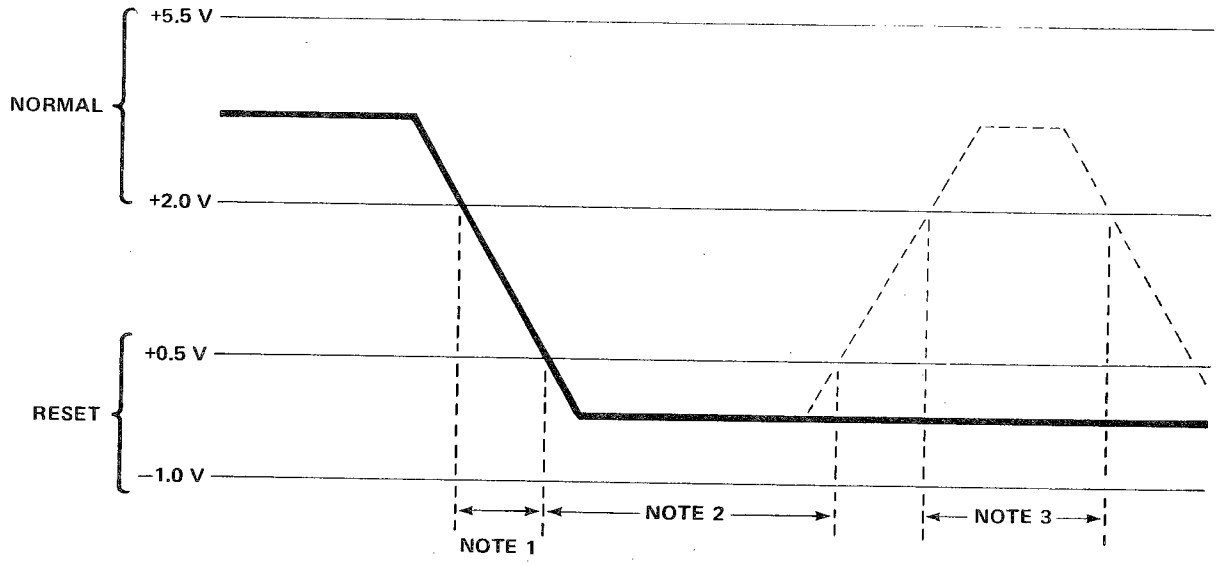
EQUIVALENT CIRCUIT



$$*R_{MIN} \geq \frac{E - (-1\ V)}{3.0\ mA}$$

$$*R_{MAX} \leq \frac{E - 2.0\ V}{0.1\ mA}$$

WAVEFORM



NOTES:

1. Falltime not critical (i.e., circuitry is DC coupled) except that digital plug-ins require fall times less than or equal to 100 ns.

2. The time for Reset is dependent on sweep plug-in state/type.

   a. Sweep not running when reset received. Reset time ≤ 400 ns. (Typical sweep plug-in values 100-300 ns).

   b. Sweep running or lockout present when reset received. Some old sweep plug-ins will not recognize this condition, but new designs must. For those that will - reset time; Total Sweep Time + Holdoff Time + Note 3 Time.

   c. When the 7D12/M2 is in Δ sampling operation, the width of the Reset Pulse determines the time difference between strobing pulses.

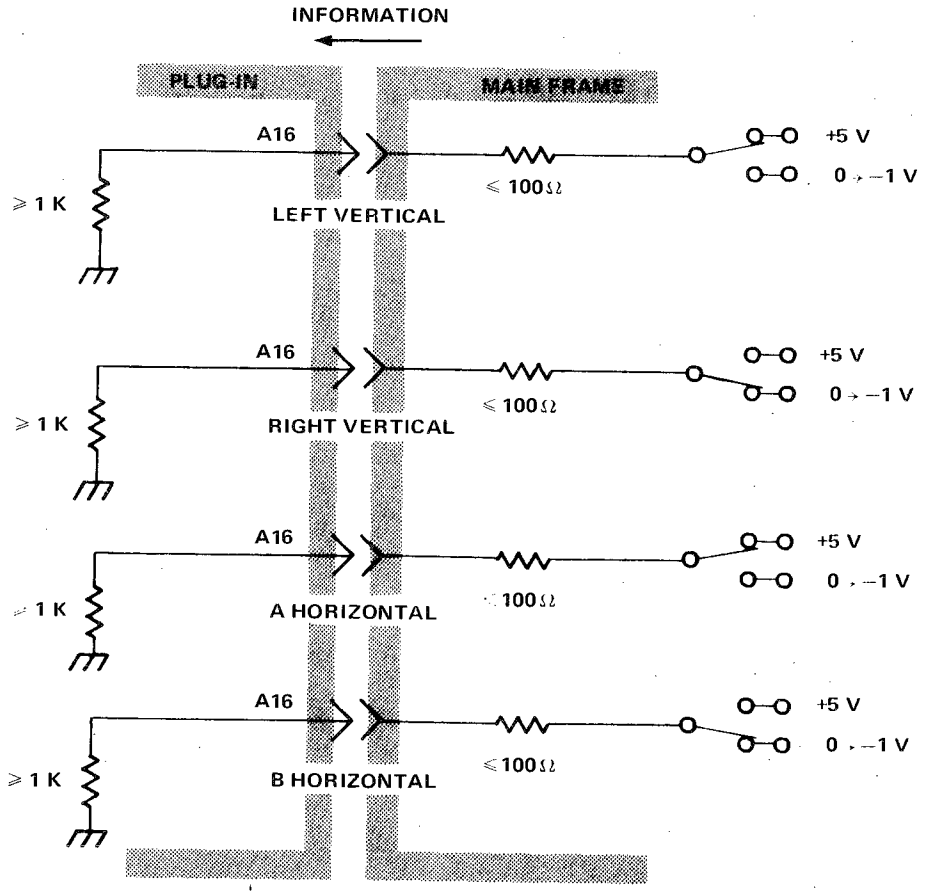
3. Normal time following reset prior to next reset ≥ 1 second. (Typical sweep plug-ins 1 ms to 800 ms.)

A16

MAIN FRAME MODE INFO

Main Frame Mode Info, A16 (with B7), is used by the plug-ins to determine when they are being displayed. This information is necessary when Aux Z (A17) and/or Aux Y (B16) is being used to insure that only the displayed plug-in is modifying the Z and/or Y axis signal.

EQUIVALENT CIRCUIT



TRUTH TABLE

B7	A16	DISPLAY
LO	LO	NO
LO	HI	YES
HI	LO	YES
HI	HI	NO

HI = +5 V ± 0.2 V

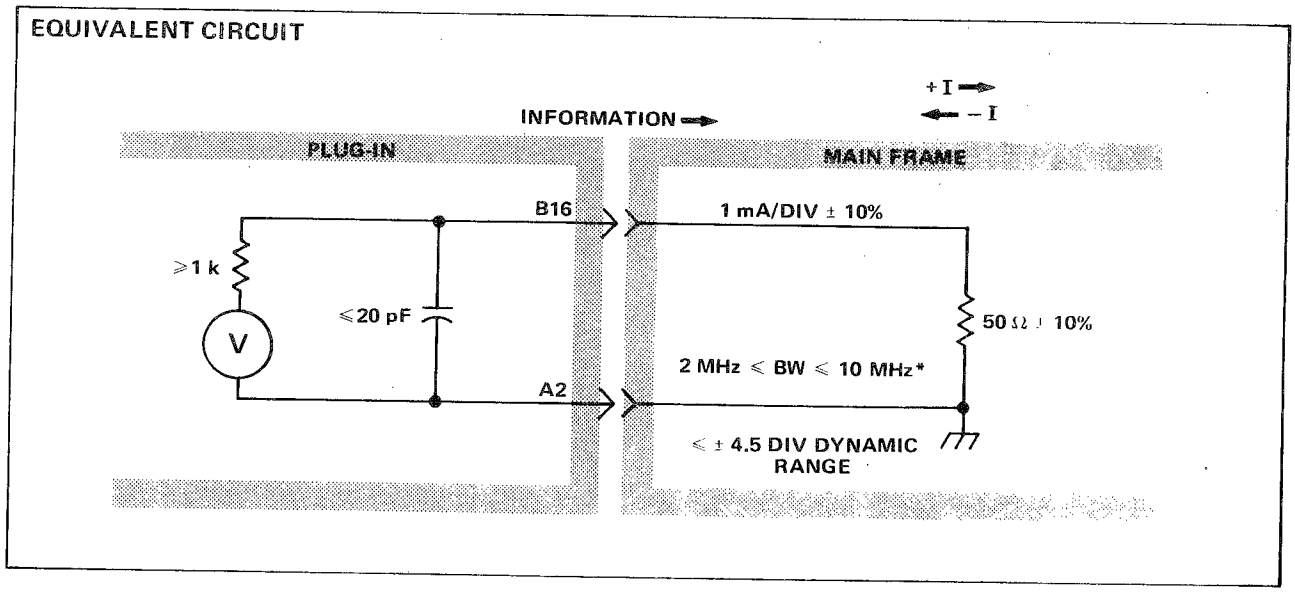
LO = 0 TO −1 V

AUX Y AXIS

Aux Y Axis, B16, is used for vertical trace separation in Sweep Switching applications. The analog signal originates in the time-base plug-in and is added to the vertical amplifier signal in the Main Frame. The displayed signal is deflected up with + I and is deflected down with − I.

This pin was introduced after the 7704 and 7504. Hence, this pin is not used in these instruments.

The plug-in must obey A16 and B7.

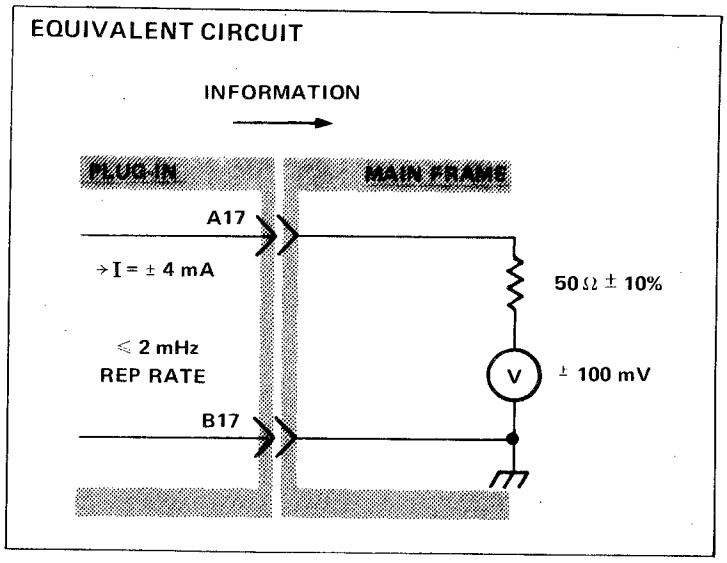


* 7704A has greater than 10 MHz bandwidth, and causes problems with logic signals coupling into B16.

A17

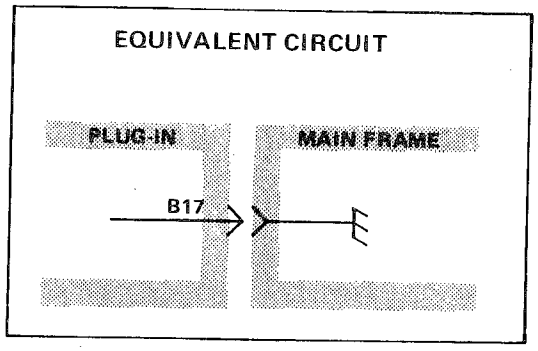
AUX Z AXIS

Aux Z Axis, A17, is used by the plug-in to intensity modulate the crt. The Aux Z Axis will dim (+ I) or brighten (−I) the trace from the level set by the Main Frame INTENSITY control (i.e., ≈ +4 mA will extinguish a maximum intensity trace). A17 is used in conjunction with A16, A7, and B7.



AUX Z AXIS COM

Aux Z-Axis Com, B17, is used to return to the Main Frame any current drawn from Aux Z-Axis (A17). This line is grounded in the Main Frame and should not connect to ground in the plug-in.



A18

+15 V POWER

+15 V Power, A18, will provide up to 500 mA to each plug-in compartment.

Each plug-in is limited to 16.5 W total power consumption.

General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

−15 V POWER

−15 V Power, B18, will provide up to 500 mA to each plug-in compartment.

Each plug-in is limited to 16.5 W total power consumption.

General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

A19

+50 V POWER

+50 V Power, A19, will provide up to 100 mA to each plug-in compartment.

Each plug-in is limited to 16.5 W total power consumption.

General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

−50 V POWER

−50 V Power, B19, will provide up to 100 mA to each plug-in compartment.

Each plug-in is limited to 16.5 W total power consumption.

General Information:

Refer to section on Power Supplies for information concerning power supply parameters.

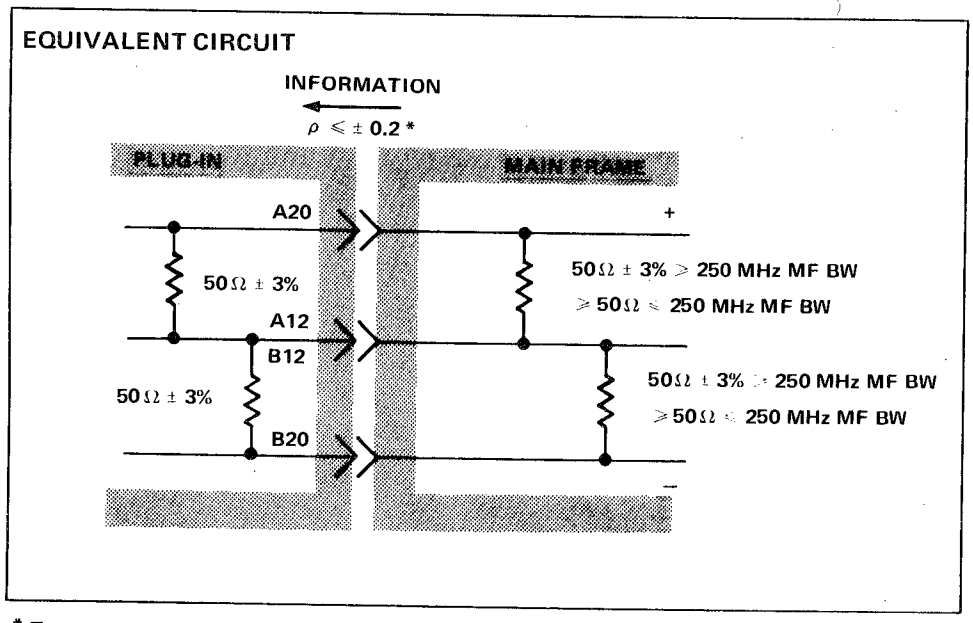
A20

+ TRIGGER IN (B20 = –A20)

+ Trigger In,A20,(with –Trigger In B20) provides a push-pull trigger signal to the horizontal plug-in. The trigger signal is positive going when the signal channel is positive going.

Main Frame Considerations (Analog Differential Signals)

Deflection Factor	50 mV/displayed div ± 5%.
Risetime	≤ to display channel.
Aberrations	≤ ± 5%. Total ≤ 5% P-P for ≤ ± 5 div signals. Or 0.5 div P-P for signals > ± 5 div.
Bandwidth	≥ display channel.
Position with Respect to Display Channel	Within ± 0.5 div over ± 5 div of display channel positioning.
Maximum Output Voltage	± 0.75 V for a total of 1.5 V differentially.
DC Common Mode Output Current to Plug-In	≤ 4 mA.
Common Mode Output Signal	≤ 0.1 differential signal.
Maximum Common Mode Current	≤ 4 mA.
Common Mode Output Resistance	≥ 25Ω.



* T_r equivalent to 0.35 ÷ 1.5 x MF BW.

– TRIGGER IN

See A20 information.

A21

+ AUX TRIGGER IN

A21 was used as + Aux Trigger In. The 7B52 uses this pin, but no other plug-ins do. This pin will be left unused.

– AUX TRIGGER IN

B21 was used as – Aux Trigger In. The 7B52 uses this pin—no other plug-ins do. This pin is now a spare.

A22

$\overline{\text{EOI}}$ (End or Identify)

Bus management signal for programmable plug-ins. This is a TTL signal specified in IEEE standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
A22	$\overline{\text{EOI}}$	EOI (end or identify) is used to indicate the end of a multiple byte transfer sequence, or, in conjunction with ATN, to execute a polling sequence.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in must be able to sink 24 mA at 0.4 V.

$\overline{\text{SRQ}}$ (Service Request)

Bus management signal for programmable plug-ins. This is a TTL signal specified in IEEE standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
B22	$\overline{\text{SRQ}}$	SRQ (service request) is used by a device to indicate the need for attention and to request an interruption of the current sequence of events.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in must be able to sink 24 mA at 0.4 V.

A23

$\overline{\text{DAV}}$ (Data Valid)

Handshake signal for programmable plug-ins. The function of this signal has been modified from Standard 488-1975. Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
A23	$\overline{\text{DAV}}$	DAV (data valid) is used to indicate the condition (availability and validity) of information on the DIO signal lines.

A plug-in may place one standard TTL and one LSTTL input on the line.

Plug-ins may not drive this line.

REN (Remote Enable)

REN is a positive-true open collector TTL line.

REN (remote enable) used by the programmable main frame to enable or disable the local operation of the plug-ins.

The plug-ins respond to the RL (Remote Local) Interface function in the subset RL2. That is, the states LWLS (Local with Lockout State) and RWLS (Remote With Lockout State) are omitted. The main frame responds to the RL1 Interface Function requirements of the GPIB. Reference Table 23, IEEE Standard 488-1975.

The plug-ins must respond to a 1 microsecond pulse of REN = Ø, which occurs when the main frame rtl (return to local) button is pressed. The plug-ins respond to the RL2 subset, but in conjunction with the main frame, have full RL1 capability.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in system controller must be able to sink 24 mA at 0.4 V.

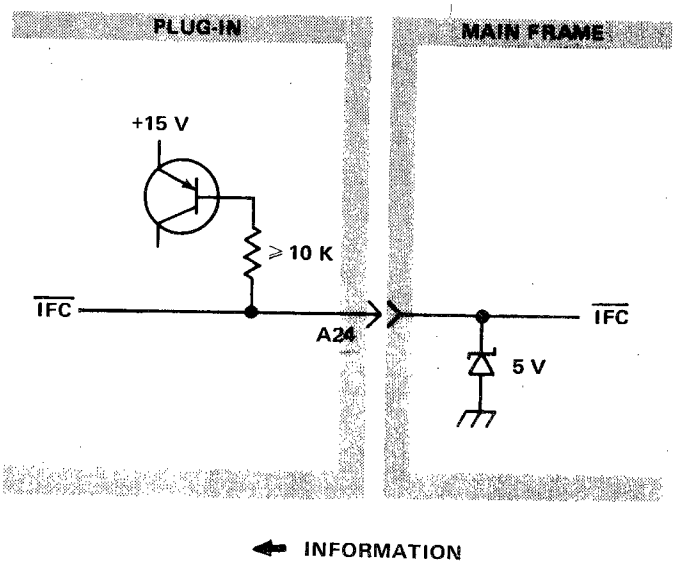
A24

$\overline{\text{IFC}}$ (Interface Clear)

Bus management signal for programmable plug-ins. This is a TTL signal specified in IEEE Standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
A24	$\overline{\text{IFC}}$	IFC (interface clear) is used to place the interface system, portions of which are contained in all interconnected devices, in a known quiescent state.

This line is also used by the Main Frame to indicate to the plug-ins that it is programmable. A non-programmable Main Frame makes no connection to A24.



A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in system controller must be able to sink 24 mA at 0.4 V.

$\overline{\text{ATN}}$ (Attention)

Bus management signal for programmable plug-ins. This is a TTL signal specified in IEEE Standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
B24	$\overline{\text{ATN}}$	ATN (attention) is used to specify how data on the DIO signal line is to be interpreted and which devices must respond to data.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in controller must be able to sink 24 mA at 0.4 V.

A25

$\overline{\text{NDAC}}$ (Not Data Accepted)

Handshake signal for programmable plug-ins. This is a TTL signal specified in IEEE Standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
A25	$\overline{\text{NDAC}}$	NDAC (not data accepted) is used to indicate the condition of acceptance of data by device(s).

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in must be able to sink 24 mA at 0.4 V.

$\overline{\text{NRFD}}$ (Not Ready for Data)

Handshake signal for programmable plug-ins. This is a TTL signal specified in IEEE Standard 488-1975 and is part of the General Purpose Interface Bus (GPIB). Refer to the section on Programming for specifications.

Pin Number	Signal Name	Description
B25	$\overline{\text{NRFD}}$	NRFD (not ready for data) is used to indicate the condition of readiness of device(s) to accept data.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in must be able to sink 24 mA at 0.4 V.

A26

LOGIC COMMON

Provides a common ground return for logic signals.

$\overline{\text{SND}}$ (Send)

A TTL signal used by the plug-ins or main frame to indicate to the GPIB Source Handshake function in the main frame, that the device has a valid byte on the internal main frame data bus which should be transmitted by the main frame Source Handshake function.

When $\overline{\text{SND}}$ is asserted, the other plug-ins must disable their diode-logic-data-bus receivers, since the diode logic used restricts a plug-in to driving the main frame load only.

A plug-in may place one standard TTL and one LSTTL input on the line.

To drive the line low, a plug-in must be able to sink 24 mA at 0.4 V.

−5 V POWER

Power for programmable plug-ins.

Maximum current available to plug-ins is 0.5 amp per plug-in.

Each plug-in is limited to 25 watts total power consumption.

Initial Accuracy: ±1%.

Drift Per Year: 0.5%.

Total Ripple: 1 mV p-p.

Current fold-back protection.

+5.1 VOLTS POWER

Power for the plug-in logic circuits.

Maximum available current is 2 amp per plug-in.

Each plug-in is limited to 25 watts total power consumption.

Adjustable to ±1% initially.

Drift Per Year: ±1%.

Total Ripple: 10 mV p-p.

Inverter shut-down protection.

A28

INTERPLUG-IN COMMUNICATIONS

Interplug-in Communications, A27 and A28, were provided in the original 7000-series instruments. Because of lack of usage, they were modified out of later instruments.

A28 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of A28 allowed several contacts to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused readout IC failures.

INTERPLUG-IN COMMUNICATIONS

Interplug-in Communications Lines, B26, B27,and B28, were provided in the original 7000-series instruments. Because of a lack of usage, they were modified out of later instruments.

B28 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of B28 allowed several pins to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused Readout IC failures.

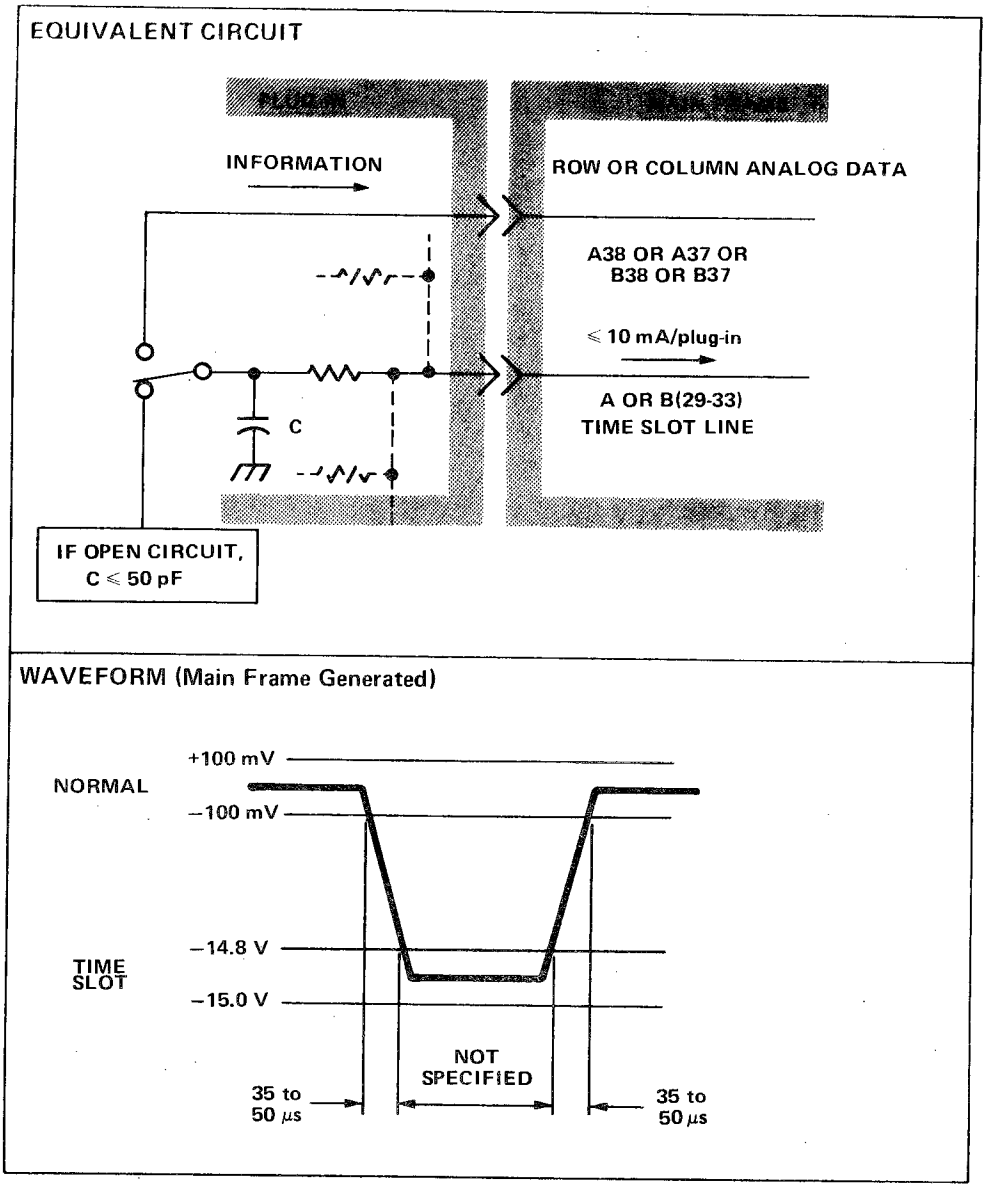
A29 A30 A31 A32 A33

TIME SLOT PULSE LINES NOS. 1 - 10

Time Slot Pulse Lines, A29-A33 and B29-B32 supply time slot #1-10 pulses to the plug-ins. Each time slot pulse encodes one character per word, and the ten pulses sequence at a fixed rate of approximately 4 kHz even when the readout is disabled at the main frame front panel, or when the readout is in its single sweep mode (except in the 7704A). The repetition rate of time slot #1-10 is 400 Hz. Frame rate is approximately 50 hertz.

For additional details of Word Scan Line Time Slots, refer to section on Readout.

For details on programmable instrument use of the time slot lines, refer to the section on Programming.



B29 B30 B31 B32 B33

TIME SLOT PULSE LINES

See A29 information.

A34

DVM LINE

A34 was originally used as the DVM line for the proposed two dot measuring system. This system has been deleted.

A34 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of A34 allowed several pins to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused Readout IC failures.

DVM COMMON LINE

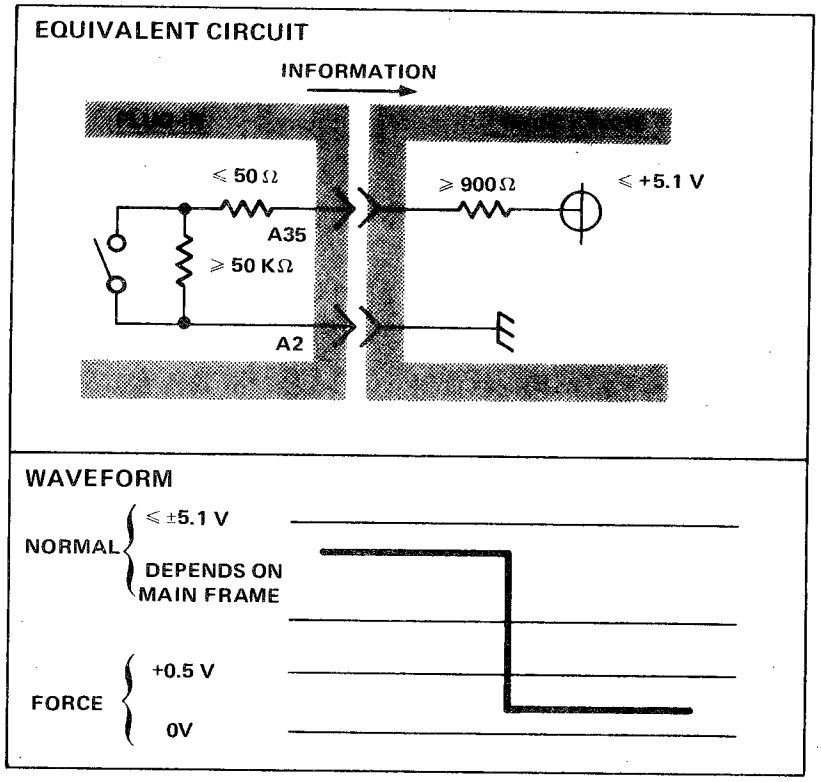
B34 was originally used as the DVM Common Line for the proposed 2-dot measuring system. This sytem has since been deleted.

B34 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of B34 allowed several pins to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused Readout IC failure.

A35

FORCE READOUT

Force Readout, A35, allows plug-in readout information to be displayed regardless of the Main Frame Mode switch setting.



PLUG-IN MODE

Plug-In Mode, B35, supplies the Main Frame with analog voltages to identify the operating mode of the dual-trace or dual-sweep plug-in.

The voltage levels below can be derived three different ways:

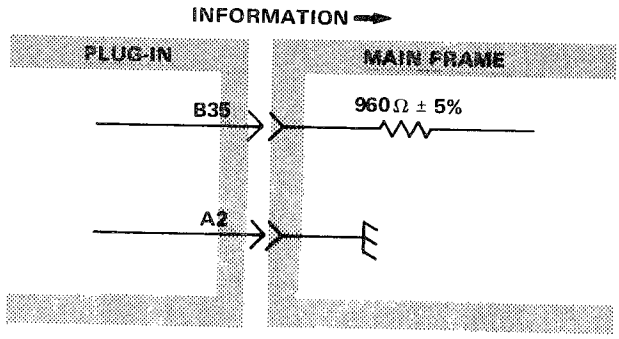
(1) Voltage drive.

(2) Current drive (0-5.2 mA).

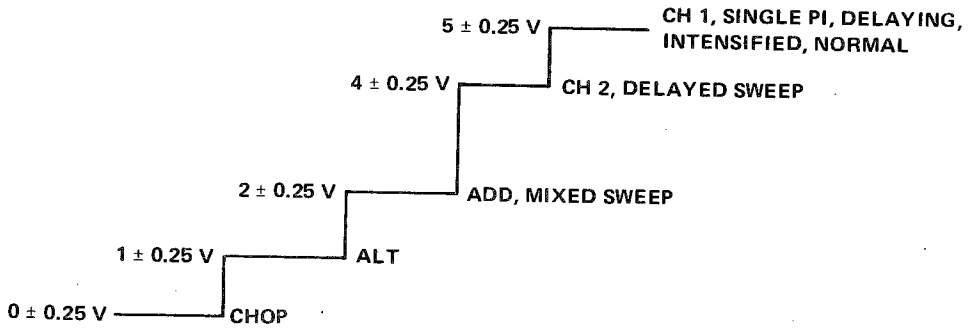
(3) Resistance to ground.

PLUG-IN MODE	RESISTANCE
Chop	0 to 47Ω ± 5%
Alt	240Ω ± 5%
Add, Mixed	620Ω ± 5%
CH 2, Delayed	3.9 KΩ ± 5%
CH 1, Intensified, Normal, Delaying	⩾30 KΩ

EQUIVALENT CIRCUIT



WAVEFORM



A36

TRUE TIME INDICATOR

A36 was originally used as the True Time Indicator line for the proposed two dot measuring system. This system has been deleted.

A36 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of A36 allowed several pins to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused Readout IC failures.

B36

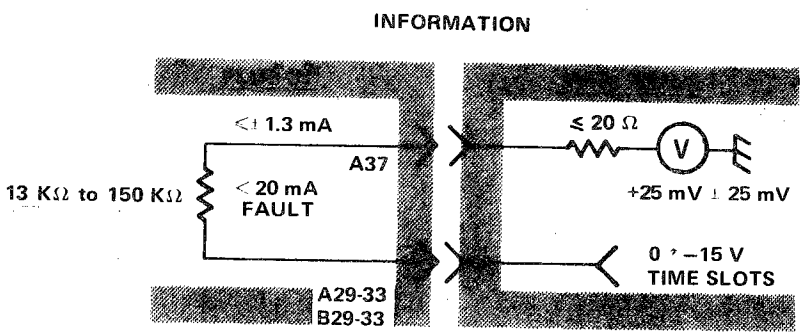
B36 was physically removed (left blank) from the plug-in and the Main Frame connector. It was found that the presence of B36 allowed several pins to be shorted together when the plug-in was mis-aligned during insertion. This contact shorting sometimes caused Readout IC failures.

A37

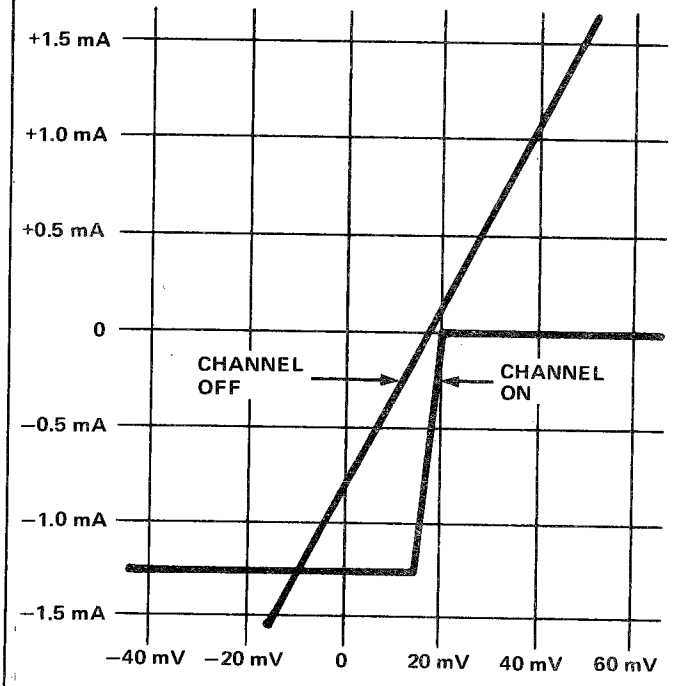
CH 1 COLUMN ANALOG DATA

CH 1 Column Analog Data provides ten or more discrete current levels from the plug-ins to the Main Frame Readout circuitry. This information with the Time-Slot Logic (A29-33 and B29-33) provides the Main Frame with plug-in scale factor readout information.

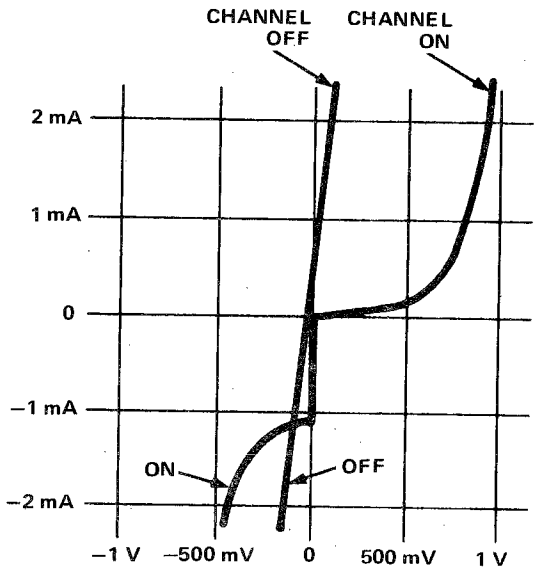
EQUIVALENT CIRCUIT



A37 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



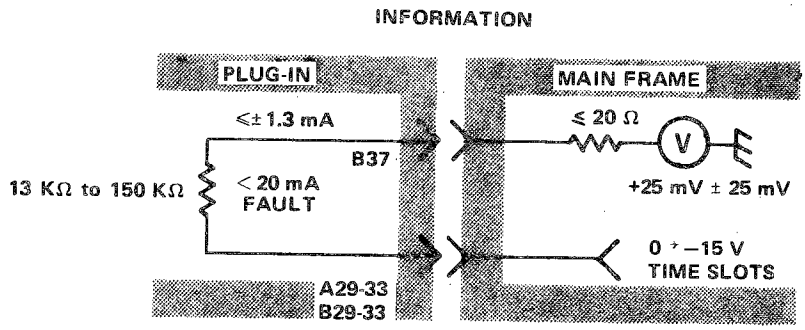
A37 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



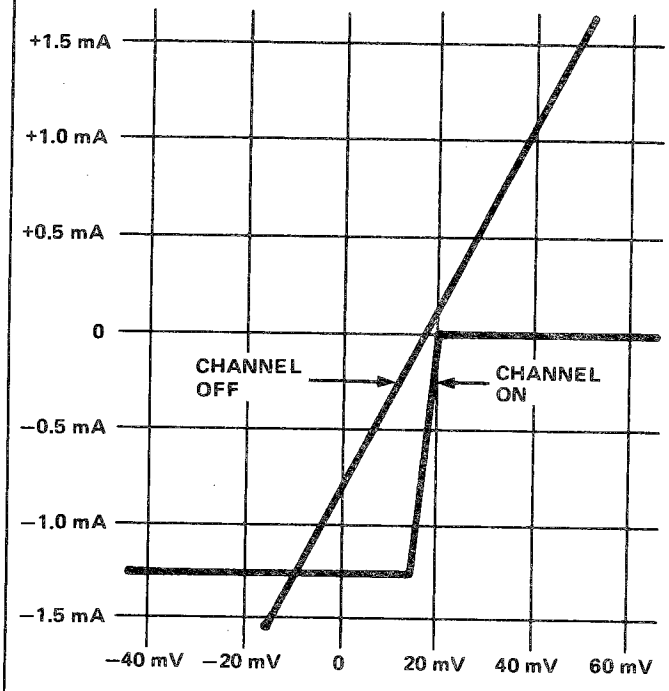
CH 1 ROW ANALOG DATA

CH 1 Row Analog Data provides ten or more discrete current levels from the plug-ins to the Main Frame Readout circuitry. This information with the Time-Slot Logic (A29-33 and B29-33) provides the Main Frame with plug-in scale factor readout information.

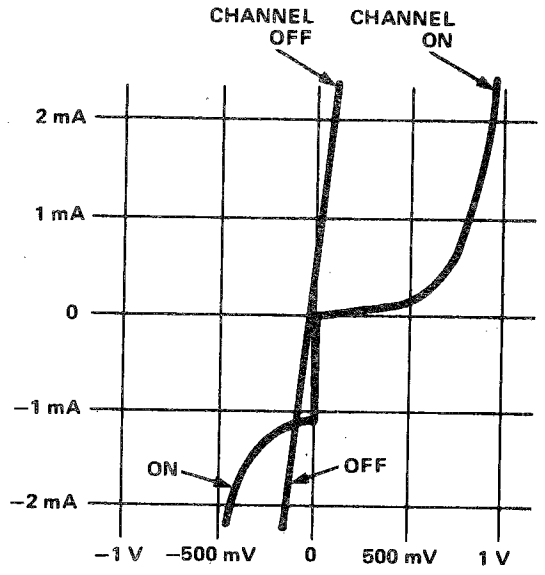
EQUIVALENT CIRCUIT



B37 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



B37 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER

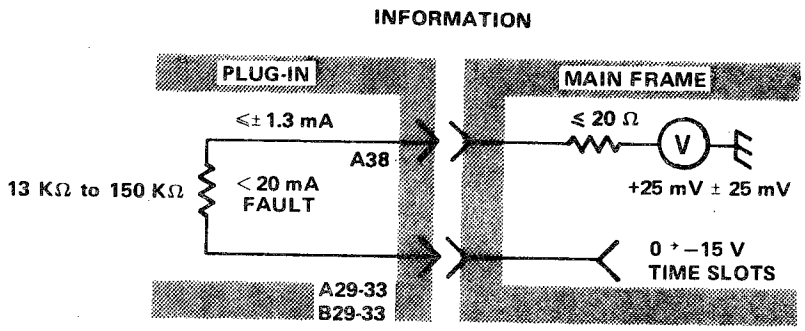


A38

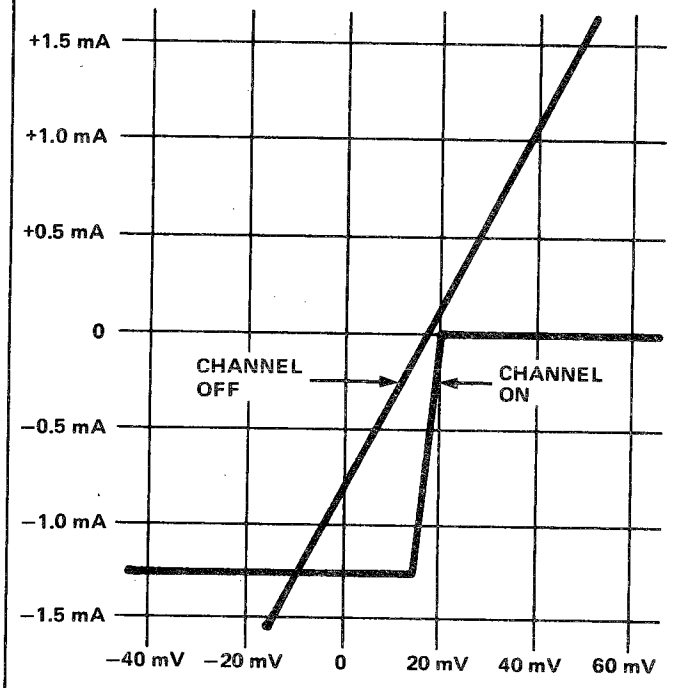
CH 2 COLUMN ANALOG DATA

CH 2 Column Analog Data provides ten or more discrete current levels from the plug-ins to the Main Frame Readout circuitry. This information with the Time-Slot Logic (A29-33 and B29-33) provides the Main Frame with plug-in scale factor readout information.

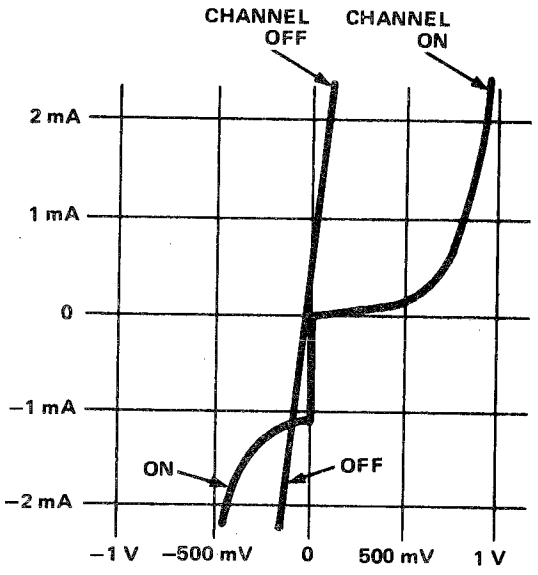
EQUIVALENT CIRCUIT



A38 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



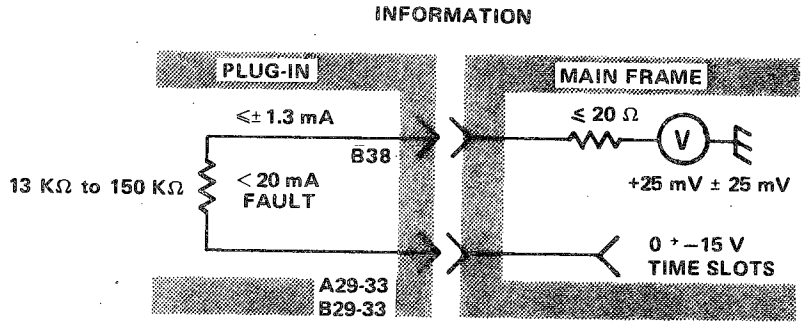
A38 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



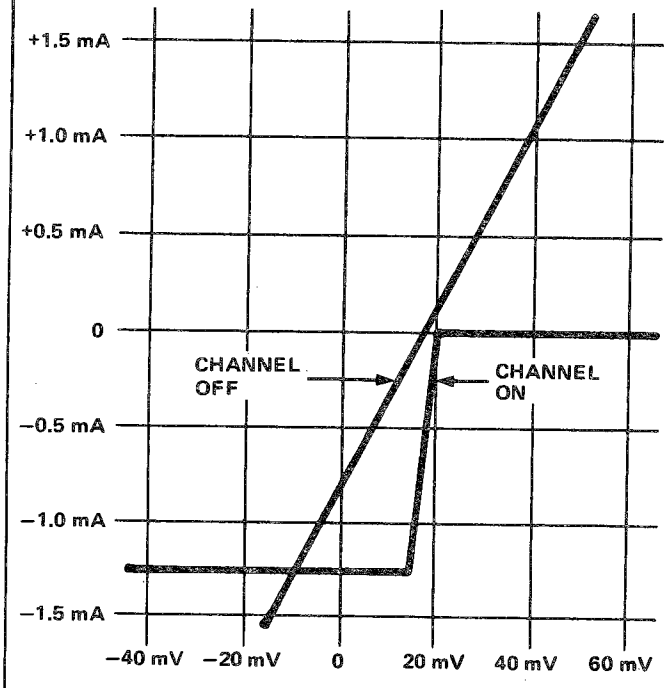
CH 2 ROW ANALOG DATA

CH 2 Row Analog Data provides ten or more discrete current levels from the plug-ins to the Main Frame Readout circuitry. This information with the Time-Slot Logic (A29-33 and B29-33) provides the Main Frame with plug-in scale factor readout information.

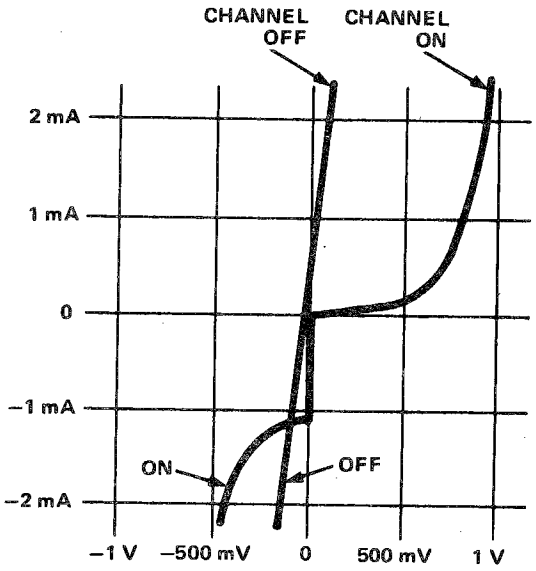
EQUIVALENT CIRCUIT



B38 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



B38 TYPICAL WAVEFORM DRIVING PIN WITH CURVE TRACER



LOGIC CIRCUIT

The Logic Circuit develops control signals for use in other circuits within this instrument. These output signals automatically determine the correct instrument operation in relation to the plug-ins installed or selected, plug-in control settings, and 7704A control settings. A block diagram of the Logic Circuit is shown in Figure 2. This diagram shows the source of the input control signals, the output signals produced by this stage, and the basic interconnections between blocks. The interconnections shown are intended only to indicate inter-relation between blocks and neither indicate a direct connection, nor that only a single connection is made between the given blocks. Details of the inter-relation between stages in this circuit are given in the circuit description which follows.

This circuit description for the Logic Circuit is written with the approach that each of the integrated circuits and its associated discrete components composes an individual stage as shown by the block diagram (Figure 2). The operation of each of these stages is discussed, relating the input signals or levels to the output, with consideration given to the various modes of operation that may affect the stage. A logic diagram is also provided for each stage. These diagrams are not discussed in detail, but are provided to aid in relating the function performed by a given stage to standard logic techniques. It should be noted that these logic diagrams are not an exact representation of the internal structure of the integrated circuit, but are only a logic diagram of the function performed by the stage. An input/output table is given, where applicable, for use along with the circuit description and logic diagram. These input/output tables document the combination of input conditions that are of importance to perform the prescribed function of an individual stage.

Horizontal Logic

The Horizontal Logic stage performs these seperate logic functions: A Sweep Lockout, B Sweep Lockout, and Alternate Pulse Generator. Figure 1 identifies the three individual stages and the input and output terminals associated with each. Notice that some of the input signals are connected internally to more than one of the individual stages.

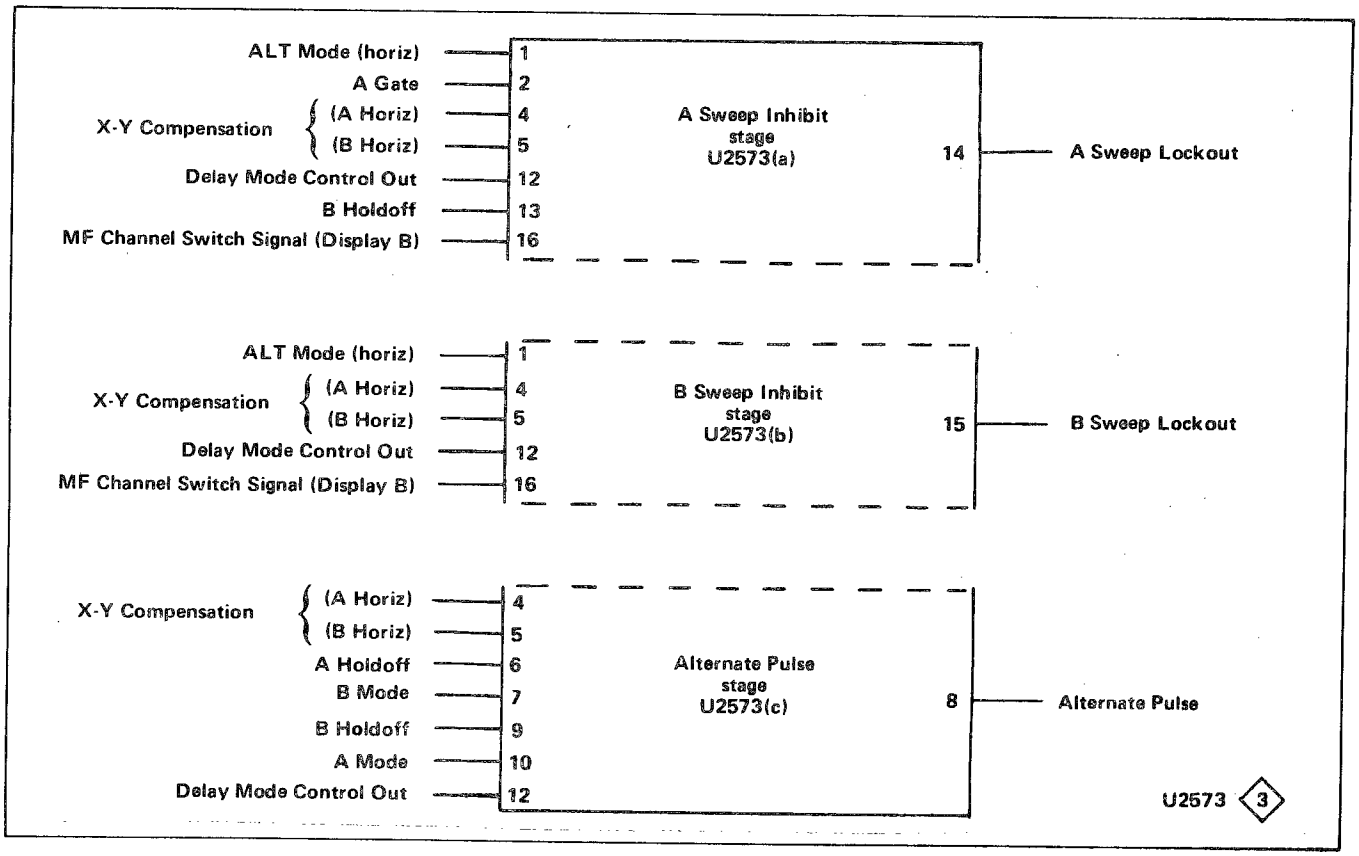


Figure 1. Breakdown of separate stages within Horizontal Logic IC (U2573) showing inputs and outputs for each stage.

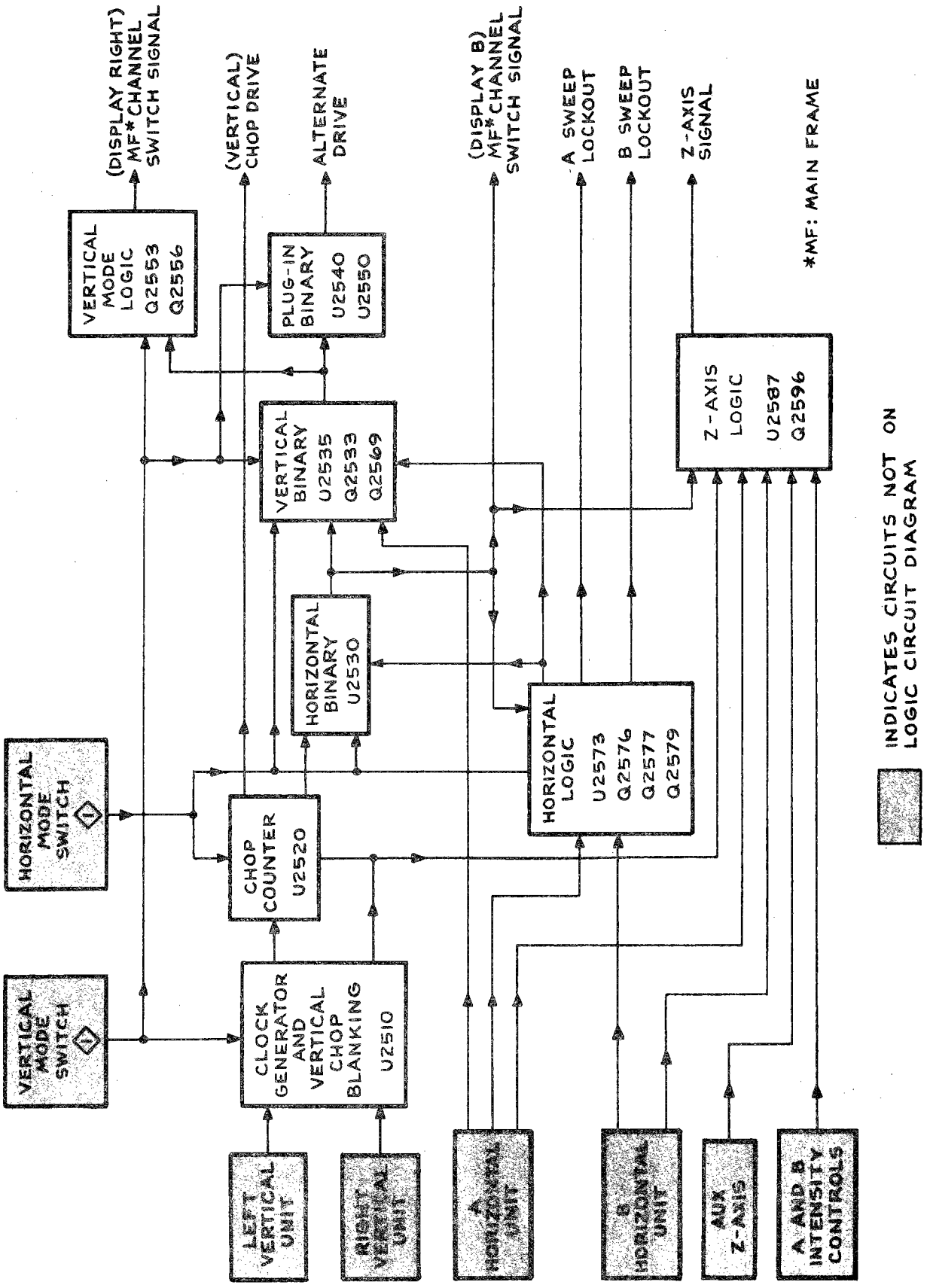


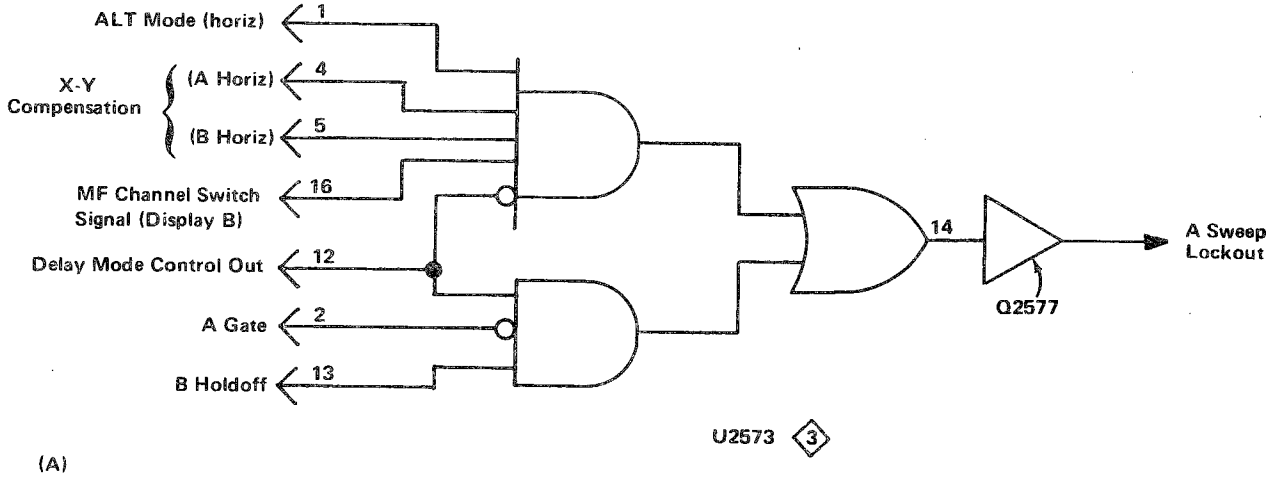
Figure 2. Block diagram of Logic Circuit.

A Sweep Lockout. The A Sweep Lockout stage produces an output level at the collector of Q2577 that determines if the A HORIZ time-base unit can produce a sweep. If this output is HI, the A HORIZ unit is locked out (disabled) so it cannot produce a sweep. If the level is LO, the A HORIZ unit is enabled and can produce a sweep when triggered.

As shown by the logic diagram and input/output table of Figure 3, only two combinations of input conditions produce an A Sweep Lockout level (HI); if any one of the prescribed conditions is not met, the A Sweep Lockout level is LO and the A HORIZ time-base unit is enabled.

The first combination disables the A sweep while the B sweep is being displayed in the ALT horizontal mode (both units must be in time-base mode) if non-delayed operation is being used. The second combination disables the A sweep during delayed-sweep operation so that the B sweep can complete its holdoff before the next A sweep begins.

B Sweep Lockout. The B Sweep Lockout stage produces an output level at the collector of Q2579 that determines if the B HORIZ time-base unit can produce a sweep. A HI output level locks out (inhibits) the B HORIZ unit and a LO level enables the B HORIZ unit to produce a sweep.



(A)

Input							Output
ALT Mode (horiz)	A Gate	X-Y Compensation: A Horiz	X-Y Compensation: B Horiz	Delay Mode Control Out	B Holdoff	MF Channel Switch Signal (Display B)	A Sweep Lockout
1	2	4	5	12	13	16	
HI	Φ	HI	HI	LO	Φ	HI	HI
Φ	LO	Φ	Φ	HI	HI	Φ	HI
All other combinations							LO

(B)

Φ = Has no effect in this case.

Figure 3. (A) Logic diagram for A Sweep Lockout stage; (B) Table of input/output combinations.

As shown by Figure 4B, the output of this stage is HI only under one set of input conditions. This set of conditions disables the B sweep while the A sweep is being displayed in the ALT horizontal mode if both units are in a time-base mode and non-delayed sweep is used. For any other combination of input conditions, the B Sweep Lockout level is LO. However, the lockout level to the B time-base unit is determined by both the Delay Gate from the A time-base unit and the B Sweep Lockout level produced by this stage. The B sweep is enabled only when both of these levels are LO.

Figure 4A shows the logic diagram of the B Sweep Lockout stage. The gate connected to the output of this stage is a phantom-OR gate located on the Main Interface diagram (a phantom-OR gate performs the OR-logic function merely by interconnection of the two signal lines).

Alternate Pulse Generator. The third function performed by the Horizontal Logic stage is to produce an Alternate Pulse signal for use by the Horizontal and Vertical Binary stages. The Alternate Pulse is produced at the end of either sweep, depending upon the operating conditions as shown in Figure 5B. The holdoff gate produced at the end of the sweep by the respective time-base unit is differentiated by either C2575 or C2573 to provide a positive-going pulse to pin 6 or 9.

In Figure 5A, note the resistors shown connected to pins 6 and 9. These resistors, which are internal to the IC, hold the levels at pins 6 and 9 LO unless a HI level is applied to the corresponding input. Since the holdoff gate is capacitively-coupled to pins 6 and 9, these inputs are at the LO level except when a differentiated A or B Holdoff gate is received.

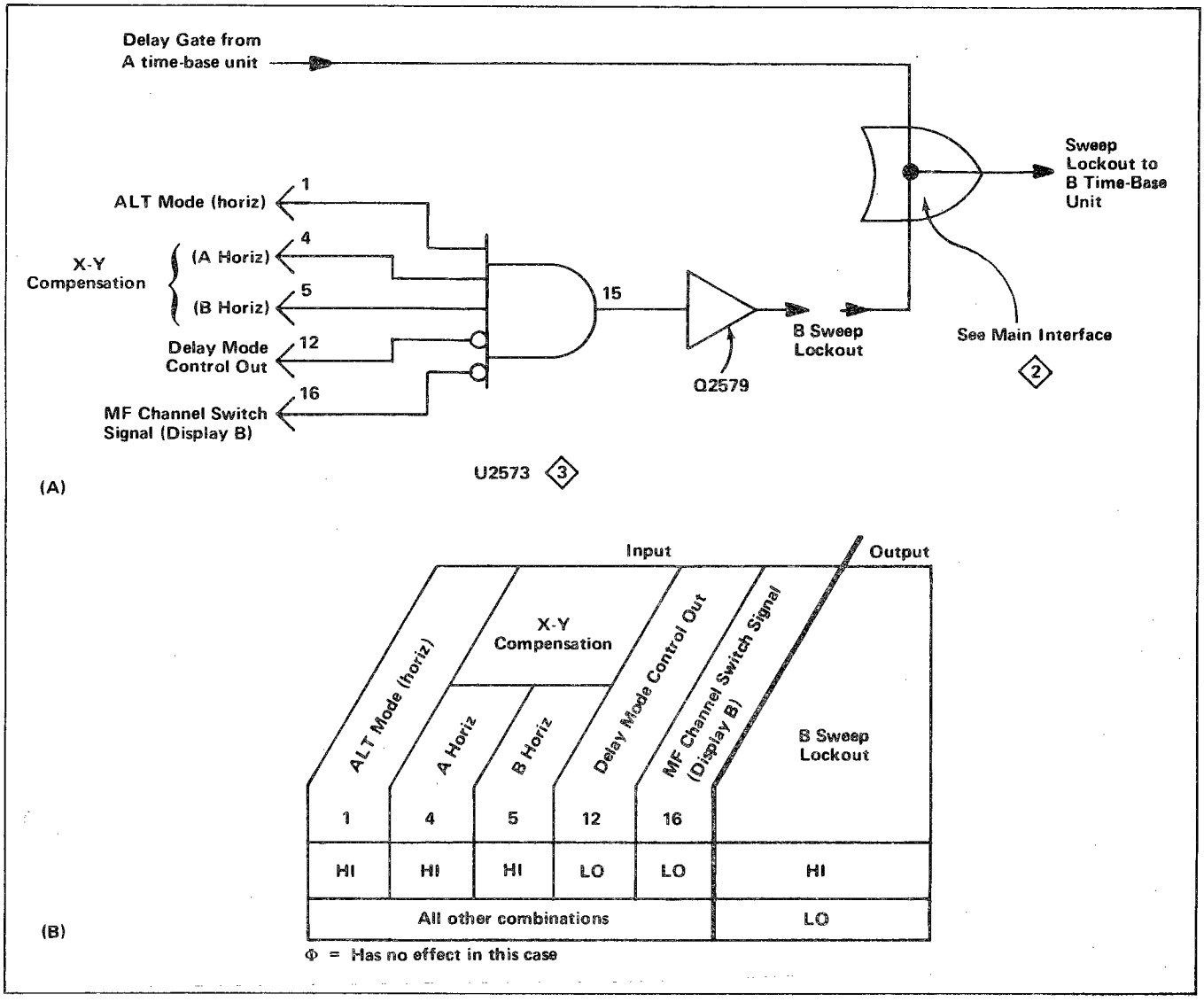
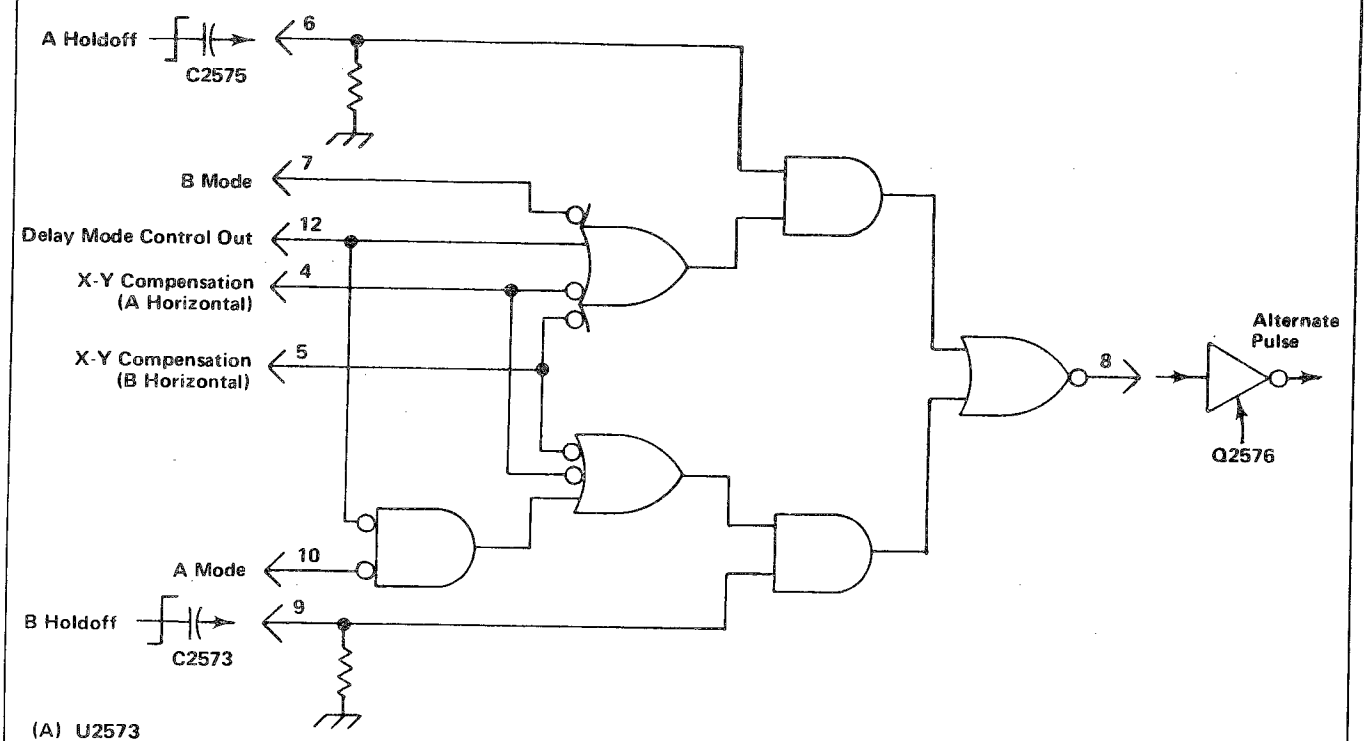


Figure 4. (A) Logic diagram for B Sweep Lockout stage; (B) Table of input/output combinations.



(A) U2573

Input							Output	
X-Y Compensation (A Horizontal) 4	X-Y Compensation (B Horizontal) 5	A Holdoff 6	B Mode 7	B Holdoff 9	A Mode 10	Delay Mode Control Out 12	Time-Base which is source of Alternate Pulse 8[2]	Horizontal Conditions
HI	Φ	HI[1]	LO	Φ	HI	Φ	A	A only
Φ	HI	Φ	HI	HI[1]	LO	LO	B	B only
HI	HI	HI[1]	LO	HI[1]	LO	LO	A and B	ALT or CHOP
HI	HI	HI[1]	Φ	Φ	Φ	HI	A	A delays B
HI	LO	HI[1]	LO	LO	Φ	Φ	A	A with amplifier unit in B compartment.
LO	HI	LO	Φ	HI[1]	LO	LO	B	B with amplifier unit in A compartment.
All other combinations							No output pulse (LO at output)	

Φ = Has no effect in this case

[1] Positive-going pulse. Where both A and B Holdoff are required to be HI, a HI at either input produces an Alternate Pulse.

[2] Negative-going pulse.

(B)

Figure 5. (A) Logic diagram for Alternate Pulse Generator stage; (B) Table of input/output combinations.

The following discussions describe the operation of the Alternate Pulse Generator stage in relation to the various combinations of input conditions shown in Figure 5B.

1. A (ONLY) MODE

An Alternate Pulse is produced at the end of each A sweep when the HORIZONTAL MODE switch is set to the A position.

2. B (ONLY) MODE

In the B position of the HORIZONTAL MODE switch, an Alternate Pulse is produced at the end of each B sweep (A time-base must be in independent, non-delayed mode).

3. ALT OR CHOP MODE

When the HORIZONTAL MODE switch is set to ALT or CHOP (A time-base unit must be in independent, non-delayed mode), an Alternate Pulse is produced at the end of each sweep. For example, an Alternate Pulse is produced at the end of the A sweep, then at the end of the B sweep, again at the end of the A sweep, etc. Although Alternate Pulses are produced in the CHOP horizontal mode, they are not used in this instrument.

4. DELAYED SWEEP (A DELAYS B)

When the A time-base unit is set for delayed operation, the operation of the Alternate Pulse Generator is changed so an Alternate Pulse is produced only at the end of the A sweep, even when the HORIZONTAL MODE switch is set to B. This is necessary since the A time-base establishes the amount of delay time for the B time-base unit whenever it is displayed.

5. AMPLIFIER UNIT IN HORIZONTAL COMPARTMENT

When an amplifier unit is installed in either of the horizontal plug-in compartments, the Alternate Pulse can be produced only from the remaining time-base unit. If amplifier units are installed in both horizontal compartments, an Alternate Pulse is not produced since there are no time-base units to produce a holdoff pulse.

Z-Axis Logic

The Z-Axis Logic stage produces an output current which sets the intensity of the display on the CRT. The level of this output current is determined by the setting of the A or B INTENSITY controls, by a current added to provide an intensified zone on the A sweep for delayed-sweep operation, or by an external signal. The input current from the A and B INTENSITY controls is switched so that the output current matches the horizontal display. The Chopped Blanking signals are applied to this stage to block the output current and blank the CRT display for vertical and horizontal chopping.

Figure 6 identifies the inputs to the Z-Axis Logic IC, U2587. This IC (integrated circuit) is current-driven at all inputs except pins 5 and 15. The current at pins 1, 2, 9, and 16 is variable from zero to four milliamperes and is determined by the applicable current source to control the output current at pin 8.

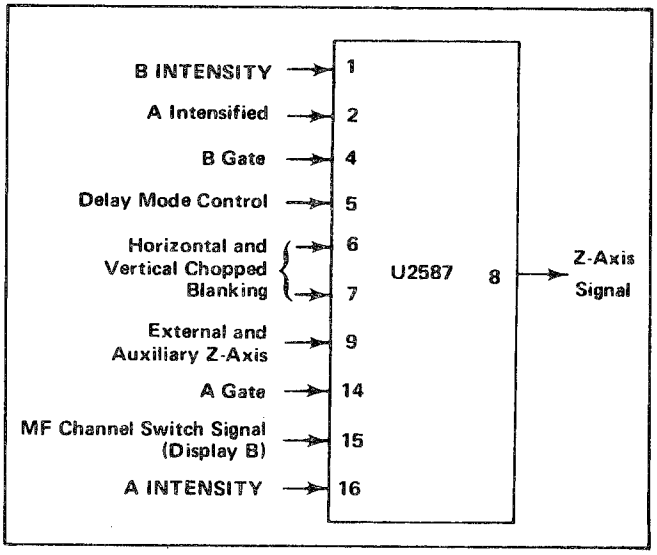
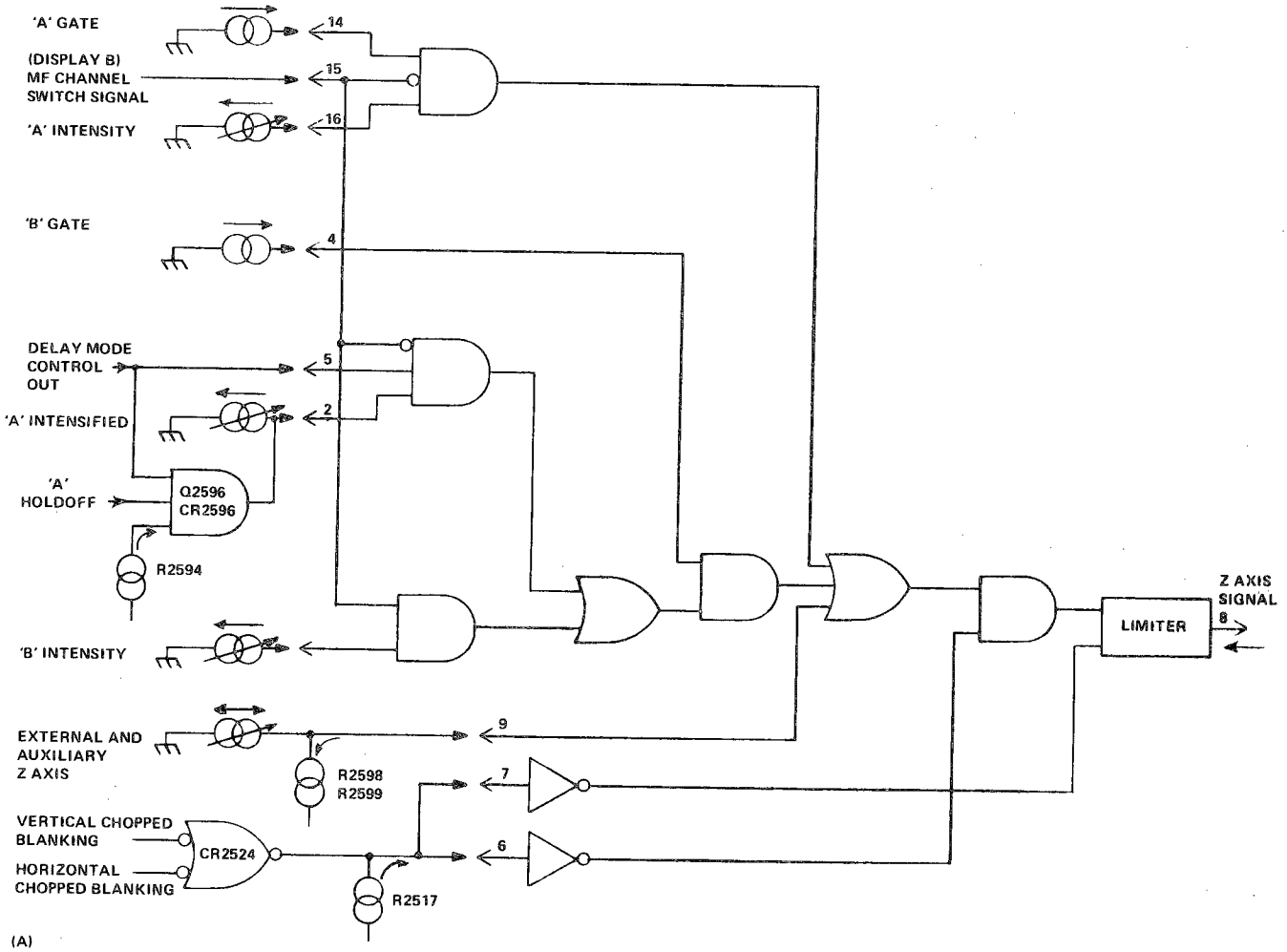


Figure 6. Input and output pins for Z-Axis Logic IC.

The Chopped Blanking signal connected to pins 6 and 7 enables or disables this stage to control all output current. Quiescently, the level at pins 6 and 7 is HI so that the intensity current from pins 1, 2, 9, and 16 can pass to the output. However, pins 6 and 7 go LO during Vertical Chopped Blanking or Horizontal Chopped Blanking. This blocks the output current and the CRT is blanked. The Vertical Chopped Blanking signal is connected directly to U2587 from pin 4 of U2510. The Horizontal Chopped Blanking is connected to U2587 from pin 4 of U2520 through LR2523 and CR2524. CR2524 is normally reverse biased. When the Horizontal Chopped Blanking level goes LO, CR2524 is forward biased to produce a corresponding LO level at pins 6 and 7 of U2573.

The A INTENSITY control sets the output current level when the A Gate at pin 14 is HI and the MF (Main Frame) Channel Switch Signal at pin 15 is LO. The A INTENSITY current is blocked whenever the A Gate level goes LO (indicating that the A sweep is complete), or the MF Channel Switch Signal goes HI (indicating that the B sweep is being displayed). The current from the A INTENSITY control (see diagram 1) is connected to pin 16 through R2587.



(A)

(B)

Input										Output	
A Holdoff	B INTENSITY 1[1]	A Intensified 2[1]	B Gate 4	Delay Mode Control Out 5	Vertical or Horizontal Chopped Blanking Inhibit 6	External and Auxiliary Z Axis 9[1]	A Gate 14	MF Channel Switch Signal 15	A INTENSITY 16[1]	Z-Axis Signal 8[1]	Current source controlling Z-Axis Signal
Φ	Φ	Φ	Φ	LO	HI	Φ[2]	HI	LO	HI	HI	A INTENSITY
Φ	HI	Φ	HI	Φ	HI	Φ[2]	Φ	HI	Φ	HI	B INTENSITY
LO	Φ	HI	HI	HI	HI	Φ[2]	HI	LO	HI	HI	A INTENSITY and A Intensified
Φ	Φ	Φ	Φ	Φ	HI	HI	Φ	Φ	Φ	HI	External signal
	All other combinations									LO	No output signal

LO = Minimum voltage or current.

HI = Maximum voltage or current.

Φ = Has no effect in this case

[1] Current level. LO = 0 mA
HI = Variable from 0 to 4 mA

[2] Current can be added or subtracted for intensity modulation.

Figure 7. (A) Logic diagram for Z-Axis Logic stage; (B) Table of input/output combinations.

Logic Circuit

In the delayed mode, current is added to the A INTENSITY current during the A sweep time to intensify a portion of the trace. This intensified portion is coincident with the B-sweep time to provide an indication of the portion of the A sweep that is displayed in the delayed mode. The A Intensified current is supplied to pin 2 of U2587 from the A INTENSITY control through R2586. With this configuration, the intensified current increases as the A INTENSITY control setting is advanced to provide a proportional intensity increase in the intensified zone as the overall A-sweep intensity increases. Therefore, the intensified zone is more readily visible at high intensity levels. The intensified current is added to the A INTENSITY current to produce an intensified zone on the A sweep under the following conditions: HI A Gate level at pin 14, LO MF Channel Switch Signal at pin 15, HI B Gate level at pin 4, HI Delay Mode Control Out level at pin 5 and the base of Q2596, and LO A Holdoff level at the emitter of Q2596.

The B INTENSITY control determines the output current when the B Gate level at pin 4 and the MF Channel Switch Signal at pin 15 are both HI. The current from the B INTENSITY control (see diagram 1) is connected to the Z-Axis Logic stage through R2588.

The current level established by the intensity controls can be altered by the External and Auxiliary Z-Axis current level at pin 9. The current at this pin can come from the Z AXIS INPUT connector on the rear panel through R2092 or from any of the plug-in compartments through R2090, R2080, R2012, or R2010 (see diagram 2). This current either increases or decreases (depending on polarity) the output current to modulate the intensity of the display. Input from the Z AXIS INPUT connector allows the trace to be modulated by external signals. The auxiliary Z-Axis inputs from the plug-in compartments allow special purpose plug-in units to modulate the display intensity. Diodes CR2585 and CR2594 limit the maximum voltage change at pin 9 to about + and −0.6 volt to protect the Z-Axis Logic stage if an excessive voltage is applied to the Z AXIS INPUT connector.

Figure 7A shows a logic diagram of the Z-Axis Logic stage. Notice the current-driven inputs as indicated by the current-generator symbols at the associated inputs. An input/output table for the Z-Axis Logic stage is given in Figure 7B.

Horizontal Binary

The MF (Main Frame) Channel Switch Signal (Display B) produced by the Horizontal Binary stage determines which horizontal unit provides the sweep display on the CRT. When this level is HI, the B HORIZ unit is displayed; when it is LO, the A HORIZ unit is displayed.

The MF Channel Switch Signal (Display B) is used in the following stages within the Logic Circuit: Horizontal Logic (for A and B Sweep Lockout), Z-Axis Logic (for blanking), and Vertical Binary (to synchronize vertical alternate switching with horizontal alternate switching). In addition, this signal is connected to the following circuits elsewhere in the instrument: Main Interface (to indicate which horizontal unit is to be displayed), Vertical Interface (for trace separation), and Horizontal Interface (for horizontal channel selection).

Notice that the levels at pins 3, 4, 7, and 10 are determined by the HORIZONTAL MODE switch (see diagram 1). This switch determines which horizontal mode has been selected by providing a HI level to only one of four output lines (the remaining lines are LO). Therefore, at any one time, either pin 3, pins 4 and 7 (notice that pins 4 and 7 are tied together), or pin 10 can be HI and the two unselected lines from the HORIZONTAL MODE switch remain LO.

The Horizontal Binary stage operates as follows for each position of the HORIZONTAL MODE switch (refer to Figure 8B for input/output conditions):

1. A MODE

When the HORIZONTAL MODE switch is set to A, the MF Channel Switch Signal (Display B) is LO to indicate to all circuits that the A HORIZ unit is to be displayed.

2. B MODE

Selecting the B horizontal mode provides a HI MF Channel Switch Signal (Display B) to all circuits.

3. CHOP MODE

In the CHOP position of the HORIZONTAL MODE switch, the MF Channel Switch Signal (Display B) switches between the HI and LO levels to produce a display that switches between the A HORIZ and B HORIZ units at a 200-kHz or 20-kHz rate, as selected by S2510. The repetition rate of the MF Channel Switch Signal (Display B) in this mode is determined by the Horizontal Chopped Blanking pulse (see Chop Counter description). Each time the Horizontal Chopped Blanking pulse at pin 1 drops LO, the output at pin 6 switches to the opposite state.

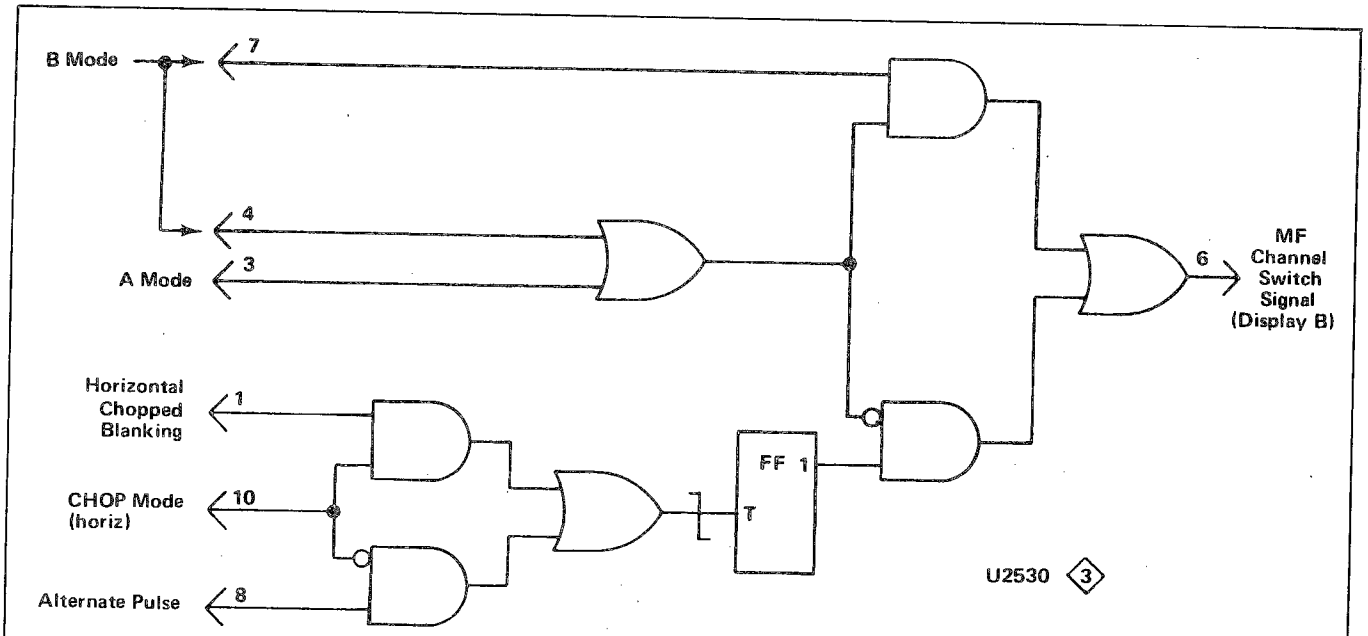
4. ALT MODE

For ALT horizontal operation, the MF Channel Switch Signal (Display B) switches to the opposite state each time the negative portion of the Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the MF Channel Switch Signal (Display B) in this mode is one-half the repetition rate of the Alternate Pulse applied to pin 8.

Figure 8A shows a logic diagram of the Horizontal Binary stage. An input/output table showing the conditions for each position of the HORIZONTAL MODE switch is shown in Figure 8B.

Vertical Binary

The Vertical Binary stage produces the Display Right Command to determine which vertical unit is to be displayed on the CRT. When this output level is HI, the RIGHT VERT unit is displayed and when it is LO, the LEFT VERT unit is displayed. In the ALT or CHOP positions of the HORIZONTAL MODE switch (non-delayed operation only), the output of this stage is slaved to the output of the Horizontal Binary stage so that the Display Right Command is always HI when the MF (Main Frame) Channel Switch Signal (Display B) is LO, and vice versa. This action allows sweep-slaving operation in the ALT position of the VERTICAL MODE switch and the ALT or CHOP positions of the HORIZONTAL MODE



(A)

Input						Output	
Horizontal Chopped Blanking	A Mode	B Mode	B Mode	Alternate Pulse	CHOP Mode (horiz)	MF Channel Switch Signal (Display B)	
1	3	4	7	8	10	6	Horizontal Display
Φ	HI	LO	LO	Φ	LO	LO	A Horizontal unit
Φ	LO	HI	HI	Φ	LO	HI	B Horizontal unit
LO[1]	LO	LO	LO	Φ	HI	n+1[2]	Chop between A and B
Φ	LO	LO	LO	LO[1]	LO	n+1[3]	Alternate between A and B

Φ = Has no effect in this case

n+1 = If output is LO prior to LO[1], it goes HI, and vice versa

[1] Actuated by negative-going edge.

[2] Repetition rate one-half Horizontal Chopped Blanking rate.

(B) [3] Repetition rate one-half Alternate Pulse rate.

Figure 8. (A) Logic diagram for Horizontal Binary stage; (B) Table of input/output combinations.

switch, whereby the LEFT VERT unit is always displayed at the sweep rate of the B time-base unit. When the A time-base unit is set to the delayed mode, the repetition rate of the Display Right Command is one-half the repetition rate of the MF Channel Switch Signal (Display B). This results in each vertical unit being displayed first against the A time-base unit (delaying), then the B time-base unit (delayed), before the display is switched to the other vertical unit.

The Display B Command is used in the following stages within the Logic Circuit: Plug-In Binary, Vertical Chopped Blanking, and Vertical Mode Logic. It is also connected to the following circuits elsewhere in the instrument to indicate which vertical unit is to be displayed (through Vertical Mode Logic stage; ALT vertical mode only): Main Interface, Trigger Selector, and Vertical Interface circuits.

The Vertical Binary stage uses the same type of IC as the Horizontal Binary stage. Figure 9 identifies the function of the input pins for U2535. Notice the Display A level at pin 7. This input is the inverse of the MF Channel Switch Signal (Display B) at pin 8. Therefore, the Display A level is always HI when the MF Channel Switch Signal (Display B) is LO, and vice versa. The following discussions describe the operation of the Vertical Binary stage in relation to the modes of operation that can occur.

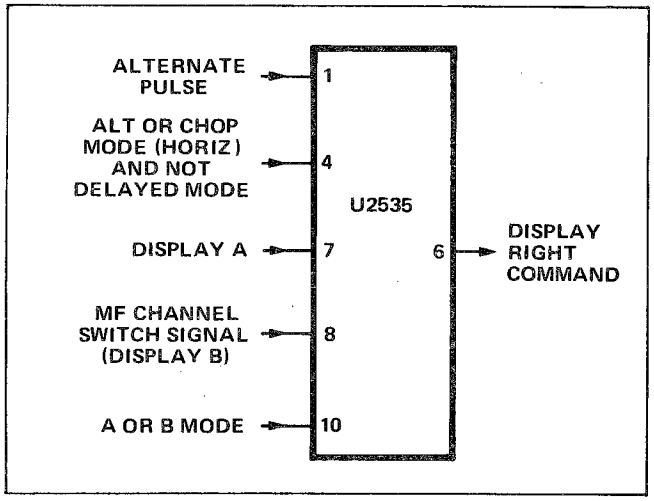


Figure 9. Input and output pins for Vertical Binary IC.

NOTE

Although the output at pin 6 of U2535 is always controlled by the HORIZONTAL MODE switch as described here, this level determines the MF Channel Switch Signal (Display Right) level at the collector of Q2556 only in the ALT position of the VERTICAL MODE switch due to AND gate CR2552-CR2553. See the discussion of the Vertical Mode Logic stage in this section for further information.

1. A OR B MODE

When the HORIZONTAL MODE switch is set to either A or B, the Display Right Command switches to the opposite state each time an Alternate Pulse is received from the Horizontal Logic stage. Repetition rate of the Display Right Command in this mode is one-half the repetition rate of the Alternate Pulse. The input conditions for these modes are:

Pin 1 LO—Alternate Pulse generated by Horizontal Logic stage goes negative.

Pin 4 LO—HORIZONTAL MODE switch in any position except ALT or CHOP, or the A time-base unit is set for delayed sweep.

Pin 10 HI—HORIZONTAL MODE switch set to A or B.

2. ALT OR CHOP MODE (HORIZ)—NON-DELAYED

In the ALT or CHOP positions of the HORIZONTAL MODE switch, the output level at pin 6 is the same as the Display A level at pin 7. The Display A level is produced by inverting the MF Channel Switch Signal (Display B) from the Horizontal Binary stage. Therefore, the repetition rate of the output signal is the same as the MF Channel Switch Signal (Display B). The result, with the VERTICAL MODE switch set to ALT and the A time-base unit set for non-delayed operation, is that the RIGHT VERT unit is always displayed at the sweep rate of the A time-base unit, and the LEFT VERT unit at the sweep rate of the B time-base unit (sweep slaving). The input conditions to provide a HI output level so that the RIGHT VERT unit can be displayed at the A-sweep rate are:

Pin 4 HI—HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

Pin 7 HI—A sweep is to be displayed; MF Channel Switch Signal (Display B) LO.

Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

The input conditions to provide a LO output level so that the LEFT VERT unit can be displayed at the B-sweep rate are:

Pin 4 HI—HORIZONTAL MODE switch set to ALT or CHOP with non-delayed sweep.

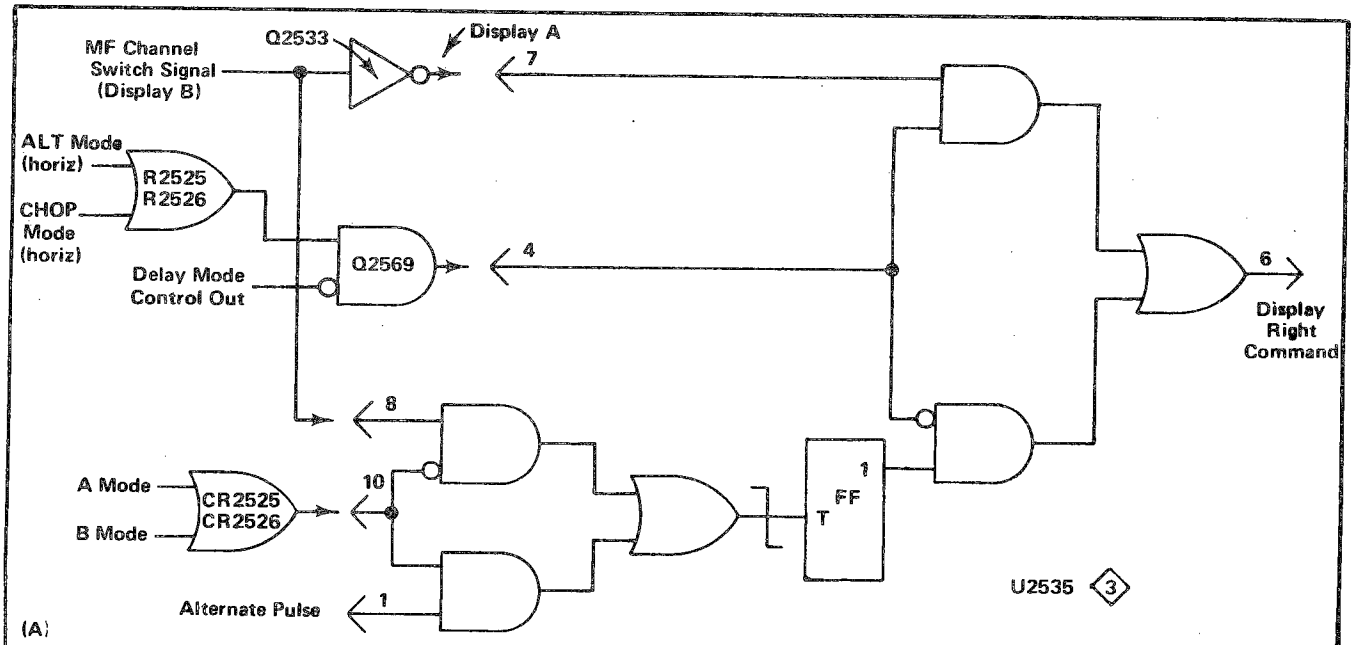
Pin 7 LO—B sweep is to be displayed; MF Channel Switch Signal (Display B) HI.

Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

The Display Right Command switches from HI to LO along with the Display A level at pin 7 (inverse of MF Channel Switch Signal, Display B). However, notice that the Display Right Command changes from HI to LO as the MF Channel Switch Signal (Display B) changes from LO to HI, and vice versa.

3. ALT OR CHOP MODE (HORIZ)–DELAYED

If the A time-base unit is set to the delayed mode when the HORIZONTAL MODE switch is set to either ALT or CHOP, the operation of the stage is changed from that discussed above. Now, the Display Right Command switches between the HI and LO states at a rate that is one-half the repetition rate of the MF Channel Switch Signal (Display B). The resultant CRT display allows the RIGHT VERT unit to be displayed first against the A sweep (delaying) and then against the B sweep (delayed). Then the display switches to the LEFT VERT unit and is displayed consecutively against the A and B sweeps in the same manner. The input conditions for this mode of operation are:



(A)

Input						Output
Alternate Pulse 1	ALT or CHOP Mode (horiz) and not Delayed Mode 4	Display A 7	MF Channel Switch Signal (Display B) 8	A or B Mode 10	Display Right Command 6	Horizontal Mode
LO[1]	LO	Φ	Φ	HI	n+1[2]	A or B
Φ	HI	HI	LO	LO	HI	Display Right — ALT or CHOP, Non-delayed Mode (Sweep-slaving)
Φ	HI	LO	HI	LO	LO	Display Left — ALT or CHOP, Non-delayed Mode (Sweep-slaving)
Φ	LO	Φ	LO[1]	LO	n+1[3]	ALT or CHOP, Delayed Mode

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1] Actuated by negative-going edge.

[2] Repetition rate one-half Alternate Pulse rate.

[3] Repetition rate one-half Display B rate. MF Channel Switch Signal (Display B)

(B)

Figure 10. (A) Logic diagram for Vertical Binary stage; (B) Table of input/output combinations.

Logic Circuit

Pin 4 LO—A time-base unit set for delayed operation.

Pin 8 LO—MF Channel Switch Signal (Display B) generated by Horizontal Binary stage goes negative.

Pin 10 LO—HORIZONTAL MODE switch set to any position except A or B.

A logic diagram of the Vertical Binary stage is shown in Figure 10A. Several logic functions in this stage are performed by logic devices made up of discrete components. The components that make up these logic devices are identified on the Logic diagram. An input/output table for the Vertical Binary stage is given in Figure 10B.

Plug-In Binary

The Plug-In Binary stage produces the Alternate Drive signal to provide a plug-in alternate command to dual-trace plug-in units. This stage uses the same type of IC as the Horizontal Binary and Vertical Binary stages. Figure 11 identifies the function of the input pins for the Plug-In Binary IC, U2540.

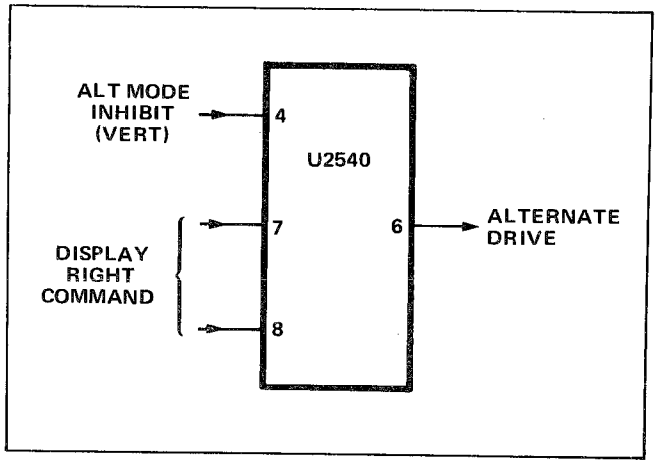


Figure 11. Input and output pins for Plug-In Binary IC.

When the Alternate Drive level is HI and the plug-in unit is set for alternate operation, Channel 2 of the dual-trace unit is displayed. When it is LO, Channel 1 is displayed. The repetition rate of the Alternate Drive output is determined by the setting of the VERTICAL MODE switch. For all positions except ALT, the Alternate Drive level is the same as the Display Right Command from the Vertical Binary stage. Since the Display Right Command was derived directly from the MF (Main Frame) Channel Switch Signal (Display B), this allows the two channels of a dual-trace vertical unit to be slaved to the time-base units (non-delayed, dual-sweep horizontal modes only) in the same manner as previously described for slaving between the vertical and time-base units. The resultant CRT presentation, when the dual-trace unit is set for alternate operation, displays the Channel 1 trace at the sweep rate of the B time-base unit and the Channel 2 trace at the sweep rate of the A time-base unit. Input conditions for a LO output so that Channel 1 of the vertical plug-in can be displayed at the B-sweep rate are:

Pin 4 HI—VERTICAL MODE switch set to any position except ALT.

Pin 7 HI—A sweep to be displayed.

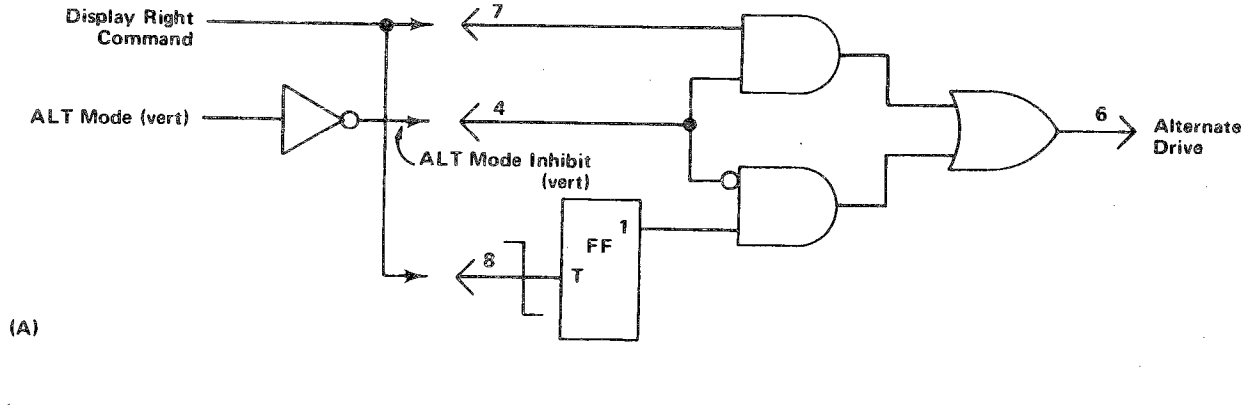
The Alternate Drive switches from HI to LO as the MF Channel Switch Signal (Display B) from the Horizontal Binary stage switches from LO to HI, and vice versa.

When the VERTICAL MODE switch is set to ALT, the Display Right Command from the Vertical Binary stage switches the vertical display between the two vertical units. However, if either of the vertical plug-in units are dual-trace units, they can be operated in the alternate mode also. To provide a switching command to these units, the Plug-In Binary stage produces an output signal with a repetition rate that is one-half the repetition rate of the Display Right Command. The sequence of operation, when two dual-trace vertical units are installed in the vertical plug-in compartments and they are both set for alternate operation, is as follows (VERTICAL MODE and HORIZONTAL MODE switches set to ALT): 1. Channel 1 of LEFT VERT unit at sweep rate of B time-base unit, 2. Channel 1 of RIGHT VERT unit at sweep rate of A time-base unit, 3. Channel 2 of LEFT VERT unit at sweep rate of B time-base unit, 4. Channel 2 of RIGHT VERT unit at sweep rate of A time-base unit. Notice that under these conditions, both channels of the LEFT VERT unit are displayed at the B-sweep rate and that both channels of the RIGHT VERT unit are displayed at the A-sweep rate. The repetition rate at the output of this stage is one-half the Display Right Command rate. Input conditions, when the VERTICAL MODE switch is set to ALT, are:

Pin 4 LO—VERTICAL MODE switch set to ALT.

Pin 8 LO—Display Right Command generated by Vertical Binary stage goes negative.

Figure 12A shows a logic diagram of the Plug-In Binary stage. An input/output table for this stage is shown in Figure 12B.



(A)

Input				Output	
ALT Mode Inhibit (vert) 4	Display Right Command 7	Display Right Command 8	Alternate Drive 6	Comments	
LO	Φ	LO[1]	n+1[2]	ALT Vertical Mode	
HI	LO	Φ	LO	Channel 1 displayed	All vertical modes except ALT, provides sweep-slaving for non-delayed dual-sweep operation.
HI	HI	Φ	HI	Channel 2 displayed	

Φ = Has no effect in this case.

n+1 = If output is LO prior to LO[1] it goes HI, and vice versa.

[1] Actuated by negative-going edge.

(B)

[2] Repetition rate one-half Display Right Command rate.

Figure 12. (A) Logic diagram for Plug-In Binary stage; (B) Table of input/output combinations.

Clock Generator

Part of integrated circuit U2510, along with the external components shown in Figure 13A, make up the Clock Generator stage. R1, Q1, Q2, and Q3 represent an equivalent circuit within U2510. The output at pin 15 is a free-running timing (Clock) signal used to synchronize the vertical, horizontal, and plug-in chopping modes.

The frequency of the Clock signal is either 200 kilohertz or two megahertz, depending on the position of the internal Chop Frequency switch S2510. The 200-kilohertz output is provided for other systems using the A7704 Acquisition Unit (the bottom half of the 7704A). For normal operation of the 7704A, the Chop Frequency switch should be left in the 2-MHz position.

When the internal Chop Frequency switch is in the 200-kHz position, the stage operates as follows: At time T_0 (see Figure 13B), the collector current through Q2 is producing a voltage drop across R1 to cut off Q1. Since there is no current through Q1, C2510 and C2511 begin to charge towards −15 volts through R2510-R2511. This causes the emitter of Q1 to gradually go negative until it is about 0.6 volt more negative than the base. At this point (T_1 on Figure 13B), Q1 is forward biased into conduction and its emitter rapidly goes positive. Since the charge on C2510-C2511 cannot change instantaneously, the sudden change in voltage at the emitter of Q1 pulls the emitter of Q2 positive also, to reverse-bias it into cutoff. When the current through Q2 stops, its collector rises to produce a positive output level at pin 14 (time T_1).

During time T_1-T_2, conditions are reversed. Since Q2 is biased off, there is no current through it and C2510-C2511 begins to discharge through R2512-R2513. The emitter level of Q2 follows the discharge of C2510-C2511 until it is about 0.6 volt more negative than the base. This forward biases Q2 and its collector drops negative to reverse-bias Q1. The level at pin 14 drops negative also, to complete the cycle. Once again, C2510-C2511 begin to charge through R2510-R2511 to start the second cycle. When S2510 is set to the 2-MHz position, R2512 is bypassed and one end of C2511 is disconnected from the RC timing circuit. The decreased RC time allows C2510 to charge and discharge at a two-megahertz rate.

Two outputs are provided by this oscillator: The Delay Ramp signal from Q1 or Q2 is connected to the Vertical Chopped Blanking stage, and a square-wave output from pin 14. The square wave at pin 14 is connected to pin 16 through an external capacitor, C2510. C2510 differentiates the square wave from pin 14 to produce a negative-going pulse coincident with the falling edge of the square wave (see pin-16 waveform on Figure 13B). This negative-going pulse is connected to pin 15 through an inverter-shaper which is part of U2510. The resulting output at pin 15 is a positive-going Clock pulse at a repetition rate of either 200 kilohertz or two megahertz, depending on the position of S2510.

Vertical Chopped Blanking

The Vertical Chopped Blanking stage is made up of the remainder of U2510. This stage determines if Vertical Chopped Blanking pulses are required, based upon the operating mode of the vertical system or the plug-in units (dual-trace units only). Vertical Chopped Blanking pulses are produced if: 1. VERTICAL MODE switch is set to CHOP; 2. Dual-trace vertical unit is operating in the chopped mode and that unit is being displayed; 3. Dual-trace vertical unit is operating in the chopped mode with the VERTICAL MODE switch set to ADD. The repetition rate of the negative-going Vertical Chopped Blanking pulse output at pin 4 is 0.2 or two megahertz for all of the above conditions (determined by the Clock Generator stage).

Figure 14 shows a logic diagram and an input/output table for the Vertical Chopped Blanking stage. Notice the comparator block on the diagram. The output of this comparator is determined by the relationship between the levels of its inputs. If pin 10 is more positive (HI) than the grounded input, the output is HI also; if it is more negative, the output is LO.

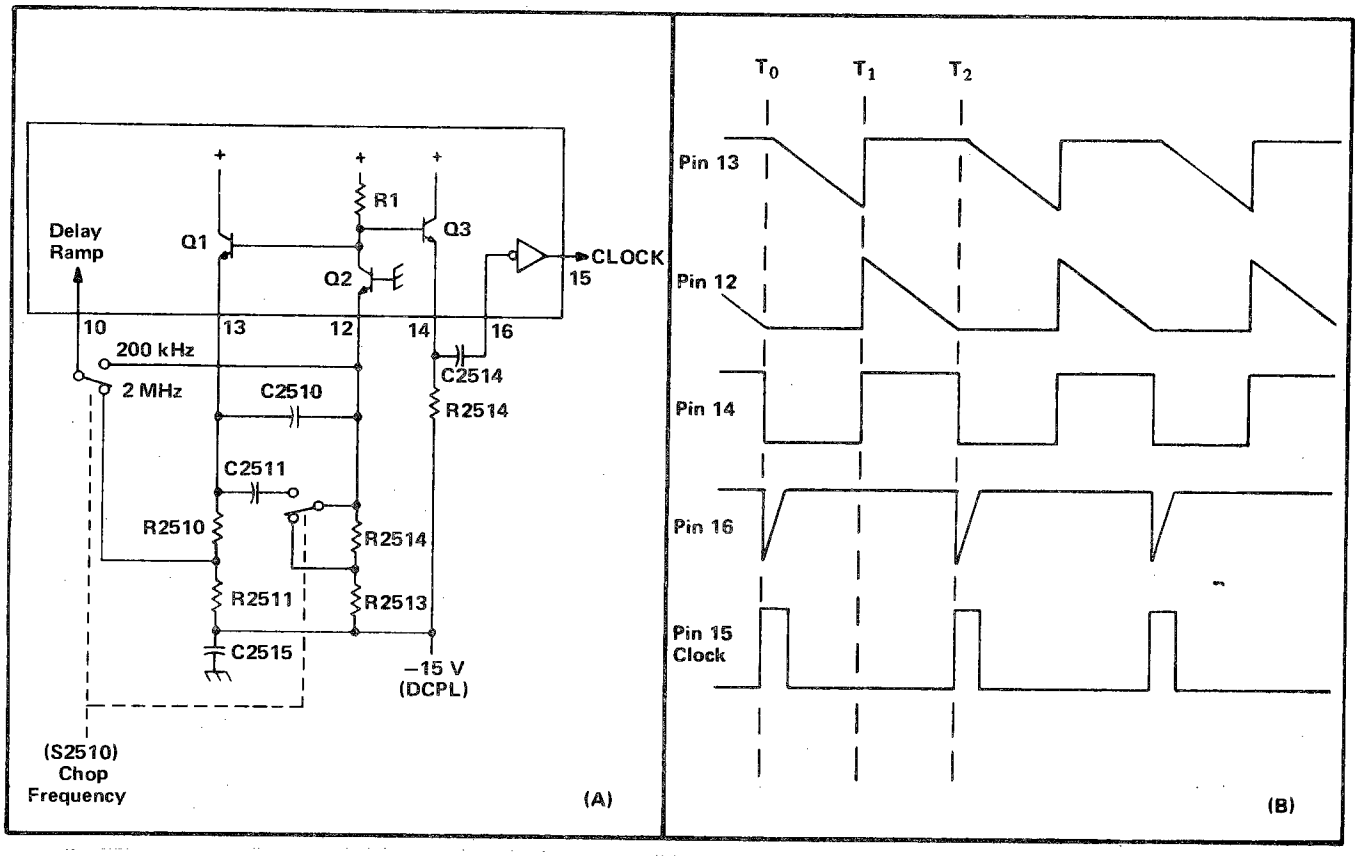
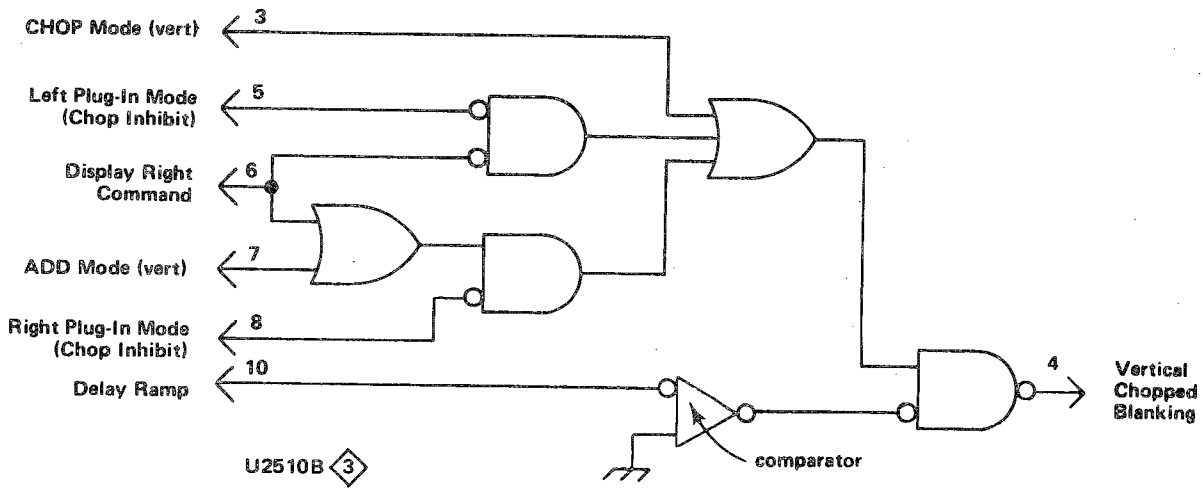


Figure 13. (A) Diagram of Clock Generator stage; (B) Idealized waveforms for Clock Generator stage.

The Delay Ramp signal from the Clock Generator stage determines the repetition rate and pulse width of the Vertical Chopped Blanking pulses. The Delay Ramp applied to pin 10 starts to go negative from a level of about +1.1 volts coincident with the leading edge of the Clock pulse (see waveforms in Figure 15). This results in a HI quiescent condition for the Vertical Chopped Blanking pulse. The slope of the negative-going Delay Ramp is determined by the Clock Generator stage. As it reaches a level slightly negative from ground, the Vertical Chopped Blanking pulse output level changes to the LO state and remains LO until the Delay Ramp goes HI again.

Notice the delay between the leading edge of the Clock pulse generated by U2510A, and the leading edge of the Vertical Chopped Blanking pulses. The amount of delay between the leading edges of these pulses is determined by the Delay Ramp applied to pin 10. This delay is necessary due to the delay line in the vertical deflection system. Otherwise, the trace blanking resulting from the Vertical Chopped Blanking pulse would not coincide with the switching between the displayed traces. The duty cycle of the square wave produced in the Clock Generator stage determines the pulse width of the Vertical Chopped Blanking pulses (see Clock Generator description for more information).

(A)



(B)

Input						Output	
CHOP Mode (vert) 3	Left Plug-In Mode (Chop Inhibit) 5	Display Right Command 6	Add Mode (vert) 7	Right Plug-In Mode (Chop Inhibit) 8	Delay Ramp 10[1]	Vertical Chopped Blanking 4[2]	Conditions
HI	Φ	Φ	LO	Φ	LO	LO	CHOP Mode (vert)
LO	LO	LO	LO	Φ	LO	LO	Left Plug-in Chopped
LO	Φ	HI	LO	LO	LO	LO	Right Plug-in Chopped
LO	LO[3]	LO	HI	LO[3]	LO	LO	ADD Mode, Left or Right Plug-in Chopped
All other combinations						HI	No Vertical Chopped Blanking pulses at output.

Φ = Has no effect in this case.

[1] Ramp signal; considered LO when more negative than about zero volts.

[2] Negative-going pulse

[3] Pin 5 can be HI and not affect operation if pin 8 is LO, and vice versa.

Figure 14. (A) Logic diagram for Vertical Chopped Blanking stage; (B) Table of input/output combinations.

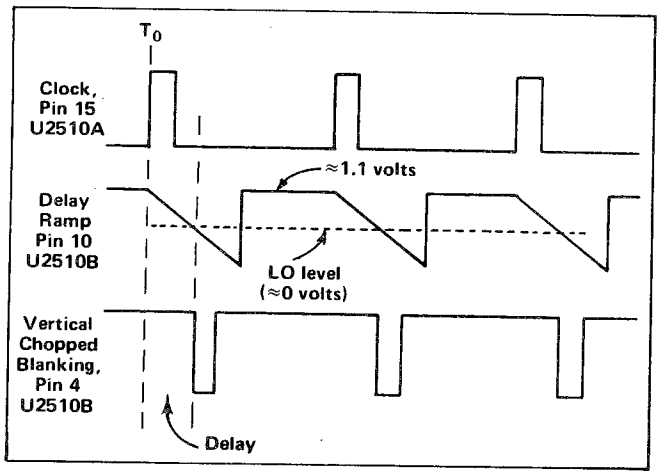


Figure 15. Idealized waveforms for Vertical Chopped Blanking stage.

Chop Counter

The Chop Counter stage of U2520 produces the Vertical Chopping Signal (pin 1), the (Vertical) Chop Drive (pin 8), and the Horizontal Chopped Blanking signal (pin 4). A logic diagram for U2520 is shown in Figure 16, along with waveforms showing the timing relationship between the input and output signals for this stage.

When the HORIZONTAL MODE switch is set to any position except CHOP, pin 6 remains LO and the repetition rate of the Vertical Chopping Signal at pin 1 is one-half the Clock rate (see time T_0 to T_1). This determines the switching rate between the left and right vertical compartments when the VERTICAL MODE switch is set to CHOP.

At the same time, the repetition rate of the (Vertical) Chop Drive at pin 8 is one-fourth the Clock rate. This provides a chopping signal to dual-trace vertical units to provide switching between the two channels. During this time, the level at pin 4 will remain HI.

When the HORIZONTAL MODE switch is set to CHOP, the basic repetition rate of the Vertical Chopping Signal and the (Vertical) Chop Drive is altered. For example, if the HORIZONTAL MODE switch is changed at time T_1 (see Figure 16), a HI level is applied to pin 6. Outputs at pins 1 and 8 will be produced in the normal manner until both outputs are HI. (See time T_2; this condition only occurs once every fifth Clock pulse and only when the HORIZONTAL MODE switch is set to CHOP.) When both of these outputs are at their HI level, the next Clock pulse (at time T_3) switches both outputs LO, and at the same time, switches the Horizontal Chopped Blanking output to the LO level, where it remains until the start of the next Clock pulse.

This change at time T_3 does not appear at pin 4 immediately, due to a delay network in the circuit. (The delay is necessary to make the Horizontal Chopped Blanking coincide with the Vertical Chopped Blanking produced by U2510A; compare bottom two waveforms of Figure 16. Also, see Vertical Chopped Blanking description.) After the delay time, the output level at pin 4 goes LO to blank the display.

The Horizontal Chopped Blanking time must be longer than the Vertical Chopped Blanking time, since it takes more time for the display to switch between horizontal units than between vertical units. During the time that the level at pin 4 is LO, the CRT is blanked and the Vertical Chopping Signal and the (Vertical) Chop Drive cannot change levels. The Clock pulse at T_3 changes only the Horizontal Chopped Blanking output. The level on pin 4 goes HI after the delay time to unblank the CRT.

For the next three Clock pulses, the Vertical Chopping Signal output and (Vertical) Chop Drive operate in the normal manner. However, at the fourth Clock pulse (Time T_4) both outputs are again at their HI level. The fifth Clock pulse at T_6 switches the output at pin 1, pin 8, and pin 4 (after delay) to the LO level to start the next cycle. Notice that a Horizontal Chopped Blanking pulse is produced at pin 4 with every fifth Clock pulse. Also notice that with the HORIZONTAL MODE switch set to CHOP, two complete cycles of the Vertical Chopping Signal are produced with each five Clock pulses (repetition rate, two-fifths Clock rate) and one complete cycle of the (Vertical) Chop Drive for every five Clock pulses (one-fifth Clock rate). Notice that the large shaded area produced by the Horizontal Chopped Blanking pulse (see Figure 16) is not part of the display time (CRT display blanked). However, about the same time segment is displayed from the vertical signal source with or without Horizontal Chopped Blanking, due to the change in repetition rate when in the CHOP horizontal mode.

The Vertical Chopping Signal at pin 1 of U2520 is connected to the Vertical Mode Logic stage (see following description) through L2519-R2519. This signal is HI when the right vertical unit is to be displayed and LO when the left vertical unit is to be displayed. The (Vertical) Chop Drive at pin 8 is connected to the plug-in units in the vertical compartments through L2528-R2528 via the Main Interface board. When this signal is HI, Channel 2 of the plug-in units can be displayed; when this level is LO, Channel 1 is displayed. The Horizontal Chopped Blanking signal at pin 4 is connected through LR2523 to the Horizontal Binary stage U2530 and to the Z-Axis Logic stage U2573 by way of CR2524. When this signal is HI, the CRT is unblanked to display the selected signal. When it is LO, the CRT is blanked to allow switching between the horizontal units.

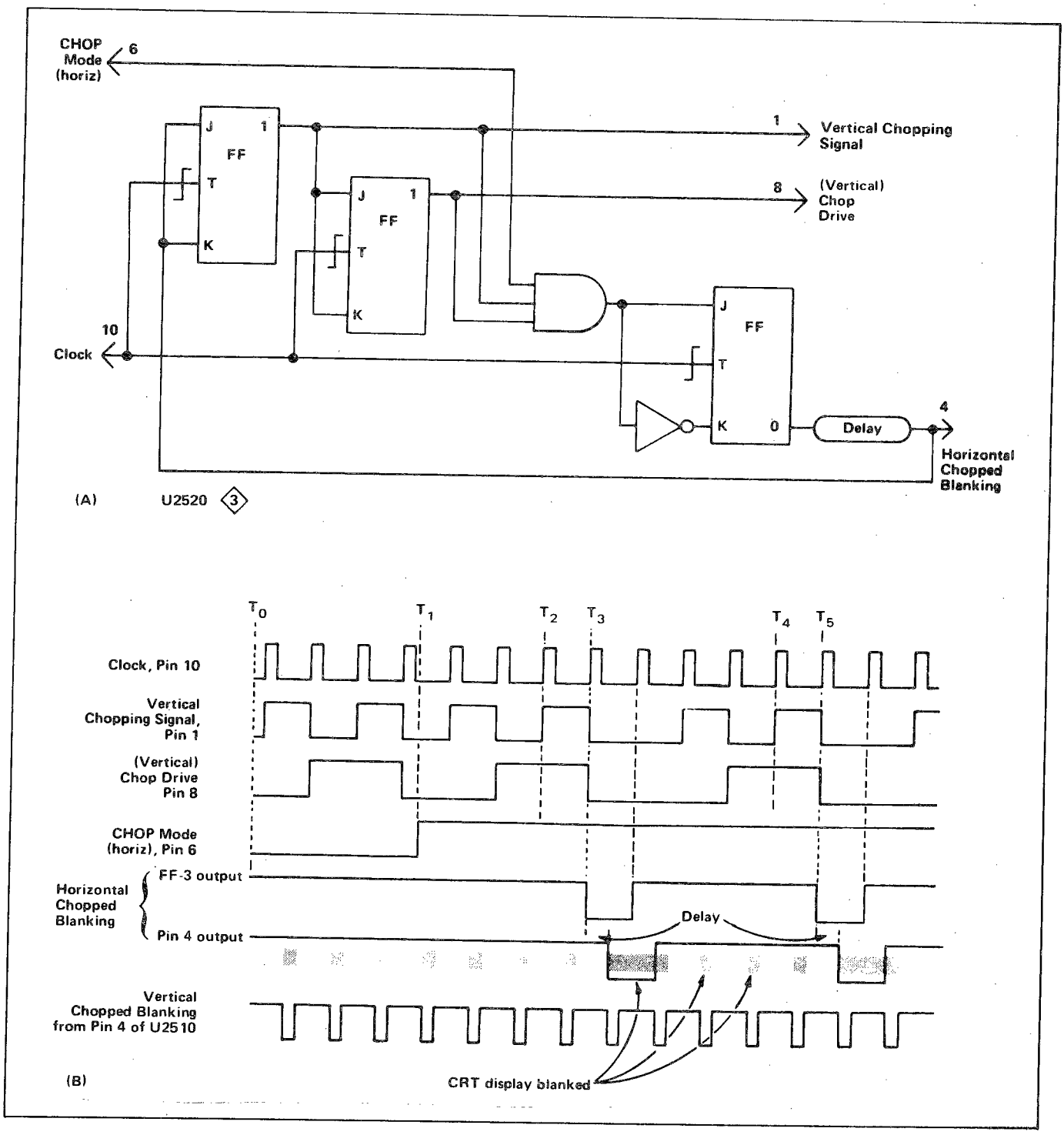


Figure 16. (A) Logic diagram for Chop Counter stage; (B) Table of input/output combinations.

Vertical Mode Logic

The Vertical Mode Logic stage is made up of discrete components CR2501-CR2502, CR2552-CR2553, and Q2553-Q2556. These components develop the MF (Main Frame) Channel Switch Signal (Display Right). This signal is connected to the Main Interface circuit (vertical plug-in compartments and trigger-selection circuitry) and to the Vertical Interface circuit to indicate which vertical unit is to be displayed. When this output level is HI, the right vertical unit is displayed; when it is LO, the left vertical unit is displayed.

The VERTICAL MODE switch shown on diagram 1 provides control levels to this stage. This switch provides a

Logic Circuit

HI level on one of five output lines to indicate the selected vertical mode; the remaining lines are LO (notice that only four of the lines from the VERTICAL MODE switch are used on this schematic). Operation of this stage is as follows:

When the VERTICAL MODE switch is set to RIGHT, a HI level is connected to the base of Q2553 through R2501. This forward-biases Q2553, and the positive-going level at its emitter is connected to the emitter of Q2556. The collector of Q2556 goes HI to indicate that the right vertical unit is to be displayed. For the CHOP position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR2501-CR2502 through R2502. Both diodes are forward biased so that the Vertical Chopping Signal from pin 1 of U2520 can pass to the base of Q2553. This signal switches between the HI and LO levels at the Clock Generator rate and produces a corresponding MF Channel Switch Signal (Display Right) output at the collector of Q2556. When this output is HI, the right vertical unit is displayed and when it switches to LO, the left vertical unit is displayed.

In the ALT position of the VERTICAL MODE switch, a HI level is applied to the anodes of CR2552-CR2553 through R2551. These diodes are forward biased so the Display Right Command from pin 6 of the Vertical Binary stage can pass to the base of Q2553 to determine the MF Channel Switch Signal (Display Right) level. The Display Right Command switches between its HI and LO levels at a rate determined by the Vertical Binary stage.

The control levels in the LEFT and ADD positions of the VERTICAL MODE switch are not connected to this stage. However, since only the selected line from the VERTICAL MODE switch can be HI, the RIGHT, CHOP, and ALT lines must remain at their LO level when either LEFT or ADD are selected. Therefore, the base of Q2553 remains LO to produce a LO MF Channel Switch Signal (Display Right) output level at the collector of Q2556.

A logic diagram of the Vertical Mode Logic stage is shown in Figure 17.

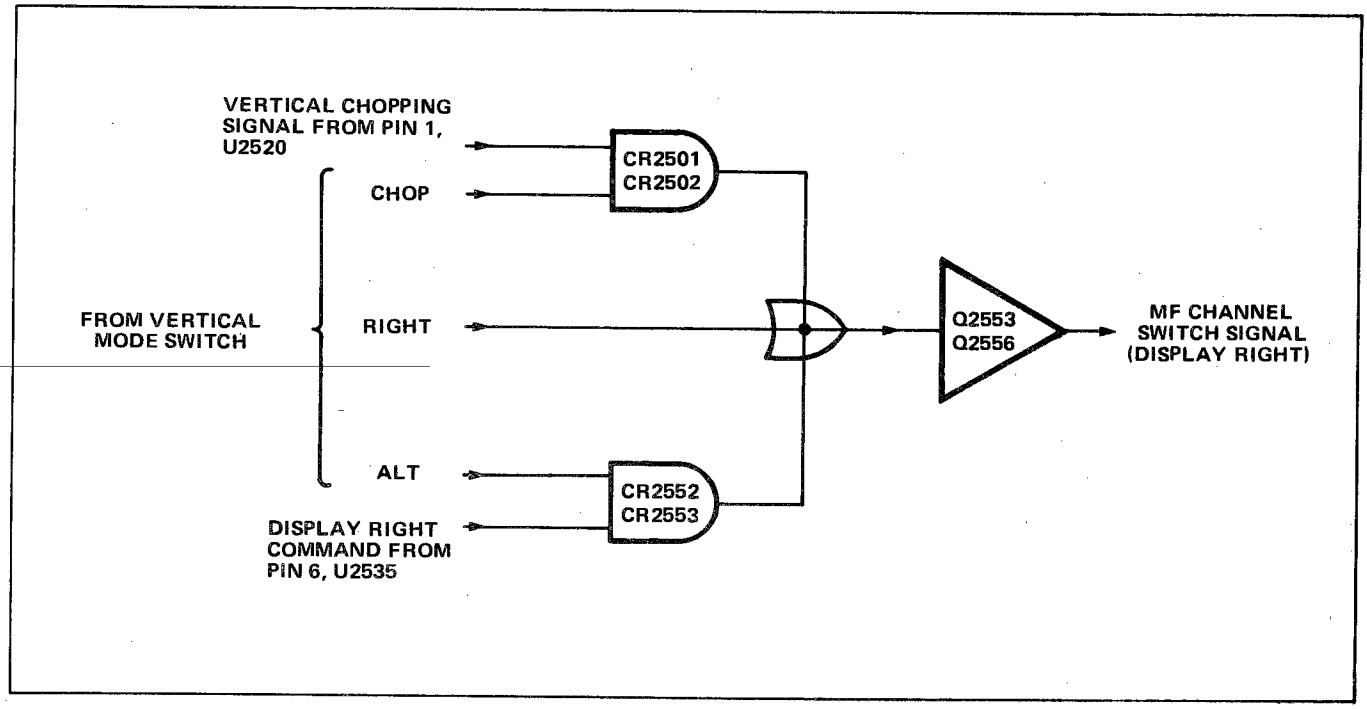


Figure 17. Logic diagram of Vertical Mode Logic stage.

POWER SUPPLIES

The 7000-Series Main Frames were the first Tektronix Laboratory oscilloscopes to have power supplies treated as a separate module. This gave the design engineer more flexibility in the choice of a power system as evidenced by the initial 7000-Series Main Frames: One with a lossy supply (7504) and the other (7704) with a high-efficiency supply.

Second generation 7000-Series Main Frames again used the separate power supply module concept. As before, two types of supplies were used: A low-efficiency low-cost unit for the 7400- and 7600-Main Frames, and an improved, more compact, reduced-cost high-efficiency supply (7800 and 7900 Main Frames). Both concepts provided for 5.25 inch-high rackmount main frame applications.

The 7400 and 7600 supplies have separate low and high voltage modules. The 7800 and 7900 supplies combine the low and high voltage supplies in the same package deriving both from the common inverter source.

The reason for continuing with two power supply concepts is primarily economical. The high efficiency supply would have been used exclusively, had its costs been lower. A comparison follows:

	Low Efficiency	High Efficiency
Cost	+ (1.0)	– (1.5 to 2.0)
Efficiency	– 50%	+ 75%
Weight	– 15 - 25 lbs.	+ 7 - 10 lbs.
Size	– (1.0)	+ (0.75)
Servicing Difficulty	+	–
EMI Generation	+	–
Reliability*	+	–

\+ = In favor.

– = Against.

* Historically this has not been true due to the high thermal stress on some low-efficiency supply components. However, a moderately stressed low-efficiency supply should be more reliable, due primarily to its lesser number of components.

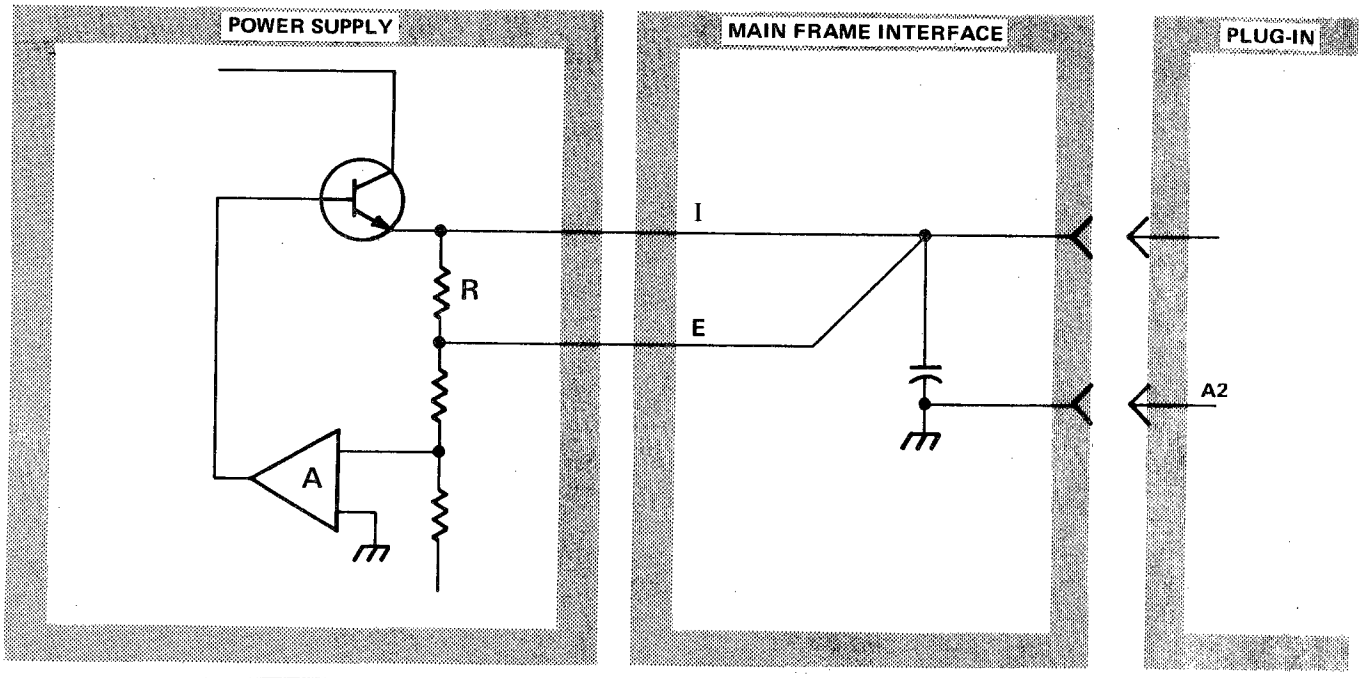
POWER SUPPLY FEATURES AND SPECIFICATIONS

Except as noted, the following are common to both the high- and low-efficiency supplies.

Voltage Sensing

Voltage sensing is used to assure accurate supply voltages at the Main Frame/Plug-In Interface. The +5 V, ±15 V, and ±50 V supplies are used by the plug-ins which require accurate voltages so that calibration can be assured regardless of the main frame used.

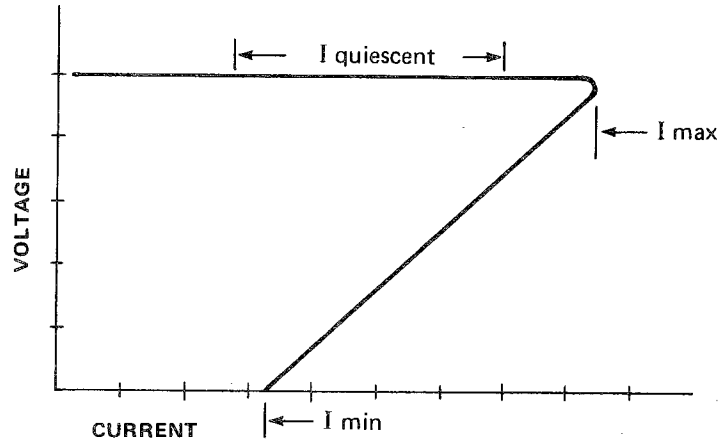
This sensing is done on the Main Interface board close to the plug-in connectors. Heavy conductor lines are provided for the current path and light conductor lines for the voltage sensing. A typical circuit is as follows:



There is essentially zero change in current in the Sense Line (E) with changing load, therefore, it is not load dependent. This is not true of the Current Line (I) as the voltage on the Series Pass Emitter will move with changing load. Resistor R prevents supply runaway if the Sense Line opens. The Resistor R is large enough to minimize loading on the Sense Line (E).

Overload Protection

The +5 V, ±15 V, and ±50 V supplies utilize foldback of the output current for protection, i.e., output current is limited to a maximum value, then as the supply output voltage is pulled toward ground, the current reduces.



Where:

I max: >I quiescent. Typically 20 - 30% over I quiescent.

I min: >0. This is necessary as the supply may sink current even when shorted to ground. I.E., amplifiers with long tail current sources will continue to deliver current to the collector supplies even if the supplies are at ground potential. Should I min be < sinking current, the supply will latch up and not return to design voltage when the short is removed. I min is typically 20 - 50% of I max.

Current foldback is a non-destructive method of protection. However, great care must be taken to assure that the pass transistor stays within its Safe Operating Area (SOA) during the excursion between I max and I min. In this region, the pass transistor power can be much greater than when in the quiescent state.

Higher voltage supplies use fusing for protection in the 7400- and 7600-series instruments. In the 7800- and 7900-series, the +130 volt components are protected by an inverter shutdown mode, i.e., the inverter control senses an overload and causes the inverter (power supply energy source) to operate in a 5% - 10% on, 90 - 95% off mode. When the overload is removed, the supply will return to normal.

The crt supplies (cathode and anode) of the 7400- and 7600-series are fuse protected. The 7800- and 7900-series supplies are protected similarly to the +130 V supply, i.e., overloads are nondestructive.

In addition, the 7800-7900 series crt anode supply has an over-voltage and over-current (beam current) recognition circuit that protects the operator from excessive radiation exposure (≤0.1 mR) and the crt phosphor from burns. The over-voltage protection is operational only when the inverter control circuitry fails to limit the supply output (a fault). The over-current protection is non-destructive and is activated at slow sweep speeds (100 ms/div and slower) and when in the Ext Horiz mode.

Specifications:

Supply	Max Current Per Plug-In ①	Initial Setting Accuracy	Maximum Specifications			Drift Per Year	Total Ripple ③	Response to a Current Step ④	
			Hi-Lo Line Variation	Temp. Coeff.	Output Resistance			Recovery to 1 mV	Time Constant of Recovery
V	mA	±%	±%	ppm/°C	mΩ	±%	mV p-p	μs	μs
+50	100	0.5	0.02	130	20	0.3	3	10	5
±15	500	0.6	0.02	130	10	0.3	1	5	2
−50	100	⩽0.2 ②	0.01	75	20	0.2	2	10	5
+5	500	1.0	0.02	200	10	0.5	1	10	5
Lights	500		1.0		180				

① Plug In dissipation ⩽ 16.5 watts maximum.

② Adjustment of −50 V sets +5 V, +15 V and +50 V. Settable to ≈ 0.1%.

③ At maximum load; measured with 500 KHz system at Plug-In Interface with 067-0588-99 Load Plug-In.

④ Measured at ½ current load with 067-0588-99 Load Plug-In.

CAMERA POWER

From Top Pin Crt Bezel Connector
(+15 V Regulated Supply)

	Power Light Off	Power Light On
Standby	30 μA or less at +20°C to +30°C	60 mA or less at +20°C to +30°C
Shutter Operation	90 mA peak*	130 mA peak*
Focus Operation	550 mA peak*; 190 mA steady state	600 mA peak*; 250 mA steady state

***Will vary with Main Frame.**

PROBE POWER

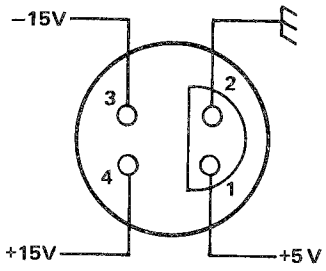
Output Regulated Voltages For Each Probe

−15 volts at 100 milliamperes maximum.

Chassis ground.

+5 volts at 100 milliamperes maximum.

+15 volts at 100 milliamperes maximum.



MAIN FRAME CONNECTOR AS SEEN FROM OUTSIDE INSTRUMENT

READOUT

READOUT SYSTEM

Contents

DEFINITIONS FOR NEW TERMS

The scale factor readout system incorporates new concepts and circuit techniques. As a result, new terminology has developed. New words have been assigned to explain various functions and, in other cases, new meanings to old words have been assigned. The purpose of the following list of definitions is to aid in the learning process.

Character. A single number, letter, or symbol which can be generated and displayed on the crt.

Word. A related group of characters having a maximum length of ten characters. The length typically varies from two to five characters.

Timeslots. Individual pulses that comprise a pulse train. The pulse train length is ten timeslots. Essentially, the timeslots interrogate the plug-ins to detect the presence of data.

Standard Format. A predetermined set of rules whereby each individual timeslot is assigned to a certain purpose. It is used for all data corresponding to a scaling factor, but may be violated in some future plug-ins.

Time Multiplexing. Transmission of data from two or more sources over a common path by using different time intervals for each source.

Matrix Coding. The code by which an address to characters or logical instructions is achieved. The readout system utilizes a 10 x 10 selection matrix. To define a character or an instruction in the matrix, a row and a column must be designated.

Column. One of the vertical lines in the character selection matrix.

Row. One of the horizontal lines in the character selection matrix.

BASIC DESCRIPTION OF READOUT SYSTEM

The readout system incorporated in the 7000-series instruments is different from readout systems used in some of our other products. The 7000-series system employs an electronic character generating circuit which time shares the crt with the normal scope functions. The characters are formed by a series of X and Y analog currents developed by Character Generating I.C.'s. A set of 50 different characters are currently provided with the capability to expand to 70 if necessary. This includes all the numerals, most of the alphabet (upper case), the symbols p, n, μ, m, and other special symbols. Although at present, only scale factor displays are utilized, the capability does exist to display a wide variety of numerical data and English text.

In order to fully utilize this capability without the need for undue coding complexity, an analog coding scheme has been developed in which data is encoded by means of resistors and switch closures. This data is generated in the plug-in by connecting these resistors between time-slot pulses and data output lines via the appropriate switch.

This coding scheme includes two channels for each plug-in so that dual trace amplifiers and delaying/delayed time base units can be accommodated. There are only two data output connections per channel—a column data line and a row data line.

The Display

Although the system is readily modified for two and three plug-in mainframes, this discussion will be restricted to the four plug-in 7000-series mainframes. A maximum of eight words may be displayed, corresponding to two channels for each of the four plug-in units. The position of each word on the crt is fixed and related to the plug-in from which it came, as shown in Figure 1.

Each channel can display one word having up to ten characters, although in general there will be between 2 and 5

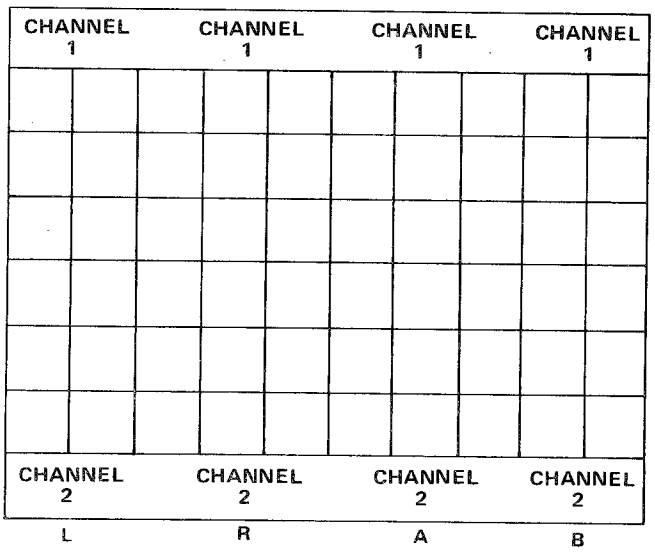


Figure 1. Location of readout display on the crt identifying the originating plug-in and channel.

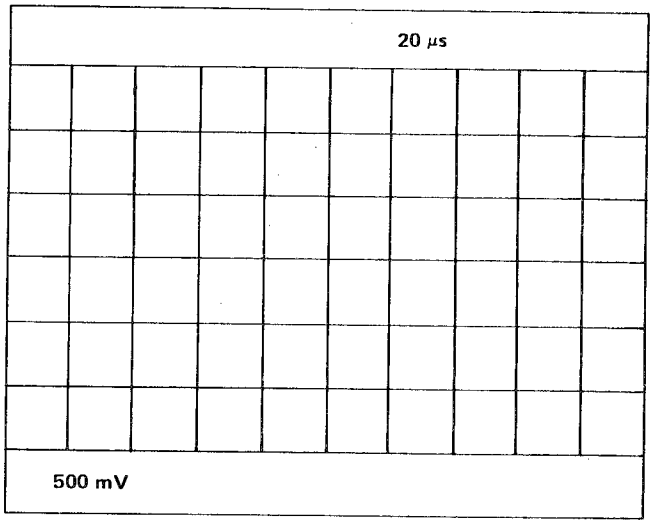


Figure 2. Typical readout display with only Channel 2 of the Left Vertical unit and Channel 1 of the A Horizontal unit displayed.

characters per word. The characters are normally written without redundant spaces, but spaces can be called for in the code.

Only channels actually in use are displayed. For example, we might have a dual trace vertical in the left compartment, a high sensitivity vertical in the right compartment, a single sweep in the A Horizontal and another in the B Horizontal, but have only selected Channel 2 of the left plug-in and the A sweep; the display would appear as shown in Figure 2.

The symbols are three millimeters high and two millimeters wide, with a spacing of 0.3 mm. This leaves a gap of about 1 character width between words under the worst case conditions, when all ten characters of each channel are used.

The readout display has a separate and independent front-panel intensity control, which also permits the readout to be switched off.

The alpha-numeric display has little effect on the intensity of the normal scope display. The reason is as follows: Each character written takes 16 μs, or 0.07% of the display cycle time. So, the full writing rate of the crt system is needed for an acceptably bright readout display. The fractional time taken out of the normal scope display, however, is proportional to the number of characters displayed and is 0.1% per symbol. Thus, a maximum of 8% (8 x 10 x 0.1%) can be used.

Although this has little effect on the intensity of a normal display, there is a possibility under certain conditions, that gaps in the waveform would be visible. With a given amount of data being displayed, there will be certain sweep repetition rates and sweep speed settings when these gaps become noticeable. The possibility of any synchronous patterning is minimized, however, by the pseudo-random timing of the readout system. The duration of each timeslot varies, depending on whether or not data is present in the plug-in during that particular timeslot.

Data Encoding and the Character Selection Matrix

Each character to be displayed must be defined by both a row current and a column current. The magnitude of these two currents determine a point on a Character Selection Matrix.

The analog code used has 11 discrete current levels, ranging from zero to 1 mA, in 100 μA increments. Figure 3 shows the Character Selection Matrix code. This coding arrangement is the key to understanding the overall operation of the readout system. Notice that there are 50 different addressable characters and a number of special instructions. The addressable points which are black are unused in the present coding arrangement.

Data for the eight channels of readout is encoded and decoded by a circuit in the readout system similar to the one in Figure 4.

ROW NUMBER / COLUMN NUMBER →	CURRENT (MILLI-AMPERES)	C-0	C-1	C-2	C-3	C-4	C-5	C-6	C-7	C-8	C-9	C-10
		0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	⩾ 1.0
R-1	0	SKIP[1]	*0*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*
R-2	0.1		*f*	*<*	*I*	*/*	*+*	*−*	*+*	*C*	*Δ*	*>*
R-3	0.2		ADD[1] ONE ZERO	ADD[1] TWO ZEROS	SHIFT[1] PREFIX ←	SHIFT[1] PREFIX ← AND ADD ONE ZERO						*IDENTIFY*[1]
R-4	0.3		*m*	*μ*	*n*	*p*	*X*	*K*	*M*	*G*	*T*	*R*
R-5	0.4		*S*	*V*	*A*	*W*	*H*	*d*	*B*	*c*	*Ω*	*E*
R-6	0.5		*U*	*N*	*L*	*Z*	*Y*	*P*	*F*	*J*	*Q*	*D*
R-7	0.6				DECIMAL[1] POINT LOCATION NO. 3	DECIMAL[1] POINT LOCATION NO. 4	DECIMAL[1] POINT LOCATION NO. 5	DECIMAL[1] POINT LOCATION NO. 6	DECIMAL[1] POINT LOCATION NO. 7			
R-8	0.7										DECIMAL[2] POINT	
R-9	0.8											
R-10	0.9	ADD SPACE IN DISPLAY[1]										

UNUSED LOCATIONS. AVAILABLE FOR FUTURE EXPANSION OF READOUT SYSTEM

[1] OPERATIONAL ADDRESS.

[2] DECIMAL POINT CHARACTER. SEE DECIMAL POINT CHARACTER DESCRIPTION IN TEXT.

Figure 3. Character Selection Matrix.

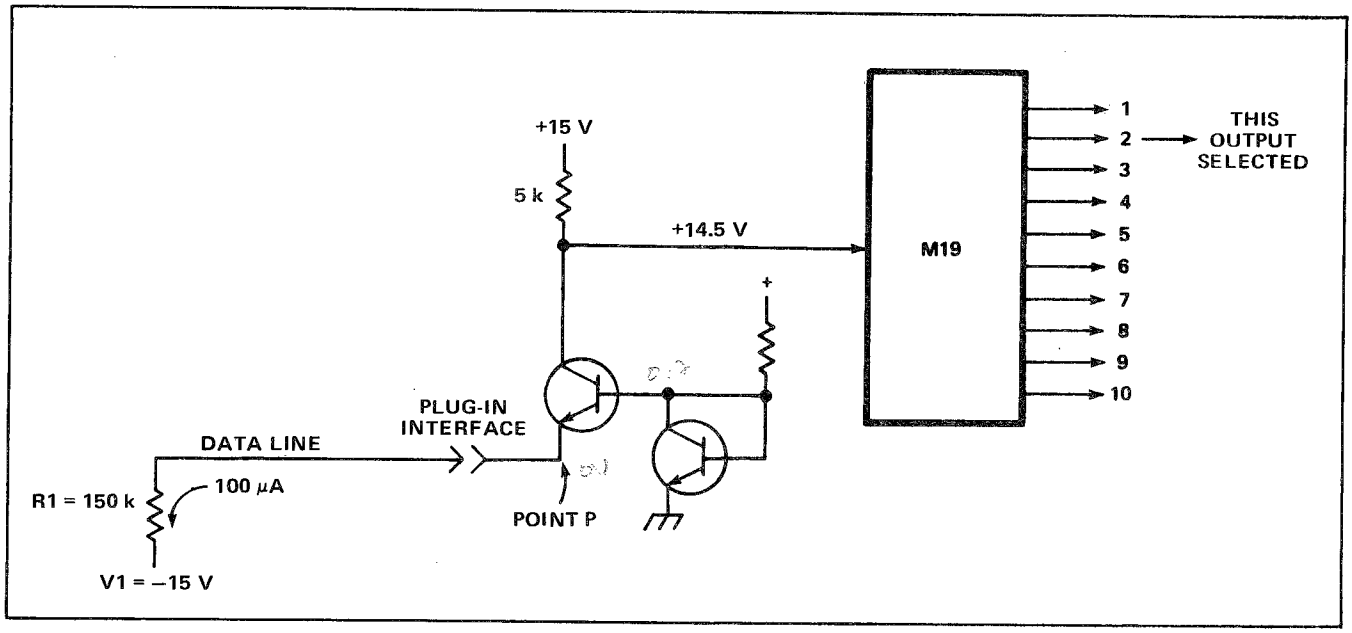


Figure 4.

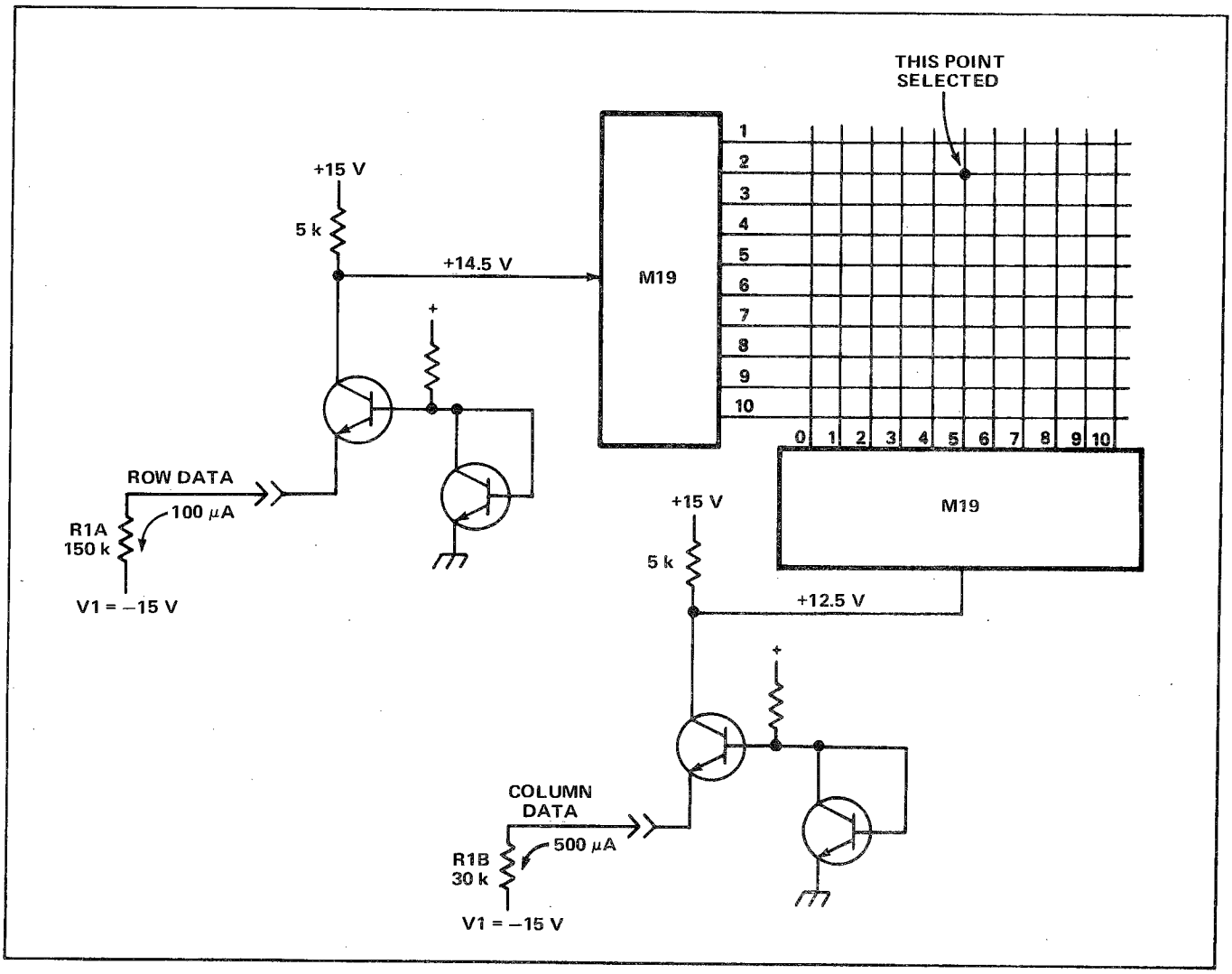


Figure 5.

Point P is very close to ground potential; hence, the collector current of the transistor is nearly V1/R1 or 100 μA. The resistor, therefore, has encoded a single analog level. Resistor values are chosen in the plug-in to choose current units of 100 μA each, ranging from zero to 1 mA. The output from the collector drives an Analog/Decimal converter (a single I.C. designated as a Row or Column Decoder, 155-0014).

Notice that output line No. 2 was selected from the A to D converter. This corresponds to row 2 in the character selection matrix.

Ten distinct outputs can be selected by this circuit (the particular one being dependent on the amplitude of the analog input). Each output then operates logic to select characters or instructions. Duplicating this, two stages can be used to encode both row and column data to select a point in the matrix. This is shown in Figure 5.

With the resistor values chosen, we have selected row 2 and column 5 in the character selection matrix, or the symbol +. This illustration depicts the selection of one character during one timeslot for 1 channel of 1 plug-in. (See Figure 5.)

By adding more encoding resistors and substituting a sequence of voltage pulses, (time slots) for V1, a sequence of analog levels is generated, which in turn selects a sequence of characters or instructions when decoded. In this manner, 1 complete word for 1 channel can be generated. Figure 6 shows such an arrangement.

Here, 10 separate time slot lines are applied to an array of encoding resistors in the plug-in. The 2 data output lines (row data and column data), would connect with the emitters shown in Figure 5. The example above encodes the word "500 mV" when decoded by the matrix.

Notice that unused time slots are skipped, that is, they do not interrupt the main scope display and the system proceeds to the next instruction. Any skipped time slots do not advance the counter when it positions the character in the word, thus unwanted gaps are prevented from appearing in the text.

So far, a single channel has been encoded and decoded. It remains only to add two Data switches. Referring to Figure 7, each data switch is an I.C. (designated 155-0015) which selects just one of the eight channels at a time and produces a time multiplexed string of analog levels that carry the data to the decoding M19.

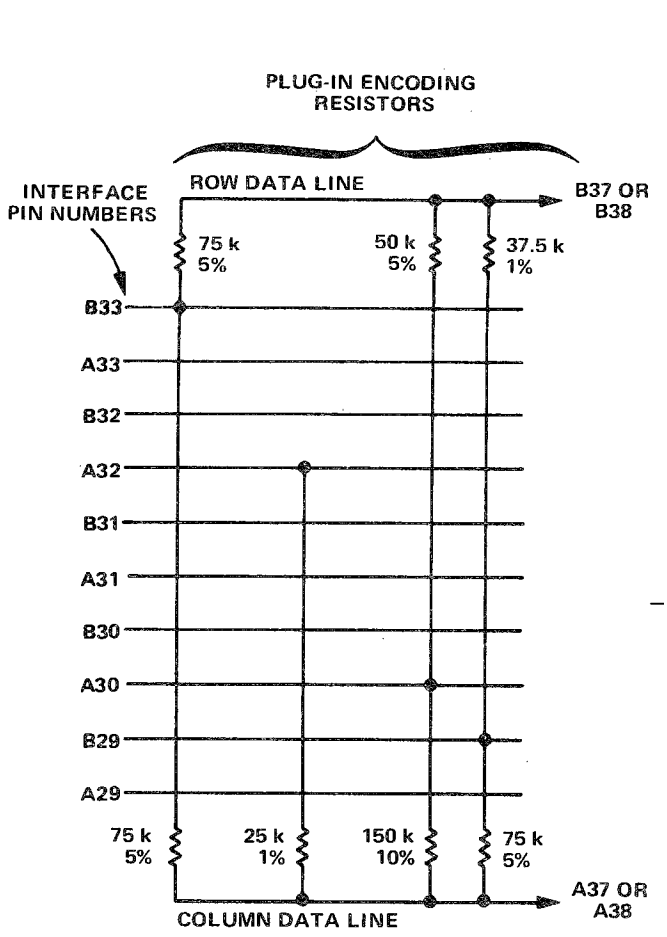
A 3 bit, binary-coded signal directs the Data Switch to a different channel after every 10 time-slot pulses. This binary signal also positions the beam to its proper location on the crt.

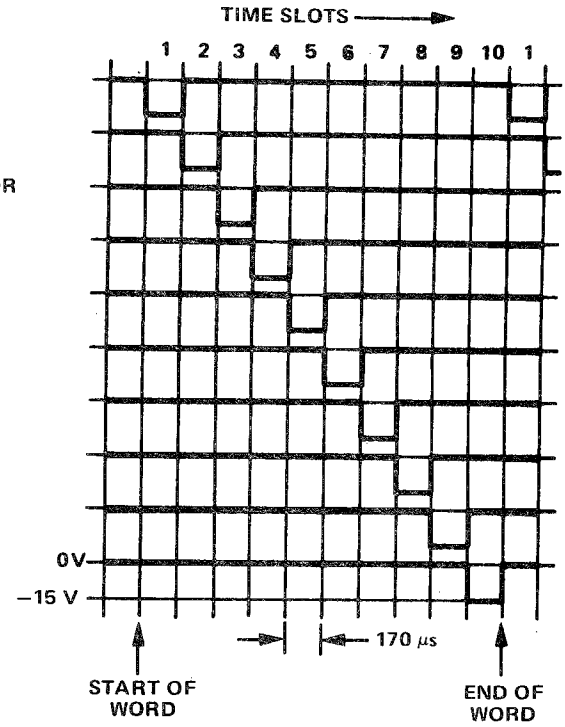
THE STANDARD FORMAT

In the previous example, each time slot had a designated purpose. That is, each time slot interrogated the plug-in for a particular kind of data. From a hardware point of view, the readout system places no restrictions on the data; any symbol in the set can appear in any position in any word. However, any data that corresponds to a waveform scaling factor must conform to a standard format. Table 1 describes the standard format presently used.

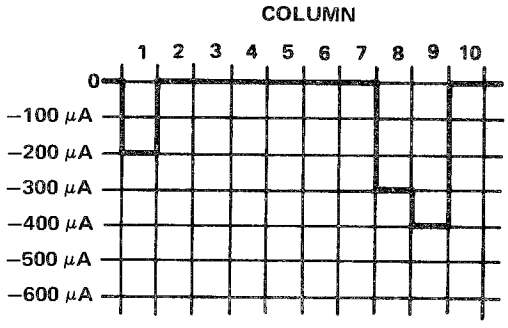
TABLE 1
Standard Readout Format

Timeslot Number	Description
TS-1	Determines decimal magnitude (number of zeros displayed or prefix change information) or the IDENTIFY function (no display during this time slot).
TS-2	Indicates normal or inverted input (no display for normal).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control (no display for calibrated condition).
TS-4	1-2-5 scaling.
TS-5 TS-6 TS-7	Not encoded by plug-in unit. Left blank to allow addition of zeros by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Defines the units of measurement of the plug-in unit. May be standard units of measurement (V, A, S, etc.) or special units selected from the Character Selection Matrix.





ANALOG DATA CURRENTS



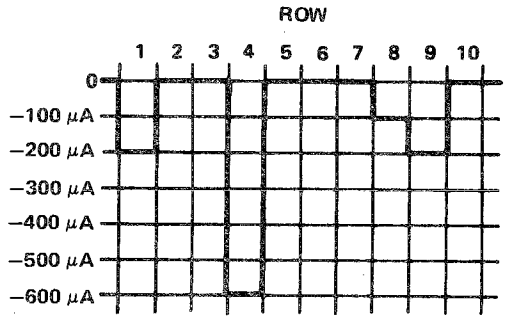


Figure 6.

Notice that the number of zeros to be displayed is determined during the first time slot. They are not displayed, until timeslots 5, 6, and 7. Time slots 5, 6 and 7 are never encoded by the plug-in. That is, during these time slots, the correct number of zeros are displayed which have been stored since time slot one in the Zeros Logic Memory. This coding scheme allows for probe coding which will be discussed next.

"ZEROS LOGIC" AND PROBE CODING

Analog coding allows a kind of data manipulation not easily achieved with binary coding. A piece of data can be modified by the addition or the subtraction of current levels. The summing point, P, in the earlier diagrams affords a convenient spot to do this. This is a powerful feature of the coding scheme used in the 7000-series readout system, and is extensively used. To explain its use in

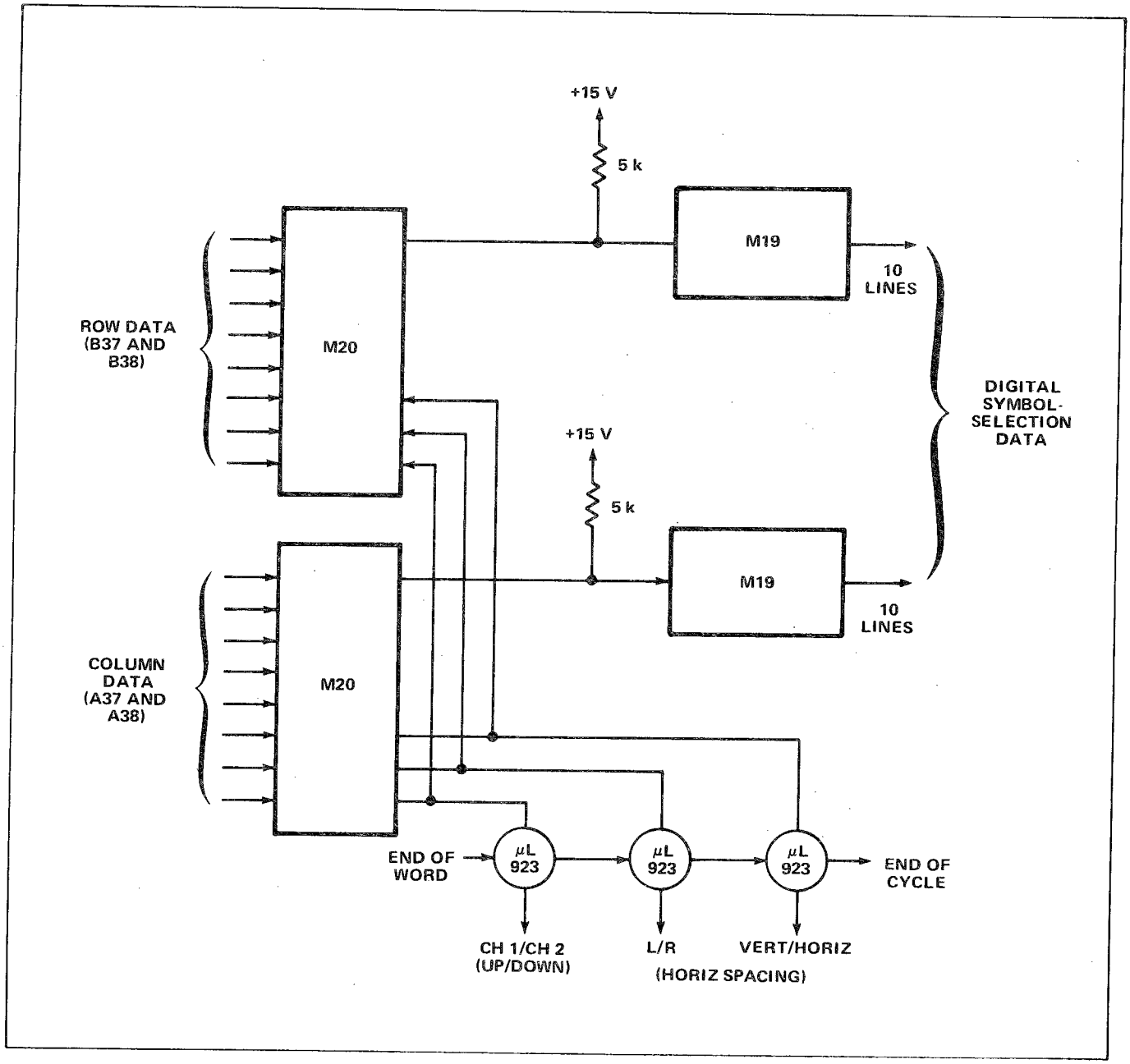


Figure 7.

coding the number of zeros that follow the 1, 2, or 5 scaling factor, let's take an example of a sensitivity setting of 10 μV without a probe. The code for "10 μV" in the standard format is as follows: The first instructions says: During timeslot 5, add one unit of current to the column code. Thus, one zero appears at this time. This instruction could be read as "31" meaning Row 3 and Column 1 in the Selection Matrix. Now, if a X10 probe is connected, one unit of current is added to the column code during time slot 1. And the instruction is changed from "31" to "32" which is interpreted: During time slots 5 and 6, add 1 unit of current to the column code. This causes 2 zeros to appear in their proper position, showing 100 μV.

When a X100 probe is added, 2 units of current are added to the column code during time slot 1 and the instruction becomes "33" meaning: During the time slot 8, subtract 1 unit of current from the column code. This changes the "μ" to "m" and the display reads "1 mV".

The circuit that stores these instructions and executes them at the proper time is the 155-0018 (an I.C. designated Zero's Logic and Memory). This I.C. also contains the logic for presenting the word IDENTIFY.

The word IDENTIFY can be displayed by increasing the column current to 1 mA during time slot 1. Referring to the Selection Matrix of Figure 3, the Trace Identify function is defined by column 10 and row 3. Whenever this column and row is decoded, the Zero's Logic instructs the Identify circuit to present the word IDENTIFY during time slots 2 through 9.

A more detailed discussion of this use of "Analog Shifting Logic" will be pursued in the circuit description. It is clearly a very flexible feature of the system.

CHARACTER GENERATING INTEGRATED CIRCUIT

The key to achieving a low cost readout system was in the development of an integrated circuit technique which permits the characters to be generated as X-Y waveforms very simply. This circuit puts 10 characters into a 16-pin, dual end line package and permits packages to be arranged in accordance with a matrix code for addressing purposes. The character size can be controlled by the magnitude of the column selection current.

There are 5 different character generator I.C.'s used in the system. The complete set of characters, symbols, or numerals which can be displayed were depicted in the Selection Matrix in Figure 3. As an example, Row 6 selects one of the character-generator I.C.'s. It can generate any of the characters depicted in Columns 1 through 10.

Each character is made up of seven continguous strokes connecting 8 coordinate points. The method of defining the coordinates utilizes the fact that a current can be accurately divided into several components by means of transistors with variable emitter areas. Consider the circuit shown in Figure 8.

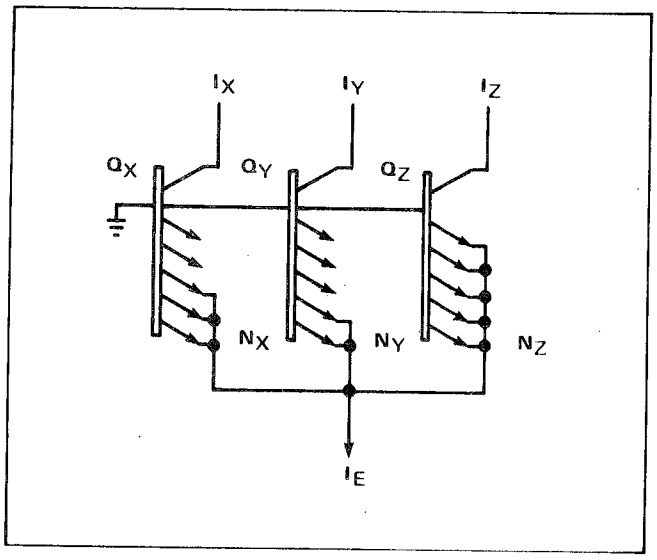


Figure 8.

The three transistors have **multiple emitters**, each of which have areas that are approximately equal, and which are connected to a common current source. Notice, however, that only some of the emitters are connected. This circuit would have the same current division properties as a variable-area emitter arrangement.

If the outputs are taken from the collectors I_X and I_Y, we have:

$$I_X = \frac{N_X}{N_X + N_Y + N_Z} I_E$$

and

$$I_Y = \frac{N_Y}{N_X + N_Y + N_Z} I_E$$

where N_X, N_Y, and N_Z and the number of emitters connected in Q_X, Q_Y, and Q_Z respectively. In the case shown,

with N_X equaling 3, N_Y equaling 2, N_Z equal to 5, we would have I_X equal to $.3I_E$ and I_Y equal to $.2I_E$.

Thus, the circuit shown in Figure 8 defines a 2-dimensional coordinate point, determined by the artio of current division. Several coordinate points could therefore, be determined by combining a number of transistor trios, each having a different configuration of connected emitters.

CHARACTER SCANNING

Several groups of 3 transistors (trios) can share a common current source but the trio whose bases are most positive (for NPN transistors) will ge the majority of the current. Further, since abrupt sequencing would display **points** (not lines) on the crt, it is necessary to gradually reudce the voltage on 1 trio of bases while increasing it on the next to produce smooth strokes. Such an action can be produced by using a special ladder network and a scanning voltage as shown in Figure 9. For clarity, only single transistors are shown as being scanned; in the actual I.C., the arrangement is a trio of transistors.

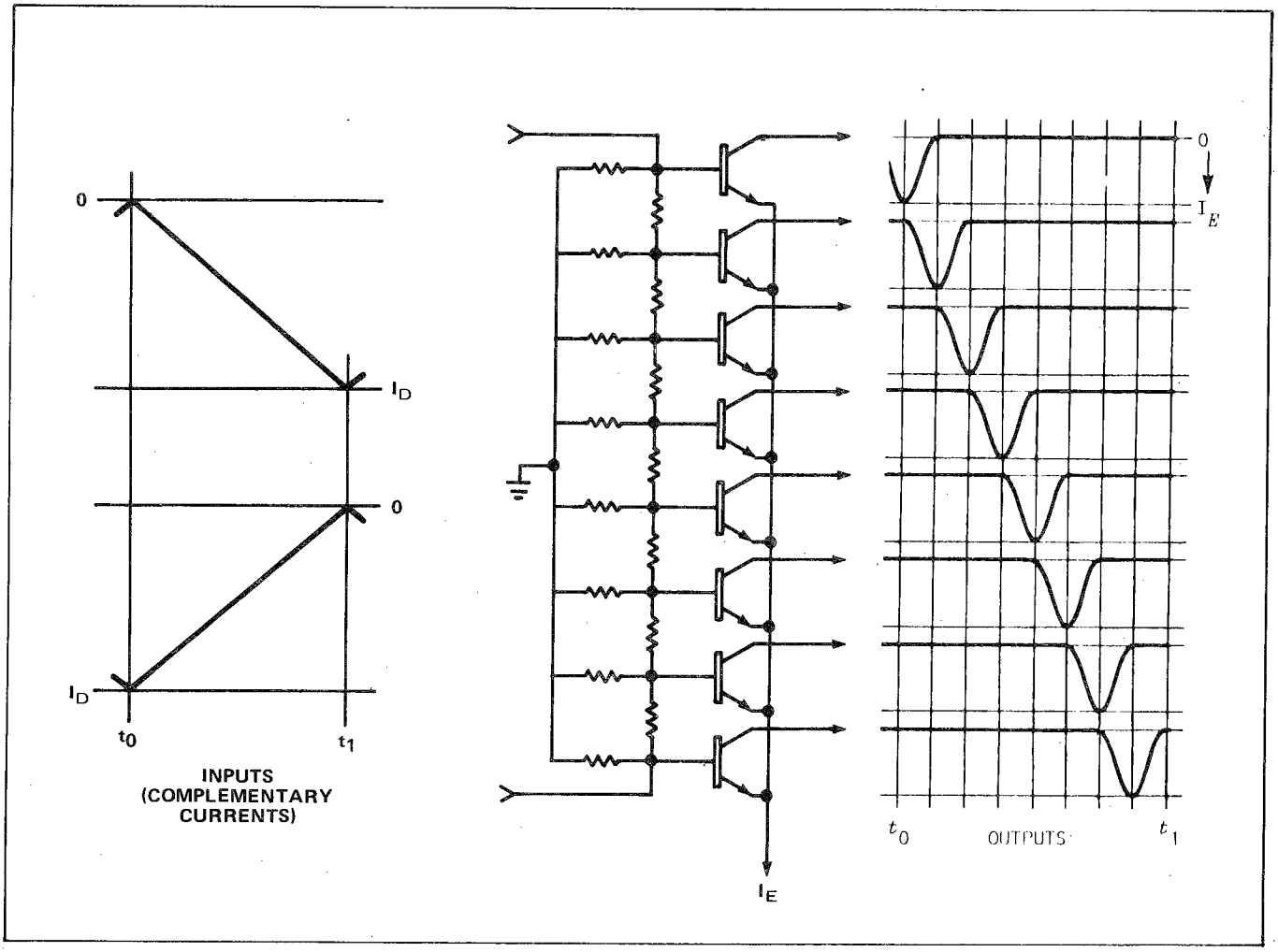


Figure 9.

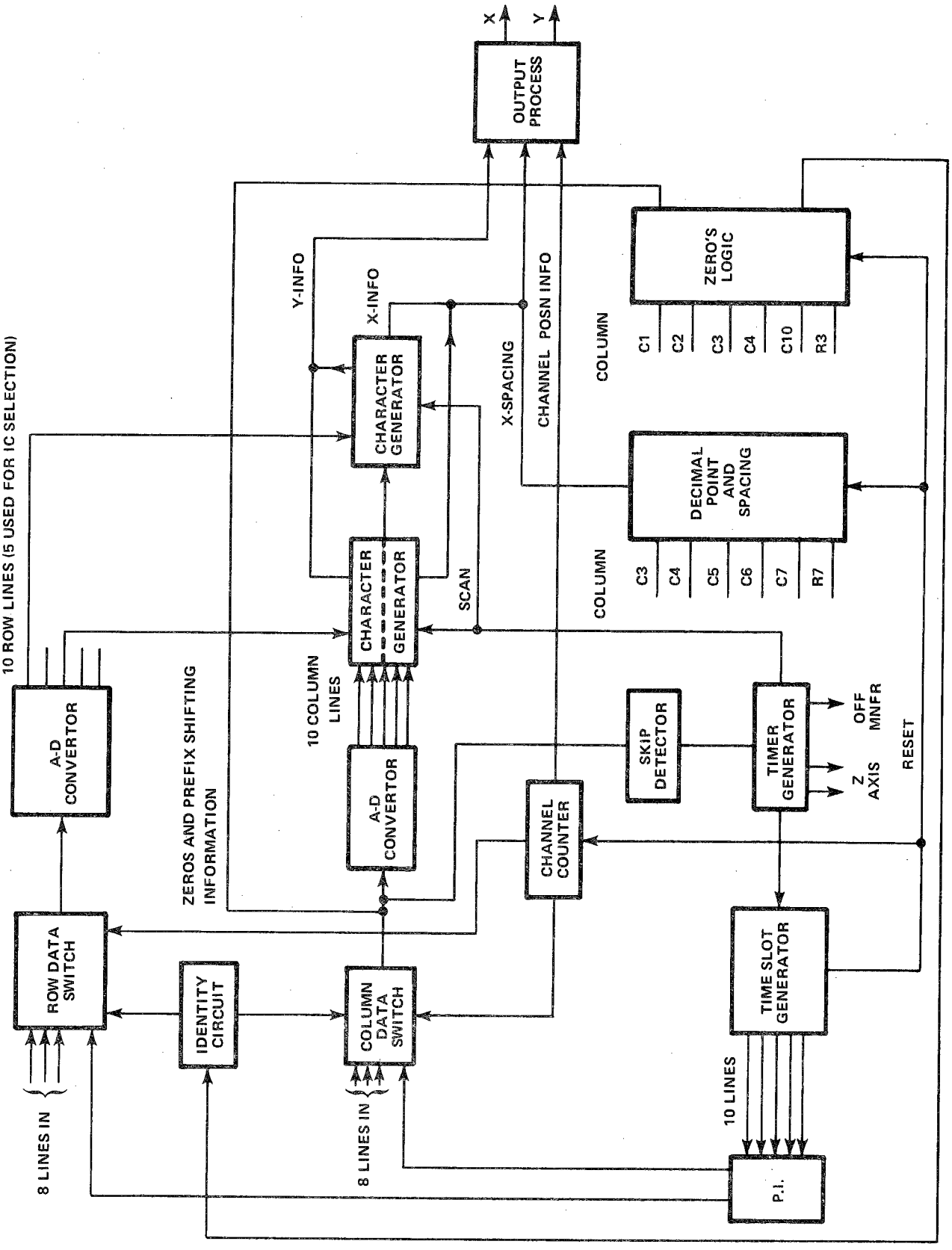


Figure 10. N. G. K. R. O. Block Diagram.

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Figure 10 is a basic block diagram of the complete readout system. Not all of the 14 Tek-made I.C.'s are shown, nor are all of the time slot lines, and data lines. This was done for simplicity sake, but the usefulness of the diagram is not destroyed. Each of the I.C.'s contained in the block diagram are listed below and its primary functions reviewed.

Timer

The Timer produces 7 time-related waveforms that coordinate the timing and sequence of overall operation. The 7 waveforms are:

1. A basic triangle signal from which all others are derived.

2. A 15 V pulse (derived from the basic waveform) to form the time slot pulse and drive the time slot counter.

3. Z-Axis OFF command to main frame logic.

4. The X-Y channel OFF command to main frame logic.

5. The Readout Z-Axis input to the main frame logic.

6. A Character Scan Triangle to character generators.

7. A trigger to time slot counter.

Some of the timing relationships of the above waveforms are shown in Figure 11. The illustration at the top (1) depicts one complete cycle of the readout system through all 8 channels. Then, 1 particular channel is expanded to show the timing relationships of the signals generated.

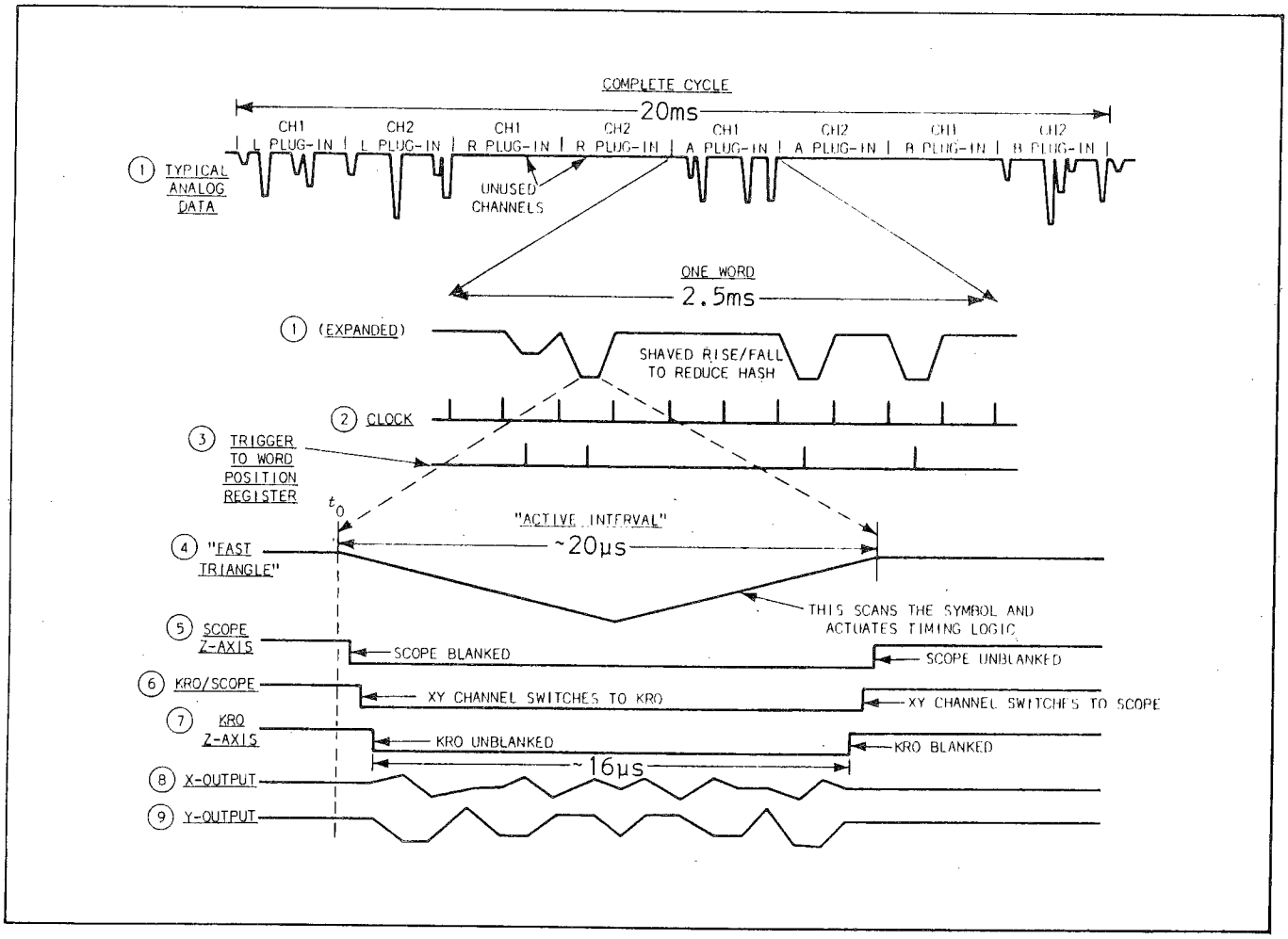


Figure 11. Some timing relationships.

Time-Slot Counter

A decade counter acting as a sequential switch. It directs the input signal (time-slot pulses) to one of its 10 output lines. Each successive input pulse appears on a different output line. The 10 output lines go to each plug-in.

The time-slot counter produces an "End of Word Pulse" at the end of time slot 10 which resets the Zeros Logic, advances the Decimal Point, and Spacing I.C., and Channel Counter.

Channel Counter

A binary-counter stage which provides the Column and Row Data switches with the code for selecting and sequencing through a total of 8 plug-in channels. The channel counter is sequenced after every 10 time slots by the Time-Slot Counter. It also provides the Format Generator with correct beam positioning information for each channel's readout.

Column and Row Data Switches

Receives the channel address code from the Channel Counter in order to select the proper plug-in channel. It accepts analog data from each plug-in channel for the duration of 10 time slots and provides a single time-multiplexed output to the Row and Column Decoders.

Display-Skip Generator

Monitors the time-multiplexed output of the Column Data Switch during each time slot. It detects the presence of data and instructs the Timer Generator to generate the sequence of logical commands which interrupt the normal scope display. If no data is present, the scope display is not interrupted.

Column and Row Decoders

Essentially, they are A/D Converters. They sense the magnitude of analog voltages at their inputs and produce a binary output on one of 10 lines. The particular output line selected during a time slot is dependent on the amplitude of the input signal.

These 2 stages select the characters to be displayed or the instructions to be executed. The selection is accomplished via a selection matrix code. For the duration of each time slot, only 1 character is displayed.

Zeros Logic and Memory

Provides a means of modifying the data at theiinput to the Column Decoder. During time slot 1, this circuit can store encoded data derived from attenuator probes (or "Mag"). Later, during time slots 5, 6, and 8, the memory contents are added to the data encoded by the plug-in. The result is a capability to add zeros or shift prefixes, thus allowing a "probe tip" scale factor display.

The Zeros Logic also instructs the identify circuit to respond whenever Column 10 and Row 3 are decoded during time slot 1. The word "IDENTIFY" is then constructed and displayed during time slots 2 through 9. The word which normally would have been displayed is deleted.

Decimal Point Logic and Character Position Counter

Produces a positioning current which is added to the X signal from the Character Generators. It is a stair-stepped waveform which positions each displayed character one character width to the right of the preceding one.

Also, if Row 10 and Column 0 are decoded, a step is generated. This would occur when an instruction for a space was received. In this case, however, no character is generated and the result is only a gap in the test.

Character Generator

Five I.C.'s which produce the X and Y positional currents to the Format Generator. The X and Y analog signals are produced after the character selection is made and a scanning voltage applied. Each I.C. can produce 10 different symbols.

One of the possible 10 output lines on both the Column and Row Decoders selects an individual character from 1 out of the 5 possible Character Generator I.C.'s. The Row Decoder selects the I.C. and the Column Decoder selects 1 out of the 10 characters contained in the I.C. A fast-ramp scanning voltage is then applied from the Timer and the selected character is generated by a series of strokes.

Format Generator

Takes the X-Y information from the Character Generator and produces the deflection voltages to the main frame

vertical and horizontal amplifiers. The Channel Address Code from the Channel Counter is added also to correctly position the starting point for each plug-in channel display. The stepping waveform from the Decimal Point and Spacing Generator is processed by the Format Generator to provide correct spacing between characters.

SOME ADVANTAGES AND CONSIDERATIONS

In summary, it may be well to list the advantages gained by this new readout system.

1. From a hardware point of view, the display capability is relatively unrestricted. The capability exists to display a wide variety of English text, numerals and symbols. The data can be displayed in any sequence desired.

2. Since the Selection current to the Character Generator I.C.'s is also a size-control signal, it would allow selection between 2 or more display sizes.

3. Additional text material can be added by expanding the number of I.C.'s used.

4. Due to all of the above, the Readout System is very compatible to more sophisticated measurement systems of the future.

The features listed in 2 and 3 above are not included in the present system, but can be incorporated in future versions.

The discussion would not be complete without also listing some of the limitations of the Readout System. Some of these considerations are:

1. Characters and symbols that are not continguous are not readily handled by the Character Generators. Some examples of this kind of text would be ! ? : ; etc.

2. Due to the fact that the alphanumeric system is a time-sharing system, there will be conditions in which gaps appear in the normal scope display due to blanking intervals.

On balance, however, these inconveniences are outweighed by the advantages. Especially the advantage of versatility--the adaptability for use with future systems.

READOUT CODING CONSIDERATIONS FOR TEK BASIC SOFTWARE

In order for 7000-series plug-ins to be compatible with the TEK BASIC software that processes readout from the plug-ins, a standard must exist. This section describes what software expects to see when evaluating scale-factors and digital readout provided by 7000-series plug-ins.

There are three types of information supplied by plug-ins. These types and their definitions are as follows:

SCALE FACTORS (Vertical and Horizontal Information). Scale factors designate the amplitude and units of either the vertical or horizontal displacements on a crt or target. Scale factors can always be separated into a numerical portion and a units portion.

DIGITAL MEASUREMENT. Any numerical information other than scale factors is treated as a digital measurement. Digital information consists of a numerical portion and a units portion.

TEXT. Any information produced by a plug-in that is not a scale factor or a digital measurement is treated as text by the software.

To determine what kind of information (scale factors, digital information, or text) is being produced by a plug-in, software looks at the character in several time slots (TS1 - TS1Ø). These characters are produced by the instrument main frame (such as a P7001) and are determined by the row and column currents present in the time slot from the plug-in.

In order for the determination to be made, one or more conditions must be met for each of the different types of information. These conditions are:

SCALE FACTORS. A valid scale factor is indicated by the presence of R3/C1* through C4 in TS1*, and at least one character other than spaces, deletes, or nulls in TS2 through TS1Ø.

DIGITAL MEASUREMENTS. A digital measurement is indicated by the presence of R2/C0 or R7/C0 in TS1. TS2 through TS1Ø contain the digital information.

TEXT. Textual information is assumed if none of the above requirements are met.

* R3 = Row 3, C1 = Column 1, TS1 = Time Slot 1.

When processing numeric information, the software expects to see the following information in the order presented. Refer to Fig. 3 for row and column interpretations. Unless otherwise indicated, each item may appear only once; however, no item is required except a digital number (for a valid scale factor of digital measurement).

UNCAL UNITS:

↓ (invert)

>< X (plug-in uncalibrated)

No more than two uncal units should appear, the first signifying that the waveform is inverted, the second that it is uncalibrated. If more appear, they are not properly processed.

DIGITAL NUMBER:

Ø - 9

A number is a string of digits with an optional decimal point. A decimal point locator (R7/C3 through C7) may appear before the number.

DIGITAL EXPONENT:

F p n u m K M G T (prefix) or

E ± dd (exponent expression, dd is two decimal numbers)

Only one prefix or exponent expression may occur. The exponent expression, if used, must appear as an "E" sign, and exactly two digits.

UNITS:

Any other characters.

The contents of any time slots remaining after the above items have been found are treated as units.

CHARACTERS IGNORED:

Once the software has determined the type of information present, the following characters are ignored:

Anything in Column Ø.

R2/C5 and C7 (except in digital exponent).

R3/C1 - C4 and C1Ø.

PROGRAMMING

Introduction

The General Purpose Interface Bus (GPIB) is thoroughly described in two documents:

(1) IEC Standard Interface System for Programmable Measuring Apparatus.

(2) IEEE Standard Digital Interface for Programmable Instrumentation (IEEE Standard 488-1975).

A system using the GPIB consists of devices which can be any combination of talkers, listeners, and controllers with a common bus joining them. A programmable 7000-series mainframe has an internal bus which is based on the GPIB.

Figure 1 is an example of a 7000-series instrument using programmable plug-ins.

Signal Names and Definitions

As can be seen in Figure 1, the plug-ins and Main Frame are devices on the internal bus. The 7000-Series Main Frame Logic decodes device dependent and interface messages, and controls the source and acceptor handshakes. Each plug-in must handle the same functions for itself.

The 7000-series instrument appears as only one device load on the GPIB, but contains five devices. The Main Frame and the four plug-ins each answer to the same primary addresses, but different secondary addresses.

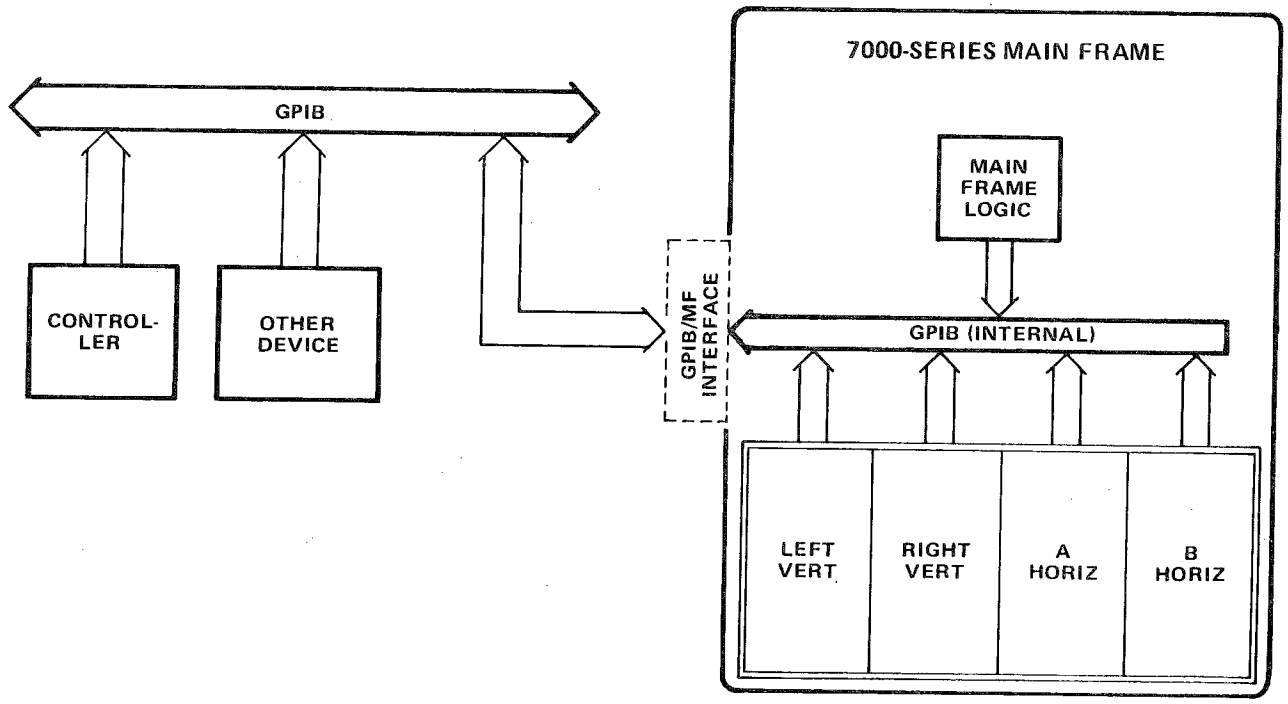


Figure 1. GPIB System diagram.

TABLE 1
GPIB Signals

Plug-In Pin Number	Signal Name	Use
A22	$\overline{EOI}$	No change to GPIB use and timing requirements.
B22	$\overline{SRQ}$	
B24	$\overline{ATN}$	
A24	$\overline{IFC}$	Must be clamped to +5 V max, and be able to sink 4 mA at 5 V. This is used by programmable plug-ins to detect if the Main-Frame is programmable.
A23	$\overline{DAV}$	Acceptor Handshake: same as GPIB. Source Handshake: see pp. 3, 4.
A25	$\overline{NDAC}$	
B25	$\overline{NRFD}$	
B23	REN (positive true)	This is the same as the GPIB line except when the Main Frame "Return To Local" button is pressed. When rtl is pressed and the main frame is in REMS (Remote State), REN is set false for 1 microsecond, which takes the plug-ins to LOCS (Local State). The external REN is unaffected. Subset RL2 (IEEE Std. 488-1975) occurs within the plug-ins and RL1 occurs within the Main Frame. The plug-ins must now respond to a 1-microsecond pulse on REN instead of the 100 microseconds specified in IEEE Standard 488-1975.
B26	$\overline{SND}$	Used by the plug-ins or Main Frame to indicate to the GPIB Source Handshake Function in the Main Frame that the device has a valid byte on the internal Main Frame data bus which should be retransmitted to the internal and external GPIB by the Main Frame Source Handshake.
A27	−5 V Power	Provides power for programmable plug-ins.
A26	Logic Common	Provides a common ground return for logic circuits.
B27	+5.1 V Power	Power for logic circuits in the plug-ins.

GPIB Modifications

The data bus in the 7704AP is based on the bus defined in IEEE Standard 488-1975, the GPIB. The functions which have been modified are Source Handshake and Remote/-Local. The Main Frame also decodes the plug-in addresses.

ADDRESS DECODING. The Main Frame modifies the information on the data lines if the data is a Primary Listen Address, Primary Talk Address, or Secondary Address. The byte is modified as follows (shown with a Primary Listen Address).

From Controller: XØ1L LLLL.

To Plug-In: XØ1X XXØ1 Not MLA for plug-in.
XØ1X XXØØ MLA for plug-in.
XØ11 1111 Unlisten.

REMOTE/LOCAL. The five GPIB devices (MF, LV, RV, AH, BH) in the box all have the same Remote/Local function. The MF has RL1 (complete) capability, and the plug-ins respond as shown in Figure 2.

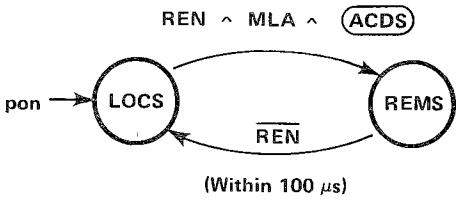


Figure 2.

The plug-ins must recognize a 1 μs pulse of REN = Ø, since this is how the MF tells the plug-ins that GTL was received or rtl was pushed. When the MF momentarily sets REN to Ø on the internal bus, the external GPIB remains unaffected. The plug-ins now do not have the GTL^ (LADS) ^ (ACDS) transition from REMS to LOCS. Instead, GTL is effective if the MF is in LADS.

REN on the internal bus is positive true, so that the MF may force REN to Ø internally even if there is an internal system controller.

DATA BUS. The eight-bit parallel data bus to the plug-ins is on A30-A33 and B29-B32, which carry TS-2 through TS-9 for non-programmable plug-ins (see Table 8). The maximum transfer rate which may be achieved by a plug-in talker is determined by T_α, the time required for the plug-in to drive the data bus back to the MF. T_α depends on the amount of pull-up current from the plug-in. (MF capacitance and T_α not yet specified.)

T_α = Data settling time, plug-in to MF* † measured from false transition of SND.

T_β = MFSH disable time after ATN asserted $\geq$ 200 ns, $\leq$ 300 ns.

T_γ = PISH data hold time after SND released $\geq$

SOURCE HANDSHAKE. There is only one source handshake function in the instrument (contained in the MF interface) and it is used by all five internal devices. There is only one source handshake function active at any time, so a common source handshake may be shared by all five devices. The only device message input to the SH State diagram in IEEE Standard 488-1975 is NBA (New Byte Available), so a ninth control line carrying this information (called SND) is added to the GPIB in the MF bus.

A data transfer from a plug-in to the rest of the plug-ins and the outside GPIB is a two-stage transfer. First, the plug-in talker asserts SND and places its data on the bus to the MF interface. When the plug-in releases SND, the MF latches the data and does the source handshake for the plug-in. State diagrams for the MF and plug-in source handshake functions are shown in Tables 2, 3, 4, 5, and in Figures 3 and 4.

Since the plug-ins do not contain the SH function, they do not have to read NRFD and NDAC, and do not have to drive DAV. The linkage from the MF SH function back to the plug-ins is on the DAV line, since NRFD and NDAC are not readable.

The Plug-In Receivers/Drivers state diagram (Figure 5) details when a particular plug-in is to enable its data bus by turning on its bus pull-ups. All other plug-ins must get off of the bus when another plug-in is asserting SND, since the diode logic on the bus results in a positive-true wire-ored bus, and a listening plug-in would drive the bus to all ones.

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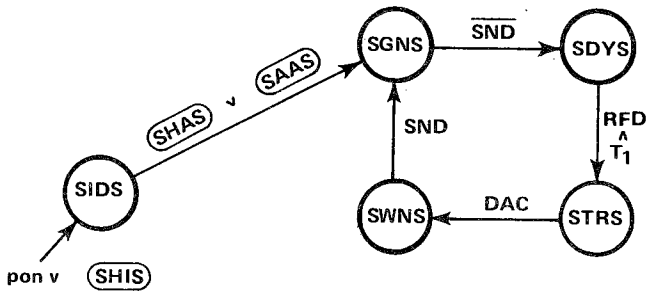
* Implementation dependent.

† First byte from internal controller, T_α > 350 ns.



* T_β is measured from assertion of ATN.

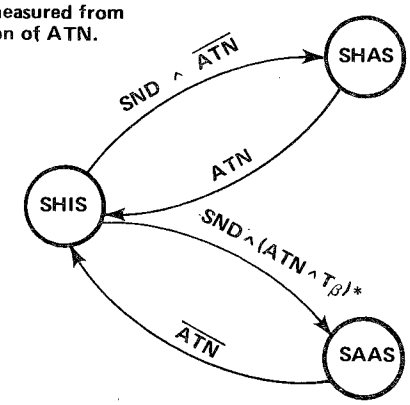
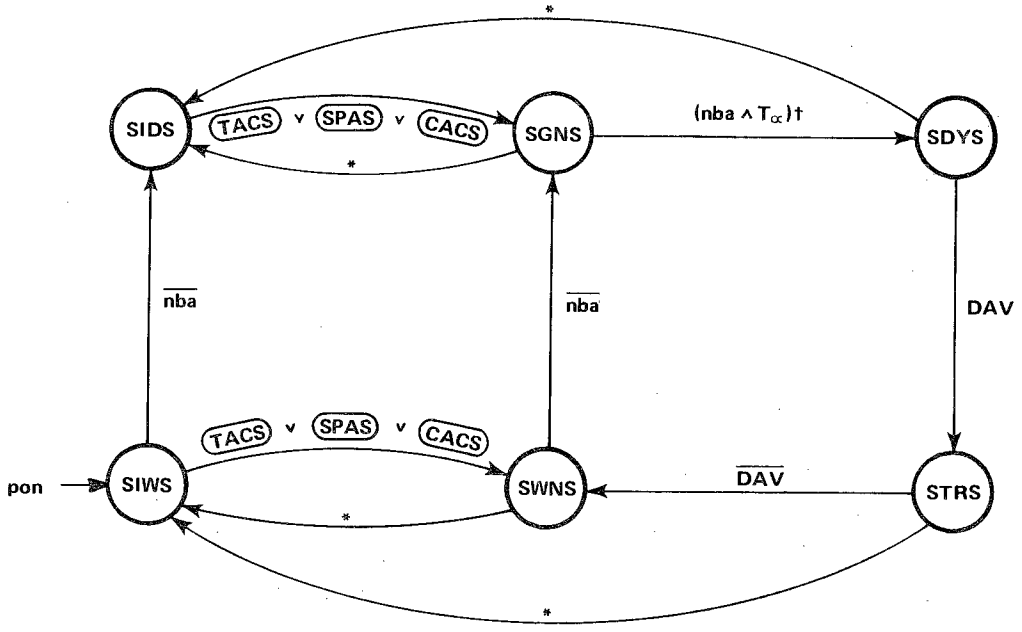


Figure 3. Main Frame Source Handshake (MFSH).

TABLE 2
MFSH Mnemonics

Messages	Interface States
pon = power on	SIDS = source idle state
ATN = attention	SGNS = source generate state
RFD = ready for data	SDYS = source delay state
DAC = data accepted	STRS = source transfer state
	SWNS = source wait for new cycle state
	SHIS = source handshake idle state
	SHAS = source handshake active state
	SAAS = source handshake attention active state



† T_α starts when nba goes true.

* (ATN ∧ $\overline{\text{CACS} \vee \text{CTRS}}$) v ($\overline{\text{ATN}}$ ∧ $\overline{\text{TACS} \vee \text{SPAS}}$) within T_2.

Figure 4. Plug-In Source Handshake (PISH).

TABLE 3
MFSH Message Outputs

SH State	Remote Message Sent: DAV	Device Function Interaction
SIDS	(F)	External data to internal bus.
SGNS	F	Internal data to external bus.
SDYS	F	Data latched, placed on both internal and external buses.
STRS	T	Data latched, placed on both internal and external buses.
SWNS	F	Data latched, or internal data to external bus

TABLE 4
PISH Mnemonics

Messages	Interface States
pon = power on	SIDS = source idle state
nba = new byte available	SGNS = source generate state
	SDYS = source delay state
DAV = data valid	STRS = source transfer state
	SWNS = source wait for new cycle state
	SIWS = source idle wait state
	(TACS) = talker active state; (SPAS) = serial poll active state } T function
	(CACS) = controller active state; (CTRS) = controller transfer state } C function

TABLE 5
PISH Message Outputs

PISH State	Main Frame Message Sent: SND
SIDS	(F)
SGNS	T
SDYS	F
STRS	F
SWNS	F
SIWS	(F)

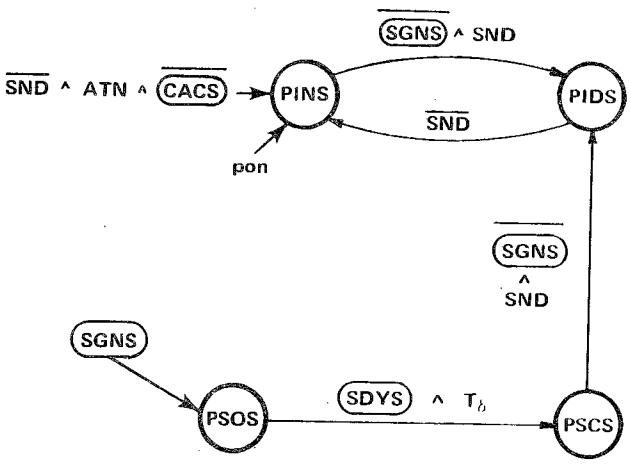


Figure 5. Plug-In Bus Receivers/Drivers (PIB).

TABLE 6
PIB Mnemonics

Messages	Interface States
SND = Plug-In Send	PINS = Plug-in bus input state PIDS = Plug-in bus idle state PSCS = Plug-in bus source change state PSDS = Plug-in bus source state SGNS = Source generate state (PISH) SDYS = Source delay state (PISH) CACS = Controller active state (C)

TABLE 7
PIB Driver/Receiver Handling

PIB State	Bus Pull-Ups	Data Direction	Data
PINS	on	input	data lines are inputs
PIDS	off		plug-in data lines are disabled
PSCS	on or off	output	data out may change
PSOS	on	output	data out may not change

Time-Slot Switching

For a programmable plug-in, the time-slot pulse lines A29 through A33 and B29 through B32 (B33 excluded) are switched to the internal GPIB data lines and one internal control signal called TSCLOCK.

Table 8 indicates the function performed by each time-slot/Data Line.

Figure 6 is a diagram of the DIODE switching logic necessary for each TS/DIO line.

TABLE 8
Time Slot/Data Lines

Pin Number	Standard Main Frame/ Programmable Main Frame
A29	TS10/TSCLOCK
B29	TS9/DIO8
A30	TS8/DIO7
B30	TS7/DIO6
A31	TS6/DIO5
B31	TS5/DIO4
A32	TS4/DIO3
B32	TS3/DIO2
A33	TS2/DIO1
B33	TS1/TS1

Intermixing of Standard and Programmable Main Frames and Plug-Ins

In a non-programmable (standard) Main Frame, the programmable plug-in interprets TS1 through TS10 as standard time-slots. Conventional row and column current information is sent by the programmable plug-in in either type of Main Frame.

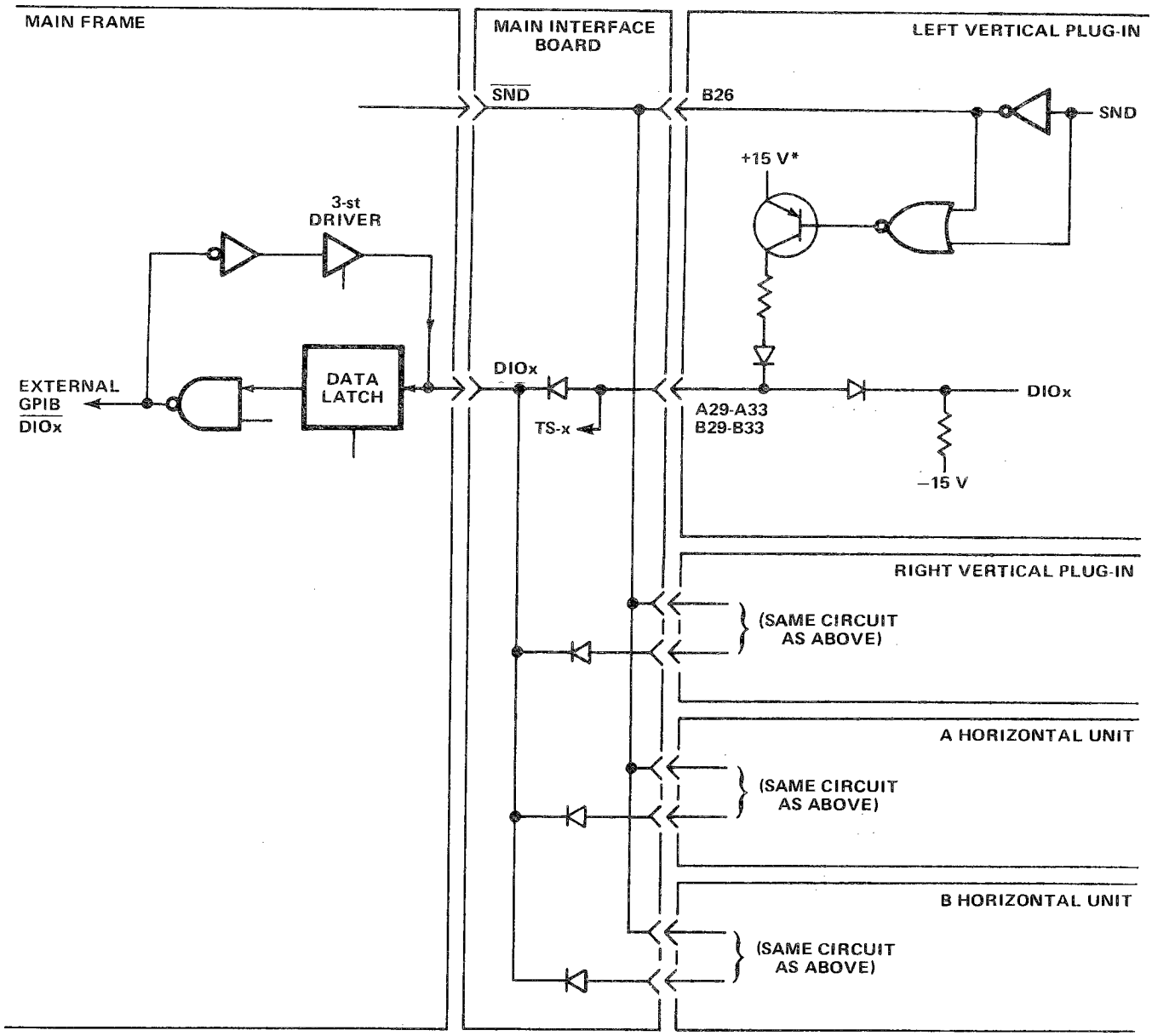
A programmable Main Frame senses the type of each plug-in and reacts as follows:

1) Standard plug-in: The time slots are used normally.

2) Programmable plug-in: Time slot 1 is unaffected and used as a sync pulse. Time slot 10 is a summation of all time slots (TSCLOCK). The summation signal drives a counter in the plug-in to determine time-slot sequence.

A programmable plug-in signals its type to the Main Frame by sourcing > 0.1 mA into TS-10 (at 0 V).

A programmable plug-in senses the Main Frame type on the IFC line. A non-programmable Main Frame leaves the pin open, while a programmable Main Frame clamps it so it may not rise above +5 volts. A plug-in may source no more than 1 mA into IFC at +5 volts.



*Switched off in a non-programmable main frame.

Figure 6. Programmable instrument typical diode switching logic.

MISCELLANEOUS INFORMATION

MISCELLANEOUS INFORMATION

7000-SERIES GATE NOMENCLATURE

There appears to be quite a bit of misunderstanding as to what types of + GATE outputs are available from our 7600 instruments. By trying out various 7000-series mainframes with a variety of time bases we found that:

(1) The 7300 and 7600 manuals are in error.

(2) There appears to be inconsistancy in the name chosen for a particular gate.

(3) The names chosen for these + Gates can easily result in confusion.

Corrective action is being taken on the manual errors; and in this article, I hope to clear up any misunderstandings in the gate nomenclature.

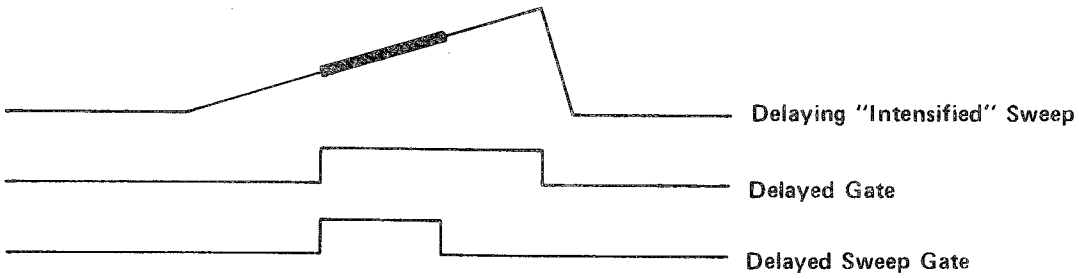
Gate Definitions

I. **Difference Between + Gate and + Sweep Gate.**

+ GATE: Positive during sweep time selected plus possibly more.

+ SWEEP GATE: Positive *only* during desired sweep time.

Example:



II. Gate Nomenclature Used.

Gate Name	Is Positive During:	Notes
Delaying Sweep Gate	ONLY during delaying (or main) "SAW" time.	Has been called: Main Gate, A Gate, and Sweep Gate.
Delayed Sweep Gate	ONLY during "SAW" time of delayed sweep.	Has been called: B Gate, DElayed Gate.
Delay Gate	TOTAL delay time plus previous hold-off time.	Used to generate external delayed trigger.
Delayed Gate	From delayed trigger to end of delaying sweep.	Inverse of DELAY GATE.
Mixed Sweep Gate	TOTAL time viewed on crt.	

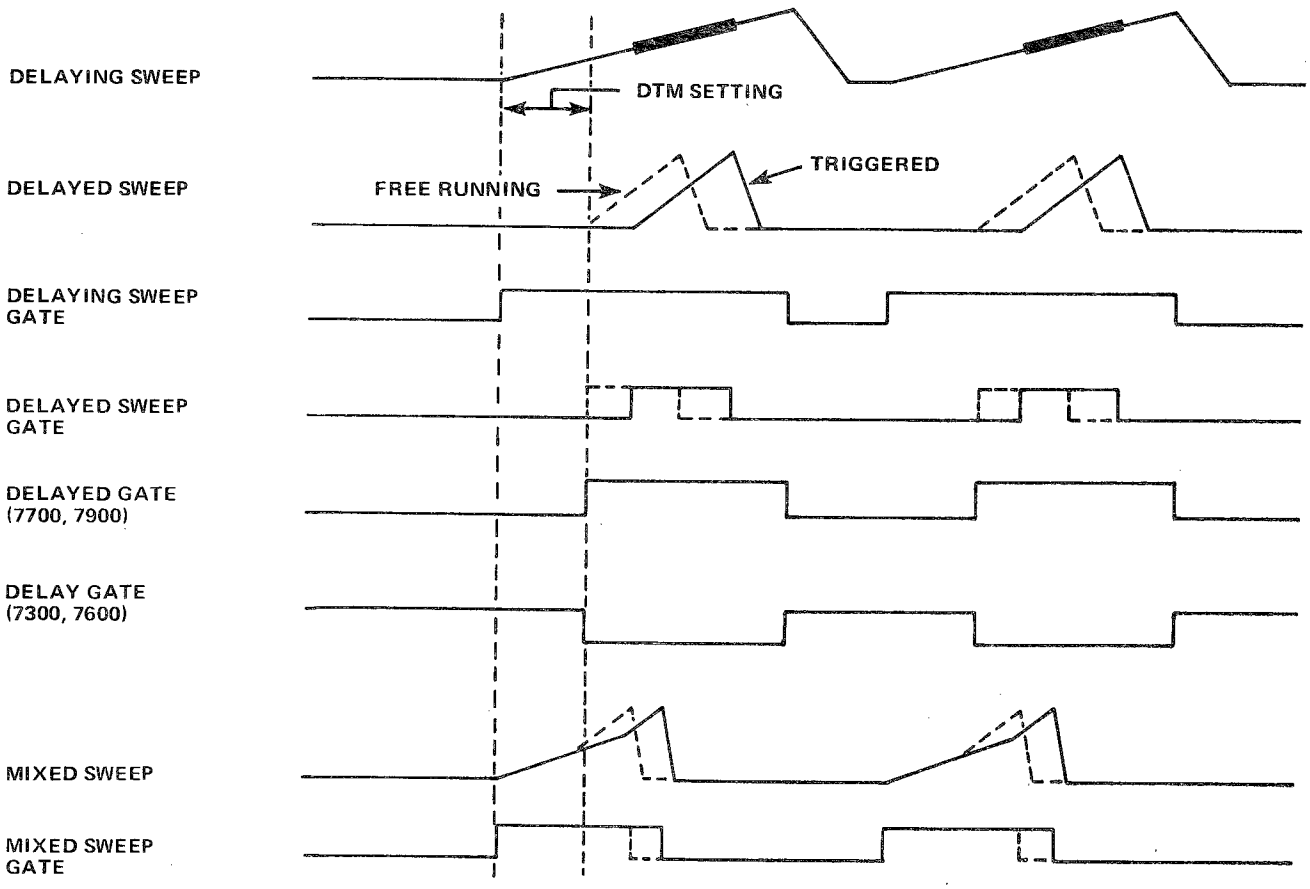


Figure 1. Timing diagram shown for "triggered delayed" operation.

DISPLAYED SWEEP OR GATE

A new term to identify the sweepoor gate that represents the sweep selected on the time base function switch, i.e., Mixed Sweep selected yields Mixed Sweep or Gate at the output. In other words, "What you see is what you get".

III. Instrument Combinations

7300 and 7600

Gate Selector Switch	7B50 7B70	7B51 7B71	7B52	7B53 (N, A, AN)	7B53AN MOD 769H	7B92
MAIN	Displayed sweep gate.	Displayed sweep gate.	Displayed sweep gate.	Displayed sweep gate.	Displayed sweep gate.	Displayed *
AUX	None.	None.	Delaying sweep gate.	Delaying Sweep gate.	Delaying sweep gate.	Delaying sweep gate.
DELAY	None.	Delay gate.	Delay gate.	None.	Delay gate.	None.
SAWTOOTH OUT	SWEEP OUT is always displayed sweep.					

*INTEN mode or INTEN ALT. DELAYED gives *DELAYED SWEEP GATE*. All other modes view DELAYED SWEEP therefore also output DELAYED SWEEP GATE.

NOTES:
1. Delayed Sweep Gate (used for counter gating) is available from 7B53 (N, A, AN) Ext Trig in jack.
2. Manuals are in error as they suggest the presence of a gate in the 7300 and 7600 instruments when used with the 7B53's and the gate function switch in the DELAY position. The manuals are being corrected.

7700 and 7900

Gate Selector	
A	Displayed Sweep Gate from plug-in A.
B	Displayed Sweep Gate from plug-in B.
DLY'D	DELAYED GATE with compatible plug-ins.*

Sweep Selector	
A	Displayed sweep from plug-in A.
B	Displayed sweep from plug-in B.

*Must have one of the following in plug-in "A" compartment (7B51, 7B52, 7B53AN Mod 769H, 7B71), and delaying sweep function selected. Plug-in "B" may be any time base unit.

Summary

The most used gates are available from all main frames except the 7400's. The most often confused are called DELAY in the 7300 and 7600 and DLY'D in the 7700 and 7900 main frames and do *not* mean the DELAYED SWEEP GATE which is probably what you were after when selecting this function.

To get this you have to either use a 7B53 (A, AN, N) or a 7B92. In the 7B53's, it comes out of the plug-in front panel, and for the 7B92 it depends on the main frame (see previous charts).

This information will appear in the Performance section of the 7000–Series General RB at the next updating.

——Ted Paulat
50-362
Ext. 6563