M377 COMPONENT SPECIFICATION

1. SCOPE

1.1. Document Description

This specification describes the requirements for an M377 in integrated die form. This component was first used in the 11A32, 11A33, 11A34 and 11A52 plug-in amplifiers.

1.2. Control Level

Not Applicable

1.3. Statement For Procurement

Not Applicable

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect at the date of shipment shall form part of this specification to the extent specified herein.

2.1.1	Visual Inspection	ICM-8-7
2.1.2	Component Evaluation	ICM-0-xxx
2.1.3	Electrical Test Specification	ICM-2A-203-0377-90
2.1.4	Plate Inspection	ICM-11-9
2.1.5	Wafer Probe Specification	ICM-1B-203-0377-01

3. REQUIREMENTS

3.1. GENERAL DESCRIPTION

The M377, when properly packaged, is a wideband general-purpose differential amplifier incorporating all the functions of a single-channel oscilloscope preamplifier except input buffering (transformation from 1 megohm input impedance to low impedance). Additionally, the outputs of up to four M377s may be combined in parallel to obtain two or four channel operation.

The M377 is 170 mils (4.32mm) by 115 mils (2.92mm) and is made with the SHF3 IC process, using 50 ohm per square nichrome, and double-layer vanadium-gold metalization. There are 556 NPN transistors, 177 PNP transistors (429 emitters), 90 unguarded schottky barrier diodes, 335 nichrome resistors, 202 active base resistors, and 70 capacitors totaling 199.4 pF in the M377.

3.2. GAIN SELECTION

Nominal gain may be selected in six steps (with a 2-5-10 sequence) from 1.2 to 60.0 using TTL gain select inputs G0, G1, and G2. In oscilloscope parlance, deflection factor is selected from 50 mV/division to 1 mV/division. Each division is defined here as 0.5 mA delivered to 100 ohms push-pull load impedance and thus is equal to 50 mV between each output terminal pair (e.g. between +OUT3 and -OUT3).

Typical M377 usage assumes that an attenuator precedes the M377 and that the M377 gain is set for less than full to allow for a variety of other possible system losses and tolerances. For example, an attenuator with a maximum dc gain of 0.93 requires that the M377 nominally operate with a gain of 1.07. At 50 mV/div, the maximum M377 gain is 1.20 with VAR set to full gain ($>+1$ volts). The M377 then has 11.6% extra gain available to make up for component tolerances, and temperature coefficients.

3.3. BANDWIDTH

The M377 bandwidth is a function of the gain as shown in the following table:

Deflection Factor	Nominal Gain	Bandwidth
50mV/div	1.2	1.0GHz
20mV/div	3.0	940MHz
10mV/div	6.0	880MHz
5mV/div	12.0	680MHz
2mV/div	30.0	470MHz
1mV/div	60.0	320MHz

On-chip bandwidth limit filters at either 100 MHz or 20 MHz may be invoked with TTL control lines B0 and B1. Both filters have four complex poles approximating a Bessel filter providing 24dB/octave attenuation outside the passband and low overshoot (approximately 2%) in the time domain. Although the transient response and frequency response shape are independent of IC processing parameters, the cutoff frequency is not. The cutoff frequency tolerance is $\pm$ 25%.

3.4. VARIABLE GAIN

The gain may additionally be controlled by an analog control voltage applied to the VAR input. Gain varies linearly from 0 to full with a VAR input of -1 volt to +1 volt. Input impedance of the VAR input is approximately 2K ohms.

The $\pm$1 volt references for the VAR control input are derived from an internal bandgap reference supply, and are largely independent of power supply voltages and temperature within 50ppm/$^\circ$C. This results in a VAR control temperature coefficient of less than 25 ppm/$^\circ$C.

The relationship between the voltage at the VAR input and the gain at a given coarse (or step) gain setting is given by the following equation:

$$GAIN=(VAR+1)/2$$ where VAR is the voltage at the VAR input.

The measured gain error based upon a a least squares fit to a straight line of VAR voltage vs measured gain is on the order of 2% from the predicted gain.

3.5. SIGNAL INPUTS

The input signal is applied differentially between +VIN and -VIN. Each input's impedance is greater than 100K ohms in parallel with 1pF, and input current is typically 20 uA (into the chip). The input circuitry is balanced and exhibits good common-mode rejection. Common mode input voltage range is plus and minus 1 volt from ground without change in gain or other specifications.

3.6. SIGNAL OUTPUTS

There are three identical push-pull outputs, each of which may be independently turned on, off, or inverted in polarity through TTL control signals. Inversion, turn on, and turn off are each achieved within 200 ns. Each output is laser trimmed at the wafer level for an output impedance of 50 ohms per side (suitable for single-channel operation), 100 ohms per side (suitable for two-channel operation when combined with another M377) or 200 ohms per side (suitable for four-channel operation when combined with three other M377s). An external 50 ohm per side load is also assumed. Therefore, in all three M377 versions, the total load (internal and external combined) on each output transistor collector is 25 ohms.

The output common-mode voltage is nominally zero whether an output is enabled or not, and the output impedance is unaffected by enabling or inversion.

3.7. POSITION CONTROL

Each 2 volts applied between the +POS and -POS inputs produces approximately one division output (50mV) between each pair of enabled output terminals, independent of gain selection (G2, G1, or G0) or variable (VAR) gain. All three outputs have exactly the same position control signal (if they are enabled). The sense of the position signal is inverted in any output which is inverted. The +POS and -POS inputs each has an input impedance of approximately 10K ohms returned to approximately -2 volts.

3.8. DIGITAL CONTROL

Three TTL inputs (G0, G1, and G2) select one of the six fixed gain settings according to the following table:

DEFLECTION FACTOR	GAIN	G2	G1	G0
50 mV/div	1.2	1	1	X
20 mV/div	3.0	1	0	X
10 mV/div	6.0	0	1	1
5 mV/div	12.0	0	1	0
2 mV/div	30.0	0	0	1
1 mV/div	60.0	0	0	0

Two TTL inputs (B0 and B1) select the bandwidth filters according to the following table:

BANDWIDTH	B1	B0
FULL	1	X
100MHz	0	1
20 MHz	0	0

STB is a level sensitive strobe input which must be a TTL 0 in order for the M377 to respond to G2, G1, G0, B1, or B0. Data transferred into the M377 when STB is 0 is latched when STB is brought to a TTL 1. This allows

several M377s to be bussed together and addressed independently. If STB is held at 0, the M377 will respond directly to TTL commands on G2, G1, G0, B1, and B0.

OUT1EN, OUT2EN, and OUT3EN must be TTL 1 to turn on their respective output terminal pairs.

OUT1INV, OUT2INV, and OUT3INV must be TTL 0 for non-inverting operation and TTL 1 for inverting of their respective outputs.

3.9. ACCURACY

The gain of each M377 is laser wafer trimmed to within 1% of nominal at the six fixed gain settings. Fine adjustment, if needed, is accomplished by adjusting VAR.

An internal bandgap reference makes the gain essentially independent of the power supply voltages.

Low frequency errors in frequency response (thermals) are a maximum of 0.1% at a VAR gain settings of +0.6 volts (80% of full gain) and -0.6 volts (20% of full gain). Thermals are a minimum at VAR gain settings of +1.0 volts (full gain) and 0 volts (half gain). At these settings, thermals are less than 0.05%.

The M377 gain changes less than 0.25% between FULL and either bandwidth limit filter and changes negligibly ($<$0.025%) with polarity inversion.

3.10. LINEARITY

Linearity is a function of how much of the dynamic range is used, but is intended to be adequate for use with 10 bit digitizers when the input does not exceed 40 times the fixed gain setting sensitivity, and the output does not exceed ten divisions (500 mV). For example, with the variable gain at full (VAR $>$ 1.0 volts), the maximum input at 50 mV per division is 500 mV (ten divisions), but with the variable at 20% of full gain (VAR = -0.6 volts), the maximum input is 2.0 volts (40 X 50 mV/div), even though this is only eight divisions (2 volts/.25 volts per division) of output signal. Position control inputs (+POS and -POS) may be used to increase the maximum input signal by reducing the output deflection to less than ten divisions. For example, with the variable gain set to full and nine divisions of position control input, the maximum input signal at 50 mV/div is 0.9 volts (19 divisions X 50 mV per division).

The following table summarizes the maximum differential input voltage as a function of deflection factor (gain) with VAR input at +1.0V:

DEFLECTION FACTOR	GAIN	G2	G1	G0	Maximum Input
50 mV/div	1.2	1	1	X	2.0 volts
20 mV/div	3.0	1	0	X	0.8 volts
10 mV/div	6.0	0	1	1	0.4 volts
5 mV/div	12.0	0	1	0	0.2 volts
2 mV/div	30.0	0	0	1	80 mV
1 mV/div	60.0	0	0	0	40 mV

3.11. TEMPERATURE COEFFICIENT

The M377 gain remains within 1% of its 25 ° C value from 0 ° C to 100 ° C, however, the temperature coefficient of gain may have a slope of up to 300ppm/ ° C over parts of the temperature range. The VAR control does not adversely affect gain stability by more than 25 ppm/ ° C. The chip is trimmed at a temperature of 40 ° C.

DC drift is less than 0.0002 divisions per degree centigrade referred to the output plus 6.4 microvolts per degree centigrade referred to the input.

3.12. NOISE

Noise is approximately 17 nV RMS (or 3.4E-07 divisions RMS) per square root Hz referred to the output plus 3.6 nV per square root Hz referred to the input. At 50 mV per division this amounts to 0.008 divisions RMS in a rectangular bandwidth of 500 MHz.

3.13. OVERDRIVE RECOVERY

Overdrive occurs when the input signal exceeds approximately 60 divisions or when the output exceeds 15 divisions of deflection.

Recovery from overdrive to within 0.04% of the input signal plus 0.1 divisions referred to the output is within 10 ns for input signals not exceeding 2.5 volts. It is in overdrive recovery performance that the M377 exceeds the performance of earlier preamplifiers most spectacularly.

3.14. HIGH FREQUENCY ADJUSTMENT

Each output has a high frequency gain control (HFADJ). A more negative voltage on HFADJ increases the M377 gain at frequencies above approximately 250 MHz. The total range is 3 dB gain change at 800 MHz for an input of approximately plus and minus 1.0 volt. Since the three outputs match each other very closely, normally it is possible to connect all three HFADJ inputs together. However, in the event that circuit conditions external to the M377 are not identical for all three outputs, individual HFADJ inputs are provided. Input impedance of each HFADJ control is approximately 2K ohms.

3.15. POWER CONSUMPTION

The M377 nominally consumes 2.160 watts plus 0.30 watts for each enabled output. Full bandwidth and 20 MHz bandwidth limit modes reduce dissipation by 197 mW and 103 mW respectively. Normal variations in nichrome sheet resistance, and other factors, will cause a 15% variation in dissipation. Current in VEE5 and VCC5 are independent of the supply voltages. Current in the +15 volt supply is roughly proportional to the +15 volt supply.

Power dissipation with no outputs enabled is given in the following table.

POWER SUPPLY	CURRENT	POWER	CURRENT	POWER	CURRENT	POWER
Bandwidth	FULL	FULL	100MHz	100MHz	20MHz	20MHz
+15V	0.041A	0.615W	0.041A	0.615W	0.041A	0.615W
+5V	0.078A	0.390W	0.092A	0.460W	0.085A	0.425W
-5V	0.192A	0.960W	0.217A	1.085W	0.203A	1.015W
TOTAL		1.965W		2.160W		2.055W

Power dissipation with all three outputs enabled is given in the following table.

POWER SUPPLY	CURRENT	POWER	CURRENT	POWER	CURRENT	POWER
BWL	FULL	FULL	100MHz	100MHz	20MHz	20MHz
+15V	0.041A	0.615W	0.041A	0.615W	0.041A	0.615W
+5V	0.168A	0.840W	0.182A	0.910W	0.175A	0.875W
-5V	0.282A	1.410W	0.307A	1.535W	0.293A	1.465W
TOTAL		2.865W		3.060W		2.955W

3.16. Electrical Requirements

3.16.1. ABSOLUTE MAXIMUM RATINGS

An absolute maximum rating defines a bias, mechanical stress, or environmental condition beyond which the device may become unserviceable.

Symbol	Identification	Min.	Max.	Units
Tj	Operating Junction Temperature	-15	125	°C
Tstg	Storage Temperature	-60	125	°C
VCC15	+15 volt supply	-0.3	+20	V
+VIN	non-inverting signal input	-5	+5	V
-VIN	inverting signal input	-5	+5	V
VAR	variable gain control input	-10	+10	V
VEE5	-5 volt supply	-6	+0.3	V
OUT1INV	output 1 polarity control (TTL)	-1	+10	V
OUT1EN	output 1 enable control (TTL)	-1	+10	V
VCC5	+5 volt supply	-0.3	+6	V
OUT2INV	output 2 polarity control (TTL)	-1	+10	V
OUT2EN	output 2 enable control (TTL)	-1	+10	V
OUT3INV	output 3 polarity control (TTL)	-1	+10	V
OUT3EN	output 3 enable control (TTL)	-1	+10	V
-OUT3	output 3 negative signal	-2.5	+5	V
+OUT3	output 3 positive signal	-2.5	+5	V
HFADJ3	output 3 high frequency adjust input	-2	+2	V
-OUT2	output 2 negative signal	-2.5	+5	V
+OUT2	output 2 positive signal	-2.5	+5	V
HFADJ2	output 2 high frequency adjust input	-2	+2	V
-OUT1	output 1 negative signal	-2.5	+5	V
+OUT1	output 1 positive signal	-2.5	+5	V
HFADJ1	output 1 high frequency adjust input	-2	+2	V
+POS	non-inverting position analog input	+20	-20	V
-POS	inverting position analog input	+20	-20	V
VCC5	+5 volt supply	-0.3	+6	V
VEE5	-5 volt supply	-6	+0.3	V
B1	bandwidth limit control bit 1 (TTL)	-1	+10	V
B0	bandwidth limit control bit 0 (TTL)	-1	+10	V
G2	gain select bit 2 (TTL)	-1	+10	V
G1	gain select bit 1 (TTL)	-1	+10	V
G0	gain select bit 0 (TTL)	-1	+10	V
STB	data strobe for gain and bandwidth (TTL)	-1	+10	V

CAUTION:

This product is sensitive to static charges and care should be taken in handling. +VIN and -VIN are especially sensitive as they connect directly to input transistor bases.

Any power supply voltage or combination of voltages may be disconnected without harm to the M377, and there are no power supply sequencing requirements. Either or both of the two inputs, +VIN or -VIN, may be open circuited temporarily without M377 degradation. Long term effects of open circuited inputs have not been evaluated.

3.16.1.1. Assembly

Die Attach	1 minute maximum	400 ° C
Wire Bond	1 minute maximum	350 ° C
Bake out/Lid Attach	2 hours maximum	175 ° C

3.16.2. Performance Characteristics

3.16.2.1. Initial Test Conditions

Pad No.	Parameter	Minimum	Nominal	Maximum	Units
1	VCC15	+14.8	+15.0	+15.2	V
2	+VIN	-.05	0	+.05	mV
4	-VIN	-.05	0	+.05	mV
5	VAR	+1.2	+1.25	+1.3	V
6	VEE5	-5.05	-5.00	-4.95	V
7	OUT1INV	+0.78	+.80	+.82	V
8	OUT1EN	+1.95	+2.00	+2.05	V
10	VCC5.	+4.95	+5.00	+5.05	V
11	OUT2INV	+0.78	+.80	+.82	V
12	OUT2EN	+1.95	+2.00	+2.05	V
13	OUT3INV	+0.78	+.80	+.82	V
14	OUT3EN	+1.95	+2.00	+2.05	V
17	HFADJ3	-.5	0	+.5	V
20	HFADJ2	-.5	0	+.5	V
23	HFADJ1	-.5	0	+.5	V
24	+POS	-20	0	+20	mV
26	-POS	-20	0	+20	mV
29	B1	+0.78	+0.80	+0.82	V
30	B0	+0.78	+0.80	+0.82	V
31	G2	+1.95	+2.00	+2.05	V
32	G1	+1.95	+2.00	+2.05	V
33	G0	+1.95	+2.00	+2.05	V
34	STB	+0.78	+0.80	+0.82	V

3.16.2.2. Electrical Characteristics

No.	Symbol	Conditions and notes	Minimum	Typical	Maximum	Units
1	Ro+OUT1	50, 100, or 200 ohms	-1.0		+1.0	%
2	Ro-OUT1		-1.0		+1.0	%
3	Ro+OUT2		-1.0		+1.0	%
4	Ro-OUT2		-1.0		+1.0	%
5	Ro+OUT3		-1.0		+1.0	%
6	Ro-OUT3		-1.0		+1.0	%
7	Av 50	Initial conditions (IC)	1.188	1.200	1.212	
8	Av 20	G2=+2.0V G1=+0.8V G0=+2.0V	2.970	3.000	3.030	
9	Av 10	G2=+0.8V G1=+2.0V G0=+2.0V	5.940	6.000	6.060	
10	Av 5	G2=+0.8V G1=+2.0V G0=+0.8V	11.88	12.00	12.12	
11	Av 2	G2=+0.8V G1=+0.8V G0=+2.0V	29.70	30.00	30.30	
12	Av 1	G2=+0.8V G1=+0.8V G0=+0.8V	59.40	60.00	60.60	
13	Vos 50	G2=+2.0V G1=+2.0V G0=+2.0V			15	mV
14	Vos 20	G2=+2.0V G1=+0.8V G0=+2.0V			15	mV
15	Vos 10	G2=+0.8V G1=+2.0V G0=+2.0V			15	mV
16	Vos 5	G2=+0.8V G1=+2.0V G0=+0.8V			15	mV
17	Vos 2	G2=+0.8V G1=+0.8V G0=+2.0V			15	mV
18	Vos 1	G2=+0.8V G1=+0.8V G0=+0.8V			15	mV
19	Vcm 1	IC	-25	0	+25	mV
20	Vcm 2	IC	-25	0	+25	mV
21	Vcm 3	IC	-25	0	+25	mV
22	Avoff 1	IC OUT1EN=+0.8V			.005	
23	Avoff 2	IC OUT2EN=+0.8V			.005	
24	Avoff 3	IC OUT3EN=+0.8V			.005	
25	Avinv 1	IC OUT1INV=+2.0V	.99975	1.0000	1.00025	
26	Avinv 2	IC OUT2INV=+2.0V	.99975	1.0000	1.00025	
27	Avinv 3	IC OUT3INV=+2.0V	.99975	1.0000	1.00025	
28	Avbwfull	IC B1=+2.0V	0.9975	1.000	1.0025	
29	Avbw100	IC B1=+0.8V	0.9975	1.000	1.0025	
30	AvPOS	IC	0.020	0.025	0.030	
31	VARlin-.75	IC	-20.0		+20.0	%
32	VARlin-.50	IC	-3.0		+3.0	%
33	VARlin-.25	IC	-2.0		+2.0	%
34	VARlin 0	IC	-2.0		+2.0	%
35	VARlin+.25	IC	-2.0		+2.0	%
36	VARlin-.50	IC	-3.0		+2.0	%
37	VARlin+.75	IC	-2.0		+2.0	%
38	VAR+int	IC	0.95	1.00	1.05	V
39	AvVARoff	IC VAR=-1.07V	-.05		+.05	%
40	VARBAL		−15	0	+15	mV
41	FULLBAL	IC B1=+2.0V	−15	0	+15	mV
42	100MHzBAL	IC B0=+2.0V	−15	0	+15	mV
43	20MHzBAL	IC	−15	0	+15	mV
44	OUT1BAL	IC OUT1EN=+0.8V	−10	0	+10	mV
45	OUT2BAL	IC OUT2EN=+0.8V	−10	0	+10	mV
46	OUT3BAL	IC OUT3EN=+0.8V	−10	0	+10	mV
47	MAXB		0	na	+20	mV

3.16.3. Schematic Diagram

See attachments

3.17. Mechanical Requirements

3.17.1. Physical Dimensions

Physical dimensions shall conform to Figure 1.

3.17.2. Die Size

Die size will be 115 x 170 mils

3.17.3. Die Thickness

Die thickness will be 19 to 21 mils.

3.17.4. Bond Pad Size

Minimum bonding pad size will be 4 x 4 mils for signal carrying bond pads. All other pads will be 5 x 5 mils.

3.17.5. Pad Identification

Pad#	Name	Input/Output	Description
1	VCC15	power supply	+15 volt power supply
2	+VIN	signal input	non-inverting signal input
3	GND	ground	
4	-VIN	signal input	inverting signal input
5	VAR	analog input	variable gain control input
6	VEE5	power supply	-5 volt power supply
7	OUT1INV	TTL input	output 1 polarity control
8	OUT1EN	TTL input	output 1 enable
9	GND	ground	
10	VCC5	power supply	+5 volt power supply
11	OUT2INV	TTL input	output 2 polarity control
12	OUT2EN	TTL input	output 2 enable
13	OUT3INV	TTL input	output 3 polarity control
14	OUT3EN	TTL input	output 3 enable
15	-OUT3	signal output	output 3 negative signal
16	+OUT3	signal output	output 3 positive signal
17	HFADJ3	analog input	output 3 high frequency adjustment
18	-OUT2	signal output	output 2 negative signal
19	+OUT2	signal output	output 2 positive signal
20	HFADJ2	analog input	output 2 high frequency adjustment
21	-OUT1	signal output	output 1 negative signal
22	+OUT1	signal output	output 1 positive signal
23	HFADJ1	analog input	output 1 high frequency adjustment
24	+POS	analog input	non-inverting position input
25	GND	ground	
26	-POS	analog input	inverting position input
27	VCC5	power supply	+5 volt power supply
28	VEE5	power supply	-5 volt power supply
29	B1	TTL input	bandwidth limit control bit 1
30	B0	TTL input	bandwidth limit control bit 0
31	G2	TTL input	gain select bit 2
32	G1	TTL input	gain select bit 1
33	G0	TTL input	gain select bit 0
34	STB	TTL input	data strobe for gain and bandwidth limit

3.18. Marking Requirement

3.19. Design and Construction

3.19.1. Process

SHF3 IC processing with double-layer vanadium-gold metalization and 50 ohms/square thin film nichrome are required. Unguarded Schottky barrier diodes are employed. There are no zener diodes.

3.19.2. Package and Materials

Top metalization shall be Gold, suitable for Gold thermo-compression ball bonding.

Die will not be Gold backed.

Die will be surface coated with glass with the exception of bonding pad areas and scribe lines.

Die topology will be as shown in Figure 1.

3.20. Product Assurance

3.20.1. Product Conformance

Devices supplied to this specification shall meet all the requirements specified for the product. The devices shall be identical with respect to design, materials, and manufacturing processes to products that have previously been qualified and approved by ICO (Integrated Circuit Operations). Substitute items shall not be shipped without prior written approval from ICO Products Management.

3.20.2. Reliability

HCO (Hybrid Circuit Operations) shall be responsible for demonstrating the achieved reliability level by testing the complete hybrid. This responsibility will begin with pre-production prototypes and will continue through the production life of the component. When correctly used within the electrical and thermal limits specified, this die is expected to achieve an intrinsic failure rate model as follows:

Base Failure Rate	.025%/1000 Hrs (90% CL)
Reference Junction Temperature	75 °C
Activation Energy (Arrhenius model)	1 electron Volt

Evidence clearly indicating die reliability less than the specified level will require corrective action by ICO.

4. QUALITY ASSURANCE PROVISIONS

4.1. Responsibility for Inspection

Unless otherwise specified ICO is responsible for the performance of all inspection requirements. In addition, HCO Incoming Inspection may perform any incoming quality testing necessary to assure the supplied components conform to requirements of this specification. ICO will maintain adequate quality history records and make them readily available to the HCO group upon request.

4.2. Quality Conformance Inspection

Characteristics	Document	LTPD, C=1
Inoperative Parts (25 °C)	Section 3.2.2	7.0
Visual	Section 2.1.1	7.0
*Mechanical	Section 2.1.2	
DC Electrical Parameters	Section 2.1.3	7.0

*These characteristics are inspected for conformance as per 2.1.2 Component Evaluation.

5. PREPARATION FOR DELIVERY

5.1. Packaging

Die shall be packaged as per 2.1.4

5.2. Package Marking

The unit package will be marked to include the following information:

a. Part number
b. Quantity
c. Lot Number
d. Date Code

5.3. Certificate of Compliance

QA Stamp of Compliance, certifying the lot meets all specified requirements, shall be placed on each wafer pack in a lot.

6. NOTES

6.1. Definitions

6.1.1. Ro

Output resistance at terminal designated by the letters following Ro. Ro is the ratio of the change in open circuit output voltage at the specified terminal divided by the change in short circuit current. The open circuit voltages and short circuit currents are generated by applying a voltage to +VIN and/or -VIN.

6.1.2. Av

Voltage gain at all output terminal pairs at the sensitivity designated by the numbers following Av. For example, Av 20 is the voltage gain from terminals +VIN and -VIN to the +OUT3 and -OUT3 terminal pairs as well as to the other two output terminal pairs at 20 mV/div. This measurement is made with a plus and minus 150 mV (plus and minus three division) output signal. The voltage gain is the short circuit current flowing between output terminal pairs multiplied by 50 ohms and divided by the voltage difference between +VIN and -VIN. This method allows all three versions of the M377 to be tested using the same test fixture.

6.1.3. Vos

Offset voltage between +VIN and -VIN required to set the voltage measured between any output terminal pair equal to zero at the sensitivity designated by the numbers following Vos.

6.1.4. Vcm

The common mode voltage at the output terminal pair designated by the number following Vcm. The common mode voltage is the mean of the two short circuit output currents of any terminal pair multiplied by 25 ohms.

6.1.5. Avoff

The voltage gain at the output terminal pair designated by the number following Avoff with the output off divided by Av at the same sensitivity. Voltage gain measurement is made with a plus and minus 3 division input signal at 50 mV/div.

6.1.6. Avinv

The voltage gain at the output terminal pair designated by the number following Avinv divided by Av at the same terminal pair at the same sensitivity. Measured at 50 mV/div for convenience.

6.1.7. Avbwfull

The low frequency voltage gain at any output terminal pair in the full bandwidth mode divided by the voltage gain at the same terminal pair in 20MHz bandwidth limit mode.

6.1.8. Avbw100

The low frequency voltage gain at any output terminal pair in the 100 MHz bandwidth limit mode divided by the voltage gain at the same terminal pair in 20MHz bandwidth limit mode.

6.1.9. VARlin

Deviation of the voltage gain (Av) vs. VAR control voltage from a straight line. Av is measured at 50 mV/div with VAR input voltages of -0.5, -0.25 0.0, +0.25, +0.50, and +0.75. A least squares fit to a straight line characterization using six voltages is calculated. Gain error at each of seven VAR control voltages is calculated as one minus the ratio of measured gain to predicted gain. Express as a percent.

6.1.10. VAR+int

The VAR voltage at which the least squares fit to a straight line determined above intercepts full gain (VAR=1.2 volts).

6.1.11. VAR-int

The VAR voltage at which the least squares fit to a straight line determined above intercepts zero gain (VAR=-1.2 volts).

6.1.12. AvVAROff

The gain of the M377 from input to output at 50mV/div divided by 1.2 (the nominal gain at 50mV/div) with the VAR control off (VAR=-1.07V). Multiply by 100 and express as percent.

6.1.13. OUT1BAL, OUT2BAL, and OUT3BAL

Set the variable control to zero gain (VAR=−1.2V), select 20MHz bandwidth limit and set the output to the non-inverting mode. Measure the output voltage. Designate this reading as PVOUT1, PVOUT2, or PVOUT3. Invoke the invert mode for the output in question and remeasure the output voltage. Designate this voltage as IVOUT1, IVOUT2, or IVOUT3. For each output, the balance error is the average of the two readings:

OUT1BAL=(PVOUT1+IVOUT1)/2 OUT2BAL=(PVOUT2+IVOUT2)/2 OUT3BAL=(PVOUT3+IVOUT3)/2

6.1.14. 20MHZBAL

The 20MHz mode dc balance error can be calculated directly as the average of the differences between the voltage readings obtained in the previous section.

20MHzBAL=(PVOUT1−IVOUT1+PVOUT2−IVOUT2+PVOUT3−IVOUT3)/6

6.1.15. 100MHzBAL

The same procedure is used to measure the 100MHz mode dc balance errors as the 20MHzBAL except, of course, the M377 is in the 100MHz mode (B0=ttl high, B1=ttl low) when all output error voltages are measured.

100MHzBAL=(PVOUT1−IVOUT1+PVOUT2−IVOUT2+PVOUT3−IVOUT3)/6

6.1.16. FULLBAL

The same procedure is used to measure the FULL mode dc balance errors as the 20MHzBAL except, of course, the M377 is in the FULL mode (B1=ttl high).

FULLBAL=(PVOUT1−IVOUT1+PVOUT2−IVOUT2+PVOUT3−IVOUT3)/6

6.1.17. VARBAL

When the variable control is set to zero gain (VAR=−1.2V), the variable control circuit has no dc balance error. That is the principle which allows us to make measurements of the various other dc balance errors. When the variable is set to full gain (VAR=+1.2V), the variable control itself produces no dc balance error, but the first stage dc balance errors come right through the variable circuit and appear in its output. To eliminate the first stage dc balance errors, it is necessary to apply a voltage to the input which counteracts the first stage dc balance error. We know that we have accomplished this when the output voltage (eg PVOUT2) is the same with VAR=+1.2V as it is with VAR=−1.2V. The output voltage change between VAR=+1.2 and VAR=−1.2V should be less than 2mV before continuing.

Set VAR=0.0V and measure the output voltage, V3. The variable control dc balance error is V3−V1.

VARBAL=V1−V3

6.1.18. MAXB

The MAXB measurement is a mathematical manipulation of the measurements already made.

If VARBAL is the same sign as the largest (in magnitude) of the three bandwidth limit dc balance errors: MAXB is the sum of the largest of the three output errors, the largest of the three bandwidth limit dc balance errors, and VARBAL all taken without regard to sign.

If sign(VARBAL)=sign(BWLmax):

$$MAXB = |OUTmax| + |BWLmax| + |VARB|$$

where |OUTmax| is the largest absolute value of OUT1BAL, OUT2BAL, OUT3BAL and |BWLmax| is the largest absolute value of FULLBAL, 100MHzBAL, and 20MHzBAL.

If VARBAL is opposite in sign of the largest (in magnitude) of the three bandwidth limit dc balance errors: MAXB is the sum of the largest of the three output errors, and the largest of the three bandwidth limit dc balance errors. VARBAL is zero.

If sign(VARBAL)≠sign(BWLmax):

$$MAXB = |OUTmax| + |BWLmax|$$

MAXB will always be a positive number.

6.2. Applications Information

The M377 requires no external biasing resistors and therefore may be mounted in a relatively simple package. Because of the power dissipation, it is recommended that the chip be mounted directly on ceramic substrate. Although power dissipation is moderately high, the sources of heat on the chip are diffuse enough that ordinary ceramic suffices.

Power supply decoupling is required primarily to reduce the effects of switching an output on or off. The resulting 30 mA current change can induce common mode signals in the input bases through the power supplies. If the two input bases are not connected to nearly identical impedances, some of this common mode signal will be converted to a differential input signal.

+POS and -POS are connected to the signal path through 9.8K ohm resistors inside the M377. In order to avoid a frequency response error due to loading at +POS or -POS, these terminals should be connected to a voltage source of not more than 1K ohms impedance. If +POS and -POS are unused, they should be connected to ground.

Full utilization of the bandwidth available requires that transmission lines of the appropriate impedance be used to connect signal leads to the surrounding circuit. In the case of the 200 ohm per side output impedance version of the M377, this is not practical. In this case, all four M377s must be mounted in close proximity or significant bandwidth degradation will occur.

The Hypcon connector system is ideally suited to meet the requirements of power dissipation and superior high frequency performance. The M377 has already been packaged in a 1.22 cm Hypcon package according to the following table:

Output impedance	Trimmed IC part number	Hybrid part number
50 ohms	to be assigned	165-2089-00

100 ohms	203-0377-90	165-2089-05
200 ohms	203-0428-90	165-2089-06

The M377 has also been packaged in a 1.22 cm Hypcon package along with a 50 ohm input termination, a diode bridge input protection network, and with an input for input base current pull-away. The part number for this hybrid is 165-2129-02, and it is trimmed for an output impedance of 100 ohms for two channel operation.

Any real implementation of the M377 will require that various sources of dc balance error be calibrated out. Depending upon the application, it may also be desirable to calibrate out gain errors. To do either of these tasks requires a knowledge of the error sources within the M377. A diagram of these sources, if not attached, is available from Brian Rhodefer. Two useful pieces of information not mentioned in the specifications are essential for implementing automatic calibration routines:

1. When an M377 output is not enabled, the output offset is truly zero and may be relied upon to calibrate subsequent circuitry.

2. When the variable gain is set to zero (VAR = -1.1V) the balance error at the output of the variable control is zero. This allows one to calibrate out dc balance errors arising from the bandwidth limit stages and the output stages. Use of the invert function will allow separation of bandwidth limit balance errors from output amplifier balance errors.