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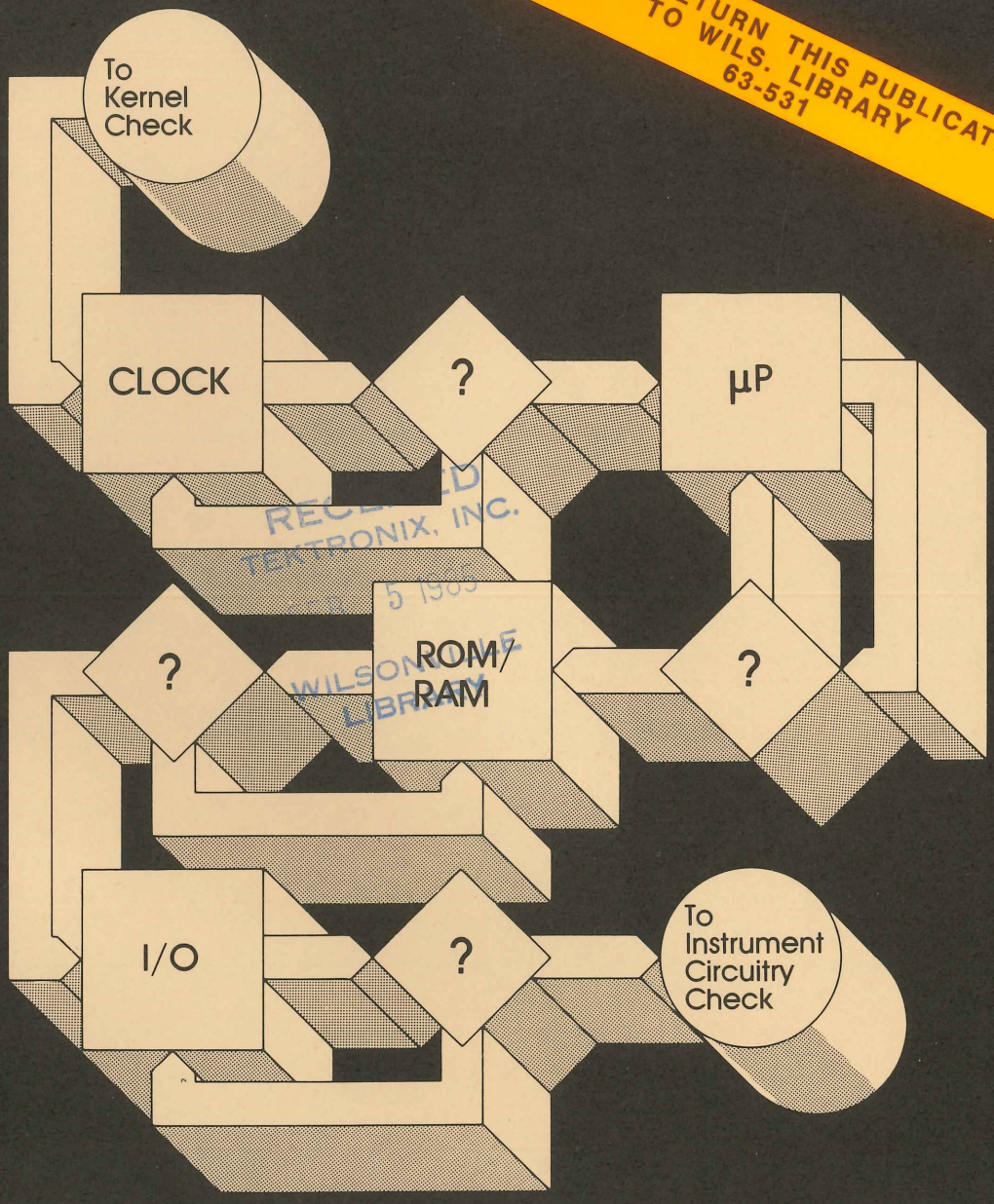

Designed-in diagnostics for processor-based products

DESIGNED-IN DIAGNOSTIC FEATURES FOR PROCESSOR-BASED INSTRUMENTS

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Almost all Tektronix business units now produce processor-based products. Computers and microprocessors have proved their usefulness in our products, but they have brought problems with them. Examples are: software, documentation, software support, standardization, and serviceability. We will examine one solution to the serviceability problem: designed-in diagnostic features (including firmware, hardware and supporting documentation). ("Designed-in diagnostic" features are also called "internal-diagnostic" or "self-diagnostic" features; "self-diagnostic" usually refers only to power-up self-tests.)

First, we'll look at the major advantages of enhancing serviceability using designed-in diagnostics, then define a diagnostic strategy, and finally discuss concepts that product and diagnostic designers can use when implementing the strategy.

ADVANTAGES

There are several major advantages of using designed-in diagnostic features for processor-based products. First, a product with designed-in diagnostic features doesn't require sophisticated or dedicated service equipment...which means less investment in specialized equipment and less training for field service personnel.

Second, designed-in diagnostic features make products more saleable. With such features, customers who service their own instruments can do so more easily than with other service techniques. Also, customers know they won't have to buy specialized test equipment.

Third, designed-in diagnostic features enhance manufacturability. Using designed-in diagnostic features alone, manufacturing test people may not be able to find problems that usually occur only in manufacturing (solder and tin bridges, wrong parts, and reversed IC's, for example). However, these features provide functional testing in the instrument, reducing the sophistication required of board testers. If diagnostic features are adequate for servicing an instrument in the field, they will also be adequate for diagnosing component failures in manufacturing.

Fourth, designed-in diagnostic programs allow the servicer to troubleshoot a product in its operating environment. The servicer doesn't have to assume, sometimes incorrectly, that all timing and other conditions have been duplicated during troubleshooting.

Fifth, product development costs less because there is less duplication of effort. With designed-in diagnostic features, no longer will designers use one diagnostic technique for testing prototypes, manufacturers another for production-line testing, and field service technicians still another.

The sixth reason for designing diagnostic features into a product is more abstract but, perhaps, also more important. If a product has such features, then at least part of the service strategy was indeed *designed* and not simply tacked on after releasing the product to manufacturing.

GLOSSARY

Kernel: a processor with its clocks, bus, some RAM and ROM, and an input/output port. The amount of memory and the kind of I/O port used depend on the instrument.

RAM: as used here, RAM means read/write memory.

Servicer: as used here, "servicer" means anyone who is troubleshooting an inoperative instrument. The term implies that designed-in diagnostic features should benefit engineering, manufacturing and field service personnel alike.

STRATEGY

The diagnostic strategy for processor-based instruments is simple: verify kernel operation and then use the kernel to verify other circuits. Troubleshooting moves from the kernel outward.

A basic principle underlying all designed-in diagnostic features is that, as much as possible, the diagnostic procedure must not depend on untested circuitry. There will be some chicken-and-egg problems; for example, a ROM diagnostic routine may have to assume the chip-select circuits work. But if the diagnostic routine reports an error, the servicer should have a chip-select test program available to help decide whether the chip-select circuits or ROM is at fault. So, a designer must decide which circuits are most likely to fail and then design the diagnostic program accordingly.

REQUIREMENTS

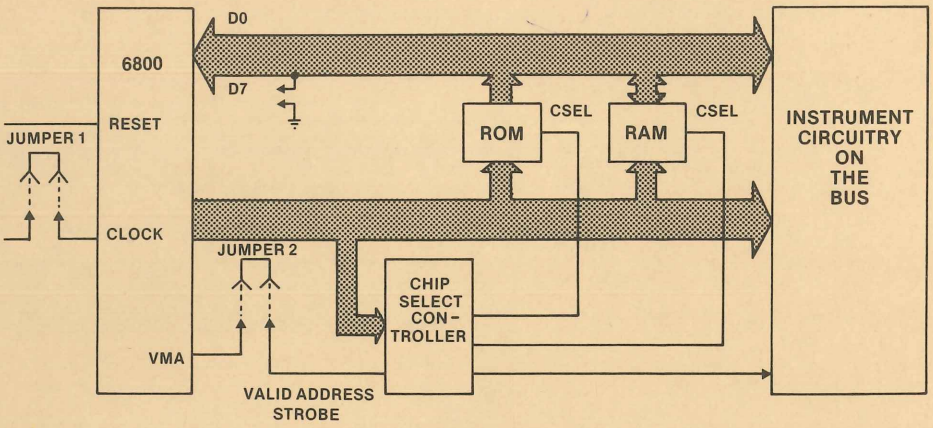
The strategy of kernel-outward verification and diagnosis is suitable for all processor-based products. In general, products designed with this strategy will require the following four designed-in diagnostic features, regardless of a product's complexity. Meeting these requirements (in the order they are presented below) constitutes a bootstrap procedure for verifying the kernel.

First, the system clock must be able to free run and there should be some way to isolate clock circuits from other circuits (if the other circuits are defective, they may load down the clock). When necessary, the designer can include jumpers to enable free-running and to isolate clocks from clocked circuitry.

Second, the processor must be able to free-run independently of conditions on its bus. This allows the processor to put repetitive signals on the data, address and control lines. To provide this, the designer can include jumpers that force the processor to repeatedly execute one instruction without addressing memory (in this stage of instrument verification or troubleshooting, memory hasn't been tested).

There are various ways to force an instruction. Figure 1 shows one way for a 6800 microprocessor. As an alternative, Hewlett-Packard Co. suggests DIP switches to latch data lines to various instructions (the instructions are processor-dependent). Microprocessor manufacturers may be able to recommend an approach. Regardless of the chosen solution, the idea is to use the microprocessor as a multiple-signal generator. (If you find new solutions, we would like to hear from you).

Third, the designer must provide hardware that forces the processor to begin executing instructions at the address of the first diagnostic routine in ROM. One way to do this is to start the diagnostic routine at the processor's power-up or restart vector address, or, if an external interrupt line is available, the designer can use its hardware vector address.



STEP	DATA LINES	R/W	ADDRESS LINES	OPERATION	STEP	DATA LINES	R/W	ADDRESS LINES	OPERATION
1	7F	R	PC	Fetch the Opcode (7F = CLR).	3	7F	R	PC+2	Fetch low-address byte.
2	7F	R	PC+1	Fetch high-address byte (of address to clear).	4	00	W	7F7F	Clear location 7F7F. Go to step 1 with the new.

Figure 1. Here's an example of "forced instruction" mode jumpering of a MC6800 microprocessor. Removing jumper 2 from the 6800's VMA disconnects the enabling signals from the chip-select circuitry. This disables everything else on the bus, causing the data lines to float (tristate). The servicer can then use the removable jumper to ground the data 7 line. The pullup resistors on the other data lines cause the 6800 to read a 7F (CLR) instruction from the data lines. The 6800 then repetitively steps through the cycles shown in the table.

During fetch cycles, the processor fetches "clear" instructions. During the execute cycles, the processor clears the data lines causing them to go low. Since the memories supply no data, the processor endlessly repeats this process. The address bus counts each bit toggling at twice the rate of the next higher-order bit, and the data lines toggle together. The resulting signals are forced onto the address and data lines independently of the operation of the circuits on the bus. This allows stuck-bus fault troubleshooting.

The fourth requirement is obvious, but should be kept in mind. There must be some way for the diagnostic routine to display error messages and some way for the servicer to input commands.

THE BOOTSTRAP

With the four designed-in diagnostic features, a servicer can verify and troubleshoot the kernel using the bootstrap sequence shown in Figure 2.

First, the servicer verifies the clock is running (step 1), removing the troubleshooting jumper if necessary. Next, the servicer puts the processor in forced instruction mode (step 2), and (with the clock connected) verifies the presence of correct signals in the processor circuitry. Continuing, the servicer disables the forced instruction mode and activates the hardware-forced vector to run the first diagnostic routine.

The first diagnostic routine should test the ROM in which the diagnostic routine resides. The diagnostic routine's starting address should be the hardware vector address. In some products, this means the servicer would turn off the product ("power down") and then turn it on again ("power up") to start or restart the diagnostic routine. Once the diagnostic routine has checked the ROM that holds the routine (step 3), the routine verifies the other ROM, the RAM (step 4) and the I/O circuits (step 5).

Testing the I/O circuits means checking circuits that the servicer uses to communicate with the instrument: front panel switches and

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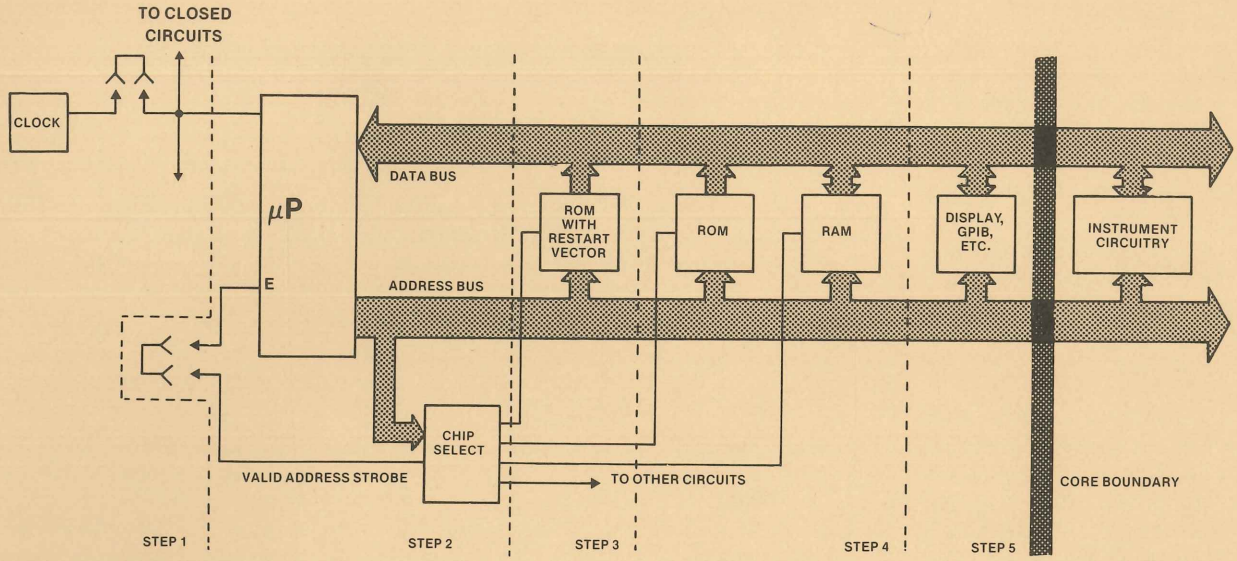

Figure 2. A servicer can verify or troubleshoot the kernel by following a step-by-step strategy. The strategy requires four designed-in diagnostic features: (1) a free-running clock, (2) a free-running processor that operates independently of bus conditions, (3) hardware that forces the processor to begin executing instructions at the address of the first diagnostic routine in ROM, and (4) there must be some way for diagnostic routines to display error messages and some way for the servicer to input commands.

lights, or an external interface (GPIB and RS232 for example).

ERROR DISPLAY

Now that we've seen an overview of the designed-in diagnostic strategy, let's look at implementations. The first concern is error display.

A servicer needs to know when a diagnostic program finds an error. A designer might decide (for example) to wink the front panel lights in code, with each code pattern representing one error condition. However, if the front panel circuits have failed, the diagnostic routine may not be able to display the code. One way the designer can eliminate this problem is placing LED's on the processor board. The servicer can "read" these indicators during the first diagnostic routine tests (before the diagnostic routine checks the I/O). When a test finds no errors, it should not turn off all displays to indicate a "pass" condition. Otherwise, a defective instrument may appear okay.

SELECTABILITY

When powered up, most processor-based instruments immediately run ROM and RAM verification routines. These routines should not disable instrument operation when they detect an error unless operation will damage the instrument. For instance, a ROM test might uncover a checksum error resulting from a ROM address not used in the customer's application. In some cases, you may decide to make all diagnostic routines selectable so servicers can run them as they need them.

Most designers "chain" diagnostic routines, but it's usually best to allow the servicer to run one routine at a time. In some cases, the servicer may select routines using the instrument's front panel which has been set up by switching or program control for use in a diagnostic mode. Or the designer can provide diagnostic routine select switches on the processor circuit board. Another way to select diagnostic routines is to use microprocessor "flag" outputs and "sense" inputs for direct communication with a terminal. But many of an instrument's circuits must be operative before the processor can run the terminal's control software.

DOCUMENTATION

Servicers need troubleshooting procedures to use with designed-in diagnostic features. A common form for such documentation is a troubleshooting tree showing what measurements to make, what the valid signal conditions are, what procedures to follow, and what components to replace. A troubleshooting tree usually is either a flowchart or a series of yes/no questions referenced to other parts of the tree. Instrument service manuals usually contain these trouble-shooting procedures plus descriptions of the diagnostic routines.

TEST INSTRUMENTS

A servicer may measure signals using various tools: logic probes, frequency and transition counters, oscilloscopes, signature analyzers, logic analyzers, or a combination of these.

For very simple circuits, a valid condition may simply be a high, a low, or a transition. Troubleshooting complex circuits may require identification of complex data streams. Signature analysis is an interesting technique because it identifies complex digital signals with little test equipment, and because a circuit defect is more likely to produce an invalid signal in a circuit than is the case with other measurement techniques.

UNIQUE SIGNALS

Refer again to figure 1. If two data lines are shorted together, a measurement may not detect the condition because the lines (except

data line D7) are toggling together anyway. Generally a diagnostic routine can't detect a short if the shorted signals are identical. Wherever possible, designers should provide unique signals.

THE COMPLETENESS TRADEOFF

Even the most sophisticated diagnostic program can't identify all failures. The designer faces a tradeoff: design and programming effort versus the percentage of failures caught by the diagnostic programs. The issue here is one of defining the acceptable percentage, and of expending sufficient effort to achieve it.

There will always be a few failures that require a staff engineer's attention. When such failures occur in the field, the servicer may have to swap boards. This issue is particularly relevant to the kernel of any processor-based instrument. It is harder to isolate failures in this circuitry than in other circuitry once the intelligence of the kernel is available to run diagnostic routines. Board swapping should be available for field failures which can not be diagnosed with designed-in features.

Designers should attempt to limit the kernel to one board or module which is easily replaced. This is not always easy or possible. Packaging constraints can limit the size of boards to the point where the kernel may require as many as three boards. In some cases, it is possible to put a small amount of ROM and some error indicators on the processor board, and to configure some kernel diagnostics in that ROM.

If the kernel is on a large board with other circuits, you might include jumpers or switches to allow isolation of the kernel from the circuitry on the bus.

HANG THE BUS

Bus hang-ups can be a problem unless the product includes bus buffering, latching or other intermediate circuits. Bus-structured instruments lend themselves to temporary swapping of a known-good kernel to isolate hang-up problems. Interconnect boards seldom have problems, but you can design a simple test card to check them out if necessary.

SIMPLIFICATION

Without designed-in diagnostic features, troubleshooting bit-slice designs, multiprocessor, or independently-controlled asychronous circuits while they're running requires service equipment with such features as multiple trigger inputs, and multichannel data pattern recognition. *Or* the designer can provide designed-in diagnostic features to simplify troubleshooting (for instance, the designer can provide jumpers that enable one asynchronous clock at a time.) Breakpoints should be provided in circuits that are self-resetting, self-clocking or that have feedback loops. (This applies to any complex digital circuit, not just bit-slice or expanded processing circuits).

To minimize the diagnostic measurement problem, a designer can reduce the number of interdependent processes that produce the measured signal. Usually this means providing individual enables so that each function can be independently exercised.

RECOMMENDED READING

Very little literature is available for designed-in diagnostic features for processor-based instruments. But we do recommend **A Designer's Guide to Signature Analysis** Hewlett-Packard Application Note 222.

ACKNOWLEDGEMENTS

We would like to extend thanks to the following people. Some provided encouragement, and others provided suggestions.

Randy Dietrich, Digital Service Instruments Engineering
Linely Grimm, F.D.I. Engineering
Gary Hoselton, Medical Products Engineering
John Lewis, T.V. Products Engineering
Roger Marin, T.V. Products Engineering

In a later issue, Chuck and Dave will discuss diagnostic strategy for circuits outside the kernel. □

IN PRINT

HIGH-PERFORMANCE SAW FILTERS

Bill Drummond (Instrument Research, Tek Labs) presented "Application of High-Performance SAW Transverse Filters in a Precision Measurement Instrument," a paper for the IEEE Ultrasonic Symposium in September 1978. For a copy of the paper, call Bill Drummond on ext. 6907.□

UV-CURABLE SYSTEMS

Doug Reed (Electrochemical Support) presented "Applications of UV-Curable Systems in the Electronics Industry," a paper for the UV Curing Conference in September 1978. For a copy of the paper, call Doug Reed on ext. 5182.□

INCIDENTAL CARRIER PHASE MODULATION

Charlie Rhodes (T.V. Products Engineering) presented "Measurement and Control of Incidental Carrier Phase Modulation in Visual Transmitters," a paper for the IEEE Fall Broadcasting Conference. For a copy of the paper, call Charlie on ext. 7068.□

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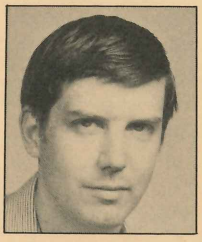
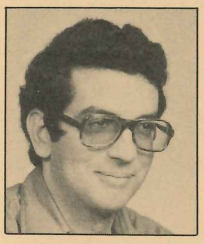
NBS TRACEABLE TRANSITION TIME MEASUREMENTS AT TEK



Bob Cram, Electrical Standards (T&M Operations), ext. 5397.



Al Caravone, Electrical Standards (T&M Operations), ext. 5397.

Electrical Standards now has a NBS-traceable transition-time calibration procedure for fast pulse generators (for pulses with transition times less than 200 ps). We can also display pulse distortions (aberrations) for pulsers (pulse generators) being tested as they would appear on the NBS Automatic Pulse Measurement System (APMS).

Electrical Standards will now reference all pulse distortion measurments for calibrated pulsers to the NBS system. Comparison with the NBS APMS is as close to traceability as we can come at this time. The calibration, though not strictly traceable, will be an in-house standard for future Tektronix pulsers, sampling instruments, and high-speed scopes.

Electrical Standards' calibration efforts have also produced a technique that calibrates the 7S12 TDR/Sampler time base with an uncertainty of 1% at sweep speeds of 50 picoseconds per division and slower. The deconvolution software we developed for transition time calibration also enables us to measure the step response of 2-port devices. We used a 100-picosecond Debye lossy transmission line filter to verify the deconvolution routines; the filter is available for use as a precision transition-time spoiler.

NEW TERMS

In Electrical Standards we are using the same terms and methods used by NBS. Because NBS has adopted the International Electrotechnical Commission standard on Pulse Techniques and Apparatus (IEC 469) and because Tektronix has made a commitment to NBS traceability, we must follow the IEC 469 standard. IEC 469 is essentially identical to IEEE standards 184 and 191.

CALIBRATING THE SAMPLING SYSTEM

A pulser under test is observed on Electrical Standards' sampling system which consists of a 7S12 TDR/Sampler, a S6 Sampling Head and a S53 Trigger Recognizer in a 7704A/P7001 Digital Processing Oscilloscope (DPO). A DEC 11/35 minicomputer, using SPS TEK BASIC software, controls the DPO. We calibrate the S6 against our

GLOSSARY

Baseline: the reference line at the 0% level of the waveform.

Deconvolution: a mathematical method used here to "subtract" the effects of a system's response function. It is the time-domain equivalent of dividing out system impulse response frequency-domain components.

Histogram: an occurence-density distribution graph (figure 4 is an example). Flat parts of a measured waveform show up as peaks in a histogram because many points on the waveform are digitized to the same level.

Minimum Radius of Curvature (MROC) points: a Tektronix term for the two points that bracket the transition at which the waveform "bends" most sharply.

Pulse distortion: the percentage difference between a reference waveform and the measured waveform. The two waveforms are compared point by point.

Root-sum-square rule: the relation for Gaussian pulses which states that a system transition time will be the square root of the sum of the squares of the component transition times. This rule is often used when one component transition time is known and the remaining transition time is to be determined.

Topline: the reference line for the 100% level on the measured waveform.

Transition time: The time between the 10% and 90% points on a transition waveform. According to the IEC469 standard: in a positive-pulse waveform, the rise time is the first transition duration and the fall time is the last transition duration.

Traceable specification: a specification that can be traced back to the National Bureau of Standards through a documented chain of calibrations and intermediate standards.

Waveform epoch: the total time span over which a display device presents waveform data. For scopes, this would be the sweep speed times 10 divisions.

standard pulser (a modified S52) using digitized waveform data from NBS. We convolute a "correction function" (see figure 1) with the acquired S6 waveforms to make our system emulate the NBS APMS. This allows us to standardize pulse distortion and arrive at repeatable transition time measurements. The 7S12 time base is calibrated directly against a 3.2 GHz sinewave.

FINDING THE TRANSITION TIME

See figure 2. Measuring transition time involves two separate measurements to obtain: (1) the 0% level (baseline) and the 100% level (topline) over a long waveform epoch of 10 nanoseconds (1 nanosecond per division sweep) and (2) the actual transition duration between the 10% and 90% points on a short waveform epoch of 500 picoseconds (50 picoseconds per division sweep). See figure 3 for an example of long and short waveform epochs.

We compute base and toplines with the pulse positioned within the long epoch such that the baseline portion occupies approximately the first 30% and the topline occupies the remaining 70% of the epoch. Electrical Standards' sampling system is programmed to determine baseline and topline from the occurence density distribution (see figure 4 for an an example) of the processed pulse waveform in the 10 nanosecond epoch. The waveform yields a bimodal histogram. The magnitudes at which the greatest number of occurences in the base histogram and the top histogram occur are chosen as the baseline and topline respectively. Our sampling system then acquires and processes a new waveform with a 500 picosecond waveform epoch to determine the time duration between the 10% and 90% points. The DPO acquires several waveforms and averages them to improve the signal-to-noise ratio.

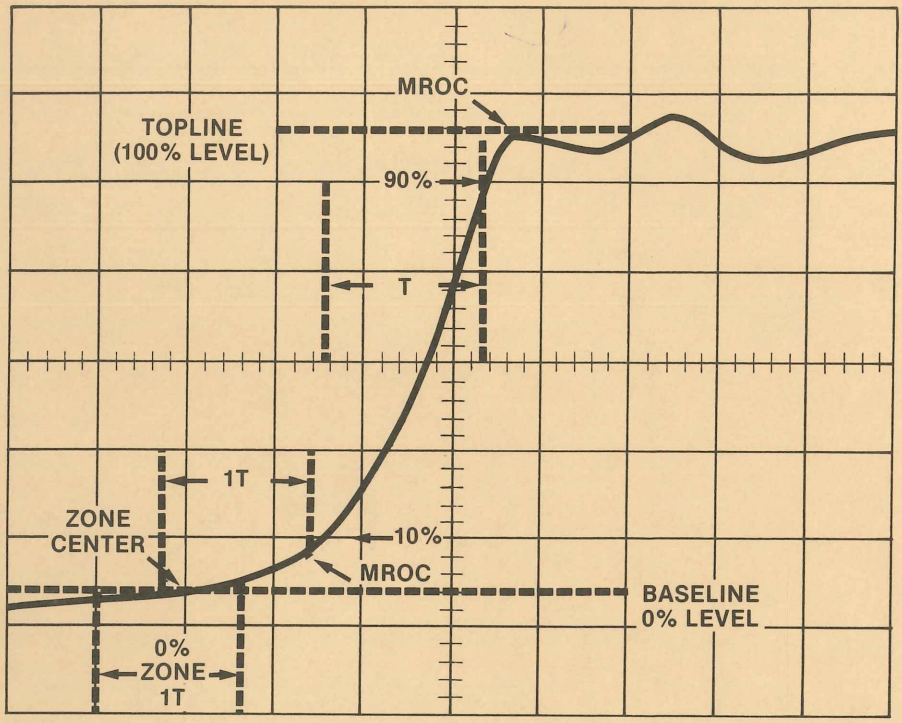


Figure 2. With a tunnel diode trigger foot present, measuring transition time (T) requires a 0% level determination as illustrated. The minimum radius of curvature (MROC) point is the reference point for finding the 0% zone's center. The average amplitude level in this zone becomes the 0% level or baseline.

$$P_{DUT} \otimes S_{NBS} = [P_{DUT} \otimes S_{TEK}] \otimes \underbrace{[P_{STD} \otimes S_{NBS}] \oslash [P_{STD} \otimes S_{TEK}]}_{\text{CORRECTION FACTOR}}$$

Where $\otimes$ denotes convolution.

and $\oslash$ denotes deconvolution.

P_{DUT} is the pulse generator being tested.

P_{STD} is Electrical Standards' standard pulse generator.

S_{NBS} is the NBS Automatic Pulse Measurement System

S_{TEK} is Electrical Standards' S6 sampler.

Figure 1. This relation uses the commutative property of convolution and allows a pulse generator under test to appear as though it were being measured on the NBS system. We need derive the correction function only once to calibrate a sampler. We can then use this function to correct any number of displayed waveforms with a simple convolution.

In Electrical Standards we follow the NBS procedure as closely as possible. The NBS sampling system has a transition time of 20 picoseconds. After we process the data we use the root-sum-squares (RSS) rule to correct for the NBS system's 20 picosecond transition time.

Extreme pulse distortions may cause the RSS rule to mispredict the transition time. We estimate the total calibration uncertainty to be +/-2% plus 1 picosecond plus the uncertainty contributed by the NBS APMS.

TRIGGER FOOT PROBLEMS

There is a problem defining the baseline of pulses produced by tunnel diode pulse generators (such as the S-52 and 284). The slow rising trigger pulse necessary to fire the

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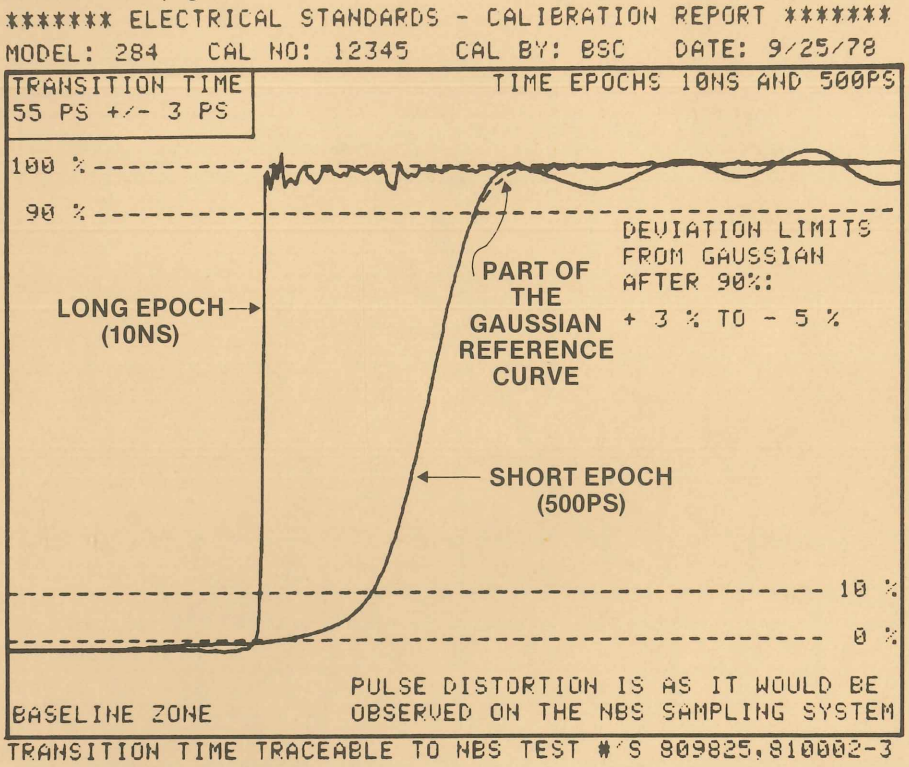


Figure 3. This is a sample calibration report. The two solid lines show the pulser under test at 1 nanosecond per division and at 50 picoseconds per division. Note that the 0% level is determined by using the trigger-foot-zone routine (see figure 2). The curved dashed line is a portion of the Gaussian reference pulse from which the pulse distortion limits are measured.

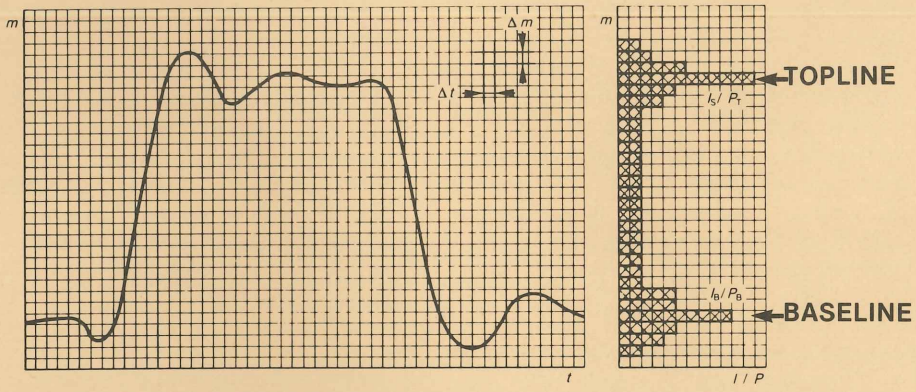


Figure 4. This is an example (taken from IEC standard 469) of a pulse and its bimodal histogram. The histogram (or occurence density distribution) on the right shows the two peaks (modes) that correspond to the baseline and topline of the waveform on the left. This method of determining the 0% and 100% levels mathematically defines the base and toplines. Visually, they correspond to the flattest portions of the pulse.

tunnel diode becomes superimposed onto the fast transition. The result is a sloping trigger "foot." This distortion produces a calculated transition time that is too long.

To avoid this problem, we use a zone method to determine the baseline. With this method, we pick a reference point that is one (estimated) transition time (T) before the first minimum radius of curvature (MROC) point (see figure 2). The baseline then becomes an average of the waveform amplitude in a one-transtion-time wide zone centered on this reference point. The zone method is a compromise between (1) selecting a point too far down on the foot, and (2) making sure the Gaussian-type lower leg of the fast transition has not begun.

PULSE DISTORTION

Pulse distortion is the percent deviation of an observed pulse from a reference waveform. We have chosen a Gaussian waveform as a reference. We match the standard to the observed waveform at the 10% and 90% points. We specify topline pulse distortion from the 90% point to the end of the waveform epoch. This could, of course, be modified to exclude any part of the topline. For example, the specification could read "distortion after five nanoseconds from the transition."

Each calibration that Electrical Standards performs will be accompanied by a hard copy of the waveform as it would appear at NBS. The copy will also include transition time and pulse distortion data (figure 3). □

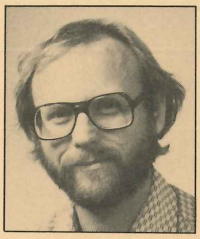
ENGINEERING ACTIVITIES COUNCIL OPENINGS

The Engineering Activities Council, originally chartered by Bill Walker (T&M Group vice president) is starting its third year. Each six months, part of the Council rotates off. This provides an opportunity for several engineers to participate on the Council.

"The basic purpose of the Council is to provide engineers with a forum in which they can present, to multiple levels of management, what engineers themselves consider to be important in their areas of technology," Walker explained in a letter to **Engineering News**.

If you are interested in contributing to better engineering communications and would like to be considered for one of the openings, call Bill Walker's secretary, Karen Hall, on ext. 7009 or drop him a note at D.S. 50-475.

DISPLAY DISTORTION IN MONO-ACCELERATOR CRT'S



Gary Nelson, Real-Time Crt Engineering (Tektronix Laboratories), ext. 5544.

Display distortion is inherent in any cathode ray tube. In mono-accelerator crt's, where an electron is at final velocity prior to deflection, one can most clearly see the factors that combine to produce distortion. Those factors are **deflection nonlinearity** and **geometric distortion.**

NON-LINEARITY

Designers of instruments using crts want the deflection voltage to correspond directly to the image displacement on the screen. Unfortunately, this correspondence is approximate and lessens with increasing scan angle. This non-linearity is expansive or compressive depending on whether the displacement is greater than or less than a proportional input voltage.

To visualize the effect, consider an electron moving within a deflection field. The lateral velocity imparted to the electron is proportional to the deflection voltage. When the electron is in the deflection field, the velocity's axial component doesn't change because no force acts in the axial direction. So, just before leaving the deflection plates, the electron's deflection angle is as shown in equation 1.

Since the lateral velocity is directly proportional to the deflection voltage, and since the axial velocity is unchanged, the scan is linear. As shown in figure 1 and in equation 2, image displacement on the screen is a product of the distance to the screen and the tangent of the deflection angle.

Figure 2 shows that the fringing fields retard the electron's motion as it leaves the deflection region because the positive deflection plate is more positive than the screen (in mono-accelerator crts the deflection plate's *average* potential equals the screen potential). The retarding field acts mostly in the axial direction. The lateral velocity doesn't change. Equation 3 shows the deflection angle.

Equation 4 now defines the image displacement. Comparing equations 4 and 2, we see that displacement increases faster than deflection voltage. The same is true in the x-axis and for the same reason. The result is expansive non-linearity.

GEOMETRIC DISTORTION

Now let's look at each of the three possible electron paths: vertical, horizontal, and diagonal. To avoid the complexities of fringe-field effects, let's consider the electron after it leaves the deflection plate region. And, for further clarity, let's assume the electron first encounters the vertical deflectors and then the horizontal.

Equation 5 defines a vertically-deflected electron's deflection angle. Similarly, equation 6 defines a horizontally-deflected electron's deflection angle. A diagonally-deflected electron is a more complex case. Refer to figure 3. The diagonally-deflected electron's trajectory begins with velocity v, leaves the vertical system with the same velocity at angle **a** to the z-axis, enters the horizontal deflection system with axial velocity v_{zv} and leaves with axial velocity v_{zd}, total velocity v, and a diagonal trajectory. The angle between the diagonal trajectory and the z-axis is indeterminant because it is a **skew** trajectory (a trajectory whose rearward projection does not cross the z-axis).

In figure 3 we can see that the diagonal trajectory's projection into the Y-Z plane is at angle **a'** to the z-axis. Angle **a'** does not equal **a** because v_{zd} does not equal v_{zv} while v_y is invariant.

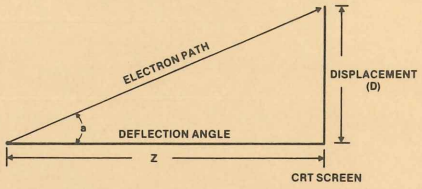


Figure 1. Image displacement on a crt screen is the product of the distance to the screen and the tangent of the deflection angle.

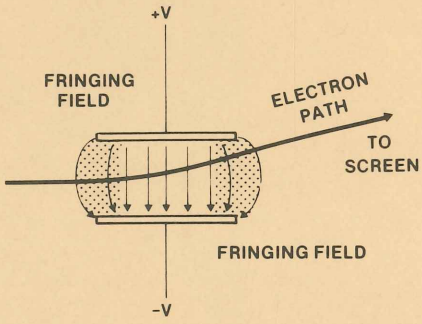


Figure 2. Fringing fields (indicated by curved lines) retard an electron's motion as it leaves the deflection field because the positive deflection plate is more positive than the screen.

Similarly, **d'** is not the deflection angle described in equation 7 because v_{ZH} does not equal v_{ZD} nor does v_X equal $v_{X'}$ (as shown in equation 7). Since we know the relationship shown in equation 8, we can substitute appropriately and derive equation 9. Unless we assume the horizontal deflection plates are shaped (radiused) such that $v'_X = v_X$, we can't define horizontal component **d'** with known quantities. (We will see later that the assumption is appropriate.) Remember that while v'_X equals v_X, **d'** does not equal **d** because v_{zd} does not equal v_{ZH}. Again from the relationship in equation 8, appropriate substitution results in equation 10.

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In equation 9, **a′** equals **a** when there is no horizontal deflection. In equation 10, **d′** equals **d** when there is no vertical deflection. Primed values larger than non-primed values indicate pincushion geometry distortion.

Crt designers commonly radius the horizontal deflection plates exit or entrance to improve display geometry. Why not radius the plates so that **d′** equals **d** and eliminate all distortion? Since **a** does not equal **a′**, pincushion distortion remains in the Y axis. The only way to correct this pincushion is to select an appropriate voltage on a "geometry element" at the deflection system's exit. Since this element will affect both axes approximately equally, it is necessary that some pincushion distortion remain in the horizontal axis (**d** does not equal **d′**). The combination of horizontal plate radiusing and a geometry element will provide good geometry but will not restore the direct proportion of displacement to input voltage. This is not necessarily bad since most deflection amplifiers are slightly compressive or can be made so. To some extent, then, crt expansion offsets amplifier compression, but the crt designer can rarely achieve a perfect match. □

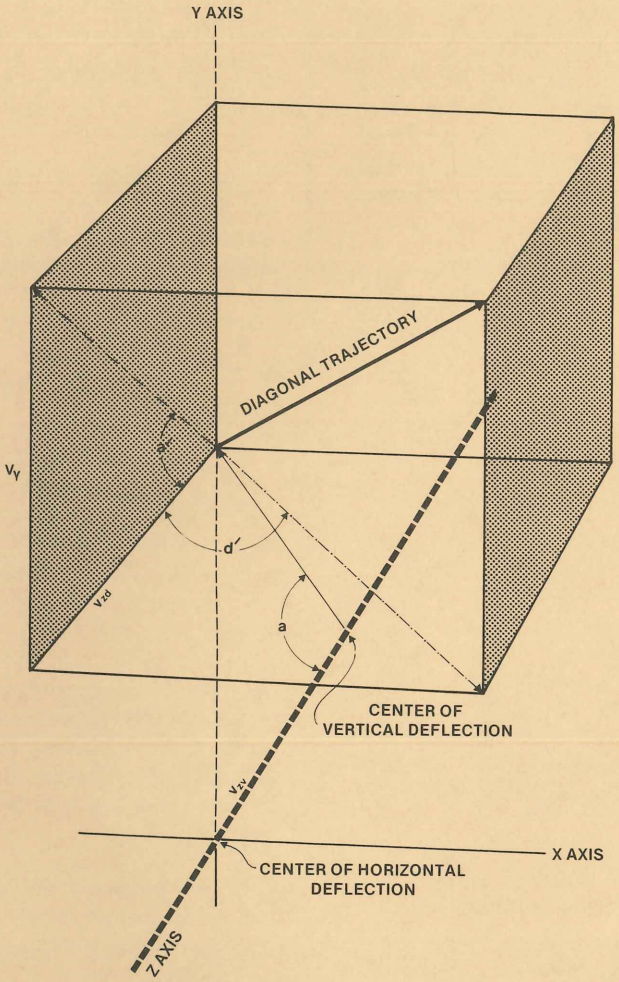


Figure 3. This velocity diagram for a diagonally-deflected electron shows the velocity components in the X, Y, and Z planes. Also shown is the physical position of the diagonal trajectory to the crt.

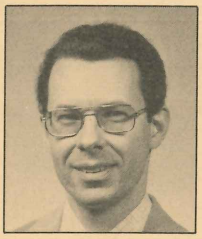
EQUATIONS

1. $\tan a_1 = \frac{v_y}{v}$
2. $D = Z \cdot \tan a_1 = \frac{k \cdot Z \cdot V_Y}{v_z}$
3. $\tan a = \frac{v_y}{v}$
   Where $v_z \neq v$
4. $D = \frac{k \cdot Z \cdot V_Y}{v\sqrt{1-\left(\frac{k \cdot V_Y}{v}\right)^2}}$
5. $\tan a = \frac{v_y}{v_{zv}}$
6. $\tan d = \frac{v_x}{v_{zh}}$
7. $\tan d' = \frac{v_x'}{v_{zd}}$
   While $v_{zd} \neq v_{zh}$ and $v_x' \neq v_x$
8. $v^2 = v_y^2 + v_{zv}^2 = v_x^2 + v_{zh}^2 = (v_x')^2 + v_y^2 + v_{zd}^2$
9. $\tan^2 a' = \frac{\sin^2 a}{\cos^2 d - \sin^2 a}$
10. $\tan^2 d' = \frac{\sin^2 d}{\cos^2 d - \sin^2 a}$

SYMBOL TABLE

a	Vertical deflection angle with no horizontal deflection.
a′	Vertical deflection angle after horizontal deflection.
a_1	Vertical deflection angle within vertical deflection plate system.
d	Horizontal deflection angle with no vertical deflection.
d′	Horizontal deflection angle when vertical deflection is present.
D	Trace displacement on CRT screen.
k	A constant.
v	Electron velocity before and after deflection.
v_x	Horizontal component of electron velocity with no vertical deflection.
v_x'	Horizontal component of electron velocity with vertical deflection.
v_y	Vertical component of electron velocity.
V_y	Deflection voltage.
v_z	Component of velocity along crt axis.
v_{zd}	Component of axial velocity after both horizontal and vertical deflection.
v_{zh}	Axial component of velocity after horizontal deflection only.
v_{zv}	Axial component of velocity after vertical deflection only.
Z	Distance from deflection origin to the screen.

25-INCH 4016 COMPUTER DISPLAY TERMINAL



Bill Devey, IDO Engineering, ext. 2520 (Wilsonville). (GMA125 project leader).

The Tektronix 4016 Computer Display Terminal, announced at the National Computer Conference in June, features a 25-inch screen, improved performance, and modular construction. (A 4016 is an integration of a 4014 terminal and a GMA125 display unit).

The 4016's most significant performance improvement is the ability to display more information. A Tektronix 19-inch crt displays about 8500 fully-resolvable characters. while the new 25-inch tube displays about 15300 characters.

FLICKER-FREE

New circuitry eliminates the erase flash present in earlier crt's by producing the double-cycle erase waveform shown in figure 1 (top). Earlier erase waveforms had a 13-millisecond fade-positive segment which produced a bright flash when screen-erase occurred (bottom, figure 1). In a dark environment our eyes become "dark-adapted," making them more sensitive to light. The bright flash strains the eye, making reading the screen momentarily difficult.

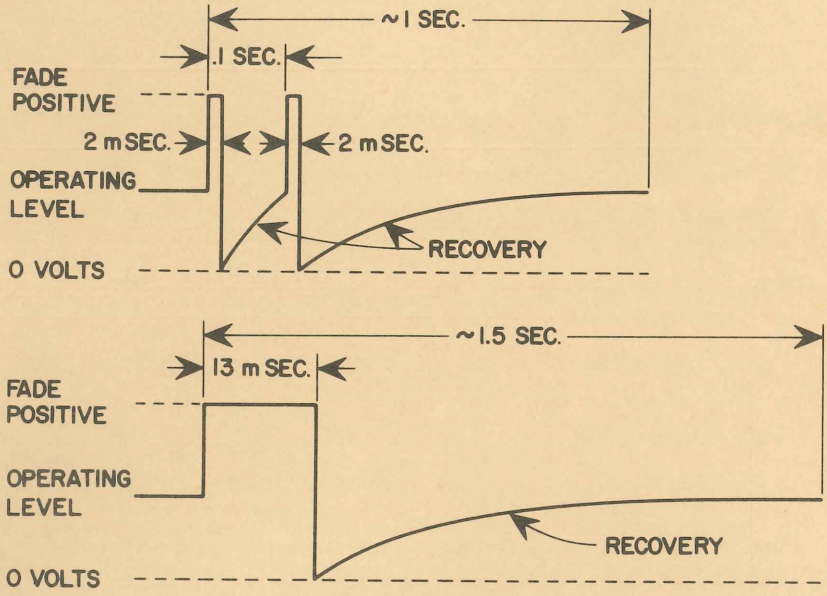


Figure 1. The 4016 Computer Display Terminal produces an erase-waveform (top) that eliminates the bright flash produced by earlier displays' erase waveforms (bottom).

However, the 4016's erase cycle includes two 2-millisecond fade-positive pulses 100 milliseconds apart. Because of the very short fade positive pulses, the operator perceives a darkening background rather than a flash.

LONGER LIFE

The 4016's tube life is much greater than for previous storage tubes because the 25-inch tube uses a new phosphor (developed by Large-Screen DVST Engineering, Tek Labs). The mean life of 19-inch tubes

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CHARACTERISTIC	O.E.M. 19 Inch Display (1977)	O.E.M. 25 Inch Display (1978)
Quality Area Size (cm)	(27.7 x 36.7)	(36.2 x 49.0)
Quality (cm^2)	1016	1773
Resolution (L.P.P.I.)	40	40
characters/line	133	180
lines	64	85
Total of characters (Resolvable in context)	8500 (>10000)	15300 (>25000)
Stored writing speed (cm/msec.)	15	20
Amplifier Deflection Speed (cm/msec.)	120	150
Slew Settling Time (μsec.)	2/cm + 3	2/cm + 1
Line Power (watts)	230	300
Figure of Merit mwatts/stored character	2.3	1.8

Table 1.The 4016 Computer Display Terminal represents major advances in display technology compared even to the 1977 version of the 19-inch terminals.

was 2000 hours. The new phosphor has about a 4000-hour life when tested with the standard quarter-page test. For more information about the new phosphor, see the April, 1978 **Engineering News** article, "Improved Phoshor Life in DVST's" by Tom Woody; call ext. 6792 (T&M Publicity) for a copy.

GREATER EFFICIENCY

Considering the greater screen size, greater amount of displayed information, and faster deflection speed (see table 1), the 4016 uses not much more power than its predecessors. Two developments account for more efficient power use. First, the 4016 has a switching low-voltage power supply in the display which is about 80% efficient (earlier crts' had linear supplies which which were about 55% efficient).

The second development is the 110-degree envelope (see figure 2). The 19-inch storage tubes used a 90-degree envelope. The 110-degree envelope allows more flood-gun current to reach the phosphor by reducing the current lost to the collimating electrodes inside the tube.

MODULARITY

The 4016's display design enables Tektronix to manufacture, calibrate, and test the 4016 in modules. (The pedestal design has always been modular.) Service technicians can replace defective modules and thereby reduce inventory costs and on-site service time. Other benefits of modularity are easy system integration and the ability to add custom-designed circuitry. □

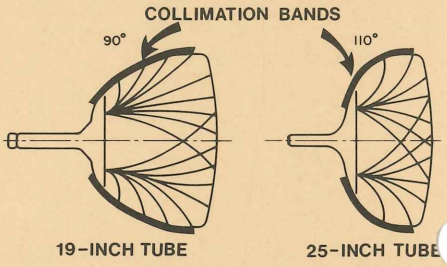

Figure 2. In the 25-inch tube used in the 4016 Computer Display Terminal, more flood-gun current reaches the target because less current is lost in the collimation bands (conductive coatings inside the crt). Consequently, the 25-inch tube requires less power.

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