TEK INFORMATION FOR TECHNOLOGISTS

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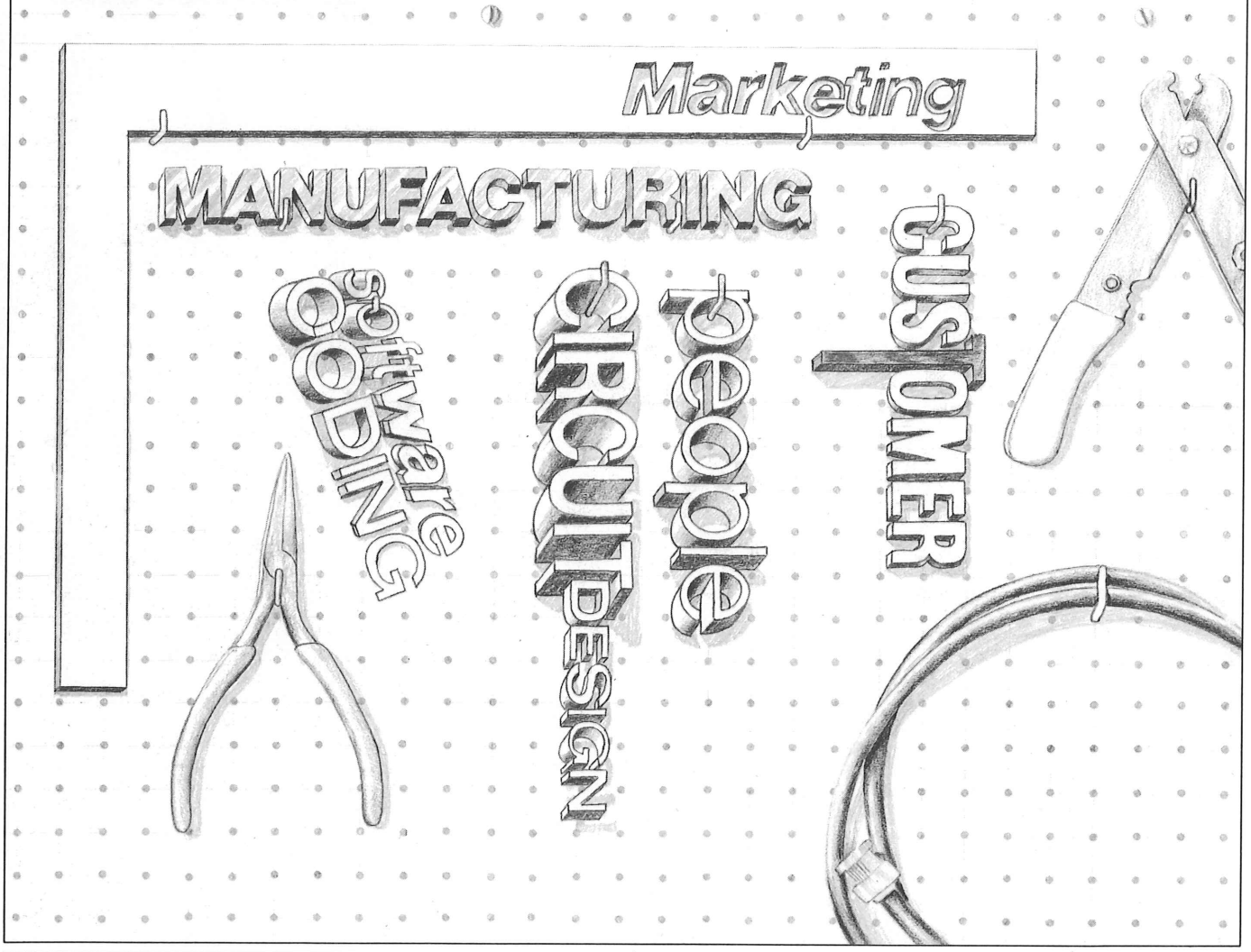
TECHNOLOGY report

ACHIEVING RESULTS IN PRODUCT DEVELOPMENT



Tektronix
COMMITTED TO EXCELLENCE

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Why TR?

Technology Report serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community).

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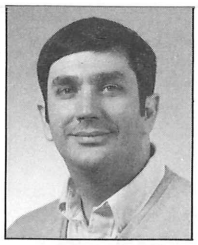
ACHIEVING RESULTS IN PRODUCT DEVELOPMENT



Steve Palmquist is the engineering manager of the Logic Analyzer business unit, part of DAD. Steve joined Tektronix in 1974 from Bell Labs where he worked on analog and digital hardware design, and test software. Earlier, he did device modeling and circuit simulations for the Atomic Energy Commission. Steve received his BSEE from Washington State University and his MSEE from the University of Illinois. Steve can be reached at ext. WR-1227.

Results . . . how do you get them in engineering projects?

Two years ago I was a member of an engineering team assigned a major project – a state-of-the-art logic analyzer. We had one advantage right at the start. We were an integrated team that had worked together on other projects at Tek. There wasn't a start-up problem caused by inexperience.

One characteristic of engineering inexperience is a tendency to pursue neat ideas for circuits and software. Things that challenge the engineer but probably won't solve the customer's problem. I think this is natural. You prefer to follow your own inclinations, a process that is not inherently wrong but is inherently limited.

Solve the Customer's Problems

When the customer defines the problem to be solved and you solve it, the result is more likely to stand up in the marketplace. The product will have a better chance to be a winner. But when a product consists primarily of neat ideas, its appeal is often limited to the designers. But how to find out what the customer needs? That's not easy. That's not something taught in engineering school.

Sometimes some answers can be found close to home. With caution, the problems of the "next bench" can be attacked. What frustrations are being experienced in-house? Are these frustrations similar to those of potential customers? Can we solve them better than someone else? If preliminary investigations confirm that Tek could solve the problems well, it is now time to find out whether the problem exists outside and if the solution fits the customer. It is essential to confirm that the commonality of the need extends beyond the business unit and division. It is time to see some customers.

A few trips to the field can confirm whether your solution matches external needs. In doing this it is essential to keep an open mind. It is always possible to reinforce preconceptions, particularly if it is assumed that your group is technically more advanced than that of the customers. Tektronix has made this error from time to time – make sure you are not the one to repeat it.

Observing customer operations and discussing problems with the guy on the bench and his or her manager may make it obvious that the proposed solution won't sell. Or another solution may be indicated. Opportunities come from customer problems. When those problems are the same as ours, we have a natural basis for product development. In logic analyzers we had a commonality with customers that allowed us to grasp the customer's situation.

In some areas, the technique of matching Tek's in-house situations and solutions to customer needs doesn't work as easily. Semiconductor test systems, for example, are used at Tek but not to the extent or in the same manner as most customers do. The more the customer differs from Tektronix, the more effort is required to understand what solutions are best for that customer's problem.

Let's use an extreme example. If we were developing electronic products for the cold-rolled steel industry, we'd have to depend a lot on market research. Our engineers, being electronic-logic oriented, would not have the feel for the customer's problems. To a large extent, Tektronix has advantages in that we and our customers have much in common; we speak the same lanquage.

The common elements in both businesses can also trap us into believing we know what the best solution would be. This hazard is especially acute with the new engineer. Almost every newly hired graduate has tried to apply that neat circuit that they had in Engineering 499. I know I did. This is dangerous.

It's dangerous because you just can't start with a circuit and wind up with a saleable product. The problem must be defined first. Then comes the circuit and the code. If you start with an attitude that a particular microprocessor is really great and base the product on that premise, there will be problems, terrible problems. I've seen the pain that the neat-circuit approach can spawn.

The Faster, Wider, and Deeper Trap

There's another bad way to approach a new product: plan it to be faster, wider, and deeper. When a product line is well received and customers are buying, what do you do next? Do you make your 10 MHz device run faster, 20 MHz perhaps? This year we have 20 channels, why not 40 next time? This, of course, is the faster, wider, deeper approach. It works until the market shifts – then this approach means market death.

A deeper memory, for example, may not be the best feature for that new product. Perhaps something to allow the user to concentrate his or her efforts on problem solution rather than instrument operation is now needed.

Consider what we are saying when we describe a product as a "logic analyzer." We don't really make a logic analyzer, we make an instrument that the customer can use to help him or her to analyze logic. Adding intelligence to the product might make the name logic analyzer an accurate description of its actual function.

Thinking about the use and the need has to be a level above the obvious. Naming the task doesn't solve it.

When we started on the Digital Analysis System (DAS), we asked ourselves: "What is it that the user will be trying to do?" For example, instead of just making a faster 7DO1 – an earlier successful analyzer – it seemed that the new product should be able to output bits, not just acquire them. For more effective circuit debugging, interactivity between the user and the instrument was needed. To fulfill that need the team developed the pattern generator concept. (See box.)

Early in the project, the question should always be: How can we solve the user's problem better? The answer may be faster, wider, deeper for a while, but this approach will eventually flop.

Understanding the customer's problem and applying that knowledge should enable the product team to tailor target specs that are most likely to match actual customer needs. Knowledge of those needs reduces the number of expensive features that can creep into a product. Neat, but useless, features should wash out early in the project. They certainly should fade from consideration before they dissipate energy in discussion and argument.

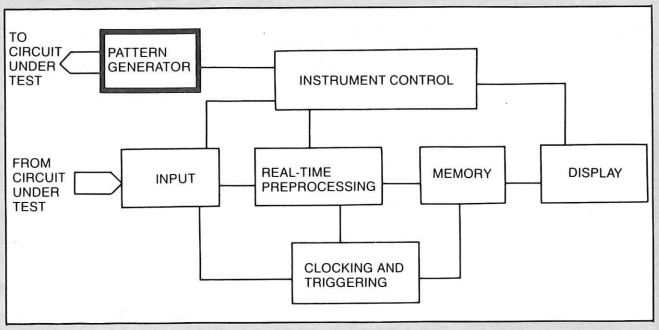
Marketing, an Engineering Responsibility Too

Again, I think it's essential that system designers get "out there." Because "help" is defined by the recipient, in this case our customers, *personal experience of customers' situations is vital.* There's a real danger in too much reliance on the market survey: Market surveys can be useful, but they are interpretations of indications, done by someone who presents conclusions to a manager who, in turn, adapts the interpreted data using his or her knowledge and bias and passes the "refined" conclusions to the bench-bound engineer, who has no direct knowledge of what the customer needs. Designing to meet what someone else interpreted from what was reported by still another person is sure to yield a less than satisfactory solution to the real problem.

Marketing is the job of every design engineer and every engineering manager. Every engineering design decision is a marketing decision. (It's a manufacturing decision too.) If the marketing job is left only to marketing specialists and the engineers confine decisions to engineering, products will be late and will miss their intended market. We have seen this happen too often.

Engineering schools don't teach the marketing aspects of an engineering decision. Perhaps this is not a teachable subject in the engineering sense of methodologies and analyses. In the absence of hard data, we tend to look to others for the answers as to what the customer will buy. We seek someone in red robes who answers the difficult (for everyone) question of customer needs rather than recognizing that we, ourselves, are in an excellent position to seek the answers.

PATTERN GENERATION



Conventional logic analyzers have six main sections: input, real-time preprocessing, memory, clocking and triggering, display, and control. In the DAS 9100, Tektronix introduced a seventh basic section – pattern generation. The 9100 was the first logic analyzer to provide both stimulation and observation capability in the same instrument.

Obviously, to observe a circuit and acquire meaningful data, something meaningful must be happening in the circuit. In the past, in order to collect meaningful data, the user often had to set up a separate stimulus instrument to drive the circuit in some known way. This need is particularly strong during the early stages of design when a circuit cannot be tested in the environment of other known good circuitry. When no pattern generation is provided by the analyzer, the user can be forced to expend time and effort to develop a suitable substitute.

The DAS 9100 was the first logic analyzer to provide both stimulation and observation capability in the same instrument. This capability can save significant time for the designer, since program circuit stimulation can be programmed in the same way the rest of the logic analyzer is set up – with prompting menus. Since the pattern generator allows algorithmic generation of data, a short program can create a much larger sequence of data for driving the circuit under test. The pattern generator can be programmed to behave like the environment in which the circuit will be used, enabling the designer to test parts of a circuit design before all prototypes are ready.

Ultimately, the prototype tests created for the pattern generator can be the basis for evaluation and manufacturing tests. The pattern generator stimulates the circuit under test and the circuit data is acquired and stored in the analyzer's acquisition memory. The contents of the acquisition memory are then compared to the contents of the reference memory to identify errors.

It is important to start with the fundamentals of engineering. That's where the good engineering school comes in. Then the manager needs to teach the new engineer to think in terms of solving the user's problems. We, as engineers, must view ourselves as "servants." A good servant solves the customer's problem, often without specific orders. We need to recognize

the customer's role as master. It is part of our role to sense what the master wants. This is not a demeaning relationship, it is a method of creating useful products. We should not be artists creating a message on our own that we will carry to the world.

In school, you can gain the impression that you are among the elite, one of those students that really understand. However, those "poor guys that don't understand" wind up working everywhere. They are here at Tektronix – and at the customers. They really do understand, but they understand differently. A product that is built without consideration as to how others understand a problem may be a brilliant solution to you but undesirable to users in general.

Looking for Mr. Long-Range

Now the individual out there tends to think of the immediate need. The measurement that has to be made today. The application that is unsolvable today – and may never again be necessary. This individual won't have the answer to your question. The engineer surveying customers needs to recognize this trap and temper judgements accordingly.

Most customers are oriented to the short term. They are solving Tuesday's problem on Tuesday and giving very little thought to a year or two down the road. For long-term insights, look for the long-range thinker. And, when you find one, use his or her thoughts, ideas, and suggestions for all they are worth.

Literal compliance with a customer's suggestion may be dangerous. Listen more closely to a customer who tells you, "I want to test parts," than to a customer who tells you that his system needs a faster widget. The closer you get to the end product of the customer, the more likely the real need will come to you. Listen to the symptoms of a problem and to the customer's suggestions – but focus on what the customer is ultimately trying to do.

Careful listening increases the chances of the new product being a solution to real problems. But experiencing problems is even better. The engineer that experiences a problem the way a customer does can contribute greatly to design architecture. Of course I don't mean that the engineer need be emotional about a solution. Objectivity is needed too.

Some business units, by the nature of their product types, are closer to the user mentality, the user experience. Others are more removed. Even so, all business units must involve their engineers with the concepts of solving the customers problems the way the customer wants to solve them.

When you are told to dig a hole for a telephone pole, you not only want to dig a hole that will fit the pole, you need to know how the hole will relate to the overall project. If there is a road to be built too, the hole can't be in the road bed. In product design, too often we put the "hole" in the wrong place. Often, it would have been no more work to determine the right place before digging.

When A Design Is Complete

When you have a solution, go with it. The window of opportunity for a particular solution is usually narrow. It is important not to improve a solution while the customer evolves new needs that your elegant, improved solution no longer fits.

When asked, "When do I know I'm done?" my first supervisor gave me some good advice. He said, "You never know when you're done." He said that the way to find out was to take your solution to the best people around; give them about an hour to evaluate what you have. If they wouldn't change anything, you are done.

Given enough time, anyone can – and will – find a way to do it better. After all, they would have the advantage of standing on your shoulders. From this vantage point, who couldn't improve on what you have done. Remember, all you have to do is solve the customer's problem – and be better than the competition in doing so.

Diagrams and Coding Should Come Last

Too often, once the decision to build a product is made, people want to start drawing diagrams and writing code. This stage should not occur until months later. Implementation should never occur until the functional blocks are worked out. How these blocks are to interrelate should be described in writing so that the design team can determine if the blocks and their relationships make sense. If this information is confined in each person's head, the sense of the system may not be understood or proven before implementation. Without written descriptions, a designer can't use the help of peers effectively. And the team cannot sense whether they are all going in the same direction.

The engineer should treat ideas as neither good nor bad but only as things to be examined for validity. This, of course, is hard for anyone to do, myself included. I think the "artist" who emotionally invests in an idea for its own sake is dangerous to a project. The investment should be in the search for a solution to the need.

Maintaining Enthusiasm

It is necessary to maintain enthusiasm. When all team members understand what we are doing and why we are doing it, they can see their part and should be able to maintain enthusiasm.

Generally, everyone wants to be part of a team. Teamwork implies dependency. You can't team with someone without depending on that person for an element or elements essential to your task. Each person supplies critical elements and each must do so when each element is needed. If each person sees what he or she contributes to the success of a product, enthusiasm is almost automatic.

The team member needs to know what he or she is expected to do and when, but the how should be left to the individual. In this way you avoid the ego bruising inherent in telling someone how to do something. When you tell someone just how to do something, you invite subtle subversion of the project objectives. Of course there are times when the details must be a certain way. If something must be done a certain way, be sure the reason for that way is explained.

What Needs to be Written

The basic functions of a new product must be documented. Without this, the hardware/firmware tradeoffs can't be made. If you don't document the functions, how can someone design the user controls and the displays? And how about manufacturing or diagnostics? All these have to be set down before one schematic is drawn.

Manufacturability

Engineers can focus so heavily on neat ideas that they overlook the fact that you can't ship something that you can't make. Sometimes the most advanced circuit or code is almost unmanufacturable.

Knowing manufacturing is part of an engineer's job. "Living" with your manufacturing group on a regular basis is one way to know their capabilities and limits, probably the best way. Strengths and weaknesses must be known before starting implementation.

The need to understand what manufacturing can do is part of the package, along with knowing customer needs and wants. When working with any group anywhere, it is very easy to find someone who will tell you something can't be done. Don't stop there; if your objective is right, search for someone who says it can be done and then let them help you. There is little that can't be done. Can't is usually an attitude rather than an absolute barrier.

If ideas or requests yield unacceptable responses from manufacturing, it is worthwhile to go over and make your needs known directly, and of course, diplomatically. It is normal for a group to lock in on their special objectives and lose sight of the end objective: Marketing losing sight of engineering, engineering losing sight of manufacturing; and soon, people are serving the system, rather than pursuing the goal.

It seems when you build a system that can monitor and control everything from a central point, that system slows everything. Such a system can prevent failures, but when you protect from failures you may protect from innovation and productivity.

Summary

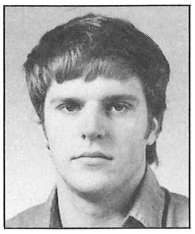
Success in the market requires a product that solves customer problems. To develop such a product requires understanding customer environments as well as knowing how to design hardware and software. Since most Tek engineers have problems akin to that of our customers, they should be able to relate to what challenges our potential customers.

The Tek engineer can't thoroughly understand the customer until he or she gets out to where the customer works and listens, and observes, and questions. In this process the engineer must look for the long-range thinker, or at least someone who defines his or her objectives – "I want to test parts" – rather than someone who narrowly defines what's needed – "I need a faster widget."

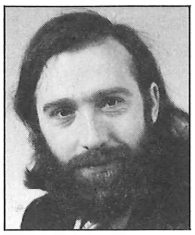
The complete engineer will take his or her technical skills and build knowledge of manufacturing capabilities. This knowledge added to marketing knowledge provides the tools needed to both conceive a useful product and design a manufacturable one.

The tool set of the experienced engineer goes beyond circuit design and software coding; it includes understanding people, marketing, manufacturing, and customers. □

TEKSIM/TLOGS: A POWERFUL TOOL FOR LOGIC SIMULATION AND TESTABILITY ANALYSIS



Gary Zeigler is an engineer II in Computer-Aided Engineering, part of the Technology Group. He received his BSEE from the University of Michigan in 1981. Gary joined Tektronix in 1981.



Graeme R. Boyle is a software engineer in Computer Aided Engineering, part of the Technology Group. He joined Tektronix full time in 1978. Earlier he worked here part-time, starting in 1974. Graeme received his PhD in electronic engineering from the University of California at Berkeley. His bachelor's degree is in engineering science, his masters in electronic engineering, both are from the University of Melbourne, Australia.

The most important requirement of any logic system, aside from attaining its specified performance, is functional reliability. Functional reliability is determined by the extent to which the system is testable.

Although testability has been a working concept for many years and testing systems have been used for circuit boards since the 1960s, the emergence of VLSI has heightened interest in an efficient testability-analysis capability for designers. We have developed a new logic analysis system, TEKSIM/TLOGS, to provide Tektronix designers with such a capability.

Logic and Fault Simulation in General

A logic simulation (also known as a normal or true-value simulation, as opposed to a fault simulation which is described below) is used to determine the propagation of logic states through a circuit consisting of logic elements. Logic simulation is used primarily as an aid in the design of digital systems. These logic elements are defined as performing a given logic operation on the logic state of their input(s) to produce the logic state(s) of their output(s). Most logic simulators use the three logic states of low (0), high (1), and undefined (⁑). Additional states such as high impedance (Z), transition states, and "strengths" associated with states may also be included to simulate the behavior of specific logic circuitry.

The input to a logic simulator consists of a list of the elements in the network being stimulated, their interconnection, a description of the input signals, and the interval (the time sweep) over which to perform the simulation. The simulation itself is performed by first initializing the state of all circuit nodes to undefined (⁑) since, in most cases, the logic states that the nodes in the circuit will "power-up" to are unknown. The input signals are then applied (at the specified times) to the circuit, and the propagation of signal changes through the circuit is determined (and carried out) at discrete time intervals. In this manner, the behavior of the circuit is "simulated."

Fault simulation is concerned with the detection of topological (interconnect) and processing (device characteristic) errors in a network. Given the numerous possible errors in a digital system, e.g., shorted wires, open connections, defective transistors, etc., and combinations of these errors, the problem of simulating the effects of these faults in a logic simulator becomes impractical for any network of moderate size or larger. A general-purpose model for these defects which gives surprisingly accurate results is known as the "stuck-at" model. In this model, the effects of network errors can be modeled by considering nodes to be stuck at logic 0 or 1 and unable to change from this state. A fault simulation consists of performing a normal logic simulation with one node of the network stuck at 1 or 0. If the effects of the fault are such that it complements the state of one or more of the network (chip) outputs, that fault has been detected. By using one of three fault simulation methods (see The Methods of Fault Simulation), stuck-at faults for every node in the circuit (or any subset of these faults) can be simulated and the results displayed (see figure 3 for an example of the fault simulator output from TLOGS).

TEKSIM/TLOGS

TEKSIM (TEKtronix SIMulation system) is an interactive user interface to four simulation programs. TEKSIM presently runs on the CDC Cyber 175 but is accessible over the hyperchannel network. TEKSIM provides an interface to:

- SPICE (Simulation Program with Integrated Circuit Emphasis), a circuit-level simulator
- SUPER-COMPACT, a general purpose circuit design system aimed primarily at microwave circuits. This "link" to TEKSIM is currently in the planning phase.
- WIRWRP, a program that translates a TEKSIM logic network description into a format suitable to run a wirewrap machine.
- TLOGS (Tektronix LOGic Simulator), is a 12-state (lo, high, undefined, and four strengths for each level) true-value/fault simulator.

The input to TEKSIM is a circuit description (logic elements or circuit-level components and their interconnection) via a hierarchical hardware description language and an analysis-control description (see figure 1 for an example of TEKSIM/TLOGS input).

The advantages of TEKSIM over the standard input/output facilities provided with these simulators are threefold:

First, because networks can be described in the same way for more than one simulator, in TEKSIM format, any differences between simulator input formats will be transparent to the user.

Second, TEKSIM provides a complete simulation environment with access to any of the NOS (the Cyber Network Operating System) commands (e.g., SCRIBE, GET, SAVE), on-line help and error messages, and print/plot capabilities for displaying the results of the simulation (see figures 4 and 5 for sample output from TEKSIM/TLOGS).

Third, and foremost, by providing multidimensional sweeps (TEKSIM/SPICE only at present), expression evaluation, and parameter passing, TEKSIM provides a more powerful analysis capability than does the simulator alone.

What Is TLOGS?

TLOGS was developed to be an efficient substitute for SALOGS (the SANdia LOGic Simulator), which has been in use at Tektronix in one form or another for the past five years, as well as to provide a fault simulation capability to Tek designers. TLOGS will enable people who still use older versions of SALOGS to switch to a compatible, but faster program that has full user support (which SALOGS does not have).

The operation of TLOGS is designed primarily for simulation of effects peculiar to MOS circuits (this is not a restriction, however, and TTL and ECL circuits can also be simulated). These include charge storage on node capacitances for logic operation, true bidirectional transfer gates and their effects on state transition delays and logic operation, and contentions of several elements driving a node. These are "strength" contentions that arise from several drivers on a node trying to force the node to different logic states. (Contentions are resolved by taking into account the strengths or physical dimensions of the elements driving the node.

In a comparison, a logic simulation of a digital operational amplifier* that required 450 seconds using the latest SALOGS version took only 132 seconds using TLOGS. In other cases, the speedup of TLOGS from SALOGS can be as significant as 20:1. Additionally, a fault simulation of the digital op-amp (which has approximately 4000 gates and 16000 total possible faults) has been projected to take 18 hours of CPU time on the Cyber 175. This was extrapolated from a 4.5 hour simulation of 4000 of the 16000 faults.

TLOGS can, while SALOGS cannot, include high-level "built-in" primitive elements such as RAMs, ROMs, FLIP-FLOPs, and PLAs. There is, however, a price to pay for these added capabilities in TLOGS. In its present form on the Cyber 175, TLOGS is limited to simulating about 14000 logic gates.

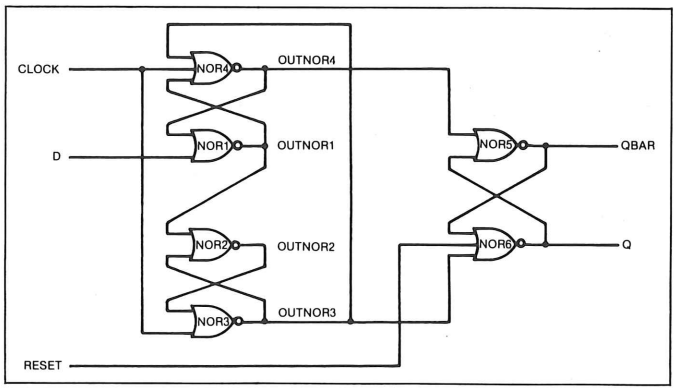


Figure 1. The D-type flip-flop used for the description in figure 2 and the outputs shown in figures 3 through 6.

```
TITLE D FLIP FLOP TESTABILITY ANALYSIS
CIRCUIT

; define the network input and output nodes
INPUT D CLOCK RESET
OUTPUT Q QBAR

GLOBALN CLOCK RESET

; describe the network topology
FLOP Q QBAR, D FLOP
MODEL FLOP SUBCKT: NODES=(Q QBAR, D)
NOR1 OUTNOR1, D OUTNOR4 NORD1
NOR2 OUTNOR2, OUTNOR1 OUTNOR3 NORD2
NOR3 OUTNOR3, OUTNOR2 CLOCK NORD3
NOR4 OUTNOR4, OUTNOR1 CLOCK OUTNOR3 NORD3
NOR5 QBAR, Q OUTNOR4 NORD4
NOR6 Q, QBAR OUTNOR3 RESET NORD4

MODEL NORD1 NOR: TRD=15N TRD=8N
MODEL NORD2 NOR: TRD=11N TFD=9N
MODEL NORD3 NOR: TRD=12N TFD=6N
MODEL NORD4 NOR: TRD= 8N TFD=7N
ENDM FLOP
ENDC

; define the nodes to keep the state of during
; the simulation
KEEP Q QBAR D CLOCK RESET

; define the input waveforms
SEQ CLOCK: HI 5ØN PERIOD=1ØØN
SEQ RESET: HI 48N
SEQ D    : LO 1ØØN PERIOD=2ØØN

; perform a States-Applied analysis and send the
; results to the file STDOUT
STATES: F=STDOUT

; perform a fault simulation on all the possible
; faults in the network, over the entire sweep range
; and send the results to FLTOUT
FAULTS: F=FLTOUT SKIP=1

; define the simulation time limits
SWEEP TIME Ø 5ØØN 1N

; display the results of the simulation
PRINTALL: Ø 3ØN F=PNTOUT
PLOTALL

GO
```

Figure 2. The TEKSIM network and control decision generated for the D-type flip-flop shown in figure 1. See figure 3 through 6 for the output generated by this run.

*Described in *Technology Report,* May 1982, pages 10–13 and in the 1982 Proceedings of the *International Conference on Circuits and Computers.*

```
1*** TEKSIM/TLOGS  VERSION 1A.3 ***
 D FLIP FLOP TESTABILITY ANALYSIS
 RUN ON 82/11/Ø1. AT 11.22.1Ø.
                    STATES - APPLIED ANALYSIS

  ELEMENT      POSSIBLE       PIN     FAULTS NOT
  NAME         FAULTS                 DETECTABLE


    INSIDE SUBCIRCUIT FLOP MODEL FLOP
 NOR4          5              I3          SAØ
 NOR6          5              I3          SAØ

 TOTAL NUMBER OF STUCK-AT FAULTS =       26
 TOTAL NUMBER OF POTENTIALLY DETECTABLE FAULTS =   24
 PERCENTAGE OF POTENTIALLY DETECTABLE FAULTS = 92.3
```

Figure 3. The states-applied output for the D-type flip-flop indicates the faults that could never be detected. This indication that input 3 of element NOR4 (i.e., node OUTNOR3) stuck at 0, and input 3 of element NOR6 (i.e., node RESET) stuck at 0 can never be detected. The maximum percentage of faults detectable is then given below.

```
1*** TEKSIM/TLOGS  VERSION 1A.3 ***
 D FLIP FLOP TESTABILITY ANALYSIS
 RUN ON 82/11/Ø1. AT 11.22.1Ø.
                      FAULT ANALYSIS

    ELEMENT     PIN       FAULT   DETECTED AT   DETECTED AT TIME
    NAME                  TYPE    OUTPUT NODE


    INSIDE SUBCIRCUIT FLOP MODEL FLOP
 NOR1          I1          SAØ     QBAR              163N
               I2          SAØ     ***         NOT DETECTED      ***
               O1          SAØ     QBAR               63N
               O1          SA1     QBAR              163N

 NOR2          I1          SAØ     Q                 263N
               I2          SAØ     ***         NOT DETECTED      ***
               O1          SAØ     QBAR              169N
               O1          SA1     Q                 263N

 NOR3          I1          SAØ     QBAR              169N
               I2          SAØ     QBAR              163N
               O1          SAØ     Q                 263N
               O1          SA1     QBAR              163N

 NOR4          I1          SAØ     ***         NOT DETECTED      ***
               I2          SAØ     QBAR              119N
               O1          SAØ     QBAR              163N
               O1          SA1     QBAR               14N

 NOR5          I1          SAØ     QBAR              213N
               I2          SAØ     QBAR              163N
               O1          SAØ     QBAR               14N
               O1          SA1     QBAR              163N

 NOR6          I1          SAØ     Q                  55N
               I2          SAØ     Q                 263N
               O1          SAØ     Q                 17ØN
               O1          SA1     Q                   7N


 TOTAL NUMBER OF POSSIBLE SIMULATED FAULTS=   24
 TOTAL NUMBER OF FAULTS DETECTED=   21
 PERCENTAGE OF SIMULATED FAULTS THAT WERE DETECTED= 87.5
```

Figure 4. The fault analysis output for the D-type flip-flop. For every fault that was simulated, the element to which it is associated (e.g., NOR1) the relative input (IXX) or output (OXX) number on the element, and the stuck-at type are given. In addition, for each fault that is detected, the output node name (i.e., one of the nodes listed after "OUTPUT" in figure 2) and the simulation time at which it was detected are given. The percentage of total number of possible faults that were detected is then given.

```
1*** TEKSIM/TLOGS2 VERSION 1A.3 ***
 D FLIP FLOP TESTABILITY ANALYSIS
 RUN ON 82/11/Ø1. AT 11.22.1Ø.
 ;PRINTING FROM: Ø TO 3ØN BY 1N
 ;
 ;---------------------
 ;
 ;       T  Q Q D C R
 ;       I     B   L E
 ;       M     A   O S
 ;       E     R   C E
 ;                 K T
 ;
 ;---------------------
 ;
         Ø  *  *  Ø  1  1
        1N  *  *  Ø  1  1
        2N  *  *  Ø  1  1
        3N  *  *  Ø  1  1
        4N  *  *  Ø  1  1
        5N  *  *  Ø  1  1
        6N  *  *  Ø  1  1
        7N  Ø  *  Ø  1  1
        8N  Ø  *  Ø  1  1
        9N  Ø  *  Ø  1  1
       1ØN  Ø  *  Ø  1  1
       11N  Ø  *  Ø  1  1
       12N  Ø  *  Ø  1  1
       13N  Ø  *  Ø  1  1
       14N  Ø  *  Ø  1  1
       15N  Ø  1  Ø  1  1
       16N  Ø  1  Ø  1  1
       17N  Ø  1  Ø  1  1
       18N  Ø  1  Ø  1  1
       19N  Ø  1  Ø  1  1
       2ØN  Ø  1  Ø  1  1
       21N  Ø  1  Ø  1  1
       22N  Ø  1  Ø  1  1
       23N  Ø  1  Ø  1  1
       24N  Ø  1  Ø  1  1
       25N  Ø  1  Ø  1  1
       26N  Ø  1  Ø  1  1
       27N  Ø  1  Ø  1  1
       28N  Ø  1  Ø  1  1
       29N  Ø  1  Ø  1  1
       3ØN  Ø  1  Ø  1  1
```

Figure 5. The print results for the D-type flip-flop.

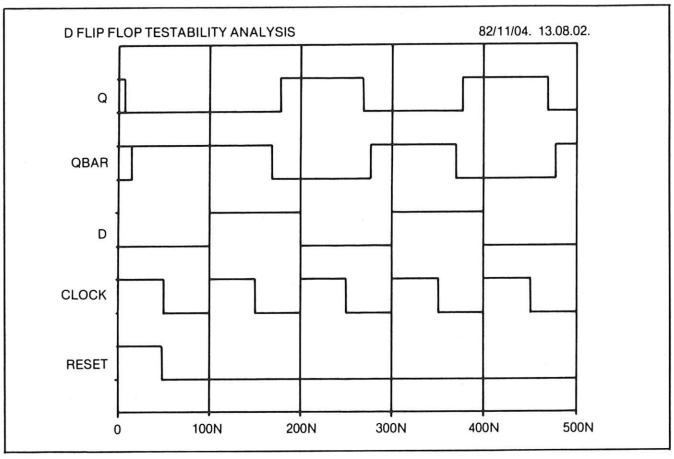


Figure 6. The plot for the D-type flip-flop.

Fault Simulation in TEKSIM/TLOGS

Fault simulation in TEKSIM/TLOGS is a two-step procedure: The first step is a states-applied analysis. The second step is an actual fault simulation. A states-applied analysis is performed by recording all logic states applied to every element in the network. This can be done during a normal true-value logic simulation and requires little execution-time overhead.

Based on the record of logic states and the element type, the analysis determines which faults could or could not be detected by monitoring the output of that element. For example, it would be impossible to detect if one input of a three-input OR gate was stuck at 0, unless the other two inputs were both forced to 0 at the same simulation time.

It must be emphasized that a states-applied analysis measures only the potential for detection. A fault that is detectable on the output of an element may never have its effects propagated to one of the designated network outputs. However, one may quickly check the effectiveness of a set of input waveforms in exercising the network by knowing that the percentage of faults detected from a fault simulation will never exceed the percentage of potentially detectable faults determined by a states-applied analysis. See figure 3 for an example of the states-applied output from TEKSIM/TLOGS.

Once the input waveforms to the network have been adjusted to provide an acceptable detection capability via the states-applied analysis, a fault simulation may be done. See figure 4 for an example of the fault simulation output from TEKSIM/TLOGS.

An added feature of the fault simulation is that the faults for an element may be marked (in the original network description) as not to be considered in the analysis. This is necessary because nonphysical elements are often included in the network to more accurately model timing in certain critical areas. Since these elements do not exist in the actual circuit, their faults should not be included in a fault simulation.

The Future of TEKSIM/TLOGS

TEKSIM/TLOGS is the basis for a high-level electrical simulation capability at Tektronix. Through its ability to handle complex built-in primitives (RAMs, ROMs, etc.), TEKSIM/TLOGS will provide designers with a mixed-mode logic and functional logic/fault simulation capability. This mixed-mode capability will allow a designer to describe a circuit in terms of logic gates and procedurally defined functional blocks. For example, the operation of an arithmetic logic unit may be described through a structured procedure for simulation purposes. The mixed-mode logic simulator will be able to simulate the behavior of the logic gates in the circuit along with functional blocks. We plan to have a rudimentary capability for this type of simulation within one and a half years.

There is, however, a limit on the number of logic gates (about 14000) that the data structures of TEKSIM/TLOGS can accommodate on the Cyber 175. This problem will disappear when a larger or virtual-memory mainframe replaces the Cyber, or when TEKSIM/TLOGS is converted to a VAX version (scheduled early this year).

TEKSIM itself however, as with TLOGS, has been specifically designed to be very transportable. Therefore, once another large mainframe is acquired, the transfer of TEKSIM/TLOGS to the new machine can be accomplished with a minimum of additional programming effort.

For More Information

For more information, call Gary Zeigler, B-4039, or get a copy of the TLOGS manual via the manual program on the Cyber 'A'. For more information concerning logic and fault simulation, see the references listed in the biography.

Acknowledgements

The authors wish to acknowledge the help of Archie Lachner and Dale Henrichs in the TLOGS project. We also wish to acknowledge with great appreciation the management support provided by Tom Bohan and Jack Hurt.

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THE METHODS OF FAULT SIMULATION

Gary Zeigler, Computer-Aided Engineering

Parallel Fault Simulation

Parallel fault simulation is one of the oldest and perhaps the easiest fault-simulation techniques to implement. In this technique, a list is first generated of all the possible faults in the circuit. This list defines all the faults that are to be simulated. The parallelism of this method comes about from the association of one computer word with the state of every node in the network being fault simulated.

Within this word, there are a particular number of bits associated with the logic state of each faulty machine being simulated, a faulty machine being the original network with one fault inserted. The effects of a fault in the network may be to make the states of certain nodes different than what they should be in the state of the good or unfaulted machine. In effect, a number of different simulations are done simultaneously or in parallel. The number of faulty machines simulated in parallel with the good machine is usually determined by the word length of the computer on which the simulator is run, although this is not a restriction.

Once the effects of a fault have been detected at the network outputs or the simulation is completed, that fault is dropped from the list of faults to simulate, and the simulation results are added to a list of faults detected/not-detected. The faults for each simulation pass are usually chosen sequentially from the list of faults to simulate until the list is empty. A degenerate case of parallel fault simulation, known as serial (or single) fault simulation, occurs when only one faulty machine is simulated in parallel with the good machine.

The computer run time for parallel fault simulation is related to the number of faults simulated, the number of machines simulated in parallel, and the efficiency of the algorithm that runs the analysis. Parallel fault simulation makes no intense use of memory. Because of the restricted memory size of the Cyber 175, it was chosen as the method for use in TLOGS.

Deductive Fault Simulation

Deductive fault simulation simulates the behavior of the fault-free circuit and deduces the behavior of the faulty circuits. In this method, there is a fault list associated with every node in the original circuit. By using the current input states of an element and the fault lists associated with these inputs, the simulation deduces which faults may be propagated to the element's outputs. Each fault list, therefore, provides a record of the faults that are detectable at that node of the circuit at each simulation timestep. As the simulation proceeds, the lists of faults associated with the network's output nodes are incorporated into the list of detected faults.

Since the number of faults that may affect a particular node is unknown before the simulation, the length of the fault list associated with each node in the network must be allowed to vary dynamically. A network for which this necessity is emphasized would contain many memory elements. These memory elements potentially propagate fault effects much further through the network than in a purely combinational circuit, and may create much longer fault lists.

The computer run time required for deductive fault simulation is related to circuit topology (for example, the presence of memory elements), and the efficiency of the algorithm. However, because sequential circuits may propagate the effects of faults further through the circuit, thus creating longer fault lists, a virtual-memory computer is almost a necessity.

Concurrent Fault Simulation

Concurrent fault simulation is similar to deductive fault simulation in that the effects of all network faults are simulated concurrently with the behavior of the good circuit (that is, only one simulation pass is done on the network). While simulating the good circuit (machine), any differences in the node states caused by the faults under consideration are noted. The effects of these faults are then simulated by adding phantom gates – known as fault-effect gates (FEGs) – into the circuit. These pseudo gates are added to and removed from the network dynamically whenever faults would change the state of a node.

The concurrent method, therefore, is more efficient than the deductive method because only faults which change the behavior of the good network are considered. The faults that are detectable are those that would cause FEGs to be connected to the outputs of the network.

The run time required for concurrent fault simulation, like the deductive method, is related to the efficiency of the timing-analysis algorithm, and the circuit topology. Concurrent fault simulation differs from the deductive method, however, in that fault lists (which may attain any length) are no longer associated with the nodes in the circuit. However, there is no prior indication as to the number or complexity of fault-effect gates which must be added to the network. A fault on the master clock of a circuit, for example, may suddenly change the network topology by forcing the addition of thousands of FEGs. Therefore, a virtual-memory computer is again a necessity for this type of fault simulation. □

INTRODUCTION TO HYBRID CIRCUITS

Mal Gilbert, Hybrid Circuits Engineering, B-4021.

Dave Miller, Hybrid Circuits Engineering, B-4023.

This article is part of the Tektronix Hybrid Circuit Design Course given from time to time by Hybrid Circuits Engineering. This course is designed to equip engineers with the knowledge, skills, and tools to:

- **Lay out hybrid circuit substrates and passive networks**
- **Perform basic feasibility and research studies using hybrid microelectronic procedures and techniques**
- **Design and develop manufacturable hybrid and passive thick film or thin film components**

The electronic industry's trend towards hybrid microcircuitry was initiated by military application requirements over 30 years ago, and now impacts every segment of the industry from avionics and instrumentation to consumer products.

During the 1970s, the hybrid industry survived the lean years, and hybrid technology matured to the point where hybrid circuits often proved to be the most cost-effective solution to today's circuit packaging problems. For many years skeptics of hybrid circuits were forecasting the demise of an industry whose current products were continually being replaced by new integrated-circuit developments. The skeptics failed to realize, however, that hybrid circuits and integrated circuits are compatible, rather than competitive technologies.

It has been demonstrated on many occasions that an IC's usefulness may be optimized by placing it in a hybrid circuit. Over the years, the non-captive hybrid industry has shown solid growth, and is forecast to continue to grow at 21 percent per year, through the 1980s.

Hybrid Technology

Although it is commonplace to refer to 'hybrid technology', in reality there are many independent hybrid technologies, pulled together by a complex network of process and package options. The unlimited design flexibility afforded hybrid designers, and the wide array of packaging styles available can appear very confusing to the casual observer. As an example, for a given set of electrical and environmental performance criteria and mechanical constraints of the component (i.e., form, fit, and function), there may be several fully acceptable hybrid solutions, each using a different technology or combination of technologies. Studying this problem, it soon becomes clear that for hybrid-circuit manufacturers to remain viable, they cannot offer every conceivable combination of these technologies, and some choices have to be made to limit the number of process, material and package options that are to be made available. These technologies must then be developed to the fullest extent possible, and their utility exploited by innovative applications, before a new technology is adopted. Each new hybrid technology requires a large capital investment and many man-years of development and characterization before it is ready to be incorporated on a production line. This makes the development choice for a new technology a very critical decision.

The range of processes and packaging styles offered by a hybrid manufacturer is a function of the market intended to be served. The Tektronix hybrid facility has evolved in such a way that the vast majority of our hybrid circuit applications can be fulfilled by the current range of technologies offered. Virtually every new hybrid circuit represents a custom design involving unique electrical and mechanical requirements tailored to a specific application, and it is necessary for hybrid manufacturing to be able to accommodate these designs while still operating within the boundaries of the chosen technologies. Obviously, the choice of technologies is crucial to the success of the operation.

A brief review of hybrid circuits and associated components currently being produced at Tektronix indicates that most components fall into one or more of the following categories:

- Low-cost thick-film networks
- General-purpose solder-reflow/surface-mount thick-film hybrids
- High performance low-volume chip-and-wire
- Low-cost, high-volume array fabricated chip-and-wire
- Thin-film, high-frequency chip-and-wire
- Thin-film precision resistor networks
- Thick-film multilayer chip-and-wire hybrids

(It should be pointed out that hybrid circuits falling into categories other than those listed here may still be candidates for hybrid production at Tektronix, but may require negotiations and a degree of coordination with the manufacturing areas. In many cases, restrictions which first appear to be due to process or package limitations may be circumvented by the use of innovative design techniques. In other cases, new materials and processes may require development in order to meet a newly identified need. An example of the latter would be large-area hermetically-sealed hybrids; such components are common in the aerospace industry, but the lack of the need for hermeticity in a typical instrument application has led to this style of packaging remaining undeveloped at Tektronix.)

It was stated earlier that this choice has evolved at Tektronix over the past decade and was primarily market-driven. This has been augmented more recently by the need to identify structured product lines in the manufacturing flow, the purpose being to increase overall productivity.

The manufacturing product lines provide the capability to process substrates and provide various assembly processes to produce hybrids at Tektronix. Substrate and assembly processes, along with package styles, are illustrated in Figure 1.

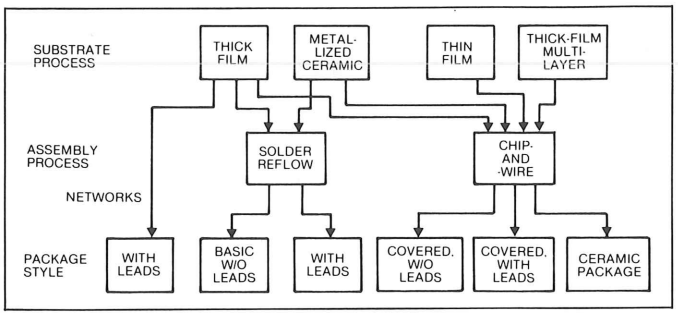

Figure 1. Tektronix basic hybrid families.

Substrates

The following discussion lists the four general classes of processed or patterned substrates, followed by an overview of each class. When substrates are used without add-on components they are referred to as 'networks', rather than hybrid circuits. Networks may, however, have pins, leads, or other interconnecting means added to them.

- **Thick-film substrates** – insulating substrates on which conductor paths and/or passive circuit elements have been deposited by a screen-printing and firing process.
- **Thin-film substrates** – insulating substrates on which conductor paths and/or passive circuit elements have been deposited by means of vacuum evaporation or sputtering techniques.
- **Multilayer-ceramic substrates** – alternating layers of insulating ceramic sheet (tape) and screen-printed refractory metal (conductor paths), laminated and co-fired to form a homogeneous substrate. The conductor layers may be interconnected by means of through-holes (vias) in the ceramic layers. Sometimes referred to as 'metallized-ceramic' substrates, there may be instances when they do not consist of multiple layers.
- **Thick-film multilayer substrates** – insulating substrates on which alternating layers of conductor paths and insulating (dielectric) material are screen-printed and fired. Conductor layers may be interconnected by means of vias in the dielectric layers.

Components

Thick- and thin-film substrate passive elements consist of resistors, capacitors, inductors, or any combination thereof. The range of both capacitive and inductive values, however, is severely limited. Resistive elements only are permitted on thick-film multilayer substrates, and passive elements are not available as part of multilayer-ceramic substrates.

Add-on components may include resistors, capacitors or inductors, together with virtually any semiconductor device made, from bipolar and FET transistors to sophisticated LSI devices, including all logic families, and memory and microprocessor ICs. The form that these components take depends upon the assembly technique used to attach them to the substrate.

Assembly

Product lines at Tektronix currently employ two basic techniques: Chip-and-Wire and Solder Reflow.

- **Chip-and-Wire** – Chip-and-wire hybrids contain active add-on devices in their silicon chip form, with their gold or aluminum metallization pads being connected to appropriate pads on the substrate pattern by means of gold wires bonded to their respective pads. Passive add-on devices are also occasionally wire-bonded, but most often are attached to the conductor pattern with conductive epoxy. Their form in this case consists of metallized end-caps on a rectangular body, although they are still usually referred to as 'chips'. Chip-and-wire attachment is applicable to all four classes of processed substrates.
- **Solder Reflow** – Using the solder reflow attachment process, all add-on devices (active and passive) must be obtained in a suitably packaged format, such as the 'small outline transistor' (SOT). In this form, the semiconductor die is attached to a 'lead' frame, wire-bonded, and epoxy encapsulated. The lead frame then forms miniature 'feet' which are subsequently reflow-soldered onto corresponding pads (the 'footprint') on the substrate conductor pattern. A major advantage of the solder reflow attachment process is that all such add-on components may be attached to the substrate in a single step, in contrast to the chip-and-wire process where each chip is individually attached to the substrate, after which all interconnecting wires are sequentially bonded. Because of the way in which the microminiature-packaged devices are placed on the surface of the substrate in the solder reflow process, hybrids employing this process will often be referred to as 'surface-mount' hybrids. Other packaged add-ons, such as chip carriers, may be substituted for small outline-packaged ICs, but typically they will be more costly than the equivalent small outline device.

In general, chip-and-wire and solder reflow are considered non-compatible processes. A successful chip-and-wire operation requires chemically clean conditions, particularly on the bond sites, which are difficult to guarantee following a soldering operation. On the other hand, if the soldering operation is performed after chip-and-wire, great care must be taken to protect the bonding wires and the chip surfaces from the solder and other materials used during the soldering operation. One case where this is acceptable is the chip-and-wire circuit which uses soldered-on leads. In this case, the chips and their bond wires are sealed with a ceramic cover, then the leads are soldered into place as the final step.

Packaging styles

All chip-and-wire hybrids require mechanical and environmental protection. This may consist of a cover epoxied onto the substrate, or the entire substrate assembly may be placed inside a sealed ceramic package. Surface-mount hybrids require no such protection, and may be used as substrate assemblies, with or without leads attached. Thick-film multilayer and thin-film substrates are suitable for chip-and-wire assemblies only. Thick-film and multilayer (metallized) ceramic substrates may be used with both basic hybrid 'product families', which are aligned to Tektronix' manufacturing capabilities. Many other technologies and materials are available on a custom basis, or in low-volume prototype runs. □

PAPERS AND PRESENTATIONS

The table below is a list of papers published and presentations given during recent months.

While providing recognition for Tektronix engineers and scientists, the presentation of papers and articles contribute to Tektronix' technological leadership image.

If you plan to submit an abstract, outline, or manuscript to a conference committee or publication editor, take advantage of the services that Technology Communication Support (TCS) offers.

TCS provides editorial and graphic assistance to Tektronix engineers and scientists for papers and articles presented or published outside Tektronix and obtains patents and confidentiality reviews as required.

Call Eleanor McElwee on ext. MR-8924. □

JUNE

TITLE	AUTHOR	PUBLISHED	PRESENTED
Industrial Robots: What and Why	Bob Rullman		International Society of Hybrid Manufacturers Regional Meeting Portland, OR
How CAD/CAM Can Enhance the Productivity of Industrial Design	Larry Eisenbach		IDSA/NCGA Joint Conference, Anaheim, CA
Serviceability: Trends and Strategies	Bob Wruble		IBM Service Seminar Poughkeepsie, NY
Birth of a Terminology Standard	Chuck Sullivan		ATSM Terminology Seminar, Toronto, Canada
Silicon Nitride for Encapsulation and Passivation of Gallium Arsenide	Venkat Rao Richard Loyama		Workshop Dielectric Systems for III-V Compounds, San Diego, CA
Digital Systems Troubleshooting with Logic Analysis	John Huber	**Electronic Servicing Technology**	
Temperature Profiles Induced by a Scanning SW Laser Beam	Rudi Hendel J.E. Moody	**Journal of Applied Physics**	
Local Area Nets: A Pair of Standards	Maris Graube	**IEEE SPECTRUM, June**	
No Loose Ends – Part I. Techniques for Tests and Measurements Using the Spectrum Analyzer	Linley Gumm	**Communications Engineering Digest**	
Designer's Guide to GPIB Instruments – Part I: Understanding IEEE-488 Basics Simplifies System Integration	Mark Tilden	**EDN, June 9**	
Coprocessing Expedites Software-Hardware	Mike Zuhl	**Electronics, June 30**	

JULY

TITLE	AUTHOR	PUBLISHED	PRESENTED
Design for Automatic Component Placement	Scott Enochs		ISHM 1982 Microelectronic Interconnect Conference, Everett, WA
High Magnetic Moment in Fe87B11Au2 Ribbons	C.S. Severin		3rd Joint Intermag Conference Montreal, Canada
CAD/CAM Workstation Design	David Verhoeven		SIGGRAPH '82
The SECAM Color Television System	Les Weaver	**Tektronix (book)**	

AUGUST

TITLE	AUTHOR	PUBLISHED	PRESENTED
Circuit-Board Vibration – A Computer-Aided Design Study	Brian Wood Barry Ratihn		ASME 2nd International Computer Engineering Conference
No Loose Ends – Part II. Techniques for Tests and Measurements Using the Spectrum Analyzer	Linley Gumm	**Communications Engineering Digest**	
What If Mass Storage Were Free?	George Copeland	**IEEE Computer**	
Designer's Guide to GPIB Instruments – Part II: GPIB Software Configuration Determines System Performance	Mark Tilden Bob Ramirez	**EDN**	
Programmable Terminals Raise Graphics Efficiency	Bruce Coorpender	**Electronic Design**	
How Good Are Today's Op-Amps?	Calvin Diller (Interview)	**Electronic Products**	

SEPTEMBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
Measures of Operator's Visual Accommodation and Convergence to Information Displays	Gerry Murch		Eurographics '82, Manchester, U.K.
A Methodology for Populating Default Color Maps	Dave Straayer		Eurographics '82, Manchester, U.K.
Effective Logic Analysis Techniques for Increased Design Productivity	Chuck Nobles John Huber John Blattner		WESCON '82, Anaheim, CA
Software Productivity in the 'Make or Buy' Decision	Rodney Bell		WESCON '82, Anaheim, CA
Designing Reconfigurable Test Systems	Steve Jumonville		WESCON '82, Anaheim, CA
Alternative Marketing Strategies for the New Electronics Markets	John Gragg		WESCON '82, Anaheim, CA
The Promise of Bipolar VLSI for High-Speed A-to-D Converters	George Wilson		WESCON '82, Anaheim, CA
Strategic Planning	Larry Mayhew		GenRad Conference, Boston, MA
Software Quality Assurance	George Tice		IEEE Computer Society Conference of Medical Computer Science and Computational Medicine
A Building Block for Digital Signal Processing: The Digital Operational Amplifier	Tran Thong Robert Sparkes		IEEE Conference on Circuits and Computers, New York, NY
Software Quality Planning	George Tice		ASQC Western Regional Conference Phoenix, Arizona
Interconnect Net Navigates Airline Reservations	Ted Harris (not bylined)	**Data Communications**	
Network Heal Thyself: A Diagnostic Primer	Garth Eimers	**Computer Design**	

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Development Systems Interface Expedites Software Design	Jim Desemer	**Electronic Design**
Storage Scopes: A Variety of Techniques and Capabilities	Doug Goodman	**Electronic Products**
Do You Need Color?	Gerry Murch	**Electronic Products and Technology (Canada)**

OCTOBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
User Interface Aspects of a Desktop CAD System	John Harms		Western Design Engineering Conference
Software Quality Assurance: A New Experience?	George Tice		SRE/ASQC Reliability and Quality-Control
Probe Gripper	Brent Anderson		Stanford University Design Affiliates Program
A System View of the Documentation Package: The Technical Editor's Contribution	Jack Falk		IEEE Professional Communications Society Conference, Boston, MA
High-Frequency IC Probe	Tom Reeder		Magnavox
The Vredeling Proposal and the Fifth Directive	John Landis		Machinery and Allied Products Institution New York, NY
Electron-Beam-Addressed Liquid-Crystal Light Value	Duane Haven		International Display Research Conference, Cherry Hill, NJ
Mechanisms of the Negative-Resistance Characteristics in AC Thin-Film Electroluminescent Devices	Kei-Wean Yang		International Display Research Conference, Cherry Hill, NJ
Organization of International Service	Larry Taylor		CBEMA Service Management Council, Washington, DC
Going International	John Landis		University of South Carolina, MBA Seminar
Using Card-Modular Equipment in the Implementation of IEEE-488 Test Systems	Dave West		ATE Seminar, Rosemont, IL
Reliability Evaluation of 16K Dynamic RAMs in Plastic Packages	Bill Roesch Art Fraser		International Symposium for Testing and Failure Analysis (ISTFA) Santa Clara, CA
Methods in the Rheological Characterization of Thick-Film Materials	Bill Howell		American Ceramic Society Pacific Coast Regional Meeting Seattle, WA
Friendly Software for Test and Measurement	Steve Peterson	**Computer Design**	
Logic Analyzer Market Belongs to Innovators	Chuck Wiley John Blattner	**Computer and Electronics Marketing**	
Testing Data Communications Networks in the Field	Robert Cook Eric B. Lane	**Electronics Test**	

No Loose Ends – Part III. Techniques for Tests and Measurements Using the Spectrum Analyzer	Linley Gumm	**Communications Engineering Digest**
Portable Spectrum Analyzers Answer Rugged Environment Requirements	Russ Brown Morris Engelson	**Military Electronics/ Countermeasures**
Tests and Measures Go On Location	Rex Stevens	**Educational and Industrial Television (E&ITV)**
Reducing Test Equipment Downtime	Ernie Johnson	**Electronic Products**

NOVEMBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
Screen Process for Very-High-Resolution Color Display	Patrick Green		Portland State University
Reduction of Power Bus Noise in GaAs Digital Systems	Arnold Frisch		GaAs IC Symposium, New Orleans, LA
GaAs Sample-and-Hold IC Using a 3-Gate MESFET Switch	Gary Barta Ajit Rode		GaAs IC Symposium New Orleans, LA
A GaAs MSI, 8-Bit Multiplexer and Demultiplexer	Gary McCormack		GaAs IC Symposium, New Orleans, LA
NATFIN – An Interactive Thermal Analysis Program for Natural Convection/Radiation-Cooled Heat Sinks	Gordon Ellison		Electronics Packaging Society National Conference, San Diego, CA
An Elastomeric Interconnect for Oscilloscope Probes	Ken Smith		Electronics Packaging Society National Conference, San Diego, CA
Edge-Printing Thick-Film Wrap-around Conductors	Dean Monthei		ISHM, Reno, Nevada (poster session)
Testing the Dynamic Performance of High-Speed A/D Converters	Kyohito Uchida		Cherry Hill Test Conference, Philadelphia, PA
Simplify Microprocessor Test Generation by Combining a Microprocessor Development System with a Test System	Charles Hinchcliff		Cherry Hill Test Conference, Philadelphia, PA
High Magnetic Moment in Fe87B11Au2 Ribbons	C.S. Severin C.W. Chen	**Journal of Applied Physics**	
Progress Report: Spectrum Analyzers	Morris Engelson	**EE Times**	
Color Display Clears Up Analysis of Digital Logic Data	Gerry Murch	**Electronic Design**	

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DECEMBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
Mathematical Modeling of Thick-Film Resistors	Raj Garg		ISHM Northwest Chapter Meeting, Seattle, WA
Vertical BMOS Power Field-Effect Transistors Optimized for High-Speed Operation	Dennis Fuoss		International Electron Devices Meeting (IEDM), San Francisco, CA
A High-Yield GaAs MSI Digital IC Process	Ajit Rode Angus McCarmant Gary McCormack Bill Vetanen		International Electron Devices Meeting (IEDM), San Francisco, CA
Local-Area Networks, Standard, and the IEEE-802 Committee	Maris Graube		Symposium on Local-Area Networks, Sydney, Australia
No Loose Ends – Part IV	Linley Gumm	**Communications Engineering Digest**	

UPDATE ON TMS 9914A GPIB INTERFACE

By John Burgess, Automatic Instrument Compatability Evaluation (AICE), ext. B-1795

Because the TMS 9914 GPIB interface IC is widely used at Tek, Tek designers know this Texas Instrument IC well. They know how to apply and program it for talker/listener and controller functions. Because of this experience and the 9914's adaptability to Tek products, AICE continues to recommend it's successor, the 9914A, for future designs.

However, there are some errors in the early TI literature on the 9914 and its associated drivers; the literature also lacks some information important to Tek designs. The literature problems and shortcomings in respect to Tek usage are described in the December 3, 1982 issue of *Component News*. I suggest that you check this information. Copies are available from Technical Communications, d.s. 76-036.

We in the AICE group would like to know of implementations of the 9914A, or if you have stumbled on any other quirks and problems in the 9914A itself or in the documentation. Your experiences can help others, perhaps, from reliving your frustrations. We need to know these details to help others use this excellent IC to full advantage.

Send your discoveries to John Burgess, d.s. 50-761 (ext. B-1795). □

EDN CARAVAN TO VISIT

The Cahners EDN Caravan will visit four Tektronix sites February 28 through March 2. This "electronic show on wheels" is directed toward hybrid circuits engineers but will be open to all Tektronix employees. Seventeen exhibitors are participating:

TRW LSI Product
RCA Solid State Division
American Microsystems, Inc.
NCR Microelectronics Division
United Technologies Mostek
Honeywell Optoelectronics Division
EECO Inc.
Robinson Nugent, Inc.
Positronic Industries Inc.
ACDC Electronics
Grayhill, Inc.
Siemens Corporation Special Product
Panduit Corp.
MUPAC Corporation
ITW Switches
Clare Division, General Instrument Corporation
Beckman Instruments, Inc.
Xicor, Inc.

Wilsonville — Monday, February 28 – 1:30–4:30 p.m.
Building 63 parking lot

Beaverton — Tuesday, March 1 – 9:00–12:30 p.m.
Building 59 parking lot

Walker Road — Tuesday, March 1 – 2:00–4:00 p.m.
Building 94 parking lot

Vancouver — Wednesday, March 2 – 8:30–10:30 a.m.
C1-South parking lot

PLASTICS SAVE, PLATING PLASTICS IMPROVES

By Marianne McPherson, Metals-Electrochem Process Engineering

Choosing to use plastic parts rather than metal often reduces both weight and costs. For example, ABS is about 1/3 the weight of 384 aluminum and 1/8 the weight of C33000 brass. Based on raw material costs, ABS costs are about 1/5 that of aluminum and 1/13 the cost of brass.

As plastic materials become an increasingly desirable alternative to metal substrates, Metals-Electrochem would like to re-emphasize its capabilities for plating Tek-made or outside-purchased plastic parts.

Plastic parts are plated to provide electrical conductivity and EMI/RFI/ESD shielding, and to improve appearance and abrasion resistance. Plating also protects plastics against harsh environments and improves a part's tensile, flexural, and impact strength.

Metals-Electrochem has processes for electroless nickel and copper plating on the following plastics: ABS (acrylonitrile-butadiene-styrene), polysulfone, and polyurethane. We are also interested in either developing an in-house capability or assisting our "customers" to find outside sources for plating other plastics such as Delrin (acetal resin), Noryl (modified polyphenylene oxide), nylon (polyamide), polycarbonate, polyethylene, polypropylene, styrene, and Teflon (polytetrafluoroethylene).

You can avoid some plating problems inherent in certain shapes and grades of plastic by talking to us. We are available for advice in these and other design decisions that can reduce your part cost. For further information contact Jerry Heppell (ext. B-2500) or Larry Helton (ext. B-0253), Metals-Electrochem Process Engineering. □

Trademarks

Delrin — duPont
Noryl — General Electric
Teflon — duPont

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Back issues of *Technology Report* are available. Call Charlotte Shumaker, ext. MR-8920 (d.s. 53-077).

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TECHNICAL STANDARDS

CAMAC Instrumentation and Interface Standards — Seven American National Standards on CAMAC are now available in hardcover. These standards cover modular instrumentation and digital interface systems, serial- and parallel-highway interface system multiple controllers in a CAMAC crate, block transfers, real-time BASIC for CAMAC, and subroutines, $34.95

EIA Proposed Standard — FOTP #83 Cable to Interconnecting Device Axial Compressive Loading (If approved, to be published in the RS-455 Series)

EIA Proposed Standard — FOTP #99 Gas Flame Test for Fiber Optic Cable (If approved, to be pubished in the RS-455 Series)

FED STD NO. 1230 — Notices 3 and 4 – Marking for Shipment (Civil Agencies)

IEC 304 — Standard Colours for Insulation for Low-Frequency Cables and Wires, $13.00

New Standard

TEKTRONIX Calibration System Requirements — 062-6922-00

Tek Standard 062-6922-00 — Describes the role and activities of the Electrical Standards Laboratory. It also explains the relationships of the laboratory to other groups involved in the electrical calibration system of the company. This standard will not be distributed automatically. For copies, contact Carol Whitmore, ext. B-1807.

Proposed Revisions

EIA-RS-469 — Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors

FOTP #49 — (If approved, to be published in the RS-455 Series) Procedure to Measure Nuclear Radiation Effects on Optical Waveguides

FOTP #88 — (If approved, to be published in the RS-455 Series) Fiber Optic Cable Corner Bend Test

UL — Supplement to Recognized Component Directory, $11.20

MIL-F-8975B — Fasteners, Blind High Strength, Installation Formed, Corrosion Resistant Steel, Heat Resistant Steel and Titanium

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BOOKLET AVAILABLE ON EMI SHIELDING OF PLASTIC

Although electric fields penetrate plastics, when metal is somehow integrated, plastics can provide effective, economic electromagnetic shielding. An analysis of ten methods of making plastics shield against E.M.I. are described in *Radiant E.M.I. Shielding for Tektronix.* This booklet is available from Electrochem Advanced Process Development, ext. B-0303.

Jerry Holly, the author concludes, from the research into 10 shielding methods: "There are several E.M.I. shielding methods available which provide excellent attenuation. The data shows that for the money, electroless nickel is the best system. Previous testing has shown electroless nickel to be environmentally acceptable. The question of U.L. approval must be addressed regardless of which method is used."

"It does not appear to be economically feasible to plate large parts, e.g., cabinets. Therefore, it is recommended that the major shielding be done directly over any noisy components. If plastic is used, an electroless nickel plate with or without some electroplate would be the best choice. Any remaining E.M.I., whether due to leakage of shielded parts, or unshielded parts, if small enough, could be shielded by coating the cabinet with a conductive paint such as a nickel loaded paint. In certain cases it may be necessary to coat both sides of the cabinet with a conductive paint, and then add a decorative coat to the outside." □