TEK SERVICE MANUAL TEKTRONIX Part No. 070-6799-00

2782 SPECTRUM ANALYZER

Module Level Service Manual

WARNING

The following servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing any service.

Please check for CHANGE INFORMATION at the rear of this manual

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Tektronix
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Table of Contents

Figures

Tables

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Do Not Service Alone
Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Do Not Wear Jewelry
Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

Use Care Servicing With Power On
Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source
This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

X-Radiation
X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the crt enclosure.

Do Not Operate In Explosive Atmospheres
To avoid explosion, do not operate the instrument in an explosive atmosphere unless it has been specifically certified for such operation.

Grounding the Product
This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger From Loss of Ground
Upon loss of the protective ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

CRT Handling

Use care when handling a CRT. Breakage of the CRT causes a high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the CRT on any object which might cause it to crack or implode. when storing a CRT, place it in a protective carton or set it face down in a protected location on a smooth surface with a soft mat under the faceplate.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors see Section 1.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER High Voltage.

Protective ground (earth) terminal.

ATTENTION Refer to manual.

General Information

This manual provides service information for the 2782 Spectrum Analyzer. It is intended for use by qualified service technicians to aid in checking performance, making adjustments, troubleshooting, and repair. Technicians should have experience with spectrum analyzer service, and should be familiar with analog and digital circuitry, including RF an d microwaves, microprocessors, computer control, etc.

Refer to the 2782 Operators Manual for a complete product description, including specifications, operating procedures, and error and warning messages.

Refer to the 2782 Programmers Reference Manual for complete programming information.

This manual contains the following sections:

Performance Check
Adjustment Procedure
Maintenance
Theory of Operation
Replaceable Electrical Parts List
Replaceable Mechanical Parts List
Exploded View Mechanical Drawings
Overall Block Diagram
RF Deck Interconnect
Motherboard Connections
Keyboard Service Commands

The Performance Check procedure uses a computer-based program to aid in checking instrument performance. The program is included on the Performance Check disk and on the Flatness Check disk, included in the disk holder in this manual.

The Adjustment Procedure provides a guide for performing regular instrument calibration.

The Maintenance section provides preventive, troubleshooting, and corrective maintenance information.

The Theory of Operation gives block descriptions to aid in servicing to the module level.

The Electrical and Mechanical parts lists provide lists of all the replaceable parts and assemblies in the instrument. The Exploded View diagrams show locations to help in removing and replacing faulty parts and assemblies

The Block Diagram, Interconnect Diagram, and Motherboard Connections provide information to help troubleshoot and adjust the instrument.

The Keyboard Service Commands dictionary provides a list of the commands available in the Service mode when using a terminal with the RS-232 port on the Processor Extender board (available in the Service Kit).

Product Service

To assure adequate product service and maintenance for our instruments, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available.

For example, for a fixed fee, a maintenance agreement program provides maintenance and recalibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time.

Tektronix emergency repair service provides immediate service when the instrument is urgently needed.

Contact your local Tektronix Service Center, representative, or sales engineer for details regarding product service.

Module Exchange Program

The TEKTRONIX 2782 Spectrum Analyzer has been designed with a module exchange service approach. Service is performed by identifying a faulty module and exchanging it with a properly functioning module. This information details the process for obtaining a properly operating module from Tektronix. A list of the exchangeable modules is contained in the Replaceable Electrical Parts List.

Note

Module service and exchange should be performed by qualified service personnel only.

Module Exchange Service (U.S. Customers)

To obtain a properly operating module, please call the Tektronix Module Exchange Center between the hours of 6:00 AM and 5:00 PM (Pacific Time) Monday through Friday, at the following telephone number:

1-800-TEKWIDE, Ext. MR8600 (for Service Assistance)

The person answering the call will confirm the availability of a proper operating module and arrange shipping within 72 hours of the confirmation. (Most modules will be shipped within 24 hours of the request.)

Module shipment will be made by your choice of carrier. (e,g, - priority, express, one-day, overnight delivery, or common carrier service). After you receive the replacement module, the faulty module must be returned immediately to Tektronix via prepaid common carrier freight. Use the packaging material from the replacement module to prepare the faulty module for return shipment. A return shipping label will be furnished with the replacement module.

A standard fee is charged for each out-of-warranty module exchanged, and will be quoted when the exchange module is requested. If the faulty module is not received at the Module Exchange Center within 15 working days after the original request, the full price of the module will be charged.

Full price will also be charged for modules returned that do not qualify for the Module Exchange Program. Modules are not acceptable for exchange rates if they are:

- Damaged from repair attempts (other than by Tektronix)
- Damaged from improper use or connection to incompatible equipment
- Modified by the customer
- Custom modified by Tektronix (by customer order)

The Module Exchange Center can provide further details on pricing, invoicing, and shipping methods.

Service for Customers Outside of the U.S.

Customers outside the United States should contact their local Tektronix sales subsidiary or distributor for details on servicing.

Power Information

The rear panel line voltage selector allows you to select either 110 V or 220 V (47 to 440 Hz) nomianl supply source. Use the 4 A 125 V fuse for 115 V operation, or the 4 A 250 V fuse for 230 V operation. The proper fuse must be used to meet the safety requirements for each level of operation.

Performance Check

This section provides a performance check procedure for the instrument.

Introduction

This performance-check procedure checks the 2782 performance against the specifications given in the Operators Manual. The performance checks are divided into two parts. The first part checks the flatness specifications for the instrument, and the second part checks the rest of the instrument specifications.

Both parts of this procedure are designed to be used with a personal computer and performance-check software, which automates some of the setup of the 2782 and the recording of test data. The flatness-check software is a stand-alone program called CATS. The performance-check software used for the remainder of the performance checks is a spread sheet that runs on Lotus 1-2-3 and Lotus Measure.

Performance Check Environment

The ambient temperature for the area where the performance check is going to be performed should be within ±5° C of the temperature at which self-correction of the instrument was performed. The ambient temperature during factory calibration is 20° C.

Before making any of these checks, the 2782 should be allowed to warm up for at least one hour.

Equipment List

The following equipment is required to perform the performance verification tests given in this section.

Table 2-1. Equipment Required for Performance Checks

Item	Characteristic	Recommended
1. Personal Computer	Intel 8088 CPU or better, MS-DOS 2.0 or better, dual floppy-disk drives or one floppy-disk drive and one hard-disk drive; 640 KBytes of RAM; graphics monitor; and one National PC2 or PC2A GPIB interface board. NOTE: An 80286-based PC (IBM PC AT or equivalent), EGA graphics card and monitor, MS-DOS 3.1 or later, and a second GPIB interface board are required for the Flatness checks. The GPIB Interface boards for the Flatness check must be National PC2A compatible.	IBM PC XT or equivalent (IBM PC AT or equivalent for Flatness checks). or TEKTRONIX PEP301 with Tektronix S3FG120 GPIB Interface board. (Two GPIB Interface boards required for Flatness checks)
2. GPIB Interface Cable(s)	GPIB Interconnecting cable, 2 meters long. NOTE: Four GPIB cables are needed for the Flatness checks, and only one cable is required for the rest of the Performance Checks.	Tektronix Part No. 012-0630-01
3. Performance Check Software		TEKTRONIX 2782 Performance Verification Software (supplied), Lotus 1-2-3 Version 2.2 or later, Lotus Measure, Version 1.0 or later. Two blank, formatted, 5.25-inch floppy disks. NOTE: For the Flatness checks, the Flatness software (supplied with the manuals) is also required.
4. Test Oscilloscope	100 MHz frequency range	TEKTRONIX 2235 Oscilloscope
5. Counter	9-digit accuracy, 10 MHz to 100 MHz frequency range, and lockable to 10 MHz external reference signal	Hewlett-Packard HP5316A

Table 2-1. Equipment Required for Performance Checks (Continued)

Item	Characteristic	Recommended
6. Power Meter	0 to 33 GHz frequency range	Hewlett-Packard HP438A with HP8484A and HP 8481A Power Sensors, and HP11708A 50 MHz 30 dB Reference Attenuator NOTE: For Flatness checks only, two additional power sensors are required.. An HP8487A replaces the HP8481A above, and an HP8482A is needed in addition to the other two power sensors.
7. Frequency Standard	10 MHz output, 0.01 Hz accuracy	WWV standards receiver or equivalent high-accuracy standard
8. Signal Generator	10 Hz to 112 MHz frequency range, with less than -50 dBc harmonic distortion. and lockable to 10 MHz external reference signal	Hewlett-Packard HP8642A Synthesized Signal Generator or equivalent
9. 500 MHz Comb Generator	500 MHz and harmonics, with connector head and 6 dB attenuator	Microwave Comb Generator. Tektronix Part No. 067-0885-00
10. Time Mark Generator	1 ns to 0.1 s marker output	TEKTRONIX TG501
11. Function Generator	3 Hz to 10 MHz frequency range	TEKTRONIX FG5010
12. Power Module	Required for TM500/TM5000-series test modules	TM5000-series Power Module (Option 02 required for external reference input)
13. Step Attenuators	1 dB steps, accurate within 0.1 dB at 100 MHz 10 dB steps, accurate within 0.5 dB at 100 MHz	Hewlett-Packard HP355C Hewlett-Packard HP 355D
14. Fixed Attenuators	6 dB 50 Ω SMA (2 each) 10 dB 50 Ω, 2 W, dc to 12.4 GHz, N Connector	Tektronix Part No. 015-1001-00 Tektronix Part No. 011-0085-00
15. Terminators	50 Ω BNC feedthrough termination. 50 Ω SMA-male end termination	Tektronix Part No. 011-0049-01 Tektronix Part No. 015-1022-00
16. Coaxial Cables	BNC, 50 Ω ±1% precision, 36 in. BNC, 50 Ω, 42 in. (2 each) SMA, 50 Ω, 28.5 in.(2782 standard accessory)	Tektronix Part No. 012-0482-00 Tektronix Part No. 012-0057-01 Tektronix Part No. 012-0649-00
17. Connector Adapters	BNC male to BNC male (2 each) BNC female to BNC female BNC female to SMA female BNC T (2 each) N female to SMA male SMA female to SMA male	Tektronix Part No. 103-0029-00 Tektronix Part No. 103-0028-00 Hewlett-Packard 1250-2015 Tektronix Part No. 103-0030-00 Hewlett-Packard 1250-1562 Hewlett-Packard 1250-1462
18. BNC-to-Dual Pin Out Cable	Provide two pins for connecting to 2782 Accessories Interface Connector (DF-15 style connector)	Tektronix Part No. 175-1178-00

Table 2-1. Equipment Required for Performance Checks (Continued)

Equipment for Optional Checks in Performance Check Procedure		
Item	**Characteristic**	**Recommended**
20. Synthesizer/Level Generator	Used only for second- and third-order intercept checks. It is used in conjunction with the signal generator specified in item 8 of this list.	Hewlett-Packard HP3336C
21. Swept Frequency Generators (2 each)	dc to 40 GHz NOTE: Second generator is required only for second- and third-order intercept checks.	Wiltron 6769B
22. Combiners (4 required)	Combiners are only needed for the second- and third-order intercept checks.	Mini-Circuits 2FSC-2-5 Mini-Circuits 2FSC-2-6 Narda 4324-2 (2 to 6 GHz) Narda 4328-2 (10 to 33 GHz) (All four are required for these checks)
23. Low-Pass Filters (4 required)	Low-pass filters are only required for second harmonic distortion check.	K&L 4751-15-B/B K&L 5L51-551-B/B K&L 5L120-850-O/O K&L 3L120-3500-O/O (All four are required for these checks)
24. Test Spectrum Analyzer	LO Out Phase Noise equal to 2782 (required only for Phase Noise Check) 10.525 GHz Center Frequency (required only for LO Emissions check)	Another TEKTRONIX 2782 or TEKTRONIX 492BP if Phase Noise check is not performed.

Table 2-1. Equipment Required for Performance Checks (Continued)

Equipment for Optional Flatness Checks		
Item	**Characteristic**	**Recommended**
25. Second GPIB Interface Board	Compatible with National PC2A. NOTE: This is in addition to the GPIB Interface board required with Item 1 of the main equipment list. For the flatness check, both boards must be PC2A compatible.	National PC2A GPIB Interface board, or Tektronix S3FG120 GPIB Interface.
26. GPIB Interface Cables (3 each)	3 GPIB cables are required in addition to the 1 cable in the main Equipment List.	Tektronix Part No. 012-0630-01
27. Connectors, Pads, and Splitters	Power Divider (dc to 40 GHz) 40 GHz flexible 50 Ω cable with K connectors 3 dB attenuator K-male-to-male connector N-female-to-SMA-male connector 2.4-mm-female-to-K-male connector K male-to-female connector (2 each) (optional) K-male-to-F-female connector (optional)	Wiltron K240C Wiltron 41KB-3 Hewlett-Packard 1250-1562 HP 11904D

Part I. Flatness Check

The 2782 spectrum analyzer incorporates an internal flatness circuitry that automatically compensates for deviations in the instrument's signal response over its entire frequency range. This automatic compensation is responsible for the instrument's extremely flat frequency response (that is, the instrument's ability to accurately measure a constant amplitude signal over the frequency range of 100 Hz to 33 GHz).

This section of the 2782 performance verification procedure describes how to measure the frequency response (or flatness) of the instrument. The flatness verification test is made with a Tektronix-designed flatness calibration and verification software package, which runs on an MS-DOS compatible personal computer.

Overview of the Flatness Test Procedure

To verify the flatness performance of a 2782, you must perform the following six steps:

1. Install the flatness software on the personal computer.
2. Set up the test equipment.
3. Run the equipment configuration program (CONFIG.EXE).

4. Run the flatness utility program (UTIL.EXE) to level the test equipment.

5. Run the QC portion of the flatness calibration and verification program (CATS.EXE) to measure the flatness of the 2782.

6. Plot the results of the flatness test with the plot program (PLOT.EXE).

The following sections describe these steps in detail.

Installing the Flatness Software on the Personal Computer

The flatness software is contained on three 5 1/4-inch floppy disks, which come with the 2782 as standard equipment. These disks contain the following files:

Disk 1:

README.DOC	Software documentation.
INSTALL.BAT	Installation batch file.
CATS.EXE	Flatness verification and preselector tracking program.

Disk 2:	
UTIL.EXE	System hardware characterization program.
TOPICS.IDX	Index file for CATS on-line help system.
*.HLP	Text files for CATS on-line help system.
Disk 3:	
CONFIG.EXE	System configuration file build utility.
DOWNLOAD.EXE	Loads flatness corrections into the 2782.
PLOT.EXE	Displays flatness results graphically on screen.
782.EIS and 2782.NUM	These two files contain the performance requirement information (specifications) that CATS uses.
HFCONFIG, SW_CONF, and FLATNESS.SEQ	These three files, plus others (created by CONFIG.EXE) describe to CATS.EXE the test equipment and all interconnections that are required.

Use the following procedure to install the flatness software on the personal computer (item 1 of the equipment list):

1. Install disk 1 in drive A of the personal computer.
2. Set the default drive for A (enter a:).
3. Enter the following command to install the flatness software on your hard disk:

```
A> install <ENTER>
```

INSTALL prompts you to switch disks.

NOTE

INSTALL.BAT is a batch file that creates a directory on your hard disk (called TEKCATS) and several subdirectories. It then copies the flatness software into these directories.

Setting Up the Personal Computer and Test Equipment

The test equipment required for the flatness verification tests is given in items 1, and 24 through 28 of the equipment list. Use the following procedure to set up this equipment.

1. Set the base addresses for the two PC2A GPIB boards and install them in the personal computer. (Instructions for setting the base addresses for these boards and installing them in the PC are contained in the instruction manual that comes with the board.)

Each GPIB board must be given a base address, that the software uses to identify the board. The PC2A boards should come with their base address set to 02E1 (hex). Leave one board set at that address, and set the address of the other board to 22E1 (hex). Leave the DMA channel* and interrupt line settings at their defaults. It is helpful to label the GPIB boards with numbers: label the board with base address 02E1 as #0, and label the other board (base address 22E1) #1.

If the personal computer you are using contains other boards that use DMA, such as a network adapter, disable DMA on both GPIB boards. Do this by setting the DMA channel selection jumpers on both boards to NOT USED.

2. Connect 2782, signal generators, and power meter to the computer through GPIB cables, as shown in Figure 2-1.

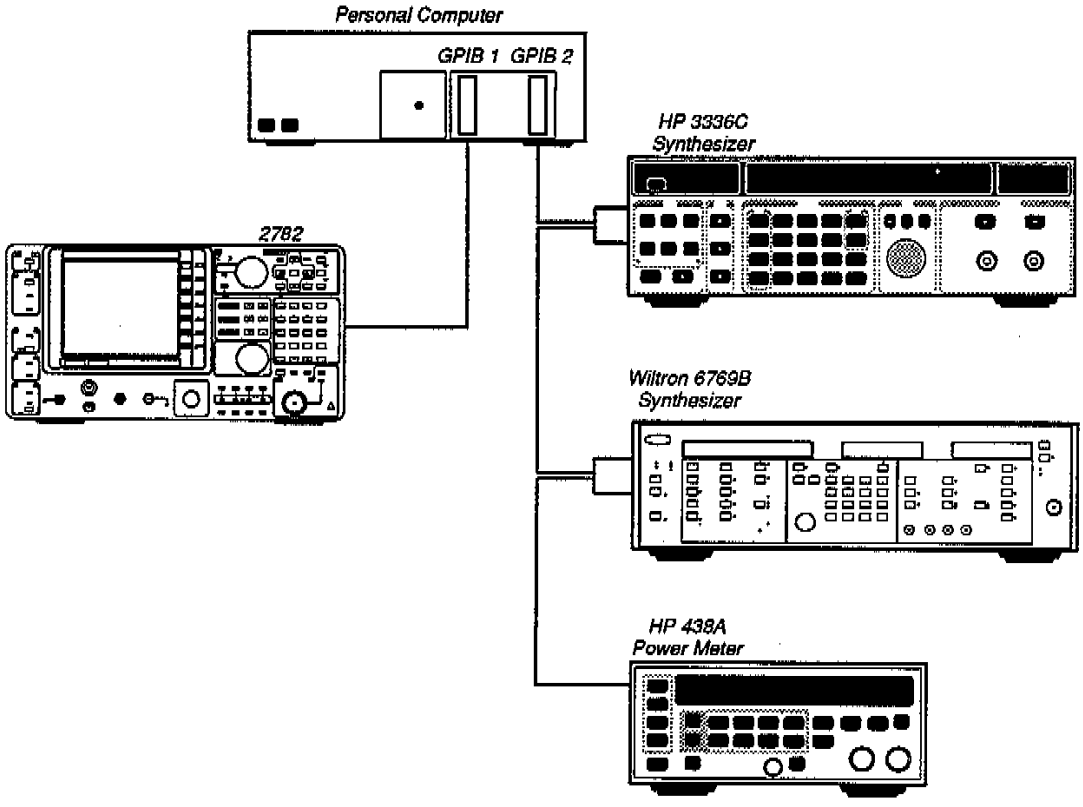


Figure 2-1. GPIB Connections for Flatness Checks.

Connect a GPIB cable from GPIB Port 1 of the 2782 to PC2A board #1. Connect GPIB cables from the generators and power meter to PC2A board #0. If this convention is not followed, the flatness test software will not operate correctly.

3. Power up the 2782 and allow it to warm up for one hour. Power up the signal generators and power meter at the same time.

4. Connect the text-fixture components as shown in Figure 2-2 and connect them to the 2782.

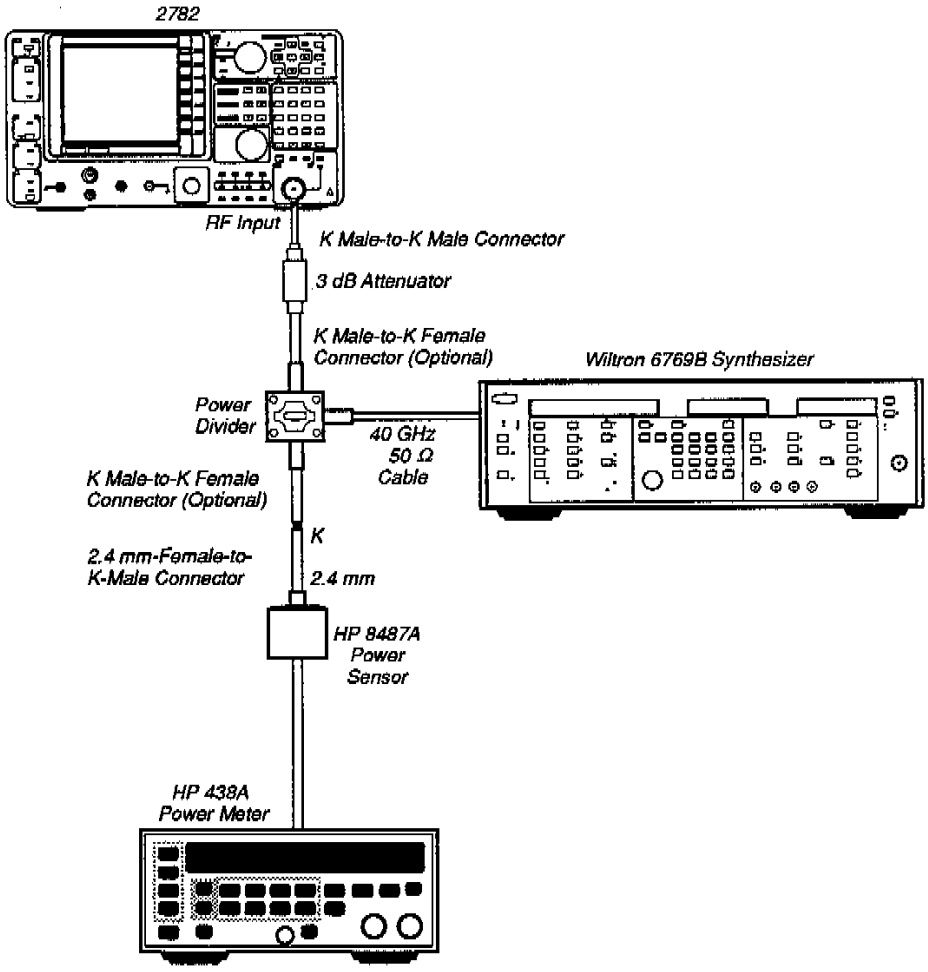


Figure 2-2. Test Fixture Setup for High Frequency Flatness Tests.

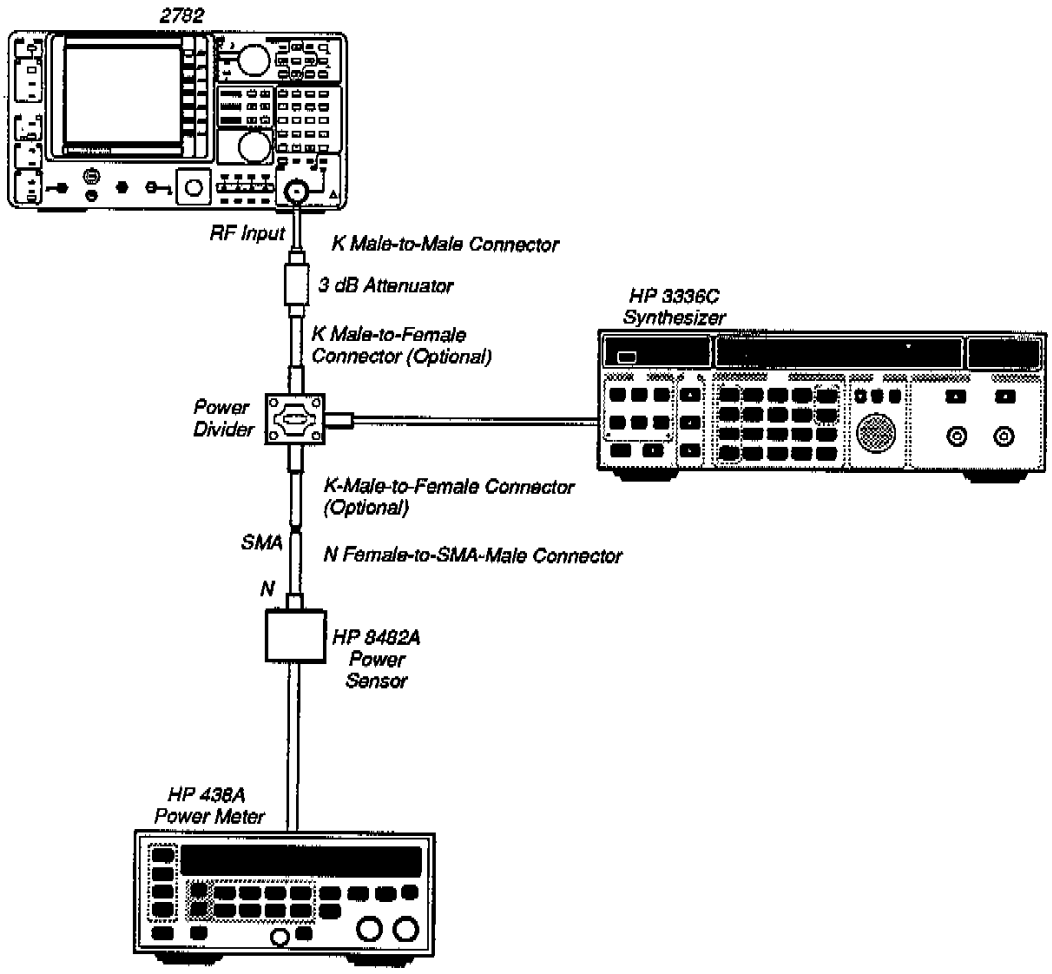


Figure 2-3. Test Fixture Setup for Low Frequency Flatness Tests.

5. Set the GPIB address of the 2782 to 1 as follows. Press the 2782 EXT INTFC CONFIG, and press the Set Port1 Address menu button. Then, enter 1 from the keypad, and press ENTER. A message is then displayed on the crt indicating that the GPIB port address has been reset.

6. Set the clock speed of the personal computer to 6 MHz.

   The 2782 is sensitive to the rate at which it receives data through its GPIB interfaces. When it is receiving a long or repetitive series of commands over the GPIB bus, it may simply quit responding to commands or queries. When this happens, the only way to restore remote control is to cycle the 2782 POWER switch off and on. This problem occurs only when the 2782 is connected to a controller (personal computer) with a very high GPIB data transfer rate (for example, 16 MHz).

   The easiest way to prevent this lock up of the 2782 is to slow the clock rate of the PC down to approximately 6 MHz. This is commonly done by

setting a switch on the personal-computer mother board or by issuing an MS-DOS command.

On the TEKTRONIX PEP 30x controllers, use the SYSENV command that is supplied with the PC to slow the clock rate. The syntax for this command is `SYSENV .6m`. If the symptom persists, slow the clock rate down again.

NOTE

Slowing the clock rate of the personal computer will not significantly increase the time required to complete the test. This is because the personal computer spends most its time waiting for the 2782 and the test equipment to execute commands.

Running the Equipment Configuration Program (CONFIG.EXE)

The CONFIG.EXE program generates a table that describes the test equipment being used and their respective GPIB addresses. It also creates a data file for each power sensor, containing the calibration factors to be used at each frequency. The calibration factor information comes from the table printed on each sensor.

Enter the following on the personal computer to run CONFIG.EXE:

```
CONFIG <ENTER>
```

NOTE

You must be in the TEKCATS directory to run any of the flatness verification software.

The program prompts you to enter the GPIB address of each generator and of the power meter. You are also asked for the date that the instrument is due for recalibration and for an identification number that will be used to track the status of the instrument. The ID number can be any unique number (letters are also allowed), such as a calibration number assigned by your calibration laboratory, the last part of the instrument's serial number, or an arbitrary number. Be sure to label the instrument with this number, so that the same number is used every time it is tested.

CONFIG.EXE asks for the same information (except for the GPIB address) for each power sensor, plus the calibration factor table.

If any piece of equipment in the system is past its calibration due date, the UTIL.EXE and CATS.EXE programs will not run. The equipment must then be recalibrated and the CONFIG program rerun, to update the calibration due date. This feature is included meet NBS traceability requirements.

Running the Flatness Utility Program (UTIL.EXE)

The flatness calibration and verification system uses a power splitter and a power meter to compensate for flatness variations in the generators and for losses in the cabling. The CATS.EXE program performs this compensation by measuring the signal amplitude at the RF Input, comparing it to a reference

amplitude, and then using the difference in the two amplitudes to correct the flatness measurement.

For this testing method to work properly, the UTIL.EXE program must be run to characterize the test fixture setups shown in Figure 2-2 and 2-3.

Enter the following on the personal computer to run UTIL.EXE:

```
UTIL <ENTER>
```

The UTIL.EXE program uses the same operator interface and menu structure as the CATS.EXE program. Refer to the section titled "Performing the Flatness Tests (CATS.EXE)" for information on the operator interface.

The test fixture characterization data that UTIL.EXE collects is stored in a file that CATS.EXE uses.

The power splitter characterization takes about an hour and a half to complete. For traceability reasons, UTIL.EXE must be run whenever the splitter or 3 dB pad are replaced (or even taken apart and put back together). Because of this, it is recommended that you purchase this pair of components specifically for this application and dedicate them to this application.

Additional information on the UTIL.EXE program and the test setup characterization is given in the READ.ME file.

Performing the Flatness Tests (CATS.EXE)

The CATS.EXE program is used both to calibrate the flatness of the 2782 and to verify flatness. Only the flatness verification portion of this program is used here.

NOTE

The CATS.EXE program performs a preselector tracking measurement that creates a preselector-tracking flatness correction table. This procedure is only used when calibrating the 2782 for flatness, it is not used for performance verification. Also, the DOWNLOAD.EXE program is not used for performance verification.

Enter the following on the personal computer to run CATS.EXE:

```
CATS <ENTER>
```

When the CATS program has been loaded, a selection screen is displayed.

NOTE

As describe earlier in this section, the user interfaces for CATS.EXE and UTIL.EXE are similar, so much of the following information also applies to UTIL.EXE.

When the program has been loaded, you are prompted to enter your name. This allows the data files that CATS.EXE generates to be traced to the operator at a later date, if desired.

Next, the current date and time are displayed, and you are prompted to verify that they are correct. If they are not, exit the program (F1,4, <ENTER>), reset the date and/or time as needed, and restart the program.

The CATS program is a menu driven program. Once you have accepted the date and time (pressed <ENTER>), a menu is displayed that allows you to select the flatness verification tests (QC) or the flatness calibration procedure (CAL). Select 1 and press <ENTER>.

You are then prompted to connect the DUT (Device Under Test -- the 2782 in this case) to the test system and power it up. You should hav e already carried out this step. If not, perform the steps listed in the previous section titled "Setting Up the Personal Computer and Test Equipment."If the 2782 is already powered up, it is a good idea to re-cycle the power at this time.

Next, you are prompted to enter the 2782's serial number (twice).

The next menu to be displayed allows you to choose how tests are to be performed. This menu provides three selections:

1) RUN FULL SEQUENCE	Every test in the testing sequence is run, in order.
2) RUN PARTIAL SEQUENCE	Selects a second menu that allows you to select a starting point in the testing sequence. The program then runs every test from that point to the end of the sequence.
3) SELECT TEST(S)	Causes a list of test to be displayed. You can then select specific tests to be run. Multiple tests can be selected by entering a series of numbers separated by commas.

Select 1 and press <ENTER>.

A menu is then displayed that allows you to select the attenuators to be tested. Menu item 15 (0-70 dB) is highlighted, indicating all attenuator settings. Press <ENTER> to select this entry.

The next menu to be displayed allows you to select the 2782 frequency bands to be tested. Here, item 6 (Bands 1-5) is highlighted, indicating all bands. Press <ENTER> to select this entry.

From this point on, CATS.EXE handles the flatness verification automatically. All you have to do is change equipment periodically (as shown in Figure 2-2 and 2-3). CATS.EXE prompts you for these changes.

Pressing the F1 key on the computer allows you to interrupt a test at any time or back up a menu level. When this key is pressed a menu of choices is displayed.

The CATS program also provides on-line help, that can be accessed by pressing the F2 key on the computer.

NOTE

Do not press the help or interrupt keys in the middle of a test unless you really need to. Once a test is interrupted, it cannot be resumed at the point of interruption; instead, it must be restarted.

Additional information about the CATS.EXE program can be found in README.DOC file

Plotting the Flatness Test Results (PLOT.EXE).

The utility program PLOT.EXE reads the corrected flatness error files and plots the data on the personal computer monitor. Figure 2-PLOTS shows an example of one of these plots.

NOTE

This program requires an EGA monitor.

To run this program enter the following from the personal compute:

```
PLOT <serial-number> <ENTER>
```

Enter the serial number of the instrument you want flatness data from. Use the same serial number you entered when you ran the flatness tests.

This program then draws a series of graphs on the monitor, each one representing the flatness error data for one RF attenuation setting. The horizontal axis of the graphs represents frequency, with the lowest band on the left and the highest band on the right. (The 0 to 6.5-GHz band is made up of the first two sections on the left side of the graph.) The vertical axis shows the flatness response in dB's. The vertical scale of the graphs is set automatically so that all of the data will fit in the window.

After each graph is drawn, PLOT.EXE pauses for you to examine the graph. Press <ENTER> to continue to the next graph. If your version of DOS will support EGA-mode screen dumps, you can use the Print Screen key to make a hard copy of any graphs you want. Just press <PRT SCR> before hitting <ENTER>.

On version 1.1 of the flatness test software, you can enter the switch /H in the command line to get a hard copy of the plots.

NOTE

The data in these graphs is used in steps 4-6 and steps7 of Part II of this performance verification procedure. It is suggested that you look ahead to these steps to see how this data is used and make the necessary measurements from the plots now, or make hard copies of the plots for later use.

The switch /U cause the uncorrected flatness data for the instrument to be plotted.

Refer to the READ.ME file for information on how to use this program.

Part II. Performance Checks (Except Flatness)

This portion of the 2782 performance check checks the non-flatness related performance and operating specifications of the 2782. This check is made with a performance-check spread sheet that runs under Lotus 123 and Lotus Measure programs, on a personal computer.

Using the Performance-Verification Software

The 2782 performance-verification software is contained on a 5.25-inch floppy disk, titled "Distribution Disk." To run this software, a copy of Lotus 1-2-3 and Lotus Measure are required, as well as two blank, formatted floppy disks. The following sections describe how to install the performance-verification software on your system, how to load the software, and how to operate the performance-verification program.

Installing the Software

1. Make a back-up copy of the Performance Verification Distribution disk and store the back-up copy in a secure place.

2. If you haven't already done so, install Lotus 1-2-3 and Lotus Measure on the personal computer. (Make sure the default directory for Lotus 1-2-3 is A:\, and that undo is disabled. Also, make sure that the printer and graphics display drivers and options are properly selected in the 123 install program.)

3. Install the software using two floppy disk drives, or using one floppy disk drive and one hard disk drive, as follows:

   Installing using two floppy drives. If you are working on a personal computer with two floppy disk drives (and no hard disk drive), perform the following procedure:

   a. Install the Performance Verification Distribution disk in drive B and the 1-2-3 working disk in drive A.

   b. Set the default drive for B (enter `b:`).

   c. Enter the following command to copy the file 2782qc.flp from the distribution disk to your 1-2-3 working disk, under the file name 2782qc.bat.

      ```
      B> copy 2782qc.flp a:2782qc.bat <ENTER>
      ```

   d. Enter the following command to copy the file nat488.set from the 1-2-3 working disk to the distribution disk.

      ```
      B> copy a:nat488.set b: <ENTER>
      ```

      The file nat488.set was created when you installed Lotus Measure.

e. Remove the 1-2-3 working disk from drive A and install a blank, formatted floppy disk in drive A.

f. Enter the following commands to create a data disk on the blank disk in drive A:

```
B> copy clear.wk1 a: <ENTER>
B> copy 2782.bcf a: <ENTER>
```

These commands copy the files clear.wk1 and 2782.bcf from the distribution disk to the new data disk. MS-DOS prompts you to change disks.

If the National PC2 GPIB card is being used instead of a PC2A, copy the file `2782.pc2.bcf` from the distribution disk to the file `2782.bcf` on the new data disk, using the following command:

```
B> copy 2782.pc2.bcf a:2782.bcf <ENTER>
```

This replaces the PC2A configuration file with the PC2 version.

Installing on a hard drive. If you are working on a personal computer that has a hard-disk drive, perform the following procedure:

a. Install the Performance Verification Distribution disk in drive A.

b. Set the default drive for A (enter a:).

c. Enter the following command to copy the file 2782qc.hrd from the distribution disk to the root directory on the hard disk, under the file name 2782qc.bat.

```
A> copy 2782qc.hrd c:\2782qc.bat
```

d. Enter the following command to copy the file nat488.set from the 1-2-3 working directory on the hard disk to the distribution disk.

```
A> copy c:\123-working-directory\nat488.set a:
```

The file nat488.set was created when you installed Lotus Measure.

e. Install a blank, formatted floppy disk in drive B.

f. Enter the following commands to create a data disk on the blank disk in drive B:

```
A> copy clear.wk1 b:
A> copy 2782.bcf b:
```

These commands copy the files clear.wk1 and 2782.bcf from the distribution disk to the new data disk. MS-DOS prompts you to change disks.

If the National PC2 GPIB card is being used instead of the PC2A, copy the file 2782.pc2.bcf to the file 2782.bcf, using the following command:

```
A> copy 2782.pc2.bcf b:2782.bcf <ENTER>
```

This replaces the PC2A configuration file with the PC2 version.

Loading the Software

Use the following procedure to load and run the 2782 Performance Verification Software on a two-floppy-disk system:

1. Place the 1-2-3 working disk in drive A and the Performance Verification Distribution disk in drive B.
2. Set the default drive for B (enter `b:`).
3. Enter the following command:

   ```
   B> 2782qc <ENTER>
   ```

4. When the spread sheet is loaded, remove the distribution disk from drive B and replace it with the data disk.

Use the following procedure to load and run the 2782 Performance Verification Software on a hard-disk system:

1. Place the Performance Verification Distribution disk in drive A.
2. Set the default drive for A (enter a:).
3. Enter the following command:

   ```
   A> 2782qc <ENTER>
   ```

4. When the spread sheet has been loaded, remove the distribution disk from drive A and replace it with the data disk.

Operating the Software

Once you have loaded Lotus 1-2-3 and Lotus Measure, you must open a new data file (if you are starting with a fresh instrument) or load an existing data file (if you are continuing with a previous performance check).

Opening a New Data File. Use the following procedure to open a new data file:

1. Select the OtherMenu R(etrieve) command. A prompt asks you if you remembered to save the measurement results. This is a safeguard against retrieving new data before the data currently loaded in the spread sheet is saved. If you are just starting out, enter y. (Enter n to save the current data.)

2. Select the clear.wk1 file with the cursor keys, and press the ENTER key.

3. Select the OtherMenu S(ave) command and enter a new file name for the data to be saved on the new instrument you are working on and hit ENTER. It is suggested that you use the serial number of the instrument as a file name (for example, B010075).

Opening an Existing Data File. Use the following procedure to open an existing data file for an instrument that has already been checked or that your are continuing to check:

1. Select the OtherMenu R(etrieve) command. A prompt asks you if you remembered to save the measurement results. Enter y.

2. Using the cursor keys, select the data file for the instrument your are currently working (the file should have a .wk1 extension) and press the ENTER key. (Press the ENTER key again if the menu does not reappear.)

Making a Measurement. Use the following procedure to make measurements, save measurement results, print results, and get out of trouble.

1. Select the S(tep) command to select a measurement step. You are then prompted for a step number. Enter the step number and hit the ENTER key. You can also select the next step or previous step with the N(ext) and P(revious) commands, respectively.

   When 1-2-3 goes to the selected step, the Measure program sets the 2782 Frequency, Span, Ref Level, Res BW, Video BW, Sweep, Mixer Overdrive, and dB/div controls according to setting included in the performance-verification spread sheet.

2. Set up the external equipment as described in this performance-check procedure for the specific step and as shown in the prompt line at the top of the spread sheet.

3. Set the 2782 markers for the measurement as instructed. You may need to turn on delta markers and bandwidth markers, or turn them off, as necessary. Markers are not used for some measurements.

4. Select the M(easure) command to read the appropriate marker value and place it in the spread sheet. If this is not a marker measurement, you are prompted to enter the measurement value. This value will come from external equipment or it may be a 1 or a 0 if the test was successful.

NOTE

The M(easure) command can be executed repeatedly until the measurement number recorded is correct. Also, errors and pass/fail indications are not re-computed until the C(alculate) command is selected explicitly. These values can be recomputed after each step, if desired, or less often to save time.

5. Go to the next step and repeat the general measurement procedure described in steps 2 through 4.

6. When you have completed measurements on a particular instrument, select the OtherMenu S(ave) command to save the data. You are prompted for a file name. If you are working with an existing data file, select the file name with the cursor keys and hit ENTER. If you have not established a data file yet, enter a new file name and hit ENTER. It is suggested that you use the instrument serial number for the file name. (Press the ENTER key again if the menu does not reappear.)

7. To print the measurement results, select the OtherMenu P(rint) command. 1-2-3 must have been set up for your printer and with compressed printing before you can print measurement results.

8. To quit a measurement session, select the Q(uit) command. You are asked if you remembered to save your current data. If you enter n, you are prompted to save it. If you enter y, the Measure program terminates. You can then use the 1-2-3 Q(uit) command (/ Q) to go back to DOS.

Getting Out of Trouble. If the menu does not return after an operation, try pressing the ENTER key. If this does not work and you find yourself hung up, press the following sequence of keys: Ctrl-Break, Esc, Alt-M. This key sequence restarts the measurement macro program from the top. Your data will not be lost.

NOTE

Occasionally, the GPIB message buffer in the 2782 overflows, causing the 2782 to hang up and not respond to messages from the computer. This can happen if you enter a series of spread-sheet commands in rapid succession. When this situation occurs, it is best to wait a minute or so to see if the 2782 is able to clear the buffer. If it does not and entering Ctrl-Break, Esc, Alt-M does not restore the spread-sheet menu, recycle the POWER button on the 2782. When the 2782 initializes itself on power up, it clears its GPIB buffer. The spread-sheet menu should then return and the spread sheet should respond to commands. You should not lose any data from this operation, although you may have to repeat a step.

Preparation for Performance Checks (Except Flatness)

1. Power up the 2782 and allow it to warm up for one hour or more.

2. Connect the GPIB cable from the GPIB-interface board on the personal computer to the GPIB 1 connector on the 2782.

3. Power up the personal computer.

4. Load the performance-verification spread sheet as described above in the section titled "Using the 2782 Performance Check Software."

5. Press the EXT INTFC CONFIG button, and press the Language Menu button. Then, press the service menu button to select the SERVICE language.

NOTE

If you do not perform step 5 above, whenever the performance verification spread sheet tries to communicate with the 2782, the 2782 will display a message on the crt to indicate that it does not recognize commands from the performance verification software.

Steps 4-6. Flatness and Frequency Response Recording

These steps enter Flatness check data for use in the performance-verification spread sheet.

a. Select step 4 from the performance-verification spread sheet.

b. From the flatness check data collected in Part I of this procedure, determine the maximum peak-to-peak corrected flatness (in dB's) for all the attenuator settings in the 0 to 6.5 GHz frequency range (see the example in Figure 2-4). Then enter one half of this value in the performance-verification spread sheet.

NOTE

Use the PLOT.EXE program either to make a hard copy of the plots of the flatness data or to examine the flatness data on the computer monitor. The PLOT.EXE program is described earlier in this section in the section titled "Plotting the Flatness Test Results (PLOT.EXE)."

The data in these plots is relative to the gain measured at 100 MHz. Therefore, the 0 dB line represents a gain equal to the gain at 100 MHz.

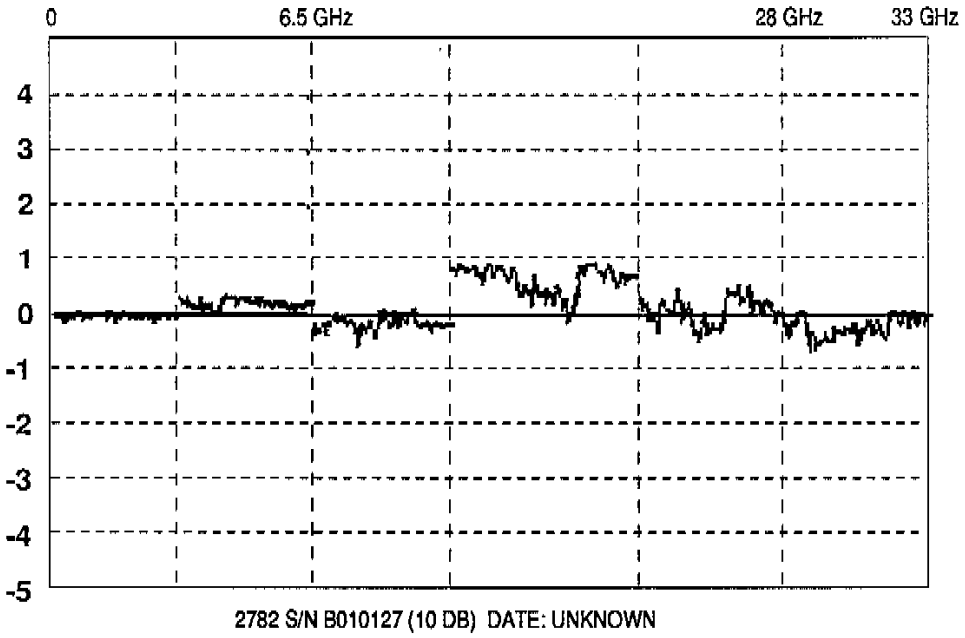


Figure 2-4. Example Plot for Flatness and RF Gain Uncertainty Measurements

c. Select step 5 the performance-verification spread sheet, and enter one half of the maximum peak-to-peak corrected flatness for the 6.5 GHz to 28 GHz frequency range in the spread sheet.

d. Select step 6 from the performance-verification spread sheet, and enter one half of the maximum peak-to-peak corrected flatness for the 28 GHz to 33 GHz frequency range in the spread sheet.

NOTE

Save the measurement data frequently, using the OtherMenu S(ave) command, to prevent loss of measurement data due to computer or power problems.

Step 7. RF Gain Uncertainty Check

This step uses the average corrected flatness data for each band to determine the error due to gain change. Gain is changed to compensate for insertion loss error in each band. (Gain error is covered by the IF Gain error check later in this procedure.)

a. Select step 7 check spread sheet.

b. Using the corrected flatness data plots obtained from the Part I flatness checks (see the example in Figure 2-4), determine the average gain for each band at 10 dB attenuation, relative to the 0 dB line.

c. Enter the value (in dB's) of the largest gain measured in step b in the performance-verification spread sheet.

Steps 8-10. Third Order Intercept Check

This checks the analyzers third order response to two input signals. We overdrive the front end in order to get distortion products large enough to show on the screen. The resulting measurements are entered into the spread sheet, where the intercept point is calculated.

Perform this check at 20 MHz and 6 GHz to check both ends of the low band path; and at 8 GHz, to check the high band path.

a. Select step 8 from the performance-verification spread sheet.

b. Connect the two synthesizer/level generators through the Mini-Circuits 2FSC-2-6 combiner to the 2782 RF INPUT connector (as shown in Figure 2-5). Do not use the 6 dB pads with the Mini-Circuits Combiner.

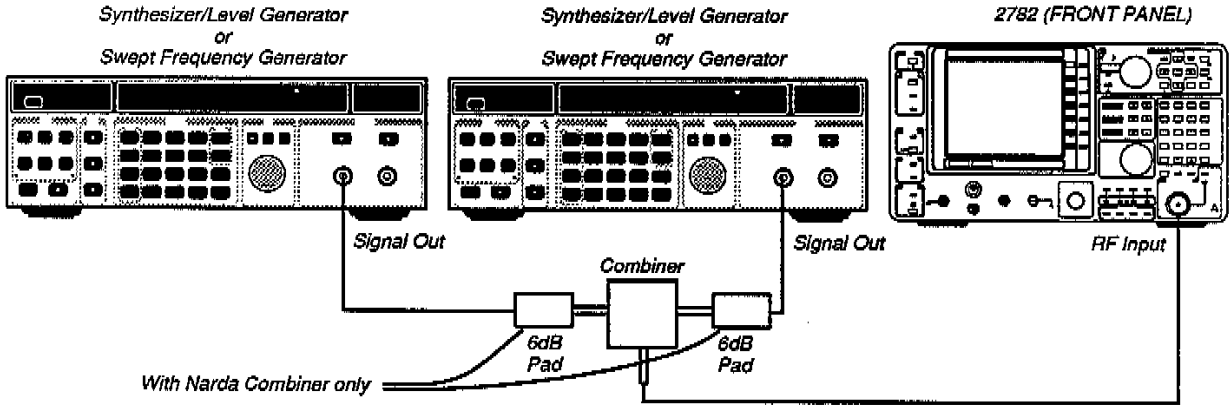


Figure 2-5. Test equipment setup for the Third Order and Second Order Intercept Checks.

c. Press the 2782 Δ MKR button to activate the delta markers.

d. Set one synthesizer for a frequency of 20 MHz and the other for 20.05 MHz.

e. Using the delta markers, position the red marker on the peak of the 20.05 MHz signal, and the yellow marker on the distortion product at 20.1 MHz (as shown in Figure 2-6).

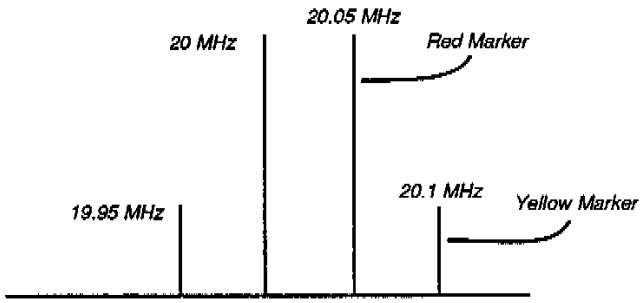


Figure 2-6. Third Order Intercept Distortion.

f. Press the M key on the computer to enter the intercept measurement in the spread sheet.

g. Select step 9 from the performance-verification spread sheet.

h. Disconnect the two synthesizer/level generators from the 2782. Connect a 6 dB pad to each input arm of the Narda 2-8 GHz combiner. Connect the two swept-frequency synthesizers the 6 dB pads, and connect the output of the combiner to the 2782 RF INPUT connector.

i. Set one synthesizer for a frequency of 6 GHz and the other for 6.00005 GHz.

j. Position the red marker on the peak of the 6.000050 GHz signal and the yellow marker on the distortion product at 6.000100 GHz, and press the M key on the computer.

k. Select step 10 from the performance-verification spread sheet.

l. Set one synthesizer for a frequency of 8 GHz and the other for 8.00005 GHz.

m. Position the red marker on the peak of the 8.000050 GHz signal and the yellow maker on the distortion product at 8.000100 GHz, and press the M key on the computer.

n. When the measurement has been entered in step 16, press the C key on the computer to check that the third-order intercept checks are within specification.

o. Disconnect the synthesizers from the 2782.

Steps 11-17. Second Order Intercept Check

This check is similar to the Third Order Intercept check, except that the analyzer second order responses are measured at the sum and difference frequencies. The input needs to be overdriven to see the responses on the screen. The check is performed at 1 GHz, 100 MHz, and 3 GHz.

a. Select step 11 from the performance-verification spread sheet.

b. Connect the two swept-frequency synthesizers through the Mini-Circuit 2FSC-2-5 combiner to the 2782 RF INPUT connector (as shown in Figure 2-5). Do not use the 6 dB pads with the Mini-Circuits Combiner.

c. Set one synthesizer for a frequency of 1 GHz and the other for 10 MHz.

d. Press the MKR button to activate the single marker, then place the single marker on the peak of the 1 GHz signal and press the M key on the computer.

e. Select step 12 from the performance-verification spread sheet.

f. Using a single marker, measure the distortion product at 1.010 GHz, and press the M key on the computer.

g. Select step 13 from the performance-verification spread sheet.

h. Set one synthesizer for a frequency of 100 MHz and the other for 10 MHz.

i. Using a single marker, measure the amplitude of the 100 MHz signal, and press the M key on the computer.

j. Select step 14 from the performance-verification spread sheet.

k. Using a single marker, measure the distortion product at 110 MHz, and press the M key on the computer.

l. Select step 15 from the performance-verification spread sheet.

m. Disconnect the two synthesizer/level generators from the 2782. Connect a 6 dB pad to each input arm of the Narda 2-8 GHz combiner. Connect the two swept-frequency synthesizers the 6 dB pads, and connect the output of the combiner to the 2782 RF INPUT connector.

n. Set one synthesizer for a frequency of 3 GHz and the other for 3.010 GHz.

o. Using a single marker, measure the amplitude of the 3.010 GHz signal,and press the M key on the computer.

p. Select step 16 from the performance-verification spread sheet.

q. Using a single marker, measure the distortion product at 6.010 GHz, and press the M key on the computer.

r. Select step 17 from the performance-verification spread sheet.

s. Using a single marker, measure the distortion product at 10 MHz, and press the M key on the computer.

t. When the measurement has been entered in step 17, press the C key on the computer to check that the second-order intercept checks are within specification.

u. Disconnect the synthesizers from the 2782.

Steps 18-24. Second Harmonic Distortion Check

These steps check analyzer distortion at the second harmonic of the input signal. The input signal second harmonic is reduced using low-pass filters to be sure that what is measured on the screen is the distortion in the analyzer. The front end doesn't need to be overdriven in this check because the allowable distortion is high enough to see on the screen.

The test is performed at fundamental frequencies of 10 MHz, 49 MHz, 500 MHz, 1 GHz, and 3 GHz. The 49 MHz frequency is chosen to avoid a potential 50 MHz spurious response that might alter the measurement.

This test is done only in the low band, because fundamental signals in the high band are so widely separated from their second harmonics that the preselector strips the harmonic off.

a. Select step 18 from the performance-verification spread sheet.

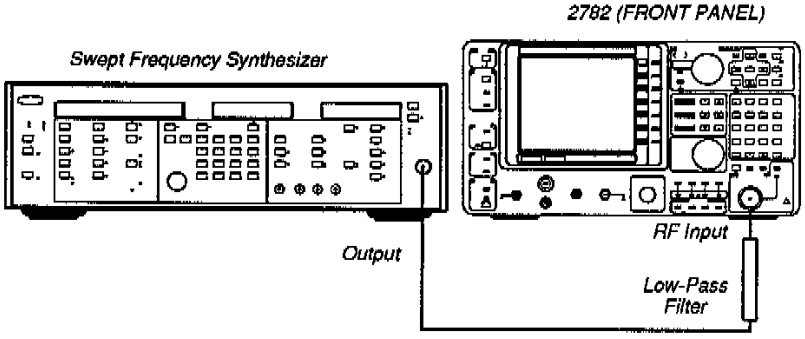


Figure 2-7. Test Equipment Setup for the Second Harmonic Distortion Check.

b. Connect a 50 Ω cable from one of the swept-frequency synthesizer through the K&L 4L51-15-B/B low-pass filter to the 2782 RF INPUT connector (as shown in Figure 2-7).

c. Set the synthesizer for a frequency of 10 MHz, and adjust the signal amplitude to full screen on the 2782.

d. Using a single marker, measure the distortion product at 20 MHz, and press the M key on the computer.

e. Select step 19 from the performance-verification spread sheet.

f. Replace the low-pass filter currently connected to the 2782 RF INPUT connector with the K&L 5L51-551-B/B low-pass filter.

g. Set the synthesizer for a frequency of 49 MHz, and adjust the signal amplitude to full screen on the 2782.

h. Using a single marker, measure the peak at 49 MHz, and press the M key on the computer.

i. Select step 20 from the performance-verification spread sheet.

j. Using a single marker, measure the distortion product at 98 MHz, and press the M key on the computer.

k. Select step 21 from the performance-verification spread sheet.

l. Replace the low-pass filter currently connected to the 2782 RF INPUT connector with the K&L 5L120-850-O/O low-pass filter.

m. Set the synthesizer for a frequency of 500 MHz, and adjust the signal amplitude to full screen on the 2782.

n. Using a single marker, measure the peak of the 500 MHz signal, and press the M key on the computer.

o. Select step 22 from the performance-verification spread sheet.

p. Using a single marker, measure the 1 GHz distortion component, and press the M key on the computer.

q. Select step 23 from the performance-verification spread sheet.

r. Replace the low-pass filter currently connected to the 2782 RF INPUT connector with the K&L 3L120-3500-O/O low-pass filter.

s. Set the synthesizer for a frequency of 3 GHz, and adjust the signal amplitude to full screen on the 2782.

t. Using a single marker, measure the peak of the 3 GHz signal, and press the M key on the computer.

u. Select step 24 from the performance-verification spread sheet.

v. Using a single marker, measure the 6 GHz distortion product, and press the M key on the computer.

w. When the measurement has been entered in step 24, press the C key on the computer to check that the second harmonic distortion checks are within specification.

x. Disconnect the synthesizer from the 2782.

Steps 25-26. Out of Band Response Checks

This step measures how well the analyzer rejects out-of-band signals. Two measurements are made, one for the low band path and one for the high band path. The low band test measures the response at 5.95 GHz for a signal input at the image frequency of 26 GHz. The high band test checks the preselector rejection by measuring the response at 6.95 GHz for a signal input at 14 GHz.

a. Select step 25 from the performance-verification spread sheet.

b. Connect the swept-frequency synthesizer through a 50 Ω cable to the 2782 (as shown in Figure 2-8).

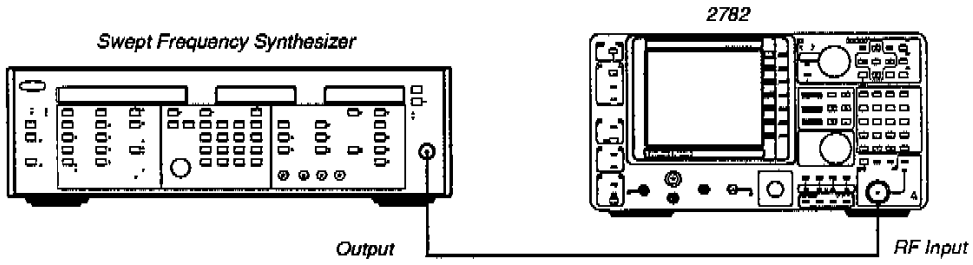


Figure 2-8. Test Equipment Setup for Out of Band Response and 1 dB Gain Compression Checks

c. Select a synthesizer signal-output frequency of 26 GHz and an amplitude of 0 dBm.

d. Using a single marker, measure the out of band response at 5.95 GHz, and press the M key on the computer.

e. Set the synthesizer signal-output frequency to 14 GHz and the amplitude to 0 dBm.

f. Select step 26 from the performance-verification spread sheet.

g. Using a single marker, measure the out of band response at 6.95 GHz, and press the M key on the computer.

h. When the measurement has been entered in step 26, press the C key on the computer to check that the out-of-band-response checks are within specification.

Steps 27-29. 1 dB Gain Compression Checks

This check sets the analyzer to the 30 dB overdrive mode for the lowest IF gain. This allows displaying the low band specification of 0 dBm at the top of the screen. The error should not accumulate to more than 1 dB at the 0 dBm level. Measure the synthesizer power level with a power meter to avoid including the error of the analyzer.

a. The swept-frequency synthesizer should still be connected to the 2782. If not, connect the synthesizer to the 2782 RF INPUT connector through a 50 Ω cable (as shown in Figure 2-8).

b. Select step 27 from the performance-verification spread sheet.

c. Press the 2782 ATTEN button, and press the RF Atten ON/off button to select OFF. Then, press the REF LEVEL button, and enter 5 dBm from the keypad.

d. Set the synthesizer signal-output frequency for 1 GHz, and adjust the signal amplitude so that the waveform peak is near the bottom of the 2782 crt screen (0 dB).

e. While observing the waveform on the 2782 crt screen, increase the synthesizer output amplitude 1 dB at a time and note the dB change on screen using a marker. Continue to increase the generator in 1 dB steps until the signal peak (as measured with the marker) falls 1 dB short of the correct level, or the top of the crt screen is reached.

f. Measure the synthesizer power output with a power meter and enter this value in the performance-verification spread sheet.

g. Select step 28 from the performance-verification spread sheet

h. Set the synthesizer signal-output frequency for 21 GHz, and adjust the signal amplitude so that the waveform peak is near the bottom of the 2782 crt screen.

i. Repeat steps e and f.

j. Select step 29 from the performance-verification spread sheet, and adjust the reference level for 0 dB.

k. Set the synthesizer signal-output frequency for 28 GHz, and adjust the signal amplitude so that the waveform peak is near the bottom of the 2782 crt screen.

l. Repeat steps e and f.

m. When the measurement has been entered in step 29, press the C key on the computer to check that the 1 dB compression checks are within specification.

n. Disconnect the synthesizer from the 2782.

o. Press the 2782 ATTEN button, and press the RF Atten on/OFF button to select ON.

Steps 30-45. Center Frequency Accuracy Check

This check measures a portion of the Center Frequency accuracy. The accuracy specification is made up of two portions: the 1st LO set to frequency relative to the reference oscillator error, and the reference oscillator error itself. This check tests the first portion. The reference oscillator error is checked later in the Frequency Reference Output check.

This check eliminates the reference oscillator error by using the REF SIGNAL OUT as the signal source. The displayed frequency error is measured at several different frequencies.

a. Select step 30 from the performance-verification spread sheet.

b. Connect a 50 Ω cable from the REF SIGNAL OUT connector of the 2782 to the RF INPUT connector (as shown in Figure 2-9).

c. Press the SINGLE SWEEP button. When the sweep has reached the far right side of the crt screen, press the PEAK FIND MAX button to place a single marker on the signal peak, then press the M key on the computer to record the center frequency measurement.

d. Select steps 31 through 45 from the performance-verification spread sheet, and repeat step c for each verification step.

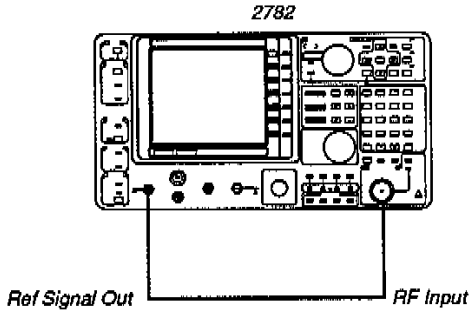


Figure 2-9. Test Setup for Center Frequency Accuracy Check

e. When the measurement has been entered in verification step 45, press the C key on the computer to check that all of the center frequency measurements are within specification.

f. Press the TRIGGER button to return the 2782 to continuous-sweep mode.

Steps 46-51. Marker/Counter Check

The Marker/Counter check measures two different things. It measures the accuracy of the marker and it checks counter sensitivity.

The markers are checked for an accurate reading at an assumed worst case condition at the right side of screen instead of at the center of the screen. This catches any errors that are more likely to show up at edges rather than center. The reference oscillator error is eliminated from the accuracy measurement by using the REF SIGNAL OUT as the signal source.

The counter sensitivity check tests two things. It checks for a 20 dB signal-to-noise (S/N) ratio, and it checks that the counter accurately counts a signal 80 dB down from the reference level. There is a potential for a noise source just off

the bottom of the screen, and this checks to see that at 80 dB down, any noise source off the bottom of the screen will not be introducing errors in the count. Another part of the 80 dB down check is to see that there is sufficient signal level coming out of the log amplifier at 80 dB down to be counted.

a. Select step 46 from the performance-verification spread sheet.

b. The 2782 calibrator signal should still be connected to the RF INPUT connector from the last check. If it is not, connect a 50 Ω cable from the REF SIGNAL OUT connector to the RF INPUT connector (as shown in Figure 2-9).

c. Press the 2782 COUNT button to turn the counter on.

d. Press 2782 PEAK FIND MAX button to place the marker on the waveform peak that appears on or near the ninth vertical graticule line (assuming the left-most vertical graticule line is line zero). Then, press the M key on the computer to record the measurement. (Wait until the sweep has reached the far right side of the crt screen and the new peak value has been displayed on the crt readout before you press the M key on the computer.)

e. Select step 47 from the performance-verification spread sheet, and repeat step d.

f. Select step 48 from the performance-verification spread sheet.

g. Press 2782 PEAK FIND MAX button to place the marker on the peak of the signal near the first graticule line. Then, press the M key on the computer.

h. Select step 49 from the performance-verification spread sheet.

i. Using the PEAK FIND <right-arrow>key, place the marker on the waveform peak on or near the ninth graticule line, and press the M key on the computer.

j. When the measurement has been entered in verification step 49, press the C key on the computer to check that the marker counter accuracy is within specification.

k. Select step 50 from the performance-verification spread sheet.

l. Disconnect the 50 Ω cable from the 2782, and connect the signal generator (item 8 in the equipment list) to the RF INPUT connector through a set of step attenuators and two 6 dB fixed attenuators (as shown in Figure 2-10). Set the signal generator for a signal output frequency of 100 MHz and an amplitude level of 12 dBm.

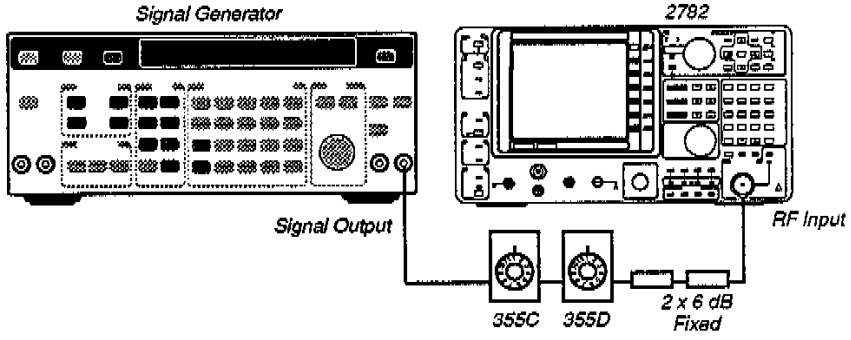


Figure 2-10. Test Equipment Setup for Steps 50 and 51 of the Marker Counter Check.

m. Set the step attenuators to reduce the signal to 20 dB above the average noise level (approximately 75 dB of attenuation), and press the PEAK FIND MAX button to place the marker on the peak of the waveform. Then, while observing the 2782 counter reading at the top of the crt screen, increase the attenuation in 1 dB steps until counting starts to vary more than ±6 Hz.

n. Press the Δ MKR button to activate the delta markers, and put the yellow marker on the peak of the signal and put the red marker on the noise floor. (The FREQUENCY/MARKERS knob and the PEAK FIND buttons only operate on the yellow marker. The Swap Ref Marker menu button allows you to swap the yellow and red markers, which in turn permits you to adjust the position of both markers.)

o. Press the M key on the computer.

p. Select step 51 from the performance-verification spread sheet.

q. Press the Delta Mkrs ON/off menu button to turn the delta markers OFF, and press the 2782 PEAK FIND MAX button.

r. Set the external attenuators for 80 dB of attenuation. Then, increase the attenuation in 1 dB steps until counting starts to vary more than ±6 Hz.

s. Press the M key on the computer, and enter the step attenuator settings (in dB's) in the performance-verification spread sheet. Then, press the C key on the computer to check that the marker counter sensitivity is within specification.

t. Disconnect the signal generator and step attenuators from the 2782.

u. Press the 2782 COUNT button, and press the Count ON/OFF menu button to select OFF.

Steps 52-76. Frequency Span Accuracy Check

This step checks uses delta markers to see that the marks are within specifications for all of the 1-2-5 sequence spans. Several different sources are used to supply adequate signal level at all spans. The time mark generator is used for most measurements. Other signal sources are used where more signal level is needed.

a. Select step 52 from the performance-verification spread sheet.

b. Connect the 500 MHz comb generator (item 9 in the equipment list) to the 2782 RF INPUT connector (as shown in Figure 2-11A). Note that the 3 dB attenuator and a connector head, which are provided with the comb generator, must be used in this test.

c. Press the Δ MKR button to activate the delta markers.

d. Place the red marker on the time mark at the first vertical graticule line (assuming the left-most vertical graticule line is line zero) and the yellow marker on the time mark at the ninth vertical graticule line. You can use the PEAK FIND <left arrow> and PEAK FIND <right arrow> buttons to place the markers on the correct time marks. The Swap Ref Marker menu button on the DELTA MARKERS menu is also useful for these tests. To use this function, set the yellow marker on the time mark at the first graticule line, then press the Swap Ref Marker button to swap the yellow and red markers. You can then position the yellow marker on the time mark at the ninth graticule line.

e. Press the M button on the computer, to enter the span accuracy measurement in the performance-verification spread sheet.

f. Disconnect the 500 MHz comb generator (including the 3 dB attenuator and the connector head) from the 2782. Then, connect a 50 Ω cable from the signal output connector of the time mark generator (item 10 in the equipment list) to the 2782 RF INPUT connector (as shown in Figure 2-11B).

g. Select steps 53 through 67 from the performance-verification spread sheet. For each step, set the time-mark generator for the setting given in the spread-sheet prompt for the verification step, and repeat steps d and e. For example, the prompt for verification step 53 says, Connect Time Mark Gen to RF input - 5 μs, indicating that the time-mark generator should be set for 5 μs time marks. Also, each time you go to a new step, press the Delta Mkrs ON/off menu button twice to toggle the red marker on again.

NOTE

In slow sweep speeds, use the single-sweep mode and make the marker measurements on the fixed display.

If on step 67 you are not able to view the peak of the fifth time mark, press the MKR/FREQ button, adjust the FREQUENCY/MARKERS knob to bring the fifth time-mark peak on screen, and press the MKR/FREQ button again.

h. Disconnect the 50-ohm cable (coming from the time-mark generator output) from the 2782 RF INPUT connector, and reconnect it to the 500 MHz comb generator Pulse input connector (as shown in Figure 2-11C). Then, connect the comb generator output to the 2782 RF INPUT connector.

i. Select steps 68 through 71 from the performance-verification spread sheet. For each step, set the time-mark generator for the setting given in the spread-sheet prompt for the verification step, and repeat steps d and e.

j. Disconnect the cables from the time-mark and comb generators. Then, reconnect a 50 Ω cable from the time-mark generator output to the 2782 RF INPUT connector.

k. Select steps 72 through 76 from the performance-verification spread sheet. For each step, set the time-mark generator for the setting given in the spread-sheet prompt for the verification step, and repeat steps d and e.

l. When the span accuracy measurement has been entered for verification step 76, press the C key on the computer to check that the span accuracy is within specification.

m. Disconnect the time-mark generator from the 2782.

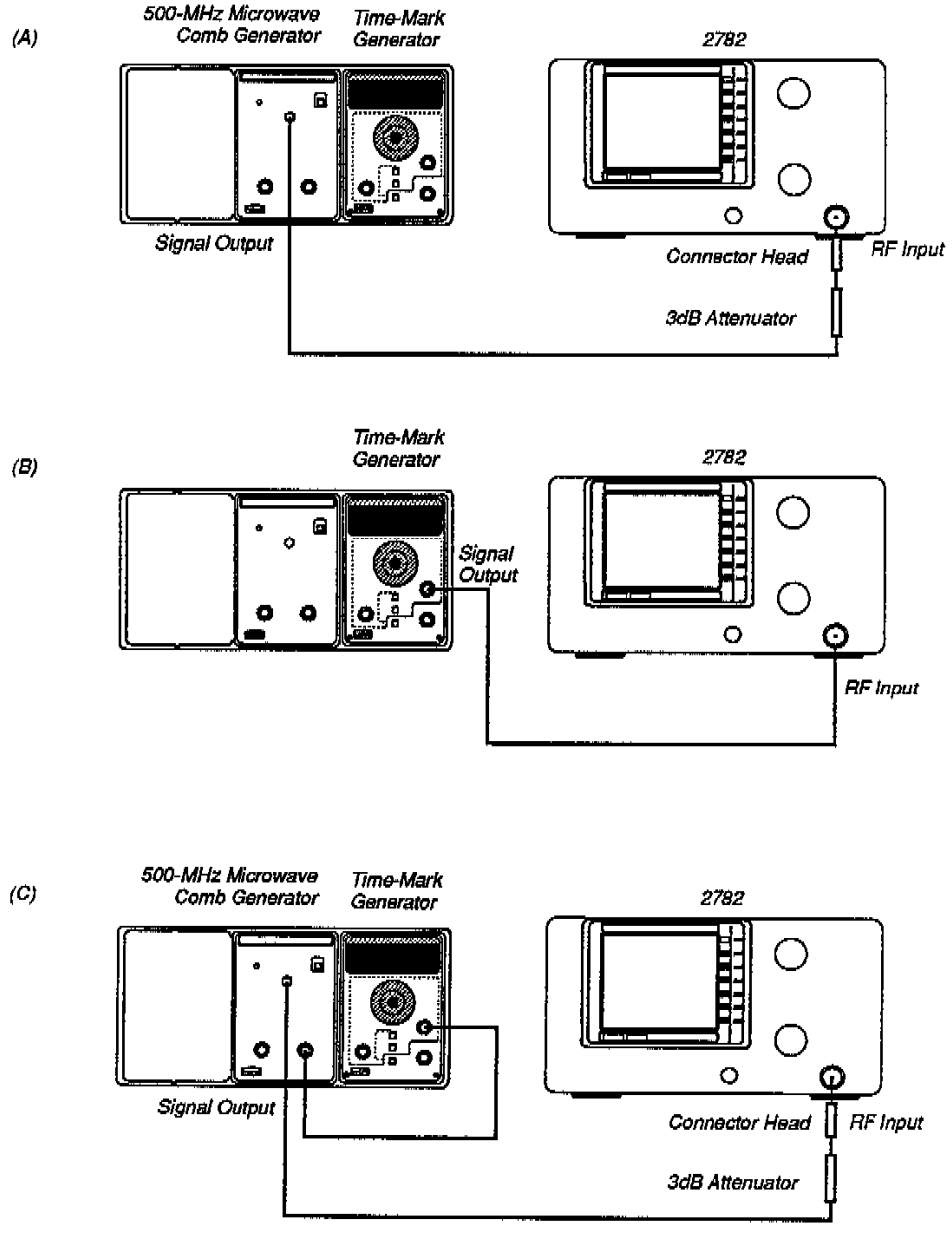


Figure 2-11. Test Equipment Setups for Frequency Span Accuracy Check

Steps 77-90. Resolution Bandwidth Accuracy Check

This check measures the bandwidth at all resolution bandwidth settings. The internal calibrator is used as a source, set BW Mkr for 6 dB offset from the menu, and measure bandwidth at all resolution bandwidth settings. These measurements are also used in the Resolution Bandwidth Shape Factor check that follows.

a. Select step 77 from the performance-verification spread sheet.

b. Connect a 50 Ω cable from the 2782 REF SIGNAL OUT connector to the RF INPUT connector (as shown in Figure 2-9).

c. Press the 2782 MKRS button, and press the BW Mkr Menu button. Then, press the Set Auto Offset button, and enter 6 dB from the keypad.

d. Press the 2782 PEAK FIND MAX button, then press the M key on the computer to enter the resolution bandwidth measurement. Be sure to allow the waveform display to stabilize and the sweep to complete its pass before you press the M key.

NOTE

This test set up measures the bandwidth of the waveform at 6 dB down relative to the marker. Neither the marker nor the 6 dB down points need to line up with horizontal graticule lines.

e. Select steps 78 through 90 from the performance-verification spread sheet, and repeat step d for each verification step.

f. When the measurement has been entered for step 90, press the C key on the computer to check that the resolution bandwidth accuracy is within specification.

g. Disconnect the cable from the 2782 REF SIGNAL OUT and RF INPUT connectors.

Steps 91-104. Resolution Bandwidth Shape Factor Check

This check measures all bandwidths again, only using 60 dB down BW MKR offset. An external source supplies the necessary power for wider bandwidths to obtain a 60 dB down signal-to-noise ratio. In narrower bandwidths, the internal calibrator supplies adequate power and eliminates source errors such as drift and FM.

The spread sheet provides the shape factor by calculating the ratio of the 6 dB bandwidths measured in the Resolution Bandwidth check, and the 60 dB bandwidths measured in this check.

a. Select step 91 from the performance-verification spread sheet.

b. Connect the signal generator (item 8 in the equipment list) to the 2782 RF INPUT connector (as shown in Figure 2-12), and set the generator for an output-signal frequency of 100 MHz and an amplitude level of 0 dBm.

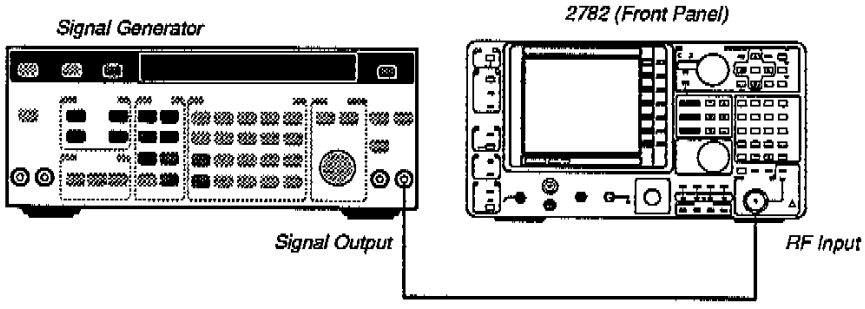


Figure 2-12. Test Equipment Setup for Steps 91-94 of Resolution Bandwidth Shape Factor Check.

c. Press the 2782 MKRS button, and press the BW Mkr Menu button. Then, press the Set Auto Offset button, and enter 60 dB from the keypad.

d. Press the 2782 PEAK FIND MAX button, then press the M key on the computer to enter the measurement.

e. Select steps 92 through 94 from the performance-verification spread sheet, and repeat step d for each verification step.

f. Disconnect the signal generator from the 2782, and connect a 50 Ω cable from the REF SIGNAL OUT connector to the RF INPUT connector (as shown in Figure 2-9).

g. Select steps 95 through 104 from the performance-verification spread sheet, and repeat step d for each verification step.

h. When the measurement has been entered for verification step 104, press the C key on the computer to check that the resolution-bandwidth shape factors are within specification.

i. Disconnect a 50 Ω cable from the REF SIGNAL OUT and RF INPUT connectors.

j. Press the MRK OFF button to turn the marker off.

Steps 105-121. Resolution Bandwidth Amplitude Accuracy Check

This check measures the absolute amplitude through each filter using the internal calibrator as a source, and then after all the measurements are made, calculates the specified accuracy. The 3 MHz filter is measured relative to -50 dBm. The other filters are specified in peak-to-peak relative amplitudes as worst case p-p variations from 10 MHz to 30 Hz, 10 MHz to 10 Hz, and 10 MHz to 3 Hz.

a. Select step 105 from the performance-verification spread sheet.

b. The 2782 calibrator signal from the REF SIGNAL OUT connector should not be connected to the RF INPUT connector. If it is, disconnect the cable from the REF SIGNAL OUT and RF INPUT connectors.

c. Press the 2782 INPUT button to select the INPUT menu. The press the Int Calib on/OFF button to select the ON mode.

d. Press the 2782 MKRS button to turn the marker on, and press the Peak Find Menu button.

e. Press the Set Peak Height menu button, and enter .1 dB from the keypad. Then, press the all menu button to select ALL.

f. Obtain a display of the internal calibrator signal on the crt display. If the peak of the waveform is off screen, press the REF LEVEL <up arrow> or <down arrow> buttons as necessary to bring the peak within the graticule window.

g. Press the 2782 PEAK FIND MAX button, then press the M key on the computer.

h. Select steps 106 through 118 from the performance-verification spread sheet, and repeat step g for each verification step.

i. Press the MKR OFF button, and press the INPUT button. Then, press the Int Calib ON/off menu button to select OFF, and press the RefSig Out on/OFF menu button to select ON.

NOTE

Steps 119 through 121 from the performance-check spread sheet perform computations only. No measurements are entered in these steps.

j. Select step 121 from the performance-verification spread sheet, and press the C key on the computer to check that the calculated value are within specification.

Steps 122-123. Residual FM Check

This check measures the fast, relatively small, frequency excursions in the analyzer. Residual FM is measured under locked and unlocked conditions using the calibrator as the signal source.

In the locked condition, the analyzer is set to a narrow span and tuned so that the center of the screen is 10 or 20 dB down the 10 Hz filter slope. Then by going to zero span while on the filter slope, any deviation in the analyzer frequency shows up as amplitude changes on the screen. The user measures the amplitude change on the screen and enters that number into the spread sheet. The spread sheet calculates the slope of the 10 Hz filter by using the data

previously measured for the resolution bandwidth and shape factor checks, and then converts the measured amplitude change into frequency change.

Measuring residual FM in the unlocked condition requires setting the analyzer for the open loop mode. This allows the analyzer to go to zero span without trying to lock. The measurement technique is the same as in the locked spans.

a. Select step 122 from the performance-verification spread sheet.

b. Connect a 50 Ω cable from the REF SIGNAL OUT connector to the the RF INPUT connector (as shown in Figure 2-9).

c. The baseline rise of the 100 MHz reference signal, which at the present span setting is a horizontal line, should be displayed on the crt (as shown in Figure 2-13). Using the 2782 FREQUENCY/MARKERS knob, center the baseline rise vertically on the crt. (Very little adjustment of the FREQUENCY/MARKERS knob is required to adjust the vertical position of the baseline rise on the crt.

NOTE

If the reference signal is not displayed, press the INPUT button, and press the RefSig Out on/OFF menu button to select ON.

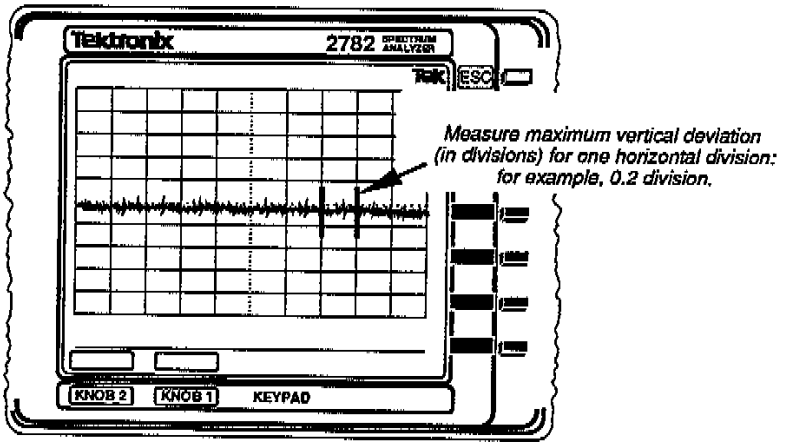


Figure 2-13. Baseline rise of 100 MHz reference signal.

d. Determine the area of the baseline rise that has the greatest vertical deviation per 1 horizontal division. Then, press the M key on the computer, and enter this vertical deviation in divisions in the performance-verification spread sheet (for example .2).

e. Select step 123 from the performance-verification spread sheet.

f. Press the 2782 UTIL button, and press the Freq Corr Menu button. Then, press the Open Loop menu button.

g. Using the FREQUENCY/MARKERS knob, place the peak of the 100 MHz calibrator signal on the center of the 2782 crt. Then, press the SPAN button and enter 0 from the keypad.

h. As in step c, the baseline rise of the calibrator signal displayed here is a horizontal line. Using the 2782 FREQUENCY/MARKERS knob, center the baseline rise vertically on the crt. (When centered, the baseline rise is a thick horizontal line.)

i. Determine the area of the baseline rise that has the greatest vertical deviation per 1 horizontal division. Then, press the M key on the computer, and enter this vertical deviation in divisions in the performance-verification spread sheet.

j. Press the 2782 UTIL button, and press the Freq Corr Menu button. Then, press the Close Loop menu button.

Step 124. Center Frequency Drift Check

CF Drift is the slow, long term frequency drift of the analyzer.

This check is done in very narrow spans and long sweep times where the analyzer frequency is corrected every sweep. The technique is to first use a relatively fast sweep speed, save the display, then go to a slow sweep speed and compare the two. The basic difference should be that it takes the analyzer a lot longer to get to the center of the screen in the slow sweep speed. Any drift occurring in the oscillators during the sweep will cause a frequency difference between the two. We measure the frequency difference and then, knowing what the sweep speeds are and the positions on screen, the program computes the drift rate.

a. Select step 124 from the performance-verification spread sheet.

b. The 2782 calibrator signal should still be connected to the RF INPUT connector from the last check. If it is not, connect a 50 Ω cable from the REF SIGNAL OUT connector to the RF INPUT connector (as shown in Figure 2-9).

c. Using the FREQUENCY/MARKERS knob, adjust the center frequency so that the rising slope of the calibrator waveform crosses the center of the graticule. Then, press the SINGLE SWEEP button.

d. Press the 2782 SWEEP button, and enter a sweep speed of 100 seconds from the 2782 Keypad. Then, press the TRIGGER button.

e. Note the horizontal position where the slope of the waveform crosses the center horizontal graticule line.

f. Calculate the difference between the horizontal position of the slope-crossing in step c and the position of the slope-crossing in step f (as shown in Figure 2-14). Then, press the M key on the computer, and enter the

difference (in horizontal divisions) in the performance-verification spread sheet.

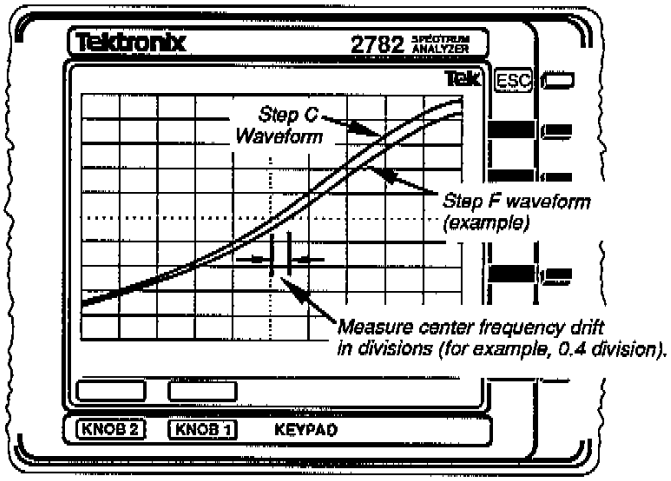


Figure 2-14. Center Frequency Drift Measurement.

NOTE

The center frequency drift specification measures the amount of drift in 50 seconds. Steps c through e should be preformed in order with no delays in between steps, to insure that approximately 50 seconds is allowed to elapse between steps c and e.

g. Press the C key on the computer to check that the center frequency drift is within specification.

h. Disconnect the cable from the REF SIGNAL OUT and RF INPUT connectors.

Steps 125-156. Logging and Lin Accuracy Check

This check measures the incremental and cumulative logging error. The incremental logging accuracy is measured for each 10 dB step in 10 dB/division. The cumulative error checks how much error accumulates at 90 dB and 100 dB down.

The test setup uses very accurately characterized step attenuators, with a couple of 6 dB attenuators between the step attenuators and the analyzer's RF INPUT to provide a stable 50Ω load for the step attenuators.

The measurement technique is to start at 10 dB/division and set the signal level for about the top of the screen. Then change the step attenuators in 10 dB steps and measure the position on the screen with the marker. The spread sheet calculates the incremental error for each 10 dB step and the makes separate calculations for 90 dB and 100 dB down.

Next, similar measurements are made for the accuracy in the volts/division and Lin modes. Start with the signal at the top of the screen, then step down to about half screen, quarter screen, and so forth in 6 dB steps. The spread sheet calculates the percentage of full screen in the Lin mode.

Similar measurements are made in the Power mode by going to Watts/division and using 3 dB steps.

NOTE

Be sure to use the cables and step attenuators called for in this step that have been recommended in the equipment list at the beginning of this section.

a. Select step 125 from the performance-verification spread sheet.

b. Connect the signal generator (item 8 from the equipment list) to the 2782 RF INPUT connector through a set of variable step attenuators and two 6 dB fixed attenuators (as shown in Figure 2-10).

c. Set the signal generator signal-output frequency for 112 MHz and the amplitude level for 12 dBm. Set the step attenuators for 0 dB attenuation.

d. Press the 2782 MKRS button, and press the Peak Find Menu button. Then, press the Set Peak Height menu button and enter .1 dBx from the 2782 keypad.

e. Press the 2782 PEAK FIND MAX button, then adjust the signal generator amplitude level to place the top of the signal at the top of the crt graticule (0 dBm as measured by the marker).

f. Press the MAX PEAK FIND button to place a single marker on the peak of the signal, then press the M key on the computer to enter the level of the signal in the spread sheet.

g. Select steps 126 through 135 from the performance-verification spread sheet. For each of these steps, set the step attenuators for the attenuation shown in the spread sheet prompt, then repeat step f. (Be sure to wait for a complete sweep before you press the M key.)

NOTE

On step 135 you may need to turn on averaging to obtain an accurate measurement. If so, press the WAVEFORM VIEW button and press the Average rd/grn/OFF menu button to select RD, and press the MKR ➡ NXT WF button to select the averaged waveform. When you have entered the measurement, press the Average RD/grn/off menu button to select OFF. This operation can be used for any step where noise or waveform instability make it difficult to accurately measure the peak of the waveform.

h. Select step 138 from the performance-verification spread sheet, and set the step attenuators for 0 dB attenuation. Then, adjust the signal generator amplitude level to place the top of the signal at the top of the crt graticule (approximately -48 dBm).

i. Press the PEAK FIND MAX button to place a single marker on the peak of the signal, and press the M key on the computer.

j. Select steps 139 through 148 from the performance-verification spread sheet. For each of these steps, set the step attenuators for the attenuation shown in the spread sheet prompt, then repeat step f.

k. Select step 149 from the performance-verification spread sheet. Then, press the 2782 REF LEVEL button, press the Vertical Scale Menu button, and press the Scale DB/v/w menu button to select V (for volts).

l. Set the step attenuators for 10 dB attenuation, and adjust the signal generator amplitude level to place the top of the signal at the top of the crt graticule (approximately 12 dBm).

m. Place a single marker on the peak of the signal, and press the M key on the computer.

n. Select steps 150 through 152 from the performance-verification spread sheet. For each of these steps, set the step attenuators for the attenuation shown in the spread sheet prompt, then repeat step f.

o. Select step 153 from the performance-verification spread sheet. Then, press the 2782 REF LEVEL button, press the Vertical Scale menu button, press the Scale db/V/w menu button to select W (for watts).

p. Set the step attenuators for 10 dB attenuation, and adjust the signal generator amplitude level to place the top of the signal at the top of the crt graticule (approximately 12 dBm).

q. Place a single marker on the peak of the signal, and press the M key on the computer.

r. Select steps 154 through 156 from the performance-verification spread sheet. For each of these steps, set the step attenuators for the attenuation shown in the spread sheet prompt, then repeat step f.

s. When the measurement has been entered in Step 156, press the C key on the computer to check that the logging, lin, and square law checks are within specification.

t. Press the 2782 REF LEVEL button, and press the Vertical Scale menu button. Then press the Scale db/v/W menu button to select DB.

Steps 157-164. RF Attenuator Accuracy Check

This checks the RF attenuator accuracy as corrected by IF Gain. The RF attenuator is characterized at the factory during initial calibration. The calibration data is stored in EEROM and is used to offset the IF Gain to compensate for attenuator errors.

The measurement technique is to compare the internal attenuation with calibrated external attenuators. An external step attenuator is set for full attenuation, and the internal attenuation is set to minimum. Then, each attenuator is changed to offset the other, keeping the signal level at the same point on the screen if the attenuators are the same. Measure each step, and the spread sheet calculates the difference. This is an absolute measurement, not incremental. That is, 30 dB attenuation should be 30 dB ± tolerance when measured.

NOTE

Be sure to use the cables and step attenuators called for in this step that have been recommended in the equipment list at the beginning of this section.

a. Select step 157 from the performance-verification spread sheet.

b. The signal generator should still be connected to the 2782 through a set attenuators. If it is not, connect the signal generator to the 2782 RF INPUT connector through a set of variable step attenuators and two 6 dB fixed attenuators (as shown in Figure 2-10).

c. Set the step attenuators for 70 dB. Then, set the signal generator frequency to 100 MHz and adjust the amplitude of the output signal so that the peak of the waveform on the 2782 is centered vertically on the crt screen (approximately 12 dBm).

e. Press the RF ATTEN button, and press the Auto ON/off button to select OFF. Then, press the RF ATTEN button again, and enter 0 dB from the keypad.

NOTE

The peak height value that the peak find buttons use should be set to 0.1 dB. If it is not press the 2782 MKRS button, and press the Peak Find Menu button. Then, press the Set Peak Height menu button, and enter .1 dBx from the 2782 keypad.

f. Press the 2782 PEAK FIND MAX button, and press the M key on the computer.

g. Select steps 158 through 164 from the performance-verification spread sheet. For each step, set the 2782 RF attenuators and the external step attenuators for the settings shown in the spread-sheet prompt, and repeat step f. To change the RF attenuators, press the RF ATTEN button and enter the attenuation from the keypad in dB (as described in step e).

h. When the measurement has been entered in verification step 164, press the C key on the computer to check that the RF attenuator accuracy is within specification.

i. Press the RF ATTEN button, and press the Auto on/OFF button to select ON.

Steps 165-268. IF Gain Accuracy Check

This check measures the accuracy of IF Gain over a 100 dB range in 1 dB steps. This is a lengthy process, taking about 15 minutes to do.

The setup is important for this check. When selecting 100 dB of external attenuation, the leakage path around the step attenuators must be much lower than the attenuation for an accurate measurement. This setup uses double-shielded cable between the generator and attenuators, 6 dB pads after the attenuator, and requires using the specified connectors.

The measurement technique is much like RF Attenuator check, matching the internal IF gain change with external attenuation. Start out with a signal at the center of the screen in 1 dB/division, and use a fairly narrow bandwidth so that the residual noise of the analyzer is low enough for the full gain positions. The test uses a 112 MHz input frequency to avoid a potential spur at 100 MHz.

Increase IF Gain by 1 dB, add in 1 dB of external attenuation, then make the measurement. Repeat this for the full 100 dB range.

Several calculations cover the specifications for this test. There are two incremental specifications and one cumulative specification. The incremental errors specify maximum error in 10 dB steps and 50 dB steps. The cumulative error is calculated over 50 dB and 100 dB. The spread sheet calculates the errors and compares them with the specifications.

NOTE

Be sure to use the cables and step attenuators called for in this step that have been recommended in the equipment list at the beginning of this section.

Also, on slow sweep speeds, be sure the sweep has gone completely across the crt screen and the marker value has been updated before you press the M key on the computer.

a. Select step 165 from the performance-verification spread sheet.

b. The signal generator should still be connected to the 2782 through a set attenuators. If it is not, connect the signal generator to the 2782 RF INPUT connector through a set of variable step attenuators and two 6 dB fixed attenuators (as shown in Figure 2-10).

c. Set the signal generator output for a frequency of 112 MHz and an amplitude level of 7 dBm. Set the variable step attenuators for 0 dB attenuation. Then, adjust the signal generator output so that the peak of the waveform is centered vertically on the 2782 crt screen.

NOTE

The peak height value that peak find buttons use should be set to 0.1 dB. If it is not press the 2782 MKRS button, and press the Peak Find Menu button. Then, press the Set Peak Height menu button, and enter .1 dBx from the 2782 keypad.

d. Press the PEAK FIND MAX button to place the marker on the peak of the waveform. Then, press the M key on the computer.

e. Select the next step from the performance-verification spread sheet, and increase the attenuation with the step attenuators 1 dB.

f. Place the marker on the peak of the waveform, and press the M key on the computer to enter the measurement.

g. Repeat steps e and f for steps 166 through 265 from the performance-verification spread sheet. (When you reach an even decade of attenuation, reset the 1 dB step attenuator to 0 dB and increase the 10 dB step attenuator by 10 dB.)

h. When the measurement has been entered for verification step 265, press the C key on the computer to check that the IF gain measured in steps 165 through 265 is within the specified range.

NOTE

If the IF gain does not meet specifications, select Othermenu, graph, IF Gain from the spread sheet menu. A graph of the accumulated IF gain error relative to the minimum IF gain is displayed on the personal computer screen. Check for a large, single-point error which would indicate a measurement error. If such an error exists, go back to those steps where the error was found and re-measure the IF gain.

i. Disconnect the signal generator and step attenuators from the 2782.

Steps 269-283. Equivalent Input Noise Check

This check measures the sensitivity of the analyzer by measuring the analyzer's internally generated noise referenced to the front end.

The first part of the equivalent input noise step measures noise with the reference level set at -70 dBm. In band one, do the test at the frequency breaks and also at 6.5 GHz. The slope of the low pass filter generally decreases all the way up to 6.5 GHz so that the maximum insertion loss can be presumed to be at 6.5 GHz.

In the other bands it's not certain where the maximum insertion loss will be. The procedure searches for the frequency of maximum noise level in each band and stores this frequency in the spread sheet. Then the analyzer is tuned to that frequency in each band, and the actual noise measurements are made.

a. Select step 269 from the performance-verification spread sheet.

b. Connect a 50 Ω terminator to the 2782 RF INPUT (as shown in Figure 2-15). Then, press the INPUT button, and press the RefSigOut ON/off button to select OFF.

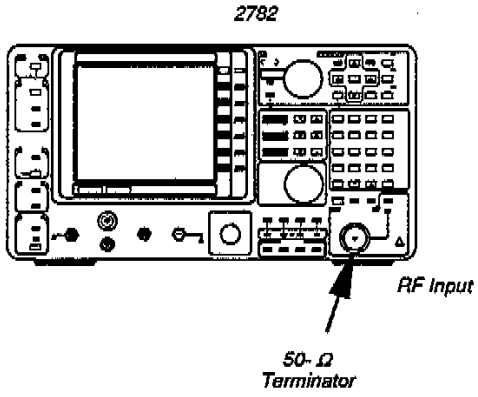


Figure 2-15. Test Setup for Equivalent Input Noise Check

c. Press the WAVEFORM VIEW button, and press the Average rd/grn/OFF menu button to select RD. Press the MKR➡NXT WF repeatedly, until the message `Marker On Average Waveform.` is displayed.

d. Using the FREQUENCY/MARKERS knob, place the single marker at the center of the screen. If a spur is present at the center of the screen, adjust the FREQUENCY/MARKERS knob to place the marker to one side of the spur within the average noise of the noise floor.

e. Allow the 2782 to sweep ten time to obtain an average noise level. (The number of sweeps in the average is read out on the crt screen, for example, `AV#6.`) When a ten sweep average is obtained, press the M key on the computer to enter the average noise measurement in the performance-verification spread sheet.

f. Select steps 270 through 273 from the performance-verification spread sheet. For each of these steps, measure the average noise at the center of the screen, as described in steps d and e.

g. Select step 274 from the performance-verification spread sheet.

h. Press the WAVEFORM VIEW button, and press the Average RD/grn/off menu button to select OFF. Press the WAVEFORM CONTROL button, and press the Acq Mode Menu button. Then, press the max button to select the MAX peak detection mode.

i. Place the marker on the highest average noise level, and press the M key on the computer.

j. Select steps 275 through 277 from the performance-verification spread sheet, and repeat step i for each step.

k. When the measurement has been entered in verification step 277, press the C key on the computer to calculate equivalent noise for steps 269 through 277.

l. Press the WAVEFORM CONTROL button, and press the Acq Mode Menu button. Then, press the min/max button to select the MIN/MAX peak detection mode.

m. Press the WAVEFORM VIEW button, and press the Average rd/grn/OFF menu button to select RD. Press the MKR➡NXT WF repeatedly, until the message `Marker On Average Waveform.` is displayed.

n. Select steps 278 through 281 from the performance-verification spread sheet. For each of these steps, measure the average noise at the center of the screen, as described in steps d and e.

o. Press the WAVEFORM VIEW button, and press the Average RD/grn/off menu button to select OFF.

p. Select step 282 from the performance-verification spread sheet.

q. Allow the 2782 to complete one sweep and obtain a stable waveform display. Then, place the single marker on the average noise level, and press the M key on the computer.

r. Select step 283 from the performance-verification spread sheet, and repeat step q.

s. When the measurement has been entered in verification step 283, press the C key on the computer to perform the overall equivalent noise calculation.

t. Disconnect the 50 Ω terminator from the RF INPUT connector. Then, press the INPUT button, and press the RefSigOut on/OFF button to select ON.

Steps 284-293. Phase Noise Check

Phase noise sidebands are low-level random noise caused by noise in the oscillator and synthesizer circuits. Phase noise sidebands extend over a wide frequency range, diminishing with frequency offset from the carrier. This check measures noise for two different carrier input frequencies. The measurement technique uses the dB/Hz measurement function, which takes care of averaging, the marker, and conversion of 1 Hz noise bandwidth, etc.

The first part of the check uses the REF SIGNAL OUT at 100 MHz as the signal source. The reference oscillator is very quiet referenced to 100 MHz, so the only measurable noise if from the synthesizers. This check measures noise at all of the specified offset frequencies.

The other measurement is made at 17.975 GHz. and is optional because of the expense of the signal source. The signal source must have as little phase noise as possible for accurate measurements. Most synthesizers in this range have too much phase noise to be used as a signal source, but using the LO OUTPUT from a second 2782 as source gives a signal with phase noise approximately equal to that of the analyzer under test. An ideal signal source would have no

phase noise sidebands, and the measurement would only reflect the noise of the analyzer under test. Assuming the two sources are equal, the measurement number will be 3 dB above the noise of either instrument. The spread sheet assumes that the sources are equal, and subtracts 3 dB from the measurement. This means that the possible measurement error is up to 3 dB if the sources are widely different. The likely error would be only 1 dB or 2 dB, if any at all.

Phase noise is measured at 1 kHz and 100 Hz offsets for the 17.975 GHz carrier. At offsets of 10 kHz and above, the instrument is still dominated by the residual noises.

a. Select step 284 from the performance-verification spread sheet.

b. Connect a 50 Ω cable from the REF SIGNAL OUT connector to the RF INPUT connector (as shown in Figure 2-9).

NOTE

If the reference signal is not displayed on the 2782 crt, press the INPUT button, and press the RefSigOut on/OFF button to select ON.

c. Press the 2782 MKRS button, and press the dBX (1 Hz) on/OFF button to select ON. Then, press the Δ MKR button to activate the delta markers.

d. Position the red marker on the peak of the calibrator signal and position the yellow marker at 100 Hz offset from the peak (either to the left or the right of the peak). The read out in the top right corner of the crt screen indicates the 100 Hz offset. (The Swap Ref Marker menu button allows you to conveniently adjust both the red and yellow markers.)

e. Wait for the dBc/Hz averaging to complete (that is, until the sweep passes the yellow marker), then press the M key on the computer to enter the phase noise measurement in the performance-verification spread sheet.

f. Select steps 285 through 288 from the performance-verification spread sheet. For each of these steps repeat steps d and e, placing the yellow marker on the following offset frequencies: 1 kHz (step 285), 10 kHz (step 286), 100 kHz (step 287), and 1 MHz (step 288).

g. When the measurement has been entered in verification step 288, press the C key on the computer to check that phase noise measured in steps 285 through 288 is with the specified range.

NOTE

Steps 289 through 293 require the use of a second 2782 Spectrum Analyzer. These steps are optional and only required to check the phase noise at 18 GHz.

h. Select step 289 from the performance-verification spread sheet.

i. Disconnect the cable from the REF SIGNAL OUT and the RF INPUT connectors. Then, connect a 50 Ω cable from the LO OUTPUT connector of

the test spectrum analyzer (another 2782) to the 2782 RF INPUT connector (as shown in Figure 2-16).

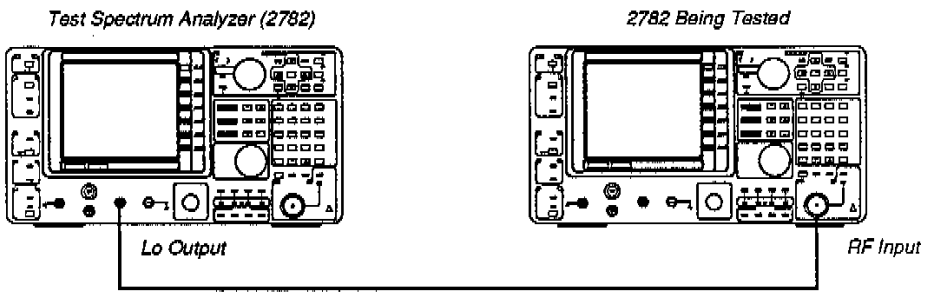


Figure 2-16. Test Equipment Setup for Steps 289-293 of Phase Noise Check.

j. Set the test spectrum analyzer for 28 GHz center frequency and zero span. This results in 17.975 GHz signal of approximately 6 dBm being generated at the LO OUTPUT connector.

NOTE

The test spectrum analyzer is being used here as a signal source. Make the control settings specified in steps k and l below on the 2782 being tested.

k. Press the Δ MKRS button to select the delta markers (if they are not already visible).

l. Place the red marker on the peak of the signal and the yellow marker at the 1 MHz offset. Then, press the M key on the computer to enter the phase-noise measurement.

NOTE

If you cannot locate the signal, press the SPAN <up arrow> button until the signal is visible, then tune the 2782 to move the signal to center screen by placing the yellow marker on the peak of the signal and pressing the MKR ➡ FREQ button. When the signal is centered, press the SPAN <down arrow> button to reduce the span to the value set by the performance-verification spread sheet program (2 MHz for step 289). At this point, you may need to press the Delta Mkrs on/OFF button twice to obtain the delta markers again.

m. Select steps 290 through 293 from the performance-verification spread sheet, and repeat step l for the offset frequencies given in the prompts for these steps.

NOTE

The performance verification spread sheet assumes that the phase noise of the test spectrum analyzer LO OUTPUT signal is equal to the phase noise of the 2782 being tested, so it subtracts 3 dB from the measured values.

n. When you have entered the measurement for step 289, press the C key on the computer to check that the phase noise measurements are within the specified range.

o. Disconnect the test spectrum analyzer from the 2782.

Steps 294-298. Residual Spur Checks

NOTE

The following procedure checks the entire frequency range of the 2782 for residual spurs. It requires as much as 16 hours to perform. It is not expected that every user will wish to invest this amount of time in a performance verification of the instrument; however, the procedure is included here for completeness.

a. Select step 294 from the performance-verification spread sheet.

b. Select OtherMenu S(ave) from the performance-verification spread sheet to save the data already accumulated in this performance-verification procedure.

c. Connect a 50 Ω to the 2782 RF INPUT connector.

d. Press the REF LEVEL button, and press the Vert Scale Menu button. Then, press the Scale DB/v/w menu button to select DB.

e. Press the FREQUENCY button, and press the Step Size Menu button. Then, press the Set Step n * Span menu button, and enter 1 from the keypad.

f. Press the FREQUENCY down arrow to step through the 2782 frequency range from 9.91 MHz center frequency to 1.11 MHz in 200 kHz steps. For each 200 kHz window, look for residual spurs greater than -77 dBm (with -76 dBm being greater than -77 dBm). If you find a residual spur, reduce the span to determine the spur's location, and write down its frequency and amplitude.

g. When you reach the center frequency of 1.11 MHz, press the 2782 SPAN button and enter 20 kHz from the keypad. Then, press the FREQUENCY down arrow to step through the frequency range from 1.11 MHz to 10 kHz, and check for residual spurs greater than -77 dBm in each 20 kHz window.

NOTE

At 10 kHz center frequency, the zero start spur can be seen on the left of the 2782 crt. Do not measure this spur.

h. Press the 2782 SPAN button and enter 2 kHz from the keypad. Then, press the FREQUENCY down arrow to step through the frequency range from 10 kHz to 0 Hz, and check for residual spurs greater than -77 dBm (other than the zero start spur).

i. At 0 Hz center frequency, press the 2782 SPAN button and enter 500 Hz from the keypad. Then, check for residual spurs greater than -77 dBm within the three horizontal divisions on the right side of the crt.

j. When you have completed the residual spur search for the 0 Hz to 10 MHz band, enter amplitude of the largest spur found into the performance verification spread-sheet. If no residual spurs greater than -77 dBm were found, enter -999 in the spread sheet.

k. Select step 295 from the performance-verification spread sheet.

l. Press the FREQUENCY up arrow to step through the frequency range of 10 MHz to 6.5 GHz in 2 MHz steps. For each 2 MHz window, look for residual spurs greater than -100 dBm. If you find a residual spur, reduce the span to determine the spur's location, and write down its frequency and amplitude.

NOTE

A 10 MHz spur appears at 10 MHz center frequency. Include the measurement of this spur in step 294, and check that it is no greater than -77 dBm.

m. When you have searched the entire frequency range of the 10 MHz to 6.5 GHz band, enter amplitude of the largest spur found into the performance verification spread-sheet. If no residual spurs greater than -100 dBm were found, enter -999 in the spread sheet.

n. Select steps 296 through 298 from the performance-verification spread sheet, and repeat steps l and m for the remaining bands of the 2782 (step 296 for the 6.5 GHz to 21.25 GHz band, step 297 for the 21.25 GHz to 28.025 GHz band, and step 298 for the 28.025 GHz to 33 GHz band.) For step 296, check for residual spurs greater than -92 dBm; for step 297, check for spurt greater than -82 dBm; and for step 298, check for spurs greater then -80 dBm.

o. Disconnect the 50 Ω terminator from the 2782 RF INPUT connector.

Step 299. Zero Start Spur Amplitude Check

This check measures the amplitude of the spur at zero frequency. The analyzer must be in full gain reduction mode to get start spur on screen.

a. Select step 299 from the performance-verification spread sheet.

b. Press the MKRS button to turn the marker on, and press the PEAK FIND MAX button to place a single marker at the peak of the zero spur.

c. Press the M key on the computer to enter the frequency of the zero spur.

d. Press the MKR OFF button to turn the marker off.

Steps 300-301. Local Oscillator Emissions Check

NOTE

Steps 300 and 301 require the use of a second Spectrum Analyzer. These steps are optional and only required to check the local oscillator emissions.

This check sets up the 2782 so that LO OUTPUT is at 10.525 GHz, then uses another analyzer to measure the signal coming out of the RF INPUT at the LO frequency. The measurement is performed at two frequencies, one in the low band and one in the high band, to test both input paths.

a. Select step 300 from the performance-verification spread sheet.

b. Connect the test spectrum analyzer to the 2782 RF INPUT connector through a 50Ω cable (as shown in Figure 2-17).

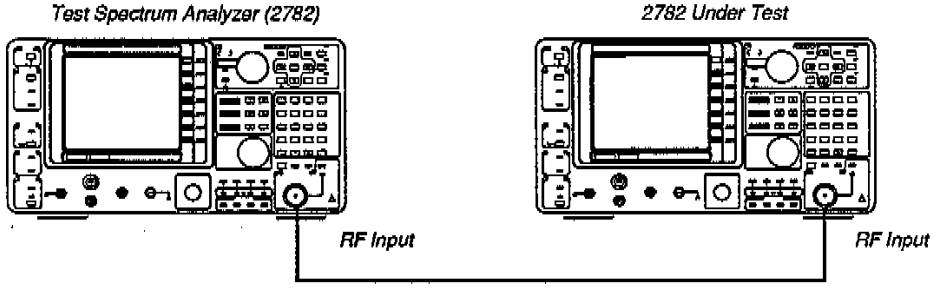


Figure 2-17. Test Equipment Setup for Local Oscillator Emissions Check

c. Set the test spectrum analyzer for a center frequency of 10.525 GHz, a span of 200 kHz, a reference level of -75 dB, and a dB/division of 10 dB.

d. On the test spectrum analyzer, measure the signal level at 10.525 GHz, due to local oscillator emissions. (The local oscillator signal will most likely not be visible in the noise floor, so measure the level of the noise floor.)

e. Press the M key on the computer, and enter the measurement.

f. Select step 301 from the performance-verification spread sheet, and repeat steps d and e.

g. Disconnect the test spectrum analyzer from the 2782.

Steps 302-305. External Frequency Reference Check

This checks that the external FREQ REF IN/OUT, when set for an input, will accept and lock to a signal over the specified frequency and amplitude range. The external source needs to be locked to a WWV frequency standard receiver or some other high accuracy source. This may involve a lengthy wait for the reference to stabilize at times.

a. Select step 302 from the performance-verification spread sheet.

b. Disconnect the cable from the 2782 RF INPUT connector (if one is still attached). Then, connect a 50Ω cable from the IN/OUT FREQ REF connector on the rear panel of the 2782 to the output of the signal generator (as shown in Figure 2-18). (The signal generator used is item 8 of the equipment list.)

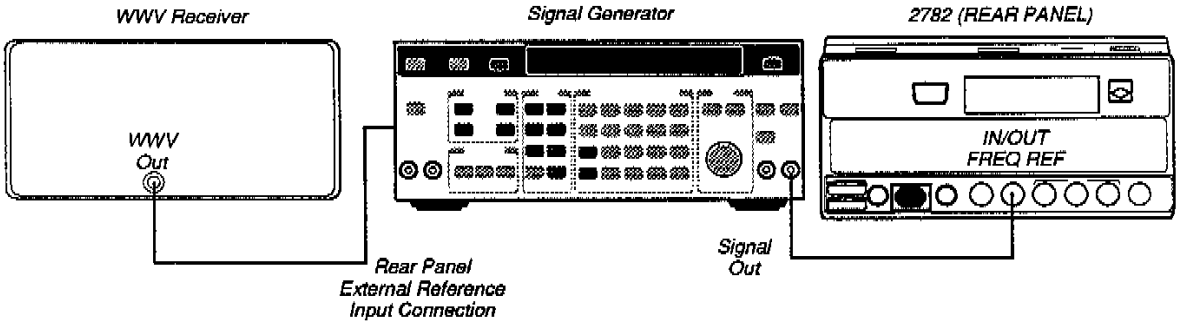


Figure 2-18. Test Equipment Connection for External Frequency Reference Check.

c. Connect a 50 Ω cable from the output of the 10 MHz frequency standard (item 7 from the equipment list) to the external reference input of the signal generator.

d. Set the signal generator output for 10.000 MHz and +5 dBm, with the signal frequency locked to the frequency standard signal.

e. Press the 2782 FREQUENCY button, and press the Configure Freq Menu button. Then press the Ref Osc INT/ext button to select the EXT reference.

f. Set the frequency of the signal generator to 9.999990 MHz, and check that the phase-lock loop for the reference frequency remains locked. If the phase-lock loop becomes unlocked, the 2782 displays the message `Reference Loop Will Not Lock.`

NOTE

Wait approximately 20 seconds after setting the signal generator frequency, to give the phase-lock loop time to respond.

g. Enter a 1 in the performance-verification spread sheet if the phase-lock loop remains locked, and enter a 0 if it does not.

h. Reset the signal generator signal output frequency to 10 MHz, and if the phase-lock loop became unlocked in step f, wait until the loop locks again and the message is removed from the screen.

i. Select step 303 from the performance-verification spread sheet.

j. Set the frequency of the signal generator to 10.000010 MHz, and check that the phase-lock loop for the reference frequency remains locked (the message `Reference Loop Will Not Lock.` is not displayed).

k. Enter a 1 in the performance-verification spread sheet if the phase-lock loop remains locked, and enter a 0 if it does not.

l. Select step 304 from the performance-verification spread sheet.

m. Set to the signal-generator output for 10 MHz and 0 dBm.

n. Check that the phase-lock loop for the reference frequency remains locked (the message `Reference Loop Will Not Lock.` is not displayed).

o. Enter a 1 in the performance-verification spread sheet if the phase-lock loop remains locked, and enter a 0 if it does not.

p. Select step 305 from the performance-verification spread sheet.

q. Set the signal-generator output amplitude +15 dBm, and check that the phase-lock loop for the reference frequency remains locked (the message `Reference Loop Will Not Lock.` is not displayed).

r. Enter a 1 in the performance-verification spread sheet if the phase-lock loop remains locked, and enter a 0 if it does not.

s. Disconnect the signal generator and 10 MHz frequency standard from the 2782.

Step 306. Frequency Reference Output Check

This step checks the 10 MHz FREQ REF IN/OUT in the output mode. The counter must be locked to an accurate reference because that is going to be a standard to make sure that the CF and Marker/Counter checks are complete. Count the reference and check to make sure it is within the absolute accuracy specification.

a. Select step 306 from the performance-verification spread sheet.

b. Connect a 50 Ω cable from the IN/OUT FREQ REF connector to the signal input to the counter (as shown in Figure 2-19). Then, connect a cable from

the 10 MHz frequency standard signal output to the reference signal input to the counter.

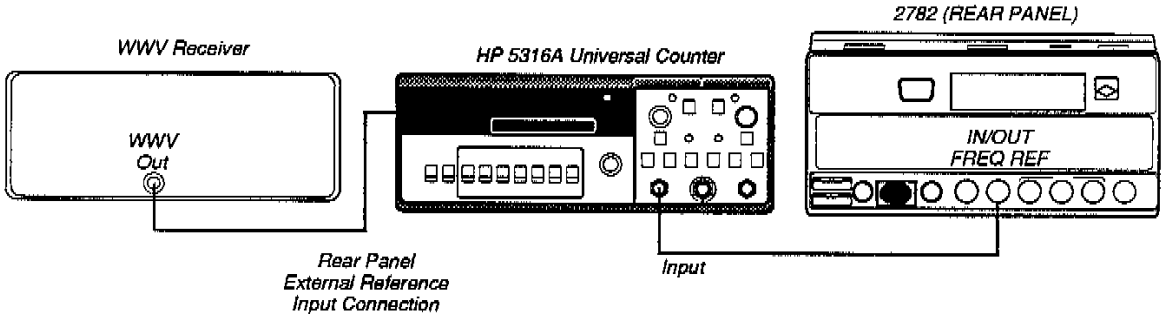


Figure 2-19. Test Equipment Connections for Frequency Reference Accuracy Check.

c. Lock the counter to the 10 MHz frequency standard.

d. Press the FREQUENCY button, and press the Configure Freq Menu button. Then, press the Ref Osc int/EXT menu button to select INT, and press the FreqRefOut on/OFF button to select ON.

e. Count the frequency of the 2782 frequency reference signal, and enter the frequency in the performance-verification spread sheet (for example, 10000000.01).

f. Press the C key on the computer to calculate the frequency reference output accuracy.

g. Press the 2782 FreqRefOut ON/off menu button to select OFF.

h. Disconnect the counter from the IN/OUT FREQ REF connector.

Steps 307-309. Internal Trigger Level and Frequency Check

These steps check that the analyzer will properly trigger on a signal that is displayed on the screen within the specified level and frequency range.

An external signal source routes into the External Video Input. This goes into analyzer prior to the point the trigger is picked off, so the analyzer can use the internal trigger, but still trigger off an external source with a nice sine wave. Display the signal and make sure all of the trigger functions, such as slope, trigger level, and HF reject, all work properly at frequencies and amplitudes specified. The amplitude is measured in divisions on the screen for this check.

a. Select step 307 from the performance-verification spread sheet.

b. Connect a BNC-Tee connector to the TRIG/HORIZ IN connector on the 2782 rear panel (as shown in Figure 2-20).

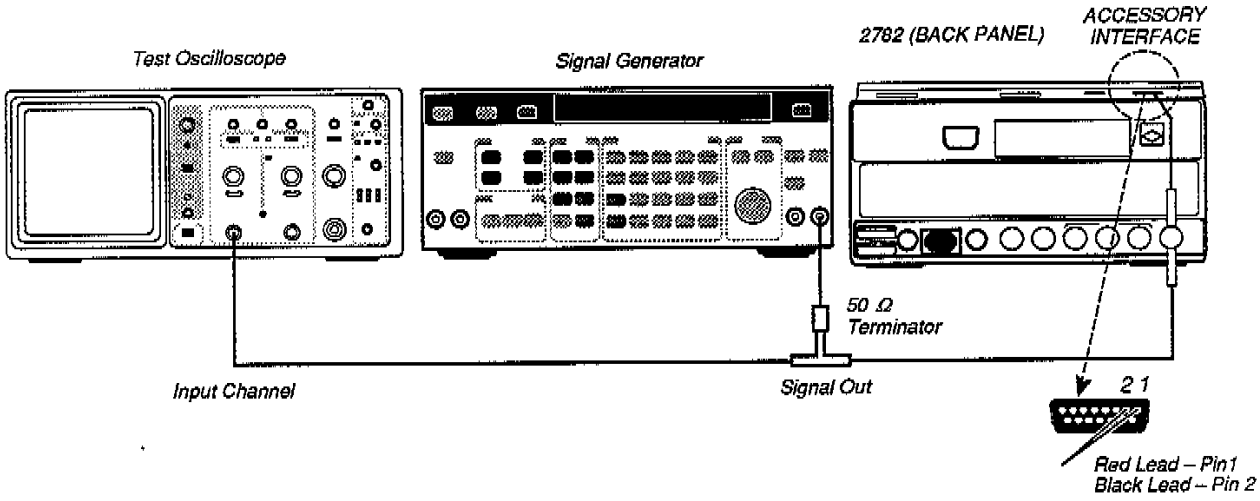


Figure 2-20. Test Equipment Connections for Internal Trigger Check.

c. Connect a 50 Ω cable to the signal-generator signal output. Connect a 50 Ω terminator to the other end of the cable, and connect the center arm of a BNC-Tee connector to the 50 Ω terminator. Then, connect a 50 Ω cable from one side of the Tee to one of the test oscilloscope's vertical inputs.

d. Connect a 50 Ω cable from the other side of the Tee coming from the signal generator to the Tee connected to the 2782 TRIG/HORIZ IN connector. Then, connect the other side of the Tee connected to the TRIG/HORIZ IN connector to pins 1 and 2 of the 2782 Accessory Interface connector. This latter connection is made through the BNC-to-Dual-Pin-Out cable (item 18 of the non-flatness equipment list), with the center conductor (the red lead of this cable) going to pin 1 of the Accessory Interface connector and the ground lead (the black lead) going to pin 2.

e. Set the signal generator for a sine wave output with a frequency of 10 Hz. Adjust the amplitude level to 200 mV peak-to-peak, as measured on the test oscilloscope.

f. Press the 2782 WAVEFORM CONTROL button, and press the Real Time Menu button. Then, press the Real Time menu button to ON, and press the Video Src menu button to select EXT.

g. Press the ESC button once, and press the Acq Mode Menu button. Then, press the min/max menu button to select the MIN/MAX mode.

h. Press the WAVEFORM VIEW button, and press the Normal GRN/rd/off button to select OFF.

i. Press the TRIGGER button, the Source Menu button, and the internal button to select INTERNAL triggering. Then, press the ESC button, and

press the Trig Level to Knob 1 button. Then, press the HF Reject on/OFF button to select ON.

j. Vary Knob 1 until a stable positive-triggered waveform is observed on the 2782 screen.

k. Press the Slope POS/neg menu button to select NEG, and check that the waveform is being triggered on the negative slope.

l. Press the Slope pos/NEG button to select POS, and check that the waveform is being triggered on the positive slope.

m. Press the M key on the computer, and enter a 1 in the performance-verification spread sheet if the 2782 triggers properly and enter a 0 if it does not.

n. Select step 308 from the performance-verification spread sheet.

o. Set the signal generator for a signal output frequency of 1 MHz, and adjust the amplitude level to 200 mV peak-to-peak, as measured on the test oscilloscope.

p. Press the TRIGGER button, and press the HF Reject ON/off button to select OFF.

q. Repeat steps j through m for the 1 MHz signal input.

r. Select step 309 from the performance-verification spread sheet.

s. Set the signal generator for a signal output frequency of 1 kHz, and adjust the amplitude to approximately 4.7 volts peak-to-peak to obtain a full screen display on the 2782.

t. Vary Knob 1 trigger level and check that the sweep remains triggered and that the slope of the signal can be adjusted over the top six vertical divisions of the 2782 crt.

u. Press the M key on the computer, and enter a 1 in the performance-verification spread sheet if the 2782 triggers properly and enter a 0 if it does not.

v. If you are not continuing with the next step, disconnect the test equipment from the 2782.

Steps 310-313. External Trigger Level and Frequency Check

This check is similar the the Internal Trigger check, except that external triggering is selected. This time the trigger signal enters the rear-panel EXT TRIG/HORIZ input. The signal is still applied to the External Video Input to provide a stable sine wave display on the analyzer. The amplitude is specified in voltage for external triggering.

a. The test equipment should still be set up as shown in Figure 2-20. If it is not, connect the equipment as describe in steps b through d for performance-verification checks 307-309 above.

b. Select step 310 from the performance-verification spread sheet.

c. Press the TRIGGER button, the Source Menu button, and the external button to select EXTERNAL triggering. Then, press the ESC button, and press the Trig Level to Knob 1 button. Then, press the HF Reject on/OFF button to select ON.

d. Set the signal generator for a signal output frequency of 10 Hz, and adjust the amplitude level to 400 mV peak-to-peak, as measured on the test oscilloscope.

e. Adjust Knob 1 (which controls the trigger level) for a stable triggered display.

f. Press the M key on the computer, and enter a 1 in the performance-verification spread sheet if the 2782 triggers properly and enter a 0 if it does not.

g. Select step 311 from the performance-verification spread sheet.

h. Set the signal generator for a signal output frequency of 5 MHz, and adjust the amplitude level to 400 mV peak-to-peak, as measured on the test oscilloscope.

i. Press the TRIGGER button, and press the HF Reject ON/Off menu button to select OFF. Then repeat steps e and f.

j. Select step 312 from the performance-verification spread sheet.

k. Set the signal generator for a signal output frequency of 1.5 kHz, and adjust the amplitude level to 400 mV peak-to-peak, as measured on the test oscilloscope.

l. Repeat steps e and f.

m. Select step 313 from the performance-verification spread sheet.

n. With the signal generator output frequency still at 1.5 kHz, increase the signal-generator amplitude level to 1.8 volts peak-to-peak, as measured on the test oscilloscope.

o. Vary Knob 1 (which controls the trigger level) and check that the sweep remains triggered and that the slope of the signal can be varied vertically over the top 6 divisions of the 2782 crt.

p. Enter a 1 in the performance-verification spread sheet if the 2782 triggers properly, and enter a 0 if it does not.

q. Disconnect the test equipment from the 2782.

Steps 314-315. External Sweep Input Check

This check makes sure that the External Sweep voltage required to get the left and right screen edges is within tolerances.

a. Select step 314 from the performance-verification spread sheet.

b. Connect a 50 Ω cable to the function-generator signal output (as shown in Figure 2-21), and connect the center arm of a BNC-Tee connector to the other end of the cable.

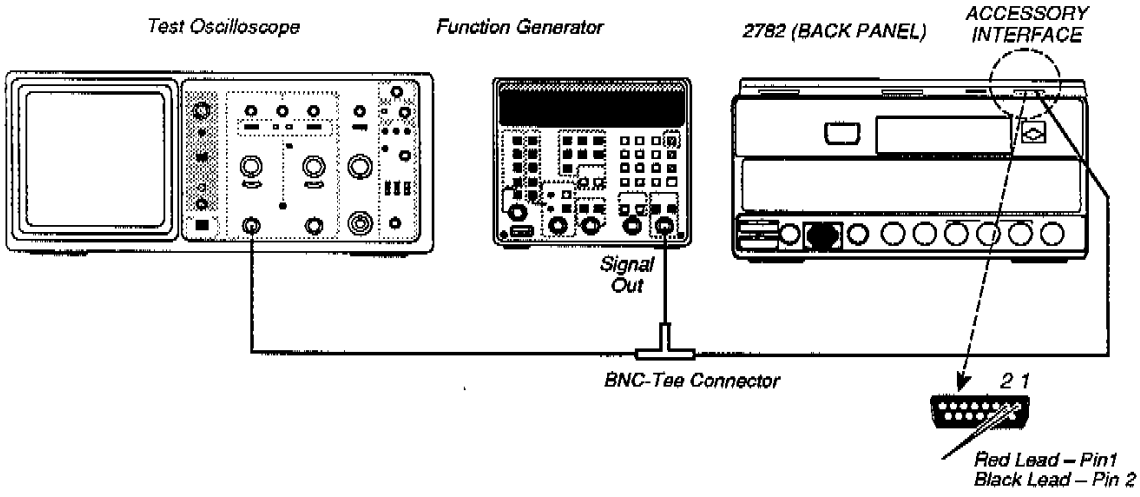


Figure 2-21. Test Equipment Connections for External Sweep Input Check.

c. Connect a 50 Ω cable from one side of the Tee to the 2782 TRIG/HORIZ IN connector on the rear panel. Connect a 50 Ω cable from the other side of the Tee to one of the test oscilloscope's vertical inputs.

d. Press the WAVEFORM CONTROL button, and press the Real Time Menu button. Then, press the Real Time on/OFF button to select ON.

e. Press the WAVEFORM VIEW button, and press the Normal GRN/rd/off menu button to select OFF.

f. Press the SWEEP button, and press the Sweep Src Menu button. Then, press the Sweep Src INT/ext button to select the EXT sweep source, and press the Ext Range 0/10 -5/5 button to select the 0/10 volt range.

g. Set the function generator for a sine wave output with a frequency of 100 Hz, and set the signal amplitude for 10 volts peak-to-peak, as measured with the test oscilloscope. Then, adjust the function-generator dc offset for 3.5 volts.

h. While viewing the signal on the 2782 crt, adjust the function generator amplitude and offset controls for a full 10 divisions of deflection on the crt graticule.

i. Determine the voltage level (relative to 0 volts) of the negative peaks of the signal displayed on the test oscilloscope. Then, press the M key on the computer, and enter the voltage in the performance-verification spread sheet.

j. Select step 315from the performance-verification spread sheet.

k. Press the SWEEP button, and press the Sweep Src Menu button. Then, press the Sweep Src INT/ext button to select the EXT sweep source.

l. Determine the voltage level (relative to 0 volts) of the positive peaks of the signal displayed on the test oscilloscope. Then, press the M key on the computer, and enter the voltage in the performance-verification spread sheet.

m. Disconnect the function generator from the 2782.

n. Press the WAVEFORM CONTROL button, and press the Real Time Menu button. Then, press the Real Time ON/off menu button to select OFF, and press the Video Src int/EXT menu button to select INT.

o. Press the WAVEFORM VIEW button, and press the Normal grn/rd/OFF button to select GRN.

Steps 316-319. External Mixer Input LO Out

When an external two-port mixer is used, the external mixer input port acts as both an IF input port and an LO output port. A diplexer inside the instrument separates these signals according to frequency. The external two-port mixers require a minimum LO level, so this checks that the 2782 supplies enough level. The LO Output is specified in three bands: <12 GHz, 12 -16 GHz, and 16 - 18 GHz. There is more power in the middle of the range and it tends to tail off at both ends. Three measurements check each LO Output band.

The measurement technique is to set the start-stop frequencies such that the LO will be swept over the frequency band specified. Start the sweep at a very slow sweep speed, then watch power meter readings and note the lowest power level during sweep. Do this for each of three bands.

a. Select step 316 from the performance-verification spread sheet.

b. Remove the 50 Ω terminator from the 2782 EXTERNAL MIXER connector, and connect the power meter to that connector (as shown in Figure 2-22). Use the Hewlett-Packard HP 8481A power sensor head with the power meter. This sensor head requires an N-to-SMA connector.

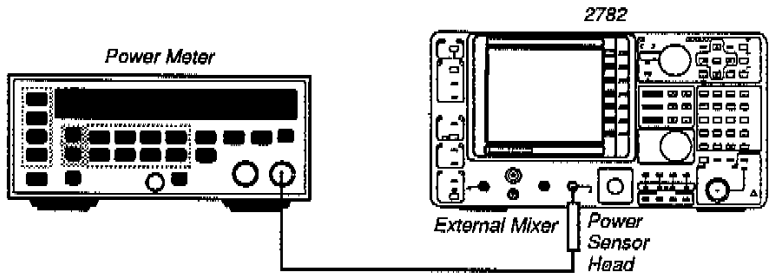


Figure 2-22. Test Equipment Connections for External Mixer Input LO Output Check.

c. Press the 2782 INPUT button, and press the Band Menu button. Then, press the Band to Knob 1 menu button, press the RFIn Limit HIGH/low menu button to select LOW, and press the Harmonics odd/EVEN menu button to select ODD harmonics.

d. Select step 317 from the performance-verification spread sheet.

e. Measure the lowest power in dBm of the external-mixer local-oscillator signal as the oscillator slowly sweeps the 12.4- to 18 GHz frequency band. Enter this value in the performance-verification spread sheet.

NOTE

For all the steps in this section, allow the 2782 to complete one sweep before you begin monitoring the level of the signal. Also, only measure the waveform where noise exits. For step 317 the noise does not start until the waveform reaches approximately the fourth division of the display and for step 319, the noise ends at approximately the end of the fifth division.

f. Select step 318 from the performance-verification spread sheet.

g. Measure the lowest power in dBm as the oscillator sweeps the 40 GHz to 65 GHz frequency band. Enter this value in the performance-verification spread sheet.

h. Select step 319 from the performance-verification spread sheet.

i. Adjust Knob 1 to select the external-mixer band of 33-50 GHz.

j. Measure the lowest power in dBm as the oscillator sweeps the 33- to 50 GHz frequency band. Enter this value in the performance-verification spread sheet.

k. Disconnect the power meter from the EXTERNAL MIXER connector, and reconnect the 50 Ω terminator to the connector.

l. Press the 2782 INPUT button, and press the Band Menu button. Then, press the RFIn Limit high/LOW menu button to select HIGH, and press the Harmonics ODD/even menu button to select EVEN harmonics.

Steps 320. 100 MHz Calibrator-Amplitude Check

This check uses a power meter to directly measure the accuracy of the REF SIGNAL OUT.

a. Select step 320 from the performance-verification spread sheet.

b. Press the 2782 INPUT button, and press the RefSig Out single/COMB menu button to select SINGLE.

c. Obtain the Hewlett-Packard HP 432A Power Meter and HP 8484A Power Sensor Head (item 6 of the equipment list), and a 10 dB attenuator.

d. If the power sensor head is not already connected to the power meter, turn off the power meter, connect the power sensor cable and the power sensor head to channel A of the power meter, and turn on the power meter. (The power meter should be turned off when connecting the power sensor head to prevent damage.)

NOTE

The HP 438A power meter has two input channels (A and B). The HP 8484A power head can be connected to either channel for this performance-verification test.

e. Connect a Hewlett-Packard HP 11708 30 dB attenuator to the POWER REF connector of the power meter.

f. Press the power meter Channel A button (or Channel B if the power head is connected to channel B), and press the ZERO button. (Wait a few seconds for the zeroing routine to complete.)

g. Press the power meter CAL FACTOR button and enter the REF CF% value that is recorded on the 8484A power sensor head from the power meter keypad (for example, 97.0 ENTER).

h. Connect the HP 8484A power sensor head to the HP 11707 30 dB attenuator that is connected to the power meter POWER REF connector (as shown in Figure 2-23A).

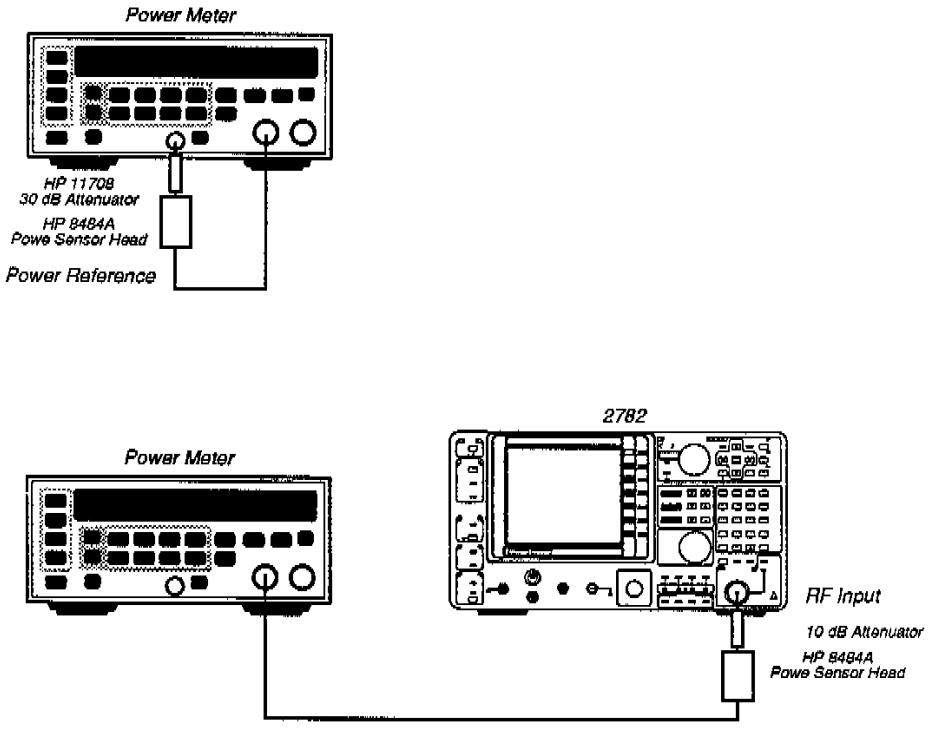


Figure 2-23. Test Equipment Connections for 100 MHz Calibrator Amplitude Check.

i. Press the power meter OSC button, and press the CAL ADJ button. Then, enter the REF CF% value entered in step g from the power meter keypad. The power meter should read -30.00 dBm.

j. Disconnect the 8484A power sensor head from the 30 dB attenuator, and connect a 10 dB N-type attenuator to the power sensor head. Then, connect the power sensor head and 10 dB attenuator back to the 30 dB attenuator connected to the power meter.

k. Press the REL button on the power meter.

l. Disconnect the power sensor head and 10 dB attenuator from the 30 dB attenuator, and reconnect the power sensor head and 10 dB attenuator to the REF SIGNAL OUT connector of the 2782 (as shown in Figure 2-23B).

m. Press the M key on the computer and enter the power meter reading in the performance-verification spread sheet in dB's.

n. Press the C key on the computer to check that the 100 MHz calibrator amplitude is within specification.

o. Disconnect the power sensor head and 10 dB attenuator from the 2782.

p. Press the 2782 INPUT button, and press the RefSig Out SINGLE/comb menu button to select COMB.

Steps 321-326. Sweep Speed Timing Accuracy Check

This check measures the time for the sweep to travel across the screen. A time-mark signal is applied to the External Video Input, and the analyzer is internally triggered from it to get a stable display. Then the sweep speed is checked over decade steps.

The check is similar to the Frequency Span check. Place the markers on the first and ninth graticule lines, and set the analyzer to 1 kHz span so that ideally the difference between markers would be 800 Hz. Use delta markers to measure. The check goes to real-time sweep, where markers can't be placed directly on the signal. The markers can still be used by storing a flat line trace at the bottom of the screen, and using the delta markers on that as an overlay for the real-time signal.

a. Select step 321 from the performance-verification spread sheet.

b. Connect the time-mark generator (through a 50Ω attenuator) to the video input of the Accessory Interface connector on the 2782 rear-panel (as shown in Figure 2-24). Use a 50Ω cable and the BNC-to-dual-pin-out cable (item 18 from the equipment list). The red lead goes to the pin 1 (the signal input) and the black lead goes to pin 2 (ground).

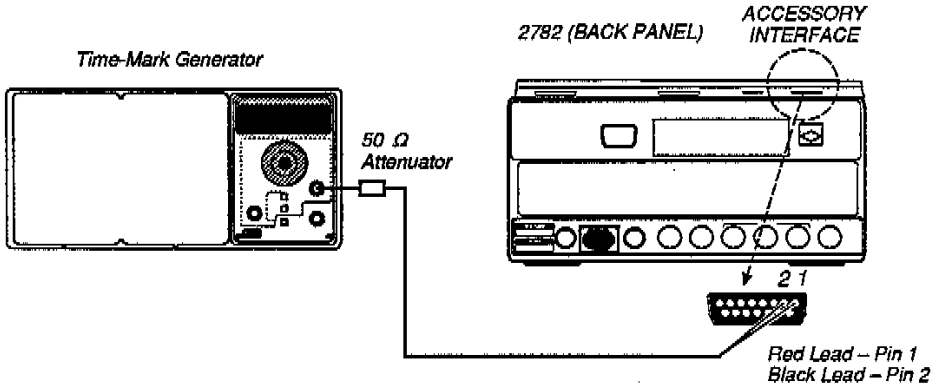


Figure 2-24. Test Equipment Connections for Sweep Speed Timing Accuracy Check.

c. Press the 2782 CONTROL button, and press the Real Time Menu button. From the Real Time Menu, press the Video Src INT/ext menu button to select EXT.

d. Press the TRIGGER button, and press the Trig Level to Knob 1 menu button. Then press the Source Menu button, and press the INTERNAL menu button.

e. Set the time-mark generator to 1 second

f. Press the Δ MKR button, and adjust Knob 1 for a stable trigger display if needed.

g. Position the 2782 delta markers on the first and ninth time marks displayed on the crt.

h. Press the M key on the computer to measure the time between the first and ninth markers.

i. Select step 322 from the performance-verification spread sheet, and set the time-mark generator for 0.1 second. Then repeat steps g and h.

NOTE

If you have difficulty triggering the display, press the 2782 SINGLE SWEEP button to make the measurement, then press the TRIGGER button and the Δ MKR button before going to the next measurement.

j. Select step 323 from the performance-verification spread sheet, and set the time-mark generator for 10 milliseconds. Then repeat steps g and h.

k. Select step 324 from the performance-verification spread sheet, and set the time-mark generator for 1 millisecond. Then repeat steps g and h.

l. Select step 325 from the performance-verification spread sheet, and set the time-mark generator for 100 microseconds. Then repeat steps g and h.

m. Disconnect the cable from the time-mark generator so that a trace is displayed on the 2782 crt, and press the 2782 SINGLE SWEEP button.

n. Select step 326 from the performance-verification spread sheet, and set the time-mark generator for 10 microseconds.

o. Press the 2782 WAVEFORM CONTROL button, and press the Real Time Menu button. Then, press the Real Time on/OFF menu button to select ON.

p. Reconnect the cable to the time-mark generator. Then, press the 2782 TRIGGER button, and adjust the 2782 triggering so that a stable display of the time marks is displayed on the 2782 crt.

q. While observing the real-time time marks, position the 2782 delta markers (on the digitized trace) under the first and ninth real-time time marks.

r. Press the M key on the computer to measure the time between the first and ninth markers.

s. Press the C key on the computer and check that the sweep-timing accuracy is within the values specified in the performance-verification spread sheet.

t. Disconnect the time-mark generator from the 2782.

Adjustments

This section provides an adjustment procedure for the instrument. It includes all the adjustments in the instrument that are visible at the module level. Adjustments within modules are not covered. Refer to Section 2, Performance Check, for instructions on checking the performance of the instrument after the adjustments have been made.

Introduction

This procedure can be used either to adjust a particular section the instrument that is not performing within specifications, or a section that has been recently repaired, or to perform an overall adjustment of the instrument as a part of routine maintenance.

The procedure is divided into two parts. The first part is used for flatness calibration and the second part is used to adjust the rest of the instrument. The flatness calibration procedure uses a special flatness calibration and verification software package, which is supplied with the instrument.

Before making any adjustment, allow the instrument to warm up for at least one hour, in an ambient temperature of +20° C to +30° C. Any waveform illustrations in this procedure are typical and may differ from one instrument to another. These waveforms do not necessarily represent specification tolerances.

Note

When any repairs or djustments are made to the 2782 vertical section, all of the vertical section adjustments should be recalibrated.

Equipment Required

Table 3-1 shows the equipment required for the flatness calibration and other adjustments.

Table 3-1. Equipment Required for Adjustments.

Item	Characteristics	Recommended
1. Personal computer	Intel 8088 CPU or better; MS-DOS 2.0 or later; dual floppy-disk drives or one floppy-disk and one hard-disk drive; 640 KBytes of RAM; graphics monitor; and one National PC2 or PC2A GPIB interface board. NOTE: An 80286-based PC (IBM PC AT or equivalent), EGA graphics card and monitor, MS-DOS 3.1 or later, and a second GPIB interface board are required for the Flatness checks. The GPIB Interface boards for the Flatness check must be National PC2A compatible.	IBM PC XT or compatible (IBM PC AT or equivalent for Flatness). TEKTRONIX PEP301 with Tektronix S3FG120 GPIB Interface board. (Two GPIB Interface boards required for Flatness checks)
2. Test Oscilloscope	100 MHz frequency range	TEKTRONIX 2235 Oscilloscope
3. Digital Voltmeter	Range 0 to ±200 volts; Accuracy 0.05%	TEKTRONIX DM5010 or DM501A Digital Multi-meter
4. Counter	9-digit accuracy; frequency range of 10 MHz to 100 MHz; and lockable to a 10 MHz reference signal	Hewlett-Packard HP5316A
5. Power Meter	Frequency range from 0 to 100 MHz (0 to 33 GHz for Flatness)	Hewlett-Packard HP438A with HP8484A and HP11708A 50 MHz 30 dB Reference Attenuator. NOTE: For Flatness only, two additional power sensors are required: an HP8487A and an HP8482A
6. 10 MHz Frequency Standard	Accurate to within 0.01 Hz	WWV receiver or other high-accuracy standard
7. Signal Generator	Frequency range of 10 kHz to 100 MHz, with less then -50 dBc of harmonic distortion.	Hewlett-Packeard HP8642A Synthesized Signal Generator, or equivalent.
8. Step Attenuators (2 Required)	1 dB/step within 0.1 dB at 100 MHz 10 dB/step within 0.5 dB at 100 MHz	Hewlett-Packard 355C Hewlett-Packard 355D
9. Fixed attenuators	6 dB, SMA (2 each) 10 dB 50 Ω, 2 W, dc to 12.4 GHz, N Conn.	Tektronix Part No. 015-1001-00 Tektronix Part No. 011-0085-00
10. Coaxial Cables	BNC, 50 Ω ±1% precision, 36 in. BNC, 50 Ω, 42 in. (2 each) SMA, 50 Ω, 28.5 in.(2782 standard accessory)	Tektronix Part No. 012-0482-00 Tektronix Part No. 012-0057-01 Tektronix Part No. 012-0649-00
11. Coaxial Adapter	BNC male to BNC male BNC female to SMA male SMA male to SMA male	Tektronix Part No. 103-0029-00 Tektronix Part No. 015-1018-00 Tektronix Part No. 015-1011-00
12. RS232 Interface		2782 processor-extender card with RS232 interface, supplied with Service Kit
13. RS-232 Cable		Supplied with Service Kit
14. Personal Computer communications program	Data transfer between computer and 2782	Kermit - public domain communcations program from Columbia University

Part I. Flatness Calibration

The 2782 spectrum analyzer incorporates an internal flatness circuitry that automatically compensates for deviations in the instrument's signal response over its entire frequency range. This automatic compensation is responsible for the instrument's extremely flat frequency response (that is, the instrument's ability to accurately measure a constant amplitude signal over the frequency range of 100 Hz to 33 GHz).

This section of the 2782 performance verification procedure describes how to calibrate the frequency response (or flatness) of the instrument. The flatness calibration is performed with a Tektronix-designed flatness calibration and verification software package, which runs on an MS-DOS compatible personal computer.

Overview of the Flatness Test Procedure

To verify the flatness performance of a 2782, you must perform the following six steps:

1. Install the flatness software on the personal computer.
2. Set up the test equipment.
3. Run the equipment configuration program (CONFIG.EXE).
4. Run the flatness utility program (UTIL.EXE) to level the test equipment.
5. Run the CAL portion of the flatness program (CATS.EXE) to calibrate the 2782'spreselector tracking and to collect uncorrected flatness data from the 2782 flatness.
6. Download the uncorrected flatness data (using DOWNLOAD.EXE) to the 2782.

The following sections describe these steps in detail.

Installing the Flatness Software on the Personal Computer

The flatness software is contained on three 5 1/4-inch floppy disks, which come with the 2782 as standard equipment. These disks contain the following files:

Disk 1:

README.DOC	Software documentation.
INSTALL.BAT	Installation batch file.
CATS.EXE	Flatness verification and preselector tracking program.

Disk 2:	
UTIL.EXE	System hardware characterization program.
TOPICS.IDX	Index file for CATS on-line help system.
*.HLP	Text files for CATS on-line help system.
Disk 3:	
CONFIG.EXE	System configuration file build utility.
DOWNLOAD.EXE	Loads flatness corrections into the 2782.
PLOT.EXE	Displays flatness results graphically on screen.
782.EIS and 2782.NUM	These two files contain the performance requirement information (specifications) that CATS uses.
HFCONFIG, SW_CONF, and FLATNESS.SEQ	These three files, plus others (created by CONFIG.EXE) describe to CATS.EXE the test equipment and all interconnections that are required.

Use the following procedure to install the flatness software on the personal computer (item 1 of the equipment list):

1. Install disk 1 in drive A of the personal computer.
2. Set the default drive for A (enter a:).
3. Enter the following command to install the flatness software on your hard disk:

```
A> install <ENTER>
```

INSTALL prompts you to switch disks.

NOTE

INSTALL.BAT is a batch file that creates a directory on your hard disk (called TEKCATS) and several subdirectories. It then copies the flatness software into these directories.

Setting Up the Personal Computer and Test Equipment

The test equipment required for flatness calibration is given in items 1, and 24 through 28 of the equipment list. Use the following procedure to set up this equipment.

1. Set the base addresses for the two PC2A GPIB boards and install them in the personal computer. (Instructions for setting the base addresses for these boards and installing them in the PC are contained in the instruction manual that comes with the board.)

Each GPIB board must be given a base address, that the software uses to identify the board. The PC2A boards should come with their base address set to 02E1 (hex). Leave one board set at that address, and set the address of the other board to 22E1 (hex). Leave the DMA channel* and interrupt line settings at their defaults. It is helpful to label the GPIB boards with numbers: label the board with base address 02E1 as #0, and label the other board (base address 22E1) #1.

If the personal computer you are using contains other boards that use DMA, such as a network adapter, disable DMA on both GPIB boards. Do this by setting the DMA channel selection jumpers on both boards to NOT USED.

2. Connect 2782, signal generators, and power meter to the computer through GPIB cables, as shown in Figure 3-1.

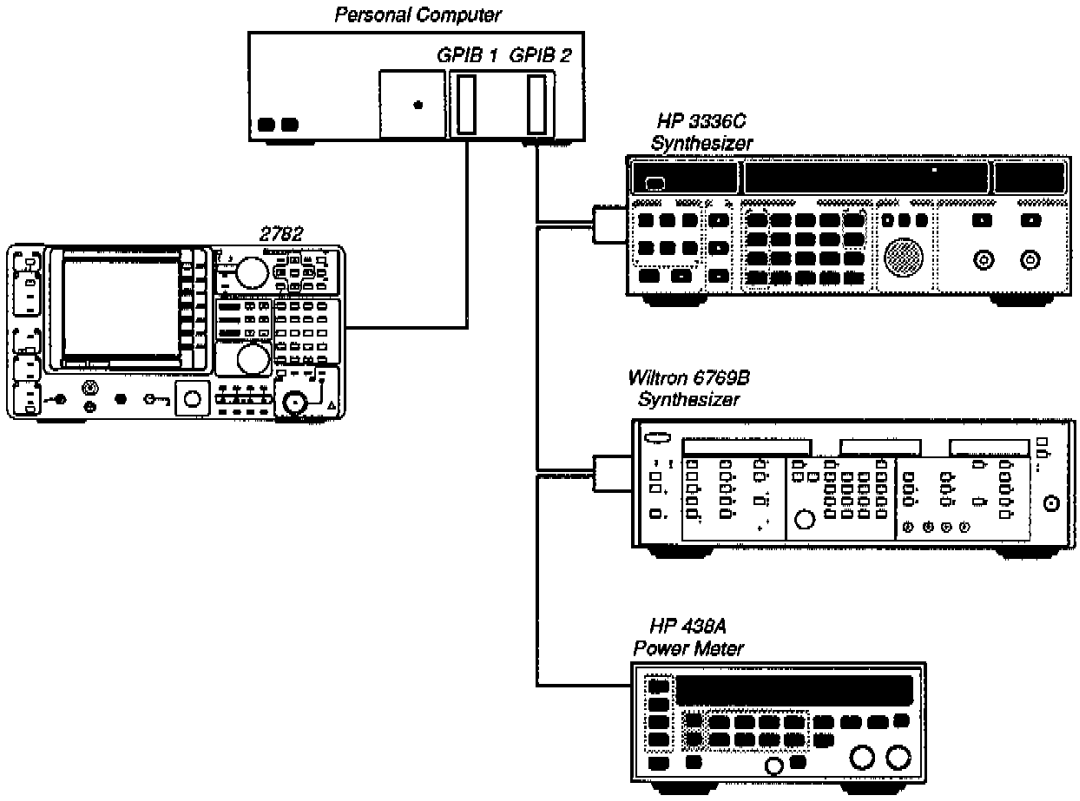


Figure 3-1. GPIB Connections for Flatness Checks.

Connect a GPIB cable from GPIB Port 1 of the 2782 to PC2A board #1. Connect GPIB cables from the generators and power meter to PC2A board #0. If this convention is not followed, the flatness test software will not operate correctly.

3. Power up the 2782 and allow it to warm up for one hour. Power up the signal generators and power meter at the same time.

4. Connect the text-fixture components as shown in Figure 3-2 and connect them to the 2782.

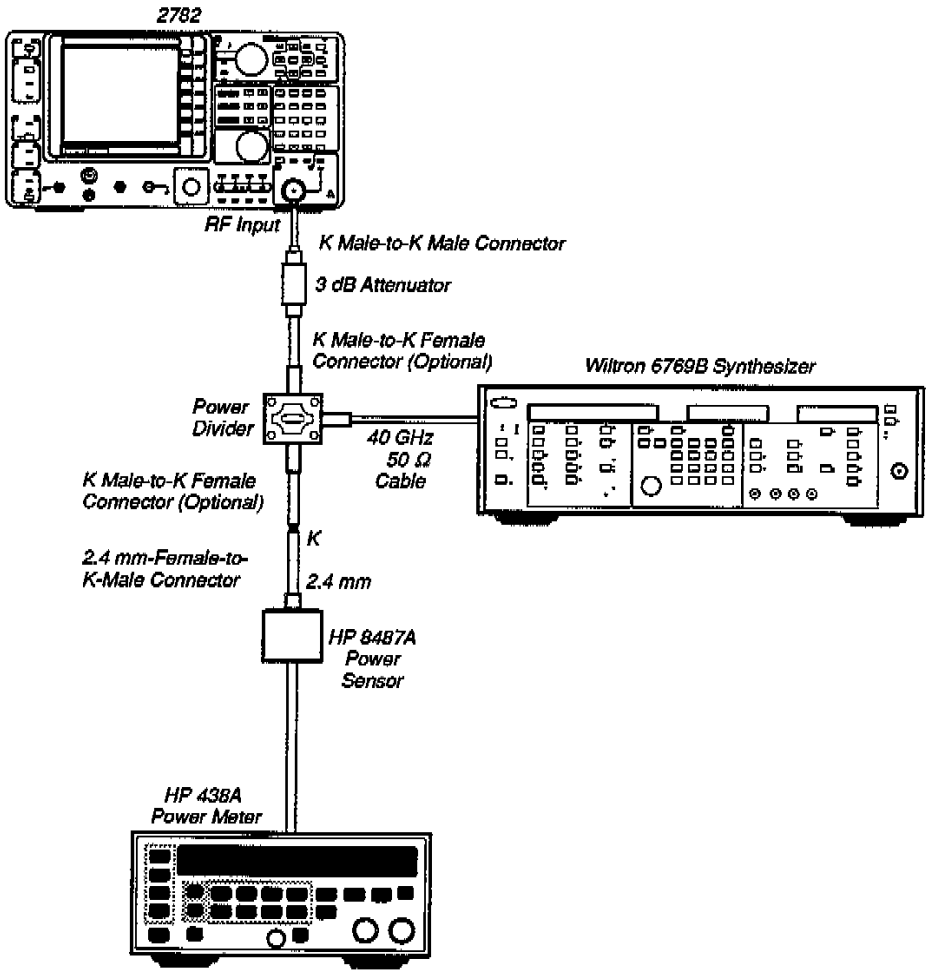


Figure 3-2. Test Fixture Setup for High Frequency Flatness Tests.

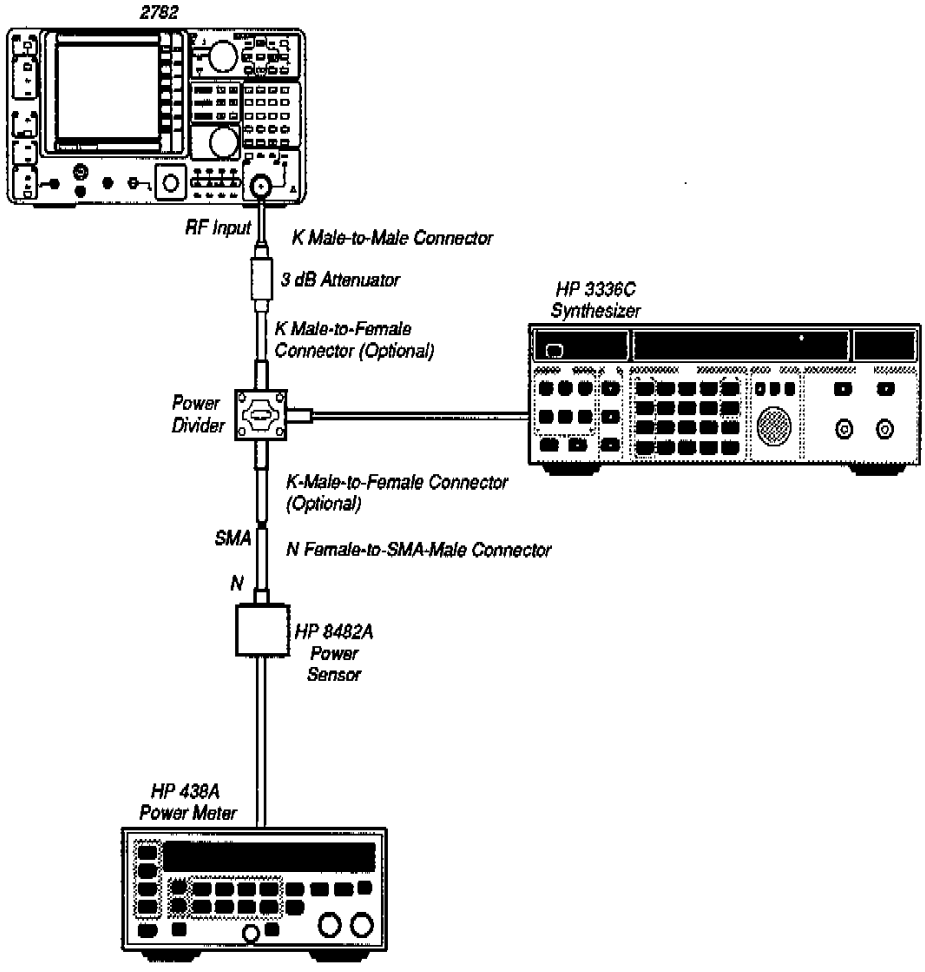


Figure 3-3. Test Fixture Setup for Low Frequency Flatness Tests.

5. Set the GPIB address of the 2782 to 1 as follows. Press the 2782 EXT INTFC CONFIG, and press the Set Port1 Address menu button. Then, enter 1 from the keypad, and press ENTER. A message is then displayed on the crt indicating that the GPIB port address has been reset.

6. Set the clock speed of the personal computer to 6 MHz.

   The 2782 is sensitive to the rate at which it receives data through its GPIB interfaces. When it is receiving a long or repetitive series of commands over the GPIB bus, it may simply quit responding to commands or queries. When this happens, the only way to restore remote control is to cycle the 2782 POWER switch off and on. This problem occurs only when the 2782 is connected to a controller (personal computer) with a very high GPIB data transfer rate (for example, 16 MHz).

The easiest way to prevent this lock up of the 2782 is to slow the clock rate of the PC down to approximately 6 MHz. This is commonly done by setting a switch on the personal-computer mother board or by issuing an MS-DOS command.

On the Tektronix PEP-30x controllers, use the SYSENV command that is supplied with the PC to slow the clock rate. The syntax for this command is `SYSENV 6m`. If the symptom persists, slow the clock rate down again.

NOTE

Slowing the clock rate of the personal computer will not significantly increase the time required to complete the test. This is because the personal computer spends most its time waiting for the 2782 and the test equipment to execute commands.

Running the Equipment Configuration Program (CONFIG.EXE)

The CONFIG.EXE program generates a table that describes the test equipment being used and their respective GPIB addresses. It also creates a data file for each power sensor, containing the calibration factors to be used at each frequency. The calibration factor information comes from the table printed on each sensor.

Enter the following on the personal computer to run CONFIG.EXE:

```
CONFIG <ENTER>
```

NOTE

You must be in the TEKCATS directory to run any of the flatness calibration software.

The program prompts you to enter the GPIB address of each generator and of the power meter. You are also asked for the date that the instrument is due for recalibration and for an identification number that will be used to track the status of the instrument. The ID number can be any unique number (letters are also allowed), such as a calibration number assigned by your calibration laboratory, the last part of the instrument's serial number, or an arbitrary number. Be sure to label the instrument with this number, so that the same number is used every time it is tested.

CONFIG.EXE asks for the same information (except for the GPIB address) for each power sensor, plus the calibration factor table.

If any piece of equipment in the system is past its calibration due date, the UTIL.EXE and CATS.EXE programs will not run. The equipment must then be recalibrated and the CONFIG program rerun, to update the calibration due date. This feature is included meet NBS traceability requirements.

Running the Flatness Utility Program (UTIL.EXE)

The flatness calibration and verification system uses a power splitter and a power meter to compensate for flatness variations in the generators and for losses in the cabling. The CATS.EXE program performs this compensation by

measuring the signal amplitude at the RF Input, comparing it to a reference amplitude, and then using the difference in the two amplitudes to correct the flatness measurement.

For this testing method to work properly, the UTIL.EXE program must be run to characterize the test fixture setups shown in Figure 3-2A and 3-2B.

Enter the following on the personal computer to run UTIL.EXE:

```
UTIL <ENTER>
```

The UTIL.EXE program uses the same operator interface and menu structure as the CATS.EXE program. Refer to the section titled "Performing the Flatness Tests (CATS.EXE)" for information on the operator interface.

The test fixture characterization data that UTIL.EXE collects is stored in a file that CATS.EXE uses.

The power splitter characterization takes about an hour and a half to complete. For traceability reasons, UTIL.EXE must be run whenever the splitter or 3-dB pad are replaced (or even taken apart and put back together). Because of this, it is recommended that you purchase this pair of components specifically for this application and dedicate them to this application.

Additional information on the UTIL.EXE program and the test setup characterization is given in the READ.ME file.

Performing the Flatness Tests (CATS.EXE)

The CATS.EXE program is used both to calibrate the flatness of the 2782 and to verify flatness. Only the flatness calibration portion of this program is used here.

Enter the following on the personal computer to run CATS.EXE:

```
CATS <ENTER>
```

When the CATS program has been loaded, a selection screen is displayed.

NOTE

As describe earlier in this section, the user interfaces for CATS.EXE and UTIL.EXE are similar, so much of the following information also applies to UTIL.EXE.

When the program has been loaded, you are prompted to enter your name. This allows the data files that CATS.EXE generates to be traced to the operator at a later date, if desired.

Next, the current date and time are displayed, and you are prompted to verify that they are correct. If they are not, exit the program (F1,4, <ENTER>), reset the date and/or time as needed, and restart the program.

The CATS program is a menu driven program. Once you have accepted the date and time (pressed <ENTER>), a menu is displayed that allows you to

select the flatness verification tests (QC) or the flatness calibration procedure (CAL). Select 2 and press <ENTER>.

You are then prompted to connect the DUT (Device Under Test -- the 2782 in this case) to the test system and power it up. You should have already carried out this step. If not, perform the steps listed in the previous section titled "Setting Up the Personal Computer and Test Equipment." If the 2782 is already powered up, it is a good idea to re-cycle the power at this time.

Next, you are prompted to enter the 2782's serial number (twice).

The next menu to be displayed allows you to choose how tests are to be performed. This menu provides three selections:

1) RUN FULL SEQUENCE	Every test in the testing sequence is run, in order.
2) RUN PARTIAL SEQUENCE	Selects a second menu that allows you to select a starting point in the testing sequence. The program then runs every test from that point to the end of the sequence.
3) SELECT TEST(S)	Causes a list of test to be displayed. You can then select specific tests to be run. Multiple tests can be selected by entering a series of numbers separated by commas.

Select 1 and press <ENTER>.

From this point on, CATS.EXE handles the flatness verification automatically. All you have to do is change equipment periodically (as shown in Figures 3-2 and 3-3). CATS.EXE prompts you for these changes.

NOTE

The calibration section of the CATS.EXE program performs two operations: calibrates the preselector tracking and measures uncorrected flatness data. The preselector tracking calibration procedure calculates new slope and offset values for the 2782's preselector tracking DACs. You are then given the option of downloading these new values to the 2782.

The uncorrected flatness measurement procedure measures the frequency response of the 2782 with the instrument's automatic flatness correction circuitry disabled. This uncorrected flatness data is then saved in a table, which you can download to the 2782 using the DOWNLOAD.EXE program.

Pressing the F1 key on the computer allows you to interrupt a test at any time or back up a menu level. When this key is pressed a menu of choices is displayed.

The CATS program also provides on-line help, that can be accessed by pressing the F2 key on the computer.

NOTE

Do not press the help or interrupt keys in the middle of a test unless you really need to. Once a test is interrupted, it cannot be resumed at the point of interruption; instead, it must be restarted.

Additional information about the CATS.EXE program can be found in README.DOC file

Downloading the Uncorrected Flatness Data to the 2782 (DOWNLOAD.EXE).

The DOWNLOAD.EXE program is used to download the uncorrected flatness table created by the CATS.EXE program to the 2782. The 2782 then uses this table to perform automatic gain adjustments. Use the following procedure to run this program.

1. Make sure the GPIB cable is connected between the computer and the 2782.
2. Enter the following command from the personal computer:

   ```
   DOWNLOAD <serial-number> <ENTER>
   ```

   Use the same serial number you used when you ran the flatness tests.

   The downloading process requires about four minutes.

Part II. Preparation for Adjustment Procedure (Except Flatness)

1. Disconnect the power cord.
2. Remove the cabinet. Put the front cover on the instrument and place the instrument on its face. Then, remove the four large screws that secure the rear feet and remove the cabinet. Place the instrument in operating position again and remove the front cover.
3. Remove the processor card-cage cover and the main card-cage cover.
4. Reconnect the power cord. The power supply fan comes on for a few seconds, then stops. This is normal behavior.
5. Press the POWER button. Nothing will happen for approximately 5 seconds, while the internal processor boots itself, then the RF attenuators are set (causing a clicking sound). Let the instrument heat up for at least one hour before continuing with the rest of this procedure.

Caution

Keep adequate air flowing through the instrument while letting it warm up by placing a piece of paper over the card cages to act as a temporary cover.

Adjustment Procedure

1. Power Supply Voltage Adjustment

1. Press the PRESET button to place the instrument settings for the factory preset state.

2. Press the SINGLE SWEEP button.

3. Using the digital voltmeter, measure the voltage between the +5VD test point on the mother board (shown in Figure 3-4) and chassis ground. The voltage should be +5 V ±0.01 V. If the voltage is not within tolerance, adjust the +5VD adjustment (also shown on Figure 3-4). Note that the fan speed changes slightly when making this adjustment, which is normal.

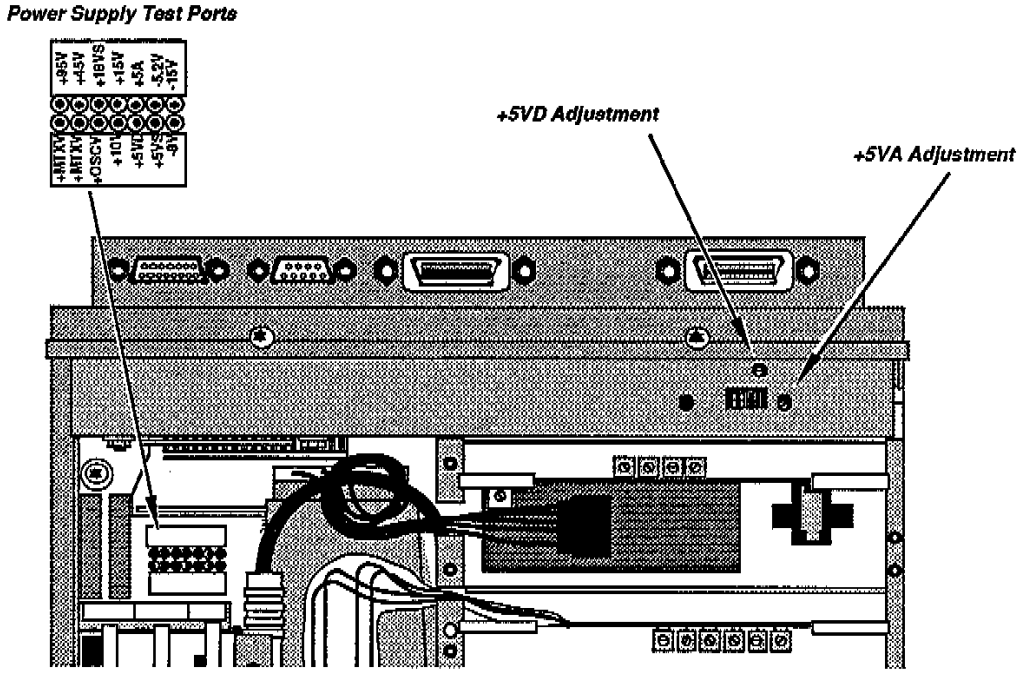


Figure 3-4. +5VD and +5VA Adjustment and Power Supply Test Points.

4. Next, measure the voltage between the +5VA test point on the mother board (also shown in Figure 3-4) and chassis ground. This voltage should also be

+5 V ±0.01 V. If the voltage is not within tolerance, adjust the +5VA adjustment (shown on Figure 3-4).

5. Repeat steps 3 and 4 until both the +5 VD and +5 VA voltages levels are within tolerance.

2. Power Supply Voltage Check

1. Connect the digital voltmeter to the voltage test points given in Table 3-2 (and shown in Figure 3-4) and check that each is within the tolerance range shown below.

Table 3-2. Power Supply Tolerances.

Voltage	Tolerance
+5VD	4.80 V to 5.20 V
+5VA	4.95 V to 5.05 V
+5VS	4.92 V to 5.08 V
+10	9.85 V to 10.15 V
+18	17.1 V to 20.7 V
+15	14.70 V to 15.30 V
+45	42.75 V to 47.75 V
+95	90.25 V to 97.85 V
-5.2	-5.14 V to -5.25 V
-15	-14.70 V to -15.30 V
-8	-7.88 V to -8.12 V

2. Press the 2782 TRIGGER button. Then, push the FREQUENCY button and enter 1 GHz from the keypad, and push the SPAN button and enter 1 GHz from the keypad.

3. Connect the digital voltmeter to the MTXV test point on the mother board (shown in Figure 3-4) and check for approximately +0.5 volts (as given for the MTXV (A) test point in Table 3-3.

4. Press the 2782 FREQUENCY button and enter 7 GHZ via the keypad.

5. With the digital voltmeter still connected to the MTXV test point, check for a voltage within the tolerance given for the MTXV (B) test point in Table 3-3.

Table 3-3. MTXV and OSCV Power Supply Tolerances.

Test Point	Voltage	Tolerance
MTXV (A)	+0.5 V	Approximate
MTXV (B)	+18 V	16.74 V to 19.26 V
MTXV (C)	+26 V	24.18 V to 27.82 V
OSCV	+18 V	16.74 V to 19.26 V

6. Enter 29 GHZ via the keypad.

7. Check for a voltage within the tolerance given for the MTXV (C) test point in Table 3-3.

8. Connect the digital voltmeter to the OSCV test point on the mother board (shown in Figure 3-4) and check for a voltage within the tolerance given for the OSCV test point in Table 3-3.

3. +10 Volt Reference Adjustment

1. Press the SINGLE SWEEP button.

2. Locate the two +10 V test points on the Sweep/Span board (shown in Figure 3-5). One test point provides access to the +10 V reference voltage, and the other test point provides access to a ground for the +10 V supply. This ground test point must be used when adjusting the +10 V reference.

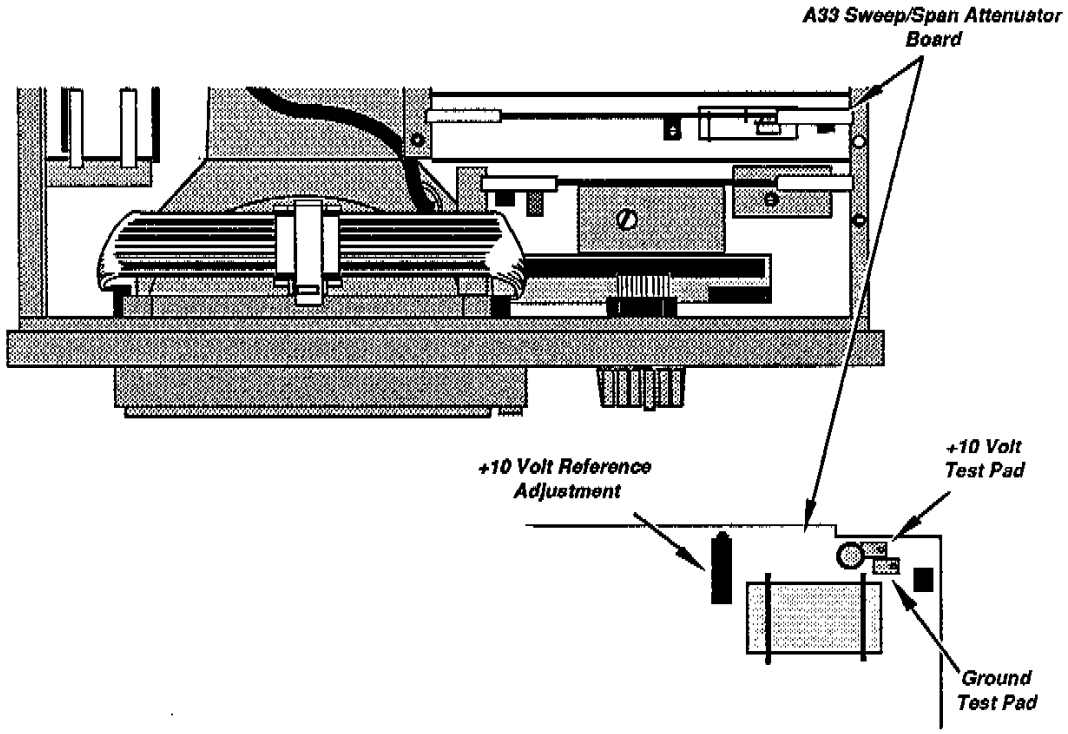


Figure 3-5. +10 Volt Reference Test Points and Adjustment.

3. Touch the ground lead of the digital voltmeter to the +10 V ground test point. Touch the other lead of the meter to the +10 V reference test point.

4. With the digital voltmeter set for the 20 V scale, adjust the +10 Volt Reference adjustment (shown in Figure 3-5) for a reading of 10.00 volts ±0.01 volt.

5. Remove the digital voltmeter leads from the +10 V test points.

6. Press the TRIGGER button to set the instrument back to the continuous-sweep mode.

4. Crt Cut-Off Adjustment

1. A graticule should be displayed on the crt screen. If there is no graticule display, press the PRESET button to reset the instrument to the factory preset settings, which should provide a graticule display.

Caution

In the next step of this procedure, do not remove the high voltage shield to make the CRT CUT-OFF adjustment. An access hole for the adjustment is provided in the shield.

2. Adjust the CRT CUT-OFF adjustment on the high voltage board (shown in Figure 3-6) until the dots that are normally blanked in the crt display are visible. Then, back off on the adjustment until the dots becomes just invisible.

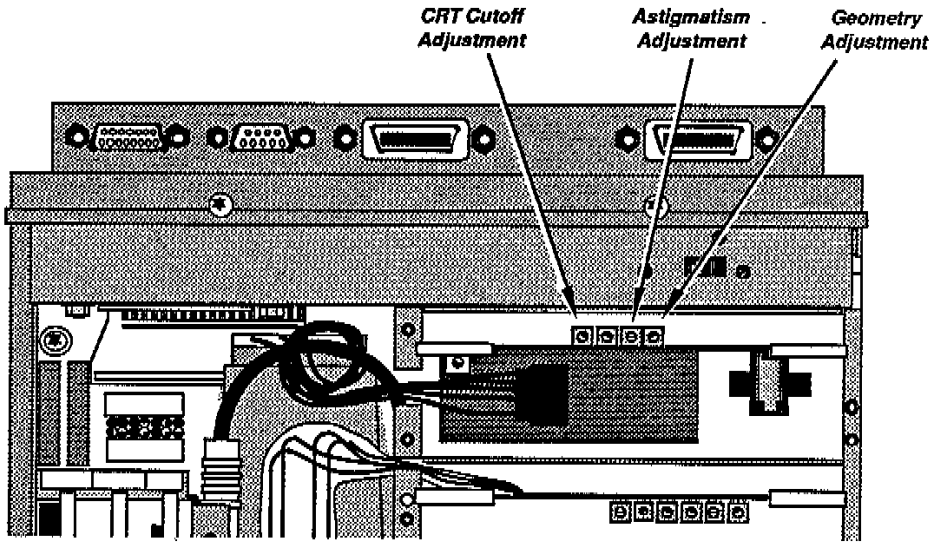


Figure 3-6. High Voltage Module Adjustments.

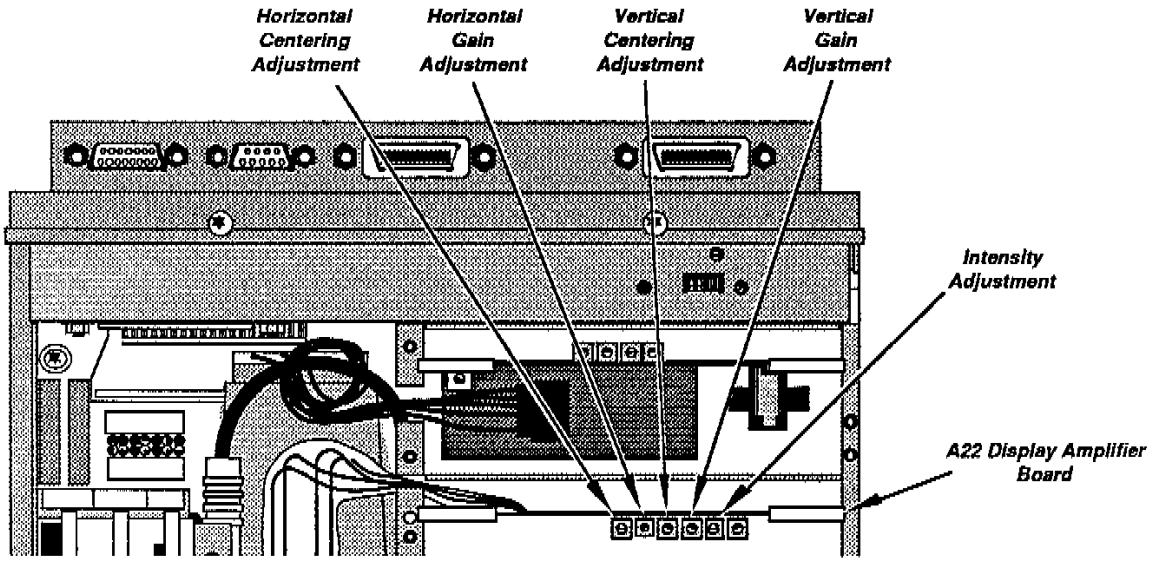


Figure 3-7. Display Amplifier Board Adjustments.

5. Intensity, Focus, and Astigmatism Adjustments

1. Press the DISPLAY button to bring up the Display Menu, and press the CRT Adjust Menu button to select the CRT Adjust Menu.
2. From the CRT ADJUST Menu, press the Set Brightness button.
3. Adjust Knob 2 on the instrument front panel to increase the brightness of the display until there is no further change in display brightness (that is, until maximum display brightness is obtained). Press the ENTER button to save this maximum brightness setting.
4. From the CRT ADJUST Menu, press the Set Focus button.
5. Turn Knob 2 clockwise, until there is no further change in display focus.
6. Adjust the INT adjustment on the Display Amplifier board (shown in Figure 3-7) until there is no degradation of character continuity (that is, until there are no tails or broken segments). This setting constitutes the maximum intensity level that can be set from the front panel.

Caution

In the next step of this procedure, do not remove the high voltage shield to make the ASTIGMATISM adjustment. An access hole for the adjustment is provided in the shield.

7. Alternately, adjust Knob 2 (set for focus) and the ASTIGMATISM adjustment on the high voltage module (shown in Figure 3-7) for optimum spot roundness on the crt display. Press the ENTER button to save this setting.
8. From the CRT ADJUST Menu, press the Set Brightness button.
9. Adjust Knob 2 for the desired brightness. Press the ENTER button to save the brightness setting.
10. From the CRT ADJUST Menu, press the Set Focus button.
11. Adjust Knob 2 for optimum focus. Press the ENTER button to save the focus setting.
12. Press the front-panel ESC button twice to exit the Display menu.

6. Geometry Adjustment

Caution

In the following procedure, do not remove the high voltage shield to make the GEOMETRY adjustment. An access hole for the adjustment is provided in the shield.

1. Adjust the GEOMETRY adjustment on the high voltage module (shown in Figure 3-6) for optimum orthogonality of the horizontal and vertical graticule lines. This means that both the horizontal and vertical lines should be straight with very little or no bowing.

7. Trace Rotation Adjustment

1. Press the DISPLAY button to bring up the Display Menu, and press the CRT Adjust Menu button to select the CRT Adjust Menu.
2. From the CRT Adjust Menu, press the Set Trace Rot button.
3. Adjust Knob 2 to align the graticule display evenly with the edges of the crt bezel.
4. Press the ENTER button to save the trace-rotation-calibration settings. Then, press the ESC button twice to exit the Display Menu.

Note

If the trace-rotation was considerably out of adjustment, recheck the geometry adjustment in the previous procedure.

8. Vertical Display Gain and Offset Adjustment

1. Press the VIEW button to obtain a display that includes the graticule and the VIEW menu.

2. Adjust the VERTICAL GAIN adjustment (vertical display width) and the VERTICAL CENTERING adjustment (vertical display position) on the display amplifier board (shown in Figure 3-7) for the following two things:

   - So that the top and bottom of the crt display extends just to the top and bottom of the crt screen, without being cut off by the edge of the crt.

   - So that the menu selections on the right side of the crt match up with the menu buttons on the CRT bezel, when viewed from a 30-degree viewing angle.

9. Horizontal Display Gain and Offset Adjustment

1. Adjust the HORIZONTAL GAIN adjustment (horizontal display width) and HORIZONTAL CENTERING adjustment (horizontal display position) on the display amplifier board (shown in Figure 3-7) so that the left and right sides of the crt display extend to within 0.125 inch (3.0 millimeters) of the left and right sides of the crt screen, respectively.

2. Press the ESC button twice to obtain a full-screen graticule, without menu information. Check that the right side of the graticule does not extend beyond the right side of the crt screen. If the graticule runs off the right side of the crt screen, readjust the HORIZONTAL GAIN and HORIZONTAL CENTERING adjustments slightly to center the graticule horizontally on the crt screen.

10. Reference Oscillator Adjustment

Note

The 2782 must have had power applied to it, either in the standby mode (STBY light lit) or the operating mode, for at least one hour before making the following adjustment.

Also, this procedure can be performed with a frequency counter in place of the oscilloscope as describe in the note at the end of this procedure.

1. As shown in Figure 3-8, connect the output of the 2782 REF SIGNAL OUT connector (located on the rear panel of the instrument) through a 50 Ω cable to one of the vertical channel inputs of the test oscilloscope.

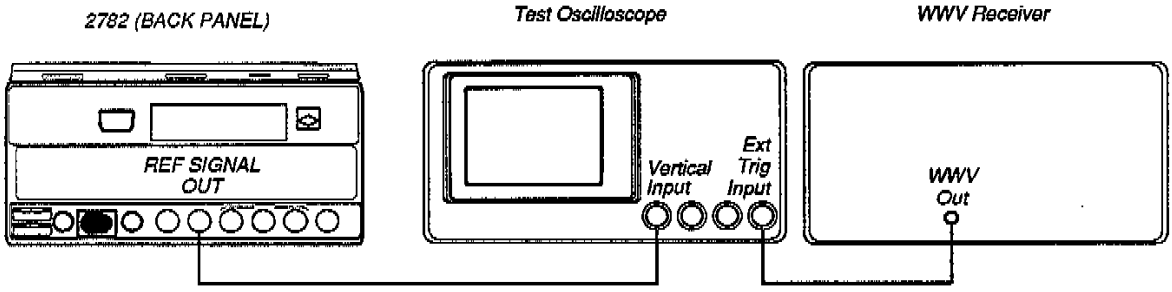


Figure 3-8. Test Equipment Connections for Reference Oscillator Check and Adjustment.

2. Connect the output of the WWV receiver to the external trigger input of the test oscilloscope.

3. Set the oscilloscope triggering for external triggering; the sweep speed for 0.05 microseconds/division; and the vertical gain for 1 volt/division.

4. Press the 2782 PRESET button to select the factory control settings. Then, make the following settings to select the reference frequency for the REF SIGNAL OUT signal.

   - Press the FREQUENCY button to select the FREQ menu.
   - Press the Configure Freq Menu button to select the Config Freq menu.
   - Press the FreqRefOut button to select ON.

5. Observe the waveform on the test oscilloscope and adjust the trigger controls, if needed, for a continuous (unbroken) waveform. The waveform may move across the screen at a slow rate of speed or be stationary.

6. Remove the adjustment protector screw from the reference oscillator container to expose the REFERENCE OSCILLATOR adjustment. This container is located on the Frequency Reference board (shown in Figure 3-9).

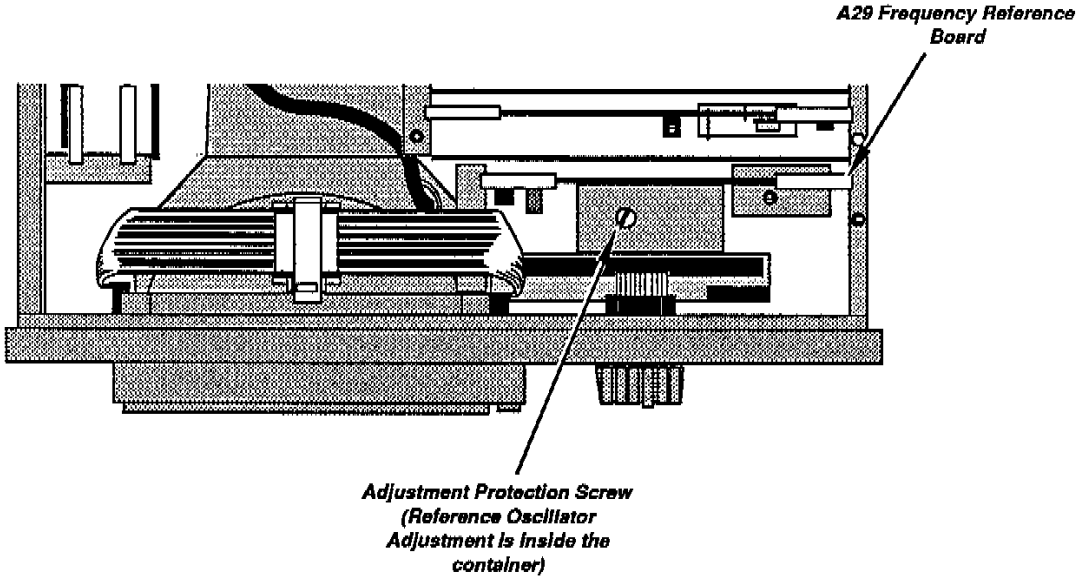


Figure 3-9. Reference Oscillator Adjustment.

7. Adjust the REFERENCE OSCILLATOR adjustment so that the that the waveform on the test oscilloscope is stationary or displays little movement. Replace the protector adjustment screw on the reference oscillator container.

8. Disconnect the cables from the 2782, the test oscilloscope, and the WWV receiver.

Note

Alternate Method

If a frequency counter is available, it can be substituted for the oscilloscope in the above procedure. Here, the 2782 reference signal from the REF SIGNAL OUT connector is connected to the counter's main input channel (generally channel A), and the WWV signal is connected to the counter's reference input. With the same 2782 settings as are described in step 4 above, adjust the REFERENCE OSCILLATOR adjustment for a counted frequency of 10.000 000 MHz.

11. Connecting the 2782 to a Personal Computer

The sweep-timing adjustment (in this section) and the RF attenuator and sweep-offset adjustments (in later sections) require the use of a personal computer, to enter commands to the main processor in the 2782. The personal computer is connected to the 2782 through an RS-232 communication board. Once this board is installed, it can be left in place for the rest of this adjustment procedure, although it is not used again until sections on the RF attenuator and sweep-offset adjustments.

1. Press the POWER button to power down the instrument. Then, disconnect the power cord for the instrument from the power source.

2. Remove the microprocessor board. Insert the processor extender board into the vacant microprocessor slot on the 2782 mother board. Move jumper B24 on the extender board to the upper two pins of B24. (Interrupt select jumper J40 should be on the center and lower pin and J30 should be on pins 1 and 2.)

3. Set the trace-mode DIP switch (switch 3) on the I/O interface board to the closed position.

4. Connect the microprocessor board and the RS-232 board onto the extender board. Connect an RS-232 cable between the RS-232 board and the RS-232 port of the personal computer.

5. Insert the disk containing the Kermit program in the personal computer, and type `KERMIT` <RETURN> on the personal-computer keyboard to load and run Kermit.

6. Reconnect the 2782 to a power source and press the POWER button. If the instrument had been connected to power prior to performing steps 1 through 5, allow the instrument to warm up for five minutes than continue with this procedure. Otherwise, allow the instrument to warm up for at least one hour before continuing.

12. Sweep-Timing Adjustment

Note

For firmware versions 1.3 and above, skip this adjustment. The adjustment is made as part of the frequency calibration operation.

1. Press the UTIL button to display the UTILITY menu, and press the Service Menu button. Then press the EnterKeybd Mode button.

2. Type `scal 1` <RETURN> on the personal-computer keyboard to initiate the automatic sweep-timing calibration routine.

3. Upon completion of the sweep-timing calibration routine, type `fpan` <RETURN> on the personal-computer keyboard.

4. Press the Freq Corr Menu button on the 2782, then press the Store Data button to store the sweep-timing setup data in NVRAM.

Note

If the RF Attenuator Calibration, Sweep Offset (Balance) Adjustment, and Log Corrections procedures (given later in this section) are not going to be performed, the personal computer can be disconnected from the 2782 at this time. The procedure for disconnecting the personal computer is given at the end of this section in the section titled "Disconnecting the Personal Computer from the 2782."

There is some benefit to leaving the personal computer attached for the remainder of the procedures in this section. If the personal computer is attached, the data being collected for the tests that the 2782 performs during its internal calibration routines is displayed on the personal-computer screen. This allows you to monitor the tests directly.

13. Real-Time Brightness and Focus Adjustment

1. Press the PRESET button

2. Press the FREQUENCY button and enter a center frequency of 100 MHz from the keyboard.

3. Press the SPAN button and enter a span of 5 GHz from the keyboard.

4. Press the CONTROL button, then press the Real Time Menu button. From the Real Time menu, press the Real Time button to select ON.

5. Press the Set RT Brightness menu button.

6. Adjust Knob 2 (real-time brightness) for a comfortable brightness level, then press the ENTER button to save the setting in NVRAM.

7. Press the Set RT Focus menu button.

8. Adjust Knob 2 (real-time focus) for a well-defined display, then press the ENTER button to save the setting in NVRAM.

14. Real-Time Clamp Adjustment

1. Observe the clamped portion of the display on the left side of the 2782 crt screen.

2. Adjust the REAL-TIME CLAMP adjustment on the Video Processor board (shown in Figure 3-10), until the left half of the real-time clamped baseline is vertically just below the digitized baseline.

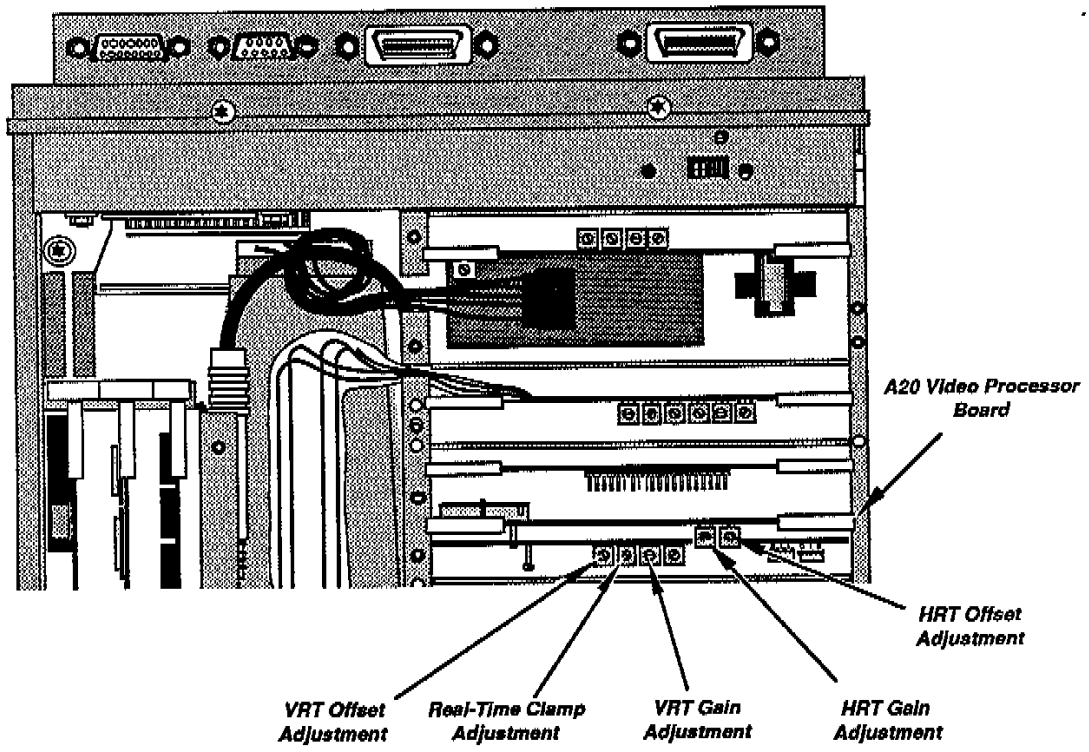


Figure 3-10. Video Processor Board.

15. Real-Time Horizontal Adjustment

1. Press the FREQUENCY button and enter a center frequency of 60 MHz from the keyboard.
2. Press the SPAN button and enter a span of 200 MHz from the keyboard.
3. Press the REF LEVEL button and enter a reference level of -50 dBm from the keyboard.
4. Press the INPUT button, and press the Int Calib on/OFF button to select ON. Then, press the ESC button twice to display the expanded graticule.

5. Alternately adjust the HRTGAIN and HRTOFFSET adjustments on the Video Processor board (shown in Figure 3-10) until the real-time display is positioned horizontally, directly over the digitized display.

16. Real-Time Vertical Adjustment

1. Press the FREQUENCY button and enter a center frequency of 100 MHz from the keyboard.
2. Press the SPAN button and enter a span of 5 MHz from the keyboard. Press the REF LEVEL button and enter a reference level of -20 dBm from the keyboard.
3. Press the RF ATTEN button, then press the Vert Scale menu button. Enter 2 dB from the keyboard.
4. Press the ESC button. An expanded graticule is displayed.
5. Using the REF LEVEL up and down arrows, position the signal near the top of the screen.
6. Alternately adjust the VRTGAIN and VRTOFFSET adjustments on the Video Processor board (shown in Figure 3-10) until the real-time display is positioned vertically, directly over the digitized display.
7. Using the REF LEVEL down arrow, position the signal to one division from the bottom graticule line and repeat step 6.
8. Repeat steps 5 through 7 until real-time display vertically overlaps the digitized display, when the signal is at the top of the screen and one division from the bottom of the screen.
9. Press the CONTROL button, then the Real Time menu button. Press the Real Time menu button of OFF.

17. Sweep Tracking (Balance) Adjustment

This procedure requires that the personal computer be connected to the 2782 through the RS-232 board. If this connection has not already been made, perform the connection procedure given earlier in this section titled "Connecting the 2782 to a Personal Computer."

Note

The 2782 must have had power applied to it, either in the standby mode (STBY light lit) or the operating mode, for at least one hour before making the following adjustment.

1. Press the PRESET button.

2. Press the UTIL button, then press the Service Menu button, followed by the Enter Keyboard Menu button.

3. Type the command prsw <ENTER> from the personal computer keyboard.

4. Connect the digital voltmeter to pin 9 on the 2782 rear panel Accessory Interface port (P10) (as shown in Figure 3-11).

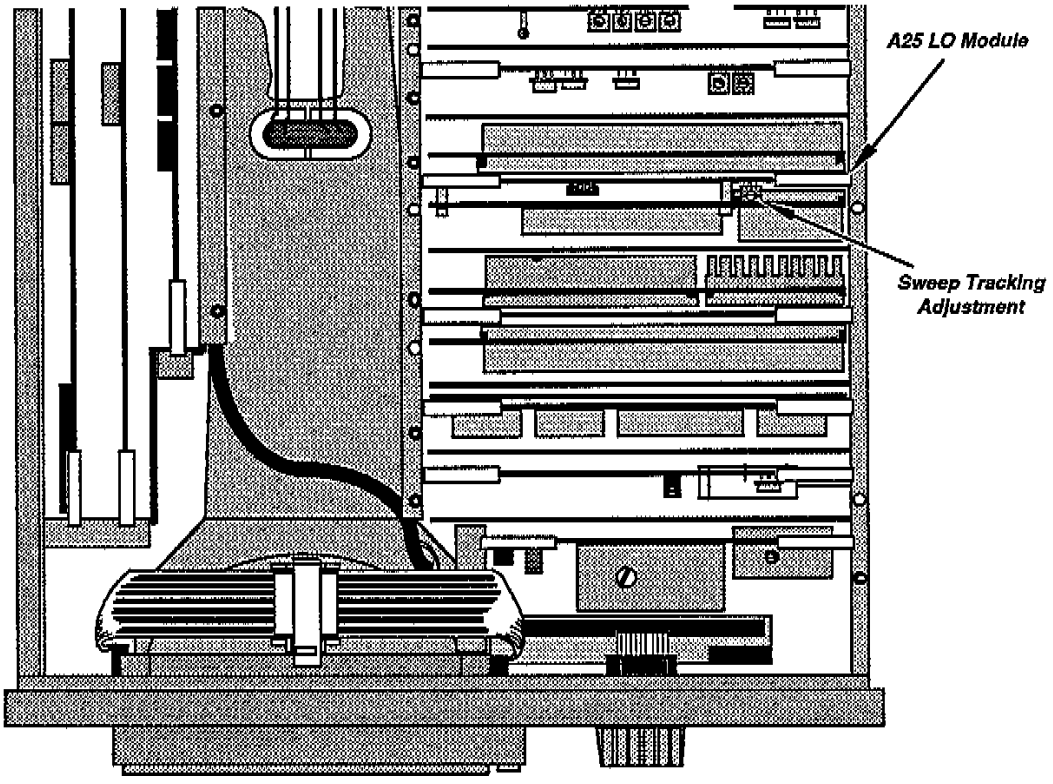


Figure 3-11. Location of Sweep Tracking Balance Test Points and Adjustment.

5. Observe the menu on the computer screen. Type 1 and <ENTER> on the computer keyboard, then wait a few seconds for the step to be completed.

6. Measure the voltage at pin 9 and write down (or otherwise note it).

7. Type 2 and <ENTER> on the computer keyboard, then wait a few seconds for the step to be completed.

8. Adjust the SWEEP TRACKING adjustment located on the LO module (shown in Figure 3-11) so that the voltage measured at pin 9 is the same as was measured in step 6.

9. Repeat steps 5 through 8, until the same voltage is measured at pin 9.

10. Remove the voltmeter from pin 9.

18. Peak Detectors Gain and Offset Adjustment

1. Press the UTIL button, then press the Misc Corr Menu button. From the MISC CORR menu, press the Peak Dtect Menu button

2. Press the Run Corr Cycle button to initiate execution of the automatic peak-detector-correction routine.

3. When execution of the peak-detector-correction routine is complete, press the Store Data menu button. This stores the peak-detector-correction data in the DCAL 2 6 section of the NVRAM calibration data base.

19. Lin Baseline Adjustment

1. Press the PRESET button

2. Press the FREQUENCY button and enter a frequency of 112 MHz from the keyboard. Press the SPAN button and enter a span of 10 MHz from the keyboard.

3. Press the REF LEVEL button, and press the Vert Scale Menu button. Then press the Scale DB/v/w menu button to select the V (voltage) scale.

4. Adjust the LIN OFFSET adjustment on the log processor board (shown in Figure 3-12) so that the lin baseline is just over the bottom graticule line. Do not over adjust.

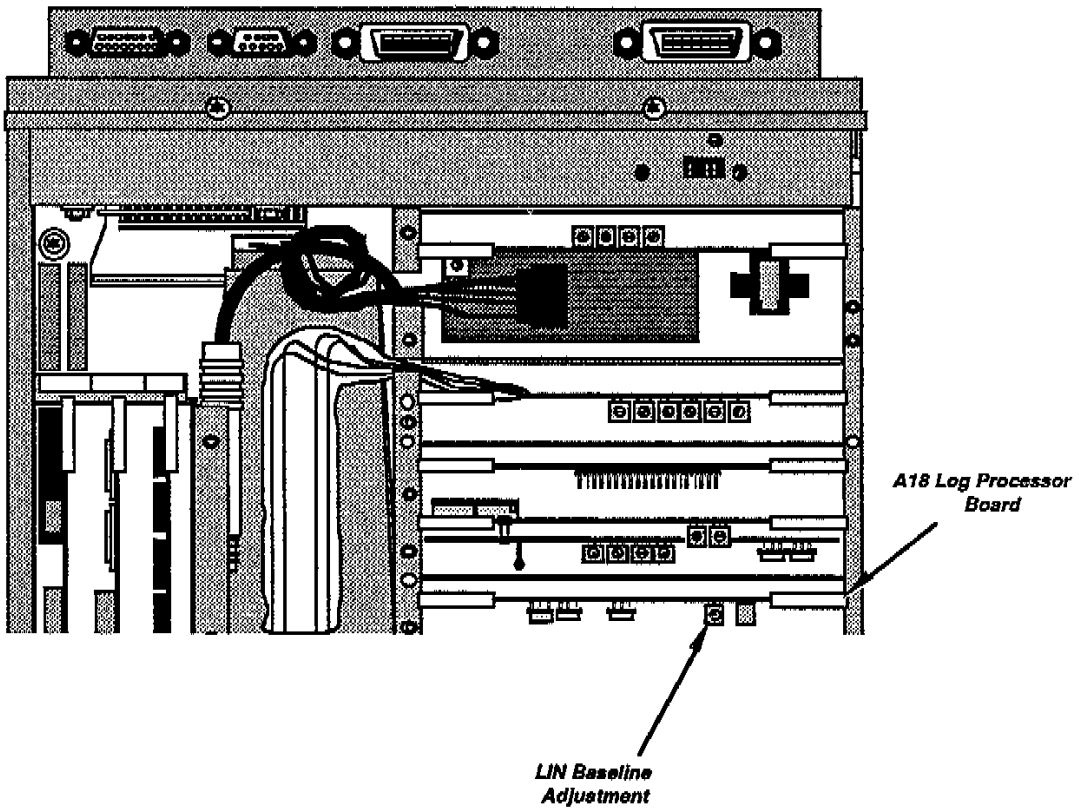


Figure 3-12. Lin Baseline Adjustment.

20. Resonator Tracking Adjustment

1. Press the UTIL button, then press the Vert Corr Menu button. From the Vert Corr menu, press the VR Reson Menu button.

2. Press the Run Corr Cycle menu button to initiate execution of the automatic resonator-tracking-correction routine.

3. When execution of the resonator-tracking-correction routine is complete, press the Store Data menu button. This stores the resonator-tracking-correction data in the DCAL 2 1 section of the NVRAM calibration data base.

21. 100 MHz Calibrator Amplitude Adjustment

1. Press the 2782 INPUT button, and press the RefSig Out single/COMB menu button to select SINGLE.

2. Obtain the Hewlett-Packard HP 432A Power Meter and HP 8484A Power Sensor Head (item 5 of the equipment list), and a 10 dB attenuator.

3. If the power sensor head is not already connected to the power meter, turn off the power meter, connect the power sensor cable and the power sensor head to channel A of the power meter, and turn on the power meter. (The power meter should be turned off when connecting the power sensor head to prevent damage.)

Note

The HP 438A power meter has two input channels (A and B). The HP 8484A power head can be connected to either channel for this performance-verification test.

4. Connect a Hewlett-Packard HP 11708 30 dB attenuator to the POWER REF connector of the power meter.

5. Press the power meter Channel A button (or Channel B if the power head is connected to channel B), and press the ZERO button. (Wait a few seconds for the zeroing routine to complete.)

6. Press the power meter CAL FACTOR button and enter the REF CF% value that is recorded on the 8484A power sensor head from the power meter keypad (for example, 97.0 ENTER).

7. Connect the HP 8484A power sensor head to the HP 11707 30 dB attenuator that is connected to the power meter POWER REF connector (as shown in Figure 3-13A).

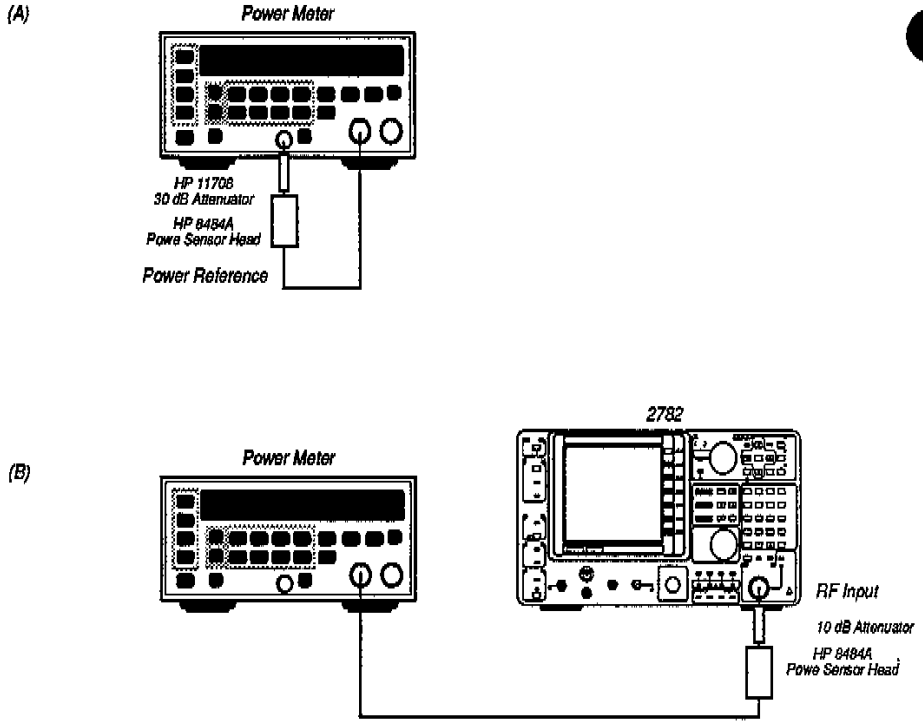


Figure 3-13. Test Equipment Connections for 100 MHz Calibrator Amplitude Adjustment.

8. Press the power meter OSC button, and press the CAL ADJ button. Then, enter the REF CF% value entered in step 6 from the power meter keypad. The power meter should then read -30.00 dBm.

9. Disconnect the 8484A power sensor head from the 30 dB attenuator, and connect a 10 dB N-type attenuator to the power sensor head. Then, connect the power sensor head and 10 dB attenuator back to the 30 dB attenuator connected to the power meter.

10. Press the REL button on the power meter.

11. Disconnect the power sensor head and 10 dB attenuator from the 30 dB attenuator, and reconnect the power sensor head and 10 dB attenuator to the REF SIGNAL OUT connector of the 2782 (as shown in Figure 3-13B).

12. Adjust the 100 MHz AMPLITUDE adjustment on the 100 MHz Calibrator module (shown in Figure 3-14) for -30.0 dBm as measured with the power meter.

13. Disconnect the power sensor head and 10 dB attenuator from the 2782.

14. Press the 2782 INPUT button, and press the RefSig Out SINGLE/comb menu button to select COMB.

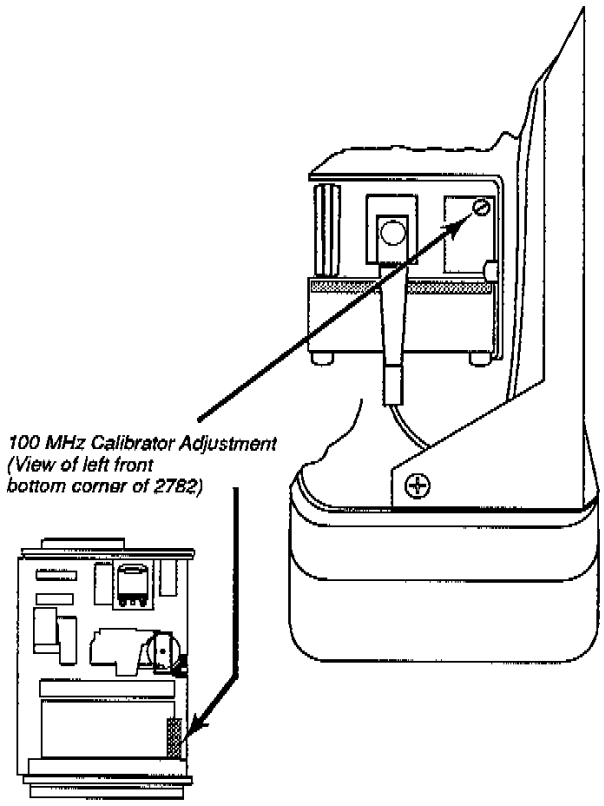


Figure 3-14. 100 MHz Amplitude Adjustment

22. Display Law Adjustment

1. With the 50-ohm cable still connected between the REF SIGNAL OUT and the RF INPUT connectors, press the UTIL button. Then press the Vert Corr Menu button.

2. From the Vert Corr menu, press the Display Law Menu button. Then, press the Run Corr Cycle menu button to initiate execution of the automatic display-law-correction routine.

4. When execution of the display-law-correction routine is complete press the Store Data menu button. This stores the display-law-correction data in the DCAL 2 2 section of the NVRAM calibration data base.

23. RF Attenuator Adjustment

This procedure requires that the personal computer be connected to the 2782 through the RS-232 board. If this connection has not already been made, perform the connection procedure given earlier in this section titled "Connecting the 2782 to a Personal Computer."

1. Connect a signal generator to the RF INPUT connector through the following three attenuators connected in series:

   - a Hewlett-Packard 355C step attenuator
   - a Hewlett-Packard 355D step attenuator
   - two 6 dB fixed attenuators

   Figure 3-15 shows how the connections should be made.

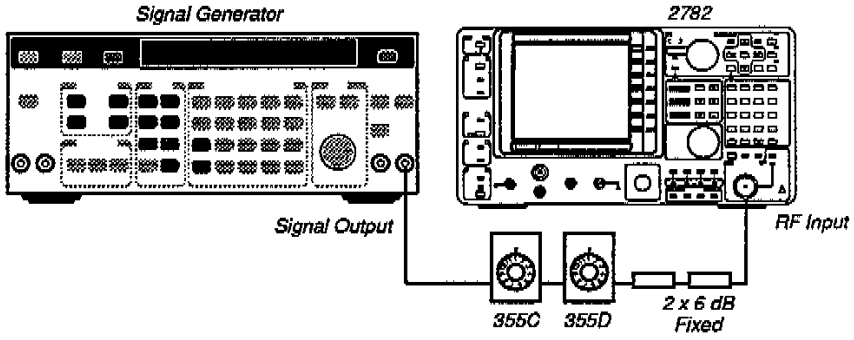


Figure 3-15. Test Equipment Connections for Reference Attenuator Adjustment.

Note

Care should be taken not to disturb any BNC connections during this procedure.

2. The step attenuators should be calibrated to within 0.5 dB on the 10 dB steps and 0.1 dB on the 1 dB steps. Determine the calibration of these attenuators at 100 MHz, and enter it in column 3 of Table 3-4.

Table 3-4. RF Attenuator Calibration Worksheet

			4 = a-x	5 = 4 - 1		7=1-6+5	
1	2	3	4	5	6	7	
Nominal Instr Atten	Nominal External Atten	Actual External Atten	External Atten Delta	External Atten Error	Marker Delta Ampl	Actual Instr Atten	
0	70	(a)	0.00	0.00	0.00	0.00	
10	60	(x)					2nd
20	50	(x)					3rd
30	40	(x)					4th
40	30	(x)					5th
50	20	(x)					6th
60	10	(x)					7th
70	0	(x)					8th

3. Press the PRESET button.

4. Press the FREQUENCY button and enter a center frequency of 100 MHz from the keyboard. Press the SPAN button and enter a span of 2 KHz from the keyboard. Press the ResBW menu button and enter a resolution bandwidth of 100 Hz.

5. Press the grey MRKS button, then press the Peak Find Menu button and the All menu button.

6. Press the Set Peak Height menu button and enter the peak height of 0.1 dB from the keypad.

7. Press the ATTEN button and enter 0 dB from the keypad. (This operation takes the instrument out of the auto mode.)

8. Set the signal generator for a frequency of 100 MHz and a output level of approximately +10 dBm. Set the step attenuator for 70 dB. Then adjust the reference level of the signal generator so that the signal on the 2782 crt screen is within on division of the top of the screen. This is a reference level of approximately -65 dBm.

9. Press the REF LEVEL button. Then press the Vert Scale Menu button and enter 1 dB from the keypad. Press the SPAN button and enter a span of 100 Hz from the keypad. Adjust Knob ?, if necessary to center the signal on the crt screen.

10. Press the STORE button, then, using Knob 1, select a vacant waveform storage register and press the ENTER button to store the waveform. Press the ESC button.

11. Press the RECALL button and use Knob 1 to select the register where the waveform was stored in step 10. Press the ENTER button, then the ESC button.

12. Press the MAX button, followed by the DELTA MKR button, and the MKR➡NXT WF button. The delta marker (colored red) should now be at the peak of the stored waveform, and the main marker (colored yellow) should be at the peak of the active waveform. All the attenuator measurements in the following steps are relative to the stored waveform.

13. Reduce the step attenuator by 10 dB. (Note the total attenuation of the step attenuator.)

14. Type `satt 10` on the computer keyboard to increase the 2782 attenuator by 10 dB.

15. Press the MAX button and record the value of the delta amplitude readout in the second row of column 6 of Table 3-4. The typical value of the delta amplitude is approximately -0.50 dB, and should always be between -1.00 dB and 1.00 dB.

16. Repeat steps 13 through 15 until the external attenuator is at 0 dB. For example, if you reduce the step attenuator by a total of 20 dB, type `satt 20` on the computer keyboard, and so on until you reach a setting of `satt 70`.

17. Compute column 4 of Table 3-4 by subtracting each entry in column 3 from the first entry in that column. The calculation for each row is the amount of external attenuation actually removed for each attenuation step. That is, it is the amount of external attenuation relative to the external attenuators setting of 70 dB.

18. Compute column 5 of Table 3-4 by subtraction the value in column 4 from the value in column 1 for each row. This calculation determines the amount of attenuation error due to the external attenuators.

19. Compute column 5 of Table 3-4 by subtracting the sum of the values in columns 5 and 6 from the value in column 1, for each row. This calculation determines the instrument-attenuation data.

20. Use the `atda` command from the computer keyboard to enter the instrument-attenuation data from column 7 of Table 3-4 into the 2782. The suggested sequence of entry is as follows:

Keyboard command:	`atda`	1	`XX.XX` (from 2nd row in column 7)
Keyboard command:	`atda`	2	`XX.XX` (from 3nd row in column 7)
Keyboard command:	`atda`	3	`XX.XX` (from 4nd row in column 7)
Keyboard command:	`atda`	4	`XX.XX` (from 5nd row in column 7)
Keyboard command:	`atda`	5	`XX.XX` (from 6nd row in column 7)
Keyboard command:	`atda`	6	`XX.XX` (from 7nd row in column 7)
Keyboard command:	`atda`	7	`XX.XX` (from 8nd row in column 7)

For example, if the data for the 30 dB attenuator has an actual value of 29.7, enter the following from the computer keyboard:

```
atda  3  29.7
```

21. Check the table for any data entry errors by typing `dcal 2 5`.

22. Disconnect the attenuators and the signal generator from the 2782.

Note

The personal computer can be disconnected from the 2782 at this time. The procedure for disconnecting the personal computer is given at the end of this section in the section titled "Disconnecting the Personal Computer from the 2782."

24. Horizontal-Frequency Self Calibration

Note

The 2782 must have been operating for at least one hour before making the following adjustment.

1. Press the UTIL button to display the UTILITY menu, and press the FREQ CORR menu button to select the Freq Corr menu.
2. Press the Run Freq Corr Cycle button to initiate the automatic frequency calibration routine. This routine takes approximately 3 minutes to run.
3. Upon completion of the frequency calibration routine, press the Store Data button to store the setup data in NVRAM.

25. Peak Detectors Recalibration

1. Repeat the Peak Detectors Gain and Offset Adjustment (procedure 18 given earlier in this section).

26. Resonator Tracking Recalibration

1. Repeat the Resonator Tracking Adjustment (procedure 20 given earlier in this section).

27. Display Law Recalibration

1. Repeat the Display Law Adjustment (procedure 22 given earlier in this section).

28. Log Corrections Adjustment

1. Connect the signal generator to the RF INPUT connector of the 2782 through a pair of variable step attenuators (10 dB and 1 dB, respectively) and a pair of 6 dB fixed attenuators (as shown in Figure 3-15).

2. Press the UTIL button, then press the Misc Corr Menu button. and then press the Start Log Corr menu. From the Vert Corr menu, press the Start Log Corr menu button.

3. Follow the on screen instructions for the log-correction routine.

4. When execution of the log-correction routine is complete, press the Store Data menu button. This stores the log-correction data in the DCAL 2 2 section of the NVRAM calibration data base.

5. Disconnect the signal generator and attenuators from the 2782.

28. Gain Steps Calibration

1. Press the UTIL button, then press the Vert Corr Menu button. From the Vert Corr menu, press the Gain Step Menu button.

2. Press the Run Corr Cycle menu button to initiate execution of the automatic gain-step-vertical-correction routine.

3. When execution of the gain-step-vertical-correction routine is complete, press the Store Data menu button. This stores the gain-step-vertical-correction data in the DCAL 2 3 section of the NVRAM calibration data base.

29. Resolution Bandwidth Adjustment

1. Press the UTIL button, then press the Vert Corr Menu button. From the Vert Corr menu, press the Res BW Menu button.

2. Press the Run Corr Cycle menu button to initiate execution of the automatic resolution-bandwidth-correction routine.

3. When execution of the resolution-bandwidth-correction routine is complete, press the Store Data menu button. This stores the resolution-bandwidth-correction data in the DCAL 2 4 section of the NVRAM calibration data base.

30. Disconnecting the Personal Computer from the 2782

1. Press the POWER button to power down the instrument. Then, disconnect the power cord for the instrument from the power source.

2. Disconnect an RS-232 cable between the RS-232 board and the RS-232 port of the personal computer. Disconnect the micro-processor board from the extender board. Replace jumper B24 on the extender board.

3. Remove the processor extender board and re-insert the microprocessor board in its slot.

4. Reset switch 3 on the I/O interface board to the open position.

Maintenance

This section describes preventive maintenance procedures, troubleshooting methods, corrective maintenance, and procedures for recalibrating those assemblies that normally do not require routine calibration.

Removing the Instrument from its Cabinet

Prepare the instrument for maintenance or adjustment as follows:

- ❑ 1. Remove the power cord.
- ❑ 2. Install the protective front cover.
- ❑ 3. Set the instrument on a secure surface, face down.
- ❑ 4. Loosen the four slotted captive screws in the rear feet.
- ❑ 5. Remove the rear feet.
- ❑ 6. Remove the case bezel.
- ❑ 7. Pull the cover up and off.
- ❑ 8. Place the instrument on the work bench and reconnect the power cord.

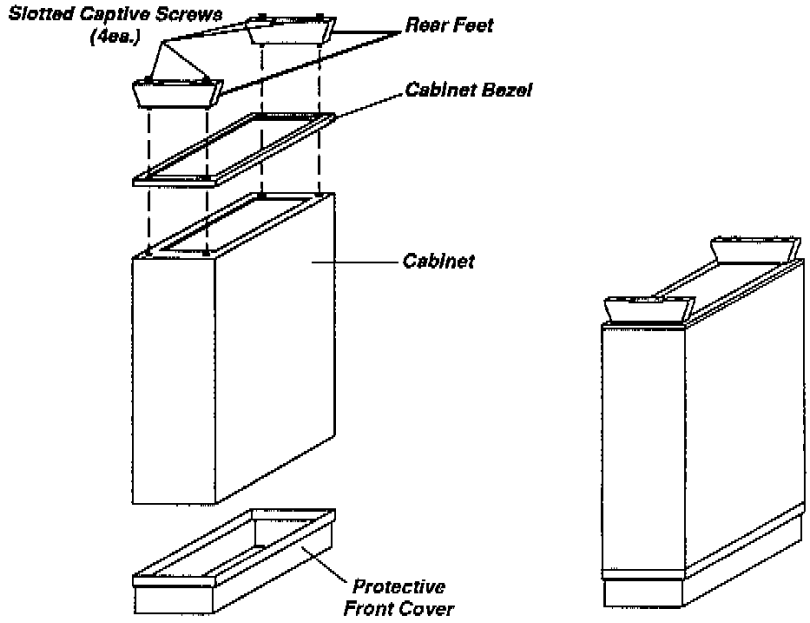


Figure 4-1. Removing the instrument from its cabinet.

Note

If you remove the covers from the top deck, place a sheet of paper over the exposed assemblies to provide proper air flow by the fan.

Static-Sensitive Components

This instrument contains electrical components that can be damaged by static discharge. See Table 4-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV can occur in unprotected environments.

Caution

Static discharge can damage any semiconductor component in this instrument.

Observe the following precautions to avoid damage:

- ❑ 1. Minimize handling of static-sensitive components.
- ❑ 2. Transport and store static-sensitive components or assemblies in their original containers, on metallized or conductive foam. Label packages that contains static-sensitive assemblies or components.
- ❑ 3. Wear a grounded wrist strap while handling these components. Static-sensitive assemblies or components should be handled and serviced only at static-free work stations by qualified service technicians.
- ❑ 4. Keep the workstation surface free of anything capable of generating or holding a static charge.
- ❑ 5. Keep the component leads shorted together whenever possible.
- ❑ 6. Pick up components by the body, never by the leads.
- ❑ 7. Do not slide the components over any surface.
- ❑ 8. Do not handle components in areas that have a floor or work-surface covering that can generate a static charge.
- ❑ 9. Use a soldering iron that is connected to earth ground.
- ❑ 10. Use only special anti-static suction type or wick type desoldering tools.

Table 4-1. Relative Susceptibility to Static Discharge Damage

Relative Semiconductor Classes	Susceptibility	Voltage Levels [a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1	100 to 500 V
ECL	2	200 to 500 V
Schottky signal diodes	3	250 V
Schottky TTL	4	500 V
High-frequency bipolar transistors	5	400 to 600 V
JFET devices	6	600 to 800 V
Linear microcircuits	7	400 to 1000 V (est)
Low-power Schottky TTL	8	900 V
TTL (Least Sensitive)	9	1200 V

[a] Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, performance check, and if needed, recalibration. Establish a preventive maintenance schedule that is based on the environment in which the instrument is operated and the amount of use. Under average conditions (laboratory situation) a preventive maintenance check should be performed every 500 hours of instrument operation.

Cleaning

Clean the instrument often enough to prevent dust or dirt from accumulating in or on it. Accumulation of dirt and grease acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high resistance electrical leakage paths between conductors or components in a humid environment.

Exterior. Clean the dust from the outside of the instrument by wiping or brushing the surface with a soft cloth or small brush. The brush will remove dust from around the front-panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

The crt faceplate is a glass cover over the liquid crystal color shutter. Use a soft, lint-free cloth dampened with a commercial glass cleaner. Do not use an alcohol-based cleaner, because the alcohol can dissolve the glue between the color shutter and the faceplate.

Interior. Clean the interior by loosening accumulated dust with a dry soft brush, then remove the loosened dirt with low pressure air to blow the dust clear. (High velocity air can damage some components.) Hardened dirt or grease may be removed with a cotton tipped applicator dampened with a solution of mild detergent in water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used. If the circuit board assemblies need cleaning, remove the circuit board by referring to the instructions under Corrective Maintenance in this section.

After cleaning, allow the interior to thoroughly dry before applying power to the instrument.

Caution

Do not allow water to get inside any enclosed assembly or components such as the hybrid assemblies, RF Attenuator assembly, potentiometers, etc. Instructions for removing these assemblies are provided in the Corrective Maintenance part of this section. Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone or similar compounds because they may damage the plastic. Do not clean the display with alcohol based cleaners.

Lubrication

This instrument does not require any lubrication.

Maintenance Fixtures and Tools

Table 4-2 lists kits and fixtures that are used in servicing the spectrum analyzer.

Table 4-2. Service Kit and Tools.

Service Kit (See Optional Accessories List in Section 7)
Processor Extender Board with RS232 Cable and adapter
Main Card Cage Extender
Card Cage Extender
Extender Coaxial Cables (for Main Extender)
Extender Cables for Power Supply, VR, and Phase Lock modules
20 dB Coupler, 0.2 to 250 MHz
Tools
Large Slotted Screwdriver - for removing case
Posidrive #1 and #2 Screwdriver
Torx T-10 and T-15 Screwdrivers for removing most assemblies (Minimum 2 inch long, narrow shaft T-10 driver required for VR and 525 MHz IF)
Torque Wrench, 5/16-in open-end for SMA and K connectors
Torque Driver, adjustable, with tips for all screws.
IC Extraction Tool for 40-pin Firmware ROMs
Temperature-Controlled Soldering Iron or Hot Air Soldering Tool for removing batteries

Visual Inspection

After cleaning, carefully check the instrument for such defects as defective connections and damaged parts. If heat-damaged parts are discovered, try to determine the cause of overheating before the damaged part is replaced; otherwise, the damage may be repeated.

Performance Checks and Recalibration

The instrument performance should be checked after each 2000 hours of operation or every 12 months if the instrument is used intermittently to ensure maximum performance and assist in locating defects that may not be apparent during regular operation. Instructions for conducting a performance check are provided by the Performance Check section of the service instructions.

Saving Stored Data in Battery-Backup Memory

If backup-battery power to the memory is interrupted, such as when changing the battery, data stored in that memory will be lost. To avoid this, only replace one battery at a time. Completely remove and replace one battery before removing the second battery.

This data can be down-loaded by a controller using a personal computer program provided on a disk supplied with the service manual.

TROUBLESHOOTING

The spectrum analyzer contains diagnostic firmware that will help find faulty modules. Troubleshooting procedures are provided as part of this section. Also included with this part is a description of the trace modes and their actions. After the defective assembly or component has been located, refer to the Replacing Assemblies and Sub-assemblies part of the Corrective Maintenance information in for removal and replacement instructions.

Troubleshooting Help

Diagrams. Functional block diagrams are located in the Theory of Operation, and an overall block diagram with signal levels is located with the foldout diagrams at the rear of the manual. There are also interconnect diagrams and information for the RF Deck and the Mother Board located at the rear of the manual. Refer to the Replaceable Electrical Parts list section for a description and ordering information of all replaceable assemblies and components.

Note

Corrections to the manual and instrument modifications between printings are documented by inserting correction pages in the Change Information section at the rear of the manual. Check this Change Information section for changes to the manual or the instrument.

Diagnostics. The spectrum analyzer firmware provides diagnostic routines that can be used with the information in this section to troubleshoot problems in some areas of the instrument.

Troubleshooting Steps

❑ 1. Be sure that the problem exists in the spectrum analyzer by checking the operation of associated test equipment. Substitute the analyzer with a similar unit if possible, but first be sure that the input signals are in the range of the analyzer. Don't use too high a power input.

❑ 2. Isolate the problem to a circuit or board level by evaluating operational symptoms; for example, too high an input power can damage the input attenuator and the mixer in the first converter

❑ 3. Run the self correction routines from the Utilities/Service menu. Note any error messages. Consult the operators manual for a complete list of error messages that might appear. This Service manual contains error messages along with troubleshooting information later in this section.

❑ 4. Study the block diagrams and descriptions to help understand the circuit operation.

❑ 5. Before removing any assembly for testing or repairing, refer to the instructions on how to remove or install replaceable assemblies, as provided in the Corrective Maintenance part of this section.

❑ 6. Visually inspect the area or assembly for such defects as broken or loose connections, improperly connected components, overheated or burned components, chafed insulation, etc. Repair or replace all obvious defects. In the case of overheated components, try to determine the cause of the overheated condition and correct before applying power.

❑ 7. Use successive electrical checks to try to locate the problem. A second spectrum analyzer and an oscilloscope are valuable for evaluating circuit performance. If applicable, check the correction adjustments; however, before changing an adjustment note its position so it can be returned to its original setting. This will ease re-correction after the trouble has been located and repaired.

❑ 8. Determine the extent of the repair needed; if complex, we recommend contacting your local Tektronix Field Office or representative. Remember that many assemblies require some re-adjustments using expensive test equipment. If you do not have the required equipment, consider having the repair done by a qualified calibration facility. If only minor repairs are required, see the Replaceable Parts list for replacement information. Removal and replacement procedure of the replaceable assemblies and sub-assemblies are described under Corrective Maintenance.

Caution

When measuring voltages and waveforms, use extreme care with the placement of test probes. Because some circuit boards have a high component density, access to points in some circuits is limited. A test probe could accidentally short a circuit and generate transient voltages that can destroy many components.

Vertical Correction Firmware Diagnostics

This information describes the the procedure for performing the initial vertical corrections for the spectrum analyzer, and contains detailed information on the individual corrections. Its purpose is to help diagnose problems in the vertical correction system.

General Information

RS-232 Interface

The main troubleshooting tool is the RS-232 or keyboard interface. When the keyboard mode is active, the terminal will display the prompt:

```
Enter command:
```

Commands accepted by this prompt are in the form of a four letter command name followed by whatever arguments are appropriate to the particular command. Refer to the Keyboard Command Dictionary, in an appendix to this manual, for details on specific commands.

Correction Data

Three sets of correction data reside in the instrument: generic, default, and current. The generic data is hardwired into ROM and cannot be affected; this data is used primarily as a starting point for the corrections, and is also referred to as factory default data. The default data resides in nonvolatile memory; placing data here is the goal of the vertical correction. The current data is in RAM, and is the data used during normal instrument operation; this data is read from default data on instrument power-up. Unless otherwise noted, all vertical corrections use generic data as their starting point.

Examining Correction Data

Correction data is listed out using the **dcal** keyboard command:

dcal *type id*

The two arguments indicate which set or subset of the data is to be listed, and whether generic, default, or current correction data is desired. The arguments have the following values:

Table 4-3. Data Type arguments for the dcal command.

Data Type	Data Type Listed
0	Generic or Factory Default data
1	Default or Stored data
2	Current data

Table 4-4. Data ID arguments for the dcal command.

Data id	Data Set Listed
0	All correction data
1	VR Resonator Data
2	Display Law Data
3	Gain Step Data
4	ResBW Data
5	Attenuator Data
6	Peak Detector Data
7	Log Curve Correction Data

For example, **`dcal 2 4`** lists the current resolution bandwidth data, and **`dcal 0 1`** lists the generic (factory default) VR resonator data. The first line of all data listings indicates both data type and which set of data is being listed. For example, the first line of the listing generated by **`dcal 0 1`** is:

```
GenericCalData-> vrres_data:
```

while the one for **`dcal 2 4`** is:

```
CurrentCalData-> resbw_data:
```

Refer to the individual correction sections for detailed explanations of the listings.

Storing/Recalling Correction Data

Several commands are provided to store and recall the correction data sets:

Table 4-5. Store and Recall Commands.

Command	Action
`rcgn n`	copies generic data set n into current data
`rcdf n`	copies default or stored data set n into current data
`stcu n`	stores current data set n into default data The value of *n* is from the Data ID table

Trace Mode

A trace mode is provided to print out information over the RS-232 interface during corrections. The trace for the vertical corrections is enabled via the keyboard interface by entering `vtra 1` and disabled by entering `vtra 0`.

A trace is also provided for the reference level gain distribution, which prints out whenever the reference level gain distribution is updated. It is enabled by entering `rtra 1` and disabled by entering `rtra 0`.

Aborting Corrections

Any correction can be aborted by pressing the "ESC" key. However, this can have undesirable side effects. Aborting a correction in firmware versions up to and including 1.2 typically causes sweep problems during subsequent corrections. This can be avoided by briefly turning the instrument off after the abort.

Initial Correction

Full Corrections

This section gives the procedure for performing a full vertical correction. The full correction is required for an instrument that is being turned on for the first time, has had its memory board replaced or erased, or has had so many modules replaced that the existing correction data is totally invalid (see table under Dependencies for details).

The corrections assume that the instrument has been warmed up for at least one hour. Corrections may be run on cold instruments for troubleshooting purposes and to verify functionality, but the resulting data will have reduced accuracy. Final correction should only be done on a fully warmed up instrument, which requires that the instrument be in its case when doing the temperature-sensitive portions of the corrections. The full vertical correction is performed as follows:

- ❑ 1. Install the CPU Extender board in the instrument and start it up. The I/O board switch controlling trace mode should be set to disable the trace; this keeps the frequency and reference level information from obscuring the vertical cal trace information. The I/O board switch controlling service mode should be set to enable service; this allows individual access to all of the correction routines, as well as the keyboard mode.

- ❑ 2. Enter keyboard mode; this is done via the soft key in the UTIL/Service menu.

- ❑ 3. Enter the command `vtra 1` to turn on the vertical cal trace mode. At this point only the vertical correction routines will print trace information.

- ❑ 4. Enter the command `fpan` to return the instrument to normal operation.

- ❑ 5. Enter the UTIL menu and run the correction routines in the following order:

Note

The instrument should be in its case and allowed to reach a stable temperature after the attenuator correction.

Peak Detector Correction
VR Resonator Correction
Display Law Correction
Attenuator Correction
Log Correction
Display Law Correction (again)
Gain Step Correction
VR Resonator Correction (again)
ResBW Correction

As soon as a routine completes without issuing errors, save the resulting data with the appropriate menu soft key. If a correction routine fails, consult the appropriate section below for further information.

❑ 6. Check the instrument performance after the vertical corrections are complete.

Partial Correction

This section gives the sequence for performing a partial vertical correction. This is the sequence to be used for an instrument that does not require new attenuator or log correction data; i.e. – the attenuator, MTX input stage, VR, reference oscillator, and log processor have not changed since the last correction (see table under Dependencies for details). This is also the basic sequence to be used to re-correct the instrument for extreme environmental temperatures.

Note

The instrument must be in its case during this sequence.

The sequence is as follows:

Peak Detector Correction
VR Resonator Correction
Display Law Correction
Gain Step Correction
VR Resonator Correction
ResBW Correction

As soon as a routine completes without issuing errors, save the resulting data with the appropriate menu soft key. If a correction routine fails, consult the appropriate section below for further information.

Dependencies

In general, the correction dependencies follow the sequence given above; i.e. – if a given correction needs to be performed, so do all of the following corrections. The two exceptions to this are the VR Resonator Correction and the Peak Detector

Correction, which are independent of the others and can be performed at any time without affecting other corrections.

The following table gives the corrections required as a result of changes to modules. If a module in the left column is repaired or replaced, all of the corresponding corrections in the right columns must be performed. The generic or factory default data for all of the indicated corrections should be recalled before starting any of the corrections.

Table 4-6. Corrections Required for Replaced Modules.

Changed Module	Required Corrections
Attenuator or Input Connector or MTX input stage	Attenuator Correction Display Law Correction Gain Step Correction VR Resonator Correction ResBW Correction
VR Module	Display Law Correction Gain Step Correction VR Resonator Correction ResBW Correction
Log Processor	Display Law Correction Log Correction Gain Step Correction VR Resonator Correction ResBW Correction
Video Processor	Peak Detector Correction Display Law Correction

Peak Detector Correction

The Video Processor module has four peak detectors that operate as sample and hold detectors. During waveform acquisition, the Video Processor alternates between the different peak detectors, with the specific detectors used depending on the acquisition mode. The purpose of this correction is to adjust the peak detectors so that they all output the same digitized value for the same input signal. The Peak Detector correction takes about 3 minutes to complete.

Instrument Setup

The correction uses the 4 MHz reference oscillator in the VR as a signal source; its height on screen is adjusted using the log offset dac on the Log Processor. This signal appears on the display as zero-span signal, i.e. – a straight horizontal line. The peak detector correction starts out by adjusting the log offset so that the signal is at mid-screen; the trace for this part looks like:

```
PeakDetCorr:
   setup_pkdet_corr: state=1
         Offset_To_Lvl: lvl=950 su  VertScale=10 dB/div
               LogOffset= 0.00 dB  ht= 837 su  err=-113 lsb
               LogOffset=11.30 dB  ht= 951 su  err=   1 lsb
         Offset_To_Lvl: lvl=500 su  VertScale=1 dB/div
               LogOffset=11.30 dB  ht=1023 su  err= 523 lsb
               LogOffset= 6.07 dB  ht=1023 su  err= 523 lsb
               LogOffset= 0.84 dB  ht=1023 su  err= 523 lsb
               LogOffset=-4.39 dB  ht= 624 su  err= 124 lsb
               LogOffset=-5.63 dB  ht= 497 su  err=  -3 lsb
```

The first two lines of the trace indicate that the instrument is being set up for peak detector correction, and will always be the same. Offset_To_Lvl identifies a firmware routine used to adjust log offset until the desired signal level is achieved. lvl=950 su indicates that the desired signal level is 950 screen units (su); these units refer to the 1000 point screen, with 0 su at the bottom and 1000 su at the top of the graticule, and a maximum digitized value of 1023 su. VertScale=10 dB/div indicates that the adjustment is occurring in 10 dB/div. The subsequent lines of the trace are the results of each iteration of the adjustment, giving the log offset in dB (LogOffset= 0.00 dB), the signal height in screen units (ht= 837 su), and the error with respect to the desired level (err=-113 lsb); the error is in screen units and is equal to the desired level minus the current level.

The signal level is first set in 10 dB/div, then in 1 dB/div. Because the peak detector correction is the first correction to be performed, no assumptions can be made concerning the correction of the display law; the two part signal adjustment is therefore used to quickly and reliably adjust the signal level no matter what state of correction the instrument is in.

The following errors can occur during this part of the correction:

```
Signal Offset. Timed Out
Missing 4 MHz VR Reference Signal
```

Signal Offset Timed Out

This error indicates that an attempt to adjust a signal level via the log offset dac has failed. Since this error can also be generated by a missing reference signal, refer to the next section and eliminate this possibility before continuing.

The obvious place to look for problems is in the Log Processor module, i.e. – in the area around the log offset dac. The log offset dac can be checked by selecting a 1 kHz resolution bandwidth, inserting a signal (4 MHz, +10 dBm) into the log amp, and exercising the dac with one of the following keyboard commands:

`offs 1ff`	(loads hex value 1ff into log offset dac)
`lofs 5.0`	(loads dac with value for 5.0 dB of log offset relative to hinge point)
`ofsq`	(prints out current value of log offset dac)

However, the problem is more likely to be due to an unstable or missing signal; i.e. – the signal level jumps around or is so low that the dac has insufficient range for the desired adjustment. If the signal is missing the correction attempts to adjust the noise floor, which moves around from sweep to sweep and is too low to offset to the top of screen (see the following section on Missing 4 MHz VR Reference Signal). Problems in the Video Processor such as a broken filter or especially a broken peak detector will result in an extremely noisy or erratic signal that can not be adjusted.

Missing 4 MHz VR Reference Signal

To check for a missing reference signal, go to keyboard mode and enter the command:

```
vpth 1000
```

This command turns on the 4 MHz reference oscillator in the VR. Connect a spectrum analyzer to the output of the VR and look for a signal at approximately 4 MHz with an amplitude between +15 and +18 dBm (between +9 dBm and +15 dBm for A16 VR versions 644-0631-00 and -01). The VR should be repaired or replaced if a 4 MHz signal with the required amplitude is not present.

Max Peak Detector Correction

Once the signal level has been adjusted, the two max peak detectors are corrected. This is done by selecting max acquisition mode (which alternates between the two max peak detectors) and a 10 msec sweep speed. This sweep speed more or less forces the acquisition to use alternate peak detectors in adjacent bins; a 5 msec sweep would guarantee this, but is too fast for any non-sample acquisition mode. The minimum and maximum signal heights for the 30 bins at the center of the display are noted, and their difference taken to be the max peak detector mismatch; the 30 bin span of this measurement guarantees that both of the max peak detectors are examined. The max peak detector offset dac is adjusted until this mismatch or noise is minimized. The displayed

waveform during this operation will resemble a noisy line (actually a square wave), or possibly a straight line with a series of spikes on it; the amplitude of the noise or spikes correspond to the difference between the two max peak detectors. As the correction proceeds, the amplitude of the noise should decrease until a clean line is obtained.

A two-pass algorithm is used to determine the best dac number. On the first pass the noise height is measured for each 16 lsb dac increment. When a minimum noise height is noted (i.e. – a minimum followed by a 5 lsb increase in the noise amplitude), a second pass is made over the 32 lsb dac range around this minimum; the second pass measures the noise for every dac dac value in this range. The minimum value found in the second pass is the correction value; if multiple minima are found, the first one is used. The trace is as follows:

```
cal max peak detectors:
      pass 1:
            dac=0x00  noise_ht=16 lsb
            dac=0x10  noise_ht=12 lsb
            dac=0x20  noise_ht= 9 lsb
            dac=0x30  noise_ht= 5 lsb
            dac=0x40  noise_ht= 2 lsb
            dac=0x50  noise_ht= 3 lsb
            dac=0x60  noise_ht= 6 lsb
            dac=0x70  noise_ht=10 lsb
      pass 2:
            min_dac=0x30  max_dac=0x50
            dac=0x30  noise_ht= 6 lsb
            dac=0x31  noise_ht= 5 lsb
            ...
            dac=0x3d  noise_ht= 3 lsb
            dac=0x3e  noise_ht= 2 lsb
            dac=0x3f  noise_ht= 2 lsb
            dac=0x40  noise_ht= 2 lsb
            dac=0x41  noise_ht= 2 lsb
            dac=0x42  noise_ht= 2 lsb
            dac=0x43  noise_ht= 1 lsb
            dac=0x44  noise_ht= 1 lsb
            dac=0x45  noise_ht= 1 lsb
            dac=0x46  noise_ht= 2 lsb
            dac=0x47  noise_ht= 2 lsb
            dac=0x48  noise_ht= 1 lsb
            dac=0x49  noise_ht= 2 lsb
            dac=0x4a  noise_ht= 1 lsb
            dac=0x4b  noise_ht= 2 lsb
            dac=0x4c  noise_ht= 2 lsb
            dac=0x4d  noise_ht= 3 lsb
            dac=0x4e  noise_ht= 2 lsb
            dac=0x4f  noise_ht= 3 lsb
            dac=0x50  noise_ht= 3 lsb
      final dac=0x43  min_ht=1 lsb
```

The trace indicates the dac value, in this case the max offset dac, and the corresponding noise height or peak detector mismatch in screen units. The 0x prefix on the dac values indicates that the value is given in hexadecimal form. When the second pass is finished, the minimum noise height (min_ht=1 lsb) and the corresponding dac value are printed. The minimum noise height should ideally be 0, with typical values of 1-2 lsb; a noise height greater than 3 will

generate a Peak Detector Max Not Corrected error. The correction will not terminate due to this error, but will proceed to min peak detector correction.

The following error can occur during this part of the correction:

```
Peak Detector Max Not Corrected
```

Peak Detector Max Not Corrected

This error indicates that the max peak detectors could not be corrected to within 3 lsb of each other. The problem will nearly always be in the Video Processor module, most likely with the peak detectors. The error indicates that max and min/max acquisition modes are either degraded or unusable. The max peak offset dac, and the corresponding correction data, can be set via the keyboard command:

pkmx 2e (loads max peak offset dac with hex value 2e)

Min Peak Detector Correction

This is identical to the max peak detector correction, except that min acquisition mode and the min offset dac are used for the correction. The trace is as follows:

```
cal min peak detectors:
      pass 1:
            dac=0x00  noise_ht=31 lsb
            ...
            dac=0xb0  noise_ht= 8 lsb
      pass 2:
            min_dac=0x70  max_dac=0x90
            dac=0x70  noise_ht= 6 lsb
            ...
            dac=0x89  noise_ht= 1 lsb
            ...
            dac=0x90  noise_ht= 2 lsb
      final dac=0x89  min_ht=1 lsb
```

The following error can occur during this part of the correction:

```
Peak Detector Min Not Corrected
```

Peak Detector Min Not Corrected

This error indicates that the min peak detectors could not be corrected to within 3 lsb of each other. The problem will nearly always be in the Video Processor module, most likely with the peak detectors. The error indicates that min and min/max acquisition modes are either degraded or unusable. The min peak offset dac, and the corresponding correction data, can be set via the keyboard command:

pkmn 2e (loads min peak offset dac with hex value 2e)

Sample Max Peak Detector Correction

The max peak detectors are used in sample acquisition mode, and require a different correction dac value for this mode of operation. The correction is identical to the max peak detector correction, except that sample mode is used for the correction. The trace is as follows:

```
cal sample max peak detectors:
       pass 1:
              dac=0x00  noise_ht=25 lsb
              ...
              dac=0x90  noise_ht=10 lsb
       pass 2:
              min_dac=0x50  max_dac=0x70
              dac=0x50  noise_ht= 7 lsb
              ...
              dac=0x65  noise_ht= 1 lsb
              ...
              dac=0x70  noise_ht= 3 lsb
       final dac=0x65  min_ht=1 lsb
```

The following error can occur during this part of the correction:

```
Peak Detector Sample Not Corrected
```

Peak Detector Sample Not Corrected

This error indicates that the max peak detectors in sample acquisition mode could not be corrected to within 3 lsb of each other. The problem will nearly always be in the Video Processor module, most likely with the peak detectors. The error indicates that sample acquisition mode is either degraded or unusable. The max peak offset dac, and the corresponding max sample correction data, can be set via the keyboard command:

pkms 2e (loads max peak offset dac - sample mode - with hex value 2e)

Gain and Offset Correction

This correction adjusts the peak gain and peak offset dacs to make the min peak detectors match the max peak detectors. The correction is iterative, alternating between the two dac adjustments until both are corrected.

The peak offset dac is adjusted at center of screen. The signal is moved to this height and swept twice, once in min and once in max acquisition mode; the difference in height between the two sweeps is the mismatch to be corrected.

When the peak offset has been corrected to eliminate this difference, the signal is moved to top of screen where the same correction is performed for the peak gain. Because the offset and gain corrections interact with each other, the correction alternates from one to the other until both are corrected.

The trace is as follows:

```
cal_gain_offs:
   cal offset:
      Offset_To_Lvl: lvl=500 su  VertScale=1 dB/div
         LogOffset=-5.63 dB  ht= 495 su  err=  -5 lsb
         LogOffset=-5.58 dB  ht= 499 su  err=  -1 lsb
      dac=0x80  err=4 lsb
      dac=0x7d  err=3 lsb
      dac=0x7b  err=0 lsb
   cal gain:
      Offset_To_Lvl: lvl=990 su  VertScale=1 dB/div
         LogOffset=-5.58 dB  ht= 499 su  err=-491 lsb
         LogOffset=-0.67 dB  ht= 982 su  err=  -8 lsb
         LogOffset=-0.59 dB  ht= 989 su  err=  -1 lsb
      dac=0x80  err=22 lsb
      dac=0x73  err=20 lsb
      dac=0x67  err=9 lsb
      dac=0x62  err=4 lsb
      dac=0x5f  err=2 lsb
      dac=0x5e  err=1 lsb
      dac=0x5d  err=1 lsb
      dac=0x5c  err=0 lsb
   cal offset:
      ...
   cal gain:
      ...
   cal offset:
      ...
   cal gain:
      Offset_To_Lvl: lvl=990 su  VertScale=1 dB/div
         LogOffset=-5.61 dB  ht= 501 su  err=-489 lsb
         LogOffset=-0.72 dB  ht= 999 su  err=   9 lsb
         LogOffset=-0.81 dB  ht= 991 su  err=   1 lsb
      dac=0x27  err=1 lsb
      dac=0x26  err=0 lsb
   cal offset:
      Offset_To_Lvl: lvl=500 su  VertScale=1 dB/div
         LogOffset=-0.81 dB  ht= 992 su  err= 492 lsb
         LogOffset=-5.73 dB  ht= 488 su  err= -12 lsb
         LogOffset=-5.61 dB  ht= 501 su  err=   1 lsb
      dac=0xc1  err=0 lsb
setup_pkdet_corr: state=0
```

The Offset_To_Lvl lines are the same as discussed under Instrument Setup. The cal_offset line identifies the peak offset correction, with the subsequent lines of the trace giving the peak offset dac value (dac=0x80) and the difference between the min and max acquisition sweeps (err=4 lsb); the error is equal to the height of the max acquisition minus the height of the min acquisition. The correction will continue for 20 iterations or until the error reaches 0 lsb. A Peak Detector Min-Max Timed Out error is generated if the error cannot be made less than 3 lsb within 20 iterations; this error will cause the correction to terminate. The correction typically takes about 3-10 iterations on the first attempt, and 2-4 iterations on subsequent tries.

The signal is then moved to top of screen and the correction repeated for the peak gain dac. The correction then alternates between gain and offset for 20 iterations or until the initial measured error for either gain or offset is zero. A Peak Detector Min-Max Not Corrected error is generated if the both gain and offset error cannot be made less than 3 lsb within 20 iterations. Typically the error goes to zero in about a dozen iterations.

The above sequence may be be complicated in detail, but is simple in principle. In essence, the correction will attempt to make all gain and offset errors go to 0 lsb, but will accept final errors of 3 lsb or less.

The following errors can occur during this part of the correction:

```
Peak Detector Min-Max Not Corrected
Peak Detector Min-Max Timed Out
Peak Detectors Not Corrected
```

Peak Detector Min-Max Not Corrected

This error indicates that the overall peak gain and offset correction has timed out. The problem is in the Video Processor Module.

Peak Detector Min-Max Timed Out

This error indicates that an individual peak gain or peak offset correction has failed. The problem is in the Video Processor Module; refer to the trace to determine whether the gain or offset dac needs to be fixed. The peak gain and peak offset dacs, and the corresponding correction data, may be manipulated via the following keyboard commands:

`pkof 5d`	(set the peak offset to hex value 5d)
`pkgn 2a`	(set the peak gain to hex value 2a)

Peak Detectors Not Corrected

This is the standard something caused the peak detector correction to fail error message. This message is generated at the end of the correction if anything went wrong; examine the preceding errors in the error log (or in the trace) to determine the specific cause of failure.

Listing Out Peak Detector Correction Data

The peak detector correction data may be listed out and examined via the `dcal 2 6` command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : vtra 1

Enter command : dcal 2 6
CurrentCalData-> pkdet_data:
  gain = 0x26
  offset = 0xbe
  min_offset = 0x8d
  max_offset = 0x47
  min_smpl_offs = 0x80
  max_smpl_offs = 0x6a
```

gain is the peak gain, offset is the peak offset, min_offset is the min offset, max_offset is the max offset, min_smpl_offs is not used and irrelevant, and max_smpl_offs is the max offset used in sample mode.

VR Resonator Correction

The resolution bandwidth filters that use the 4 MHz IF (i.e. – resolution bandwidths less than or equal to 1 MHz) are composed of a series of six individual filters or resonators; alignment of these resonators is critical for dynamic range, filter shape , and center frequency accuracy specs. The 4 MHz IF frequency is achieved by mixing the 25 MHz IF coming into the VR with a 29 MHz LO, whose frequency is adjustable with a tune dac. The six resonators are also individually controlled by tune dacs. The resonator tracking correction aligns the six resonators, sets their center frequencies to 4 MHz, and sets the 29 MHz LO to exactly 29 MHz. The resonator tracking correction takes about 30 seconds to complete.

Setting 29 MHz LO

The 29 MHz tune dac is adjusted until the frequency is within 0.7 Hz of 29 MHz; the dac has 11 bits, with a nominal resolution of 0.5 Hz/lsb. The trace is as follows:

```
VRResonatorCorr:

  set_vcor_stgs:
  set_dacs: td_freq=4000000.00 Hz  lo29_freq=29000000.00 Hz
        setting lo29
        set_lo29_to_freq: tune_freq=29000000.00 Hz
              dac=0x400  freq=29000149.36 Hz  err=149.36 Hz
              dac=0x2d6  freq=29000012.77 Hz  err=12.77 Hz
              dac=0x2bd  freq=29000001.24 Hz  err=1.24 Hz
              dac=0x2bb  freq=29000000.23 Hz  err=0.23 Hz
        lo29_actual=29000000.23 Hz  td_freq=4000000.23 Hz
```

The first four lines of the trace identify specific firmware routines, and are always the same. The set_lo29_to_freq line indicates that the 29 MHz LO is to be set to a specific tune_freq, in this case 29000000.00 Hz.

The subsequent lines give information for each iteration of the 29 MHz LO correction. The dac column indicates the value in the dac, in hexadecimal (the 0x prefix always indicates hex format); freq indicates the measured frequency of the

LO; err is the difference from 29 MHz. After the 29 MHz LO has been corrected, the remaining error is incorporated into the tune dac frequency td_freq; this value is the frequency to which the resonators will be set. The correction times out if the 29 MHz LO is not set in 10 tries or less.

The following errors can occur during this part of the correction:

```
29 MHz LO Set To Limit Value
29 MHz LO Does Not Converge
29 MHz LO Count Terminated
29 MHz LO Count Data Unknown
29 MHz LO Not Set
```

29 MHz LO Set To Limit Value

The 29 MHz LO dac has insufficient range to tune the LO to 29 MHz. This error can also be generated if there are problems counting the LO (see below). The LO frequency can be checked by selecting the 3 MHz resolution bandwidth (to select the 25 MHz log amp), going to keyboard mode and entering the following:

```
vpth 901        (route LO 29 signal to output of VR)
ifen 1          (enable count path through log amp)
log4 1          (select 25 MHz log amp)
lo29 4096       (count LO 29 using period counter)
```

The resulting value should be checked against a good frequency counter hooked up to the output of the VR. The counter should agree with the number resulting from the lo29 4096 command. Note that a discrepancy here could be due to the 2782's 100 MHz reference being off; this possibility should be checked and eliminated before commencing repairs on the VR.

The LO 29 dac can be set by typing in sllo xx, where xx is the dac value in hex. The frequency range of the dac can be checked out by entering the extreme dac values:

```
sllo 0
lo29 4096       (result should be below 29 MHz)
sllo 7ff
lo29 4096       (result should be above 29 MHz)
```

29 MHz LO Does Not Converge

The 29 MHz LO tune dac should be very linear in terms of Hz per lsb. If the 29 MHz LO correction does not converge, this error is generated. The cause is either a bad tune dac (see previous error description for diagnosis) or a problem in the count path (see next error).

29 MHz LO Count Terminated
29 MHz LO Count Data Unknown

29 MHz LO Does Not Converge
29 MHz LO Not Set
29 MHz LO Set To Limit Value

These errors can all be generated if the 29 MHz LO cannot be counted; this can be due to a missing 29 MHz LO signal, or a problem in the count path. The problem is characterized by large frequency errors (of 100 kHz and up) in the err column of the trace. A weak signal will result in smaller errors. The period counter requires that the signal be at least 20 dB above the noise floor for accurate counts; a signal near this 20 dB threshold will have small frequency count errors, which increase for lower signal amplitudes.

To check the 29 MHz LO, set up the instrument as above (3 MHz ResBW, vpth 901) and connect a spectrum analyzer to the output of the VR. A missing 29 MHz signal indicates that the VR needs to be repaired or replaced.

To check the count path, connect the input of the log amp to a signal generator set to 29 MHz. Select a 3 MHz ResBW and switch to keyboard mode. Use the following commands to set up and operate the period counter:

`vpth 901`	(route LO 29 signal to output of VR)
`ifan 1`	(enable count path through log amp)
`log4 1`	(select 25 MHz log amp)
`lo29 4096`	(count LO 29 using period counter)

Adjust the signal generator amplitude and repeat the lo29 4096 command to determine the minimum signal amplitude required for repeatable counts. If this amplitude is below that of the 29 MHz signal coming out of the VR, the problem is not in the VR. To eliminate the log amp, check the IFPC line to the motherboard; this line should have a TTL square wave with a frequency equal to the 29 MHz divided by 1024 (i.e. – about 28.3 kHz). A missing, erratic, or noisy IFPC signal indicates a problem in the log amp, which should be repaired or replaced. A clean IFPC signal indicates a problem in the period counter, which should be repaired or replaced.

Setting Up Crystal Resonator Ringdown

The center frequencies of crystal resonators are determined by ringing down each resonator and counting its resonant frequency. This requires charging up each resonator with energy from a 25 MHz ringdown oscillator in the VR; the signal from this oscillator is mixed down to 4 MHz to provide the actual charging signal. To maximize the energy in the resonators, it is highly desirable to have the charging signal be as close to the nominal 4 MHz resonator frequency as possible; this is done by adjusting the 29 MHz LO until a 4 MHz IF is achieved with the ringdown oscillator turned on. The LO is adjusted until the IF is within 5 Hz of 4 MHz.

The firmware also checks the range of the first crystal tune dac. This range check was used to tailor the correction for a specific VR revision during development. Since all production instruments should have the same VR version, this check is largely irrelevant.

The trace is as follows:

```
set_lo25:
  dac=0x400  freq=3999926.76 Hz  err=-73.24 Hz
  dac=0x492  freq=3999989.01 Hz  err=-10.99 Hz
  dac=0x4a7  freq=3999997.25 Hz  err=-2.75 Hz
setup_rdown_vr:
  chk_td_slope: xlc_mode=0
        max_freq=4000041.50 Hz
        min_freq=3999952.70 Hz
        dac range=88.81 Hz
```

For the set_lo25 part of the trace, dac is the 29 MHz LO tune dac value, freq is the frequency of the resulting 4 MHz IF, and err is the difference between the IF and 4 MHz.

setup_rdn_vr indicates that the VR is being set up for resonator ringdowns. chk_td_slope: xlc_mode=0 identifies the dac range check for the first crystal resonator; min_freq, max_freq, and dac range are the minimum frequency, maximum frequency, and range of the tune dac. The correction times out after 10 tries. Failure of this step will result in the crystal resonators being charged up to a lower level (due to the charging signal being lower on the filter skirts), which may cause the crystal resonator tracking to fail.

The following error can occur during this part of the correction:

```
29 MHz LO Out Of Range
```

29 MHz LO Out Of Range

The 29 MHz LO dac has insufficient range to mix the 25 MHz ringdown oscillator to within 5 Hz of 4 MHz. This error can also be generated if there are problems counting the LO (see below). The LO frequency can be checked by selecting the 1 kHz resolution bandwidth (to select the 4 MHz log amp), going to keyboard mode and enter the following:

```
vpth 532      (turn on 25 MHz signal and mix down to 4 MHz)
ifsn 1        (enable count path through log amp)
log4 0        (select 4 MHz log amp)
eyef 4096     (count 4 MHz IF using period counter)
```

The resulting value should be checked against a good frequency counter hooked up to the output of the VR. The counter should agree with the number resulting from the eyef command. The LO 29 dac can be set by typing in sllo xx, where xx is the dac value in hex. The frequency range of the dac can be checked by entering the extreme dac values:

```
sllo 0
eyef 4096     (result should be below 4 MHz)
sllo 7ff
```

```
eyef 4096      (result should be above 4 MHz)
```

Failure of this check indicates that the frequency of the 25 MHz ringdown oscillator needs to be adjusted; the VR needs to be either adjusted, repaired, or replaced.

25 MHz LO Count
4 MHz IF count bad data
4 MHz Terminated
29 MHz LO Timed Out
25 MHz ringdown oscillator not set
29 MHz LO Out of Range

These errors can all be generated if the 25 MHz ringdown oscillator cannot be counted via the 4 MHz IF; this can be due to a missing 25 MHz signal, or a problem in the count path. It could be due to a missing 29 MHz LO as well, but this problem would have been caught earlier in the correction. The problem is characterized by large frequency errors (of 100 kHz and up) in the err column of the trace; a weak signal will result in smaller errors. The period counter requires that the signal be at least 20 dB above the noise floor for accurate counts; a signal near this 20 dB threshold will have small frequency count errors, which increase for lower signal amplitudes.

To check the 25 MHz ringdown oscillator, set up the instrument as above (1 kHz ResBW, vpth 532) and connect a spectrum analyzer to the output of the VR. A missing 25 MHz signal indicates that the VR needs to be repaired or replaced.

To check count path, connect the input of the log amp to a signal generator set to 4 MHz. Select a 1 kHz ResBW and switch to keyboard mode. Use the following commands to set up and operate the period counter:

```
vpth 532       (route LO 25 signal to output of VR)
ifen 1         (enable count path through log amp)
log4 0         (select 4 MHz log amp)
eyef 4096      (count 4 MHz IF using period counter)
```

Adjust the signal generator amplitude and repeat the eyef 4096 command to determine the minimum signal amplitude required for repeatable counts. If this amplitude is below that of the 4 MHz signal coming out of the VR, the problem is not in the VR. To eliminate the log amp, check the IFPC line to the motherboard; this line should have a TTL square wave with a frequency equal to the 4 MHz IF divided by 256 (i.e. – about 15.6 kHz). A missing, erratic, or noisy IFPC signal indicates a problem in the log amp, which should be repaired or replaced. A clean IFPC signal indicates a problem in the period counter, which should be repaired or replaced.

Crystal Resonator Tracking

Each crystal resonator is adjusted to within 0.7 Hz of 4 MHz; their tune dacs have 8 bits, with a nominal resolution of 0.5 Hz/lsb. The resonators are measured by charging them up with the 25 MHz oscillator and counting the ringdown frequency when the oscillator is turned off. When a signal source is removed from a resonator, the decaying output signal is at the natural frequency of the resonator. To ensure that only a single resonator is counted, the resonator is placed in min bandwidth crystal mode, with the rest set to LC mode; the LC resonators decay fast enough (i.e. – several orders of magnitude faster than the crystals) that their transients will be long gone by the time the period counter is turned on. The correction times out if the resonator is not set in 10 tries or less.

The trace should look like:

```
setting crystal tune_dac 0:
set_xtal_to_freq: tune_freq=4000000.23 Hz
   dac=0x46  freq=3999982.91 Hz  err=-17.32 Hz
   dac=0x6f  freq=3999998.47 Hz  err=-1.76 Hz
   dac=0x73  freq=4000000.31 Hz  err=0.07 Hz
setting crystal tune_dac 1:
set_xtal_to_freq: tune_freq=4000000.23 Hz
   dac=0x46  freq=3999982.61 Hz  err=-17.63 Hz
   dac=0x6f  freq=3999998.78 Hz  err=-1.45 Hz
   dac=0x72  freq=4000000.00 Hz  err=-0.23 Hz
setting crystal tune_dac 2:
   ...
setting crystal tune_dac 3:
   ...
setting crystal tune_dac 4:
   ...
setting crystal tune_dac 5:
set_xtal_to_freq: tune_freq=4000000.23 Hz
   dac=0x46  freq=3999984.44 Hz  err=-15.80 Hz
   dac=0x6b  freq=3999998.17 Hz  err=-2.06 Hz
   dac=0x6f  freq=3999999.39 Hz  err=-0.84 Hz
   dac=0x71  freq=4000000.31 Hz  err=0.07 Hz
```

dac is the tune dac value, freq is the resonator frequency, and err equals freq minus the target frequency tune_freq. Failure to track the crystal resonators results in reduced dynamic range and/or lumpy filter shapes in the narrowest crystal bandwidths (3 Hz and 10 Hz).

The following errors can occur during this part of the correction:

```
Crystal Resonator Set To Limit Value
Ringdown Count Terminated
4 MHz Terminated
Crystal Resonator Timed Out
```

Crystal Resonator Set To Limit Value

This error indicates insufficient dac range for a particular resonator; the dac number in the trace will indicate a value of 0x00 or 0xff. Note the number of the failing resonator(s), i.e the number in the setting crystal tune_dac 3 part of the trace. This error can also be generated if there are problems counting the

ringdown signal (see below). The ringdown frequency can be checked by going to keyboard mode and entering the following:

vset	(Setup instrument for counting ringdown)
minb xx	(Set resonator to min bw mode; see below)
xlcm xx	(Set all other resonators to LC mode)
xfrq	(count ringdown frequency)

The arguments for the minb and xlcm commands are hex numbers to be loaded into the corresponding shift registers on the VR; the values for each resonator are as follows:

Table 4-7. Resonator Command Arguments.

Resonator	minb	xlcm
0 (1st)	01	3e
1	02	3d
2	04	3b
3	08	37
4	10	2f
5 (6th)	20	1f

After the above setup has been entered, repeat the xfrq command several times; the resulting frequencies should be within 0.35 Hz of each other. Variations greater than 1-2 Hz indicate counting problems; see next section. If the frequency counts are consistent, exercise the dac by entering several dac values:

stnd *n xx*	(Set resonator n to hex value xx)
xfrq	**(Count ringdown frequency)**

Try dac numbers of 00 (frequency should be below 4 MHz), ff (frequency should be above 4 MHz), and 80 (frequency should be about midway between other two). If the frequency range of the dac does not straddle 4 MHz, the tune dac needs to be set to center with the hardware adjustments. The above procedure should be performed for each resonator that the firmware cannot correct.

Ringdown Count Terminated
4 MHz Terminated
Crystal Resonator Timed Out
Crystal Resonator Set To Limit Value

These errors can all result from problems counting the ringdown frequency of the resonators. Counting problems are usually characterized by erratic resonator frequencies with large (100 kHz) errors. After noting the number(s) of the failing resonator(s), check out each failing resonator as in the last section by going to keyboard mode and entering the following:

```
vsat          (Setup instrument for counting ringdown)
minb xx       (Set resonator to min bw mode; see above)
xlcm xx       (Set all other resonators to LC mode)
xfrq          (count ringdown frequency)
```

After the above setup has been entered, repeat the xfrq command several times; the resulting frequencies should be within 0.5 Hz of each other. Variations greater than 1-2 Hz indicate counting problems. The count system is checked out as follows:

With the instrument set up as above, check the period counter via:

```
vpth 532      (Turn on ringdown oscillator)
eyef 256      (Count 4 MHz IF)
```

Repeat the eyef 256 command several times; the resulting frequency should be consistent to within 0.5 Hz. If it is not, check the output of the VR with a spectrum analyzer; a 4 MHz signal with an amplitude of -20 dBm or greater should be present. If the signal is low in amplitude (i.e. – -20 dBm or less) or missing, disconnect the VR from the log amp; connect an external signal generator to the input of the log amp (4 MHz, 0 dBm signal) and repeat the eyef 256 command. Inconsistent counts indicate problems in either the log processor and/or period counter. If the counts are consistent, reduce the signal level in 10 dB steps, repeating the eyef 256 at each step; note the signal amplitude at which the counts start varying. This signal level should be about 30 dB above the noise floor of the log amp (log amp noise floor is at -90 dBm); i.e. – good counts should be obtainable for signal levels as low as -70 dBm. Count failure at higher levels indicate a noisy log amp and/or count path.

If the counting system checks out, the problem must be in the VR. With a spectrum analyzer connected to the output of the VR, exercise the ringdown oscillator with the instrument set up as above:

```
vpth 532      (Turn on ringdown oscillator)
vpth 522      (Turn off ringdown oscillator)
```

When the oscillator is on, there should be a strong (-20 dBm or greater) 4 MHz signal present; this signal should disappear when the oscillator is turned off.

Insufficient signal amplitude is most likely due to the ringdown oscillator frequency not lining up with the resonator(s); when this occurs, the oscillator amplitude is attenuated by the resonator skirts. With a spectrum analyzer in count mode and the oscillator turned on, measure the 4 MHz IF; it should be within 5 Hz of 4 MHz. Reconnect the VR to the log amp and count the 4 MHz IF with the eyef 4096 command; the result should match that of the analyzer. If the results do not match, there is a difference between the frequency references in the external analyzer and the analyzer under test that needs to be resolved, since the ringdown oscillator frequency is corrected at the module level using an external reference. If the analyzer under test's period counter and the external analyzer

both agree that the IF is not within 5 Hz of 4 MHz, then the 25 MHz oscillator frequency needs to be checked and readjusted; see above.

If the oscillator frequency and amplitude check out, try looking for anomalies in the ringdown. Connect the output of the VR to a spectrum analyzer set to zero span. Use the xfrq keyboard command to initiate a ringdown. The ringdown curve is captured by operating the external analyzer in single sweep mode; the resulting trace should start above -20 dBm and drop with a clean, straight slope into the noise.

LC Resonator Tracking

Each LC resonator is adjusted to within 500 Hz of 4 MHz; the tune dacs have 8 bits, with a nominal resolution of 315 Hz/lsb. The resonator frequencies are determined by setting each resonator in min bandwidth mode and executing a sweep; the marker is used to determine the resonator frequency. Before the first resonator is measured, the reference level and VR gain are adjusted to position the waveform in the upper half of the screen. The firmware also checks the range of the first LC tune dac. This range check was used to tailor the correction for a specific VR revision during development. The correction times out if the resonator is not set in 10 tries or less.

The trace should look as follows:

```
set_lc_lvl:
  Set_Filter_Rlv:
        Setting 10 dB/div level to 950 su
        pk_y=1004 su  err=  54 lsb
        pk_y= 948 su  err=  -2 lsb
  Set_Filter_Gain:
        Setting 1dB/div level to 800 su
        StepGain=29 dB  pk_y= 412 su  err=-388 lsb
        StepGain=33 dB  pk_y= 854 su  err=  54 lsb
  chk_td_slope: xlc_mode=1
        max_freq=4033400.00 Hz
        min_freq=3962000.00 Hz
        dac range=71400.00 Hz
setting LC tune_dac 0:
set_lc_to_freq: tune_freq=4000000.23 Hz
  dac=0x46  freq=3989000.00 Hz  err=-11000.23 Hz
  dac=0x68  freq=4000200.00 Hz  err=199.77 Hz
setting LC tune_dac 1:
set_lc_to_freq: tune_freq=4000000.23 Hz
  dac=0x46  freq=3990400.00 Hz  err=-9600.23 Hz
  dac=0x64  freq=3999800.00 Hz  err=-200.23 Hz
setting LC tune_dac 2:
  ...
setting LC tune_dac 3:
  ...
setting LC tune_dac 4:
  ...
setting LC tune_dac 5:
set_lc_to_freq: tune_freq=4000000.23 Hz
  dac=0x46  freq=3991600.00 Hz  err=-8400.23 Hz
  dac=0x60  freq=3999400.00 Hz  err=-600.23 Hz
  dac=0x61  freq=3999800.00 Hz  err=-200.23 Hz
```

The dac, freq, and err columns are as described for the crystal resonator trace. chk_td_slope: xlc_mode=1 identifies the dac range check for the first LC resonator; min_freq, max_freq, and dac range are the minimum frequency, maximum frequency, and range of the tune dac. Failure to track the LC resonators results in reduced dynamic range and/or lumpy filter shapes in the narrowest LC bandwidths (10 kHz and 30 kHz).

The following errors can occur during this part of the correction:

```
LC Resonator Set To Limit
LC Resonator Tracking Timed Out
LC Resonator Set To Limit
Signal Level Timed Out
Signal Gain Timed Out
VR Gain Truncated
VR Resonator Internal Self-Corr Failed
```

LC Resonator Set To Limit

This error indicates insufficient dac range; the dac number in the trace will indicate a value of 0x00 or 0xff. This error can also be generated by a missing or noisy signal (see below). Note the number of the failing resonator(s). To exercise the LC tune dacs, select the following instrument settings from the front panel:

Frequency	100 MHz
Internal calibrator	ON
Reference level	-50 dBm
Span	100 kHz
Resolution BW	10 kHz

Go to keyboard mode and enter the following:

minb *xx*	(Set resonator to min bw mode)

Return to front panel and adjust reference level for good waveform in 1 dB/div. Go to keyboard mode and exercise the dac by entering several dac values:

stnd *n xx*	(Set tune dac n to hex value xx)
swep	(Sweep)

Try dac numbers of 00 (signal should move to right), ff (signal should move to left), and 80 (signal should be about midway between other two). If the signal cannot be moved to center of screen, the dac needs to be adjusted via the hardware.

LC Resonator Tracking Timed Out
LC Resonator Set To Limit

These errors can be the result of a missing or erratic signal; If this is the case, the waveform will consist of a noise floor instead of a filter shape; the firmware will find peaks in the noise and attempt to center them. This can be checked out from the instrument front panel by selecting the following settings: Frequency 100 MHz Reference Level -50 dBm Internal calibrator on (under INPUT menu) Decrement the span until a span of 100 kHz is reached. The calibrator signal should be clearly visible and centered. If not, the calibrator and/or frequency control hardware should be checked out.

Signal Level Timed Out

This error indicates an inability to set the signal level for the LC resonator tracking. This error is specific to the use of instrument reference level for setting signal amplitudes. Failure usually indicates faulty correction data for display law, gain step, or log curve correction; these corrections should be performed to correct the problem. Since the reference level is only used for coarse signal adjustment in 10 dB/div, the indicated correction data would have to be grossly incorrect to affect this correction; this could indicate hardware problems in the VR or Log Processor modules.

Signal Gain Timed Out

This error indicates an inability to set the signal level for the LC resonator tracking. This error is specific to the use of VR gain for setting signal amplitudes. The error can be due to hardware problems in the VR 25 MHz gain stages. It can also be caused by incorrect log curve data. Incorrect log data means that the Log Processor has been replaced and the instrument is using data for the old module; this adjustment should always work for generic log data.

VR Gain Truncated

This error indicates an inability to set the signal level for the LC resonator tracking. This error is specific to the use of VR gain for setting signal amplitudes, and indicates that the VR has insufficient gain to achieve the desired signal level. The error is due to either too much or too little gain in the system. Signal levels should be checked through the signal path from the calibrator to the Log Processor to determine which module has the problem; the VR is a likely cause.

VR Resonator Internal Self-Corr Failed

This is the standard something caused the VR resonator correction to fail error message. This message is generated at the end of the correction if anything went wrong; examine the preceding errors in the error log (or in the trace) to determine the specific cause of failure.

Listing Out VR Resonator Correction Data

The VR resonator correction data may be listed out and examined via the dcal 2 6 command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 1
CurrentCalData-> vrres_data:
   lo29 = 0x2ca
   lo25 = 0x48e
   td_tbl =
          0x84          0x6e
          0x7e          0x69
          0x79          0x6a
          0x73          0x65
          0x80          0x65
          0x76          0x67
```

lo29 = 0x2ca is the 29 MHz LO tune dac value; lo25 = 0x48e is the 29 MHz LO tune dac value used during the crystal resonator tracking; td_tbl is the table of tune dac values for the six resonators, with the crystal values in the first column and the LC values in the second column. All values are in hexadecimal.

Automatic Resonator Correction in Narrow Bandwidths

When the instrument is operating in resolution bandwidths of 30 Hz or narrower, a subset of the resonator tracking is automatically performed every 15 minutes for the first two hours of instrument operation. This compensates for the long (2 hour) time required for the resonator tune circuits to warm up and stabilize. The automatic correction is identical to the full resonator tracking except that it terminates after the crystal resonators are tracked; i.e. – it only corrects the 29 MHz LO and the crystal resonators. This subset takes about 10 seconds, and can be disabled by the user.

The automatic correction is performed only if (1) the resolution bandwidth is less than or equal to 30 Hz and (2) the last resonator tracking occurred longer that 15 minutes ago. If a narrow resolution bandwidth is selected for the first time and the resonators have not been tracked in the last 15 minutes, a correction will start as soon as the current sweep has finished.

Attenuator Correction

Although the attenuator module is manufactured to very tight tolerances, impedance mismatch between the attenuator and the First Converter may cause the attenuator steps to have different values when installed in the instrument. Incorrect attenuation values result in incorrect dB/div correction data; this in turn causes the log correction to function improperly. To avoid this problem, the attenuator must be characterized and the resulting data entered into the instrument.

Unlike the other corrections, the attenuator characterization is an entirely manual operation. Care should be taken to avoid mistakes during the characterization

and the subsequent computations. The RF Attenuator Adjustment procedure is located in the Adjustments section of this manual. Perform that procedure to correct the attenuator.

Potential Problems

The following problems may occur during attenuator correction:

Noisy Signal

This is most likely due to bad connections and/or cables in the test setup; check cables and connections. If the the test setup checks out, the problem is due to the instrument noise floor being too high.

Unstable Signal

A signal that is moves in either frequency or amplitude can introduce significant errors into the correction. The problem is either in the test setup (i.e. due to a defective cable or signal generator), or in the instrument; an instability in the instrument could be due to any number problems.

Tables

These tables are provided to aid in computing the attenuator correction values. The first table is a completed example; the second is a blank table intended to be copied and used during the correction.

Table 4-8. Attenuator Correction Table (Example)

Attenuator Correction Table (Example)						
1	2	3	4	5	6	7
Nominal Instr Atten	Nominal External Atten	Actual External Atten	External Atten Delta	External Atten Error	Marker Delta Amplitude	Actual Instr Atten
0	70	70.50	0.00	0.00	0.0	0.0
10	60	60.50	10.00	0.00	-0.1	10.1
20	50	50.50	20.00	0.00	-0.2	20.2
30	40	40.30	30.20	0.20	-0.5	30.3
40	30	30.20	40.30	0.30	-0.7	41.0
50	20	20.10	50.40	0.40	-0.4	50.8
60	10	10.10	60.40	0.40	-0.2	60.6
70	0	0.00	70.50	0.50	-0.2	70.7

Table 4-9. Attenuator Correction Table

Attenuator Correction Table						
1	2	3	4	5	6	7
Nominal Instr Atten	Nominal External Atten	Actual External Atten	External Atten Delta	External Atten Error	Marker Delta Amplitude	Actual Instr Atten
0	70		0.00	0.00	0.0	0.0
10	60					
20	50					
30	40					
40	30					
50	20					
60	10					
70	0	0.00				

Listing Attenuator Correction Data

The attenuator correction data may be listed out and examined via the "dcal 2 5" command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command: vtra 1

Enter command: dcal 2 5
CurrentCalData-> atten_data:
  atten[0]=0.00
  atten[1]=10.26
  atten[2]=20.11
  atten[3]=30.11
  atten[4]=40.07
  atten[5]=50.05
  atten[6]=59.96
  atten[7]=69.
```

The number in the brackets indicates the attenuation index (equal to the nominal attenuation divided by 10), and the number to the right of the "=" is the corresponding attenuation data.

In the above example, "atten[1]=10.26" indicates that the 10 dB attenuator has an actual value of 10.26 dB.

Log Correction

The log transfer curve correction characterizes the non-linearities in the log amplifier module. The resulting data is used to increase the accuracy of marker amplitude measurements and to correct the display law. The correction consists of using a set of external step attenuators to step down the log amp in 1 dB steps. This is performed for both the 4 MHz and 25 MHz IFs. The correction takes about 20 minutes.

Note

The instrument must be in its can for this correction to have accurate results. The RS-232 interface should be used for diagnostic purposes only, since it requires the removal of the instrument can.

Setting Up

The setup is the same as for the attenuator correction, except that the signal generator is set to an amplitude of 0 dBm. The setup is as follows:

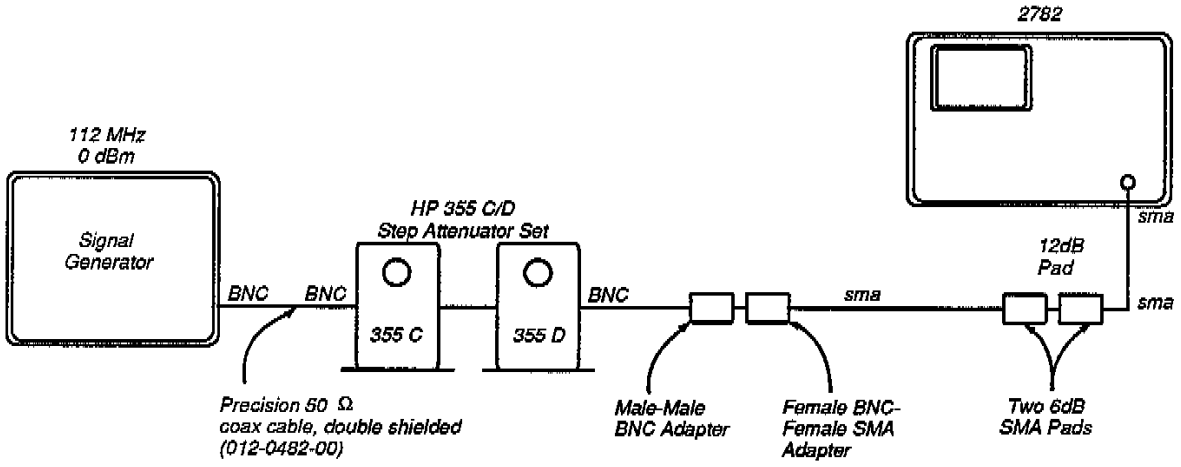


Figure 4-2. Log Correction Equipment Setup.

After both the instrument and signal generator have warmed up, set the 2782 center frequency to 112 MHz and span down on the signal. The signal from the generator should be horizontally centered on screen in a 100 Hz span; adjust the frequency of the signal generator if the signal is not within 10 Hz of center screen.

The instrument display will explicitly indicate settings for both the 10 dB and 1 dB external step attenuators. Whenever a 10 dB step is changed, the step is compared against 10 dB of 1 dB steps, and the VR gain adjusted to account for the difference; this compensates for the fact that the 10 dB steps have looser specifications than the 1 dB steps. The attenuator prompt looks like:

```
Set external attenuator to 10+3=13 dB.
```

The first number (in this case "10") is the setting for the 10 dB step attenuator, while the second number ("3") is the 1 dB step attenuator setting; the last number ("13") is the total value of the external attenuation.

The attenuation settings run from 0 to 85 dB for the 4 MHz log, and 0 to 50 dB for the 25 MHz log. The waveforms should be clean and stable for all attenuator settings except for about the last 10 in the 4 MHz path.

Setting Up the 4 MHz Log Correction

Start the correction by pressing the "RUN" key under the log correction menu; the instrument display will prompt the user to set the external attenuators.

When the attenuators have been set to the indicated values, press the "ENTER" key to continue. At this point the instrument will be set up for the initial measurement. The log offset is set to 0.0 dB (i.e. the top end of the log amp), and the VR gain adjusted until the signal is at the top graticule line in 1 dB/div. The signal for the 4 MHz log is a 100 Hz resolution bandwidth filter in a narrow span; the signal should be clean and stable for most of the log correction. The trace is as follows:

```
setup_lcorr: path=0
        Set_Filter_Lvl: lvl=1000  VertScale=10 dB/div
              su_per_lsb=0.50  max_err=3 su
              c_gain=0x22  f_gain=0x93  err= 100 su
              c_gain=0x24  f_gain=0x80  err= -34 su
              c_gain=0x24  f_gain=0xc0  err=  -3 su
              c_gain=0x24  f_gain=0xc6  err=  -1 su
        Set_Filter_Lvl: lvl=1000  VertScale=1 dB/div
              su_per_lsb=5.00  max_err=4 su
              c_gain=0x24  f_gain=0xab  err=-117 su
              c_gain=0x24  f_gain=0xc0  err= -15 su
              c_gain=0x24  f_gain=0xc3  err=  -1 su
  LogOffset=0.00 (0x1c1)
  gain=0x24 0xc3
```

"Set_Filter_Lvl" identifies the routine that sets signal levels using the VR gain. "lvl" is the desired signal level in screen units, "VertScale" is the current vertical scale, "su_per_lsb" is the resolution of the VR pin gain dac in screen units, and "max_err" is the accuracy (in screen units) to which the routine will set the level. For each iteration, "c_gain" is the bit code for the coarse VR gain steps, "f_gain" is the fine VR gain (i.e. the pin gain dac), and "err" is the measured signal level minus the desired "lvl" value.

Note

Since viewing the trace requires an RS-232 hookup with the instrument can removed, the trace should only be used for diagnosing log correction failures. Normal correction requires that the instrument be in its can.

When the setup is finished, the log offset and final gain is printed out. At this point the display should have the following prompt:

```
Set external attenuator to 00+1= 1 dB.
```

The following errors can occur during this part of the correction:

Signal level too high
Signal Gain Timed Out
VR Gain Truncated

All of the above errors can be generated if the signal level is either too high or missing. An excessively strong signal can cause failure to set signal level during VR gain adjustments; try reducing the signal generator amplitude to -10 dBm. If this results in a weak or noisy signal at the bottom end of the log characterization, the instrument is not meeting its dynamic range specifications; this problem should be pursued and fixed before proceeding.

Log Curve Measurements

Once instrument setup is complete, the user proceeds in a repetitive cycle of waiting for the prompt, setting the attenuator, and pressing "ENTER" for each attenuator setting. The trace for this part of the correction is as follows:

```
LC_Ref=1000  sig_ht=999  LC_Data[0]=-1
LC_Ref=900   sig_ht=908  LC_Data[1]=108
LC_Ref=800   sig_ht=806  LC_Data[2]=206
LC_Ref=700   sig_ht=701  LC_Data[3]=301
LC_Ref=600   sig_ht=600  LC_Data[4]=400
LC_Ref=500   sig_ht=498  LC_Data[5]=498
LC_Ref=400   sig_ht=399  LC_Data[6]=599
LC_Ref=300   sig_ht=307  LC_Data[7]=707
LC_Ref=200   sig_ht=216  LC_Data[8]=816
LC_Ref=100   sig_ht=131  LC_Data[9]=931
```

"LC_Ref" is the reference signal height, i.e. the height for which the signal would have no log ripple; this value decreased by 100 (1 division) for each attenuator increment. "sig_ht" is the actual measured signal height. "LC_Data[]" is a table of log data as a function of attenuation.

The following error can occur during this part of the correction:

Incorrect signal level encountered.

This prompt is displayed if an unexpected signal level is encountered. The instrument checks if the user has correctly set the attenuator, and will prompt the user to correct it if it does not see a 0.5 to 1.5 dB movement for each 1 dB attenuator change. A more subtle problem involves changing the attenuator while the instrument is adjusting the signal level; the attenuator change is absorbed into the adjustment and is not seen, resulting in the attenuator being out of step with the instrument. If this has happened, the correction must be terminated and started over.

This problem can also occur if the signal becomes too noisy, i.e. the noise amplitude is large enough to trip the above check. If this is the case, the instrument noise floor may be higher than expected; try increasing the signal generator amplitude to +10 dBm.
If this results in an excessively strong signal at the top end of the log characterization, the instrument is not meeting its dynamic range specifications; this problem should be pursued and fixed before proceeding.

Screen Offset

When the signal has been decremented to within 1.5 divisions of the bottom of screen, the signal level is adjusted before proceeding to the next measurement. This is done by increasing the log offset until the signal has been increased by an even 8 divisions, i.e to near the top of the display.
The trace for this part of the correction is as follows:

```
moving signal level to 931...
        Set_Filter_Offs: lvl=931 su  VertScale=1 dB/div
              LogOffset= 0.00 dB  ht= 131 su  err=-800 lsb
              LogOffset= 8.00 dB  ht= 939 su  err=   8 lsb
              LogOffset= 7.92 dB  ht= 931 su  err=   0 lsb
  adj sig_ht=931 LogOffset=7.92 (0x289)
LC_Ref=800  sig_ht=839  LC_Data[10]=1039
```

"moving signal level to 931..." indicates where the signal is being moved to. This is followed by the trace for the level-setting routine ("Set_Filter_Offs: lvl=931 su ..."), which gives the log offset ("LogOffset= 0.00 dB"), signal height ("ht=131 su"), and error ("err=-800") for each iteration. When finished, the final signal height ("adj sig_ht=931") and log offset ("LogOffset=7.92 (0x289)") are printed; the number in parenthesis is the value of the log offset dac.

Note

If the step attenuator is inadvertently changed during this part of the correction, the prompts will no longer line up with the attenuator settings. If this happens, the correction must be terminated and started over.

The following error can occur during this part of the correction:

Signal Offset Timed Out

The "Signal Offset Timed Out" error is generated if a noisy signal is present while repositioning the signal via log offset. This problem can arise if the instrument noise floor is higher than expected; try increasing the signal generator amplitude to +10 dBm. If this results in an excessively strong signal at the top end of the log characterization, the instrument is not meeting its dynamic range specifications; this problem should be pursued and fixed before proceeding.

Step Attenuator Compensation

Whenever a 10 dB attenuator step is changed, it is compared with the corresponding 10 dB of 1 dB steps and any discrepancy adjusted out. This compensates for the fact that the specifications on the 10 dB steps of the HP step attenuator set are much looser than those for the 1 dB steps. This is to deal with a worst-case set of attenuators; typically no adjustment is needed.

The firmware makes the measures the log amp as usual, with a typical prompt of:

```
Set external attenuator to 00+10=10 dB.
```

and the corresponding trace:

```
LC_Ref=800  sig_ht=839  LC_Data[10]=1039
```

The signal level is noted (in this case 839), and followed by a prompt to remove 10 dB of 1 dB steps and increase the 10 dB steps by 10 dB:

```
Set external attenuator to 10+0=10 dB.
```

The VR gain is then adjusted to make the signal level the same as that noted for the last step, with the following trace:

```
Set_Filter_Gain:
      Setting 1dB/div level to 839 su
      StepGain=17 dB  pk_y= 836 su  err=  -3 lsb
adj sig_ht=835  gain=0x24 0xc3
```

In this example, no adjustment was needed. The correction then continues:

```
LC_Ref=700  sig_ht=740  LC_Data[11]=1140
LC_Ref=600  sig_ht=635  LC_Data[12]=1235
LC_Ref=500  sig_ht=524  LC_Data[13]=1324
   ...
```

Note

If the attenuator is inadvertently changed during this part of the correction, the prompts will no longer line up with the attenuator settings.If this happens, the correction must be terminated and started over.

The following error can occur during this part of the correction:

Signal Gain Timed Out

This error can be generated if a noisy signal is present during VR gain adjustments. This problem can arise if the instrument noise floor is higher than expected; try increasing the signal generator amplitude to +10 dBm. If this results in an excessively strong signal at the top end of the log characterization, the instrument is not meeting its dynamic range specifications; this problem should be pursued and fixed before proceeding.

Setting Up the 25 MHz Log Correction

This is identical to the 4 MHz correction, except that the measurements are made in zero span with a resolution bandwidth of 3 MHz. All errors and prompts are the same as for the 4 MHz log.

Listing Out Log Correction Data

The log correction data may be listed out and examined via the "`dcal 2 7`" command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 7
CurrentCalData-> lcurv_data:
     LogTbl_4MHz =
       0     9    19    29    39    49    59    69    79    89
      99   109   119   129   139   149   159   169   179   189
     199   209   219   229   239   249   259   269   279   289
     298   308   318   328   338   348   358   368   378   388
     398   408   418   428   438   448   458   468   478   488
     498   508   518   528   538   548   558   568   578   588
     597   607   617   627   637   647   657   667   677   687
     697   707   717   727   737   747   757   767   777   787
     797   807   817   827   837   847   857   867   877   887
     896   906   916   926   936   946   956   966   976   986

   ...

    9999 10009 10019 10029 10039 10049 10059 10069 10079 10089
   10099 10109 10119 10129 10139 10149 10159 10169 10179 10189
   10199 10209 10219 10229 10239 10249 10259 10269 10279 10289
   10299 10309 10319 10329 10339 10349 10359 10369 10379 10389
   10399 10409 10419 10429 10439 10449 10459 10469 10479 10489
   10499 10509 10519 10529 10539 10549 10559 10569 10579 10589
   10599 10609 10619 10629 10639 10649 10659 10669 10679 10689
   10699 10709 10719 10729 10739 10749 10759 10769 10779 10789
   10799 10809 10819 10829 10839 10849 10859 10869 10879 10889
   10899 10909 10919 10929 10939 10949 10959 10969 10979 10989

   10999 11009 11019 11029 11039 11049 11059 11069 11079 11089
   11099 11109 11119 11129 11139 11149 11159 11169 11179 11189
   11199 11209 11219 11229 11239 11249 11259 11269 11279 11289
   11299 11309 11319 11329 11339 11349 11359 11369 11379 11389
   11399 11409 11419 11429 11439 11449 11459 11469 11479 11489
   11499

     LogTbl_25MHz =
       0    10    20    30    40    50    60    70    80    90
     100   110   120   130   140   150   160   170   180   190
     200   210   220   230   240   250   260   270   280   290
     300   310   320   330   340   350   360   370   380   391
     401   411   421   431   441   451   461   471   481   491
     501   511   521   531   541   551   561   571   581   591
     601   611   621   631   641   651   661   671   681   691
     701   711   721   731   741   751   761   771   782   792
     802   812   822   832   842   852   862   872   882   892
     902   912   922   932   942   952   962   972   982   992

   ...

   10999 11009 11019 11029 11039 11049 11059 11069 11079 11089
   11099 11109 11119 11129 11139 11149 11159 11169 11179 11189
   11199 11209 11219 11229 11239 11249 11259 11269 11279 11289
   11299 11309 11319 11329 11339 11349 11359 11369 11379 11389
   11399 11409 11419 11429 11439 11449 11459 11469 11479 11489
   11499
```

The data consists of two 1151-element tables, one for the 4 MHz log and one for the 25 MHz log. Each data table is formatted as a correction table, as opposed to an error table. The table indices correspond to the log amplifier output, while the table values correspond to the corrected log amplifier output. The indices are scaled to a 1000 point, 100 dB log amp, with an index of 0 at the bottom and an index of 1000 at the hinge point (nominally +16 dB into the log amp); the table values follow the same scale, but are multiplied by a factor of 10 to preserve data accuracy.

Only the top 85 dB of the 4 MHz log is characterized; this corresponds to elements 150 to 1000 of the 4 MHz table. Similarly the top 50 dB of the 25 MHz log are characterized and mapped into elements 500 to 1000 of the 25 MHz table. The remaining table elements are generated by creating data corresponding to a straight line between the endpoints of the table and the nearest actual data.

Since the log data tables are large, unwieldy, and difficult to interpret directly, the data should be appropriately scaled and plotted for interpretation. The following program converts the two tables into a set of plot commands for a 4001 X 4001 point plot suitable for use with a Tektronix 4200-series terminal; the code (written in C) is primarily provided to indicate how to generate your own plot utility. A similar function will be provided as part of the instrument QC software.

The resulting plot is overlaid with a 10 X 10 graticule. The horizontal axis is log input, with the top of the log (i.e. +16 dBm) at the left edge and 100 dB down at the right. The vertical axis is the log error, with 0 dB error at center and scaled to 1 dB of error per division. This plot is consistent with the oscilloscope trace produced by the log amplifier test fixture, with the same axis orientation and similar scaling.

```
#define X_SCALE     4   /* 1 for 1000 point x-axis.  */
#define Y_SCALE     4   /* 1 for 1000 point y-axis.  */

main()
{
    long int    err_temp;
    long int    log_in_temp;
    int         log_in[2000];
    int         log_out;
    char        string1[40];
    char        string2[40];


    /* clear header strings */

    scanf("%s %s", string1, string2);/* clear "CurrentCalData-> lcurv_data:'
*/

    scanf("%s %s", string1, string2);/* clear "LogTbl_4MHz = " */
    printf("SGDELETE 3\en");
    printf("SGOPEN 3\en");
    printf("DAVISIBILITY 0\en");
    printf("LINEINDEX 1\en");        /* 4 MHz plotted in red */
    printf("MOVE 0 2000\en");

    for (log_out=0; log_out <= 1150; log_out++)
        scanf ("%d", &(log_in[log_out]));

    for (log_out=1000; log_out >= 0; log_out--)
    {
        err_temp = log_out * 10;
        err_temp -= log_in[log_out];
        err_temp *= Y_SCALE;
        err_temp += 2000;
        log_in_temp = 10000 - log_in[log_out];
        if (log_in_temp < 0)
            log_in_temp = 0;
        log_in_temp *= X_SCALE;
        log_in_temp /= 10;
        printf("DRAW %ld %ld\en", log_in_temp, err_temp);
    }
    printf("SGCLOSE\en\en");

    scanf("%s %s", string1, string2);/* clear "LogTbl_25MHz = " */
    printf("SGDELETE 4\en");
    printf("SGOPEN 4\en");
    printf("DAVISIBILITY 0\en");
    printf("LINEINDEX 3\en");        /* 25 MHz plotted in green */
    printf("MOVE 0 2000\en");

    for (log_out=0; log_out <= 1150; log_out++)
        scanf ("%d", &(log_in[log_out]));

    for (log_out=1000; log_out >= 0; log_out--)
    {
        err_temp = log_out * 10;
        err_temp -= log_in[log_out];
        err_temp *= 4;
        err_temp += 2000;
        log_in_temp = 10000 - log_in[log_out];
        if (log_in_temp < 0)
            log_in_temp = 0;
        log_in_temp *= 4;
        log_in_temp /= 10;
        printf("DRAW %ld %ld\en", log_in_temp, err_temp);
    }
    printf("SGCLOSE\en\en");
}
```

Gain Step Correction

The gain step correction corrects the discrete gain steps used by the reference level firmware; these gain steps are located in the VR and microwave IF modules. The gain step correction assumes that display law and log corrections have been performed. The gain step correction takes about 30 seconds to complete.

The sequence performed by the firmware is as follows:

Microwave IF Gain Step Correction

The microwave IF gain step is a single switchable gain stage in the microwave IF module. The correction of this step consists of measuring its value and storing the result in the gain step data for use by the reference level firmware. The microwave step is set to its high gain position, the log offset is set to 0 dB, and the VR gain adjusted for a top of screen signal in 1 dB/div. The microwave step is then switched off and the change in signal level noted. The trace for this part of the correction is as follows:

```
meas_uwif_step:
      adjusting vr gain...
      LogOffset=0.00
            Gain_To_Lvl: lvl=990  VertScale=10 dB/div
                  su_per_lsb=0.50  max_err=3 su
                  c_gain=0x24  f_gain=0x00  err=-295 su
                  c_gain=0x12  f_gain=0xd5  err=   2 su
            Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
                  su_per_lsb=5.00  max_err=4 su
                  c_gain=0x12  f_gain=0xd5  err= -73 su
                  c_gain=0x12  f_gain=0xd5  err= -73 su
                  c_gain=0x12  f_gain=0xd5  err= -72 su
                  c_gain=0x12  f_gain=0xe3  err=   5 su
                  c_gain=0x12  f_gain=0xe2  err=  -1 su
      top_ht=999 su  bot_ht=547 su  uw_gain=4.52 dB
```

"meas_uwif_step" identifies that the microwave IF step is being measured. "LogOffset=0.00" indicates the log offset during the gain adjustment; this value should always be 0.0 dB. The "Gain_To_Lvl" routine sets the signal level using VR gain (see under **Display Law Correction** for details); The signal is first set to a height of 990 su in 10 dB/div, then to 1000 in 1 dB/div. Once the signal level has been set and the final level noted, the microwave step is turned off; "top_ht" is the signal level with the gain on, "bot_ht" is the signal level with the gain off, and "uw_gain" is the difference in dB.

The following errors can occur during this part of the correction:

Signal Gain Timed Out.
VR Gain Truncated.

See previous section.

Microwave IF Gain Step Out Of Range.

This error indicates that the microwave IF gain step does not meet its EIS specification. The step must have a measured value between 3.0 and 8.0 dB. This error indicates that the instrument may not meet its specifications, but does not cause this correction to abort. The measured value is recorded and used as if they were correct.

VR Output Gain Step Correction

The VR output gain is a set of switchable gain stages with nominal values of 0, 10, and 20 dB. These steps are corrected by measuring their values and storing the results in the gain step data for use by the reference level firmware. The trace for this part of the correction is as follows:

```
meas_vr_out:
      adjusting vr gain...
      LogOffset=0.00
            Gain_To_Lvl: lvl=910  VertScale=10 dB/div
                  su_per_lsb=0.50  max_err=3 su
                  c_gain=0x24  f_gain=0x00  err=-410 su
                  c_gain=0x09  f_gain=0x40  err=  20 su
                  c_gain=0x09  f_gain=0x15  err=  -1 su
            Gain_To_Lvl: lvl=100  VertScale=3 dB/div
                  su_per_lsb=1.67  max_err=3 su
                  c_gain=0x09  f_gain=0x15  err= 591 su
                  c_gain=0x12  f_gain=0x2b  err= -32 su
                  c_gain=0x12  f_gain=0x2b  err= -32 su
                  c_gain=0x12  f_gain=0x3e  err=  -6 su
                  c_gain=0x12  f_gain=0x42  err=   1 su
      top_ht=409 su  bot_ht=101 su  vr_out[1]= 9.24 dB
      top_ht=739 su  bot_ht=101 su  vr_out[2]=19.14 dB
```

"meas_vr_out" identifies that the VR output gain is being measured. The log offset is set to 0 dB ("LogOffset=0.00"), and the signal level adjusted to a height 1 division above the bottom of screen in 3 dB/div; this is done with the VR output gain steps set to 0 dB. The output gain steps are then switched in and the dB value computed from the change in signal level; the 10 dB step is measured first, then the 20 dB step. "top_ht" is the signal level with the step switched in, "bot_ht" is the base signal level with no gain switched in, and "vr_out[]" is the resulting output gain in dB; "vr_out[1]" is the 10 dB step and "vr_out[2]" is the 20 dB step.

The following errors can occur during this part of the correction:

Signal Gain Timed Out.
VR Gain Truncated.

See previous section.

VR Output Gain Out Of Range.

This error indicates that the VR output gain steps do not meet their EIS specifications. The 10 dB step must have a measured value between 8 and 11 dB,

and the 20 dB step must have a measured value between 17 and 21 dB. This error indicates that the instrument may not meet its specifications, but does not cause this correction to abort. The measured value(s) are recorded and used as if they were correct.

1 dB Gain Step Correction

The 1 dB gain steps are a combination of discrete gain steps and a pin dac in the VR. The VR has two discrete gain steps, each with nominal settings of 0, 9, and 18 dB, for a total of 36 dB. There is also an 8-bit pin gain dac with nominal gain values from 0 to 12 dB, in 0.05 dB steps. Each 1 dB gain step is corrected by determining the combination of discrete gain steps (hereafter referred to as "coarse gain") and pin dac value (hereafter referred to as "fine gain") that most closely results in the nominal 1 dB gain step value. These settings are tabulated in the gain step data for use by the reference level firmware.

The gain step correction firmware handles the sequencing of the combined coarse and fine gain; i.e. which gain is to be used first. The coarse gain is internally organized into a sequence of steps from 0 to 36 dB, in 9 dB steps. Starting from default settings, the firmware attempts to calibrate each gain step using the fine gain dac. If this dac runs out of range, the next coarse gain setting is selected and the fine gain dac set to the appropriate extreme; e.g. if the fine gain dac runs out at its lower end, the next lowest coarse gain is selected and the fine dac set to its maximum value, and the calibration continued.

The 1 dB steps are corrected in 1 dB/div, starting with the 0 dB setting and working up. When the signal level reaches the top of screen, the log offset is used to bring it back down. The correction terminates when either gain or log offset runs out. An error is generated if the gain range at termination does not meet VR specifications.

The trace for this part of the correction is as follows:

```
cal_gain_steps:
      adjusting log offset...
            Offset_To_Lvl: lvl=910 su  VertScale=10 dB/div
                  LogOffset= 0.00 dB  ht= 456 su  err=-454 lsb
                  LogOffset=45.40 dB  ht= 912 su  err=   2 lsb
            Offset_To_Lvl: lvl=100 su  VertScale=1 dB/div
                  LogOffset=45.40 dB  ht=  99 su  err=  -1 lsb
      gs_tbl[1]:
      set_gain_to_lvl: lvl=200 su
            c_gain=0x24  f_gain=0x15  err= -4 su
      gs_tbl[2]:
      set_gain_to_lvl: lvl=300 su
            c_gain=0x24  f_gain=0x2b  err= -2 su
      gs_tbl[3]:
      set_gain_to_lvl: lvl=400 su
            c_gain=0x24  f_gain=0x40  err= -3 su
      ...
      gs_tbl[7]:
      set_gain_to_lvl: lvl=800 su
            c_gain=0x24  f_gain=0x95  err=  5 su
      gs_tbl[8]:
      set_gain_to_lvl: lvl=900 su
            c_gain=0x24  f_gain=0xab  err= 21 su
            c_gain=0x24  f_gain=0xa7  err=  1 su
      gs_tbl[9]:
      adjusting log offset...
            Offset_To_Lvl: lvl=100 su  VertScale=1 dB/div
                  LogOffset=45.40 dB  ht= 901 su  err= 801 lsb
                  LogOffset=37.39 dB  ht=  94 su  err=  -6 lsb
                  LogOffset=37.45 dB  ht= 102 su  err=   2 lsb
      set_gain_to_lvl: lvl=200 su
            c_gain=0x24  f_gain=0xc0  err= 21 su
            c_gain=0x24  f_gain=0xbc  err=  0 su
      gs_tbl[10]:
      set_gain_to_lvl: lvl=300 su
            c_gain=0x24  f_gain=0xd5  err= 28 su
            c_gain=0x24  f_gain=0xcf  err= -6 su
      ...
      gs_tbl[52]:
      set_gain_to_lvl: lvl=500 su
            c_gain=0x09  f_gain=0xff  err= 39 su
            c_gain=0x09  f_gain=0xf7  err=-10 su
            c_gain=0x09  f_gain=0xf8  err= -4 su
      gs_tbl[53]:
      set_gain_to_lvl: lvl=600 su
            c_gain=0x09  f_gain=0xff  err=-62 su
      max_gs=52 dB
```

"cal_gain_steps" identifies that the 1 dB gain steps are being corrected. At this point the 1 dB steps (i.e. the coarse and fine gain) are set to zero, as are the VR output and microwave IF gain steps. The log offset is used to set the signal to a height of 100 (i.e 1 division up from the bottom of screen) in 1 dB/div ("Offset_To_Lvl..."). For each gain step being corrected, the table entry is indicated by "gs_tbl[*n*]," where *n* is the gain step being corrected. "set_gain_to_lvl: lvl=200 su" indicates the target signal height for the correction, in this case 200. For each iteration, "c_gain" is the bit-mapped switch setting for the coarse gain, "f_gain" is the fine gain dac, and "err" is the difference between the measured signal height and the target. It should be noted that the measured signal height has been log-corrected, and so may not correspond to the displayed

signal height on the instrument CRT. The correction for each gain step completes when the error is less than 10 su.

When the target signal level reaches a height of 900 su (1 division below top of screen), the log offset is used to reduce the signal height down to 100 su ("Offset_To_Lvl..."). Since the VR gain increases as the correction proceeds, the log offset always decreases, usually by about 8 dB. The correction terminates at this point if the log offset goes negative.

The correction proceeds until the VR is out of gain or the log offset goes negative. The former is indicated by the trace displaying "c_gain=0x09 f_fain=0xff" with an "err" greater than or equal to 10. When this happens the value of the previous gain step (i.e. the maximum valid one) is recorded ("max_gs=52") and checked against its specifications.

The following errors can occur during this part of the correction:

Signal Offset Timed Out.
Signal Offset Truncated.

See previous section.

Gain Step Correction Took Too Long

This error indicates that the correction of the current gain step did not succeed within 20 tries. The most likely cause is something causing an erratic signal level to be measured; i.e. a noisy signal trace, or an instability somewhere in the instrument.

Gain Step Correction Terminated
Hardware Failure Indicated

This error indicates that the correction required a negative gain setting to correct the current gain step. This is caused by a severe inability of the instrument to correctly measure signal levels, and indicates a serious instrument-level malfunction.

VR 25 MHz Gain Out Of Range.

This error indicates that the maximum VR gain does not meet its EIS specification. The "max_gs" value in the above trace must be between 45 and 58 dB. This error indicates that the instrument may not meet its specifications, but does not cause this correction to abort. The measured value(s) are recorded and used as if they were correct.

Gain Step Internal Self-Corr Terminated

This is the standard "gain step correction failed" error. It is generated at the end of the gain step correction if any other errors occurred; these errors should be used to determine what actually caused the failure.

Dumping Out Gain Step Correction Data

The gain step correction data may be dumped out and examined via the "dcal 2 3" command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 3 CurrentCalData-> gstep_data:
    gs_tbl[ 0]=0x24 0x00gs_tbl[ 1]=0x24 0x15gs_tbl[ 2]=0x24 0x2b
    gs_tbl[ 3]=0x24 0x40gs_tbl[ 4]=0x24 0x55gs_tbl[ 5]=0x24 0x6b
    gs_tbl[ 6]=0x24 0x80gs_tbl[ 7]=0x24 0x95gs_tbl[ 8]=0x24 0xa7
    gs_tbl[ 9]=0x24 0xbcgs_tbl[10]=0x24 0xd0gs_tbl[11]=0x22 0x13
    gs_tbl[12]=0x22 0x28gs_tbl[13]=0x22 0x3egs_tbl[14]=0x22 0x54
    gs_tbl[15]=0x22 0x68gs_tbl[16]=0x22 0x7dgs_tbl[17]=0x22 0x93
    gs_tbl[18]=0x22 0xa9gs_tbl[19]=0x22 0xbdgs_tbl[20]=0x12 0x05
    gs_tbl[21]=0x12 0x19gs_tbl[22]=0x12 0x2cgs_tbl[23]=0x12 0x41
    gs_tbl[24]=0x12 0x56gs_tbl[25]=0x12 0x6egs_tbl[26]=0x12 0x85
    gs_tbl[27]=0x12 0x99gs_tbl[28]=0x12 0xacgs_tbl[29]=0x12 0xbf
    gs_tbl[30]=0x11 0x09gs_tbl[31]=0x11 0x1egs_tbl[32]=0x11 0x33
    gs_tbl[33]=0x11 0x4ags_tbl[34]=0x11 0x61gs_tbl[35]=0x11 0x79
    gs_tbl[36]=0x11 0x8dgs_tbl[37]=0x11 0xa0gs_tbl[38]=0x11 0xb4
    gs_tbl[39]=0x11 0xc6gs_tbl[40]=0x09 0x04gs_tbl[41]=0x09 0x1b
    gs_tbl[42]=0x09 0x31gs_tbl[43]=0x09 0x48gs_tbl[44]=0x09 0x5c
    gs_tbl[45]=0x09 0x71gs_tbl[46]=0x09 0x85gs_tbl[47]=0x09 0x99
    gs_tbl[48]=0x09 0xadgs_tbl[49]=0x09 0xc1gs_tbl[50]=0x09 0xd5
    gs_tbl[51]=0x09 0xe7gs_tbl[52]=0x09 0xf7gs_tbl[53]=0x09 0xff
    gs_tbl[54]=0x09 0xffgs_tbl[55]=0x09 0xffgs_tbl[56]=0x09 0xff
    gs_tbl[57]=0x09 0xffgs_tbl[58]=0x09 0xffgs_tbl[59]=0x09 0xff
    max_gs=52
    uwave_gain=4.53
    vr_out[0]=0.00
    vr_out[1]=9.27
    vr_out[2]=19.14
```

"gs_tbl[*n*]" is the correction data for the *n*'th gain step. The first number is the coarse gain, which is decoded as follows:

Table 4-10. Coarse Gain Values.

Coarse Gain	Gain Value
0x24	0 dB
0x22	9 dB
0x12	18 dB
0x11	27 dB
0x09	26 dB

The second number is the fine gain dac value. "max_gs" is the maximum gain step in dB, and indicates the last "gs_tbl[]" entry containing valid data. "uwave_gain" is the value of the microwave gain step in dB. "vr_out[1]" is the value of the 10 dB VR output gain step, "vr_out[2]" is that of the 20 dB step; "vr_out[0]" is the value of the 0 dB step, and is always 0.00 by definition.

Several keyboard commands are available for manipulating the gain steps. "ganc *x*" sets the VR coarse gain, where *x* is one of the values from the above table, in

hexadecimal. "ganf *x*" sets the VR coarse gain, where *x* is the fine gain dac value, in hexadecimal; values can range from 00 to ff. "uwif 1" turns the microwave IF step off; "uwif 0" turns it on. "gred *n*" sets the VR output gain to 0, 10, and 20 dB for *n* values of 0, 1, and 2, respectively.

Resolution Bandwidth and Reference Level Correction

The resolution bandwidth correction adjusts the resolution bandwidth filters for correct bandwidth, and computes the reference level correction factors for each filter. In addition, a "negative resistance" correction is performed to maximize the dynamic range of the VR. These corrections are primarily concerned with the VR module, and most errors can be traced back to problems with the VR. The resolution bandwidth correction is the last vertical correction to be executed, and assumes that all of the other vertical corrections have been successfully performed. It is particularly important that the instrument be fully warmed up, and that resonator tracking be performed immediately prior to resolution bandwidth correction. This correction takes approximately 15 minutes to complete.

Fine control of the resolution bandwidth is via the VBW (Variable BW) dac on the VR module. The mapping from dac value to actual bandwidth is controlled by the bandwidth "range;" this is a collection of VR settings that determine the behavior of the VBW dac. The bandwidth ranges are as follows:

Table 4-11. Bandwidth Range Settings

Range Number	ResBW Range	MinBW Mode	RS1 RS2	Z	LC/Crystal Mode	VRPath Bits	Pre/Post Filter Gain
0	3Hz- 33Hz	MinBW	0x2	0	Crystal	0x322	0x04
1	33Hz- 47Hz	Normal	0x2	0	Crystal	0x322	0x02
2	47Hz- 230Hz	Normal	0x0	0	Crystal	0x322	0x01
3	230Hz- 190Hz	Normal	0x3	1	Crystal	0x322	0x02
4	190Hz- 370Hz	Normal	0x1	1	Crystal	0x322	0x02
5	370Hz- 680Hz	Normal	0x2	1	Crystal	0x322	0x02
6	680Hz-5300Hz	Normal	0x0	1	Crystal	0x322	0x01
7	5 Hz- 12 Hz	MinBW	0x2	0	LC	0x342	0x04
8	12 Hz- 83 Hz	MinBW	0x2	0	LC	0x542	0x04
9	83 Hz-120 Hz	Normal	0x2	0	LC	0x542	0x02
10	120 Hz-580 Hz	Normal	0x0	0	LC	0x542	0x01
11	580 Hz-630 Hz	Normal	0x3	1	LC	0x542	0x02
12	630 Hz-920 Hz	Normal	0x1	1	LC	0x542	0x02
13	920 Hz-1.7 MHz	Normal	0x2	1	LC	0x542	0x02

The above table lists the approximate resolution bandwidth range corresponding to each range, along with the VR settings that define the range. Several of the ranges are currently unused. "MinBW Mode" indicates whether the VR resonators are operating in their minimum bandwidth (MinBW) or normal mode. "RS1-RS2" indicates which of the two switchable resistors (RS1 and RS2) are on; 0x2 indicates RS1, 0x1 indicates RS2, and 0x3 indicates both. "Z" is 1 for high Z, 0 for low Z. LC/Crystal Mode indicates whether the resonators are in LC or crystal mode. "VRPath Bits" are the bit-mapped VR path switches. "Pre/Post Flt Gain" indicates the pre- and post-filter gain state. See the VR EMS for further details.

The resolution bandwidths are corrected by adjusting the VBW dac until the bandwidth meets specification; the range is adjusted as well if the VBW dac runs out of range. The 3 MHz and 10 MHz bandwidths are fixed filters, and cannot be adjusted. Once the bandwidth for a filter is correct, the reference level is corrected by determining an appropriate reference level correction factor; this is done for the fixed filters as well. The negative resistance amplifier is adjusted to provide coarse bandwidth levelling prior to attempting any bandwidth correction.

Negative Resistance Correction

The VR has a negative resistance amplifier which is used to level the bandwidths for each High Z/Low Z and LC/Crystal combination. The negative resistance (or negative R) dac value is determined for each combination that will make all bandwidths within that combination be about the same amplitude. For each combination, the correction starts by making initial amplitude and bandwidth measurements at the minimum and maximum bandwidths; these are used to compute a target amplitude where the negative R will be correct. Since the minimum bandwidth is where the negative R is most sensitive, this setting is used to adjust the negative R dac until the target amplitude is reached.

Because this dac is highly nonlinear, a binary search algorithm is used to determine the desired amplitude. This search technique starts by making a measurement at the midpoint of the dac range. By noting whether the signal level is too high or too low, the appropriate half of the dac range can be eliminated from the search range. The next measurement is taken at the midpoint of the remaining range, and the appropriate half of this range is again eliminated. This continues until the search range is reduced to one lsb. This method allows the optimum dac value to be determined with only eight measurements. Once the best value is obtained, the corresponding error is checked to make sure it is within specifications.

The trace for this part of the correction is as follows:

```
ResBWCorrection :
cal_neg_res:
 cal_neg_res: Lo Z  Crystal
       measure_y0:
             min_rng= 0  min_rbw=10 Hz min_vbw=0x60
             max_rng= 2  max_rbw=100 Hzmax_vbw=0xf0
             ResBWLvl=0xd0
             y2=805 su  rt2= 432.80 ohms
             y1=147 su  rt1=  18.25 ohms
             y0 (final) = 877 su
       bw_lvl=0x80  lvl_err=-82.80 dB
       bw_lvl=0xbf  lvl_err=-78.50 dB
       bw_lvl=0xdf  lvl_err=-56.80 dB
       bw_lvl=0xef  lvl_err= 14.10 dB
       bw_lvl=0xe7  lvl_err=-33.60 dB
       bw_lvl=0xeb  lvl_err=-15.00 dB
       bw_lvl=0xed  lvl_err= -3.90 dB
       bw_lvl=0xee  lvl_err=  2.50 dB
       bw_lvl=0xee (final)
 cal_neg_res: Hi Z  Crystal
       ...
 cal_neg_res: Lo Z  LC
       ...
 cal_neg_res: Hi Z  LC
       ...
```

"cal_neg_res: Lo Z Crystal" identifies that the negative R is being corrected for the low Z crystal combination. "measure_y0" is the header for the target amplitude determination. "min_rng= 0 min_rbw=10 Hz min_vbw=0x60" indicates the range number, nominal resolution bandwidth, and specific VBW dac value used for the narrow bandwidth end of the measurement; "max_rng= 2 max_rbw=100 Hz max_vbw=0xf0" indicates the same information for the wide bandwidth end. "ResBWLvl" is the specific negative R dac value at which the measurements are made. The next two lines ("y2=805 ... y1=147 ...") are the results of the wide and narrow bandwidth measurements; "y2" and "y1" are the wide and narrow bandwidth signal heights, respectively; "rt2" and "rt1" are termination resistances computed from the corresponding measured bandwidth values. "y0 (final)" is the target amplitude computed from "y1," "y2," "r1," and "r2."

The dac value and signal level error is listed for each iteration of the binary search; "bw_lvl" is the negative R dac value, and "lvl_err" is the difference between the measured level and "y0" in dB. The final dac value ("bw_lvl=0xee (final)") is printed when the search is finished, and the corresponding error checked for validity; an error is generated if the error is greater than 5.0 dB. The following errors can occur during this part of the correction:

```
VR Negative Resistance DAC Too Coarse
Low Z, Crystal Neg R DAC Too Coarse.
High Z, Crystal Neg R DAC Too Coarse.
Low Z, LC Neg R DAC Too Coarse.
High Z, LC Neg R DAC Too Coarse.
Measure Bandwidth Found Bad Waveform
```

VR Negative Resistance DAC Too Coarse.

This error is generated if any of the negative R corrections fails to meet specifications. The specific correction is identified by one or more of the following errors. This error indicates a problem in the negative R circuits of the VR module.

Low Z, Crystal Neg R DAC Too Coarse.
High Z, Crystal Neg R DAC Too Coarse.
Low Z, LC Neg R DAC Too Coarse.
High Z, LC Neg R DAC Too Coarse.

Each of these errors identifies a specific High Z/Low Z LC/Crystal combination whose level could not be calibrated to within 5 dB of target. These errors indicates a problem in the negative R circuits of the VR module.

Measure Bandwidth Found Bad Waveform.

This error is generated by an unsuccessful attempt to make a bandwidth measurement. This is the result of an invalid waveform; i.e. the signal is missing or severely distorted. The most likely cause is some problem in the VR module (i.e an oscillation causing a rise in the noise floor); however, it could also be due to system problems such as loss of frequency lock.

ResBW and Reference Level Correction

The resolution bandwidths are now corrected with respect to bandwidth (if appropriate) and amplitude. For each bandwidth, the nominal setting is selected using the default correction data and the appropriate negative R value from the previous section. A rough reference level correction is performed to position the signal level at two divisions from top of screen in 1 dB/div. The bandwidth is now corrected to within 4% of its nominal value; the bandwidth range and the corresponding settings are changed if necessary. The final reference level correction is now performed to produce a signal level of -50 dBm with an accuracy of +/- 0.05 dB.

The exceptions to this procedure are the 3 Hz, 3 MHz, and 10 MHz filters. The 3 MHz and 10 MHz bandwidths are fixed filters whose bandwidth cannot be adjusted. Although the 3 Hz bandwidth is adjustable, its bandwidth cannot be measured accurately enough for meaningful correction. Therefore these bandwidths are are corrected for amplitude only.

Since the trace information is highly repetitive, the trace for most of the resolution bandwidths has been omitted from this document. The traces for the 3 Hz and 10 Hz bandwidths have been chosen as examples of amplitude-only and full bandwidth correction, respectively.

The trace for the 3 Hz bandwidth is as follows:

```
Calibrating ResBW=3 Hz
 cal_bw_lvl: 10 dB/div
       lvl=1000 su  max_err=20 lsb
       ResBWLvlCorr=30.00  gain=43 dB  offset=0.39 dB  err= 200 su
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err=  -5 su
 cal_bw_lvl: 1 dB/div
       lvl=1000 su  max_err=5 lsb
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err= -58 su
       ResBWLvlCorr=10.58  gain=23 dB  offset=0.97 dB  err=  -8 su
       ResBWLvlCorr=11.24  gain=24 dB  offset=0.63 dB  err=1 su
```

"Calibrating ResBW=3 Hz" identifies that the 3 Hz bandwidth is being corrected. "cal_bw_lvl" is the routine used to correct the reference level for the current bandwidth. The reference level is corrected first in 10 dB/div, then in 1 dB/div for maximum accuracy. "lvl" is the height to which the signal is adjusted, and "max_err" is the accuracy to which this is to be done. For each iteration, "ResBWLvlCorr" is the resolution bandwidth level correction factor used by the reference level firmware; this number is in dB. "gain" and "offset" are the VR gain and log offset corresponding to "ResBWLvlCorr." "err" is the reference level error in screen units. The 3 Hz bandwidth is corrected for amplitude only.

The trace for the 10 Hz bandwidth is as follows:

```
Calibrating ResBW=10 Hz
 cal_bw_lvl: 10 dB/div
       lvl=980 su  max_err=20 lsb
       ResBWLvlCorr=30.00  gain=43 dB  offset=0.39 dB  err= 200 su
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err= -39 su
       ResBWLvlCorr=13.90  gain=27 dB  offset=0.29 dB  err=  -1 su
 cal_bw_lvl: 1 dB/div
       lvl=920 su  max_err=20 lsb
       ResBWLvlCorr=13.90  gain=27 dB  offset=0.29 dB  err=-158 su
       ResBWLvlCorr=15.48  gain=28 dB  offset=0.87 dB  err=  -5 su
 range=0  vbw=0xc9  bw_err=-1.74 Hz (-17.4 %)
 range=0  vbw=0xd3  bw_err=0.74 Hz (7.4 %)
 range=0  vbw=0xcf  bw_err=-0.07 Hz (-0.7 %)
 cal_bw_lvl: 1 dB/div
       lvl=1000 su  max_err=5 lsb
       ResBWLvlCorr=15.48  gain=28 dB  offset=0.87 dB  err=-101 su
       ResBWLvlCorr=16.49  gain=29 dB  offset=0.88 dB  err=  -6 su
       ResBWLvlCorr=16.55  gain=29 dB  offset=0.94 dB  err=0 su
```

Because correction of the filter bandwidth causes small changes in signal amplitude, the reference level correction is broken up into two parts. The "cal_bw_lvl" routine is used to adjust the signal level to 2 divisions below top of screen in 1 dB/div; the trace for this is as for the previous bandwidth. For each iteration of the bandwidth correction, "range" is the bandwidth range, "vbw" is the VBW dac value, and "bw_err" is the bandwidth error in both Hz and percent; the bandwidths are corrected to within 4%. Once the bandwidth has been corrected, the reference level is corrected as for the 3 Hz filter.

The following errors can occur during this part of the correction:

```
BW Correction Timed Out; Terminated
Bandwidth Correction Reached Limit
BW Level Correction Timed Out
Resolution Bandwidth Self-Corr Failed
```

BW Correction Timed Out; Terminated.

This error indicates that the bandwidth could not be corrected within 10 iterations. A VR problem is the most likely cause.

Bandwidth Correction Reached Limit.

This error indicates that a bandwidth could not be corrected because the hardware had insufficient range. This error should only occur for the 1 MHz and possibly the 10 Hz bandwidths. A problem in the VR is indicated.

BW Level Correction Timed Out;

This error indicates that the bandwidth could not be corrected within 15 iterations. This error is almost always due to incorrect correction data for either display law correction, gain step correction, log correction, or a combination of these. If this error shows up, it will likely be intermittent and difficult to track down. The most likely cause is either the VR or Log Processor modules; these modules should be replaced and the ResBW correction run at least 10 times to verify that the problem has been fixed.

Resolution Bandwidth Self-Corr Failed.

This is the standard "resolution bandwidth correction failed" error. It is generated at the end of the resbw correction if any other errors occurred; these errors should be used to determine what actually caused the failure.

Dumping Out Resolution Bandwidth Correction Data

The resolution bandwidth correction data may be dumped out and examined via the "dcal 2 4" command. The trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : dcal 2 4
CurrentCalData-> resbw_data:
 ResBW   VRPath MinBW  RS   Neg_R VBW  PFGain Z XLC   Range Refl_Corr
     3   0x0322 0x3f  0x2  0xef  0x6e  0x40 0x00   0    7.89 dB
    10   0x0322 0x3f  0x2  0xef  0xce  0x40 0x00   0   16.24 dB
    30   0x0322 0x3f  0x2  0xef  0xf5  0x20 0x00   0   16.11 dB
   100   0x0322 0x00  0x0  0xef  0xb7  0x10 0x00   2   14.70 dB
   300   0x0322 0x00  0x1  0x74  0xf4  0x21 0x00   4   18.17 dB
  1000   0x0322 0x00  0x0  0x74  0x9d  0x11 0x00   6   17.61 dB
  3000   0x0322 0x00  0x0  0x74  0xf3  0x11 0x00   6   17.59 dB
 10000   0x0342 0x3f  0x2  0xc7  0x9e  0x40 0x3f   7   23.09 dB
 30000   0x0542 0x3f  0x2  0xc7  0xdd  0x20 0x3f   8   21.79 dB
100000   0x0542 0x00  0x0  0xc7  0x50  0x20 0x3f  10   21.66 dB
300000   0x0542 0x00  0x0  0xc7  0xc5  0x10 0x3f  10   21.05 dB
1000000  0x0542 0x00  0x2  0x70  0x91  0x21 0x3f  13   20.12 dB
3000000  0x0844 0x00  0x0  0x00  0x00  0x00 0x00  14   47.06 dB
10000000 0x0884 0x00  0x0  0x00  0x00  0x00 0x00  14   46.09 dB
```

"ResBW" is the resolution bandwidth for the row of data. "VRPath" is the bit-mapped VR path switches. The bit mapping is as follows:

Table 4-12. VR Path Bit Map

Bit	Function
bit 0 (lsb)	29 MHz count (VR 1)
bit 1	4 MHz path (VR 1)
bit 2	25 MHz path (VR 1)
bit 3	NBW for 25 MHz ringdown (VR 1)
bit 4	25 MHz source (VR 1)
bit 5	xtal filter (VR 1)
bit 6	3 MHz filter (VR 1)
bit 7	10 MHz filter (VR 1)
bit 8	29 MHz osc on/off (VR 2)
bit 9	BP (VR 3)
bit 10	LP (VR 3)
bit 11	25 MHz path (VR 3)
bit 12 (msb)	4 MHz source (VR 3)

"MinBW" indicates whether the resonators are in minimum bandwidth mode; 0x3f means all 6 are in minimum bandwidth mode, 0x00 means none of them are. "RS" is the state of RS1 and RS2; 0x2 means RS1 is switched in, 0x1 means RS2 is switched in, and 0x3 means both are switched in. "Neg_R" is the negative R (or resbw level) dac value. "VBW" is the VBW dac value. "PFGain" is the pre-filter and post-filter gain:

Table 4-13. VR Path Switch Bit Maps

PFGain Value	Pre-Filter Gain	Post-Filter Gain
0x0	off	off
0x1	+6 dB	-6 dB
0x2	0 dB	0 dB
0x4	-6 dB	+6 dB

"Z" is 1 for high Z, 0 for low Z. "XLC" is the LC/Crystal mode; 0x00 indicates all resonators in crystal mode, 0x3f indicates all in LC mode. "Range" is the resolution bandwidth range. "Refl_Corr" is the reference level correction factor in dB. Most of these items refer to specific controls on the VR module; refer to the VR documentation for mode details.

Video Processor Troubleshooting

Analog Video Processor

Input Switch

Basic Function

The Input Switch is a two input one output multiplexor. The selection of either channel is achieved by switching a TTL level signal called VIDSEL. Currently this amplifier can only be switched from the keyboard mode.

Both the inputs and the outputs of the Input Switch are differential. The outputs of the switch drive the Input Switch Buffer.

Module Level Correction

There is no self correction required for the Input Switch.

Self-Correction Requirements

There is no module level correction required for the Input Switch.

Failure Modes and Symptoms

There are two failure modes in the Input Switch. They are:

Switch Channel Not Selectable
With a signal applied to both inputs of the Input Switch one of the applied signals will not be displayed when switching between Internal and External Video sources. The two signals applied must be different in some manner.

Neither Channel of Input Switch Passes Signal
There will be a straight line somewhere on the display. Most likely at either the top or the bottom of the screen

Input Switch Buffer

Basic Function

The Input Switch Buffer is a single ended unity gain amplifier designed to drive the large load that is connected to the Input Switch. There are two of these buffers, one for each output of the Input Switch.

Module Level Correction

There is no module level correction required for the Input Switch Buffer.

Self-Correction Requirements

There is no self correction required for the Input Switch Buffer.

Failure Modes and Symptoms

There is only one possible failure mode in the Input Switch Buffer. It is a general circuit failure. This will cause a straight line to appear somewhere on the screen, most likely at the top or the bottom.

Video Filters

Basic Function

The Video Filters are differential single pole (simple RC) filters. The filters are user selectable in values ranging from 0.03 Hz to 300 kHz in a 1-3-10 sequence. The filters are selected by switches on both a bank of resistors and a bank of capacitors.

The Video Filters are currently selectable from the front panel and the keyboard mode.

Module Level Correction

There is no module level correction required for the Video Filters.

Self-Correction Requirements

There is no self correction required for the Video Filters.

Failure Modes and Symptoms

There are two possible failure modes in the Video Filters. They are:

Control Signal, Part Failure, or Switch Failure
This failure will appear as a lack of change or inconsistent change in the peak-to-peak height of the displayed noise floor.

Filtered Path Buffer Failure
This failure will appear as a straight line somewhere on the screen, most likely at the top or the bottom, when the Video Filter Bandwidth is 300 kHz or less.

Video Filter Buffer

Basic Function

The Video Filter Buffer is a single ended amplifier which provides the appropriate gain and offset to scale the signal for the Analog to Digital Convertor (ADC). There are two of these amplifiers, positive and negative. The Negative Video Filter Buffer contains variable gain and offset controls, while the Positive Video Filter Buffer contains neither a gain or offset control. The reasoning for this is describe under the Self Correction Requirements below.

The outputs of the Video Filter Buffer drive the Trigger Circuits, the Peak Detectors, the Analog Max/Min Detectors, and the Vertical Real Time Clamp.

Module Level Corrections

There is one module level correction that needs to be performed on this portion of the circuit. This correction is the adjustment of a reference voltage, which in turn adjusts out the offsets due to resistor tolerances of the previous amplifiers.

Self-Correction Requirements

There are two self correction requirements of the Video Filter Buffer. These corrections are the gain and offset adjustments for the vertical path (on the Video Processor).

Positive Video Filter Buffer
The Positive Video Filter Buffer does not have any self correction adjustments on it. The reason for this is that the positive channel is used to calibrate the entire vertical channel and cannot be changed at any time.

Negative Video Filter Buffer
The Negative Video Filter Buffer contains a gain and offset adjustment that is adjusted by the self correction firmware so that the output voltage is the same as the Positive Video Filter Buffer across the visible screen.

Failure Modes and Symptoms

There are two failure modes in the Video Filter Buffers. They are:

General Circuit Failure
This failure will cause a straight line on the screen, most likely at the top or the bottom of the screen.

Gain or Offset DAC failure
This failure will cause the Peak Detector Correction to fail while calibrating the Minimum Peak Detectors to match the Maximum Peak Detectors (the calibrating gain and offset message on the screen).

Peak Detectors

Basic Function

The Peak Detectors are a special type of a single ended amplifier. They have the ability to track the input voltage, detect and store the maximum input voltage, and hold (store) the input voltage any level. These three modes are selected via two control lines. One control line switches between the track and peak detect functions. While the other line switches between the track and hold functions.

The four Peak Detectors are arranged with two Peak Detectors on the positive video line (the Maximum A and B Peak Detectors) and two Peak Detectors on the negative video line (Minimum A and B Peak Detectors). They are controlled in such a manner that there is always one Peak Detector peak detecting while the other Peak Detector is tracking or holding. This ensures that a signal cannot escape being detected.

The Peak Detectors are also used as high speed sample and hold amplifiers. In this mode only the Maximum Peak Detectors are used. They are switched between the track and hold modes only. Once again there is always one Peak Detector tracking while the other is holding.

The outputs of the Peak Detectors drive the Vin Multiplexor and the Analog Max/Min Detector.

Module Level Correction

There is no module level correction required for the Peak Detectors.

Self-Correction Requirements

Both the Maximum B and the Minimum B Peak Detectors require a self correction adjustment. In this adjustment the output voltage of the B Peak Detector is adjusted to equal the output of the A Peak Detector.

This correction is required before any of the vertical channel self correction firmware is run. If this correction is not performed the self correction procedures may fail or at least not give accurate results.

Failure Modes and Symptoms

There are three possible failure modes in the Peak Detectors. They are:

General Circuit Failure

If general circuit failure occurs in only one Peak Detector then there will be single "bin" wide "sticks" from the signal to either the top or the bottom of the screen (depending on the acquisition mode).

If general circuit failure occurs in two Peak Detectors of the same type (i.e. maximum or minimum) then there will be a straight line at either the top or the bottom of the screen when the appropriate acquisition mode is selected.

Hold Mode Failure

This type of failure will give the same symptoms as described in the General Circuit Failure as well as one more. The third symptom is that the noise floor peaks are not random, but tend to always stay at the same value.

Peak Detect Mode Failure

This type of failure will give the same symptoms as described in the General Circuit Failure as well as one more. The third symptom is that the noise floor in the Maximum and Minimum Acquisition modes will look the same as the Sample Acquisition mode.

Vin Multiplexor

Basic Function

This circuit uses four analog switches to select which Peak Detector output is going to be digitized by the ADC. The selection of the switch is determined by a state machine on the Digital Board.

Module Level Correction

There is no module level correction required for the Vin Multiplexor.

Self-Correction Requirements

There is no self correction required for the Vin Multiplexor.

Failure Modes and Symptoms

There is really only one possible failure mode for the Vin Multiplexor. The symptom is that the noise floor peaks for some of the points will appear to stay at the same value.

Analog Max/Min Detector

Basic Function

This circuit is a set of four comparators which compare the inputs and outputs of the Peak Detectors during the peak detect mode. The comparators are set up to look for a signal which falls below the peak detected signal. The outputs of these comparators are used by the state machines on the Digital Board to help implement the Max/Min display algorithm.

Module Level Correction

There is no module level correction required for the Analog Max/Min Detector.

Self-Correction Requirements

There is no self correction required for the Analog Max/Min Detector.

Failure Modes and Symptoms

The only failure mode in this circuit is the general circuit failure. The symptom for this type of failure is narrow pulses not being displayed with the correct amplitude in successive sweeps while in the Max/Min Acquisition Mode.

Vertical Real-Time Amplifier and Clamp

Basic Function

The Vertical Real-Time Amplifier and Clamp is basically just the buffer for the vertical real-time signal, with a couple of additions. The first addition is a high speed clamp circuit which clamps the output signal to a voltage set by the CLAMP adjustment. This circuit is there to prevent the Display Amplifier inputs from being over driven in the negative direction.

The other additions to the circuit are gain and offset adjustments for aligning the real-time display to the digitized display.

Module Level Correction

There is no module level correction for the Vertical Real-Time Amplifier and Clamp circuits.

Instrument Level Correction

The alignment of the real-time and digitized displays mentioned above is done at the instrument level. This adjustment should be done only after the rest of the vertical correction has been completed.

Current the adjustment is made using a "normal" display that occupies the entire screen. In the future there will be a display designed to aid in making this adjustment as well as to verify the interface between the Video Processor and Digital Storage.

Self-Correction Requirements

There is no self correction required for the Vertical Real-Time Amplifier and Clamp.

Failure Modes and Symptoms

There are three possible failure modes in the Vertical Real Time Clamp. They are:

General Circuit Failure
This failure will cause a straight line on the screen, most likely at either the top or the bottom of the screen or no real time signal displayed at all. There may also be some other problems with the real time display (i.e. distortion in the Digital Storage Display).

Clamp Circuit Failure

This failure will cause the real time signal to not be adjustable or the real time signal will be a flat line at the bottom of the screen.

Input Circuit Failure
This failure will show up as an inability to adjust the real time gain and offset to match the digitized signal.

Serial Interface and Decoding Circuits

Basic Function

This circuit is the interface between the Main Processor and the Video Processor. The outputs of the SIC are decoded into several control lines. These control lines in turn go to the horizontal and vertical state machines, as well as the various DAC's, and FET switches on the Analog Board.

Module Level Correction

There is no module level correction required for the Serial Interface and Decoding Circuits.

Self-Correction Requirements

There is no self correction required for the Serial Interface and Decoding Circuits.

Failure Modes and Symptoms

There are two possible failure modes for the Serial Interface and Decoding Circuits. They are:

Serial Interface Chip Failure
This type of failure will most likely be detected by the Main Processor and an error will be displayed on the screen.

Decoding Circuit Failure
The symptoms for this type of failure are not being able to change acquisition modes, video filters can't be changed, etc.

Horizontal Acquisition

Basic Function

The Horizontal Acquisition is configured as a closed loop system. The Sweep voltage is buffered by an op-amp whose output is summed with the output of a 10 bit Digital to Analog Convertor (DAC). This summing point then drives two comparators. One comparator detects when the summing point is above a given threshold (up comparator), while the second comparator detects when the summing point is below ground (down comparator). The outputs of these two comparators drive the horizontal state machine. Two control lines from the horizontal state machine then drive a 10 bit counter whose outputs drive the

DAC. Thus when the current drawn by the DAC (magnitude of current is set by the 10 bit counter) through the summing resistor is the same voltage as is on the Sweep lines, the summing point is at zero volts and the counters don't move. As soon as the summing point changes the counters move to bring the summing point back to zero.

There are also two other modes of the Horizontal Acquisition. They are the Log Correction Acquisition (LCA) and the Test Mode Acquisition. The LCA mode is a single sweep at a very precise rate. This used in the self correction routines of the vertical channel. The Test mode is used to help in troubleshooting the horizontal acquisition.

Module Level Correction

There is no module level correction required for the Horizontal Acquisition circuits.

Self-Correction Requirements

There is no self correction required for the Horizontal Acquisition circuits. The self correction routines do use the LCA mode of the Horizontal Acquisition during the vertical correction routines.

Failure Modes and Symptoms

There are two possible failure modes for the Horizontal Acquisition. They are:

Up/Down Comparator Failure
Failures in this area of the Horizontal Acquisition will prevent the digitized portion of the sweep from being digitized in the direction of the comparator that failed.

General Circuit Failure
This type of failure will prevent any digitizing of the sweep. This will also cause the Self-Correction routines to fail.

Vertical Acquisition

Basic Function

The Vertical Acquisition is used to control the ADC, the Peak Detectors, Vertical Acquisition Mode, and data output. All of these functions are implemented using three state machines.

ADC Control, etc.

There are two control lines for the ADC which are generated in the vertical state machines. These control lines are used by the ADC to start a conversion and read the data from the ADC. Once the data is read from the ADC it is stored in one of two storage registers depending on the current Vertical Acquisition Mode. There is a state machine which tells the Peak Detector Control state machine and the Vertical Sub State machine which type of peak detector acquisition is currently being processed. This state machine is called the Vertical Main state machine. The Peak Detector Control state machine controls all of the functions of the Peak Detectors, switching them into the right modes at the right times.

Vertical Acquisition Modes

There are four types of vertical acquisitions that may be selected from the front panel. Each of these acquisition types are implemented in the Vertical Sub state machine and are described below.

Maximum Mode. The Maximum Mode displays the maximum of all the values digitized in a given horizontal bin.

The Maximum Mode stores, in the maximum storage register , the maximum value digitized for the current horizontal bin. At the end of the horizontal bin this maximum data is output to Digital Storage. The maximum and minimum storage registers are then cleared and a new maximum and minimum value are stored. The cycle then repeats itself for the new horizontal bin.

Minimum Mode. The Minimum Mode displays the minimum of all the values digitized in a given horizontal bin.

The Minimum Mode stores, in the minimum storage register, the minimum value digitized for the current horizontal bin. At the end of the horizontal bin this minimum data is output to Digital Storage. The maximum and minimum storage registers are then cleared and a new maximum and minimum valued are stored. The cycle then repeats itself for the new horizontal bin.

Sample Mode. The Sample Mode displays the last value digitized in a given horizontal bin.

The Sample Mode takes the digitized value and stores it in the minimum storage register regardless of the data that was previously stored. At the end of the horizontal bin the data in the minimum storage register is output to Digital Storage. The cycle then repeats itself for the new horizontal bin.

Max/Min Mode. The Max/Min Mode displays the maximum of all values digitized in a given horizontal bin if signal is detected, the maximum of all values digitized in a given horizontal bin if noise is detected and the horizontal bin is odd, and the minimum of all values digitized in a given horizontal bin if noise is detected and the horizontal bin is even.

The Max/Min Mode stores the maximum of values digitized in the maximum storage register and the minimum of the values digitized in the minimum storage register, for the current horizontal bin. At the end of the horizontal bin the appropriate data (as described in the paragraph above) is sent to Digital Storage. The maximum and minimum storage registers are then cleared and a new maximum and minimum valued are stored. The cycle then repeats itself for the new horizontal bin.

Module Level Correction

There is no module correction required for the Vertical Acquisition.

Self-Correction Requirements

There is no self correction required for the Vertical Acquisition.

Failure Modes and Symptoms

There are basically two failure modes in the Vertical Acquisition. They are:

Data Output Failure
This type of failure is shown on the display as one axis of the digitized data remains stationary while the other axis moves with the incoming digitized data (i.e. if the vertical data failed the horizontal axis would sweep normally and the vertical axis would remain stationary).

Acquisition Mode Failure
This type of failure would give a display that is not consistent with the expected display for the selected acquisition mode.

Horizontal Real-Time

Basic Function

The Horizontal Real-Time circuit consists of an amplifier that attenuates and buffers the Sweep inputs. The amplifier also contains gain and offset adjustments. These adjustment are used to align the real-time signal with the digitized signal. To make sure that the real-time single shrinks when a menu is displayed a fixed gain and offset adjustment are switched in to the existing gain and offset adjustments, when a menu is displayed.

Module Level Correction

There is no module level correction required for the Horizontal Real-Time Circuits.

Instrument Level Correction

The Horizontal Real-Time must be aligned with the digitized signal at the instrument level. Currently this done using a "normal" display which occupies the entire screen. In the future a display will be generated which will aid in the aligning of the real-time and digitized displays.

Self-Correction Requirements

There are no self correction requirements for the Horizontal Real-Time Circuits.

Failure Modes and Symptoms

There are three possible failure modes for the Horizontal Real-Time circuits. They are:

General Circuit Failure
This type of failure will produce a real-time display that will not sweep and may not even be on the display. This type of failure may also cause distortion in the Digital Storage Display.

Adjustment Failure
This type of failure will prevent the adjusting of the Horizontal Real-Time display gain and offset to the digitized display.

Compressed Screen Failure
This type of failure will produce a display that will always be compressed (real-time display with a menu displayed) or a real-time display that fails to compress when a menu is displayed.

Display Section Troubleshooting

Table 4-14. Display Section Problems and Possible Causes.

Problem	Possible Causes
Display Blank	Over Voltage shutdown condition in HV Power Supply Disconnected cable Z-axis IC failure on Display Amplifiers Faulty blanking input to Display Amplifiers
No Color	Disconnected or Shorted Cable Color Shutter driver failure No DIGCOLOR signal from Digital Storage Color Shutter Failure
Color Smearing	Color Shutter driver malfunction resulting in no color inhibit signal sent to Digital Storage Open or short on Display Amplifiers involving a Color Shutter timing component Digital Storage not responding to /DIGINH signal
Dot in Middle of Screen	Shorted deflection/Z-axis cable causing +87 V regulator to fold-back Deflection cable unplugged Failed Deflection Amp/Z-axis IC causing +87 V regulator to fold back
Dot in Corner of Screen	No Digital Storage deflection signals due possibly to a continuously inhibited state Digital Storage display control program execution error Extreme overdrive of Deflection Amplifier inputs
Display Out of Focus	Failed Focus Amplifier on Display Amplifiers Failed Focus Amplifier on High Voltage Power Supply Brick failure Oscillation on Deflection Amplifier output
Insufficient Gain Range	Display too small, HV Power Supply in an over-voltage condition Display too large, HV Power Supply in an under-voltage condition
Distortion on Display	Overdrive of Deflection Amplifier inputs +87 V regulator on Display Amplifiers going into current limit Bit stuck on Digital Storage DAC High Voltage Power Supply cable intermittent Oscillation on Deflection Amplifier outputs

Digital System Diagnostics

There are two levels of diagnostic tests in the instrument. Power Up Diagnostics automatically run each time the instrument is turned on. This provides a quick check of the instrument before operation begins. Advanced Diagnostics are available for more detailed and time consuming checks.

The advanced diagnostics tests provide extended testing for each module and they aid in fault isolation if there is a problem. The tests start from a central point and work out to the user interfaces, and then to the other modules. The advanced tests are called by setting switches on the Main Processor board.

Each advanced test has two modes of operation, single pass and looping. In the single pass mode the diagnostics stop if there is an error and display an appropriate error message. Otherwise, a single pass of the test is completed and normal operations resume. The looping test mode of diagnostics continues testing the modules until a failure occurs, then displays an error message.

Power Up Diagnostics

This information explains the power up diagnostics for the Main Processor board. The sixteen LEDs on the Main Processor board display test information. The test descriptions use 4-digit hexadecimal (hex) equivalents of the 16-digit binary codes. The following table converts four digits of the LED binary code into one digit of the hex values used in the test descriptions.

Table 4-15. Hex to Binary Conversion for LEDs

Hex Value	LED Pattern	Hex Value	LED Pattern
0	0000	8	1000
1	0001	9	1001
2	0010	A	1010
3	0011	B	1011
4	0100	C	1100
5	0101	D	1101
6	0110	E	1110
7	0111	F	1111

The LEDs start with the MSB to the left and the LSB to the right, the same is true for the hex values. A lit LED is a 1 and an unlit LED is a 0. For example, an LED display of 0000000000000001 gives a hex value of 0001

Microprocessor Self Test

The first test turns all of the LEDs off, sets the internal flags for the processor chip, and then checks that each flag has been set. If there are no errors, the internal flags are cleared and checked again. Then there is a quick check of all available internal registers. If there is an error the program will stop.

Initialize Processor IO

Entering this test, the LED pattern displays the hex value of 0001. This initialize routine sets up the various controller chips that make up the system. After the setup is completed, the switches are checked to see if the advanced diagnostics tests are selected or if normal operation should proceed.

Check System ROM

Entering this test, the LED pattern displays the hex value of 0002. If the check fails, the system will halt.

RAM Test

Entering this test, the LED pattern displays the hex value of 0004. The test first fills the RAM with all logic highs, and then verifies that the data is correct. After all the banks are checked the test fills the RAM with all logic lows and then verifies that the data is correct. If the test fails the system halts.

Remaining ROM Test

Entering this test, the LED pattern displays a hex pattern for the ROM being checked. The hex values are shown in the following. If the check fails, the system will halt.

Table 4-16. LED patterns for ROM identification.

ROM	LED Value
ROM 4	0008
ROM 6	0009
ROM 8	000A
ROM A	000B
ROM C	000C

Interrupt Controller Test Setup

Entering this test, the LED pattern displays the hex value of 0010. The first step is to setup the interrupt vectors and to initialize the stack area. After that, a check is made for any pending interrupts. Then all interrupts are disabled.

Initialize Interrupt Vectors

Entering this test, the LED pattern displays the hex value of 0011. This routine initializes the vectors that are used to drive the functions defined by the interrupts.

Timer Tests

Entering this test, the LED pattern displays the hex value of 0020. This test checks each of the timers used for bus tests as well as doing a simple functional test of one of the counters.

DMA Initialization

Entering this test, the LED pattern displays the hex value of 0040. This test does a simple bus test of the DMA controller and then sets up the DMA controller for normal operation.

Power Supply Control

Entering this test, the LED pattern displays the hex value of 0080. This test does a simple write-read test of the power supply and YIG control bits. After the test is complete, the LED pattern displays the hex value of 0081 to show that the system is waiting for the power supply to turn on and reach the proper operating voltage.

Non-Volatile Memory Control Checks

Entering this test, the LED pattern displays the hex value of 0100. This is a test of the control circuits on the IO Interface Board.

Instrument Bus Check

Entering this test, the LED pattern displays the hex value of 0200. This test checks for access to the control bus interface.

Digital Bus Check

Entering this test, the LED pattern displays the hex value of 0201. This test checks for access to the display bus interface.

Initialize RAM Values

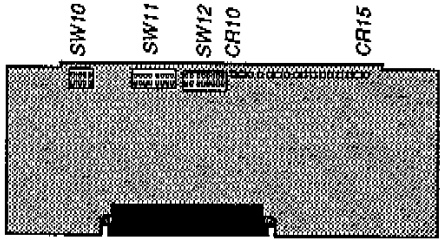
Entering this test, the LED pattern displays the hex value of 8000. This routine copies data from the ROMs into the RAM before the start of the operating system.

Advanced Diagnostics

The advanced diagnostics are started by setting the Main Processor switches.

Setting Main Processor Switches

The first method is to set switches on the main processor to select the advanced diagnostic mode. Once that has been done, select either single pass or an indefinite loop. Next, select the module to test, or select to test all modules. Then select whether to execute all tests or only one specific test. After the module and test selections are completed, the Main Processor board must be restarted for the changes to take effect and to start the tests.



A41 Main Processor Board

Figure 4-3. Main Processor board switches and LEDs.

Switch Definitions

The following table shows how the switches are defined for selecting the test mode of operation, selecting test modules, and selecting tests.

Note

All except switch number 15 are defined by the firmware. Write down the current settings before starting advanced diagnostics.

Table 4-17. Switch Configuration

Switch Number	Location	Function
15	Main Processor SW11	Normal Diagnostics/ Advanced Diagnostics
14	Main Processor SW11	Single Pass/Continuous Looping
8-13	Main Processor SW11	Module Selections
0-7	Main Processor SW12	Test Selections

Selecting Modules

The following table shows how to set switches 8 through 13 to select the module or modules to be tested. The switch positions are labeled "0" for open and "C" for closed.

Table 4-18. Module Selections

Switch Number 13	12	11	10	9	8	Module Selected
0	0	0	0	0	0	All Modules Tested
0	0	0	0	0	C	Main Processor
0	0	0	0	C	0	Memory Board
0	0	0	0	C	C	IO Interface
0	0	0	C	0	0	Comm. Interface
0	0	0	C	0	C	Proc. Extender

Selecting Tests

The exact function of the test selections switches, 0 through 7, varies from module to module. The settings for these switches will be defined where the tests for a particular module are described. To run all available tests on a module, set all of the test selection switches open.

Starting the Tests

Restart the processor system by toggling switch 10 position D on the Main Processor. The advanced diagnostics start after the power up diagnostics finish.

Main Processor User Feedback

The advanced diagnostics provide feedback to the user through the light-emitting diode (LED) indicators on the Main Processor Board, shown in Figure 4-3.. There are sixteen indicators that make up a digital word for user feedback. The indicators show the current test and module, and in addition, CR10 shows that a long test is running. If a test fails, the indicators display a set pattern. The first sign is that all the indicators turn on and then specific information about the module and test that failed is shown. If possible, the test shows additional information. The indicators are set so that CR10 is bit 15 of the data word and CR25 is bit 0.

Module or Test Selection Errors

If the switches on the Main Processor Board are not set to select the correct test module or the correct test within the module, a fault sequence is shown before normal operations continue.

If the module selection fault occurs, the upper 8 indicators flash on and off, followed by the maximum value of module that can be selected, and then by the actual module selected. This pattern is repeated several times before continuing normal operation. Note that the selected module test is ignored until a valid module is selected.

If the test selection fault occurs, the lower 8 indicators flash, followed by the maximum value of test that can be selected, and then followed by the actual test selected. This pattern is also repeated several times before normal operation is continued. This error message also shows which test has been selected.

Test Failure
If a module test fails, one of two things happens, depending on the selected mode of operation.

If the single pass mode is selected, all sixteen of the indicators will flash on and then show the module and test that failed, and the component that failed if possible. This sequence repeats until the service person terminates the test. Each test has information describing what information is displayed when an error occurs. There is no further testing until the module board test or tests are restarted. If the digital storage system is working, the current status is displayed along with any error messages that are necessary.

If continuous looping is selected, the processor repeats the failure message as before, until the main processor is reset. The looping tests can only be executed from the Main Processor switches, and not from any other point.

Main Processor Advanced Diagnostics

The following information shows how the advanced diagnostics are done for the Main Processor board. These diagnostics are in addition to the power up diagnostics and include several built-in fault isolation tools.

Built-In Diagnostic Tools
Clock Generation Circuit
Processor Address Testing
Processor Reset

The Main Processor board is a self-contained module and only requires a power supply applied to the board to be able to run the advanced diagnostics.

Built-In Diagnostic Tools

There are several tools built into the hardware to help isolate faults on the Main Processor board when that board cannot be operated normally.

Clock Generation Circuit
If there is no clock for the Microprocessor, the clock generator circuit may be defective. To help isolate the defective component it is possible to use an external clock to check the 82C84 clock generator chip. Closing Main Processor switch SW 10 position B selects the external clock on the clock generator chip. By applying an external clock of 14 MHz to 22 MHz to J10 it is possible to run the processor system.

Processor Address Testing
If the microprocessor address lines are questionable, it is possible to put the microprocessor into a self test mode that will exercise the lower sixteen address bits. This mode is started by closing Main Processor switch SW 10 position A and

resetting the microprocessor. Use an oscilloscope to check the latched address lines, LA0 to LA15, for signal levels.

Processor Reset
If the power up reset circuit is in question, it is possible to reset the microprocessor by toggling the Main Processor switch, SW 10 position D. This allows starting the microprocessor if the supply monitoring circuit is not preventing the system reset.

Processor Disable Function
If there is a problem in the 'Ready' signal to the microprocessor chip it is possible to check the circuit by putting the processor system in a loop test for the LEDs and then applying a 50 kHz signal to the 'ProcDis' pin on the edge connector, J60A pin 10. This allows checking most of the signals between the microprocessor chip and the DMA controller chip.

Main Processor Tests

The following table shows the correct switch positions to select the advanced diagnostic test. A 0 stands for an open switch, and C stands for a closed switch.

Table 4-19. Main Processor Test Selections

Switch Number 7	6	5	4	3	2	1	0	Test Selected
0	0	0	0	0	0	0	0	All Safe Tests Selected
0	0	0	0	0	0	0	C	LED Test
0	0	0	0	0	0	C	0	Switch Test
0	0	0	0	0	0	C	C	System ROM Test
0	0	0	0	0	C	0	0	RAM Test 1st Bank XOR
0	0	0	0	0	C	0	C	RAM Test 1st Bank LONG
0	0	0	0	0	C	C	0	RAM Test 1st Bank SOAK
0	0	0	0	0	C	C	C	RAM Test 2nd Bank XOR
0	0	0	0	C	0	0	0	RAM Test 2nd Bank LONG
0	0	0	0	C	0	0	C	RAM Test 2nd Bank SOAK
0	0	0	0	C	0	C	0	Interrupt Controller Bus Test
0	0	0	0	C	0	C	C	Timer Controller Bus Test
0	0	0	0	C	C	0	0	Timer Controller Functional Test
0	0	0	0	C	C	0	C	Interrupt Controller Functional Test
0	0	0	0	C	C	C	0	DMA Controller Bus Test
0	0	0	0	C	C	C	C	Power Supply YIG Control Test
C	C	C	C	C	C	C	C	Module Verification Test

All Tests Selected
This performs all of the tests for the Main Processor board. Each test executes once and then continues to the next test. Note that the RAM test performed with this selection is a short non-destructive test.

LED Test
All LEDs turn off for a short time. Then each LED turns on one at a time. After the last LED is turned on, a pattern of every other LED is turned on. After that, the data pattern is reversed. In test looping the pattern is repeated. There is no failure mode for this test, as it must be determined visually that the LEDs are working.

Switch Test
This test provides an LED display of the data read from switches SW11 and SW12. The LED associated with each switch is off for a closed switch and on for an open switch. This is a visual test, so there is no failure mode. With module looping, the data is displayed for a short time. With test looping, the switches can be opened and closed as necessary. The test repeats as long as the looping switch is closed.

System ROM Test
This test does a checksum of the system ROM, U63, on the Main Processor board. If there is an error the display first turns all the LEDs on, displays the module and test that failed, followed by the expected checksum, and then the actual checksum.

RAM Test 1st Bank XOR
The 1st Bank consists of U39, bits 8 to 15, and U60, bits 0 to 7. This is a non-destructive test of the memory devices (the contents of memory will be the same after the test as before). The test reads the data from the first memory location and stores the value. Then the data is exclusive-OR'ed (XOR'ed) with the first value and written to the same location. The data is then verified to be sure that new value has been stored correctly. If there are no errors then the processor does a second XOR test. Again if there are no errors a third XOR test is done which restores the original value. This sequence is repeated until all locations have been tested. During the test, only the module and test value are indicated.

If a failure is detected, it is indicated by first turning all LEDs on, followed by the module and test that failed. This is followed by the address that failed. This is followed by the expected data and then the data that failed. If test looping has been selected then the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 1st Bank LONG
The 1st Bank consists of U39, bits 8 to 15, and U60, bits 0 to 7. This is a destructive test of the data stored in memory (one that changes the values in memory when the test is executed). The test is based on a test method described as the "Moving Inversions Test Pattern".

Since this is a long test, the farthest left LED, CR10, blinks on and off indicating that the test is running. The LEDs also display the current test and module.

If a failure is detected, it is indicated by first turning all LEDs on, followed by the module and test that failed. This is followed by the address that failed. This is followed by the expected data and then the data that failed. If test looping has been selected then the program will attempt to read and write from the current failed address, until the system is reset.

RAM Test 1st Bank SOAK
The 1st Bank consists of U39, bits 8 to 15, and U60, bits 0 to 7. This is a destructive test of the data stored in memory, which changes the values in memory when the test is executed. This test stores a specific pattern into the ram chips, then waits about a minute and then verifies that all locations have the correct data. Three patterns are tested before the test is completed. Since this is a long test, the left most LED will blink on and off indicating that the test is running. The LEDs also display the current test and module.

If a failure is detected it is indicated by first turning all LEDs on, followed by the module and test that failed. This is followed by the address that failed. This is followed by the expected data and then the data that failed. If test looping has been selected then the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 2nd Bank XOR
The 2nd Bank consists of U29, bits 8 to 15, and U49, bits 0 to 7. This test is a non destructive test, one that will retain the memory contents after the test. The test reads the data from the first memory location and stores the value. Then the data is XOR with the first value and written to the same location. The data is then verified to insure that new value is stored correctly. If there are no errors then process does a second XOR test. Again if there are no errors a third XOR test is done which restores the original value. This sequence repeats until all locations are tested. During the test, only the module and test value are indicated.

If a failure is detected it is indicated by first turning all LEDs on, followed by the module and test that failed, the address that failed, the expected data, and then the data that failed. If test looping is selected then the program attempts to read and write from the current failed address until the system is reset.

RAM Test 2nd Bank LONG
The 2nd Bank consists of U29, bits 8 to 15, and U49, bits 0 to 7. This is a destructive test, of the data stored in memory, which changes the values in memory when the test is executed. The test is based upon a test method described as the "Moving Inversions Test Pattern". Since this is a long test, the farthest left LED blinks on and off indicating that the test is running. The current test and module are also displayed.

If a failure is detected it is indicated by first turning all LEDs on, followed by the module and test that failed, the address that failed, the expected data, and then the data that failed. If test looping is selected then the program attempts to read and write from the current failed address until the system is reset.

RAM Test 2nd Bank SOAK
The 2nd Bank consists of U29, bits 8 to 15, and U49, bits 0 to 7. This is a destructive test, of the data stored in memory, which changes the values in memory when the test is executed. This test is will store a specific pattern into the ram chips then wait about a minute and then verify that all locations have the correct data. There are three patterns that are tested before the test is completed. Since this is a long test the left most LED will blink on and off indicating that the test is running. The LEDs also display the current test and module.

If a failure is detected it is indicated by first turning all LEDs on, followed by the module and test that failed, the address that failed, the expected data, and then the data that failed. If test looping is selected then the program attempts to read and write from the current failed address until the system is reset.

Interrupt Controller Bus Test
There are two simple tests for the Interrupt Controller chip. The first test verifies that the data bus to and from the Interrupt Controller chip is functional, and the second test checks that no interrupts have occurred that are still pending after the test is complete.

If there is a failure detected it is indicated by first turning all the LEDs on, followed by the module and test failed. The address that failed is displayed next, followed by the expected data and the actual data that failed.

Timer Controller Bus Test
There are several simple tests for checking the bus interface to the Timer Controller chip. Each of these tests program one of the timers for a mode of operation, verifies that it is programmed, and then verifies that the counter was programmed correctly. The following table shows how the timers are programmed during each test.

Table 4-20. Timer Test Configurations

Test Number	Timer Select	Byte Set	Mode Select	Count Mode
1	0	MSB	0	BCD
2	0	LSB	1	Binary
3	1	LSB	2	BCD
4	1	MSB	3	Binary
5	2	MSB	4	BCD
6	2	LSB	5	Binary

If there is a failure detected it is indicated by first turning all the LEDs on, followed by which module and test failed. The address that failed is displayed next, followed by expected data and the actual data that failed.

Timer Controller Functional Test
This test sets each of the timers to mode 2, square wave, but at different frequencies. The first output divides the processor bus clock by 2, the second timer by 4, and the third timer by 8. The test then delays so that the outputs can be checked with a scope at their test points to verify the timer outputs. The Main Processor board test points are as follows:

Table 4-21. Timer output test points.

Timer Number	Test Point
Timer 1	TP11
Timer 2	TP12
Timer 3	TP13

This test checks the timer outputs for the proper logic levels. This allows verifying that the outputs are working.

Interrupt Controller Functional Test
This test checks that the output of the Timer Controller is being received by the Interrupt Controller. The test sets the first timer into a constant square wave output. The interrupt vectors point to a dummy routine that returns a value when called.

If there is a failure detected it is indicated by first turning all the LEDs on, followed by the module and test that failed. The expected data and the actual data that failed is displayed next.

DMA Controller Bus Test
This is a basic write and verify test for three of the internal registers on the DMA Controller Chip. This test writes every possible bit pattern to each of the registers. The first step is to initialize the DMA controller chip and to define the data width.

If there is a failure detected it is indicated by first turning all the LEDs on, followed by which module and test failed. The address that failed is displayed next, followed by expected data and the actual data that failed.

Power Control YIG Control Test
This is a basic write and verify test for the latch and buffer controlling the fan speed, YIG power supply, and the power supply control lines. The test writes a data pattern out and then verifies that the correct data is stored.

If there is a failure detected it is indicated by first turning all the LEDs on, followed by which module and test failed. The expected data and the actual data, that was returned, is displayed next.

Module Verification Test
This test executes the selected tests for verifying the operation of the Main Processor board. The following tests may be selected.

LED Test
Switch Test
System ROM Test
RAM Test 1st Bank LONG
RAM Test 2nd Bank LONG
Interrupt Controller Bus Test
Timer Controller Bus Test
Timer Controller Functional Test
Interrupt Controller Functional Test
DMA Controller Bus Test
Power Supply YIG Control Test

Caution

These are destructive tests, and will change the values in memory. If possible, download any important data before running these tests.

Memory Board Advanced Diagnostics

The following information describes the advanced diagnostics for the Memory board. For execution of the advanced diagnostics the Memory board requires that there is a working Main Processor board, an interconnect board or extender board, and the correct power supply voltages.

The following table shows the correct switch positions for selecting the advanced diagnostic tests. "0" stands for open switch, and "C" stands for a closed switch. These are positions 0 through 7 on switch SW12 on the Main Processor board.

Table 4-22. Memory Board Test Selections

Switch Number 7	6	5	4	3	2	1	0	Test Selected
0	0	0	0	0	0	0	0	All Safe Tests Selected
0	0	0	0	0	0	0	C	RAM Test 3rd Bank XOR
0	0	0	0	0	0	C	0	RAM Test 3rd Bank LONG
0	0	0	0	0	0	C	C	RAM Test 3rd Bank SOAK
0	0	0	0	0	C	0	0	RAM Test 4th Bank XOR
0	0	0	0	0	C	0	C	RAM Test 4th Bank LONG
0	0	0	0	0	C	C	0	RAM Test 4th Bank SOAK
0	0	0	0	0	C	C	C	ROM 4 Test
0	0	0	0	C	0	0	0	ROM 6 Test
0	0	0	0	C	0	0	C	ROM 8 Test
0	0	0	0	C	0	C	0	ROM A Test
0	0	0	0	C	0	C	C	ROM C Test
C	C	C	C	C	C	C	C	Module Verification Test

The tests are done in the sequence show above.

RAM Test 3rd Bank XOR

The 3rd Bank consists of U16, bits 8 to 15, and U20, bits 0 to 7. This test is a non-destructive test, one that retains the contents of memory. The test reads the data from the first memory location and stores the value read. Then the data is XOR'ed with the first value and written to the same location. The data is then verified to be sure that the new value is stored correctly. If there are no errors then the processor does a second XOR test. Again if there are no errors a third XOR test is done which will restore the original value. This sequence repeats until all locations are tested. During the test, only the module and test value are indicated.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping has been selected then the program attempts to read and write from the current failed address until the system is reset.

RAM Test 3rd Bank LONG

The 3rd Bank consists of U16, bits 8 to 15, and U20, bits 0 to 7. This is a destructive test of the data stored in memory, which changes the values in memory when the test is executed. The test is based upon a test method described as the "Moving Inversions Test Pattern". Since this is a long test the farthest left LED blinks on and off indicating that the test is running. The current test and module are also displayed.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping is selected, the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 3rd Bank SOAK

The 3rd Bank consists of U16, bits 8 to 15, and U20, bits 0 to 7. This is a destructive test of the data stored in memory, which changes the values in memory when the test is executed. This test stores a specific pattern into the ram chips, waits about a minute, and then verifies that all locations have the correct data. There are three patterns that are tested before the test is completed. Since this is a long test the farthest left LED will blink on and off indicating that the test is running. The current test and module are also displayed.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping is selected, the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 4th Bank XOR

The 4th Bank consists of U15, bits 8 to 15, and U19, bits 0 to 7. This test is a non-destructive test, one that retains the contents of memory. The test reads the data from the first memory location and stores the value read. Then the data is XOR'ed with the first value and written to the same location. The data is then verified to be sure that the new value is stored correctly. If there are no errors then the processor does a second XOR test. Again if there are no errors a third XOR test is done which will restore the original value. This sequence repeats until all locations are tested. During the test, only the module and test value are indicated.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping is selected, the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 4th Bank LONG

The 4th Bank consists of U15, bits 8 to 15, and U19, bits 0 to 7. This is a destructive test of the data stored in memory, which changes the values in memory when the test is executed. The test is based upon a test method described as the "Moving Inversions Test Pattern". Since this is a long test the farthest left LED blinks on and off indicating that the test is running. The current test and module are also displayed.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping is selected, the program will attempt to read and write from the current failed address until the system is reset.

RAM Test 4th Bank SOAK

The 4th Bank consists of U15, bits 8 to 15, and U19, bits 0 to 7. This is a destructive test, of the data stored in memory, which changes the values in memory when the test is executed. This test is will store a specific pattern into the ram chips then wait about a minute and then verify that all locations have the correct data. There are three patterns that will be tested before the test is completed. Since this is a long test the left most LED will blink on and off indicating that the test is running. The LEDs also display the current test and module.

If a failure is detected it is indicated by first turning all LEDs on, followed by which module and test failed. This is followed by the address that failed, the expected data, and then the data that failed. If test looping is selected, the program will attempt to read and write from the current failed address until the system is reset.

ROM 4 Test

This does a check sum of the system EPROM on the Memory Board, U11. If there is an error the display will first turn all the LEDs on, then display the module and test that failed, followed by the expected checksum, and then the actual checksum.

ROM 6 Test

This does a check sum of the system ROM on the Memory Board, U12. If there is an error the display will first turn all the LEDs on, then display the module and test that failed, followed by the expected checksum, and then the actual checksum.

ROM 8 Test

This does a check sum of the system ROM on the Memory Board, U13. If there is an error the display will first turn all the LEDs on, then display the module and test that failed, followed by the expected checksum, and then the actual checksum.

ROM A Test

This does a check sum of the system ROM on the Memory Board, U14. If there is an error the display will first turn all the LEDs on, then display the module and test that failed, followed by the expected checksum, and then the actual checksum.

ROM C Test

This does a check sum of the system ROM on the Memory Board,U10. If there is an error the display will first turn all the LEDs on, then display the module and test that failed, followed by the expected checksum, and then the actual checksum.

Module Verification Test

This test will execute the selected tests for verifying the operation of the Main Processor board. The same tests described above will be executed, but only the following tests will be performed:

RAM Test 3rd Bank LONG
RAM Test 4th Bank LONG
ROM 4 Test
ROM 6 Test
ROM 8 Test
ROM A Test
ROM C Test

IO Interface Advanced Diagnostics

The following information describes the advanced diagnostics for the IO Interface board. For execution of the advanced diagnostics, the IO Interface requires that there is a working Main Processor board, a working Memory Board, an interconnect board or extender board, and the correct power supply voltages.

The following table shows the correct switch positions to select the advanced diagnostic tests. A "0" stands for open switch, and a "C" stands for a closed switch. The switch is SW12 on the Main Processor board.

Table 4-23. IO Interface Test Selections

Switch Number 7 6 5 4 3 2 1 0	Test Selected
0 0 0 0 0 0 0 0	All Tests Selected
0 0 0 0 0 0 0 C	NVRAM

The tests are done in the sequence shown above.

NVRAM

If All Tests is selected, the check for the NVRAM is a non-destructive test. This allows verifying that the NVRAM is usable without changing the data stored.

If the actual test has been selected then the program will execute a destructive test, leaving the entire NVRAM cleared.

CAUTION

Any data stored in NVRAM will be lost if this test is run. Be sure to back up stored data before running this test.

All the LEDs turn on to indicate a failure has occurred. Then the module and test are shown, followed by the current block selected. The block address is shown next, followed by the expected data. After which the actual data is presented. This pattern is repeated until the system is reset.

Table 4-24. RAM Block Locations

Upper 8 Bits LED Pattern	NVRAM Location Lower	Upper
A0	U14	U40
A8	U15	U39
B0	U12	U38
B8	U13	U37

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques and procedures that may be required to remove and replace assemblies and/or components in this instrument are described here.

Handling Static Sensitive Components

Most semiconductor types, both separately and in assemblies, are susceptible to damage to static charge. See Table 4-1, at the start of this section, for voltage levels. Use static sensitive procedures whenever handling semiconductors or assemblies containing them.

Obtaining Replacement Parts

Replacement assemblies and parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts.

Parts orientation and lead dress should be duplicated because some components are oriented to reduce interaction between circuits or to control circuit characteristics.

Where applicable, an improved part will be substituted when a replacement is ordered. If the change is complex, your local Field Office or representative will contact you concerning the change. After repair, the circuits may need recalibration.

Module Exchange Program

The TEKTRONIX 2782 Spectrum Analyzer has been designed with a module exchange service approach. Service is performed by identifying a faulty module and exchanging it with a properly functioning module. This information details the process for obtaining a properly operating module from Tektronix. A list of the exchangeable modules is contained in the Replaceable Electrical Parts List.

Note

Module service and exchange should be performed by qualified service personnel only.

Module Exchange Service (U.S. Customers)

To obtain a properly operating module, please call the Tektronix Module Exchange Center between the hours of 6:00 AM and 5:00 PM (Pacific Time) Monday through Friday, at the following telephone number:

1-800-TEKWIDE, Ext. MR8600 (for Service Assistance)

The person answering the call will confirm the availability of a proper operating module and arrange shipping within 72 hours of the confirmation. (Most modules will be shipped within 24 hours of the request.)

Module shipment will be made by your choice of carrier. (e,g, - priority, express, one-day, overnight delivery, or common carrier service). After you receive the replacement module, the faulty module must be returned immediately to Tektronix via prepaid common carrier freight. Use the packaging material from the replacement module to prepare the faulty module for return shipment. A return shipping label will be furnished with the replacement module.

A standard fee is charged for each out-of-warranty module exchanged, and will be quoted when the exchange module is requested. If the faulty module is not received at the Module Exchange Center within 15 working days after the original request, the full price of the module will be charged.

Full price will also be charged for modules returned that do not qualify for the Module Exchange Program. Modules are not acceptable for exchange rates if they are:

- Damaged from repair attempts (other than by Tektronix)
- Damaged from improper use or connection to incompatible equipment
- Modified by the customer
- Custom modified by Tektronix (by customer order)

The Module Exchange Center can provide further details on pricing, invoicing, and shipping methods.

Service for Customers Outside of the U.S.

Customers outside the United States should contact their local Tektronix sales subsidiary or distributor for details on servicing.

Firmware Version and Error Message Readout

This feature provides readout of the firmware version when the power on/off is cycled. During the initial power-up cycle, the instrument firmware version is displayed on the crt for a short time. Firmware may be updated by replacing the ROMs. (Also see the information in this section titled 'Updating Firmware' and the appendix titled 'Firmware Versions'.)

When an error occurs, a message appears on the screen describing the nature of the error. Status messages or prompts are also displayed when running a diagnostic test or self correction routine.

Removing or Replacing Semi-rigid Coaxial Cables

Performance of the instrument may be degraded if the connectors on semi-rigid cables are loose, dirty, or damaged. The following procedure will help ensure that the connection is good enough to maintain proper performance.

- ❑ 1. Use a 5/16 " open-end wrench to loosen or tighten the connectors. It is good practice to use a second wrench to hold the rigid (receptacle) portion of the connector to prevent bending or twisting the cable.
- ❑ 2. Ensure that the plug and receptacle are clean and free of any foreign matter.
- ❑ 3. Insert the plug connector fully into the receptacle before screwing the nut on. Tighten the connection to 8 in-lbs to ensure that the connection is tight. Do not over-tighten (15 to 20 in-lbs) because this can damage the connector.

Torque Specifications

SMA connectors and K connectors, as noted above, are tightened to 8 in-lbs.

Torx T-10 screws are tightened to 5 in-lbs unless otherwise noted.

Posidrive screws are tightened to 10 in-lbs unless otherwise noted.

Replacing Assemblies

When replacing assemblies, prepare the instrument for service, and use the following illustrations as a guide to locate the assembly locations.

Note

Removal of any assembly with SMA connectors in the signal path requires checking and readjusting flatness. If you do not have the equipment required to check flatness, we recommend returning the instrument to Tektronix for repair and adjustment.

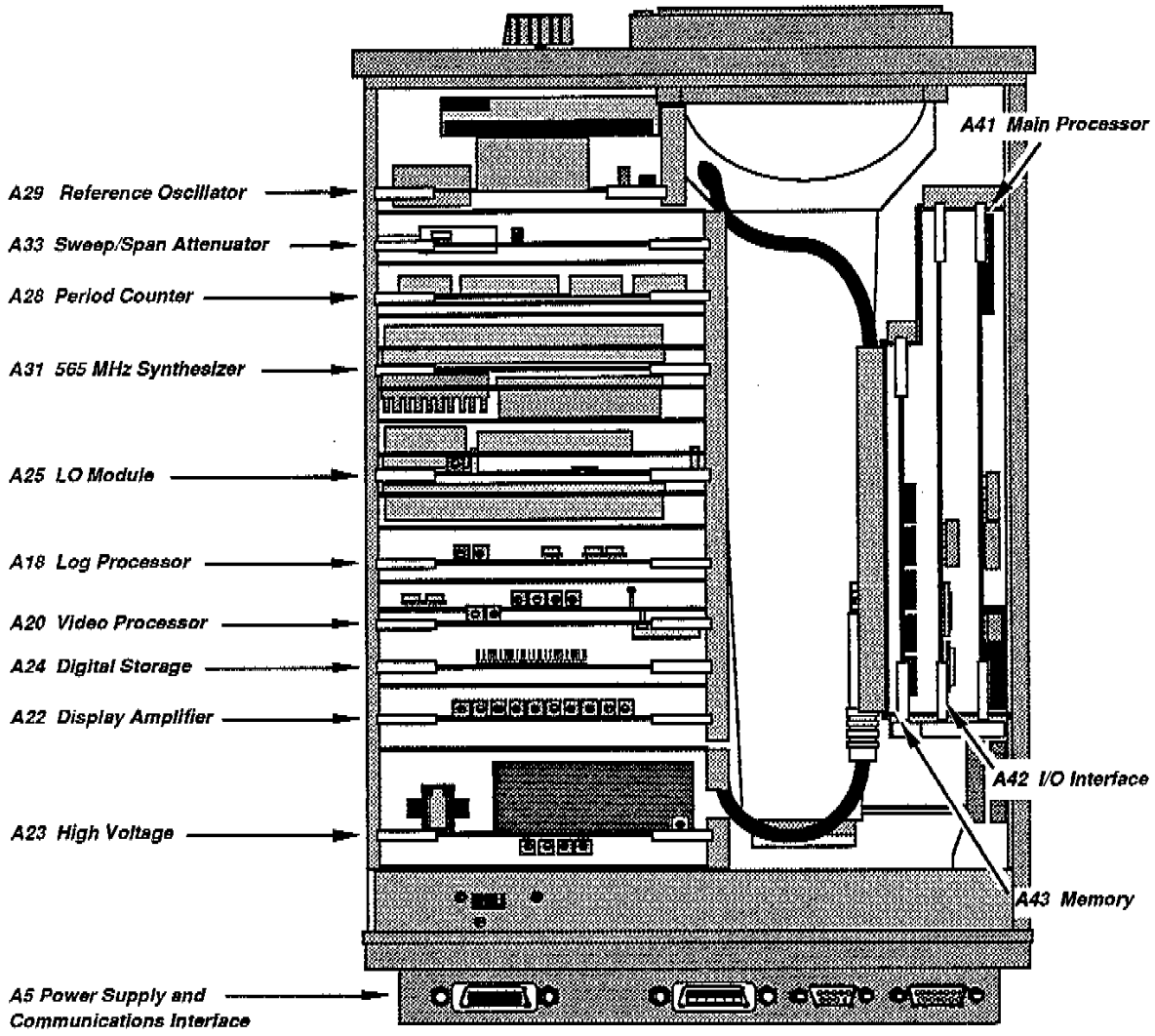


Figure 4-4. 2782 Top Deck assembly locations.

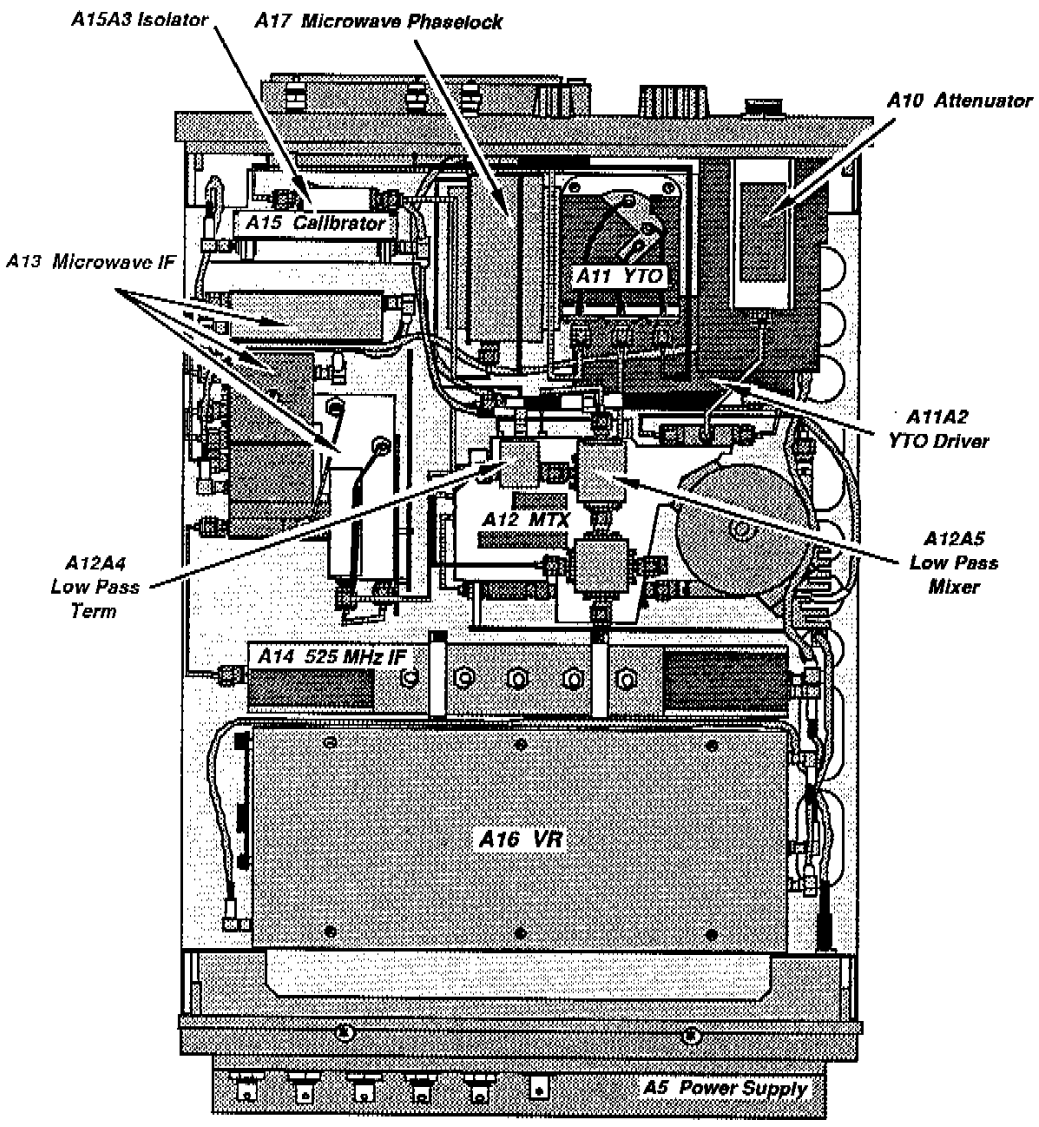


Figure 4-5. 2782 Bottom Deck (RF Assemblies).

Replacing the RF Attenuator (A10)

Removing the RF Attenuator

❑ 1. Remove the 5/16" SMA connector from the rear of the attenuator. If necessary, loosen the connector on the other end of the cable to allow moving the cable out of the way while removing the RF Attenuator. Do not bend the semi-rigid coaxial cable.

❑ 2. Remove the 3/4" nut from the front panel RF INPUT 50Ω connector.

❑ 3. Gently pull the Attenuator assembly backwards to disconnect the circuit board connector from the Front Panel circuit board assembly. If needed, apply slight pressure on the corner of the Front Panel assembly. Be careful to not damage the YTO Driver assembly (A11A2) beneath the RF Attenuator.

Installing the RF Attenuator

❑ 1. Reverse the removal procedure. Tighten the SMA connector to 8 in-lbs. Do not over tighten.

❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

❑ 3. Run the following Vertical Self-Correction routines:

- Attenuator Correction
- Display Law Correction
- Gain Step Correction
- VR Resonator Correction
- ResBW Correction

Replacing the MTX Assembly (A12)

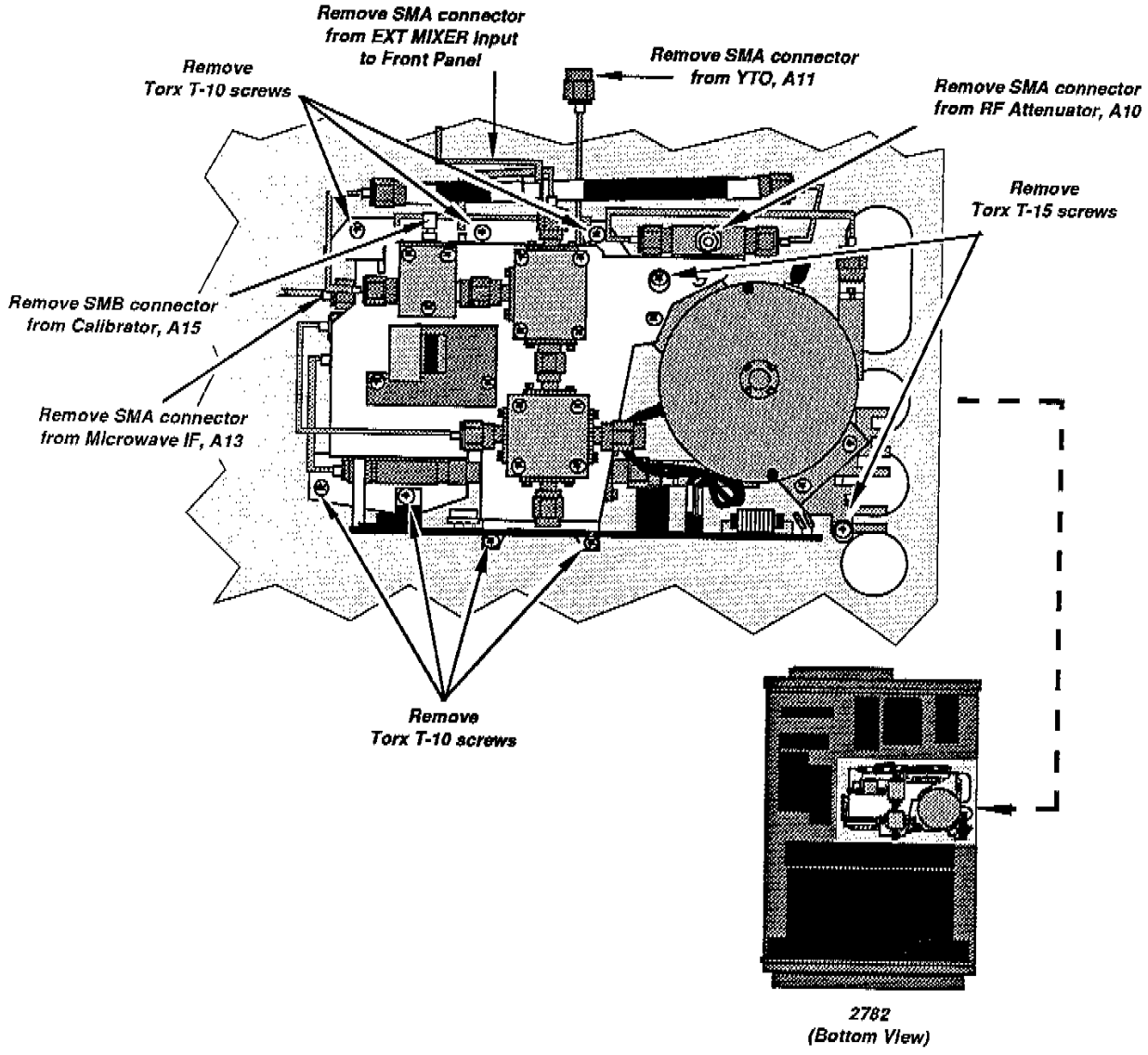


Figure 4-6. Removing the MTX Assembly (A12).

Removing the MTX Assembly

The MTX assembly may be replaced as a unit. Individual subassemblies that may be replaced are the Low Pass Termination (A12A4) and the Low Pass Mixer (A12A5). Procedures for removing these items follow the main MTX removal procedure.

Use the following procedure to remove the MTX Assembly:

- ❑ 1. Disconnect the 5/16" SMA connector from the RF Attenuator (A10) at the MTX end.
- ❑ 2. Disconnect the SMA connector from the YTO (A11) at the YTO end.
- ❑ 3. Disconnect the Low Pass filter, FL100, from the Microwave IF at the MTX end.
- ❑ 4. Disconnect the External Mixer Input cable at the front panel.
- ❑ 5. Disconnect the SMB connector from the Calibrator (A15) at the MTX end.
- ❑ 6. Remove the six Torx T-10 and two T-15 screws as shown. Use a T-10 screwdriver or bit with 3" clearance to reach the screws next to the 525 MHz IF (A14).
- ❑ 7. Remove the MTX assembly from the chassis. Be careful to not bend any semi-rigid coaxial cables. If necessary, loosen or remove connectors at their associated assemblies to provide clearance for the MTX assembly.

Installing the MTX Assembly

- ❑ 1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.
- ❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.
- ❑ 3. Run the following Vertical Self-Correction routines:
  - Attenuator Correction
  - Display Law Correction
  - Gain Step Correction
  - VR Resonator Correction
  - ResBW Correction

Removing the MTX Low Pass Termination (A12A4)

- ❑ 1. Disconnect the two 5/16" SMA connections and one SMB connection to the assembly.
- ❑ 2. Remove the three Posidrive P1 screws from the top of the assembly.
- ❑ 3. Remove the assembly.

Installing the MTX Low Pass Termination Assembly

- ❑ 1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.

❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

❑ 3. Run the following Vertical Self-Correction routines:

- Attenuator Correction
- Display Law Correction
- Gain Step Correction
- VR Resonator Correction
- ResBW Correction

Removing the MTX Low Pass Mixer (A12A5)

❑ 1. Disconnect the three 5/16" SMA connections to the assembly.

❑ 2. Remove the four Posidrive P1 screws from the top of the assembly.

❑ 3. Remove the assembly.

Installing the MTX Low Pass Mixer Assembly

❑ 1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.

❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

❑ 3. Run the following Vertical Self-Correction routines:

- Attenuator Correction
- Display Law Correction
- Gain Step Correction
- VR Resonator Correction
- ResBW Correction

Replacing the YTO Assembly (A11)

The YIG Tuned Oscillator, YTO, Assembly (A11) is replaceable as two units; the YTO with its interface board (A11) and the YTO Driver (A11A2).

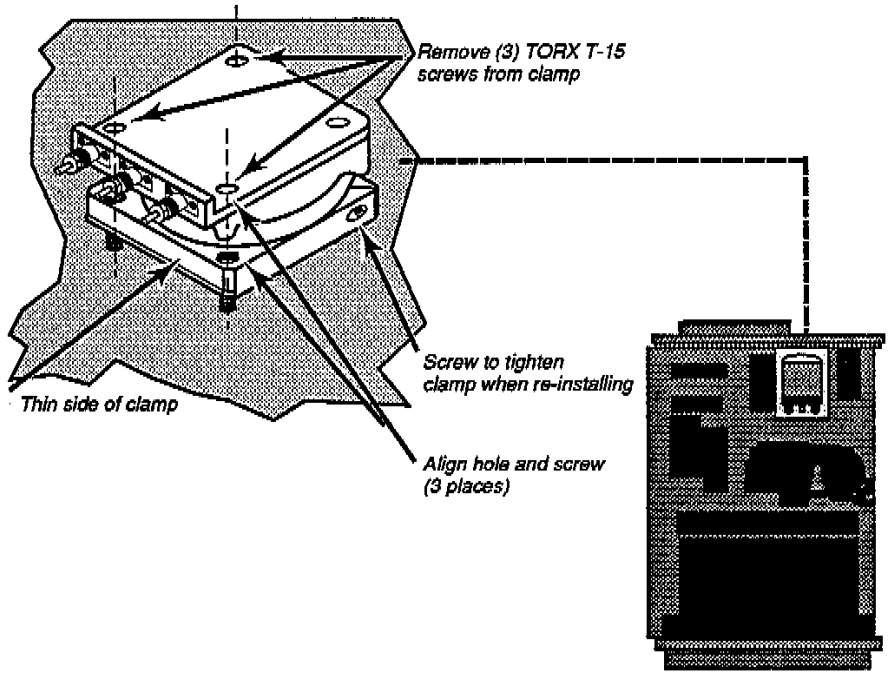


Figure 4-7. Removing the YTO Assembly (A11)

Removing the YTO Assembly

- ❑ 1. Disconnect the three 5/16" SMA connectors from the YTO Assembly.
- ❑ 2. Remove the four 7/64" Allen (Hex) screws from the YTO Assembly.
- ❑ 3. Gently pull the YTO Assembly away from the chassis to disconnect it from the YTO Driver Assembly (A11A2).

Installing the YTO Assembly

- ❑ 1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.
- ❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

Removing the YTO Driver Assembly (A11A2)

- ❑ 1. Remove the YTO Assembly using the previously described procedure.
- ❑ 2. Remove the Torx T-10 screws as shown in the accompanying illustration.
- ❑ 3. Gently pull the YTO Driver Assembly away from the chassis to disconnect it from the Mother Board Assembly (A1).

Installing the YTO Driver Assembly

- ❑ 1. Reverse the removal procedure. When replacing the YTO Assembly, tighten all SMA connectors to 8 in-lbs. Do not over tighten.
- ❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

Replacing the Microwave IF Assembly (A13)

The Microwave IF Assembly (A13) is replaceable as a single item. The assembly consists of two groups of subassemblies connected by cables. Both groups must be replaced as a unit. Removal of the assembly involves the following connections:

Removing the Microwave IF Assembly

- ❑ 1. Disconnect the two 5/16" SMA connectors and two SMB connectors shown in the illustration.
- ❑ 2. Remove the Torx T-10 screws.
- ❑ 3. Gently lift the main assembly by the circuit board to disconnect the edge connector from the Mother Board (A1).
- ❑ 4. Remove the two Microwave IF subassembly groups, with remaining cables attached.

Installing the Microwave IF Assembly

- ❑ 1. Reverse the removal procedure. Tighten the SMA connectors to 8 in-lbs. Do not over tighten.
- ❑ 2. Check and adjust instrument flatness. See the Adjustment Procedure.

Replacing the Calibrator (A15) and Isolator (A15A3)

Removing the Calibrator and Isolator

- ❑ 1. Disconnect the three SMB and two SMA connectors.
- ❑ 2. Remove the four Torx T-10 screws.
- ❑ 3. Gently lift the assembly to disconnect the edge connector from the Mother Board (A1).
- ❑ 4. Remove the four screws holding the Isolator (A15A3) to the Calibrator.

Installing the Calibrator and Isolator

- ❑ 1. Reverse the removal procedure. Tighten the SMA connectors to 8 in-lbs. Do not over tighten.

Replacing the Microwave Phaselock (A18)

Removing the Microwave Phaselock

- ❑ 1. Disconnect the 5/16" SMA connector.
- ❑ 2. Remove the four Torx T-10 screws.
- ❑ 3. Gently lift the assembly to disconnect the edge connector from the Mother Board (A1).
- ❑ 4. Disconnect the SMB connector.

Installing the Microwave Phaselock

- ❑ 1. Reverse the removal procedure. Tighten the SMA connector to 8 in-lbs. Do not over tighten.
- ❑ 2. Check and adjust offset. See the Adjustment Procedure for instructions.

Replacing the 525 MHz IF (A14)

Removing the 525 MHz IF

- ❑ 1. Disconnect the 5/16" SMA connector.
- ❑ 2. Disconnect the SMB connectors.
- ❑ 3. Remove the Torx T-10 screws. Use a screwdriver with 3" clearance to reach the screws.
- ❑ 4. Gently lift the assembly to disconnect the edge connector from the Mother Board (A1).

Installing the 525 MHz IF

- ❑ 1. Reverse the removal procedure. Tighten the SMA connector to 8 in-lbs. Do not over tighten.

Replacing the VR Assembly (A16)

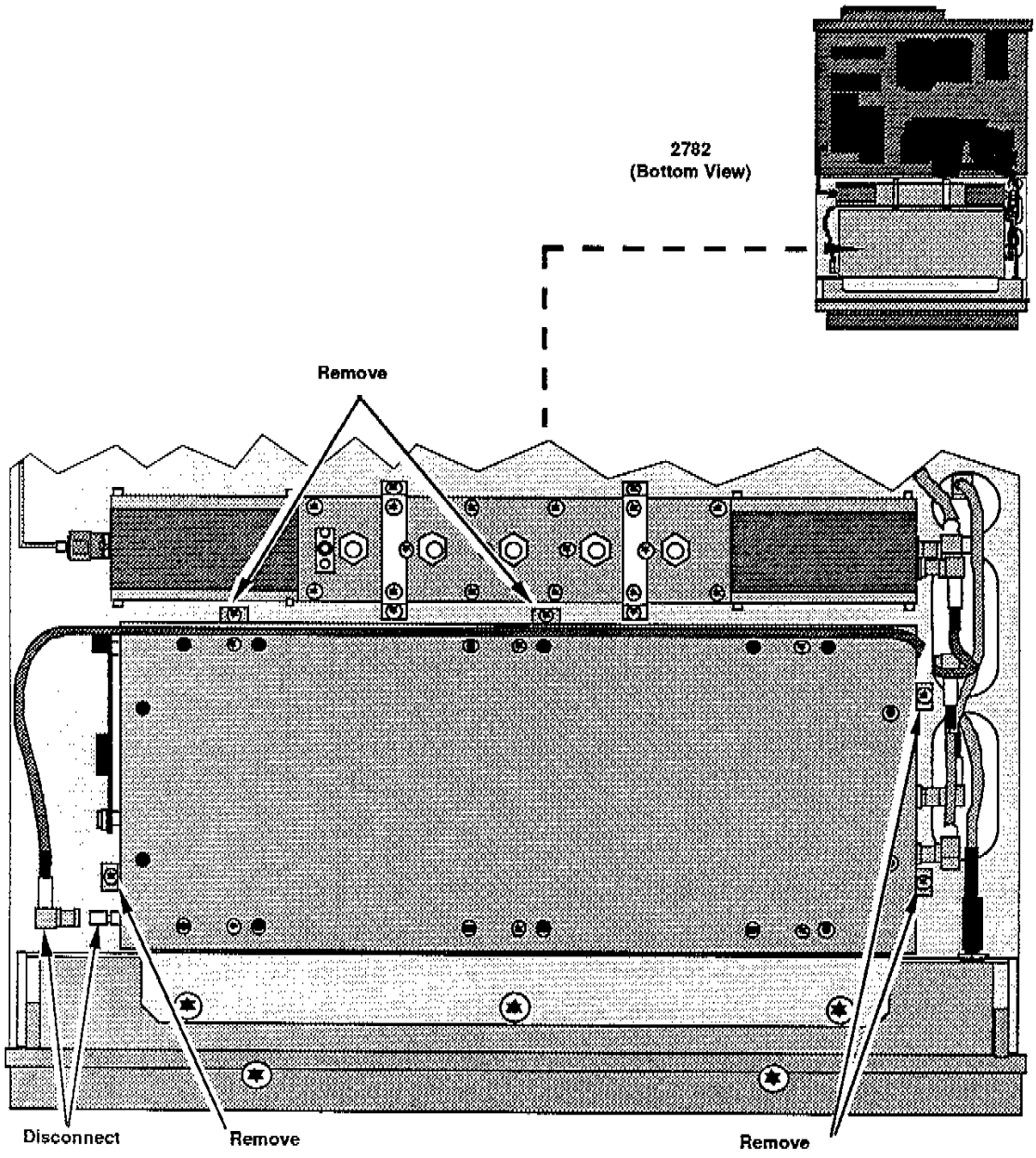


Figure 4-8. Removing the VR Assembly (A16).

Removing the VR Assembly

❑ 1. Disconnect the SMB connectors.

❑ 2. Remove the Torx T-10 screws. Use a screwdriver with 3" clearance to reach the screws next to the 525 MHz IF (A14).

❑ 3. Gently lift the assembly to disconnect the edge connector from the Mother Board (A1).

Installing the VR Assembly

❑ 1. Reverse the removal procedure.

❑ 2. Run the following Vertical Self-Correction routines:

- Display Law Correction
- Gain Step Correction
- VR Resonator Correction
- ResBW Correction

Removing the Card Cage Covers

Circuit cards on the top side of the instrument are covered with metal shields. Separate shields cover the main card cage, the High Voltage assembly, and the processor system card cage. The main card cage shield and the High Voltage assembly shield hook over the outside edge of the card cage, and are held by Torx T-10 screws on the inside edge of the card cage. The processor system shield is similar, but is secured with screws on both sides. The following figure shows the card cage cover locations.

Note

If you remove the covers from the top deck, place a sheet of paper over the exposed assemblies to provide proper air flow by the fan.

Card Cage Covers

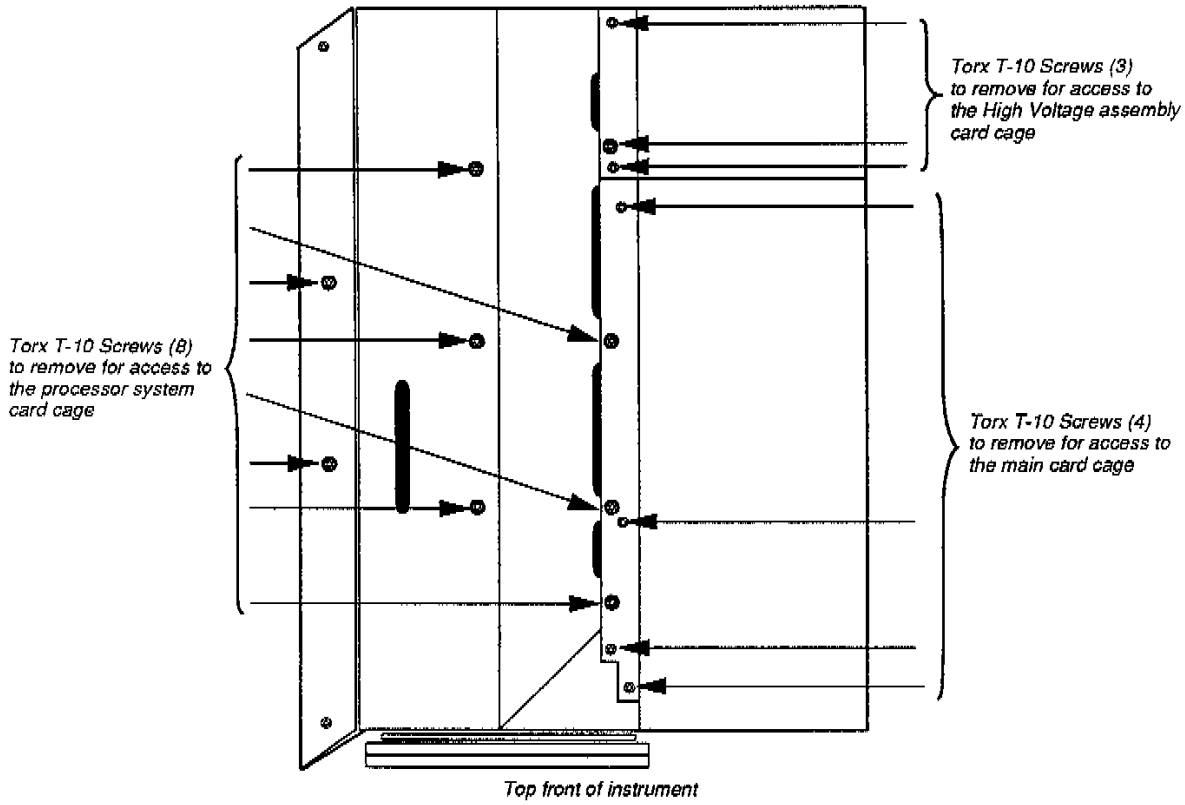


Figure 4-9. Removing the Card Cage covers.

Replacing the Reference Oscillators (A29)

Removing the Reference Oscillators

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Disconnect the SMB connector on the bottom of the assembly, from the RF deck side of the instrument, through the chassis hole. If necessary, disconnect the other end of the cable from the Microwave IF (A13).
- ❑ 3. Remove the assembly from the card cage using the circuit board levers.

Installing the Reference Oscillators

- ❑ 1. Reverse the removal procedure.

Replacing the Sweep/Span Attenuator (A33)

Removing the Sweep/Span Attenuator

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Remove the assembly from the card cage using the circuit board levers.

Installing the Sweep/Span Attenuator

- ❑ 1. Reverse the removal procedure.

Replacing the Period Counter (A28)

Removing the Period Counter

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Unseat the assembly from the Mother Board edge connector using the two board levers, and gently lift out of the card cage until the SMB connector on the bottom of the assembly is accessible.
- ❑ 3. Disconnect the SMB connector.
- ❑ 4. Remove the assembly from the card cage.

Installing the Period Counter

- ❑ 1. Reverse the removal procedure.

Replacing the 565 MHz Synthesizer (A31)

Removing the 565 MHz Synthesizer

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Remove the assembly from the card cage using the circuit board levers.

Installing the 565 MHz Synthesizer

- ❑ 1. Reverse the removal procedure.

Replacing the LO Module (A25)

Removing the LO Module

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Disconnect the SMB connector on the bottom of the assembly, from the RF deck side of the instrument, through the chassis hole. If necessary, disconnect the other end of the cable from the Microwave Phaselock (A17).
- ❑ 3. Disconnect the SMB connector.
- ❑ 4. Remove the assembly from the card cage using the circuit board levers.

Installing the LO Module

- ❑ 1. Reverse the removal procedure.

Replacing the Log Processor (A18)

Removing the Log Processor

- ❑ 1. Remove the main card cage cover.
- ❑ 2. Remove the assembly from the card cage using the circuit board levers.

Installing the Log Processor

- ❑ 1. Reverse the removal procedure.
- ❑ 2. Run the following Vertical Self-Correction routines:

  - Display Law Correction
  - Log Correction
  - Gain Step Correction
  - VR Resonator Correction
  - ResBW Correction

Replacing the Video Processor (A20)

Removing the Video Processor

❑ 1. Remove the main card cage cover.

❑ 2. Remove the assembly from the card cage using the circuit board levers.

Installing the Video Processor

❑ 1. Reverse the removal procedure.

❑ 2. Readjust the Video Processor Vertical Gain (VGAIN), Vertical Offset (VOFF), CLAMP, Horizontal Gain (HGAIN), and Horizontal Offset (HOFF).

❑ 3. Run the Vertical Display Law Corrections and Peak Detector Corrections, and the Frequency Corrections from the self correction menus.

Replacing the Digital Storage (A24)

Note

Firmware ROMs are ordered separately from the boards. If the ROMs are bad, just order the replacement ROM set. If the board is being replaced, use the old ROMs in the replacement board.

Removing the Digital Storage

❑ 1. Remove the main card cage cover.

❑ 2. Remove the assembly from the card cage using the circuit board levers.

❑ 3. Remove the firmware ROMs from the board using an IC extraction tool. See Updating Firmware, later in this section, for ROM locations.

Installing the Digital Storage

❑ 1. Reverse the removal procedure.

❑ 2. Replace the Digital Storage firmware ROM, U11. See Updating Firmware, later in this section, for the ROM location.

❑ 3. Readjust the Video Processor and Display Amplifier adjustments.

Replacing the Display Amplifiers (A22)

Removing the Display Amplifiers

❑ 1. Remove the main card cage cover.

❑ 2. Remove the assembly from the card cage using the circuit board levers.

Installing the Display Amplifiers

❑ 1. Reverse the removal procedure.

❑ 2. Readjust the Display Amplifier adjustments.

Replacing the HV Power Supply (A23)

Warning

The crt anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short the anode lead to the main chassis immediately after disconnecting the lead. Hold the lead to the chassis until the crt is fully discharged. This may take several minutes.

Caution

The high voltage charge on the anode lead can damage other circuits in this instrument. Be sure to fully discharge the anode lead to the main chassis, as described above.

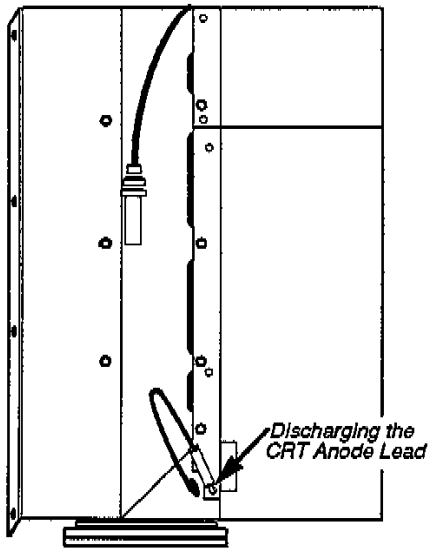


Figure 4-10. Discharging the CRT anode lead to the chassis.

Removing the HV Power Supply

❑ 1. Disconnect the multi-pin connector from the top of the assembly.

❑ 2. Unseat the assembly from the Mother Board edge connector using the two board levers, and gently lift out of the card cage until two more multi-pin connectors on the crt side of the assembly are accessible.

❑ 3. Disconnect the two remaining multi-pin connectors.

❑ 4. Remove the assembly from the card cage.

Installing the HV Power Supply

❑ 1. Reverse the removal procedure.

❑ 2. Readjust the High Voltage adjustments.

Replacing the Main Processor System Boards (A41, A42, and A43))

The Main Processor System consists of the Main Processor (A41), the I/O Interface (A42), and the Memory (A43) – all located in the Main Processor card cage; and the Communications Interface (A5A6), which is physically located in the Power Supply assembly (A5). This procedure is for the card cage assemblies only. A separate procedure for replacing the Communications Interface is described with the other Power Supply assemblies.

Note

Firmware ROMs are ordered separately from the boards. If the ROMs are bad, just order the replacement ROM set. If the board is being replaced, keep the old ROMs.

Removing the Main Processor System Boards

❑ 1. Remove the processor card cage cover.

❑ 2. Remove the desired assembly from the card cage using the circuit board levers.

❑ 3. Remove the firmware ROMs from the board using an IC extraction tool. See Updating Firmware, later in this section, for ROM locations.

Installing the Main Processor System Boards

❑ 1. Reverse the removal procedure.

❑ 2. Replace the firmware ROMs to their proper sockets. See Updating Firmware, later in this section, for ROM locations.

Replacing the LV Power Supply and Communications Interface (A5)

Removing the LV Power Supply

- ❑ 1. Remove the three Torx T-10 screws attaching the Power Supply to the bottom rear chassis bracket.
- ❑ 2. Remove the four Posidrive screws attaching the Power Supply to the side rails at the rear of the chassis.
- ❑ 3. Move the assembly away from the chassis, then disconnect the three ribbon cables from the Mother Board (A1) at locking connectors A1J22, A1J23, and A1J24. Label the cables going to J23 and J24, if they are not already labeled, to help re-install them properly.
- ❑ 4. Disconnect the SMB connector.
- ❑ 5. Remove the Power Supply assembly.

Installing the LV Power Supply

- ❑ 1. Reverse the removal procedure.

Disassembling the LV Power Supply Halves

- ❑ 1. Open the Power Supply assembly by removing the four Torx T-10 screws from the top and bottom of the assembly.
- ❑ 2. Disconnect the SMB connector on the end of the IF OUT coaxial cable, A5W516.
- ❑ 3. Disconnect the two multi-pin connector cables.

Assembling the LV Power Supply Halves

- ❑ 1. Reverse the disassembly procedure.

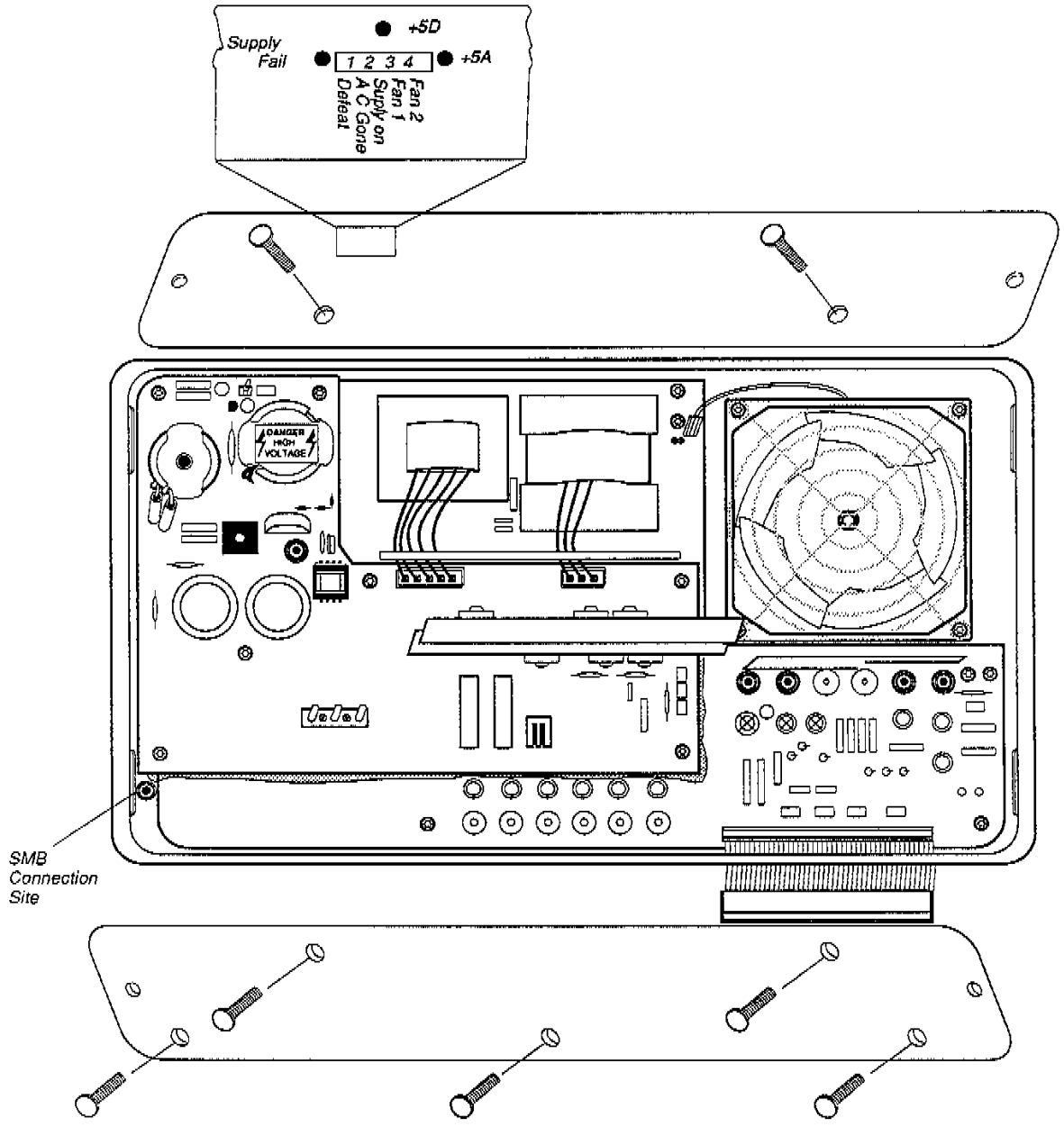


Figure 4-11. Removing the LV Power Supply.

Replacing the Thermal Fuse (A5A1F10)

Warning

The Thermal Fuse opens at a temperature of about 98° C. Let the instrument cool to a safe temperature before replacing the Thermal Fuse.

- ❑ 1. Disassemble the Power Supply halves. (See the above procedure.)
- ❑ 2. Use pliers to remove the Thermal Fuse (A5A1F10). See Figure 4-12.
- ❑ 3. Install the replacement fuse in the socket.
- ❑ 4. Reassemble the Power Supply halves.
- ❑ 5. Re-install the Power Supply.

Caution

To avoid instrument damage, determine why the instrument overheated before re-applying power for long periods. Check for sufficient clearance around the air vents or electrical problems that might be causing the temperature rise.

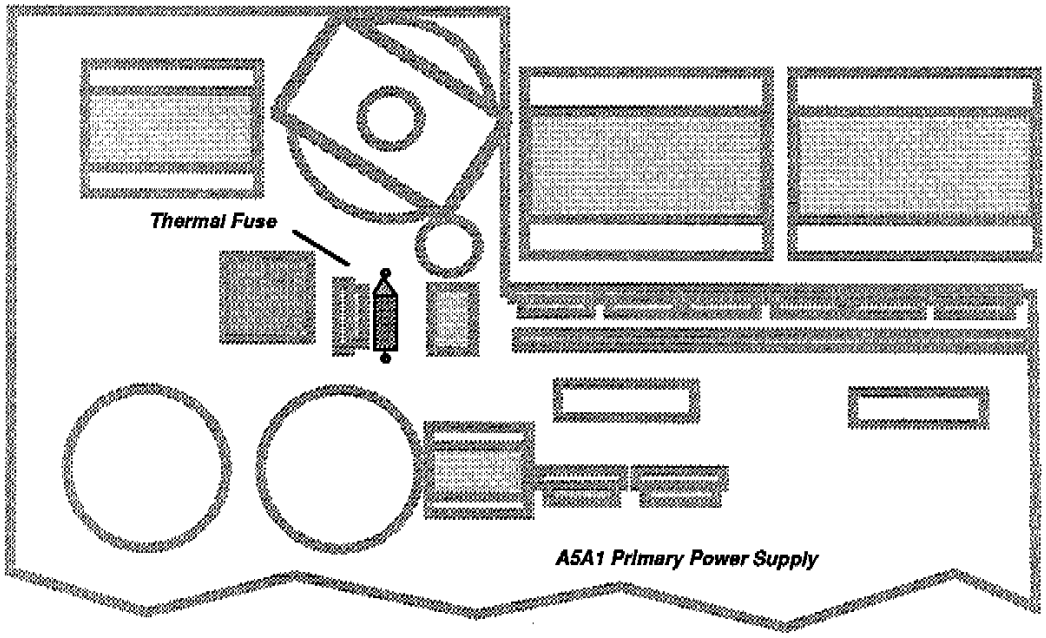


Figure 4-12. Replacing the Thermal Fuse.

Removing the Primary Board (A5A1)

- ❑ 1. Remove the Power Supply assembly (A5) from the instrument (see separate procedure).
- ❑ 2. Disassemble the Power Supply halves (see separate procedure).
- ❑ 3. Remove the seven 0.75 inch Torx T-10 screws from the Primary board.
- ❑ 4. Gently lift the Primary board at the end nearest the fan to disconnect the multi-pin connector from the Secondary board.
- ❑ 5. Continue lifting on the fan end until the board clears the heat sink on the Secondary board. Then remove the Primary board.
- ❑ 6. Remove the plastic insulating sheet from the standoffs on the bottom of the assembly.
- ❑ 7. Note the switch positions for re-installation.

Installing the Primary Board (A5A1)

- ❑ 1. Replace the plastic insulator sheet on the standoffs.
- ❑ 2. Place the wide end of the Primary board under the indents at the end of the Power Supply chassis.
- ❑ 3. Connect the fan end of the Primary board to the multi-pin connector on the Secondary board.
- ❑ 4. Replace the seven 0.75 inch Torx T-10 screws
- ❑ 5. Connect the two multi-pin connector cables.
- ❑ 6. Set the switches to the positions noted when removing the board.
- ❑ 7. Assemble the Power Supply halves (separate procedure).
- ❑ 8. Install the Power Supply in the instrument (separate procedure).

Removing the Secondary Board (A5A2)

- ❑ 1. Remove the Power Supply assembly (A5) from the instrument (see separate procedure).
- ❑ 2. Disassemble the Power Supply halves (see separate procedure).
- ❑ 3. Remove the Primary board (see separate procedure).
- ❑ 4. Disconnect the Fan connector. Note the wire positions. The red wire, positive, is farthest away from the fan.
- ❑ 5. Remove the four Torx T-10 screws as shown in the illustration.

Installing the Secondary Board (A5A2)

- ❑ 1. Replace the Secondary board and the four Torx screws in the positions shown in the illustration.
- ❑ 2. Connect the Fan connector.
- ❑ 3. Replace the Primary board (separate procedure).
- ❑ 4. Assemble the Power Supply halves (separate procedure).
- ❑ 5. Install the Power Supply in the instrument (separate procedure).

Removing the Communications Interface (A5A6)

- ❑ 1. Remove the Power Supply assembly (A5) from the instrument (see separate procedure).
- ❑ 2. Disassemble the Power Supply halves (see separate procedure).
- ❑ 3. Disconnect the ribbon cable connector from the Rear Panel BNC Interface (A5A7).
- ❑ 4. Remove the outside nuts from the four connectors attached to the frame.
- ❑ 5. Remove the two Torx T-10 screws from the board.

Installing the Communications Interface (A5A6)

- ❑ 1. Reverse the removal procedure.

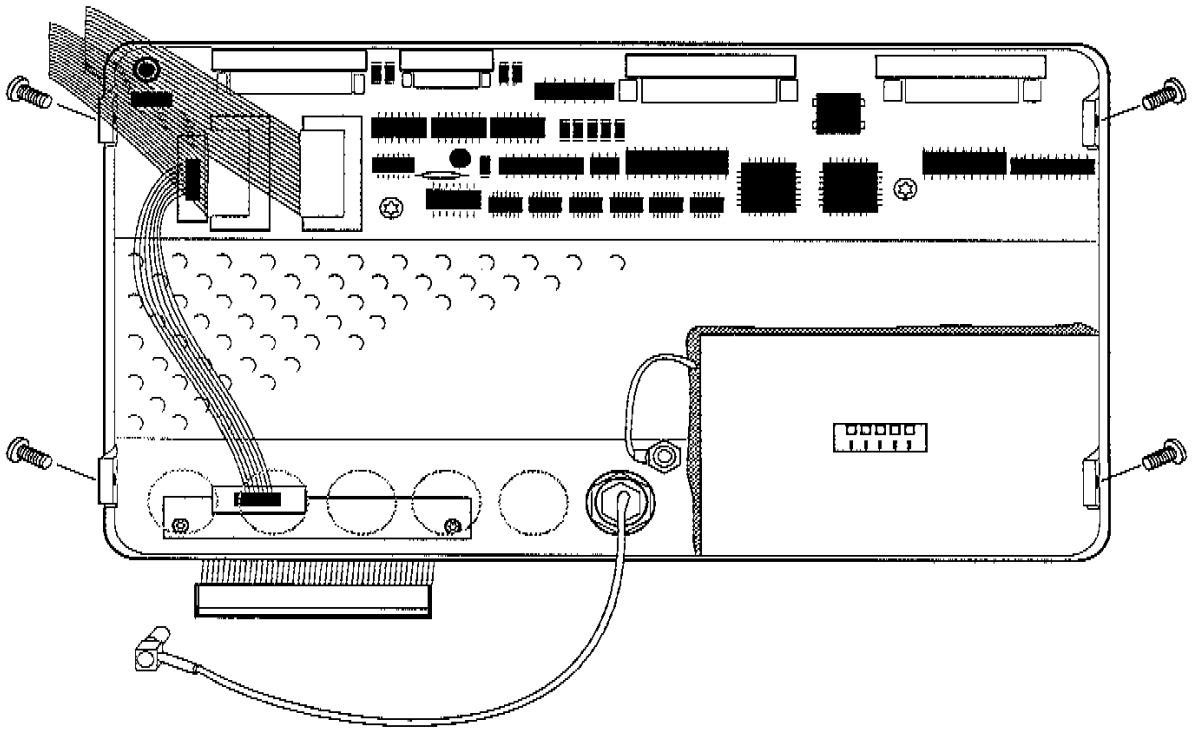


Figure 4-13. Communications Interface side of the Power Supply.

Removing the Rear Panel BNC Interface (A5A7)

❑ 1. Disconnect the ribbon cable connector.

❑ 2. Remove the nuts from the BNC connectors.

❑ 3. Remove the BNC Interface board.

Installing the Rear Panel BNC Interface (A5A7)

❑ 1. Reverse the removal procedure.

Removing the Fan (A5B100)

❑ 1. Disconnect the multi-pin connector to the Secondary board. Note the wire positions.

❑ 2. Remove the four nuts from the fan grill.

❑ 3. Remove the fan.

Installing the Fan (A5B100)

- ❑ 1. Connect the multi-pin connector to the Secondary board.
- ❑ 2. Install the fan and the grill. Make sure that the fan has the label pointing to the inside, and that the grill extends out from the frame (does not rub against the fan).

Removing the EMI Filter (A5FL500)

- ❑ 1. Remove the Power Supply Assembly (A5) from the instrument and separate the halves (see previous procedures).
- ❑ 2. Remove the nut from the green-yellow ground wire.
- ❑ 3. Remove the two Torx T-10 screws at the sides of the power input connector.
- ❑ 4. Remove the EMI filter.

Installing the EMI Filter (A5FL500)

- ❑ 1. Reverse the removal procedure.

Replacing the Color Shutter and CRT Bezel Assembly

Removing the Color Shutter and CRT Bezel

❑ 1. Remove the two Torx T-10 screws from the bottom of the crt bezel.

❑ 2. Lift the bezel away from the crt and disconnect the multi-pin connector. Note the wire positions for re-installation.

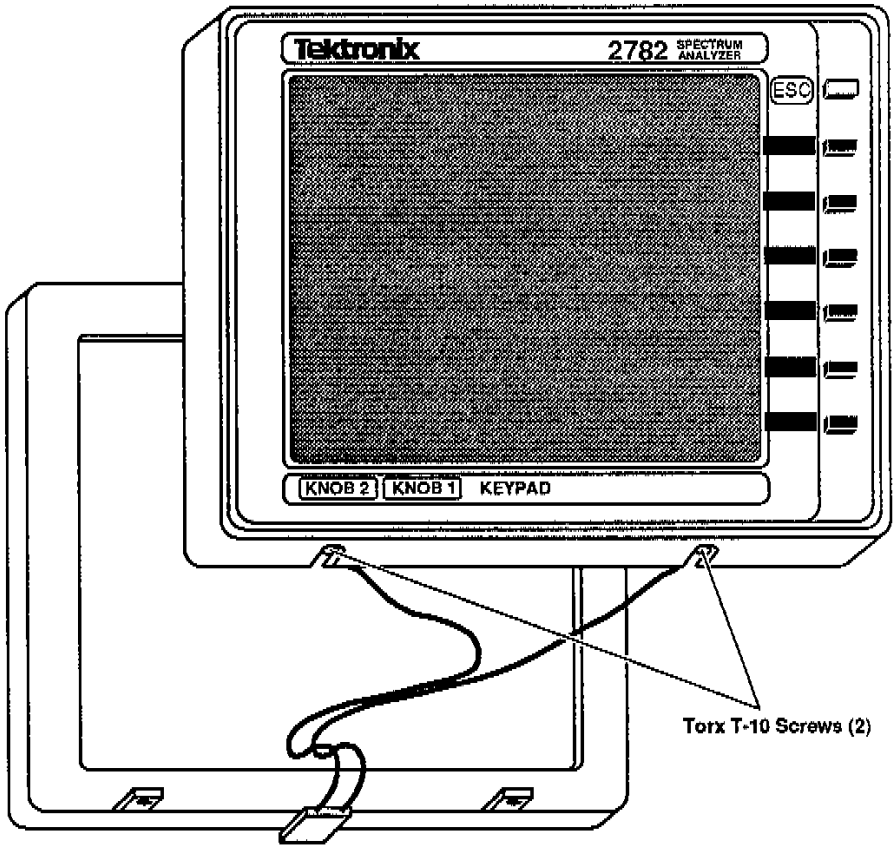


Figure 4-14. Removing the Color Shutter and CRT Bezel.

Installing the Color Shutter and CRT Bezel

❑ 1. Connect the multi-pin connector and position the wires below the glass plate of the color shutter.

❑ 2. Hook the top of the bezel over the indents in the frame and align the pushbuttons into position.

❑ 3. Place the bezel into position, while checking for proper clearance for the wires and pushbuttons.

❑ 4. Install the two Torx screws.

Replacing the CRT

Warning

The crt anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short the anode lead to the main chassis by placing the lead againts the chassis for at least five minutes to fully discharge the andoe.

Use extreme care when handling the crt. If the crt breaks, an implosion may result causing glass fragments to scatter at high velocity. Wear protective clothing and safety glasses when handling the crt. Do not allow the crt to strike against anything that might cause it to crack or implode. When storing a crt, place it in a protective carton if available, or set the crt face down on a soft mat in a protected location that has a smooth surface.

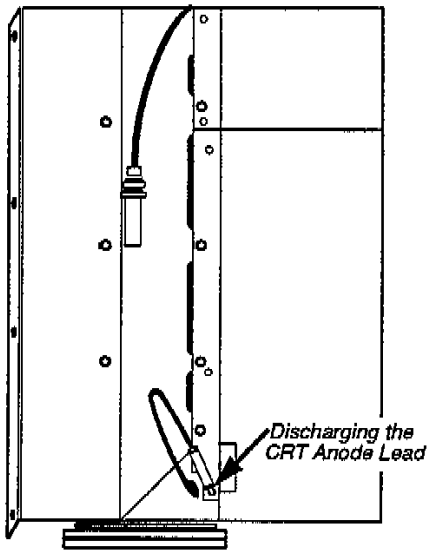


Figure 4-15. Discharging the CRT anode lead to the chassis.

Removing the CRT and Trace Rotation Coil

Refer to Figures 4-15, 4-16, and 4-17 while performing this procedure.

Caution

The high voltage charge on the anode lead can damage other circuits in this instrument. Be sure to fully discharge the anode lead only to the main chassis, as described below.

❑ 1. Remove the Processor System card cage cover to gain access to the crt anode connector, and then disconnect the crt anode connector. Replace the Processor System cover and discharge the anode lead to the chassis, holding the lead against the main chassis for at least five minutes until the crt is fully

discharged. Be sure to avoid contact with the metal end of the anode connector. Find a spot on the chassis to support the lead, and leave it there until the crt is fully discharged.

❑ 2. Remove the Power Supply assembly (A5) to gain access to the crt socket. (See separate procedure.)

❑ 3. Remove the crt socket. Be careful to not bend the crt pins. This could result in an implosion or lose vacuum in the crt.

❑ 4. If replacing the Trace Rotation Coil, disconnect its multi-pin connector from the side of the Display Amplifier assembly. Note the orientation of the wires for use when re-installing the crt.

❑ 5. Remove the horizontal and vertical deflection connectors from the crt neck. Note the wire colors and locations for use when re-installing the crt. Be careful to not bend the crt neck pins.

❑ 6. Remove the Color Shutter and CRT Bezel assembly (see separate procedure).

❑ 7. Remove crt as follows:

- Remove the eight screws from the crt frame.
- Remove the crt frame, polycarbonate window, and mylar shim from the crt. Then remove the crt from the shield. The crt retainers will come out of the shield with the crt. Place the crt retainers aside for the time being. (Note that the upper left and lower right retainers are different from the upper right and lower left retainers. Two are white and two are grey, however in early instruments, they might be the same color, be sure to return to proper place for correct alignment)

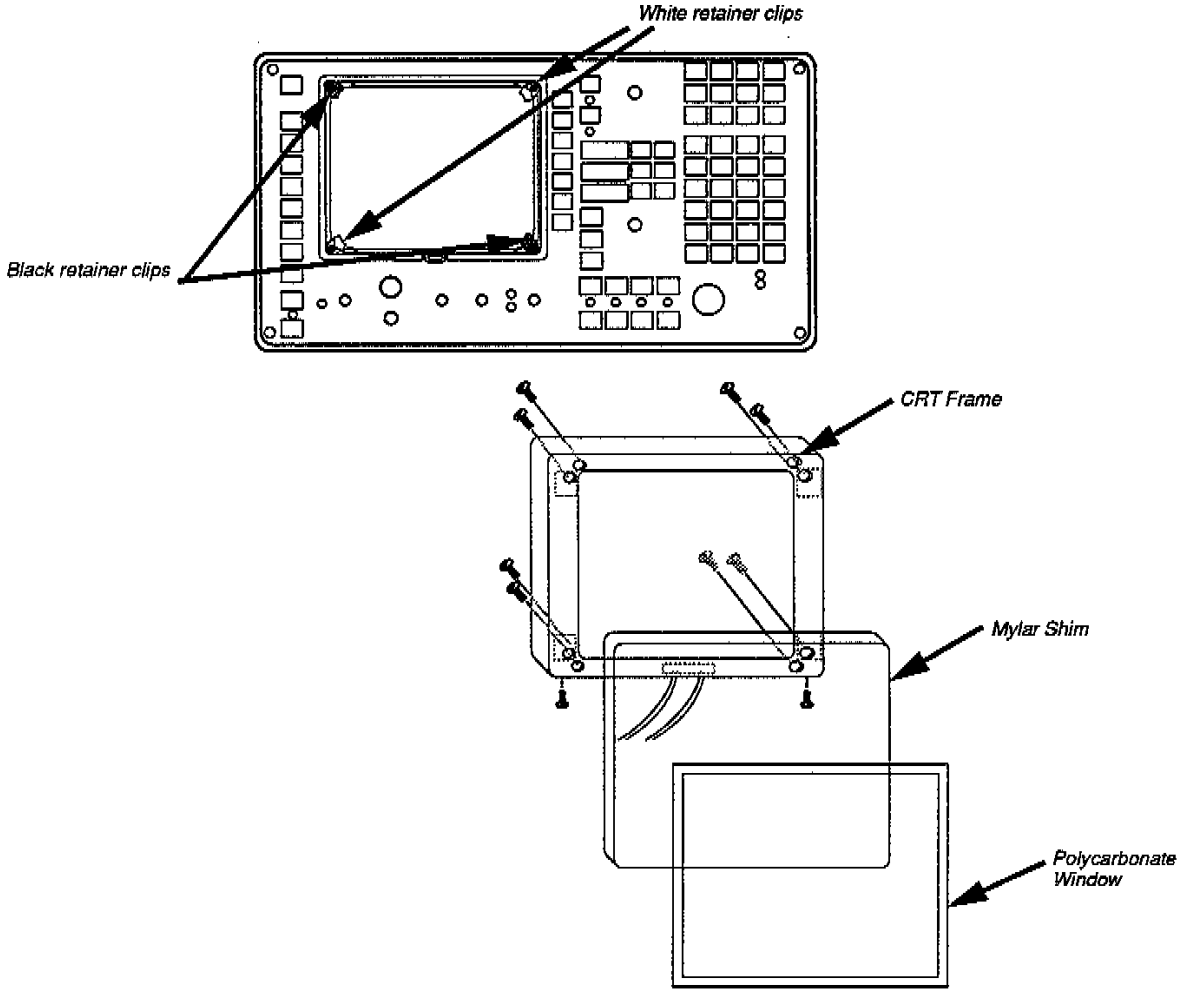


Figure 4-16. Replacing the CRT Front Panel screws.

❑ 8. If replacing the Trace Rotation coil, remove it from the crt shield.

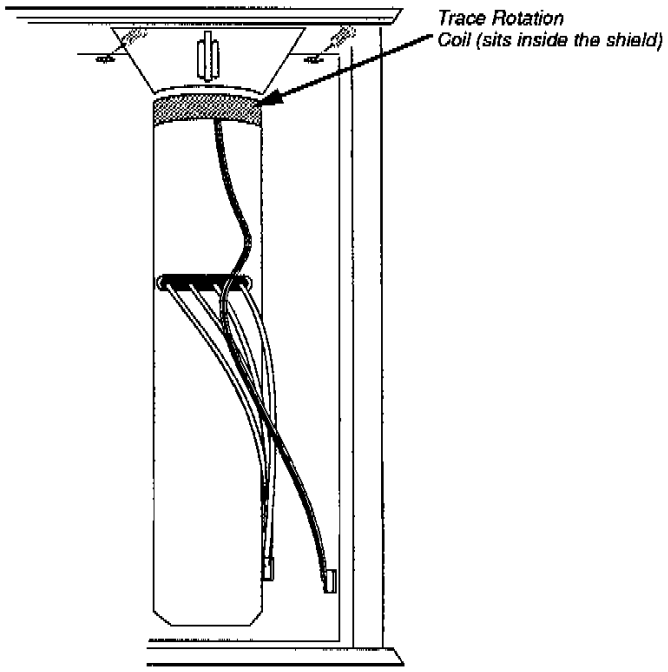


Figure 4-17. Replacing the Trace Rotation coil.

Installing the CRT and Trace Rotation Coil

❑ 1. Reverse the removal procedure, except when replacing the crt frame and retainers, make sure the retainers are in the proper places, and use the following procedure:

- Center the polycarbonate window in the crt frame, and tighten the four inner Torx screws to 10 in-lbs each.
- Adjust the retainers screws equally, going around the frame, to bring the retainers into place to keep the crt properly aligned and mechanically stable. Tighten the screws to 10 in-lbs. Do not over-tighten.

Note

Be sure that all optical surfaces are clean and lint-free before re-installing the crt and color shutter.

Observe the same precautions as when removing the crt.

❑ 2. Readjust the Display Amplifiers and the High Voltage adjustments.

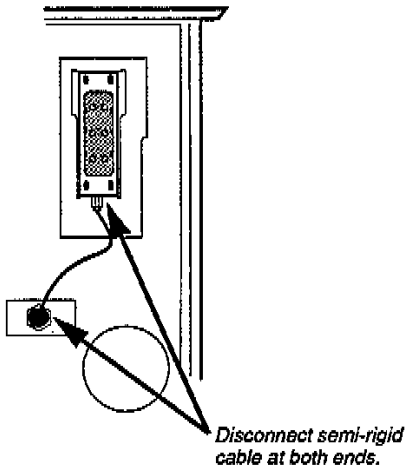
Replacing the Front Panel Assemblies

Remove the front panel with the crt attached. Start with the bottom of the instrument (RF deck) exposed.

❑ 1. Remove the RF Attenuator (A10) and the cable attaching it to the 1st Converter (A12 MTX). (See separate procedure for replacing the Attenuator.)

Caution

Removing the RF Attenuator is recommended to avoid possible damage to the attenuator and cable while replacing the front panel.



(View from underneath instrument-front, right side)

Figure 4-18. Removing the RF Attenuator cable

❑ 2. Disconnect the 5/16" SMA connectors at the rear side (inside the instrument) of the front panel REF SIGNAL OUT, LO OUTPUT, and EXTERNAL MIXER connectors.

❑ 3. Remove the two Torx T-10 screws that attach through thet chassis bottom to the crt frame.

❑ 4. Turn the instrument as necessary to work on the top side of the instrument (card cage side).

❑ 5. Remove the Processor System card cage cover to allowing unclipping the anode lead connector, then loosely replace the cover.

Warning

The crt anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short the anode lead to the main chassis after disconnecting the lead. Place the lead against the chassis for at least five minutes to fully discharge the crt.

Caution

The high voltage charge on the anode lead can damage other circuits in this instrument. Be sure to fully discharge the anode lead only to the main chassis.

❑ 6. Disconnect the crt anode lead and immediately discharge it to the main chassis for at least one minute.

❑ 7. Remove the High Voltage card cage cover and disconnect the multi-pin connectors that go to the crt socket from the High Voltage assembly. (This is easier and safer than removing the crt socket from the crt.)

❑ 8. Remove the Main card cage cover, then carefully pull the Display Amplifier assembly (A22) partially out of the cage, and disconnect the multi-pin connector on the rear side of the board. Feed the cables out of the side hole in the card cage. This completes disconnecting the crt leads.

❑ 9. Disconnect the ribbon connector from the right front of the Mother Board (A1). The other end of this cable is soldered to the far right side of the Right Front Panel assembly (A2A2).

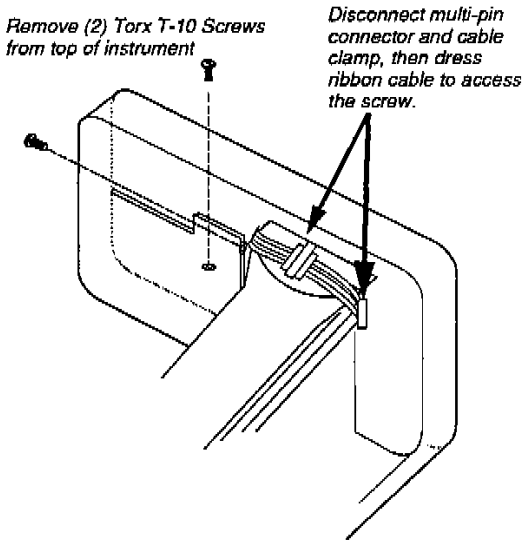


Figure 4-19. Removing the screws from the crt shield and chassis.

❑ 10. Undo the ribbon cable clamp on the top of the front end of the crt shield, then disconnect the end of the ribbon cable going to the Left Front Panel assembly (A2A1). This is on the left side while facing the front of the instrument.

❑ 11. Move this ribbon cable to the right to provide access to the two Torx T-10 screws going through the card cage side to the right side of the crt frame.

❑ 12. Remove the two screws, using a long shaft or right angle driver.

❑ 13. Remove the four Posidrive screws from the main chassis side rail where they attach to the front panel frame, two from each side.

❑ 14. Remove the entire Front Panel assembly (A2).

Removing the Left Front Panel Assembly (A2A1)

Place the assembly face down on a flat surface to protect buttons, etc. from falling out while board is not in place.

❑ 1. Remove the entire front panel assembly as discussed above.

❑ 2. Make sure the ribbon cable multi-pin connector is disconnected from the assembly. (It should already be disconnected after the previus procedure.)

❑ 3. Remove the five Torx T-10 screws from the assembly.

❑ 4. Remove the board (A2A1) from the assembly. Do not disturb the front panel frame while the board is removed

Installing the Left Front Panel Assembly (A2A1)

❑ 1. Reverse the removal procedure.

Removing the Right Front Panel Assembly (A2A2)

❑ 1. Remove the entire Front Panel assembly as previously described.

❑ 2. Remove the knobs from the KNOB 1 and KNOB 2 controls. KNOB 1 has one 1/16 inch Allen set screw, and KNOB 2 has two set screws.

❑ 3. Remove the Attenuator (A10). (See separate procedure.)

❑ 4. Disconnect the ribbon cable going over the crt shield from the clamp on the crt shield and from the multi-pin connector on the Left Front Panel (A2A1). The ribbon cable is soldered to this assembly, and is replaced as part of the assembly.

❑ 5. Disconnect the multi-pin connector that connects the FREQUENCY/MARKERS control to the board.

❑ 6. Disconnect the multi-pin connectors to the ACCESSORY IN and PROBE POWER connectors.

❑ 7. Place the assembly face down on a flat surface for the rest of this procedure. This keeps the buttons in place until the replacement assembly is installed to provide support.

❑ 8. Remove fourteen Torx T-10 screws holding the board to the front panel frame.

❑ 9. Remove the board. Also, remove the two ground springs around the shafts of the KNOB 1 and KNOB 2 controls, or from the frame if they cling there. Keep the springs and knobs to use when installing the replacement board.

Installing the Right Front Panel Assembly (A2A2)

❑ 1. Reverse the removal procedure.

Installing the Front Panel Assembly

❑ 1. Reverse the removal procedure.

❑ 2. Check flatness after reinstalling the Front Panel Assembly. (Flatness checks should be performed any time SMA connectors are changed in the front end signal path.)

Replacing the NVRAM Batteries

The batteries that power the nonvolatile RAM (NVRAM) must be replaced once a year under normal use. The procedure replaces one battery at a time, so that the other battery can supply the NVRAM during the replacement process. If both batteries are disconnected, stored data will be lost.

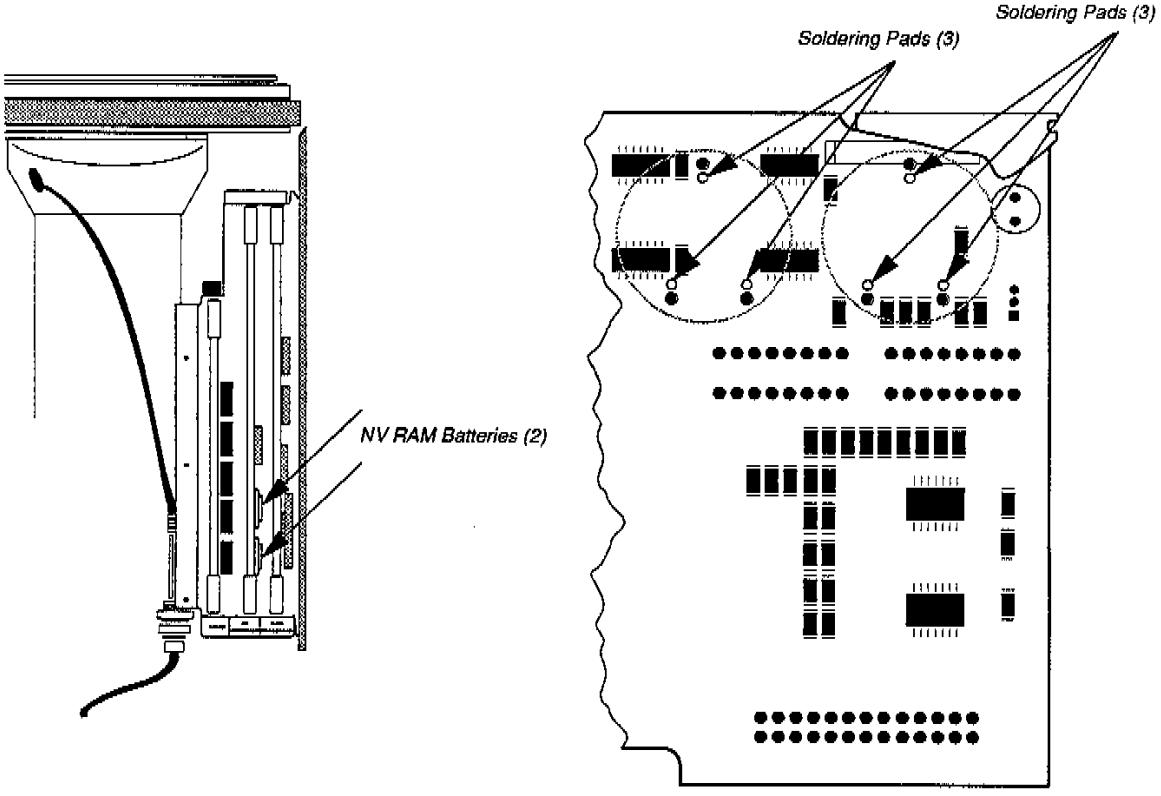


Figure 4-20. NVRAM Battery locations.

Replacement Procedure

❑ 1. Remove the I/O Interface (A42) from the instrument.

❑ 2. Determine which battery to replace first by measuring the levels of the two batteries with a volt meter. Replace the batteries according to the following criteria:

- If both batteries measure over 2 V, replace the higher voltage battery first.
- If one battery is under 2 V, replace the lower voltage battery first.
- If both batteries are under 2 V, data is probably already lost, and you can replace either battery first.

❑ 3. Unsolder the first battery to be replaced, being careful to not overheat the circuit board pads. Use desoldering tools to aid the process. Carefully remove the battery. See the disposal instructions.

❑ 4. Install the first replacement battery by soldering into the empty battery pads. Be sure to not overheat the pads.

❑ 5. Repeat the process to replace the remaining battery.

❑ 5. Re-install the I/O Interface assembly.

Battery Disposal and First Aid

Warning

Improper handling may cause fire, explosion, or severe burns. *To avoid personal injury, observe proper procedures for the handling of lithium batteries. Do not recharge, crush, disassemble, heat the battery above 302°F (126°C), incinerate, or expose the contents to water.*

Lithium Battery Disposal

Dispose of the battery according to local, state, and federal agencies.

Note

Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.

Larger quantities must be sent by surface transport to a hazardous waste disposal facility. the batteries should be individually packaged to prevent shorting. Then, pack them into a sturdy container that is clearly labeled:

Lithium Batteries – DO NOT OPEN

Lithium Battery Emergency and First Aid Information

- **Manufacturer:** Catalyst Research or Sanyo
- **Battery Type:** Lithium

Table 4-25 lists the emergency procedures to follow should you come in contact with battery solvent.

Table 4-25. Lithium Battery Emergency Procedures

Contact	Do This:
Skin	Wash promptly with plenty of water.
Eyes	Flush immediately with plenty of water and use an emergency eye wash, if available. Report to a medical professional for treatment.
Inhalation	Leave the area and get fresh air. Report to a medical professional for treatment.
Ingestion	Non-toxic according to laboratory testing. However, report to a medical professional for advice.

In case of venting, clear the immediate area. Venting will usually last only a few seconds.

Updating Firmware

Firmware is updated in this instrument by replacing ROMs. The ROMs are located on four separate boards, Figure 4-26 shows the firmware ROM locations. There are three sets of firmware in the instrument, and these might be updated at different times. An appendix at the rear of this manual provides a table of firmware compatibility. The boards and their respective firmware are:

Table 4-26. Firmware Locations

Board	Firmware	IC
A24 Digital Storage	Digital Storage	U11
A41 Main Processor	Main Processor FW	U63
A42 I/O Interface	I/O Interface portion of the Main Processor FW	U37, U38, U39, and U40
A43 Memory	Main Processor FW	U10, U11, U12, U13, U14

All of the ICs listed above are ordered as sets and are separate from the boards they reside on. The Main Processor firmware on the Main Processor (A41) and Memory (A43) boards must be replaced as a set. The I/O Interface portion of the Main Processor firmware (if any) may be replaced independently of the rest of the Main Processor firmware. The Digital Storage firmware is replaced independently. Check the Firmware Version chart at the rear of this manual for firmware compatibility.

Note

In early instrument, the I/O Interface board (A42) does not have any ROMs installed. The sockets are present for use with future firmware versions. Check the Firmware Version information at the rear of this manual for current information.

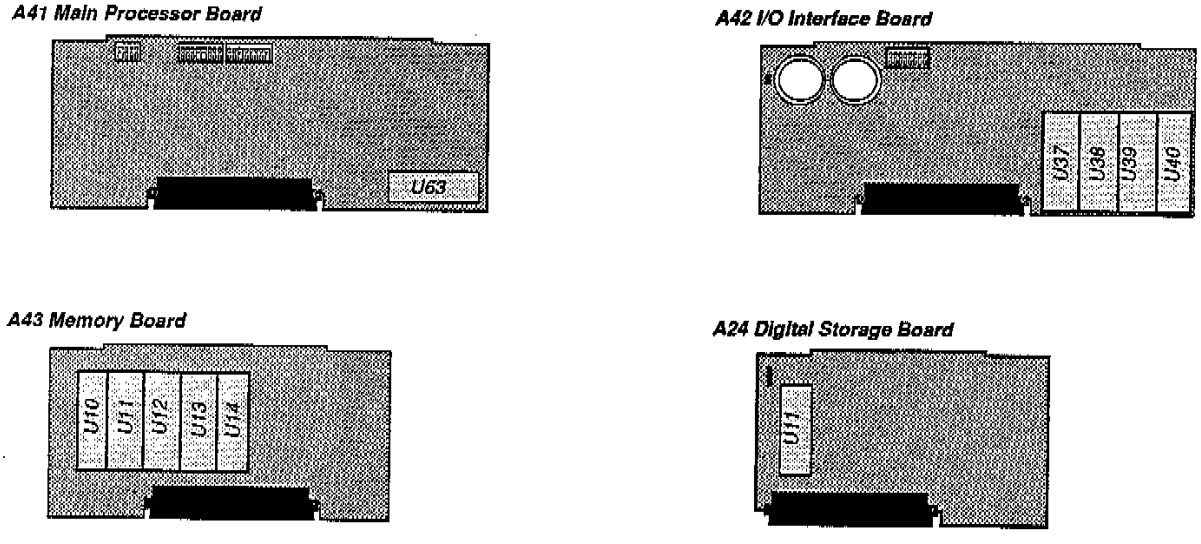


Figure 4-21. Firmware ROM locations.

Switches and Jumpers

The following information gives the switch and jumper positions Factory-set default settings are in ALL CAPS.

IO Interface

A42 I/O Interface Board

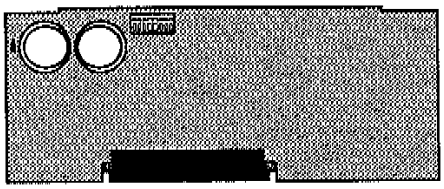


Figure 4-22. I/O Interface switch positions.

Table 4-27. I/O Interface Switch Functions and Positions.

Switch Number and Function	Position	
	Open	Closed
1. Sweep Board version	Open	CLOSED
2. Ref Osc version	Open	CLOSED
3. Trace Mode	DISABLED	enabled
5. Frequency Control Loop	Open Loop	CLOSED LOOP
8. MTX version	Open	CLOSED

Table 4-28. I/O Interface Jumpers.

Jumpers	Positions	
J10	Pins 1 and 2 Normal (Data Saved)	Pins 2 and 3 Secure (Data Erased)
J11	Information Not Available	
J12	Information Not Available	
J13	Information Not Available	

Processor

A41 Main Processor Board

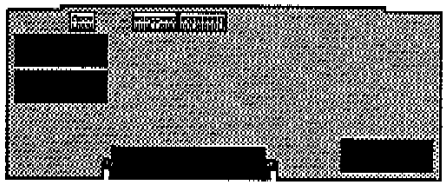


Figure 4-23. Main Processor Switch Locations.

Table 4-29. Main Processor Switch Functions (Left Switch).

Left Switch

Switch Number and Function	Position	
	Open	Closed
1. Extended Diagnostics	DO NOT RUN	Run
2. Power Up ROM Checksum test	RUN	Do Not Run
3. Service Mode	DISABLED	Enabled
4. Error Reporting	ENABLED	Disabled
7. FP Version	OPEN	Closed
8. FP Standby Switch	ENABLED	Disabled

Table 4-30. Main Processor Switch Functions (Right Switch).

Right Switch

Switch Number and Function	Position	
	Open	Closed
1. NMI Enable	ENABLED	Disabled
5. Force Recall of Default Settings	ENABLED	Disabled
6. Periodic Calibration	ENABLED	Disabled
7. Overdrive limit for 10 kHz BW	Disabled	ENABLED
8. Power Supply version	OPEN	Closed

Power Supply

Table 4-31. Primary Switches.

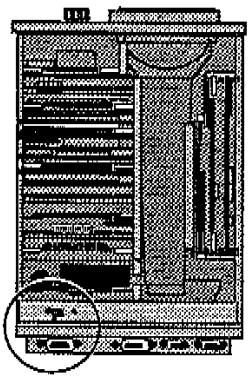
A5A1 Primary Switches		
S10 - 1 Main Chopper Control	On	OFF
S10 - 2 Pulse Width Modulator Sense Voltage	On	OFF

Table 4-32. Secondary Switches.

A5A2 Secondary Switch		
S10 - 1 /ACGONE Defeat	On (Defeated)	OFF (ACTIVE)
S10 - 2 Main Chopper Control	Main Choppers On	OFF
S10 - 3 & 4 Fan Control	See next table (Works only if disconnected from processor)	

Table 4-33. Fan Speed Switch Positions.

Function Fan Speed	S10-3 Fan 2	S10-4 Fan 1
OFF (Normal)	OFF	OFF
Low	On	Off
Medium	Off	On
High	On	On



A5 Power Supply

Figure 4-24. Switches Located on Power Supply Secondary.

Theory of Operation

This section describes the spectrum analyzer circuitry. The section begins with a functional description of the major circuit blocks and follows with more detailed descriptions of each block.

While reading these descriptions, refer to the corresponding block diagram. The Functional Block diagram shows how the major sections in the instrument relate and the paths of the major signals. Block diagrams showing more detail of these main sections accompany the text that follows the Functional Block diagram.

FUNCTIONAL DESCRIPTION

The spectrum analyzer accepts an electrical signal as its input and displays the signal's frequency and amplitude components on a cathode ray tube (crt). Signals to 33 GHz can be applied directly to the RF INPUT connector. Higher frequency signals can be down converted using external waveguide mixers.

The input signal appears on the crt as a graph where the horizontal axis represents frequency and the vertical axis is amplitude. Displays can be stored in memory for future use and can be plotted on GPIB-compatible plotters.

The instrument can be operated either manually with front-panel controls, or remotely via the GPIB.

The Spectrum Analyzer operates as a swept, variable bandwidth, receiver. The normal waveform is updated horizontally as a range of frequencies is spanned. When a signal is detected, the waveform moves vertically as a function of input power at the detected frequency.

The analyzer measures frequency by comparing the local oscillator frequency against a reference. Amplitude is measured by calibrating the REF LEVEL and RF attenuator. Internal microcomputers perform control, storage, signal processing, and communications functions.

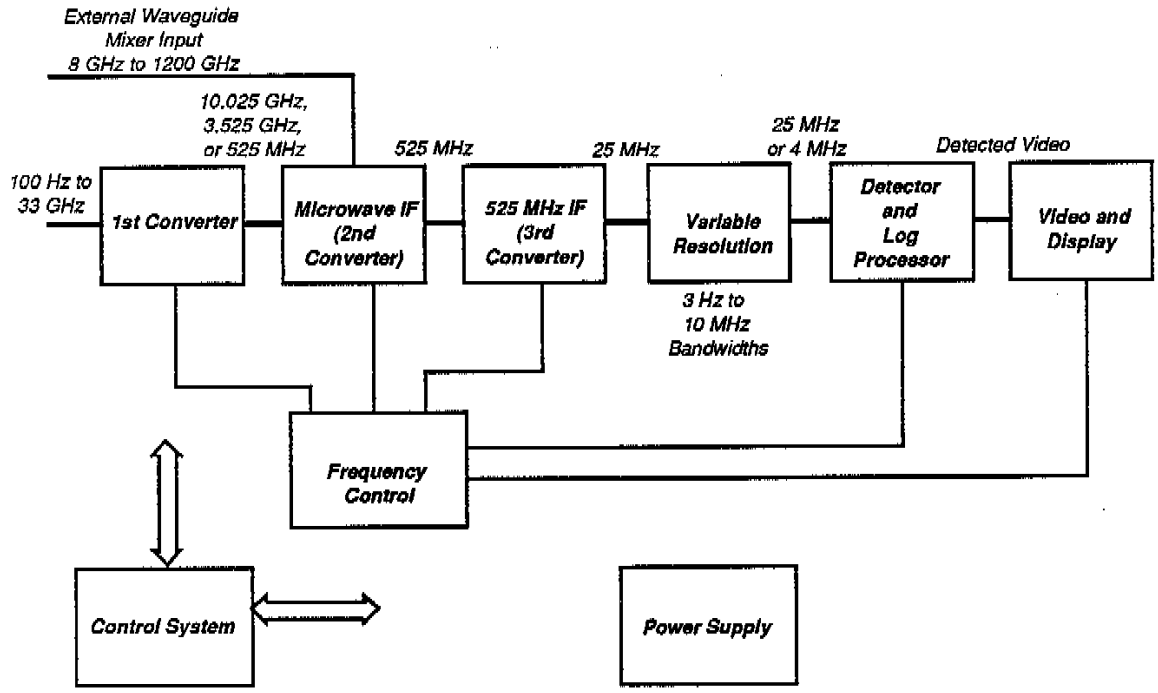


Figure 5-1. 2782 Spectrum Analyzer Block Diagram.

1st, 2nd, and 3rd Converters

The spectrum analyzer acts as a superheterodyne receiver. Converter stages mix the RF input frequency with appropriate local oscillators (LOs) to arrive at intermediate frequencies (IFs) where bandwidth filtering occurs. At each stage, one range of frequencies is converted in a mixer, switched by an appropriate local oscillator frequency, and passed through band-pass filters to the next stage, eventually reaching the detector. Tuning the 1st LO changes the received frequency.

The first converter, called the MTX for magnetically tuned converter, acts as the front end of the instrument. It converts the input signal frequency to an intermediate frequency (IF) of either 3.525 GHz or 10.025 GHz, depending on which band is in use. The internal mixer converts signals over the input range of 100 Hz to 33 GHz. External mixers may be used for signals into the millimeter wavelengths. When the internal mixer is used, either a preselector or a low-pass filter is inserted in the signal path to reduce unwanted signals or images and spurious responses.

The second converter, called the Microwave IF, amplifies the first IF and converts it to 525 MHz. One of two second converters is automatically selected for each band so the input frequency range does not overlap the first IF frequency. Each second converter has its own local oscillator, mixer, and filters. Both convert the signal down to 525 MHz, which is then sent to the third converter.

When an external mixer is used in the 18 GHz to 26.5 GHz band, it already provides the 525 MHz IF. When this is the case, the second converter is by-passed and the signal passes directly through to the third converter. In other external mixer bands, the 525 MHz path is used to identify the actual signal versus spurious signals. In the Identify mode, the 1st Local Oscillator frequency and the display color is changed on alternate sweeps. The spurious signals change with the oscillator frequency so that only the actual signal appears the same on both sweeps.

The third converter, called the 525 MHz IF, amplifies the 525 MHz IF signal and converts it to an intermediate frequency of 25 MHz which is more suitable for band-pass filtering. The third converter passes the signal to the Variable Resolution (VR) stage for band-pass filtering.

Variable Resolution and Log Processor

This section adjusts the bandwidth, calibrates amplitude, performs logarithmic conversion, and detects the signal.

The 25 MHz IF signal is used where the widest bandwidths of 10 MHz and 3 MHz are desired. For narrower bandwidths, the 25 MHz signal is converted to 4 MHz within the VR module. The 4 MHz signal is filtered by a set of digitally-controlled synchronously-tuned resonators giving variable bandwidths from 1 MHz to 3 Hz. Resolution bandwidth is selected using the RES BW menu. In the auto mode the microcomputer selects the best combination of bandwidth and sweep time for the selected span unless overridden by the operator.

Weak signals can be amplified by a set of switchable amplifiers that switch the dynamic display range (vertical window) up or down. The REF LEVEL control selects the gain and input RF attenuation to frame this window between the reference level at the top of the display screen and the bottom of the display. A flatness correction circuit helps provide flat frequency response across the input frequency range. The signal is amplified by a logarithmic amplifier to scale the vertical signal in decibels.

The detector produces a voltage that corresponds to the input signal strength in decibels. The detector output is then sent to the vertical channel of the display section to be digitized.

Display

The display section is a general purpose vector and graphics processor. It digitizes the signal, and then processes it for display along with the graticules, menus and other readouts. The menus and readouts are based on data from the Digital Control section.

The video processor scales the detector output for vertical deflection in decibels or performs a log/linear conversion, depending on the vertical display mode. The video processor also provides additional video filtering from 0.03 Hz to 300 kHz in 1-3-10 steps.

Digital storage circuits provide two functions; they provide a flicker-free display at slow sweep rates, and they temporarily store the display for later viewing. Battery powered non-volatile memory in the Digital Control circuits provides long term storage for up to twenty waveform displays. The digital storage circuits also provide the Max Hold, Average, Math, Markers, and Bandwidth Marker functions.

A color display helps distinguish between signals, markers, different readouts, on and off menu selection, etc. In this instrument, color is provided by a color shutter that attaches to the crt. Switching circuitry selects what color the crt data will be when it is viewed by the user. Menu selections allow choosing the color of each waveform.

Frequency Control

The spectrum analyzer sweeps through a frequency range that is set by the frequency control section. The FREQUENCY /MARKERS control sets the 1st LO frequency.

The span attenuator scales the sweep generator output to sweep a range or span of frequencies. The span attenuator output drives both the 1st LO and the video processor that controls horizontal deflection. This sweeps the digitizer in proportion to the local oscillator so that the horizontal axis is calibrated to represent the input frequencies.

The frequency control section also tunes the preselector so that it tracks the signal frequency being detected over the 6.3 GHz to 33 GHz range.

The LO Module, Period Counter, 565 MHz Synthesizer, and Microwave Phase Lock module form the core of the frequency control circuits. The 1st LO frequency is controlled by a firmware-based control loop. Data from the Period Counter feeds back to control the oscillator frequency. Accurate signal frequency measurement is possible by counting the frequency of the third IF.

The Microwave Phase Lock system stabilizes the 1st LO frequency for use in narrow resolution bandwidths.

Digital Control

The spectrum analyzer operational modes and internal functions are selected and controlled directly from the front panel. The modes and functions that are selected are processed and activated by the instrument main microcomputer which talks and listens to all circuits over the instrument bus. The instrument can also be remotely controlled from an external controller through the IEEE-488 (GPIB) connector.

Front panel control and selector data is processed by a front panel processor that interfaces with the main microcomputer over the instrument bus. The main microcomputer receives and sends all of its information over the instrument bus to the internal circuits. The instrument communicates with other instruments through the GPIB connectors using a programmable control language that corresponds to front-panel controls.

Battery-powered non-volatile memory stores up to twenty different displays with their readouts. The stored display data can be transmitted through the IEEE-488 port to a plotter or to GPIB compatible controllers or instruments. The non-volatile memory can also store up to twenty front panel control settings. In addition, electronically-erasable ROMs (EEPROMs) hold other changeable data – such as calibration factors, flatness data, and menu information.

Power Supply

The power supply section provides regulated dc power and forced air cooling for all circuits in the instrument. The switching supply is capable of providing regulated voltages over a wide range of input line frequencies and voltages. The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all sections of the instrument in proportion to the heat generated by circuits within those sections. Internal temperature variations are minimized to provide reliable operation.

The communications interface is also included in the Power Supply assembly. For this description the Communications Interface will be discussed with the other Digital Control circuits.

Other Sections

Connections between assemblies are made through a common interface called the Mother board and by cabling. Most circuit board assemblies plug into the top side of the Mother board. Assemblies on the RF deck are connected to the bottom side of the Mother board and through cables.

Block Descriptions

1st Converter

The First Converter takes the RF input signal or the external mixer input signal and converts it to an intermediate frequency. The IF output is at either 10.025 GHz, 3.525 GHz, or 525 MHz, depending on the frequency band being analyzed. The circuitry consists of:

- RF Attenuator (A10)
- Magnetically Tuned Converter assembly (MTX - A12)
- 1st Local Oscillator (YTO - A11).

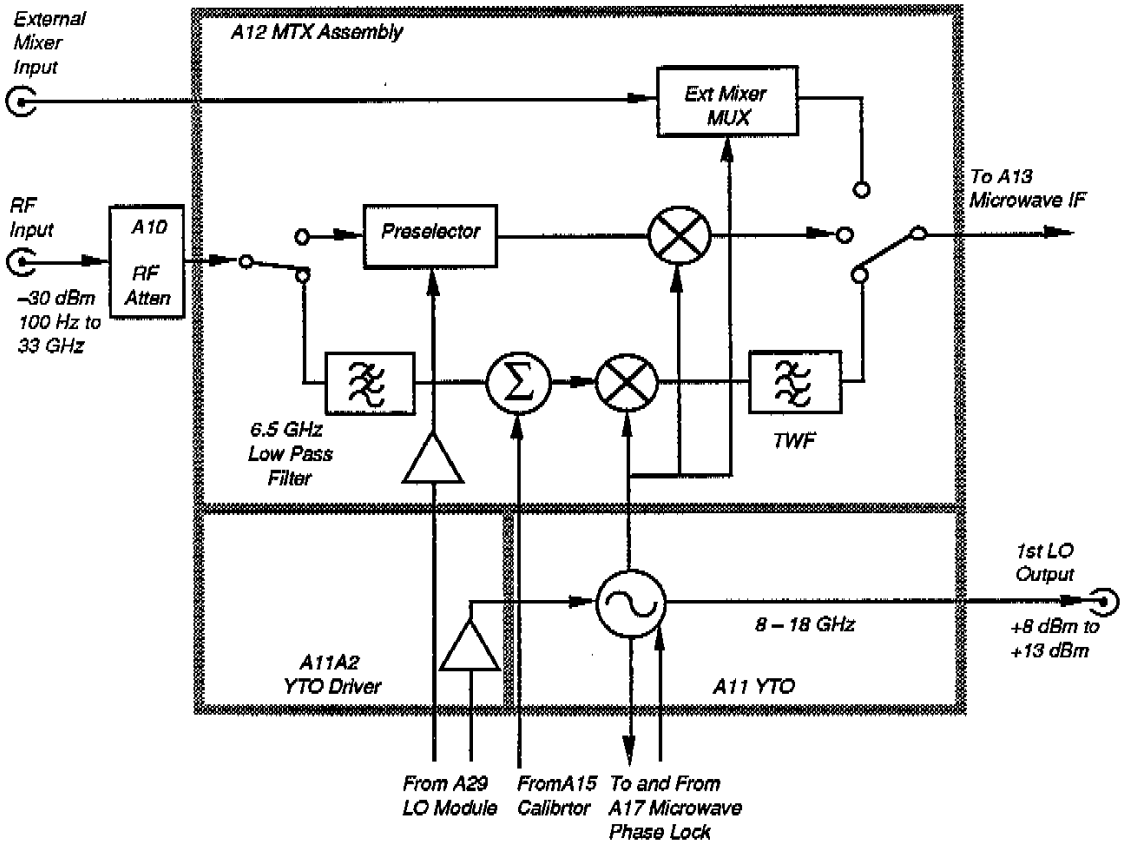


Figure 5-2. 1st Converter Block Diagram

RF Attenuator

The RF signal enters the instrument through a Planar Crown connector system. The RF Attenuator (A10) attenuates the incoming RF signal from 0 dB to 70 dB in 10 dB steps. From the RF Attenuator, the signal goes to the MTX.

MTX

The MTX assembly (A12) contains the main body of the First Converter. The incoming RF signal from the RF Attenuator feeds a switched diplexer that selects a low pass path for frequencies under 6.5 GHz, or selects the high pass path for signals from 6.5 GHz to 33 GHz. Signals from waveguide sources are converted down by external waveguide mixers. The waveguide mixer connects to the EXTERNAL MIXER INPUT, which also supplies a multiplexed local oscillator signal to drive the mixer.

The MTX assembly is replaceable as one unit. Two sub-assemblies, the Low Pass Termination (A12A4) and the Low Pass Mixer (A12A5), are replaceable individually. If any of the remaining subassemblies fail, the entire MTX assembly must be replaced in order to preserve calibration of the unit.

Low Pass Path

The low pass path converts signals under 6.5 GHz. The signal goes through a Low Pass Filter, Low Pass Termination (A12A4) , Low Pass Mixer (A12A5), Traveling Wave Filter, and output Switching circuit.

6.5 GHz Low Pass Filter
A 6.5 GHz Low Pass Filter (A12FL2) keeps higher frequency signals from entering the low pass path. This keeps down ripple on the display.

Low Pass Termination
The Low Pass Termination (A12A4) terminates the low pass filter and the low pass mixer RF input, and it combines the 100 MHz Reference Signal to the mixer input. This supplies the internal reference signal selectable from the Input menu. This sub-assembly is replaceable.

Low Pass Mixer
The Low Pass Mixer (A12A5) mixes the RF input with the 1st local oscillator signal to produce a 10.025 GHz IF. This sub-assembly is replaceable.

Traveling Wave Filter
The Traveling Wave Filter (A12FL3) acts as a 10.025 GHz bandpass filter. The desired 10.025 GHz signal passes to the IF switching circuit while the unwanted signals are terminated by the filter.

High Pass Path

The high pass path converts RF input signals from 6.5 GHz to 33 GHz. The signal is automatically preselected by a tunable bandpass filter before driving the high pass mixer. The mixer output goes to the IF output switch circuit

Preselector
The Preselector (A12FL1) is a wide range tunable bandpass filter covering 6.5 GHz to 33 GHz. Signals over 6.5 GHz go through the switched input diplexer to the Preselector. The Preselector consists of crystal spheres, tuned by changing the magnetic field around them.

The Preselector Driver (A12A7) supplies current to the Preselector coil to tune the filter. The tuning signal corresponds with the sweep so that the displayed signal and the input filter are synchronous.

High Pass Mixer
The High Pass Mixer (A12A2) mixes the preselected input signal to the intermediate frequency. The IF output from the mixer feeds the Switch module, where it is filtered and ported to the second converter.

Switch Module

The Switch assembly (A12A3) provides LO amplification, switching , filtering, and signal multiplexing.

The LO signal is applied to this assembly, where it is amplified to provide a high level drive for the mixers. PIN diode switches select whether the LO will drive the low pass, high pass, or external mixer.

The signal from the low pass path arrives at the Switch module through the Traveling Wave Filter. A PIN diode switch connects the signal to the IF output for the assembly.

The high pass path signal is also selected by PIN diode switches. The signal goes through a low pass filter for those bands that have a 3.525 GHz IF and through a bandpass filter for the 10.025 GHz IF bands.

In the external mixer path, the LO signal multiplexes onto the same line as the external mixer's IF output. This allows using two-port waveguide mixers. The LO signal is tunable from 8 GHz to 18 GHz and the IF output from the external mixer is at either 3.525 GHz or 525 MHz, depending on the band and LO harmonic (N) used. The multiplexing is accomplished using a high pass filter and a low pass filter as a diplexer to separate the IF and the LO. The LO signal passes through a high pass filter to the EXTERNAL MIXER INPUT to drive the waveguide mixer. The IF output from the external mixer is below the LO frequency, and will not pass through the high pass filter. Instead, the IF goes through a low pass filter to the assembly IF output. The low pass filter, in turn, does not pass the LO signal to the IF output.

MTX Control

The MTX Control circuit (A12A6) interfaces to the main processor and provides power supply filtering. A serial-slave interface chip decodes control signals from the instrument bus. These are converted to control signals for the PIN diode switches, LO switching, and bias for external mixers.

1st Local Oscillator

The first local oscillator provides a high level signal tunable over an 8 GHz to 18 GHz range. The LO can be phase locked to the instrument Reference Oscillator in narrow sweep spans to provide stability and low phase noise. The

circuits consist of the YIG Tuned Oscillator (YTO - A11) and the YTO Driver (A11A2). These assemblies are replaceable if necessary.

YTO

The YTO (A11) is a magnetically tuned YIG oscillator. Current through the magnet coils tunes the resonant frequency. Tuning current is supplied by the YTO Driver (A11A2) and the Microwave Phase Lock assembly (A17). The oscillator has three outputs; one driving the MTX, one to the Microwave Phase Lock, and one to the front panel 1st LO OUTPUT

YTO Driver

The YTO Driver (A11A2) converts drive voltage into coil current, switches a noise filter across the coil, clamps the coil during retrace, and provides power supply filtering.

The drive voltage from the LO Module (A25) is converted to a current to drive the main YIG coil. This is proportional to the Preselector drive when the Preselector is in use.

The noise filter reduces noise current across the coil above 1.5 kHz. Capacitors are chosen to optimize coil transient response.

During wide sweeps, more than 100 V of back swing is needed across the coil. The retrace clamp helps get the coil back to the start of the sweep as quickly as possible.

2nd Converter

The Microwave IF Assembly is the second converter for the instrument. It amplifies, filters, and converts signals coming from the MTX assembly, the first converter. A signal enters from the first converter at either 525 MHz, 3.525 GHz, or 10.025 GHz. A 525 MHz signal is passed through an isolation switch to an IF selector at the output, and a 3.525 GHz or 10.025 GHz signal is converted to the second IF of 525 MHz. Phase lock circuitry controls the local oscillators used for the conversions.

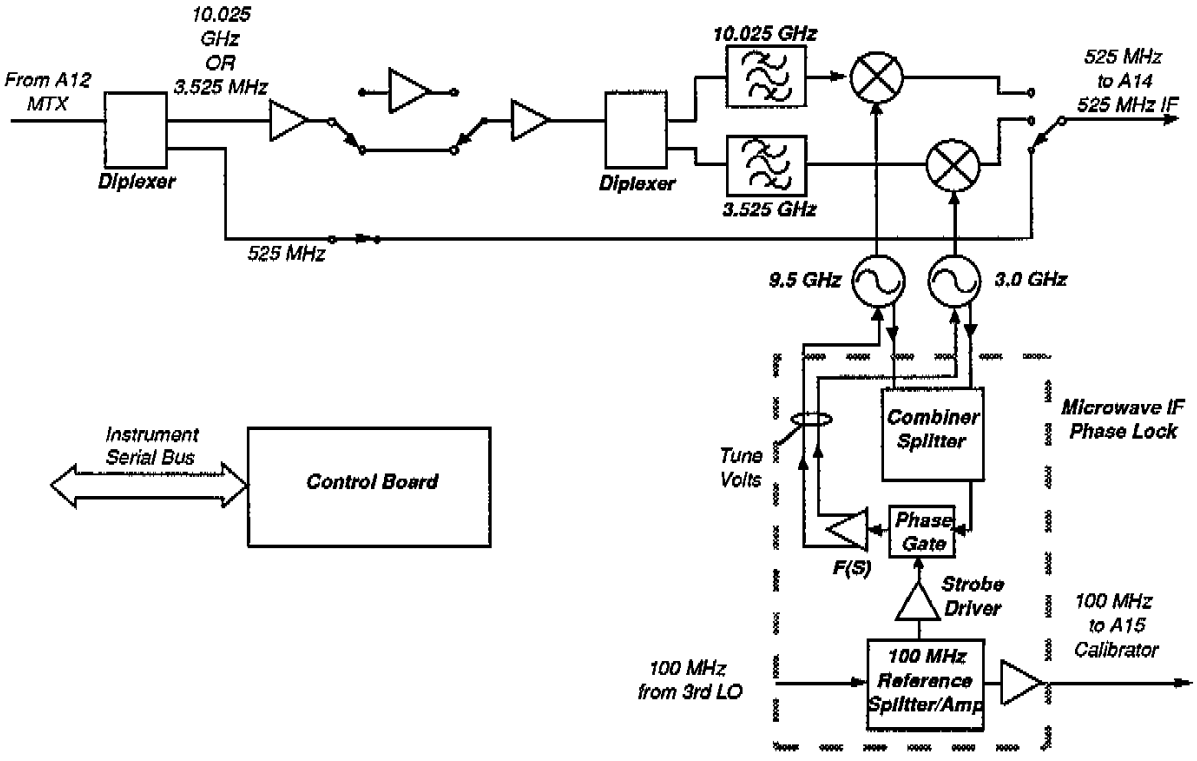


Figure 5-3. Microwave IF (A13)

Converters

Input Amplifier

The input signal first feeds a diplexer. Any frequency components under 600 MHz are split off and sent to the 525 MHz path. Components over 3 GHz are sent to the amplifier stage.

The amplifier section consists of three stages of GaAs FET amplifiers. The first stage is a balanced stage, followed by a switchable gain stage, and the output stage is again a balanced amplifier.

The first amplifier is a low noise stage. This feeds a second amplifier that can be switched in and out of the circuit via pin diodes. This gain step overcomes losses in Band 2 and above due to increased insertion loss in the MTX module (first converter). The last stage is a balanced amplifier that sends the signal to another diplexer. This diplexer splits the 3.525 GHz and 10.025 GHz signals onto separate paths.

Filters

The diplexer output signals are cabled from the amplifier to bandpass filters with center frequencies of 3.525 GHz and 10.025 GHz. The filters each have 100 MHz bandpass.

Mixers & LOs

The bandpass filter outputs feed into their respective mixers. Each mixer is driven by a separate local oscillator, one at 3 GHz for the 3.525 MHz IF and one at 9.5 GHz for the 10.025 GHz IF. These produce the desired product of 525 MHz from each mixer.

Both mixer outputs then feed the IF Selector. The IF Selector selects the appropriate mixer output for the band in operation, or the 525 MHz path from the Isolation Switch when an external mixer is being used.

Phase Lock

The Microwave IF Phase Lock Module controls the local oscillators. The module consists of the LO Power Splitter, Strobe Driver, 100 MHz Splitter, F(s) Amplifier and Phase Gate hybrid. The phase locked loop is made up of the two microwave local oscillators, a power splitter, a 100 MHz reference signal, a phase gate, and the F(S) amplifier.

The Microwave IF Phase Lock module samples the LO signal and provides correction voltages to the local oscillators, locking them to the 100 MHz reference. The LO signal for the band in use enters through a power splitter to drive a phase gate. The 100 MHz reference signal strobes the phase gate, producing a difference signal. This signal drives the F(S) amplifier where it is filtered to stabilize the loop, and then fed back to the local oscillators as a control signal.

LO Power Splitter

The power splitter is a hybrid that accepts and isolates LO power from the 3 GHz LO and 9.5 GHz LO and provides the proper level to the phase gate.

F(S) Amplifier

The F(s) amplifier provides a filter to stabilize the loop. It also contains circuitry to sense an out-of-lock condition and then sweep the tuning voltage of the microwave local oscillators to find and lock to the proper beat note, as well as a

buffer amplifier for the phase gate, and circuitry to remove offset voltages coming from the phase gate.

Reference Amplifier

The Reference Amplifier and Splitter board accepts the 100 MHz signal at about +3.5 dBm and amplifies it to about +10 dBm for the strobe amplifier. It also splits the 100 MHz to another port at about the same level as the input (+3.5 dBm) and has its power applied or removed by instructions from the main processor, through the SIC on the control board, to reduce the calibrator signal when not used.

Strobe Driver

The Strobe driver board accepts the +10 dBm signal from the splitter board and then amplifies it to drive the snap-off diode in the phase gate. There are two bias adjustments on the strobe driver board to properly bias the snap-diodes. These are only adjusted when replacing the module.

Control Board

The Control board is an interface between the mother board and the modules that make up the second converter. The board contains the SIC to take instructions from the microprocessor concerning the band of frequencies to be converted or passed by the module, concerning the IF gain, and also to switch power to the proper modules. The board also contains post-regulated plus and minus twelve volts and FET switches to steer all the supplies to the modules as directed by the SIC.

3rd Converter

The Third Converter converts the 525 MHz IF signal from the Second Converter to 25 MHz to drive the Variable Resolution circuits. The Third Converter circuits consist of the 525 MHz IF (A14), the Reference Oscillator (A29), and the X5 Multiplier (part of A28). The signal enters the 525 MHz IF module and is mixed down to 25 MHz by beating against a 500 MHz LO. The 500 MHz LO is derived from multiplying the 100 MHz Reference Oscillator output five times. the Reference Oscillator provides the frequency reference for the instrument.

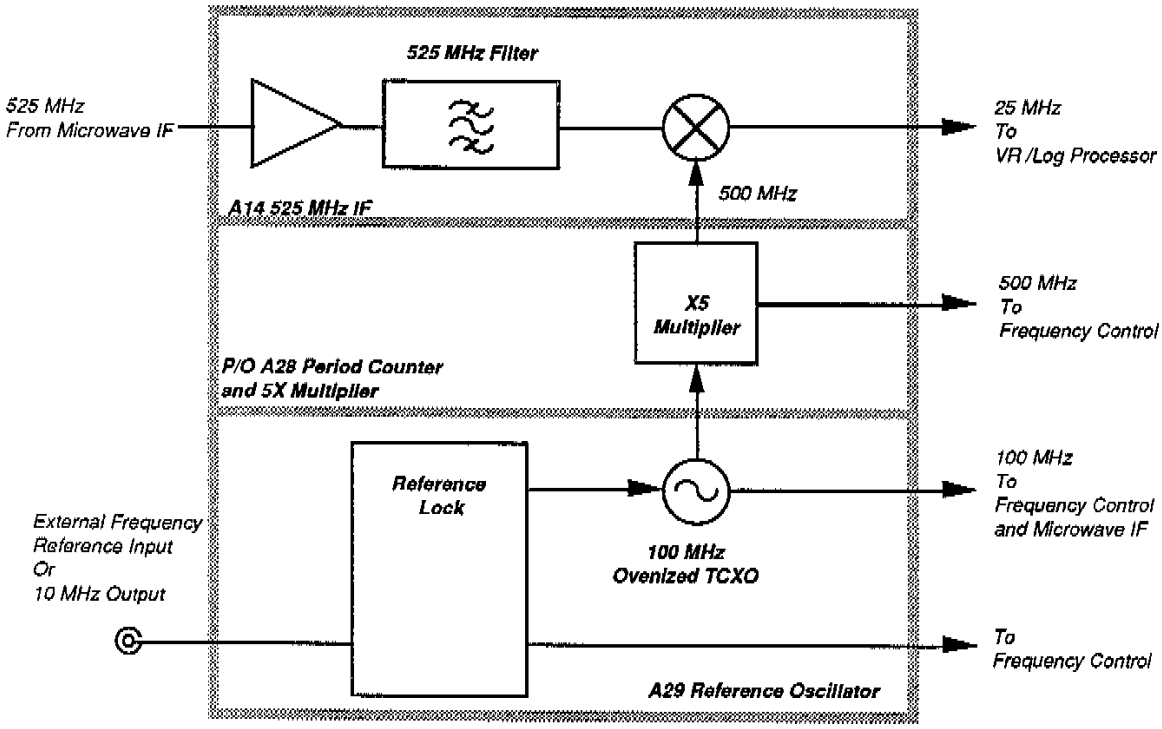


Figure 5-4. 3rd Converter

525 MHz IF

The 525 MHz IF converts the Second Converter 525 MHz output to 25 MHz. The module is mounted on the RF deck just forward of the VR. The module can be viewed as having three main circuits; an input amplifier, a bandpass filter, and a mixer.

525 MHz Input Amplifier

The input circuit acts as a buffer between the second and third converters, and includes filtering to reject the 475 MHz image from the mixer in this stage.

525 MHz Bandpass Filter

The bandpass filter has about 10 MHz bandwidth and works with filters in the VR circuit to produce the wide resolution bandwidths.

525 MHz Mixer

The mixer is driven by the 525 MHz IF signal and by the 500 MHz LO signal from the X5 Multiplier. The LO signal is amplified on this module to produce a high level, about +17 dBm, for driving the mixer. The 25 MHz mixer output then drives the VR stage.

Reference Oscillator

The Reference Oscillator (A29) provides the instrument with its frequency reference. An internal 100 MHz oven-compensated crystal oscillator (OCXO) acts as an accurate and stable frequency source. A phase lock circuit allows locking the 100 MHz source to an external source. If needed, a 10 MHz output signal, derived from the 100 MHz source, can be selected instead of an external input.

100 MHz Source

The signal source is a low phase noise 100 MHz oscillator. Four separate isolation amplifiers buffer the oscillator output to drive . The 100 MHz oven-compensated crystal oscillator (OCXO) is powered from the standby +18 VS re-regulated to +15 V. The oscillator is operating whenever the line cord is plugged in (Standby mode) to minimize warm up frequency error. The OCXO has a tune input that is used for fine adjust or to phase lock to an external reference.

Isolation Amplifiers

Isolation amplifiers feed P14, P500, P501, and the internal dividers. The amplifiers to P14 and P500 are identical, providing +3 dBm outputs to the X5 Multiplier . The amplifier to P501 is a common emitter amplifier with –3 dB gain. The fourth amplifier buffers the oscillator signal to the internal dividers.

Dividers

Two cascaded decade dividers are used for external reference lock and sweep time calibration. The first divider operates continuously to provide a 10 MHz signal. When internal reference out is selected, the signal is switched to a high current, low impedance buffer. Added series resistance provides a match to 50 ohm loads. The 10 MHz also feeds the phase lock circuit and the second, switchable, decade divider. The 1 MHz output connects to J10-B1 and is used by the period counter to measure sweep gate duration.

Reference In/Out

A bnc connector on the rear panel connects through the mother board to J10-A9 where three circuits are connected. The buffer and series resistance were mentioned above as a signal source. This is the 50 ohm load when an external signal is applied. A detector is used to signal that a signal is present, and an isolation stage improves switch isolation.

External Phase Lock

When an external signal is present, it can be checked and verified suitable to use for locking. The signal is divided to 1 MHz and phase/frequency detected. The signal is low pass filtered and converted to single ended operation. A loop integrator sets a critically damped 0.1 Hz bandwidth. If the integrator reaches an excursion limit, the input will have to deviate from 0 volt. A detector detects a + or – excursion and trip the data latch. A switch circuit selects between lock to an external reference or lock disable. The Tune adjustment allows fine tuning the source when lock is disabled. A diode makes a single break point shaper and a tune voltage limiter for the OCXO tune port. With the very narrow lock bandwidth, the loop takes nearly 30 seconds to reach lock and stabilize. the narrow bandwidth minimizes the addition of external reference noise and sidebands to the reference signal.

The 1 MHz lock frequency is divided by sixteen before sending signals on to the Period Counter.

Digital Control

A slave-serial interface chip (SIC) communicates with the instrument main processor. A set of latches provide five different control lines for the module. Two data lines return status information. Data line I0 is connected high to indicate the use of a 100 MHz OCXO. The SIC control lines connect directly to the divider to set the divide ratios.

Power

A voltage regulator circuit provides independence from instrument voltages. This is followed by an active filter to supply the buffer amplifiers and phase lock buffer. There is a second active filter inside the shielded compartment. A third active filter provides +5 V to critical digital circuits.

X5 Multiplier

The X5 Multiplier is the source of 500 MHz signals used in the instrument. The circuits are found on the Period Counter and 500 MHz Sources assembly (A28), which contains two sub-assemblies – the Period Counter (A28A2) and the X5 Multiplier (A28A1). The entire assembly is replaceable as a single unit. The Period Counter is described with the Frequency Control circuits, later in this section.

Three 500 MHz signals are derived from a common 100 MHz input. This signal comes by coaxial cable from the Reference Oscillator (A29) and drives the X5 multiplier. The X5 output is buffered and sent to a bandpass filter. The filter drives three output amplifier-isolation stages.

Two low level amplifiers are identical and driven from a tap on the band pass filter. Each has three common base stages with the first and last having tunable resonators.

The high level amplifier is driven from the top of the bandpass filter and uses two common base stages (at higher current), an interstage resonator, and a 2:1 output transformation. Part of the 100 MHz signal is routed to a buffer and interconnect pins route to the Period Counter board.

Calibrator

The Calibrator assembly, A15, supplies a reference amplitude and frequency that is used in the self-test, or calibration mode of operation. Two outputs supply calibration signals for the instrument. One output goes to the MTX assembly (A13) where it provides an accurate 100 MHz amplitude and frequency reference for internal calibration. The second output contains harmonics and routes to the front panel as a calibration reference. The self correction routines compare the 100 MHz fundamental and the 6.4 GHz harmonic to characterize band 1 and band 2.

Two sets of circuits process the signal. One set has a leveling circuit for accurate amplitude calibration, and the other set generates harmonics for a comb of frequencies.

The 100 MHz signal from the Reference Oscillator (A29) in the 3rd LO routes through the Microwave IF Phase Lock assembly via connector J151. This signal is routed from the Phase Lock in order to limit the number of coax lines running through the instrument.

The 100 MHz signal passes through a splitter amplifier that provides two outputs of approximately +10 dBm. One of the outputs goes to an amplifier that drives a snap diode, generating a harmonic-rich output spectrum. This output spectrum can be switched on or off. A high-pass filter removes the fundamental from the output spectrum. A diplexer at the output combines the harmonic comb with the leveled 100 MHz from the hybrid circuit to provide an accurate calibration signal at the output.

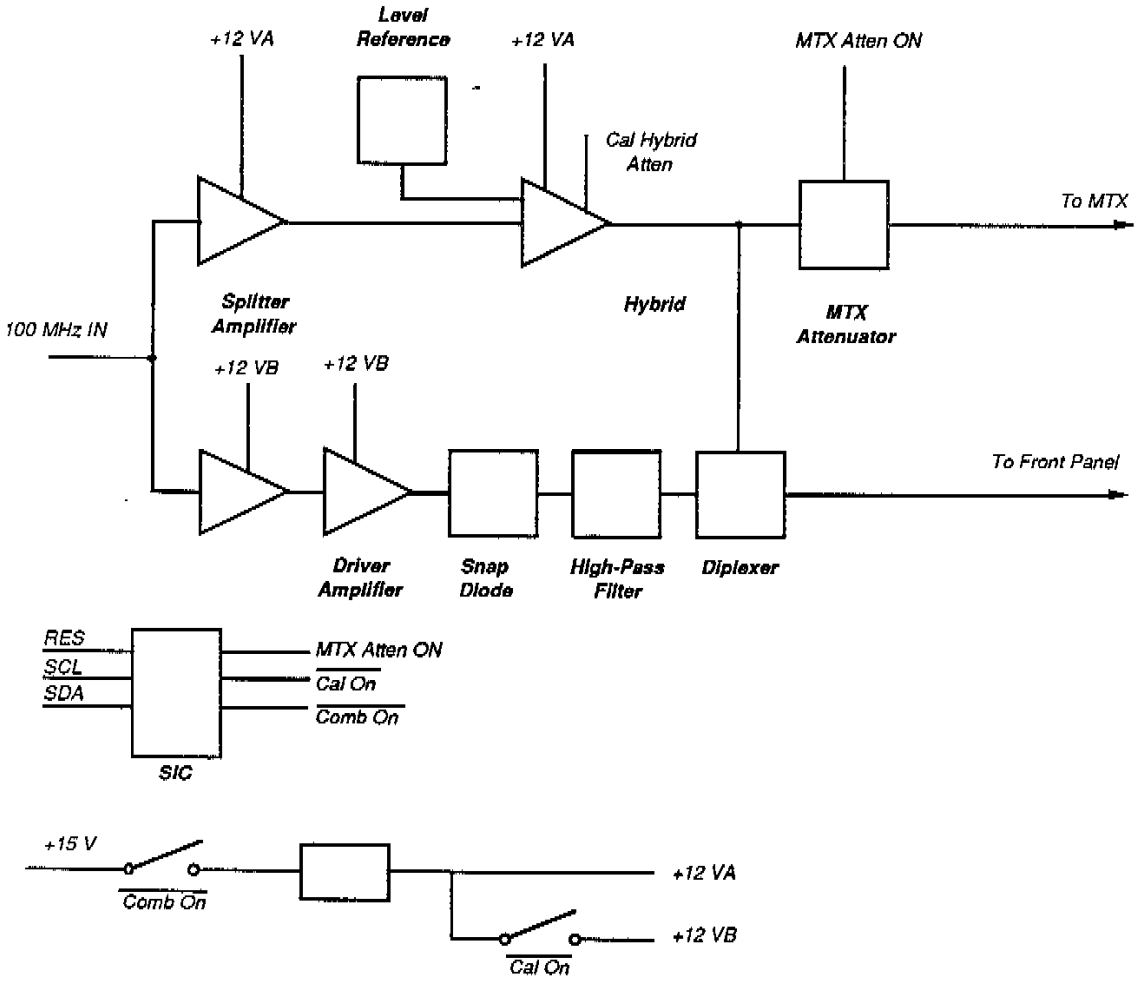


Figure 5-5. Calibrator Block Diagram.

The other splitter output goes to a hybrid amplifier that has an internal detector and leveling circuit. A reference network external to the hybrid sets the desired output level of the amplifier to –20 dBm and is adjustable by approximately ±1 dBm.

The hybrid amplifier output can be inhibited during modes of operation where this output is not desired, adding to the overall attenuation through the assembly. The hybrid amplifier's output is split along two paths. The first path is to an attenuation unit that adds approximately 30 db of attenuation to the signal path when selected. This output is through connector J150 and goes to the MTX assembly in the instrument. A dc switching voltage is also carried on this line to control an attenuator on the Low Pass Termination board in the MTX assembly.

The second signal path from the hybrid joins the harmonic-rich signal described previously and is routed to the instrument Front Panel connector J152 for the external reference.

The Calibrator is addressed by the instrument Main Processor via the serial bus at hex address B4. Three signals are decoded from the serial bus; the COMB ON, CAL ON, and MTX ATTEN ON signals. The CAL ON signal switches the +12 V regulator on and off to control both paths. The COMB ON signal also switches the +12 V output to the amplifiers in the harmonic generator, allowing separate control of those circuits. The CAL HYBRID ATTEN signal is derived from the CAL ON signal. When the calibrator is on, the hybrid attenuation is off.

All of the voltages required for Calibrator operation are obtained from the instrument motherboard by way of the 20-pin connector and are filtered to reduce noise. The +15 volt and –15 volt supplies are re-regulated to +12 and –12 volts respectively and distributed throughout the unit.

Variable Resolution (VR)

The Variable Resolution (VR) module, A16, amplifies and bandpass filters the 25 MHz IF signal. The module accepts an input frequency of 25 MHz at a nominal power level of –37 dBm. This signal is bandpass-filtered and amplified to a level of +10 dBm to drive the log amplifier. Bandwidth is selectable from 10 MHz to 3 Hz in 1–3–10 steps.

The 10 MHz and 3 MHz bandwidths are filtered at the 25 MHz IF. In bandwidths 1 MHz and below, the 25 MHz signal converts down to 4 MHz. The bandwidth of the 4 MHz center frequency bandpass filters is variable from 3 Hz to 1 MHz.

The circuitry is divided between four assemblies, VR #1 through VR #4. VR #1, A16A1, receives the 25 MHz IF output signal from the 525 MHz IF module. The circuits on VR #1 amplify, select bandpass paths, and filter the signal. The second VR stage, A16A2, converts the 25 MHz IF to 4 MHz, provides pre-filter gain compensation, and the first three variable bandwidth resonators. The VR #3 board, A16A3, has the last three of the six variable bandpass filters in the VR module, and has a post-filter gain stage that works in conjunction with the pre-filter gain stage on VR #2. VR #4, A16A4, is the power supply and microprocessor interface board.

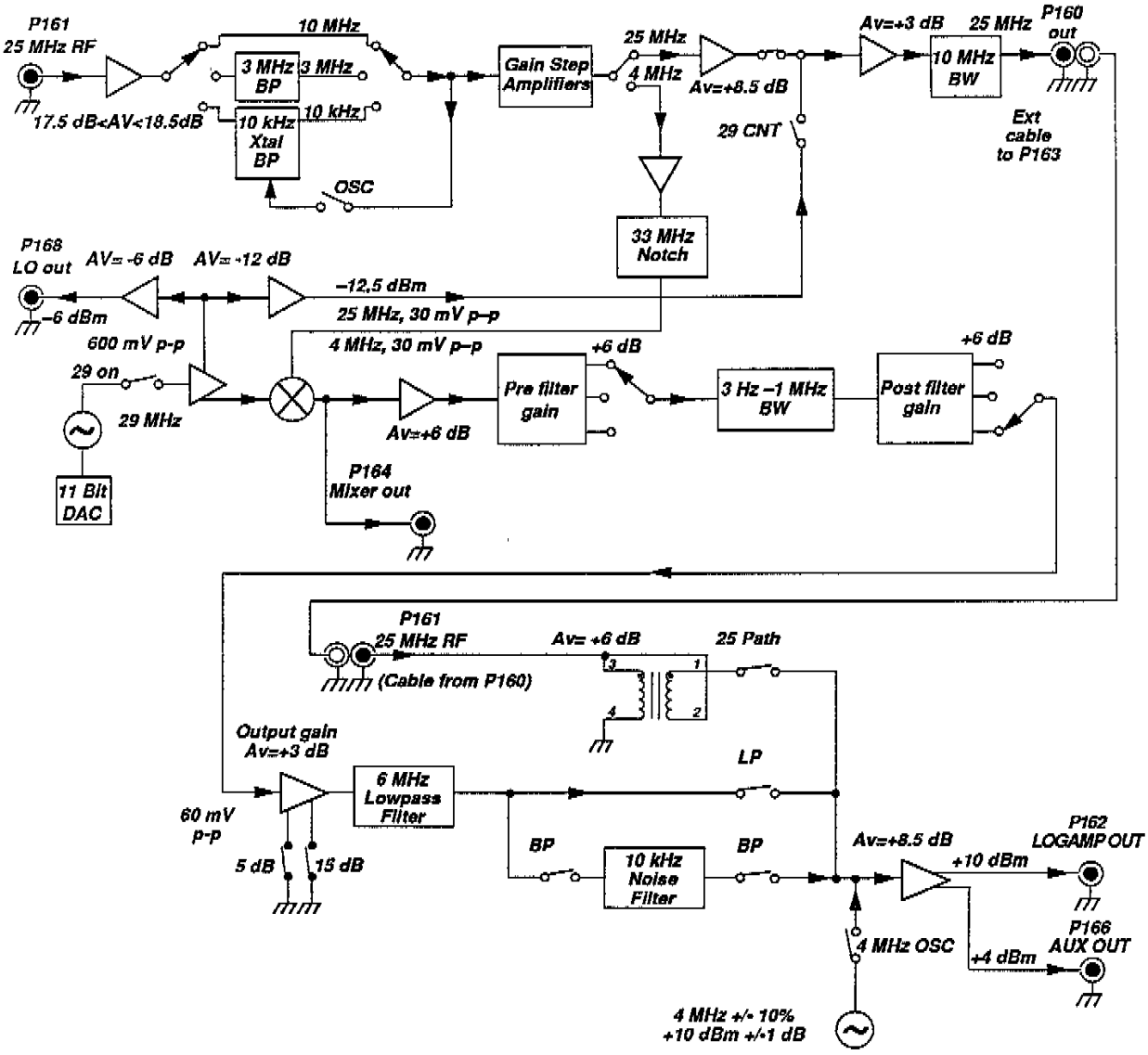


Figure 5-6. Variable Resolution Block Diagram.

Input Amplifier

The input is amplified by a fixed gain stage. The output of this stage feeds to one of three bandpass paths. The path used depends on the instrument bandwidth:

10 MHz Bandpass	10 MHz Path (No Filtering)
3 MHz to 10 kHz	3 MHz Path
3 kHz through 3 Hz	10 kHz Crystal Path

For self-correction, the 10 kHz crystal bandpass filter is connected as a 25 MHz oscillator to generate a signal for ringdown log correction and frequency counting of the resonators.

Gain Step Amplifiers

After a path is selected, three variable gain amplifiers provide gain steps. The first and third stages are identical transformer step up/down stages, while the second amplifier is controlled by a DAC with approximately 0.05 dB/LSB resolution. The output of the third variable gain stage drives two buffer amplifiers. One drives the 25 MHz path and one drives the 4 MHz path.

25 MHz Path

The output of 25 MHz path buffer has an additional 10 dB of gain and a 10 MHz bandpass filter with a 25 MHz center frequency. This output is sent to VR #3 as the 25 MHz IF signal. The signal is routed via a coaxial cable outside of the VR module.

4 MHz Path

The 4 MHz path provides the variable resolution bandwidth filtering for bandwidths below 3 MHz. The 25 MHz signal is converted to 4 MHz required by the resonators in the filter.

33 MHz Notch Filter

The other buffer has a 4 MHz bandpass at 25 MHz with a notch filter at 33 MHz to help eliminate unwanted 4 MHz ghost products from the mixer in the next stage. This output is then sent to VR #2, A16A2, for variable bandwidth filtering.

Mixer and 29 MHz LO

On VR #2, the 25 MHz IF signal mixes with a 29 MHz crystal oscillator signal to obtain the 4 MHz IF. The 29 MHz local oscillator is tuned by a DAC so that the output of the mixer is at the common center frequency of the resonators. The oscillator signal is sent through a buffer amplifier to a separate output for other applications.

Pre-Filter Gain

A pre-filter gain stage works in conjunction with the post-filter gain stage on VR #3. These two stages together keep the power into the resonators from going too high while at the same time not losing any gain through the resonators.

Variable Bandwidth

There are six resonators in the variable bandwidth stage. The first three resonators are on VR #2, and the last three are on VR #3. There is an amplifier after each three stages. Bandwidth is controlled by selecting LC or crystal resonators, and by adjusting the resonator termination resistance.

Post-Filter Gain

A post-filter gain stage works in conjunction with the pre-filter gain stage on VR #2. These two stages together keep the power into the resonators from going too high while at the same time not losing any gain through the resonators.

Output Gain and Filters

After the post-filter gain, another variable gain stage sets the correct output power range. For an improved noise figure, a 6 MHz low pass filter follows the variable gain amplifier. When in the narrow bandwidth filters, an additional 10 kHz noise filter can be inserted.

VR Output

The 25 MHz Path signal, from the 10 MHz and 3 MHz filters, is switched into the output buffers after the noise filters. There are two output buffer amplifiers. One drives the log processor module (internal video channel), while the other is an auxiliary output for external signal processing applications. There is also a 4 MHz oscillator to test the video channel during self-correction.

Control Circuitry

The logic control circuitry on VR #2 consists of shift registers and DACs used to develop the adjustment signal for tuning each resonator to a common center frequency, setting the resonator bandwidth, and zeroing out the resonator resistance losses. VR #3 is connected to VR #2 through a 20 pin cable.

Logic control circuitry adjusts the resonator center frequencies, coarse bandwidth modes, pre-gain level, 29 MHz oscillator ON mode, and frequency control. Resonator bandwidth information and the signal for zeroing out the resonator resistance are received from the VR #3 board, A16A3. The VR #2 board is connected to the VR #1 and VR #3 boards through 20 pin cables.

VR #4, A16A4, contains the power supply and microprocessor interface board. The low frequency power supply decoupling circuits are on this board. Also, the serial interface and module logic driver circuitry reside here. This module is mounted outside the VR assembly on one end, and is connected through the box by an EMI suppressor connector to the VR #3 board.

Log Processor

The Log Processor module, A18, consists of the Log Amplifier on the back side of the board, and the Video Preprocessor on the front. The main functions of the log processor are listed below.

- Detect the IF signal from the VR
- Provide frequency output to Period Counter
- Filter IF from the detected signal.
- Provide linear or power modes of operation.
- Scale the filtered video signal.
- Add or subtract offset from the video signal
- Correct for hinge point offsets
- Correct for frequency unflatness in the front end.

Log Amplifier

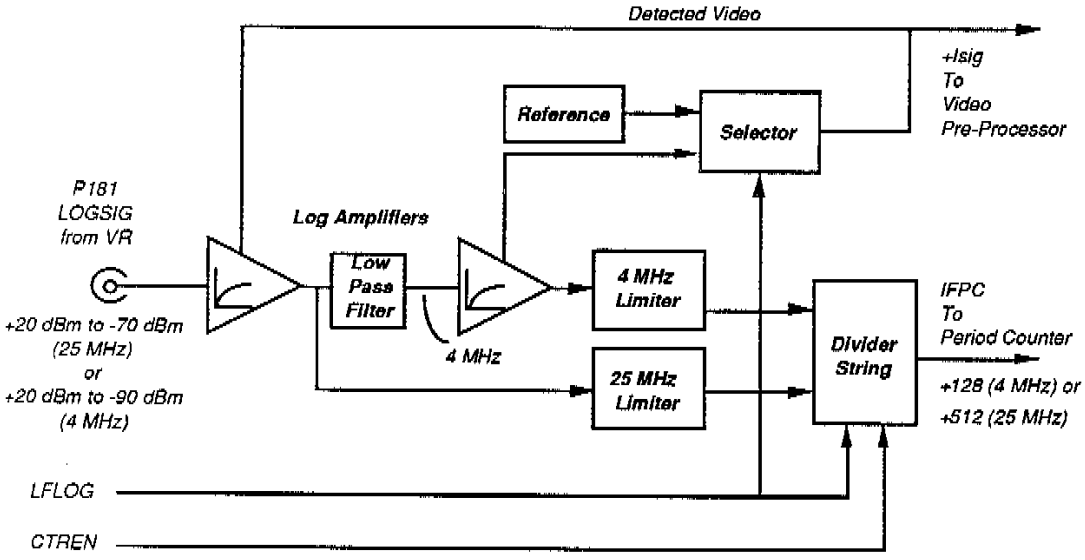


Figure 5-7. Log Amplifier Block.

The Log Amplifier logarithmically amplifies the VR signal to provide an output that can be calibrated in decibels. The VR signal arrives at anywhere from +20 dBm to -70 dBm for the wide bandwidths that use the 25 MHz IF, and at +20 dBm to -90 dBm for the narrower bandwidth signals using the 4 MHz IF. More stages of amplification are included for the narrower bandwidths to account for the lower noise floor at those bandwidths.

The amplifier stages provide detected video outputs that are summed to drive the Video Preprocessor. This is a current output at 14.1 mA for a +20 dBm input signal. The signal changes at 80 µA/dB of input signal change.

The LFLOG signal sets the amplifiers for 4 MHz or 25 MHz operation. When LFLOG is low, 25 MHz operation is selected; and when LFLOG is high, 4 MHz operation is selected.

The amplifier stages also provide IF outputs. These outputs are limited through a 4 MHz Limiter and a 25 MHz Limiter to drive a divider string The Divider String provides a TTL output signal, IFPC, to the Period Counter. The CTREN signal enables the divider string, and the LFLOG signal selects the divide ratio; 128 for the 4 MHz IF or 512 for the 25 MHz IF. The LFLOG signal is low when the 25 MHz IF is in use, and high for the 4 MHz IF.

Video Preprocessor

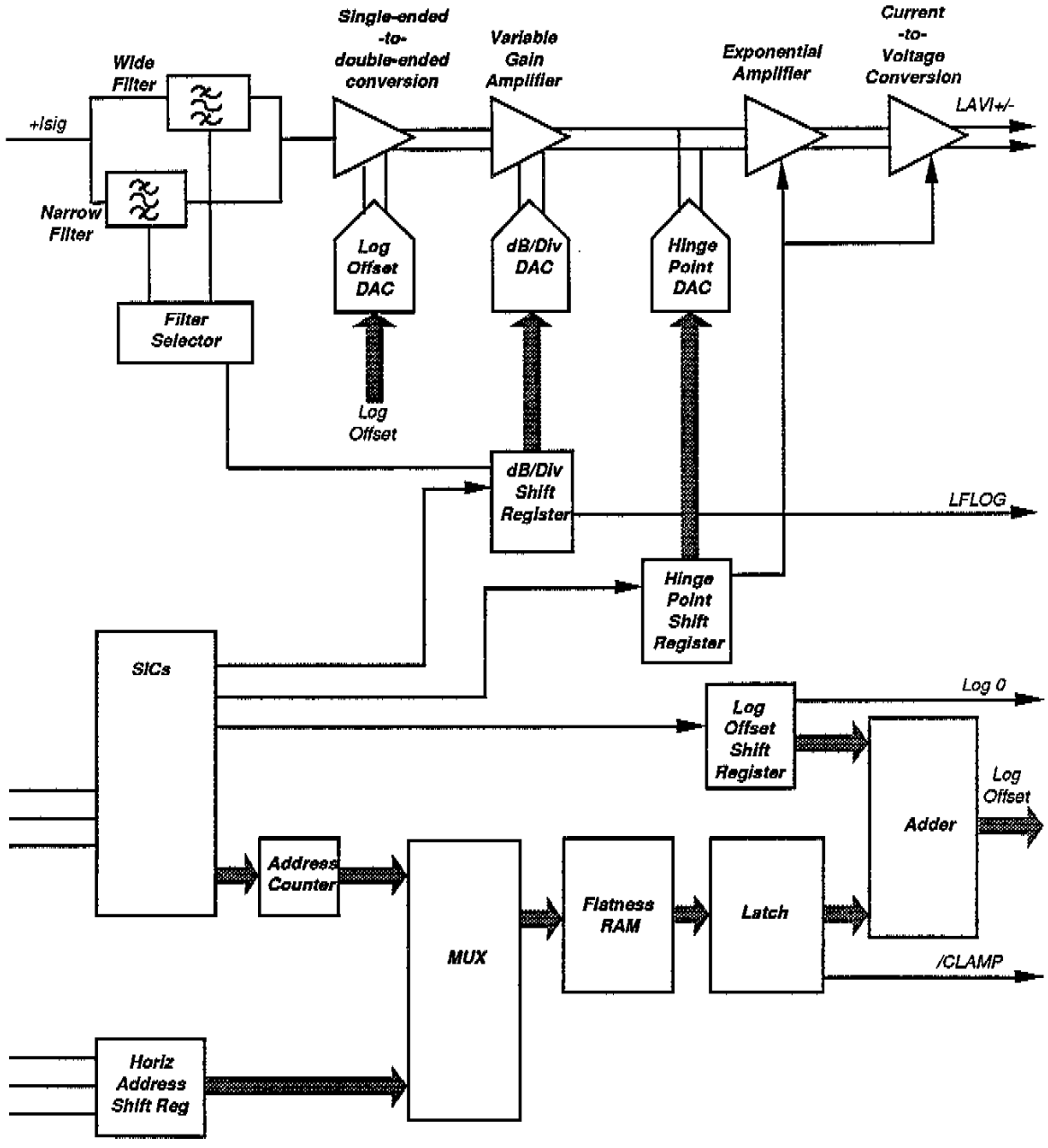


Figure 5-8. Video Pre-Processor

The Video Preprocessor filters the Log Amp output; sets the offset, vertical scale, and hinge point; performs the log/linear conversion for linear modes; and compensates for front end frequency unflatness.

The Log Amp output (+Isig) is filtered to remove the IF component of the detected signal. A narrow bandwidth filter (1 MHz) is used for the 4 MHz IF and bandwidths below 1 MHz. A 10 MHz bandwidth filter is used for the 25 MHz IF for resolution bandwidths of 3 MHz and 10 MHz.

Signal offset is added or subtracted to the video signal in front of the scaling amplifier. This sets the reference power level of the "hinge point". The hinge point is a point on screen that doesn't move when gain scaling is changed, and this is where the differential input to the analog multiplier is zero. The log offset adjustment is accomplished by a 12 bit current output DAC loaded with data from the Log Offset Shift Register and the Flatness RAM.

The filtered video is scaled from 1 dB/div to 15 dB/div. In linear mode 10 dB/div is selected and in power mode 5 dB/div is selected along with the exponential IC in exponential mode. Gain scaling is achieved by a 12 bit current output DAC, that sets a bias control current on an analog multiplier cell.

Ideally the hinge point is at the top-of-screen. To correct for any system offsets the hinge point can be moved around by another 12 bit current output DAC. This DAC adjusts the differential current level between the scaling amplifier and the exponentiator amplifier.

The post log signal is exponentiated in order to provide linear or power modes of operation. This operation is done via a monolithic exponential converter IC.

Frequency unflatness of the front end of the instrument is corrected by summing the log offset bits with the output of one of 250 locations of an 8 bit by 2K RAM, for four horizontal screen locations. The resulting sum is input to the log offset DAC.

Display Section

The Display Section is composed of the major components listed below:

- Video Processor (A20)
- Digital Storage (A24)
- Display Amplifiers (A22)
- High Voltage Power Supply (A23)
- CRT and Color Shutter

The Display Section displays the response of the analyzer as it appears at the output of the Log Processor. This response may be digitized and viewed as a stored waveform, or viewed directly in "real-time" mode. In both "stored" and "real-time" modes, the waveform may be filtered to reduce the level of the noise displayed on screen. In the "stored" mode, a number of other options become available to the user. The waveform may be digitized in one of four acquisition modes: Sample, Max Hold, Min Hold, or Min/Max. In all modes but Sample, the waveform is "peak-detected" so that narrow pulses are captured by the digitizer. The digitized waveform may then be averaged with successive sweeps, stored for later viewing or plotting, or processed using the available math functions.

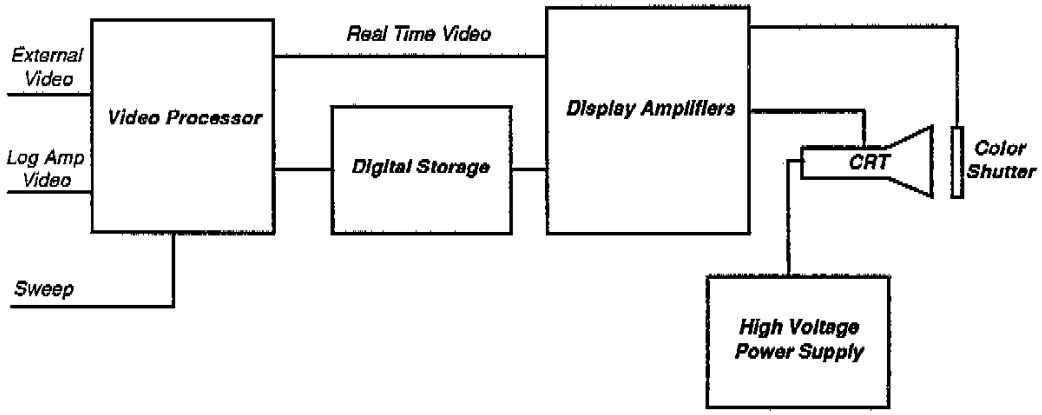


Figure 5-9. Display System Block Diagram.

Video Processor

The Video Processor Module receives either the video signal output from the Log Processor (LAVI+/-), or an external video input from the rear panel (EXTVI+/-), and performs a 10-bit digitization on the signal. The module also digitizes a sweep output (SWEEP+/-) from the Sweep/Span Attenuator Module (A33). The sweep output is used to associate the digitized vertical data with a particular frequency location on screen. The Video processor sends this digitized horizontal and vertical information serially to the Digital Storage Module for further processing, and to be displayed.

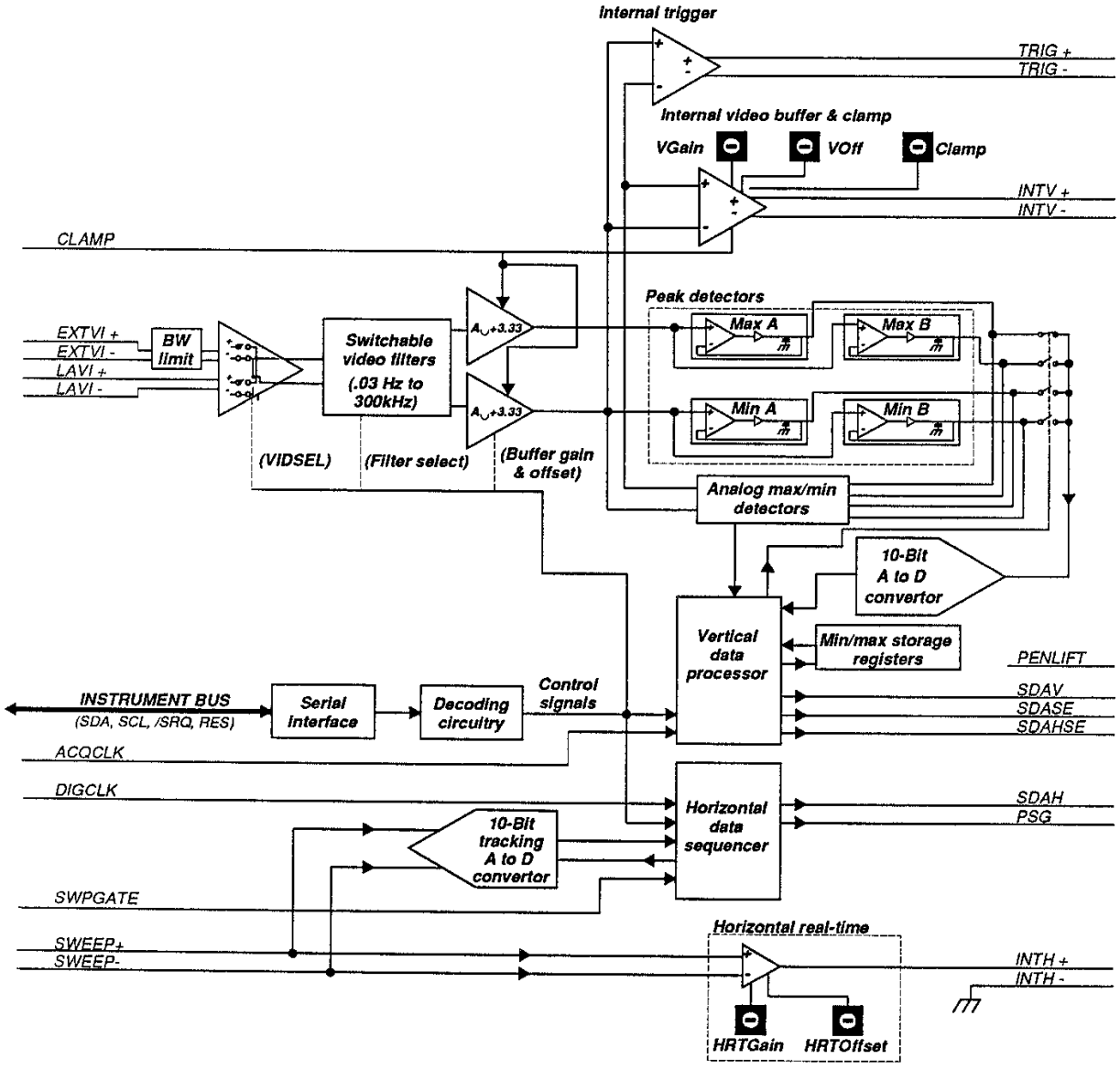


Figure 5-10. Video Processor Block Diagram.

The Video Processor Module is capable of processing the video input signal by means of an array of switchable low-pass filters with bandwidths ranging from 300 kHz to 0.03 Hz. The module also contains four peak detectors for capturing narrow pulses. These four detectors (two positive and two negative) are controlled in a way that minimizes the possibility of a narrow pulse escaping detection. Video amplifiers are also included in the module to scale and buffer the internal video signals that are sent to the Display Amplifiers Module.

The Video Processor also performs some basic digital signal processing on the digitized data in Min, Max, and Min/Max acquisition modes before the data is

sent to the Digital Storage Module. This processing consists of determining the minimum and maximum digitized values from within one horizontal location, and then, depending on the acquisition mode, transmitting the appropriate value.

Digital Storage

The Digital Storage Module receives the serially transmitted vertical and horizontal digitized data from the Video Processor Module. It converts this data, via the 80C186 display microprocessor, into a form that can be processed by the Vector Display chip set. It also makes this data available to the main instrument processor, thus providing closed loop feedback of frequency and amplitude information within the instrument, allowing self-correction firmware routines to "see" the results of current and past instrument settings.

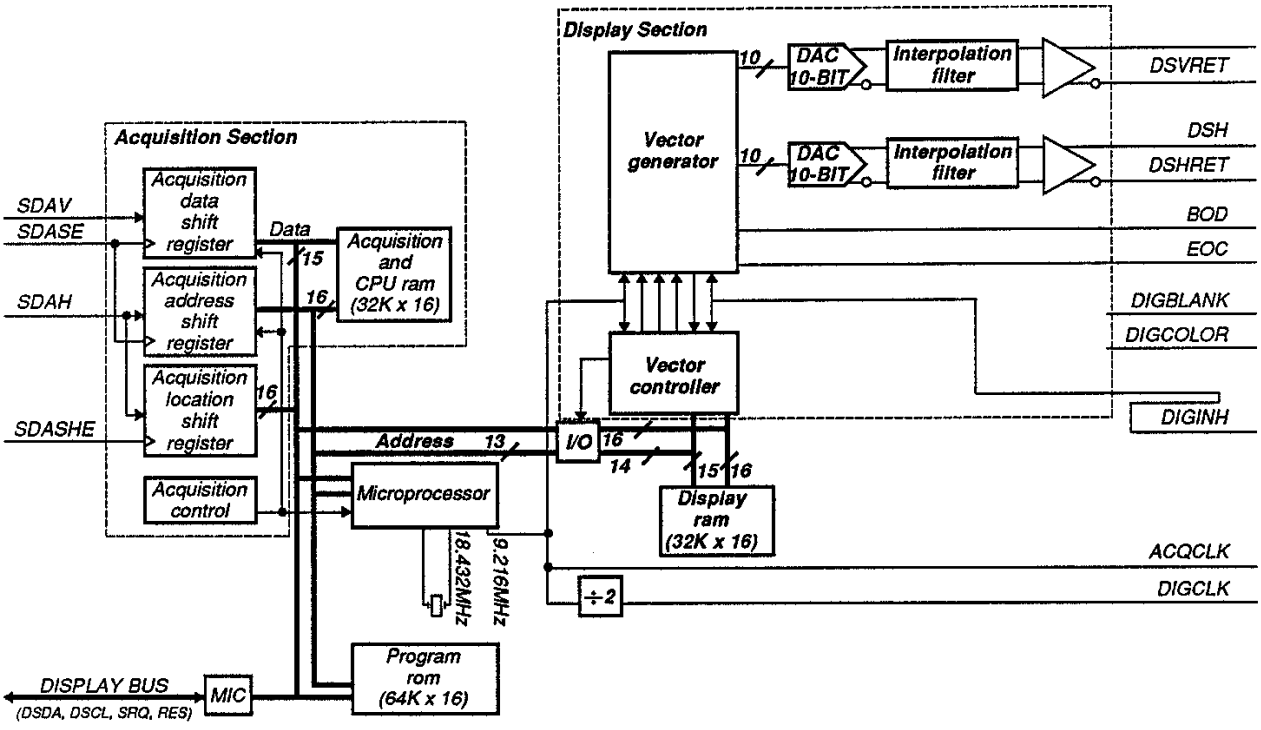


Figure 5-11. Digital Storage Block Diagram.

In addition to facilitating the flow of acquired data into memory, the display microprocessor may also mathematically manipulate this data, or aid in waveform transfer via the instrument serial bus. It also modifies the display control program to keep the screen updated with current readout and menu information.

The Vector Display chip set consists of the Vector Controller and Vector Generator IC's. Together, these two IC's generate the display pattern on the screen. The pattern can include digitized waveforms, readout, graticules, and

menus. The Vector Controller IC functions as a dedicated processor that shares the address and data busses with the display microprocessor. The Vector Controller executes the display control program, which consists primarily of statements that translate into "moves" and "draws" on the screen, and to a lesser extent, instructions that control the flow of program execution. The display control program is copied from program ROM into display RAM upon power-up and gets modified during instrument operation by the display microprocessor. The Vector Generator IC, along with two 10-bit dacs and interpolation circuitry, takes the digital information representing vector lengths and locations from the Vector Controller, and generates the low-level deflection and blanking signals that are sent to the Display Amplifiers Module to drive the cathode ray tube (crt).

Display Amplifiers

The Display Amplifiers Module receives low-level deflection signals from the Video Processor and Digital Storage modules, and the rear panel, then multiplexes and amplifies them to generate the horizontal and vertical signals that drive the crt deflection plates. The module also processes blanking signals from the above sources, along with intensity and focus information derived from front panel inputs, to generate the intensity (grid-drive) and focus signals that are applied to the crt.

In addition, the circuitry to control the various display modes for displaying one or more channels simultaneously (i.e. – "Real-time" mode) is located in the module in the form of a semi-custom cmos IC. This dedicated display controller asynchronously receives handshaking signals from the Digital Storage Module, and performs all the necessary channel selection and blanking to allow multi-source displays.

Finally, the Display Amplifiers module contains the circuitry that drives the Liquid Crystal Color Shutter (LCCS). The state of the LCCS (Red or Green) is determined by the Digital Color (DIGCOLOR) signal that is generated in the Digital Storage Module.

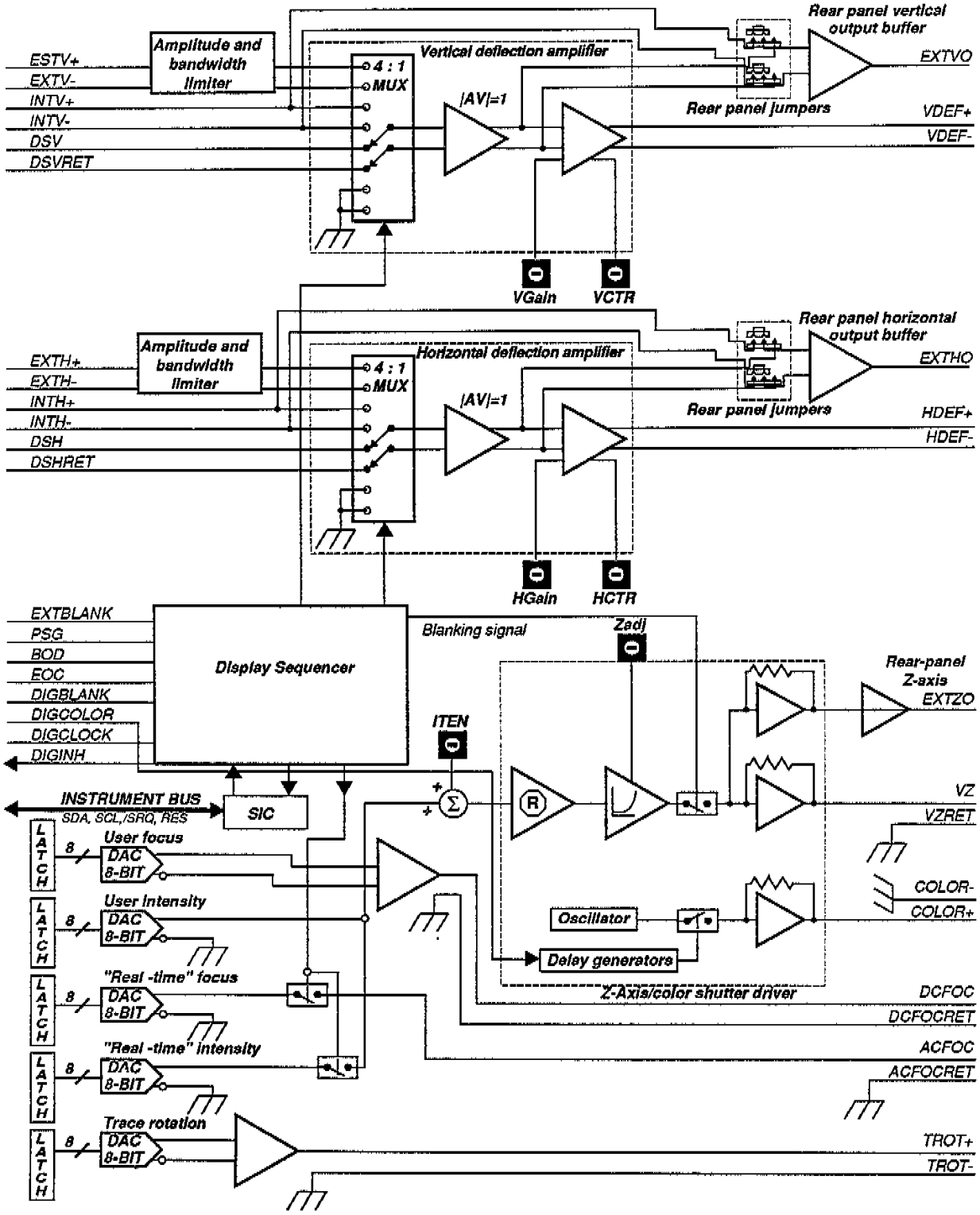


Figure 5-12. Display Amplifiers Block Diagram.

High Voltage Power Supply

The High Voltage Power Supply provides the bias and control voltages required to operate the crt. The module contains an oscillator that converts power from a low voltage un-regulated supply to a voltage level usable by the crt and its support circuitry. Because of the high voltages present, a portion of the circuitry is encapsulated.

Warning

The crt anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short the anode lead to the main chassis immediately after disconnecting the lead. Hold the lead to the chassis for at least one minute to fully discharge the crt.

Caution

The high voltage charge on the anode lead can damage other circuits in this instrument. Be sure the card cage covers are all installed, and fully discharge the anode lead only to the main chassis, as described above.

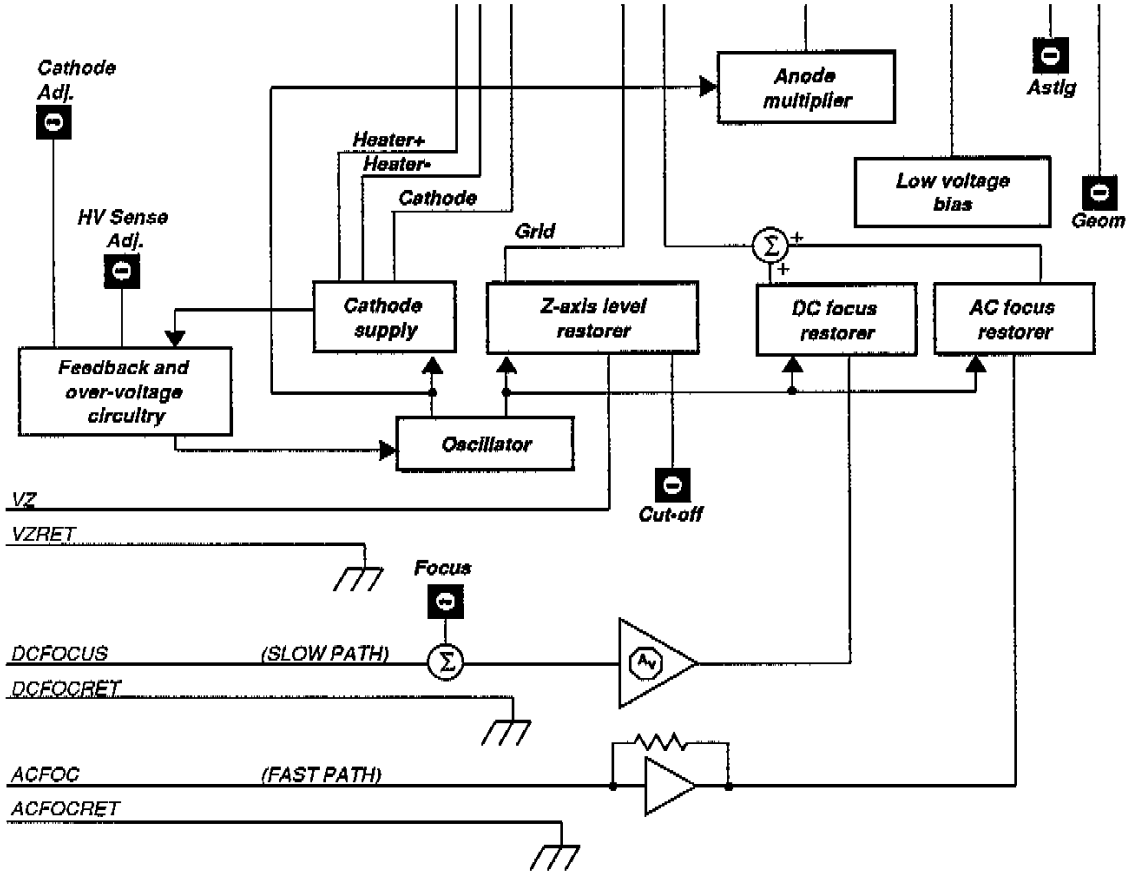


Figure 5-13. High Voltage Block Diagram.

This module accepts the low-level ac and dc focus signals (ACFOC and DCFOCUS) from the Display Amplifiers module, amplifies, level-shifts, and sums them together to form the "FOCUS" signal which sets the potential on the focus barrel in the crt. It also receives the grid drive signal (VZ) from the Display Amplifiers module, which it level shifts and references to the cathode potential.

Adjustments on the module allow the setting of the cathode potential, over-voltage shutdown point, cut-off, focus, astigmatism, and geometry.

The secondary voltage in the supply is monitored by a circuit which detects when the voltage level exceeds 7% of its nominal value, and shuts down the oscillator to prevent excessive x-radiation emission from the crt. This circuit may be disabled by means of a movable jumper on the circuit board to allow servicing of the module.

CRT and Color Shutter

Warning

The crt anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short the anode lead to the main chassis immediately after disconnecting the lead. Hold the lead to the chassis for at least one minute to fully discharge the crt.

Use extreme care when handling the crt. If the crt breaks, an implosion may result causing glass fragments to scatter at high velocity. Wear protective clothing and safety glasses when handling the crt.. Do not allow the crt to strike against anything that might cause it to crack or implode. When storing a crt, place it in a protective carton if available, or set the crt face down on a soft mat in a protected location that has a smooth surface.

Caution

The high voltage charge on the anode lead can damage other circuits in this instrument. Be sure the card cage covers are all installed, and fully discharge the anode lead only to the main chassis, as described above.

The crt is an electrostatically deflected, post-deflection accelerated tube. The tube has a dispenser cathode, which gives the tube extremely long lifetimes even under high duty, high drive operating conditions. The tube uses a special phosphor with a spectral emission optimized for use with the "red-green" Liquid Crystal Color Shutter (LCCS).

The crt light output passes through the Color Shutter, which functions as an electronically controlled optical filter. In the driven state, the color shutter allows transmission of the green spectral component of the phosphor, while the red component is suppressed. In the off (or semi-relaxed) state, the red spectral component of the phosphor is transmitted, while the green component is suppressed. To give the appearance of a multi-color display, the shutter is switched between its "green" and "red" transmission states each display frame. The color of the waveforms and characters on the screen will be determined by the state of the color shutter when they are drawn. A display drawn once in the "green"state, and then again in the "red"state, will appear yellow. The states are controlled by the Digital Storage Module.

Frequency Control

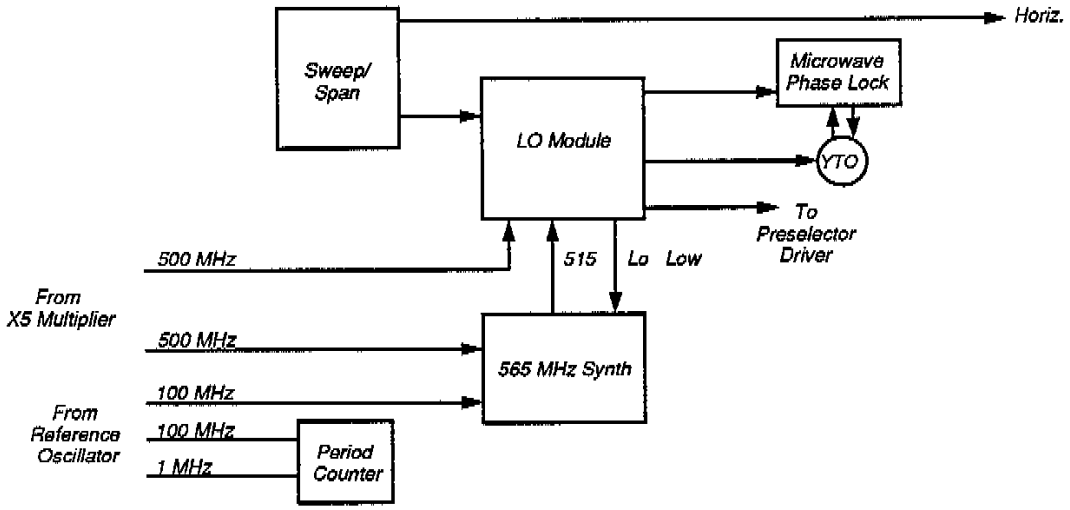


Figure 5-14. Frequency Control Circuits.

The Frequency Control circuits provide the tuning and scan functions for the 1st LO and also provide the sweep voltage for the horizontal deflection circuits. This section contains the following major circuits.

- Sweep/Span
- 565 MHz Synthesizer
- Microwave Phase Lock
- LO Module
- Period Counter

These circuits rely on the Reference Oscillator and X5 Multiplier as frequency references. Those circuits are described with the Third Converter. The object of many of the Frequency Control circuits is the control of the 1st LO, which is described with the 1st Converter.

Sweep/Span

The Sweep/Span module generates the horizontal timebase voltage for driving the X axis and the frequency sweep span attenuator that drives the Local Oscillators. In addition, the +10 V reference is also located on this board.

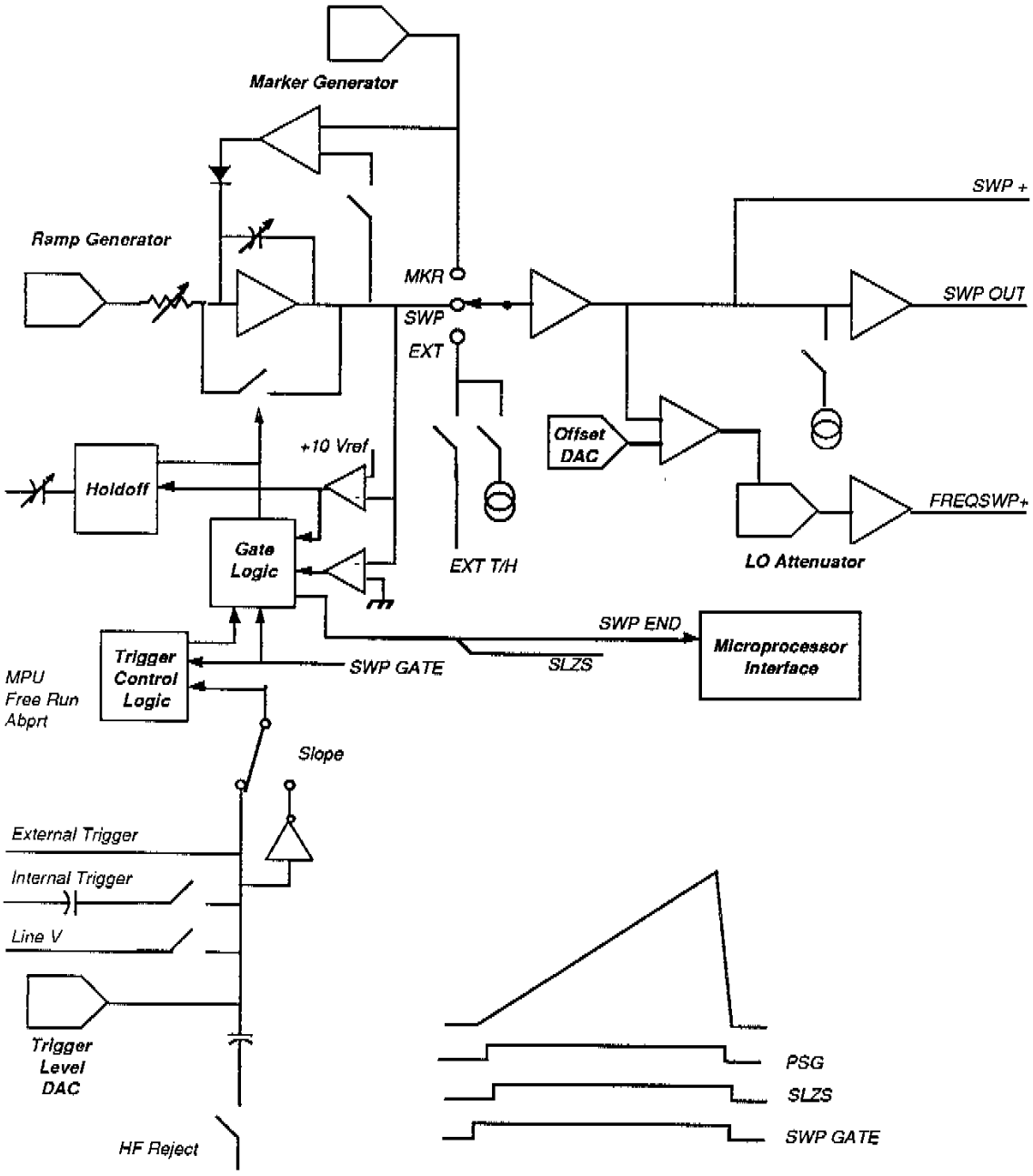


Figure 5-15. Sweep/Span Block Diagram.

Microprocessor Interface

The Microprocessor Interface consists of the SIC, twelve 4-bit latches that are selected by two de-multiplexers, and a pair of microprocessor-compatible DACS that contain internal latches.

There is an interrupt circuit that can be tripped by a Sweep End condition or a TD (Track DAC) interrupt. It pulls on the SRQ and sets a high on an SIC pin. The circuit can be reset by the SIC.

Ramp Generator

This circuit consists of an analog integrator. The heart of the integrator is a JFET input op-amp. Coarse sweep is varied by switching in or out three resistors and three capacitors, while fine sweep adjust is via an 8-bit DAC.

Analog switches select either the Ramp Generator output, External Horizontal input, or the Marker DAC.

Track DAC

This circuit clamps the ramp in place while a marker is being generated. When completed, ramping continues from the stop point. A compensation loop provides at least 45 degrees of phase margin throughout the range of operation.

External T/H Input

An op-amp is set up for differential mode such that an offset is applied by a second op-amp to allow either a -5/+5 V ramp or 0/+10 V ramp input for sweeping the instrument.

LO Attenuator

The LO Attenuator controls the frequency span width. A 12-bit DAC with an output swing up to ±10 V provides the single ended sweep voltage

Trigger

The complete trigger circuit is composed of two edge-triggered D–type flip-flops. the circuit incorporates a trigger enable, slope control via an Exclusive Or gate, a trigger amplifier with a DAC-adjustable trigger level, a switchable 1.6 kHz HF Reject filter, trigger selection via analog switches, and an internal video amplifier to allow more sensitive triggering.

Holdoff

The Holdoff circuit determines the time between retrace and the start of the sweep. This circuit consists of a one-shot multivibrator and switchable capacitors. Control is by a single D–type flip-flop and two comparators. Four different holdoff times are available by switching capacitor values.

Gate Logic

The retrace circuit is composed of a D–type flip-flop that switches a discharge FET on or off. The FET is used to short out the sweep capacitors to generate retrace. A double low input state is used to simplify logic. Appropriate gating is included to insure that the inputs are never switched high at the same time, thereby avoiding an unstable state. When in free run, the clear line is always held low.

Sweep length during zero span (SLZS) is controlled by a single D–type flip-flop and an inverter connected to generate a high during the 11 div sweep window.

+10 V Reference

This an adjustable Zener reference with a transistor buffered op-amp for internal gain. Current limiting is provided by a 78L12 regulator.

565 MHz Synthesizer

The purpose of this module is to produce a spur-free, low phase noise signal from 552 MHz to 579 MHz. This signal is used to phaselock the 129 MHz oscillator in spans of 2 MHz or less.

The module consists of the following circuits:

- 113 MHz Synthesizer
- Fractional N Synthesizer
- Mixer
- Phase Detector
- 565 MHz Oscillator

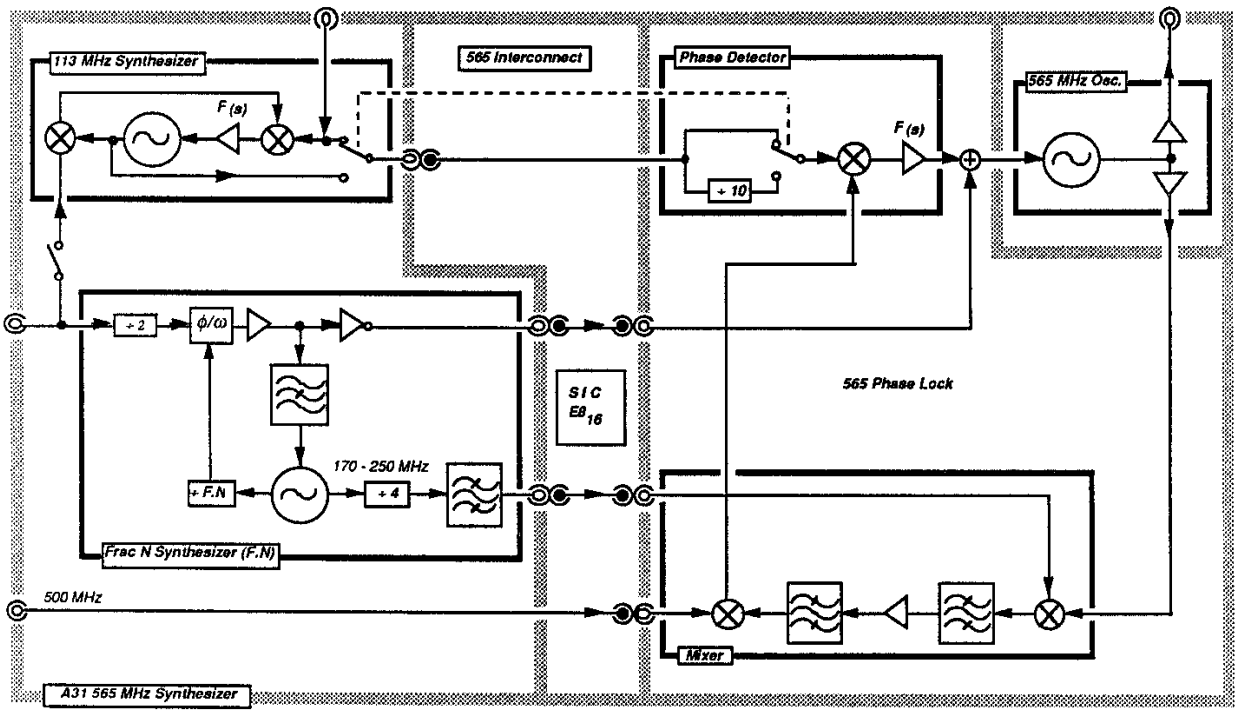


Figure 5 - 16. 565 Synthesizer Block Diagram.

565 MHz Oscillator

The 565 MHz Oscillator provides the 552 MHz to 579 MHz, +3 dBm output to the LO Module. A separate output amplifier also drives the Mixer circuit in the phase lock loop. The frequency is controlled by summing the error signals from the Phase Detector and the Fractional N Synthesizer.

Fractional N Synthesizer

The Fractional N Synthesizer is based on a 170 - 240 MHz oscillator. The oscillator output is divided by a programmable divider and phase/frequency compared against the 100 MHz system reference. The error output is then summed with the output of the Phase Detector circuit to control the 565 MHz Oscillator. The error signal is also fed back to the 170 - 240 MHz oscillator through a band stop filter. The oscillator output feeds a divide-by-four circuit and then a low pass filter to drive to the 565 MHz mixer circuit.

113 MHz Synthesizer

The 113 MHz Synthesizer receives the LO Low signal (10.1 MHz to 16.2 MHz) at 0 dBm from the LO Module. The circuit consists of a 113 MHz oscillator, two mixers, and an error amplifier. The circuit only operates in spans 20 kHz and below. In wide spans, the LO Low signal feeds directly to the Phase Detector.

In narrow spans, the 113 MHz Oscillator drives the Phase Detector circuit. It is controlled by comparing its output to the 100 MHz system reference. The oscillator output drives one input of a mixer and the 100 MHz reference drives the other input. The mixer output drives a second mixer to be compared against the LO Low signal. The second mixer output feeds an error amplifier to control the 113 MHz oscillator.

Mixer

The Mixer circuit is part of the 565 MHz phase lock loop. The circuit contains two mixers, and amplifier, and two bandpass filters. The first mixer is driven by the 565 MHz Oscillator output and by the Fractional N Synthesizer output at 42.5 to 62.5 MHz.

The bandpass filters and amplifier separate the 500 MHz difference frequency to drive the second mixer. The second mixer is also driven by 500 MHz from the X5 Multiplier circuit, derived from the 100 MHz system reference. The output of the second mixer drives the Phase Detector circuit.

Phase Detector

The Phase Detector circuit compares the phase of the Mixer output and either the LO Low signal, or the 113 MHz Synthesizer output. The circuit consists of a divide-by-ten divider, a mixer, and an error amplifier.

In wide spans, the LO Low signal drives the mixer. This is a 10.1 to 16.1 MHz signal. The Mixer circuit output drives the other Phase Detector mixer input. The resulting signal is passed through an error amplifier to be summed with the Fractional N Synthesizer error signal for control of the 565 MHz Oscillator.

In narrow spans, the 113 MHz Synthesizer output drives the divide-by-ten circuit, and then drives the Phase Detector mixer. The divider increases stability

Microwave Phase Lock

The Microwave Phase Lock module (A17) locks the 8-18 GHz 1st LO to a harmonic of the 129 MHz reference oscillator for narrow band sweeps (spans under 2 MHz), and it provides a means of counting the beat note frequency between the 1st LO and the 565/4 MHz output from the LO Module, which is used to calibrate and set the 1st LO.

The module consists of the following circuits:

- Leveling Bandpass Hybrid
- Phase Gate Hybrid
- Strobe Driver
- F(S) Driver

Leveling Bandpass Hybrid

The PIN attenuator sets the level of the 1st LO signal to provide a constant level at the detector output. The attenuator presents a 50 ohm match at the input and output of the attenuator. Attenuation is controlled by the error signal from the detector.

The bandpass filter following the PIN attenuator stops out of band signals from reaching the Phase Gate and also prevents strobe energy from the Phase Gate from coming back through to the 1st LO. The filter has a 12 GHz bandwidth centered at 13 GHz with 0.5 dB of ripple.

A detector following the bandpass filter samples the RF energy to indicate the power level that can be fed back through the error amplifier and control the PIN attenuator to set the RF level and achieve flatness.

The error amplifier monitors the output of the detector and adjusts the bias in the PIN attenuator in a manner that attempts to maintain the 1st LO signal at a constant level.

Phase Gate Hybrid

The Phase Gate is a frequency mixing device that accepts a high power strobe signal in the 100-150 MHz range and a microwave input signal in the 3-18 GHz range, producing a mixing or beat frequency signal when a multiple of the strobe frequency is near the input frequency.

The 3 dB bandwidth of the Phase Gate is about 1.5 MHz. The output drives a voltage follower buffer in the Strobe Driver circuit.

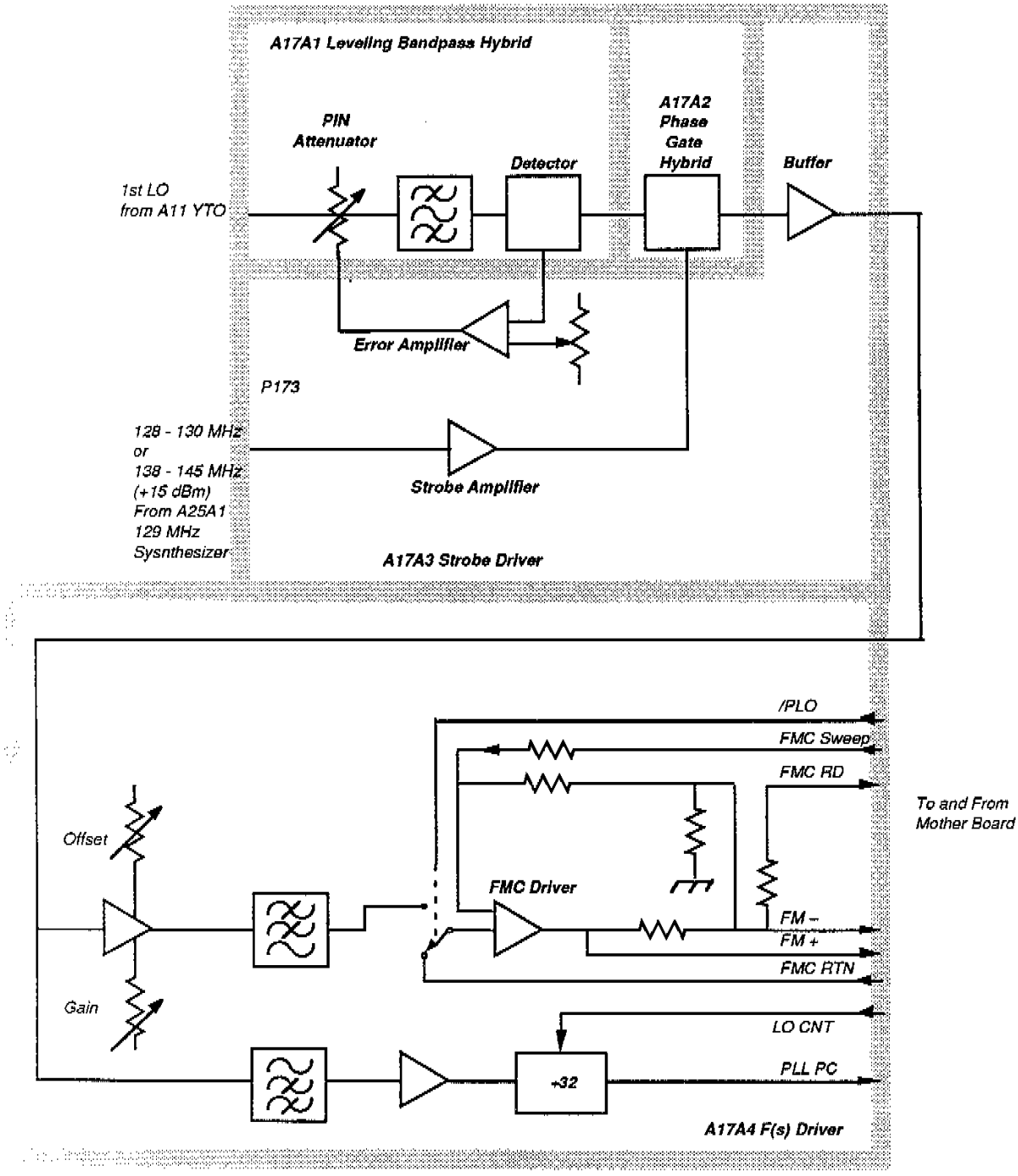


Figure 5-17. Microwave Phase Lock Block Diagram.

Strobe Driver

The Phase Gate voltage follower buffer has high input impedance, low input capacitance, low offset voltage and drift, and low noise characteristics. The 20 MHz small-signal bandwidth allow the higher frequency beat-note from the Phase Gate to be virtually unaffected.

The leveling bandpass error amplifier provides a feedback path around the leveling bandpass hybrid, which allows the 1st LO power applied to the Phase Gate to be adjusted, or leveled. This leveling is accomplished by amplifying the difference between the output of the detector and a thermally compensated (adjustable) reference voltage, and using this signal to control the PIN attenuator. Leveling the signal minimizes variations in loop gain resulting from YIG unflatness.

At low frequencies, variations on the DET line are amplified by the full open loop gain of the error amplifier, thus allowing only a small error signal to exist within the loop. This causes the detector output to closely resemble the reference voltage. The loop corrects for any differences between the detector output and the reference voltage. As the frequency of the error signal increases, the error amplifier gain falls at a rate of 20 dB/decade until it reaches unity above about 150 kHz.

F(S) Driver

The buffered Phase Gate output voltage is filtered, then passed through a variable gain and offset stage. The range of the offset is dependent on the gain setting, and can vary from ±1.2 V (minimum gain) to ±4.1 V (maximum gain). In both cases, it corresponds to about ±100 mV of offset at the input of this stage.

The output of the variable gain and offset stage is passed through a loop filter and FM coil driver. The FM coil driver output goes through the Mother Board to the FM coil on the YTO (A11).

The buffered Phase Gate output also drives a divide-by-32 circuit to provide an output for the Period Counter. The beat note from the buffer is filtered and amplified to provide signal levels to drive the logic circuitry. Then the signal is divided by thirty-two so that it can be sent through the Mother Board to the Period Counter.

LO Module

The LO Control module (A25) controls the center frequency and span width of the 1st Local Oscillator (YIG Tuned Oscillator, A11) and the Preselector (A12FL1).

The module consists of five circuit boards:

- LO Control (A25A2)
- Microwave Control (A25A3)
- 129 MHz Synthesizer (A25A1)
- 129 MHz Oscillator (A25A1A1)
- 500 MHz Mixer (A25A1A2)

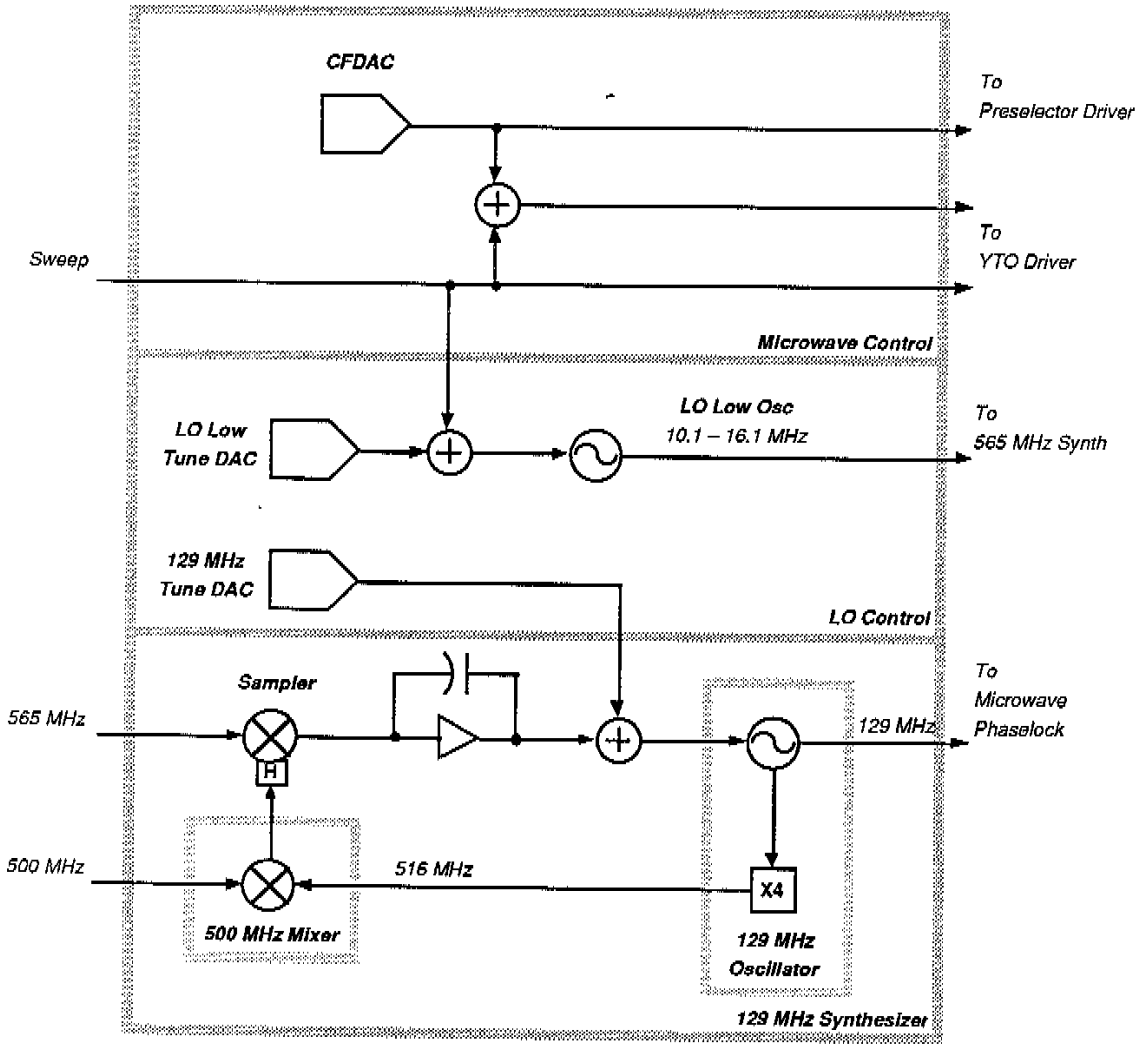


Figure 5-18. LO Module Block Diagram.

LO Control

The LO Control Board (A25A2) contains the LO low oscillator and associated tune DACs for control of this oscillator. In addition, there are tune DACs that supply the tune voltage and feed forward for the 129 MHz Oscillator.

A slave serial interface chip (SIC) controls the DACs and the D flip-flops used to store control signals. The SIC on this board has the hex address DC.

Microwave Control

The Microwave Control board (A25A3) controls the center frequency of the YIG oscillator and the preselector filter. The board also contains the LO module's power supply re-regulation and filtering circuitry. The address of the SIC on this board is B0 (hex).

129 MHz Synthesizer

The 129 MHz Synthesizer (A25A1) contains the majority of the analog circuitry. Two sub-assemblies, the 129 MHz Oscillator and the 500 MHz Mixer, are mounted to the 129 MHz Synthesizer. The YTO (A11) is locked to the 129 MHz oscillator in spans of 2 MHz or less. In general, the synthesizer generates the 129 MHz signal, multiplies it by four, mixes it down, and harmonically mixes this with the 565 MHz synthesizer output to complete the 129 MHz phaselock loop. The circuit is divided into three separate compartments; the 129 MHz oscillator, the mixer, and the sampler compartments.

129 MHz Oscillator

The 129 MHz Oscillator board is mounted on the back side of the 129 MHz Synthesizer board. The oscillator has an LC resonator with a varactor tuning diode. The oscillator output is multiplied by four to produce 516 MHz, and then amplified to +4 dBm output to the 500 MHz mixer.

500 MHz Mixer

The 500 MHz mixer board is located on the backside of the 129 MHz synthesizer board, in its mixer compartment. This board mixes the 516 MHz from the oscillator compartment with the 500 MHz rf input. The 516 MHz input is amplified to +10 dBm and then bandpass filtered before reaching the LO input of the mixer. The 500 MHz input is bandpass filtered and delivered to the rf input of the mixer. The 16 MHz IF output of the mixer drives the sampler board.

Sampler

In the sampler compartment the 16 MHz undergoes some additional low pass filtering and is then amplified to drive a snap diode in the phase gate circuitry. A detector circuit samples the 565 MHz Synthesizer frequency. An error amplifier tunes the 129 MHz oscillator, enabling it to track the appropriate subharmonic of the 565 MHz Synthesizer. Valid harmonic numbers range from 28 to 46.

Period Counter

The Period Counter and 500 MHz Sources assembly (A28) contains two sub-assemblies, the Period Counter (A28A2) and the X5 Multiplier (A28A1). The assembly is replaceable as a single unit. The X5 Multiplier is described with the 3rd Converter circuits.

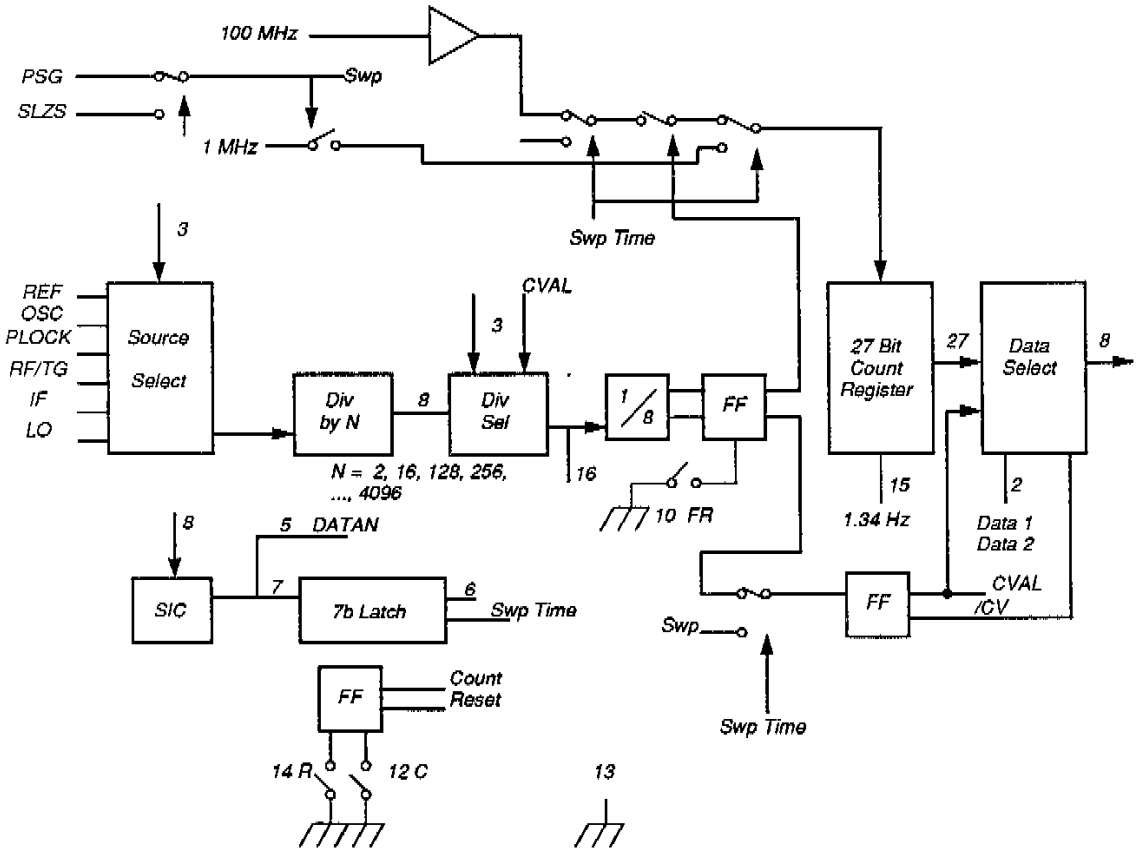


Figure 5-19. Period Counter Block Diagram.

Period Counter

The Period Counter measures various internal frequencies to calibrate the system frequency and display the frequency of applied signals. Period measurement improves speed over other frequency counting methods that might be used. The Period Counter measures internal signals to maintain instrument calibration as follows:

- The 4 MHz crystal filter set in the VR is aligned and measured.
- The swept oscillator can be set for span as well as center frequency.

- Beat notes from the LO phaselock system are counted to determine YTO frequency.

- Sweep speed is also kept in calibration with the period counter by measuring a sweep gate with a 1 μS clock.

The Period Counter returns the binary value of the number of 10 nS clock pulses occurring during a selectable multiple of periods of a selectable input frequency. This reciprocal method offers high measurement speed because 10^7 pulses occur in 0.1 second, which would allow 1 Hz resolution of a 10 MHz signal. The counter register overflows in 2^{27} pulses (=134,217,728 or approximately 1.34 seconds). Resolution can be improved by using this overflow. When sweep duration is measured, the clock pulse is reduced to a 1 μS rate to give usable resolution for each of the three sweep capacitors.

The signal to be measured is selected in an eight-input multiplexer and enabled at the start of a count. The signal goes to a twelve stage binary divider that allows further division according to the resolution required. Outputs of these states are low prior to .the count. The 2^N selector is an eight-input multiplexer. The six outputs from the end states of the divider are in 2:1 steps and the first two are 8:1 steps. The sequential 2:1 steps allow the best compromise between measurement time and resolution. The selected $F_{in}/2^N$ feeds a divide-by-eight circuit, which combines with a flip-flop to form the period count gate. The gated 100 MHz signal feeds the counter register which is a 27-stage binary divider that starts with all outputs low.

At the end of the count gate a flip-flop goes high to indicate count valid (CV). This signal disables the 2^N multiplexer and prevents further functioning of the divide-by-eight. This line is also the twenty-fourth bit connected to the output multiplexer. When the CV line goes low, it enables the I0–4 output lines so they do not pulse while a count is underway. If necessary, the processor can monitor the CV line at I5 to wait until a count is complete.

When a sweep duration measurement is needed, a gated 1 MHz signal is connected to the counter chain by logic switches. The processor must stop and reset the sweep, issue a count signal, then start a single sweep. When the sweep ends, CV goes high and the duration may be read out. This count is also modulus 2^{27} (approximately 134 seconds).

Digital Interface

The eight SIC data lines are divided into seven data lines and one address line (D7). Two four-line data latches are loaded when NBA goes high. These are selected with D7 low. With D7 high D0 controls a D flip-flop to determine Count or Reset. Four other lines operate directly from the SIC. Four dual 4:1 multiplexers are used to return data to the I lines.

Digital Control System

CPU Description

The Main Processor System has three functional sections that are connected by a local bus. This local bus is made available to the processor group bus via the 96-pin edge connector. The three sections are:

- Processor System.
- System Memory.
- Local I/O Locations.

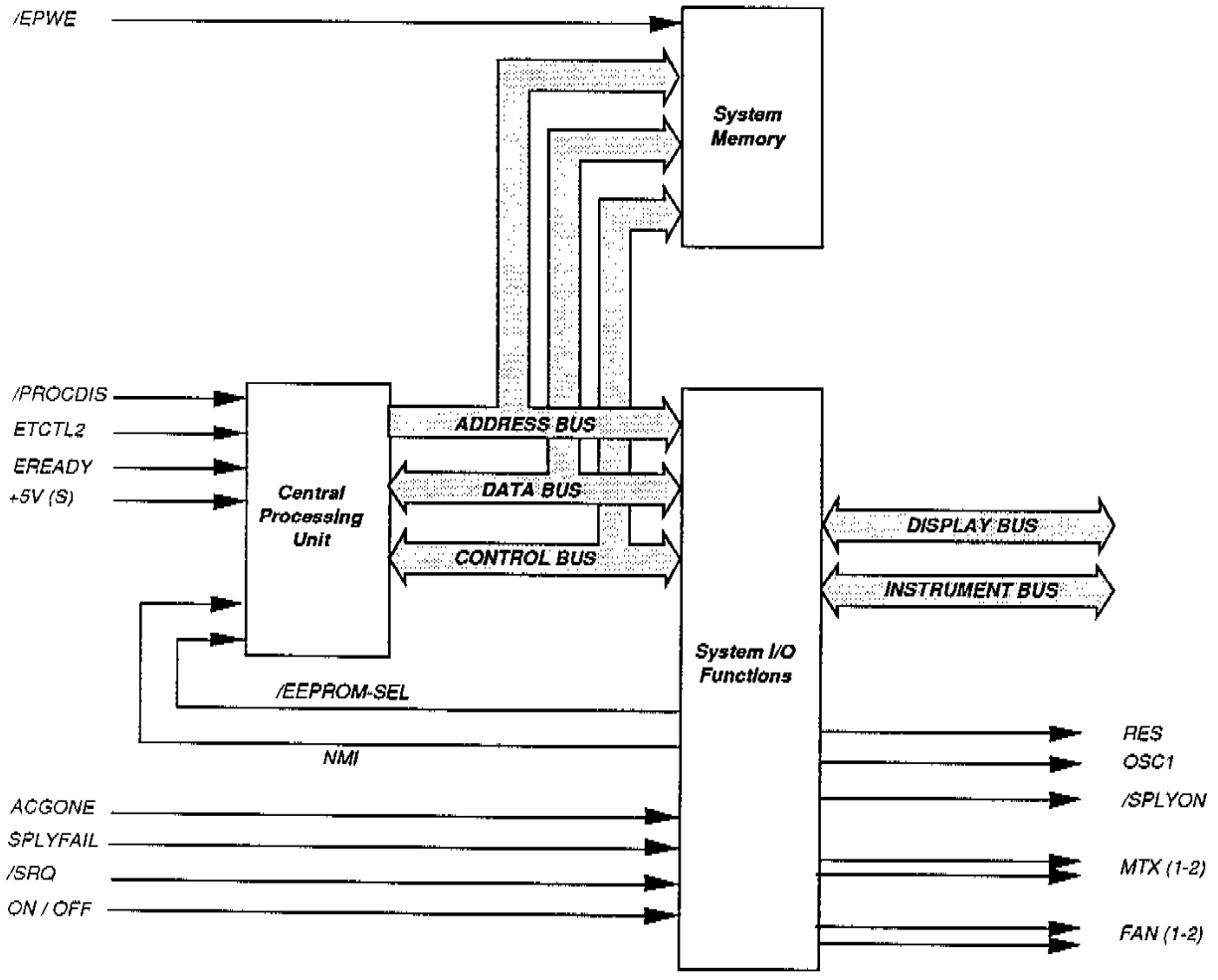


Figure 5-20. CPU System Block Diagram.

The Processor bus is separated from the I/O and Memory bus for several reasons listed below:

1. The processor buffers can be tri-stated, allowing an external programmer to write data directly into the EEPROM's through the edge connector.

2. Testing of the board is facilitated by using an external controller to write and read to memory as well as access the I/O circuitry, all with the resident processor disconnected from the bus. Fast, automated, and comprehensive operational checks may be performed in this manner.

3. To reduce the number of actual loads seen by the other modules that interface with the common external bus.

4. The large memory array is protected from fault conditions that may occur on the external bus.

There are several banks of switches and LED's that are on the Main Processor Board that are used for diagnostic purposes and to control some of the specific hardware functions. Below are a list of the definitions for the switches:

Table 5-1. Control Processor Switch Descriptions

Switch Circuit	Switch Number	Function
S10	A	Enable / disables the bus self test when the Main Processor system boots.
S10	B	Enables / disables the external clock to the clock generator chip.
S10	C	Not used currently.
S10	D	When closed and then opened will cause the processor system to halt and reset as if a power up reset has occurred.
S11	Bit 15	Enables (closed) or disables (open) the advanced diagnostics for the Processor System.
S11	Bit 8 to 14	Defined by the firmware
S12	Bit 0 to 7	Defined by the firmware

NOTE

If S11 bit 15 is closed then there are new definitions for the rest of S11 and S12. Please refer to the section on the "Advanced Diagnostics" for further details.

The Processor System

The Processor System is built around the following functional blocks:

- Clock Generator.
- Main Processor / Math Coprocessor.
- Bus Controller.
- Interrupt Controller.
- Self Test / Control Hardware.
- Timer Controller.
- DMA Controller.
- Wait State Generators.
- Address and Data buffers.
- Control Transfer and Disable Circuit.

Each of these blocks are described according to function, inputs, and outputs in the following sections.

Clock Generator

The clock generator creates the clock signal for the Processor system and synchronizes the processor ready and processor reset signals to the clock. The clock generator can generate a processor clock using a crystal oscillator or by using an external signal supplied from J10.

The source for the processor clock is selected from a switch. When the switch is open the crystal oscillator is used, and when the switch is closed an external oscillator can be used. The external frequency must be between 6 MHz and 21.1122 MHz and be compatible with TTL input levels. The clock frequency is then divided by three to create a processor bus clock frequency of 7.0374 MHz.

The reset signal source is from the power supply control circuit. It is also possible to cause a processor reset by closing and opening the right most switch of S10.

The output of the clock generator is the processor clock, processor ready signal, and system reset signal. The master clock generates "/CLK" which is delayed by a Schmitt trigger inverter. This signal drives one of the latches in the processor transfer circuit. The signal is again delayed by another Schmitt trigger inverter to drive the processor clock out and the timer controller clocks.

Main Processor / Math Coprocessor

The Main Processor and Math Coprocessor work in tandem with each other to form the heart of the processor system. The Main Processor is based on the NEC V30 processor chip. The main function of the Math Coprocessor is to increase the speed of math operations. It talks to the Main Processor by the means of several control lines: /RQ, /AK1, QS0, and QS1. These lines allow the two processors to work together to form a single functional processor block.

The processor block uses a common ready signal, a common clock, and a common reset signal source. The Main Processor also uses two interrupt pins for servicing external hardware. The non-masked interrupt signal, NMI, notifies the Main Processor if the standby supply voltage levels are below the recommended

operating tolerance. The masked interrupt is driven from the interrupt controller. The processor block outputs can be divided into the groups detailed in the following table:

Table 5-2. Main Processor / Math Coprocessor Signals.

Signal Group	Data Direction	Purpose
CPUA16 - CPUA19	Outputs	Create the upper four bits of the actual memory address.
/CPUUBE	Output	Indicates the data word width along with the A0 output to access a 16 bit wide data word.
CPUBS0 - CPUBS2	Output	Indicates the type of instruction cycle being executed.
CPUAD0 - CPUAD15	Bidirectional	Multiplexed address and data lines for the memory and I/O locations.
/BUSLOCK	Output	Prevents other controllers from using the bus during a response to an interrupt vector.

Bus Controller

The bus controller works with the processor block to generate the necessary timing signals for reading and writing data to either memory or I/O locations. There are also control lines, signals "PAEN" and "/PAEN", that prevent the output of the timing signals during direct memory access (DMA) transfers. The output signals are synchronized with the system clock. There are several outputs that control many different functions for these signals. The following table describes the output signals:

Table 5-3. Bus Controller Outputs.

Signal Names	Function
/CPUMRD	Provides read strobe for all memory locations.
/CPUMWR	Provides write strobe for all memory locations.
/CPUIORD	Provides read strobe for all I/O locations.
/CPUIOWR	Provides write strobe for all I/O locations.
/INTA	Provides a strobe to the interrupt controller to send the address of the interrupt during an interrupt acknowledge cycle.
DT/R	Provides a signal to determine the direction of the data to the processor block.
88DEN	Provides a signal to enable the data bus for data to and from the processor block.
CPUALE	Provides a strobe to latch the address from the processor block.

Interrupt Controller

The interrupt controller expands the single masked interrupt input to the Main Processor. The interrupt controller must be programmed and is part of the local I/O. The data bus is connected directly to the Main Processor bus for access during interrupt handling routines. The address line and the read write lines are

buffered from the DMA I/O buffers. The chip select line is decoded in the local I/O map to address the internal control registers. The Main Processor can access the interrupt information when the bus controller asserts "/INTA" and the Main Processor reads the data from the interrupt controller. The actual interrupt signal inputs come from other components in the system. There are two interrupt signals that come from the processor system, all other interrupts are external to the processor system. The following table shows each interrupt and the driving source.

Table 5-4 . Interrupt Vector Sources.

Interrupt Vector	Source
#0	Timer Controller output of timer 0.
#1	DMA Terminal Count output.
#2	Display Bus Controller.
#3	GPIB Port 0 Controller.
#4	GPIB Port 1 Controller or RS-232 Controller.
#5	Instrument Bus Controller.
#6	SRQ request for service by either Display Bus Controller or Instrument Bus Controller.
#7	Power supply "ON/OFF" request from the front panel.

Self Test / Control Hardware

The self test hardware is made up of pull up resistors and a dual diode. In normal operation the switch, S10 position 1, is open and the pull up resistors have little or no effect on the data bus. If the switch is closed two of the data bits are held at a logic low by the diode. When the processor system is reset the Main Processor begins a looping process that tests the lower address lines only. There are no actual data transfers that occur during this time. This mode of operation continues until the switch is opened again and the processor system is reset.

Timer Controller

The timer controller has three internal sixteen bit counters that can be programmed in any one of six different modes of operation. The firmware can change the mode of operation as needed to perform the necessary timing functions.

At this time, timer 1, creates a timesharing clock for the operating system. Timer 2 has no delegated functions. The third counter, timer 3, is set up for future hardware requirements. All three counters use the buffered clock, "BCLK".

The programming of the timer controller is part of the local I/O on the Main Processor Board. The data bus is buffered by the same buffers as the DMA controller, along with the address and control lines.

DMA Controller
The DMA (Direct Memory Access) controller transfers data between memory locations and peripheral I/O locations. Before a DMA transfer can begin, the DMA controller waits for a request from one of the I/O peripherals and for the main processor to complete the present bus cycle. Once the DMA controller starts the transfer, it will take control of the external bus and assert the proper address and control strobes as necessary to complete the transfer from memory to the I/O location. When the transfer is completed, the DMA controller issues an interrupt. The DMA controller does not use the data bus except during the programming mode of operation. All DMA transfers are done by transferring on the data bus without storing the data in a register.

The DMA requests are buffered before reaching the DMA controller. The DMA acknowledge is also buffered before leaving the DMA controller.

Wait State Generators
There are two wait state generators for the main processor system, one for the main processor controller and one for the DMA controller. This is required due to the different timing relationships between the two controllers. There are also provisions for external hardware to control the number of wait states inserted, but these are not used at this time.

The Main Processor wait state generator must select the number of wait states for different memory and I/O addresses. The memory components require one wait state, most I/O locations require two wait states, and the EEPROM requires three wait states.

The Main Processor wait state generator is clocked by the master clock and controlled by the processor transfer circuit. Under normal operation the wait state generator starts counting the clock cycles after an instruction starts. Then it selects the correct delay for the function being done and causes the clock generator to create a wait state for the correct number of cycles.

The DMA wait state generator uses the delay clock, "/CLK" for clocking a counter. DMA transfers only require that two wait states be inserted.

Address and Data Buffers
The address and data buffers are used to combine the normal operation of the main processor system and the DMA controller. They also control the data to and from the local I/O devices that make up the processor system.

The address buffers / latches and data buffers for the main processor are only active when the main processor or the math coprocessor are controlling the bus. Part of the address buffers for the DMA Controller are bidirectional to allow programming of the DMA control and to allow a control signal for reading and writing.

Some of the DMA address lines are not latched, but are buffered to allow 64 Kbyte transfer to and from memory. The data buffers for the DMA controller are active only when programming the DMA controller or the timer controller.

The data buffers for the Main Processor are active during any control by the main processor system except during DMA transfers and during interrupt acknowledge cycles.

Control Transfer and Disable Circuit
The control transfer circuit allows the transfer of control without causing bus contention. The DMA controller requests the use of the external bus by asserting the signal "HOLD". The DMA controller then waits until a "HOLDACK" is returned before controlling the external bus.

A single clock cycle is required from the time that the hold request is asserted, the main processor finishes the bus cycle, until the hold acknowledge is returned to the DMA controller. When this change is done, the main processor is put into a wait state and all processor address and data buffers become tri-stated. After the DMA controller has completed its transactions the Main Processor is given control again after one bus cycle is complete.

Another input to this circuit is the "/PROCDIS". This signal will put the Main Processor into a wait state mode, and the DMA controller will not be granted any requests. This will allow an external processor system to share the current RAM storage in either I/O space or Memory.

System Memory

The system memory and some of the local I/O share the same address and data buffers. This is done to reduce the number of CMOS loads that are on the external processor bus. These data buffers and control circuits, and other gates are common to both the System Memory and the local I/O locations. The Memory board also has address and data buffers that protect the devices that reside there, but are part of the system memory. Since both system isolations work the same, only one will be covered. The data buffers are turned on and off as needed to access the memory and I/O locations on these boards.

The EPROM's are write-protected during normal operation. They can be write-enabled for on-board programming by "/EPWE", the EEPROM Write Enable signal. This is done only at authorized centers for firmware updates.

Memory Map
The system memory is made up of both RAM and EPROM's. Some of the parts reside on the Main Processor Board (A41). The remaining parts reside on the Memory board (A43) and form a direct extension of the system memory. The processor system requires the entire 1 MByte, or 512 KWords, of addressed space that the processor can address. Below is a map showing the current partitions of the system memory.

Table 5-5. Memory Map.

Type	Location	ID Numbers	Size	Segment
RAM	Main Processor	U60, U39	32 KWord	0
RAM	Main Processor	U29, U49	32 KWord	1
RAM	Memory Board	U16, U20	32 KWord	2
RAM	Memory Board	U15, U19	32 KWord	3
EPROM	Memory Board	U11	64 KWord	4, 5
EPROM	Memory Board	U12	64 KWord	6, 7
EPROM	Memory Board	U13	64 KWord	8, 9
EPROM	Memory Board	U14	64 KWord	A, B
EPROM	Memory Board	U10	64 KWord	C, D
EPROM	Main Processor	U63	64 KWord	E, F

Programming of EPROMs

Both the Main Processor Board and the Memory board have provisions for programming the EEPROM's while they are on the board. This is only done by authorized centers for firmware upgrades.

All power supplies, VC, VCC, and VPP, have separate power supply pins, which on the Mother Board are connected to +5V standby. Each board has a signal, "/EPWE", that allows reading and writing to each EEPROM location, but not during normal operation. The Main Processor also has a signal, "/PROCDIS", that disables the processor system from controlling the bus.

Local I/O Locations

The local I/O is located only on the Main Processor board. The local I/O can be divided into two groups, one group is for the processor system internal functions, and the other group is system I/O. A map of the I/O that is present on the Main Processor Board follows.

Table 5-6. Local I/O MAP.

Function	I/O Address or Range of Addresses (Hex)
DMA Controller	0000 to 000F
Interrupt Controller	0010 to 0012
Timer Controller	0020 to 0026
Power Controller	0040
Diagnostic Controller	0060

The decoding for all local I/O is done by cascaded decoders. These are also qualified by the gate matrix to decode absolute I/O locations in the I/O map.

Processor I/O
The local I/O for the processor is made up of the three function blocks that are part of the processor system; the DMA, Interrupt, and the Timer controllers. Each of these controllers have unique addresses for internal registers that control there various functions. The following sections deal with the circuits used to program these devices.

DMA Programming Control
The DMA programming is done using the address and data buffers that are used by the DMA controller. The chip select for the DMA controller is used to enable the data, address, and control buffers.

Timer Programming Control
The Timer programming is done using the same address and data buffers as in the DMA controller. The only valid address for the timer controller are on even boundaries, so the chip select is qualified with address line 0, "BA0".

Interrupt Programming Control
The Interrupt programming is done using the internal processor system bus, which is done to allow the processor access to the interrupt controller when responding to an interrupt vector call. The only valid address for the interrupt controller are on even boundaries so the chip select is qualified with address line 0, "BA0".

System I/O
The remaining I/O is for two functions, Diagnostics and Power control. These functions are located here to increase testability of the Main Processor board, and due to hardware limitations.

Diagnostic Aids
The diagnostic aids consist of sixteen switches and sixteen LED's, both are one word wide. The switches and the LED's are at the same I/O location to write data to the LED's and read data from the switches. The LED's require a logic high, written to the corresponding bit location, to be turned on. The switches will return a logic high when open and a logic low when closed.

Power Supply Control
The power supply control block is made up of four different blocks:

- Fan speed control
- MTX voltage control
- Power supply on/off control
- AC power supply monitor control

Each of these functions are controlled by controlling the bits and reading the byte at the power supply control I/O location. Each function controls part of the processor control of the power supply and related functions.

The fan speed control consists of the lower two bits, 0 and 1. Changing the bit pattern changes the fan speed from off to one of three speeds.

Bits 2 and 3 are the MTX voltage control. They control the voltage supplied to the MTX.

Bit 4 is the power supply on/off control. This is used to allow the processor to turn the power supply outputs on or off as the user presses the front panel power button.

There is also a status line from the power supply board that indicates a power supply has failed due improper voltage.

The AC power supply monitor is used to monitor if the AC power source is removed. If so, a non-maskable interrupt is presented to the processor system, if the hardware is enabled. The AC power supply monitor will also monitor the +5 V standby voltage and reset the processor after the power supply reaches 4.5 V or higher for at least 375 mS.

I / O Interface

The IO Interface contains most of the remaining IO locations for the Processor System. There are two basic groups of IO located on the board; a silicon disk drive for data storage, and the remaining IO for internal and external interfaces. The following table shows the functional blocks:.

1. Complete IO decoding map for Processor System.
2. Silicon Disk
    a. Disk Address Generator / Latch.
    b. Disk Selection.
    c. Disk Address, Data and Control Buffers.
    d. Disk Control and Status Buffer.
    e. EPROM.
    f. EEPROM.
    g. NVRAM.
3. IO Access
    a. Peripheral Data Switch.
    b. Peripheral Switch and Latch / Buffer.
    c. Real Time Clock.
    d. Instrument Control Bus.
    e. Display Control Bus.
    f. Communications Interface Port.

The following shows all IO locations, on the Main Processor board, on the IO Interface board, on the Comm. Interface board, and on the Processor Extender board. This map is complete and includes all other maps.

Table 5-7. Decoding Map.

Circuit Board	IO Address	Description
Main Processor	0000 to 000F	DMA Controller registers.
Main Processor	0010 to 0012	Interrupt Controller registers.
Main Processor	0020 to 0025	Timer Controller registers.
Main Processor	0040	Power Control register.
Main Processor	0060	Diagnostic register.
Comm. Interface	0080 to 008F	GPIB port 0 control registers.
Comm. Interface	0090 to 009F	GPIB port 1 or RS-232 control registers.
Comm. Interface	00A0	Thermometer registers.
Comm. Interface	00B0	Comm. Interface control and status register.
IO Interface	00C0 to 00C7	Display Bus Controller.
IO Interface	00C8 to 00CF	Instrument Bus Controller.
IO Interface	00D0	Disk control and status register.
IO Interface	00D4	Disk address and status register.
IO Interface	00D8	Diagnostic switches.
IO Interface	00D9	Diagnostic latch and status buffer, and bit 0 controls the YTO power supply voltage, logic low is for 18V and logic high is for 26V.
IO Interface	00E0 to 00FF	Real Time Clock.
Proc. Extender	0100 to 010F	Service RS-232 interface.

The address locations are unique to help prevent any possible conflicts with other IO locations, or additional IO locations that may be on future boards.

The address range of 0110 to 1FFF is reserved for future peripherals within the IO space.

The address range of 2000 to DFFF is the address range of the silicon disk for read and write operations. The following table shows the address for each drive of the silicon disk. Note that all addresses are not used at this time.

Table 5-8. Silicon Disk Drives.

Drive	Address Range	Storage Type	Status
0	2000 to 3FFF	EPROM	Used
1	4000 to 5FFF	EPROM	Not Used
2	6000 to 7FFF	EEPROM	Used
3	8000 to 9FFF	EEPROM	Not Used
4	A000 to BFFF	NVRAM	Used
5	C000 to DFFF	NVRAM	Not Used

The address range of E000 to FFFF is reserved for future expansion of IO operations.

Silicon Disk

The silicon disk is an IO addressable group of memory blocks organized similar to that of a conventional disk drive. The disk is composed of EPROM, EEPROM, and NVRAM. It is partitioned into the logical equivalents of disk drives, sectors, and tracks. Its organization arises from the derivation of the lower eight bits of its address bus. These addresses are generated by an IO port referred to as the address generator / latch. This effectively increases the IO address space by a factor of 256, allowing over 16 MBytes of possible storage. The maximum IO address range of the microprocessor is only 64 K and substantially more storage was required for the intended applications. Addresses above A7 are decoded to provide the tracks, sectors and 8 512 KByte "drives". Not all of the upper addresses are currently used. The first "drive" is used for conventional IO (0000 to 1FFF). The last "drive" is reserved for future expansion (E000 to FFFF).

Note that in the following discussions, disk and IO addresses will be distinguished by a different prefix since the buffered microprocessor address lines have different binary weights on the silicon disk due to the generated lower 8 disk address lines. The silicon disk is located on a separate data bus from the peripheral data bus. The silicon disk provides long term storage of the instrument settings, waveforms, configuration information, calibration information, and text for the menu driven display interface. The silicon disk has write protection and may be enabled or disabled under software control. It also has provisions for protecting against data loss due to power interruption. All data, address, and control lines are buffered to the memory on the silicon disk through tri-state buffers. This allows for implementation of the disk enable feature and allows the isolation of the memory from the buses during the standby mode. In the standby mode of operation part of the silicon disk, the EEPROM devices are powered down. The rest of the silicon disk, the EPROM and NVRAM, can remain active during the standby mode of operation.

Disk Address Generator/Latch

The silicon disk is an IO addressable group of memory blocks organized similar to that of a conventional disk drive. The disk is composed of EPROM, EEPROM, and NVRAM. It is partitioned into the logical equivalents of disk drives, sectors, and tracks. Its organization arises from the derivation of the lower 8 bits of its address bus. These addresses are generated by an IO port referred to as the address generator / latch. This effectively increases the IO address space by a factor of 256, allowing over 16 MBytes of possible storage. The maximum IO address range of the microprocessor is only 64 K and substantially more storage was required for the intended applications. Addresses above A7 are decoded to provide the tracks, sectors and 8 512 KByte "drives". Not all of the upper addresses are currently used. The first "drive" is used for conventional IO (0000 to 1FFF). The last "drive" is reserved for future expansion (E000 to FFFF).

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has provisions for protecting against data loss due to power interruption. All data, address, and control lines are buffered to the memory on the silicon disk through tri-state buffers. This allows for implementation of the disk enable feature and allows the isolation of the memory from the buses during the standby mode. In the standby mode of operation part of the silicon disk, the EEPROM devices are powered down. The rest of the silicon disk, the EPROM and NVRAM, can remain active during the standby mode of operation.

Disk Decoding

The decoding for the silicon disk is done with cascaded decoder chips. The decoding for the EEPROM and EPROM uses the same decoder and then uses a buffer chip to select between the two drives. The decoding for the NVRAM is done with a battery backup / decoding chip. This provides the necessary decoding for the NVRAM and also prohibits access while the standby voltage is removed.

Disk Address, Data, and Control Buffering

The disk address and control buffers are made up of two groups of buffer chips. One set of buffer chips, U541, U540, and U521, is used to control the address and control lines to the EEPROM chips. The second set of buffer chips, U31, U25, and U528, is used to control the address and control lines to the EPROM and NVRAM chips. They are enabled by their own disk enable signals.

The disk data buffers are also made up of two banks of buffer chips, one bank of U542 and U34 for the EPROM and NVRAM, and the other bank of U534 and U529 for the EEPROM. The buffers are enabled by the chip selects, for the silicon disk drives, and the disk enable lines. Note that there are provisions for on board programming of the EPROM's.

Disk Control

The disk control block uses an eight bit latch to control the access to the silicon disk, which is located at IO address 00D0. There is also a feedback register for monitoring some of the bits necessary for disk control. Below is a map to define the write bits.

Table 5-9. Disk Control Table.

Bit	Cycle	Function
0	WRITE	Write protection of the entire silicon disk, active logic low.
1	WRITE	Enable for the EPROM and NVRAM silicon disks, active logic high.
2	WRITE	Auto increment enable, logic low, for disable, logic high for enable.
3	WRITE	Instrument and Display bus reset control.
4	WRITE	Enable for the EEPROM silicon disks.
5	WRITE	Not defined.
6	WRITE	Real time clock test control.
7	WRITE	Real time clock stop control.
0	READ	Write protection status bit.
1	READ	Enable status for EPROM and NVRAM silicon disks.
2	READ	Auto increment status bit.
3	READ	Instrument and Display bus reset status.
4	READ	Real time clock alarm status bit.
5	READ	Interrupt 6 status bit.
6	READ	Interrupt 7 status bit.
7	READ	Enable status for EEPROM silicon disks.

Disk enable bits 1 and 7 control the access to the silicon disk. Bit 1 controls the access to the NVRAM and the EPROM, while bit 7 controls the access to the EEPROM. If both of the silicon disks are disabled then access to the silicon disk is prohibited. This will allow independent control of the silicon disk depending on if the +5V digital voltage is on or not, as well as disable access to the rest of the silicon disk when necessary.

The write protect bit is used to control the write access to the silicon disk. This line is used to inhibit the "/EIOWR" line signal from the processor system.

The auto increment bit is used to control if the "disk address latch / generator" will automatically increment with each word access or remain the same for EPROM programming.

NOTE

All drives have 2 MByte capacity but may be only partially filled and decoded, yielding "phantom" address ranges.

EPROM - DRIVE 0

This drive contains 4 X 64 KWords of erasable EPROM, 64 KWords in each 40 pin dip package. The devices are the same as those used on the Main Processor board and the Memory board. Timing analysis indicates 2 required wait states due to the further buffering of the select lines from the address decoding section. Logic is provided to prevent writing to these devices except when being programmed from an outside source. This is not to be confused with the disk write protect function.

EEPROM - DRIVE 2

This drive consists of four EEPROM's of 32 KBytes each. These low power devices provide long term storage of instrument calibration factors and configuration data. They function the same as SRAM from a standard +5 volts but maintain data throughout power loss. The write cycle time is on the order of 10 mS during which the processor may poll the EEPROM's by reading the last byte written to the device. If the internal program cycle is unfinished, the data read will be the complement of that written. The data will revert to its true state upon completion of the internal& programming cycle.

NVRAM - DRIVE 4

This drive consists of eight, 8 KByte, low power CMOS rams. This memory provides faster access than the EEPROM and may contain such information as instrument presets, and user storage information. Provision have been made for next generation of denser parts if required. A non volatile controller / decoder, U50, provides battery backed protection against data loss during the time that standby voltages are not present. This device supplies VCC to the RAM's either from the +5V standby or either of two Lithium battery cells. An internal comparator senses which voltage is higher, battery or +5V standby and automatically switches between the two. This controller / decoder also inhibits the chip selects in the event that the +5V standby falls below 4.5 volts. Write protection is delayed however in the event that a write is currently taking place, avoiding corruption of data. During processor reset, the silicon disk is deselected, further protecting against data loss.

The NVRAM can be operated in two different modes of operation, normal and secure. In the normal mode, J10 must be installed between points 1 and 2. This allows the NVRAM to be protected during the times that the ac line voltage is not present at the instrument. The secure mode of operation has J10 between pins 2 and 3. This erases the entire contents of NVRAM each time the ac line voltage is removed from the instrument. Several error messages will show that the data has been lost. This mode is used to ensure that sensitive data is not available in the instrument.

IO

The remaining IO locations are referenced as byte wide devices and not word wide devices like the silicon disk storage locations. To program or access these devices, for normal operations and for DMA transfers, a data switch method has been implemented. The address decoding has been described before as to the actual IO address. Within each address range may be additional IO address for controlling internal registers of the different IO functions.

Peripheral Data Switch

The peripheral data switch, or PDS, provides for bidirectional data transfer between the processor memory and byte wide IO devices. This switch also selects the data direction based on the type of transfer being performed, processor controlled or DMA. The switch itself consists of two 74HCT234 bidirectional buffers, U26 and U33, whose direction is controlled by the DMA acknowledge lines and the processor BS1, read or write. The processor side buffer IO lines are connected to D0 - D15. The peripheral bus IO lines are

connected together so that the 16 bit uPD70116, V30, data bus is effectively multiplexed to the peripheral data bus. There are several signals, from the processor, that are used to determine which, if any, buffer is active. At no time are both buffers enabled simultaneously. All IO devices on the peripheral data bus have 8 bit data ports. This includes the GPIB ports on the Comm. Interface board. These IO ports have been located on even address boundaries. During processor IO operations the PDS functions as a data buffer in the following ways:

Table 5-10. Peripheral Data Bus Transfers.

Processor IO Operation	Peripheral Data Bus
Byte, even boundary	Byte transfer
Byte, odd boundary	Byte transfer
Word, even boundary	Low byte transfer
Word, odd boundary	High byte followed by low. (Two cycle operation.)

This scheme allows data transfers to take place between the word organized 16 bit processor and the byte wide peripherals without tying up the processor in data formatted steps to get the data from the upper data bus to the lower data bus. During DMA transfers "BBS1" and the exclusive OR of any of the DMA acknowledge signals are used to determine the data direction on the PDS bus. DMA transfers from a peripheral to memory is presented to the bus as a memory write. DMA transfers from memory to a peripheral is presented to the bus as a memory read. Since BS1 indicates whether a read or write is taking place, it must be inverted to control the peripheral's buffer direction during DMA transfers.

Peripheral Switch and Latch / Buffer

There is an option switch that can be read by the Control Processor, locate on the IO Interface board, at IO address 00D8. This switch is defined by firmware. There is also a latch, at IO address 00D9, that is used to verify the upper byte of the PDS. This latch also use bit 0 to control the signal "OSC1".

Real Time Clock

The real time clock consists of a single chip clock, U23, which has long access times. Special sequence for writing or reading data from the chip. To help in developing the user interface for the chip, U539 and U28 have been added to help sequence the operation of read and write sequences. By latching different data, in U539 and U525, it is possible to control all of the control lines and the address and data lines. Please refer to the technical reference for the 58321 for programming details.

Instrument Bus Controller

A master bus IC, U27, is used to interface with the instrument control bus. There are active pull ups for the SDA and SCL lines, these pull ups insure data transitions on the control bus lines which connect through the motherboard to most of the instrument modules.

Display Bus Controller
This is the interface between the IO Interface module and the Communications Interface which contains the GPIB ports, a thermometer, RS-232, and serial control bus ports. It consists of bidirectional and unidirectional buffers which buffer bus data, address, and control signals to the Comm. Interface board. These buffers are active only when the IO addresses corresponding to the Comm. Interface are accessed or during a A master bus IC, U41, is used to interface with the display control bus. There are active pull ups for the DSDA and DCL lines, these pull ups insure data transitions on the control bus lines which connect through the motherboard to the Digital Storage board, and Video Processor board.

Bus Pull Ups
The active pull ups used on the Display Bus and the Instrument bus are implemented using current mirrors. The reference current for the active pull ups is established by the action of R529, R528, and Q512. These values were picked so that the collector current of Q512 is 5 mA. This in turn sets the reference current for the active pull ups, Q511, Q510, Q513, and Q514. There is a 10 ohm resistor connected between the power supply and each of the emitters to reduce the effect of the transistor gain variations.

Communications Interface Port
This is the interface between the IO Interface module and the Communications Interface which contains the GPIB ports, a thermometer, RS-232, and serial control bus ports. It consists of bidirectional and unidirectional buffers which buffer bus data, address, and control signals to the Comm. Interface board. These buffers are active only when the IO addresses corresponding to the Comm. Interface are accessed or during a response to a DMA cycle. This keeps the mother board runs and cable to the Comm. Interface quiet except during use, minimizing EMI.

Communications Interface

The Communications Interface (A5A6) is part of the processor system, and is part of the IO for the processor system. The following functions are supported by the Communications Interface board:

- Processor Interface.
- GPIB Port 0 and GPIB Port 1.
- Thermometer.
- Interface Control / Status.
- External Serial Bus Interface.
- Interface Analog Input and Outputs.

This board is mounted in the Power Supply casting and is then cabled to the Mother board by two forty-conductor cables.

Processor Interface.

The Communications Interface is an extension of the IO Interface (A42), which supplies address lines, data lines, and control lines to the Communications Interface. The data, address, and most of the control lines are buffered between the Communications Interface and the IO Interface. Some of the control lines, DMA acknowledge, DMA request, and interrupt request lines are not buffered . The DMA acknowledge lines, "/BDMAAK1" and "/BDMAAK2", and the Communications Interface select, "/COMSEL", are used to enable the data buffers. The DMA acknowledge lines also prevent any of the peripherals from being selected during a DMA transfer cycle. The remaining peripheral selects are done by decoding the addresses, "CLA5" and "CLA4". The following table shows the IO addresses that are on the Communications Interface board.

Table 5-11. Communications Interface IO Addresses.

Addresses	Function
0080H to 008FH	GPIB port 0 control registers.
0090H to 009FH	GPIB port 1 control registers.
00A0H	Thermometer register.
00B0H	Communications Interface control and status register.

GPIB Port 0 and GPIB Port 1

Both GPIB ports are identical, with the exceptions listed in the table.

Table 5-12. GPIB Differences.

Reference	GPIB Port 0	GPIB Port 1
DMA acknowledge signal	"/BDMAAK1"	"/BDMAAK2"
DMA request signal	"/BDMARQ1"	"/BDMARQ2"
Interrupt request signal	"/EINTP3"	"/EINTP4"
Base IO address (Hex)	0080	0090

The 4.9 MHz clock is buffered before going to the GPIB controller chips. The GPIB controller chip is reset to a known state each time the processor system resets. This allows the GPIB controller to be initialized to a known state on power up. The strobe, from the GPIB controller, that controls the read cycle is exclusive OR'ed with the DMA acknowledge signal. This allows the processor system to do DMA transfers on the data bus without storing the data in a register. The write signal is applied directly to the GPIB controller. The DMA request and acknowledge signals are used during the DMA data transfers only. The address lines are used to select the internal registers to be accessed. The chip select completes the chip enable for the programming of the GPIB controller. The interrupt pin is used to request service by the processor system. The data lines provide the remaining processor interface.

The GPIB bus interface contains two linear transceiver chips. One is used to buffer the IEEE-488 data lines. Provisions have been made to allow selection of

either push / pull outputs or open collector outputs. The other is used in buffering the management lines from the IEEE-488 bus.

Thermometer.

The thermometer is made up of three basic components, an A/D converter, a voltage reference, and a temperature transducer. The A/D converter has a built-in bus interface located in the IO address space at 00A0. The conversion process requires a write of any data followed by a 10 µS delay for the conversion. The conversion process can be monitored by the processor system by reading the status latch, detailed later. The binary data can then be read from the A/D converter. A 2.5 V reference is applied to a resistor divider network, which is then applied to the negative input of the A/D. The temperature transducer provides a current between 248 µA to 378 µA, scaled dependent on the exhaust temperature, and provides the positive input to the A/D converter.

Interface Control Status.

The interface control is made up of a write function and a read function. The write function sets the various control bits, and the read function returns the current status. The bits for this address are defined in the following table.

Table 5-13. Control / Status Bit Definitions .

Bit	Signal Name	Cycle	Function
0	SCON0	WRITE	If GPIB port 0 is a system controller, active high.
1	SCON1	WRITE	If GPIB port 1 is a system controller, active high.
2	/PORTEN0	WRITE	Enable for the external Serial Bus interface, active low.
3	STAT0	WRITE	Status line to be defined by the external Serial Bus interface.
4	STAT1	WRITE	Status line to be defined by the external Serial Bus interface.
5		WRITE	Not defined.
6		WRITE	Not defined.
7		WRITE	Not defined.
0	SCON0	READ	System controller enable of GPIB port 0.
1	SCNO1	READ	System controller enable of GPIB port 1.
2	/PORTEN0	READ	External Serial Bus enable line.
3	STAT0	READ	Control line to the external Serial Bus.
4	STAT1	READ	Control line to the external Serial Bus.
5	DATDIR	READ	Direction for the external serial bus, logic high the data goes to the serial bus and logic low the data is from the serial bus.
6	TCONV	READ	Conversion process for the thermometer, logic high when conversion is complete.
7	/PORTEN1	READ	External Serial Bus, logic low external serial bus in use, logic high no external serial bus.

External Serial Bus Interface.

The external Serial Bus interface has a processor controlled enable line, and an external enable line. This allows the processor to control the interface as well as determining when an external Serial Bus is present. When the external Serial Bus interface is disabled, all signals at the connector become tri-stated.

The reset signal and the service request signal are read by the Main Processor to provide external control of the Serial Bus. The reset signal and the clock line are buffered and then sent to the external Serial Bus. The service request line is a buffered input from the Serial Bus. Its purpose is to request service by the Main Processor system.

The data line is bidirectional, allowing data to flow both to and from the external Serial Bus. Note that the external Serial Bus must control the direction that the data is to be transferred.

Interface Analog Input and Outputs.

The Communications Interface board also routes many of the analog signals from the Motherboard to the rear panel. These signals do not control any functions on the Communications Interface but are routed to several of the connectors on the rear panel.

CPU Extender

The Processor Extender board is part of the optional Service Kit. The board provides a means of extending any of the processor system boards and providing access to the signals that interface the system board with the Mother board. There are jumpers on each signal line to allow attaching of a logic analyzer or scope probe. This also provides a means of isolating any signals by removing a jumpers from the extender board. There are also test points for the power supply voltages and for ground references.

The Processor Extender board also has a secondary function to provide a tool for instrument fault isolation, instrument calibration, and assistance with the advanced diagnostics of the processor system. The following chart shows each of these functions

1. RS-232 Interface.
    a. Address and Control Buffers.
    b. Data Buffer and Control Logic.
    c. Address Decoding and Control.
    d. RS-232 Interface and Buffer.
2. Advanced Diagnostic Features.
    a. Power Control LED's.
    b. Internal Serial Bus Test Hardware.
    c. Optional Comm. Interface Ports.

It should be noted that there are provisions on the extender board for some functions that may be used by manufacturing or factory service; these will be covered in the circuit description.

RS-232 Interface

The RS-232 Interface is used to control the instrument during the calibration sequence and to help in fault isolation. The usage of the RS-232 interface will be documented by the firmware group.

Address and Control Buffers
All of the address lines, "LA0" to "LA15", and control lines, "LBS1", "LBS2", "/IORD", "/IOWR", and "ERESOUT", are buffered from the edge connector. This allows only one active load to be presented to the processor system by the RS-232 interface.

Data Buffer and Control Logic
The data buffer is enabled by the address decoding and by "/ATEST". "/ATEST" is used disable the RS-232 interface data bus during the self test mode of operation by the Main Processor board. The direction that the data will travel is determined by "BBS1" bus status. Note that only eight of the data lines from the processor system are used in controlling the RS-232 Interface.

Address Decoding and Control
The decoding is done by cascaded decoders, and is qualified by logic gates to ensure an absolute address decoding. There is a jumper, J30, that can be used to disable the RS-232 interface.

RS-232 Interface and Buffer
The RS-232 interface is based on a Zilog 85C30 Communications Controller chip. The control lines for IO read and write operations are qualified by the processor reset signal. A clock generator chip, Y10, is used to provide the 4.9 MHz clock signal required for the RS-232 interface. The Communications controller has two interfaces built into the device, but only one half of the chip is used.

The communications controller outputs and inputs are then passed to a buffer chip that converts between the RS-232 signal levels to TTL signal levels. The output connector, a 9 pin "D" connector has the same pin out as the RS-232 ports on AT style personal computers. The interrupt signal from the RS-232 Interface is inverted and then sent to the desired interrupt signal, 3 or 4, by selecting one of the positions of J40. Note that the interrupt selected may need to be disabled on the IO Interface board or on the Processor Extender board to prevent contention of the signals.

Below is a chart showing all of the possible combinations of boards on the extender, and how the jumpers need to be set to use the RS-232 interface on the Processor Extender board.

Table 5-14. RS-232 Jumper Configurations.

Boards Extended	Board with Jumper	Jumper to Remove	Interrupt Selected
Main Processor	IO Interface	J13	3
Main Processor	IO Interface	J12	4
Main Processor	Processor Ext.	A 24	3
Main Processor	Processor Ext.	B 24	4
IO Interface IO Interface		J13	3
IO Interface IO Interface		J12	4
IO Interface			
Main Processor	IO Interface	J13	3
IO Interface			
Main Processor	IO Interface	J12	4

Advanced Diagnostic Features

There are provisions on the Processor Extender board for several advanced diagnostic aids. These aids were designed to enhance the support that could be given by the advanced diagnostics.

Power Control LED's

The power control lines from the Main Processor board go to the Power Supply. The LED's on the extender board make it possible to monitor the signal outputs are changing logic states. The following chart shows the LED circuit identification and what Main Processor signal is driving that LED. These are also used in the advanced diagnostics tests.

Table 5-15. LED Reference Table.

LED Reference	Signal Name
DS 10	/SPLYON
DS 11	FAN1
DS 12	FAN2
DS 13	MTX1
DS 14	MTX2

Internal Serial Bus Test Hardware

The internal bus signals are routed to J80 for the purpose of testing the bus without any external modules other than the processor system boards being required. Provisions have been made on the IO Interface board to reduce the pull up current of the two serial buses by 50 % by removing J11. Then the data lines and the clock lines can be connected to allow the advanced diagnostics to test the MIC's on the IO Interface.

Optional Communications Interface Ports
All processor signals for the Communications Interface have been routed to connectors P10 and P11. This will allow the user to add the connectors and then test the Communications Interface outside of the instrument. Note that the internal Communications Interface must be removed before these connectors can be used, and by adding these connectors the board can not be installed in the instrument but must be mounted on another extender board. Installing these connectors requires that the user have two extender boards.

Front Panel Processor

The Front Panel Processor acts as an interface between the user and the instrument. These circuits translate operator actions on front-panel controls into data for the Main Processor to read and implement. The circuits output data showing current operating modes to the user via LED's (light emitting diodes) and crt readout.

The circuits consist of a Communications Port to interface with the rest of the instrument, a Processor System to process the data to and from the user, an LED Matrix to display data to the user, a Key Matrix to read data from the user, and a Chip Select circuit for read and write control of the other circuits.

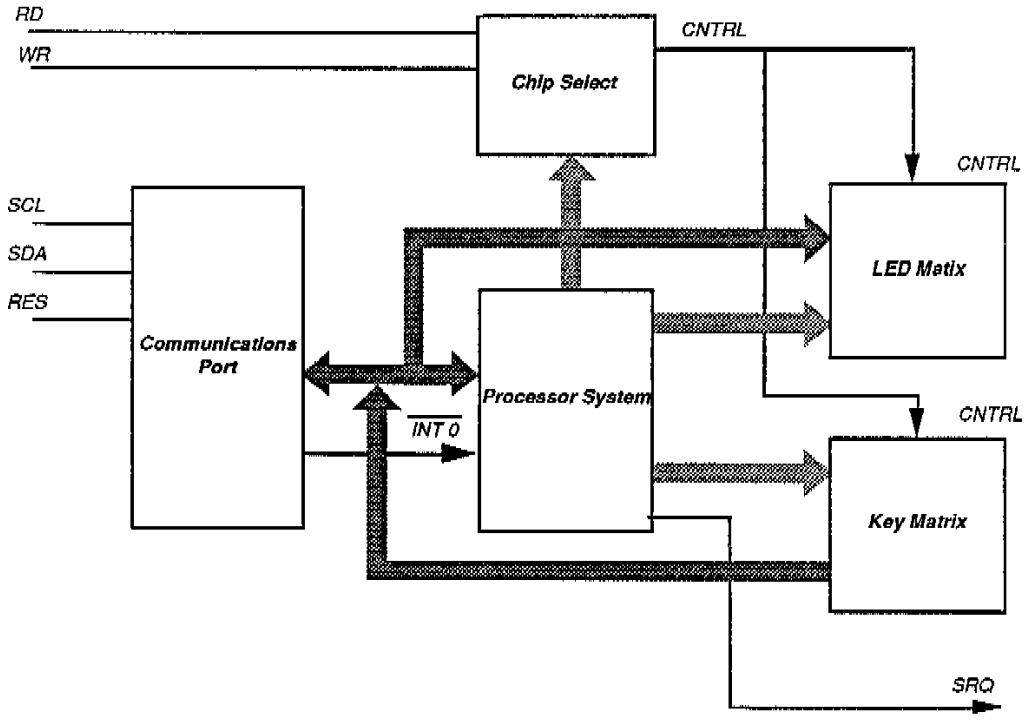


Figure 5-21. Front Panel Processor Block Diagram.

Key Matrix

The Key Matrix reads the front panel push buttons and knobs to determine the operating conditions. The front panel keys push against switches on the board. The knobs are optical encoders that convert knob rotation into digital numbers. One of the knobs takes the speed of rotation into account also.

LED Matrix

The LED Matrix lights the front panel indicators to show the selected buttons and conditions of operation.

Communications Port

The Communications Port interfaces the Front Panel circuits with the rest of the instrument. The port performs the serial-to-parallel conversion from the instrument bus to the front panel bus. This circuit issues interrupts to the front panel processor when a key or knob requests service.

Processor System

The Processor System consists of a one-chip computer, complete with RAM and ROM on the chip. The processor provides fast implementation of the knob and button requests. The circuit also issues an SRQ (Service Request) signal to the rest of the instrument.

Chip Select

The Chip Select circuit controls which of the other Front Panel circuits will read or write.

LV Power Supply

The Low Voltage Power Supply (A5) provides the low voltage power sources for the instrument. The assembly uses switching circuitry to provide high power, low ripple, and good regulation, with a minimum of weight and space. The supply is also well filtered for Electromagnetic Interference (EMI). The circuits are contained in a metal enclosure containing:

- EMI Filter (A5FL500)
- Primary Assembly (A5A1)
- Secondary Assembly (A5A2)
- Fan (A5B100)
- Communications Interface (A5A6)
- Rear Panel BNC Assembly (A5A7)

Note

The Communications Interface is part of the Digital Control circuits, and is described in that part of the circuit description.

The 125 Vdc primary voltage is chopped and coupled to the secondary through two power transformers. Secondary power is rectified, filtered, and in some cases regulated. Current is delivered from the secondary assembly (A5A2) to the mother board and then is distributed throughout the instrument.

EMI Filter

The EMI filter (A5FL500) has two main purposes. First, it is a power entry module that provides voltage selection, over-current protection, and voltage surge protection. Second, it attenuates high-frequency noise generated in the instrument that otherwise would be injected onto the power bus.

This noise has two components (for the three-wire system). One is common-mode noise, where the voltages (or currents) on both the high and neutral line vary together with respect to ground. The other is differential-mode (or normal-mode) noise, where the noise voltage (or current) on high and neutral lines vary 180 degrees out of phase with respect to one another.

Low pass filters for each noise mode reduce the amount of noise that enters or leaves the instrument. The normal-mode filter is contained in the EMI Filter Assembly. The common-mode filter components are located on both the Primary assembly (A5A1) and the EMI Filter Assembly.

Some important protection circuits are included in the EMI filter. These are:

- Input fuse
- Two surge protectors
- Two thermistors

Surge protectors clamp input voltage to 230 V for the 110 V selection and 460 V for the 220 V selection. (At 132 V_{rms}, the maximum peak voltage from the line

should be 187 V.) If the line input has a high-voltage spike with a lot of energy, the surge-protector clamps and blows the fuse. The thermistors limit in-rush current when the supply begins to receive line power.

Primary Circuits

Power is delivered to the Primary at 110 Vac or 220 Vac. There, an input rectifier converts the power to about 300 Vdc. At this point there is about 15 volts of 120 Hz ripple. A flyback regulator converts this noisy dc voltage to steady 125 Vdc. There are some EMI filtering components on the primary board. This filter keeps switching-frequency noise generated in the flyback regulator and power transformers from being injected onto the power bus.

On the primary assembly, the first step of protection is a 98°C thermal fuse (A5A1F10). The actual range is 94°C to 98°C. The fuse is inserted in the high-line path and protects the instrument from overheating. This fuse does not reset when the temperature decreases; if it opens, it must be replaced. (See the Corrective Maintenance part of the Maintenance Section for details.)

The pre-regulator has over-current and over-voltage protection. If for any reason the output of the pre-regulator increases above 158 V, the pulse-width modulator circuit senses the over-voltage, sets an error latch, and turns off the FET switches. The current through the pre-regulator is sensed by a current-sensing transformer and detected by the pulse-width modulator. The error latch is set when the current is about 3.8A.

Small current-sensing resistors sense the main and auxiliary push-pull power return current. Short-circuit conditions on unregulated power supply outputs are protected this way. The voltage developed across the current-sensing resistors is filtered and compared with a reference. When the current in either of the power converters is too high, the pulse-width modulator sets the error latch, and the FET switches turn off on both the pre-regulator and the push-pull power converters.

Whenever the error latch is set, the voltage on Vh goes to zero. This causes the pulse-width modulator input voltage (V_{in}) to drop until the pulse-width modulator turns off and the error latch resets. Then input voltage increases as the trickle-charger charges two large capacitors, and the pulse-width-modulator turns on again. If the fault condition still exists, the error latch will set again, FET switches will turn off, and V_{in} power to the pulse-width modulator will collapse resetting the error latch. This process will continue until the fault is corrected or the supply is unplugged. An audible ticking at a 4-to-10 Hz rate can be heard when supply is cycling through the fault mode.

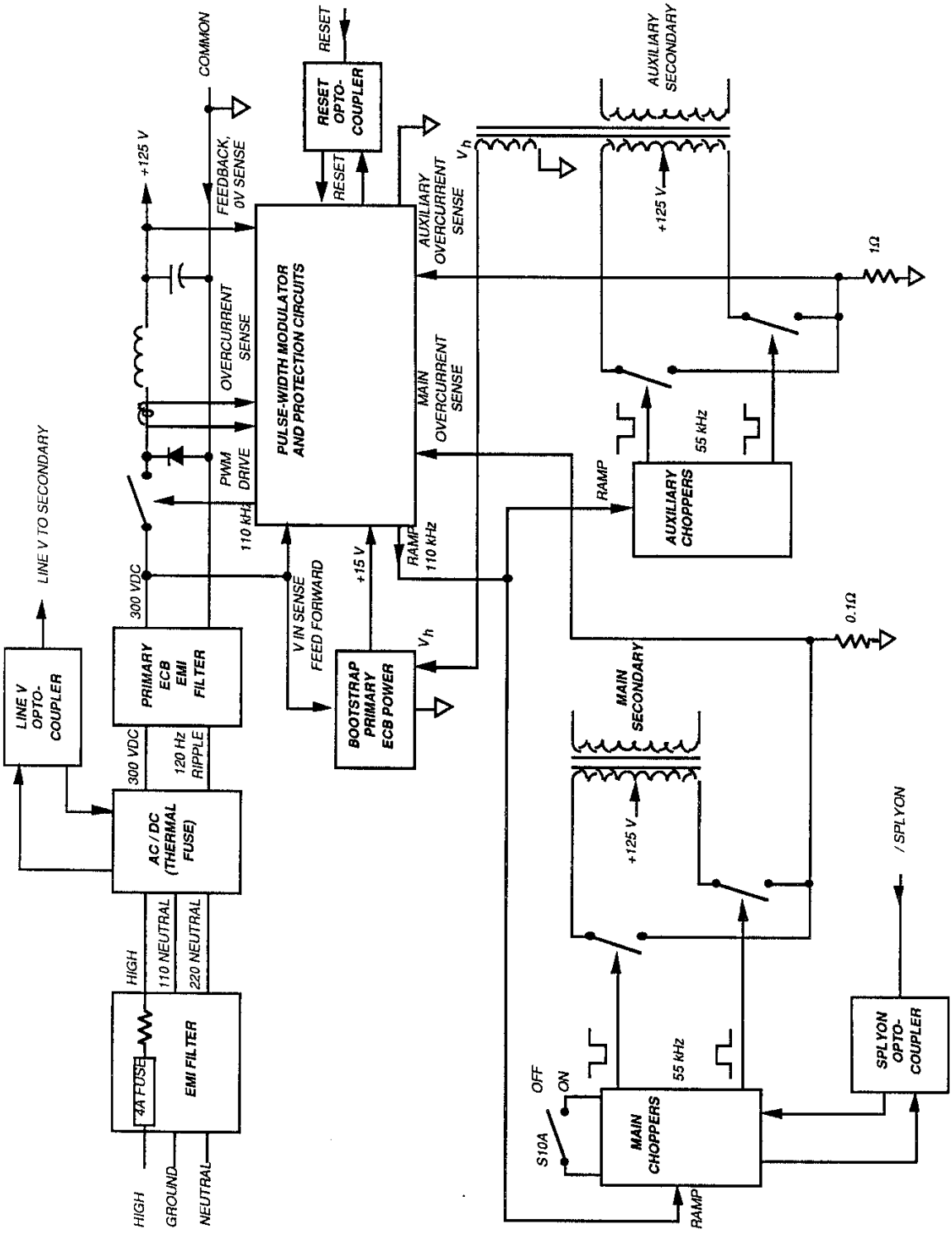


Figure 5-22. Low Voltage Power Supply Primary Block Diagram.

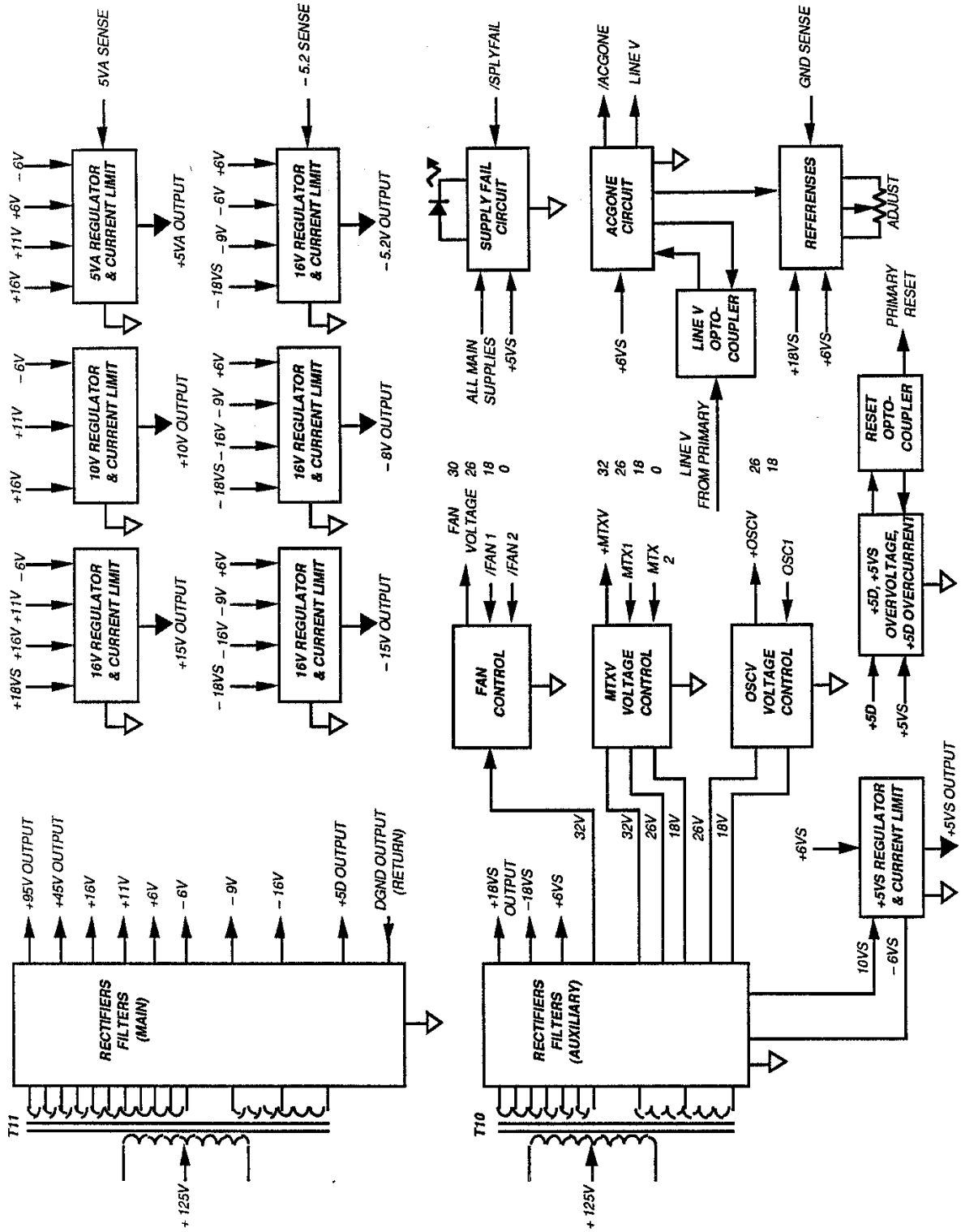


Figure 5-23. LV Power Supply Secondary Block Diagram.

Secondary Circuits

The secondary has seven regulated outputs, two switchable unregulated outputs (not including the fan voltage), and four other unregulated outputs. All seven regulators use high-gain amplifiers with pass bipolar junction transistors (BJTs) and also employ current foldback to protect against short-circuits. Each supply uses one or two low-pass pi filters to reduce high-frequency noise. Most of the outputs to the mother board are decoupled at the motherboard connector to further reduce noise on the outputs.

Regulator outputs are set by a reference circuit. The output voltage of a stable Zener diode is divided, filtered, and set at 5.0 V for the +5 VS reference. The other six references are set using operational amplifiers and 0.1% dividing resistors. The ground for these references is sensed at the mother board since there can be a large voltage drop from the mother board ground to the power supply ground. The reference circuit operates in standby mode so the main power supplies turn on quickly, about 20 to 40 milliseconds.

Auxiliary Supplies

If line voltage is applied to the supply, the auxiliary power converter is operating. There are eleven pairs of rectifiers that are powered by the auxiliary supply: one pair for the fan, three for +MTXV, two for +OSCV, one for +18 VS, one for -18 VS (used internally), and three for +5 VS. All of these rectifiers drive highly-capacitive filters as well as loads.

The fan has its own rectifier to help keep noise off of other outputs. Since the fan motor is major noise source, the fan voltage is decoupled. The fan speed can be controlled with /FAN1 and /FAN2. These control lines switch resistances attached to an adjustable voltage regulator via a 2-to-4 de-multiplexer.

Table 5-16. Fan Control Logic.

/FAN1	/FAN2	FAN
0 (LV)	0 (LV)	High
0 (LV)	1 (HV)	Medium
1 (HV)	0 (LV)	Low
1 (HV)	1 (HV)	Off

There are two supplies that have switchable output voltages: +MTXV and +OSCV. The +MTXV drives the preselector. The +MTXV output is set by decoding MTX1 and MTX2 and turning on one of three p-channel FETs. These FETs have extra gate-to-source capacitance in order to slow down voltage transitions and limit inrush current during switching. The following table shows the +MTXV control logic.

Table 5-17. MTXV Control Logic.

MTX2	MTX1	+MTXV
0	0	0 V
0	1	18 V
1	0	26 V
1	1	32 V

The +OSCV is switched between 18 Vdc and 26 Vdc by turning a p-channel FET on or off. When the FET is on, +OSCV has 26 Vdc of output and the 18 V rectifier diodes are back biased. When the FET is off, +OSCV current is sourced through the 18 V rectifier diodes.

Table 5-18. OSCV Control Logic.

OSC1	OSCV
0	18 V
1	26 V

+18 VS and -18 VS are two unregulated un-switchable auxiliary supplies. +18 VS is used internally on the Secondary assembly as well as used to power a heater for the Reference Oscillator oven. The -18 VS is used only as an internal power supply for the Secondary assembly.

The +6 VS is also used to power Secondary assembly control circuitry, but its main function is to source output current for the +5 VS (+5 V Standby) regulator. The +5 VS supply powers the Main Processor system as well as the Communications Interface. A shunt regulator provides over-voltage protection to preserve these sensitive loads. When +5 VS increases above 5.5 V, the shunt regulator latches and sends a signal to the Primary assembly through the RESET opto-coupler to reduce the pre-regulator duty cycle and output voltage.

Main Supplies

The main supply has three unregulated outputs and six regulated outputs. The +5D (+5 V digital) has a separate current return called DGND (digital ground). The separate ground keeps digital noise from being induced into other supplies. The +5D supply is current-protected by sensing the voltage drop across filter inductors. When the current in +5D gets close to 10 A, a signal sent through the RESET opto-coupler reduces the pre-regulator duty cycle and output voltage on the Primary assembly. The +5D supply also has over-voltage protection using the same type of circuit described above for +5 VS supply.

The +95 V and +45 V supplies are low-current unregulated supplies used in display circuits. The +45 V supply is created by doubling the voltage off of the 16 V winding and adding the 11 V winding voltage. Although this seems to add up to be 43 V, the +45 V output is actually close to 45 V.

Other unregulated main supplies on the Secondary assembly are used to source output current for the regulators. These are +16 V, +11 V, +6 V, -6 V, -9 V, and -

16 V. The regulators, +15 V, +10 V, +5 VA (+5 V analog) -5.2 V, -8 V, and -15 V are all similar to the +5 VS regulator. The +5 VA and -5.2 V output voltages are sensed at the mother board to keep a low tolerance on these supplies.

The LINEV opto-coupler transmits a line-frequency square wave to an amplifier on the Secondary assembly. The output is AC coupled and routed to the mother board. The LINEV signal is also monitored with a peak detector. If line power shuts off, LINEV will cease to switch and the peak detector will discharge underneath the ACGONE threshold. This causes /ACGONE to switch low, and it signals the processor that the instrument lost line power. The processor then turns off the main supply and does other shut-down routines before auxiliary power collapses.

The output of all the regulated supplies is sensed in the supply fail circuit. A current sum circuit is used to sense the combined voltage. If one supply goes far out of tolerance, the /SPLYFAIL bit goes low and the green LED (DS10) on the Secondary assembly turns off. The +95 V and +45 V supplies are also sensed for failures. This circuit helps in trouble-shooting instrument problems.

Protection Circuits

Several protection circuits are included on the Secondary assembly. They control the RESET opto-coupler:

- +5 VS over-voltage
- +5 VD over-voltage
- +5 VD over-current

When the RESET signal on the Primary assembly goes low, the duty cycle of the pulse-width modulator drive goes to zero. The supply will not shut down all the way, but the the +125 Vdc pre-regulator output will get very small. Oscillation between low-output and fault states can occur with these fault conditions and is noticeable by an audible whine or buzz. (It is easily seen on an oscilloscope by probing the +5D output.)

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

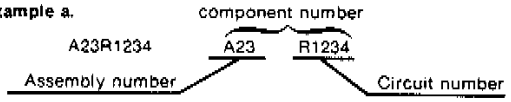
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

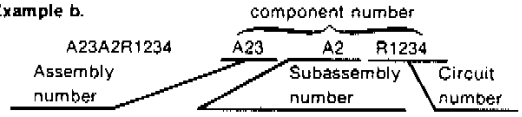
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

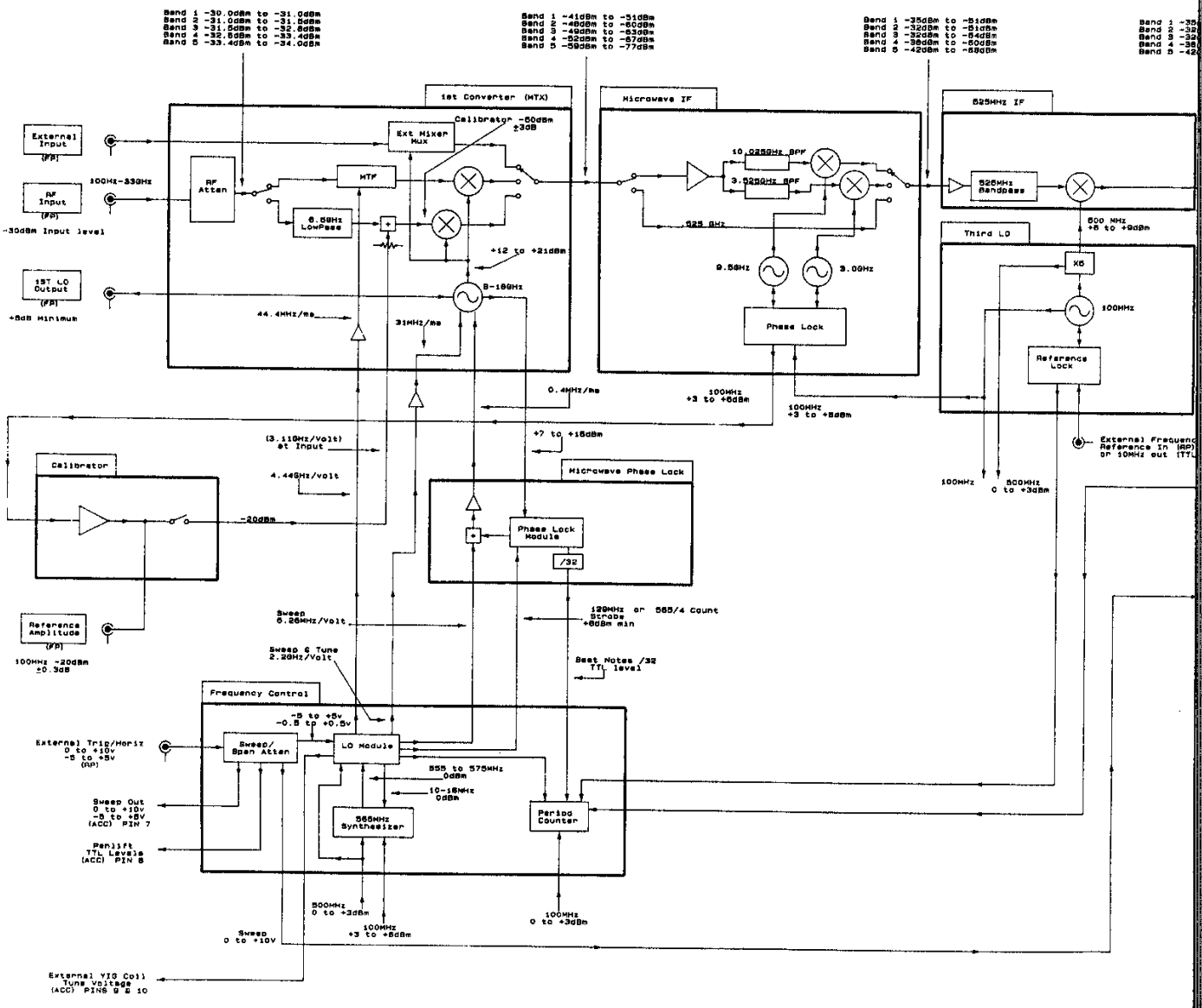
CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00681	MINE SAFETY APPLIANCE CO CATALYST RESEARCH DIV	1421 CLARKVIEW RD	BALTIMORE MD 21209-2103
14482	WATKINS-JOHNSON CO	3333 HILLVIEW AVE	PALO ALTO CA 94304-1204
27012	MICRO DEVICES CORP SUB OF EMERSON ELECTRIC CO	1320 S MAIN ST PO BOX 3538	MANSFIELD OH 44907-2516
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	670-9439-01			CIRCUIT BD ASSY:MOTHER	80009	670-9439-01
A2A1	670-9466-00	B010100	B010128	CIRCUIT BD ASSY:FRONT PANEL #1	80009	670-9466-00
A2A1	670-9466-01	B010129		CIRCUIT BD ASSY:FRONT PANEL #1	80009	670-9466-01
A2A2	670-9465-01			CIRCUIT BD ASSY:FRONT PANEL #2	80009	670-9465-01
A3	012-1283-00			CABLE ASSEMBLY:FLAT FLEX COAX	80009	012-1283-00
A5	621-0038-01	B010100	B010147	PWR SUPPLY ASSY:	80009	621-0038-01
A5	621-0038-02	B010148		PWR SUPPLY ASSY:2782	80009	621-0038-02
A5B100	119-2222-01	B010100	B010147	FAN,TUBEAXIAL:24V,2.6W,3450RPM,36CFM,BRUSHL ESS,WITH CONNECTORS	80009	119-2222-01
A5B100	119-2222-02	B010148		FAN,TUBEAXIAL:24V,2.6W,3450RPM,36CFM,BRUSHL ESS,WITH CONNECTORS	80009	119-2222-02
A5FL500	119-3127-00			FILTER ASSEMBLY:EMI,ENCAPSULATED	80009	119-3127-00
A5W516	174-0372-00			CABLE ASSY,RF:50 OHM COAX,9.0 L	80009	174-0372-00
A5A1	670-9450-01	B010100	B010147	CIRCUIT BD ASSY:POWER SUPPLY PRIMARY	80009	670-9450-01
A5A1	670-9450-02	B010148		CIRCUIT BD ASSY:POWER SUPPLY PRIMARY	80009	670-9450-02
A5A1F10	159-0321-00			FUSE,TERMINAL:15A,98DRG C MAX OPENING TEMP	27012	4204A1
A5A2	670-9451-01	B010100	B010147	CIRCUIT BD ASSY:POWER SUPPLY SECONDARY	80009	670-9451-01
A5A2	670-9451-02	B010148		CIRCUIT BD ASSY:POWER SUPPLY SECONDARY	80009	670-9451-02
A5A6	671-0082-01	B010100	B010152	CIRCUIT BD ASSY:COMMUNICATIONS INTERFACE	80009	671-0082-01
A5A6	671-0082-02	B010153		CIRCUIT BD ASSY:COMMUNICATIONS INTERFACE	80009	671-0082-02
A5A7	670-9495-00	B010100	B010134	CIRCUIT BD ASSY:REAR PANEL BNC	80009	670-9495-00
A5A7	670-9495-01	B010135		CIRCUIT BD ASSY:REAR PANEL BNC	80009	670-9495-01
A10	119-2675-00	B010100	B010133	ATTENUATOR:33GHZ,70DB	80009	119-2675-00
A10	119-2675-01	B010134		ATTENUATOR:33GHZ-70DB	80009	119-2675-01
A11	119-2496-01			YIG OSC ASSY:8-18GHZ	80009	119-2496-01
A11A2	671-0242-01			CIRCUIT BD ASSY:YIG OSC DRIVER	80009	671-0242-01
A12	119-2743-01	B010100	B010118	CONVERTER ASSY:MAGNETICALLY TUNED	80009	119-2743-01
A12	119-2743-02	B010119		CONVERTER ASSY:MAGNETICALLY TUNED	80009	119-2743-02
A12A4	119-2742-00			TERMINATOR ASSY:LOW PASS	80009	119-2742-00
A12A5	119-2876-00			MIXER,LOW PASS:10.025GHZ,50MHZ	14482	M52DC-1
A13	119-2887-02			MWIF ASSEMBLY:MICROWAVE IF	80009	119-2887-02
A14	119-2285-00	B010100	B010129	INTMD FREQ ASSY:525 IF MODULE	80009	119-2285-00
A14	119-2285-01	B010130		INTMD FREQ ASSY:525 IF MODULE	80009	119-2285-01
A15	119-3072-00			CALIBRATOR ASSY:	80009	119-3072-00
A15A3	119-3676-00			ISOLATOR,RF:WIDE BAND,8-18GHZ	80009	119-3676-00
A16	644-0631-02	B010100	B010126	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-02
A16	644-0631-03	B010133	B010135	VR ASSEMBLY:VARIBLE RESOLUTION	80009	644-0631-03
A16	644-0631-04	B010127		VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-04
A17	119-2938-02	B010100	B010126	PHASELOCK ASSY:MICROWAVE	80009	119-2938-02
A17	119-2938-03	B010127		PHASELOCK ASSY:MICROWAVE	80009	119-2938-03
A18	670-9438-02			CIRCUIT BD ASSY:LOG PROCESSOR	80009	670-9438-02
A20	672-0257-02			CIRCUIT BD ASSY:DIGITAL VIDEO PROCESSOR	80009	672-0257-02
A22	670-9448-02	B010100	B010125	CIRCUIT BD ASSY:DISPLAY AMP	80009	670-9448-02
A22	670-9448-03	B010126		CIRCUIT BD ASSY:DISPLAY AMP	80009	670-9448-03
A23	670-9449-01			CIRCUIT BD ASSY:HIGH VOLTAGE	80009	670-9449-01
A24	670-9447-01			CIRCUIT BD ASSY:DIGITAL STORAGE	80009	670-9447-01
A24U16	160-5825-00			MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5825-00
A25	672-1269-01	B010100	B010132	CIRCUIT BD ASSY:LO MODULE	80009	672-1269-01
A25	672-1269-02	B010133	B010139	CIRCUIT BD ASSY:LO MODULE	80009	672-1269-02
A25	672-1269-03	B010140	B010149	CIRCUIT BD ASSY:LO MODULE	80009	672-1269-03
A25	672-1269-04	B010150		CIRCUIT BD ASSY:LO MODULE	80009	672-1269-04
A28	672-0195-02	B010100	B010134	CIRCUIT BD ASSY:PERIOD COUNTER	80009	672-0195-02
A28	672-0195-03	B010135		CIRCUIT BD ASSY:PERIOD COUNTER	80009	672-0195-03
A29	670-9461-02	B010100	B010135	CIRCUIT BD ASSY:REFERENCE OSC	80009	670-9461-02
A29	670-9461-03	B010136		CIRCUIT BD ASSY:REFERENCE OSC	80009	670-9461-03
A31	672-0190-01	B010100	B010116	CIRCUIT BD ASSY:PHASE LOCK	80009	672-0190-01
A31	672-0190-02	B010117		CIRCUIT BD ASSY:PHASE LOCK	80009	672-0190-02
A33	670-9459-01			CIRCUIT BD ASSY:SWEEP/SPAN ATTEN	80009	670-9459-01
A41	670-9463-00	B010100	B010125	CIRCUIT BD ASSY:MAIN PROCESSOR	80009	670-9463-00

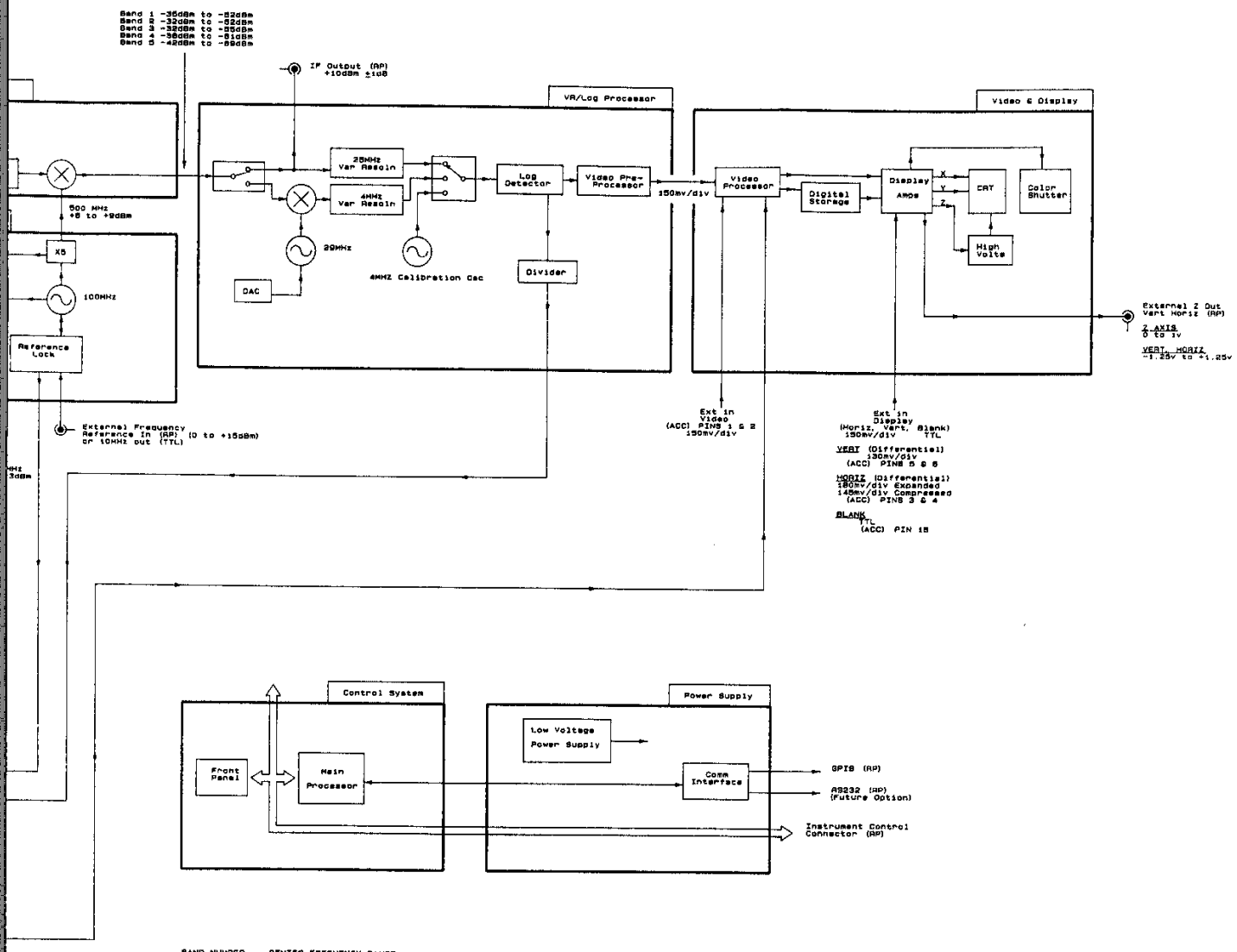
Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A41	670-9463-01	B010126		CIRCUIT BD ASSY:MAIN PROCESSOR	80009	670-9463-01
A41U63	160-5824-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5824-00
A41U63	160-5824-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5824-01
A42	670-9464-01			CIRCUIT BD ASSY:I/O INTERFACE	80009	670-9464-01
A42BT10	146-0044-00			BATTERY,DRY:3V,0.17AH @ 0.85MA,BUTTON CELL, LITHIUM-MANGANESE DIOXIDE	00681	ORDER BY DESCR
A42BT11	146-0044-00			BATTERY,DRY:3V,0.17AH @ 0.85MA,BUTTON CELL, LITHIUM-MANGANESE DIOXIDE	00681	ORDER BY DESCR
A43	670-9462-00			CIRCUIT BD ASSY:ROM	80009	670-9462-00
A43U10	160-5823-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5823-00
A43U10	160-5823-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5823-01
A43U11	160-5819-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5819-00
A43U11	160-5819-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5819-01
A43U12	160-5820-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5820-00
A43U12	160-5820-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5820-01
A43U13	160-5821-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5821-00
A43U13	160-5821-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5821-01
A43U14	160-5822-00	B010100	B010135	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5822-00
A43U14	160-5822-01	B010136		MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5822-01
	670-9447-01			CIRCUIT BD ASSY:DIGITAL STORAGE	80009	670-9447-01
F10	159-0319-00			FUSE,CARTRIDGE:4A,125V,FAST	80009	159-0319-00
F10	159-0320-00			FUSE,CARTRIDGE:4A,250V,FAST (OPTIONS A1, A2, A3, A4, A5 ONLY)	80009	159-0320-00
FL100	174-1068-00			CABLE ASSY,RF:50 OHM COAX,8.335 L	80009	174-1068-00
L10	108-1335-00			COIL,TUBE DEFL:FXD,TRACE ROTATOR	80009	108-1335-00
P16	015-0567-00			TERMN,COAXIAL:50 OHM 0.5W DC TO 18.0GHZ	34078	2444MC-032
P18	015-0567-00			TERMN,COAXIAL:50 OHM 0.5W DC TO 18.0GHZ	34078	2444MC-032
V100	154-0891-00			ELECTRON TUBE:T6630,CRT FINISHED	80009	154-0891-00
W100	174-1112-00			CABLE ASSEMBLY:ATTEN/SW DIPLEXER,2.958 L	80009	174-1112-00
W112	174-0355-00			CABLE ASSY,RF:SEMIRIGID,50 OHM COAX,10.715 L	80009	174-0355-00
W114	174-1863-00			CABLE ASSY,RF:50 OHM SEMI RIGID	80009	174-1863-00
W140	174-0380-00			CABLE ASSY,RF:50 OHM COAX,10.0 L	80009	174-0380-00
W150	174-0357-00			CABLE ASSY,RF:50 OHM COAX,4.06 L	80009	174-0357-00
W152	174-0373-00			CABLE ASSY,RF:50 OHM COAX,9.14 L	80009	174-0373-00
W154	174-1864-00			CABLE ASSY,RF:50 OHM SEMI RIGID	80009	174-1864-00
W166	174-0361-00			CABLE ASSY,RF:50 OHM COAX,4.625 L	80009	174-0361-00
W250	174-0374-00			CABLE ASSY,RF:50 OHM COAX,13.75 L	80009	174-0374-00
W280	174-0375-00			CABLE ASSY,RF:50 OHM COAX,19.75 L	80009	174-0375-00
W292	174-0376-00			CABLE ASSY,RF:50 OHM COAX,14.625 L	80009	174-0376-00
W1280	174-0377-00			CABLE ASSY,RF:50 OHM COAX,20.0 L	80009	174-0377-00
W1320	174-0356-00			CABLE ASSY,RF:SEMIRIGID,50 OHM COAX,14.578 L	80009	174-0356-00
W1334	174-0378-00			CABLE ASSY,RF:50 OHM COAX,5.25 L	80009	174-0378-00

BLOCK DIA.
SHT. 1 OF 2



2782

BLOCK DIA.
SHT. 2 of 2

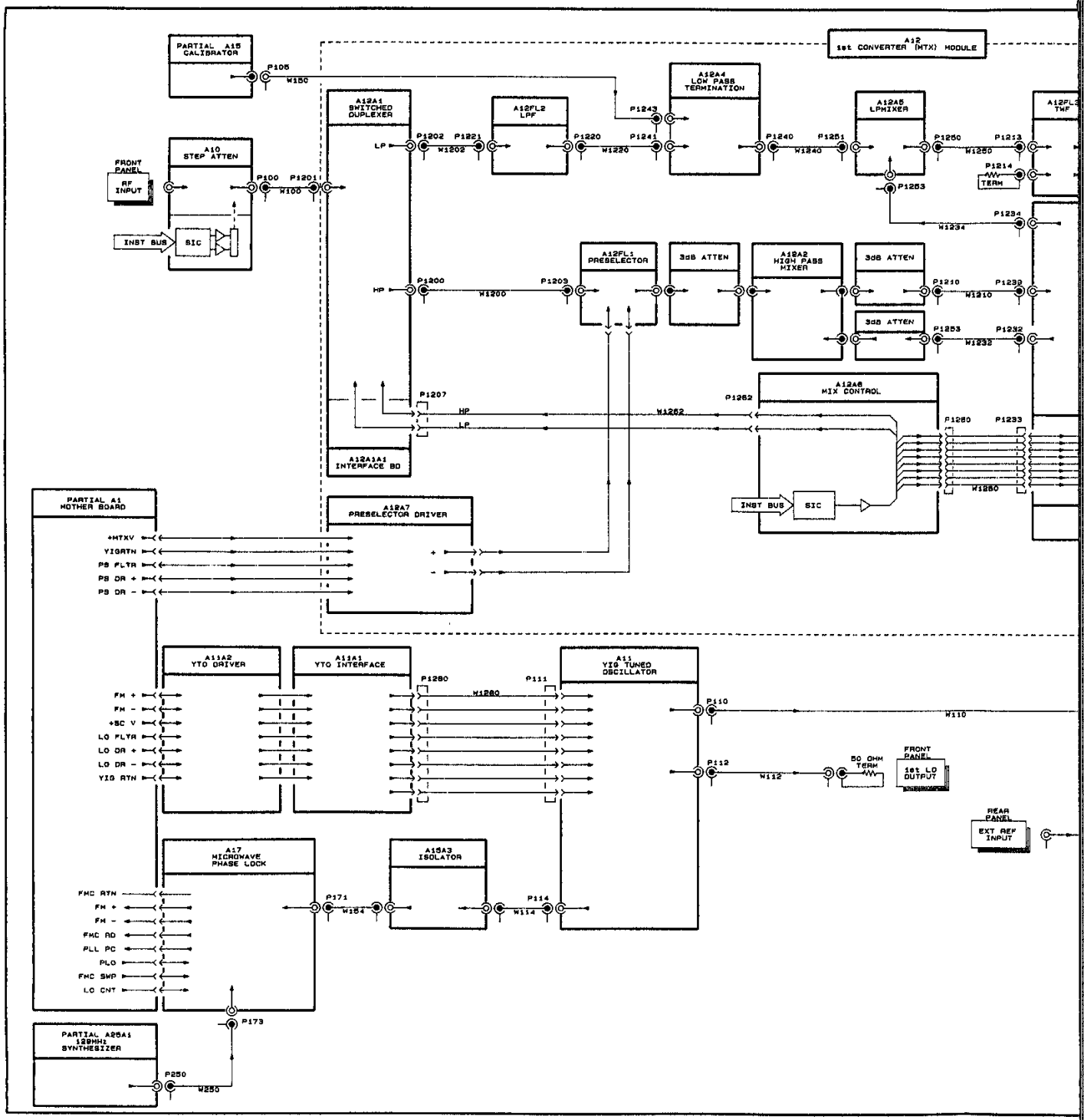


BAND NUMBER	CENTER FREQUENCY RANGE
Band 1:	0 to 6.6GHz
Band 2:	6.5 to 12.7GHz
Band 3:	12.7 to 21.7GHz
Band 4:	21.7 to 28GHz
Band 5:	28 to 33GHz

SIGNAL LEVELS SHOWN WITH
-30dBm INPUT SIGNAL AND
-30dBm REFERENCE LEVEL

BLOCK DIAGRAM

RF DECK INTRCNCT.
SHT. 1 OF 2



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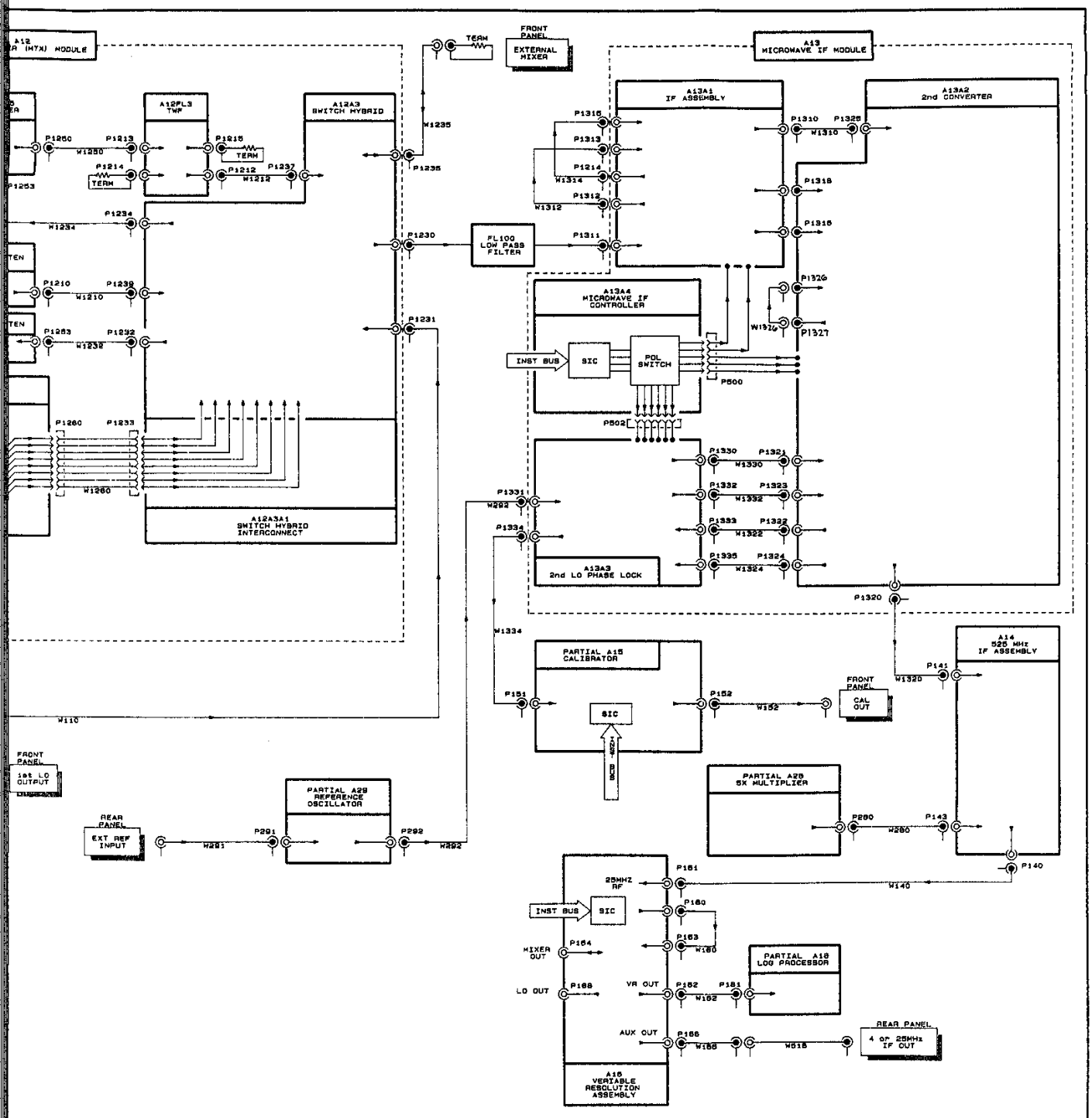
RF DECK INTRCNCT.
SHT. 2 OF 2



RF DECK INTERCONNECT

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
                - - - * - - -
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
                - - - * - - -
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
                - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
04348	LAWRENCE ENGINEERING AND SUPPLY INC	500 S FLOWER ST P O BOX 30	BURBANK CA 91503
09772	WEST COAST LOCKWASHER CO INC	16730 E JOHNSON DRIVE P O BOX 3588	CITY OF INDUSTRY CA 91744
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125-4632
16179	M/A-COM OMNI SPECTRA INC MICROWAVE COMPONENT DIV SUB OF M/A-COM INC	21 CONTINENTAL BLVD	MERRIMACK NH 03054-4303
16428	COOPER BELDEN ELECTRONIC WIRE AND CA SUB OF COOPER INDUSTRIES INC	NW N ST	RICHMOND IN 47374
18565	CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801-1039
19505	APPLIED ENGINEERING PRODUCTS	1475 WHALLEY AVE PO BOX A-D	NEW HAVEN CT 06525
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
39766	MERRILL MFG CORP	236 S GENESEE ST PO BOX 566	MERRILL WI 54452-3314
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
70903	COOPER BELDEN ELECTRONICS WIRE AND C SUB OF COOPER INDUSTRIES INC	2000 S BATAVIA AVE	GENEVA IL 60134-3325
72228	AMCA INTERNATIONAL CORP CONTINENTAL SCREW CO DIV	459 MT PLEASANT	NEW BEDFORD MA 02742
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
77900	ILLINOIS TOOL WORKS SHAKEPROOF DIV	ST CHARLES RD	ELGIN IL 60120
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
83385	MICRODOT MFG INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
91836	KINGS ELECTRONICS CO INC	40 MARBLEDALE ROAD	TUCKAHOE NY 10707-3420
93459	WEINSCHEL ENGINEERING CO INC	1 WEINSCHEL LANE	GAITHERSBURG MD 20877
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
98291	SEALECTRO CORP BICC ELECTRONICS	40 LINDEMAN DR	TURNBULL CT 06611-4739
S3109	FELLER	72 Veronica Ave Unit 4	Summerset NJ 08873
TK0433	PORTLAND SCREW CO	6520 N BASIN	PORTLAND OR 97217-3920
TK0858	STAUFFER SUPPLY CO (DIST)	810 SE SHERMAN	PORTLAND OR 97214
TK1302	MOUNTAIN MOLDING	606 SECOND STREET	BERTHOUD CO 80513
TK1312	LEMO USA INC	335 TESCONI CIR PO BOX 11006	SANTA ROSA CA 95406
TK1373	PATELEC-CEM (ITALY)	10156 TORINO	VAICENTALLO 62/455 ITALY
TK1375	ESAM	PO BOX 376	GRANTS PASS OR 97526
TK1543	CAMCAR/TEXTRON	600 18TH AVE	ROCKFORD IL 61108-5181

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	200-3475-00			1	COVER,FRONT:POLYCARBONATE	80009	200-3475-00
-2	348-1011-00			4	FOOT,CABINET:TOP	80009	348-1011-00
					(ATTACHING PARTS)		
-3	211-0674-00			4	SCREW,MACHINE:6-32 X 0.312,TRH,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-4	386-5719-00			4	PLATE,FOOT:TOP,ALUMINUM	80009	386-5719-00
-5	348-1012-00			4	FOOT,CABINET:BOTTOM	80009	348-1012-00
					(ATTACHING PARTS)		
-6	211-0674-00			4	SCREW,MACHINE:6-32 X 0.312,TRH,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	386-5718-00			4	PLATE,FOOT:BOTTOM,ALUMINUM	80009	386-5718-00
-8	366-0579-00			2	PUSH BUTTON:ALUMINUM	80009	366-0579-00
-9	129-1108-00			2	SPACER,POST:0.1 L,6-32 THD BOTH ENDS,PLSTC	80009	129-1108-00
-10	367-0384-00			1	HANDLE ASSEMBLY:PLASTIC/ALUMINUM/RUBBER	80009	367-0384-00
					(ATTACHING PARTS)		
-11	212-0560-00			6	SCREW,MACHINE:10-32 X 0.312,FLH,100 DEG	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-12	380-0668-00			2	HOUSING,INDEX:	80009	380-0668-00
					(ATTACHING PARTS)		
-13	213-0858-00			8	SCREW,TPG,TR:6-32 X 0.5 L,TAPTITE,FLH	83385	ORDER BY DESCR
					(END ATTACHING PARTS)		
-14	386-5625-00			2	PLATE,HANDLE:ALUMINUM	80009	386-5625-00
-15	200-2694-00			2	COVER,INDEX:ALUMINUM	80009	200-2694-00
					(ATTACHING PARTS)		
-16	213-0918-00			6	SCREW,TPG,TR:8-32 X 0.625,FLH,82 DEG,POZ	72228	ORDER BY DESCR
					(END ATTACHING PARTS)		
-17	214-3200-00			2	SPRING,HLCPS:0.798 OD X 1.1 L,CLE,MUW	80009	214-3200-00
-18	105-0893-00			2	INDEX RLSE,HDL:	80009	105-0893-00
-19	105-0894-00			2	INDEX STOP,HDL:	80009	105-0894-00
-20	214-3198-00			2	INDEX,HANDLE:	80009	214-3198-00
-21	200-3624-00			1	COVER,REAR:POLYCARBONATE	80009	200-3624-00
-22	348-1017-00			2	FOOT,CABINET:REAR	80009	348-1017-00
					(ATTACHING PARTS)		
-23	212-0630-01			4	SCREW,SPCL MACH:10-24 X 1.55 L,FLH,45 DEG	TK0858	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	426-2220-00			1	FRAME,REAR:ALUMINUM	80009	426-2220-00
-25	334-7025-00			1	MARKER,IDENT:MKD 2782 SPECTRUM ANALYZER	80009	334-7025-00
-26	334-7700-00			1	MARKER,IDENT:MKD CAUTION	80009	334-7700-00
-27	437-0355-00			1	CABINET,SA:	80009	437-0355-00

FIG. 1 CABINET ASSY.
SHT. 1 OF 2

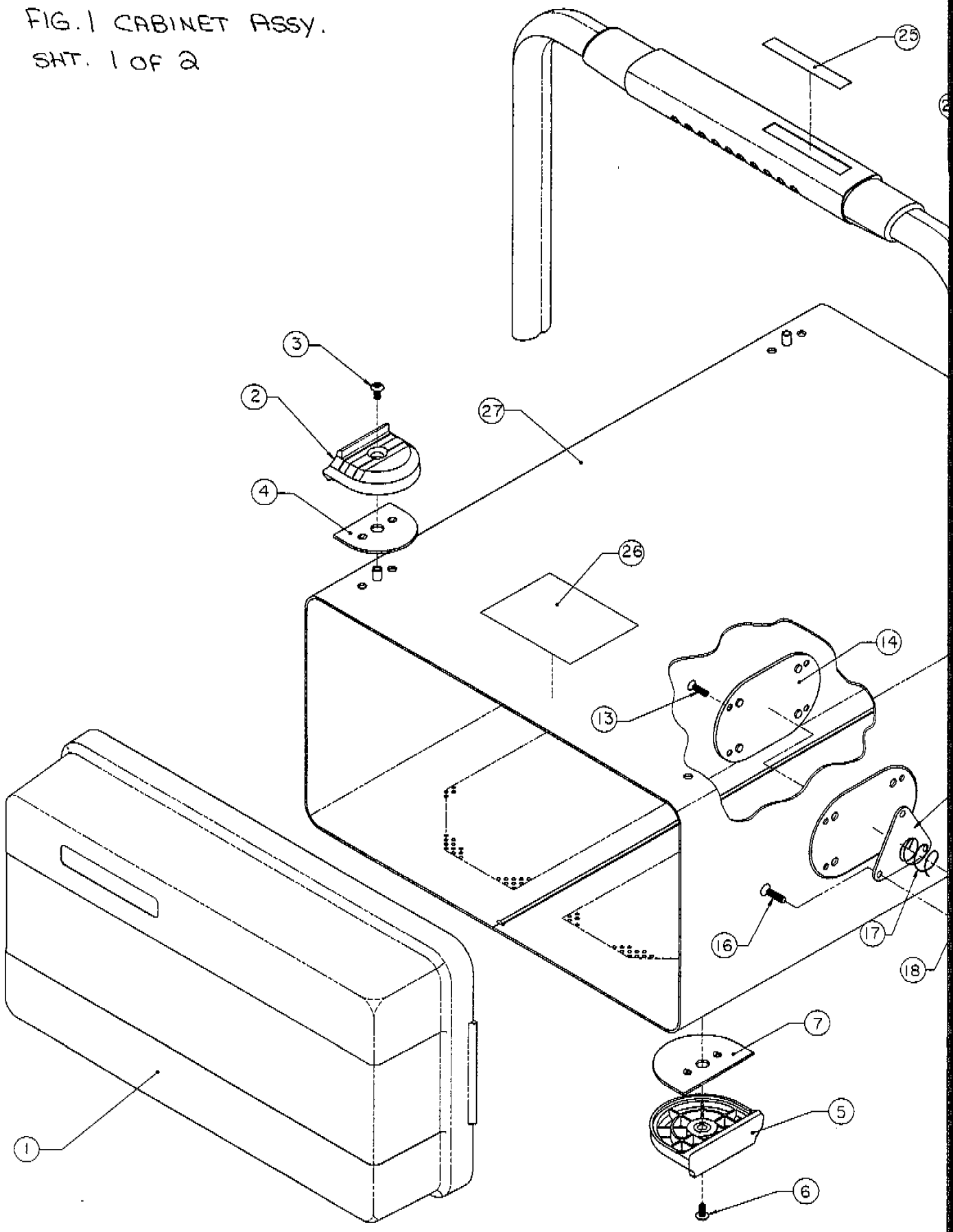


FIG. 1 CABINET ASSY.
SHT. 2 OF 2

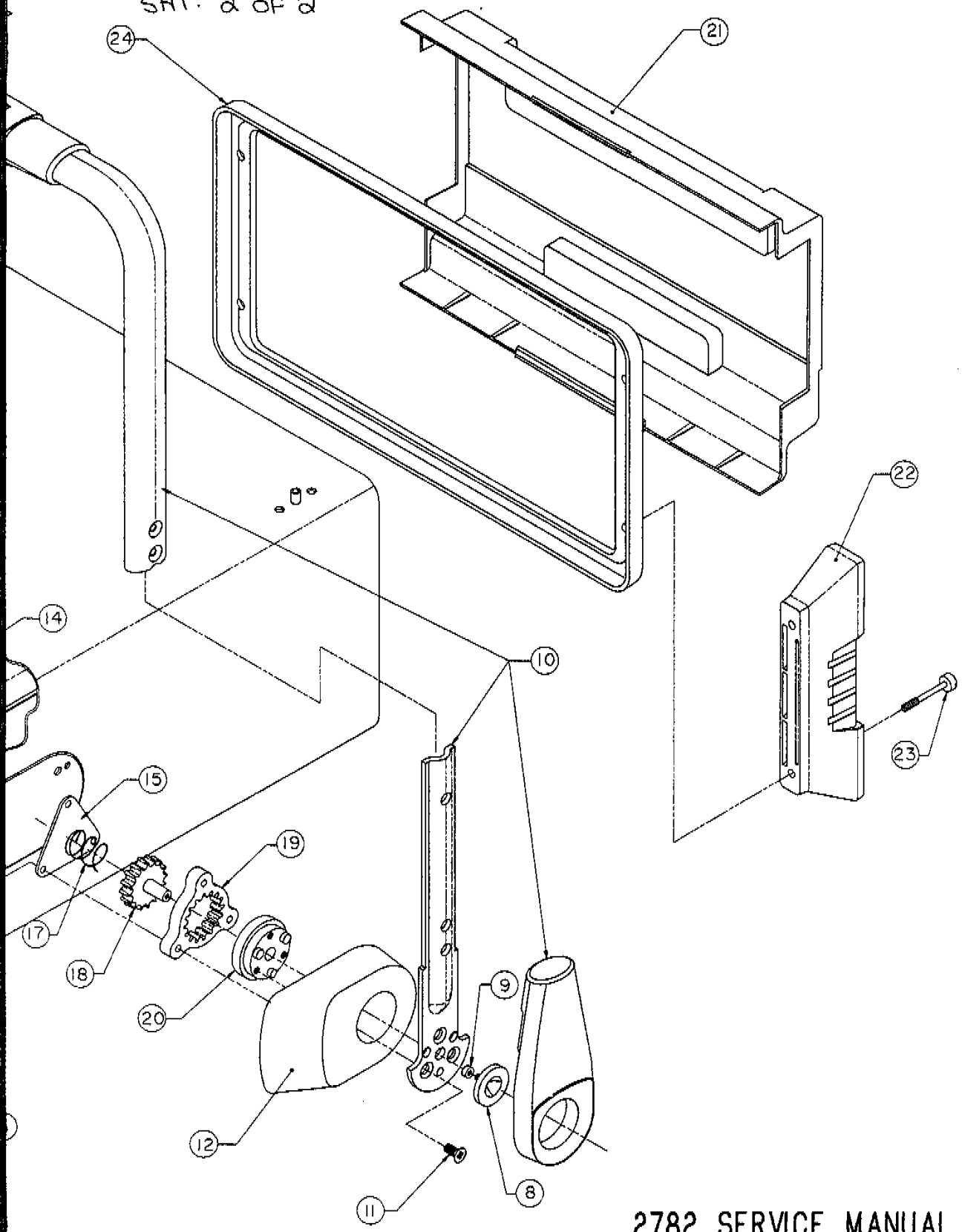
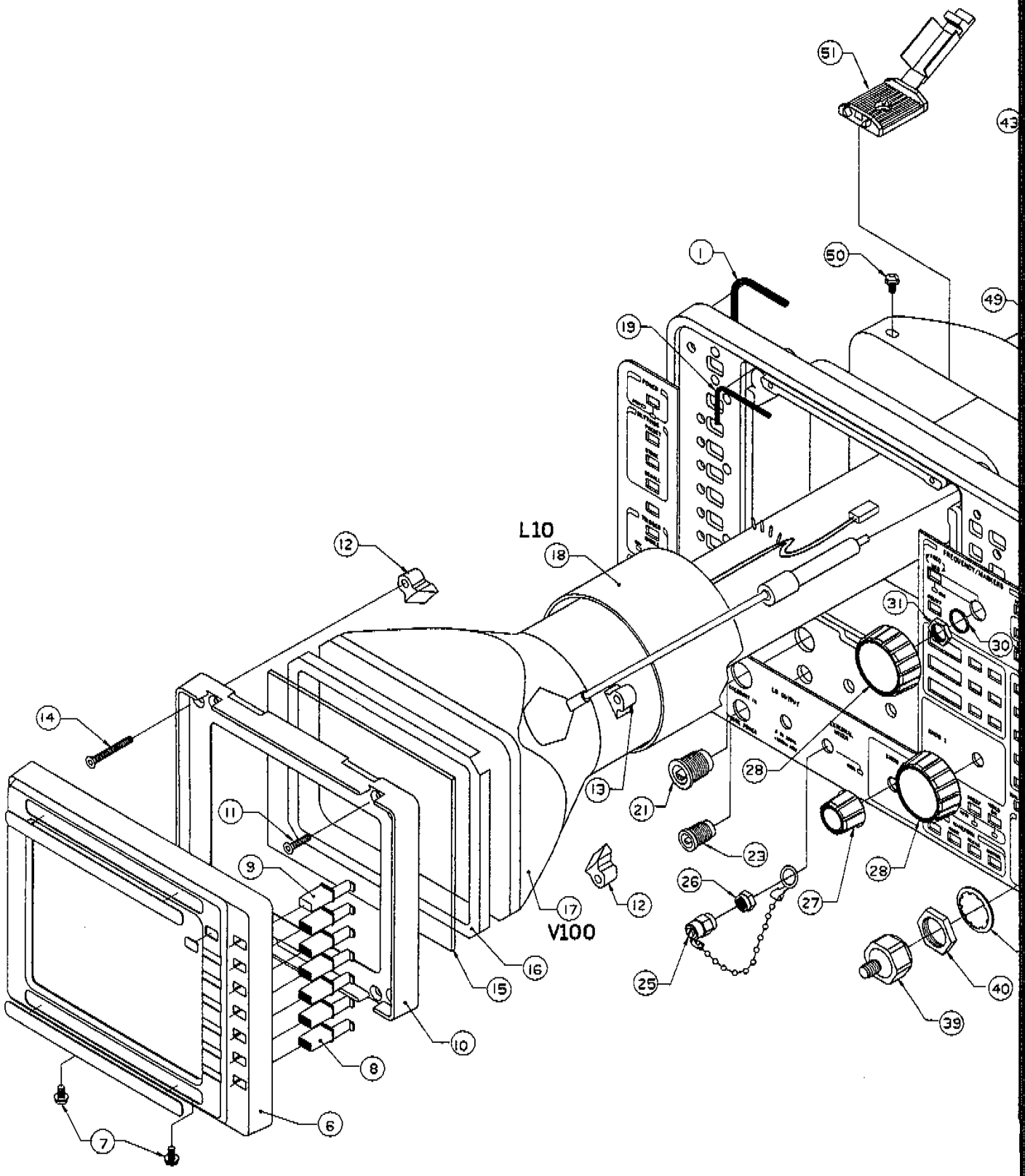


FIG. 1 CABINET ASSY.

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	337-0925-04			1	SHLD GSKT,ELEK:37.0 L	TK1375	ORDER BY DESCR
-2	386-5381-00			1	SUBPANEL,FRONT:	80009	386-5381-00
					(ATTACHING PARTS)		
-3	212-0650-00			4	SCREW,MACHINE:10-32 X 0.437,FLH,100 DEG,SST	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-4	136-0935-00			1	SKT,PL-IN ELEK:ELECTRON TUBE,W/LEADS	80009	136-0935-00
-5	200-0917-01			1	COVER,CRT SKT:2.052 OD X 0.291 H,PLASTIC	80009	200-0917-01
-6	119-2939-00			1	COLOR SHUTTER A:RED/GREEN 5 INCH DIAGONAL	80009	119-2939-00
					(ATTACHING PARTS)		
-7	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-8	366-0609-00			6	PUSH BUTTON:MENU	80009	366-0609-00
-9	366-0730-00			1	KEYCAP:MENU APPEARANCE BEZEL	80009	366-0730-00
-10	426-2129-00			1	FRAME,CRT:	80009	426-2129-00
					(ATTACHING PARTS)		
-11	211-0777-00			4	SCREW,MACHINE:6-32 X 0.5,FH TORX	80009	211-0777-00
					(END ATTACHING PARTS)		
-12	343-1354-00			2	RETAINER,CRT:LOWER RIGHT,UPPER LEFT,PLASTIC	80009	343-1354-00
-13	343-1355-00			2	RETAINER,CRT:UPPER RIGHT,LOWER LEFT,PLASTIC	80009	343-1355-00
					(ATTACHING PARTS)		
-14	211-0523-00			4	SCREW,MACHINE:6-32 X 0.875,FLH,100 DEG,STL	04348	ORDER BY DESCR
					(END ATTACHING PARTS)		
-15	331-0492-00			1	WINDOW,CRT:EMI,OPTICAL POLYCARBONATE	80009	331-0492-00
-16	361-1537-00			1	SHIM:0.25 THK X 3.39 X 4.24,MYLAR	80009	361-1537-00
-17	----- -----			1	ELECTRON TUBE:FINISHED(SEE V100 REPL)		
-18	----- -----			1	COIL,TUBE DEFL:FXD,TRACE ROTATOR		
					(SEE L10 REPL)		
-19	348-1016-00			1	GASKET,RF:CRT FRAME,0.1 DIA	80009	348-1016-00
-20	174-0359-00			1	CA ASSY,SP,ELEC:8,26 AWG,5.0 L	80009	174-0359-00
-21	131-1011-00			1	CONN,RCPT,ELEC:SNAP LOCK,2 MALE,2 FEMALE	TK1312	RA 1.304
					(ATTACHING PARTS)		
-22	210-0021-00			1	WASHER,LOCK:0.476 ID,INTL,0.018 THK,STL	78189	1222-01
					(END ATTACHING PARTS)		
-23	131-0771-00			1	CONN,RCPT,ELEC:2 MALE,2 FEM,PNL MT W/O MTG HDW	91836	1904-2M58
					(ATTACHING PARTS)		
-24	220-0551-00			1	NUT,PLAIN,HEX:9 MM X 1.00,BRS NP	73743	ORDER BY DESCR
					(END ATTACHING PARTS)		
-25	----- -----			2	TERMN,COAXIAL:(SEE P16,P18 REPL)		
					(ATTACHING PARTS)		
-26	220-0531-02			3	NUT,PLAIN,HEX:0.25-36 X 0.312 HEX,BRS NP	80009	220-0531-02
	210-0940-00			1	WASHER,FLAT:0.25 ID X 0.375 OD X 0.02,STL	12327	ORDER BY DESCR
					(USED ON CALIBRATOR OUT CONNECTOR)		
					(END ATTACHING PARTS)		
-27	366-0670-00			1	SHELL,KNOB:SILVER GRAY	80009	366-0670-00
-28	366-0685-00			2	SHELL,KNOB:SILVER GRAY	80009	366-0685-00
-29	260-2412-00			1	SWITCH ASSEMBLY:OPTICAL,ROTARY,256 POS	50434	QEDS-7189
					(ATTACHING PARTS)		
-30	210-0590-00			1	NUT,PLAIN,HEX:0.375-32 X 0.438 BRS CD PL	73743	28269-402
-31	210-0012-00			1	WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL	09772	ORDER BY DESCR
					(END ATTACHING PARTS)		
-32	214-2617-00			2	SPRING,GROUND:0.248 ID,COPPER BERYLLIUM	80009	214-2617-00
-33	386-5824-00			1	PLATE,CONNECTOR:ALUMINUM	80009	386-5824-00
-34	131-2343-00			3	CONN,RCPT,ELEC:SMA,DOUBLE FEMALE	16179	2084-3202-02
-35	174-0381-00			1	CA ASSY,SP,ELEC:2,26 AWG,4.0 L,RIBBON	80009	174-0381-00
-36	119-3557-00			1	FILTER ASSEMBLY:FRONT PANEL	80009	119-3557-00
					(ATTACHING PARTS)		
-37	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-38	----- -----			1	ATTENUATOR:33GHZ-70DB(SEE A10 REPL)		
					(ATTACHING PARTS)		
-39	131-4328-00			1	CONN,RCPT,ELEC:THREADED,SMA,FEMALE	93459	7005-1
-40	210-0579-00			1	NUT,PLAIN,HEX:0.625-24 X 0.75,BRS CD PL	73743	48046-402
-41	210-0049-00			1	WASHER,LOCK:0.65 ID INTL,0.022 THK,STL	77900	128-02-00-0541C
					(END ATTACHING PARTS)		
-42	333-3313-00			1	PANEL,FRONT:	80009	333-3313-00
-43	260-2317-00			1	SWITCH ASSEMBLY:W/2 BEZELS	80009	260-2317-00
-44	260-2461-00			1	SWITCH ASSEMBLY:ELASTOMER KEYPAD	80009	260-2461-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-45	----- -----			1	CKT BOARD ASSY:FRONT PANEL #2 (SEE A2A2 REPL) (ATTACHING PARTS)		
-46	211-0408-00			14	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX (END ATTACHING PARTS)	93907	ORDER BY DESCR
-47	----- -----			1	CKT BOARD ASSY:FRONT PANEL #1 (SEE A2A1 REPL) (ATTACHING PARTS)		
-48	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX (END ATTACHING PARTS)	93907	ORDER BY DESCR
-49	337-3308-00			1	SHIELD,CRT: (ATTACHING PARTS)	80009	337-3308-00
-50	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX (END ATTACHING PARTS)	93907	ORDER BY DESCR
-51	343-1370-00			1	CLAMP,CABLE:1.27 L,PLASTIC	80009	343-1370-00
-52	348-0762-00			1	GROMMET,PLASTIC:NATURAL,ROUND,0.54 ID	TK1302	ORDER BY DESCR
-53	174-0382-00			1	CA ASSY,SP,ELEC:6,26 AWG,13.25 L,RIBBON	80009	174-0382-00
-54	348-0085-00			2	GROMMET,PLASTIC:GRAY,U-SHAPE,0.48 ID	80009	348-0085-00

FIG. 2 FRONT PANEL & CRT
SHT. 1 OF 2



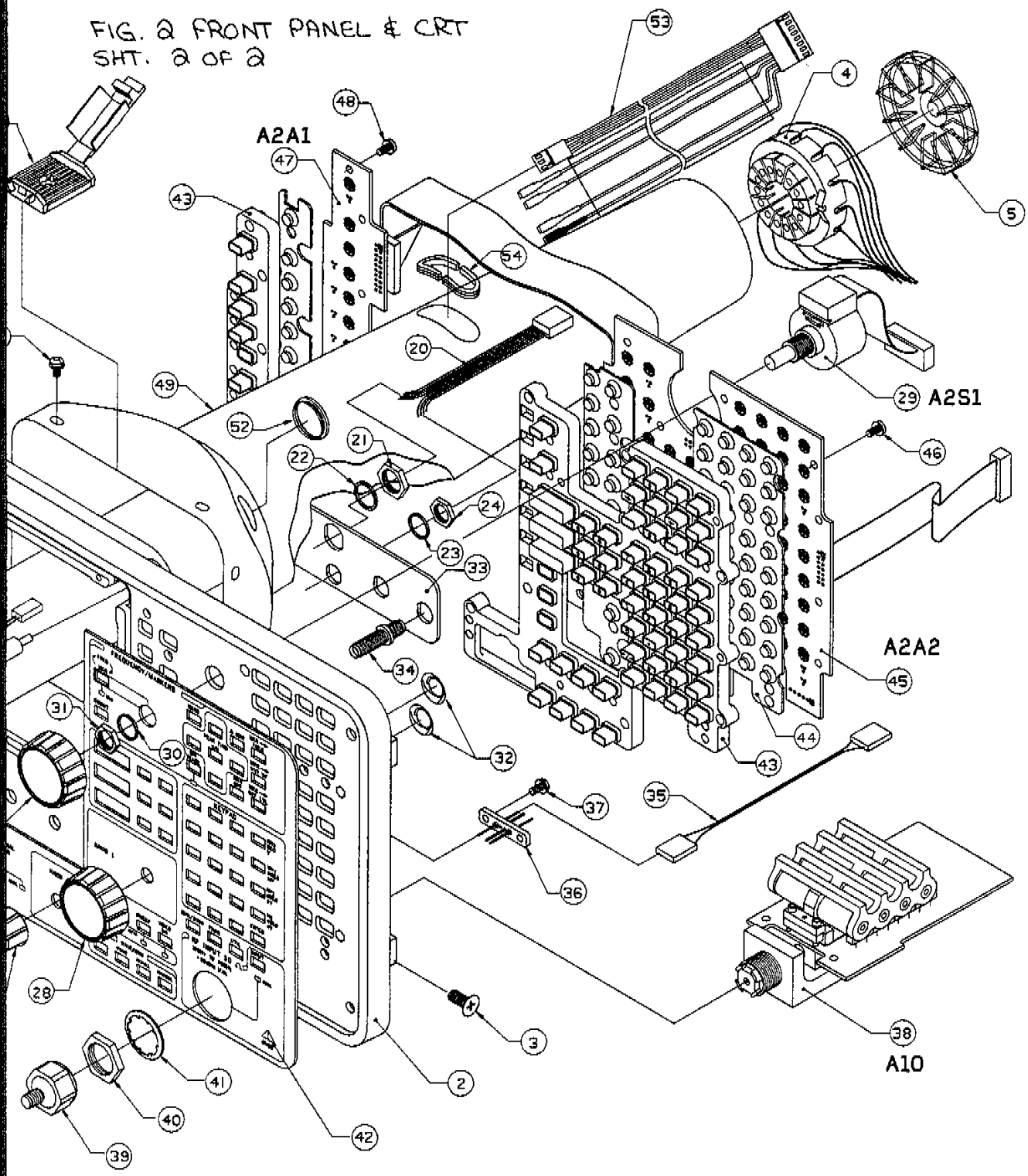


FIG. 2 FRONT PANEL AND CRT

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-	----- -----			1	POWER SUPPLY:(SEE A5 REPL)		
					(ATTACHING PARTS)		
-1	212-0650-00			4	SCREW,MACHINE:10-32 X 0.437,FLH,100 DEG,SST	83486	ORDER BY DESCR
-2	211-0734-00			3	SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
					POWER SUPPLY INCLUDES:		
-3	426-2148-00			1	.FRAME SECTION:REAR PANEL	80009	426-2148-00
-4	334-6977-00			1	.MARKER,IDENT:POLYCARBONATE FILM,REAR PNL,LO	80009	334-6977-00
					.WER		
-5	----- -----			1	.CKT BD ASSY:REAR PANEL BNC(SEE A5A7 REPL)		
					(ATTACHING PARTS)		
-6	210-1039-00			5	.WASHER,LOCK:0.521 ID,INT,0.025 THK,SST	24931	ORDER BY DESCR
-7	220-0497-00			5	.NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
					(END ATTACHING PARTS)		
-8	334-6978-00			1	.MARKER,IDENT:POLYCARBONATE FILM,REAR PNL,UP	80009	334-6978-00
					.PER		
-9	----- -----			1	.CABLE ASSY,RF(SEE A5W516 REPL)		
-10	131-4293-00			1	.CONN,RCPT,ELEC:PANEL MOUNT,SMB	98291	51-075-0000
-11	----- -----			1	.CKT BD ASSY:COMM INTERFACE(SEE A5A6 REPL)		
					(ATTACHING PARTS)		
-12	020-1612-00			2	.ACCESSORY KIT:W/BRACKET & SCREWS	80009	020-1612-00
-13	131-0890-01			4	.LOCK,CONNECTOR:4-40 X 0.312 L,HEX HD,STL	00779	205818-2
-14	211-0408-00			2	.SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-15	342-0891-00			1	.INSULATOR:POWER SUPPLY	80009	342-0891-00
-16	----- -----			1	.FILTER ASSY:EMI(SEE A5FL500 REPL)		
					(ATTACHING PARTS)		
-17	211-0409-00			2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
-18	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					(END ATTACHING PARTS)		
-19	342-0798-00			1	.INSUL,PWR SPLY:POLYESTER	80009	342-0798-00
-20	----- -----			1	.CKT BD ASSY:PRIMARY POWER SUPPLY		
					.(SEE A5A1 REPL)		
					(ATTACHING PARTS)		
-21	211-0302-00			7	.SCR,ASSEM WSHR:4-40 X 0.75,PNH,STL,TORX DR	01536	ORDER BY DESCR
					(END ATTACHING PARTS)		
-22	----- -----			1	.CKT BD ASSY:SECONDARY POWER SUPPLY		
					.(SEE A5A2 REPL)		
					(ATTACHING PARTS)		
-23	211-0408-00			4	.SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	----- -----			1	.FAN,TUBEAXIAL:(SEE A5B100 REPL)		
					(ATTACHING PARTS)		
-25	211-0702-00			4	.SCREW,CAP:6-32 X 0.375,HEX SKT,SST	TK0433	ORDER BY DESCR
-26	210-0457-00			4	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	78189	511-061800-00
					(END ATTACHING PARTS)		
-27	378-2049-00			1	.GRILLE,FAN:3.07 DIA	39766	ORDER BY DESCR
-28	441-1735-01			1	.CHAS,PWR SUPPLY:ALUMINUM	80009	441-1735-01
					(ATTACHING PARTS)		
-29	211-0734-00			4	.SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		

FIG. 3 PWR. SUPPLY ASSY.
SHT. 1 OF 2

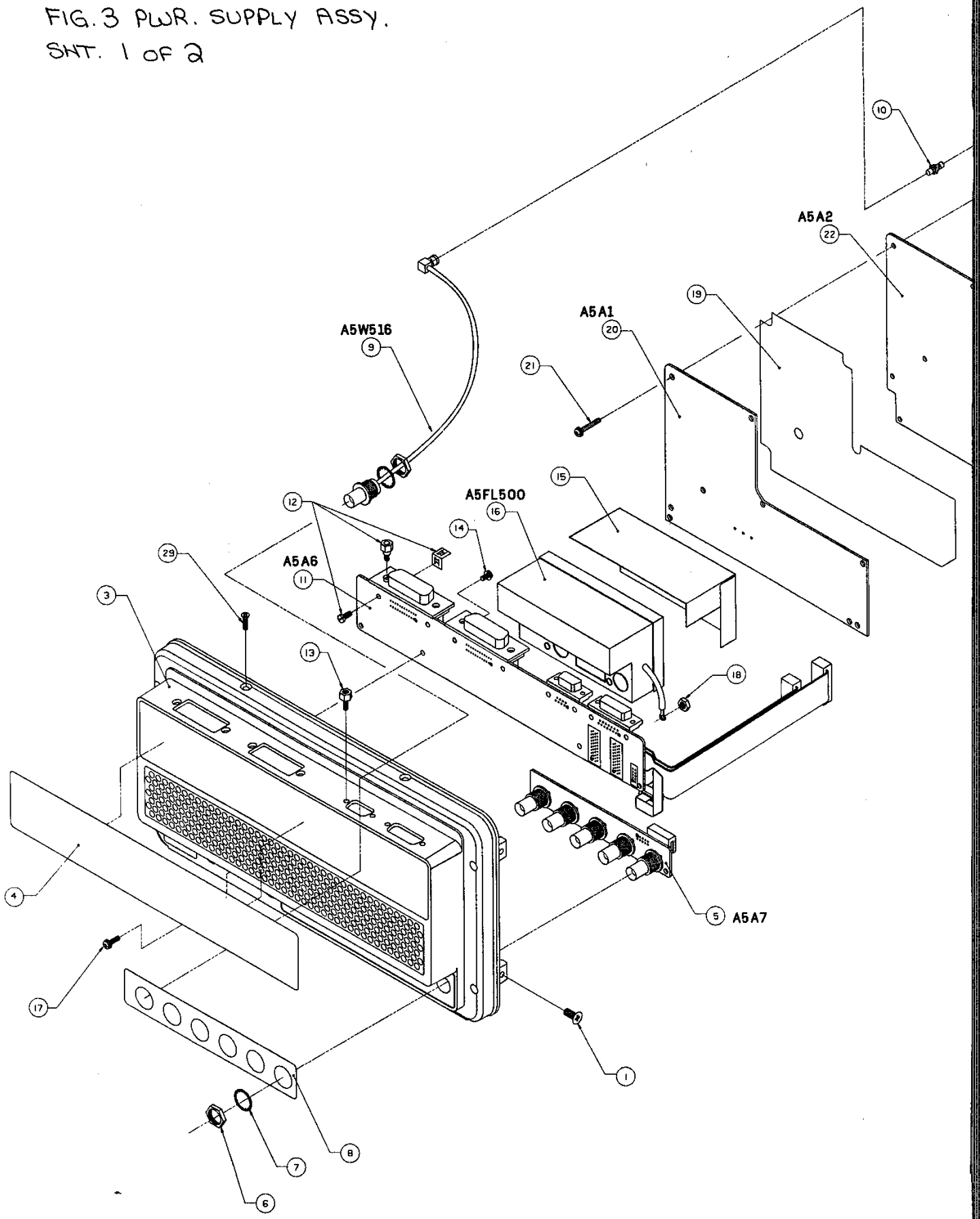


FIG. 3 PWR. SUPPLY ASSY.
SHT. 2 OF 2

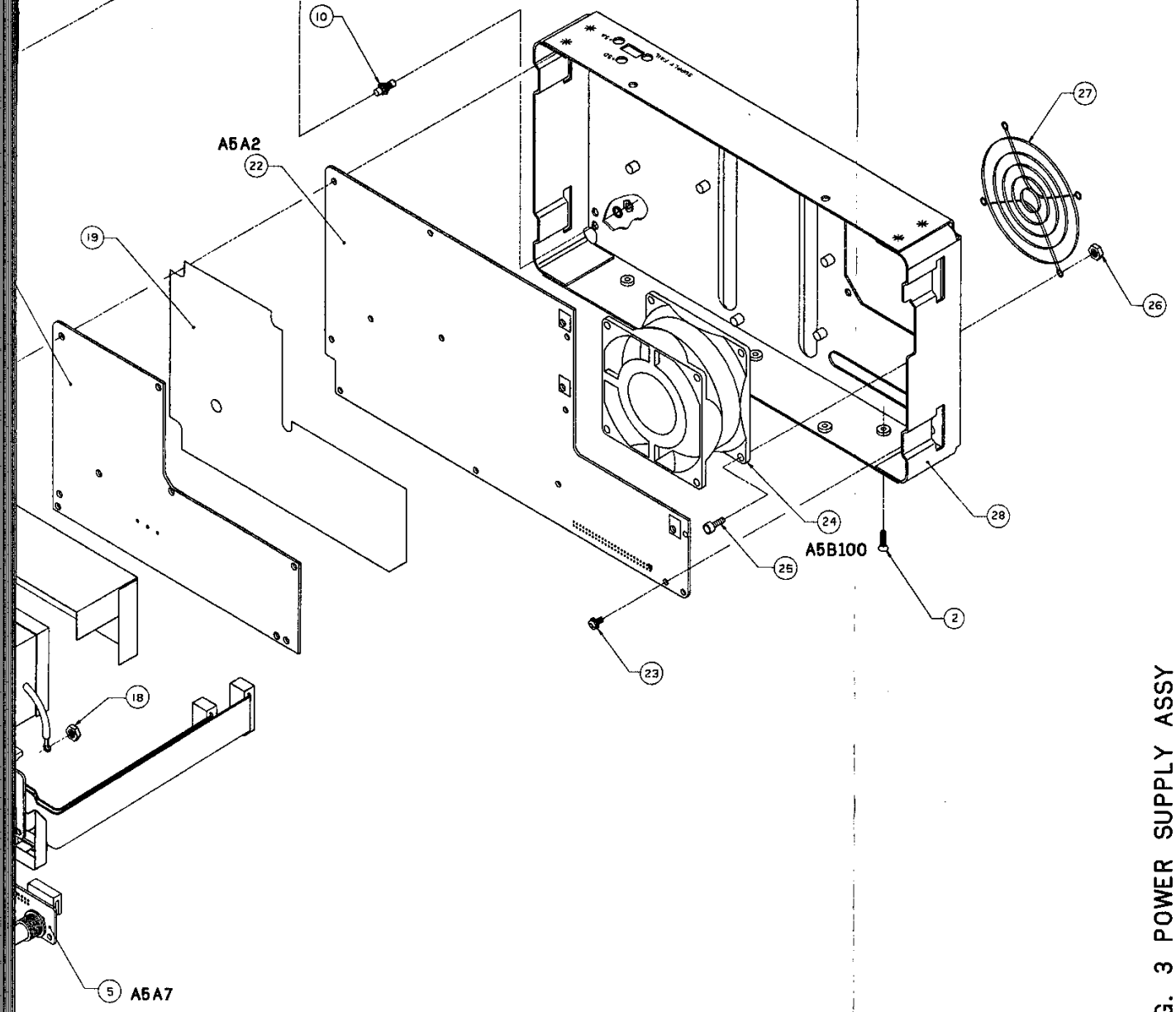


FIG. 3 POWER SUPPLY ASSY

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
4-1	200-3438-01			1	COVER,CARD CAGE:AL,PROCESSOR	80009	200-3438-01
					(ATTACHING PARTS)		
-2	211-0408-00			9	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-3	200-3654-01			1	COVER,CARD CAGE:AL,HIGH VOLTAGE	80009	200-3654-01
					(ATTACHING PARTS)		
-4	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-5	200-3655-01			1	COVER,CARD CAGE:AL,MAIN	80009	200-3655-01
					(ATTACHING PARTS)		
-6	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	----- -----			1	CKT BOARD ASSY:REFERENCE OSCILLATOR		
					(SEE A29 REPL)		
-8	----- -----			1	CKT BOARD ASSY:SWEEP/SPAN ATTENUATOR		
					(SEE A33 REPL)		
-9	----- -----			1	CKT BOARD ASSY:PERIOD COUNTER		
					(SEE A28 REPL)		
-10	----- -----			1	CKT BOARD ASSY:PHASE LOCK,565		
					(SEE A31 REPL)		
-11	----- -----			1	CKT BOARD ASSY:LO MODULE		
					(SEE A25 REPL)		
-12	----- -----			1	CKT BOARD ASSY:LOG PROCESSOR		
					(SEE A18 REPL)		
-13	----- -----			1	CKT BOARD ASSY:DIGITAL VIDEO PROCESSOR		
					(SEE A20 REPL)		
-14	----- -----			1	CKT BOARD ASSY:DIGITAL STORAGE		
					(SEE A24 REPL)		
-15	----- -----			1	CKT BOARD ASSY:DISPLAY AMP		
					(SEE A22 REPL)		
-16	----- -----			1	CKT BOARD ASSY:HIGH VOLTAGE		
					(SEE A23 REPL)		
-17	----- -----			1	CKT BOARD ASSY:MAIN PROCESSOR		
					(SEE A41 REPL)		
-18	----- -----			1	CKT BOARD ASSY;I/O INTERFACE		
					(SEE A42 REPL)		
-19	----- -----			1	CKT BOARD ASSY:MEMORY		
					(SEE A43 REPL)		
-20	441-1736-00			1	CARD CAGE ASSY:ALUMINUM	80009	441-1736-00
					(ATTACHING PARTS)		
-21	211-0408-00			8	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-22	441-1784-01			1	CHAS,CARD CAGE:AL,MAIN	80009	441-1784-01
					(ATTACHING PARTS)		
-23	211-0408-00			19	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	012-1283-00			1	CABLE ASSEMBLY:FLAT FLEX COAX	80009	012-1283-00
-25	----- -----			1	CKT BOARD ASSY:MAIN MOTHER		
					(SEE A1 REPL)		
					(ATTACHING PARTS)		
-26	211-0408-00			3	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-27	441-1748-00			1	CHASSIS,MAIN:ALUMINUM	80009	441-1748-00

FIG. 4 CHASSIS (TOP)
SHT. 1 OF 2

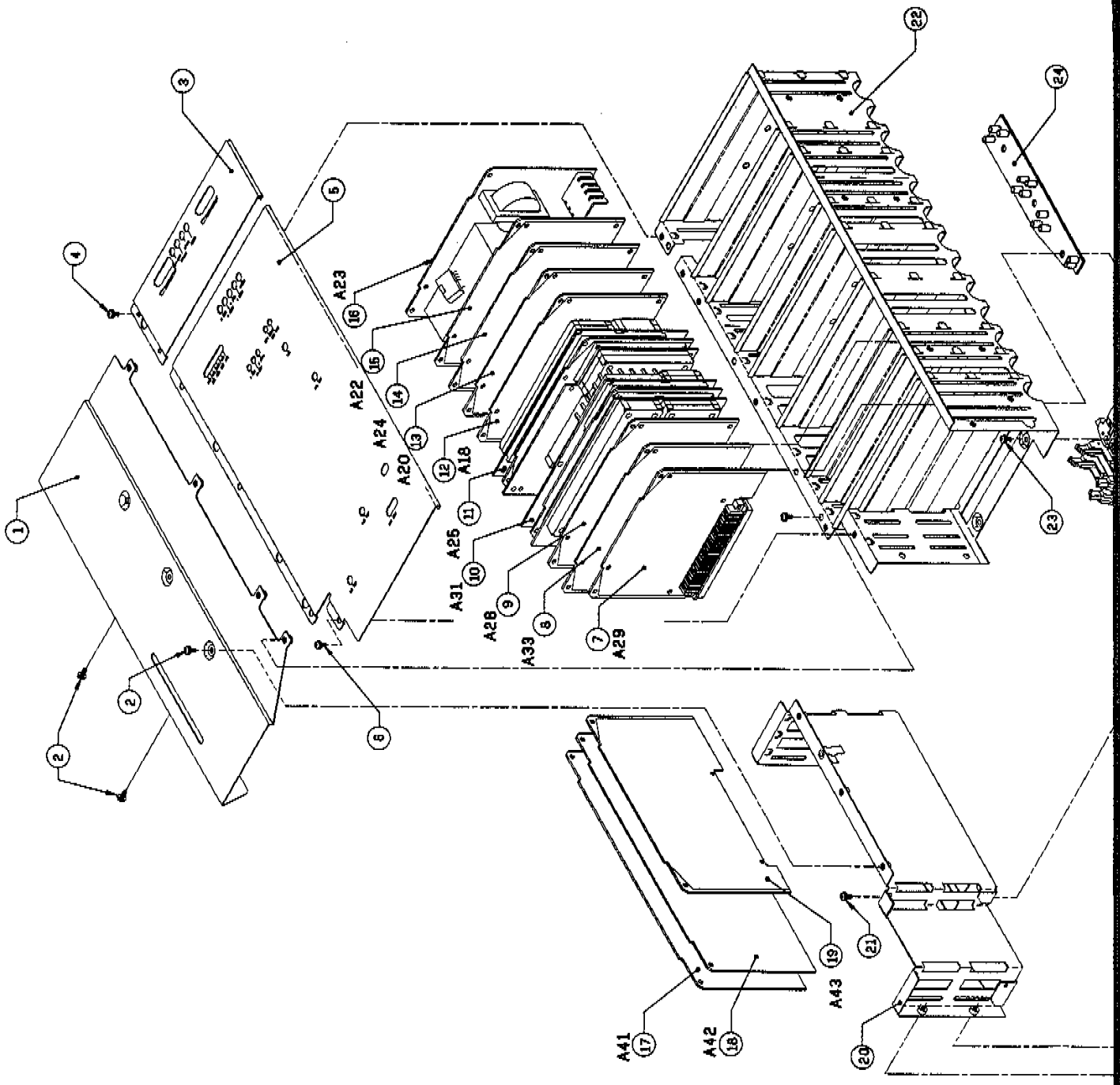


FIG. 4 CHASSIS (TOP)
SHT. 2 OF 2

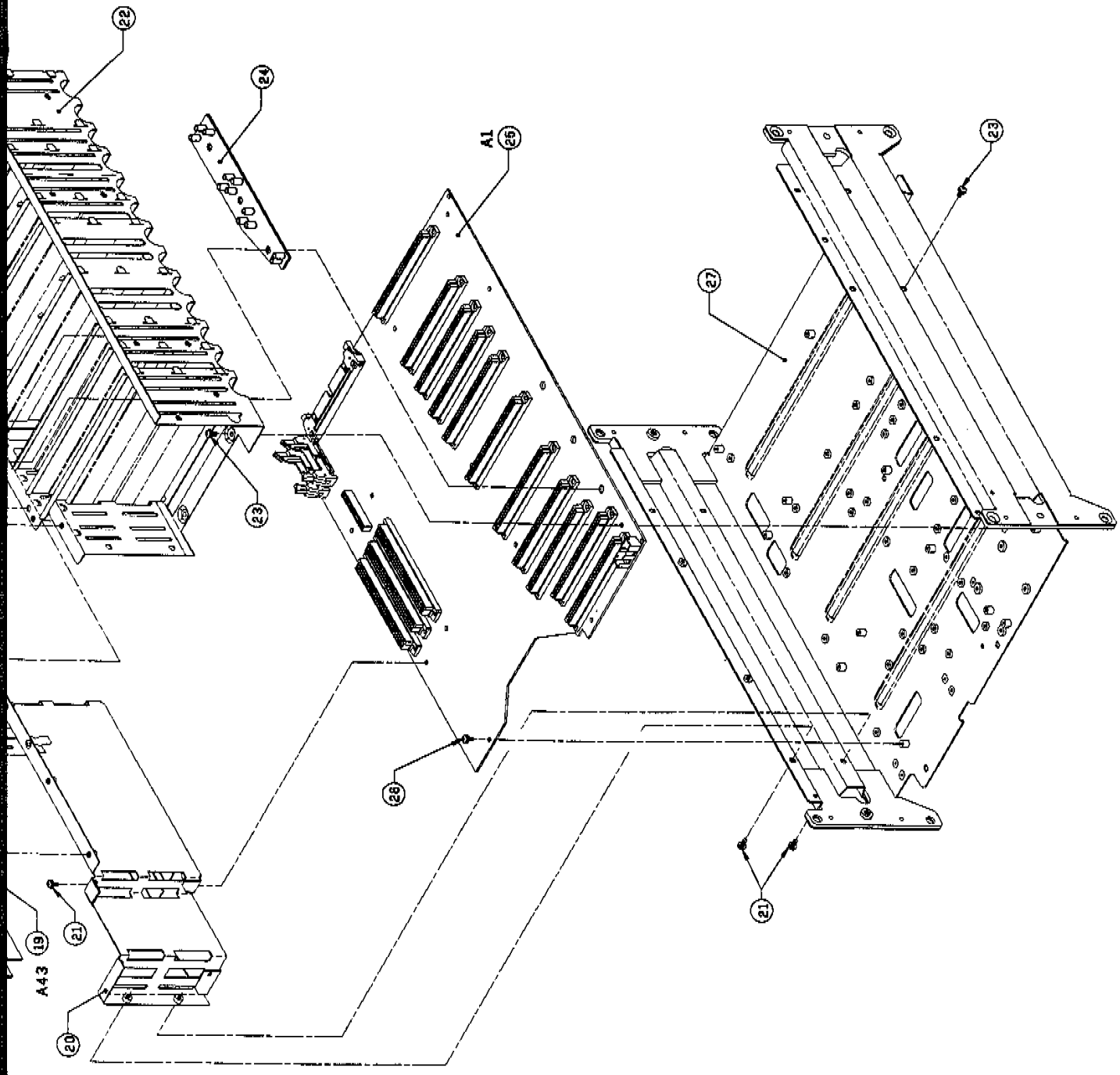
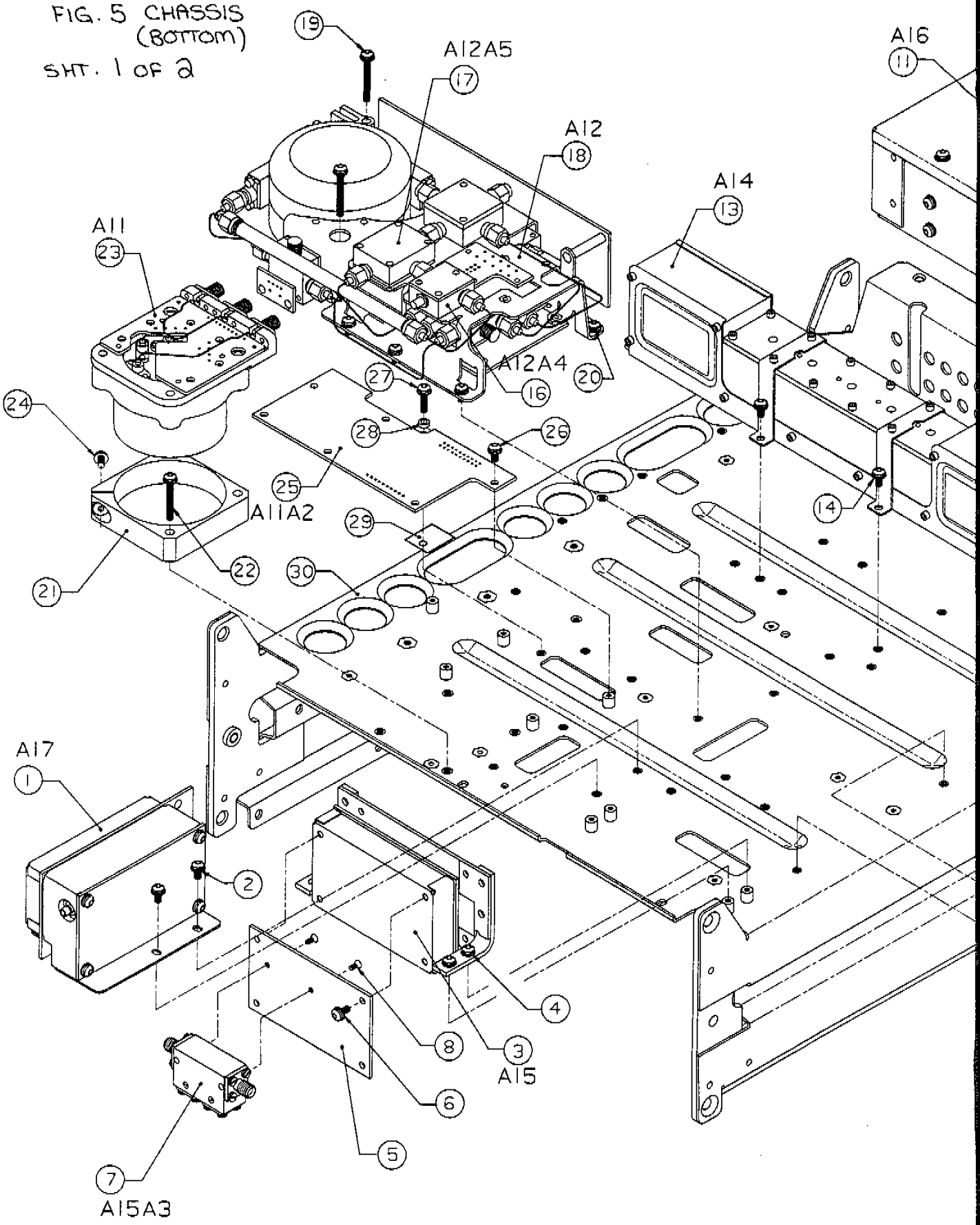


FIG. 4 CHASSIS (TOP)

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
5-1	----- -----			1	PHASELOCK ASSY:MICROWAVE(SEE A17 REPL)		
					(ATTACHING PARTS)		
-2	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-3	----- -----			1	CALIBRATOR ASSY:(SEE A15 REPL)		
					(ATTACHING PARTS)		
-4	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-5	407-3902-00			1	BRACKET,MTG:ALUMINUM	80009	407-3902-00
					(ATTACHING PARTS)		
-6	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	----- -----			1	ISOLATOR,RF:WIDE BAND,8-18GHZ		
					(SEE A15A3 REPL)		
					(ATTACHING PARTS)		
-8	211-0390-00			2	SCREW,MACHINE:2-56 X 0.188,FH,STL CD PL	80009	211-0390-00
					(END ATTACHING PARTS)		
-9	----- -----			1	MICROWAVE IF ASSY:(SEE A13 REPL)		
					(ATTACHING PARTS)		
-10	211-0408-00			6	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-11	----- -----			1	VR ASSEMBLY:(SEE A16 REPL)		
					(ATTACHING PARTS)		
-12	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-13	----- -----			1	INTMD FREQ ASSY:525MHZ(SEE A14 REPL)		
					(ATTACHING PARTS)		
-14	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
-15	211-0409-00			2	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-16	----- -----			1	TERMINATION AS:LOW PASS(SEE A12A4 REPL)		
-17	----- -----			1	MIXER,LOW PASS:(SEE A12A5 REPL)		
-18	----- -----			1	CONVERTER ASSY:(SEE A12 REPL)		
					(ATTACHING PARTS)		
-19	211-0754-00			2	SCR,ASSEM WSHR:6-32 X 1.375,PNH,STL	93907	ORDER BY DESCR
-20	211-0408-00			6	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-21	343-1447-00			1	CLAMP,MTG:YTO,INSTR,ALUMINUM	80009	343-1447-00
					(ATTACHING PARTS)		
-22	211-0732-00			3	SCR,ASSEM WSHR:6-32 X 0.75,PNH,STL,CD PL,TO	TK1543	ORDER BY DESCR
					RX T15		
					(END ATTACHING PARTS)		
-23	----- -----			1	YIG OSC ASSY:(SEE A11 REPL)		
					(ATTACHING PARTS)		
-24	211-0730-00			1	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL CD PL,T	80009	211-0730-00
					ORX T15		
					(END ATTACHING PARTS)		
-25	----- -----			1	CKT BOARD ASSY:YIG OSC DRIVER		
					(SEE A11A2 REPL)		
					(ATTACHING PARTS)		
-26	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
-27	211-0409-00			1	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
-28	210-1291-01			1	WASHER,SHLDR:0.118 ID X 0.202 OD X 0.1 THK	80009	210-1291-01
					(END ATTACHING PARTS)		
-29	342-0563-00			1	INSULATOR,PLATE:TRANSISTOR,FIBERGLASS REINF	18565	69-11-8805-1674
					ORCED SILICON RUBBER		
-30	441-1748-00			1	CHASSIS,MAIN:ALUMINUM	80009	441-1748-00

FIG. 5 CHASSIS (BOTTOM)
SHT. 1 OF 2



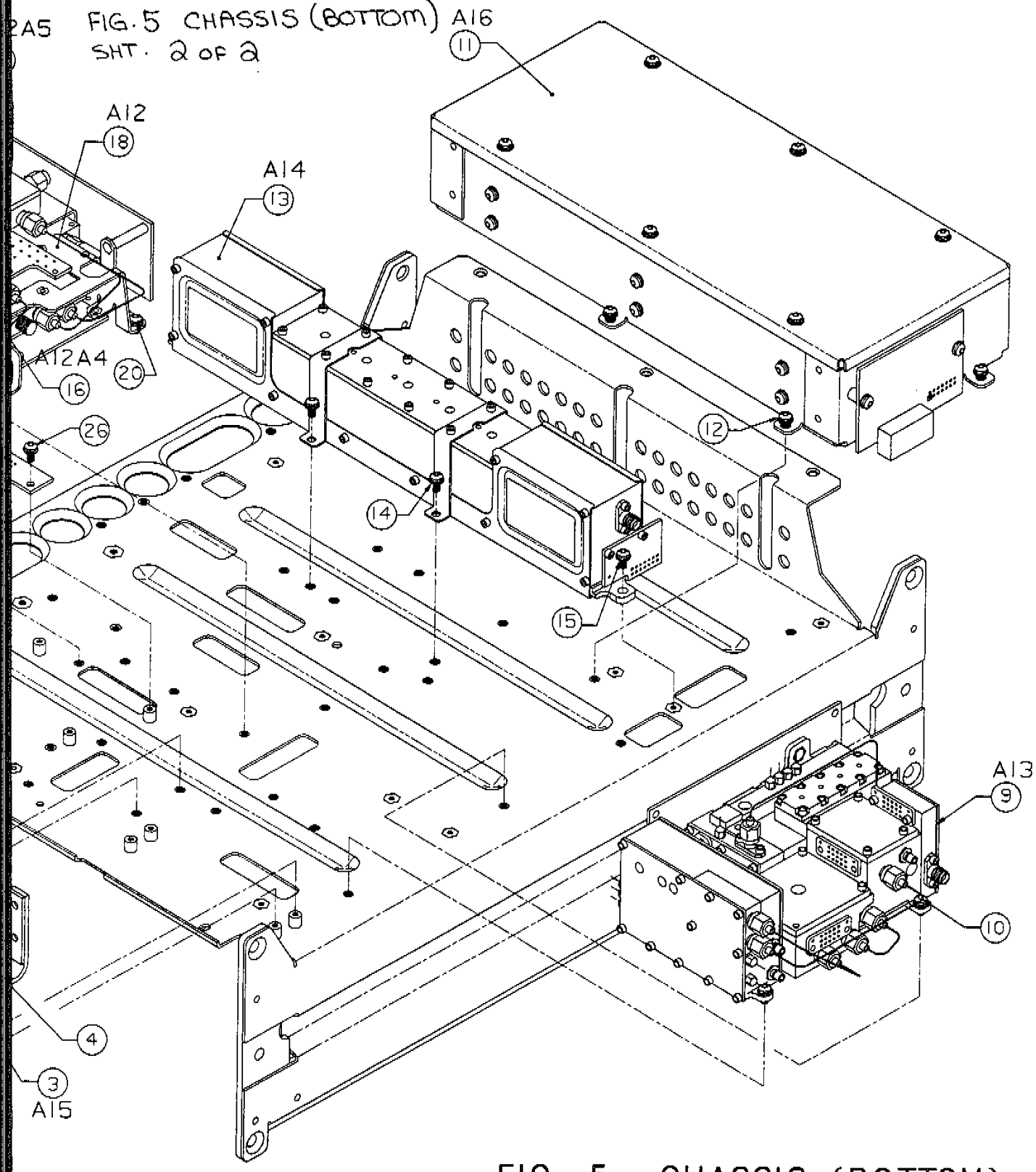


FIG. 5 CHASSIS (BOTTOM)

2782 SERVICE MANUAL

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
6-1	161-0104-00			1	CABLE ASSY,PWR,:3 WIRE,98.0 L,W/RTANG CONN	16428	CH8352, FH-8352
-2	161-0104-06			1	CABLE ASSY,PWR,:3 X 0.75MM SQ,220V,98.0 L (OPTION A1 EUROPEAN ONLY)	S3109	ORDER BY DESCR
-3	161-0104-07			1	CABLE ASSY,PWR,:3 X 0.75MM SQ,240V,98.0 L (OPTION A2 UNITED KINGDOM ONLY)	TK1373	A25UK-RA
-4	161-0135-00			1	CABLE ASSY,PWR,:3,0.75MM SQ,240V,3.05M L (OPTION A3 AUSTRALIAN ONLY)	S3109	SAA/3-0D3CCFC3X0
-5	161-0134-00			1	CABLE ASSY,PWR,:3,18 AWG,240V,120.0 L (OPTION A4 NORTH AMERICAN ONLY)	70903	ORDER BY DESCR
-6	161-0167-00			1	CABLE ASSY,PWR,:3.0 X 0.75,6A,240V,2.5M L (OPTION A5 SWISS ONLY)	S3109	ORDER BY DESCR
-7	012-0649-00			1	CABLE ASSY,RF:50 OHM COAX,28.5 L	19505	80-9902-201
-8	103-0045-00			1	ADAPTER,CONN:N MALE TO BNC FEMALE	24931	29 JP104-3
-9	159-0319-00			2	FUSE,CARTRIDGE:4A,125V,FAST	80009	159-0319-00
	159-0320-00			2	FUSE,CARTRIDGE:4A,250V,FAST (OPTION A1,A2,A3,A4,A5 ONLY)	80009	159-0320-00
-10	131-4329-00			1	CONN,RCPT,ELEC:THREADED,N-TYPE,FEMALE	80009	131-4329-00
	070-6794-00			1	MANUAL,TECH:OPERATORS,2782 ANALYZER	80009	070-6794-00
	070-6795-00			1	MANUAL,TECH:OPERATORS HANDBOOK,2782	80009	070-6795-00
	070-6796-00			1	MANUAL,TECH:PROGRAMMERS W/8566 LANGUAGE	80009	070-6796-00
	070-6798-00			1	MANUAL,TECH:PROGRAMMERS REF GUIDE	80009	070-6798-00
					OPTIONAL ACCESSORIES		
	015-0509-00			1	ADAPTER ASSY:N MALE TO N FEMALE 50 OHM,10KH Z TO 21GHZ,50V	93459	5201
	016-1019-00			1	RACK ADPTR KIT:PORT SPECTRUM ANALYZER	80009	016-1019-00
	070-6799-00			1	MANUAL,TECH:SERVICE,2782 VOLUME I	80009	070-6799-00
	006-7334-00			1	FIELD SVC KIT:2782	80009	006-7334-00
	012-1243-00			1	.CABLE,INTCON:9 PIN MONITOR	80009	012-1243-00
	012-1347-00			1	.CABLE ASSEMBLY:2782 SERVICE KIT,POWER SUPPL .Y	80009	012-1347-00
	013-0260-00			2	.ADAPTER ELEC:PLUG TO JACK	80009	013-0260-00
	015-0599-00			1	.ADAPTER,CONN:9 TO 25 FEMALE	80009	015-0599-00
	174-2013-00			6	.CABLE ASSY,RF:50 OHM COAX,3.1 L	80009	174-2013-00
	376-0243-00			1	.COUPLER:20DB,0.2-250MHZ	80009	376-0243-00
	671-0725-00			1	.CIRCUIT BD ASSY:CARD CAGE EXTENDER	80009	671-0725-00
	671-0726-00			1	.CIRCUIT BD ASSY:MAIN CARD CAGE EXTENDER	80009	671-0726-00
	671-0727-00			1	.CIRCUIT BD ASSY:PROCESSOR EXTENDER	80009	671-0727-00

FIG. 6 ACCESSORIES
SHT. 1 OF 2

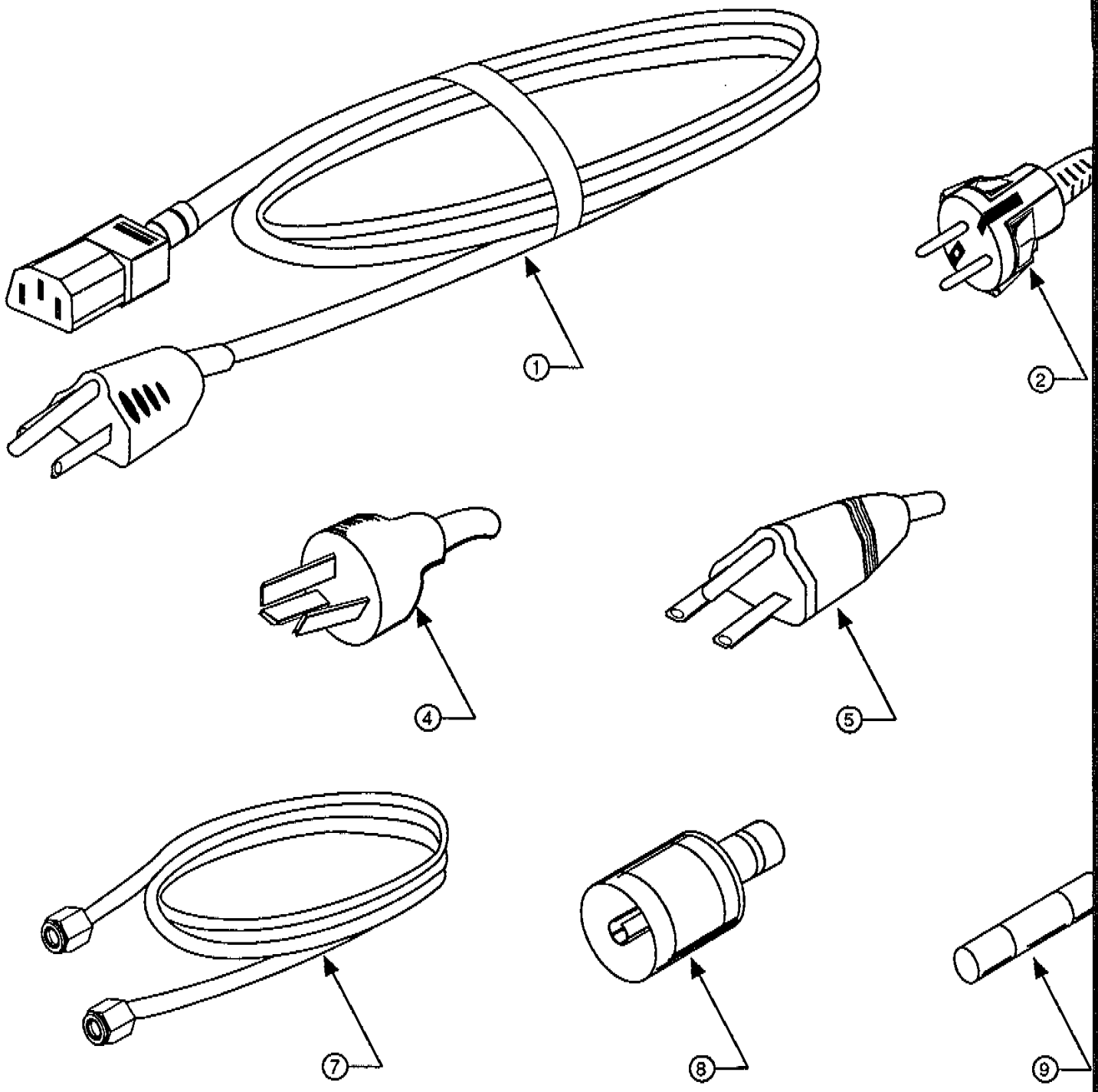


FIG. 6 ACCESSORIES
SHT. 2 OF 2

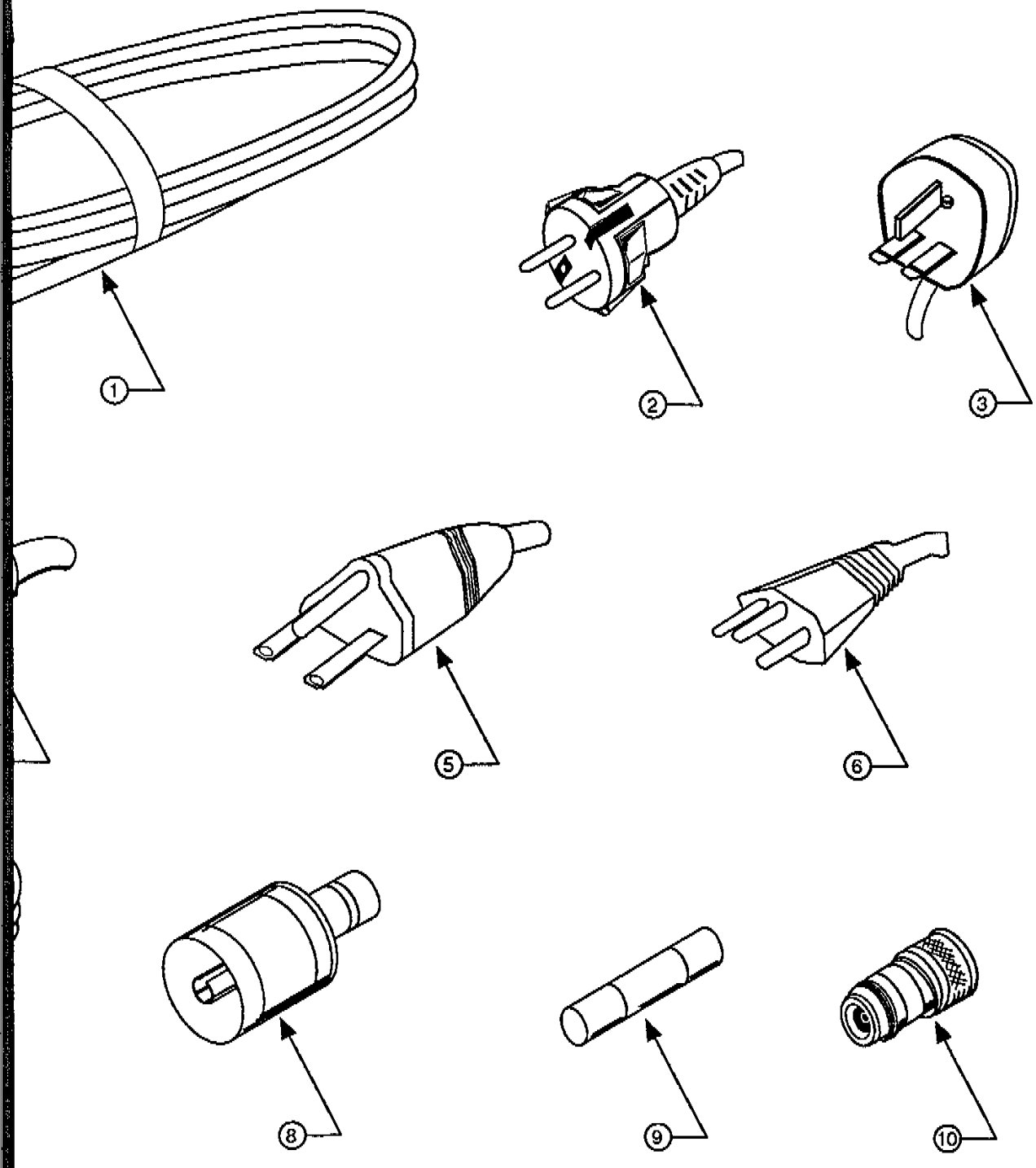


FIG.6 ACCESSORIES

Motherboard Connections

The following information is a copy of the engineering documentation for the 2782 Motherboard connections. This describes the individual conductors, including the signal sources and destinations, and diagrams showing the pinout and location of the motherboard connector for each module.

There are references in this documentation to part numbers and project code names. Use only the part numbers located in the Replaceable Electrical and Mechanical Parts Lists. Where the code name "Jupiter" appears, the information does not apply to this instrument. Where the code name "Saturn" appears, or where there is no code name, the information does apply to this instrument.

CONTENTS

1. CONDUCTOR DEFINITIONS

1.1 +10V

SOURCE : LV POWER SUPPLY A12,B12

DESCRIPTION : +10V supply (+/- 1.5% tolerance)

DESTINATION(S) :

SPARE	A16,B16
REFERENCE OSC.	A16,B16
HIGH VOLTAGE	A16,B16
DISPLAY AMPLIFIERS	A16,B16
DIGITAL STORAGE	A16,B16
VIDEO PROCESSOR	A16,B16
LOG PROCESSOR	A16,B16
LO MODULE	A16,B16
565 SYNTHESIZER	A16,B16
PERIOD COUNTER	A16,B16
SWEEP/SPAN ATTEN.	A16,B16
SATURN CALIBRATOR	B3
SATURN 1ST LO	B5
SATURN MTX CONTROL	A10,B10
SATURN PRESEL DRVR	A5
MICROWAVE IF	B1

1.2 +10VREF

SOURCE : SWEEP/SPAN ATTEN. B27

DESCRIPTION : +10V reference

DESTINATION(S) :

SPARE	B27
REFERENCE OSC.	B27
HIGH VOLTAGE	B27
DISPLAY AMPLIFIERS	B27
DIGITAL STORAGE	B27
VIDEO PROCESSOR	B27
LOG PROCESSOR	B27
LO MODULE	B27
565 SYNTHESIZER	B27
PERIOD COUNTER	B27
SATURN CALIBRATOR	B5
SATURN MTX CONTROL	A5
VR ASSEMBLY	A1
MICROWAVE IF	B9

1.3 +10VRRET

SOURCE : SWEEP/SPAN ATTEN. A27

DESCRIPTION : +10V reference return

DESTINATION(S) :

SPARE	A27
REFERENCE OSC.	A27
HIGH VOLTAGE	A27
DISPLAY AMPLIFIERS	A27
DIGITAL STORAGE	A27
VIDEO PROCESSOR	A27
LOG PROCESSOR	A27
LO MODULE	A27
565 SYNTHESIZER	A27
PERIOD COUNTER	A27
SATURN CALIBRATOR	A5
SATURN MTX CONTROL	B5
VR ASSEMBLY	A3
MICROWAVE IF	B10

1.4 +15V

SOURCE : LV POWER SUPPLY A10,A11,B11

DESCRIPTION : +15V supply (+/- 2% tolerance)

DESTINATION(S) :

FRONT PANEL	A7
SPARE	A26,B26
REFERENCE OSC.	A26,B26
HIGH VOLTAGE	A26,B26
DISPLAY AMPLIFIERS	A26,B26
DIGITAL STORAGE	A26,B26
VIDEO PROCESSOR	A26,B26
LOG PROCESSOR	A26,B26
LO MODULE	A26,B26
565 SYNTHESIZER	A26,B26
PERIOD COUNTER	A26,B26
SWEEP/SPAN ATTEN.	A26,B26
JUPITER 1ST CONVERTER	B3
SATURN CALIBRATOR	B4
SATURN 1ST LO	A4
MICROWAVE PHASE-LOCK	B6
SATURN MTX CONTROL	A6
VR ASSEMBLY	B1
SATURN PRESEL DRVR	A4
MICROWAVE IF	A6,B6
525 IF	B3

1.5 +18VS

SOURCE : LV POWER SUPPLY A21

DESCRIPTION : +18V standby supply (+15%, -5% tolerance)

DESTINATION(S) :

REFERENCE OSC.	B21

1.6 +45V

SOURCE : LV POWER SUPPLY B21

DESCRIPTION : +45V supply (+/- 5% tolerance)

DESTINATION(S) :

SPARE	A15,B15
REFERENCE OSC.	A15,B15
HIGH VOLTAGE	A15,B15
DISPLAY AMPLIFIERS	A15,B15
DIGITAL STORAGE	A15,B15
VIDEO PROCESSOR	A15,B15
LOG PROCESSOR	A15,B15
LO MODULE	A15,B15
565 SYNTHESIZER	A15,B15
PERIOD COUNTER	A15,B15
SWEEP/SPAN ATTEN.	A15,B15

1.7 +5VA

SOURCE : LV POWER SUPPLY A15,B15

DESCRIPTION : +5V analog supply (+/- 1% tolerance)

DESTINATION(S) :

SPARE	A28,B28
REFERENCE OSC.	A28,B28
HIGH VOLTAGE	A28,B28
DISPLAY AMPLIFIERS	A28,B28
DIGITAL STORAGE	A28,B28
VIDEO PROCESSOR	A28,B28
LOG PROCESSOR	A28,B28
LO MODULE	A28,B28
565 SYNTHESIZER	A28,B28
PERIOD COUNTER	A28,B28
SWEEP/SPAN ATTEN.	A28,B28
JUPITER 1ST CONVERTER	A7

SATURN CALIBRATOR	B6
SATURN 1ST LO	A3
MICROWAVE PHASE-LOCK	A4
SATURN MTX CONTROL	A4,B4
VR ASSEMBLY	B2
SATURN PRESEL DRVR	A3
MICROWAVE IF	B5

1.8 +5VAsens

SOURCE : LV POWER SUPPLY B16

DESCRIPTION : +5V analog supply sense line

1.9 +5VD

SOURCE : LV POWER SUPPLY A22,A23,A24,A25

DESCRIPTION : +5V digital supply (+/- 4% tolerance)

DESTINATION(S) :

FRONT PANEL	A1
SPARE	A32,B32
REFERENCE OSC.	A32,B32
HIGH VOLTAGE	A32,B32
DISPLAY AMPLIFIERS	A32,B32
DIGITAL STORAGE	A32,B32
VIDEO PROCESSOR	A32,B32
LOG PROCESSOR	A32,B32
LO MODULE	A32,B32
565 SYNTHESIZER	A32,B32
PERIOD COUNTER	A32,B32
SWEEP/SPAN ATTEN.	A32,B32
PROCESSOR SPARE	C32
I/O INTERFACE 1	C32
MAIN PROCESSOR	C32
SATURN CALIBRATOR	B10
SATURN 1ST LO	A1
MICROWAVE PHASE-LOCK	B1
SATURN MTX CONTROL	B1
SATURN PRESEL DRVR	A1
MICROWAVE IF	A1

1.10 +5VS

SOURCE : LV POWER SUPPLY B1,B2,B3,B4

DESCRIPTION : +5V standby supply (+/- 1.5% tolerance)

DESTINATION(S) :

FRONT PANEL	B5
PROCESSOR SPARE	A32,B32,C10
I/O INTERFACE 1	A32,B32,C10
COMM INTERFACE 2	35,36
MAIN PROCESSOR	A32,B32,C10
COMM INTERFACE 1	17,18,19

1.11 +95V

SOURCE : LV POWER SUPPLY B9

DESCRIPTION : +95V supply; used only in the High Voltage and Display Amplifiers Modules. (+ 3%, -5% tolerance)

DESTINATION(S) :

HIGH VOLTAGE	A1
DISPLAY AMPLIFIERS	A1

1.12 +MTXV

SOURCE : LV POWER SUPPLY A5

DESCRIPTION : Processor variable voltage supply used by the preselector in the Saturn Preselector Driver module. Nominal values are 0, 18V,26V and 32V. (+/- 7% tolerance)

DESTINATION(S) :

SATURN PRESEL DRVR	B6

1.13 +OSCV

SOURCE : LV POWER SUPPLY B5

DESCRIPTION : Processor variable voltage supply used in the Saturn 1st LO module. Nominal values are 18V and 26V. (+/- 7% tolerance)

DESTINATION(S) :

SATURN 1ST LO	B6

1.14 -15V

SOURCE : LV POWER SUPPLY A16

DESCRIPTION : -15V supply (+/- 2% tolerance)

DESTINATION(S) :

FRONT PANEL	A6
SPARE	A23,B23
REFERENCE OSC.	A23,B23
HIGH VOLTAGE	A23,B23
DISPLAY AMPLIFIERS	A23,B23
DIGITAL STORAGE	A23,B23
VIDEO PROCESSOR	A23,B23
LOG PROCESSOR	A23,B23
LO MODULE	A23,B23
565 SYNTHESIZER	A23,B23
PERIOD COUNTER	A23,B23
SWEEP/SPAN ATTEN.	A23,B23
JUPITER 1ST CONVERTER	B7
SATURN CALIBRATOR	A4
SATURN 1ST LO	A8
MICROWAVE PHASE-LOCK	A6
SATURN MTX CONTROL	A7
VR ASSEMBLY	B7
SATURN PRESEL DRVR	B5
MICROWAVE IF	A8,B8

1.15 -5.2sens

SOURCE : LV POWER SUPPLY B13

DESCRIPTION : -5.2V supply sense line

1.16 -5.2V

SOURCE : LV POWER SUPPLY A14,B14

DESCRIPTION : -5.2V supply (+/- 1% tolerance)

DESTINATION(S) :

FRONT PANEL	B6
SPARE	A20,B20
REFERENCE OSC.	A20,B20
HIGH VOLTAGE	A20,B20
DISPLAY AMPLIFIERS	A20,B20
DIGITAL STORAGE	A20,B20
VIDEO PROCESSOR	A20,B20
LOG PROCESSOR	A20,B20
LO MODULE	A20,B20

565 SYNTHESIZER	A20,B20
PERIOD COUNTER	A20,B20
SWEEP/SPAN ATTEN.	A20,B20
SATURN CALIBRATOR	A3
SATURN 1ST LO	B4
MICROWAVE PHASE-LOCK	A3
SATURN MTX CONTROL	B7
SATURN PRESEL DRVR	B4
MICROWAVE IF	A9

1.17 -8V

SOURCE : LV POWER SUPPLY A19,B19

DESCRIPTION : -8V supply (+/- 1.5% tolerance)

DESTINATION(S) :

SPARE	A4,B4
FRONT PANEL	A5
REFERENCE OSC.	A4,B4
HIGH VOLTAGE	A4,B4
DISPLAY AMPLIFIERS	A4,B4
DIGITAL STORAGE	A4,B4
VIDEO PROCESSOR	A4,B4
LOG PROCESSOR	A4,B4
LO MODULE	A4,B4
565 SYNTHESIZER	A4,B4
PERIOD COUNTER	A4,B4
SWEEP/SPAN ATTEN.	A4,B4
JUPITER 1ST CONVERTER	B5
SATURN CALIBRATOR	A2
SATURN 1ST LO	B8
VR ASSEMBLY	B6
SATURN PRESEL DRVR	B3
MICROWAVE IF	A10

1.18 /ACGONE

SOURCE : LV POWER SUPPLY A8

DESCRIPTION : A control line which gives warning of imminent departure of the power supplies due to the loss of the AC line voltage.

DESTINATION(S) :

PROCESSOR SPARE	C30
I/O INTERFACE 1	C30
MAIN PROCESSOR	C30

1.19 /ATEST

SOURCE : MAIN PROCESSOR B12

DESCRIPTION : (TTL) This signal is used to disable the memory and ROM during processor self-test.

DESTINATION(S) :

PROCESSOR SPARE	B12
I/O INTERFACE 1	B12

1.20 /BDDIR

SOURCE : I/O INTERFACE 2 A7

DESCRIPTION : (TTL) Buffered Data DIRection signal: This signal indicates the direction of data flow to/from the communications interface. HIGH => from the comm. interface, and LOW => to the comm. interface.

DESTINATION(S) :

COMM INTERFACE 1	39

1.21 /BDMAAK1

SOURCE : I/O INTERFACE 2 B2

DESCRIPTION : (TTL) Buffered DMA AcKnowledge signal from processor to peripheral (GPIB0) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

COMM INTERFACE 1	4

1.22 /BDMAAK2

SOURCE : I/O INTERFACE 2 A2

DESCRIPTION : (TTL) Buffered DMA AcKnowledge signal from processor to peripheral (GPIB1) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

COMM INTERFACE 1	5

1.23 /BEIORD

SOURCE : I/O INTERFACE 2 A8

DESCRIPTION : (TTL) Buffered External IO ReaD signal to the communications interface (active LOW).

DESTINATION(S) :

COMM INTERFACE 1 38

1.24 /BEIOWR

SOURCE : I/O INTERFACE 2 B8

DESCRIPTION : (TTL) Buffered External IO WRite signal to the communications interface (active LOW).

DESTINATION(S) :

COMM INTERFACE 1 37

1.25 /CLAMP

SOURCE : LOG PROCESSOR B7

DESCRIPTION : (TTL) This active low signal causes the video processor to clamp the display to the baseline when the sweep is outside the frequency scan range of the instrument.

DESTINATION(S) :

VIDEO PROCESSOR B7

1.26 /COMSEL

SOURCE : I/O INTERFACE 2 A4

DESCRIPTION : (TTL) Communications interface select signal (Active LOW). When active, the I/O devices on the communications interface are selected and can transfer data to/from the main processor.

DESTINATION(S) :

COMM INTERFACE 1 9

1.27 /DIGINH

SOURCE : DISPLAY AMPLIFIERS A7

DESCRIPTION : (TTL) This signal is generated in the "display sequencer" IC and is used to disable the vector generator on the Digital Storage board.

DESTINATION(S) :

DIGITAL STORAGE	A7

1.28 /EDMAAK0

SOURCE : MAIN PROCESSOR C20

DESCRIPTION : (TTL) DMA AcKnowledge from processor to peripheral (Instrument Serial Bus) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

PROCESSOR SPARE	C20
I/O INTERFACE 1	C20

1.29 /EDMAAK1

SOURCE : MAIN PROCESSOR A21

DESCRIPTION : (TTL) DMA AcKnowledge from processor to peripheral (GPIB0) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

PROCESSOR SPARE	A21
I/O INTERFACE 1	A21

1.30 /EDMAAK2

SOURCE : MAIN PROCESSOR B21

DESCRIPTION : (TTL) DMA AcKnowledge from processor to peripheral (GPIB1) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

PROCESSOR SPARE	B21
I/O INTERFACE 1	B21

1.31 /EDMAAK3

SOURCE : MAIN PROCESSOR C21

DESCRIPTION : (TTL) DMA AcKnowledge from processor to peripheral (High Speed Serial Bus) which allows the peripheral to proceed with the programmed operation.

DESTINATION(S) :

PROCESSOR SPARE	C21
I/O INTERFACE 1	C21

1.32 /EDMARQ1

SOURCE : COMM INTERFACE 1 2

DESCRIPTION : (TTL) DMA ReQuest #1 from communications interface (Active LOW)

DESTINATION(S) :

I/O INTERFACE 2	B1

1.33 /EDMARQ2

SOURCE : COMM INTERFACE 1 3

DESCRIPTION : (TTL) DMA ReQuest #2 from communications interface (Active LOW)

DESTINATION(S) :

I/O INTERFACE 2	A1

1.34 /EINTP3

SOURCE : COMM INTERFACE 1 7

DESCRIPTION : (TTL) Inverted (active LOW) processor interrupt 3 (GPIB0)

DESTINATION(S) :

I/O INTERFACE 2	A3

1.35 /EINTP4

SOURCE : COMM INTERFACE 1 6

DESCRIPTION : (TTL) Inverted (active LOW) processor interrupt 4 (GPIB1)

DESTINATION(S) :

I/O INTERFACE 2	B3

1.36 /EIORD

SOURCE : MAIN PROCESSOR B19

DESCRIPTION : (TTL) This signal indicates an IO read cycle (active LOW).

DESTINATION(S) :

PROCESSOR SPARE	B19
I/O INTERFACE 1	B19

1.37 /EIOWR

SOURCE : MAIN PROCESSOR B20

DESCRIPTION : (TTL) This signal indicates an IO write cycle (active LOW).

DESTINATION(S) :

PROCESSOR SPARE	B20
I/O INTERFACE 1	B20

1.38 /EMRD

SOURCE : MAIN PROCESSOR A19

DESCRIPTION : (TTL) This signal indicates a memory read cycle (active LOW).

DESTINATION(S) :

PROCESSOR SPARE	A19
I/O INTERFACE 1	A19

1.39 /EMWR

SOURCE : MAIN PROCESSOR A20

DESCRIPTION : (TTL) This signal indicates a memory write cycle (active LOW).

DESTINATION(S) :

PROCESSOR SPARE	A20
I/O INTERFACE 1	A20

1.40 /EPWE

SOURCE : MAIN PROCESSOR B10

DESCRIPTION : (TTL) This signal disables the EPROM write protect circuitry controlling the data buffers to allow for external programming. (Active LOW)

DESTINATION(S) :

PROCESSOR SPARE	B10
I/O INTERFACE 1	B10

1.41 /ERESOUT

SOURCE : I/O INTERFACE 2 B4

DESCRIPTION : (TTL) Active low system reset function; internally synchronized with CLKOUT.

DESTINATION(S) :

COMM INTERFACE 1	8

1.42 /LUBE

SOURCE : MAIN PROCESSOR C8

DESCRIPTION : (TTL) Latched Upper Byte Enable. A LOW on this line indicates that the upper byte of the 16 bit data bus has valid data.

DESTINATION(S) :

PROCESSOR SPARE	C8
I/O INTERFACE 1	C8

1.43 /PLO

SOURCE : LO MODULE B13

DESCRIPTION : (TTL) Phase Lock On; A digital signal used to turn the 1st LO Phase-lock on (active LOW).

DESTINATION(S) :

MICROWAVE PHASE-LOCK	B2

1.44 /PROCDIS

SOURCE : MAIN PROCESSOR A10

DESCRIPTION : (TTL) This signal disables the processor from the system bus to allow the use of multiple processors.

DESTINATION(S) :

PROCESSOR SPARE	A10
I/O INTERFACE 1	A10

1.45 /RESET

SOURCE : DISPLAY AMPLIFIERS B7

DESCRIPTION : (TTL) "Inverted" system reset pulse, used to initialize the over-voltage protection circuitry on the High Voltage Power Supply module.

DESTINATION(S) :

HIGH VOLTAGE	B7

1.46 /SPLYON

SOURCE : MAIN PROCESSOR C27

DESCRIPTION : (TTL) A control bit used to enable the power supply output.

DESTINATION(S) :

PROCESSOR SPARE	C27
LV POWER SUPPLY	A7
I/O INTERFACE 1	C27

1.47 /SRQ

SOURCE : MAIN PROCESSOR A29

DESCRIPTION : (TTL) Serial bus service request line (Active LOW). This signal notifies the processor of module service requests.

DESTINATION(S) :

FRONT PANEL	B3
SPARE	A29
REFERENCE OSC.	A29
HIGH VOLTAGE	A29
DISPLAY AMPLIFIERS	A29
DIGITAL STORAGE	A29
VIDEO PROCESSOR	A29

LOG PROCESSOR	A29
LO MODULE	A29
565 SYNTHESIZER	A29
PERIOD COUNTER	A29
SWEEP/SPAN ATTEN.	A29
PROCESSOR SPARE	A29
I/O INTERFACE 1	A29
COMM INTERFACE 2	37
SATURN CALIBRATOR	A8
VR ASSEMBLY	A6
MICROWAVE IF	B2
525 IF	B5

1.48 1MHZ

SOURCE : REFERENCE OSC. B1

DESCRIPTION : (TTL) 1/100th of the 100MHz reference frequency (sent to the Period Counter).

DESTINATION(S) :

PERIOD COUNTER	B1

1.49 ACFOC

SOURCE : DISPLAY AMPLIFIERS B12

DESCRIPTION : The portion of the total focus signal that is used to keep the display focussed in response to a "sudden" change in intensity.

DESTINATION(S) :

HIGH VOLTAGE	B12

1.50 ACFOCRET

SOURCE : DISPLAY AMPLIFIERS B11

DESCRIPTION : Return for ACFOC

DESTINATION(S) :

HIGH VOLTAGE	B11

1.51 ACQCLK

SOURCE : DIGITAL STORAGE B9

DESCRIPTION : (TTL) An internal clock generated on the Digital Storage board that is divided down in the Video Processor module and used to run the digitizer. Its frequency is 9.216 MHz +/- 0.02%.

DESTINATION(S) :

VIDEO PROCESSOR B9

1.52 BLA1

SOURCE : I/O INTERFACE 2 B5

DESCRIPTION : (TTL) Buffered latched address 1

DESTINATION(S) :

COMM INTERFACE 1 11

1.53 BLA2

SOURCE : I/O INTERFACE 2 A5

DESCRIPTION : (TTL) Buffered latched address 2

DESTINATION(S) :

COMM INTERFACE 1 12

1.54 BLA3

SOURCE : I/O INTERFACE 2 B6

DESCRIPTION : (TTL) Buffered latched address 3

DESTINATION(S) :

COMM INTERFACE 1 13

1.55 BLA4

SOURCE : I/O INTERFACE 2 A6

DESCRIPTION : (TTL) Buffered latched address 4

DESTINATION(S) :

COMM INTERFACE 1 14

1.56 BLA5

SOURCE : I/O INTERFACE 2 B7

DESCRIPTION : (TTL) Buffered latched address 5

DESTINATION(S) :

COMM INTERFACE 1 15

1.57 BOD

SOURCE : DIGITAL STORAGE B2

DESCRIPTION : (TTL) Beginning Of Display handshaking signal between the Digital Storage and Display Amplifiers Module. This signal is pulsed high to indicate that a color change has just taken place.

DESTINATION(S) :

DISPLAY AMPLIFIERS B2

1.58 BPD0

SOURCE : I/O INTERFACE 2 B9

DESCRIPTION : (TTL) Buffered processor data bit 1 of 8-bit data bus (LSB)

DESTINATION(S) :

COMM INTERFACE 1 21

1.59 BPD1

SOURCE : I/O INTERFACE 2 A9

DESCRIPTION : (TTL) Buffered processor data bit 2 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 23

1.60 BPD2

SOURCE : I/O INTERFACE 2 B10

DESCRIPTION : (TTL) Buffered processor data bit 3 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 25

1.61 BPD3

SOURCE : I/O INTERFACE 2 A10

DESCRIPTION : (TTL) Buffered processor data bit 4 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 27

1.62 BPD4

SOURCE : I/O INTERFACE 2 B11

DESCRIPTION : (TTL) Buffered processor data bit 5 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 29

1.63 BPD5

SOURCE : I/O INTERFACE 2 A11

DESCRIPTION : (TTL) Buffered processor data bit 6 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 31

1.64 BPD6

SOURCE : I/O INTERFACE 2 B12

DESCRIPTION : (TTL) Buffered processor data bit 7 of 8-bit data bus

DESTINATION(S) :

COMM INTERFACE 1 33

1.65 BPD7

SOURCE : I/O INTERFACE 2 A12

DESCRIPTION : (TTL) Buffered processor data bit 8 of 8-bit data bus (MSB)

DESTINATION(S) :

COMM INTERFACE 1	35

1.66 COLOR+

SOURCE : DISPLAY AMPLIFIERS A25

DESCRIPTION : Color shutter drive signal (approx. 40V, 2kHz square wave).

DESTINATION(S) :

FRONT PANEL	A4

1.67 COLOR-

SOURCE : DISPLAY AMPLIFIERS A24

DESCRIPTION : Return for COLOR+

DESTINATION(S) :

FRONT PANEL	B4

1.68 D0

SOURCE : MAIN PROCESSOR C12

DESCRIPTION : (TTL) Bit 1 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C12
I/O INTERFACE 1	C12

1.69 D1

SOURCE : MAIN PROCESSOR A13

DESCRIPTION : (TTL) Bit 2 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	A13
I/O INTERFACE 1	A13

1.70 D10

SOURCE : MAIN PROCESSOR A16

DESCRIPTION : (TTL) Bit 11 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	A16
I/O INTERFACE 1	A16

1.71 D11

SOURCE : MAIN PROCESSOR B16

DESCRIPTION : (TTL) Bit 12 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	B16
I/O INTERFACE 1	B16

1.72 D12

SOURCE : MAIN PROCESSOR C16

DESCRIPTION : (TTL) Bit 13 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C16
I/O INTERFACE 1	C16

1.73 D13

SOURCE : MAIN PROCESSOR A17

DESCRIPTION : (TTL) Bit 14 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	A17

I/O INTERFACE 1 A17

1.74 D14

SOURCE : MAIN PROCESSOR B17

DESCRIPTION : (TTL) Bit 15 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	B17
I/O INTERFACE 1	B17

1.75 D15

SOURCE : MAIN PROCESSOR C17

DESCRIPTION : (TTL) Bit 16 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C17
I/O INTERFACE 1	C17

1.76 D2

SOURCE : MAIN PROCESSOR B13

DESCRIPTION (TTL) Bit 3 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	B13
I/O INTERFACE 1	B13

1.77 D3

SOURCE : MAIN PROCESSOR C13

DESCRIPTION : (TTL) Bit 4 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C13
I/O INTERFACE 1	C13

1.78 D4

SOURCE : MAIN PROCESSOR A14

DESCRIPTION : (TTL) Bit 5 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	A14
I/O INTERFACE 1	A14

1.79 D5

SOURCE : MAIN PROCESSOR B14

DESCRIPTION : (TTL) Bit 6 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	B14
I/O INTERFACE 1	B14

1.80 D6

SOURCE : MAIN PROCESSOR C14

DESCRIPTION : (TTL) Bit 7 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C14
I/O INTERFACE 1	C14

1.81 D7

SOURCE : MAIN PROCESSOR A15

DESCRIPTION : (TTL) Bit 8 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	A15
I/O INTERFACE 1	A15

1.82 D8

SOURCE : MAIN PROCESSOR B15

DESCRIPTION : (TTL) Bit 9 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	B15
I/O INTERFACE 1	B15

1.83 D9

SOURCE : MAIN PROCESSOR C15

DESCRIPTION : (TTL) Bit 10 of the 16 bit processor data bus

DESTINATION(S) :

PROCESSOR SPARE	C15
I/O INTERFACE 1	C15

1.84 DCFOC

SOURCE : DISPLAY AMPLIFIERS A22

DESCRIPTION : This signal is the "DC" or user variable portion of the total focus signal that is sent to the High Voltage Power Supply.

DESTINATION(S) :

HIGH VOLTAGE A22

1.85 DCFOCRET

SOURCE : DISPLAY AMPLIFIERS B22

DESCRIPTION : Return for DCFOC

DESTINATION(S) :

HIGH VOLTAGE B22

1.86 DIGBLANK

SOURCE : DIGITAL STORAGE A10

DESCRIPTION : (TTL) Digital Storage blanking signal (HIGH ==> blank)

DESTINATION(S) :

DISPLAY AMPLIFIERS A10

1.87 DIGCLK

SOURCE : DIGITAL STORAGE A9

DESCRIPTION : (TTL) An internal clock generated on the Digital Storage board that is used to run the acquisition system and the display sequencer. Its frequency is 4.608 MHz +/- 0.02%.

DESTINATION(S) :

DISPLAY AMPLIFIERS	A9
VIDEO PROCESSOR	A9
LOG PROCESSOR	A9

1.88 DIGCOLOR

SOURCE : DIGITAL STORAGE A8

DESCRIPTION : (TTL) This signal is used to control the color of the display (HIGH ==> green, LOW ==> red)

DESTINATION(S) :

DISPLAY AMPLIFIERS	A8

1.89 DSCL

SOURCE : MAIN PROCESSOR C28

DESCRIPTION : (TTL) High speed serial bus clock line: A serial clock used to control the movement of data between the Log Processor and Digital Storage modules, and the Main Processor System.

DESTINATION(S) :

DIGITAL STORAGE	B30
LOG PROCESSOR	B30
PROCESSOR SPARE	C28
I/O INTERFACE 1	C28

1.90 DSDA

SOURCE : MAIN PROCESSOR A28

DESCRIPTION : (TTL) High speed serial bus data line: Serial data line for the master IC bus linking the Log Processor, Digital Storage, and the Main Processor System.

DESTINATION(S) :

DIGITAL STORAGE	B29
LOG PROCESSOR	B29
PROCESSOR SPARE	A28
I/O INTERFACE 1	A28

1.91 DSH

SOURCE : DIGITAL STORAGE B5

DESCRIPTION : (ANALOG) Digital Storage Horizontal Deflection signal. A single-ended low-level deflection signal having a sensitivity of 1.5V for full screen deflection, and a nominal range of +/- 750mV.

DESTINATION(S) :

DISPLAY AMPLIFIERS B5

1.92 DSHRET

SOURCE : DIGITAL STORAGE A5

DESCRIPTION : Return for DSH

DESTINATION(S) :

DISPLAY AMPLIFIERS A5

1.93 DSV

SOURCE : DIGITAL STORAGE B3

DESCRIPTION : (ANALOG) Digital Storage Vertical Deflection signal. A single-ended low-level deflection signal having a sensitivity of 1.5V for full screen deflection, and a nominal range of +/- 750mV.

DESTINATION(S) :

DISPLAY AMPLIFIERS B3

1.94 DSVRET

SOURCE : DIGITAL STORAGE A3

DESCRIPTION : Return for DSV

DESTINATION(S) :

DISPLAY AMPLIFIERS	A3

1.95 DSZ

SOURCE : DIGITAL STORAGE A6

DESCRIPTION : (ANALOG) Digital Storage Z-Axis (Intensity) signal. A single-ended signal whose function is to allow Digital Storage to modulate the intensity of the display to allow for markers, high-lighted zones, intensified readout, etc. (Not implemented at this time.)

DESTINATION(S) :

DISPLAY AMPLIFIERS	A6

1.96 DSZRET

SOURCE : DIGITAL STORAGE B6

DESCRIPTION : Return for DSZ

DESTINATION(S) :

DISPLAY AMPLIFIERS	B6

1.97 ECLKOUT

SOURCE : MAIN PROCESSOR C26

DESCRIPTION : (TTL) Processor system synchronized clock.

DESTINATION(S) :

PROCESSOR SPARE	C26
I/O INTERFACE 1	C26

1.98 EDMARQ0

SOURCE : I/O INTERFACE 1 A22

DESCRIPTION : (TTL) DMA request input line 0 (Instrument Serial Bus)

DESTINATION(S) :

PROCESSOR SPARE	A22
MAIN PROCESSOR	A22

1.99 EDMARQ1

SOURCE : I/O INTERFACE 1 B22

DESCRIPTION : (TTL) DMA request input line 1 (GPIB0)

DESTINATION(S) :

PROCESSOR SPARE	B22
MAIN PROCESSOR	B22

1.100 EDMARQ2

SOURCE : I/O INTERFACE 1 C22

DESCRIPTION : (TTL) DMA request input line 2 (GPIB1)

DESTINATION(S) :

PROCESSOR SPARE	C22
MAIN PROCESSOR	C22

1.101 EDMARQ3

SOURCE : I/O INTERFACE 1 A23

DESCRIPTION : (TTL) DMA request input line 3 (High Speed Serial Bus)

DESTINATION(S) :

PROCESSOR SPARE	A23
MAIN PROCESSOR	A23

1.102 EINTP2

SOURCE : I/O INTERFACE 1 C23

DESCRIPTION : (TTL) Processor interrupt 2 (High Speed Serial Bus)

DESTINATION(S) :

PROCESSOR SPARE	C23
MAIN PROCESSOR	C23

1.103 EINTP3

SOURCE : I/O INTERFACE 1 A24

DESCRIPTION : (TTL) Processor interrupt 3 (GPIB1)

DESTINATION(S) :

PROCESSOR SPARE	A24
MAIN PROCESSOR	A24

1.104 EINTP4

SOURCE : I/O INTERFACE 1 B24

DESCRIPTION : (TTL) Processor interrupt 4 (GPIB2)

DESTINATION(S) :

PROCESSOR SPARE	B24
MAIN PROCESSOR	B24

1.105 EINTP5

SOURCE : MAIN PROCESSOR C24

DESCRIPTION : (TTL) Processor interrupt 5 (Instrument Serial Bus)

DESTINATION(S) :

PROCESSOR SPARE	C24
I/O INTERFACE 1	C24

1.106 EINTP6

SOURCE : MAIN PROCESSOR A25

DESCRIPTION : (TTL) Processor interrupt 6 (Service request SRQ)

DESTINATION(S) :

PROCESSOR SPARE	A25
I/O INTERFACE 1	A25

1.107 EINTP7

SOURCE : MAIN PROCESSOR B25

DESCRIPTION : (TTL) Processor interrupt 7 (On/Standby)

DESTINATION(S) :

PROCESSOR SPARE	B25
I/O INTERFACE 1	B25

1.108 EOC

SOURCE : DIGITAL STORAGE A11

DESCRIPTION : (TTL) End Of Character signal. This handshaking signal is used during "real-time" modes to indicate that Digital Storage has just completed drawing a character.

DESTINATION(S) :

DISPLAY AMPLIFIERS	A11

1.109 EPROMOE

SOURCE : EXTERNAL PROGRAMMING STATION

DESCRIPTION : (TTL) EPROM Output Enable for on-board programming.

DESTINATION(S) :

DIGITAL STORAGE	A22

1.110 EPROMVCC

SOURCE : EXTERNAL PROGRAMMING STATION

DESCRIPTION : EPROM programming voltage for VCC. Normally tied to +5VD by a jumper on the Digital Storage Board.

DESTINATION(S) :

DIGITAL STORAGE	A25

1.111 EPROMVPP

SOURCE : EXTERNAL PROGRAMMING STATION

DESCRIPTION : EPROM programming voltage for VPP. Normally tied to +5VD by a jumper on the Digital Storage Board.

DESTINATION(S) :

DIGITAL STORAGE	A25

1.112 EREADY

SOURCE : PROCESSOR SPARE C19

DESCRIPTION : (TTL) This signal allows peripheral devices to lengthen a bus cycle by forcing the processor to insert wait states (when the signal is LOW).

DESTINATION(S) :

I/O INTERFACE 1	C19
MAIN PROCESSOR	C19

1.113 ERESOUT

SOURCE : MAIN PROCESSOR C9

DESCRIPTION : (TTL) Active high system reset function; internally synchronized with CLKOUT.

DESTINATION(S) :

PROCESSOR SPARE	C9
I/O INTERFACE 1	C9

1.114 ETCTL2

SOURCE : I/O INTERFACE 1 B28

DESCRIPTION : (TTL) Timer 2 control line

DESTINATION(S) :

PROCESSOR SPARE	B28
MAIN PROCESSOR	B28

1.115 ETOUT2

SOURCE : MAIN PROCESSOR B23

DESCRIPTION : (TTL) Timer 2 output (internal timer output)

DESTINATION(S) :

PROCESSOR SPARE	B23
I/O INTERFACE 1	B23

1.116 EXT:T/H+

SOURCE : COMM INTERFACE 2 25

DESCRIPTION : External trigger and horizontal input (positive).

DESTINATION(S) :

SWEEP/SPAN ATTEN. A5

1.117 EXT:T/H-

SOURCE : COMM INTERFACE 2 26

DESCRIPTION : External trigger and horizontal input (negative).

DESTINATION(S) :

SWEEP/SPAN ATTEN. B5

1.118 EXTBLANK

SOURCE : COMM INTERFACE 2 22

DESCRIPTION : (TTL) External blanking input accessible from the rear panel. (HIGH ==> blank)

DESTINATION(S) :

DISPLAY AMPLIFIERS B9

1.119 EXTH+

SOURCE : COMM INTERFACE 2 14

DESCRIPTION : (ANALOG) External Horizontal Deflection input (positive): A low-level deflection signal having a sensitivity of approximately 90 mV/div when driven differentially with EXTH-.

DESTINATION(S) :

DISPLAY AMPLIFIERS B14

1.120 EXTH-

SOURCE : COMM INTERFACE 2 16

DESCRIPTION : (ANALOG) External Horizontal Deflection input (negative): A low-level deflection signal having a sensitivity of approximately 90 mV/div when driven differentially with EXTH+.

DESTINATION(S) :

DISPLAY AMPLIFIERS A14

1.121 EXTHO

SOURCE : DISPLAY AMPLIFIERS A13

DESCRIPTION : (ANALOG) Single-ended horizontal deflection signal having a range of -1.25V to +1.25V.

DESTINATION(S) :

COMM INTERFACE 2 27

1.122 EXTPSDR

SOURCE : LO MODULE B14

DESCRIPTION : This is a scaled version of the preselector drive voltage that is sent to the rear panel.

DESTINATION(S) :

COMM INTERFACE 2 7

1.123 EXTPSRET

SOURCE : LO MODULE A14

DESCRIPTION : Return for EXTPSDR

DESTINATION(S) :

COMM INTERFACE 2 6

1.124 EXTREF

SOURCE : COMM INTERFACE 2 2

DESCRIPTION : External reference signal

DESTINATION(S) :

REFERENCE OSC. A19

1.125 **EXTV+**

SOURCE : COMM INTERFACE 2 18

DESCRIPTION : (ANALOG) External Vertical Deflection input (positive): A low-level deflection signal having a sensitivity of approximately 65 mV/div when driven differentially with EXTV-.

DESTINATION(S) :

DISPLAY AMPLIFIERS B17

1.126 **EXTV-**

SOURCE : COMM INTERFACE 2 20

DESCRIPTION : (ANALOG) External Vertical Deflection input (negative): A low-level deflection signal having a sensitivity of approximately 65 mV/div when driven differentially with EXTV+.

DESTINATION(S) :

DISPLAY AMPLIFIERS A17

1.127 **EXTVI+**

SOURCE : COMM INTERFACE 2 10

DESCRIPTION : (ANALOG) External Video input (positive): An external video signal (capable of being filtered and digitized) having a sensitivity of approximately 87 mV/div when driven differentially with EXTVI-.

DESTINATION(S) :

VIDEO PROCESSOR B5

1.128 **EXTVI-**

SOURCE : COMM INTERFACE 2 12

DESCRIPTION : (ANALOG) External Video input (negative): An external video signal (capable of being filtered and digitized) having a sensitivity of approximately 87 mV/div when driven differentially with EXTVI+.

DESTINATION(S) :

VIDEO PROCESSOR A5

1.129 EXTVO

SOURCE : DISPLAY AMPLIFIERS B13

DESCRIPTION : (ANALOG) Single-ended vertical deflection signal having a range of -1.25V to +1.25V.

DESTINATION(S) :

COMM INTERFACE 2	29

1.130 EXTZO

SOURCE : DISPLAY AMPLIFIERS A12

DESCRIPTION : (ANALOG) External monitor Z-axis modulation signal having a range of 0 to 1V.

DESTINATION(S) :

COMM INTERFACE 2	31

1.131 FAN1

SOURCE : MAIN PROCESSOR B26

DESCRIPTION : (TTL) LSB control bit for fan speed.

DESTINATION(S) :

LV POWER SUPPLY	A20
PROCESSOR SPARE	B26
I/O INTERFACE 1	B26

1.132 FAN2

SOURCE : MAIN PROCESSOR B27

DESCRIPTION : (TTL) MSB control bit for fan speed.

DESTINATION(S) :

LV POWER SUPPLY	B20
PROCESSOR SPARE	B27
I/O INTERFACE 1	B27

1.133 FM+

SOURCE : MICROWAVE PHASE-LOCK A5

DESCRIPTION : FM Coil tune (positive): This signal is the amplified sum of the FM coil sweep voltage (FMCSWP) and the filtered phase error voltage (1st LO) during "locked" modes, and equals the amplified FM coil sweep voltage (FMCSWP) during "unlocked" modes.

DESTINATION(S) :

SATURN 1ST LO A10

1.134 FM-

SOURCE : MICROWAVE PHASE-LOCK B5

DESCRIPTION : FM Coil tune (negative): Return for FM+

DESTINATION(S) :

SATURN 1ST LO B9

1.135 FMCRET

SOURCE : LO MODULE A21

DESCRIPTION : Return for FMCSWP

DESTINATION(S) :

MICROWAVE PHASE-LOCK A7

1.136 FMCSWP

SOURCE : LO MODULE B21

DESCRIPTION : FM coil sweep voltage

DESTINATION(S) :

MICROWAVE PHASE-LOCK B7

1.137 FMRD

SOURCE : MICROWAVE PHASE-LOCK B4

DESCRIPTION : (ANALOG) FM coil Rail Detect; This signal senses the bias on the FM coil, and causes the bias on the main YIG coil to be adjusted if the FM coil is tuned beyond its range.

DESTINATION(S) :

LO MODULE A13

1.138 FR

SOURCE : REFERENCE OSC. A12

DESCRIPTION : This is the output of the "divide by R" counter that is internally connected to the phase detector input in the Reference Oscillator frequency synthesizer. This signal is therefore locked to the 100MHz reference frequency, and has a typical value of 250kHz.

DESTINATION(S) :

PERIOD COUNTER A12

1.139 FREQSWP+

SOURCE : SWEEP/SPAN ATTEN. B19

DESCRIPTION : (ANALOG) Frequency sweep voltage (positive).

DESTINATION(S) :

LO MODULE B19

1.140 FREQSWP-

SOURCE : SWEEP/SPAN ATTEN. A19

DESCRIPTION : (ANALOG) Frequency sweep voltage (negative).

DESTINATION(S) :

LO MODULE A19

1.141 FV

SOURCE : REFERENCE OSC. A13

DESCRIPTION : This is the output of the "divide by N" counter that is internally connected to the phase detector input in the Reference Oscillator frequency synthesizer. This signal is therefore locked to the 100MHz reference frequency, and has a

typical value of 250kHz.

DESTINATION(S) :

PERIOD COUNTER	A13

1.142 GND

SOURCE : LV POWER SUPPLY A1,A2,A3,A4,B10,A13,A17,B17,B22,B23 B24,B25

DESCRIPTION : Common return

DESTINATION(S) :

FRONT PANEL	B1
LO MODULE	A2,B2,A3,B3,A6,B6,A8,A9,B9,A18,B18 B24,B25,A31,B31
565 SYNTHESIZER	A2,B2,A3,B3,A6,B6,A8,A9,B9,A18,B18 B24,B25,A31,B31
SPARE	A18,B18,B24,B25,A31,B31
REFERENCE OSC.	A18,B18,B19,B24,B25,A31,B31
HIGH VOLTAGE	A18,B18,B24,B25,A31,B31
DISPLAY AMPLIFIERS	A18,B18,B24,B25,A31,B31
DIGITAL STORAGE	A18,B18,B24,B25,A31,B31
VIDEO PROCESSOR	A18,B18,B24,B25,A31,B31
LOG PROCESSOR	A18,B18,B24,B25,A31,B31
PERIOD COUNTER	A18,B18,B24,B25,A31,B31
SWEEP/SPAN ATTEN.	A18,B18,B24,B25,A31,B31
PROCESSOR SPARE	A1,B1,C1,A11,B11,C11,A18,B18,C18,A31 B31,C31
I/O INTERFACE 1	A1,B1,C1,A11,B11,C11,A18,B18,C18,A31 B31,C31
COMM INTERFACE 2	1,3,8,9,11,13,15,17,19,21,23,28,30 32,34
MAIN PROCESSOR	A1,B1,C1,A11,B11,C11,A18,B18,C18,A31 B31,C31
COMM INTERFACE 1	1,10,16,20,22,24,26,28,30,32,34,36,40
JUPITER 1ST CONVERTER	A5
SATURN CALIBRATOR	A6
SATURN 1ST LO	A5,B10
MICROWAVE PHASE-LOCK	B3
SATURN MTX CONTROL	A3,B3,A9,B9
VR ASSEMBLY	B4
SATURN PRESEL DRVR	A2
MICROWAVE IF	A2,B4,A5,A7,B7
525 IF	A3

1.143 HVOFF

SOURCE : DISPLAY AMPLIFIERS B10

DESCRIPTION : (TTL) An active HIGH signal that can be used to turn off the high voltage power supply. (At the present time this signal is grounded through a resistor on the Display Amplifiers board.)

DESTINATION(S) :

HIGH VOLTAGE B10

1.144 IFG

SOURCE : PERIOD COUNTER B7

DESCRIPTION : (TTL) IFG is used to turn the calibrator or tracking generator off for the purposes of self calibration. (Not implemented at this time.)

DESTINATION(S) :

SATURN CALIBRATOR A7

1.145 IFPC

SOURCE : LOG PROCESSOR B9

DESCRIPTION : (TTL) IF output to period counter.

DESTINATION(S) :

PERIOD COUNTER B9

1.146 INTH+

SOURCE : VIDEO PROCESSOR B19

DESCRIPTION : (ANALOG) Internal real-time horizontal deflection signal: A low-level deflection signal having a sensitivity of 150 mV/div (expanded mode) and 120 mV/div (compressed mode).

DESTINATION(S) :

DISPLAY AMPLIFIERS B19

1.147 INTH-

SOURCE : VIDEO PROCESSOR A19

DESCRIPTION : Return for INTH+

DESTINATION(S) :

DISPLAY AMPLIFIERS A19

1.148 INTV+

SOURCE : VIDEO PROCESSOR B21

DESCRIPTION : (ANALOG) Internal real-time vertical deflection signal (positive): A low-level deflection signal having a sensitivity of approximately 60 mV/div when driven differentially with INTV-.

DESTINATION(S) :

DISPLAY AMPLIFIERS B21

1.149 INTV-

SOURCE : VIDEO PROCESSOR A21

DESCRIPTION : (ANALOG) Internal real-time vertical deflection signal (negative): A low-level deflection signal having a sensitivity of approximately 60 mV/div when driven differentially with INTV+.

DESTINATION(S) :

DISPLAY AMPLIFIERS A21

1.150 LA0

SOURCE : MAIN PROCESSOR A2

DESCRIPTION : (TTL) Bit 1 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE A2
I/O INTERFACE 1 A2

1.151 LA1

SOURCE : MAIN PROCESSOR B2

DESCRIPTION : (TTL) Bit 2 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B2
I/O INTERFACE 1	B2

1.152 LA10

SOURCE : MAIN PROCESSOR B5

DESCRIPTION : (TTL) Bit 11 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B5
I/O INTERFACE 1	B5

1.153 LA11

SOURCE : MAIN PROCESSOR C5

DESCRIPTION : (TTL) Bit 12 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C5
I/O INTERFACE 1	C5

1.154 LA12

SOURCE : MAIN PROCESSOR A6

DESCRIPTION : (TTL) Bit 13 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A6
I/O INTERFACE 1	A6

1.155 LA13

SOURCE : MAIN PROCESSOR B6

DESCRIPTION : (TTL) Bit 14 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B6
I/O INTERFACE 1	B6

1.156 LA14

SOURCE : MAIN PROCESSOR C6

DESCRIPTION : (TTL) Bit 15 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C6
I/O INTERFACE 1	C6

1.157 LA15

SOURCE : MAIN PROCESSOR A7

DESCRIPTION : (TTL) Bit 16 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A7
I/O INTERFACE 1	A7

1.158 LA16

SOURCE : MAIN PROCESSOR B7

DESCRIPTION : (TTL) Bit 17 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B7
I/O INTERFACE 1	B7

1.159 LA17

SOURCE : MAIN PROCESSOR C7

DESCRIPTION : (TTL) Bit 18 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C7

I/O INTERFACE 1 C7

1.160 LA18

SOURCE : MAIN PROCESSOR A8

DESCRIPTION : (TTL) Bit 19 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A8
I/O INTERFACE 1	A8

1.161 LA19

SOURCE : MAIN PROCESSOR B8

DESCRIPTION : (TTL) Bit 20 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B8
I/O INTERFACE 1	B8

1.162 LA2

SOURCE : MAIN PROCESSOR C2

DESCRIPTION : (TTL) Bit 3 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C2
I/O INTERFACE 1	C2

1.163 LA3

SOURCE : MAIN PROCESSOR A3

DESCRIPTION : (TTL) Bit 4 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A3
I/O INTERFACE 1	A3

1.164 LA4

SOURCE : MAIN PROCESSOR B3

DESCRIPTION : (TTL) Bit 5 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B3
I/O INTERFACE 1	B3

1.165 LA5

SOURCE : MAIN PROCESSOR C3

DESCRIPTION : (TTL) Bit 6 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C3
I/O INTERFACE 1	C3

1.166 LA6

SOURCE : MAIN PROCESSOR A4

DESCRIPTION : (TTL) Bit 7 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A4
I/O INTERFACE 1	A4

1.167 LA7

SOURCE : MAIN PROCESSOR B4

DESCRIPTION : (TTL) Bit 8 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	B4
I/O INTERFACE 1	B4

1.168 LA8

SOURCE : MAIN PROCESSOR C4

DESCRIPTION : (TTL) Bit 9 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	C4
I/O INTERFACE 1	C4

1.169 LA9

SOURCE : MAIN PROCESSOR A5

DESCRIPTION : (TTL) Bit 10 of 20-bit latched address bus

DESTINATION(S) :

PROCESSOR SPARE	A5
I/O INTERFACE 1	A5

1.170 LAVI+

SOURCE : LOG PROCESSOR B17

DESCRIPTION : (ANALOG) Log Amp Video (positive): A low-level video signal having a sensitivity of 75 mV/div (when driven differentially with LAVI-), centered about ground. This input comes into the video chain before the Video Processor, and therefore can be filtered and digitized.

DESTINATION(S) :

VIDEO PROCESSOR B17

1.171 LAVI-

SOURCE : LOG PROCESSOR A17

DESCRIPTION : (ANALOG) Log Amp Video (negative): A low-level video signal having a sensitivity of 75 mV/div (when driven differentially with LAVI+), centered about ground. This input comes into the video chain before the Video Processor, and therefore can be filtered and digitized.

DESTINATION(S) :

VIDEO PROCESSOR A17

1.172 LBS1

SOURCE : MAIN PROCESSOR B9

DESCRIPTION : (TTL) Latched bus status signal 1: Used to indicate the type of bus cycle being performed by the processor. 1 ==> WRITE : 0 ==> READ

DESTINATION(S) :

PROCESSOR SPARE	B9
I/O INTERFACE 1	B9

1.173 LBS2

SOURCE : MAIN PROCESSOR A9

DESCRIPTION : (TTL) Latched bus status signal 2: Used to indicate the type of bus cycle being performed by the processor. 1 ==> MEM : 0 ==> I/O

DESTINATION(S) :

PROCESSOR SPARE	A9
I/O INTERFACE 1	A9

1.174 LINEV

SOURCE : LV POWER SUPPLY A9

DESCRIPTION : (ANALOG) A low-level 60Hz signal for line triggering.

DESTINATION(S) :

SWEEP/SPAN ATTEN.	A14

1.175 LOCNT

SOURCE : LO MODULE B8

DESCRIPTION : (TTL) This signal is used to enable the output of the divide-by-32 counter in the Microwave phase-lock module, allowing the period counter to count the beat frequency between the 1st LO and the 565/4 output.

DESTINATION(S) :

MICROWAVE PHASE-LOCK	A2

1.176 LODR+

SOURCE : LO MODULE A25

DESCRIPTION : (ANALOG) YIG center frequency tune voltage (positive).

DESTINATION(S) :

SATURN 1ST LO A7

1.177 LODR-

SOURCE : LO MODULE A24

DESCRIPTION : (ANALOG) YIG center frequency tune voltage (negative).

DESTINATION(S) :

SATURN 1ST LO B7

1.178 LOFLT

SOURCE : LO MODULE B7

DESCRIPTION : (TTL) This signal controls the bandwidth reduction on the main YIG coil.

DESTINATION(S) :

SATURN 1ST LO B1

1.179 LOFRQ

SOURCE : LO MODULE B5

DESCRIPTION : This is a scaled version of the main YIG coil tune voltage that is sent to the rear panel.

DESTINATION(S) :

COMM INTERFACE 2 4

1.180 LOFRQRTN

SOURCE : LO MODULE A5

DESCRIPTION : Return for LOFRQ

DESTINATION(S) :

COMM INTERFACE 2 5

1.181 LOPC

SOURCE : LO MODULE B10

DESCRIPTION : (TTL) This is the LO output for the period counter.

DESTINATION(S) :

PERIOD COUNTER	B10

1.182 MTX1

SOURCE : MAIN PROCESSOR A26

DESCRIPTION : (TTL) LSB control bit for the +MTXV supply.

DESTINATION(S) :

LV POWER SUPPLY	A18
PROCESSOR SPARE	A26
I/O INTERFACE 1	A26

1.183 MTX2

SOURCE : MAIN PROCESSOR A27

DESCRIPTION : (TTL) MSB control bit for the +MTXV supply.

DESTINATION(S) :

LV POWER SUPPLY	B18
PROCESSOR SPARE	A27
I/O INTERFACE 1	A27

1.184 ON/OFF

SOURCE : FRONT PANEL B7

DESCRIPTION : (TTL) This signal is connected to the front panel power switch, and is used to request changes between the standby and normal power supply modes.

DESTINATION(S) :

PROCESSOR SPARE	C25
I/O INTERFACE 1	C25
MAIN PROCESSOR	C25

1.185 OSC1

SOURCE : I/O INTERFACE 2 B13

DESCRIPTION : (TTL) Control bit for the +OSCV supply. (Currently not implemented.)

DESTINATION(S) :

LV POWER SUPPLY B7

1.186 PENLIFT

SOURCE : VIDEO PROCESSOR A7

DESCRIPTION : (TTL) An output to the rear panel to lift the pen of a plotter during sweep retrace. This signal can also be used as the "real-time" blanking signal in external monitor mode.

DESTINATION(S) :

COMM INTERFACE 2 24

1.187 PLLPC

SOURCE : MICROWAVE PHASE-LOCK A1

DESCRIPTION : (TTL) Output of the 1st LO phase-lock system to the period counter. This signal is the output of the divide-by-32 counter which counts the beat frequency between the 1st LO and the 565/4 output.

DESTINATION(S) :

PERIOD COUNTER B11

1.188 PSDR+

SOURCE : LO MODULE B17

DESCRIPTION : (ANALOG) Positive drive voltage for the preselector.

DESTINATION(S) :

SATURN PRESEL DRVR A7

1.189 PSDR-

SOURCE : LO MODULE A17

DESCRIPTION : (ANALOG) Negative drive voltage for the preselector.

DESTINATION(S) :

SATURN PRESEL DRVR	B7

1.190 PSFLT

SOURCE : SATURN MTX CONTROL B8

DESCRIPTION : (TTL) This signal controls the bandwidth on the preselector coil.

DESTINATION(S) :

SATURN PRESEL DRVR	B1

1.191 PSG

SOURCE : VIDEO PROCESSOR B8

DESCRIPTION : (TTL) Precision Sweep Gate: This signal indicates when the sweep voltage is within the digitizing limits of the horizontal acquisition system.

DESTINATION(S) :

DISPLAY AMPLIFIERS	B8
PERIOD COUNTER	B22

1.192 RDTRIG

SOURCE : VIDEO PROCESSOR B22

DESCRIPTION : (TTL) This signal is used to initiate resonator ring-down during calibration in order to synchronize the horizontal digitizer with the beginning of the "ring-down".

DESTINATION(S) :

VR ASSEMBLY	A5

1.193 RES

SOURCE : MAIN PROCESSOR A30

DESCRIPTION : (TTL) Serial bus reset line.

DESTINATION(S) :

FRONT PANEL	A3

SPARE	A30
REFERENCE OSC.	A30
HIGH VOLTAGE	A30
DISPLAY AMPLIFIERS	A30
DIGITAL STORAGE	A30
VIDEO PROCESSOR	A30
LOG PROCESSOR	A30
LO MODULE	A30
565 SYNTHESIZER	A30
PERIOD COUNTER	A30
SWEEP/SPAN ATTEN.	A30
PROCESSOR SPARE	A30
I/O INTERFACE 1	A30
COMM INTERFACE 2	40
JUPITER 1ST CONVERTER	A1
SATURN CALIBRATOR	A9
SATURN MTX CONTROL	B2
VR ASSEMBLY	B5
MICROWAVE IF	B3
525 IF	B4

1.194 RF/TG-PC

SOURCE : SATURN CALIBRATOR B7

DESCRIPTION : (TTL) Divided down Calibrator/Tracking Generator output to the Period Counter module. (Not implemented at this time.)

DESTINATION(S) :

PERIOD COUNTER	B8

1.195 SCL

SOURCE : MAIN PROCESSOR B30

DESCRIPTION : (TTL) Serial bus clock line: A serial clock used to control the movement of data on the serial bus.

DESTINATION(S) :

FRONT PANEL	B2
SPARE	B30
REFERENCE OSC.	B30
HIGH VOLTAGE	B30
DISPLAY AMPLIFIERS	B30
VIDEO PROCESSOR	B30
LO MODULE	B30
565 SYNTHESIZER	B30
PERIOD COUNTER	B30
SWEEP/SPAN ATTEN.	B30

PROCESSOR SPARE	B30
COMM INTERFACE 2	39
I/O INTERFACE 1	B30
JUPITER 1ST CONVERTER	B1
SATURN CALIBRATOR	B9
SATURN MTX CONTROL	A1
VR ASSEMBLY	B3
MICROWAVE IF	A4
525 IF	A4

1.196 SDA

SOURCE : MAIN PROCESSOR B29

DESCRIPTION : (TTL) Serial bus data line.

DESTINATION(S) :

FRONT PANEL	A2
SPARE	B29
REFERENCE OSC.	B29
HIGH VOLTAGE	B29
DISPLAY AMPLIFIERS	B29
VIDEO PROCESSOR	B29
LO MODULE	B29
565 SYNTHESIZER	B29
PERIOD COUNTER	B29
SWEEP/SPAN ATTEN.	B29
PROCESSOR SPARE	B29
I/O INTERFACE 1	B29
COMM INTERFACE 2	38
JUPITER 1ST CONVERTER	A3
SATURN CALIBRATOR	A10
SATURN MTX CONTROL	A2
VR ASSEMBLY	A2
MICROWAVE IF	A3
525 IF	A5

1.197 SDAH

SOURCE : VIDEO PROCESSOR B12

DESCRIPTION : (TTL) Serial data line for the digitized horizontal data.

DESTINATION(S) :

DIGITAL STORAGE	B12
LOG PROCESSOR	B12

1.198 SDAHSE

SOURCE : VIDEO PROCESSOR A13

DESCRIPTION : (TTL) Seria DAta Horizontal Shift Enable: This signal enables the shifting of only the horizontal data into the acquisition shift register on the Digital Storage board.

DESTINATION(S) :

DIGITAL STORAGE	A13

1.199 SDASE

SOURCE : VIDEO PROCESSOR A12

DESCRIPTION : (TTL) Serial DAta Shift Enable: This signal enables the shifting of the serially transmitted vertical and horizontal digitized data into the acquisition shift registers on the Digital Storage board.

DESTINATION(S) :

DIGITAL STORAGE	A12
LOG PROCESSOR	A12

1.200 SDAV

SOURCE : VIDEO PROCESSOR B11

DESCRIPTION : (TTL) Serial data line for the digitized vertical data.

DESTINATION(S) :

DIGITAL STORAGE	B11

1.201 SLZS

SOURCE : SWEEP/SPAN ATTEN. B2

DESCRIPTION : Sweep Length Zero Span: This signal is counted by the period counter to define an 11 division window.

DESTINATION(S) :

PERIOD COUNTER	B2

1.202 SPLYFAIL

SOURCE : LV POWER SUPPLY B8

DESCRIPTION : (TTL) This signal indicates a loss of regulation condition in the power supply, due to current limit, short circuit, etc.

DESTINATION(S) :

PROCESSOR SPARE	C29
I/O INTERFACE 1	C29
MAIN PROCESSOR	C29

1.203 SWEEP+

SOURCE : SWEEP/SPAN ATTEN. A25

DESCRIPTION : (ANALOG) 0 to 10V sweep signal used to drive the acquisition system.

DESTINATION(S) :

VIDEO PROCESSOR	A25

1.204 SWEEP-

SOURCE : SWEEP/SPAN ATTEN. A24

DESCRIPTION : Return for SWEEP+

DESTINATION(S) :

VIDEO PROCESSOR	A24

1.205 SWPGATE

SOURCE : SWEEP/SPAN ATTEN. A22

DESCRIPTION : (TTL) This signal indicates valid sweep by going HIGH when the sweep is active and LOW during retrace and hold-off.

DESTINATION(S) :

VIDEO PROCESSOR	A22
LOG PROCESSOR	A22

1.206 SWPOUT

SOURCE : SWEEP/SPAN ATTEN. A6

DESCRIPTION : Sweep voltage output to rear panel. Selectable ranges of 0 to 10V, or -5V to +5V (corresponds to the sweep input).

DESTINATION(S) :

COMM INTERFACE 2 33

1.207 TRIG+

SOURCE : VIDEO PROCESSOR B3

DESCRIPTION : Internal TRIGger (positive): A differential signal provided for internal triggering. Ranges from +1V to -1V.

DESTINATION(S) :

SWEEP/SPAN ATTEN. B3

1.208 TRIG-

SOURCE : VIDEO PROCESSOR A3

DESCRIPTION : Internal TRIGger (negative): A differential signal provided for internal triggering. Ranges from +1V to -1V.

DESTINATION(S) :

SWEEP/SPAN ATTEN. A3

1.209 WBD

SOURCE : DIGITAL STORAGE A2

DESCRIPTION : (TTL) Waveform Being Drawn: When HIGH, this signal indicates that a digitally stored waveform is being drawn. This distinguishes the waveform from readout and graticule information.

DESTINATION(S) :

DISPLAY AMPLIFIERS A2

1.210 YIGRET

SOURCE : LV POWER SUPPLY A6,B6

DESCRIPTION : Current return line for the +MTXV and +OSCV supplies

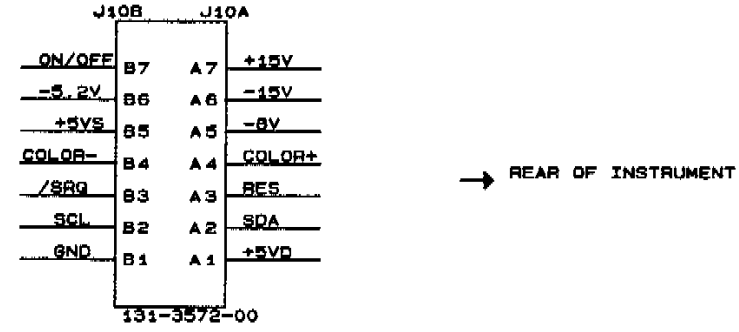
DESTINATION(S) :

SATURN 1ST LO	A6
SATURN PRESEL DRVR	A6

2. CONNECTOR PINOUTS

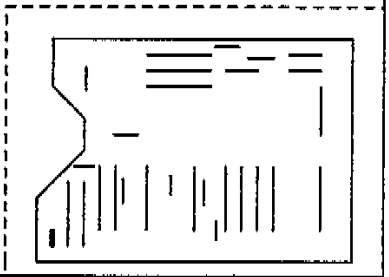
2.1 J10 - FRONT PANEL

CRT



FRONT PANEL:
FRONT PANEL #1 388-9035-01
FRONT PANEL #2 388-9034-01

CONNECTOR LOCATION



TEKTRONIX, INC.

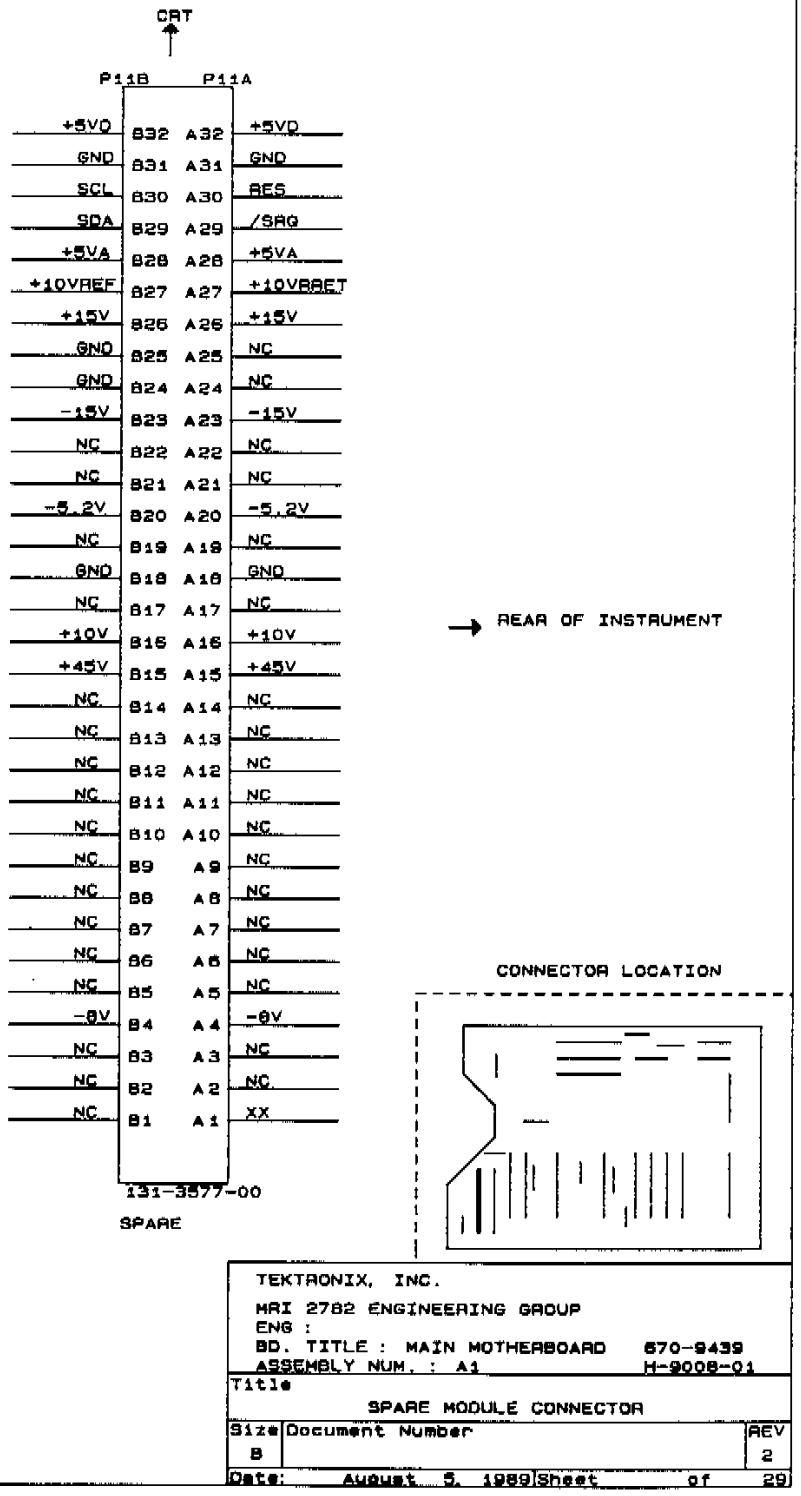
MRI 2782 ENGINEERING GROUP
ENG : RICK WILSON PHONE : 627-1469
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
FRONT PANEL CONNECTOR

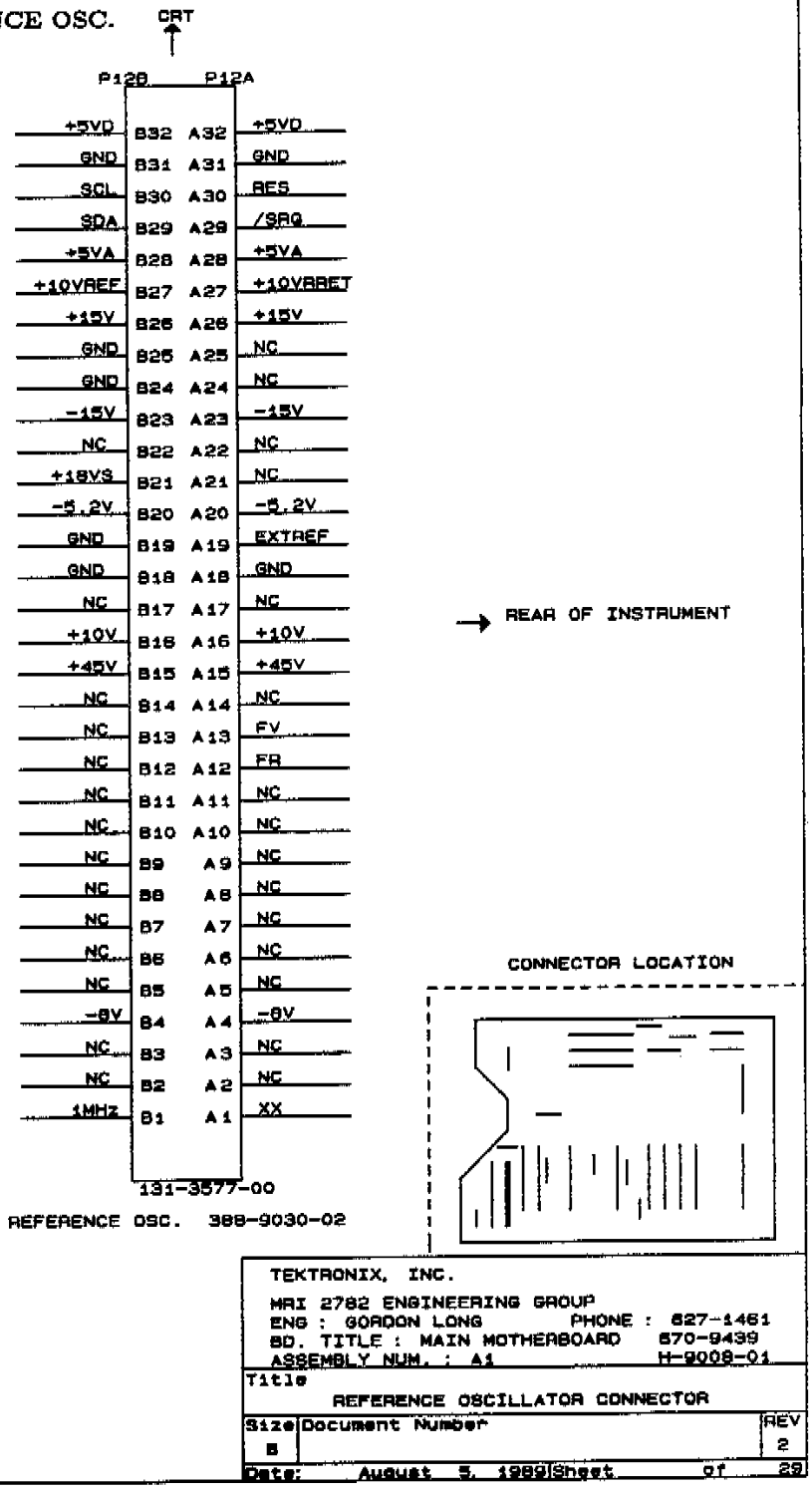
Size	Document Number	REV
B		2

Date: August 5, 1989 Sheet of 29

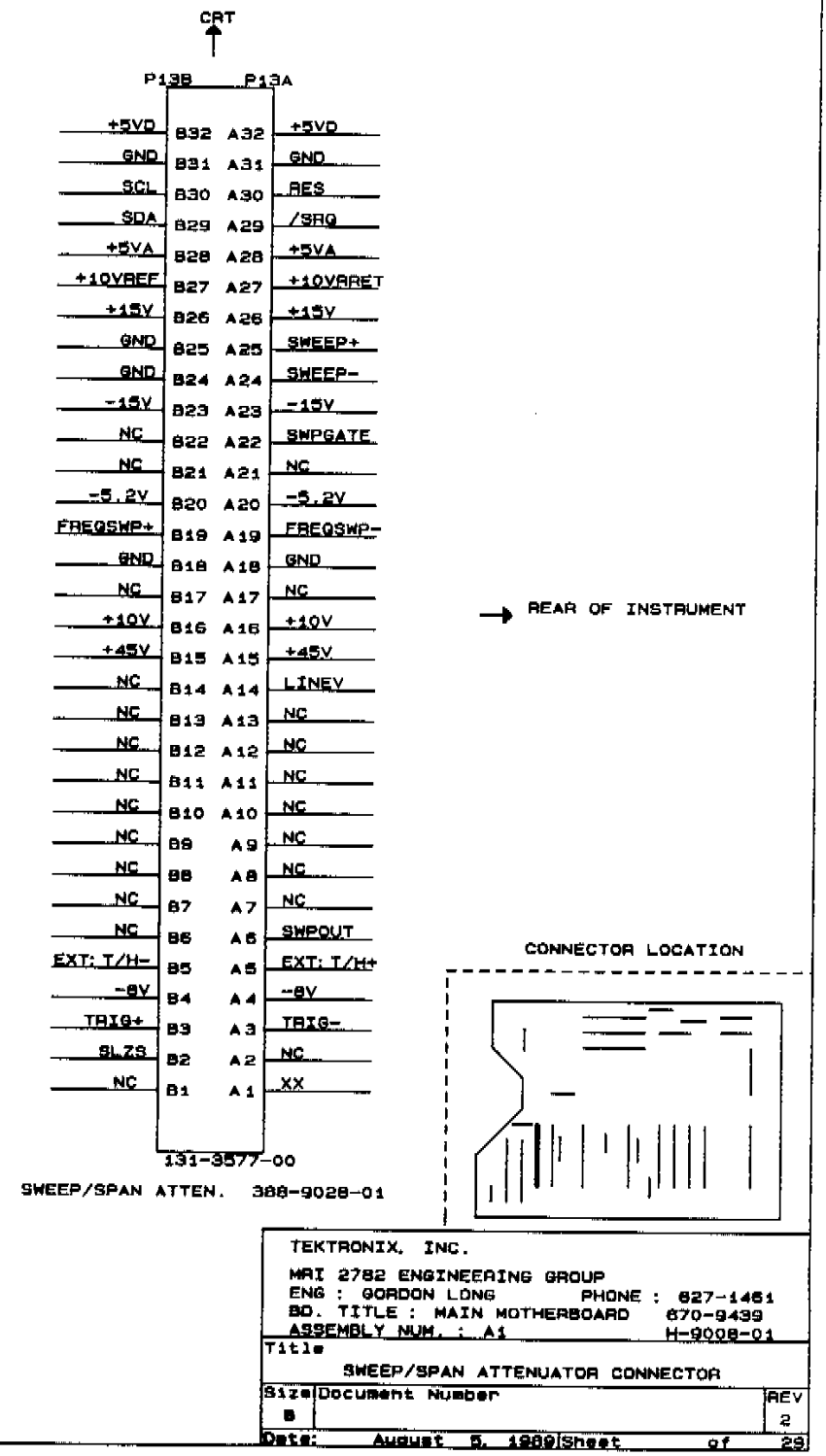
2.2 P11 - SPARE


CRT
P11B P11A
+5VD B32 A32 +5VD
GND B31 A31 GND
SCL B30 A30 BES
SDA B29 A29 /SRQ
+5VA B28 A28 +5VA
+10VREF B27 A27 +10VRET
+15V B26 A26 +15V
GND B25 A25 NC
GND B24 A24 NC
-15V B23 A23 -15V
NC B22 A22 NC
NC B21 A21 NC
-5.2V B20 A20 -5.2V
NC B19 A19 NC
GND B18 A18 GND
NC B17 A17 NC
+10V B16 A16 +10V
+45V B15 A15 +45V
NC B14 A14 NC
NC B13 A13 NC
NC B12 A12 NC
NC B11 A11 NC
NC B10 A10 NC
NC B9 A9 NC
NC B8 A8 NC
NC B7 A7 NC
NC B6 A6 NC
NC B5 A5 NC
-8V B4 A4 -8V
NC B3 A3 NC
NC B2 A2 NC
NC B1 A1 XX
131-3577-00
SPARE
REAR OF INSTRUMENT
CONNECTOR LOCATION
TEKTRONIX, INC.
MRI 2782 ENGINEERING GROUP
ENG :
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01
Title
SPARE MODULE CONNECTOR
Size B
Document Number
REV 2
Date: August 5, 1989 Sheet of 29

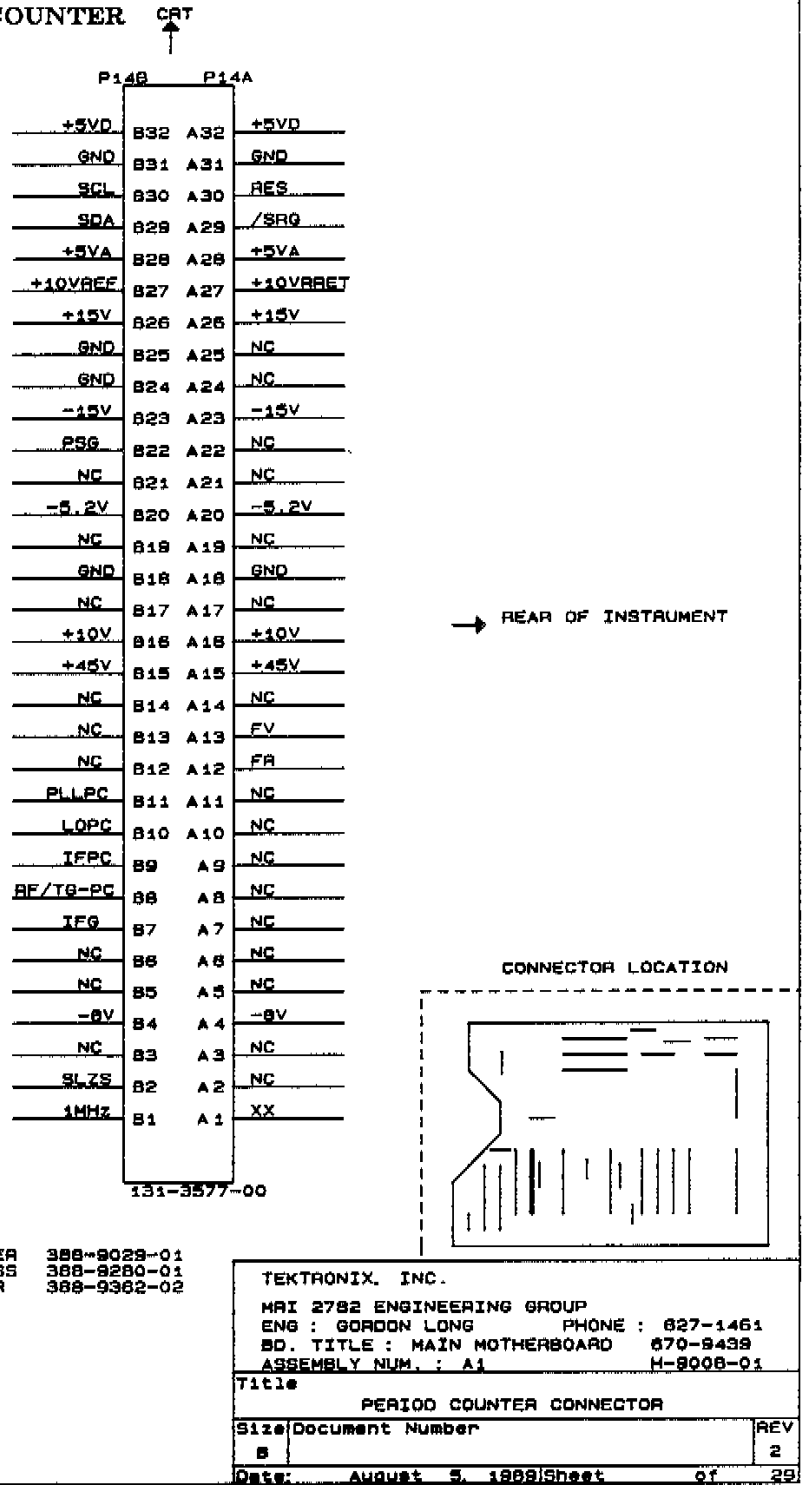
2.3 P12 - REFERENCE OSC.



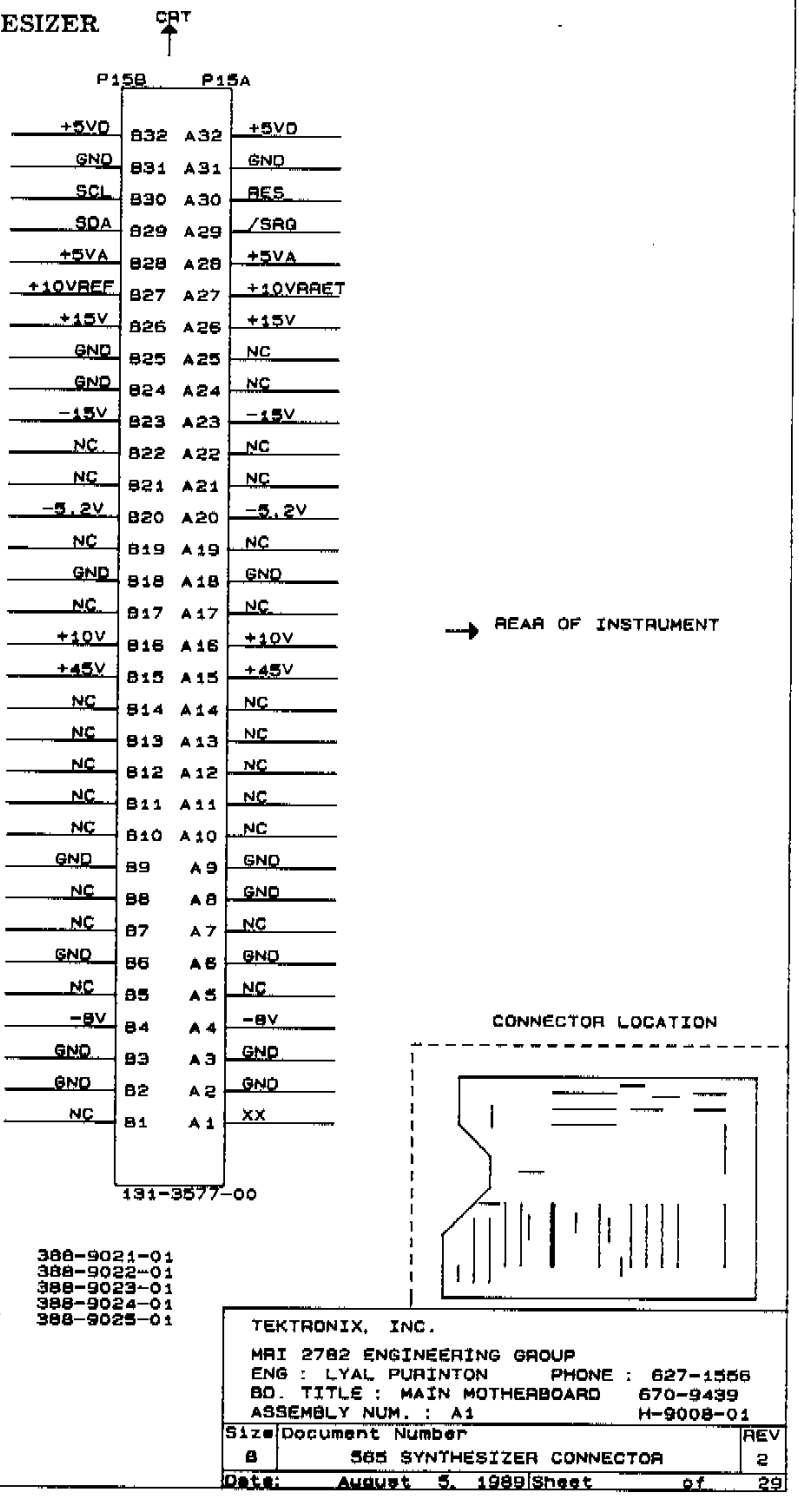
2.4 P13 - SWEEP/SPAN ATTEN.



2.5 P14 - PERIOD COUNTER



2.6 P15 - 565 SYNTHESIZER



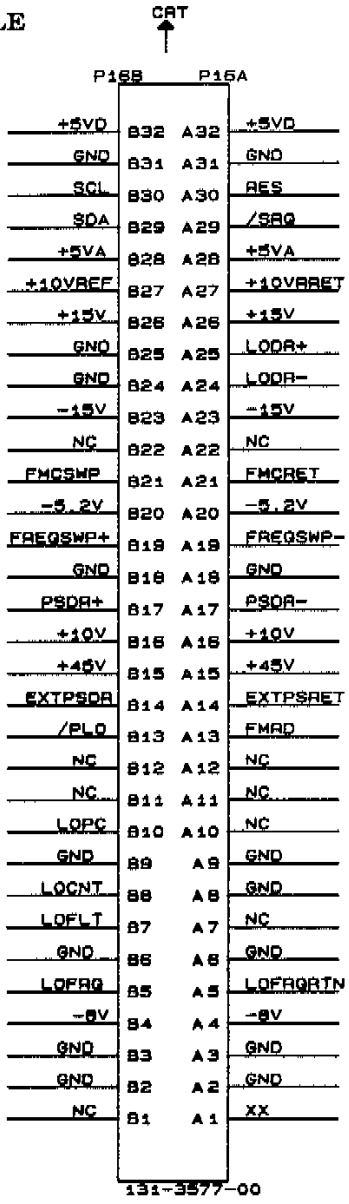
565 SYNTHESIZER:

565 OSCILLATOR	388-9021-01
565 MIXER	388-9022-01
565 PHASE LOCK	388-9023-01
FRACT. N SYNTH.	388-9024-01
565 INTERCONNECT	388-9025-01

TEKTRONIX, INC.
MRI 2782 ENGINEERING GROUP
ENG : LYAL PURINTON PHONE : 627-1556
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

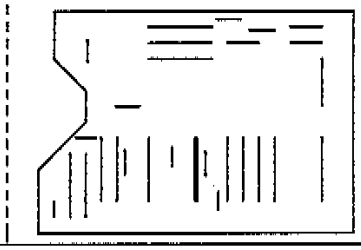
Size	Document Number	REV
B	565 SYNTHESIZER CONNECTOR	2
Date: August 5, 1989	Sheet of	29

2.7 P16 - LO MODULE



REAR OF INSTRUMENT

CONNECTOR LOCATION



LO MODULE:

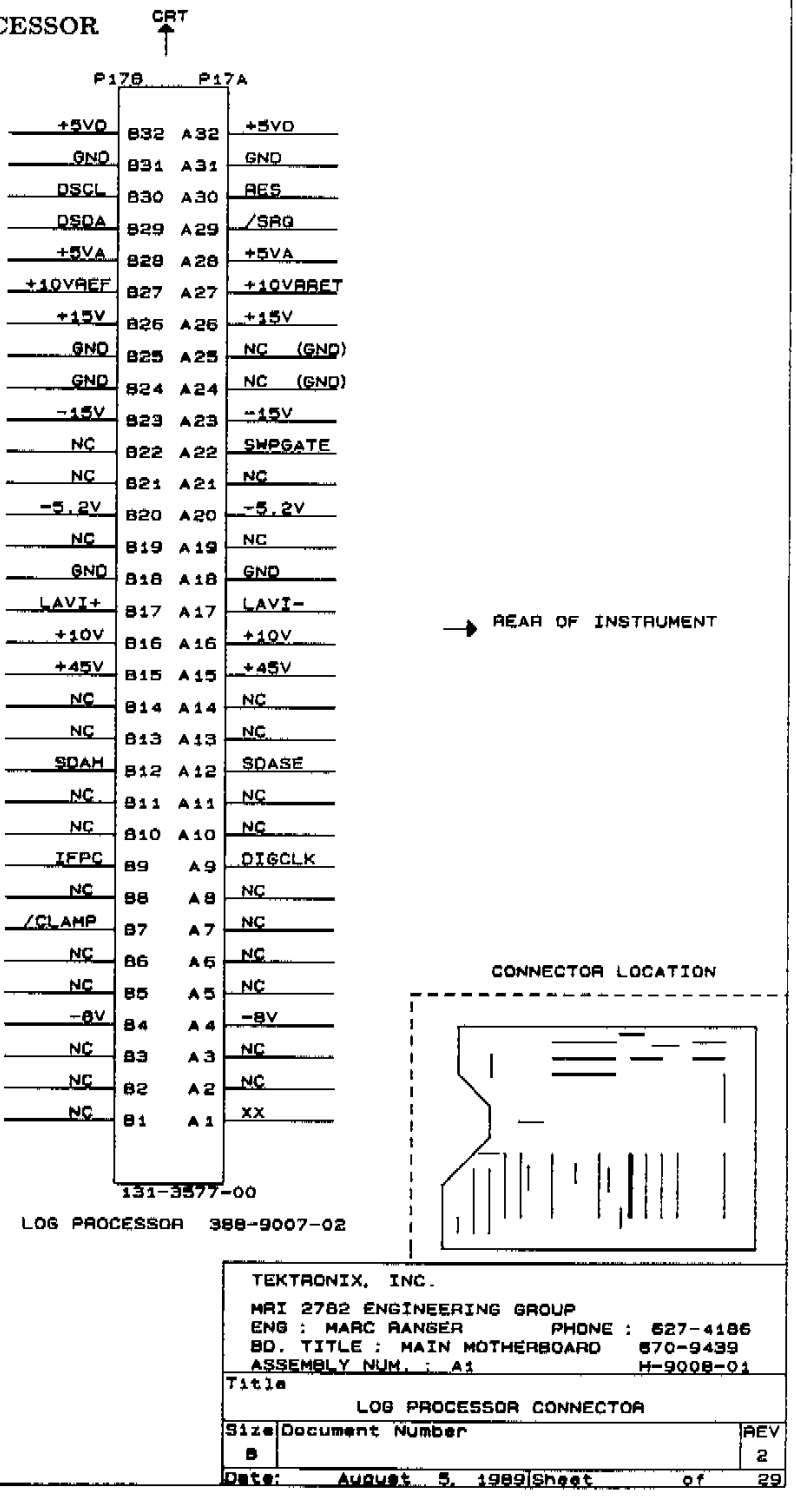
129 MHZ OSC.	388-9379-01
500 MHZ MIXER	388-9380-02
129 MHZ SYNTH.	388-9519-02
MICROWAVE CONTROL	388-9520-01
LO CONTROL	388-9027-01

TEKTRONIX, INC.

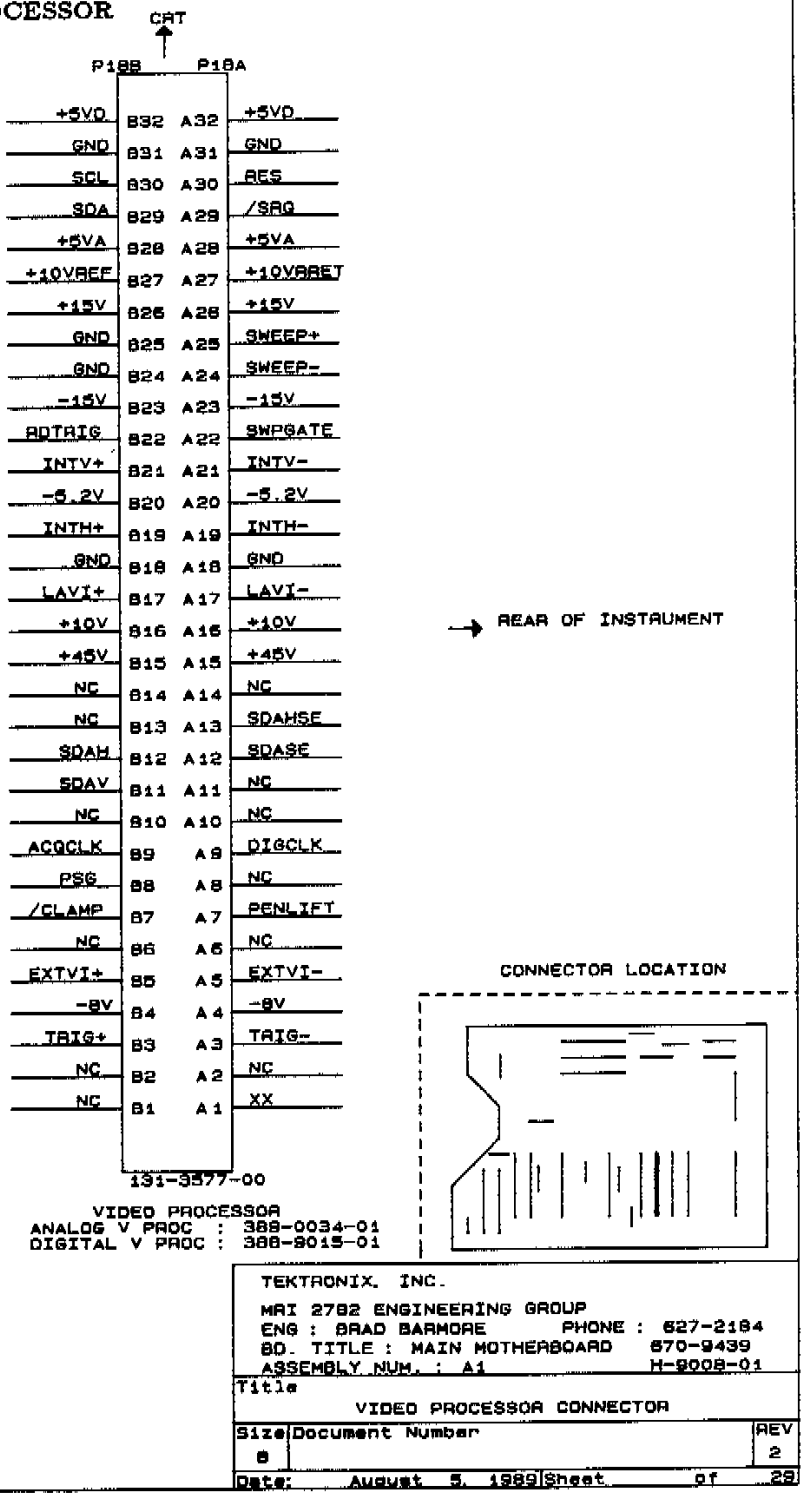
MAI 2782 ENGINEERING GROUP
ENG : LYAL PURINTON PHONE : 627-1556
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Size	Document Number	REV
B	LO MODULE MOTHERBOARD CONNECTOR	2
Date: August 5, 1989	Sheet of	29

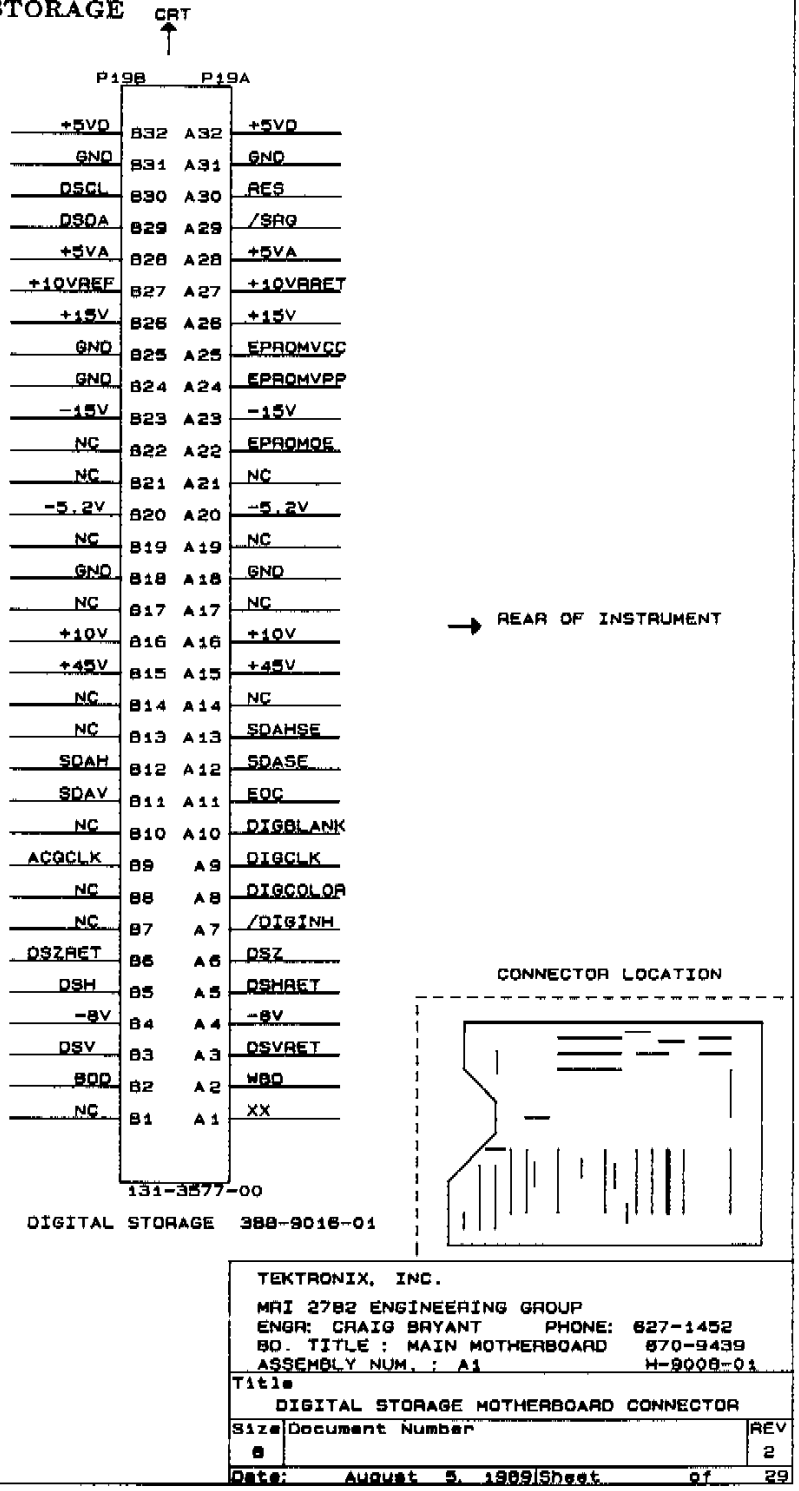
2.8 P17 - LOG PROCESSOR



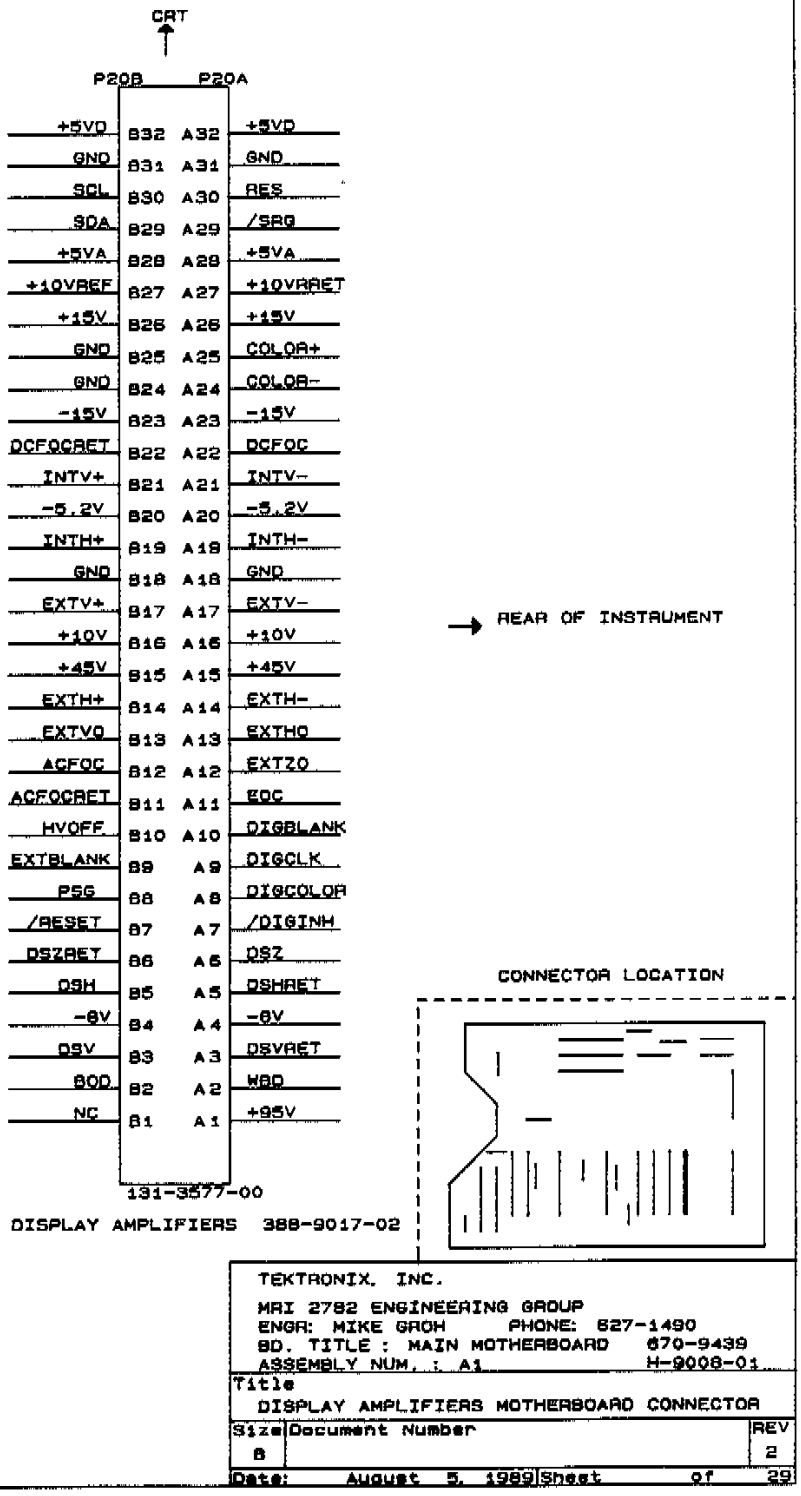
2.9 P18 - VIDEO PROCESSOR



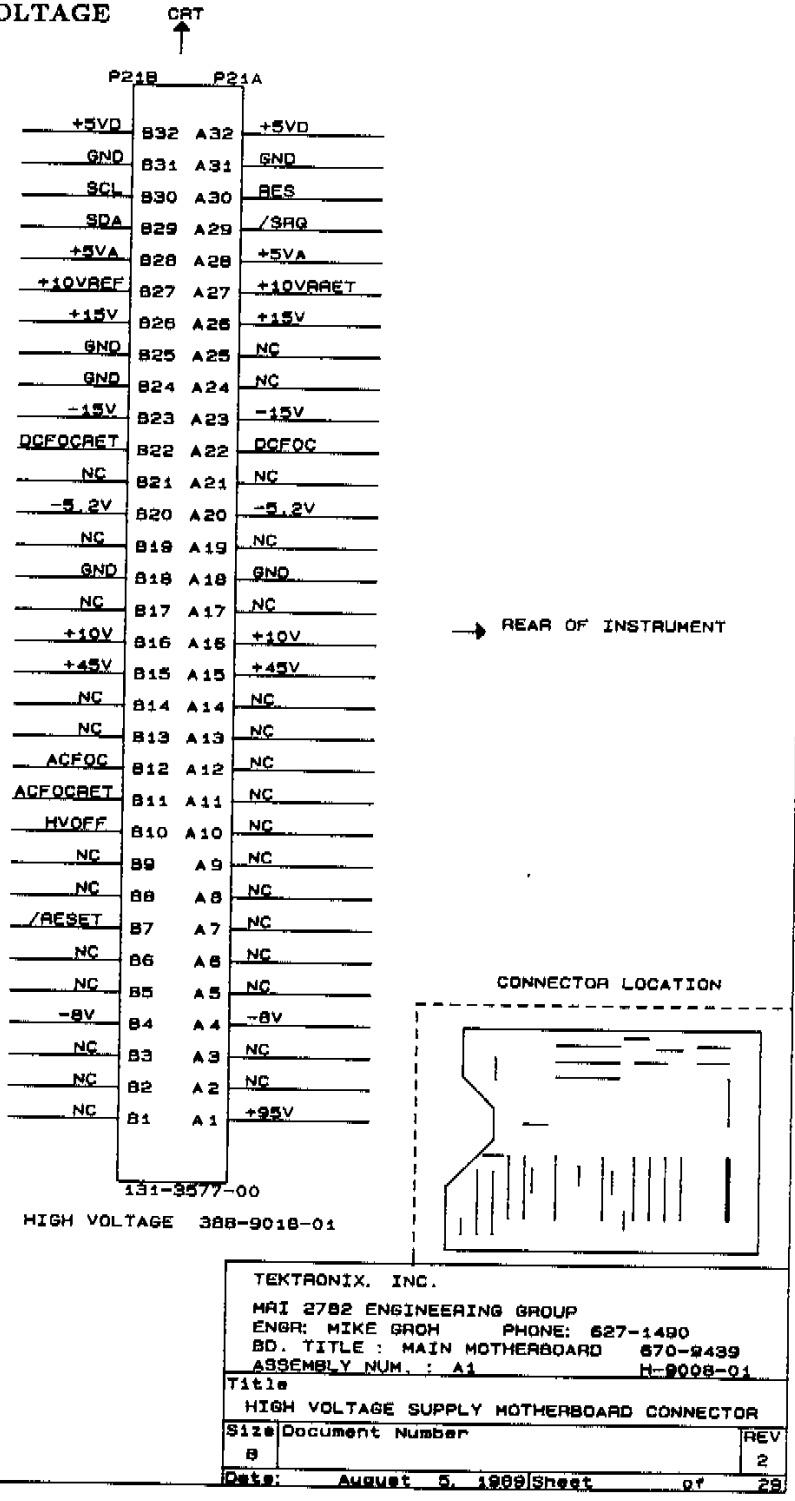
2.10 P19 - DIGITAL STORAGE



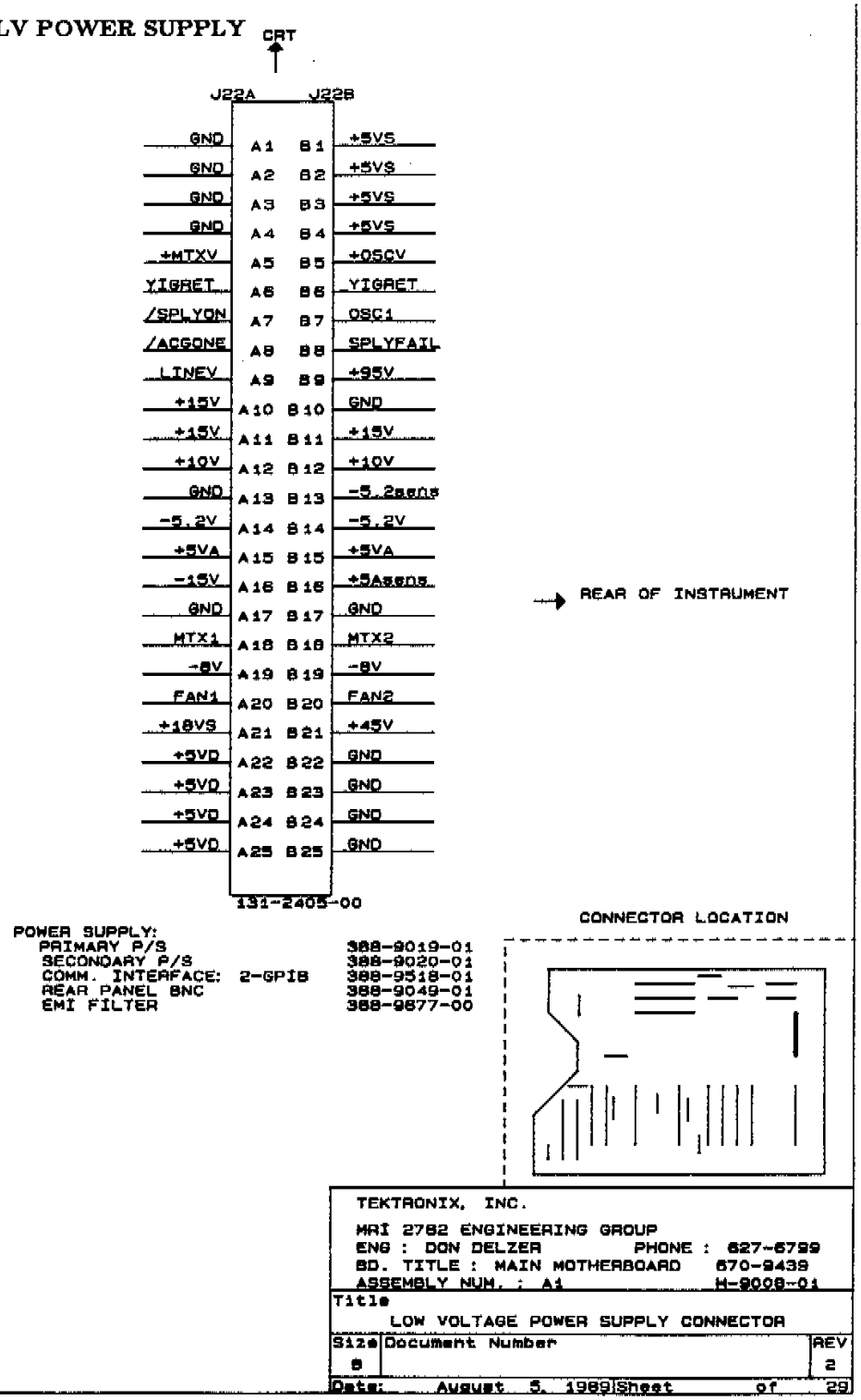
2.11 P20 - DISPLAY AMPLIFIERS



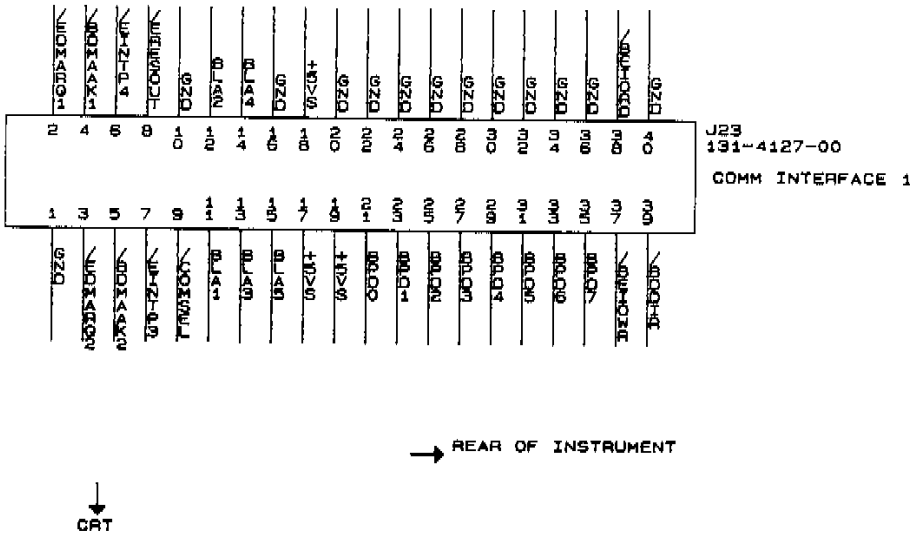
2.12 P21 - HIGH VOLTAGE



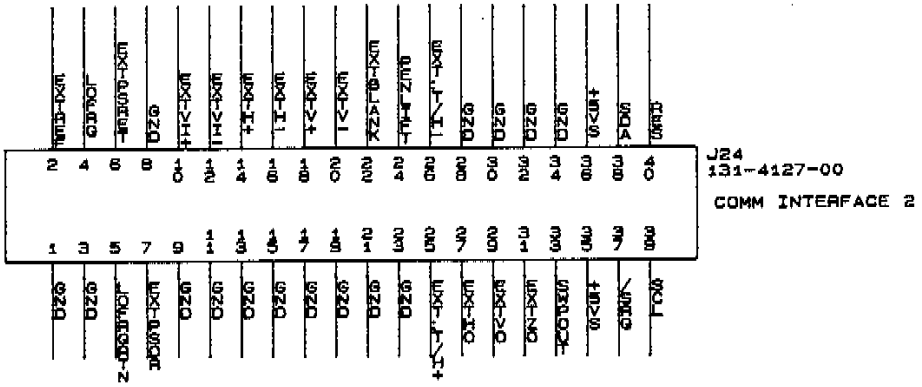
2.13 J22 - LV POWER SUPPLY



2.14 J23 - COMM INTERFACE 1



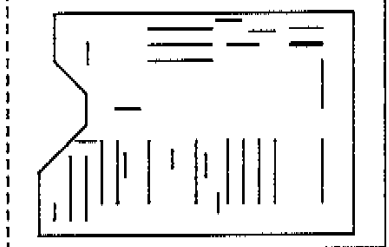
2.15 J24 - COMM INTERFACE 2



REAR OF INSTRUMENT

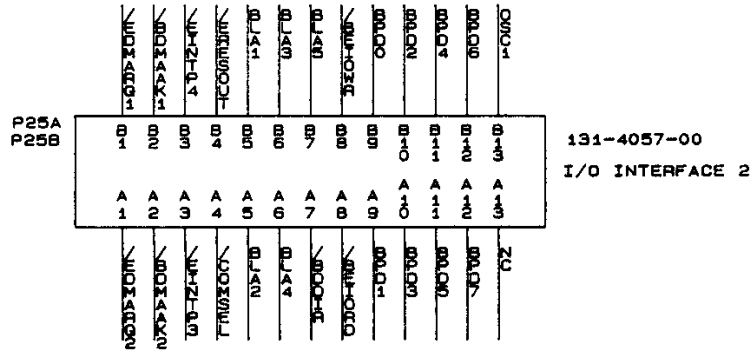
CRT

CONNECTOR LOCATION



TEKTRONIX, INC.		
MRI 2782 ENGINEERING GROUP		
ENG : GEORGE RICH	PHONE :	627-6055
BD. TITLE : MAIN MOTHERBOARD		670-9439
ASSEMBLY NUM. : A1		H-9008-01
Title: COMMUNICATIONS INTERFACE 2 CONNECTOR		
Size: B	Document Number	REV: 2
Date: August 5, 1989	Sheet of	28

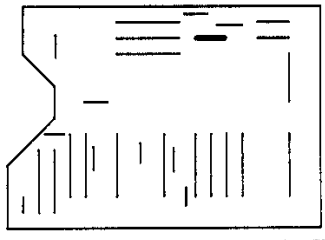
2.16 P25 - I/O INTERFACE 2



→ REAR OF INSTRUMENT

↓ CRT

CONNECTOR LOCATION



TEKTRONIX, INC.

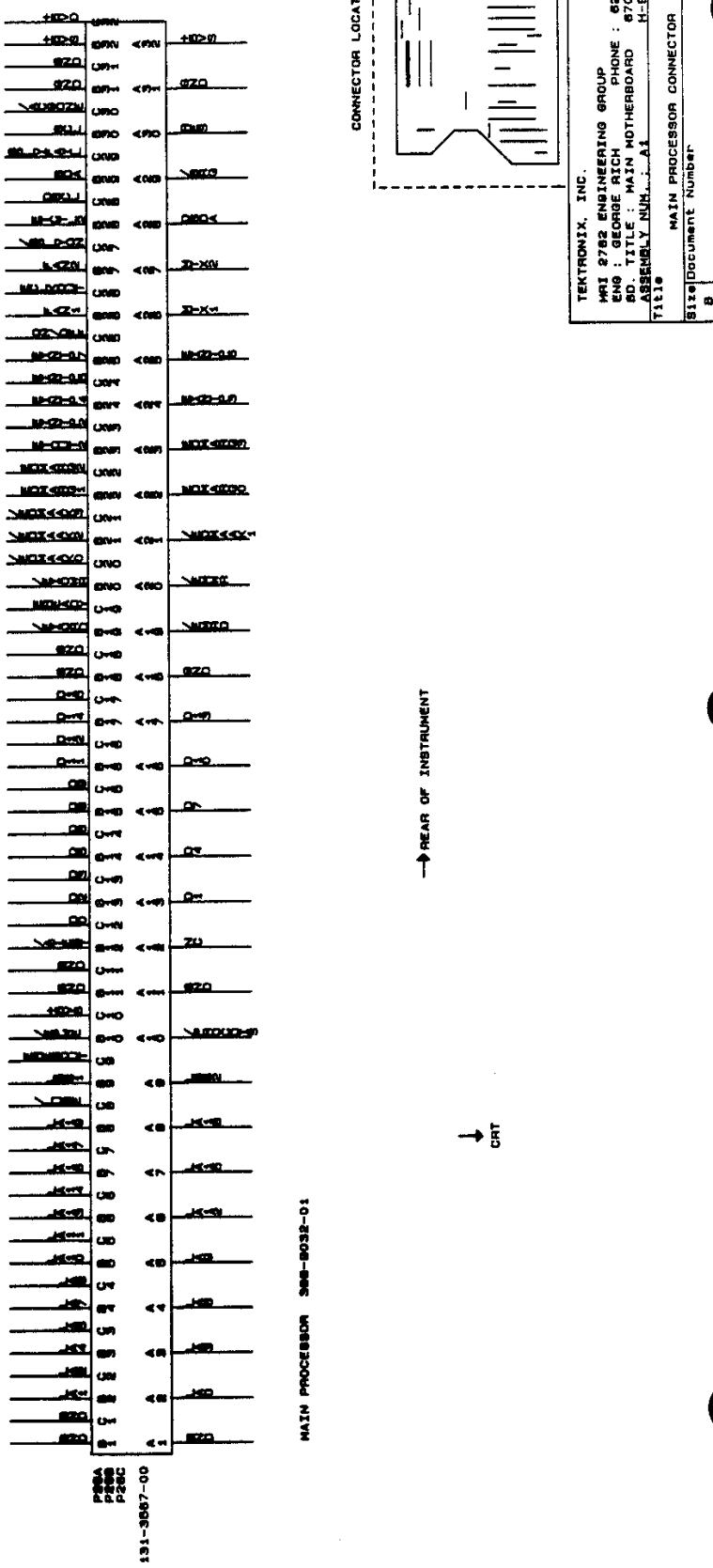
MRI 2782 ENGINEERING GROUP
ENG : GEORGE RICH PHONE : 627-6055
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
I/O INTERFACE 2 CONNECTOR

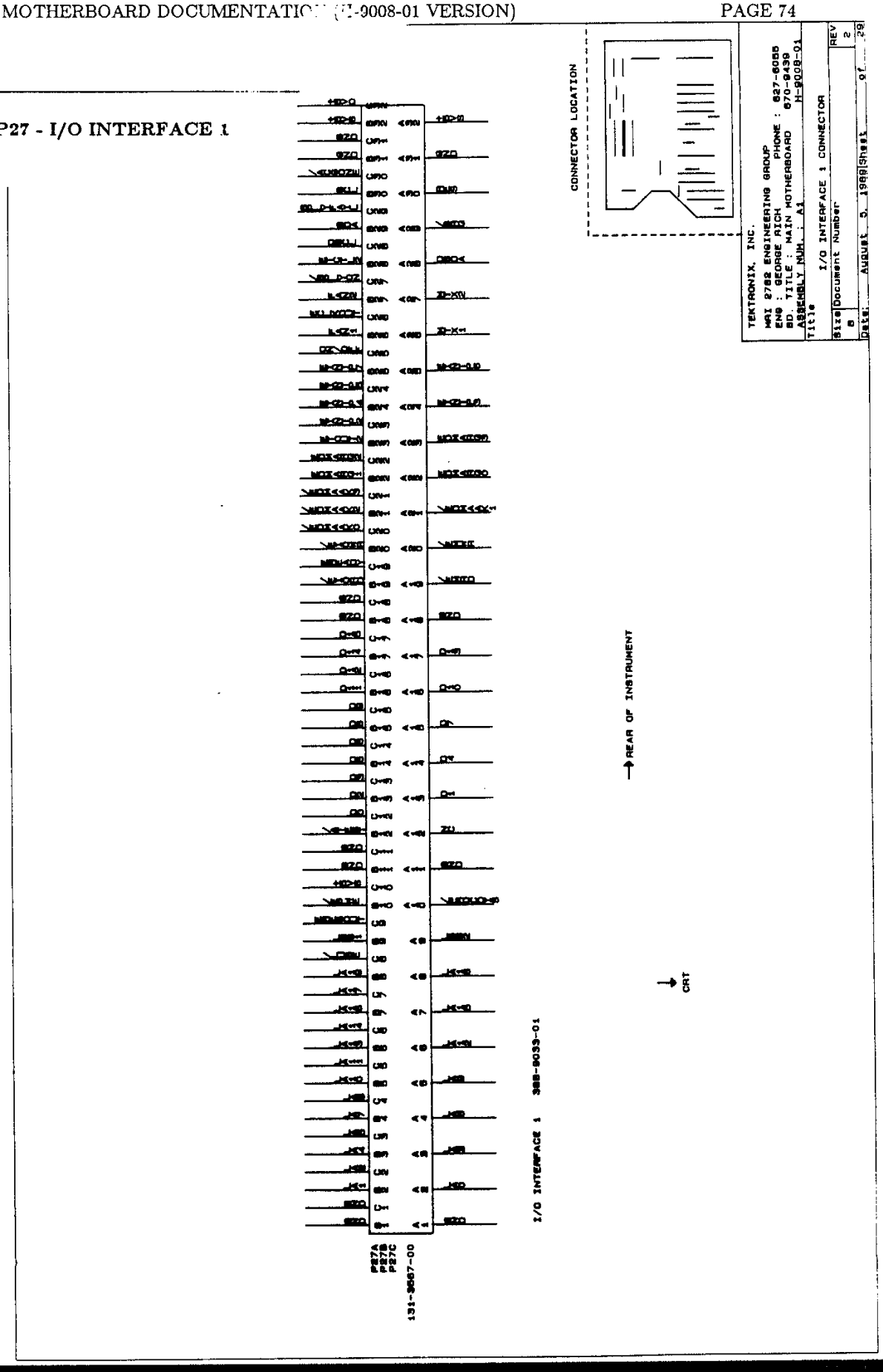
Size	Document Number	REV
B		2

Date: August 5, 1989 Sheet of 29

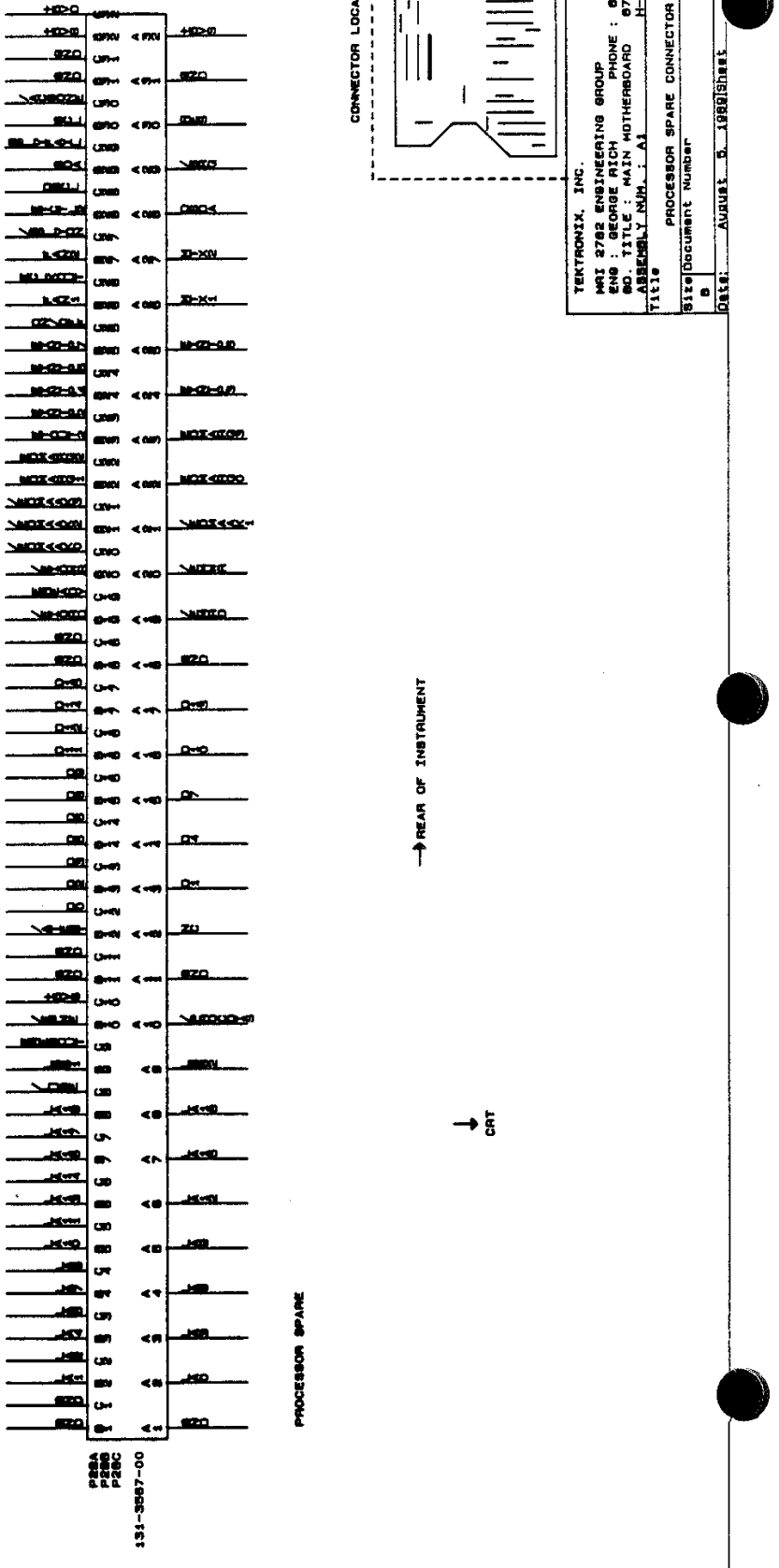
2.17 P26 - MAIN PROCESSOR



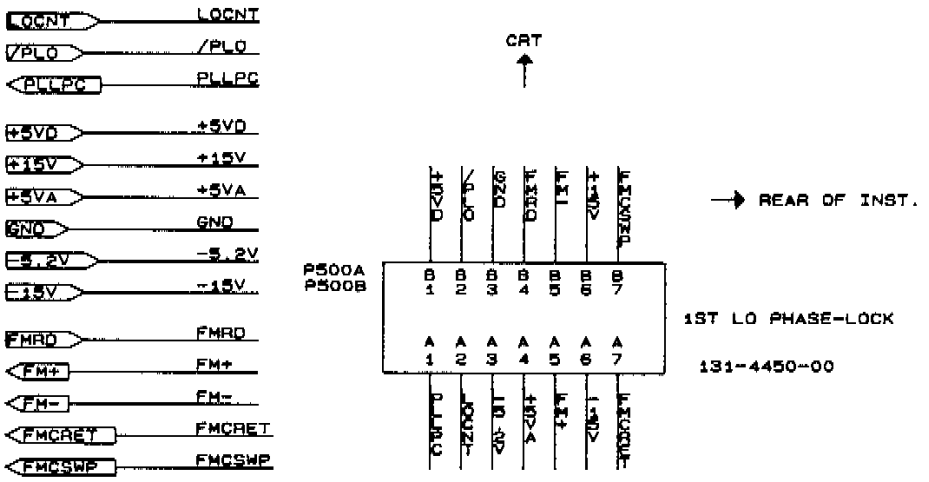
2.18 P27 - I/O INTERFACE 1



2.19 P28 - PROCESSOR SPARE



2.20 P500 - MICROWAVE PHASE-LOCK



1ST LO PHASE-LOCK
F(S) DRIVER : 388-9727-00
STROBE LO : 388-9709-02

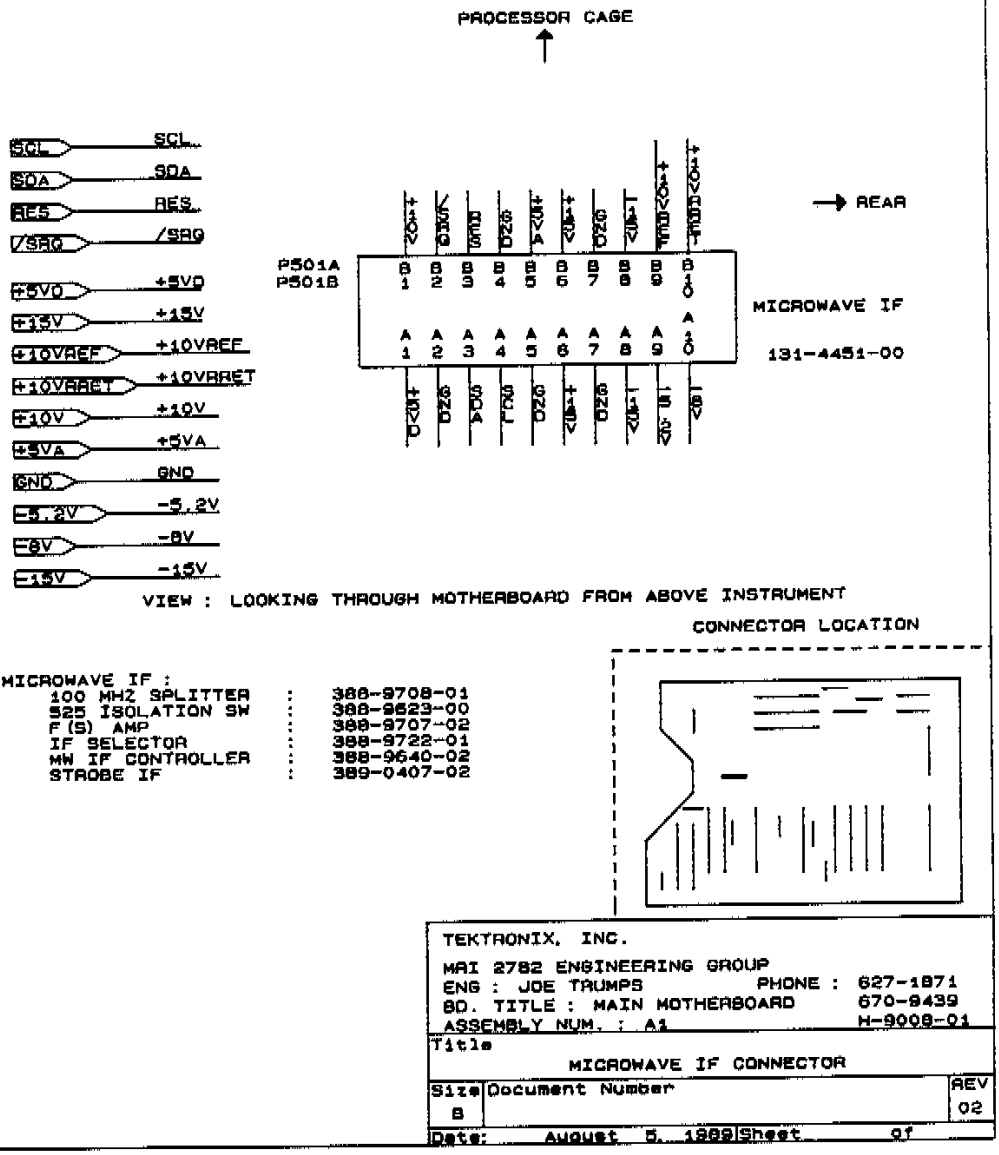
TEKTRONIX, INC.
MAI 2782 ENGINEERING GROUP
ENG: MIKE GROH PHONE : 627-1490
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
1ST LO PHASE-LOCK MOTHERBOARD CONNECTOR

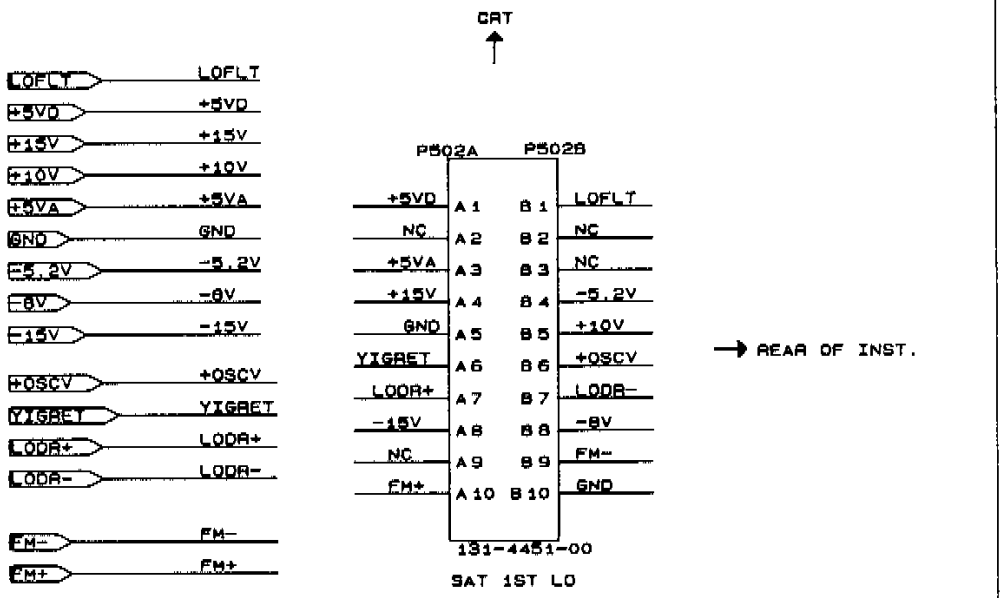
Size	Document Number	REV
B		02

Date: August 5, 1989 Sheet of

2.21 P501 - MICROWAVE IF

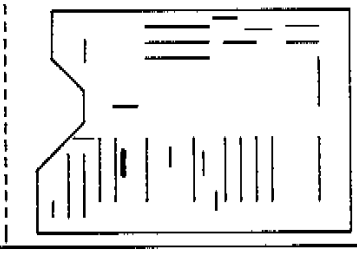


2.22 P502 - SATURN 1ST LO



VIEW : LOOKING THROUGH MOTHERBOARD FROM ABOVE INSTRUMENT

CONNECTOR LOCATION



SATURN 1ST LO
YTO DRIVER : 388-9642-01
YTO INTERFACE : 388-9641-02

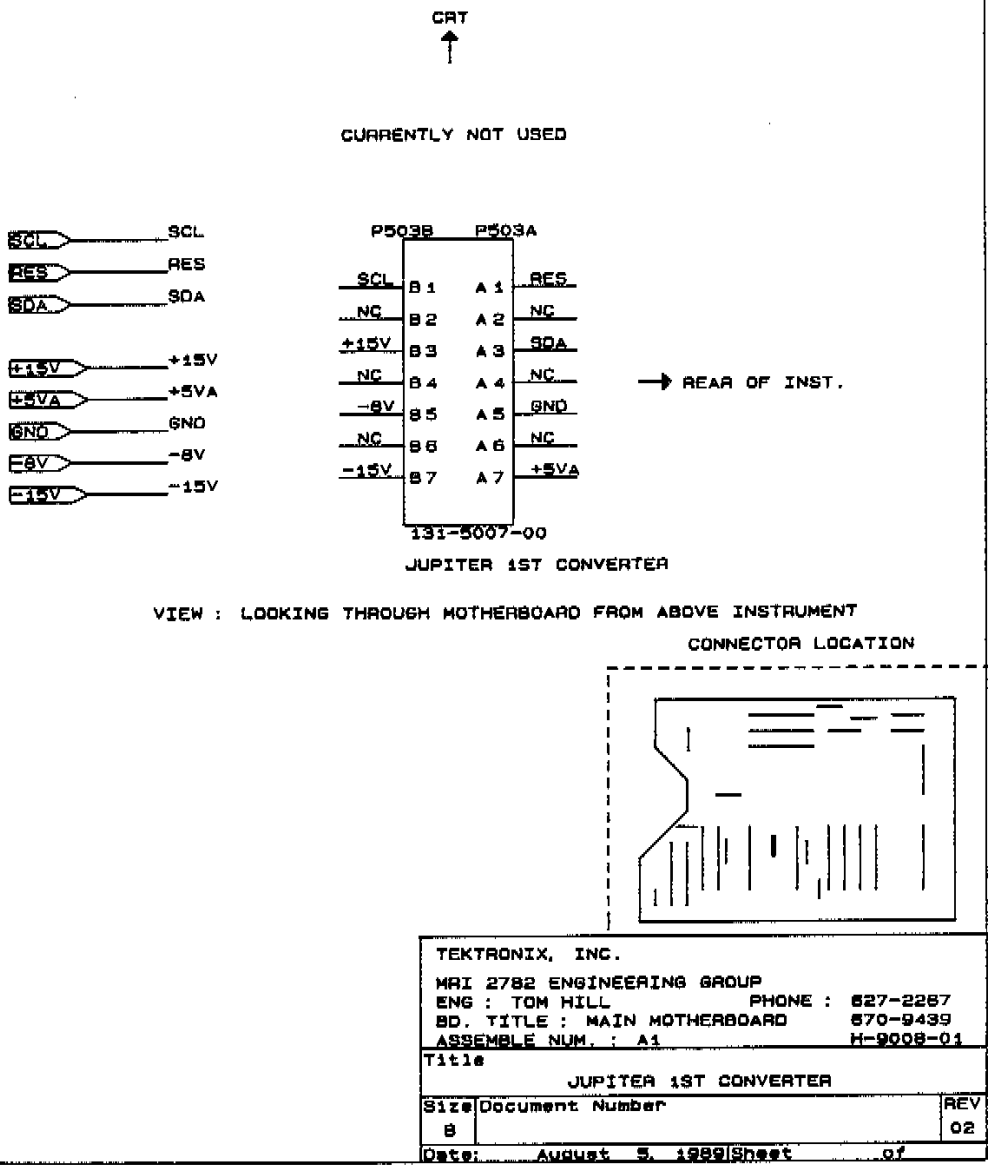
TEKTRONIX, INC.
MRI 2782 ENGINEERING GROUP
ENG : GORDON LONG PHONE : 627-1461
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
SATURN 1ST LO CONNECTOR

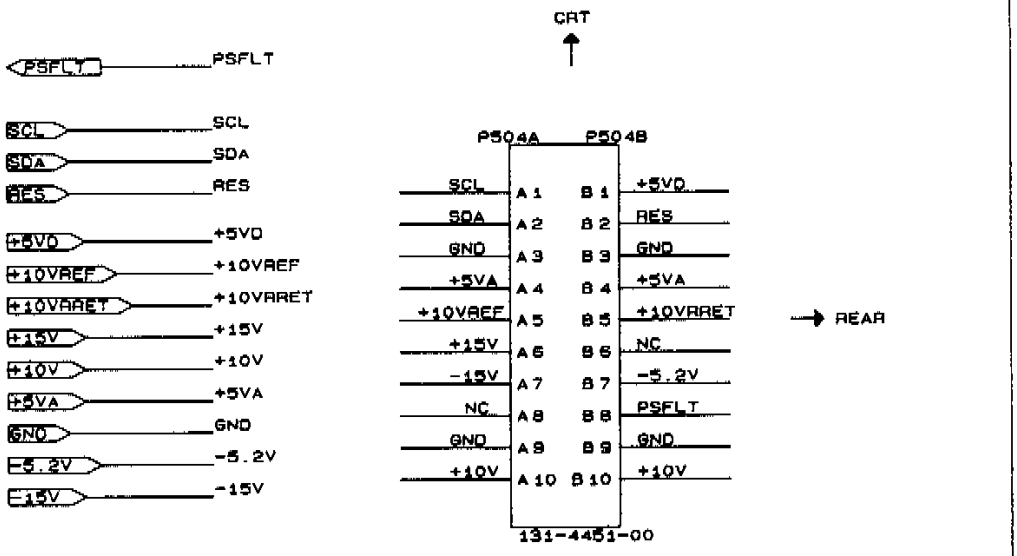
Size B | Document Number | REV 02

Date: August 5, 1989 Sheet of

2.23 P503 - JUPITER 1ST CONVERTER

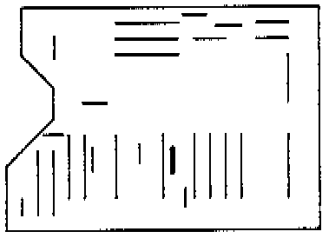


2.24 P504 - SATURN MTX CONTROL



VIEW : LOOKING THROUGH MOTHERBOARD FROM ABOVE INSTRUMENT

CONNECTOR LOCATION



SATURN MTX CONTROL

SATURN MTX CONTROL	:	388-9621-01
SW DIPLEXER INT	:	388-9756-01
SW HYBRID IN	:	388-9747-01

TEKTRONIX INC.

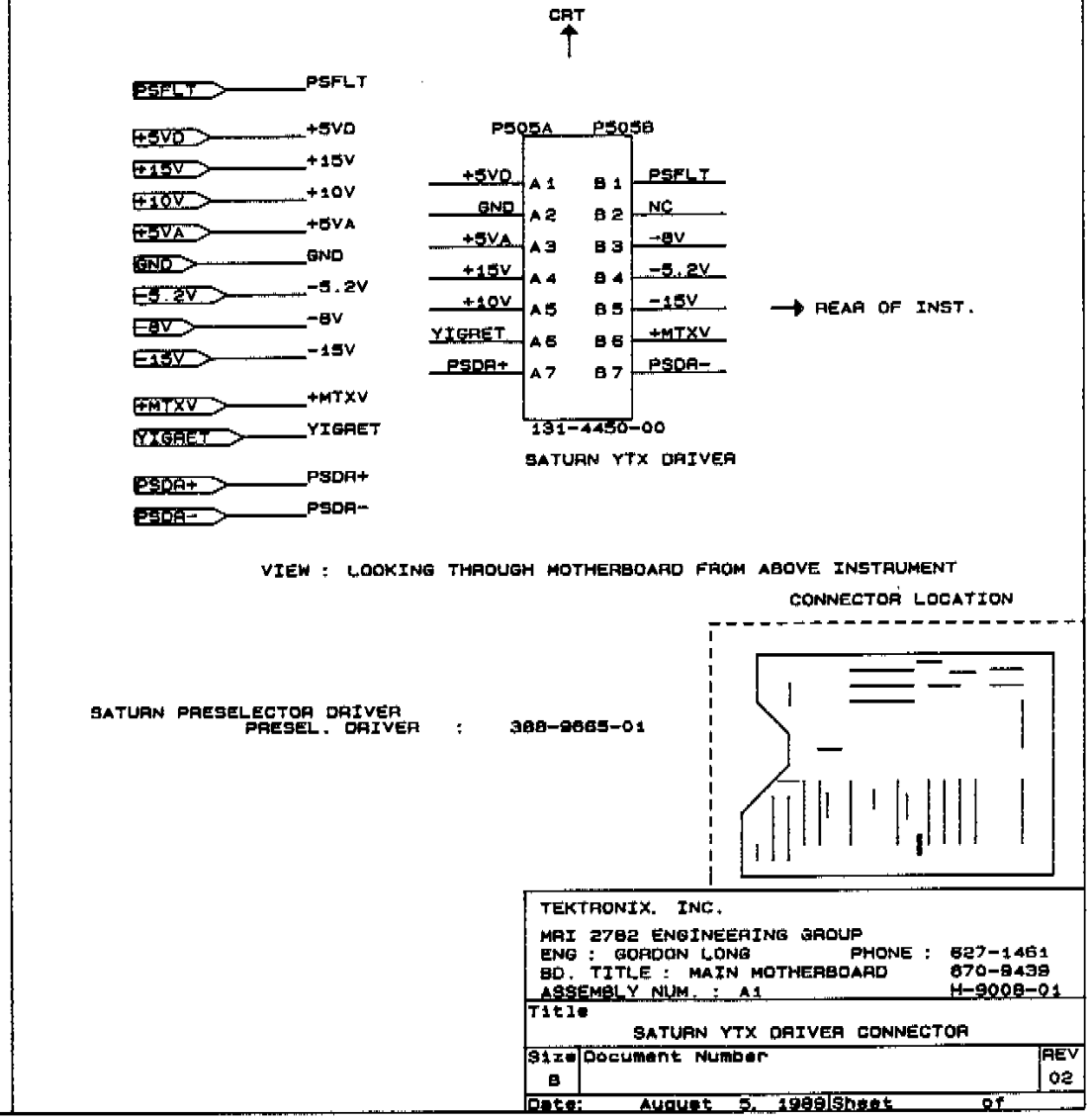
MAI 2782 ENGINEERING GROUP
ENG : GORDON LONG PHONE : 627-1461
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
SATURN MTX CONTROL CONNECTOR

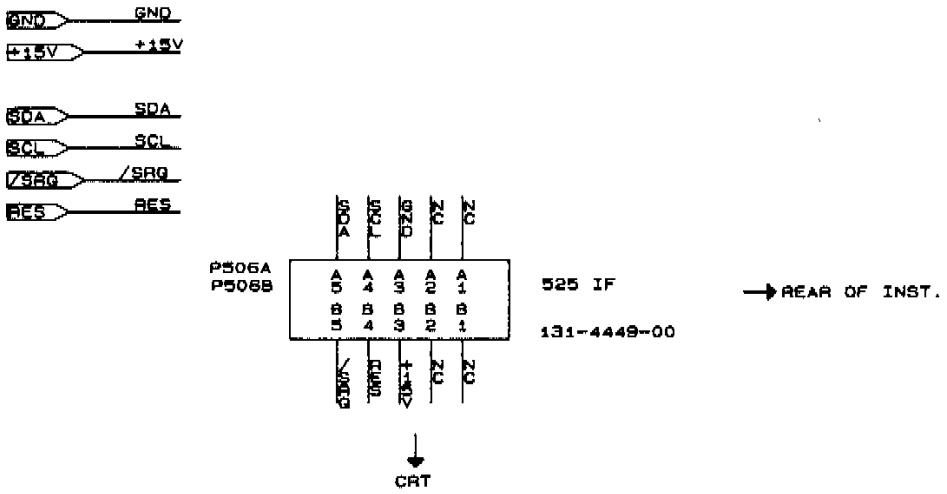
Size	Document Number	REV
B		02

Date: August 5, 1989 Sheet of

2.25 P505 - SATURN PRESEL DRVR



2.26 P506 - 525 IF

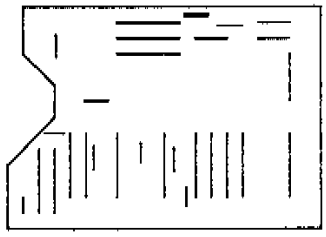


VIEW : LOOKING THROUGH MOTHERBOARD FROM ABOVE INSTRUMENT

525 IF

525-IF MIXER	:	388-9012-01
525-IF LO AMP	:	388-9013-02
525-IF INTERFACE	:	388-9014-02

CONNECTOR LOCATION



TEKTRONIX, INC.

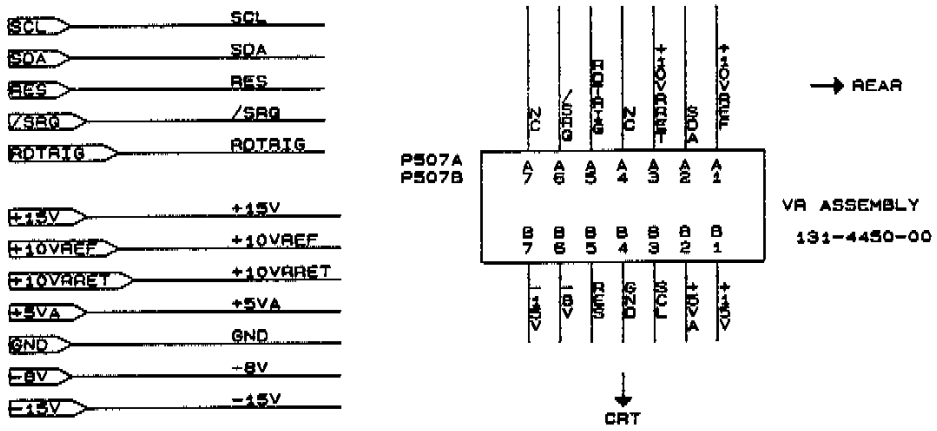
MRI 2782 ENGINEERING GROUP
ENG : DON DELZER PHONE : 627-6799
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title: 525 IF CONNECTOR

Size	Document Number	REV
B		02

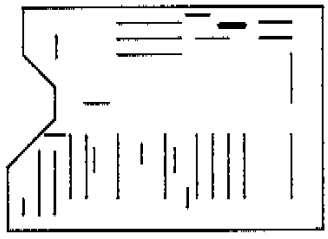
Date: August 5, 1989 Sheet of

2.27 P507 - VR ASSEMBLY



VIEW : LOOKING THROUGH MOTHERBOARD FROM ABOVE INSTRUMENT

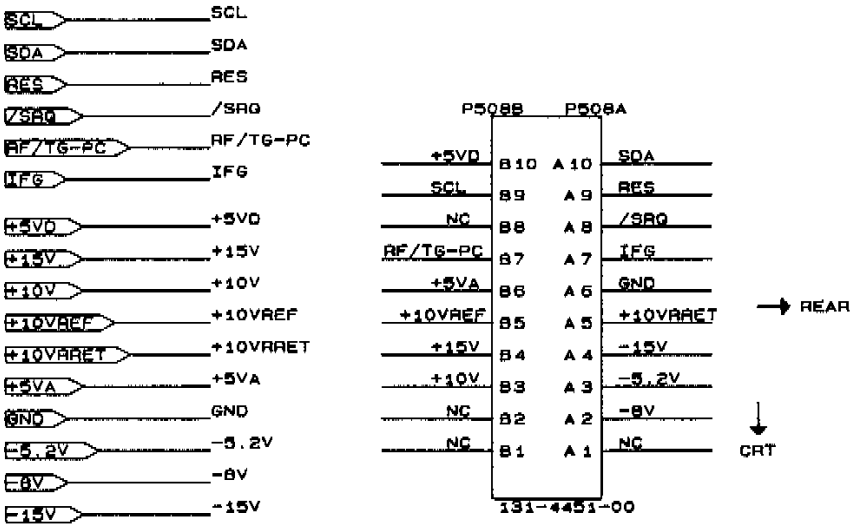
CONNECTOR LOCATION



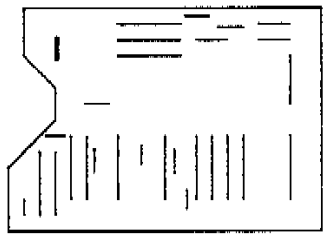
VR ASSEMBLY
VR #1 : 388-9004-01
VR #2 : 388-9005-02
VR #3 : 388-9006-02
VR #4 : 388-9234-01

TEKTRONIX INC		
MRI 2782 ENGINEERING GROUP		
ENG : MARC RANGER	PHONE :	627-4186
BD. TITLE : MAIN MOTHERBOARD		670-9439
ASSEMBLY NUM. : A1		H-9008-01
Title: VR ASSEMBLY CONNECTOR		
Size: B	Document Number	REV: 02
Date: August 5, 1989	Sheet of	

2.28 P508 - SATURN CALIBRATOR



CONNECTOR LOCATION



SATURN CALIBRATOR
100 MHZ @ 6.4 GHZ : 388-9828-01
REG/SERIAL INTERFACE : 388-9827-01

TEKTRONIX INC

MAI 2782 ENGINEERING GROUP
ENG : CRAIG BRYANT PHONE : 627-1452
BD. TITLE : MAIN MOTHERBOARD 670-9439
ASSEMBLY NUM. : A1 H-9008-01

Title
SATURN CALIBRATOR CONNECTOR

Size	Document Number	REV
B		02

Date: August 5, 1989 Sheet of

Keyboard Service Commands

These are the commands available in the RS-232 keyboard command mode using the Processor Extender Board (part of the 2782 Service Kit). Bold faced characters are keyboard commands, and those in italics are variables that may be selected for the command.

achp *0 / 1*

Select whether chop/alt display is automatically selected. 1 selects auto chop/alt, 0 selects manual chop/alt.

acun *0 / 1*

Turn unconditional acquisition on (1) or off (0).

adel *time*

Set alt delay, in seconds.

atda *att_idx atten*

Enter atten cal data value. "att_idx" is the attenuation index (0-7); "atten" is the attenuation in dB.

beat

Count the beat note from the phase gate, using 1024 as the period counter prescale value.

bofs *band att_idx offset*

Enter band offset value. "band" is the current instrument band number (0-4); "att_idx" is the attenuation index (0-7); "offset" is the offset in dB. Offset for band 0 should always be 0.0 dB. Also sets the hardware.

boli

Print list of band offset values.

`bost`

Store band offset values into NVRAM.

`bswe` *0|1*

Enable (1) or disable (0) backward sweep acquisitions. (BSPD bit on video processor).

`bwfg` *bw_idx gain*

Enter the fine gain level into the resbw cal data. "bw_idx" is the resbw table index; "gain" is the gain, in dB, required to make the reflvl come out right. Also sets the hardware.

`bwlv` *bw_idx bw_lvl*

Enter the bw level dac value into the resbw cal data. "bw_idx" is the resbw table index; "bw_lvl" is the dac value in hex. Also sets the hardware.

`bwrs` *bw_idx rs*

Enter RS value into resbw cal data. "bw_idx" is the resbw table index. "rs" is hex number equal to 2*rs1 + rs2; i.e the 2's bit is rs1 and the 1's bit is rs2. Also sets the hardware.

`bwvr` *bw_idx vbw*

Enter the hex "vbw" dac value into the resbw cal data. "bw_idx" indicates the resbw table index. Also sets the hardware.

`cdel` *min max*

Select min and max chop delay times. "min" and "max" have values ranging from 0 to 3. See display amp EMS for details.

`cler`

Clears all errors by running NoErrorReport().

`clvl` *lvl*

Enter internal calibrator signal level into current cal data. "lvl" is the signal level at the input connector, in dB, that is equivalent to the internal calibrator level.

`cmem`

Returns the amount of memory used.

`cntv` *0|1*

Set continuous vertical data out bit on video processor. "1" to enable, "0" to disable.

`cnvr` *reflvl old_units new_units*

Converts "reflvl" in "old_units" to the equivalent value in "new_units." "old_units" and "new_units" are as follows:

0	dBm
1	dBmV
2	Volts
3	Watts
4	User (Not implemented)
5	dBV
6	dBuV
7	dBuW
8	dBuV
9	Current instrument units

`ctps` *pos1 pos2*

Set the signal counter positions to "pos1" and "pos2".

`dcal` *source data_id*

Print (list) cal data. Vertical cal trace must have been enabled ("vtra 1).

"source" indicates where the data to be printed comes from:

0	Generic cal data (ROM)
1	Default cal data (NVRAM)
2	Current cal data (RAM)

"data_id" indicates which data is to be printed:

0	All data
1	Resonator tracking data
2	Display law data
3	Gain step data
4	ResBW data
5	Attenuator and calibrator data
6	Acquisition peak detector data
7	Log correction data

`dscr` *0 | 1*

Disable/enable frequency corrections. A 0 argument will enable frequency corrections (closed loop). A 1 argument will disable frequency corrections (open loop).

`dsen` *0 | 1*

Set display amp display enable; 1 enables display, 0 disables display.

`dsrc` *vert_src hor_src*

Select vertical and horizontal source for the real time display. Source selections are:

0 ground
1 internal
2 external

`echp`

Execute auto chop/alt routine.

`erde` *0 | 1*

BDisplayErrors - Turns on or off the display of errors.

`erdm` *0 | 1 mask*

BErrDispMask - Turns mask bits on or off, effects display of errors and warnings by instrument functional section. "mask" is a bits8 value.

`erdw` *0 | 1*

BDisplayWarnings - Turns on or off the display of warnings.

`erep` *error_number*

Report a error specified by the decimal argument "error_number".

`erle` *0 | 1*

BLogErrors - Turns on or off the logging of errors.

`erlm mask 0|1`

BErrLogMask - Turns mask bits on or off, effects logging of errors and warnings by instrument functional section. "mask" is a bits8 value.

`erlw 0|1`

BLogWarnings - Turns on or off the logging of warnings.

`eyef periods`

Count the 4 MHz IF. "periods" specifies the period counter prescale value to use.

`f129`

Count the 129 MHz synthesizer, using 1024 as the period counter prescale value.

`f565`

Count the 565 MHz synthesizer, using 1024 as the period counter prescale value.

`facc file`

See if the specifed NVRAM, EEPROM, or EPROM file is accessable. Argument "file" specifies what file to check. To see if NVRAM file "abc" is accessable, enter "facc RAM/abc". To see if EEPROM file "def" is accessable, enter "facc EEPROM/def". To see if EPROM file "ghi" is accessable, enter "facc EPROM/ghi".

`fcat file`

Dump the contents of a NVRAM, EEPROM, or EPROM file in hex format. Argument "file" specifies what file to dump. To dump NVRAM file "abc", enter "fcat RAM/abc". To dump EEPROM file "def", enter "fcat EEPROM/def". To dump EPROM file "ghi", enter "fcat EPROM/ghi".

`fclo file_descriptor`

Close a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt".

fcrt *file*

Create a silicon disk file for reading and writing in NVRAM or EEPROM and return a file descriptor of the created file. The file to be created is specified by the argument "file". To open a NVRAM file "abc", enter "fopn RAM/abc". To open a EEPROM file "def", enter "fopn EEPROM/def".

fdfo *0 | 1*

Enable/disable the strobe to the phase gate. A 0 argument will disable the strobe. A 1 argument will enable the strobe. To obtain a strobe, the fractional N should be set to the proper value for the desired strobe frequency.

fdir *file_system*

Do a directory list of the specified file system. If argument file_system is "RAM" the contents of the NVRAM silicon disk is displayed. If argument file_system is "EEPROM" the contents of EEPROM silicon disk is displayed. If argument file_system is "EPROM" the contents of EPROM silicon disk is displayed.

fldz

Fill the EEPROM flatness tables with zeros.

flgn *bits*

Set the pre- and post-filter gain bits on the VR. "bits" simultaneously sets both pre- and -post filter gain as follows:

1	-6 dB pre-filter, +6 dB post-filter
2	-6 dB pre-filter, +6 dB post-filter
4	-6 dB pre-filter, +6 dB post-filter

fltz *0 | 1*

Set the termination resistance Z on the VR. 0 selects low Z; 1 selects high Z.

fnuk *file_system*

Delete all files in the specified file system. If file_system = 0, all NVRAM files will be removed. If file_system = 1, all EEPROM files will be removed.

`fopn file`

Open a file for reading and writing in NVRAM, EEPROM, of EPROM (read only). and return a file descriptor of the opened file. The file to be opened is specified by the argument "file". To open a NVRAM file "abc", enter "fopn RAM/abc". To open a EEPROM file "def", enter "fopn EEPROM/def". To open a EPROM file "ghi", enter "fopn EPROM/ghi".

`fpos position`

Set the frequency reference position to "position"

`fred file_descriptor bytes`

Read data from a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". The argument "bytes" specifies how many bytes to read from the file.

`fren from to`

Rename a silicon disk file. The argument "from" is the name of the file to be renamed. The argument "to" is the name the file will be moved to.

`fsck file_system`

Run a file system consistency check on the specified file system. If argument file_system is "RAM" the NVRAM drive is checked. If argument file_system is "EPROM" the EPROM drive is checked. If argument file_system is "EEPROM" the EEPROM drive is checked.

`fsdf file_system`

Show the amount of free space left for the specified file system. If argument file_system is "RAM" the contents of the NVRAM silicon disk is displayed. If argument file_system is "EEPROM" the contents of EEPROM silicon disk is displayed. If argument file_system is "EPROM" the contents of EPROM silicon disk is displayed.

`fsek file_descriptor mode offset`

Seek to a position in a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". If argument "mode" is 0, the file pointer is set to "offset" bytes. If argument "mode" is 1, the file pointer is set to the current location plus "offset" bytes. If argument "mode" is 2, the file pointer is set to the size of the file plus "offset" bytes. The argument "offset" is the number of bytes to move within the file.

`fswp 0|1`

Enable (1) or disable (0) fast sweep mode of video processor.

`ftra [+-]source...`

Enable/disable tracing of the specified frequency control "source(s)". A leading "+" will enable the "source" while a leading "-" will disable the "source". More than one "source" may be specified, each with its own leading "+" or "-". The allowable values for "source" are:

129 29 count lohi (Jupiter only) lolo pres span sweep yig

`fwrt file_descriptor string`

Write a string to a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". The argument string is a quoted string of the text to write to the file.

`fyig frequency`

Perform a FindYIG. FindYIG assumes that the YTO is at "frequency".

`ganc dac`

Set the coarse gain dac on the VR to the hex value "dac." The dac is actually a set of bits, each of which selects a gain setting. The bits are decoded as follows:

bits 0-2	1st gain stage of VR1
bits 3-5	3rd gain stage of VR1 Meaningful values are:
24	0 dB
22	9 dB
12	18 dB
11	27 dB
09	36 dB

`ganf dac`

Set fine gain dac on VR. This is the 2nd gain stage on VR1. "dac" is a hex value corresponding to a 12 dB gain range.

`gilb dac`

Set the gilbert (dB/div) dac on the log processor. "dac" is a 12 bit hex value (000-fff).

`glbq`

Print current value of the gilbert multiplier (dB/div) dac, in hex.

`gmax` *max_step*

Enter max VR gain step into current cal data. "max_step" is an integer value with units of dB.

`gmlg` *path slope icept*

Enter dB/div data into current cal data. "path" is the log IF frequency: 0 for 4 MHz; 1 for 25 MHz. "slope" and "icept" are the slope and offset parameters characterizing the dB/div vs gilbert dac relationship: dac = (dB/div)/slope + icept.

`gnuw` *gain*

Set the value of the microwave IF gain step value to "gain".

`gred` *gain*

Set the output gain steps on VR 3. "gain" selects the gain as follows:

0	0 dB
1	10 dB
2	20 dB

`hgpt` *dac*

Set the hinge position dac in the log preprocessor. "dac" is the dac value in hex (000-fff).

`hofs` *path dac*

Enter the zero hinge power dac value into the current display law cal data, and set the corresponding hardware. "path" is 0 for 4 MHz log amp, 1 for 25 MHz. "dac" is the log offset dac in hex (000-fff).

`ifen` *0|1*

Enable/disable the IF. A 0 argument will disable the IF. A 1 argument will enable the IF.

`l129`

Lock the 129 MHz synthesizer to the 565 MHz synthesizer.

`lacq` *0 | 1*

Set log acquisition bit on video processor. A log acquisition is acquired when the bit is changes from 0 to 1. The bit is normally set to 0.

`lcen` *0 | 1*

Enable (1) or disable (0) log correction.

`lcev` *0 | 1*

Sets log correction evaluation mode; "1" enables eval mode, "0" disables eval mode.

`lifd` *band att_idx*

List flatness data for "band" and "att_idx"

`linh` *dac*

Enter the hinge position dac number for lin mode into current display law data. "dac" is in hex (000-fff). Also sets the hardware.

`litd`

Print current lo29 and tune dac values for VR.

`livr`

Print contents of the VR registers.

`lo29` *periods*

Count the 29 MHz LO. "periods" specifies the period counter prescale value to use.

`lofs` *val*

Sets log offset to "val" in dB.

`log4 0|1`

Set the 4 MHz mode of the log processor. An argument of 0 indicates 4 MHz mode; 1 indicates 25 MHz mode.

`logh dac`

Enter the hinge position dac number for log mode into current display law data. "dac" is in hex (000-fff). Also sets the hardware.

`lolo`

Count LOlo using a period counter prescale value of 512.

`minb bits`

Set the VR resonators to minimum bandwidth mode. "bits" is a hex number, each bit of which sets a single resonator to minbw mode; a high bit (1) selects minbw mode, while a low bit (0) selects normal mode. The bits are decoded as follows:

bit 0	resonator 0
bit 1	resonator 1
bit 2	resonator 2
bit 3	resonator 3
bit 4	resonator 4
bit 5	resonator 5

`mono 0|1`

Set monochrome display on (1) or off (0).

`nres rs`

Set RS1/RS2 on the VR. "rs" equals 2*rs1 + rs2; i.e. rs1 is the 2's bit while rs2 is the 1's bit.

`nsge 0|1`

Enable (1) or disable (0) min/max noise signal in acquisition data. (NSGE bit on video procesor).

`offs dac v`

Set the log offset dac on the log processor. "dac" is a 12-bit hex value (000-fff).

`ofsq`

Print contents of log offset dac on log processor.

`ofsr path offset_res`

Enter relolution of the log offset dac ("offset_res") in dB/lsb. "path" indicates the log IF: 0 for 4 MHz; 1 for 25 MHz.

`otda`

Performs a sweep and prints out level of signal in screen units (0-1023). Signal is assumed to be of constant level.

`pkgn dac`

Enter peak detector gain dac value into cal data. "dac" is in hex. Also sets the hardware.

`pkmn dac`

Enter min peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.

`pkms dac`

Enter max sample peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.

`pkmx dac`

Enter max peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.

`pkof dac`

Enter peak detector offset dac value into cal data. "dac" is in hex. Also sets the hardware.

`prcd`

Calculate the preselector slope and offset DAC values for the bands for which sample peaks have been taken with the "prfo" command.

`prfl`

Flush the current list of preselector peak samples taken with the "prfo" command.

`prfo`

Find the line equation relating the preselector slope and offset DACs at the current frequency and reference level. If the line is successfully found, save the line for use by the "prcd" command.

`prio` *task_number task_priority*

Prioritize a task. The argument "task_number" specifies which task to re-prioritize. Valid values are listed in Task.h. The argument "task_priority" specifies the new priority for the task. A task of "0" is the lowest priority, "255" is the highest priority.

`prsl` *band slope offset*

Set the preselector slope and offset DACs for band "band" to "slope" and "offset" respectively. "band" specifies a preselected coax band, and ranges from 1 through 5.

`prsw`

Enter the preselector sweep adjustment mode. Follow the menu presented.

`rblv` *dac*

Set the resbw level dac on the VR. "dac" is the dac value in hex.

`rcnt` *div*

Count the frequency of the selected reference source. "Div" is the value which will be loaded into the divider in the reference oscillator module.

`rcpc`

Recall preselector cal data from NVRAM.

`recl`

Recalibrate the frequency control system.

`refl` *`reflvl`*

Set the reference level to "reflvl." Units are whatever the current instrument units are.

`relt` *`mode`*

Select real time mode: 0 selects digital storage display, 1 or 2 selects double channel real time display.

`rflt`

Read contents of flatness RAM on log processor.

`rlck` *`0 | 1`*

Lock or unlock the reference oscillator loop. 0 unlocks, 1 locks.

`rmhz` *`0 | 1`*

Turn the 1 MHz output from the reference oscillator module to the period counter on or off. 0 turns on, 1 turns off.

`rord`

Read and report the locked/unlocked and external power detected/not detected status of the reference oscillator module.

`rstr` *`SIC_address num_of_bytes`*

Recieve data from a SIC. The hex argument "SIC_address" specifies which SIC address to read from. The decimal argument "num_of_bytes" specifies how many bytes to read.

`rtra` *`0 | 1`*

Enable or disable the reflvl trace. 0 disables trace; 1 enables trace.

`rver`

Determine the hardware version of the reference oscillator which is installed.

`s129` *`frequency`*

Turn on and set the 129 MHz synthesizer to "frequency".

`satt atten_val`

Set the attenuator to "atten_val," in dB. This command sets only the attenuator, bypassing the reference level firmware entirely. Use of this command results in incorrect reference level and marker readouts.

`scal 0|1`

Calibrate the sweep. "0" does not print results, "1" does.

`schp 0|1`

Select chop (0) or alt (1) display mode.

`sdbg reg1 reg2 reg3`

Set the debug registers in the display amp. "reg1-3" are the registers in hex (0000-ffff).

`sfrn N`

Set the fractional N synthesizer value to "N". This control the 565 MHz synthesizer frequency.

`sllo value`

Set the "Last LO" bit pattern to "value"

`slol frequency precision`

Set LOlo to "frequency" within "precision" Hz.

`stgn gain`

Set the VR 1 dB gain steps to "gain," in dB.

`stnd type res_num dac`

Enter tune dac value into resonator tracking cal data. "type" is 0 for crystal resonators, 1 for LC. "res_num" is the resonator number (0-5). "dac" is the tune dac value in hex (00-ff). Also sets the hardware.

`svpc`

Save preselector cal data in NVRAM.

`swep`

Do a single sweep.

`swrc` *`range mintime`*

Set the minimum sweep time for sweep range "range" to "mintime"

`syig` *`frequency`*

Set the YTO to "frequency".

`tabl`

Display the current frequency calibration table.

`ttst` *`time`*

Test the processor timer by delaying "time" seconds between two printed messages.

`tund` *`bits`*

Load tune dacs with appropriate values from resonator cal data for the specified "bits" value. "bits" is the LC/crystal control byte as defined in the "xlcm" command.

`u129`

Unlock and turn off the 129 MHz synthesizer.

`unlk` *`file`*

Remove a file from NVRAM or EEPROM. The file to be removed is specified by the argument "file". To remove NVRAM file "abc", enter "unlk RAM/abc". To remove EEPROM file "def", enter "unlk EEPROM/def".

`uwif` *`0|1`*

Insert/remove the microwave IF attenuation

`vbws` *source*

Select the source for the video processor; 0 selects internal, 1 selects external.

`vers`

Print the FW version string.

`vout` *type*

Select rear pane video output type: 0 for real time, 1 for composite.

`vpth` *path_bits*

Set the VR path bits. "path_bits" is a collection of VR switches that the firmware treats as a single register on the VR. "path_bits" is decoded as follows:

0001	29 MHz count (VR 1)
0002	4 MHz path (VR 1)
0004	25 MHz path (VR 1)
0008	NBW for ringdown filter (VR 1)
0010	25 MHz ringdown oscillator (VR 1)
0020	XTAL filter (VR 1)
0040	3 MHz filter (VR 1)
0080	10 MHz filter (VR 1)
0100	29 MHz oscillator on/off (VR 1)
0200	BP filter (VR 3)
0400	LP filter (VR 3)
0800	25 MHz path (VR 3)
1000	4 MHz oscillator (VR 3)

Useful values include:

vpth 901 Route LO 29 signal to output of VR
vpth 532 Turn on ringdown oscillator
vpth 522 Turn off ringdown oscillator

`vpts` *0 | 1*

Set the test bit on the video processor. 1 turns on test mode, 0 turns it off.

`vres` *dac*

Set the variable bw dac (VBW) on the VR. "dac" is an 8-bit hex number (00-ff).

`vset`

Set up instrument for "xfrq" command.

`vtra` *0 | 1*

Enable or disable vertical cal trace. 0 disables trace, 1 enables trace.

`xfrq`

Count ringdown frequency of xtal resonator. Assumes instrument and VR have been properly set up with the "vset" command.

`xlcm` *bits*

Set the VR resonators to LC or crystal mode. "bits" is a hex number, each bit of which sets a single resonator to the desired mode mode; a high bit (1) selects LC mode, while a low bit (0) selects crystal mode. The bits are decoded as follows:

bit 0	resonator 0
bit 1	resonator 1
bit 2	resonator 2
bit 3	resonator 3
bit 4	resonator 4
bit 5	resonator 5

`xstr` *address num_bytes hex_byte...*

Send hex bytes to a SIC. The SIC address is specified by the hex argument "address". The number of bytes to be transmitted is specified by the decimal argument "num_bytes". The actual data to be sent is entered as hex numbers. The number of hex digits should match the argument "num_bytes". For example; to send hex digits 0x10, 0x43, 0xfe, and 0x32, to SIC address 0xde, enter "xstr de 4 10 43 fe 32"

Firmware Versions

The following table shows the compatibility of the various firmware versions supported in this instrument. When replacing firmware ROMs, be sure that the firmware version is compatible with the other firmware in the instrument. Incompatible versions are separated by a horizontal line. This table gives the firmware version and the part number suffix as printed on the ROM label. Also see *Updating Firmware* in the *Maintenance* section of this manual.

Table C-1. Firmware Version Compatibility

Date	Main Processor	IO Interface	Digital Storage
JUL 1989	1.3 (160-XXXX-00)	None	1.3 (160-XXXX-00)
NOV 1989	1.4 (160-XXXX-01)	None	1.3 (160-XXXX-00)

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages. If it does not, your manual is correct as printed.