

**TYPE 453
LECTURE
NOTES**

WRITTEN AND PRODUCED IN MARKETING TECHNICAL TRAINING

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I. INTRODUCTION

- A. The Type 453 is a transistorized portable oscilloscope designed to operate in a wide range of environmental conditions.
- B. General Information
 - 1. The Vertical system features dual-channel DC - 50 mc operation.
 - a. Calibrated vertical deflection factors from 5 mv to 10 volts/div are provided.
 - b. The two Input Preamps may be cascaded to provide a 1 mv/div deflection factor.
 - 2. The trigger circuits provide stable triggering over the full range of vertical frequency response.
 - a. A "bright line automatic" circuit is featured that, in the absence of triggers, causes the sweep to free run at a rate determined by the TIME/DIV control.
 - 3. The Time Base circuits provide a maximum sweep rate of .1 μ sec/div (10 nsec/div using the X10 magnifier).
 - a. Minimum sweep speed is 5 sec/div.
 - b. A delayed sweep is provided, with a range of .1 μ sec/div to .5 sec/div.
 - 4. Accurate X-Y measurements may be made with Channel 1, providing horizontal deflection, and Channel 2, providing the vertical deflection.
 - a. Both vertical and horizontal deflection sensitivities may be calibrated.
 - b. TRIGGER switch is set to CH 1 ONLY and the HORIZ DISPLAY switch is set to EXT HORIZ.

C. Characteristics

1. The following characteristics apply over an ambient temperature range of -15°C to $+55^{\circ}\text{C}$ except as otherwise indicated.

a. Allow 20 minutes warm-up time for the indicated accuracies.

VERTICAL DEFLECTION SYSTEM

Characteristic	Performance Requirement		Supplemental Information	
Deflection Factor	5 millivolts/division to 10 volts/division in 11 calibrated steps for each channel		Steps in 1-2-5 sequence	
Deflection Accuracy	Within $\pm 3\%$ of indicated deflection with VARIABLE control fully clockwise		With gain correct at 20 mV	
Variable Deflection Factor	Uncalibrated deflection factor at least 2.5 times the VOLTS/DIV switch indication. This provides a maximum uncalibrated deflection factor of 25 volts/division in the 10 volts position.			
Frequency Response (not more than 30% down) 20 mV to 10 VOLTS/DIV	Type 453 Only	With P6010 Probe		
	Dc to 52.5 Mc	Dc to 50 Mc		
	10 mV/DIV	Dc to 46.5 Mc	Dc to 45 Mc	
	5 mV/DIV	Dc to 41 Mc	Dc to 40 Mc	
	Channel 1 and 2 cascaded	Dc to 25 Mc	Dc to 25 Mc	Measured at 1 millivolt/division
Added	Dc to 52.5 Mc	Dc to 50 Mc	Measured at 20 mV	
Risetime (calculated) 20 mV to 10 VOLTS/DIV	Less than 6.7 nanoseconds	7		
	Less than 7.5 nanoseconds	7.8		
	Less than 8.75 nanoseconds	8.75		
	Channel 1 and 2 cascaded	Less than 14 nanoseconds	14	Measured at 1 millivolt/division
	Added	Less than 6.7 nanoseconds	7	Measured at 20 mV
Input Rc Characteristics			Typically 1 megohm ($\pm 2\%$), parallel by 20 pf ($\pm 3\%$)	
Maximum Input Voltage			600 volts combined dc and peak ac	
Input Coupling Modes	Ac or dc, selected by front-panel switch			
AC Low-frequency response			Typically 30% down at 1.6 cps, AC GND DC switch set to AC	
Trace Shift Due to Input Grid Current	Less than 0.4 division at 5 mv			
Vertical Display Modes	Channel 1 only Channel 2 only Dual-trace, alternate between channels Dual-trace, chopped between channels Added algebraically			

VERTICAL (cont'd)

Characteristic	Performance Requirement	Supplemental Information		
Chopped Repetition Rate	Approximately 1-microsecond segments from each channel displayed at repetition rate of 500 kc, $\pm 20\%$			
Attenuator Isolation	Greater than 10,000:1, dc to 20 Mc			
Common Mode Rejection Ratio	Greater than 20:1 at 20 Mc; input signal less than eight times VOLTS/DIV switch setting	With optimum GAIN adjustment at low frequency		
Linear Dynamic Range useful for Common-Mode Rejection in ADD Mode		Less than 10% incremental signal distortion for instantaneous input voltage of -10 or $+10$, times VOLTS/DIV switch setting		
Polarity Inversion	Signal on Channel 2 can be inverted			
Signal Delay		Approximately 140 nanoseconds		
Vertical Linearity	Less than 0.15 division compression or expansion of 2 division signal when positioned to vertical extremes of display area	Includes crt linearity		
Trace Drift (after 15 minute warm up) 20 mV to 10 VOLTS/DIV		Time	Temperature	
		Typically less than 0.25 division/hour	Typically less than 0.025 division/degree C	
		10 mV/DIV	Typically less than 0.5 division/hour	Typically less than 0.05 division/degree C
		5 mV/DIV	Typically less than 1 division/hour	Typically less than 0.1 division/degree C
Channel 1 Output Signal Output Voltage	Greater than 25 millivolts/division of crt display into 1 megohm load	At CH 1 OUT Connector. Channel 1 VARIABLE VOLTS/DIV control set to CAL		
Frequency Response (not more than 30% down)	Dc to 25 Mc when cascaded with Channel 2 or into 50-ohm load			
Risetime (calculated)	14 nanoseconds			
Output Coupling	Dc			
Output Resistance		Approximately 50 ohms		

TRIGGERING (A AND B SWEEP)

Characteristic	Performance Requirement	Supplemental Information	
Source	Internal from displayed channel or from Channel 1 only Internal from ac line External External divide by 10		
Coupling	Ac Ac low-frequency reject Ac high-frequency reject Dc		
Polarity	Sweep can be triggered from positive-going or negative-going portion of trigger signal		
Internal Trigger Sensitivity AC	0.2 division of deflection, minimum, 30 cps to 10 Mc; increasing to 1 division at 50 Mc	Typically 30% down at 16 cps	
LF REJ	0.2 division of deflection, minimum, 30 kc to 10 Mc; increasing to 1 division at 50 Mc	Typically 30% down at 16 kc	
HF REJ	0.2 division of deflection, minimum, 30 cps to 50 kc	Typically 30% down at 16 cps and 100 kc	
DC	0.2 division of deflection, minimum, dc to 10 Mc; increasing to 1 division at 50 Mc.		

TRIGGERING (cont'd)

Characteristic	Performance Requirement	Supplemental Information
External Trigger Sensitivity AC	50 millivolts, minimum, 30 cps to 10 Mc; increasing to 200 millivolts at 50 Mc	Typically 30% down at 16 cps
LF REJ	50 millivolts, minimum, 30 kc to 10 Mc; increasing to 200 millivolts at 50 Mc	Typically 30% down at 16 kc
HF REJ	50 millivolts, minimum, 30 cps to 50 kc	Typically 30% down at 16 cps and 100 kc
DC	50 millivolts, minimum, dc to 10 Mc; increasing to 200 millivolts at 50 Mc	
Auto Triggering (A Sweep only)	Provides normal triggering capability for trigger signals above 20 cps and produces free-running sweep in absence of trigger signal.	
Single Sweep (A Sweep only)	Triggering capability same as normal trigger Performance Requirement.	
Display Jitter	Less than 1 nanosecond at 10 nanoseconds/division sweep rate (MAG switch set to $\times 10$)	
Maximum Input Voltage		600 volts combined dc and peak ac
External Trigger Input Rc Characteristics (approximate)		1 Megohm paralleled by 20 pf, except in LF REJ
LEVEL Control Range	At least ± 2 volts, SOURCE switch in EXT position At least ± 20 volts, SOURCE switch in EXT $\div 10$ position	

**HORIZONTAL DEFLECTION SYSTEM
A and B Sweep Generator**

Characteristic	Performance Requirement		Supplemental Information
Sweep Rates A Sweep	0.1 microsecond/division to 5 seconds/division in 24 calibrated steps		A Sweep is main and delaying sweep
B Sweep	0.1 microsecond/division to 0.5 second/division in 21 calibrated steps		B Sweep is delayed sweep
Sweep Accuracy — A and B Sweep	0°C to +40°C	-15°C to +55°C	A VARIABLE and B TIME/DIV VARIABLE controls set to CAL
5 SEC to 0.1 SEC/DIV	Within $\pm 3\%$ of indicated sweep rate	Within $\pm 5\%$ of indicated sweep rate	
50 mSEC to 0.1 μ SEC/DIV	Within $\pm 3\%$ of indicated sweep rate	Within $\pm 4\%$ of indicated sweep rate	
Variable Sweep Rate	Uncalibrated sweep rate to at least 2.5 times the TIME/DIV indication, or a maximum of at least 12.5 seconds/division in the 5 SEC position (B Sweep, maximum of 1.25 seconds/division in the .5 SEC position).		
Sweep Length A Sweep	Variable from less than 4 divisions to 11.0, ± 0.5 division		A TIME/DIV switch set to 1 mSEC
B Sweep	11.0 divisions, ± 0.5 division		B TIME/DIV switch set to 1 mSEC
Sweep Hold-off—A Sweep 5 SEC to 10 μ SEC/DIV	Less than one times the A TIME/DIV switch setting		
5 μ SEC to 0.1 μ SEC/DIV	Less than 2.5 microsecond		
Gate Output Signal Waveshape	Rectangular pulse		
Polarity	Positive-going		Baseline at about -0.7 volts
Amplitude	12 volts, $\pm 10\%$		
Duration	About 11 times TIME/DIV switch setting		A GATE duration variable between about 4 and 11 times A TIME/DIV switch setting with A SWEEP LENGTH control
Output resistance			Approximately 1.5 kilohms

Sweep Magnifier

Characteristic	Performance Requirement	Supplemental Information
Sweep Magnification	Each sweep rate can be increased 10 times the indicated sweep rate by horizontally expanding the center division of display	Extends fastest sweep rate to 10 nanoseconds/division
Magnified Sweep Accuracy	1% tolerance added to specified sweep accuracy	
Magnified Sweep Linearity	$\pm 1.5\%$ for any eight division portion of the total magnified sweep length (excluding first and last 60 nanoseconds of magnified sweep)	
Normal/Magnified Registration	Less than ± 0.2 division trace shift at graticule center when switching MAG switch from $\times 10$ to OFF	

Sweep Delay

Characteristic	Performance Requirement		Supplemental Information
Calibrated Delay Time Range	Continuous from 50 seconds to 1 microsecond		A VARIABLE control set to CAL for indicated delay
Delay Time Accuracy 5 SEC to 0.1 SEC/DIV 50 mSEC to 1 μ SEC/DIV	0°C to +40°C	-15°C to +55°C	Includes incremental multiplier linearity
	Within $\pm 2.5\%$ of indicated sweep rate	Within $\pm 3.5\%$ of indicated sweep rate	
	Within $\pm 1.5\%$ of indicated sweep rate	Within $\pm 2\%$ of indicated sweep rate	
Incremental Multiplier Linearity	$\pm 0.2\%$	$\pm 0.3\%$	
Delay Time Jitter	Less than 1 part in 20,000 of 10 times A TIME/DIV switch setting		

External Horizontal Amplifier

Characteristic	Performance Requirement		Supplemental Information
Input to Channel 1 (TRIGGER switch in CH 1 ONLY) Deflection factor	5 millivolts/division to 10 volts/division in 11 calibrated steps		Steps in 1-2-5 sequence. Channel 1 VARIABLE control does not affect horizontal deflection
Accuracy	0°C to +40°C	-15°C to +55°C	With External Horizontal gain correct at 20 mV
	Within $\pm 5\%$ of indicated deflection	Within $\pm 8\%$ of indicated deflection	
Frequency response	Dc to 5 Mc, not more than 30% down		
Input rc characteristics			Typically .1 megohm ($\pm 2\%$), paralleled by 20 pf ($\pm 3\%$)
Phase difference between X and Y amplifiers at 50 KC			Less than 3°
Input to EXT HORIZ Connector Deflection factor	B TRIGGERING SOURCE switch in EXT — 270 millivolts/division, $\pm 15\%$ B TRIGGERING SOURCE switch in EXT $\div 10$ — 2.7 volts/division, $\pm 20\%$		
Frequency response	Dc to 5 Mc, not more than 30% down		
Input rc characteristics (approximate)			1 megohm, paralleled by 20 pf
Phase difference between X and Y amplifiers at 50 KC			Less than 3°

CALIBRATOR

Characteristic	Performance Requirement		Supplemental Information
Waveshape	Square wave		
Polarity	Positive going with baseline at zero volts		
Output Voltage	0.1 volt or 1 volt, peak to peak		Selected by CALIBRATOR switch on side panel
Output Current	5-milliamps through PROBE LOOP on side panel		
Repetition Rate	1 kc		
Voltage Accuracy	0°C to +40°C	-15°C to +55°C	
	±1%	±1.5%	
Current Accuracy	±1%	±1.5%	
Repetition Rate Accuracy	±0.5%	±1%	
Risetime	Less than 1 microsecond		
Duty Cycle	49% to 51%		
Output Resistance			Approximately 200 ohms in 1 V position Approximately 20 ohms in .1 V position

Z AXIS INPUT

Characteristic	Performance Requirement	Supplemental Information
Sensitivity	5 volt peak-to-peak signal produces noticeable modulation	
Usable Frequency Range	Dc to greater than 50 Mc	
Input Resistance at DC		Approximately 47 kilohms
Input Coupling	Dc coupled	
Polarity of Operation		Positive-going input signal will decrease trace intensity Negative-going signal will increase trace intensity
Maximum Input Voltage		200 volts combined dc and peak ac

POWER SUPPLY

Characteristic	Performance Requirement	Supplemental Information
Voltage Requirements		
115-volt range	LOW—96 to 127 volts, rms, ac line voltage provides regulated dc voltages HIGH—103 to 137 volts, rms, ac line voltage provides regulated dc voltages	Applicable when line contains less than 2% total harmonic distortion
230-volt range	LOW—192 to 254 volts, rms, ac line voltage provides regulated dc voltages HIGH—206 to 274 volts, rms, ac line voltage provides regulated dc voltages	
Line Frequency	45 to 440 cps	
Power Consumption		Approximately 100 watts

CATHODE-RAY TUBE (CRT)

Characteristic	Information
Tube Type	T4530-31-1 rectangular, glass envelope
Phosphor	P31 standard. Others available on special order
Accelerating Potential	Approximately 10 kv (gun potential, 2 kv)
Graticule Type	Internal
Area	6 divisions vertical by 10 divisions horizontal. Each division equals 0.8 centimeter
Illumination	Variable edge lighting
Unblinking	Dc-coupled to crt grid from Sweep Generator

MECHANICAL CHARACTERISTICS

Characteristic	Information
Construction	Aluminum-alloy chassis, panel and cabinet Glass laminate etched-wiring boards
Finish	Anodized panel, blue vinyl-coated cabinet
Overall Dimensions (measured at maximum points)	7.25" high, 12.5" wide, 23.5" long (includes panel cover and handle)
Net Weight	29 lbs. 2 oz. (includes power cord and panel cover without accessories)

ENVIRONMENTAL CHARACTERISTICS**NOTE**

The Type 453 has been designed to meet the following environmental characteristics. During production, samples of the Type 453 will be checked to assure that the instrument continues to meet the environmental characteristics. Environmental tests can be grouped into two general categories: Tests which may be repeated an indefinite number of times without physical damage to, or performance deterioration of, the instrument (Category I); and tests which should be repeated only once as they may cause minor damage to the instrument without causing it to malfunction (Category II). The following environmental characteristics will be grouped into these categories. Complete details on environmental test procedures, including failure criteria, etc., may be obtained from Tektronix, Inc. Contact your local Field Office or representative.

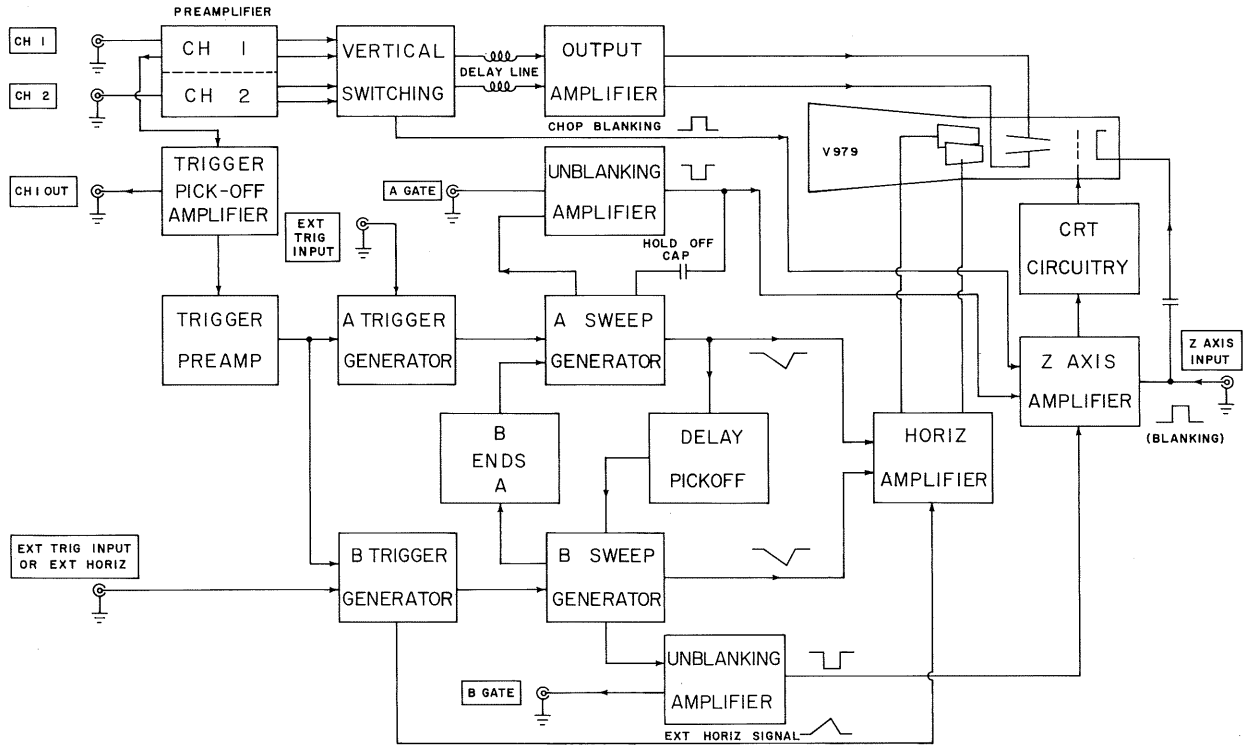
Category I

Characteristic	Requirement
Temperature Operating	Type 453 will perform to limits given in this section over a temperature range of -15°C to $+55^{\circ}\text{C}$. Maximum operating temperature must be derated $1^{\circ}\text{C}/1000$ feet increase in altitude from 5000 to 15,000 feet. Fan at rear of instrument blows filtered air throughout instrument. Automatic resetting thermal cut-out interrupts instrument power if internal temperature exceeds a safe operating level.
Non-Operating	-55°C to $+75^{\circ}\text{C}$
Altitude Operating	Type 453 will perform to limits given in this section up to 15,000 feet. See derating information under 'Temperature'.
Non-Operating	50,000 feet maximum

Category II

Characteristic	Requirement
Humidity Non-Operating	Instrument will perform to limits given in this section following 5 cycles (120 hours) of Mil-Std-202B, Method 106A (exclude freezing and vibration).
Vibration Operating and Non operating	Instrument will perform to limits given in this section following vibration test. Vibrated for 15 minutes along each axis at a total displacement of 0.025-inch peak to peak (4G at 55 cps) from 10-55-10 cps in 1 minute cycles. Held for 3 minutes at 55 cps. Total vibration time, 55 minutes.
Shock Operating and Non-Operating	Instrument will perform to limits given in this section following shock test. 30G, one-half sine, 11 millisecond duration. Two shocks each direction along each axis (total of 12 shocks).
Transportation Non-operating	Meets National Safe Transit type of test when factory packaged. Package shake test—One hour in excess of 1G. Package drop test—30-inch drops on one corner, three edges and all flat surfaces (total of 10 drops).

D. Block Diagram



TYPE 453 GENERAL BLOCK DIAGRAM

B-453-0000
6-18-65 jg

II. CHANNEL 1 INPUT AMPLIFIER

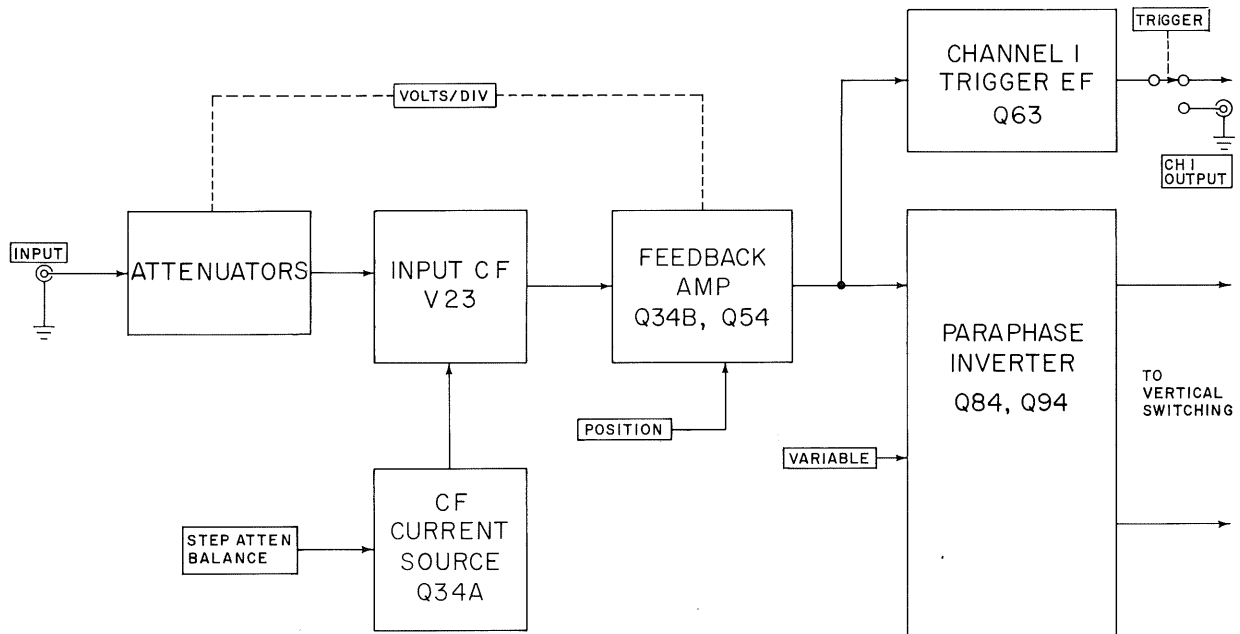
A. The Channel 1 Input Amplifier amplifies and attenuates the input signal.

1. The circuit provides a push-pull current drive to the Vertical Switching circuit and the Vertical Amplifier.
2. A Channel 1 Trigger signal is also provided.

B. Circuits that comprise the Channel 1 Input Amplifier.

1. Attenuator and Input Switches.
2. Input CF, V23.
3. CF Current Source, Q34A.
4. Feedback Amplifier; Q34B, Q54.
5. Paraphase Inverter; Q84, Q94.
6. Channel 1 Trigger EF, Q63.

C. Block Diagram



TYPE 453 CHANNEL 1 INPUT AMPLIFIER
BLOCK DIAGRAM

B-453-0001
5-12-'65dl

D. Block Logic

1. The Input Amplifier has a signal current output of about .5 ma/div per side.
 - a. Since the amplifier has a voltage input and a current output, the signal transfer is rated as transadmittance* .
 - b. Transadmittance gain, $T_Y = \frac{i_{out}}{e_{in}}$.
2. Eleven sensitivity positions are available on the VOLTS/DIV switch from 5 mv/div to 10 v/div in 1, 2, 5 sequence.
3. Basic sensitivity of the vertical is 20 mv/div in all positions of the VOLTS/DIV switch from 20 mv/div to 10 v/div.
4. The amplifier changes its basic sensitivity in the 5 mv/div and 10 mv/div positions of the VOLTS/DIV switch.
 - a. At 5 mv/div, $T_Y = 100,000 \mu\text{mhos}$.
 - (1) $T_Y = \frac{i_{out}}{e_{in}}$.
 - (2) $T_Y = \frac{.5 \text{ ma/div}}{5 \text{ mv/div}}$.
 - (3) $T_Y = 100,000 \mu\text{mhos}$.
 - b. At 10 mv/div, $T_Y = 50,000 \mu\text{mhos}$.
 - (1) $T_Y = \frac{.5 \text{ ma/div}}{10 \text{ mv/div}}$
 - (2) $T_Y = 50,000 \mu\text{mhos}$.
 - c. At 20 mv/div and all other sensitivities (20 mv/div to 10 v/div), $T_Y = 25,000 \mu\text{mhos}$.
 - (1) $T_Y = \frac{.5 \text{ ma/div}}{20 \text{ mv/div}}$
 - (2) $T_Y = 25,000 \mu\text{mhos}$.

* See June 1963 Service Scope .

- d. Bandpass of the vertical is reduced in the 5 mv/div position to DC to 40 mc and at 10 mv/div to DC to 45 mc.
4. Input impedance is 1 megohm $\pm 2\%$ paralleled by 20 pF $\pm 3\%$.
5. Input coupling is selected by means of a lever switch.
 - a. AC, DC or GND is available.
6. The Input CF, a nuvistor, provides high input impedance.
7. A two stage transistorized feedback amplifier includes a section of the VOLTS/DIV switch that changes the basic gain of the amplifier.
 - a. In the 5 mv/div position of the VOLTS/DIV switch, the Feedback Amplifier has a gain of 10.
 - b. In the 10 mv position, the Feedback Amplifier gain is 5.
 - c. In the 20mv position and all other positions, the Feedback Amplifier gain is 2.5.
8. The STEP ATTEN BAL control operating through the CF Current Source transistor, Q34A, adjusts potentials at the Feedback Amplifier so changing sensitivity positions will not shift the trace.
9. The POSITION control operating through the Feedback Amplifier has a range of about ± 15 divisions.
10. The output from the Feedback Amplifier at about 50 mv/div is fed via Channel 1 Trigger EF to the Trigger Preamp.
 - a. The signal is attenuated in the EF circuit to about 25 mv/div.
 - b. The EF also feeds the CH 1 OUT jack.

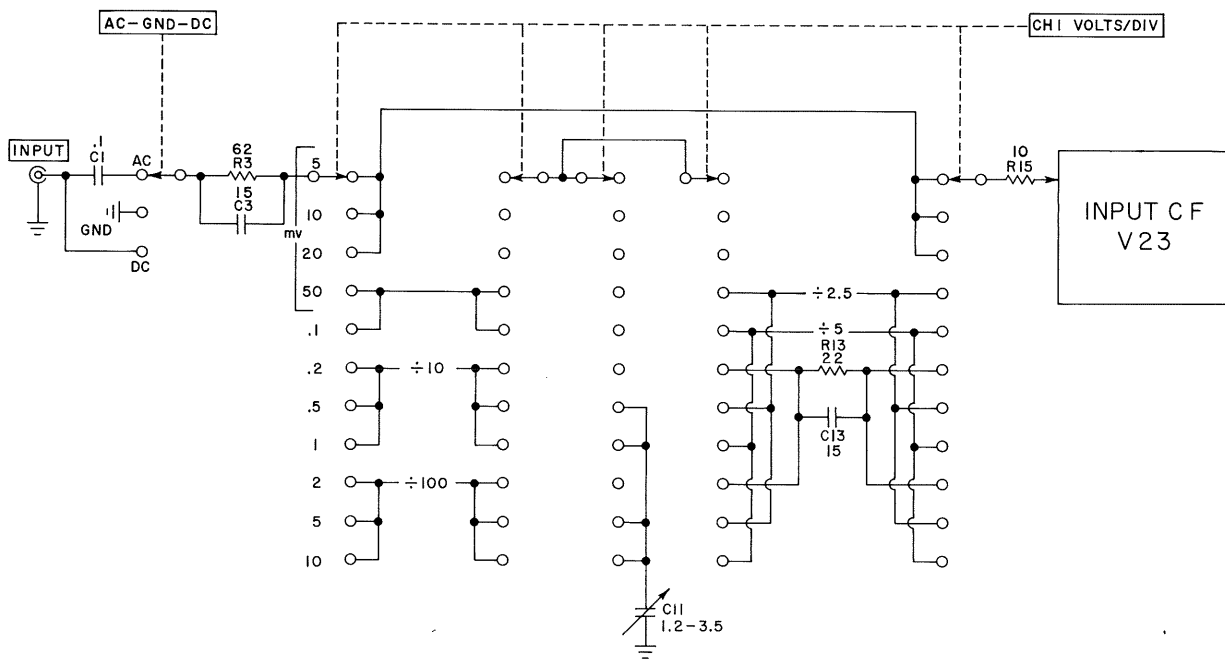
11. The single ended signal voltage output from the Feedback Amplifier becomes a push-pull signal current in the Paraphase Inverter.

a. The VARIABLE VOLTS/DIV control has an attenuator range of $\geq 2.5:1$.

12. The current drive to the Vertical Switching circuit and Vertical Amplifier is about .5 ma/div per side.

E. Attenuators and Input Switches

1. The circuit includes the Coupling Switch, a portion of the VOLTS/DIV switch and four attenuators.

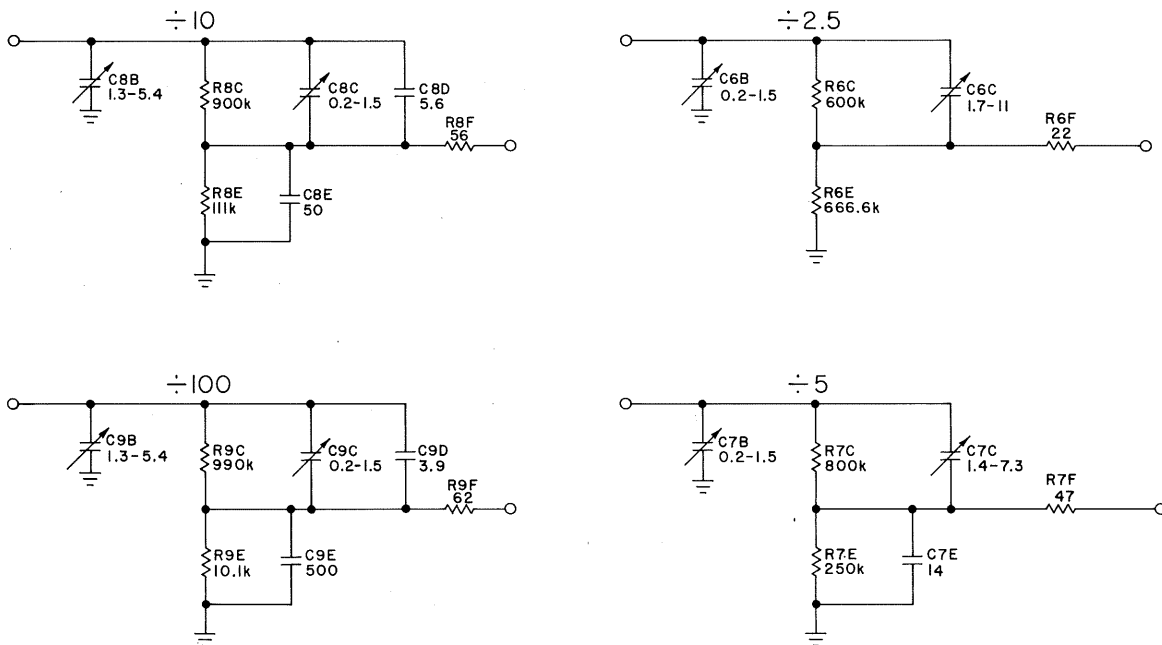


TYPE 453 CHANNEL I INPUT AMPLIFIER
ATTENUATOR SWITCHES

B-453-0002
5-13-'65 dl

2. The input jack is a BNC connector.
3. Input impedance is 1 megohm $\pm 2\%$ paralleled by 20 pF $\pm 3\%$.
4. Input is limited to an excursion of ± 600 volts combined DC and peak AC.
5. A front panel level switch is used for coupling selection.
 - a. The AC position inserts a .1 μ F tubular capacitor.
 - (1) Low frequency cut off is 1.59 cps.
 - b. The GND position opens the input connection and grounds the Cathode Follower input through the attenuator.
 - c. The DC position connects the input through the attenuators to CF input.
6. Stacked attenuators are used.
 - a. The first bank (of attenuators) includes the $\div 1$ (a straight wire), the $\div 10$, and $\div 100$.
 - b. The second bank includes the $\div 2.5$, the $\div 5$ and a $\div 1$ position composed of a 22Ω anti-ringing resistor (R13) and its bypass capacitor, C13.
7. In the 5 mv, 10 mv and 20 mv/div positions, the attenuators are bypassed, thereby reducing stray C. The basic sensitivity of the Feedback Amplifier is changed in these three positions.
 - a. Only two switch wafers are used instead of the five used in other positions.
 - b. The jumper has about 3 pF capacitance.
8. R3 and R15 break up lead inductance, thereby prevent ringing.
9. In positions where attenuators are stacked (.5v, 1v, 5v and 10v positions), C11 is connected in shunt with the second attenuator bank.
 - a. The X1 attenuator in the second bank has higher shunt capacitance than the $\div 2.5$ and $\div 5$ compensated attenuators.

10. The attenuators are conventional compensated attenuators.



TYPE 453 CHANNEL I INPUT AMPLIFIER
INPUT ATTENUATORS

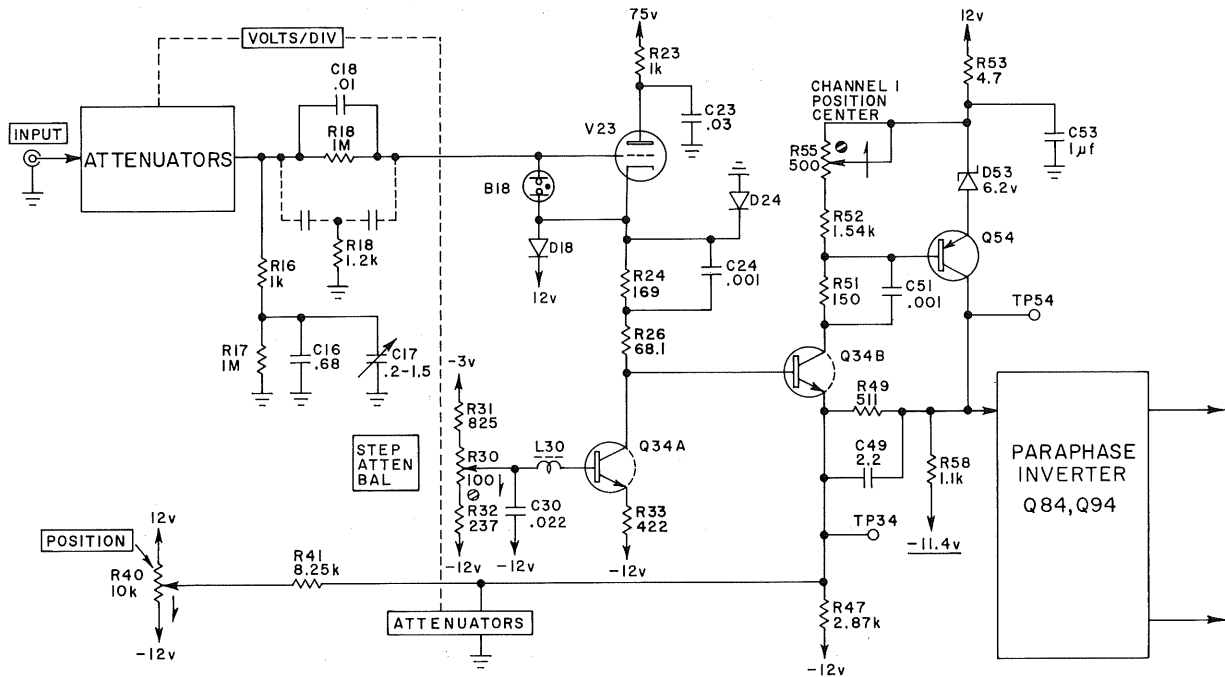
B-453-0003
5-14-'65 dl

- 1% precision resistors are used in the X2.5 and X5 attenuators.
- 1/2% precision resistors are used in the X10 and X100 attenuators.
- Series resistors, R6F, R7F, R8F and R9F break-up lead inductance.

F. Input CF, V23

- The input CF provides a high Z input impedance and isolates the input from any change in impedance as gain or sensitivity of the amplifier is changed.

2. V23 grid current should not exceed 2 nanoamps.
3. V23 is an 8393 nuvistor with a mu of 35.
 - a. The protective diodes are 6185 silicon diodes.



TYPE 453 CHANNEL I INPUT AMPLIFIER
INPUT CF AND FEEDBACK AMPLIFIER

B-453-0004
5-17-'64 di

4. The CF has a gain of about .97.
 - a. With the high Z cathode tail through Q34A, gain is about

$$\frac{\mu}{\mu + 1}$$
5. Circuit protection:
 - a. The input is limited to $\pm 600v$ (including DC and peak AC).

- b. R18 limits V23 grid current to $600 \mu\text{a}$ if the input is raised to 600v .
 - (1) C18 bypasses the protective resistor for AC.
 - (2) C18 provides charging current for V23 input C.
- c. B18 provides protection when V23 grid is dropped below its cathode.
 - (1) B18 ignites at about 80v and sustains at about 60v .
 - (2) V23 is protected from grid-cathode arc-over.
- d. D24 protects V23 grid during tube warm-up.
 - (1) V23 cathode is prevented from dropping below $-.6\text{v}$.
- e. D18 protects Q34A from base-collector breakdown.
 - (1) D18 conducts if V23 cathode is lifted above 12v .
- 6. C17 is used to standardize the input at 20 pF in the "straight through" positions.
- 7. R17 provides the 1M input resistance in the straight through positions.
 - a. R17 is also part of the attenuator network at all VOLTS/DIV positions above 20 mv/div .
- 8. R16, C16 and C17 compensate for an increase in V23 input C as the input signal frequency increases.
 - a. V23 input C is about 5 pF at low frequency.
 - b. At higher frequency, the input C increases until at 100 mc it reaches about 11 pF .
 - (1) Since the cathode cannot follow the grid without some delay at high frequencies, the input appears more capacitive.
 - (2) The negative resistance component is about 900Ω .

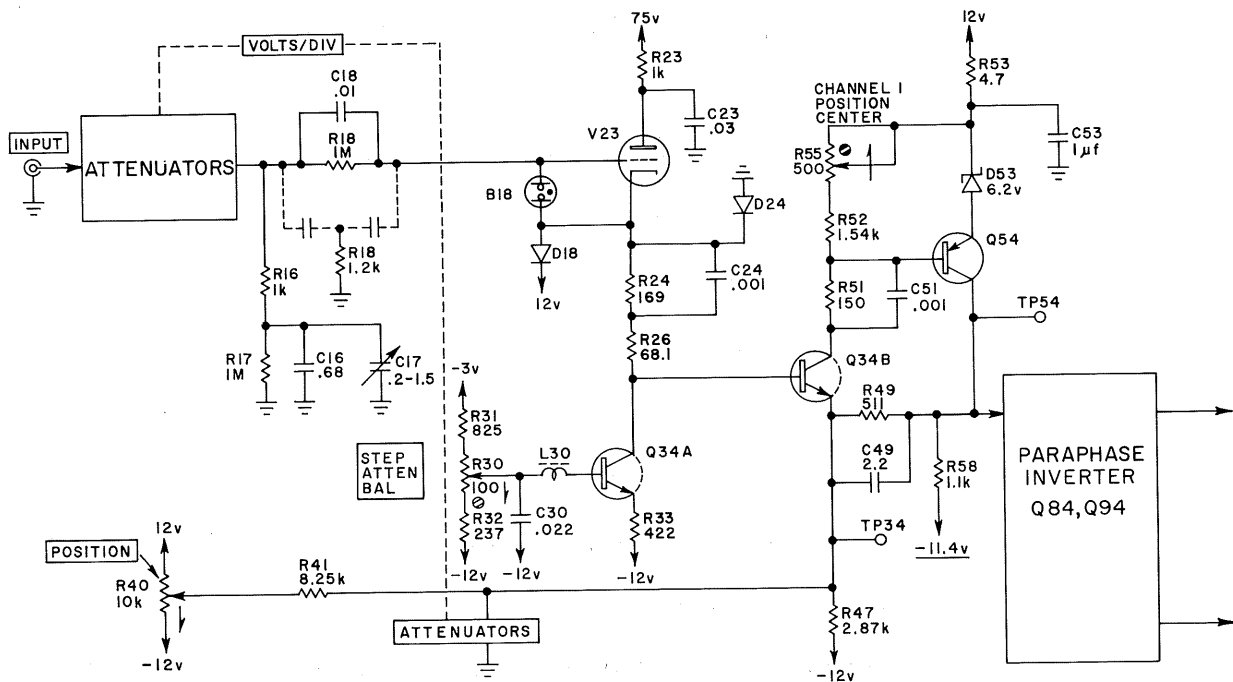
- c. At low frequencies, the parallel equivalent of R16, C16, C17 and the stray capacitance of R17 appears as a very high resistance in shunt with about 2.5 pF.
 - (1) This C plus additional C around R18 is in shunt with V23 input C.
 - d. At high frequencies, the parallel equivalent appears as a much lower R in shunt with a much lower value of C.
 - e. Since the equivalent shunt capacitance decreases as V23 input C increases, the total input and shunt C remains fairly constant.
 - f. The equivalent shunt resistance matches the negative resistance input of V23.
9. R16, R17, R18, C18 and C16 are mounted on stand-off insulators to prevent a dielectric hook.
- a. If the components were mounted on the PC board, dielectric changes with frequency (of the PC board base material) would cause an overshoot to an increasing voltage step -- hook effect.
 - b. However, capacitive coupling from the stand-off insulators to the PC board dielectric still introduced hook.
 - c. To correct this effect, a tie point was placed on the PC board at a point equidistant from the ends of R18.
 - d. A strap was installed to the sleeve of each of the stand-off insulators supporting R18 and tied to the tie point.
 - e. The tie point could have been tied to ground, thereby removing the hook.
 - f. Using a 1.2k resistor (R19) to connect the tie point to ground, however, served two purposes.

- (1) The stand-off insulator's C was now returned to ground instead of to the PC board dielectric.
- (2) The series RC circuit, thus formed, supplements the circuit composed of R16, C16 in compensating for the increasing C (with frequency) of V23 input.

10. R23, C23 decouple V23 plate supply.
11. R24 and R26 set the Q34B base level.
 - a. C24 improves the transient response.

G. CF Current Source, Q34A

1. Q34A is a constant current source for V23.
 - a. Long tail resistance seen by the CF is about 100k.



TYPE 453 CHANNEL I INPUT AMPLIFIER
INPUT CF AND FEEDBACK AMPLIFIER

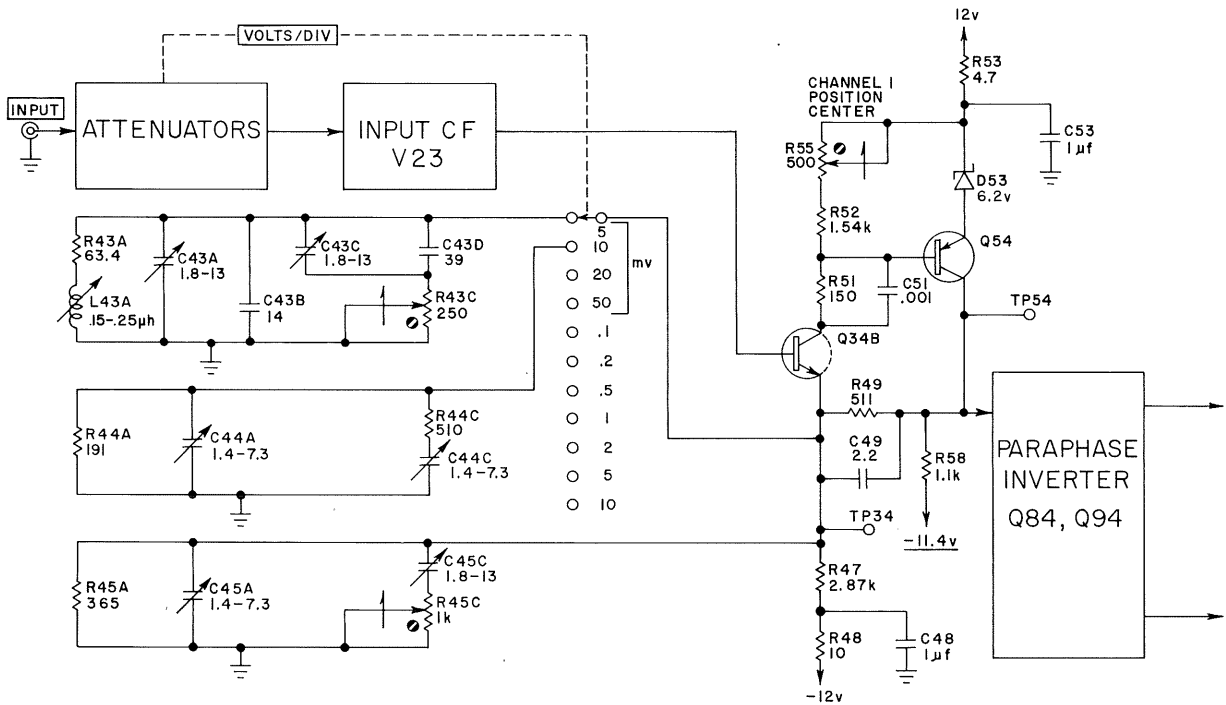
B-453-0004
5-17-'64 dl

2. Q34A is a variable current source for V23.
 - a. Using the STEP ATTEN BAL control, V23 current is adjusted so that Q34B emitter sets at zero volts DC.
 - b. Under this condition, the VOLTS/DIV switch can be rotated to change Q43B emitter resistance to ground without causing a trace shift.
3. Q34A is half a 151-139, a silicon NPN dual transistor -- a dual 151-109.
 - a. The other half is Q34B.
 - b. The two transistors in one can provide temperature compensation through common environment.
 - c. R33, Q34A emitter resistance matches its collector load (R24, R26 and V23 Z_k).
 - d. Q34A, therefore, has a gain of 1 so any thermal change in Q34A will exactly match the change in Q34B.
4. Q34A base, connected to the STEP ATTEN BAL control, can set voltages (at its base) from -9.4v to -10.2v.
5. To minimize the effect of any noise from the -12v supply on Q34A output, the base and emitter are both returned to -12v.
 - a. The -3v is zener referenced to -12v so the entire STEP ATTEN BAL control moves with any -12v supply changes.
 - b. C30 AC couples -12v noise directly to Q34A base to change Q34A input C.
6. L30 suppresses an oscillation.

H. Feedback Amplifier; Q34B, Q54

1. The Feedback Amplifier consists of a transistor pair in feedback configuration that controls the basic sensitivity of the CH 1 Input Amplifier.

- a. Q34B is half a 151-139 -- Q34A is the other half.
- b. Q54 is a 151-167 silicon PNP transistor.
- c. D53 is a 152-166, 6.2v, 5% zener.



TYPE 453 CHANNEL 1 INPUT AMPLIFIER
FEEDBACK AMP AND MV ATTENUATORS

B-453-0005
5-20-'65dl

2. Gain of the Feedback Amplifier is changed by settings of the VOLTS/DIV control as different values of R_a are switched in.

3. As a feedback amplifier, gain is virtually independent of transistor beta.

a.
$$A = 1 + \frac{R_f}{R_a}$$

(1) R_f is R49.

(2) R_a is primarily various values switched in by the VOLTS/DIV switch -- R47 is in shunt as part of R_a .

b. In the 5 mv position, $A = 10$.

(1) R_a is R43A in shunt with R45A and R47.

(2) $A = 1 + \frac{511}{54}$.

(3) $A \approx 10$.

c. In the 10 mv position, $A = 5$.

(1) R_a is R44A in shunt with R45A and R47.

(2) $A = 1 + \frac{511}{125}$.

(3) $A \approx 5$.

d. In the 20 mv position and all other positions, $A = 2.5$.

(1) R_a is R45 in shunt with R47.

(2) $A = 1 + \frac{511}{322}$.

(3) $A \approx 2.5$.

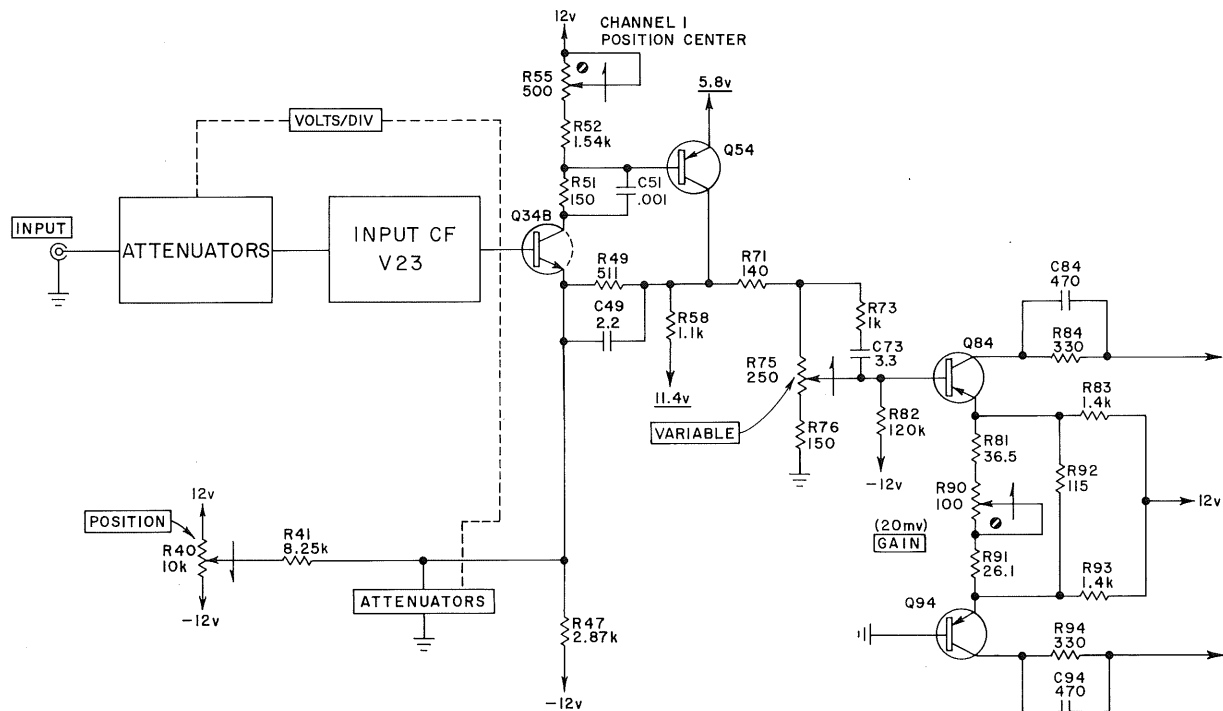
4. Proper setting of the STEP ATTEN BAL control sets Q34B emitter at 0v DC.

a. With Q34B emitter and the VOLTS/DIV switch arm at 0v, different values of R_a can be switched in without altering static current into the Feedback Amplifier.

b. No trace shift occurs as the switch is rotated.

5. Each R_a value (switched in by the VOLTS/DIV switch) is compensated.
 - a. Essentially the time constants for R_f and R_a should be the same.
 - b. Additional RC and RL networks provide adjustable HF correction for losses in the Feedback Amplifier, thereby improving transient response.
 - c. No provision is made for adjusting gain in each sensitivity position.
 - (1) R49, R43A, R44A and R45A are 1% resistors.
6. R48, C48 decouple the emitter return from the 12v supply.
7. Q54 emitter is set at 5.8v by D53, a 6.2v zener.
 - a. R53, C53 decouple the 12v supply.
8. R51 provides current limiting.
 - a. If V23 cathode is raised to its 12v limit (limited by D18), Q34B and Q54 will saturate.
 - b. Without R51, a low resistance path exists through R53, D53, saturated Q54, saturated Q34B and R_a (63Ω in 5 mv position) to ground.
 - c. About 80 ma would flow through the circuit under this condition.
 - d. R51 reduces the saturation current to about 24 ma.
 - (1) C51 is a speed-up cap.
9. The POSITION control varies trace position ± 13.5 div to ± 16.5 div.
 - a. The control has a swing of $\pm 12v$.

- b. R41 is R_f for the Feedback Amplifier.
- c. Current into Q34B emitter is varied ± 1.45 ma.
- d. Since Q34B emitter is a low Z point, the value of R_a (as switched in by the VOLTS/DIV switch) has practically no effect on the action of the POSITION control.



TYPE 453 CHANNEL 1 INPUT AMPLIFIER
PARAPHASE INVERTER

B-453-0006
5-21-'65 dl

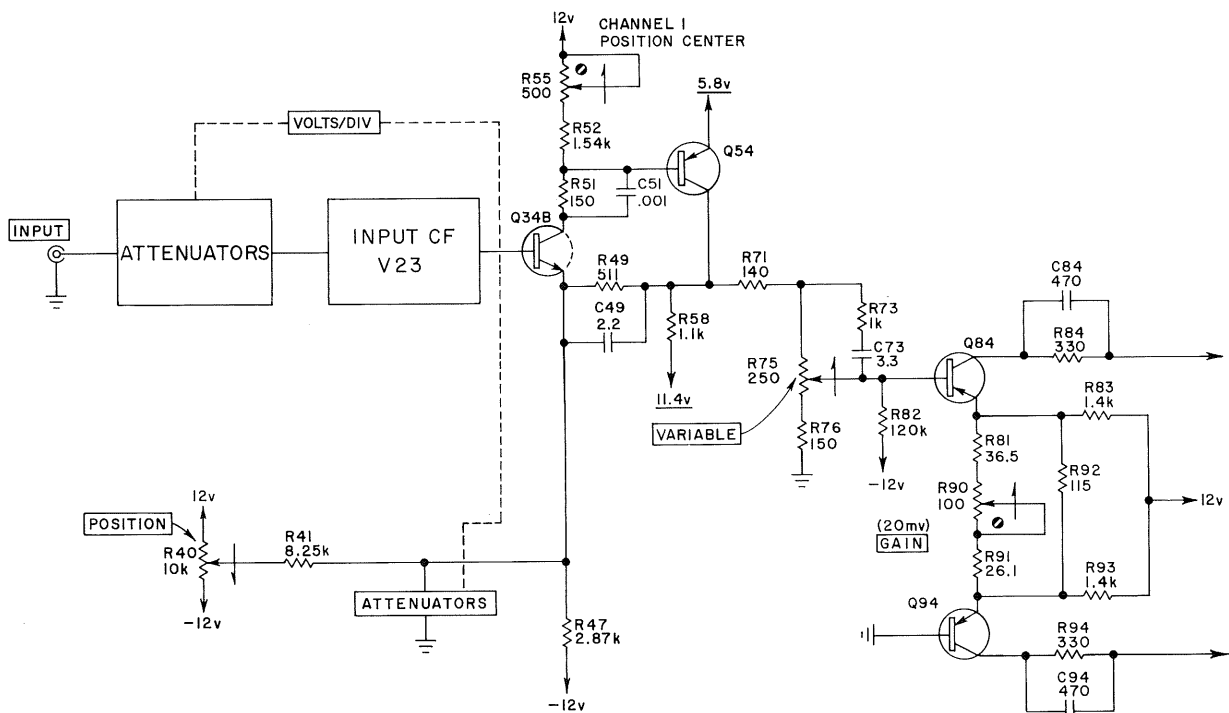
- 10. R55 (the CH 1 POSITION CENTER adj) is adjusted to place Q54 collector at ground potential*.
 - a. The POSITION control is first set with the arm at 0v.

* See Page 2-17.

11. R58 supplies Q54 collector current -- 10 ma.
12. Signal level at the Feedback Amplifier output is about 50 mv/div.

I. Paraphase Inverter; Q84, Q94

1. The Paraphase Inverter provides a push-pull drive to the Vertical Amplifier.
 - a. Since the Vertical Driver Amplifier is an operational amplifier, the Paraphase Inverter functions as a current drive.
 - b. The collector load appears in the Vertical Amplifier circuit.
 - c. Signal current out of the Paraphase Inverter is .5 ma/div per side.



TYPE 453 CHANNEL I INPUT AMPLIFIER
PARAPHASE INVERTER

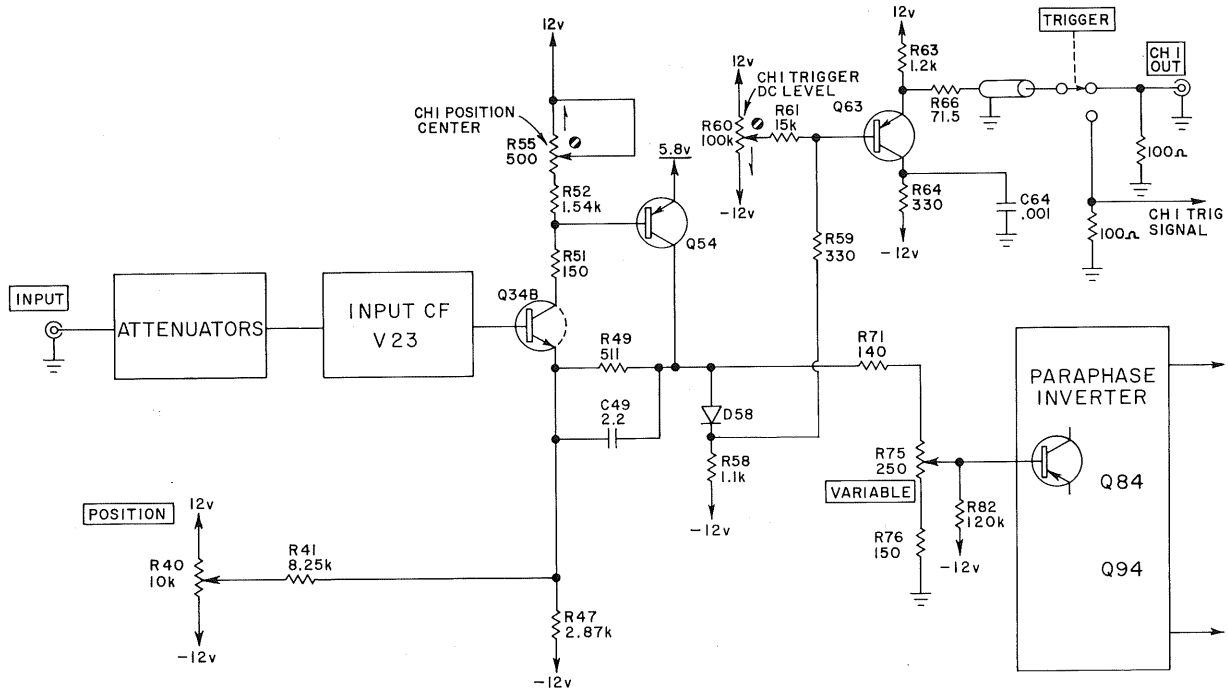
B-453-0006
5-21-'65 dl

2. Q84 and Q94 are 151-167 silicon PNP transistors.
3. With the Feedback Amplifier output (Q54 collector) at ground potential (set by the CH 1 POSITION CENTER control), the VARIABLE control has no static current through it.
 - a. R82 supplies Q84 base current, so Q84 base and the VARIABLE control arm are also at 0v DC.
 - (1) 0v on Q84 base matches the grounded Q94 base.
 - b. Rotating the VARIABLE control, therefore, does not change the static current into Q84 -- the trace does not shift.
 - c. DC balance is achieved, however, only when the trace is centered by the POSITIONING control.
4. R71 and R76 maintain a reasonably constant impedance as seen by Q84 base as the VARIABLE control is rotated.
 - a. R76 (150 Ω) below the control is matched by R71 plus the Feedback Amplifier output impedance above the control.
 - b. The impedance seen by Q84 base swings from 110 Ω to 138 Ω with rotation of the control -- 138 Ω at control center.
 - (1) This variation in impedance causes about 4% risetime degradation at the control center.
 - c. R73, C73 improve the transient response of the circuit.
5. Signal voltage at Q84 base is about 36 mv/div with the VARIABLE control in its calibrated position and 14 mv/div fully CCW.
 - a. The control has an attenuation range of a little more than 2.5:1.

- b. An UNCAL light lights when the control is moved off the fully clockwise detent.
 - c. The control attenuates the range of the POSITION control to ± 6 div.
6. R84 and R94 provide thermal balance* for the push-pull stage.
- a. C84 and C94 bypass the thermal balance resistors, thereby reducing miller capacitance.
 - b. The capacitors prevent HF signal voltages from being developed across R84 and R94.
 - c. If the paraphase inverter has no voltage gain at high frequencies, miller capacitance cannot exist.
7. Static collector current is 8 ma per side.
8. R90, the (20 mv) GAIN adj, is a front panel screwdriver adjustment.
- a. The 20 mv label indicates the recommended position of the VOLTS/DIV switch when adjusting the control.
 - b. R81 and R91 limit the minimum emitter tying resistance.
 - (1) Two resistors are used (one on each end of the control) as damping resistors to break up lead inductance.
 - c. R92 reduces the range of the control to an effective 27Ω .
- J. Trigger EF, Q63
- 1. The Trigger EF supplies a single ended trigger signal to the Trigger Preamp.
 - a. The signal is used in the CH 1 only position of the TRIGGER (CH 1 - NORM) switch.

* See Transistor Program, Volume 7, Page 111.

- b. In the NORM position, the signal is connected to the CH 1 OUT jack.



TYPE 453 CHANNEL 1 INPUT AMPLIFIER
TRIGGER E F

B-453-0007
6-2-'65dl

2. Q63 is a 151-133 silicon PNP transistor.
 - a. D58 is a 6185 silicon diode.
3. The signal at Q63 base is about 50 mv/div.
4. R66 and the transistor, r_e , provide an approximate impedance match for the inter-chassis coax.
 - a. The value for R66, however, was chosen to assure greater than 25 mv output to the CH 1 OUT jack.

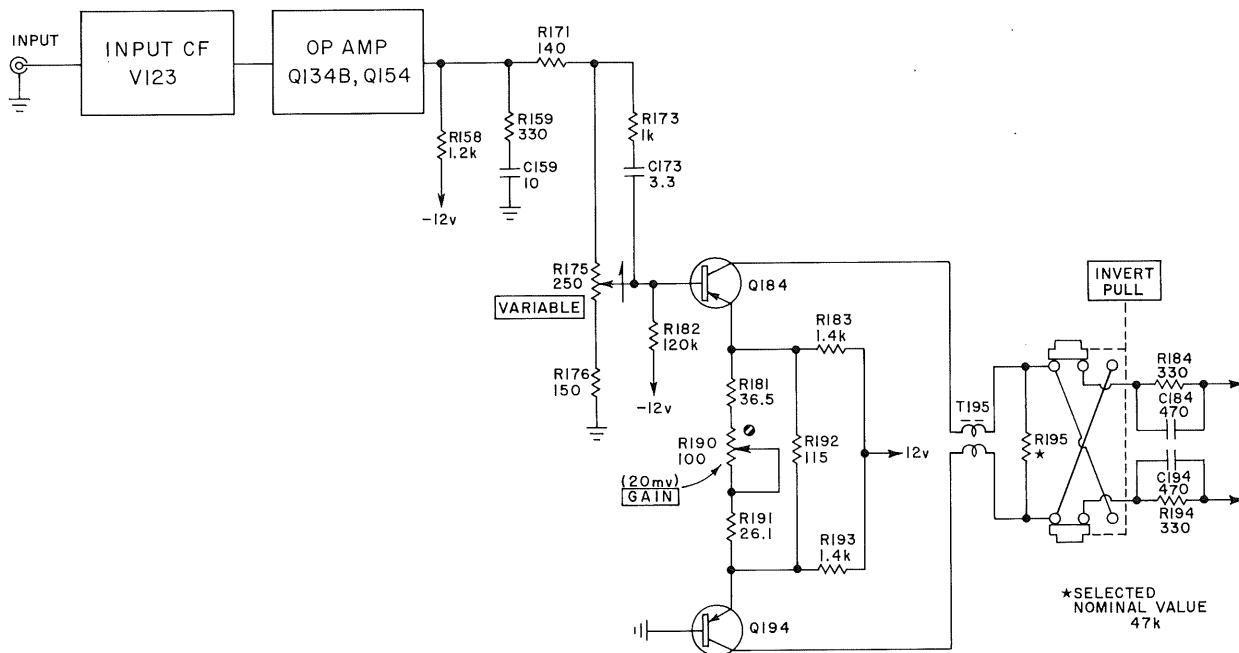
- b. Losses through the CF and in coupling to the EF deliver slightly less than 50 mv/div at Q63 base .
 - c. R66, Q63 r_e and a 100 Ω resistor at the CH 1 OUT form a divider that delivers about 27 vm/div .
 - d. The "greater than 25 mv/div" output is useful when cascading CH 1 and CH 2 Input Amplifiers
 - (1) The CH 2 VARIABLE (VOLTS/DIV) control can be used to calibrate the sensitivities of the cascaded amplifiers .
 - e. The ≈ 27 mv/div level is also useful when using the CH 1 Input Amplifier to feed an external signal to the Horizontal Amplifier* .
 - (1) The EXT HORIZ GAIN adj is used to calibrate the total sensitivities of the CH 1 Input Amplifier, the Trigger Preamplifier and the Horizontal Amplifier .
 - f. Output Z is $\approx 50\Omega$.
 - g. Frequency response is DC to >25 mc at 30% down at < 1 mv/div .
5. D58 temperature compensates Q63 base-emitter junction .
- a. Equal currents (10 ma) through the two junctions assure maximum matching of junction drops as temperature changes .
6. CH 1 TRIGGER DC LEVEL sets the DC level at zero volts at the Trigger Preamp output .

* See Page 12-3.

III. CHANNEL 2 INPUT AMPLIFIER

A. The Channel 2 Input Amplifier is the same as Channel 1 Input Amplifier with two exceptions.

1. The addition of an INVERT PULL switch.
2. The amplifier does not have a Trigger EF.
3. Crosstalk between channels is 100:1 to 20 mc.



TYPE 453 CHANNEL 2 INPUT AMPLIFIER
PARAPHASE INVERTER, INVERT SWITCH

B-453-0008

6-3-'65dl

B. Invert Switch Circuit

1. The INVERT PULL switch merely inverts the Channel 2 output.
 - a. The inverted signal is useful when operating in the ADD mode.
 - b. The trace should not shift more than ± 1 div from graticule center.

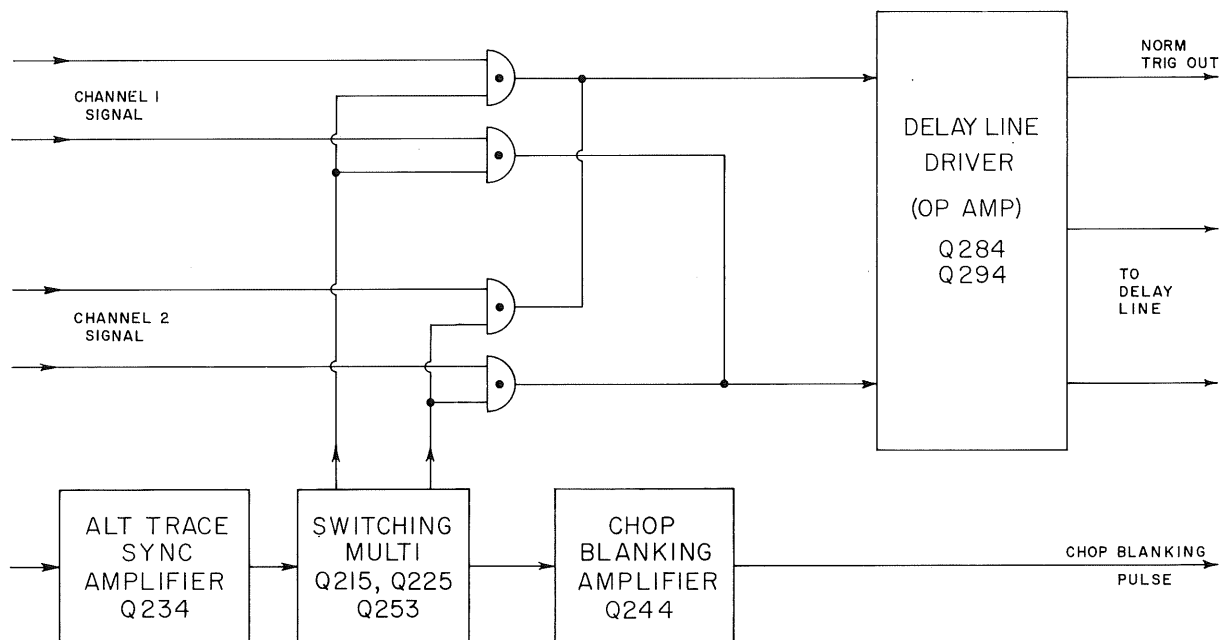
2. It is important that the transient response of the two input amplifiers match.
 - a. The output C of Channel 2 is greater, however, by the C added by the INVERT switch.
 - (1) The physical location of R184, C184, and R194, C194 at a location farther from the transistors also increases the shunt C.
 3. R195, a selected resistor (typically 47k), is used to match the response of the two amplifiers.
 - a. The T_c of Channel 2 (without R195) will always be greater than that of Channel 1.
 - b. The addition and selection of R195 can be used to reduce the T_c of Channel 2 to match that of Channel 1.
 - c. New transistors in either Paraphase Inverter will probably require a new resistor.
 - d. T195 suppresses an oscillation in ADD mode.
- C. There is no trigger take-off from the CH 2 Input Amplifier, therefore, no Trigger EF.
1. R159, C159 provide a load equal to that of the Trigger EF in the CH 1 Input Amplifier.

IV. VERTICAL SWITCHING

A. The Vertical Switching circuit determines which of the Input Vertical Preamp signals is connected to the Vertical Output Amplifier.

1. The vertical signal is amplified in the Delay Line Driver Amplifier before being fed to the Delay Line.
2. A Vertical Chop Blanking pulse is generated.

B. Block Diagram



TYPE 453 VERTICAL SWITCHING AND DRIVER AMP
BLOCK DIAGRAM

B-453-0009
6-4-'65 d1

C. Circuits that comprise the Vertical Switching circuit:

1. Switching Logic Gate.
2. Delay Line Driver Amplifier; Q284, Q294.
3. Switching Multi; Q215, Q225, Q253.

4. Alternate Trace Sync Amplifier, Q234.
5. Chop Blanking Amplifier, Q244.

D. Block Logic

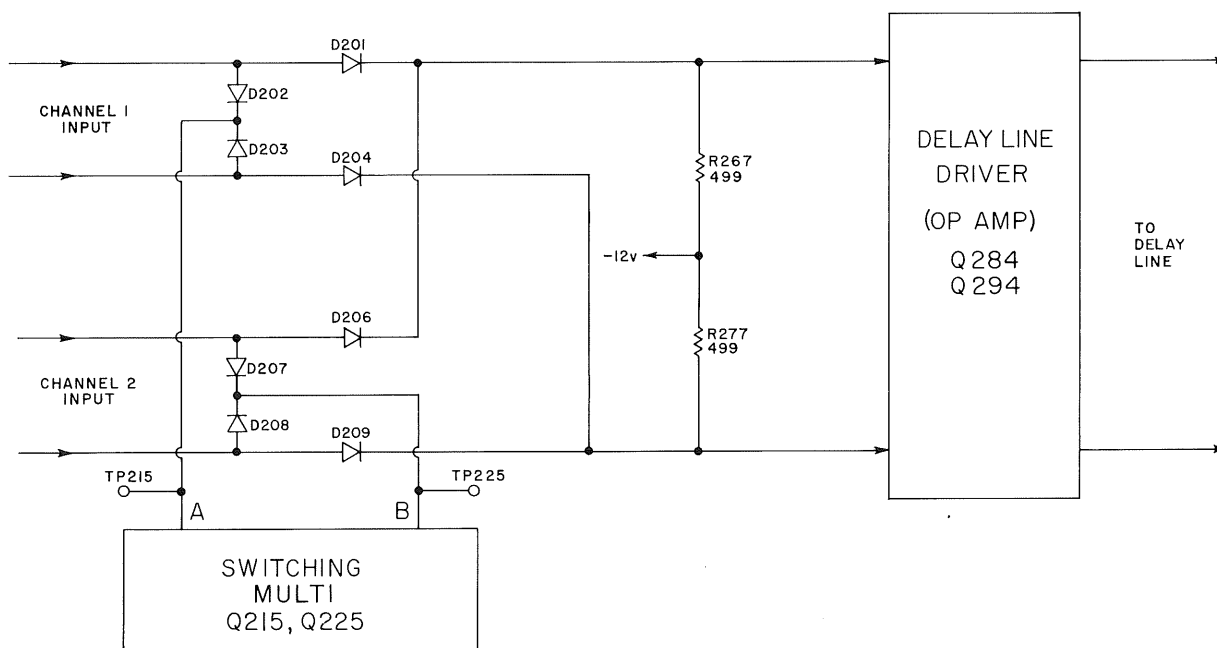
1. The output from each Vertical Preamp is a signal current about .5 ma/div per side.
 - a. 8 ma of static current also flows in each output lead.
 - b. DC level is -6v when the channel is off and -5v when connected to the Delay Line Driver Amplifier.
 - c. The small change in voltage as switching occurs helps maintain thermal balance in the CH 1, CH 2 Paraphase Inverter.*
2. The Switching Logic Gates switch the signal and static currents.
 - a. When ON, the signal currents drive the Delay Line Driver Amplifier.
 - b. When OFF, the signal and static currents are shunted through the Switching Multi circuit.
3. The Switching Multi controls the action of the Logic Gates.
4. Five modes of operation may be selected by the MODE switch.
 - a. CH 1: The output from the Channel 1 Input Amplifier is selected.
 - b. CH 2: The output from the Channel 2 Input Amplifier is selected.
 - c. ALT: The outputs from the two Input Preamplifiers are selected alternately at the end of each sweep.
 - d. CHOP: Signal from Channel 1 and Channel 2 are switched at a 500 kc rate.

* See Transistor Program, Volume 7, Page 111.

- e. ADD: The outputs from the two Input channels are added algebraically -- CMR is $\geq 20:1$ at 20 mc for common mode signals up to 8 divisions.
5. The vertical signal is amplified in the Delay Line Driver Amplifier to drive the Delay Line.
- Signal voltage into the delay line is 83 mv/div each side.
 - Signal current into the delay line is .9 ma/div.
6. A Chop Blanking signal is fed to the CRT circuit to blank switching transients in the CHOP mode.

E. Switching Logic Gates

1. The Switching Logic Gates consist of two sets of four diodes in bridge configuration.
- One logic gate for Channel 1 and a gate for Channel 2.
 - All eight diodes are 1N3605 silicon signal diodes.



TYPE 453 VERTICAL SWITCHING
SWITCHING GATES

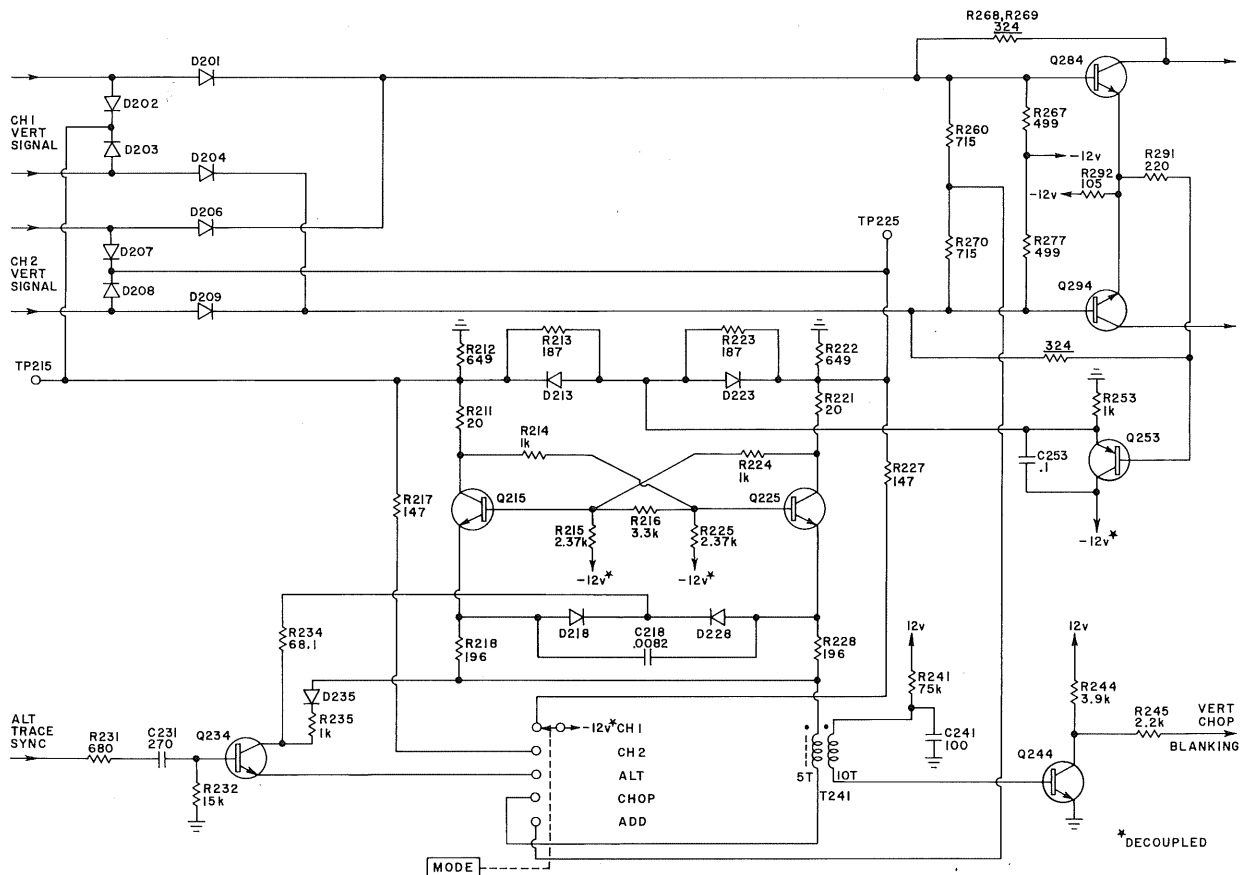
B-453-0010
6-9-'65dl

2. Switching voltage for the Logic Gates is supplied by the Switching Multi.
 - a. The switching voltage (from the Multi) swings from -5v to -6.7v .
3. About 8 ma of static current flows through each of the diodes (D201, D204, D206, D209) in the signal path.
 - a. The 8 ma supplies the Paraphase Inverter collectors (CH 1 and CH 2 Input Amplifiers).
 - b. About $.5\text{ ma/div}$ of signal current flows through each diode.
 - c. The signal current drives the Delay Line Driver Amplifier.
 - d. The static current is supplied through R267 and R277 from -12v .
4. The signal buses into the Delay Line Driver Amplifier set at about -6v .
5. When a signal path is opened by the Logic Gate, the signal current and the static current flows through the Multi circuit.
6. Assume that Multi output B (TP225) is at -5v and output A (TP215) is at -6.7v .
 - a. D202 and D203 will conduct as their cathodes are pulled down to -6.7v .
 - b. D201 and D204 cut off as their anodes are pulled down to -6.1v .
 - c. Collector current for the CH 1 Input Amplifier Paraphase Inverter transistors is now supplied by the Multi circuit.
 - d. Channel 1 is opened.
 - e. D207 and D208 cathodes are lifted to -5v cutting them off.

- f. D206 and D209 conduct -- the 8 ma static current and .5 mv/div signal current flows through each diode.
- g. Channel 2 signal current drives the Delay Line Driver.

F. Switching Multi, Alternate Trace Sync Amplifier and Chop Blanking Amplifier; Q215, Q225, Q253, Q234, Q244.

- 1. The Switching Multi is a transistorized multi that may be operated in either an astable or bistable mode.



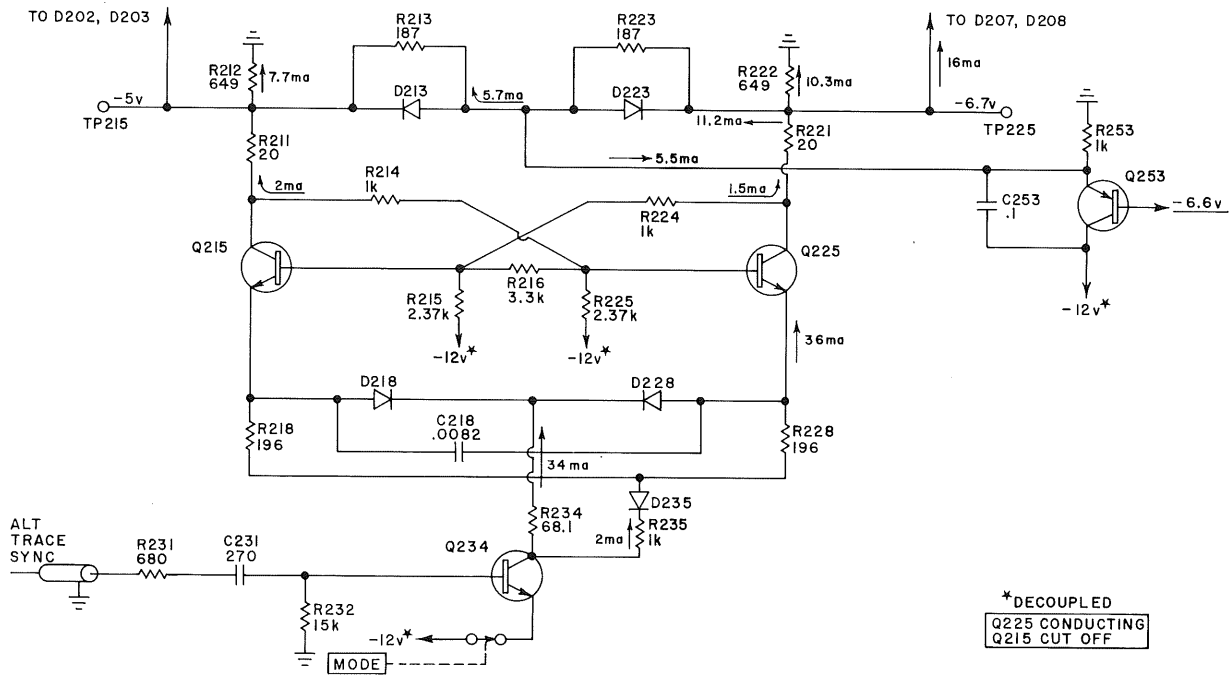
TYPE 453 VERTICAL SWITCHING SWITCHING MULTI

B-453-0011
6-11-'65dl

2. The circuits use five transistors and four diodes.
 - a. Q215 and Q225 are 151-136, 2N3053 silicon NPN transistors.
 - b. Q234 and Q244 are 151-108, 2N2501 silicon NPN transistors.
 - c. Q253 is a 151-087, 2N1131 silicon PNP transistor.
 - d. D213 and D223 are 6185 silicon diodes.
 - e. D218 and D228 are 1N3605 silicon diodes.
3. The Multi transistors receive emitter current through the MODE switch.
 - a. In CHOP and ALT modes, emitter current is supplied.
 - b. In all other modes, the Multi is turned off.
 - c. In CHOP mode, the multi is astable; switching at a 500 kc rep rate $\pm 20\%$.
 - d. In the ALT mode, the Multi is connected for bistable operation, switching with a trigger at the end of each sweep.
4. Operation in the ALT mode:
 - a. Quiescently, Q234 is saturated.
 - (1) The base is returned to ground.
 - (2) Q234 emitter is tied to $-12v^*$ (decoupled) through the MODE switch.
 - b. Assume Q225 is conducting and Q215 is cut off.
 - (1) TP225 sets at $-6.7v$ and TP215 sets at $-5v$.

* $-12v$ decoupled sets at about $-11.5v$.

- c. D228 is conducting Q225 emitter current (about 34 ma through D228).
- (1) A shunt current path through R235, D235 passes about 2 ma.



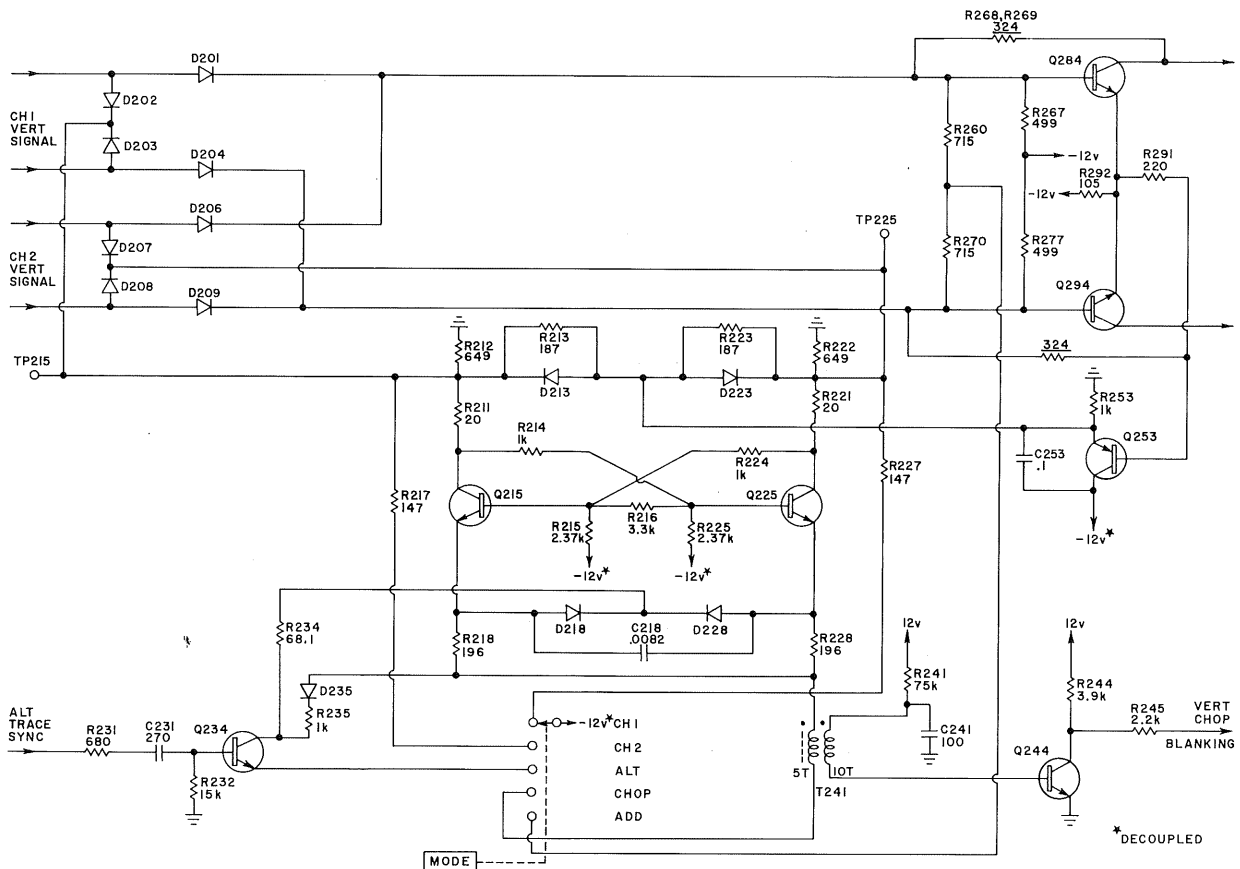
TYPE 453 VERTICAL SWITCHING
MULTI CURRENTS, ALT MODE

B-453-0012
6-14-'65dl

- d. Q225 collector is pulled down to -6.7v.
- e. Q225 base sets at -7.5v; Q215 base at -8.4v.
- f. Q225 emitter sets at -8.2v; Q215 emitter at -8.5v.
- (1) The divider composed of R228, D235 and R235 sets Q215 emitter level.
- (2) C218 is charged to 300 mv.
- g. At the end of sweep, the negative going Alt Trace sync pulse cuts off Q234.

- (1) The pulse is a negative step differentiated in C231, R232.
- (2) The pulse has a time constant of about 4 μ sec.
- h. Q234 cuts off for the pulse duration.
- i. Robbed of emitter current, Q225 cuts off.
 - (1) Both Q215 and Q225 are cut off for the pulse duration.
- j. Q225 collector (TP225) rises to -5v.
- k. As Q234 again saturates (after the sync pulse has passed), Q215 conducts.
 - (1) During the time both transistors were cut off, the bases were set by the cross coupled network at -8.4v.
 - (2) The 300 mv charge on C218 places Q215 emitter more negative than Q225 emitter.
 - (3) The charge on C218 (the commutator capacitor) directs Q215 to turn on.
- e. Through multi action, Q225 is held cut off until the arrival of the next sync pulse.
- 5. When Q225 is conducting, D207, D208 are pulled into conduction.
 - a. Channel 2 is cut off.
 - b. The 16 ma collector current for the Channel 2 Paraphase Inverter is supplied by Q225.
 - c. 36 ma flows through Q225 and 1.5 ma through R224, R215.
 - d. In addition to the 16 ma through D207, D208, 10.3 ma flows through R222 to ground, and 11.2 ma flows through D223.
 - (1) D223 clamps TP225 negative excursion at -6.7v.

6. Q215 collector sets at -5v (when cut off) lifting D202, D203 to cut off.
7. Q253 is an emitter follower connected in a DC feedback circuit whose purpose is to maintain the same voltage drops across the gate diodes even though the DC level on the signal buses might change.



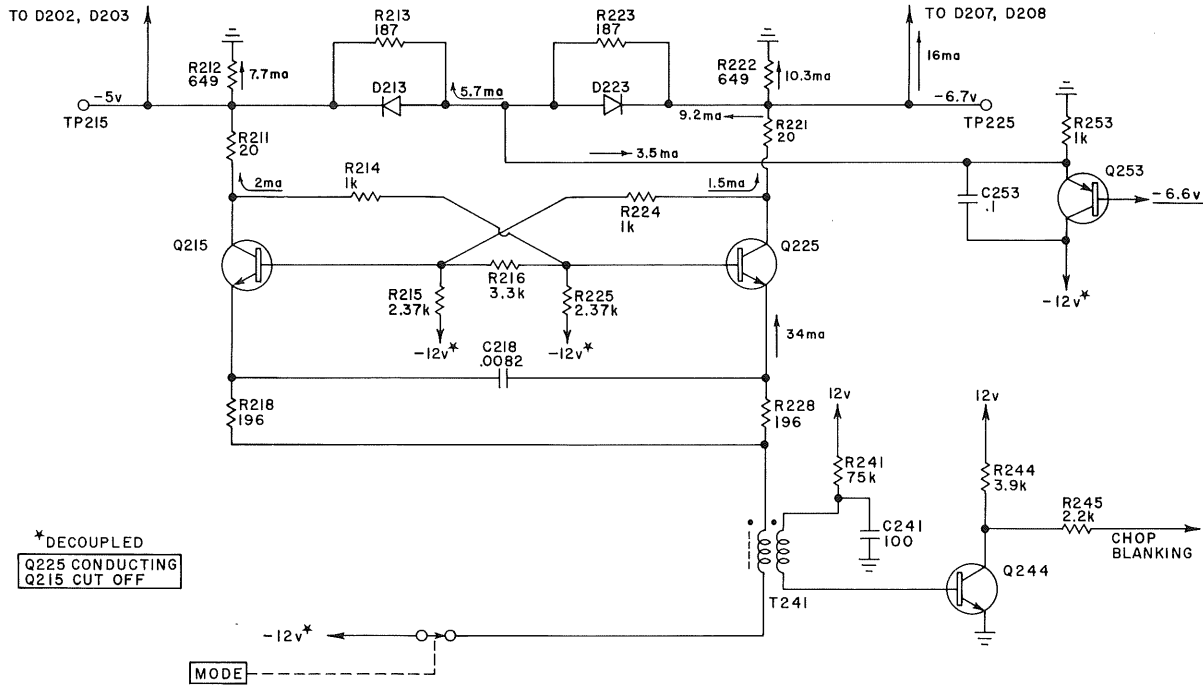
TYPE 453 VERTICAL SWITCHING
SWITCHING MULTI

B-453-0011
6-11-65dl

- a. Q253 base samples the DC level at Q284, Q294 common emitters (nominally -6.7v).
- b. The voltage on Q253 base is stepped .7v less negative to -6v at the emitter and back to -6.7v at D223 cathode (assuming Q225 conducting).

- c. The junction drop across D207, D208 sets the DC level at D206, D209 anodes to $-6v$.
 - d. Q284, Q294 base-emitter junction in turn places their bases at $-6v$.
 - e. D206 and D209, therefore, appear to be zero biased.
 - f. Q284, Q294, however, have a slightly greater base-emitter junction drop than Q253.
 - (1) Q284, Q294 each conduct about 26 ma.
 - (2) Q253 conducts a maximum of 3.2 ma.
 - g. The difference in junction drops reverse biases D206, D209 about 100 mv, assuring cut-off of the channel.
8. When both multi transistors are cut off, for the duration of the ALT trace pulse, all four of the series diodes (D201, D204, D206 and D209) conduct.
- a. 16 ma flows through each signal bus instead of 8 ma.
 - b. The signal buses rise about 1.2v for this period.
 - c. Q284, Q294 emitters and Q253 base rise a like amount.
 - d. Q253 emitter is held by the charge on C253.
 - e. Since this is a common mode signal, it disappears in subsequent push-pull stages.
9. In the CHOP mode, the multi becomes astable, running at 500 kc, $\pm 20\%$.
- a. Q234 is cut off as its emitter supply is opened by the MODE switch.
 - b. Robbed of current, D218, D228 and D235 cut off.

- c. Q215, Q225 emitters are returned through R218, R228 to -12v decoupled.



TYPE 453 VERTICAL SWITCHING
MULTI CURRENTS, CHOP MODE

B-453-0013
6-16-'65dl

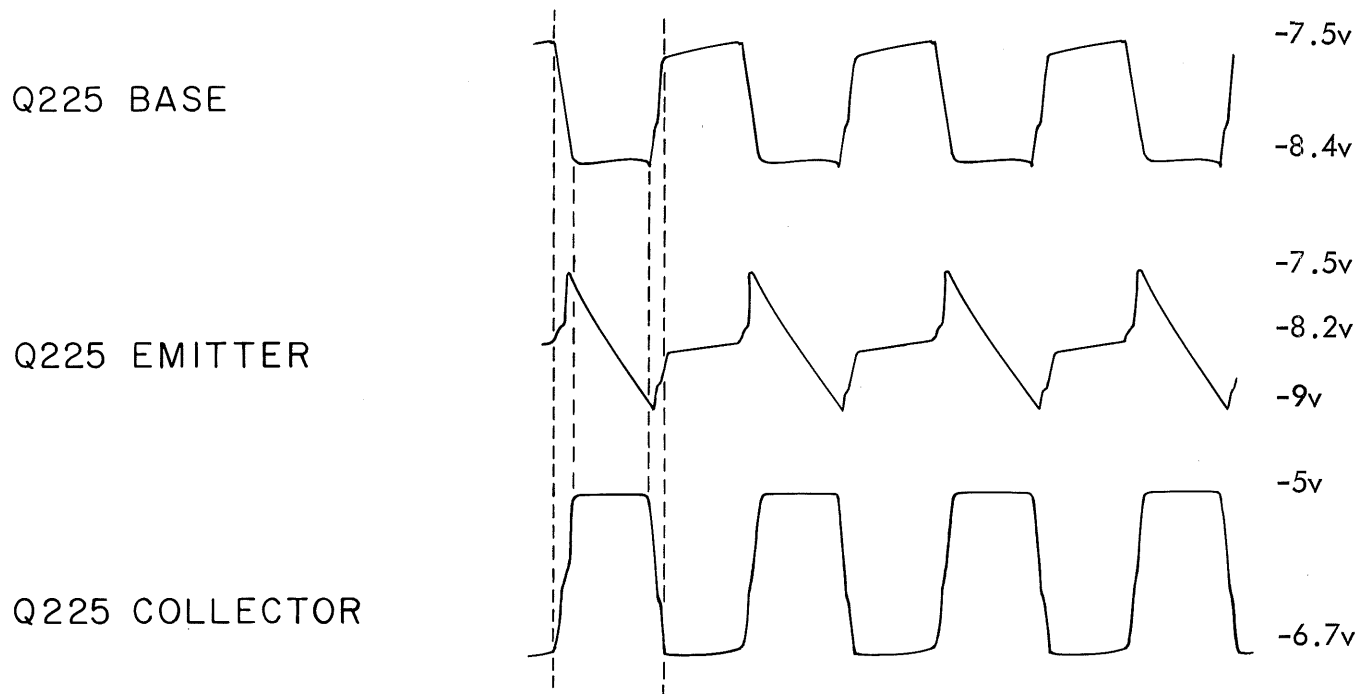
10. Assume Q225 is conducting and Q215 is cut off.

- a. Voltage levels on Q225 (conducting):

- (1) Base, -7.5v.
- (2) Emitter, -8.2v.
- (3) Collector, -6.7v.

b. Voltage levels on Q215 (cut off):

- (1) Base, -8.4v .
- (2) Collector, -5v .
- (3) Emitter, decreasing from -7.5v to -9v as C218 charges.



TYPE 453 VERTICAL SWITCHING
CHOP MODE WAVEFORM

B-453-0014

6-22-'65dl

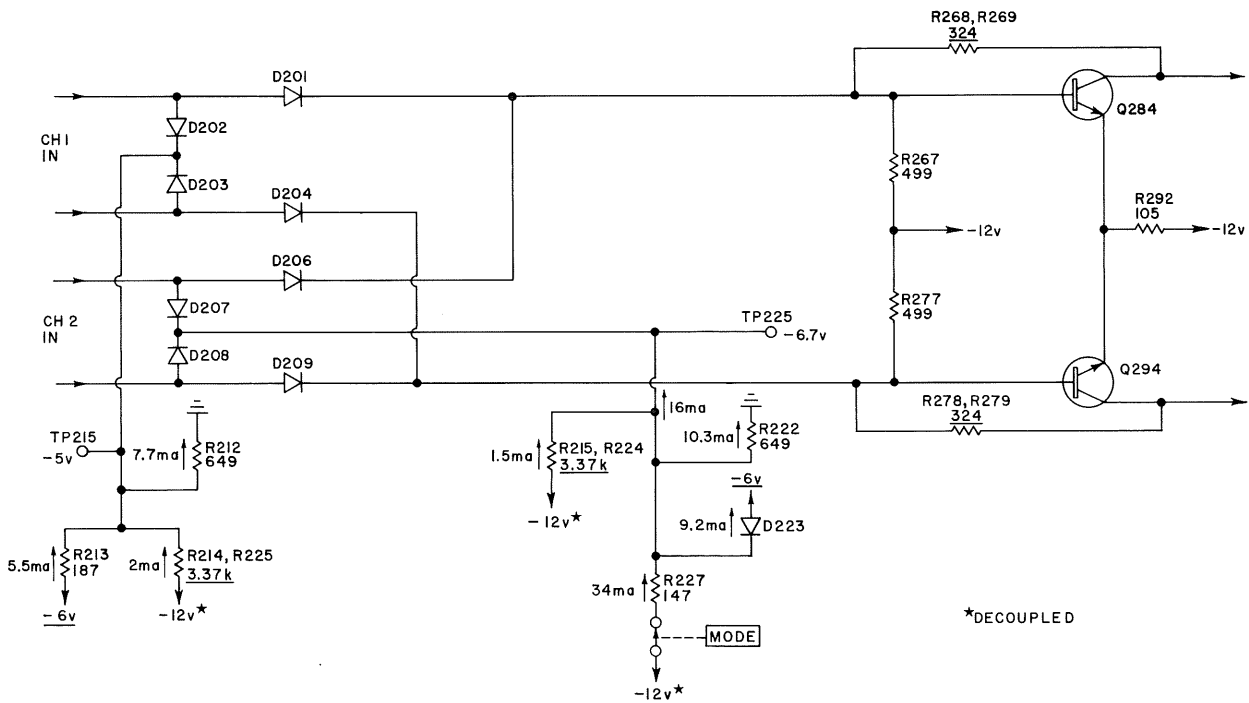
- c. As Q215 emitter reaches a point $.6\text{v}$ more negative than its base (about -9v), Q215 begins to conduct and the multi switches.
- d. As the multi flips and Q215 turns on, its emitter is pulled up to -8.2v .

- e. The .8v step couples through C218 to Q225 emitter, raising its level to -7.5v cutting off Q225.
 - f. As C218 discharges, Q225 remains cut off.
 - g. When Q225 emitter has dropped to -9v, Q225 conducts and the multi switches, completing the cycle.
11. Q225 (when conducting) conducts about 34 ma.
- a. About half the current flows through C218.
 - b. Current distribution is about the same as in ALT mode.
12. R211 and R221 prevent the multi from "sticking" at the time of initial turn on.
- a. If both transistors conduct simultaneously, D213 and D223 would both conduct.
 - b. The low impedance formed by the conducting diodes would effectively tie the collectors together, thereby reducing multi gain until the multi could not switch.
 - c. The resistors provide enough collector load resistance to allow the multi to switch.
13. Q244 is the CHOP Blanking Amplifier.
- a. When either of the multi transistors conduct, both emitters raise about .8v.
 - b. Most of the voltage drop appears across T241 primary.
 - c. The initial step is differentiated in T241 to appear as a negative going pulse at Q244 base.

- d. Q244 is saturated, quiescently.
 - (1) Q244 emitter is returned to ground.
 - (2) The base is tied through R241 to 12v.
- e. The pulse cuts off Q244 and its collector raises to 12v.
 - (1) A 2 ma pulse is fed to the Z axis amplifier for CRT blanking.
 - (2) The pulse is about .3 μ sec wide.

14. In the CH 1 and CH 2 positions of the mode switch, the multi is turned off.

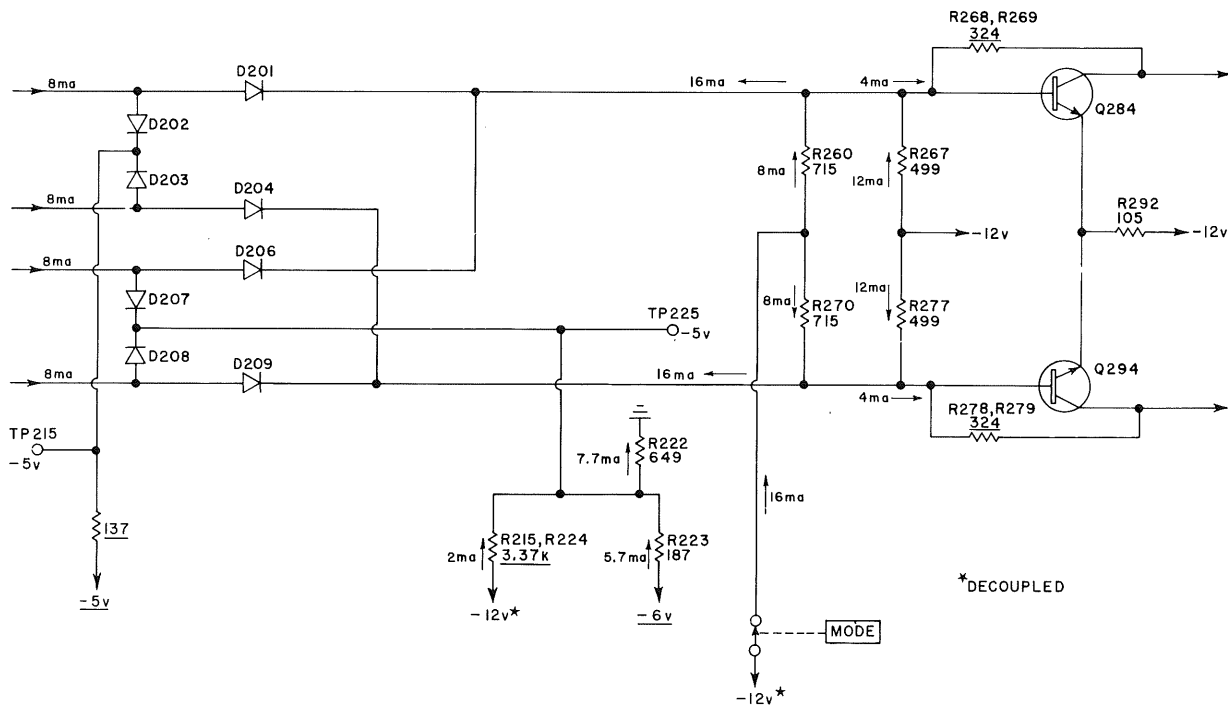
- a. The MODE switch opens the emitter supply to both transistors.



TYPE 453 VERTICAL SWITCHING
DIODE CURRENTS, CHANNEL I MODE

B-453-0015
6-21-'65dl

15. In CH 1 position, shunt diodes, D207 and D208, are connected through R227 to -12v decoupled.
- A total of 34 ma flows through R227.
 - 16 ma total flows through D207 and D208 to supply CH2 Paraphase Inverter collector current.
 - 10.3 ma flows through R222 and 9.2 ma through D223.
 - D207, D208 cathodes are pulled down to -6.7v.
 - D206, D209 are cut off.
 - Channel 2 is off.
16. Diodes, D202 and D203, are tied to the junction of R212, R213 and R214.
- The divider formed of these resistors lifts D202, D203 anodes to -5v, cutting off the diodes.
 - D201 and D204 conduct, passing Channel 1 signal current.



TYPE 453 VERTICAL SWITCHING
GATE CURRENTS, ADDED MODE

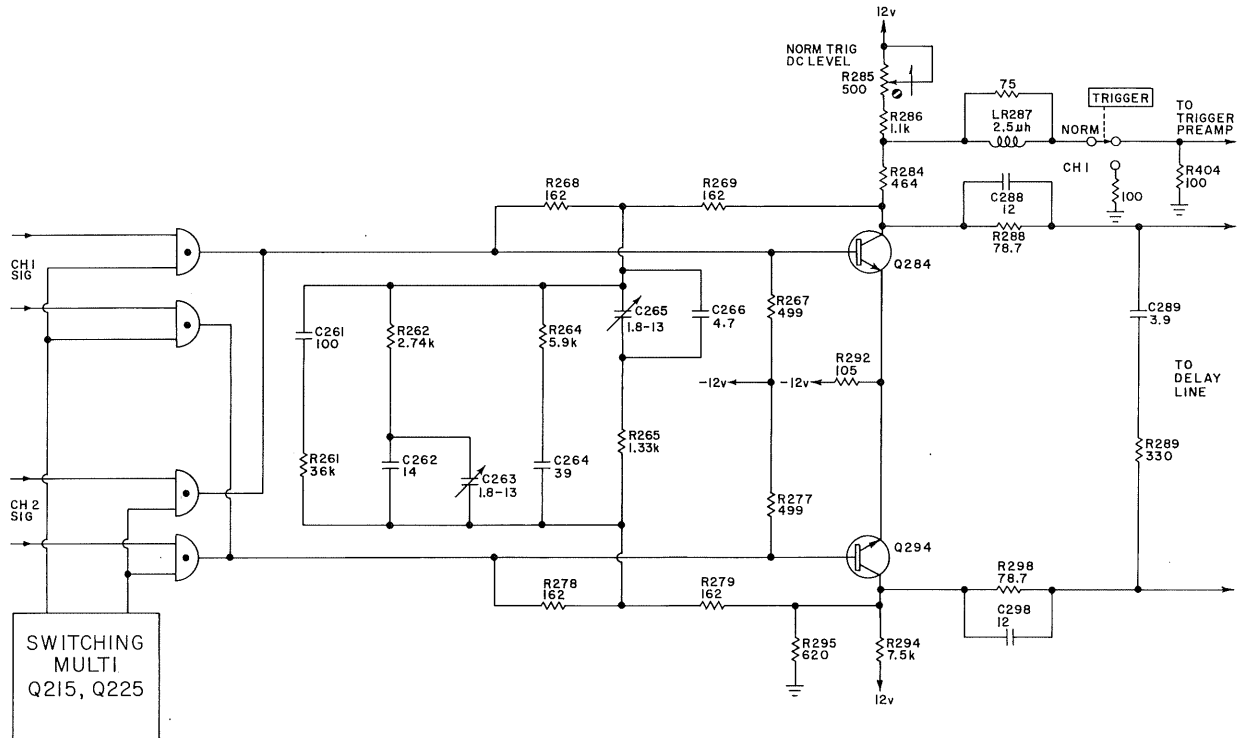
B-453-0016
6-23-'65 dl

17. In ADD (added algebraically) position, the Switching Multi is turned off as the MODE switch opens the emitter supply.
- a. The cathodes of all shunting diodes (D202, D203, D207 and D208) are tied to an equivalent -5v through an equivalent 137Ω .
 - b. The divider consisting of R215, R224, R222, and R223 (and the equivalent network composed of R225, R214, R212 and R213) form the equivalent 137Ω .
 - c. Both TP215 and TP225 set at -5v .
 - d. All shunting diodes are cut off.
 - e. All series diodes are conducting.
 - f. Each signal bus carries a total of 16 ma static current instead of the usual 8 ma.
 - g. Since no current is supplied by the shunting diodes, a circuit is provided to supply the required 16 ma.
 - h. R260 and R270 are connected in the ADD position of the MODE switch.

G. Delay Line Driver; Q284, Q294

1. The Delay Line Driver provides a push-pull signal voltage drive to the Delay Line.
 - a. The circuit is a push-pull feedback amplifier.
2. The transimpedance (from base to collector) is 310Ω .
 - a. Input signal current is $.49\text{ ma/div}$ per side.
 - b. Output signal voltage is 152 mv/div per side.
 - c. Signal current through the Delay Line is $.9\text{ ma/div}$ per side.
 - d. Current gain of the amplifier is 1.8.

3. Q284 and Q294 are 151-160, NPN silicon transistors.



TYPE 453 VERTICAL SWITCHING
DELAY LINE DRIVER

B-453-0017
6-25-65dl

4. DC conditions, center screen:
- Bases, -6v.
 - Emitters, -6.7v.
 - Collectors, -4.25v.
5. About 25.5 ma of static collector current flows through each transistor.
- 5.4 ma flows from the feedback path.
 - 10 ma flows through the rest of the collector load.

- c. 20 ma flows through the delay line to supply emitter current to the next stage.
6. The 8 ma collector current for the Paraphase Inverters in the input channel selected by the Mode switch is supplied by current through R267 and R277.
- a. R267 and R277 each supply 12 ma.
 - b. Aside from the 8 ma Input Amplifier, 5.4 ma flows through the feedback resistors (R268, R269, and R278, R279).
 - c. Q284, Q294 base current supplies the balance of the current.
7. R288, R298 plus the output impedance of the feedback amplifier provides the 93Ω per side reverse termination for the delay line.
- a. C289, R289 provides AC reverse termination.
 - b. C288, C298 compensate for increased output Z from the feedback amplifier at higher frequencies.
8. The feedback is shaped by a compensating network composed of four RC time constants.
- a. Two of the RC networks are variable.
 - b. The networks compensate for delay line and amplifier losses.
9. A single ended signal is taken off Q284 collector to feed the Trigger Preamp.
- a. Connection is made to the Trigger Preamp in the NORM position of the TRIGGER switch.
 - b. In the CH 1 position, the signal is terminated in 100Ω .

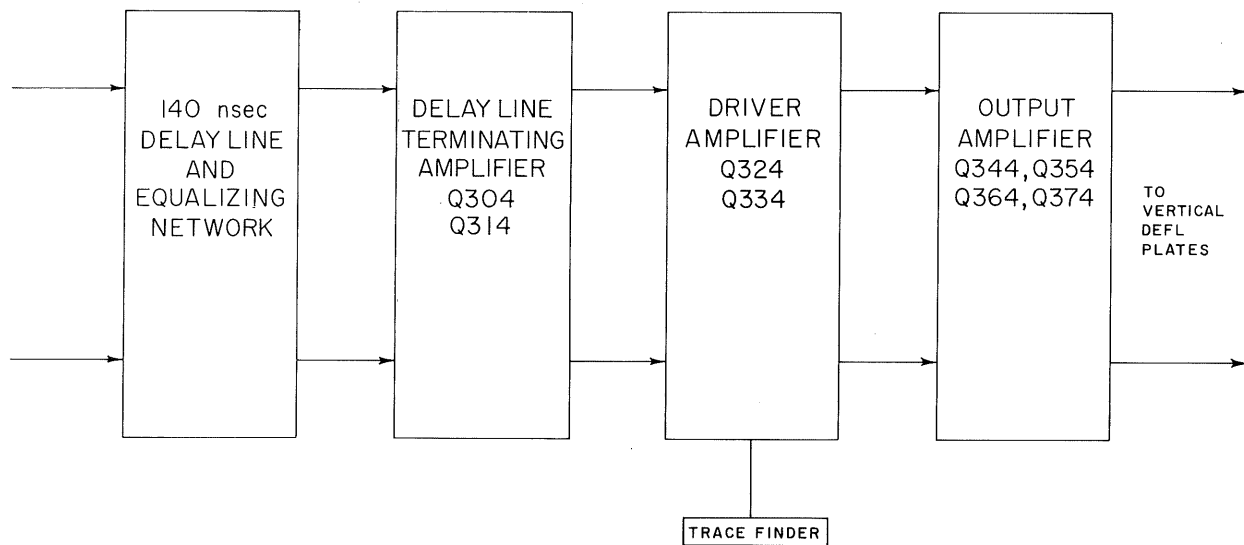
- c. Load impedance in either position is 100Ω .
 - d. Signal level is about 25 mv/div.
 - (1) The 152 mv/div at Q284 collector is attenuated in the divider formed of R284 and R404.
 - e. LR287 compensates for the overpeaking introduced by the feedback compensating networks.
 - (1) The vertical signal is overpeaked to drive the delay line.
 - (2) The trigger signal, however, is not subject to delay line losses, so the overpeaking must be reduced.
10. The NORM TRIG DC LEVEL control adjusts the Trigger Preamp output DC level to zero volts.
- a. The DC levels in all positions of the (Trigger) SOURCE switch are made compatible.
11. R295, R294 (in shunt with the feedback network) provide Q294 collector load resistance to match that of Q284.
- a. Q284 collector load resistance consists of R284 in series with R404 and LR287 in shunt with R286, R285 (in shunt with the feedback network).

V. VERTICAL OUTPUT AMPLIFIER

A. The Vertical Output Amplifier provides deflection voltage to the CRT vertical deflection plates.

1. CRT deflection sensitivity is 4.6 v/div* (2.3v/div per side).
2. A signal delay of 140 nsec is provided.
3. A TRACE FINDER switch limits the scan to about 4 div.

B. Block Diagram



TYPE 453 VERTICAL AMPLIFIER
BLOCK DIAGRAM

B-453-0018
6-25-'65 dl

* Spec is 4.1 v/div to 5.1 v/div.

C. Circuits that comprise the Vertical Output Amplifier:

1. Delay line and equalizing network.
2. Delay Line Terminating Amplifier; Q304, Q314.
3. Driver Amplifier; Q324, Q334.
4. Output Amplifier; Q344, Q354, Q364, Q374.

D. Block Logic

1. The T4530 CRT has a vertical sensitivity of 4.6 v/div (2.3 v/div per side).
2. Signal current through the delay line is .9 ma/div per side.
3. Transimpedance of the amplifier from delay line to CRT is 2.55k.

$$a. \quad T_Z = \frac{e_{out}}{i_{in}} .$$

$$b. \quad T_Z = \frac{2.3 \text{ v/div}}{.9 \text{ ma/div}} .$$

4. Gain of the entire vertical system changes with settings of the VOLTS/DIV switch.
- a. In the 5 mv/div position, the system has a voltage gain of 920.

$$(1) \quad A = \frac{4.6 \text{ v/div}}{5 \text{ mv/div}} .$$

$$(2) \quad \text{or } A = T_Y \times A_1 \times 2T_Z^*$$

where T_Y is the transadmittance of the input amplifier;

A is the current gain of the Delay Line Driver Amplifier;

T_Z is the transimpedance of the Vertical Output Amplifier.

$$(3) \quad A = 100,000 \mu\text{mhos} \times 1.8 \times 5.1\text{k} .$$

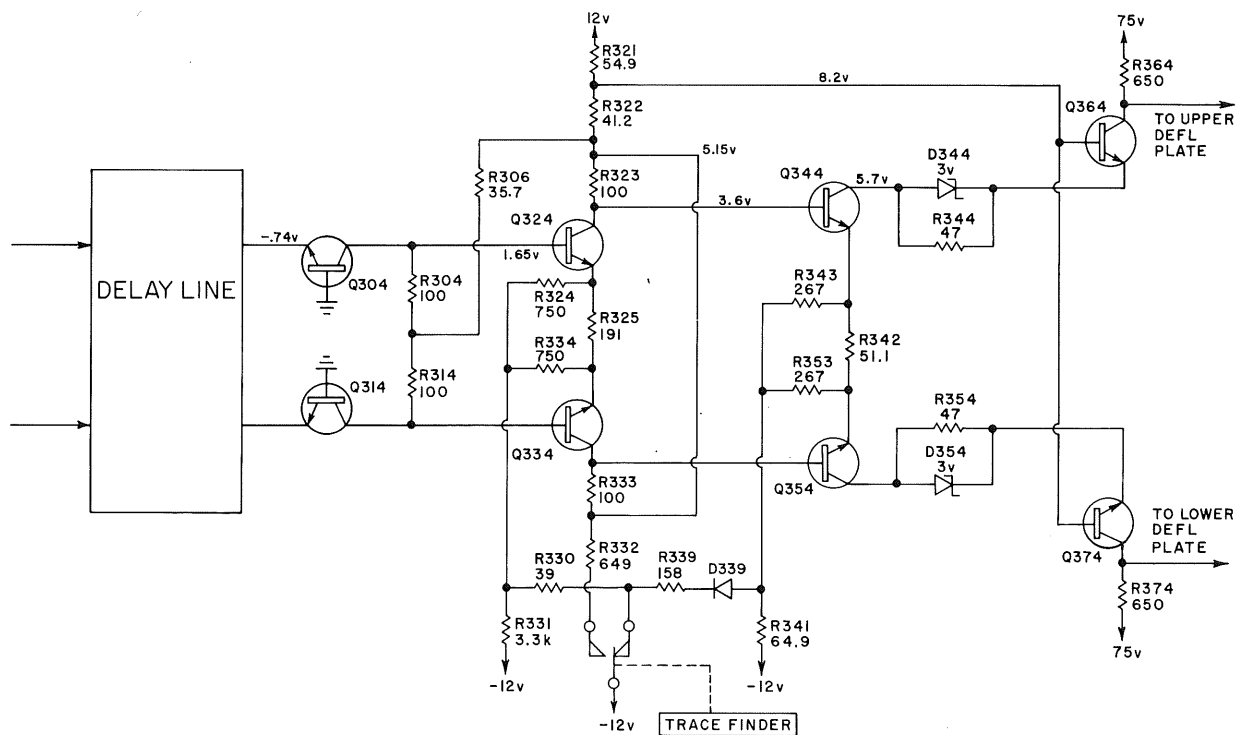
$$(4) \quad A = 920 .$$

* The push-pull amplifier has a value of $2 T_Z$.

- b. At 10 mv/div, $A = 460$.
 - c. At .02 v/div, $A = 230$.
5. The push-pull signal is delayed 140 nsec in the delay line.
 6. The Delay Line Terminating Amplifier is a grounded base stage.
 7. The Driver Amplifier is a push-pull stage with an output of 92 mv/div per side.
 8. The Output Amplifier is a push-pull cascode stage driving the vertical deflection plates with a push-pull voltage of 4.6 v/div.

E. DC Considerations

1. Common mode gain (DC) is reduced by tying the three stages to a common supply string.



TYPE 453 VERTICAL AMPLIFIER
DC CONSIDERATION

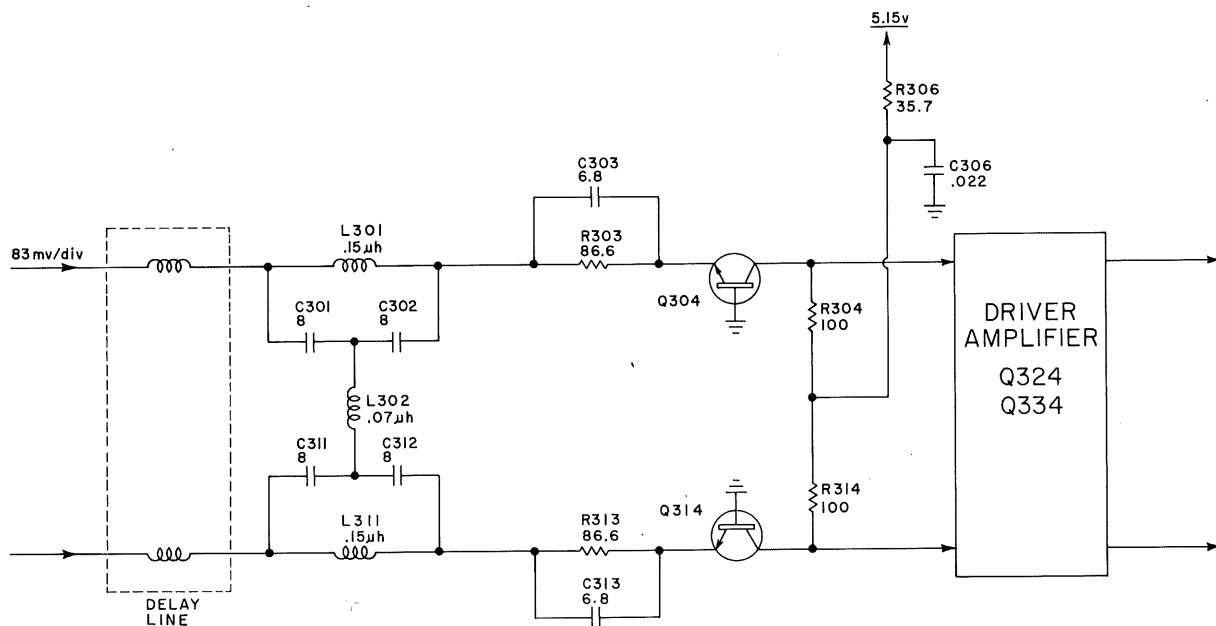
B-453-0019
6-29-'65dl

- a. Q304, Q314 collectors and Q324, Q334 collectors connect to a common point.
- b. Q364, Q374 bases connect to the same resistor string.
2. Thermal balance* conditions established in both the Driver and Output stages can be maintained if the base to collector voltages remain fairly constant.
3. Any common mode change at Q324, Q334 bases is effectively distributed among three pairs of transistors.
 - a. If a common mode signal would lift Q324, Q334 bases, the connection through R304, R314 and R306 would lift Q324, Q334 collector supply.
 - b. Q324, Q334 collectors would rise to compensate for the rise on the bases.
 - c. A portion of the change through R306 would lift the junction of R321, R322.
 - d. As Q364, Q374 bases rise, their emitters follow.
 - e. Since Q344, Q354 collectors are supplied by Q364, Q374 emitters, the collectors would rise to compensate for the rise on Q344, Q354 bases.
 - f. Some of the change would appear across Q364, Q374 base-collector junction.
 - g. Ideally, a third of the common mode change at Q324, Q334 bases would be dropped equally across each of the three pairs of transistors.

* See Transistor Program, Volume 7, Page 111.

F. Delay Line and Terminating Network.

1. The Delay Line is a counter wound 140 nsec cable.
 - a. It provides a delay so the signal that triggers the display can be displayed at the beginning of sweep.
 - b. The line delays both sides of the push-pull signal.
 - c. Characteristic impedance is 186Ω (93Ω per side).
 - d. The Delay Line and container are Tek made -- the same unit as used in the Type 647.
 - e. The line is shielded which allows it to be wound into a small container without coupling between input and output.



TYPE 453 VERTICAL AMPLIFIER
DELAY LINE AND EQUALIZING NETWORK

B-453-0020
6-30-'65dl

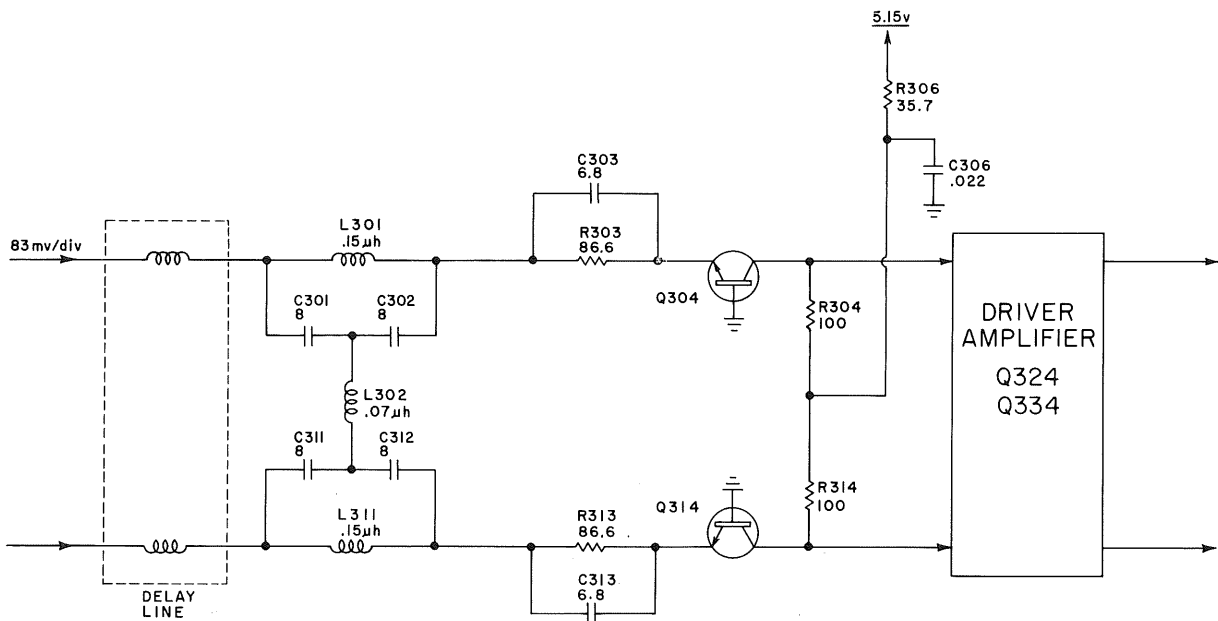
2. A delay line responds to a step with a preshoot (anticipation bump) and a risetime characteristic (dribble-up*).
 - a. The preshoot consists of two or three cycles of near 200 mc information that is coupled across the delay line with less than 140 nsec delay.
 - b. The dribble-up has a time constant of about 6 nsec.
 - c. A Phase Equalizer compensates for the preshoot.
 - d. A compensating network in the Delay Line Driver Amplifier overpeaks the signal before it enters the Delay Line, thereby reducing dribble-up.
3. L301, C301 and C302 (and L311, C311 and C312) form a Phase Equalizing network**.
 - a. The network provides a linear bandpass with a non-linear phase shift.
 - b. It corrects for delay line phase shift without frequency attenuation.
 - c. The 200 mc signal that comprised the preshoot is delayed the same amount in the Phase Equalizer as the rest of the signal is delayed in the delay line.
4. R303 (and R313) plus the emitter impedance of the Delay Line Terminating transistors provide the 93Ω (per side) Delay Line termination.
 - a. C303 (and C313) compensate for the increase in emitter impedance at higher frequencies.
 - b. AC termination is satisfied at all frequencies.

* See Nanosecond Pulse Measurements, by C. N. Winningstad.

** See Page 244, Radio Engineers Handbook, Terman.

G. Delay Line Terminating Amplifier; Q304, Q314

1. The DL Terminating Amplifier provides a low impedance termination for the Delay Line and isolates the Delay Line from the Driver Amplifier.



TYPE 453 VERTICAL AMPLIFIER
DELAY LINE AND EQUALIZING NETWORK

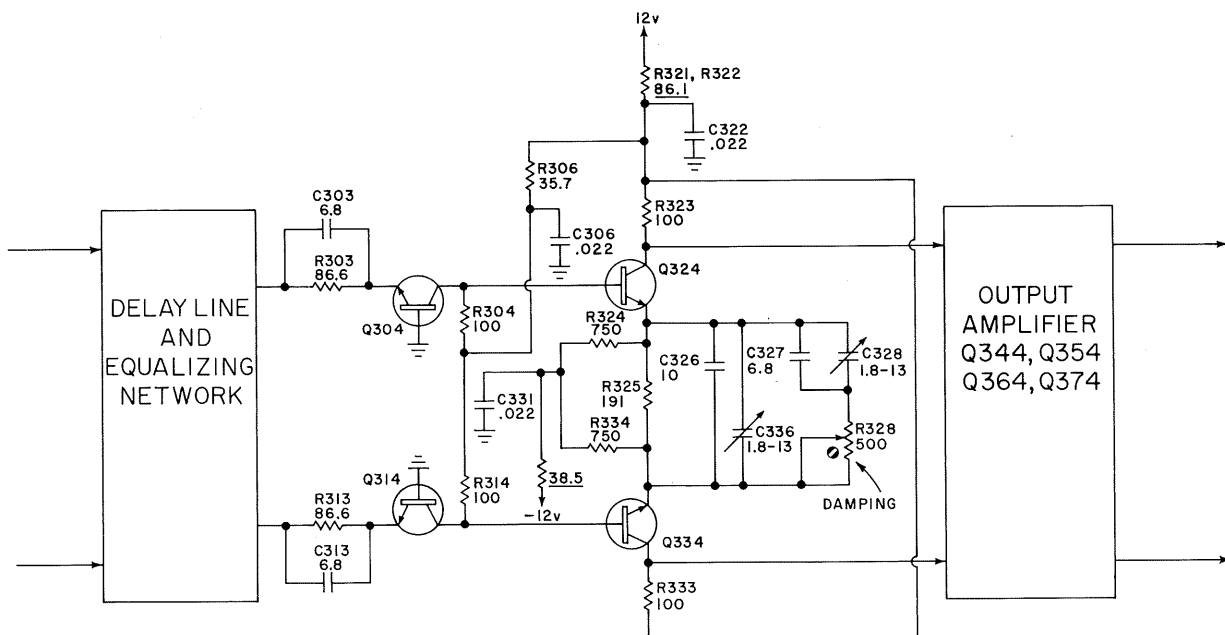
B-453-0020
6-30-'65 dl

2. The circuit consists of two grounded base amplifiers -- one for each side of the push-pull circuit.
 - a. The transistors are 151-108, 2N2501 silicon NPN transistors.
3. The amplifiers have no current gain.

- a. Signal current through each transistor is .9 ma/div.
 - b. Static collector current is about 20 ma per side.
4. R303 plus Q304 emitter resistance (and R313, Q314 r_e) provides the 93Ω per side delay line termination.

H. Driver Amplifier; Q324, Q334

1. The Driver Amplifier provides a voltage drive to the Output Amplifier.



TYPE 453 VERTICAL AMPLIFIER
DRIVER AMPLIFIER

B-453-002I
6-30-'65dI

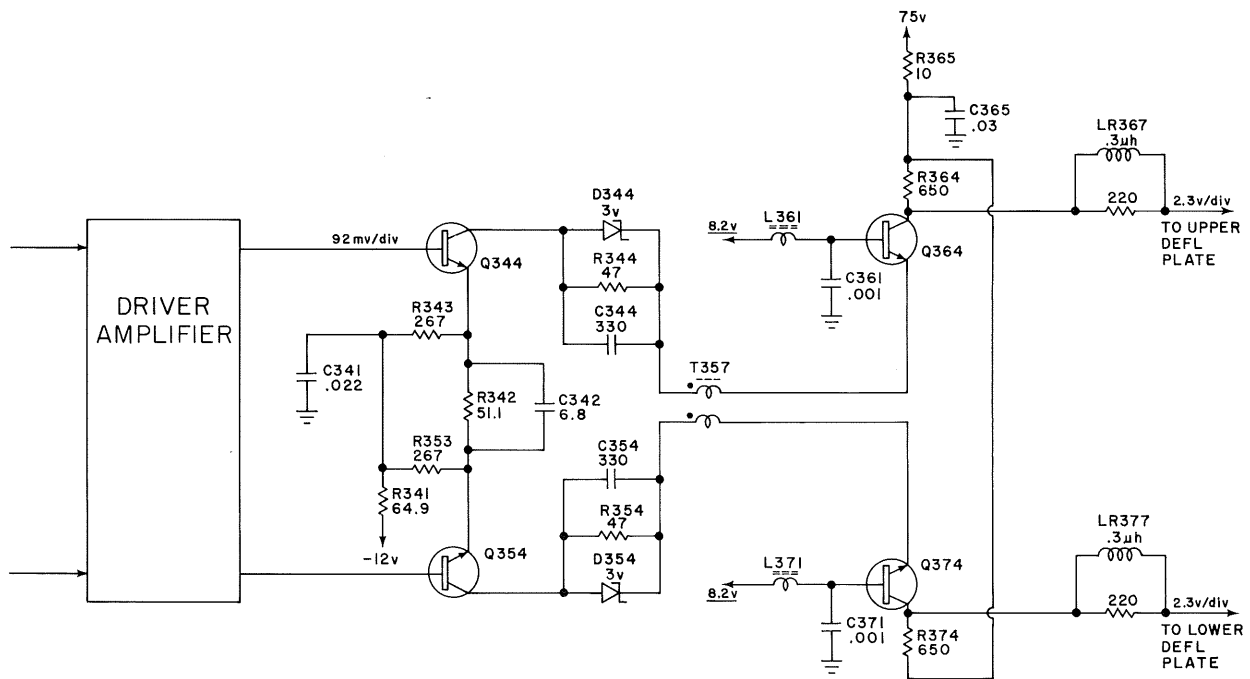
2. The amplifier has a transimpedance of about 100Ω .
 - a. Input signal current is $.9 \text{ ma/div}$.
 - b. Output voltage is 92 mv/div per side.
 - c.
$$T_Z = \frac{e_{\text{out}}}{e_{\text{in}}}$$

$$T_Z = \frac{92 \text{ mv/div}}{.9 \text{ ma/div}}$$

$$T_Z \approx 100\Omega.$$
3. The circuit is an emitter coupled push-pull amplifier.
 - a. The transistors are 151-120, 2N2475 silicon NPN transistors.
4. DC levels -- center screen.
 - a. Bases, 1.65v .
 - b. Emitters, 1v .
 - c. Collectors, 3.56v .
 - d. The junction of R323, R333 sets at 5.15v .
5. Collector load resistance is chosen to operate the transistors at the maximum power point on the curve for thermal balance in the push-pull circuit.
6. RC networks in the emitter coupling overpeak the signal to compensate for losses in the CRT circuit.
 - a. R325 introduces degeneration at medium and low frequencies.
 - b. The RC networks reduce the degeneration at high frequencies.
 - c. Two adjustable time constants are used.
 - d. The amount of peaking required is adjustable by the Damping control -- a screwdriver adjust on the Output Amplifier board.
7. C322 provides power supply decoupling.

I. Output Amplifier; Q344, Q354, Q364, Q374.

1. The Output Amplifier provides the voltage drive to the CRT vertical deflection plates.



TYPE 453 VERTICAL AMPLIFIER
OUTPUT AMPLIFIER

B-453-0022
7-2-'65dl

2. The circuit is a push-pull cascode amplifier.

- Q344 and Q354 are 151-127, 2N2369 silicon NPN transistors.
- Q364 and Q374 are 153-524, TA1938 silicon NPN transistors that are Tek matched for common base input capacitance.
 - They are mounted on berilium oxide heat sinks.
- D344 and D354 are 152-076, 3v 10% zener diodes.

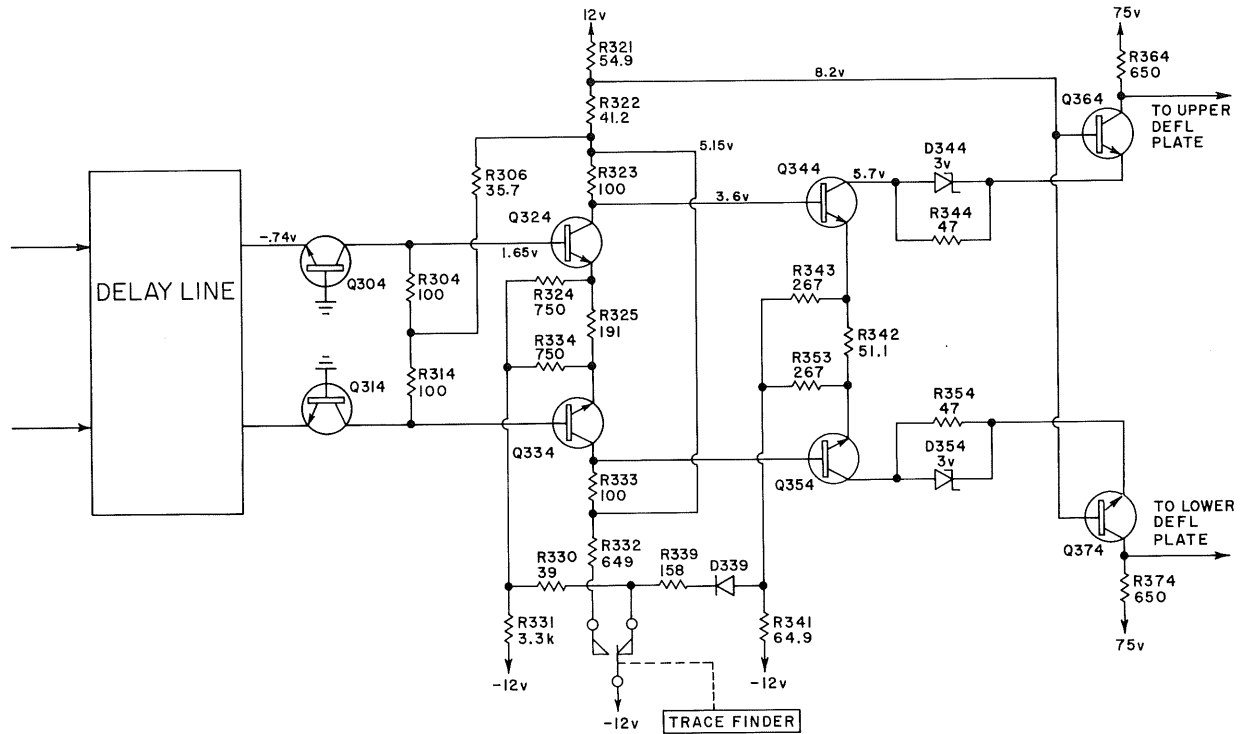
3. Essentially, the cascode amplifier is composed of an emitter coupled push-pull amplifier driving a grounded base amplifier.
 - a. The cascode amplifier does not load the Driver Amplifier with Miller capacitance.
4. CRT vertical deflection sensitivity is 4.6 v/div* push-pull (2.3 v/div per side) -- 48.8v center screen.
 - a. Mid screen current is 40.25 ma per side.
 - b. Signal current is 3.5 ma/div.
 - c. For the 6 division graticule signal current requirement is 21 ma.
 - d. Design considerations call for a 3 screen diameter capability (the 453 has a 3.8 screen diameter capability).
 - (1) For three screen diameters, the output would have a current swing of 8.75 ma to 71.25 ma -- $d_i = 62.5$ ma.
5. CRT deflection plate C, transistor C, stray C, and mounting plate C total about 10 pf per side.
 - a. Signal current required to drive the 10 pf is 15 ma
 - (1) $I = C \frac{d_e}{d_t}$
 where C is the 10 pf; d_e is 2.3v x 4.8 div (80% of 6 div graticule); d_t is 7 nsec risetime of the scope.
 - (2) $I = 15$ ma.
 - b. This additional current is generated in the peaking network in the Driver Amplifier.
6. Voltage gain of the amplifier is 350.
 - a. $A = \frac{3.2 \text{ v/div}}{92 \text{ mv/div}}$
 $A = 350$.

* Spec is 4.1v - 5.1 v/div.

7. R344 and R354 provide thermal balance for Q344, Q354
 - a. C344 and C354 keep HF signal voltage from forming across the thermal balance resistors, thus preventing Miller capacitance from loading the previous stage.
8. D344 and D354 keep Q344 and Q354 from saturating when the trace is driven off screen.
 - a. Stored charge in a saturated transistor would delay recovery after being overdriven.
 - b. D344 and D354 do not conduct in their zener region when the trace is on screen.
 - c. If the trace is moved below the screen, for example, increased current through Q344 would (without D344) pull its collector into saturation.
 - d. When the voltage drop across R344 reaches 3v, D344 conducts limiting Q344 collector and preventing saturation.
9. T357, a toroid transformer, improves push-pull balance by attenuating any AC common mode signal.
10. C361 and C371 bypass their respective bases.
 - a. L361 and L371 isolate the bypassed bases so they won't ring with lead inductance.
11. R364 and R374, the collector load resistors, are Tek made 4 watt components.
12. LR367 and LR377 separate the collector capacitance from deflection plate capacitance.
 - a. Low Q series peaking is provided by the L/R.

J. Trace Finder

1. The TRACE FINDER control is a front panel push button spring return switch.



TYPE 453 VERTICAL AMPLIFIER
DC CONSIDERATION

B-453-0019
6-29-'65dl

2. The control limits the range of the Driver Amplifier so the display cannot be driven off screen.
3. In the quiescent condition, all the Driver and the Output transistors are supplied with emitter current through one contact of the TRACE FINDER switch to -12v.

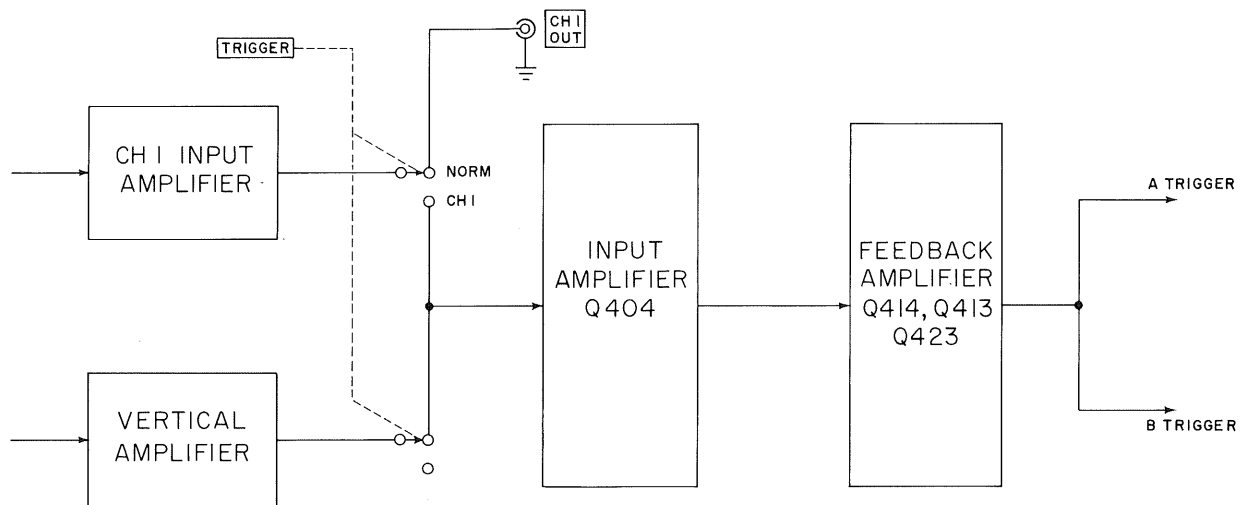
- a. About 14 ma is supplied to each Driver transistor through R330 and R331.
 - b. About 40 ma is supplied to each half of the Output Amplifier through R341 and R339 (equivalent 46.3Ω to $-11.6v$).
4. When the TRACE FINDER button is pressed, the connection to $-12v$ is opened.
- a. Current to the Driver Amplifier transistors is reduced to 3.5 ma total through R331.
 - b. As the display is moved to the bottom of the screen, one transistor in the push-pull amplifier will cut off.
 - c. The other transistor, robbed of its low impedance emitter ground return, becomes degenerative and cannot amplify.
 - d. The result is a display that is limited to less than the CRT screen excursion.
5. When the TRACE FINDER button is pressed, R332 is connected to $-12v$.
- a. 27 ma flows through the resistor to the $+12v$ supply to compensate for the lower current through Q324 and Q334.
6. Reduced current through Q324, Q334 causes their collectors to rise.
- a. Q344, Q354 bases will also rise.
 - b. As Q344, Q354 are biased to greater conduction, the increased current from the $75v$ supply might pull the supply out of regulation.
 - c. To compensate, D339 disconnects, increasing the emitter supply resistance to 64.9 (R341 instead of R341, R339 in parallel).
 - d. The resultant current through Q344, Q354 is essentially the same in either position of the TRACE FINDER switch.

VI. TRIGGER PREAMP

A. The Trigger Preamp amplifies the internal trigger signal to the level necessary to drive the Trigger Generator.

1. The circuit has inputs from the CH 1 Input Amplifier and the Vertical Delay Line Driver Amplifier.
2. The circuit can also be used to amplify an external signal to feed the EXT Horizontal Amplifier*.

B. Block Diagram



TYPE 453 TRIGGER PREAMP
BLOCK DIAGRAM

B-453-0023
7-6-'65 dl

C. Circuits that comprise the Trigger Preamp:

1. Input Amplifier, Q404.
2. Feedback Amplifier; Q414, Q413, Q423.

* See Page 12-3.

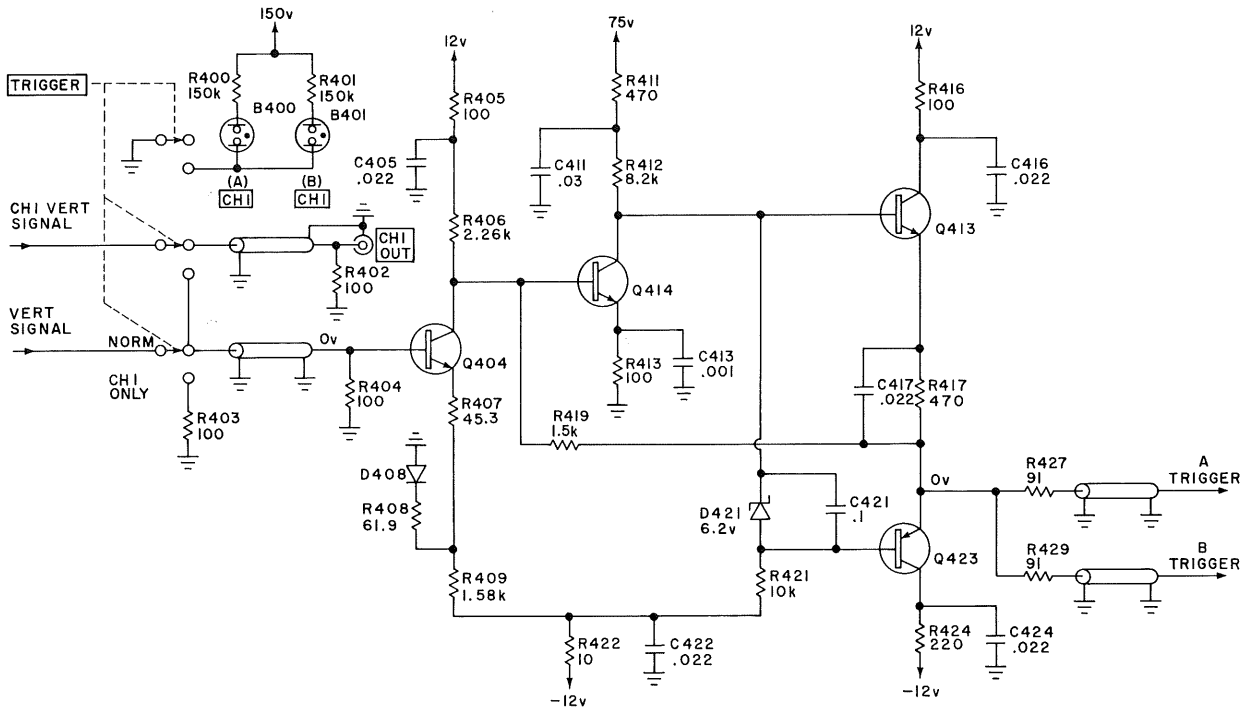
D. Block Logic

1. The Trigger Preamplifier has a gain of about 10.
2. Inputs are selected by the TRIGGER switch.
 - a. In the CH 1 position, the signal is taken from the CH 1 Trigger Out EF.
 - b. In the NORM position, the signal is taken from Q284 collector in the Vertical Delay Line Driver Amplifier.
3. Signal level in either case is 25 mv/div to 27 mv/div.
4. When the TRIGGER switch is in the NORM position, the CH 1 signal is present at the CH 1 OUT jack at the side panel.
5. The Input Amplifier has a signal current output to drive the Feedback Amplifier.
 - a. Signal output is about .167 ma/div.
6. DC level at the output is 0v.
 - a. The 0v level is set in the CH 1 position by the CH 1 TRIGGER DC LEVEL adj.
 - b. The level is set at 0v in the NORM position by the NORMAL TRIGGER DC LEVEL adj.
 - c. The DC level at the Trigger Preamp input will be near 0v*.
7. The Feedback Amplifier has 250 mv/div output signal.
 - a. INT trigger spec is .2 div (DC to 10 mc).
 - b. .2 div provides an output from the Trigger Preamp of 50 mv/div.
 - c. This is compatible with the 50 mv (DC to 10 mc) spec for EXT Trigger.

* If the CH 1 and CH 2 Input Amplifiers are cascaded (DC coupled), any DC offset at the CH 1 OUT jack could drive the trace off screen. CH 2 POSITION control may be adjusted to compensate for the offset, however.

E. Input Amplifier, Q404

1. The Input Amplifier provides a current drive for the Feedback Amplifier.



TYPE 453 TRIGGER PREAMP
TRIGGER PREAMP

B-453-0024
7-8-'65 dl

2. Q404 is a 151-120 silicon NPN transistor selected from 2N2475.
 - a. D408 is a 1N3605 silicon diode.
3. The TRIGGER switch is concentric with the Vertical Switching MODE switch.
 - a. It selects either the signal from the CH 1 Input EF or from the Delay Line Driver Amplifier.

- b. In the NORM position the switch selects the output from the Vertical Switching circuit.
 - (1) The trigger, therefore, depends on the position of the MODE switch.
 - c. In the CH 1 position, two indicator neons light -- one near the A TRIGGER SOURCE switch and one near the B TRIGGER SOURCE switch.
4. The 25 mv/div inputs from the CH 1 Input Amplifier and Vertical Amplifier are terminated in 100 ohms.
- a. These are 1% resistors that allow switching without changing the load on the Vertical Amps.
5. Q404 DC levels, with no trigger signals and VERTICAL POSITION centered:
- a. Base, 0v.
 - b. Emitter, -.7v.
 - c. Collector, 1.4v.
6. About 3.6 ma flows through Q404.
- a. Quiescently, 3.5 ma flows through D408.
 - b. About 7.1 ma flows through R409.
7. D408 temperature compensates Q404 base-emitter junction (ΔV_{BE}).
8. As the trigger signal varies the current through Q404, current through D408 varies inversely.
- a. Current through R409 remains constant.
9. Signal current drive to the Feedback Amplifier is .167 ma/div.

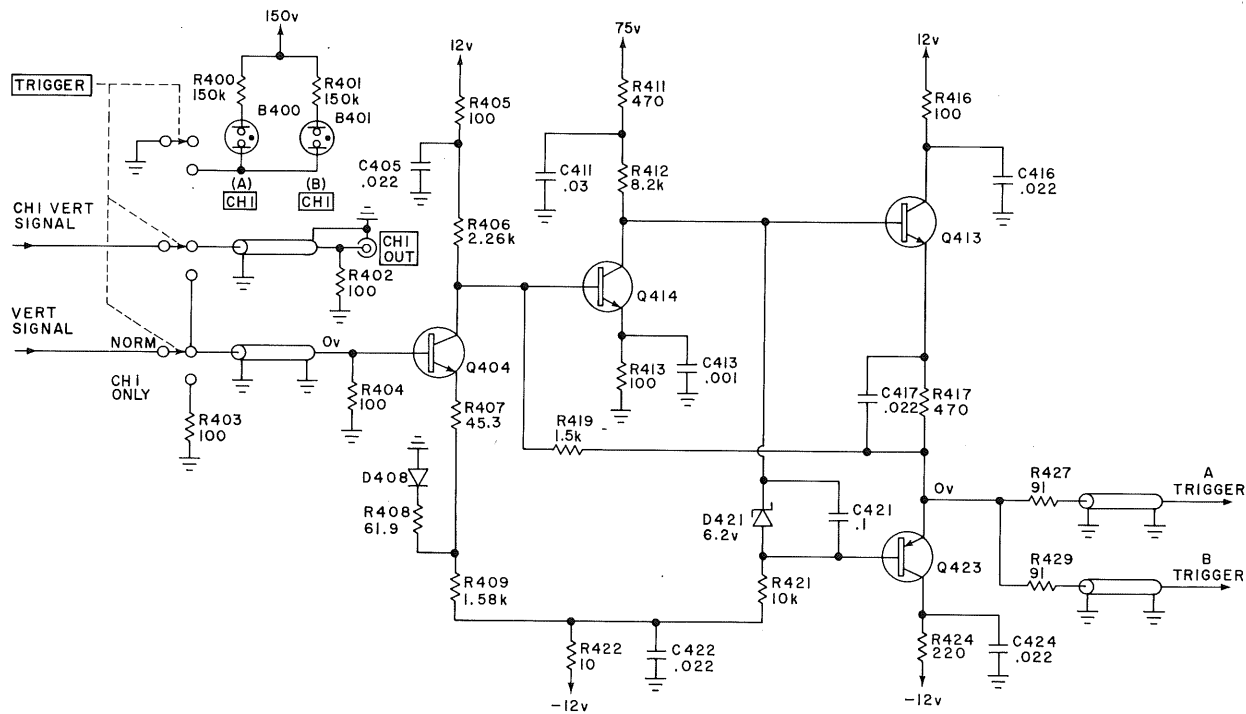
a. Transadmittance of the stage is $6700\mu\text{mhos}$.

$$\begin{aligned}
 \text{b. } T_Y &= \frac{i_{\text{out}}}{e_{\text{in}}} \\
 &= \frac{.167 \text{ ma/div}}{25 \text{ mv/div}}
 \end{aligned}$$

10. R405, C405 decouple the 12v supply.

F. Feedback Amplifier

1. The Feedback Amplifier supplies the voltage drive to the Trigger Generators.



TYPE 453 TRIGGER PREAMP
TRIGGER PREAMP

B-453-0024
7-8-'65 dl

2. The circuit consists of a gain stage, and a complimentary pair of emitter followers.
 - a. Q414 is a 151-127 silicon NPN transistor, type 2N2369.
 - b. Q413 is a 151-108 silicon NPN transistor, type 2N2501.
 - c. Q423 is a 151-133, MM999 silicon PNP transistor.
 - d. D421 is a 152-166, 6.2v 5% zener diode.
3. The complimentary emitter followers (one NPN and one PNP) provide near equal rise and fall times.
 - a. A PNP emitter follower has inherently poor risetime and good fall time (to a positive-going input signal).
 - b. An NPN EF has poor fall time and good risetime.
4. Open loop gain of the circuit is about 43.
5. The circuit has a transimpedance of 1500 ohms.
 - a.
$$T_Z = \frac{e_{out}}{i_{in}}$$

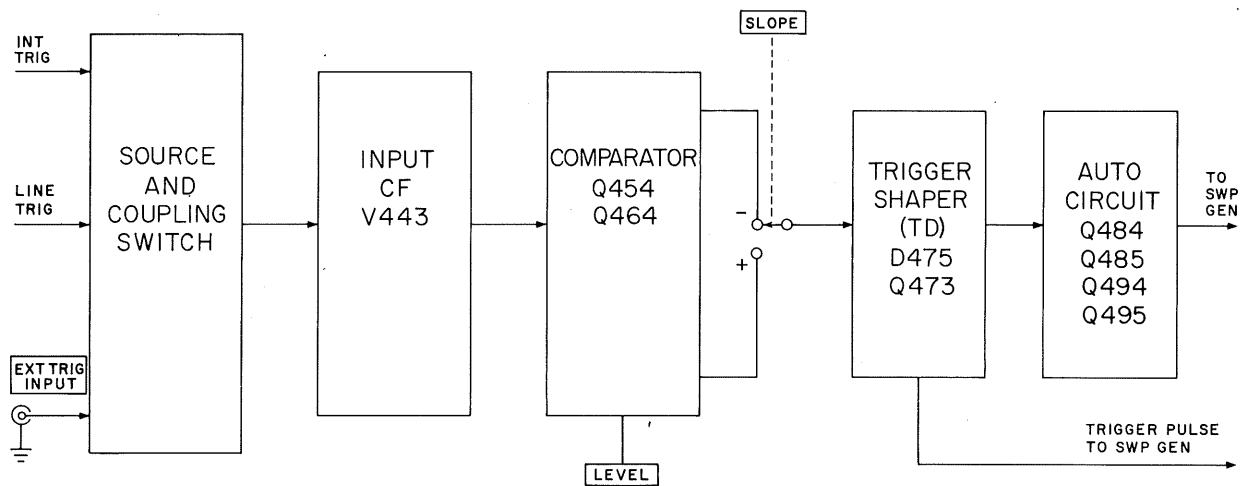
$$= \frac{250 \text{ mv/div}}{.167 \text{ ma/div}}$$
6. Q414 collector load is R412 in shunt with R421 -- an equivalent 4.5k.
7. The .167 ma/div signal current flows through R419 to swing the output 250 mv/div.
8. R417 sets the static current in the EF pair at 10 ma.
9. D421 sets Q423 base potential at -.66v.
10. All supplies are individually decoupled.
11. The outputs present identical drives to the A and B Trigger Generators.
 - a. R427 and R429 (plus the output Z of the feedback amplifier) reverse terminates the 93Ω coax cables that couple the signals to the two Trigger Generator boards.

VII. A TRIGGER GENERATOR

A. The A Trigger Generator provides a trigger of uniform shape and polarity for the A Sweep Generator.

1. An automatic circuit generates a signal that, in the absence of trigger, causes the A Sweep Generator to free-run.

B. Block Diagram



TYPE 453 A TRIGGER GENERATOR
BLOCK DIAGRAM

B-453-0025

7-9-'65 dl

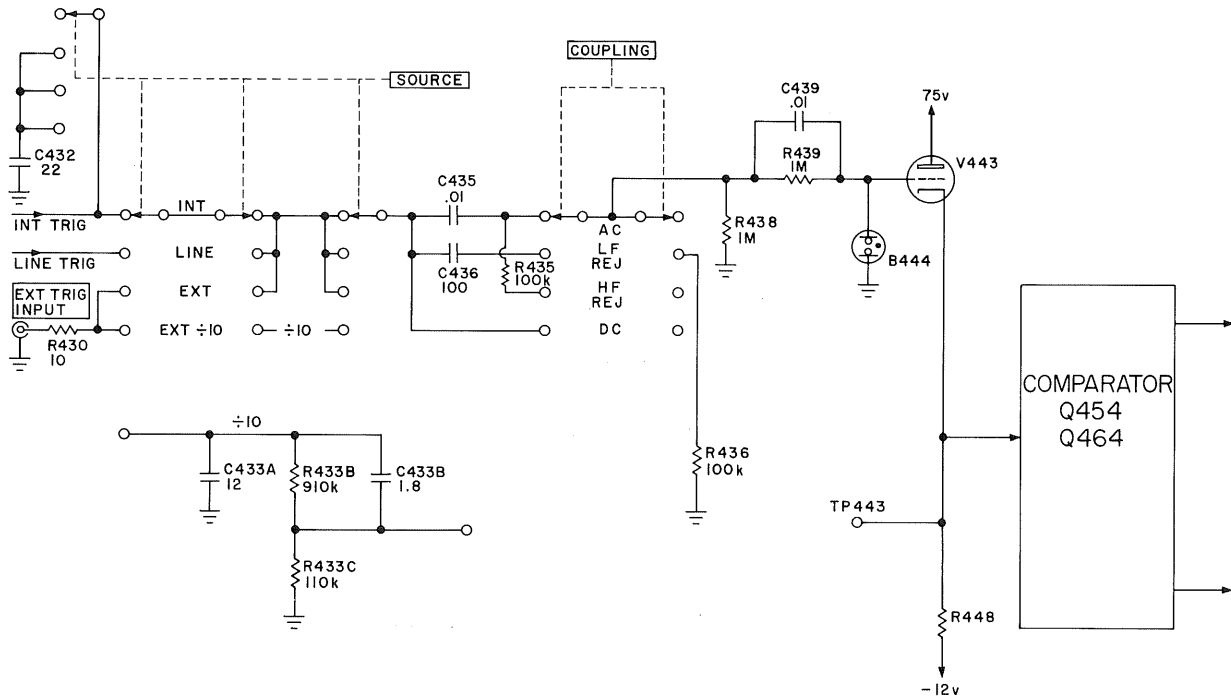
- C. Circuits that comprise the A Trigger Generator:
1. COUPLING and SOURCE switches.
 2. Trigger Input CF, V443.
 3. Comparator; Q454, Q464.
 4. TD Circuit; D475, Q473.
 5. Auto Circuit; Q484, Q485, Q494, Q495.
- D. Block Logic
1. The SOURCE switch has four positions, selecting three inputs:
 - a. INT: The internal trigger from the Trigger Preamp is selected.
 - b. LINE: 1.5v (RMS) AC is selected.
 - c. EXT: Connection is made to the EXT TRIG jack.
 - d. EXT $\div 10$: The External signal passes through a $\div 10$ attenuator.
 2. The COUPLING switch has four positions*:
 - a. AC: Lower 30% down at ≈ 16 cps.
 - b. LF REJ: Lower 30% down point, ≈ 16 kc.
 - c. HF REJ: Lower 30% down point, ≈ 16 cps, and upper 30% point is ≈ 100 kc.
 - d. DC: DC coupling.
 3. The selected trigger signal passes through the Input CF and is applied to the comparator.
 4. The trigger signal is compared (in the comparator) with a voltage level from the (Trigger) LEVEL control.
 5. When Trigger and LEVEL voltage comparison is made, a current from the comparator switches the Trigger Shaper TD.

* See Chapter 1 for trigger specifications.

6. Slope selection, made by the SLOPE switch, determines which trigger slope will switch the TD.
7. The output from the Trigger Shaper is a negative going trigger pulse that drives the A Sweep Generator.
8. A positive going trigger pulse inhibits the AUTO circuit.

E. SOURCE Switch

1. A lever wafer switch provides selection of INT, LINE, EXT and EXT ÷10.



TYPE 453 A TRIGGER GENERATOR
SOURCE AND COUPLING SWITCH

B- 453-0026
7-12-'65 dl

2. In the INT position, the output from the Trigger Preamp is selected.
 - a. Signal level is between 250 mv/div and 270 mv/div.
 - b. The INT signal is in turn subject to selection by the TRIGGER (CH 1 - NORM) switch.
 - c. Trigger sensitivity is .2 div to 10 mc, increasing to 1 div at 50 mc.
 - d. Source impedance is 93Ω .
3. In LINE position, a 1.5v RMS voltage is taken off the power transformer.
 - a. Source impedance is about 4.5k.
 - b. The AC trigger is phased so the trigger will be in phase with the power line (115v operation).
4. In the EXT position, connection is made directly to the EXT TRIG INPUT -- a BNC connection on the front panel.
 - b. R430 breaks up lead inductance.
 - c. Input Z is 1 Meg paralleled by approximately 20 pf -- not standardized.
 - (1) In LF REJ, the input Z changes to 91k paralleled by about 16 pf.
 - d. Maximum input voltage is $\pm 600v$ combined DC and peak AC.
 - e. Trigger sensitivity is 50 mv to 10 mc increasing to 200 mv at 50 mc.
5. In the EXT $\div 10$ position, a compensated attenuator is connected in series with the EXT TRIG INPUT.
 - a. Input Z is about 1 meg paralleled by about 20 pf.

- b. The attenuator is "approximately compensated" -- both the compensating cap and the standardizing cap are fixed 10% components.
- c. The resistors are 5%.

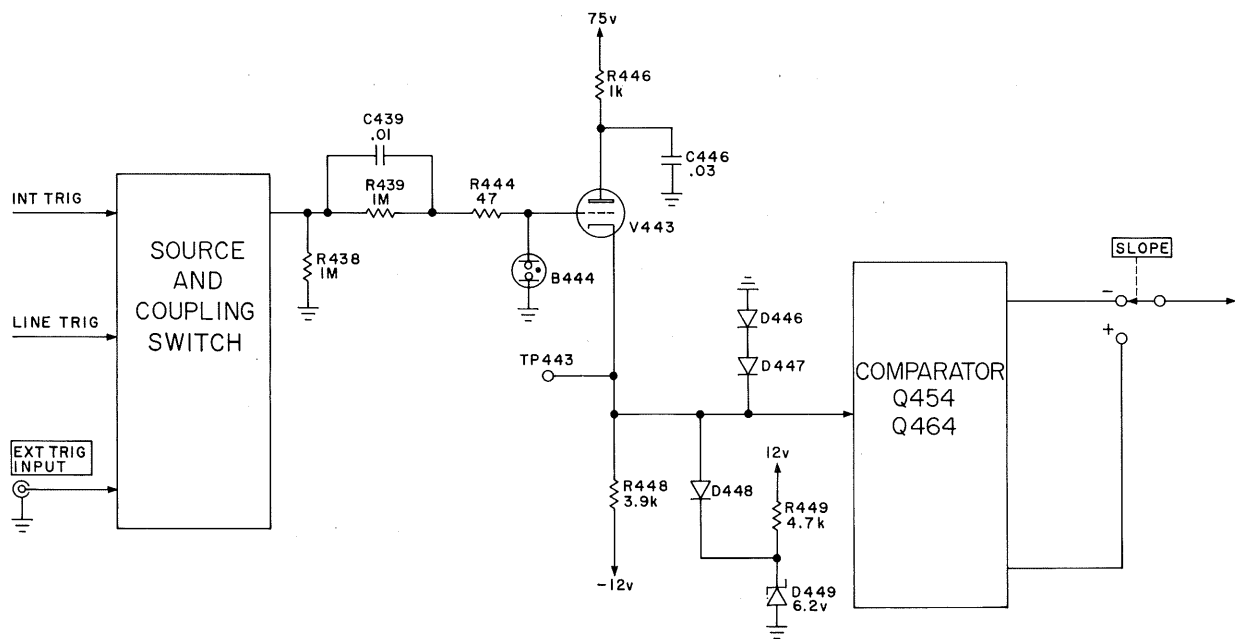
F. COUPLING Switch

1. The COUPLING switch is a lever wafer switch, selecting AC, LF REJ, HF REJ and DC coupling.
2. In the AC position, a .01 μf 1000v coupling cap is inserted.
 - a. Lower 30% down point is ≈ 16 cps.
 - b. The time constant is 10 msec.
3. In the LF REJ position, a 100 pf cap (C436) is placed in series with the input and a 100k resistor (R436) is placed in shunt with the 1M input R.
 - a. Input resistance is reduced to 91k (in series with 100 pf).
 - b. Input C remains about the same (as in AC), since the capacitance of R436 makes up for the C lost by placing C436 in series.
 - c. The lower 30% down point is about 16 kc.
 - d. T_C is about 9 μsec .
 - e. When the SOURCE switch is in the EXT $\div 10$ position, input Z is about 1M (960k AC), paralleled by about 20 pf.
4. In the HF REJ position, a 100k (R435) is placed in series with the input.
 - a. The input is AC coupled by C435.
 - b. The lower frequency 30% down point is ≈ 16 cps.

- c. Upper 30% down point is ≈ 100 kc.
- d. The higher frequencies are rolled off by integrating the input signal through R435 and the CF input C (plus strays).
- e. Input C is reduced to about 13 pf.

G. Input CF, V443

1. The Input CF provides high input impedance, and isolates the input from the load of the comparator circuit.



TYPE 453 A TRIGGER GENERATOR
INPUT CF

B-453-0027
7-12-65 dl

2. V443 is a 8393 nuvistor with a mu of 35.
 - a. The nuvistor has a 13.5v, 60 ma heater.
 - (1) It operates at 12v, however.
3. The signal, from the front panel mounted COUPLING switch, is fed to the A Trigger Generator board by a twisted pair -- the ground is carried by the other wire.
 - a. The twisted pair provides shielding without the high capacitance of a coax.
4. The nuvistor plate is decoupled from the 75v supply by R446, C446.
5. The cathode sets at a nominal 1.6v.
 - a. The nuvistor draws 3.5 ma.
6. R438 is the standard 1 meg input resistance.
7. R439 is a protective resistor that protects V443.
 - a. If a voltage at the EXT TRIG INPUT jack is raised to +600v, R439 limits nuvistor grid current to 600 μ a.
 - (1) A 8393 has a 2 ma maximum grid current rating.
 - b. C439 bypasses the protective resistor, supplying current to charge V443 input C.
8. B444 protects V443 from grid cathode arc-over.
 - a. If the EXT TRIG INPUT jack voltage is dropped below -80v, B444 will fire then sustain at about 60v.
 - b. V443 cathode will be clamped at -1.2v by D446, D447.
 - c. V443 bias, therefore, will ideally not exceed 58.8v.
 - (1) Actually, the bias will be 78.8v as the neon ignites.
 - (2) Since B444 is a 10% device, the bias could be as great as 96.6v at the time of ignition.

d. An 8393 has a maximum bias rating of 55v.

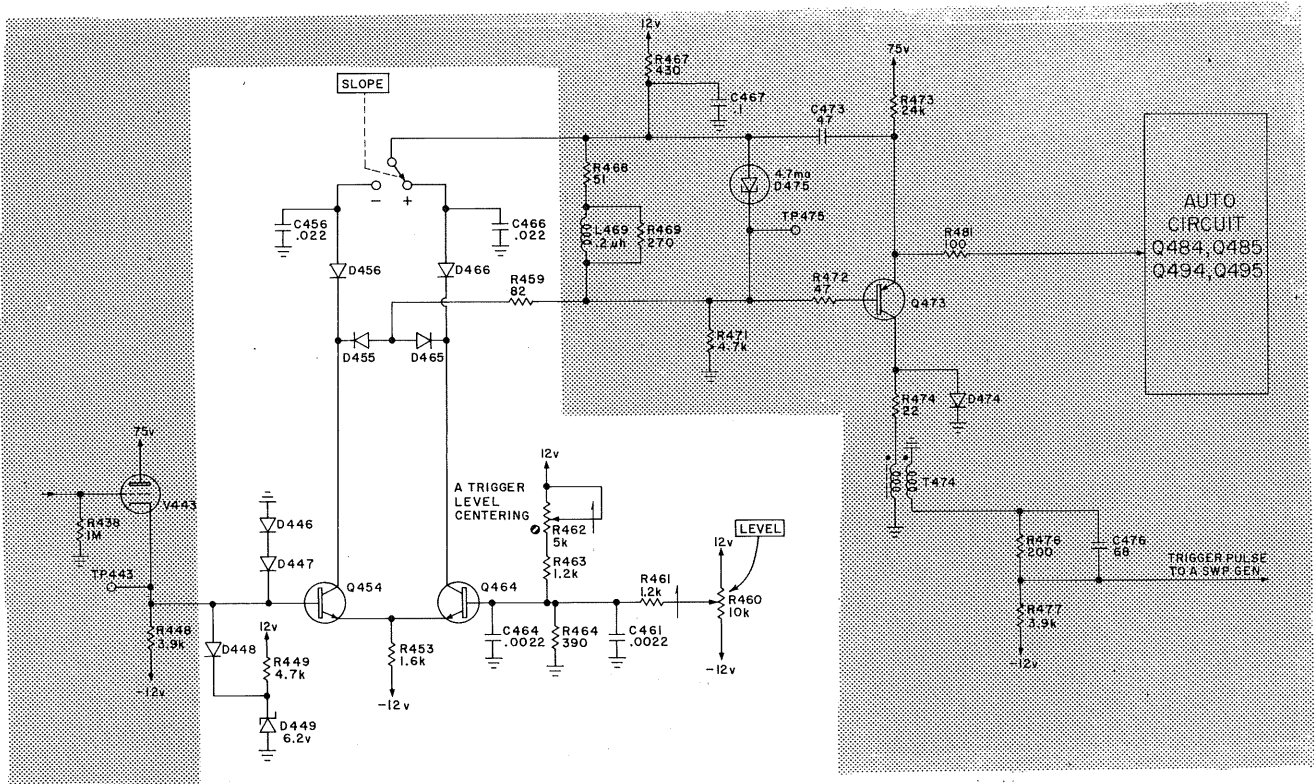
9. D446, D447 and D448 protect the Comparator transistors*.

H. Comparator; Q454, Q464

1. The Comparator provides a current trigger for the TD.

2. Q454 and Q464 are 151-108 silicon NPN, 2N2501 transistors.

a. The protective diodes and the switching diodes are 1N3605 silicon diodes.



TYPE 453 A TRIGGER GENERATOR
COMPARATOR

B-453-0028
7-14-'65 dl

* See Page 7-10.

3. Trigger voltage on the base of Q454 is compared with the voltage on Q464 base, as set by the (Trigger) LEVEL control.
4. The SLOPE switch provides selection of either + or - slope.
5. Each collector has two current paths selected by the SLOPE switch.
 - a. In the + SLOPE position, Q454 collector current passes through D455 and the TD circuit to +12v (through R467).
 - (1) D456 is cut off with its supply opened by the SLOPE switch.
 - b. In the + SLOPE position, D466 anode is connected to +8v*.
 - c. Q464 collector current flows through D466 to +8v*.
 - (1) D465 cathode is pulled up, cutting it off.
6. In the + SLOPE position, a positive going trigger will be applied to Q454 base.
 - a. Prior to the arrival of a trigger, Q454 and Q464 will be conducting equally -- about 4 ma each, depending on biasing or level setting.
 - b. As the signal on Q454 base raises the voltage level above that (set by the LEVEL control) on Q464 base, Q454 will increase conduction.
 - c. Q454 increased current flowing through the TD will switch it to its high state, generating a trigger pulse.
7. In the - SLOPE position, a negative going trigger or slope at Q454 base will initiate a trigger.
 - a. In this switch position, Q464 collector is connected through D465 to the TD.
 - b. Prior to the arrival of a negative going trigger signal, both transistors will conduct equally.

*12v decoupled through R467 places D456, D466 anodes at about 8v.

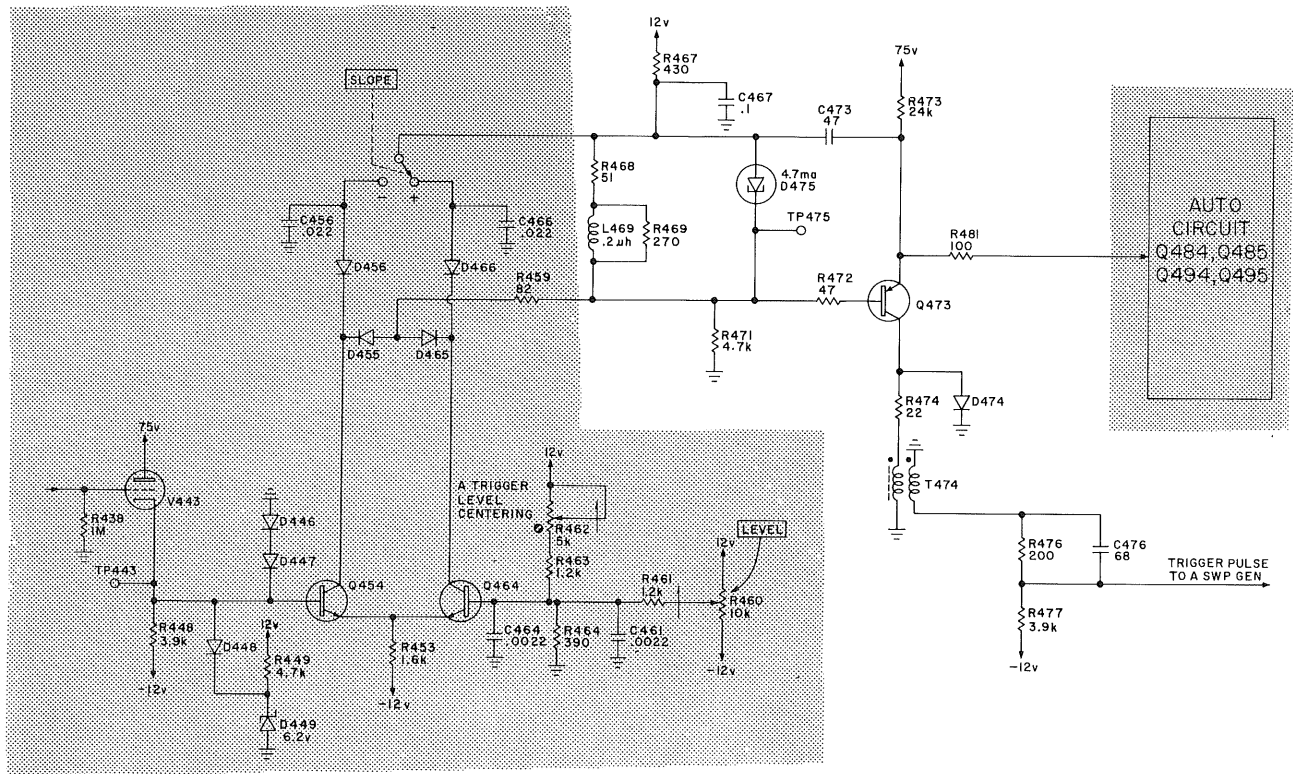
- c. As the trigger signal drops the voltage on Q454 base, its emitter follows.
 - d. Q454 conduction decreases as Q464 conduction increases.
 - e. Increased Q464 collector current switches the TD to its high state, initiating the trigger pulse.
8. The (Trigger) LEVEL control has a swing (at Q464 base) of about 5v -- one instrument tested had a swing of -1.6v to 4v.
9. The A TRIGGER LEVEL CENTERING control compensates for differing biases required for V443 -- tube aging, changing tubes, etc.
- a. The control has a range at Q464 base of about .7v.
 - b. When the control is properly adjusted (and the LEVEL control is centered), Q464 and Q454 conduct equally.
10. Although the Comparator bases normally operate close together, it is possible for the bases to be 9v apart.
11. D446, D447 and D448 protect Q454 and Q464 from base-emitter breakdown damage.
- a. Q454 base (and V443 cathode) is limited by D448 and D449 to about +7v.
 - (1) Q464 base can swing to -2.2v (both the LEVEL and TRIG LEVEL CENTERING controls full CCW).
 - (2) Q464 base-emitter junction would be reverse biased about 9v.
 - (3) A 151-108 is BV_{EBO} rated at 6v.
 - (4) Breakdown current is limited, however, to a safe value.

b. Q454 base is limited in its negative excursion by D446 and D447 to -1.2v.

- (1) Q464 base can be raised to +4.3v (both controls clockwise).
- (2) Under this condition, Q454 base-emitter junction would be reverse biased about 5.2v.

I. Tunnel Diode Trigger Shaper; D475; Q473

1. The Trigger Shaper provides a trigger of fairly uniform amplitude and shape to drive the Sweep Generator.



TYPE 453 A TRIGGER GENERATOR TD CIRCUIT

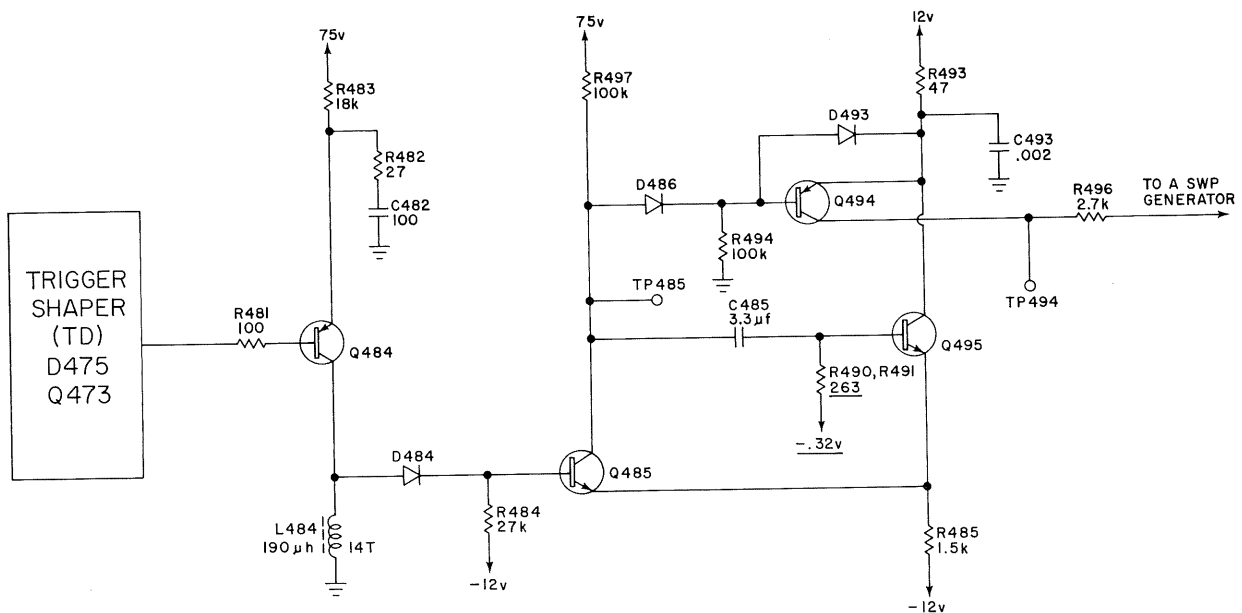
B-453-0028.1
7-14-'65 dl

2. The circuit uses a TD, a transistor and a signal diode.
 - a. D475 is a 152-125, 1N3717, 4.7 ma tunnel diode.
 - b. Q473 is a 151-131, 2N964 germanium PNP transistor.
 - c. D474 is a 1N4244 silicon diode.
3. The output trigger (to the Sweep Generator) is a negative going 3 ma to 8 ma pulse of about 8 nsec duration.
4. The TD (D475) is quiescently in its low state.
 - a. About 5.7 ma flows through the TD and its load resistor, R468.
 - (1) 4 ma flows from the comparator.
 - (2) 1.7 ma flows through R471.
 - b. 5.9 ma (through the TD and load resistor) is required to switch the TD to its high state.
 - c. Voltage drop across D475 is about 65 mv.
 - d. D475 cathode (and Q473 base) sets at about 8v.
5. Quiescently, Q473 draws about 2.8 ma.
6. The arrival of a trigger signal causes the comparator current to increase.
 - a. When the current through the TD and its load resistor reaches 5.9 ma, the TD switches to its high state.
 - b. The voltage drop across the TD jumps to approximately 500 mv.
 - c. D475 anode is held, momentarily by C467.
7. As D475 cathode (TP475) drops, Q473 current increases.
 - a. Q473 emitter is bypassed, briefly, by C473.
 - (1) The time constant is about 1 nsec.

- b. As Q473 collector pulls up, it is caught at .6v by D474.
 - (1) D474 limits the range of the output current pulse.
 - (2) As current through T474 primary reaches 5 ma to 8 ma, the additional collector current is supplied by D474.
 - c. After C473 time constant, Q473 emitter degeneration virtually stops collector current and the trigger pulse ceases.
 - (1) The trigger is 3 to 5 nsec wide.
 - d. As C473 discharges and Q473 emitter begins to follow its base, the emitter waveform is coupled to the Auto circuit.
 - (1) The waveform is a negative going 500 mv step.
8. Signal current through R467 will cause the decoupled supply voltage (decoupled by R467, C467) to move with respect to ground.
- a. Any signal applied to the Comparator will cause the decoupled supply to move with inverted polarity.
 - b. A calibrator signal, for example, will show a square wave with some rounding of the leading edge as C467 charges.
 - c. The waveform at TP475 will be the composite of the voltage at the decoupled supply and the drop across D475.
 - (1) If the SLOPE switch is in + SLOPE, the two voltages will add.
 - (2) If in - SLOPE, the voltages will appear as the difference; showing a series of spikes where the fast switching waveform of the TD appears during the interval when C467 is charging.

9. L469 and R469 form part of the TD AC load impedance.
 - a. When the TD switches to its high state, the inductance provides a high load resistance, thereby increasing the voltage drop across the TD as it switches to its high state.
 - b. The Trigger Shaper will follow an input trigger to about 65 mc.
10. R459 isolates the fast switching TD from the Comparator circuit.
11. The circuit output to the Sweep Generator is set at $-.57$ volts by the compensated divider composed of R476, R477 and C476.

K. Auto Multi; Q484, Q485, Q494, Q495



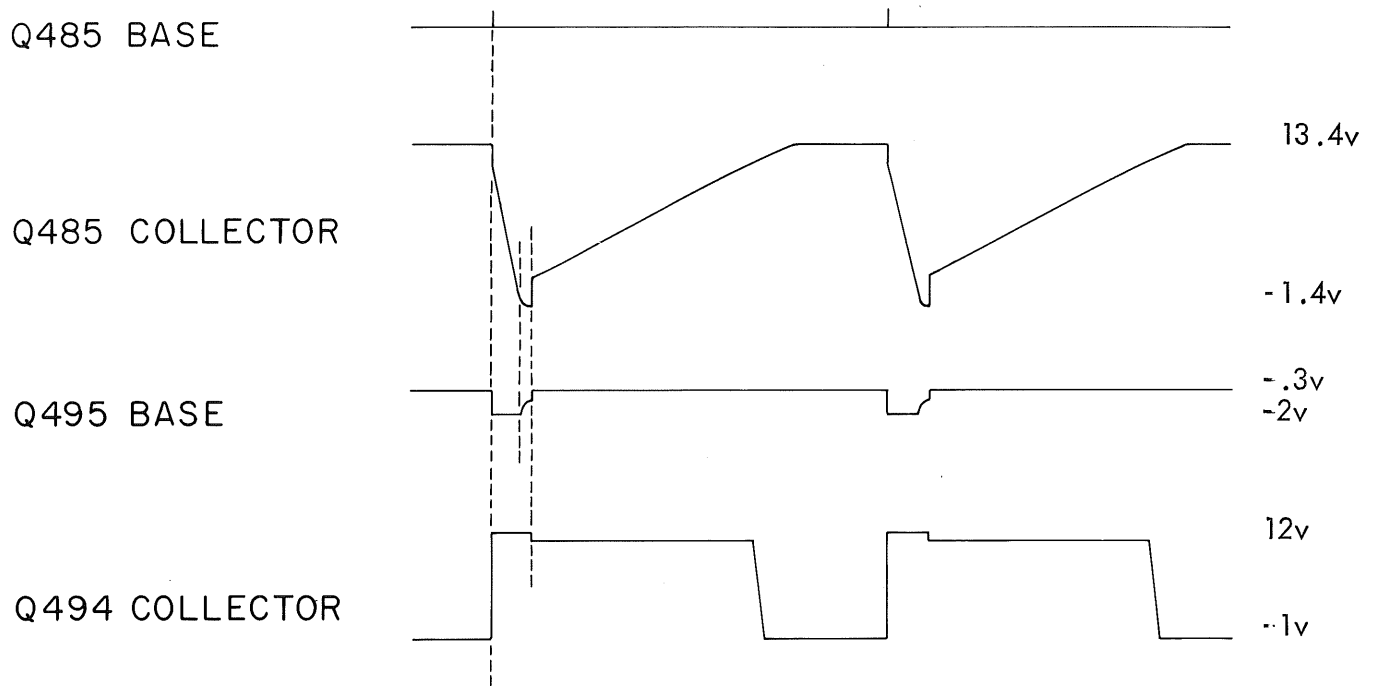
TYPE 453 A TRIGGER GENERATOR
AUTO CIRCUIT

B-453-0029
7-28-65 dl

1. The Auto Multi provides a signal to the Sweep Generator that causes it to free run when no triggers are being applied.
2. The output (TP494) is at about +12v when triggers are being received.
 - a. Triggers must be repetitive (above about 20 cps) to hold the output at 12v.
3. In the absence of triggers (for greater than 85 msec) the output (TP494) drops to -1v.
 - a. In this condition, the Sweep Generator will free run.
4. Q485 and Q495 form a monostable multivibrator.
 - a. Q485 and Q495 are 151-108 silicon NPN transistors.
5. Q484 is a shaper amplifier that provides the positive going trigger pulse for the multi.
 - a. Q484 is a 151-131, 2N964, germanium PNP transistor.
 - b. D484 is a 1N4244 silicon diode.
6. Q494 is an electronic switch that supplies the 12v that constitutes the circuit output.
 - a. Q494 is a 151-087, 2N1131 silicon PNP transistor.
 - b. D486 and D493 are 1N3605 silicon diodes.
7. The signal at Q484 base is a negative going step which occurs as the TD switches to its high state.
 - a. The transistor inverts the step and L484 in the collector differentiates it to a sharp positive going pulse.
 - (1) A negative going pulse from L484 reactive kick is also present.

- b. C482 bypasses Q484 emitter for the pulse duration.
 - c. R482 keeps the circuit from ringing.
 - d. The positive pulse passes through D484 to apply the trigger to Q485 base.
 - (1) The negative excursion of the trigger pulse disconnects the diode.
8. When no triggers are arriving, Q495 is conducting and Q485 is cut off.
- a. R490, R491 places Q495 base at $-.3\text{v}$.
 - b. D484 clamps Q485 base at $-.7\text{v}$.
9. Q495 collector and Q494 emitter are connected rather solidly to the 12v supply -- decoupled by R493, C493.
10. Q485 collector is clamped at 13.4v by D486 and D493 in series.
11. Q494 is cut off.
- a. D493 junction drop reverse biases Q494 base-emitter junction $.7\text{v}$.
 - (1) Q494 emitter sets at $+12\text{v}$.
 - b. Q494 collector rests at -1v .
12. The arrival of a trigger on Q485 base turns on the transistor and switches the multi to its unstable state.
- a. Q485 collector is pulled down abruptly about 2v , dropping Q495 base a like amount.
 - b. The collector then drops exponentially as C485 discharges.
 - c. Q495 base is held at -2v by charging current through C485.
 - d. The multi switches about 7 ma .

13. The initial negative step on Q485 collector disconnects D486 and D493.



TYPE 453 A TRIGGER GENERATOR
 AUTO MULTI WAVEFORMS

B-453-0030

7-29-'65dl

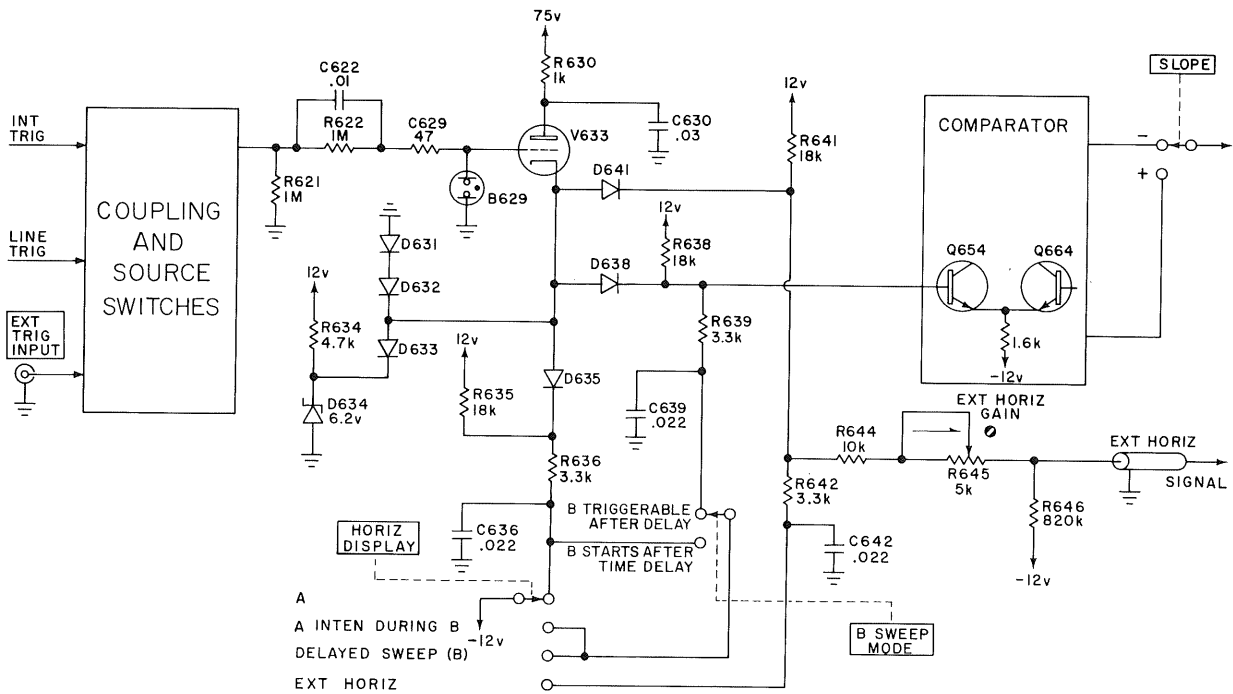
- a. As Q494 base drops toward ground, the transistor saturates at about 12v.
 - b. The collector level at 12v is the circuit output that switches the Sweep Generator to a triggered sweep.
14. When Q485 collector has dropped to -1.4v and C485 has discharged, the transistor saturates.
- a. Q495 base is now free to move toward -0.3v (from -2v) as C485 charges.

- b. When Q495 base reaches about -0.3v , the multi switches to its stable state.
15. As Q485 cuts off, its collector will rise toward 75v as C485 charges.
- a. When the Q485 collector reaches 12.5v , D486 will lift Q494 base to cut off.
 - b. As its collector drops, the Sweep Generator again free runs.
 - c. The collector continues to rise until clamped by D486, D493 at 13.4v .
16. The above discussion assumed the arrival of only one trigger.
- a. Triggers may interrupt the sequence at any time.
 - b. If triggers arrive at greater than a 20 cps rate, Q494 will never turn off and the circuit output will keep the Sweep Generator in its triggered state.

VIII. B TRIGGER GENERATOR

- A. The B Trigger Generator is similar to the A Trigger Generator.
- B. Circuit Differences (from A Trigger Generator):
 - 1. Differences include a gate in the Input CF circuit.
 - a. The Gate is controlled by the HORIZ DISPLAY switch and the B SWEEP MODE switch.
 - b. The Gate controls the destination of the CF output.
 - 2. The B Trigger Generator does not include an AUTO circuit.

C. Input CF and Gate, V633



TYPE 453 B TRIGGER GENERATOR
INPUT C.F.

B-453-0031
8-5-65 dl

1. The Gate circuit has three possible conditions steering the CF output.
 - a. Trigger signal fed to the B Trigger Comparator and Trigger Shaper.
 - b. Trigger signal locked out.
 - c. Trigger signal or EXT HORIZ signal fed to the Horizontal Amplifier.

2. The HORIZ DISPLAY switch has primary control of the gate.
 - a. A -- the Trigger input is locked out.
 - b. A INTEN DURING B -- Trigger is fed to the B Trigger Generator, providing the B SWEEP MODE switch is in its B TRIGGERABLE AFTER DELAY position.
 - (1) In the B STARTS AFTER TIME DELAY position of the B SWEEP MODE switch, the trigger is locked out.
 - c. DELAYED SWEEP (B) -- same as A INTEN DURING B mode.
 - d. EXT HORIZ -- any signal fed into the Trigger Preamp will be fed to the Horizontal Amplifier.

3. Operation in the "A" mode of the HORIZ DISPLAY switch.
 - a. V633 cathode is returned through D635, R636, and the HORIZ DISPLAY switch to -12v.
 - (1) R635 and R636 form an equivalent 2.8k to -8.3v.
 - b. D641 is cut off.
 - (1) The anode (and V633 cathode) will set at about 1.5v.
 - (2) The cathode is pulled up to $\approx 12v$.

- c. D638 is cut off.
 - (1) The cathode is pulled up to about 5v by Q654 base-emitter junction (Q654 beta will determine the level).
 - d. Q654 draws about 10 ma I_C , pulling its emitter up to +4v.
 - e. If the SLOPE switch is in + SLOPE, Q654 collector current flowing through the Trigger Shaper TD will switch it to its high state where it will remain.
 - f. If the SLOPE switch is in - SLOPE, Q654 emitter will lift Q664 emitter cutting off the transistor.
 - (1) In this case, the TD will remain in its low state.
 - g. Since D638 is cut off and the TD cannot switch, triggers are not formed.
 - h. D631, D632 and D633 are protection diodes for the Comparator*.
4. Operation in the A INTEN DURING B and DELAYED SWEEP (B) positions of the HORIZ DISPLAY switch.
- a. If the B SWEEP MODE switch is in B STARTS AFTER TIME DELAY position operation is the same as in A mode -- triggers are locked out.
 - b. With the B SWEEP MODE switch in B TRIGGERABLE AFTER DELAY position, triggers are fed to the Comparator.
 - c. D635 is cut off.
 - (1) The cathode is pulled up to 12v (through R635) as the -12v return is opened.

* See Page 7-10.

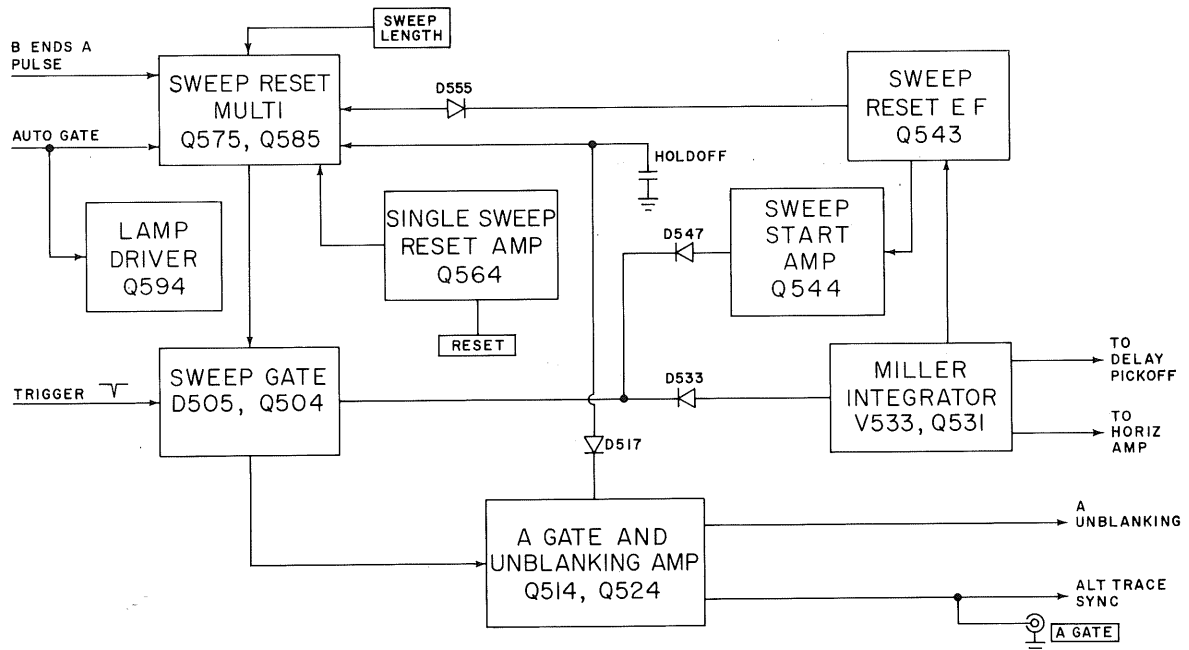
- d. D641 is cut off.
 - (1) The cathode is pulled up to $\approx 12\text{v}$.
 - e. Current for R638 is now supplied through R639 from -12v .
 - f. D638 cathode is pulled down, forward biasing the diode.
 - g. V633 cathode current is supplied through D638 and R639.
 - h. The Comparator can function in the normal manner -- triggers are generated.
5. Operation in EXT HORIZ mode of the HORIZ DISPLAY switch:
- a. With their current supply opened, D635 and D638 are cut off.
 - (1) Trigger signals cannot pass D638.
 - b. D641 is forward biased.
 - c. Any signal supplied to the Input CF is fed through D641 to the Horizontal Amplifier.
 - d. The external horizontal signal may be obtained either from the EXT HORIZ jack (SOURCE switch in EXT or EXT $\div 10$) or from the CH 1 Input Amplifier when the TRIGGER switch is in CH 1 ONLY position and the SOURCE switch is in INT*.
 - e. Gain of the External Horizontal circuit is set by R645.
 - (1) A signal applied to Channel 1 INPUT will produce the indicated horizontal deflection.

IX. A SWEEP GENERATOR

A. The A Sweep Generator supplies a linear sweep ramp to the Horizontal Amplifier.

1. The generator will run in all positions of the HORIZONTAL DISPLAY switch.

B. Block Diagram



TYPE 453 A SWEEP GENERATOR
BLOCK DIAGRAM

B-453-0032
8-17-'65dl

C. Circuits that Comprise the A Sweep Generator:

1. Sweep Gate; D505, Q504.
2. Miller Integrator; V533, Q531.
3. A Gate and Unblanking Amplifier; Q514, Q524.
4. Sweep Reset EF, Q453.

5. Sweep Start Amplifier, Q544.
6. Sweep Reset Multi; Q575, Q585.
7. Single Sweep Reset Amplifier, Q564.
8. Ready Light Driver, Q594.

D. Three Sweep modes are available:

1. AUTO -- The sweep free runs when triggers are absent and becomes a triggered sweep when triggers are present.
2. NORM -- Triggers start the sweep.
3. SINGLE SWEEP -- One sweep ramp will be generated with the first trigger after manual RESET.

E. Outputs

1. The A Sweep waveform to the Delay Pick-Off circuit.
 - a. A negative going $\approx 10\text{v}$ voltage ramp -- from $\approx 12\text{v}$ to $\approx 2\text{v}$.
2. The A Sweep waveform to the Horizontal Amplifier.
 - a. A negative going 2 ma current ramp.
3. The A GATE out waveform.
 - a. A positive going 12v square wave -- from $\approx 0\text{v}$ to $\approx 12\text{v}$.
4. The Unblanking pulse to the CRT via the Z axis amplifier.
 - a. A negative going 2 ma current pulse.
5. The Alt Sync Pulse to the Vertical Switching circuit.
 - a. A 3v positive going square wave.
 - b. The trailing edge -- at the end of sweep -- is used.

F. Inputs

1. Negative going current trigger from the A Trigger Generator.
 - a. 3 ma to 8 ma pulse, 3 to 5 nsec wide.

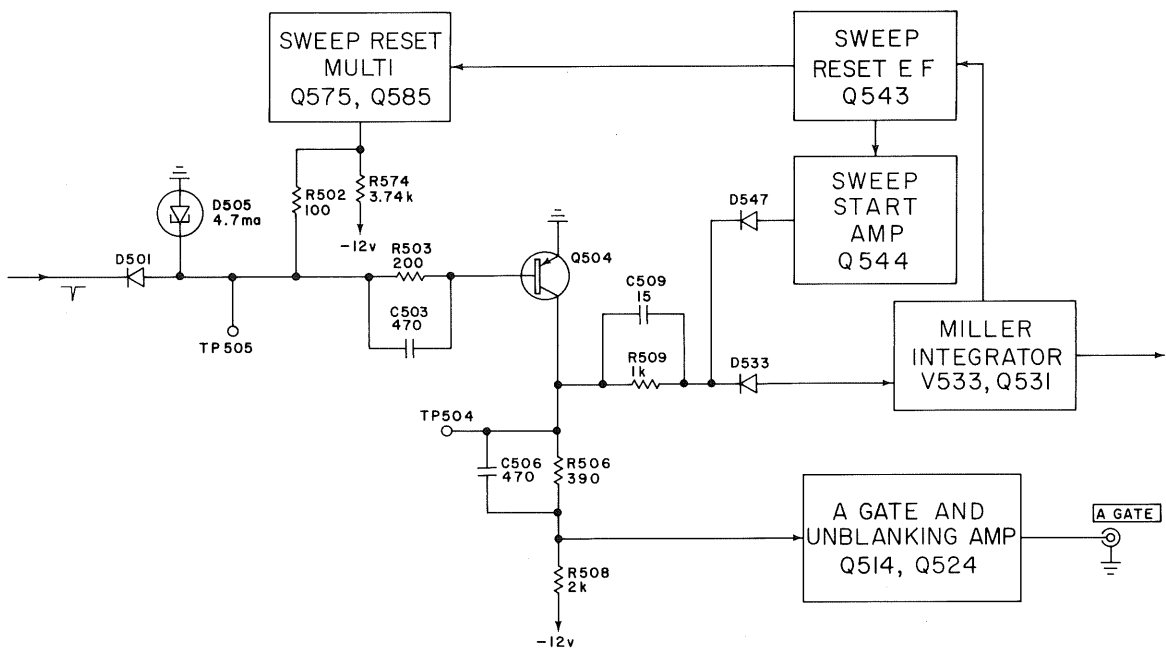
2. Auto enabling signal from the A Sweep Generator.
 - a. When triggers are present the enabling voltage is 12v -- the Sweep Generator becomes a triggered sweep.
 - b. When no triggers are arriving the voltage is -1v -- the sweep will free run.
3. A "B ENDS A" pulse from the B Sweep Generator.
 - a. At the end of B Sweep a negative going 12v pulse terminates A Sweep.
 - b. The SWEEP LENGTH control must be in its B ENDS A detent for the pulse to appear.

G. Block Logic

1. A negative going trigger from the A Trigger Generator switches the Sweep Gating TD into its high state.
2. The output from the Sweep Gating circuit is a positive going 4.4v step.
3. The step cuts off the disconnect diode, starting sweep.
4. The Miller Integrator output is a negative going ramp about 10v peak-to-peak.
 - a. The sweep ramp is fed to the Horizontal Amplifier.
5. The Sweep ramp is fed back through the Sweep Reset EF to the Sweep Reset Multi.
6. When the ramp has reached its full amplitude, the Sweep Reset Multi switches.
7. The Sweep Reset Multi reverses the current in the TD and it switches to its low state.
 - a. In this condition triggers cannot alter its state.

8. The negative step at the Sweep Gate output turns on the disconnect diode (D533) stopping sweep -- retrace begins.
 9. A gate, the same duration as the sweep, is amplified in the A Gate and Unblanking Amplifier.
 - a. The gate is fed to the Z Axis Amplifier for CRT unblanking, to the Vertical Switching circuit for dual trace switching, and to the A Gate jack.
 10. At the start of retrace, D555 disconnects.
 - a. At the end of retrace, D547 connects as the Sweep Start Amplifier sets the starting point for each sweep.
 11. A positive going step from the A Gate Amplifier disconnects D517, starting hold-off.
 12. At the end of hold-off, the Sweep Reset Multi switches, resetting the Sweep Gating TD.
 13. Arrival of a trigger will start a new sweep.
- H. Sweep Gate; D505, Q504
1. The Sweep Gate circuit gates the Miller Integrator on to start sweep and off to stop sweep.
 - a. The circuit also drives the A Gate and Unblanking Amplifier.
 2. The circuit uses one transistor and a tunnel diode.
 - a. D505 is a 152-125, TD3A, 4.7 ma tunnel diode.
 - b. Q504 is a 151-131, 2N964 germanium PNP transistor.

3. In the quiescent condition, the TD is in its low state with about 3.1 ma forward current .

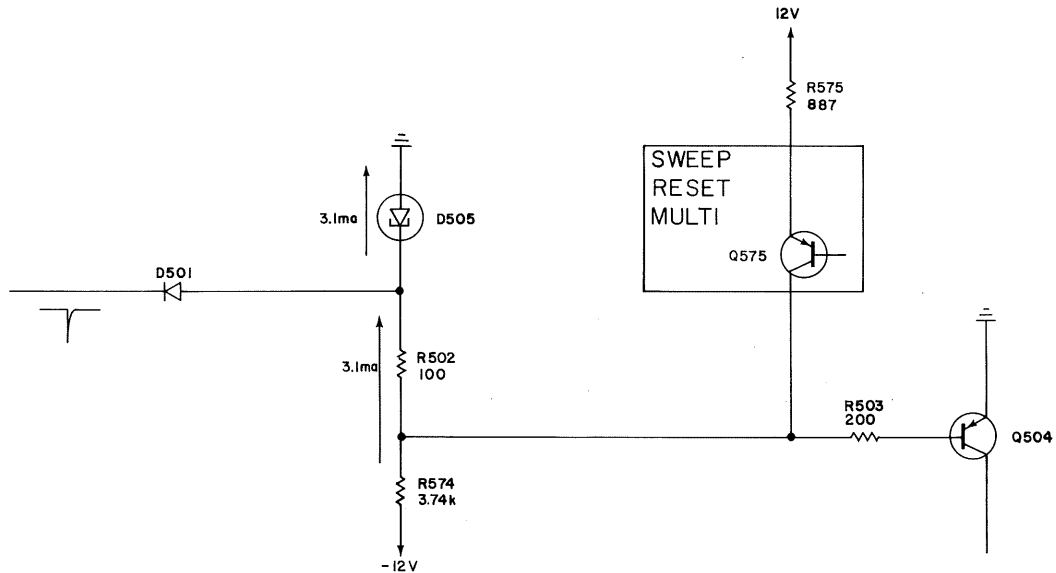


TYPE 453 A SWEEP GENERATOR
SWEEP GATE

B-453-0033
8-17-'65dl

- a. Q504 is cut off.
b. D501 is conducting a few microamps.

4. Current distribution in the quiescent state -- prior to sweep.



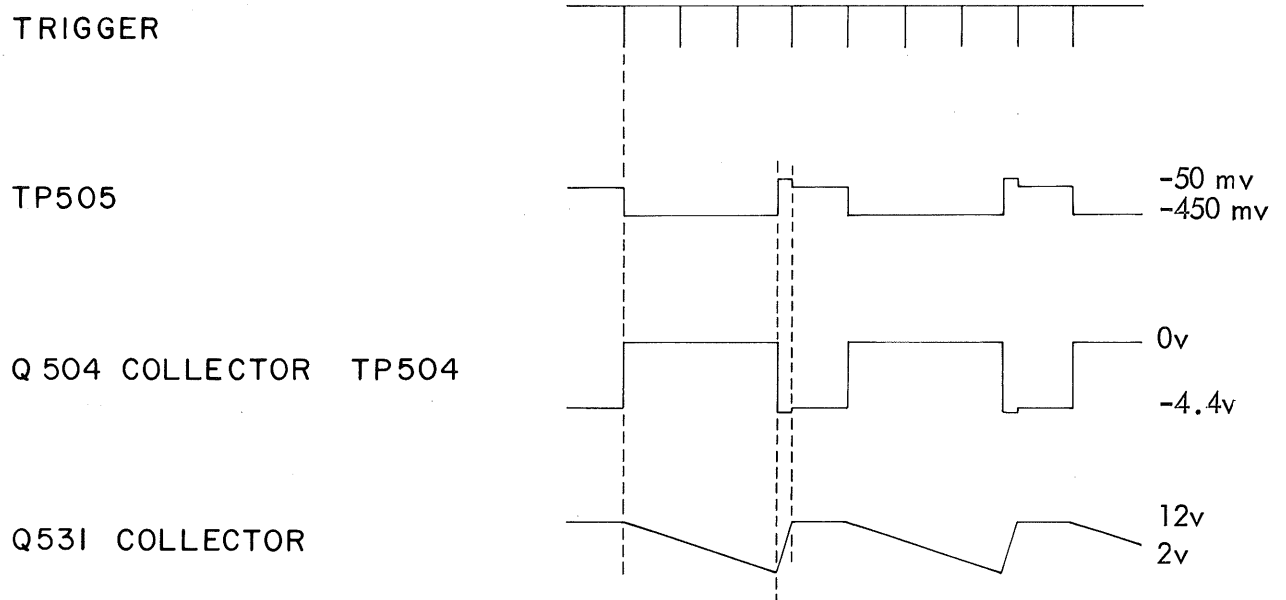
TYPE 453 A SWEEP GENERATOR
TD CURRENTS

B-453-0034

8-14-65 ba/jg

- Q575 in the Sweep Reset Multi is cut off.
- About 3.1 ma flows through R574, R502 and D505 to place the TD in its ready state, awaiting a trigger.
- The TD requires an additional 1.6 ma to switch it to its high state.

5. Sequence of operation at the start of sweep.



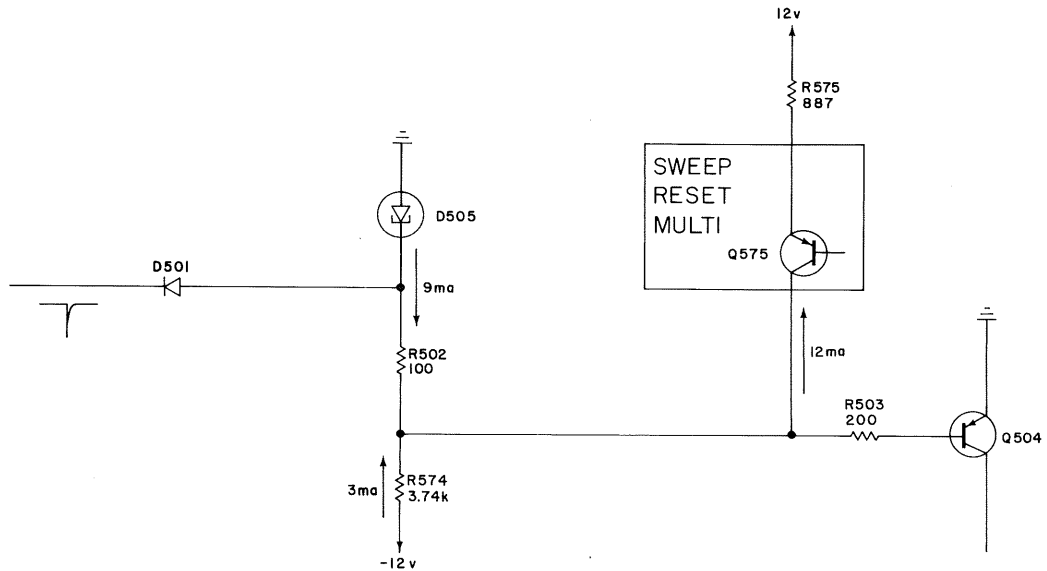
TYPE 453 A SWEEP GENERATOR
WAVEFORMS NO. I

B-453-0035

8-24-65jg

- a. A negative going current trigger is passed through D501.
 - (1) The current pulse adds 5 to 8 ma to the TD bias for 3 to 5 nsec.
- b. The TD (D505) switches to its high state.
 - (1) D505 cathode drops to -450 mv.
- c. D501 cuts off, disconnecting the Trigger Generator output.
- d. Q504 saturates as its base is pulled down to -350 mv.
 - (1) The collector raises to 0v.
 - (2) The saturated transistor draws about 5 ma base current from R574, R502.

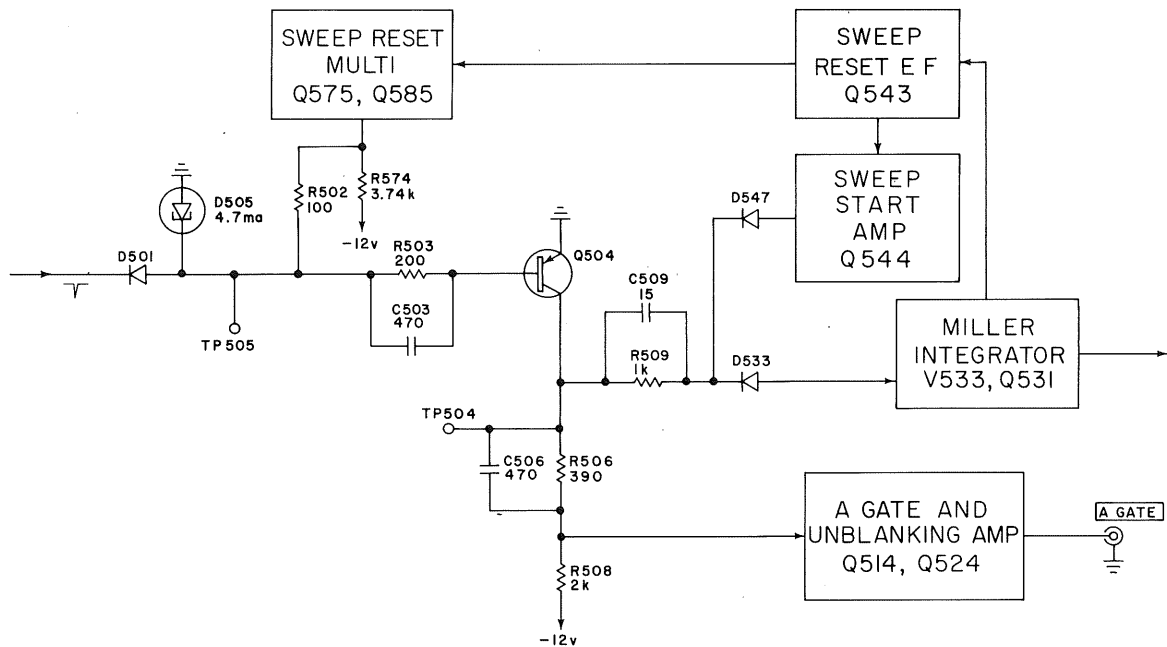
- (3) R503 limits the current and keeps Q504 from turning off the TD.
- e. The disconnect diode turns off and sweep starts.
- 6. When the sweep reaches its maximum, the Sweep Reset Multi switches.
 - a. As Q575 (Reset Multi) conducts, 12 ma is pulled from the TD circuit.
 - b. D505 conducts reverse current, switching it to its low state.
- 7. Current distribution with D505 in its low state -- during hold-off.



TYPE 453 A SWEEP GENERATOR
TD CURRENTS

B-453-0034.1
8-14-65.jg

- a. Q575 draws 12 ma.
- b. 3 ma flows through R574.
- c. The balance of the current, 9 ma, flows (reverse) in D505.
- d. D505 cathode rises to +50 mv.



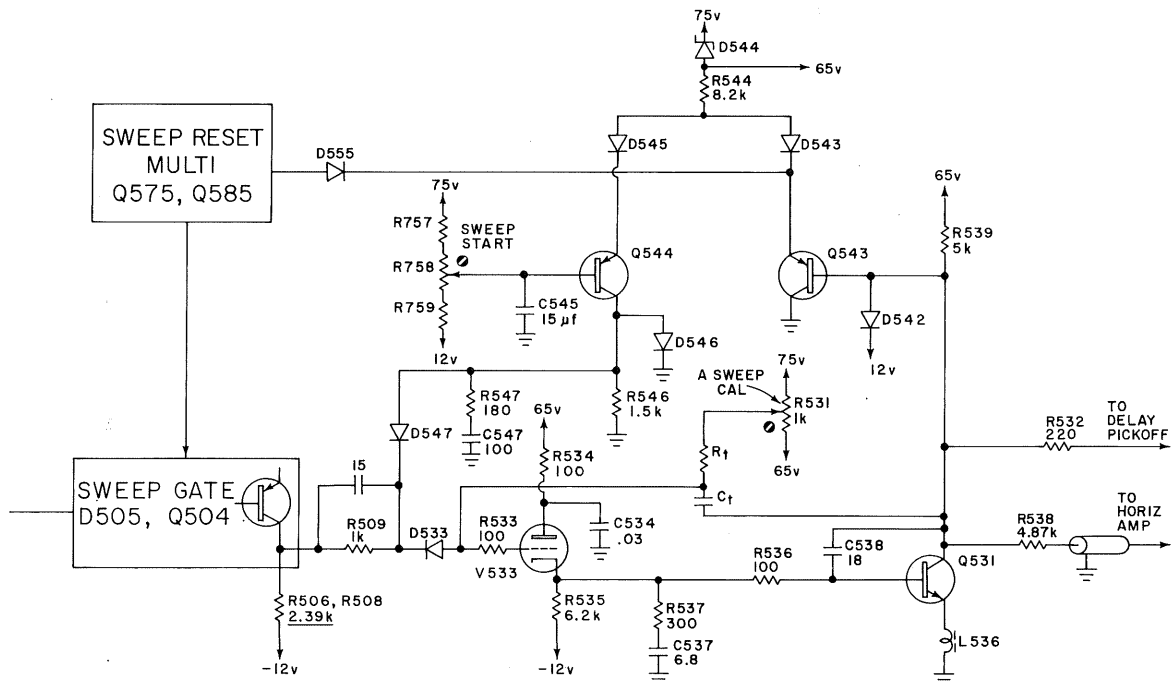
TYPE 453 A SWEEP GENERATOR
SWEEP GATE

B-453-0033
8-17-'65dl

8. Sequence of operation at the end of sweep.
 - a. Q504 base swings positive and the transistor cuts off.

- b. The collector drops to -4.4v .
 - c. D533 connects, stopping sweep and starting retrace.
 - d. The positive step out of the Gate Amplifier starts hold-off.
 9. At the end of hold-off, the Sweep Reset multi again switches.
 - a. Q575 cuts off.
 - b. D505 becomes forward biased about 3.1 ma .
 - c. The circuit is in its ready state awaiting the next trigger.
 10. R509 is part of the divider between the Sweep Start Amplifier and -12v that sets the start of sweep and the Gate Amplifier bias.
 - a. C509 couples fast Sweep Gates across R509.
- I. Miller Integrator; V533, Q531
Sweep Reset EF, Q543
Sweep Start Amplifier, Q544
 1. The Miller Integrator supplies a negative going linear ramp to the Horizontal Amplifier.
 - a. 10v peak-to-peak.
 - b. From 12v to 2v at Q531 collector.
 2. The circuit is a Miller "run-down" instead of the familiar Miller run-up circuit.
 - a. A run-down circuit was used because a regulated positive supply was available for charging the timing caps, but no regulated negative supply of sufficient voltage.

3. The circuits use a nuvistor, three transistors and six diodes.



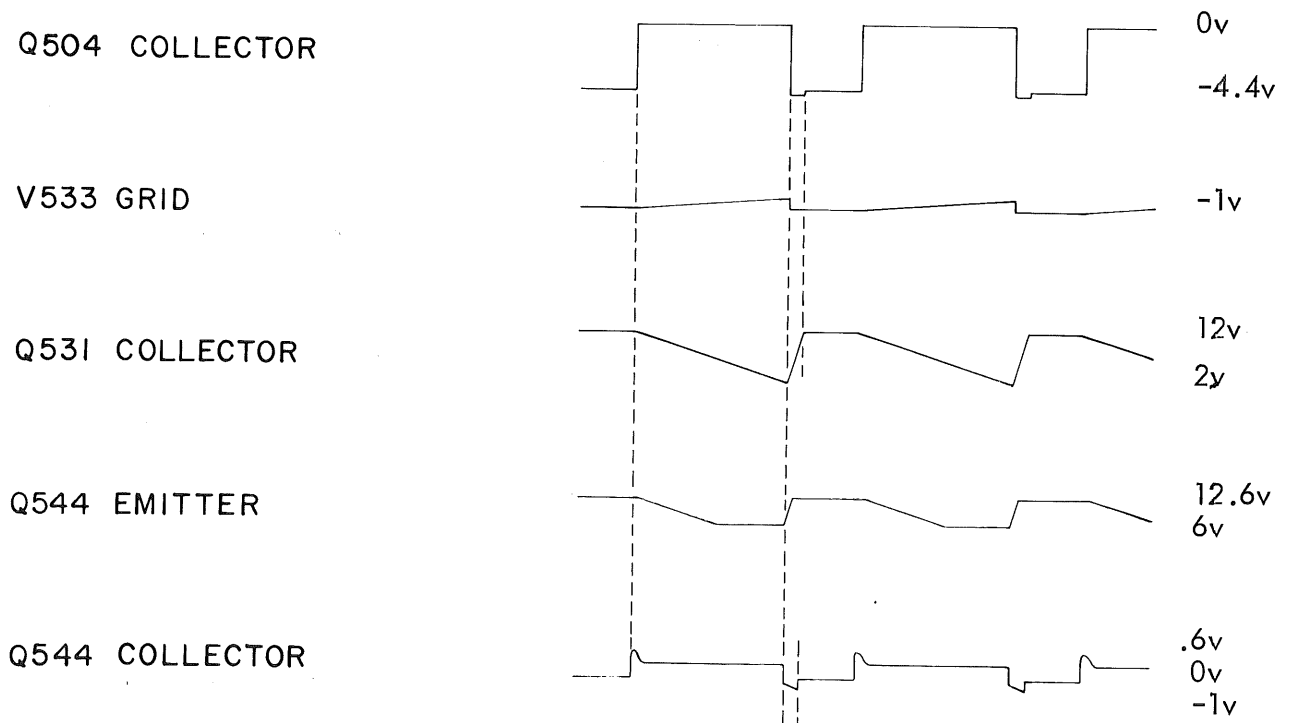
TYPE 453 A SWEEP GENERATOR
MILLER INTEGRATOR

B-453-0036
8-19-'65 dl Ⓢ

- a. V533 is a 8393 RCA nuvistor.
 - (1) The nuvistor has a 13v heater but runs on 12v.
- b. Q531 is a 151-127, silicon NPN transistor.
- c. Q543 and Q544 are 151-133 silicon PNP transistors.
- d. D542, D546 and D547 are silicon diodes replaceable by 1N3605.
- e. D533 is a 152-173 silicon diode selected for fast switching and low leakage.

4. Sweep linearity design spec is $\pm 1.5\%$.
 - a. Low leakage currents (typically below 20 na) contribute to the linearity spec.
 - b. Nuvistor input, selected disconnect diodes, and low leakage Tek-made timing capacitors all help keep leakage low.
5. The nuvistor (V533) provides the low leakage currents and the transistor (Q531) provides the gain.
 - a. The nuvistor is used as a cathode follower.
 - b. The plate supply is decoupled by R534, C534 from 65v.
 - (1) The 65v is offset from the 75v supply by the 10v zener, D544.
 - c. Bias is nominally 1.7v.
 - d. I_p is about 2 ma.
 - e. Gain of the circuit is about 140.
6. The Sweep starting point is set by the Sweep Start amplifier.
 - a. A feedback loop is formed of Q543, D543, D545, Q544, D547, D533, V533 and Q531.
 - b. The SWEEP START adj, a screwdriver adjustment (on the B Sweep board) sets the bias on Q544.
 - (1) The same control is used for B Sweep start, thereby providing accurate delay pickoff.
 - c. The current path that establishes the sweep starting point consists of R508, R506, R509, D547, Q544, D545, R544, D544 to 75v.

- d. 3.2 ma flows through the network.
 - e. Q544 collector sets at ground so no current flows through R546.
 - f. Up to 700 μ a will flow through D533 and the timing resistors.
 - g. With the level at Q544 collector established, the feedback loop sets the ramp start (at Q531 collector) quite accurately.
7. Quiescently, V533 grid sets at about -1v.
- a. Q531 collector sets at 12v.
 - b. About 8 ma flows through the transistor, increasing to 13 ma at the end of sweep.
8. Sequence of events as sweep starts.



TYPE 453 A SWEEP GENERATOR
WAVEFORMS NO. 2

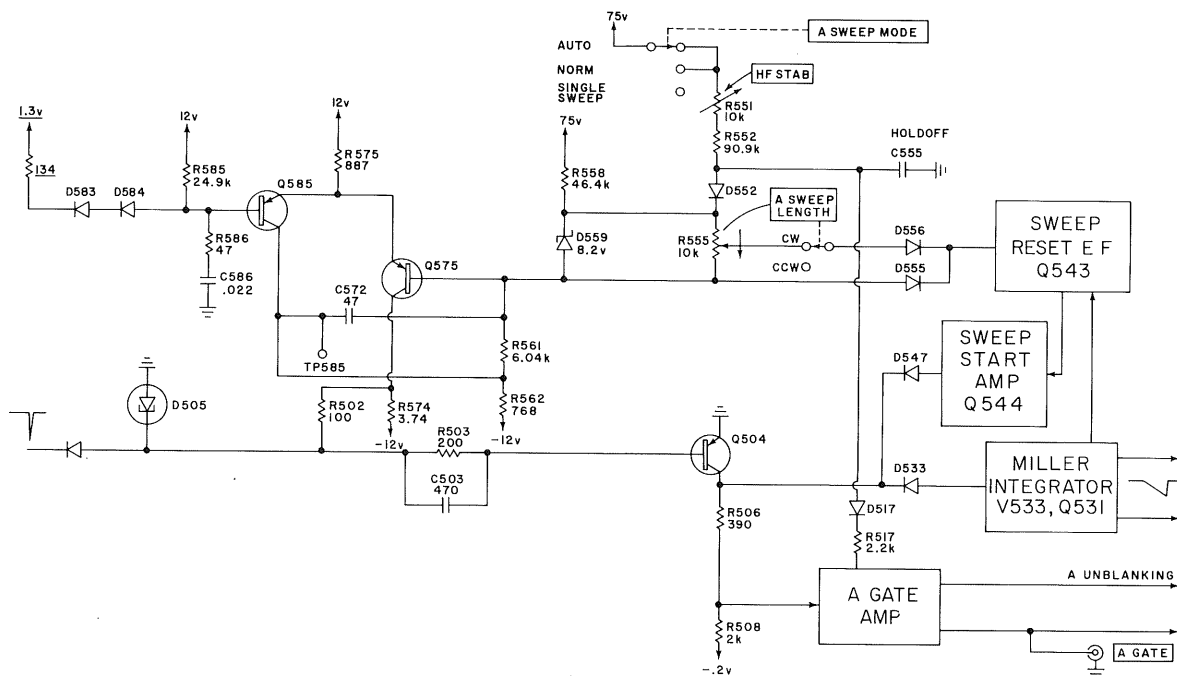
B-453-0037

8-25-65jg

- a. When a trigger arrives, the Sweep Gate output rises to 0v (from -4.4v).
 - b. D533 and D547 disconnect.
 - c. V533 grid rises toward 70v (center of Sweep Cal).
 - d. V533 cathode follows, lifting Q531 base.
 - e. The change on V533 grid is inverted and amplified in Q531.
 - f. The collector begins to run down, driving the Horizontal Amplifier, the Timing Capacitor and the Sweep Reset EF.
 - g. The negative going ramp is fed back through the timing cap to V533 grid.
 - (1) V533 grid change is opposed.
 - (2) The grid change on V533 grid is about 70 mv.
 - (3) The grid change depends on system gain.
 - h. Since the voltage drop across the timing resistor remains virtually constant, the current through the timing resistor will be virtually constant.
 - i. A constant current into a capacitor will result in a linear voltage ramp across it.
 - j. A linear ramp to the $\pm 1.5\%$ spec is assured.
 - k. Time of sweep run-down is controlled by settings of the TIME/DIV switch.
9. As the ramp runs down Q543 emitter follows.
- a. Q544 cuts off.
 - b. D545 disconnects, protecting the EB junction of Q544.
 - c. D543 temperature compensates D545.
 - d. Q543 emitter drives the Sweep Reset Multi.

10. When the Sweep ramp has reached 2v, the Reset Multi switches and the Sweep Gate output drops to -4.4v.
 - a. D533 conducts, dropping V533 grid about 70 mv.
 - b. Q531 collector rises as retrace begins.
 - c. The timing cap discharges.
 - (1) Discharge path is through R508, R506, R509, D533, C530 (the timing cap), R539 to 65v.
 - (2) Current into the charging cap is a fairly constant 3.5 ma.
 - (3) Retrace, therefore, is a linear ramp.
 - (4) The Miller feedback loop remains connected.
 - d. When the ramp has risen to about 6v, D545 conducts.
 - e. As the retrace ramp continues to rise, Q544 turns on, establishing the starting point for a new sweep.
 - (1) The Sweep Start loop is again connected.
11. D542 protects Q543 during warm-up when V533 cathode is at -12v and Q531 is cut off.
 - a. It also offers protection if V533 opens or is pulled out of its socket.
 - b. The diode limits Q531 collector and Q543 base rise to 12.7v, preventing breakdown.
12. D546 limits Q544 collector positive excursion to .6v.
 - a. When D547 cuts off (at the start of weep), Q544 collector would (without D546) rise about 5v.
 - b. D547 would reconnect.
 - c. D546 limits the rise to .6v assuring D547 remains cut off for the duration of sweep.

13. Several components were empirically added to suppress oscillation at various sweep speeds.
 - a. R537, C537 at V533 cathode.
 - b. Feedback cap, C538 from Q531 collector to base.
 - c. L536, a ferrite bead in the Q531 emitter ground lead.
 - d. C530H, C530K, C530J and C740H on the Timing Switch.
 14. R547, C547 suppress a ringing at the end of retrace.
- J. Sweep Reset Multi; Q575, Q585
1. The Sweep Reset Multi is a bistable multi that locks out -- then resets the Sweep Gating TD.
 - a. Prior to Sweep, the Multi draws no current from the TD circuit, allowing the Sweep Gate to reset.
 - b. At the end of sweep -- during hold-off -- 12 ma is drawn from the Sweep Gating Circuit locking it out.
 - c. At the end of hold-off the multi again switches to its reset position -- it allows the Sweep Gate to accept a trigger.
 2. The circuit uses two transistors, five signal diodes and a zener diode.
 - a. Q575 and Q585 are 151-133 silicon PNP transistors.
 - b. The diodes are all 6185 silicon diodes.
 - c. D559 is a 8.2v, 5% zener diode.
 3. Prior to Sweep, Q575 is cut off and Q585 is conducting -- reset or ready condition.
 - a. The common emitters set at 3v.

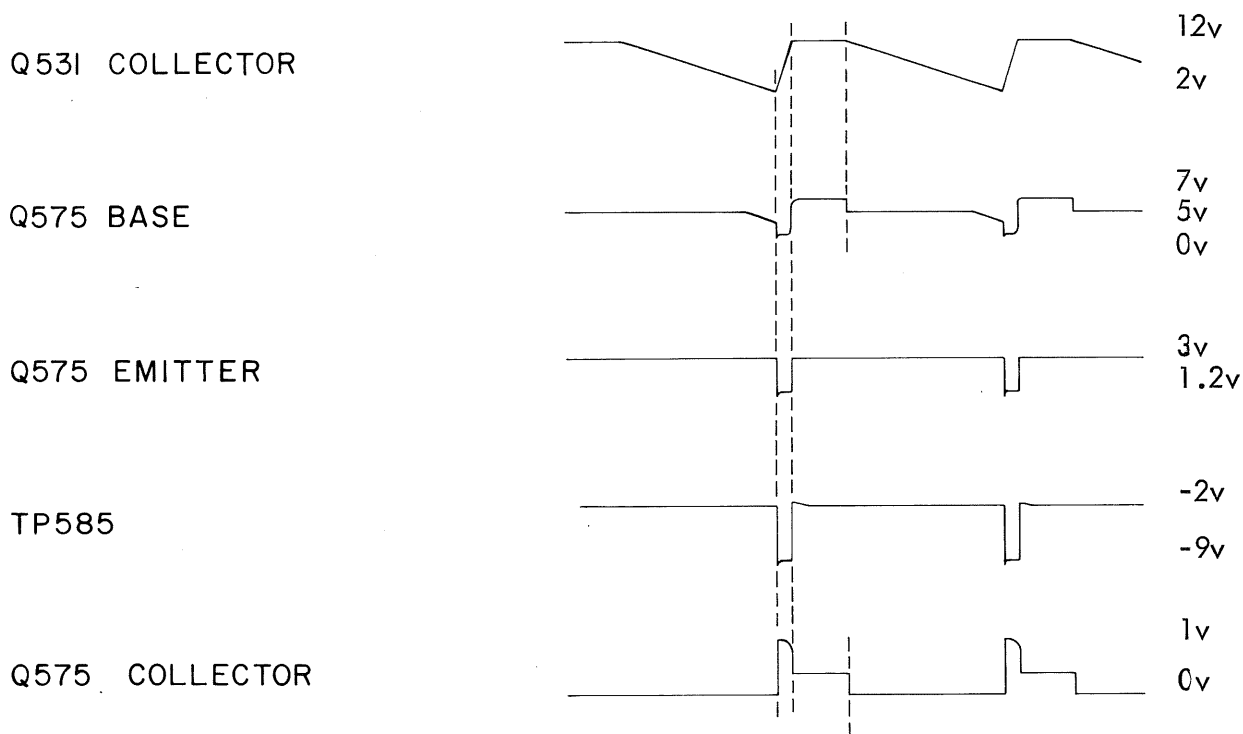


TYPE 453 A SWEEP GENERATOR
RESET MULTIVIBRATOR

B-453-0038
8-24-'65dl

- b. Q585 base is set at 2.3v.
 - c. Q585 collector, -2v.
 - d. Q575 base, 7v.
 - e. Q575 collector, 0v.
 - f. 3.1 ma through R574 flows through the TD.
 - g. D555 and D556 are cut off with their cathodes at 13v.
- (1) D556 will conduct if the SWEEP LENGTH control is CCW (but not in the detent).

4. As a trigger arrives and the Sweep Gating TD switches to its high state, the Reset Multi is not affected.



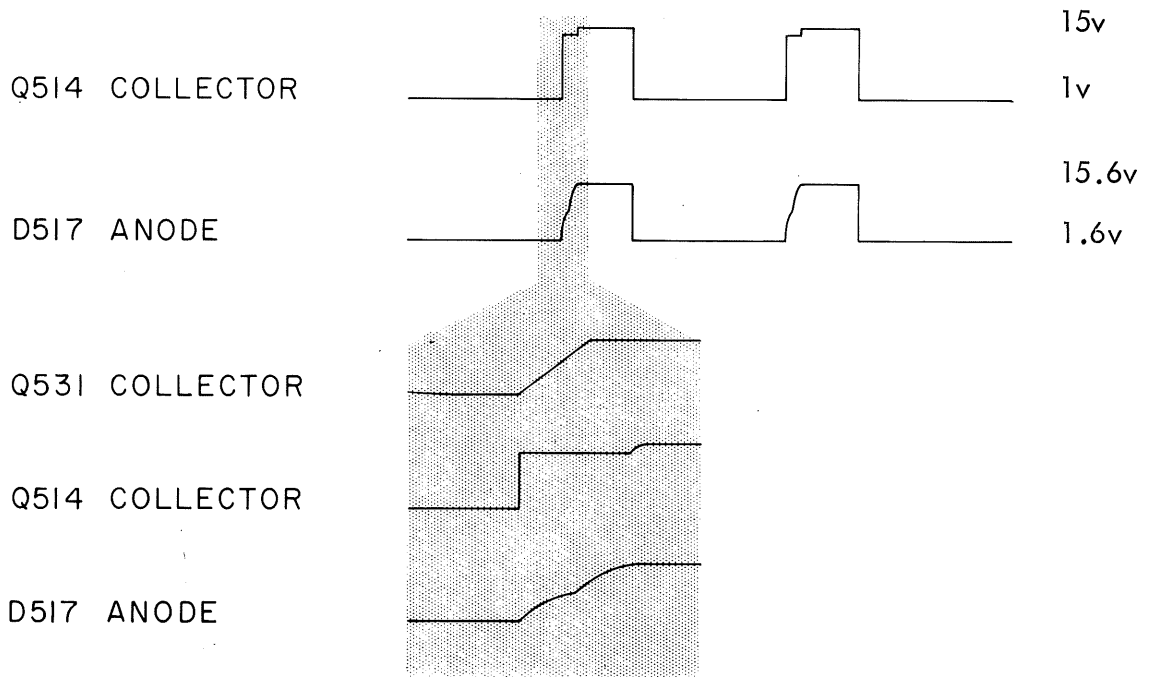
TYPE 453 A SWEEP GENERATOR
WAVEFORMS NO. 3

B-453-0039

8-25-65jg

- a. Q575 collector is pulled down to -450 mv as D505 cathode drops.
 - b. Q575 base drops to 5v (from 7v) as a negative step from the A Gate Amplifier discharges the hold-off cap, C555.
 - (1) The Multi does not switch.
 - (2) If D556 is conducting (see previous page) it now turns off.
5. The sweep waveform from the Sweep Reset EF brings D556 and/or D555 into conduction when their cathodes reach 5v.

- a. As the diodes conduct, Q575 base follows the sweep ramp until at about 2.6v, Q575 conducts.
 - b. The multi switches, turning off Q585.
 - c. Q575 collector pulls up to 1v as it draws 12 ma.
 - (1) 3 ma flows through R574.
 - (2) 9 ma of reverse current flows in the TD.
 - d. The TD switches to its low state, stopping sweep.
 - e. The circuit is now in its locked out condition.
6. As retrace starts, D555 and D556 cut off.



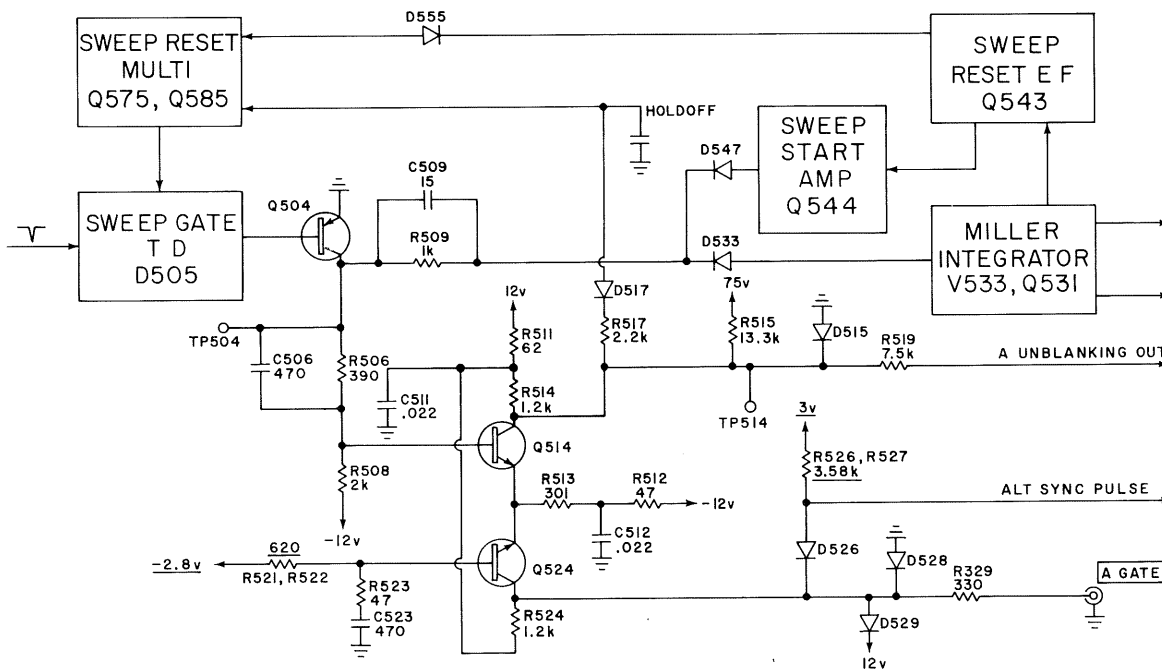
TYPE 453 A SWEEP GENERATOR
 WAVEFORMS NO. 4

B-453-0040
 8-20-'65dl

- a. The positive going 14v step at the A Gate output raises D517 cathode to 15v (from 1v) cutting it off.
 - b. The hold-off cap begins to charge toward 75v.
 - c. Q575 base follows the hold-off charging curve.
 - d. When Q575 base reaches 2.6v, the transistor turns off and the multi flips.
 - e. Q575 base jumps to about 5v as the multi switches, then as the charging hold-off cap catches up with the base potential, it rises exponentially to 7v.
 - f. D517 conducts, clamping the hold-off cap at 15.6v.
7. At the end of hold-off, when the Reset Multi switches, all circuits return to the reset condition awaiting a new trigger.
- a. Six sets of hold-off caps are used.
 - (1) .1 μ sec/div to 5 μ sec/div hold-off is about 2.5 μ sec.
 - (2) 10 μ sec/div to 50 μ sec/div hold-off is about 8 μ sec.
 - (3) .1 msec/div to .5 msec/div hold-off is about 65 μ sec.
 - (4) 1 msec/div to 5 msec/div hold-off is about 650 μ sec.
 - (5) 10 msec/div to 50 msec/div hold-off is about 7 msec.
 - (6) .1 sec/div to 5 sec/div hold-off is about 70 msec.
8. Sweep length may be controlled by the rotation of the SWEEP LENGTH control.
- a. When rotated CCW (but not to the detent switch) the sweep is shortened to about 4 divisions.
 - b. The control is in shunt with D559, an 8.2v zener diode.
 - c. The control arm, therefore, can be placed at any point between the 5v base potential of Q575 and 13.2v.

- d. If rotation of the control arm has placed the anode of D556 at a potential above 5v, the sweep ramp will not have to advance as far before D556 conducts.
 - e. When D556 conducts, the sweep ramp will drop Q575 base to switch the Reset Multi and stop the sweep.
 - f. In the full CCW position, a switch opens to disconnect D556.
 - g. With only D555 in the circuit, the sweep length assumes its maximum length of 11 div \pm .5 div.
9. The HF STABILITY permits the operator to vary hold-off time about 10%.
- a. At high triggering frequencies (above 10 mc or so), triggering may become erratic (jitter horizontally).
 - b. By varying hold-off time, the coincidence of the Sweep Gate becoming triggerable (reset) relative to the arrival of triggers can be adjusted to eliminate jitter.
10. D583, D584 temperature compensated D555 and Q543 base-emitter junction.
- a. Q585 base-emitter junction temperature compensates Q575 base-emitter junction.
11. C586 bypasses Q585 base.
- a. R586 prevents ringing with lead inductance at Q585 base.
- K. A Gate and Unblinking Amplifier; Q514, Q524
- 1. The A Gate and Unblinking Amplifier has three outputs.
 - a. A Gate: A positive going 13v gate (from $-0.7v$ to $12.7v$); the same duration as A Sweep.
 - (1) The waveform appears at a BNC connector on the side panel.

- b. A Unblanking: A 2 ma negative going current pulse; the same duration as A Sweep.
 - (1) Fed to the Z axis amplifier.
- c. Alt Trace Sync Pulse: A 3v positive going waveform; the same duration as A Sweep.
 - (1) The trailing edge is used -- the negative step -- to trigger the Vertical Switching Multi.



TYPE 453 A SWEEP GENERATOR
A GATE AND UNBLANKING AMP

B-453-0041
8-25-'65 dl

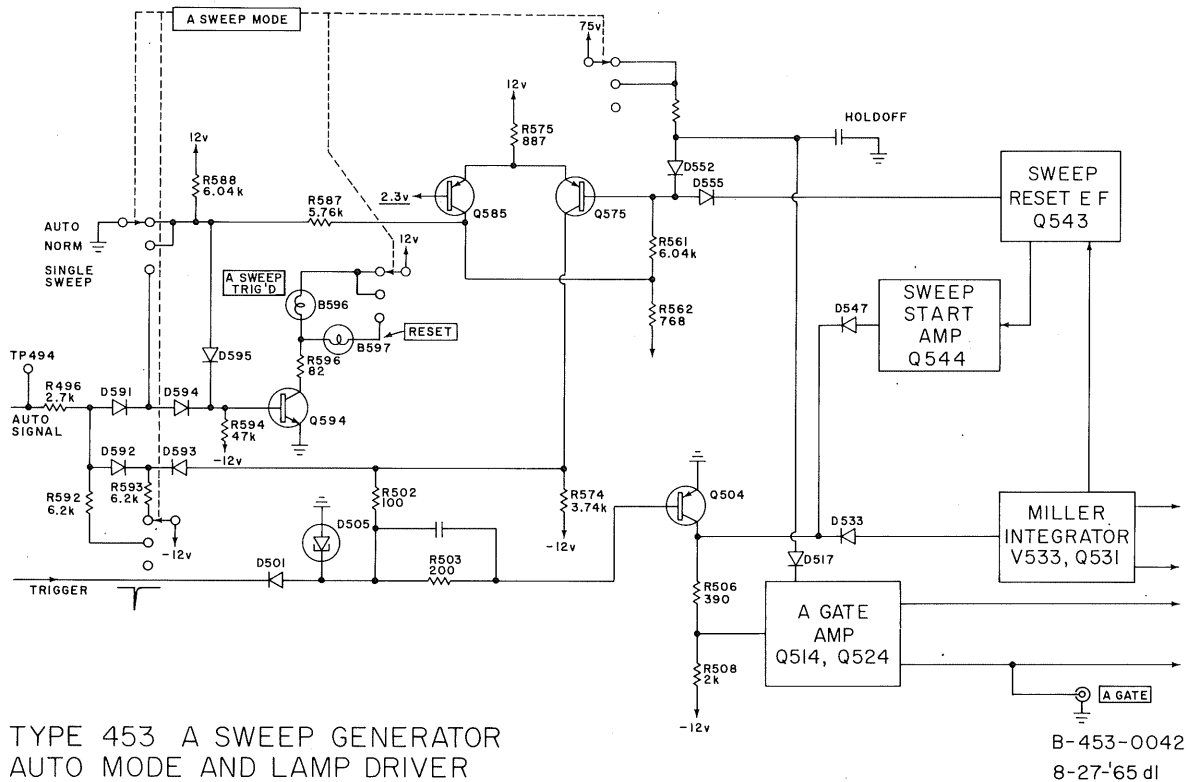
2. The circuit is an emitter coupled paraphase inverter.
 - a. Q514 and Q524 are 151-108 silicon NPN transistors.
 - b. The diodes are 6185 silicon signal diodes.
3. The waveform at Q504 collector (TP504) is a positive going rectangular waveform from -4.4v quiescently to 0v during sweep.
 - a. Applied to the base of Q514, the voltage steps from -6v to -2v.
 - b. C506 is a speed-up cap to supply charging current for Q514 input C.
4. The collector supply is decoupled by R511, C511 from the 12v supply.
 - a. The emitter supply is decoupled by R512, C512 from the -12v supply.
5. R521, R522 set Q524 base level at -2.8v.
 - a. C523 provides an AC ground for the grounded base transistor.
 - b. R523 prevents ringing by breaking up inductance at the base of Q524.
6. Q514 collector swings from -.7v (during sweep where it is limited by D515) to 15v.
 - a. The output drives through R519 to the low impedance Z axis amplifier input.
 - b. Practically the entire 15v voltage waveform appears across R519, generating the 2 ma current drive to the Z axis amplifier.

7. Q524 collector swing is limited by D529 to 12.7v (during sweep) and by D528 at $-0.7v$.
 - a. This voltage swing constitutes the A GATE.
8. A divider composed of R526 and R527 forms an equivalent $3.58k$ to $3v$.
 - a. The divider limits the Alt Trace Sync voltage positive excursion to $3v$.
 - b. D526 disconnects, allowing the A GATE to rise to $12.7v$.

L. Auto Trigger Mode of Operation

1. In the absence of triggers, the sweep circuit free runs at a rate set by the TIME/DIV switch.
 - a. When triggers arrive (above 20 cps), the A Sweep Generator becomes a triggered sweep.
2. The control signal from the Auto Multi appears at TP494.
 - a. If no triggers are present, TP494 is at $0v$.
 - b. If triggers are arriving (20 cps or above), TP494 is at $12v$.
3. In the NORM position of the A SWEEP MODE switch, D593 is cut off.
 - a. If triggers are arriving, the signal from the Auto Multi will forward bias D592, which in turn will back bias D593.
 - b. If triggers are not arriving, D592 anode will set at $-12v$, cutting off both D592 and D593.
 - (1) With D592 cut off, D593 has no current path.

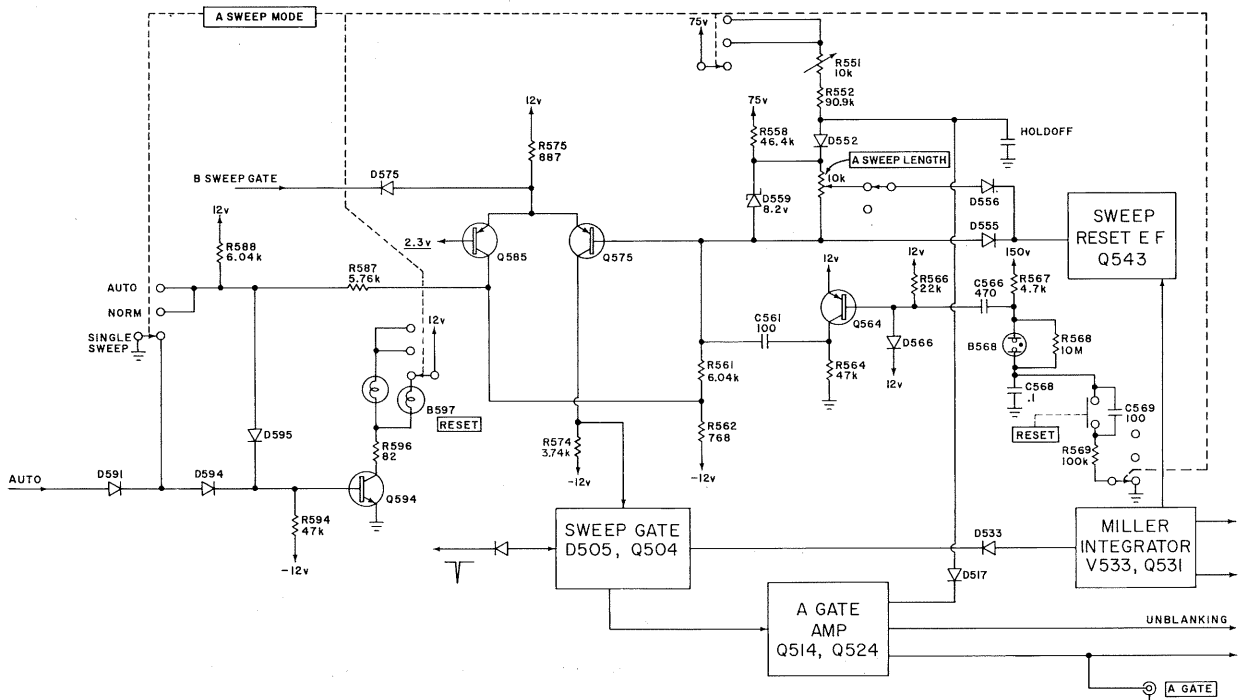
4. In the AUTO position of the A SWEEP MODE switch, D593 cathode is returned to -12v through R593.



- a. If no triggers are arriving and the Auto circuit output is at 0v, D593 conducts.
- b. 2 ma flows through R593 and D593 to the TD circuit.
- c. This 2 ma causes the Sweep Generator to free run.
- d. If triggers are arriving and the AUTO circuit output is at 12v, D592 conducts, lifting D593 cathode to cut-off.

- e. When the sweep has reached its maximum run-down and the Reset Multi switches, 12 ma is required by Q575.
- f. 7 ma of this current reverse biases D505, switching it to its low state, stopping sweep.
- g. At the end of hold-off, the Reset Multi returns to its Reset condition -- Q575 cuts off.
- h. The 5 ma forward current through D505 immediately switches the TD to its high state, starting a new sweep.
 - (1) 3 ma flows through R574 and 2 ma through R593.

M. Single Sweep Reset Amplifier, Q564



TYPE 453 A SWEEP GENERATOR
SINGLE SWEEP

B-453-0043
8-31-'65dl

1. The Single Sweep Reset Amplifier provides a pulse that switches the Reset Multi to its Reset or ready condition.
2. The circuit uses one transistor, a diode and a neon.
 - a. Q564 is a 151-087 silicon PNP transistor.
 - b. D566 is a 6185 silicon signal diode.
 - c. B568 is an A1D indicator type neon.
3. When the A SWEEP MODE switch is placed in the SINGLE SWEEP mode, the sweep circuit is placed in the lockout condition.
 - a. When the RESET button is pressed, the Reset Multi switches, placing the Sweep Gate in its Reset condition.
 - (1) The RESET light lights.
 - b. The first trigger to arrive initiates sweep.
 - c. At the end of sweep, the Reset Multi switches to its locked out position where it remains until the RESET button is again pressed.
4. The A SWEEP MODE switch has five contacts that are changed in the SINGLE SWEEP position.
 - a. The connection from the SWEEP LENGTH control through D552 etc., to 75v is opened.
 - (1) When a sweep is initiated, the negative pulse out of the A Gate Amplifier through D517 will cut off D552, disconnecting hold-off.
 - b. D591 cathode and D594 anode are grounded.
 - (1) The Auto control is disconnected.
 - (2) The ground on the Reset Multi drive to the Light Driver (Q594) is removed.

- c. The Light Driver collector is tied to the RESET light instead of the A SWEEP TRIG'D light.
 - d. The tie from D593 cathode to -12v and from D592 anode to -12v is removed*.
 - (1) This prevents the sweep from becoming reset prior to pressing the RESET button.
 - e. The bottom of R569 is tied to ground.
 - (1) C568 charges to 150v, arming the Reset circuit.
5. Quiescently, Q564 is cut off.
- a. Both the emitter and base are tied to 12v.
6. The Reset Multi is in its locked out position -- Q575 is on and Q585 is cut off.
- a. The Sweep Gate TD (D505) is reverse biased, electrons flowing from anode to cathode.
 - b. Q575 base sets at 500 mv.
 - c. D555 and D556 are disconnected.
 - d. Q585 collector (TP585) is at -9v.
7. Quiescently, C566 and C568 are charged to 150v**.
8. When the RESET button is pressed, C568 discharges through R569.
- a. When the drop across B568 has reached the ignition potential (about 80v), the neon fires.
 - b. As the neon fires, it immediately switches to its sustaining voltage of about 60v.
 - c. The bottom of the neon is held by C568.

* See Diagram, Page 9-25.

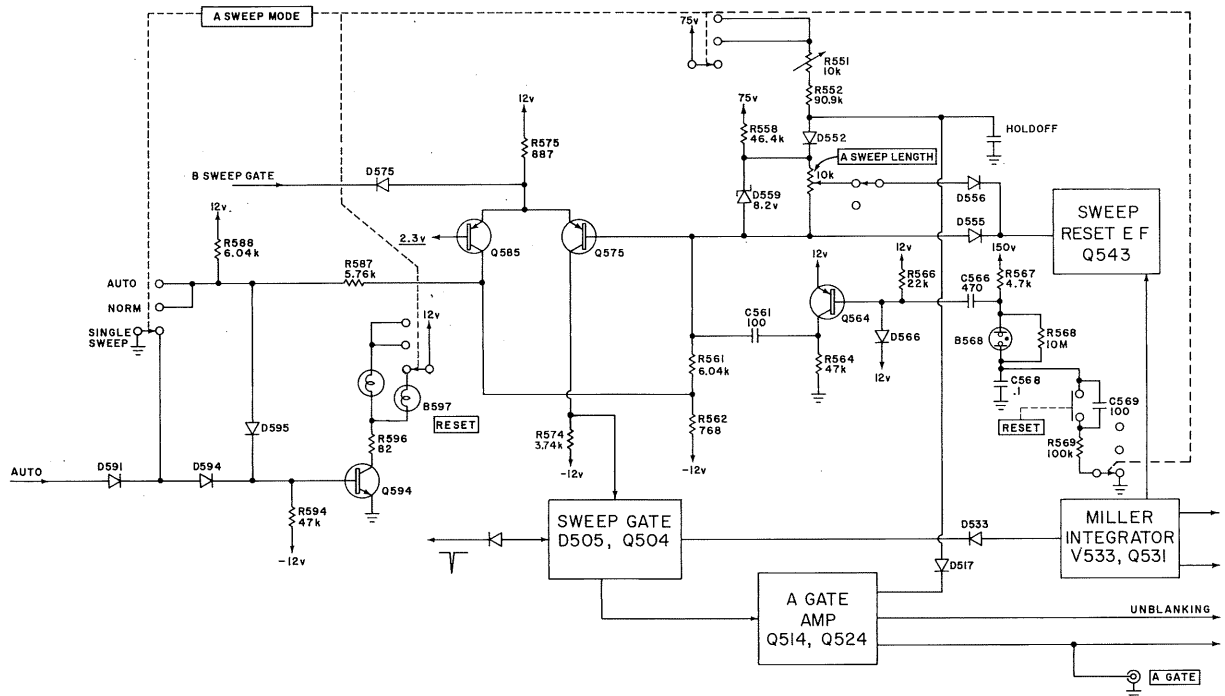
** The 150v supply is unregulated and may vary from 130v to 165v.

- d. The top of the neon, therefore, drops 20v.
 - e. A portion of the charge on C566 is dumped into Q564, saturating the transistor.
9. As Q564 collector pulls up to 12v (from 0v), the pulse couples through C561 to Q575 base.
- a. Q575 cuts off as the multi switches to its reset condition.
 - b. The Sweep Gating TD is reset awaiting a trigger.
10. When the Reset Multi switches and Q585 turns on, its collector rises to -2v to turn on the RESET light.
11. The first trigger after Reset will initiate sweep.
- a. The Sweep Gate pulls down on D517, discharging the hold-off cap and disconnecting D552.
 - b. Hold-off remains disconnected.
12. As the sweep ramp reaches its maximum negative excursion, D555 and/or D556 will conduct, pulling down on Q575 base.
- a. Q575 turns on, switching the multi to its locked out condition.
 - b. Since hold-off is disconnected, the multi cannot reset.
 - c. One Single Sweep cycle is complete.
13. D566 limits Q564 base positive excursion to .6v.
- a. When the RESET button is released, D566 clamps Q564 base while C566 charges to 150v.
14. The rather elaborate Reset circuit, with its slight delay before the neon fires the Reset pulse, assures positive Single Sweep reset.
- a. At fast sweep speeds, most switch contacts will, if used to directly actuate the Reset circuit, cause multiple sweeps.

N. Lamp Driver, Q594

1. The Lamp Driver lights an A SWEEP TRIG'D light when triggers are arriving in either AUTO or NORM position of the A SWEEP MODE switch.

a. The circuit also lights the RESET light in the SINGLE SWEEP position of the A SWEEP MODE switch.



TYPE 453 A SWEEP GENERATOR
SINGLE SWEEP

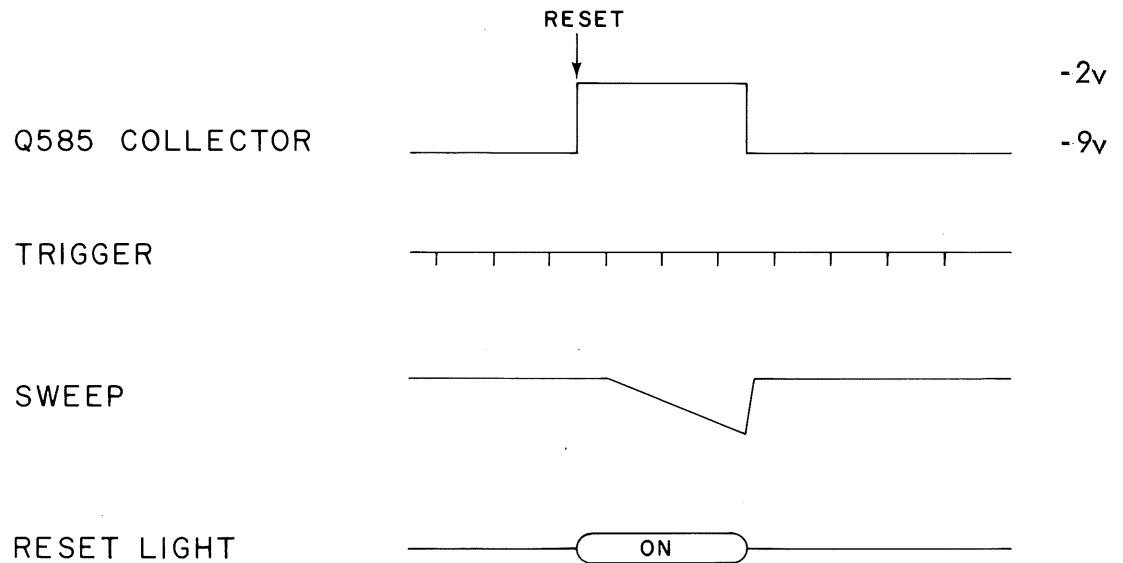
B-453-0043
8-31-65dl

2. Q594 is a 151-136 silicon NPN transistor.

a. The diodes are 6185 silicon signal diodes.

- b. B596 is a GE2107-D, 10v, 40 ma pilot light.
 - c. B597 is a 2187 bulb housed in the RESET switch button.
 - (1) It is a 14v, 80 ma bulb with a 100,000 hour rating.
 - (2) It doesn't come out -- the switch must be replaced.
3. Operation of the Lamp Driver circuit is the same in both the AUTO and NORM positions of the SWEEP MODE switch.
- a. D595 anode is connected to ground, removing any influence from the Reset Multi.
 - b. The Auto Multi (see page 7-14) functions regardless of SWEEP MODE position.
4. When no triggers are present and the Auto output is -1v, Q594 is cut off.
- a. Q594 base sets at -0.7v , clamped by D595.
 - b. The A SWEEP TRIG'D light is OFF.
5. When triggers arrive and the Auto output raises to 12v, Q594 saturates.
- a. With TP494 at 12v, 1.3 ma flows through D591 and D594.
 - (1) $230\ \mu\text{a}$ flows through R594.
 - (2) The balance, 1.1 ma, is Q594 saturated base current.
 - b. As Q594 collector pulls down to ground, the A SWEEP TRIG'D light turns on.
 - c. The light remains on as long as triggers arrive.
6. When the A SWEEP MODE switch is in the SINGLE SWEEP position, D594 anode is tied to ground.
- a. Through D591, the ground shorts out the Auto Multi output.
 - b. The Light Driver now becomes subject to control by the Reset Multi through D595.

- c. Q585 collector has two levels:
 - (1) -2v during Reset .
 - (2) -9v during hold-off -- locked out condition .
 - d. When the SWEEP MODE switch is placed in the SINGLE SWEEP position, the Reset Multi will be in its locked out condition -- Q585 cut off .
 - e. The -9v at Q585 collector will place D595 anode at .5v .
 - f. A .7v offset through D595 places Q594 base at -.2v to turn off the transistor .
 - g. The RESET light is OFF .
7. When the RESET button is pressed and the Reset Multi switches to its Reset condition, Q585 collector rises to -2v .



TYPE 453 A SWEEP GENERATOR
 RESET WAVEFORMS

B-453-0044
 8-20-'65 dl

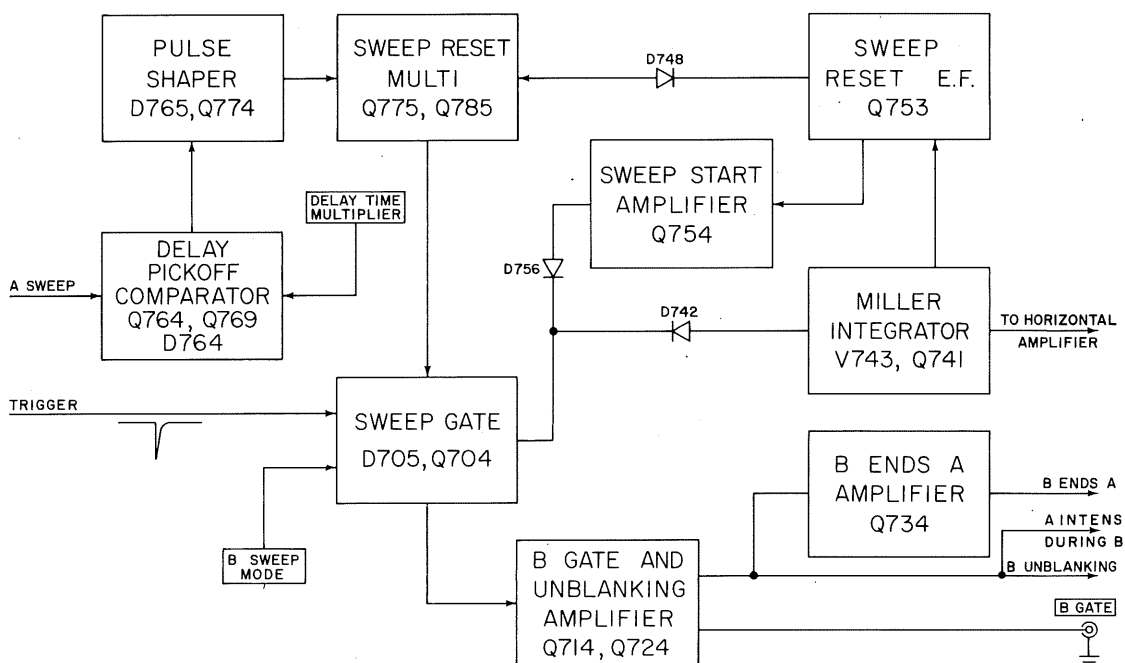
- a. D595 conducts, lifting Q594 base to saturation.
 - (1) D595 anode sees an equivalent 2.7k to +4.3v.
 - b. As Q594 collector pulls down to ground, the RESET light lights.
8. At the end of sweep the Reset Multi switches and Q585 collector again drops to -9v.
- a. The RESET light goes out.

X. B SWEEP GENERATOR

A. The B Sweep Generator is considered the Delayed Sweep.

1. The B Sweep Generator delivers a sweep ramp to the Horizontal Amplifier in the following mode of the HORIZ DISPLAY switch.
 - a. DELAYED SWEEP (B).
2. The Generator will supply a gate to the side panel B GATE jack in the following positions of the HORIZ DISPLAY switch.
 - a. A INTEN DURING B.
 - b. DELAYED SWEEP (B).
 - c. EXT HORIZ.
3. The B Sweep may be triggered (B SWEEP MODE switch in B TRIGGERABLE AFTER TIME DELAY position) in two positions of the HORIZ DISPLAY switch.
 - a. A INTEN DURING B.
 - b. DELAYED SWEEP (B).

B. Block Diagram



TYPE 453 B SWEEP GENERATOR
BLOCK DIAGRAM

C. Circuits that comprise the B Sweep Generator:

1. Sweep Gate; D705, Q704.
2. Miller Integrator; V743, Q741.
3. Sweep Reset EF; Q753.
4. Sweep Start Amplifier, Q754.
5. Sweep Reset Multi; Q775, Q785.
6. B Gate and Unblanking Amplifier; Q714, Q724.
7. B Ends A Amplifier, Q734.
8. Delay Pick-Off Comparator; Q764, Q769, D764.
9. Delay Pulse Shaper; D765, Q774.

D. Outputs

1. B Sweep waveform to the Horizontal Amplifier.
 - a. Negative going 2 ma current ramp.
2. B Unblanking pulse to the Z Axis Amplifier and the CRT.
 - a. A negative going 2 ma current pulse -- same duration as the sweep.
3. A Intensity Unblanking to the Z Axis Amplifier.
 - a. A negative going .3 ma current pulse the same duration as sweep.
4. B ends A pulse to the A Sweep Generator Reset Multi.
 - a. A negative going 12v pulse at the end of B Sweep.
5. B Gate waveform at the side panel BNC jack.
 - a. A positive going 12v gate $\approx 0v$ to $\approx 12v$.

E. Inputs

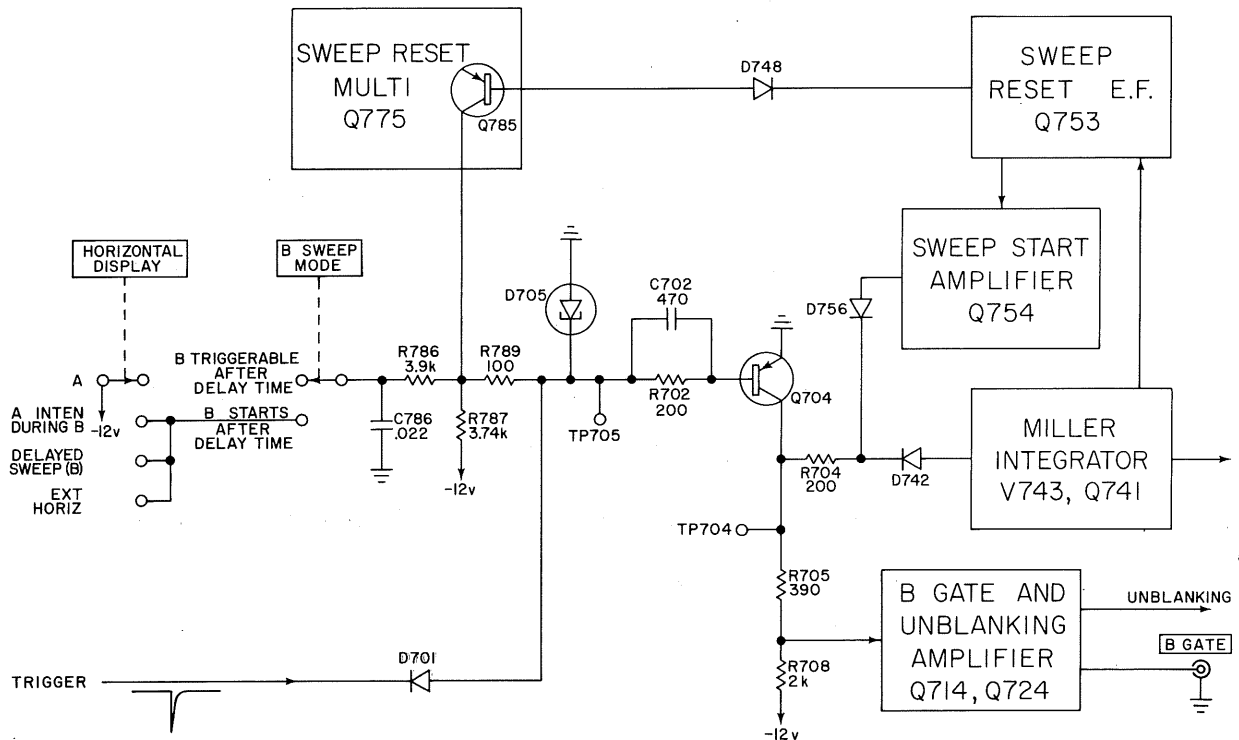
1. Negative going A Sweep ramp from the A Sweep Generator.
 - a. A 10v negative going ramp from $\approx 12\text{v}$ to $\approx 2\text{v}$.
2. Negative going trigger pulse from the B Trigger Generator.
 - a. 3 ma to 8 ma pulse, 3 to 5 nsecs wide.
 - b. The trigger is available only in the A INTEN DURING B and DELAYED SWEEP modes.

F. Block Logic

1. Quiescently the Sweep Gating TD is held in its "locked out" state by the Reset Multi.
2. The A Sweep Ramp is fed to the Delay Pickoff Comparator.
3. The comparator compares the A Sweep Ramp with a voltage set by the DELAY-TIME MULTIPLIER control.
4. When the Ramp voltage becomes equal to the DELAY-TIME MULTIPLIER voltage a signal is fed to the Pulse Shaper where the Delay Trigger is generated.
5. The Delay Trigger switches the Sweep Reset Multi to its ready state.
6. The Multi, in turn, places the Sweep Gate in its ready state.
 - a. If the B SWEEP MODE switch is in its B TRIGGERABLE AFTER DELAY TIME position, the Sweep Gate will switch with the arrival of the first trigger.
 - b. If the switch is in its B STARTS AFTER DELAY TIME POSITION, the Sweep Gate will switch immediately.
7. When the Sweep Gate switches, its output rises, disconnecting D742 and D756.

8. The Miller Integrator starts its run-down.
9. The B Sweep Ramp is fed to the Horizontal Display switch and is fed back through the Sweep Reset EF to the Reset Multi.
10. As the B Sweep Ramp runs down, either of two signals can switch the Reset Multi to its locked out condition, stopping sweep.
 - a. If the A Sweep terminates while B sweep is running down, the A Sweep retrace will reach comparison in the Delay Pickoff Comparator, causing a pulse to form in the Pulse Shaper which, in turn, will switch the Reset Multi.
 - b. If the B Sweep ramp reaches its full negative excursion before the A Sweep terminates, the B Sweep ramp will switch the Reset Multi.
11. When the Multi switches, it directs the Sweep Gate to its locked out condition.
12. The Sweep Gate output drops, connecting D742 (the disconnect diode).
13. Sweep stops and retrace starts.
14. At the end of retrace, D756 conducts, allowing the Sweep Start Amplifier to set the start of the next sweep.
15. There is no hold-off since the Sweep Reset Multi can be reset only by the Delay Pick-Off actuated by A Sweep.
16. The A Gate and Unblanking Amplifier provide waveforms of proper amplitude and polarity to drive the Unblanking circuits and B GATE output jack.

G. Sweep Gate; D705, Q704

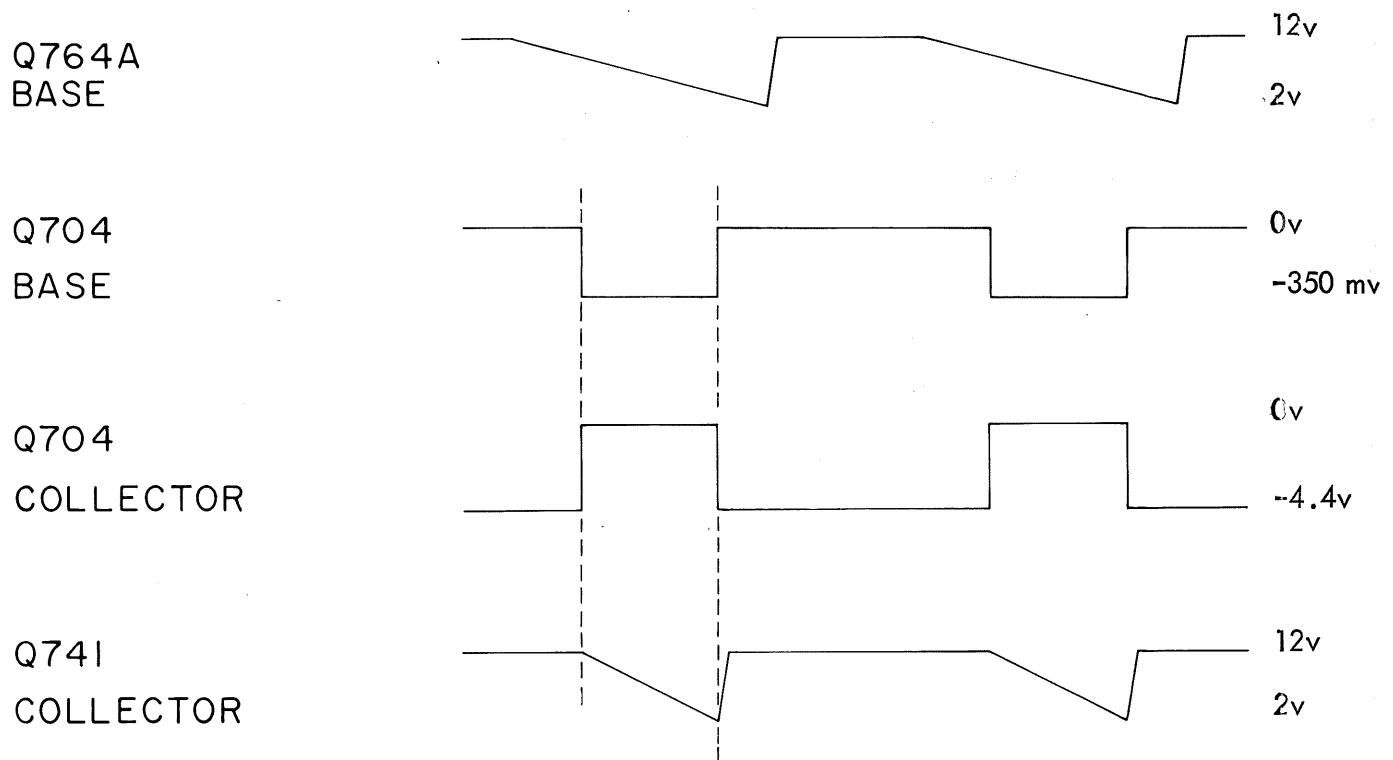


TYPE 453 B SWEEP GENERATOR
SWEEP GATE

B-453-0046
9-1-'65 mw

1. In the B TRIGGERABLE AFTER DELAY TIME position of the B SWEEP MODE switch, the B Sweep Gate is identical in operation to the A Sweep Gate.
2. Quiescently, the Reset Multi is in its locked out state.
 - a. The Sweep Gate TD (D705) is in its locked out condition.
 - (1) Q785 is conducting 9.3 ma.
 - (2) 3.1 ma flows through R787.
 - (3) 6.2 ma reverse biases D705.

- b. Q704 is cut off.
- (1) Emitter tied to ground.
 - (2) Base at 0v.
 - (3) Collector at -4.4v.
3. When the Delay Pick-Off switches the Reset Multi, Q785 cuts off.
- a. The 3.1 ma through R787 forward biases D705 placing it in its low state -- reset condition.
 - b. When a trigger arrives, the current trigger through D701 switches the TD to its high state.
4. D705 switches, turning on Q704. As Q704 collector rises to 0v, D742 disconnects starting sweep.

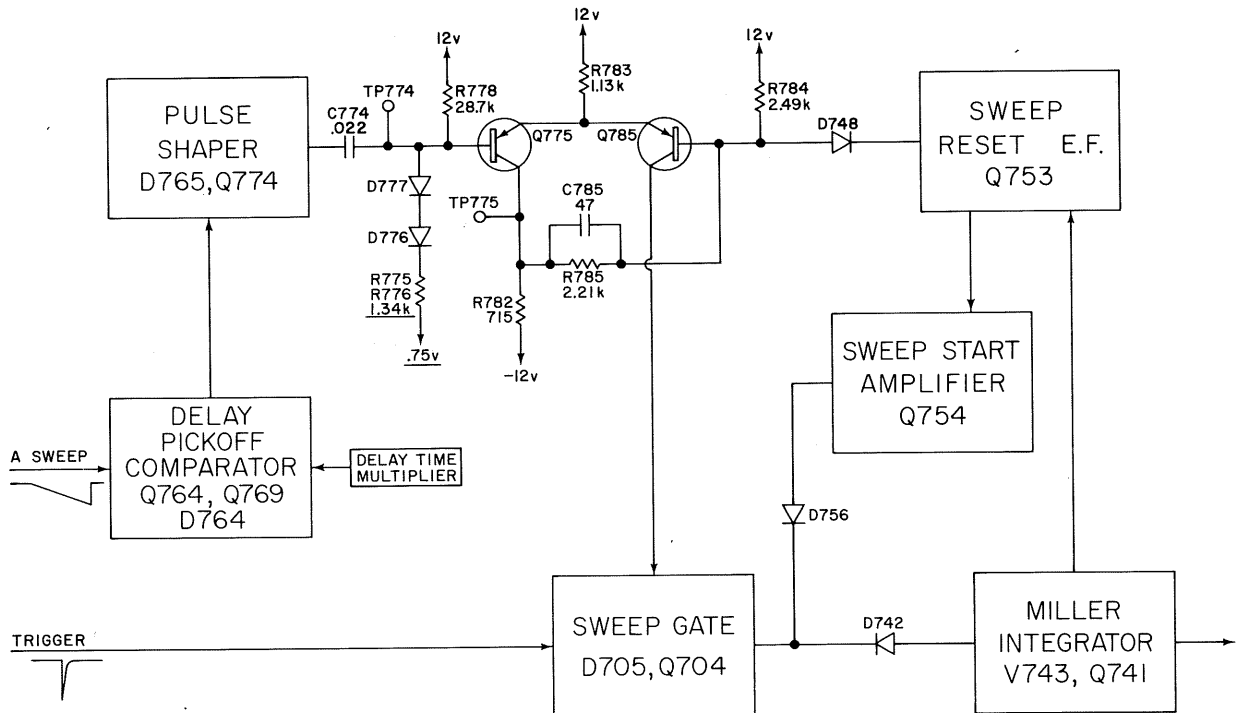


TYPE 453 B SWEEP GENERATOR
WAVEFORMS NO. I

B - 453-0047
9-3-'65 dl

5. The Reset Multi switches to its locked out condition.
 - a. The pulse initiated by A Sweep retrace (via the Delay Pick-Off) or the B Sweep ramp can switch the Reset Multi -- whichever comes first.
 - b. Q785 again draws 9.3 ma from the TD circuit.
 - c. The TD becomes reverse biased and cannot accept triggers.
 - d. The Sweep Gate is locked out.
 6. In the B STARTS AFTER DELAY TIME position of the B SWEEP MODE switch, R786 is tied to -12v provided the HORIZ DISPLAY switch is in either the A INTEN DURING B, DELAYED SWEEP or EXT HORIZ positions.
 - a. About 3 ma flows through R786.
 7. In the quiescent condition (Reset Multi locked out), Q785 draws 9.3 ma from the TD circuit.
 - a. 3 ma flows through R787 and 3 ma through R786.
 - b. 3 ma reverse biases D705.
 - c. The Sweep Gate is locked out.
 8. When the Reset Multi resets (Q785 cuts off), the 3 ma through R787 and the 3 ma through R786 switch the TD to its high state.
 - a. Sweep starts.
 - b. The circuit does not wait for a trigger.
- H. Miller Integrator; V743, Q741
Sweep Reset EF, Q753
Sweep Start Amplifier, Q754
1. The circuits are the same as in the A Sweep Generator.
 - a. There is only one ramp output, however, to the Horizontal Amplifier.

I. Sweep Reset Multi; Q775, Q785

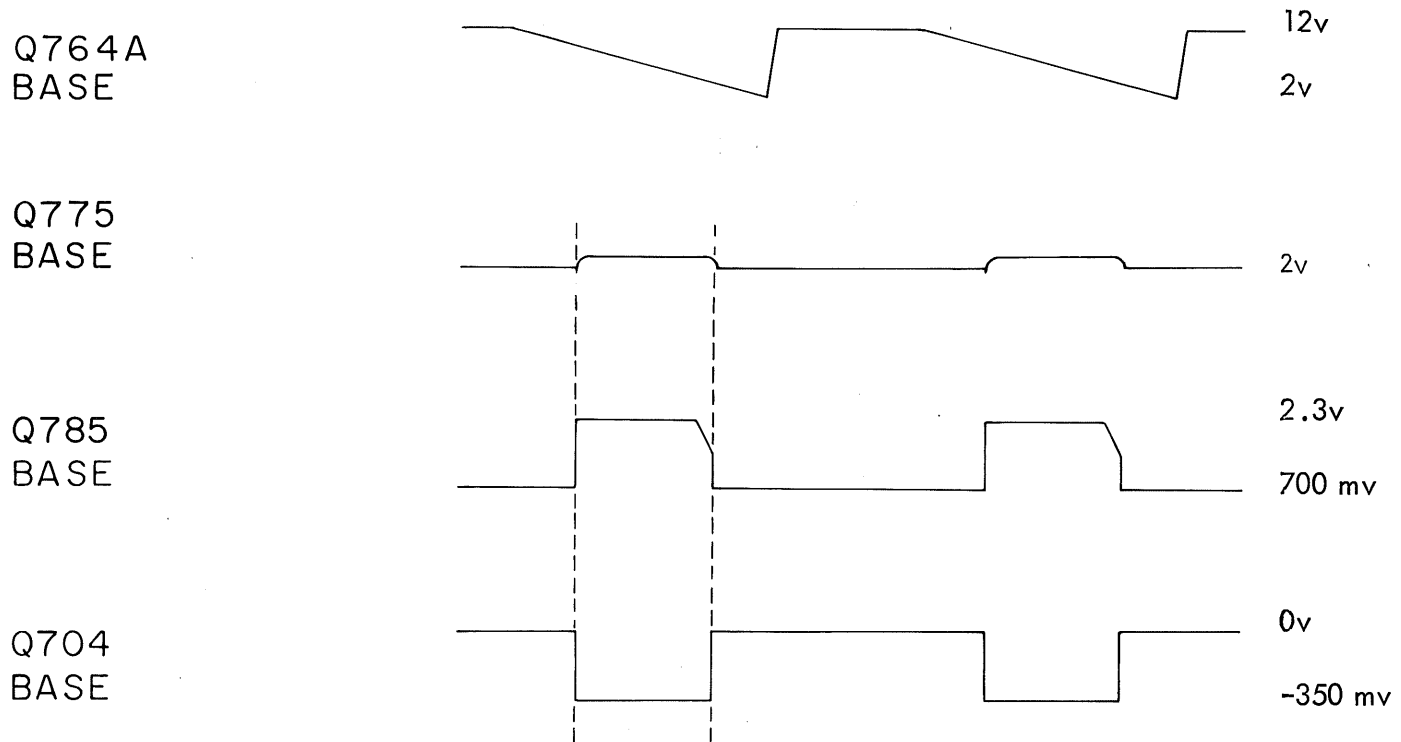


TYPE 453 B SWEEP GENERATOR
RESET MULTIVIBRATOR

B-453-0048
9-2-65 mw

1. The Reset Multi is a Schmitt multi that controls the operating condition of the Sweep Gate.
 - a. When Q785 is conducting and Q775 is cut off, Q785 pulls 9.3 ma from the Sweep Gate, placing it in its locked out condition -- it cannot initiate sweep.
 - b. When Q775 is conducting and Q785 is cut off, no current is drawn from the Sweep Gate -- the gate is reset.

2. When the Multi is in its locked out condition (Q785 conducting), it can be switched only by a pulse from the Delay Pick-Off circuit.



TYPE 453 B SWEEP GENERATOR
WAVEFORMS NO. 2

B-453-0049

9-3-'65 dl

- a. When A Sweep has reached a point in time indicated by the DELAY TIME MULTIPLIER, a negative going pulse will be applied to Q775 base through C774.
 - b. As the pulse biases Q775 to conduction, the Multi switches.
 - c. The Sweep Gate resets.
3. As B Sweep starts and A Sweep continues to run down, either of these waveforms can cause the Sweep Reset Multi to again switch to its locked out state.

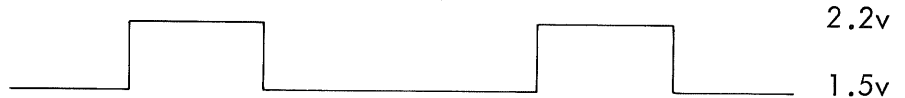
- a. If the B Sweep reaches its maximum run down before A Sweep ends, the B Sweep ramp will switch the Multi.
 - (1) In its Reset condition, Q785 base sets at 2.3v.
 - (2) When the B Sweep ramp reaches this level, D748 conducts.
 - (3) Q785 base follows the ramp down until at about 1.5v the transistor conducts, switching the multi.
 - b. If the A Sweep ends before the B Sweep has reached its full run down, A Sweep retrace initiates a positive going pulse (through the Time Delay Pickoff) that switches the Multi.
 - (1) Q775 base sets at about 2v.
 - (2) The positive going pulse applied to Q775 base cuts off the transistor switching the Multi.
 - c. When the Multi switches the Sweep Gate switches to its locked out condition, stopping sweep.
 - (1) B Sweep retrace disconnects D748.
 - (2) There is no hold-off.
 - d. The Multi remains in its locked out state until another pulse arrives from the Delay Pick-Off.
- J. Delay Pick-Off; Q764, D764, Q769, D765, Q774
1. The circuit compares the A Sweep ramp with a voltage selected by the DELAY TIME MULTIPLIER.

- a. A pulse generated by the comparison is fed to the Reset Multi to switch it to its reset condition.
- b. The delay, after the start of sweep, is set by the DELAY TIME MULTIPLIER.
- c. The setting of the A TIME/DIV control is multiplied by the reading on the DELAY TIME MULTIPLIER DIAL to obtain delay time.
- d. As an example, the waveforms below were taken with A TIME/DIV at .5 msec/div, B TIME/DIV at .2 msec/div, and the DELAY TIME MULTIPLIER at 3.8.

Q764 A
BASE



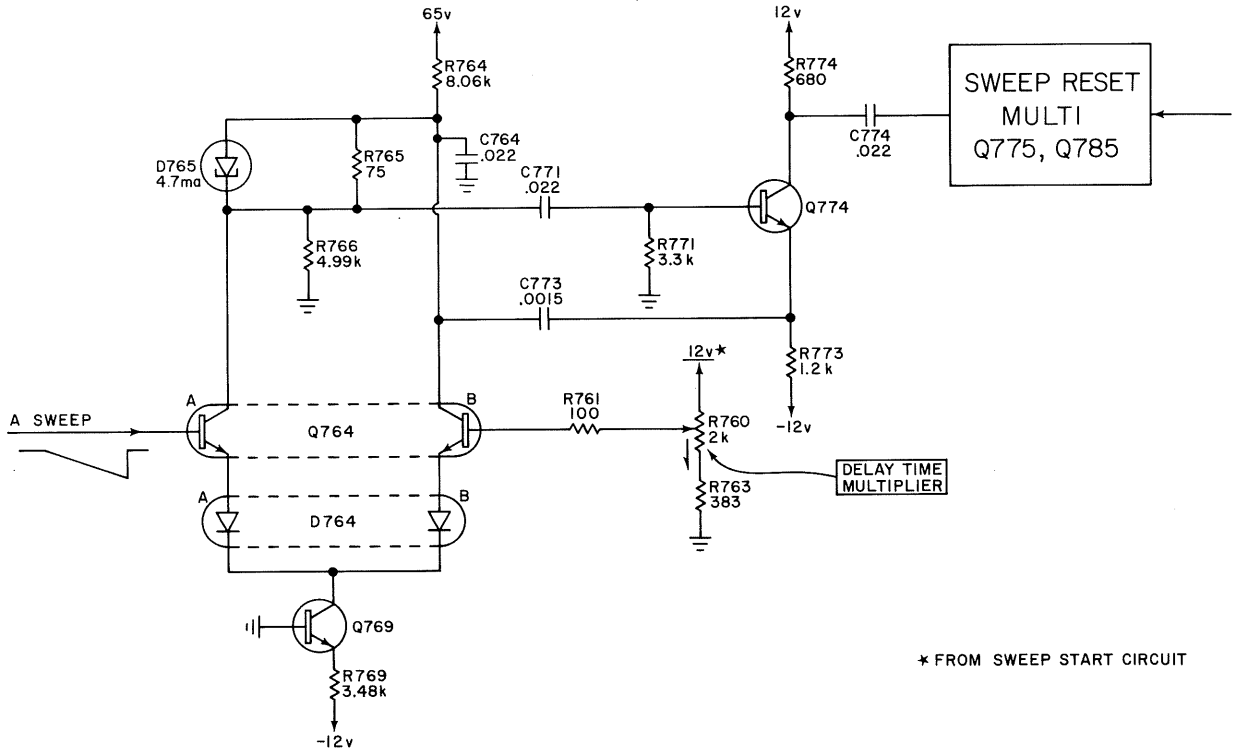
Q775, Q785
EMITTER



TYPE 453 B SWEEP GENERATOR B-453-0051
WAVEFORMS NO. 3 9-3-'65 dl

- e. $.5 \text{ msec/div} \times 3.8 = 1.9 \text{ msec delay.}$
2. The circuit uses three transistors, a tunnel diode and a dual diode.
 - a. Q764 is a 151-104 dual silicon NPN transistor.
 - b. Q769 and Q774 are 151-108, 2N2501 silicon NPN transistors.
 - c. D765 is a 152-125, 4.7 ma selected TD3A tunnel diode.

- d. D764 is a 152-151 composed of a pair of 1N3605 diodes encapsulated together.



* FROM SWEEP START CIRCUIT

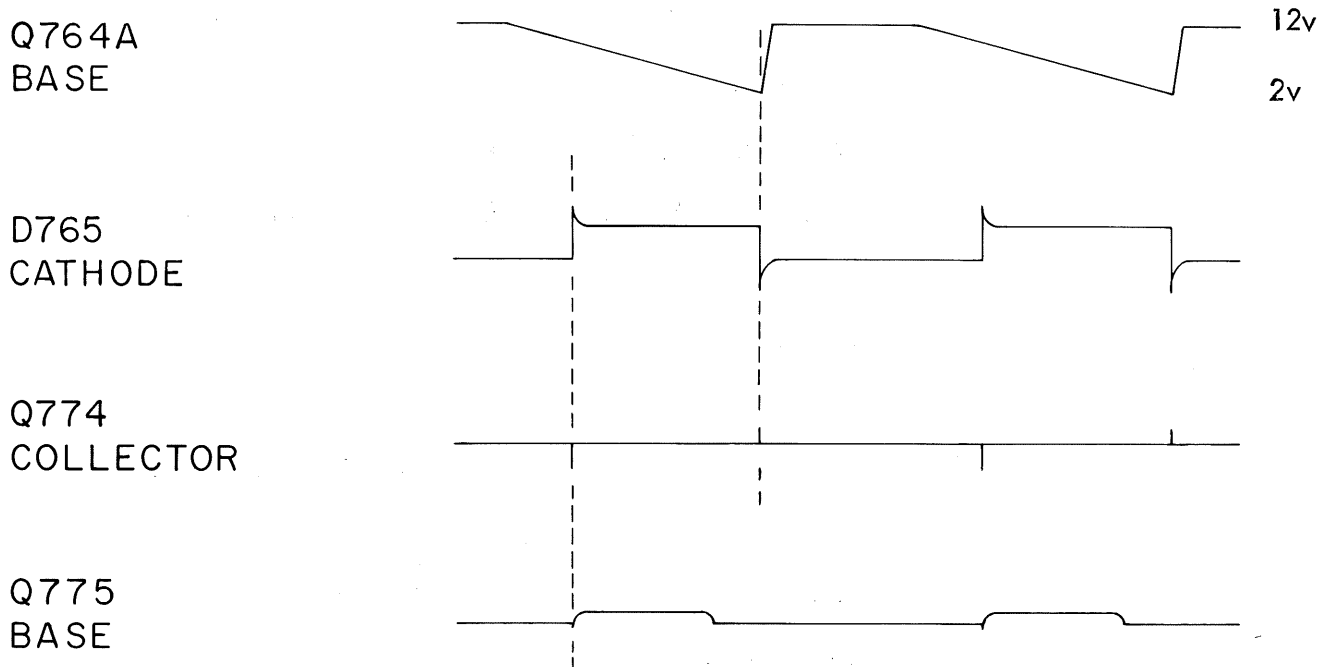
TYPE 453 B SWEEP GENERATOR
DELAY PICKOFF

B-453-0050
9-3-'65 mw

3. Q764 is the comparator.
 - a. The dual transistors in a common temperature environment assure Delay Pick-Off independent of temperature.
4. Q769 provides a constant current source for the Comparator and Pulse Shaper.
 - a. 3.25 ma flows through Q769, the Comparator and the TD circuit.

- b. The constant current source provides virtually the same switching current at any delay time.
5. D764 protects Q764 from reverse base-emitter breakdown.
- a. A 151-104 has a V_{EBO} of 8v.
 - b. Q764A base has an 11v swing.
6. R760, the DELAY TIME MULTIPLIER, is a 2k, 10 turn miniature wire-wound potentiometer.
- a. The pot has a resistance tolerance of $\pm 3\%$ and a linearity spec of .1%.
 - b. The top of the control ties to a 12v point on the SWEEP START divider (Sweep Start Amplifier).
 - c. A and B Sweep Start and Delay Pick-Off are all tied to the same voltage divider.
 - d. The control swings from 2v to 12v.
7. The Pulse Shaper consists of a TD and an AC coupled amplifier.
- a. The TD anode is anchored by C764 for any fast switching transients.
 - b. 3 ma flows through R766, placing the TD at about 15v.
8. Assume a DTM setting of 3.8, an A TIME/DIV setting of .5 msec/div, and a B TIME/DIV setting of .2 msec/div.
- a. The DTM arm and Q764B base set at about 8.8v.
 - b. At the start of A Sweep, Q764A base will be more positive than Q764B base.
 - (1) A Sweep ramp starts at about 12v.

- c. Q764A, therefore, will be conducting and Q764B cut off.



TYPE 453 B SWEEP GENERATOR
WAVEFORMS NO. 4

B-453-0052

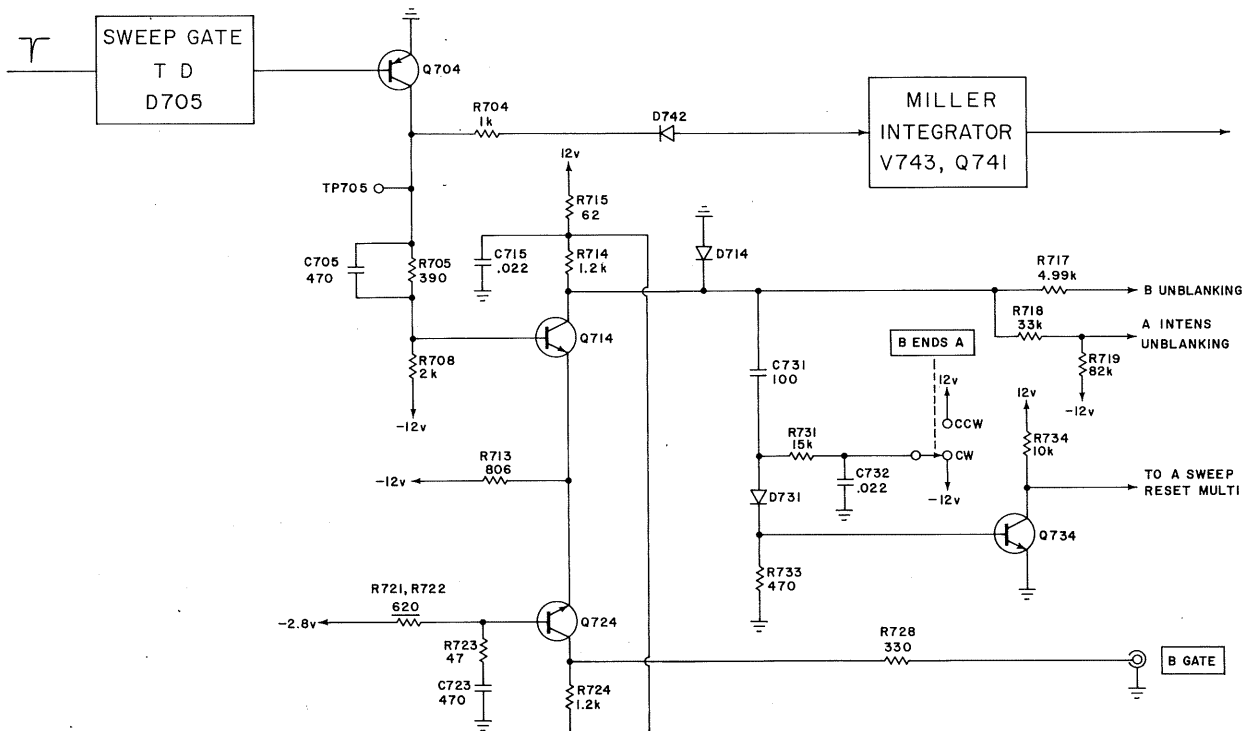
9-3-'65 dl

9. D765 is in its high state.
 - a. 3 ma flows through R766.
 - b. 3.2 ma flows through Q764A.
10. As A Sweep ramp drops Q764A base to 8.8v, Q764B begins to conduct.
 - a. Since the current supply is constant at 3.2 ma, less current will flow through Q764A and the TD.
 - b. When current through the TD circuit has dropped to the valley level*, the TD switches to its low state.

* See Transistor Program, Volume 2, Set 25.

- c. As the voltage drop across D765 drops from ≈ 350 mv to ≈ 50 mv, the cathode jumps 300 mv.
 - d. The 300 mv positive step is coupled through C771 to Q774 base.
 - (1) Q774 is conducting with its collector at 6v.
 - (2) C773 bypasses Q774 emitter for a brief period, differentiating the step.
 - (3) The cap returns the current to the TD circuit instead of ground where ground loops might occur.
 - e. The pulse is amplified and inverted in Q774 to drive the Reset Multi.
 - f. The pulse switches the Multi to its reset state.
11. When A Sweep retrace raises Q764A base to about 8.8v (DTM at 3.8), Q764A will turn on.
- a. As current through D765 increases, the TD switches to its high state.
 - b. The negative step inverted, amplified and differentiated in Q774 is applied to the Reset Multi.
 - c. If the Reset Multi has not been returned to its locked out condition by the B Sweep, the pulse from the Pulse Shaper will switch the multi.
- K. B Gate and Unblanking Amplifier; Q714, Q724
- 1. The circuit is essentially the same as that used in the A Sweep Generator.

2. Since there is no hold-off in the B Sweep Generator, the diode coupling to the hold-off is not included.



TYPE 453 B SWEEP GENERATOR
B GATE & UNBLANKING AMPLIFIER

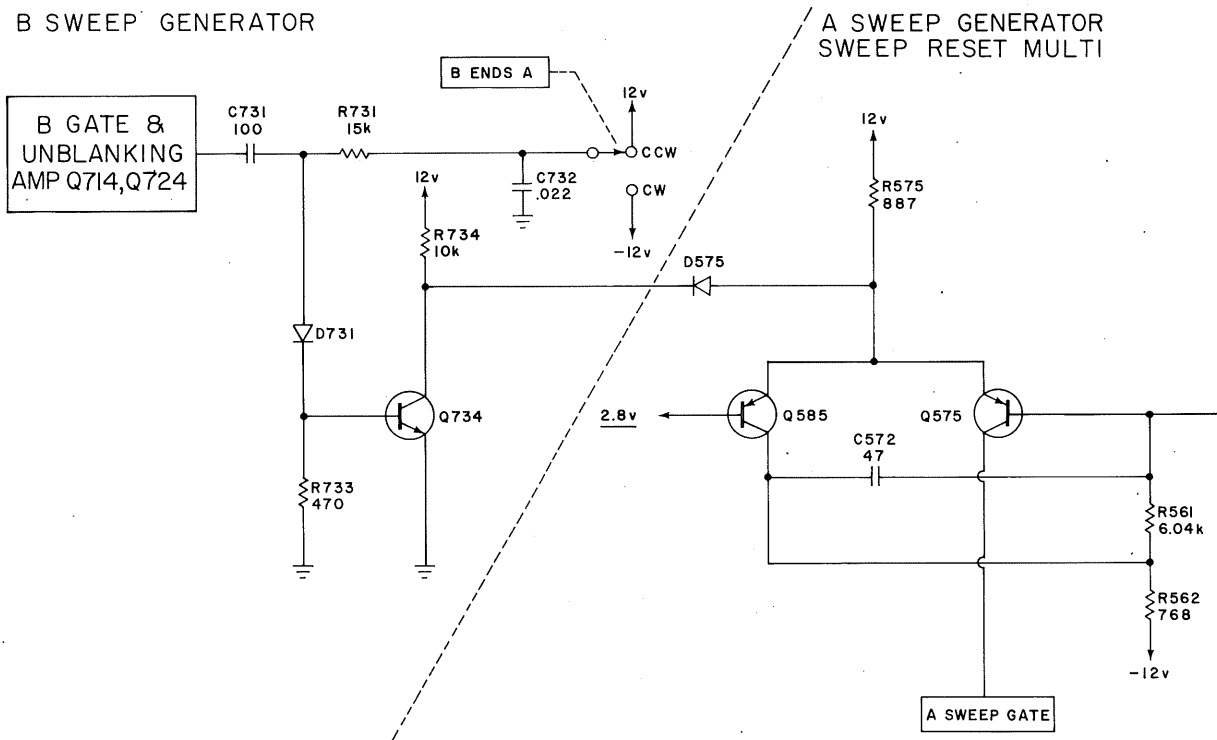
B-453-0053
9-2-65jg

3. The voltage swing at Q714 collector is about 9v instead of the 15v excursion found in the A Sweep Generator.
- The larger voltage swing in the A Sweep Generator is necessary to drive the hold-off circuit.
 - A lower value of R717 (4.99k instead of the 7.5k for R519) is required to match the 2 ma current unblanking pulse used in the A Sweep Generator.

4. The Sweep Generator Unblanking output for use during A INTENS DURING B mode is driven through R718 to the Z Axis Amplifier.
 - a. The current pulse is about .3 ma.

L. B Ends A Amplifier, Q734

1. The Amplifier provides a pulse to stop the A Sweep at the end of B Sweep.
 - a. The SWEEP LENGTH control (A Sweep Generator diagram) must be fully counter-clockwise in the B ENDS A detent.



TYPE 453 B SWEEP GENERATOR
B ENDS A AMPLIFIER

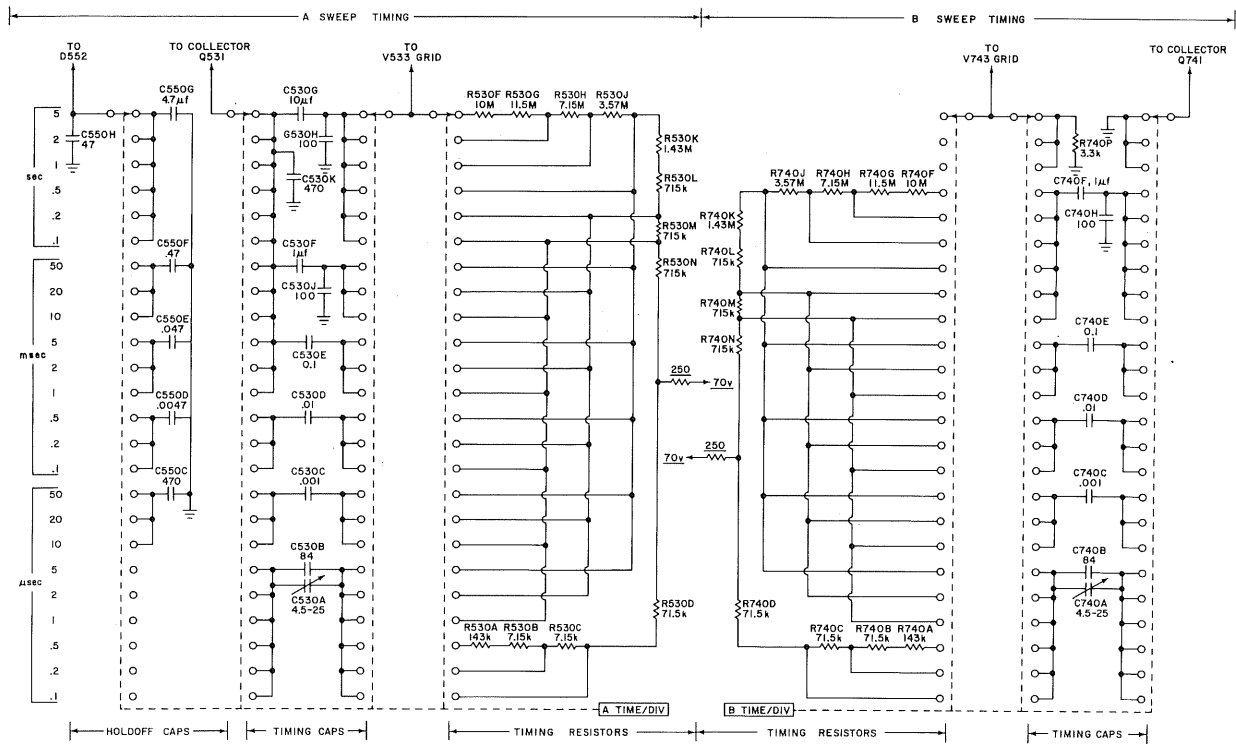
B-453-0054
9-3-'65 jg

2. When the B ENDS A switch is ON, R731 is connected to 12v.
 - a. D731 conducts and lifts Q734 base to about 350 mv.
 - b. Q734 is cut off.
3. When the B Gate Amplifier output rises to $\approx 9v$ (from $\approx 0v$), the step is differentiated in C731, R733 and lifts Q734 base to saturation.
4. The negative going 12v pulse (from 12v to 0v) turns on D575 and drops Q575, Q585 common emitters.
5. Since A Sweep is running down, Q575 is off and Q585 is on.
6. Q585 cuts off for the pulse duration.
 - a. As Q585 collector drops (from -2v to -9v), the step couples through C572 to turn on Q575 and switch the Multi.
 - b. The Reset Multi switches to its locked out state stopping A sweep.
7. When the B ENDS A switch is OFF, R731 is connected to -12v.
 - a. D731 cuts off.
 - b. The B Gate cannot pass to Q734.
 - c. Q734 remains cut off.
8. There is no danger of the A Sweep Reset Multi switching out of its locked out condition if the B Ends A circuit sends out a pulse during A Sweep retrace.
 - a. If, in the locked out condition (Q575 conducting, Q585 cut off), a B Ends A pulse cuts off Q575, the multi would not switch.
 - b. There is no coupling from Q575 to Q585 when the emitters are cut off.

XI. TIMING SWITCHES

A. There are two sets of timing switches that control sweep time for the two sweep generators.

1. The A Sweep Generator Timing Switch switches timing resistors, timing capacitors, and hold-off capacitors.



TYPE 453 TIMING SWITCHES

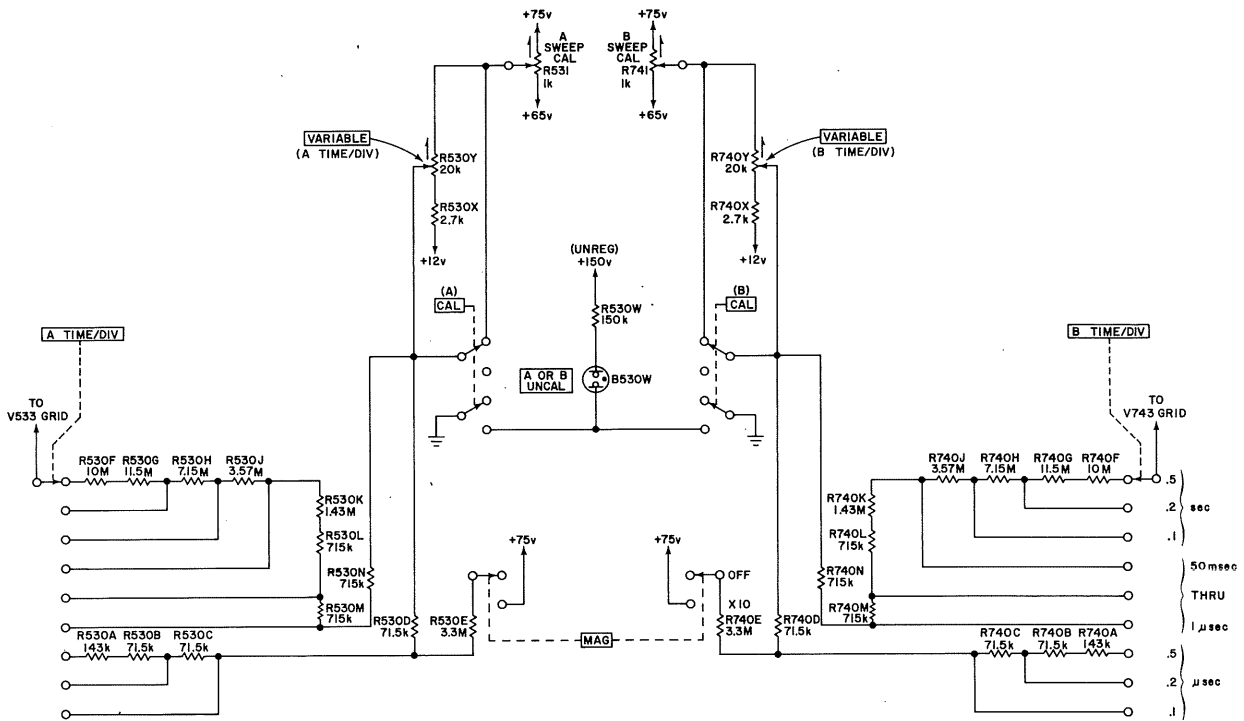
B-453-0055
8-27-65 mw

2. The B Sweep Generator Timing Switch switches timing resistors and timing capacitors.

a. The B Sweep Generator has no hold-off circuit.

B. A variable control is provided for both A Sweep and B Sweep (VARIABLE TIME/DIV).

1. The controls provide a variable increase in timing up to 2.5:1 over the calibrated sweep ranges.



TYPE 453 TIMING SWITCHES
VARIABLE (TIME/DIV)

B-453-0056
8-31-65 mw

2. An UNCAL light lights when either knob is turned away from its clockwise calibrated detent.
3. The A VARIABLE control is located concentric with the A and B Sweep Timing knobs.
4. The B VARIABLE control is mounted on the recessed side panel.
5. When the controls are in the CAL detent, a switch bypasses the VARIABLE control.

C. A Timing Switch

1. Timing caps.

- a. Timing positions .1 sec/div to 5 sec/div use 10 μ f TEK made mylar caps.
- b. Positions 10 msec/div to 50 msec/div use polystyrene 1 μ f TEK made caps.
- c. From 1 msec/div to 5 msec/div polystyrene .1 μ f TEK made caps are used.
- d. From .1 msec/div to .5 msec/div, .01 μ f polystyrene TEK made caps are used.
- e. From 10 μ sec/div to 50 μ sec/div, .001 μ f TEK polystyrene caps are used.
- f. From .1 μ sec/div to 5 μ sec/div, 84 pf mica caps paralleled by a trimmer capacitor are used.

2. Timing resistors:

- a. Metal film precision resistors are used in the timing circuit.
 - (1) R530N is a 715K .1% resistor
 - (2) R530K, R530L and R530M are .5%.
 - (3) All other timing resistors are 1%.
- b. Various multiples of 715K are used from 1 μ sec/div to 5 sec/div.
- c. The three fastest ranges, .1 μ sec/div to .5 μ sec/div, use multiples of 71.5K.
- d. The 5 sec/div position uses a total of 35.795 megohms.
- e. The .1 μ sec/div position uses a single 71.5K resistor providing the highest timing current of \approx 1 ma.

3. Hold-off capacitors:
 - a. The hold-off circuit uses six sets of hold-off caps to provide hold-off times from 2.5 μ sec to 70 msec*.
4. Three capacitors were empirically added to the timing circuit to suppress oscillations at various sweep speeds.
 - a. C530H, C530K and C530J serve this purpose.

D. B Timing Switch

1. The B Sweep does not function in the three slowest sweep speeds -- 1 sec/div, 2 sec/div and 5 sec/div.
2. In other positions, the same RC combinations as A Sweep timing are used.
3. C740H suppresses oscillation.

E. SWEEP CAL

1. Both timing circuits tie to a SWEEP CAL control.
2. The controls are tied between 65v and 75v.
 - a. The 65v is zener offset from the 75v supply by D544 (A Sweep Generator diagrams).
3. The control allows a $\pm 4.7\%$ variation in the voltage to be integrated.
4. Both the controls are mounted on the B Sweep Generator board.

F. MAG Switch

1. In the three fastest positions of both TIME/DIV switches, the MAG switch has supplementary control.
2. When in the X10 position of the MAG switch, 23 μ a of additional timing current is provided.

* See Page 9-20.

- a. A connection through a 3.3M resistor (R530E or R740E) to 75v provides the added current.
3. Timing speed is increased up to 2.3% to compensate for losses in the Horizontal Amplifier.
- a. Timing speed increase is 2.3% at .1 $\mu\text{sec}/\text{div}$, 1.15% at .2 $\mu\text{sec}/\text{div}$ and .5% at .5 $\mu\text{sec}/\text{div}$.

XII. HORIZONTAL AMPLIFIER

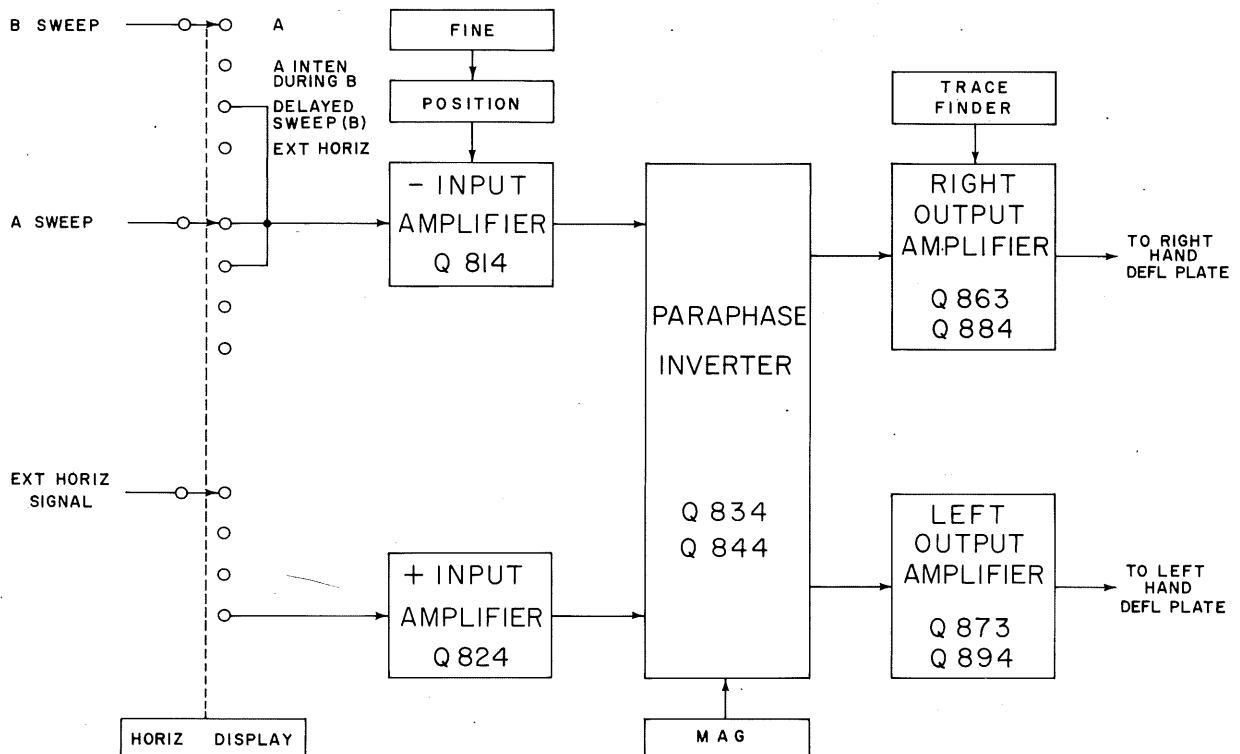
A. The Horizontal Amplifier provides the voltage drive to the CRT horizontal deflection plates.

1. The output requirement is a push-pull voltage ramp 130v* peak-to-peak for 11 divisions.

a. 65v per side.

b. CRT sensitivity is nominally 11.8 v/div push-pull or 5.9 v/div each plate.

B. Block Diagram



TYPE 453 HORIZONTAL AMPLIFIER
BLOCK DIAGRAM

B-453-0057
8-16-65 jg

* Deflection sensitivity is spec'd at 11.0 v/div to 12.6 v/div. Scan is spec'd at 11 div \pm .5 div. Voltage drive to the CRT may vary, therefore, from 115.5v to 145v.

C. Circuits that comprise the Horizontal Amplifier.

1. - Input Amplifier, Q814.
2. + Input Amplifier, Q824.
3. Paraphase Inverter; Q834, Q844.
4. Right and Left Hand Output Amplifiers; Q863, Q873, Q884, Q894.

D. Inputs

1. A Sweep Ramp
 - a. A negative going 2 ma current ramp from the A Sweep Generator.
2. B Sweep Ramp
 - a. Negative going 2 ma current ramp from the B Sweep Generator.
3. External Horizontal Input
 - a. From the B Sweep Trigger Cathode Follower.
 - b. The signal may originate at the EXT HORIZ jack or may come from the CH 1 Input Amplifier.

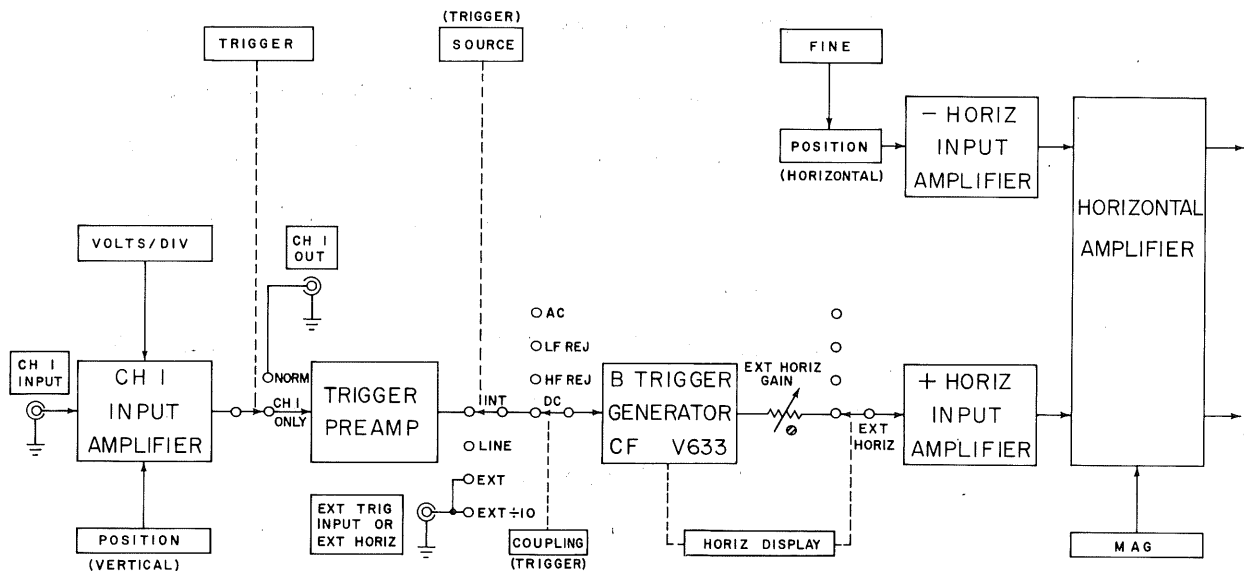
E. Block Logic

1. Sweep inputs are amplified in the - Input Amplifier.
2. Input selection is made by means of the HORIZ DISPLAY switch.
 - a. In the A position A Sweep is selected.
 - b. In the A INTENS DURING B position, A Sweep is selected.
 - c. In the DELAYED SWEEP (B) position, B Sweep is selected.
3. The External Horizontal signal is amplified by the + Input Amplifier.
4. Signal current into the - Input Amplifier is 200 $\mu\text{a}/\text{div}$.
5. Transimpedance of the Horizontal Amplifier in the Sweep Mode is about 59K.

$$\begin{aligned}
 \text{a. } T_Z &= \frac{E_{\text{out}}}{i_{\text{in}}} \\
 &= \frac{11.8 \text{ v/div}}{200 \mu\text{a/div}} \\
 &= 59\text{K}
 \end{aligned}$$

6. In the EXT HORIZ position of the HORIZONTAL DISPLAY switch, a calibrated XY display is possible.

a. The signal is applied to the CH 1 Input jack.



TYPE 453 HORIZONTAL AMPLIFIER
EXTERNAL HORIZONTAL BLOCK

B-453-0058
8-16-65jg

- b. The signal appears at the Channel 1 Trigger EF* at about 27 mv/div.
- c. The CH 1 - NORM switch is placed in the CH 1 position.

* See Page 2-18.

- d. The signal is then amplified in the Trigger Preamp (gain about 10).
- e. The Trigger Preamp output, about 270 mv/div, is fed to the B Trigger Generator circuit.
- f. The B (TRIGGER) SOURCE switch must be in the INT position.
- g. The B (TRIGGER) COUPLING switch should be in DC*.
- h. The signal passes through the B Trigger CF.
- i. The EXT HORIZ position of the HORIZ DISPLAY switch directs the signal to the Horizontal Amplifier instead of to the B Trigger Generator circuit.
 - (1) The HORIZ DISPLAY switch also selects the External Horizontal signal to drive the Horizontal Amplifier.
 - (2) The switch also places the Horizontal Amplifier on X10 MAG.
- j. By adjusting the EXT HORIZ GAIN control (B Sweep Generator board), the CH 1 VOLTS/DIV control may be calibrated to indicate the Horizontal deflection factor.

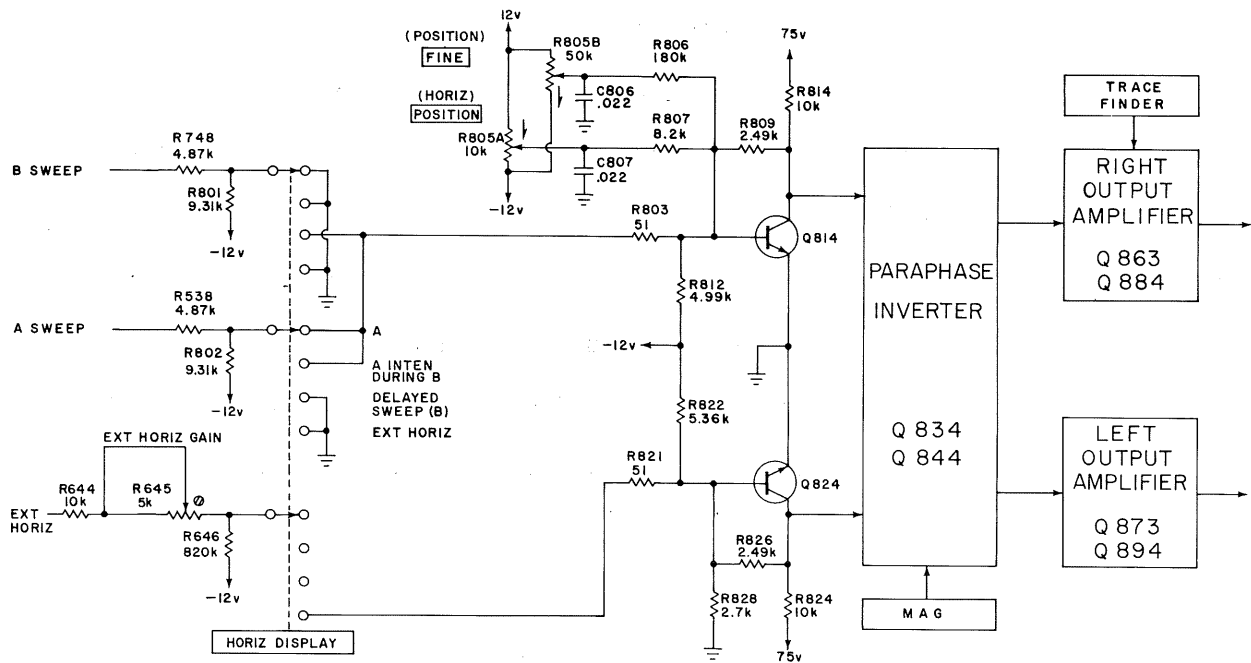
*Procedure:

1. Place B (TRIGGER) COUPLING switch in AC.
2. With no signal applied, center the spot horizontally using the (HORIZ) POSITION control.
3. Switch to DC and use (CH 1) POSITION control for horizontal positioning.
4. Do not use (HORIZ) POSITIONING control for positioning for XY operation.
 - a. CH 1 Input Amplifier can be overdriven with the spot on the screen if the procedure is not followed.

- k. The signal is subject to control by the CH 1 VOLTS/DIV control, the (VERTICAL) POSITION control, the TRIGGER (CH 1 - NORM) control, the (TRIGGER) SOURCE switch, the (TRIGGER) COUPLING switch, the HORIZ DISPLAY switch, and the (HORIZONTAL) POSITION control.
 - l. The signal is not subject to control by the VARIABLE (VOLTS/DIV) control or the (CH 1 VERTICAL) GAIN control.
7. Calibrated deflection factor of the Horizontal system is, therefore, 5 mv/div to 10v/div in 1-2-5 sequence.
- a. Gain of the system (from CH 1 Input jack to CRT Horizontal Deflection plates) is about 2360 (in 5 mv/div setting).
 - b. Frequency response is DC to >5 mc.
8. The instrument may also be operated in the EXT HORIZ mode by selecting EXT or EXT $\div 10$ position of the (B TRIGGER) SOURCE switch.
- a. Input is via the EXT TRIG INPUT or EXT HORIZ jack.
 - (1) A front panel BNC connector.
 - b. Deflection factor is 270 mv/div, $\pm 15\%$ in the EXT position.
 - c. Deflection factor is 2.7 v/div, $\pm 20\%$ in the EXT $\div 10$ position.
 - d. Frequency response is DC to 5 mc.
 - e. Input Z is approximately 1 meg paralleled by 20 pF.

9. The outputs from the - Input Amplifier and the + Input Amplifier drive the Paraphase Inverter.
 - a. Since the Sweep ramp is negative going, polarity reversal is required (in the - Input Amplifier) to move the trace from left to right.
10. The Paraphase Inverter drives the Output Amplifier.
11. The TRACE FINDER switch limits the range of the Horizontal Amplifier to about 8 divisions.
12. The MAG switch increases the gain of the Horizontal Amplifier by 10.

F. Input Amplifiers; Q814, Q824



TYPE 453 HORIZONTAL AMPLIFIER
INPUT AMPLIFIERS

B-453-0059
8-17-'65 jg

1. Two amplifiers are used to drive the Paraphase Inverter.
 - a. The - Amplifier is used to amplify the Sweep and Position information.
 - b. The + Amplifier amplifies the External Horizontal signal.
 - c. The circuits are single stage feedback amplifiers.
2. Q814 and Q824 are 1510127 silicon NPN transistors selected from 2N2369.
3. The Sweep waveforms from the A and B Sweep Generators are voltage ramps as they appear at the left of R538 and R748.
 - a. R538 and R748 are R_i resistors for the feedback amplifier.
 - b. Signal current is $200 \mu\text{a}/\text{div}$ -- a total of 2.2 ma for 11 divisions.
4. R801 and R802 satisfy the static current needs of the R_i resistors.
 - a. Center screen current through R538 and R748 is 1.5 ma.
 - b. This current is satisfied by R801 and R802.
 - c. No current flows through the HORIZ DISPLAY switch when the beam is at center screen.
 - d. When the switch is in the EXT HORIZ position, with no signal present, the beam will rest at center screen (with position control centered).
5. The sweep input is grounded by the HORIZ DISPLAY switch when not in use.
6. Q814 and Q824 bases set at .7v and the collectors at 7.25v.
 - a. The emitters are grounded.
 - b. There is very little signal voltage at Q814 base -- 2-3 mv/div.
 - c. The signal at Q814 collector is about 500 mv/div.

7. Both the POSITION control and the FINE control drive into the - Input Amplifier.
 - a. R807 is R_i for the POSITION control and R806 is R_i for the FINE control.
 - b. With MAG OFF and the POSITION control clockwise, the start of sweep is positioned to the right of graticule center.
 - c. CCW, the control, positions the end of sweep to the left of graticule center.
 - d. The FINE control has a range of 5 divisions to 8 divisions.
 - e. C806 and C807 bypass stray transient spikes.
8. The + Input Amplifier amplifies the External Horizontal signal.
 - a. The amplifier accepts a positive going signal to move the beam to the right.
 - (1) There is no polarity reversal in the CH 1 Input Amplifier or in the Trigger Preamplifier.
 - b. The signal to the left of R644 has a deflection factor of about 270 mv/div.
 - c. Signal current into Q824 is about 20 μ a/div.
 - d. R646 supplies static current to R644 and R645 so no static current flows through the switch.
 - e. When no External signal is applied, the trace is centered on the graticule.
 - (1) When EXT Horizontal is connected to the CH 1 Input Amplifier, Vertical Positioning constitutes a signal to the Horizontal Amplifier that will deflect the beam.

G. Paraphase Inverter; Q834, Q844

1. The Paraphase Inverter provides the push-pull drive to the Output Amplifiers.

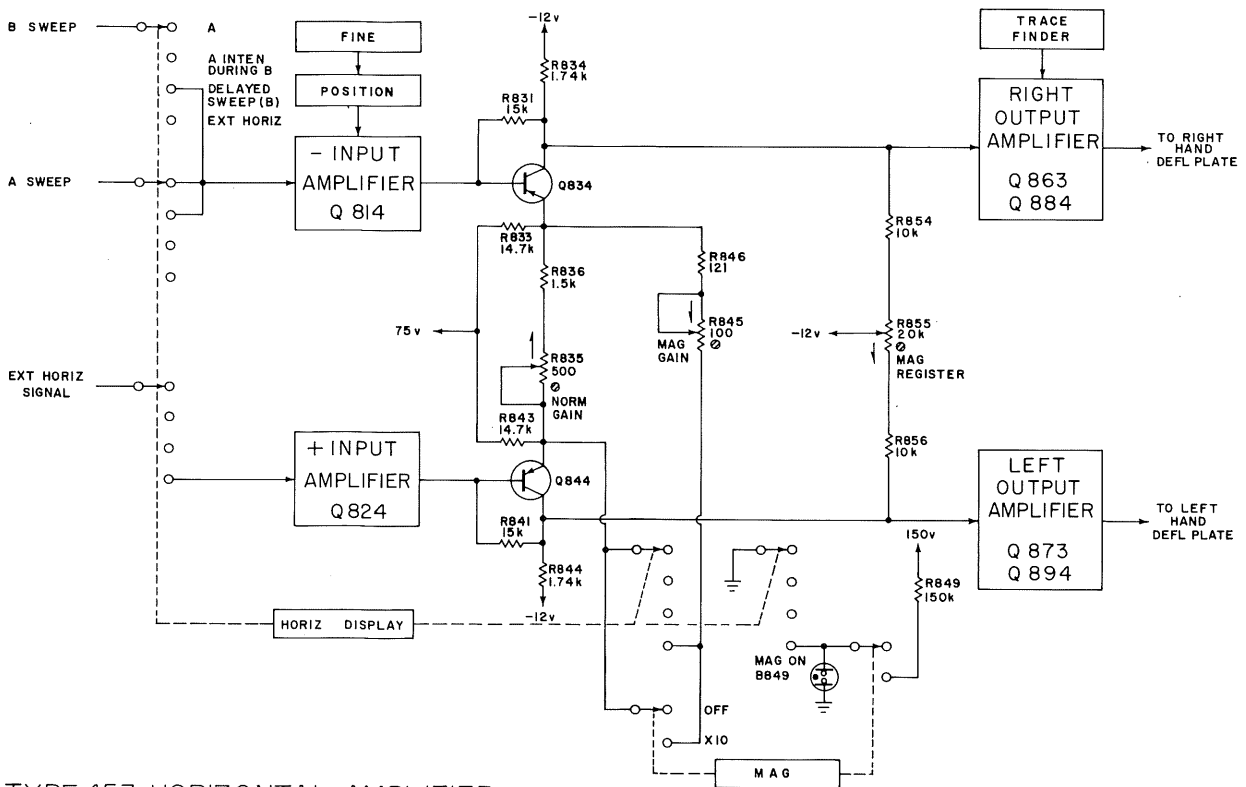
a. The circuit is an emitter coupled Paraphase Inverter with negative feedback.

b. Output signal current is 267 $\mu\text{a}/\text{div}$ per side.

$$(1) \frac{5.9 \text{ v/div/side}}{22.1\text{K}}$$

c. Transadmittance is 530 μhos .

$$(1) T_Y = \frac{i_{\text{out}}}{e_{\text{in}}} = \frac{267 \mu\text{a/div}}{500 \text{ mv/div}}$$



TYPE 453 HORIZONTAL AMPLIFIER
PARAPHASE INVERTER

B-453-0060
8-23-65jg

2. Q834 and Q844 are 151-133 silicon PNP transistors selected from 2N3251.
3. Typical DC levels:
 - a. Bases, 7.25v.
 - b. Emitters, 7.9v.
 - c. Collectors, -.75v.
4. Resistors, R831 and R841, compensate for the inherent signal unbalance in a paraphase inverter.
 - a. The emitter return resistors shunt the undriven side of the paraphase inverter.
 - b. Assume Q834 is driven.
 - c. Signal currents through Q834 collector load would exceed those in Q844 collector load by the amount flowing through R833.
 - d. Signal current through R831 will exactly oppose the currents through R833.
 - e. The result is equal output signal currents at each collector.
5. Paraphase Inverter typical output signal current is about 267 $\mu\text{a}/\text{div}$ per side.

$$a. \quad \Delta i_{\text{out}} = \frac{\Delta e_{\text{in}}}{R_e}$$

where e_{in} is 500 mv/div

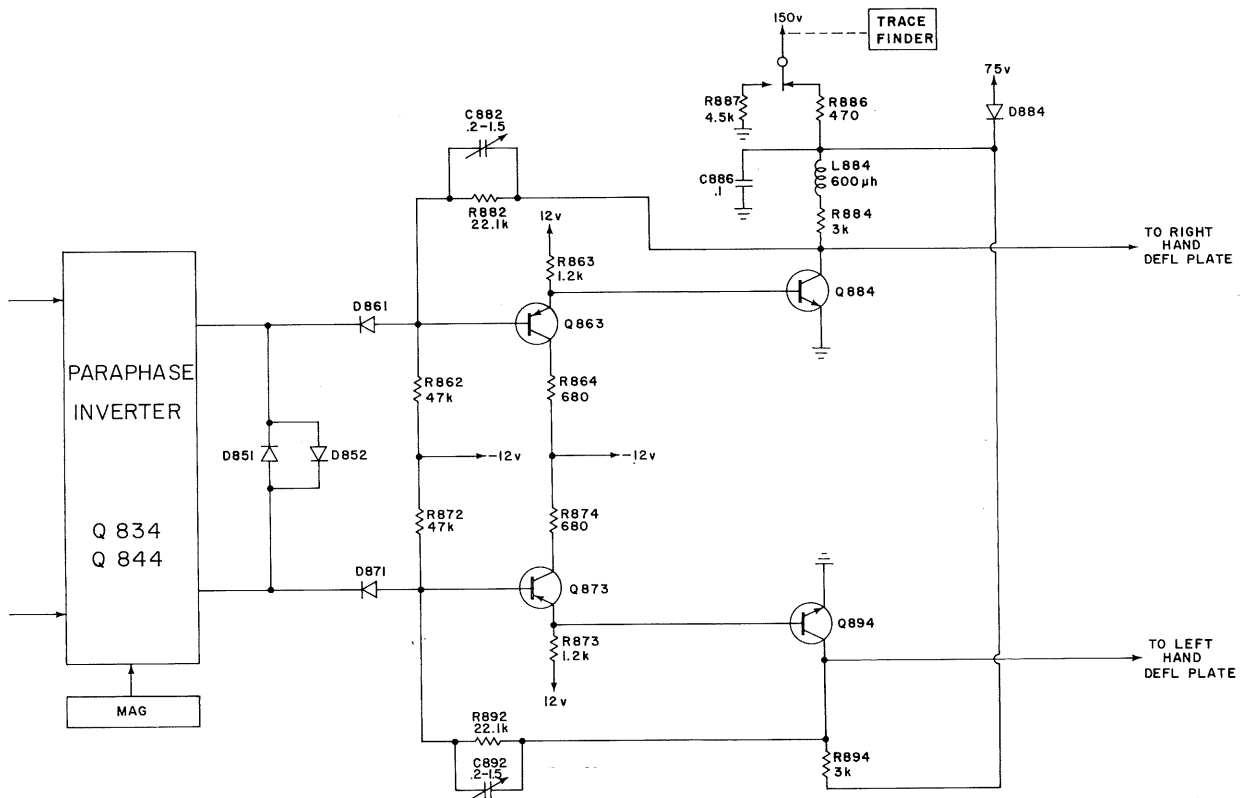
R_e is R836 plus R835 at mid range.

- (1) The effect of R833 is compensated for by R831 so is not part of R_e in this problem.

- b. The NORM GAIN control (mounted on the Horizontal Amplifier board) varies R_e by a factor of 25%.
 - c. Output signal may be varied by $\pm 12\%$ by the NORM GAIN control.
6. The MAG control connects R846 and R845 in shunt with R836 and R835.
- a. R_e is reduced to 154 ohms (with the MAG GAIN mid range).
 - b. Output signal current is increased by a factor of 10.
 - c. The MAG GAIN control has a 37% range.
 - d. The MAG is connected by either the MAG switch or by placing the HORIZ DISPLAY switch in the EXT HORIZ position.
 - e. Whenever the MAG switch is ON, an indicator neon lights.
7. The MAG REGISTER control (mounted on Horizontal Amplifier board) assures that the display at screen center does not shift when the MAG is switched in and out.
- a. The POSITION control can be adjusted so Q834 and Q844 emitters are at the same potential.
 - b. Under this condition no current flows through the NORM GAIN or MAG GAIN controls.
 - c. No trace shift occurs as the MAG is switched in and out.
 - d. The MAG REGISTER places the beam at center screen when the POSITION control is centered.
 - (1) The control varies the static current into the Output Amplifier.

H. Output Amplifiers; Q863, Q884, Q873, Q894

1. The two Output Amplifiers drive the CRT Horizontal deflection plates.



TYPE 453 HORIZONTAL AMPLIFIER
OUTPUT AMPLIFIERS

B-453-0061
8-26-65jg

2. The amplifiers are transistor pair feedback amplifiers.
3. Four transistors and five diodes are used.
 - a. Q863 and Q873 are 151-133 silicon PNP transistors.
 - b. Q884 and Q894 are 151-124 silicon NPN transistors selected from TA1938.
 - (1) The transistors are mounted on beryllium oxide heat sinks.

- c. D861 and D871 are 1N3605 silicon diodes.
 - d. D851 and D852 are 6153 silicon diodes -- similar to 1N4244.
 - e. D884 is a 6061 silicon diode.
4. Nominal DC voltage levels:
- a. Q863, Q873 bases, -.1v.
 - b. Q863, Q873 collectors, -5.3v.
 - c. Q863, Q873 emitters, +.55v.
 - d. Q884, Q894 bases, +.55v.
 - e. Q884, Q894 collectors, 47v.
5. Q884 and Q894 each draw 23.7 ma at mid screen.
- a. 2.1 ma flows through the feedback resistors, R882 and R892.
 - b. When driven off screen, Q884 and Q894 collector current reaches a maximum of 39 ma and a minimum of 3.8 ma.
6. Transimpedance of the amplifiers is nominally 22K.
- a. $T_Z = \frac{5.9 \text{ v/div}}{267 \text{ } \mu\text{a/div}}$
7. Voltage swing at the deflection plates for 11 divisions is $\approx 65\text{v}$ -- 15v to 80v.
- a. Mid screen level is 47v.
 - b. With MAG ON the amplifier output limits at 5v and 97v to 99v.
8. D861 and D871 prevent the output transistors from saturating.
- a. Stored charge in the saturated transistors would delay recovery after being overdriven.
 - b. Assume signal current causes D861 to turn off.
 - c. Output voltage at collector of Q884 will be about 5v.

- d. 5v is the minimum output voltage and is mainly determined by the current flowing in R862.
 - e. Further positive signal current causes the cathode of D861 to rise in voltage until D852 conducts.
 - g. When D852 conducts, the input current is effectively short circuited.
 - (1) The collector of Q894 will be at the maximum output voltage.
 - (2) Q894 collector voltage limits before Q894 cuts off.
 - h. The limiting operation for the opposite polarity occurs in the same fashion using D871 and D851.
 - i. The swing at each output is thereby limited at 5v and 98v (47v, +51v, -42v).
 - j. The diodes, therefore, protect the output circuit from overdrive in either direction.
9. C882 and C892 adjust the damping factor of the amplifier and thereby the high speed linearity.
10. The TRACE FINDER limits the output swing to 20v to 65v.
- a. The display will occupy the center 8 graticule divisions.
 - b. The control is a two position spring return switch.
 - (1) The rest of the switch limits the vertical drive.
 - c. When the switch "breaks", it disconnects Q884, Q894 collector supply from 150v (through R886).
 - (1) D884 connects, providing a collector current path to 75v.
 - d. When the switch "makes", it connects R887 to the 150v supply.

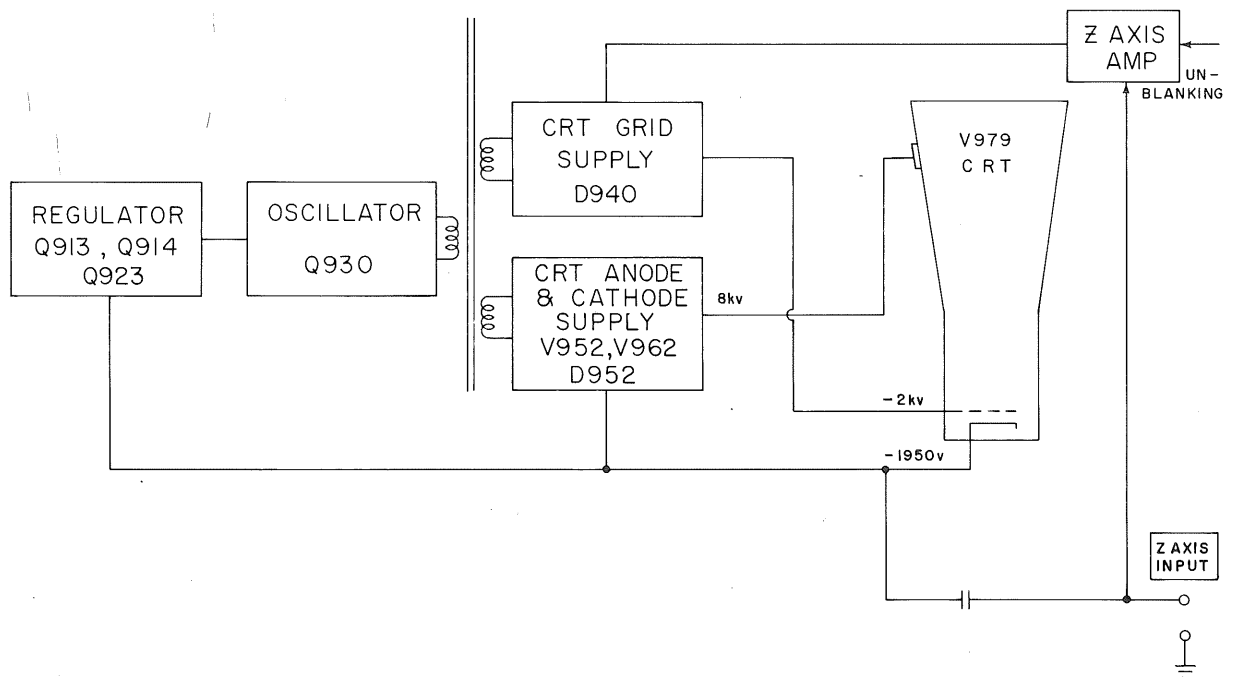
- (1) 33.3 ma is drawn from the 150v supply to make up for the loss of collector current.
- e. Mid screen collector current drops to 6.8 ma.
- f. When the trace is moved to the right, Q884 cuts off.
 - (1) Q884 collector raises to 65v, set by R884, R882.
- g. The feedback loop is broken.
- h. As the sweep ramp runs down, Q863 base can drop more rapidly without feedback.
- i. D851 conducts, limiting the rise at Q873 base.
- j. When Q873 base rise becomes limited, the output at Q894 collector limits at 20v.

XIII. CRT AND HIGH VOLTAGE CIRCUIT

- A. The circuit consists of the CRT, its associated controls and the regulated CRT anode, grid and cathode supplies.
- B. Outputs from the regulated supply:
 - 1. 8 kv for the post accelerator anode.
 - 2. -2 kv for the CRT grid.
 - 3. -1,950v for the CRT cathode.
- C. Z Axis Modulation
 - 1. DC coupled through the Z Axis Amplifier to the CRT grid.
 - 2. AC coupled to the CRT cathode.
- D. Front Panel Controls
 - 1. FOCUS.
 - 2. INTENSITY (part of Z Axis Amplifier).
- E. Adjustments
 - 1. TRACE ROTATION -- on the side panel.
 - 2. ASTIGMATISM -- on the side panel.
 - 3. GEOMETRY -- on the Z Axis Amplifier board.
 - 4. CRT GRID BIAS -- on the High Voltage board.
 - 5. HIGH VOLTAGE -- on the High Voltage Regulator board.
 - 6. Y Axis Alignment -- on the left side panel.
- F. Circuits that comprise the CRT and High Voltage Circuit:
 - 1. Oscillator, Q930.
 - 2. High Voltage Regulator; Q913, Q914, Q923.

3. CRT Anode and Cathode supply; V952, V962.
4. CRT Grid supply, D940.
5. CRT Circuit.

G. Block Diagram



TYPE 453 CRT AND HIGH VOLTAGE
BLOCK DIAGRAM

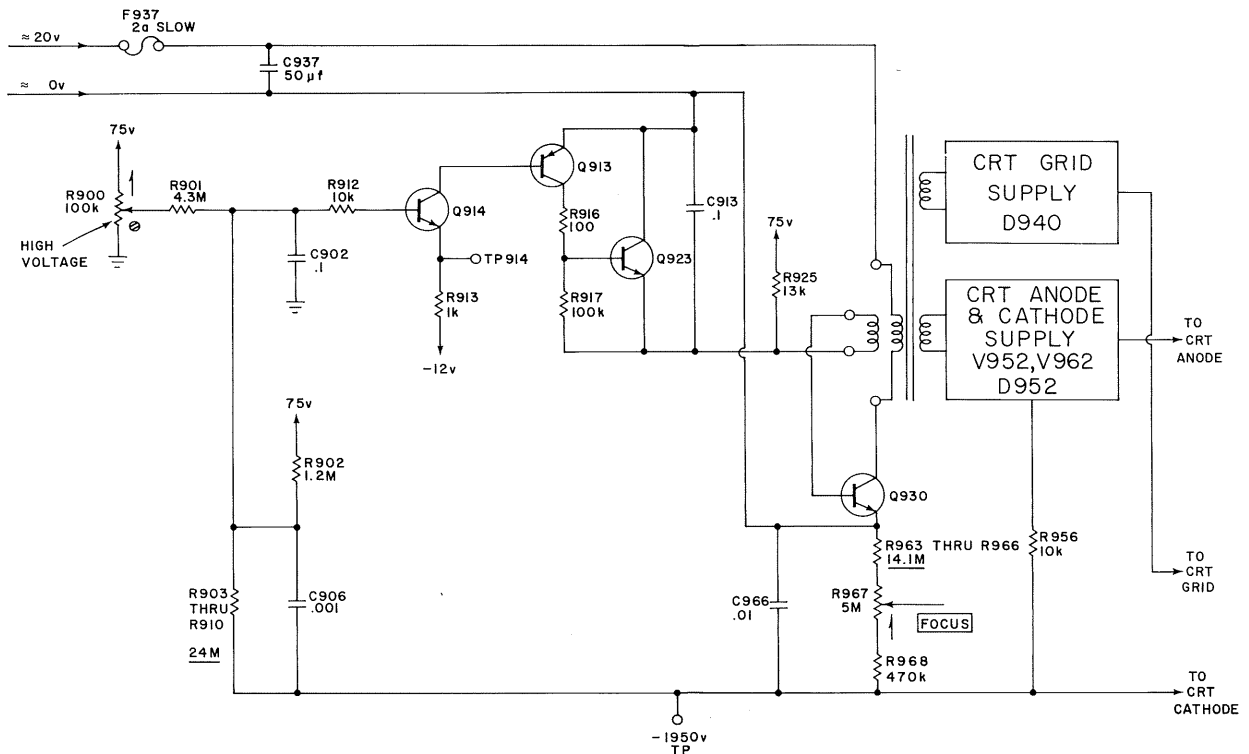
B-453-0062
8-26-'65 jg Ⓢ

H. Block Logic

1. The free running oscillator develops a 40 kc sine wave.
2. The sine wave voltage is stepped up in the HV transformer and rectified in three supplies.

- a. 8 kv supplies the CRT post acceleration anode.
 - b. -2 kv supplies the CRT grid.
 - c. -1950v supplies the CRT cathode.
3. The cathode supply output is fed back to the Regulator Circuit.
 4. The Regulator Circuit controls the voltage output from the Oscillator and thus controls the rectified voltages that supply the CRT.
 5. Unblanking pulses and Z axis information is DC coupled through the floating CRT grid supply to the CRT grid.
 - a. Unblanking information includes A Sweep and B Sweep unblanking and A Sweep Intensified By B information.
 - b. Chop blanking pulses from the Vertical Switching Multi blank the CRT during dual trace switching time.
 6. Z axis modulation is also applied (AC coupled) to the CRT cathode.
 - a. The TC is such that the cathode drive takes over when the Z axis amplifier begins to roll off.
- I. Oscillator, Q930
1. The Oscillator is an armstrong circuit operating at approximately 40 kc.
 2. Q930 is a 151-140, 2N3055 silicon NPN transistor.
 - a. The transistor is mounted on the aluminum rear sub panel.
 3. The sine wave output across T930 primary is about 22v peak-to-peak.
 - a. About 2.5v of 120 cycle ripple rides on the sine wave output.

4. Current source for the oscillator is the unregulated 20v from the 12v supply.



TYPE 453 CRT AND HIGH VOLTAGE
OSCILLATOR AND REGULATOR

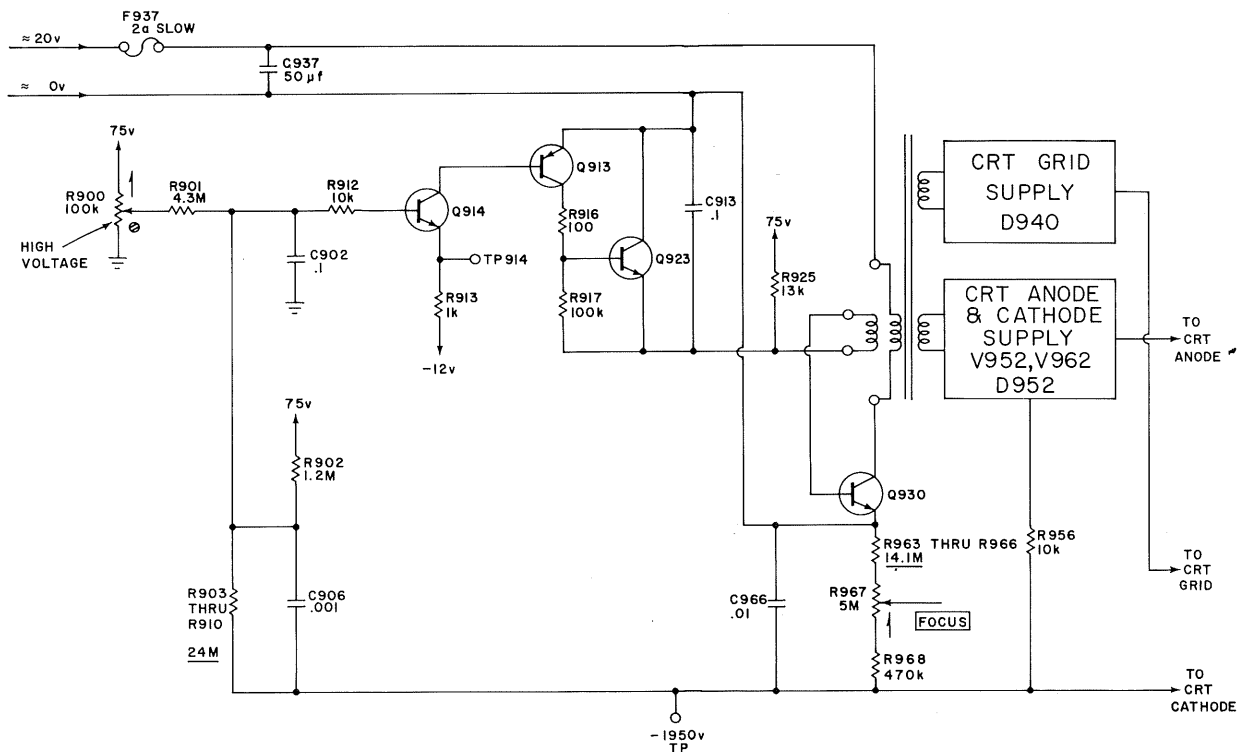
B-453-0063
8-27-65 jg

- F937, a 2a SLO BLO fuse, protects the oscillator transistor.
- About 500 ma is supplied.
- All ground returns in the CRT and High Voltage circuit return to the minus side of the 12v supply.
- The return point is isolated $.3\Omega$ from ground, thereby providing a return for the 40 kc without ground current.
- Base starting current is provided by R925 to 75v.

5. Stray C and the inductance of the transformer primary determines the oscillator frequency.
6. About 13v of sine wave is fed back to Q930 base.
 - a. Only the peak of the sine wave positive excursions cause Q930 conduction.
7. Regulator voltage, set by regulator transistor (Q923), sets the base level and regulates the 40 kc output amplitude.

J. Regulator; Q913, Q914, Q923

1. The Regulator circuit samples the output from the CRT cathode supply and biases the HV oscillator to correct for any change in voltage.
2. Q923 is a shunt regulator. Q913 and Q914 are error amplifiers.



TYPE 453 CRT AND HIGH VOLTAGE OSCILLATOR AND REGULATOR

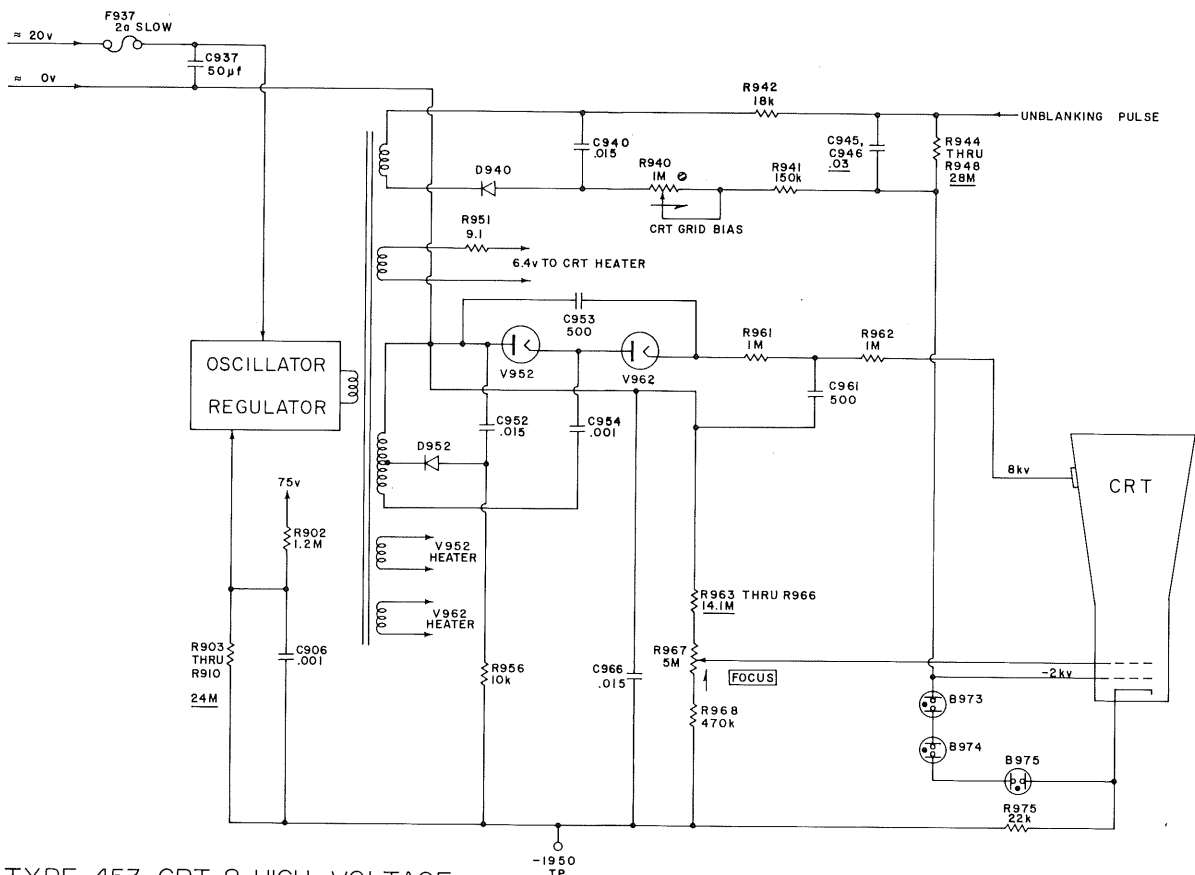
B-453-0063
8-27-65 jg

- a. Q913 is a 151-133 silicon PNP transistor.
 - b. Q914 is a 151-126 silicon NPN transistor, 2N2484.
 - c. Q923 is a 151-136 silicon NPN transistor, 2N3053.
2. Q913 and Q923 use the oscillator as a power source.
 - a. The Regulator in turn controls the oscillator bias.
 - b. Current for Q913 and Q923 is rectified by Q930 base-emitter junction and filtered by C913.
 - c. C913 is shunted by a variable resistance composed of Q923.
 - d. The resistance of Q923 determines the average charge on C913 and thus the operating bias on Q930.
 - e. The value of Q923 as a shunt resistance is controlled by the error amplifiers, Q914 and Q913.
 3. A sample of the CRT cathode supply voltage is picked off the divider, composed of resistors R520 through R510.
 - a. About 4% of the error voltage is applied to the Regulator input at Q914 base.
 - b. C906 and C902 compensates the divider.
 - c. R912 protects Q914 should a sudden positive step couple across C906.
 - (1) If the CRT cathode supply becomes shorted to ground, a 19v step would appear across R912.
 - (2) The -1950 at the bottom of the divider is divided down by the 100:1 ratio of C902, C906.
 4. Q923 emitter will average -6v, with an AC component of about 2.5v.
 5. R917 supplies Q923 base leakage current.

6. R916 limits Q913 saturation current, and R913 limits Q914 saturation current.
 - a. Neither transistor will saturate during normal operation; only if a short occurs to the HV supply.
7. The HIGH VOLTAGE control is part of the error divider.
 - a. It allows a fine adjustment of the sample of High Voltage fed back to the Regulator.
 - b. Reading at the -1950v test point, the control has a range of -1790v to -2170v.

K. High Voltage Supplies; V952, V962

1. The High Voltage Supplies provide high voltage potentials for the CRT post accelerating anode, the cathode and the grid.

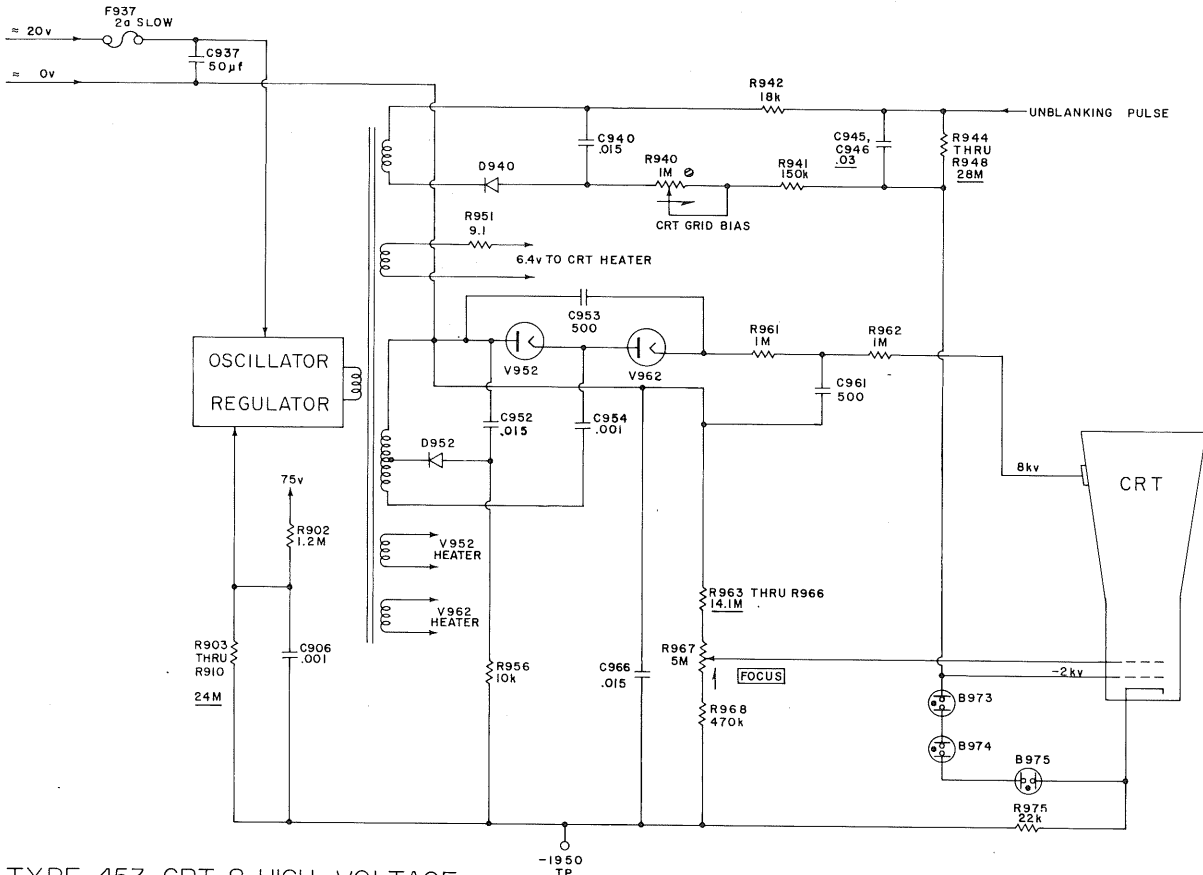


TYPE 453 CRT & HIGH VOLTAGE
HIGH VOLTAGE SUPPLY

2. The supplies use two tubes and two diodes.
 - a. V952 and V962 are 5642 rectifiers.
 - (1) The tubes have a PIV of 10,000v.
 - b. D940 and D952 are 152-192-1A rectifier diodes.
 - (1) They are Varo 7701-5X 50 ma diodes with a PIV of 5000v.
3. The TEK made high voltage transformer (T930) delivers the following secondary voltages.
 - a. CRT grid winding, 1500v RMS at 1 ma.
 - b. CRT anode winding, 2840v RMS at 80 μ a.
 - c. CRT cathode winding, 1400v RMS at 1 ma.
 - d. CRT heater winding, 7.75v RMS at 100 ma.
 - e. Two rectifier heater windings are looped through one turn windings of 1.25v each.
4. The CRT Grid supply is a variable floating supply with the plus side tied to the Z axis (and Unblanking) Amplifier.
 - a. The negative side connects directly to the CRT grid.
 - b. The simple half wave rectifier delivers -2000v to the CRT grid.
 - c. The CRT GRID BIAS control adjusts the grid supply output over a very narrow range (relative to the CRT cathode voltage), to compensate for differences in cut-off bias for different CRT's.
 - d. C940 filters the rectified output.

5. C945, C946 couple the unblanking (and Z axis) signal across the 28M bleeder string.
6. R942 and R941 isolate the unblanking information from the HV transformer capacitance.
 - a. The CRT Grid supply winding has about .001 μ f capacitance to ground.
7. C945, C946 and the 28 megohm bleeder string (R944 through R948) have a time constant of about .28 sec.
 - a. R942 and the HV transformer C have a time constant of about .018 msec.
8. The initial unblanking step will lift the CRT grid about 50v through C945, C946.
 - a. The HV transformer C will hold the left side of R942 and R941 momentarily, then allow the supply to rise along the .018 msec time constant.
 - b. Before the .28 sec T_c of C945, C946 and the bleeder string can cause the CRT grid voltage to sag, the supply (with its shorter time constant) will have established the unblanking level at the CRT grid.
 - c. The circuit constitutes DC unblanking.
9. The CRT Anode Supply uses a voltage doubler to develop the 8 kv accelerating anode potential.
10. The negative side of the supply at V952 anode is tied to the minus side of the -12v supply silicon stack.
11. The rectified output is filtered by R961, C961, R962 and CRT accelerator anode capacitance.

12. The CRT Cathode supply uses a single solid state diode as a half wave rectifier to develop the -1950 CRT cathode potential.



TYPE 453 CRT & HIGH VOLTAGE
HIGH VOLTAGE SUPPLY

B-453-0064
8-30-65jg

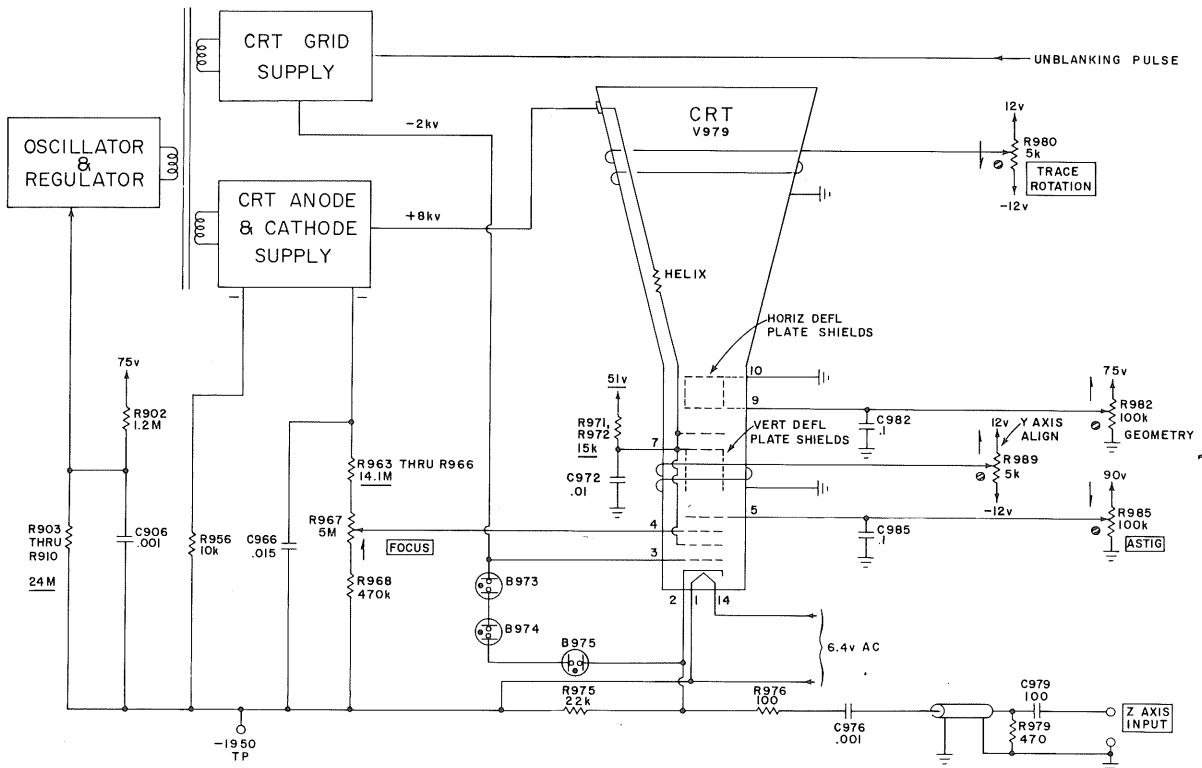
- a. The voltage may be varied from -1790v to -2170v by the HIGH VOLTAGE adj.
 - b. C952, R956 and C966 filter the rectified output.
 - c. The cathode supply bleeder string consists of R968, the FOCUS control and resistors R963 through R966, totaling 19.57 megohms.
13. The CRT heater is supplied by a 7.75v winding on the HV transformer.

- a. The winding provides regulated heater voltage .
- b. R951 drops the supply to about 6.4v RMS for use by the CRT.

14. Two loop-through single turn windings supply V952 and V962 heaters.

L. CRT Circuit, V979

- 1. The CRT is a T4530 aluminized 3-3/8 x 3-7/8 inch rectangular flat-faced cathode ray tube that features electrostatic focus and deflection, a mesh shielded helical post accelerator and a low power cathode .



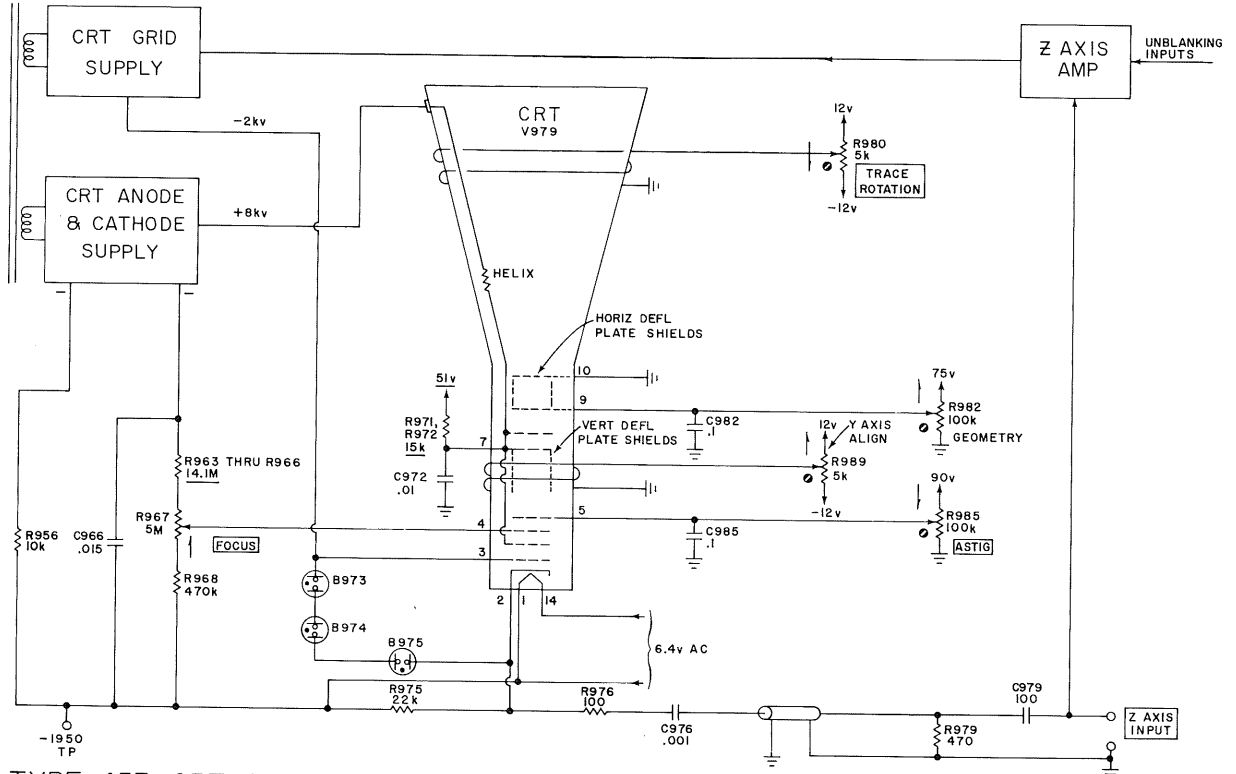
TYPE 453 CRT & HIGH VOLTAGE CRT CIRCUIT

B-453-0065
9-1-65jg 40

- a. Display area is 3-3/16 inches wide by 2 inches high --
6 x 10 divisions.
- b. The tube is available with or without a lighted internal
graticule.
- c. The CRT has a P31 phosphor as standard.
2. Total accelerating potential is 10 kv (CRT rating is 12.5 kv
maximum).
 - a. Post accelerating anode is 8 kv and the cathode is -1950v.
3. Intensity is controlled through the Z Axis (and Unblanking) Amplifier
by changing grid bias.
4. The FOCUS control is part of the cathode bleeder resistor string.
 - a. Focus electrode voltage is spec'd at 150v to 450v with
respect to the cathode.
5. Post accelerator helix resistance may vary from 200M to 4000M
in different CRT's.
6. The GEOMETRY control is connected to the Horizontal Deflection
Plate shield.
 - a. The control has a range from 1950v to 2025v with respect
to the cathode.
7. The ASTIGMATISM control has a range from 1950v to 2040v.
8. The Vertical Deflection Plate shields have a fixed voltage 2000v
from the cathode.
9. The post accelerator grid ties to ground which places it 1950v
from the cathode.

10. The TRACE ROTATION control has a range of $\pm 6^\circ$.
 - a. The control is tied between +12v and -12v.
 - b. The trace rotation coil is connected between the control arm and ground.
 - c. The control can select either plus or minus current to flow through the TRACE ROTATION coil.
11. The Y AXIS ALIGNMENT control corrects for a Y axis misalignment caused by TRACE ROTATION.
 - a. The TRACE ROTATION field does not exert equal correction to both axes of the CRT display.
 - b. The Y AXIS ALIGNMENT control corrects for the misalignment by adjusting only the Y axis.
12. The grid has its own regulated -2000v supply.
 - a. Typical grid voltage relative to cathode is -75v to -105v.
 - b. The grid bias is adjustable by the CRT GRID BIAS control.
 - c. The DC coupled unblanking waveform of up to 60v peak-to-peak (depending on the INTENSITY control setting) is added to the grid bias during sweep.
 - d. DC coupled Z axis modulation drives the grid through the Z Axis Amplifier.
 - e. Three neons between the grid and cathode protect the CRT if the grid supply should fail, or if (on initial turn on) the grid and cathode supplies do not come up to voltage simultaneously.
13. The cathode has its own -1950v supply.
 - a. Z Axis modulation may be applied to the cathode.

14. The CRT heater is elevated to -1950v (the cathode potential) to prevent cathode-heater breakdown.



TYPE 453 CRT & HIGH VOLTAGE
Z AXIS INPUT

B-453-0065.1
9-21-'65dl

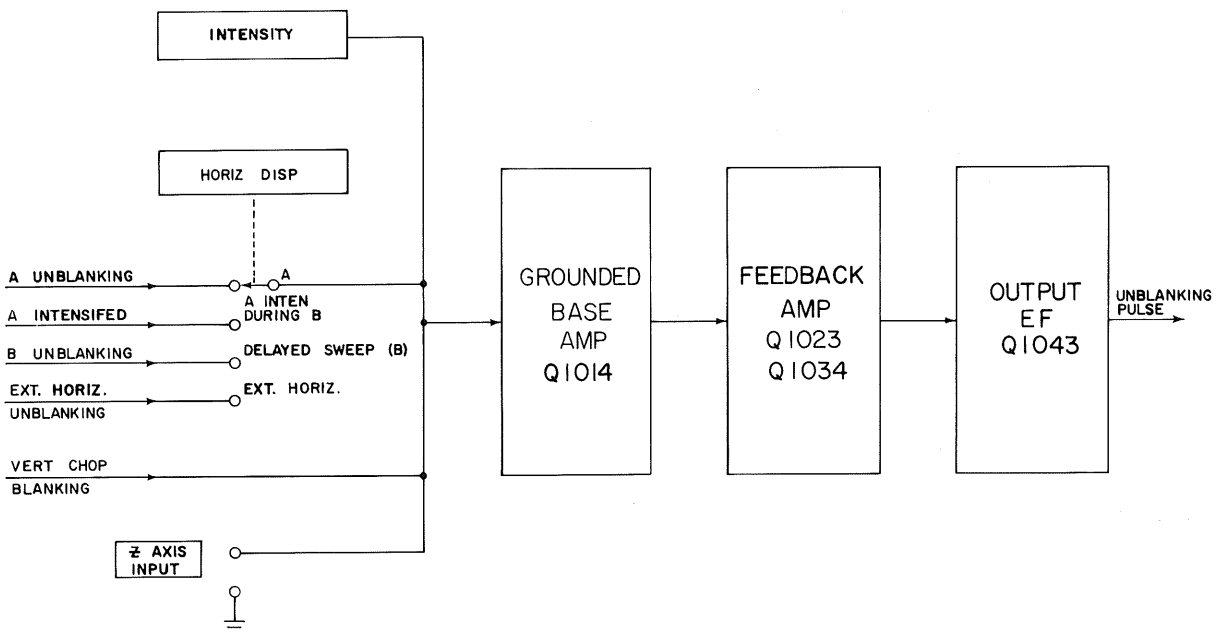
15. AC coupled high frequency Z axis signals may be applied to the cathode.
- When a signal is applied to the Z AXIS INPUT jack, it is amplified (DC coupled) and inverted in the Z Axis Amplifier.
 - The DC coupled Z axis signal drives the CRT grid.
 - Bandpass of the Z Axis Amplifier rolls off at about 4.5 mc.

- d. At this frequency, the signal couples through C979 to drive the CRT cathode.
- e. Bandpass of the Z Axis Input, therefore, is 0 to >50 mc with a crossover to the cathode drive at 4.5 mc.
- f. C976 is a blocking cap, keeping the -1950v cathode potential off the crossover network (C979, R979).
- g. R975 allows the cathode to respond to Z axis signals without the loading effects of C966.
- h. Z AXIS INPUT is limited to ± 200 v, combined DC plus peak AC.
- i. A 5v peak-to-peak Z axis signal will usually cause adequate intensity modulation.
- j. Input resistance is ≈ 47 k for DC inputs.

XIV. Z AXIS AMPLIFIER

A. The Z Axis Amplifier mixes the various signals that Z axis modulate the CRT and after amplification applies them to the CRT grid.

B. Block Diagram



TYPE 453 Z AXIS AMPLIFIER
BLOCK DIAGRAM

B-453-0066
8-31-65 bja

C. Circuits that constitute the Z Axis Amplifier:

1. Input Switching (HORIZ DISPLAY switch).
2. Grounded Base Amplifier, Q1014.
3. Feedback Amplifier; Q1023, Q1034.
4. Output EF, Q1043.

D. Inputs

1. A Unblanking pulse from the A Sweep Generator.
 - a. A negative going 2 ma current pulse, the same duration as A Sweep.
 - b. From 2 ma prior to sweep to 0 ma during sweep.
2. B Unblanking pulse from the B Sweep Generator, for the duration of B Sweep.
 - a. A negative going 2 ma current pulse.
3. A Intensified pulse from the B Sweep Generator, the same duration as the B Sweep.
 - a. Negative going current pulse.
 - b. .12 ma prior to B Sweep, -.15 ma during B Sweep.
4. External Horizontal Unblanking
 - a. 1 ma is drawn from the Z Axis input when the HORIZ DISPLAY switch is in the EXT HORIZ position.
5. Vertical Chop Blanking pulse from the Vertical Switching Multi.
 - a. A 2 ma positive going current pulse of about .25 μ sec duration.
 - b. The pulse is present whenever the Vertical Switching Multi switches in CHOP mode.
6. Z AXIS INPUT from a rear panel banana jack.
 - a. A 5v signal applied to the jack will cause a noticeable change in intensity at normal INTENSITY settings.
 - b. A positive going signal will dim the trace.

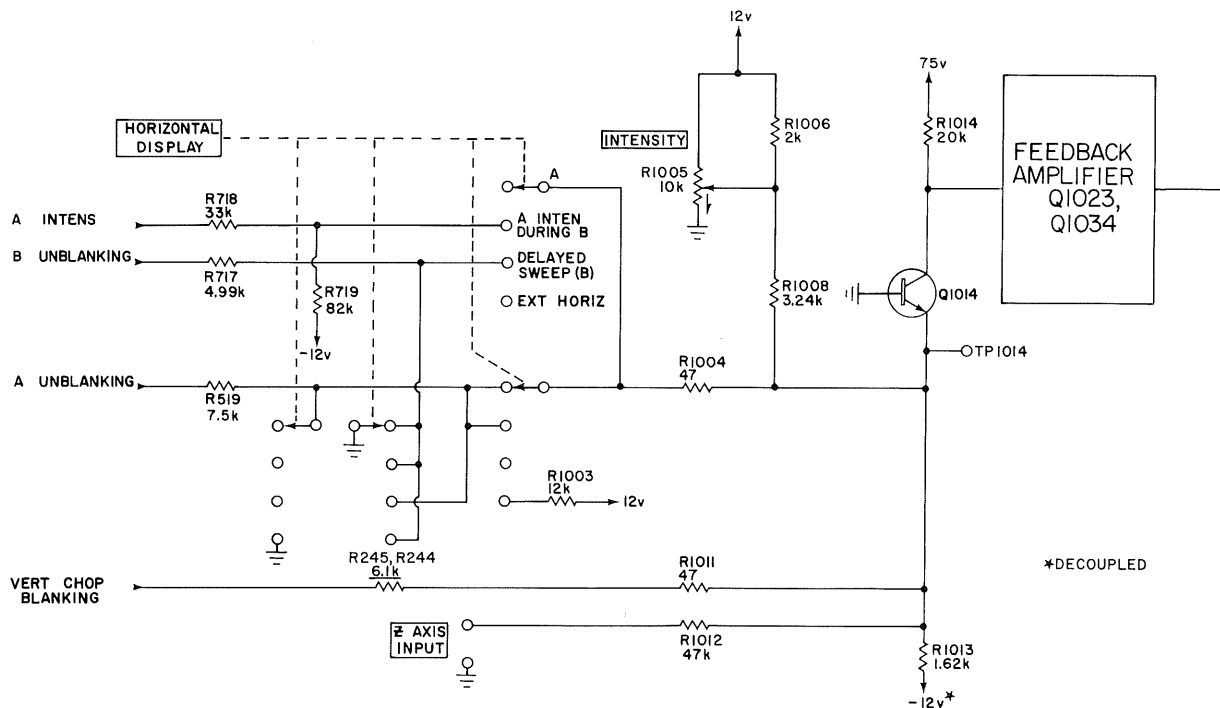
E. Output

1. The Z Axis Amplifier output drives the CRT grid.
 - a. The output can swing from 10 volts to normal unblanking level of 60v.
 - b. High INTENSITY settings can swing the output to 90v during Unblanking.

F. Block Analysis

1. The various inputs and the INTENSITY control vary the current into the Grounded Base Amplifier.
2. The Grounded Base Amplifier drives the Feedback Amplifier; a gain stage with a voltage output.
3. The Output EF provides a low impedance drive to the CRT grid.

G. Grounded Base Amplifier and Input Switching, Q1014

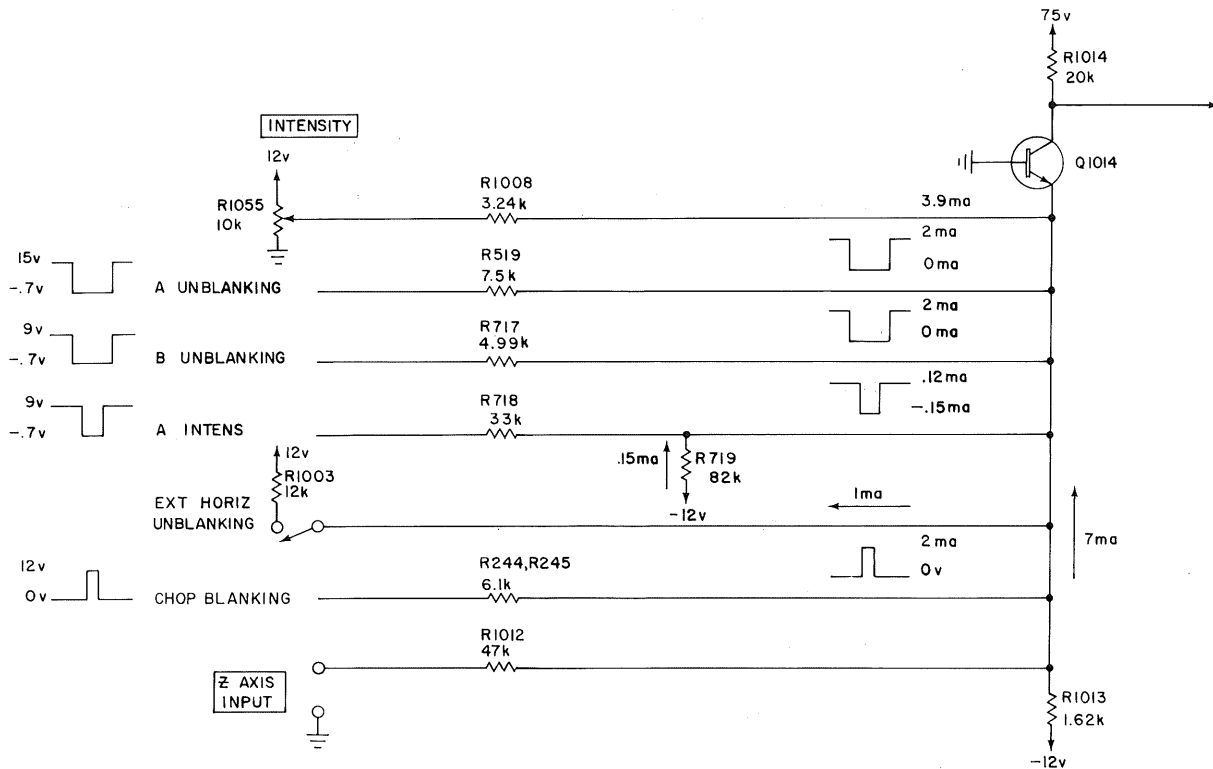


TYPE 453 Z AXIS AMPLIFIER
INPUT AND GROUNDED BASE AMP.

B-453-0067
9-2-65 bja

1. Three of the Inputs to the Grounded Base Amplifier are selected by the HORIZ DISPLAY switch.
 - a. In the A position, the A Unblanking pulse is selected.
 - b. In the A INTEN DURING B position, both the A Unblanking pulse and the A INTENS DURING B Unblanking pulse are connected.
 - c. In the DELAYED SWEEP (B) position, the B Unblanking pulse is selected.
 - d. In the EXT HORIZ position, a connection is made through 12k (R1003 to +12v).
 - e. The sweep inputs are grounded when not in use.
2. Three of the inputs are not selected by the HORIZ DISPLAY switch -- they are permanently connected.
 - a. The INTENSITY control can be considered an input.
 - b. The Vertical Chop Blanking connection is permanent, but the pulses are present only in the CHOP mode of the Vertical Switching Multi.
 - c. The Z AXIS INPUT is permanently connected to the rear panel jack.
3. About 7 ma flows through R1013.
 - a. Part of this current is diverted from Q1014 emitter to reduce the intensity of the CRT beam.
 - b. Up to 3.9 ma will flow through R1008 and the INTENSITY control (in its CCW position) to completely cut off the trace.
 - (1) The Z Axis Amplifier output is about 10v.

4. As the INTENSITY control is advanced (and less current flows through R1008), the beam begins to become visible.



TYPE 453 Z AXIS AMPLIFIER
INPUT CURRENTS*

B-453-0068
9-1-65 bja

- a. As less current flows through R1008, more current can flow through Q1014.
 - b. About 4.5 ma through Q1014 will show a dim trace.
5. When the HORIZ DISPLAY switch is in its A position and no sweep is present, 2 ma flows through R519.
 - a. The voltage level (at the left of R519) is at 15v.

* The illustration shows current during blanking and unblanking with no regard for switch positions.

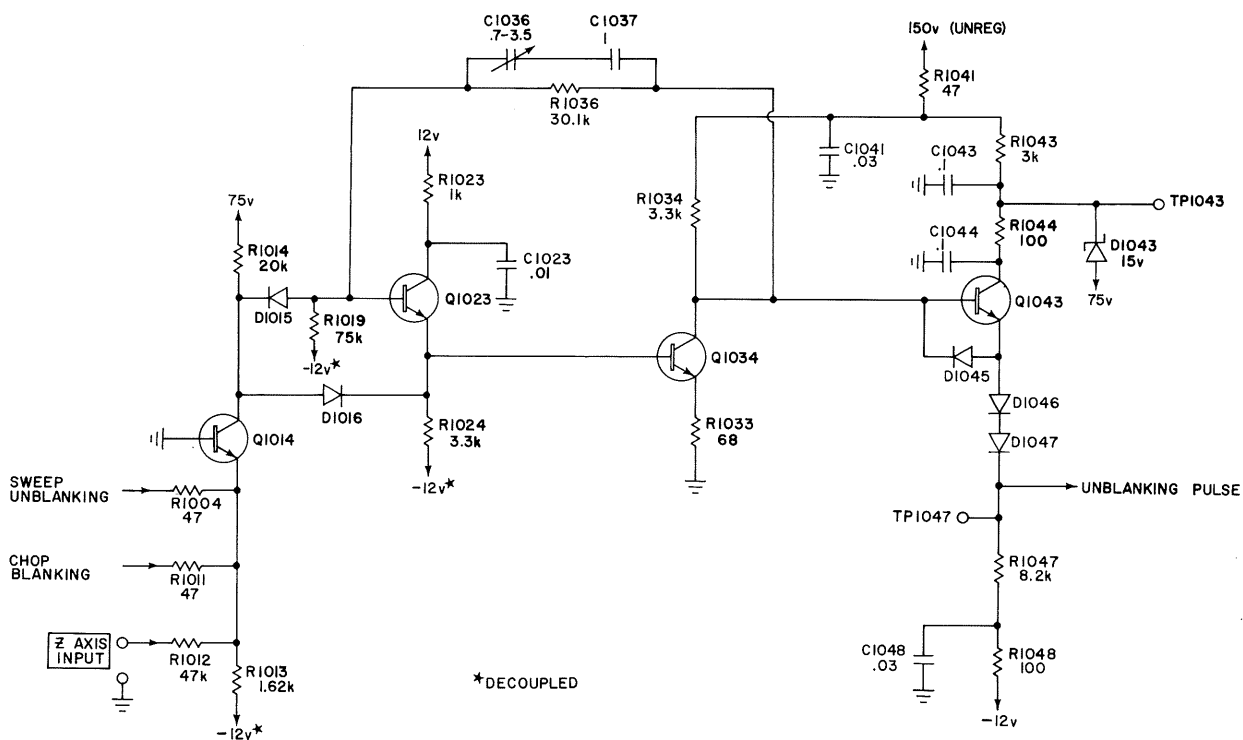
- b. If current through R1008 plus current through R519 has reduced the current through Q1014 to less than 4.5 ma, the CRT will be blanked.
 - c. The Z Axis output will be at 15v or less.
6. When sweep starts, current through R519 stops.
- a. The Unblanking Voltage pulse (at the left of R519) drops to $-.7v$.
 - b. Current through Q1014 increases by 2 ma.
 - c. The CRT is unblanked.
 - d. The Z Axis output will rise to approximately 60v.
7. In the DELAYED SWEEP position of the HORIZ DISPLAY switch prior to sweep, 2 ma flows through R717.
- a. The voltage level to the left of R717 is about 9v.
 - b. The CRT is blanked.
8. When sweep starts, current through R717 stops.
- a. The CRT is unblanked.
9. In the A INTENS DURING B position of the HORIZ DISPLAY switch, prior to sweep, 2 ma flows through R519 and .12 ma flows through R719 to Q1014.
- a. .15 ma flows through R719 and .27 ma flows through R718.
 - (1) The difference, .12 ma, flows from R1013.
 - b. The 2.12 ma, in addition to that flowing through the INTENSITY control, robs Q1014 of enough current to blank the CRT slightly more than in the A Display modes.

- c. When A Sweep starts (but not B), the current through R519 stops but the .12 ma through R719 still flows.
 - d. The trace is unblanked but somewhat dimmer than in the A mode.
 - e. When B Sweep starts, the current through R718 stops.
 - f. The .15 ma through R719 now flows to Q1014 (adding to that flowing from R1013) to intensify the trace.
10. In the EXT HORIZ mode of the HORIZ DISPLAY switch, all sweep inputs are disconnected.
- a. R1003 is connected to 12v.
 - b. 1 ma flows through R1003.
 - c. Unblanking current, therefore, is halfway between the blanked and unblanked current values established in the A mode.
 - d. The INTENSITY control must be advanced to obtain a visible spot.
11. The CHOP Blanking pulse robs Q1014 of 2 ma for the pulse duration.
- a. The 2 ma blanks the CRT to the same level as A mode blanking level.
 - b. The pulse is about .25 μ sec wide.
12. A positive signal is required at the Z AXIS INPUT jack to dim the trace.
- a. About 100v is required to provide the 2 ma blanking current used by the CHOP Blanking pulse.
 - b. 5v is usually adequate, however, to cause a noticeable dimming of the trace.

- 13. The Grounded Base Amplifier, Q1014, is a 151-108, 2N2501 silicon NPN transistor.
- 14. Although the Z Axis and Unblanking signals drive into the low impedance emitter of Q1014, there is about 1.5v of CHOP Blanking signal kick-back out the Z AXIS INPUT jack.
- 15. Q1014 provides a current drive to the Feedback Amplifier.

H. Feedback Amplifier and Output EF; Q1023, Q1034, Q1043

- 1. The Feedback Amplifier is the gain stage and Q1043 provides the low impedance drive to the CRT grid.



TYPE 453 Z AXIS AMPLIFIER
 FEEDBACK AMPLIFIER AND OUTPUT E.F.

B-453-0069
 9-3-65 bja

2. The circuits use three transistors, five signal diodes and a zener diode.
 - a. Q1023 is a 151-108, 2N2501 silicon NPN transistor.
 - b. Q1034 and Q1043 are 151-124, TA1938 silicon NPN transistors.
 - (1) Q1034 is mounted on a beryllium oxide heat sink on the rear sub panel.
 - c. D1015, D1016 and D1045 are 152-185, 1N3605 silicon diodes.
 - d. D1046 and D1047 are 152-002, 1N1329 silicon diodes.
 - e. D1043 is a 1N3024A, 15v, 10% zener diode.
3. The Feedback Amplifier is current driven by Q1014.
 - a. The amplifier has a transimpedance of about 30k.
4. D1015 cuts off if Q1014 is overdriven, allowing Q1014 collector to rise above 4.2v.
 - a. If D1015 was not allowed to disconnect, Q1034 would become saturated.
5. D1016 protects Q1014 from base-collector breakdown when D1015 disconnects.
 - a. Q1014 collector rise is clamped by D1016 at 4.4v.
6. C1036 and C1037, in the feedback path, help the Feedback Amplifier maintain constant gain at higher frequencies.
7. Q1034 collector is supplied by 150v unregulated.
 - a. The unblanking level will vary about 1 volt from low to high line.
 - b. The supply is decoupled by R1041, C1041.

8. The output EF, Q1043, is voltage driven by the Feedback Amplifier.
 - a. The collector supply is zener offset by D1043 to 90v.
 - b. The 90v supply is also used at the CRT ASTIG control.
 - c. C1044, R1044 decoupled the supply.
9. A fast negative step at Q1043 base could cut off the transistor.
 - a. In this case, D1045 would connect, coupling the fast negative step to the emitter.
10. D1046 and D1047 protect the amplifier from a large positive step (at TP1047) should the CRT grid become shorted to ground.
 - a. D1046 and D1047 are high capacitance diodes.
 - b. The diode capacitance drives the CRT supply capacitance preventing the diodes from disconnecting on fast negative steps.
11. Q1043 emitter supply is decoupled by R1048, C1048.

XV. LOW VOLTAGE POWER SUPPLY

A. The Low Voltage Power Supply provides three regulated voltage sources and one unregulated supply.

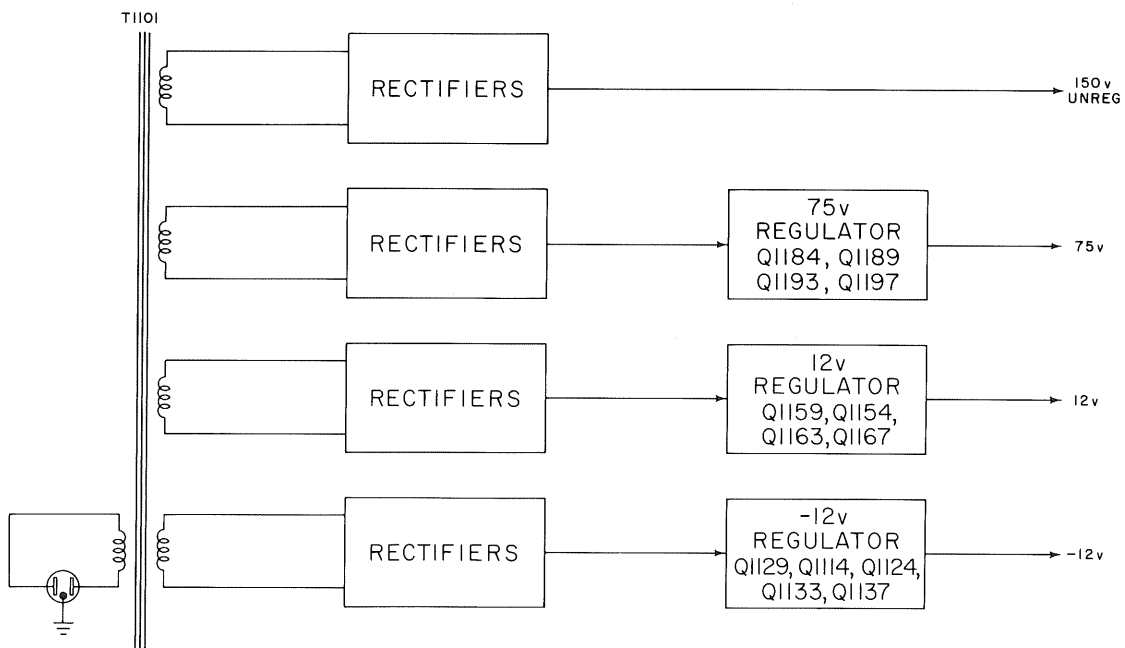
1. Regulated Supplies:

- a. -12v.
- b. +12v.
- c. +75v.

2. Unregulated Supply

- a. +150v.

B. Block Diagram



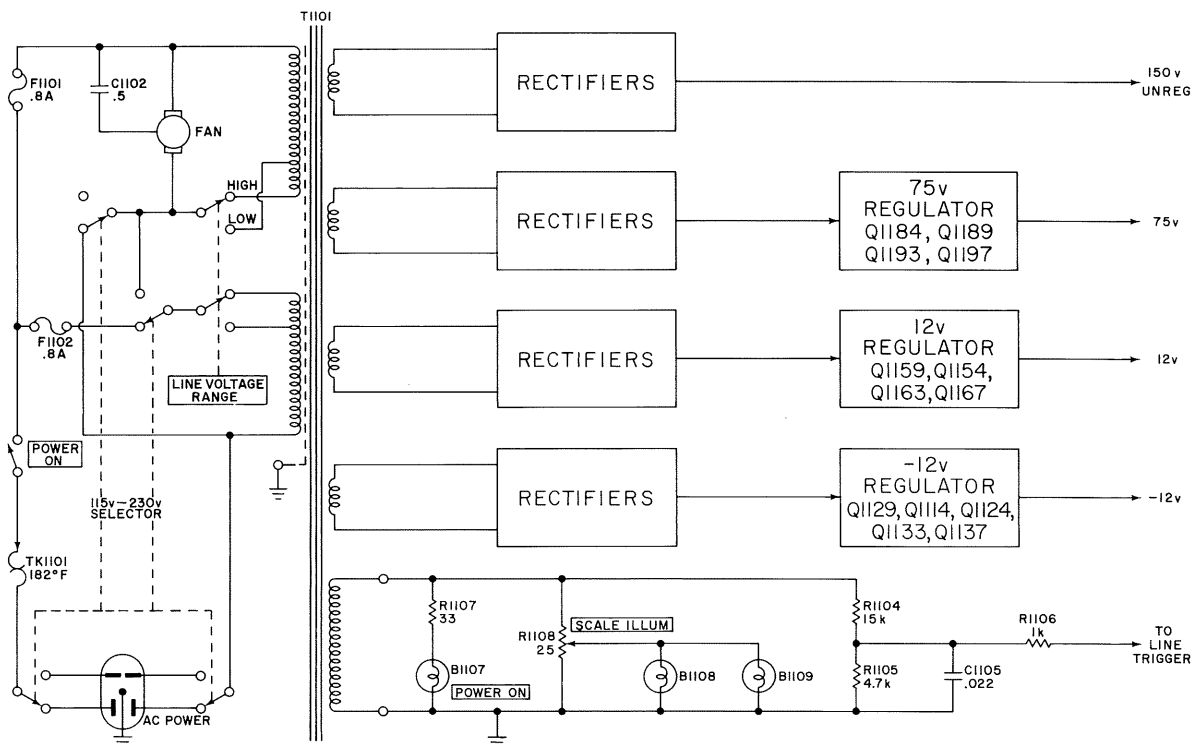
TYPE 453 POWER SUPPLY
BLOCK DIAGRAM

B-453-0070
9-3-'65 mw

C. Block Logic

1. The -12v supply has a zener reference.
2. The +12v and +75v supplies use the -12v supply as reference.
3. The 150v unregulated supply is stacked on the 75v supply.

D. Power Transformer Circuit



TYPE 453 POWER SUPPLY
TRANSFORMER CIRCUIT

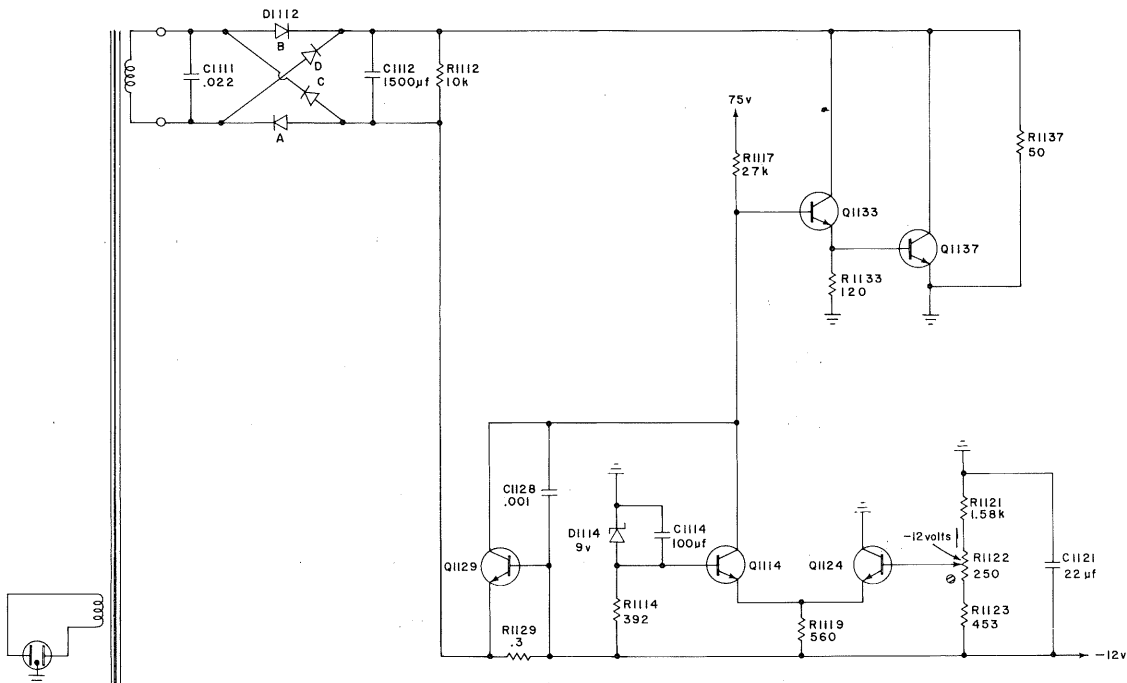
B-453-0071
9-8-'65 mw

1. Only one 6.3v AC supply is provided.
 - a. The POWER indicator light, the SCALE ILLUM lights and the LINE Trigger are supplied from the 6.3v winding.
 - b. The nuvistor heaters use DC from the regulated supplies.

2. Two detachable three wire power cords are supplied.
 - a. One for 115v and one for 230v.
 - b. When plugged into the scope, the power cord plugs are indexed to activate the 115v-230v SELECTOR switch.
3. Two primary windings are used.
 - a. In the 115v position of the SELECTOR switch, the primary windings are connected in parallel.
 - (1) Each primary is protected with a .8a SLO BLO fuse.
 - b. In the 230v position, the windings are connected in series.
 - (1) Just one .8a SLO BLO fuse is used.
3. The POWER SWITCH opens one side of the line.
4. TK1101, a thermal cut-out, opens one side of the line if the ambient temperature exceeds 182°F.
5. A LINE VOLTAGE RANGE switch, on the rear panel selects either HIGH LINE or LOW LINE.
 - a. In the LOW LINE position, the scope will regulate from 96v to 127v AC with the 115v power cord connected.
 - b. In LOW LINE, 230v operation, the scope will regulate from 192v to 254v AC.
 - c. HIGH LINE, 115v operation, regulates from 103v to 137v.
 - d. HIGH LINE, 230v operation, regulates from 206v to 274v.
6. Line frequency ranges from 45 cycles to 440 cycles.
7. About 100 watts are consumed at 115v AC, 60 cps.
8. The TEK made power transformer is not mounted in the usual case.
 - a. A weight, cost and space saving is made.
 - b. A grounded, mu metal shield surrounds the center section.

- 9. The POWER indicator light is a front panel mounted (behind a removable green jewel) incandescent light.
 - a. A GE 685 bulb is used; a 5v, 50 ma device with a life expectancy of 100,000 hours.
- 10. The two SCALE ILLUM lights are CN8-398 bulbs.
 - a. The lights can be completely extinguished by a CCW rotation of R1108.
- 11. Four sets of silicon rectifiers supply the three regulators and one unregulated supply.

- E. -12v Regulated Supply; Q1114, Q1124, Q1129, Q1133, Q1137
 - 1. The -12v supply is a transistorized regulated supply, fed by a full wave silicon bridge rectifier.

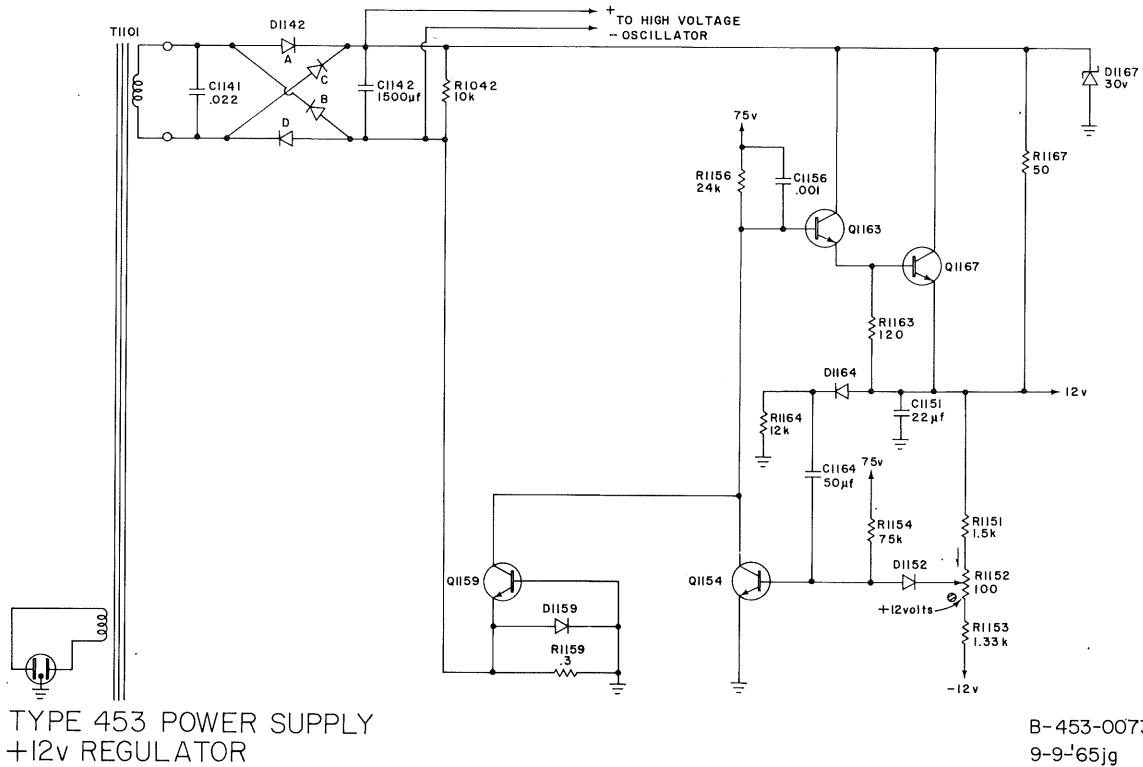


TYPE 453 POWER SUPPLY
-12v REGULATOR

2. The regulated supply delivers about 700 ma.
3. The circuit consists of five transistors, four silicon rectifiers and a zener diode.
 - a. Q1114 and Q1124 are 151-151 silicon NPN transistors, selected from 2N930.
 - b. Q1129 and Q1133 are 151-136, 2N3053 silicon NPN transistors.
 - c. Q1137 is a 151-140, 2N3055 silicon NPN transistor.
 - d. D1112A, B, C and D are MR1032A, 3 amp silicon rectifier diodes with a PIV of 200v.
 - e. D1114 is a 1N936, 9v 5% zener.
4. The full wave silicon bridge supplies about 18 volts.
 - a. C1111 reduces silicon switching transients.
 - b. C1112 filters the rectifier output.
5. Q1114 and Q1124 form a comparator.
 - a. A sample of the -12v output is taken from the error divider composed of R1121, R1122 and R1123.
 - b. The error signal at Q1124 base is compared with the zener reference voltage at Q1114 base.
 - (1) C1114 filters zener noise.
6. Q1133 is a current amplifier and Q1137, the series regulator.
 - a. The comparator output is taken across Q1114 collector load resistor, R1117.
 - b. Q1133 provides a current drive to the regulator.
 - c. Shunt resistor, R1137, supplies about 120 ma to the load.

7. Overload protection .
 - a. Q1129 provides overload or short protection .
 - b. Load current from the -12v supply flows through R1129.
 - c. If an overload increases the current to 2a, Q1129 turns on .
 - d. Q1129 collector current through R1117 drops Q1133 base .
 - e. Q1133 and Q1137 are biased to deliver less current to the load .
 - f. The system will deliver no more than a safe 2 amps .
 8. C1128 and the output cap, C1121, prevent the regulator from oscillating .
 9. Dynamic output impedance is about $.1\Omega$.
 10. The Supply may be adjusted to -12v by R1122 (located on the Regulator board) .
 - a. Long term drift is spec'd at $\pm 1\%$.
 - b. Ripple is ≤ 2 mv .
- F. +12v Supply; Q1154, Q1159, Q1163, Q1167
1. The +12v Supply is a transistorized regulated supply fed by a full wave silicon bridge rectifier .
 2. The regulated supply delivers about 600 ma .
 3. The circuit uses four transistors, four silicon rectifiers, three signal diodes and a zener diode .
 - a. Q1154 is a 151-151 silicon NPN transistor, selected from 2N930 .
 - b. Q1159 and Q1163 are 151-136 silicon NPN, 2N3053 transistors .

c. Q1167 is a 151-140 silicon NPN, 2N3055 transistor.



- d. D1142A, B, C and D are 152-198, MR10033A silicon rectifier diodes.
- e. D1152, D1159 and D1164 are 1N3605 silicon signal diodes.
- f. D1167 is a 1N972, 30v 10% zener.
4. The silicon bridge develops about 19v.
- a. The unregulated DC supplies the High Voltage circuit.
- (1) About 500 ma is used by the HV Supply.

5. Q1154 is an error amplifier.
 - a. A sample of the 12v output is taken from the error divider composed of R1151, R1152 and R1153.
 - b. The error signal, amplified and inverted in Q1154, is applied to Q1163 base.
6. Q1163 is a current amplifier and Q1167 the series regulator.
 - a. Shunt resistor, R1167, supplies about 130 ma of the total 600 ma delivered to the load.
7. D1152 temperature compensates Q1154 base-emitter junction.
8. C1164 couples ripple across the error divider to drive Q1154 base.
9. Overload protection:
 - a. Q1159 conducts if load current through R1159 exceeds 2 amps.
 - b. Q1159 biases Q1163 and Q1167, limiting the load current to a safe 2 amps.
 - c. If the +12v output is shorted to ground, D1164 disconnects, thereby protecting Q1164 base-emitter junction.
 - (1) Without D1164, a negative step would couple across C1164 to Q1154 base.
 - (2) R1164 provides keep-alive current for D1164.
10. Protection from shorts in the High Voltage supply.
 - a. If a short occurs in the CRT cathode supply, a large voltage surge will lift the 12v supply.
 - b. D1159 conducts, protecting Q1159 base-emitter junction.

c. D1167 protects Q1167.

(1) The initial voltage surge would be limited at 30v by D1167.

(2) The surge can damage Q1167 before D1159 can turn on.

11. Dynamic output impedance is about $.1\Omega$.

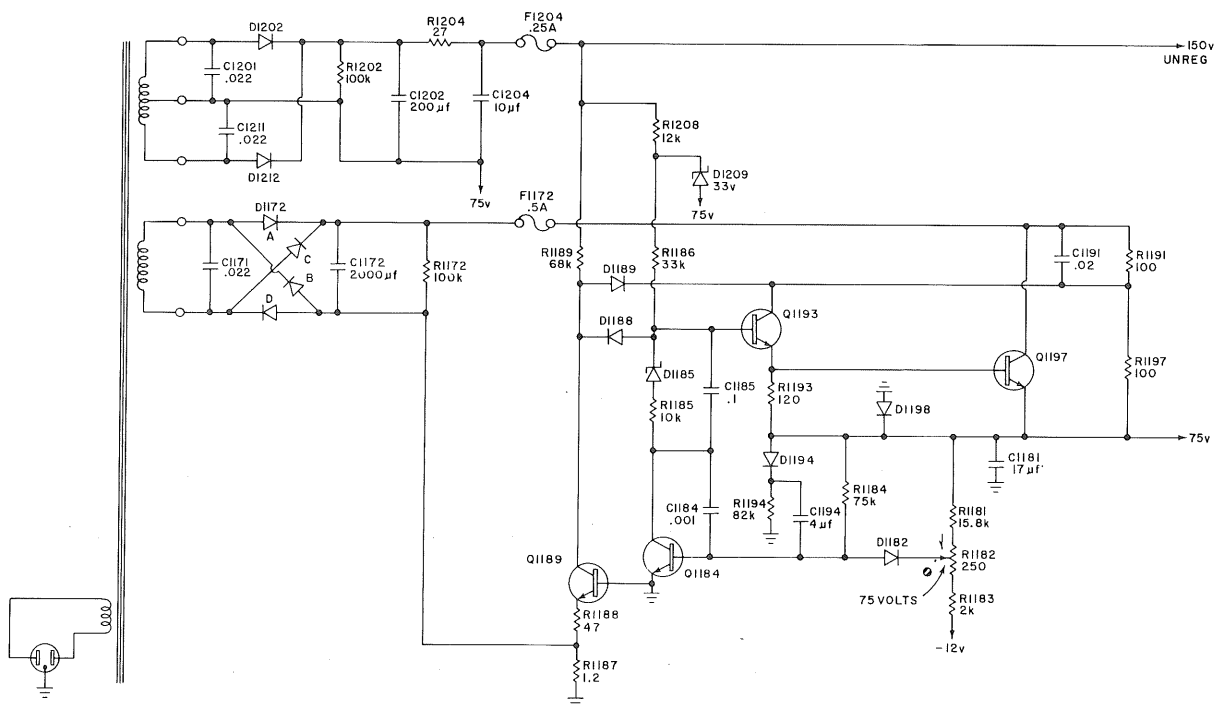
12. The supply may be adjusted to +12v by R1152 (located on the regulator board).

a. Long term drift spec is $\pm 1.7\%$.

b. Ripple is ≤ 2 mv.

G. +75 (and 150v) Supply; Q1184, Q1189 Q1193, Q1197

1. The 75v Supply is a transistorized regulated supply fed by a full wave silicon bridge rectifier.



TYPE 453 POWER SUPPLY
75v REGULATOR

2. The regulated supply delivers about 350 ma.
3. Four transistors, four rectifier diodes, five signal diodes and two zeners are used in the 75v Supply.
 - a. Q1184 is a 151-151 silicon NPN transistor selected from 2N930.
 - b. Q1189 is a 151-096 silicon NPN transistor selected from 2N1893.
 - c. Q1193 is a 151-136 silicon NPN, 2N3053 transistor.
 - d. Q1197 is a 151-149, 2N3441 silicon NPN transistor.
 - e. D1172A, B, C and D are 152-066, 1N3194 silicon rectifier diodes.
 - f. D1182, D1188, D1189 and D1194 are 1N3605 silicon diodes.
 - g. D1198 is a 1N3194 silicon diode.
 - h. D1185 is a 1N3037B, 51v, 5% zener.
 - i. D1209 is a 1N3032, 33v, 20% zener.
4. The silicon bridge develops 102v.
5. Q1184 is the error amplifier.
 - a. D1182 temperature compensates Q1184 base-emitter junction.
6. Q1193 is a current amplifier and Q1197 is the series regulator.
 - a. D1185 provides a DC offset to place Q1193 at a compatible DC level.
 - b. Q1184 collector is supplied from the 150v unregulated bus.

- (1) D1209 tied to the 75v regulated output sets the collector supply at a regulated 108v.
 - c. The shunt resistors, R1191, R1197, supply 135 ma of the total 350 ma output from the regulated supply.
 - (1) The junction of the two resistors provides the proper voltage for Q1193 collector.
9. Overload protection:
 - a. Q1189 conducts when the load on the 75v supply reaches .5 amps.
 - (1) As Q1189 collector drops, D1189 cuts off and D1188 conducts biasing Q1193 and Q1197 to a safe .5a output.
 - (2) D1189 limits Q1189 collector rise to 88v when the transistor is cut off.
 - b. If the 75v supply shorts, D1194 cuts off, thereby protecting Q1184 base-emitter junction.
 - c. If the 150v supply shorts, D1198 connects preventing the 75v supply from dropping below ground.
 - (1) A negative 150v step couples through C1204 to drive the 75v output bus below ground.
10. F1172 (.5a Fast Blow) protects the supply.
 - a. Even though Q1189 protects the regulator transistors from overload, a short at the 75v output would draw .5a from the rectifiers through the shunt resistors, R1191, R1197.
11. The 150v is stacked on the 75v supply.
 - a. The full wave rectifier supplies 75v.

- b. D1202 and D1212 are 1N3194 silicon diodes.
 - c. The supply delivers about 100 ma.
 - d. The 150v bus will vary from 138v at low line to 162v at high line.
12. F1204 (.25a Fast Blow) protects the 150v supply.

XVI. CALIBRATOR

A. The Calibrator supplies a 1 kc square wave to a front panel BNC jack.

1. A slide switch on the side panel selects the .1v and 1v levels.

2. Calibrator specifications:

a. Repetition rate 1 kc \pm .5% from 0°C to +40°C and \pm 1% from -15°C to +55°C.

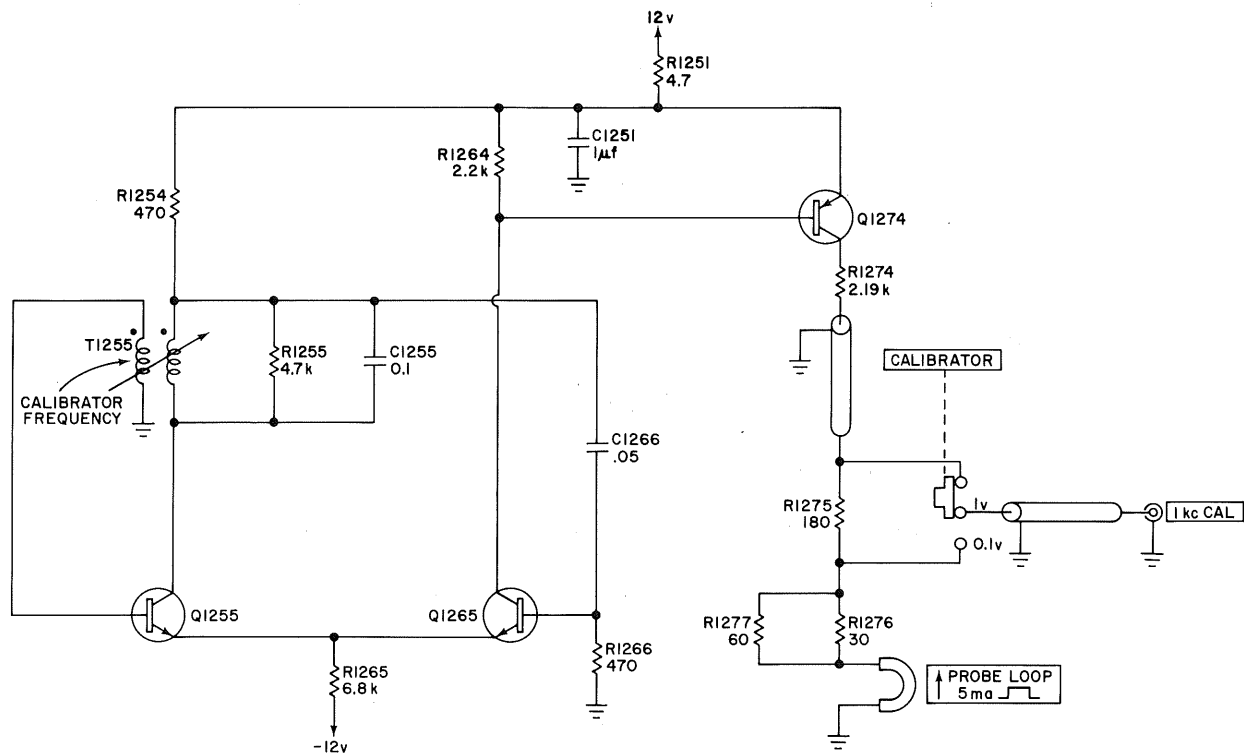
b. Voltage output \pm 1% from 0°C to 40°C and \pm 1.5% from -15°C to 55°C.

c. Duty cycle, 49% to 51%.

d. Risetime, \leq 1 μ sec.

e. Output Z, \approx 200 Ω in the 1v position; \approx 20 Ω in the .1v position.

f. Current loop, 5 ma \pm 1% from 0°C to 40°C and \pm 1.5% from -15°C to 55°C.



TYPE 453 CALIBRATOR

B-453-0075

9-10-'65 mw

B. Oscillator; Q1255, Q1265

1. Q1255 and Q1265 form an oscillator-multivibrator that free runs at 1 kc.
 - a. The transistors are 151-136 silicon NPN devices replaceable by 2N3053.
2. There is no provision for turning off the oscillator.
3. Regenerative feedback through T1255 to Q1255 base and through C1266 to Q1265 base sustains oscillation.
 - a. The double feedback path provides fast switching.
4. Oscillator frequency is determined by T1255 and C1255.
 - a. C1255 is a 1% component with a temperature coefficient opposite to that of T1255.
 - b. The opposing temperature coefficients result in frequency accuracy and stability.
5. The waveforms at Q1255 base and collector are sinusoidal.
 - a. Q1255 collector swings about 8v (from 6v to 14v).
 - b. The base swing is about 1v, centered at ground.
6. The oscillator output at Q1265 collector is a 1v square wave from 11v to 12v.

C. Output Amplifier, Q1274

1. Q1274 is a 151-087 silicon PNP transistor selected from 2N1131.
2. The signal from Q1265 drives Q1274 from cut-off to saturation.
3. When Q1274 saturates its collector pulls up to about 12v.
 - a. The voltage is divided down to 1v by the divider composed of R1274, R1275 and R1276, R1277.
 - b. The +12v supply is adjusted to 1v at the calibrator output.

- c. In the .1v position of the CALIBRATOR switch, R1275 is shorted, dividing the output tap to .1v.
 - d. When saturated, Q1274 draws 5 ma through the divider and the PROBE (current) LOOP.
4. When Q1274 cuts off, its collector and the Calibrator output drops to ground.

453 SLIDE LIST

General Block Diagram

B-453-0000

Channel 1 Input Amplifier

B-453-0001

0002

0003

0004

0005

0006

0007

Channel 2 Input Amplifier

B-453-0008

Vertical Switching

B-453-0009

0010

0011

0012

0011

0013

0014

0015

0016

0017

Output Amplifier

B-453-0018

0019

0020

0021

0022

0019

Trigger Preamplifier

B-453-0023

0024

A Trigger Generator

B-453-0025

0026

0027

0028

0029

0030

B Trigger Generator

B-453-0031

A Sweep Generator

B-453-0032

0033

0034

0035

0034.1

0033

0036

0037

0038

0039

0040

0041

0042

0043

0044

B Sweep Generator

B-453-0045
0046
0047
0048
0049
0051
0050
0052
0053
0054

Timing Switch

B-453-0055
0056

Horizontal Amplifier

B-453-0057
0058
0059
0060
0061

CRT and H.V. Circuit

B-453-0062
0063
0064
0065
0065.l

Z Axis Amplifier

B-453-0066
0067
0068
0069

Power Supply

B-453-0070
0071
0072
0073
0074

Calibrator

B-453-0075

Panel

B-453-2001
2003
2004

Schematic

C-453-0001
0002
0003
0004
0005
0006
0007
0008
0009
0010
0011
0012
0013
0014
0014
0015
0016
0017
0018
0019

453 RECOMMENDED HANDOUTS

B-453- 0201

2003

2004

0000

0001

0005

0009

0010

0012

0013

0014

0015

0016

0018

0023

0025

0030

0034

0035

B-453- 0034.1

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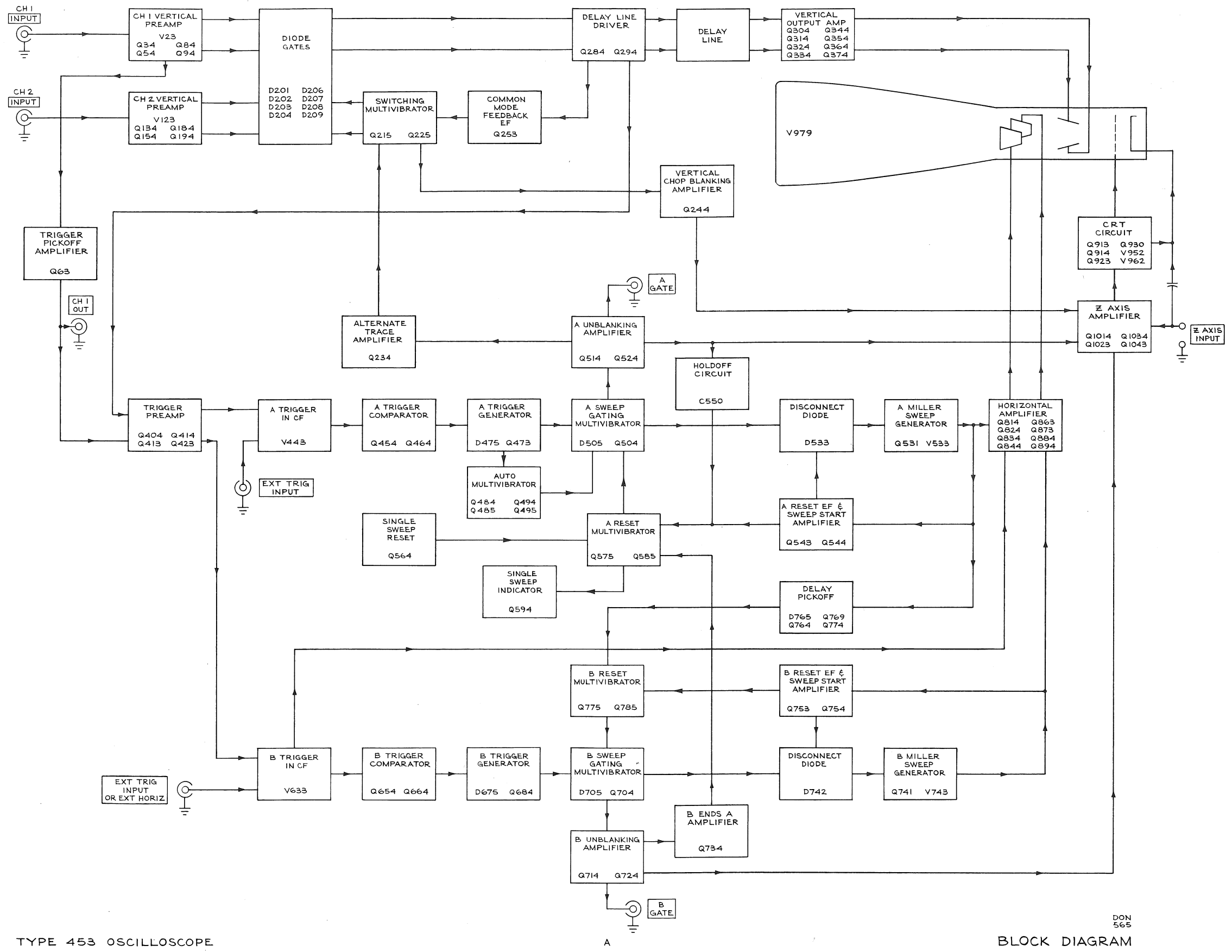
0058

0062

0066

0068

0070



TYPE 453 OSCILLOSCOPE

BLOCK DIAGRAM

DON 565

IMPORTANT**VOLTAGE AND WAVEFORM CONDITIONS**

Circuit voltages measured with a 20,000 Ω /volt VOM. All readings in volts. Voltages are measured with respect to chassis ground unless otherwise noted.

Waveforms shown are actual waveform photographs taken with a Tektronix Oscilloscope Camera System and Projected Graticule.

Voltages and waveforms on the schematics (shown in blue) are not absolute and may vary between instruments. Any apparent differences between voltage levels measured with the voltmeter and those shown on the waveforms are due to circuit loading of the voltmeter.

The test oscilloscope used had the following characteristics: Minimum deflection factor, 0.2 volts/division using a 10 \times probe; frequency response, dc to 40 Mc. Dc input coupling was used except as noted otherwise. To indicate true time relationship between signals, the test oscilloscope was externally triggered.

Voltage readings and waveforms were obtained under the following conditions unless otherwise noted on the individual diagrams:

Crt controls

INTENSITY	Midrange
FOCUS	Adjust for focused display
SCALE ILLUM	As desired

Vertical controls (both channels if applicable)

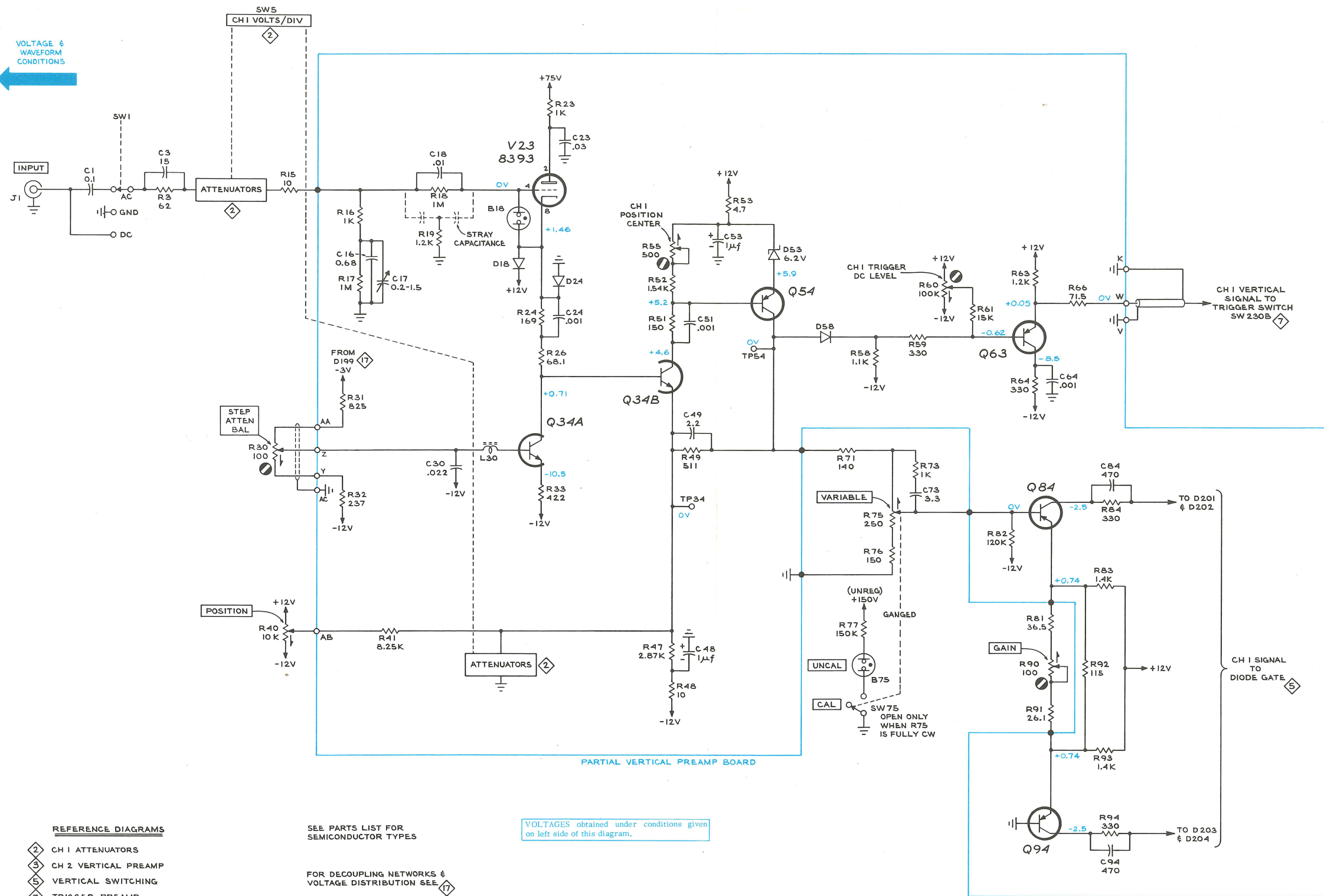
VOLTS/DIV	20 mV
VARIABLE	CAL
POSITION	Midrange
AC GND DC	GND
MODE	CH 1
TRIGGER	NORM
INVERT	Pushed in

Triggering controls (both A and B if applicable)

LEVEL	0
SLOPE	+
COUPLING	AC
SOURCE	INT

(Continued on diagram )

VOLTAGE & WAVEFORM CONDITIONS
←



- REFERENCE DIAGRAMS
- ② CH 1 ATTENUATORS
 - ③ CH 2 VERTICAL PREAMP
 - ⑤ VERTICAL SWITCHING
 - ⑦ TRIGGER PREAMP
 - ⑩ POWER SUPPLY & DISTRIBUTION

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE ⑩

VOLTAGES obtained under conditions given on left side of this diagram.

Sweep controls

DELAY-TIME MULTIPLIER	0.50
A TIME/DIV	1 mSEC
B TIME/DIV	1 mSEC
A VARIABLE	CAL
A SWEEP MODE	AUTO TRIG
B SWEEP MODE	B TRIGGERABLE AFTER DELAY TIME
HORIZ DISPLAY	A
MAG	OFF
A SWEEP LENGTH	FULL
POSITION	Midrange
POWER	ON

Side-panel controls

B TIME/DIV VARIABLE	CAL
CALIBRATOR	1 V

Rear-panel controls

LINE VOLTAGE RANGE	HIGH
--------------------	------








Line voltage 115 volts

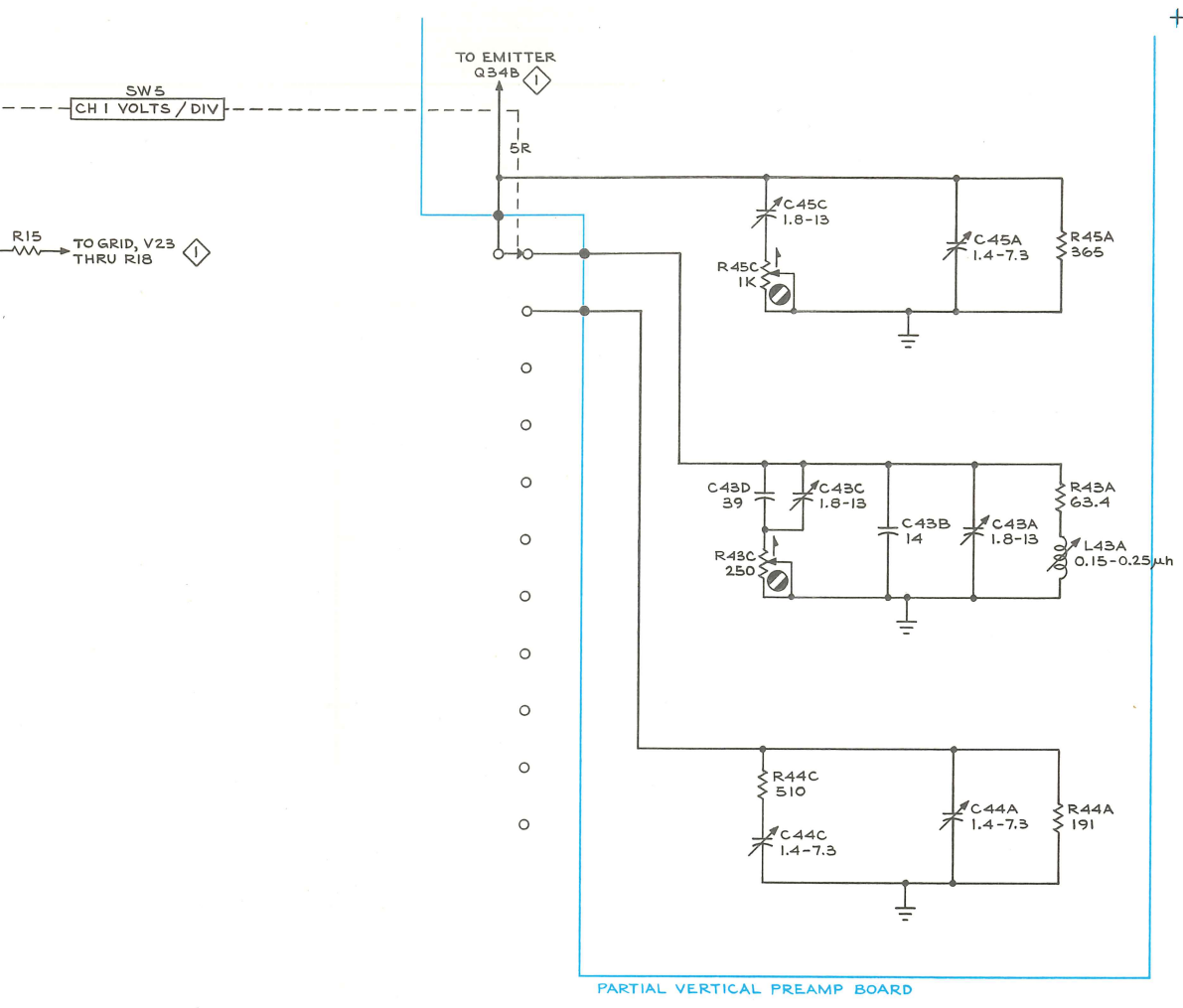
Signal applied None

Trace position Centered

Schematic Symbols

The following symbols are used on the schematics:

	Screwdriver adjustment
	Front-panel control or connector.
	Clockwise control rotation in direction of arrow.
	Connection made at indicated pin on etched-wiring board.
	Connection soldered to etched-wiring board.
	Blue line encloses components located on etched-wiring board.
	Input from, or output to indicated schematic.



PARTIAL VERTICAL PREAMP BOARD

REFERENCE DIAGRAMS

- ① CH 1 VERTICAL PREAMP

R5F
2

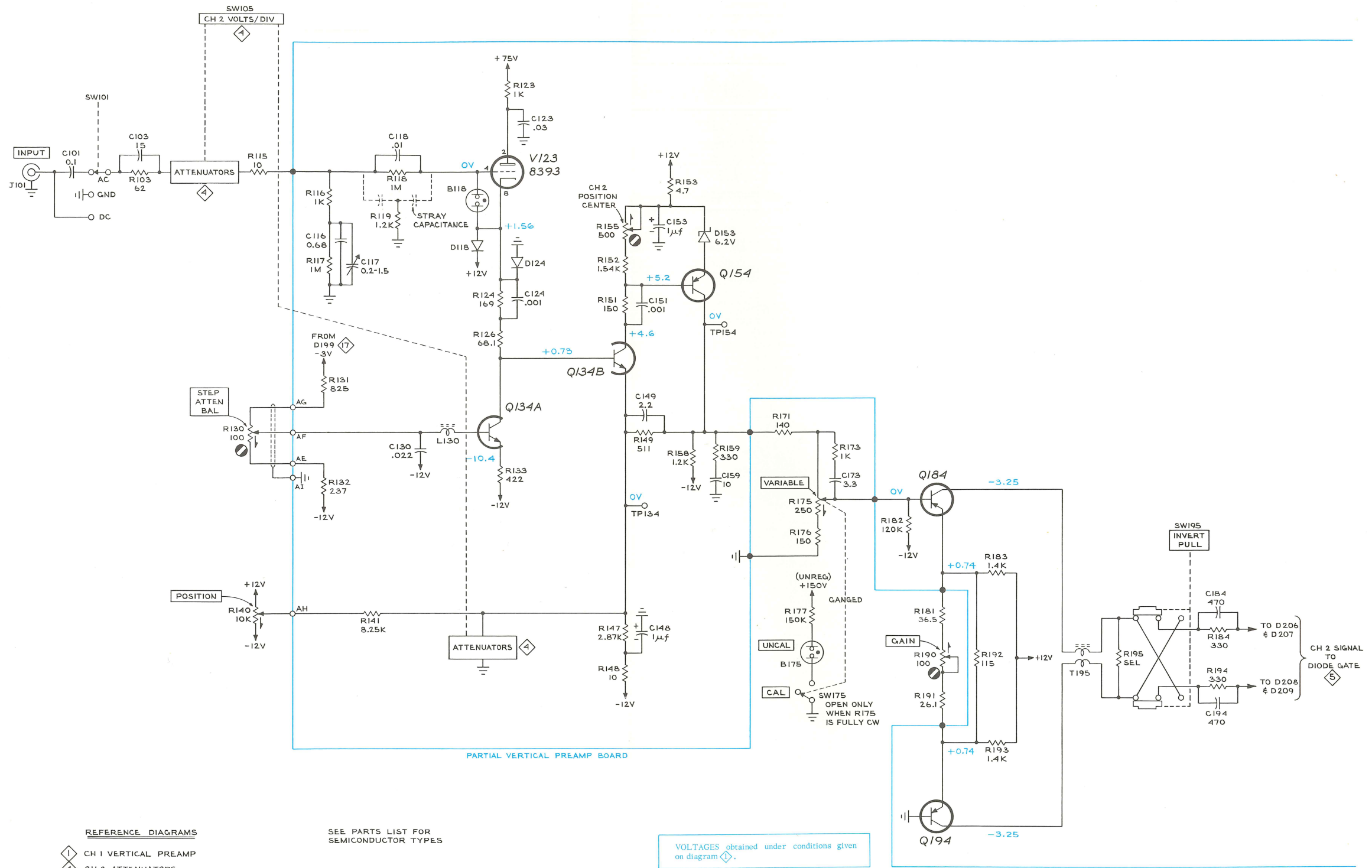
R7F
47

A

DON
565
CH 1 ATTENUATORS ②

CH 1 ATTENUATORS

②



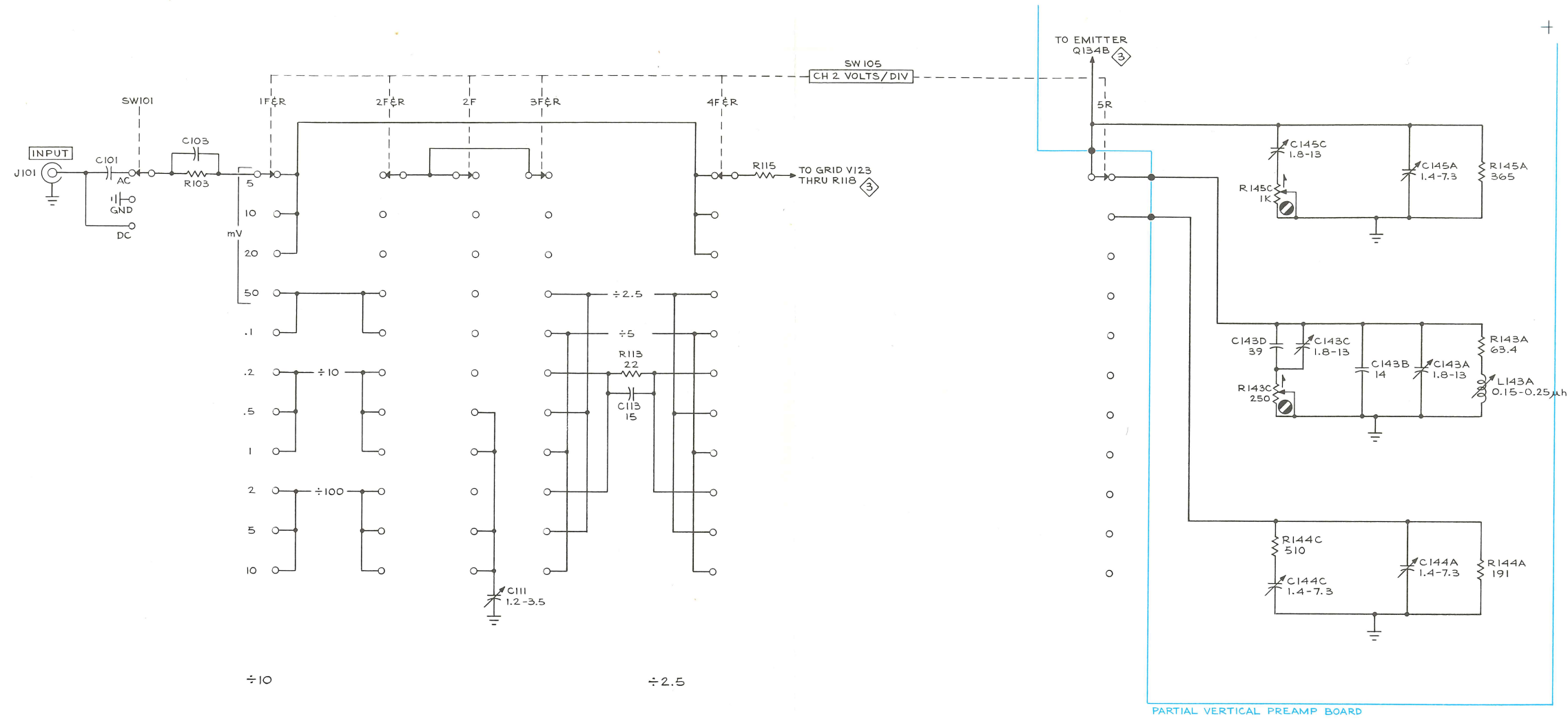
- REFERENCE DIAGRAM
- ① CH 1 VERTICAL PREAMP
 - ④ CH 2 ATTENUATORS
 - ⑤ VERTICAL SWITCHING
 - ⑦ POWER SUPPLY & DISTRIBUTION

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

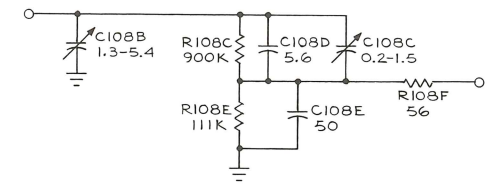
FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE ⑦

VOLTAGES obtained under conditions given on diagram ④.

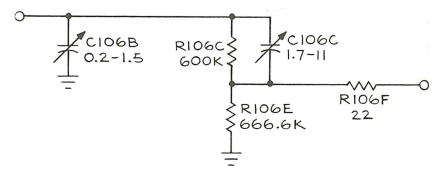
CMD 565



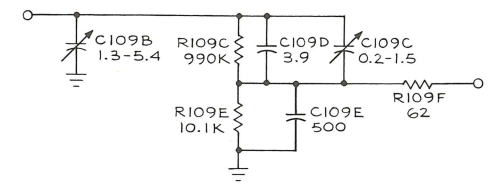
PARTIAL VERTICAL PREAMP BOARD



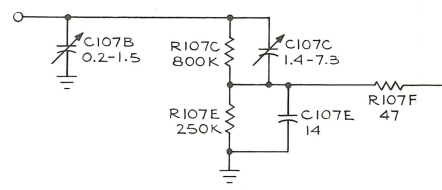
÷100



÷5



÷100



÷5

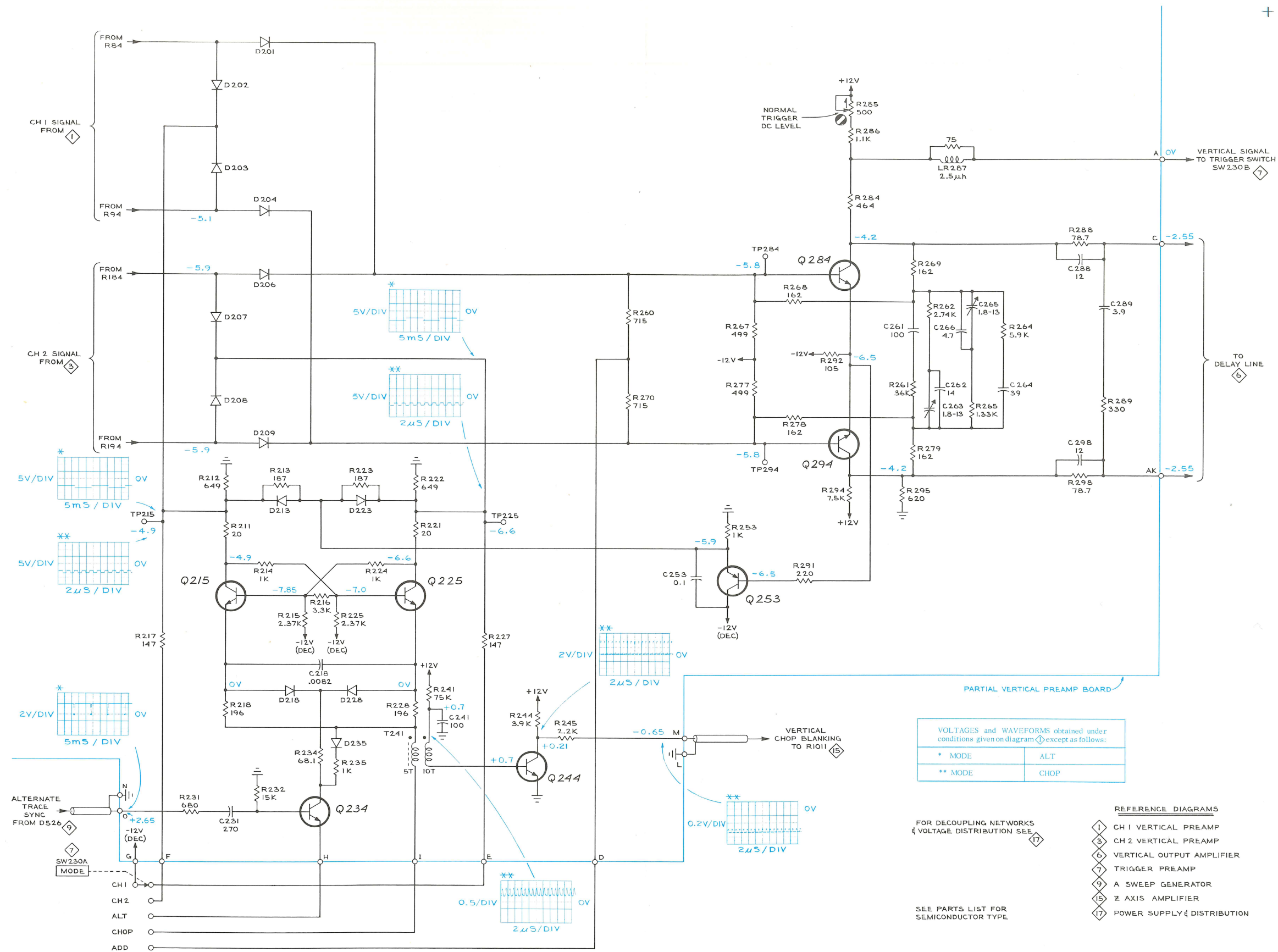
REFERENCE DIAGRAMS
CH 2 VERTICAL PREAMP

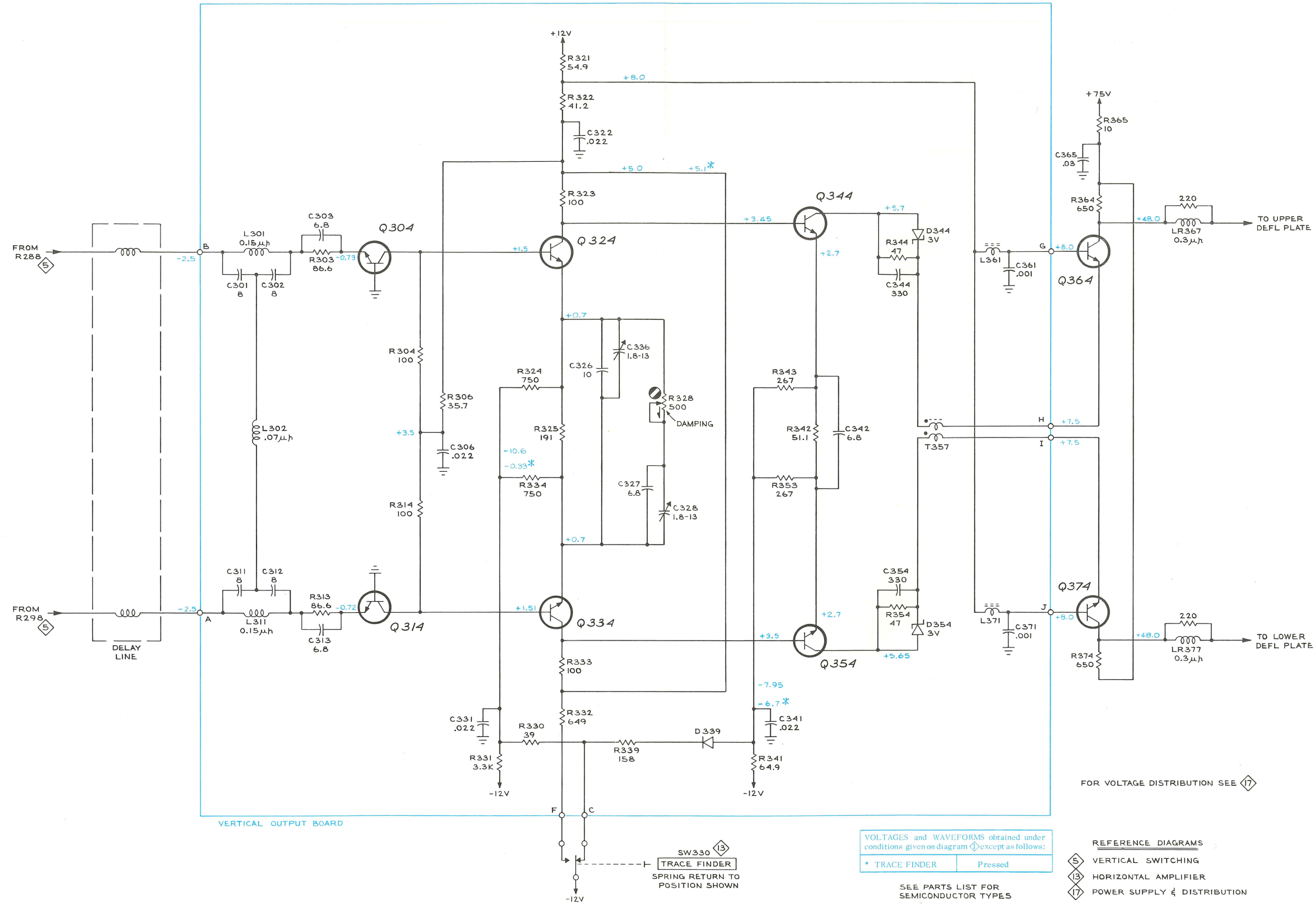
TYPE 453 OSCILLOSCOPE

A

DON
565
CH 2 ATTENUATORS

+

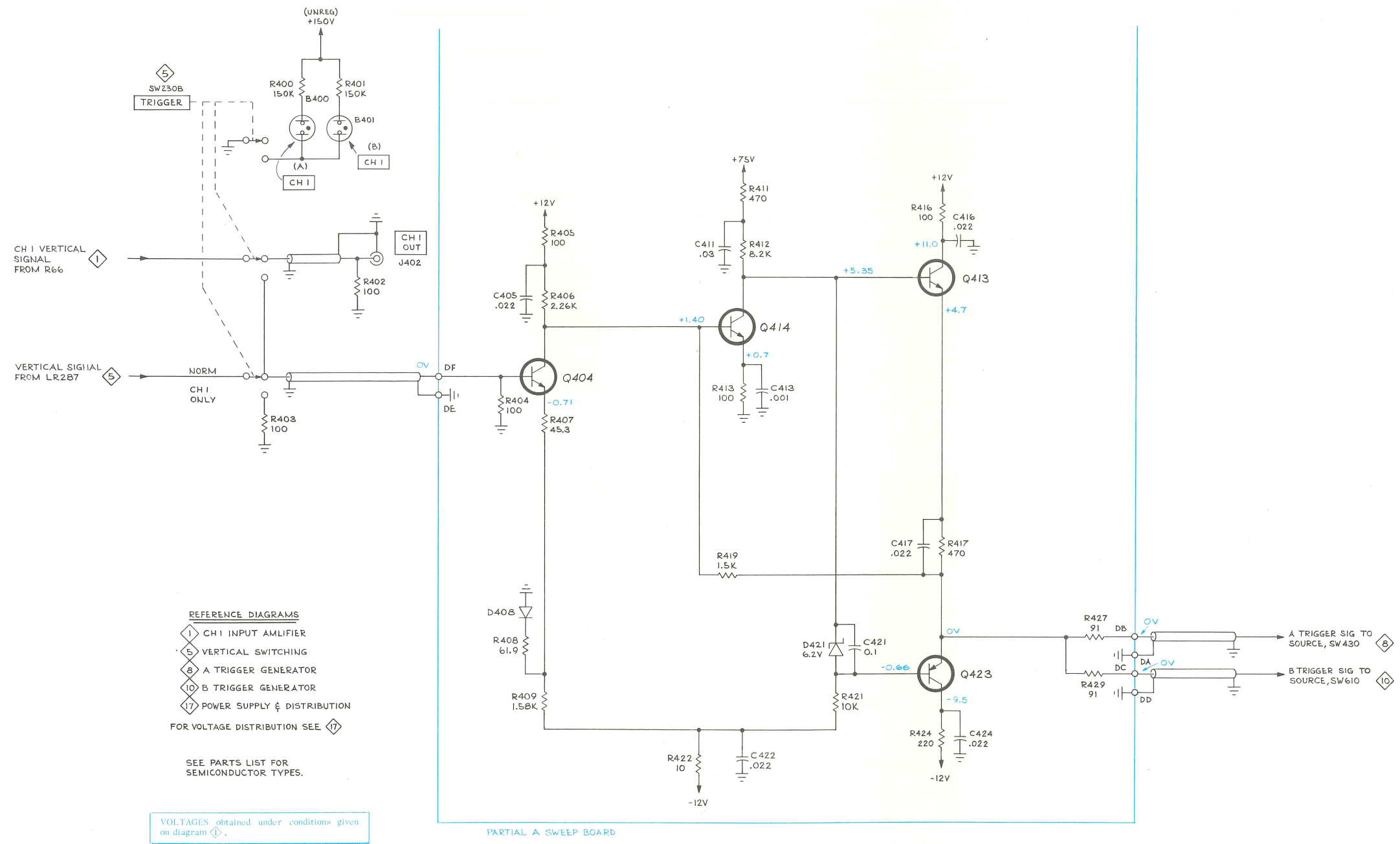




TYPE 453 OSCILLOSCOPE

VERTICAL OUTPUT AMPLIFIER

CMD 565



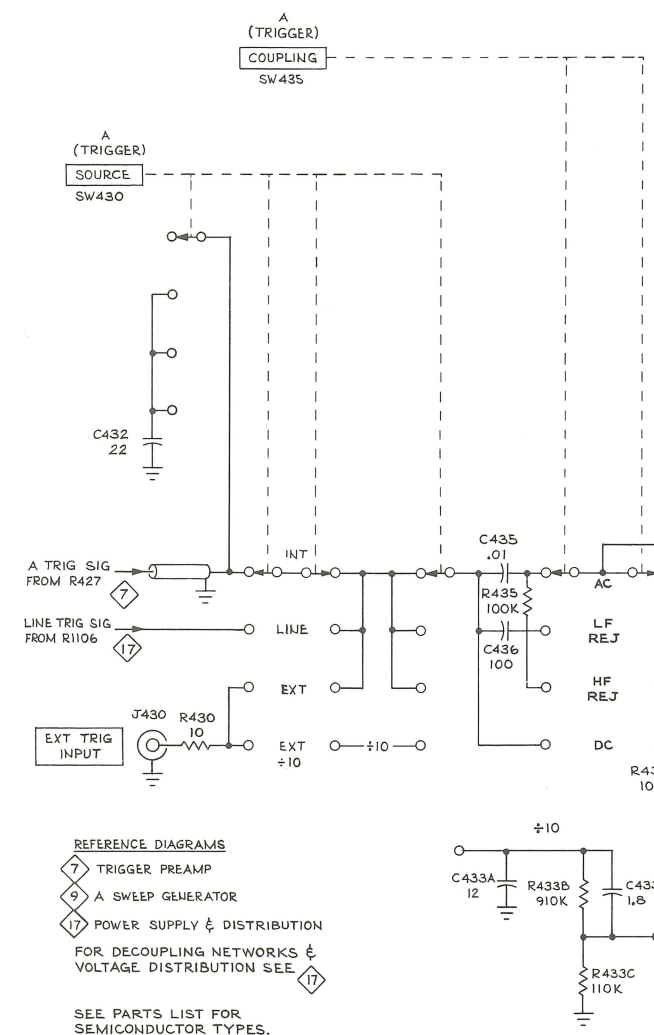
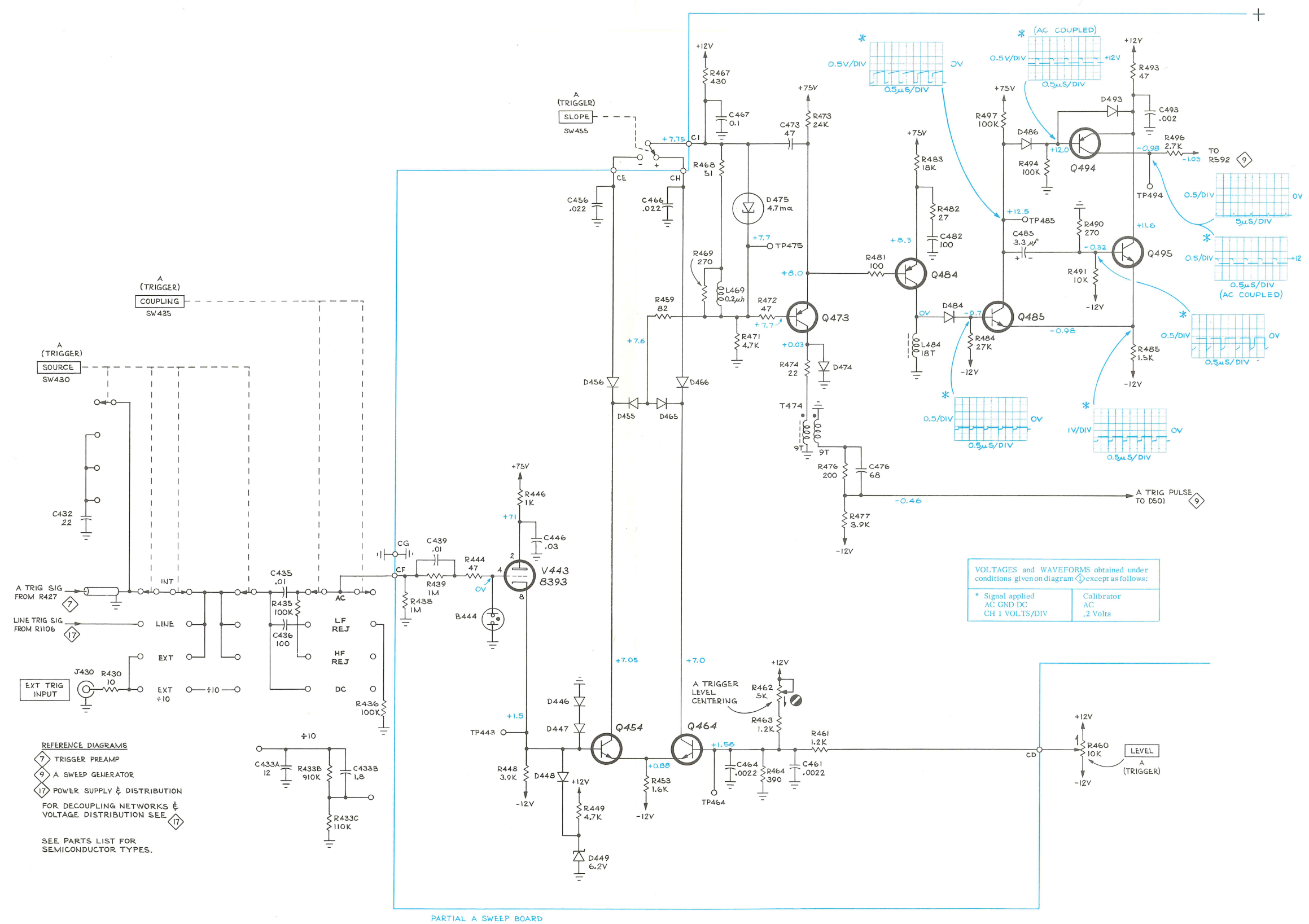
TYPE 453 OSCILLOSCOPE

A

JN 565
TRIGGER PREAMP 7

TRIGGER PREAMP

7

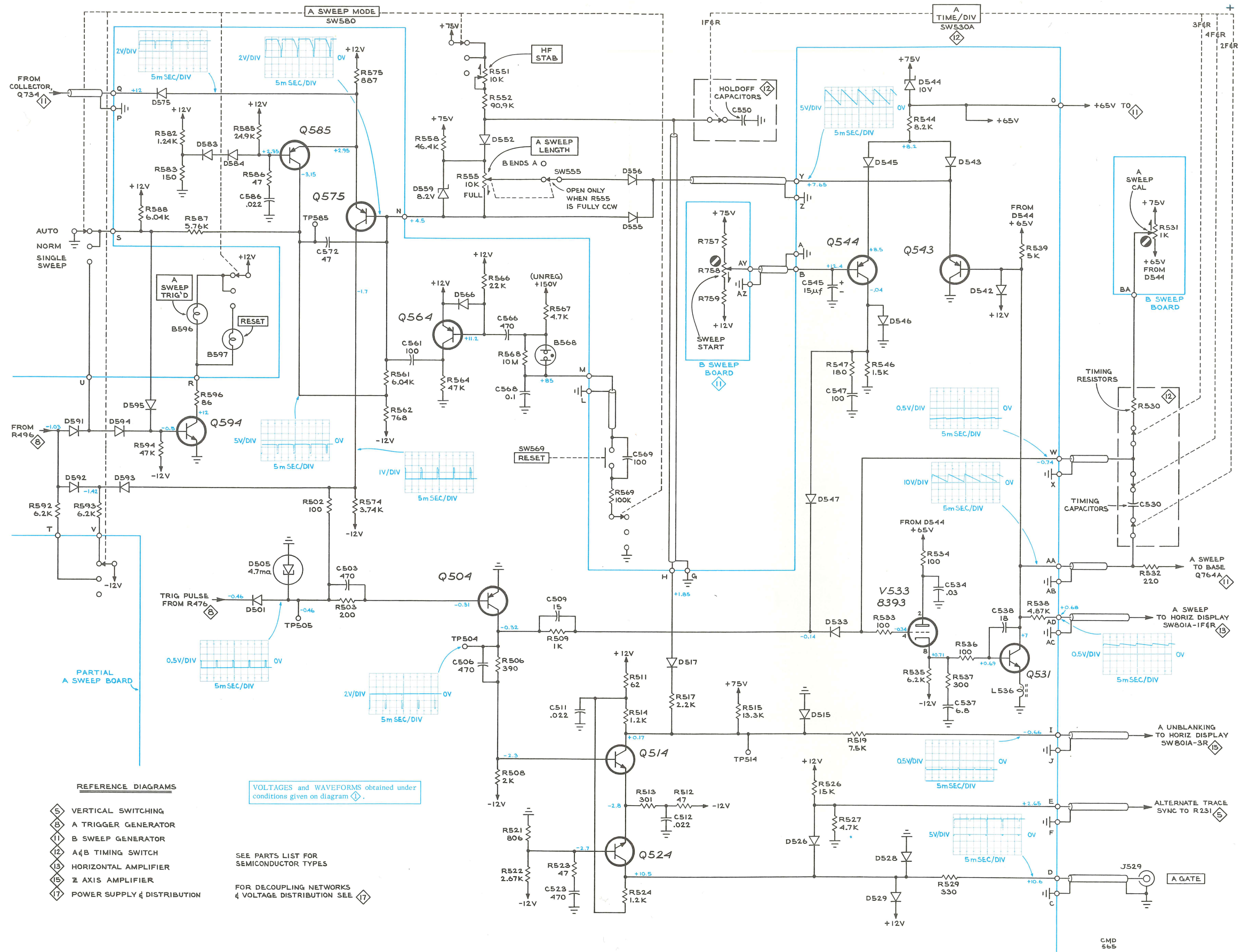


TYPE 453 OSCILLOSCOPE

PARTIAL A SWEEP BOARD

A

JUN 56S
A TRIGGER GENERATOR 8

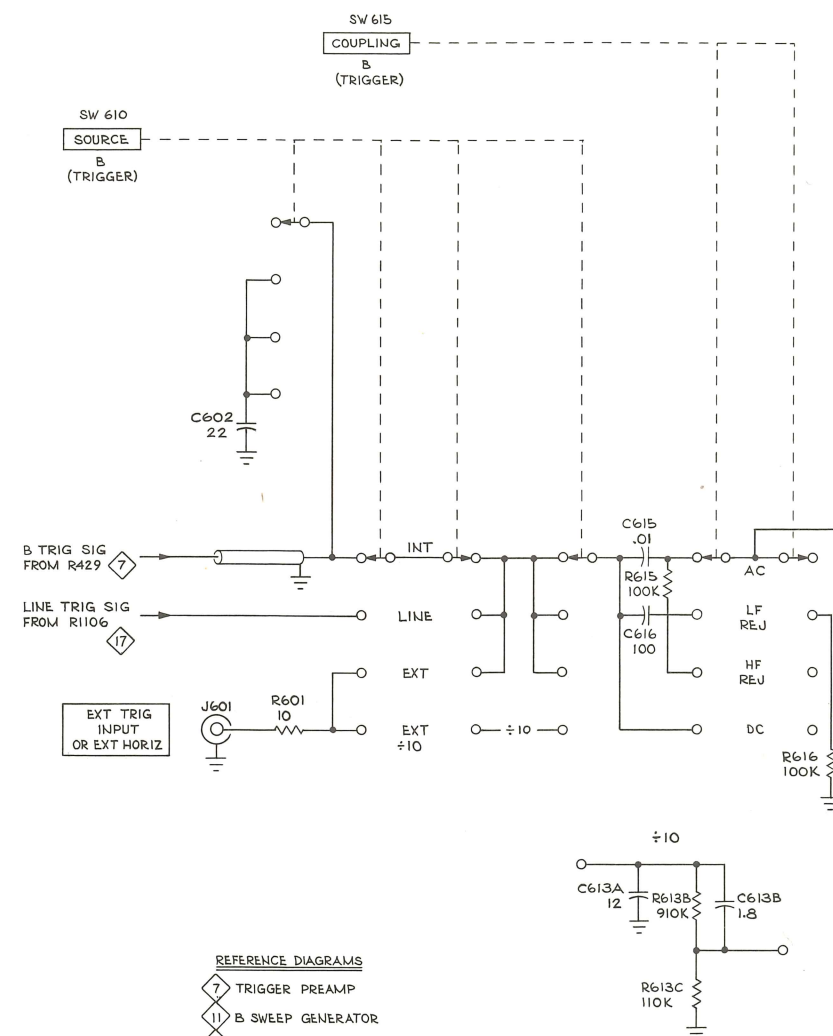


REFERENCE DIAGRAMS

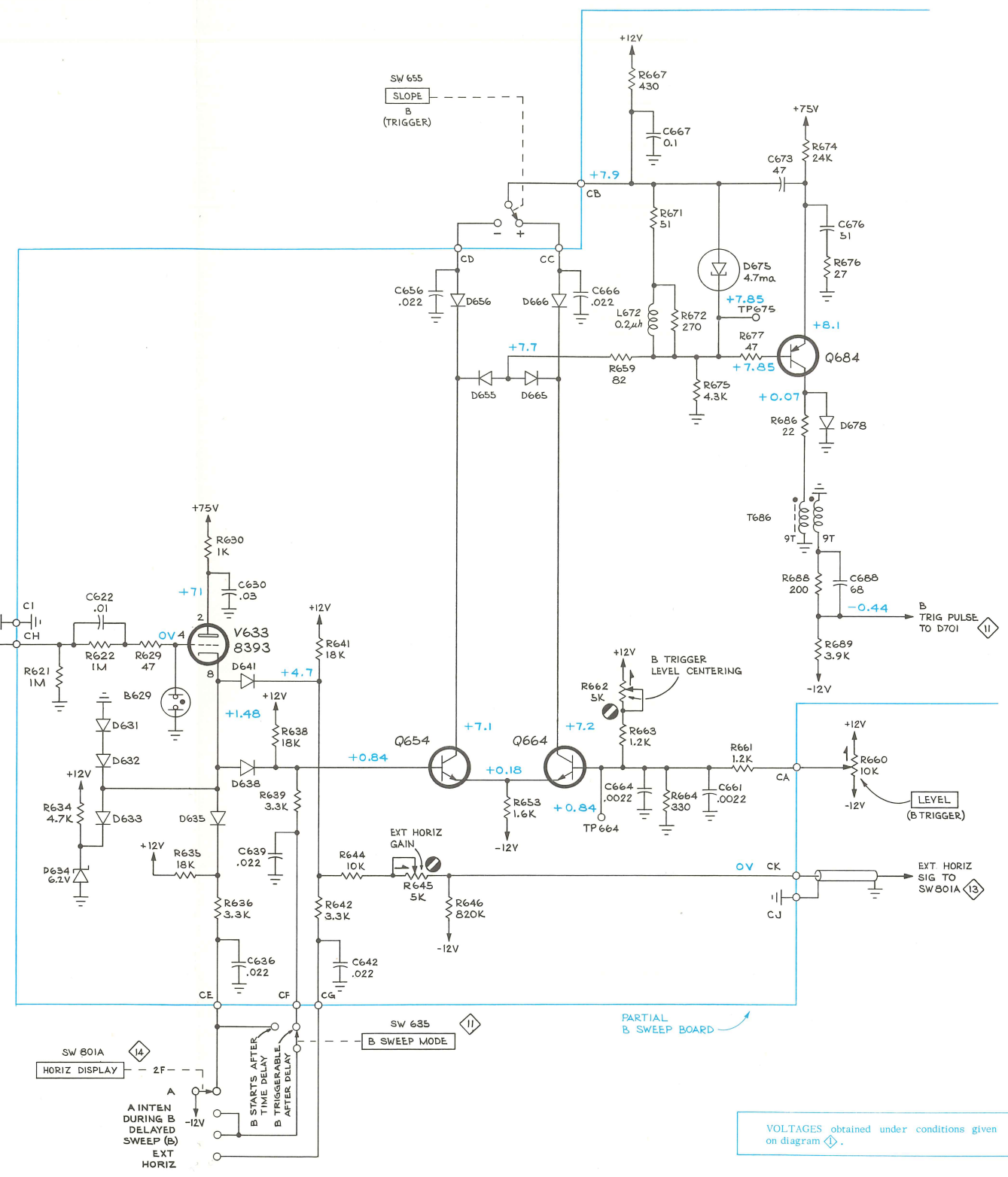
- 5 VERTICAL SWITCHING
- 8 A TRIGGER GENERATOR
- 11 B SWEEP GENERATOR
- 12 A & B TIMING SWITCH
- 13 HORIZONTAL AMPLIFIER
- 15 Z AXIS AMPLIFIER
- 17 POWER SUPPLY & DISTRIBUTION

VOLTAGES and WAVEFORMS obtained under conditions given on diagram.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES
FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE 17

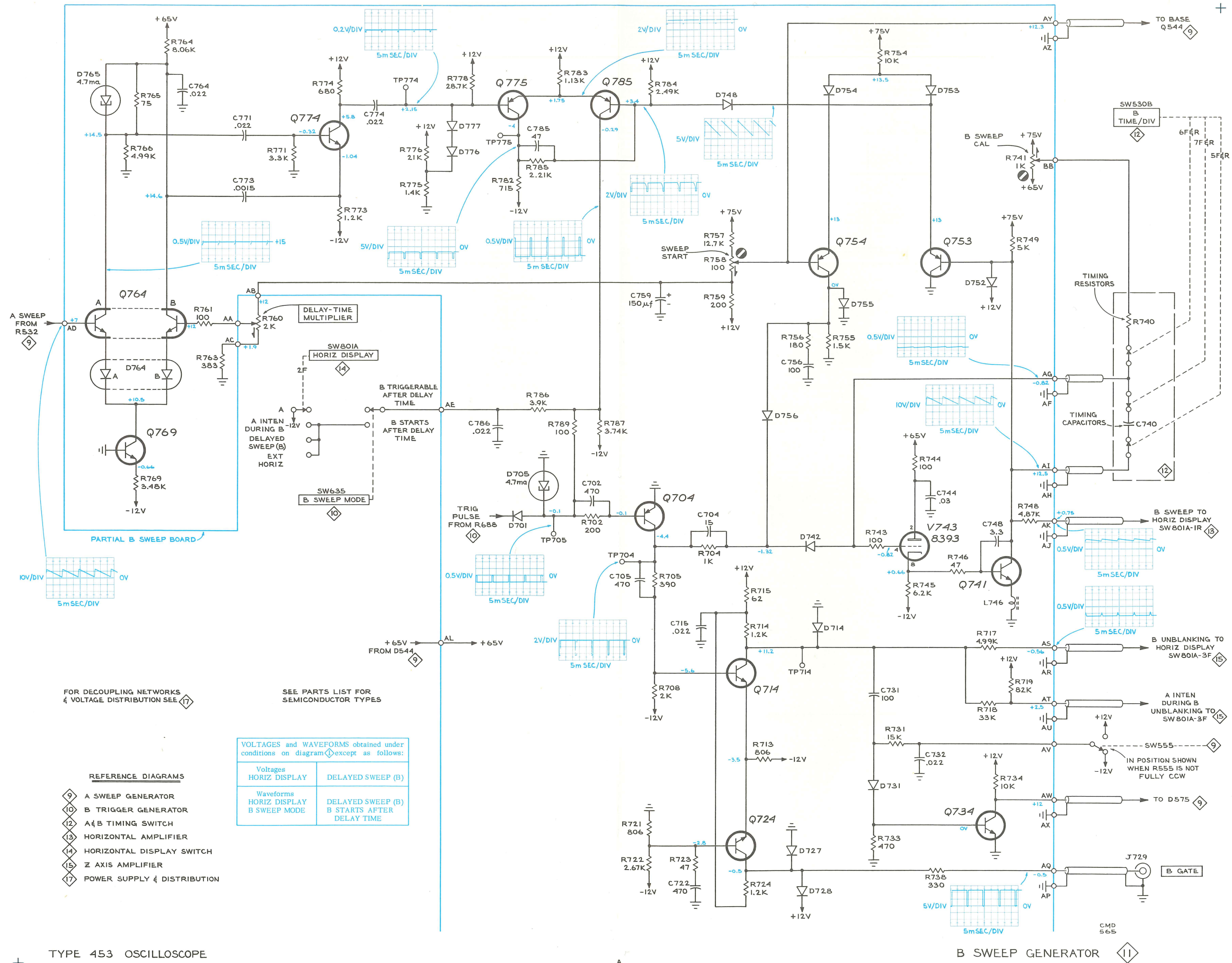


REFERENCE DIAGRAMS
 7 TRIGGER PREAMP
 11 B SWEEP GENERATOR
 13 HORIZONTAL AMPLIFIER
 14 HORIZONTAL DISPLAY SWITCH
 17 POWER SUPPLY & DISTRIBUTION
 FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE 17
 SEE PARTS LIST FOR SEMICONDUCTOR TYPES.



SW 801A 14 HORIZ DISPLAY - 2F -
 A A INTEN DURING B DELAYED SWEEP (b)
 B STARTS AFTER TIME DELAY AFTER DELAY
 B TRIGGERABLE AFTER DELAY
 EXT HORIZ

VOLTAGES obtained under conditions given on diagram.



FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE 17

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

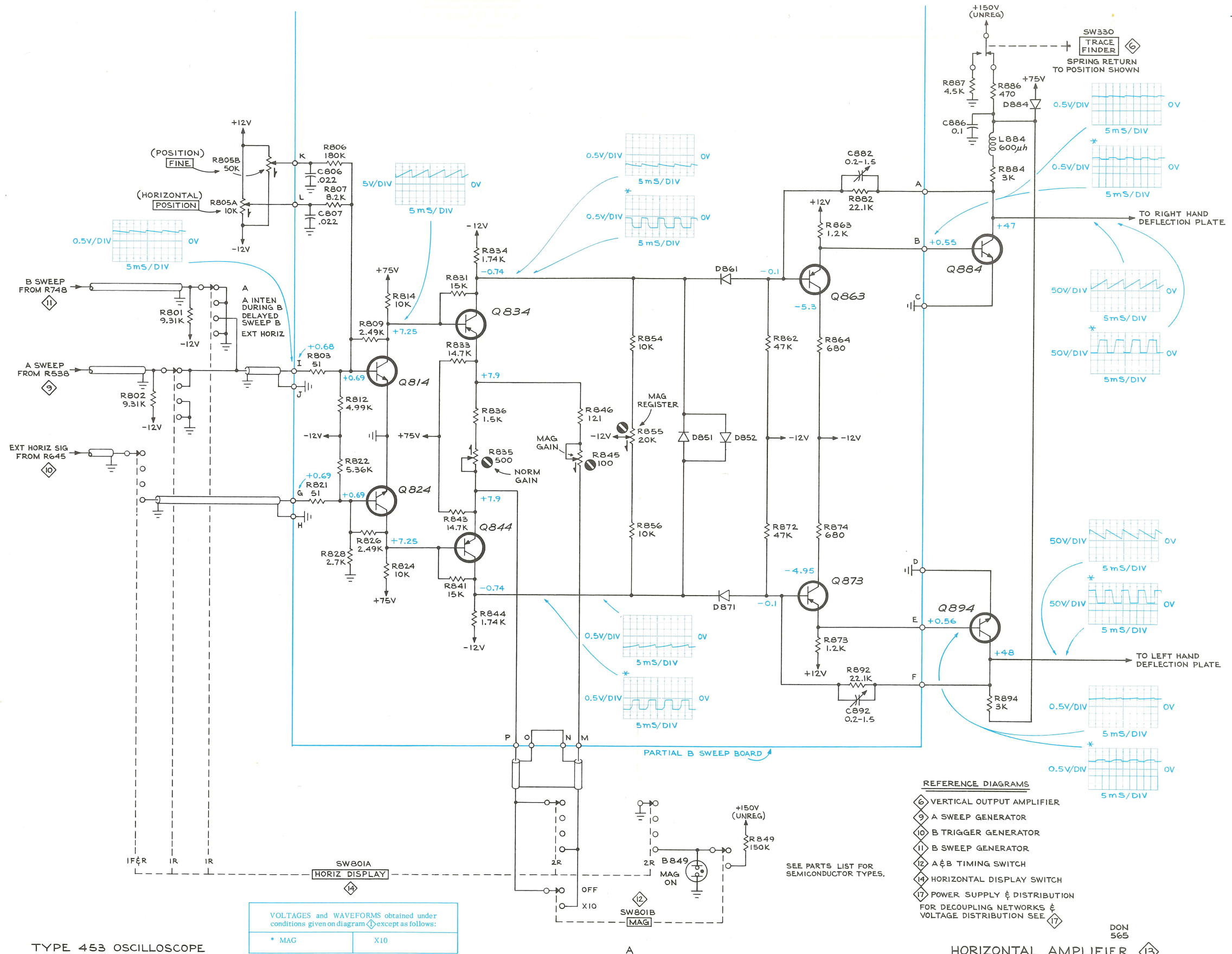
VOLTAGES and WAVEFORMS obtained under conditions on diagram except as follows:

Voltages HORIZ DISPLAY	DELAYED SWEEP (B)
Waveforms HORIZ DISPLAY B SWEEP MODE	DELAYED SWEEP (B) B STARTS AFTER DELAY TIME

- REFERENCE DIAGRAMS
- 9 A SWEEP GENERATOR
 - 10 B TRIGGER GENERATOR
 - 12 A & B TIMING SWITCH
 - 13 HORIZONTAL AMPLIFIER
 - 14 HORIZONTAL DISPLAY SWITCH
 - 15 Z AXIS AMPLIFIER
 - 17 POWER SUPPLY & DISTRIBUTION

TYPE 453 OSCILLOSCOPE

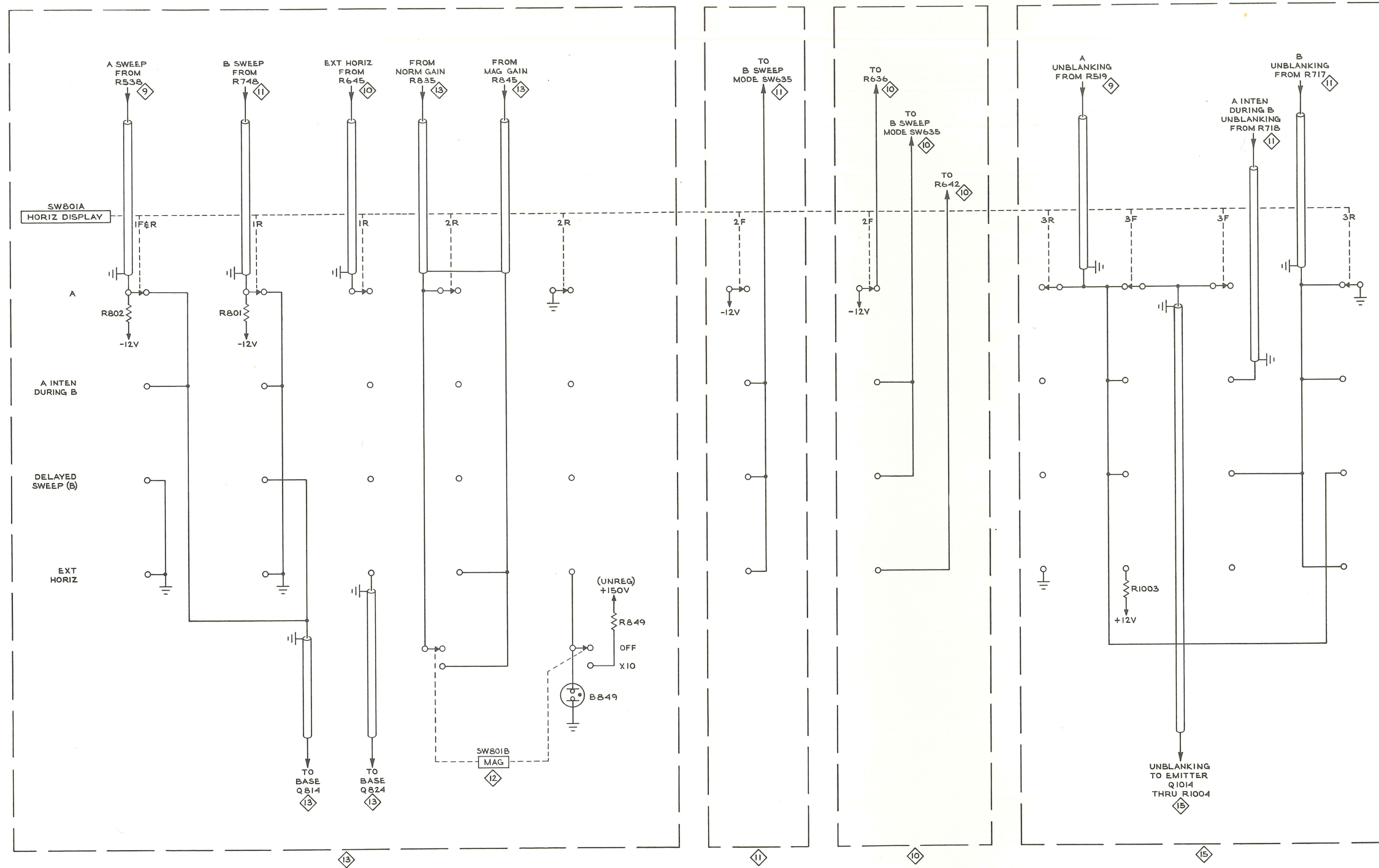
B SWEEP GENERATOR



TYPE 453 OSCILLOSCOPE

HORIZONTAL AMPLIFIER

⑬

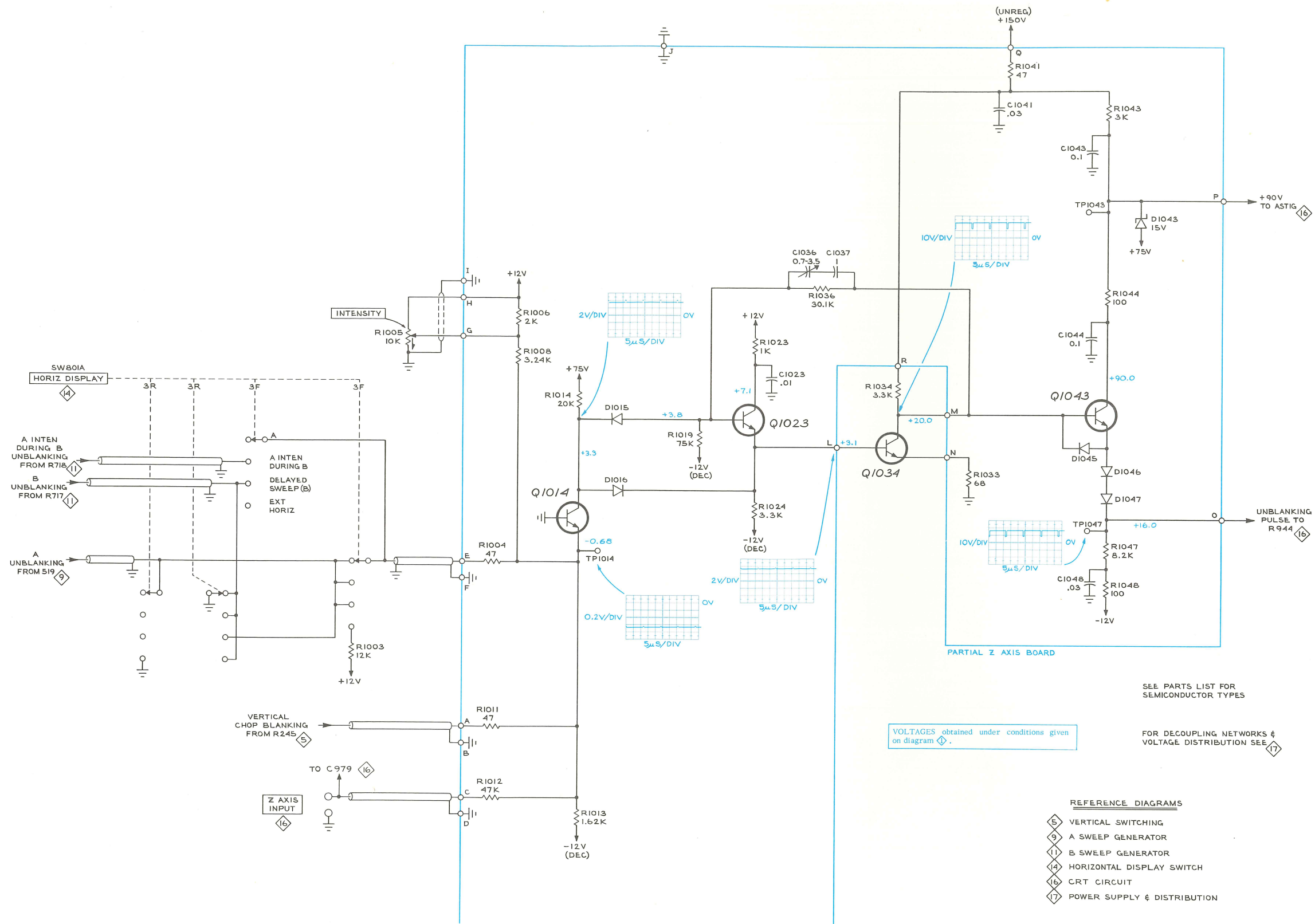


- REFERENCE DIAGRAMS
- 9 A SWEEP GENERATOR
 - 10 B TRIGGER GENERATOR
 - 11 B SWEEP GENERATOR
 - 13 HORIZONTAL AMPLIFIER
 - 15 Z AXIS AMPLIFIER
 - 12 A & B TIMING SWITCH

TYPE 453 OSCILLOSCOPE

HORIZONTAL DISPLAY SWITCH 14

CMD 565



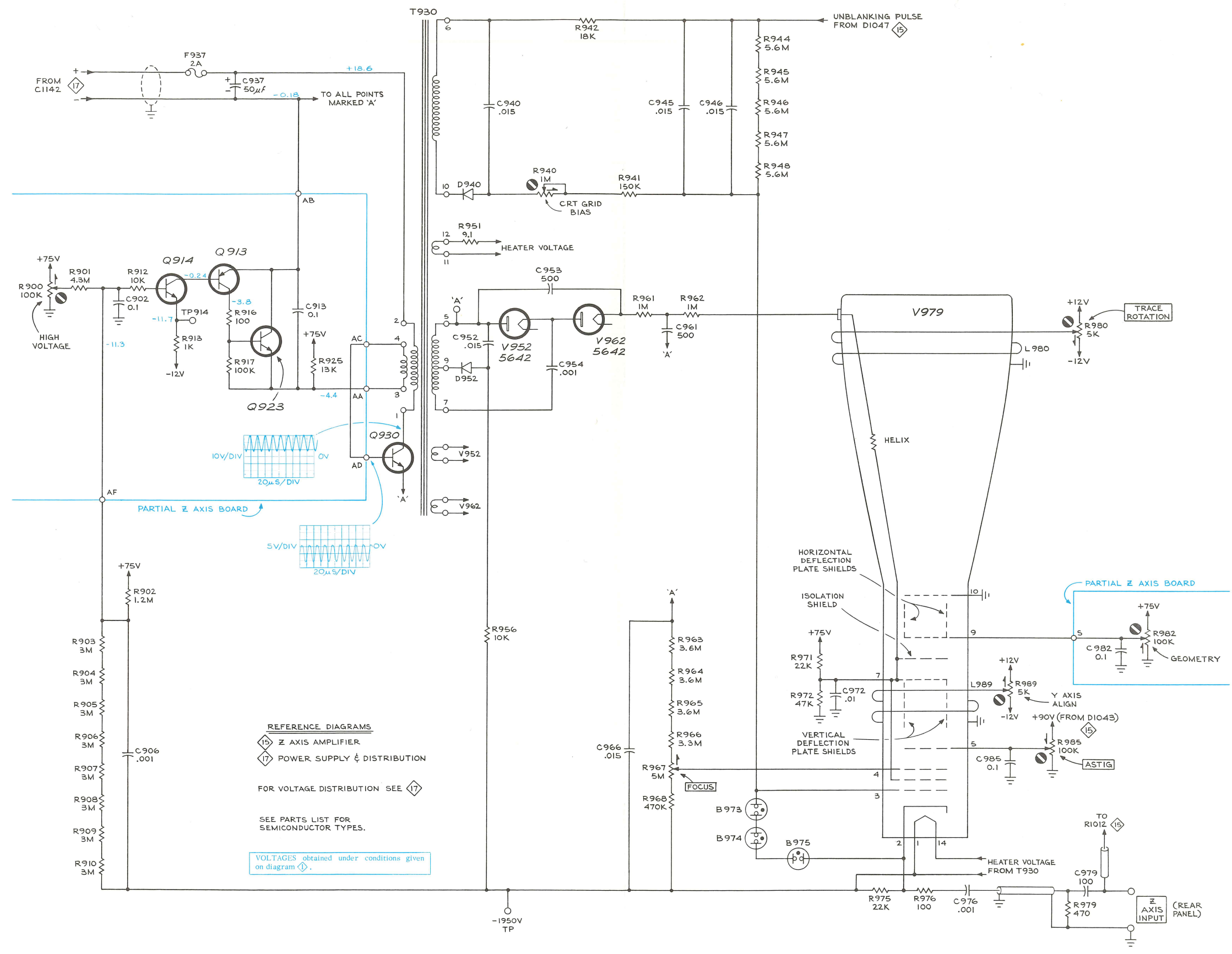
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

VOLTAGES obtained under conditions given on diagram.

FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE

REFERENCE DIAGRAM

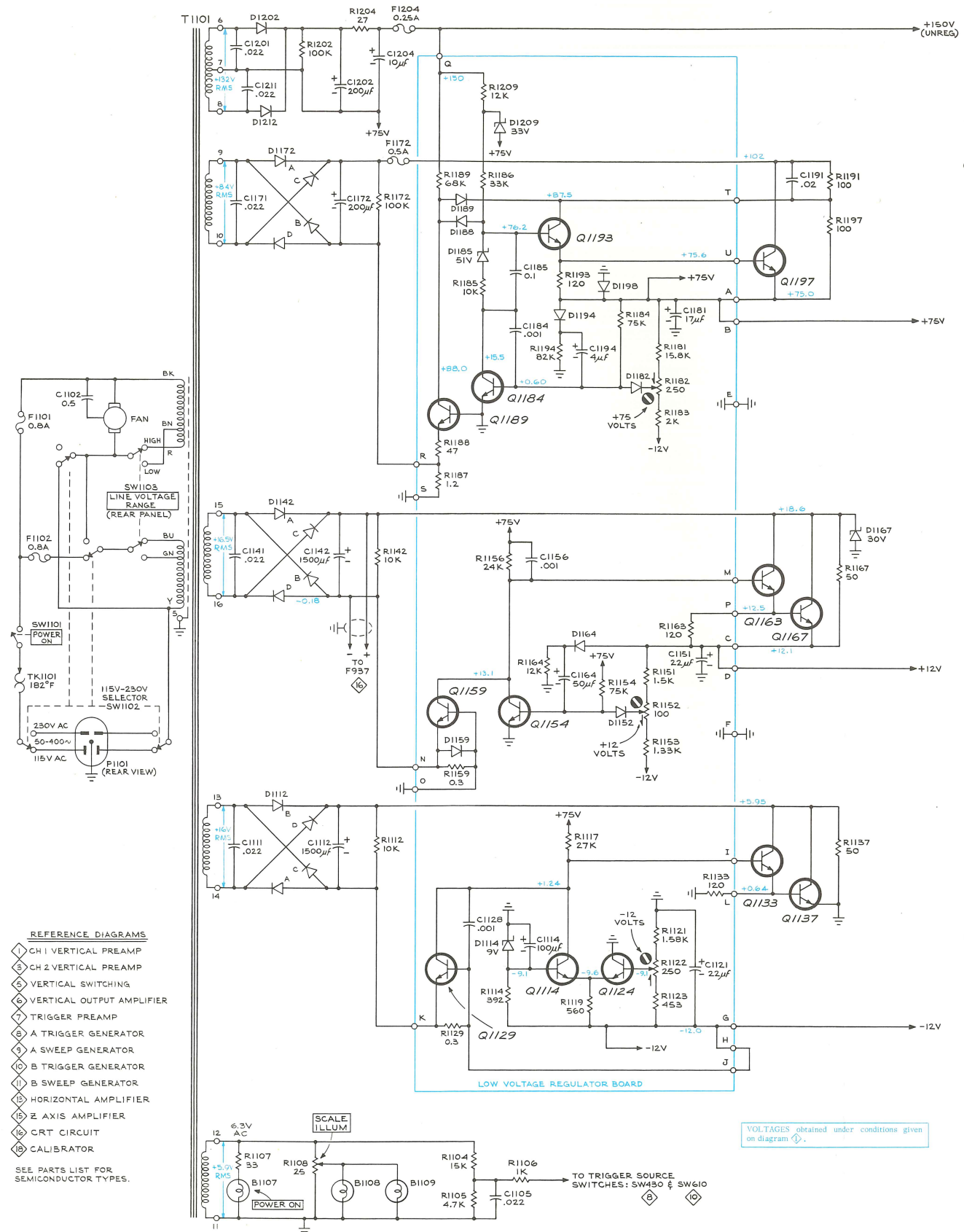
- 5 VERTICAL SWITCHING
- 9 A SWEEP GENERATOR
- 11 B SWEEP GENERATOR
- 14 HORIZONTAL DISPLAY SWITCH
- 16 CRT CIRCUIT
- 17 POWER SUPPLY & DISTRIBUTION



TYPE 453 OSCILLOSCOPE

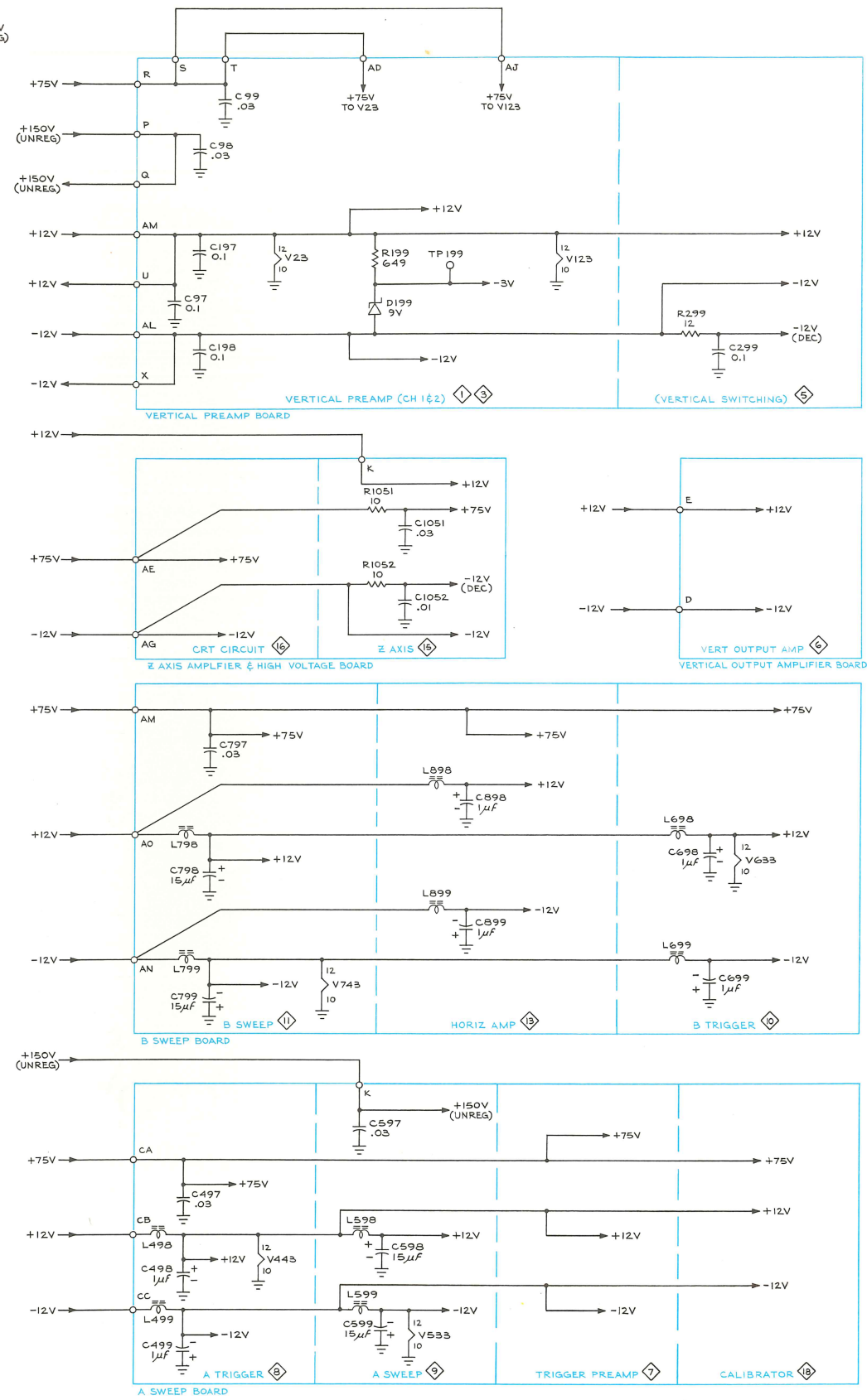
A

CRT CIRCUIT 16 DON 565



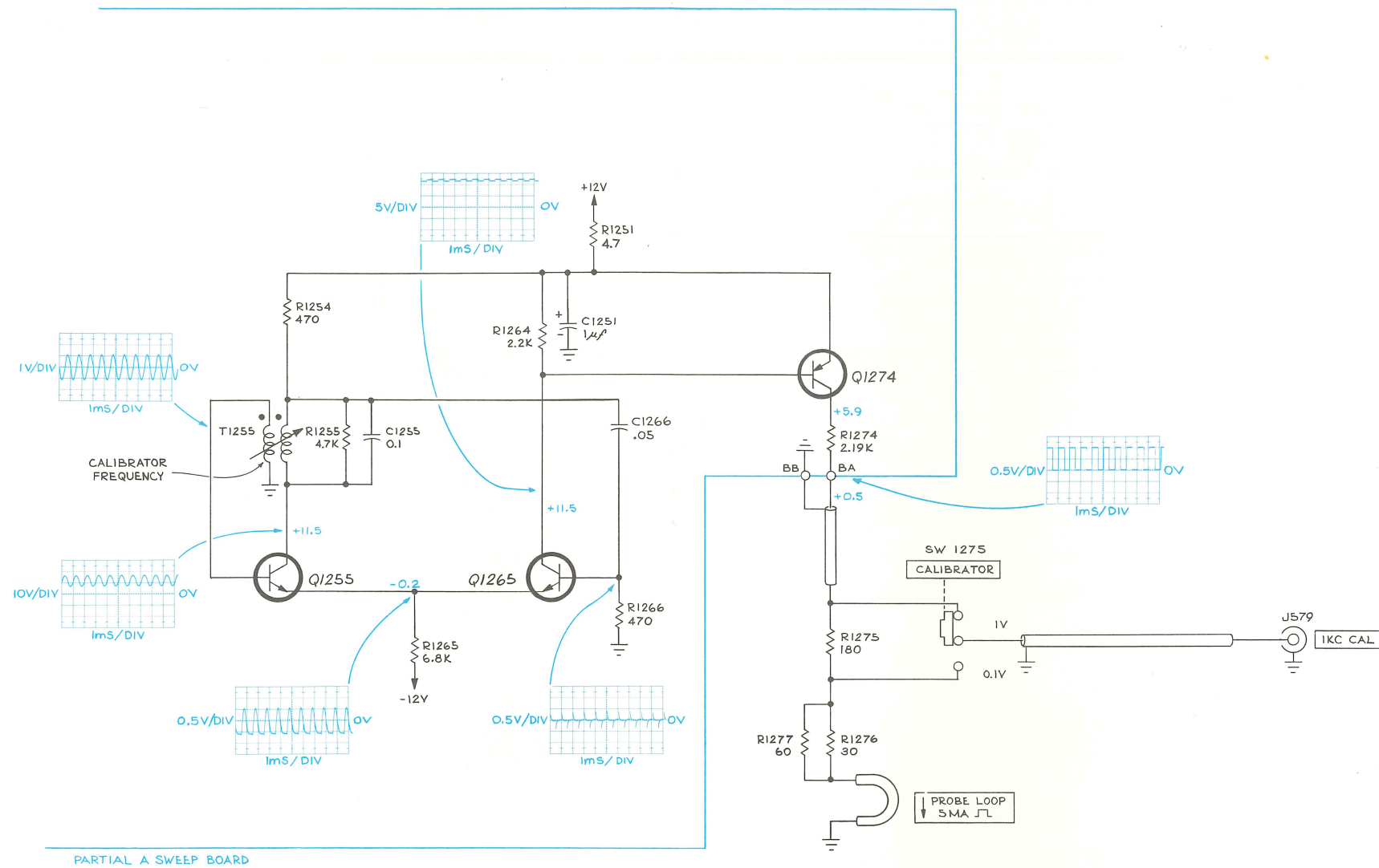
- REFERENCE DIAGRAMS**
- ① CH 1 VERTICAL PREAMP
 - ② CH 2 VERTICAL PREAMP
 - ③ VERTICAL SWITCHING
 - ④ VERTICAL OUTPUT AMPLIFIER
 - ⑤ TRIGGER PREAMP
 - ⑥ A TRIGGER GENERATOR
 - ⑦ A SWEEP GENERATOR
 - ⑧ B TRIGGER GENERATOR
 - ⑨ B SWEEP GENERATOR
 - ⑩ HORIZONTAL AMPLIFIER
 - ⑪ Z AXIS AMPLIFIER
 - ⑫ CRT CIRCUIT
 - ⑬ CALIBRATOR
- SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

VOLTAGES obtained under conditions given on diagram.



TYPE 453 OSCILLOSCOPE

POWER SUPPLY & DISTRIBUTION



PARTIAL A SWEEP BOARD

FOR DECOUPLING NETWORKS & VOLTAGE DISTRIBUTION SEE 

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

VOLTAGES and WAVEFORMS obtained under conditions given on diagram 