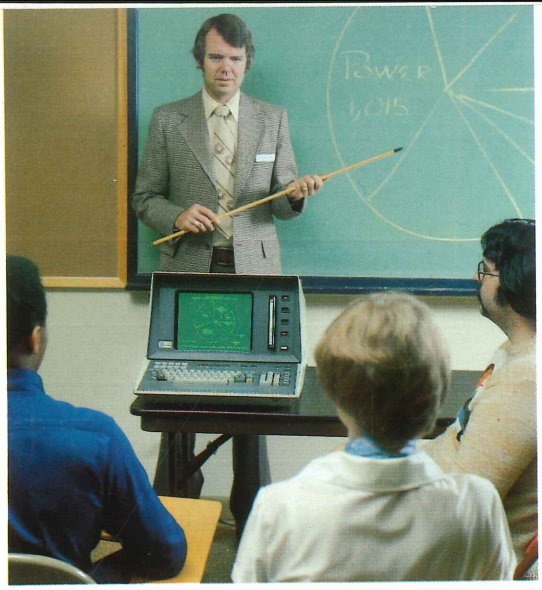
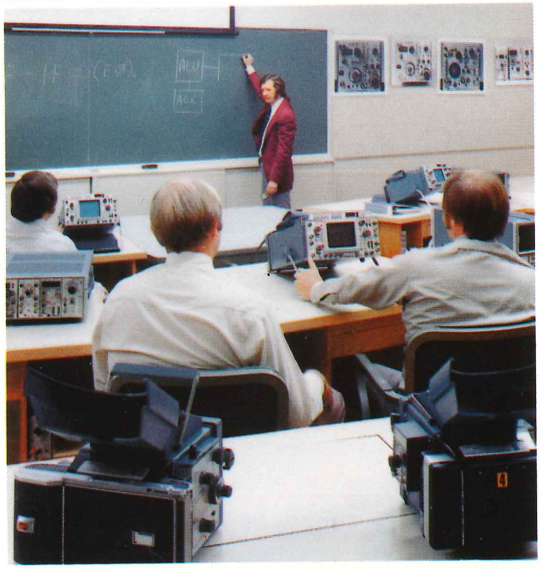
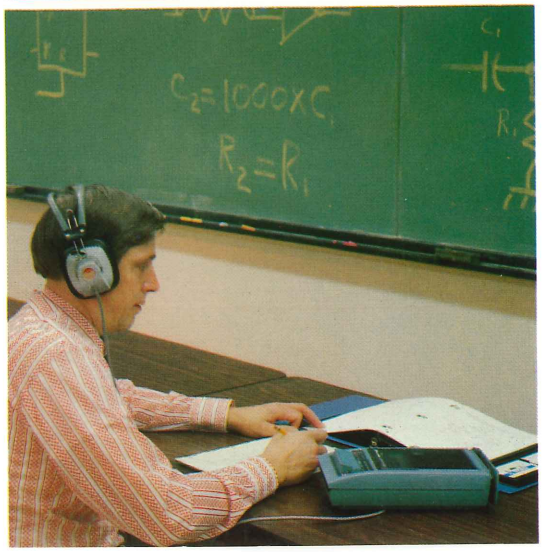






Introduction to Sampling Concepts

Tektronix®
COMMITTED TO EXCELLENCE

TEKTRONIX PART
062-5260-00

MARKETING TRAINING
JUNE 1980

Introduction to Sampling Concepts

Tektronix®
COMMITTED TO EXCELLENCE

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SAFETY INFORMATION SUMMARY

The general safety information contained here is for operating and servicing personnel of electronic instruments except where otherwise noted to be exclusively for servicing personnel. Specific warnings and cautions will be found throughout this document where they apply, but may not appear in this summary.

TERMS AND SYMBOLS

IN THIS DOCUMENT

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.


Static-sensitive device.


Applicable cautionary information.

AS MARKED ON TEKTRONIX EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.


DANGER — High voltage.


Protective ground (earth) terminal.


ATTENTION — Refer to manual.

WARNINGS

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your electronic instrument. Use only power cords which are in good condition. Refer power cord and connector changes to qualified service personnel.

GROUNDING THE EQUIPMENT

Line-voltage operated electronic equipment should be grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the equipment input or output terminals. A protective ground connection, by way of the grounding connector in the power cord, is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

USE THE PROPER FUSE

Only use replacement fuses which are identical in type, voltage rating, and current rating as those specified by the manufacturer's parts list.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERE

To avoid explosion, do not operate any electronic equipment in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT OPERATE WITHOUT COVERS OR PANELS

To avoid personal injury, do not operate electronic equipment without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

The following are for use by qualified service personnel only. Refer also to the preceding Safety Information Summary.

WARNINGS

DO NOT SERVICE EQUIPMENT ALONE

Do not perform internal service or adjustment of electronic equipment unless another person, capable of rendering first aid and resuscitation, is present.

CRT HANDLING

Use care when handling a crt. Breakage of a crt causes a high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking the crt on any object which might cause cracking or imploding. The crt should be stored in a protective carton or placed face down in a protected location on a smooth surface with a soft mat under the faceplate.

USE CARE WHEN SERVICING WITH POWER ON

Disconnect power before removing protective panels, soldering, or replacing components. Because dangerous voltages may exist at several points within the equipment, do not touch exposed connections or components while the power is on.

SILICONE GREASE HANDLING

Handle silicone grease with care. Avoid getting the silicone grease in your eyes and always wash your hands thoroughly after using it.

CAUTIONS

CHECK LINE-VOLTAGE SELECTOR SETTING

Some electronic instruments are capable of operating from several line-voltage sources. To prevent damage to the instrument, check that the line-voltage source matches the setting of the instrument line-voltage selector before applying power.

CHECK VENTILATION CLEARANCES

To prevent overheating, check that the manufacturer's recommendations for ventilation clearances and ambient operating temperatures are adhered to.

ESTABLISH THE CORRECT CRT INTENSITY

To avoid damage to the crt phosphor, do not allow stationary, bright, focused spots to remain on the display screen.

CHAPTER 1
USING THIS INSTRUCTIONAL MODULE

With this instructional module of the Tektronix Sampling Concepts Training Package you will learn typical vertical-sampling concepts as well as the various methods of timing used by sampling oscilloscope systems. Also included in this module is a glossary of sampling terms. Read the Prerequisites, Objectives, and Getting Set before you proceed.

PREREQUISITES

To facilitate study of this instructional module you should first:

1. Complete a course in electronic theory, or the equivalent, in which the following concepts are explained:
   a. TTL (transistor-transistor logic).
   b. CRT (cathode-ray tubes).
   c. Bipolar and field-effect transistors.
2. Complete a course in maintenance of electronic instruments, or the equivalent, in which you have demonstrated:
   a. Safety procedures for operating and servicing electronic equipment.
   b. Procedures for the care and handling of static-sensitive devices.
   c. Soldering techniques for component replacement on multilayer circuit boards.
   d. Proper use of an oscilloscope, multimeter, and digital voltmeter.
   e. Selection and use of tools needed for disassembly of electronic equipment.

OBJECTIVES

To demonstrate successful completion of this instructional module you will:

1. Define commonly used sampling terms.
2. State the effect of dot density upon display reconstruction time in the equivalent-time sampling mode.
3. Name the sampling circuit which minimizes signal kickout and smooths displayed noise.
4. Name the component(s) which maintain the Memory output level.
5. State three factors which control the effective sampling time.
6. State one advantage of a loop gain which is less than unity.
7. Describe what level the Sampling Bridge output should be adjusted to for reduction of strobe-pulse kickout.
8. State one advantage of using dc offset in a vertical sampling circuit.
9. Name the two timing methods used to produce a display successively across the crt from the left to the right.
10. Identify the two signals necessary to produce a coherent sampling display.
11. State one difference between a sampling slewing ramp and a conventional timing ramp.
12. Describe how the sequential mode slewing-ramp slope affects the time per division of the display.
13. Describe the effect of the Trigger Holdoff stage on the sampling ramp signals.
14. Describe the purpose for the staircase voltage in the sequential sampling mode.
15. Identify the signals which cause the vertical input signal and the timing ramp to be sampled in the random sampling mode.

GETTING SET

The Introduction to Sampling Concepts instructional module includes a videotape and this booklet. For maximum learning effectiveness, study this module in the following manner:

1. View the videotape *Sampling Concepts* (Tektronix Part 068-0102-00).
2. Read the remaining sections of this booklet, performing the quizzes as encountered. Check your responses against the answer key.
3. Proceed with the 7S11 Circuit Description instructional module.

In addition to the components of this module provided with this training package, you will require a standard format 3/4-inch video cassette recorder with monitor in order to view the videotape.

CHAPTER 2
SAMPLING CONCEPTS

INTRODUCTION

A sampling system looks at (samples) the instantaneous amplitude of the input signal during a specific small time period, remembers the amplitude, and displays a single dot (data point) on the crt corresponding to the sampled amplitude. After the data point is displayed for a fixed amount of time, the system again samples the instantaneous amplitude of the input signal and displays this sample as the next data point in the display.

The timing between samples determines the type of sampling method being used. In general, real time and equivalent time are the two basic types of sampling. In real-time sampling the data points are taken sequentially, at equal increments in time, and the time taken to complete the display is equal to the time represented by the display. Real-time sampling can usefully display signals only when the signal frequency components are well below the sampling frequency. Real-time sampling is used for acquisition of both single-shot and repetitive signals. See Figure 1.

Equivalent-time sampling is used only for acquiring signals which are repetitive. In sequential equivalent-time sampling each successive sample is taken at a slightly later time in relation to a fixed trigger point on the trigger signal. Generally, the horizontal position of each displayed data point represents the equivalent time when the sample was acquired. After many cycles of the input signal, the sampling system has reconstructed and displayed a single facsimile made up of many samples—each taken from different input cycles. Oscilloscopes using equivalent-time sampling can obtain acquisition bandwidths well above the sampling frequency.

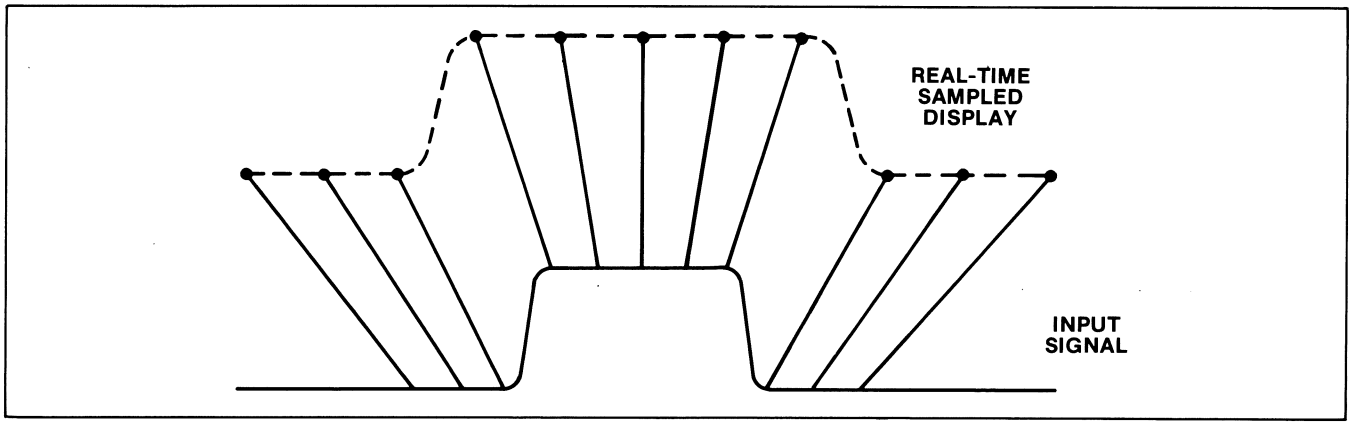


Figure 1. Real-time sampling displays each point as it really occurs in time and requires only one complete sweep.

The timing method used to display the data points may be either sequential or random. With sequential timing, the dots appear on the crt as a very orderly series of equally spaced points; with random timing, successively displayed dots seem to appear randomly across the horizontal axis of the crt. Figure 2 illustrates the two methods of displaying an equivalent-time sampled display. Note that sequential sampling and random sampling are both types of equivalent-time sampling.

DISPLAY AND INPUT SIGNAL CONSIDERATIONS

Dot density, the number of data points per horizontal display division, should be set by the operator for the best compromise between resolution and repetition rate of the display. With equivalent-time sampling only one data point is sampled from any particular input cycle. The time required to fully reconstruct a cycle is a function of the dot density selected and the repetition rate of the input signal. The higher the dot density, the better the resolution of the displayed signal will be; however, the time required to complete the display will now be longer. The higher the repetition rate of the input signal, the less time will be required to reconstruct the waveform. (This is limited by the specified maximum trigger repetition rate of the system.)

Sampling systems have maximum trigger signal repetition rates at which data points can be sampled and accurately displayed. The primary limiting factor for this specification is the time required for the preamplifier and ac amplifier stages to stabilize after a data point has been sampled. For input signals above the specified maximum trigger repetition rate most sampling systems will hold off (delay) retriggering. This means that a data point will not be sampled from every cycle of a high repetition-rate trigger signal. Only those cycles occurring after holdoff will be sampled. However, if the signal is truly repetitive (each cycle being identical), these missed cycles are of little significance.

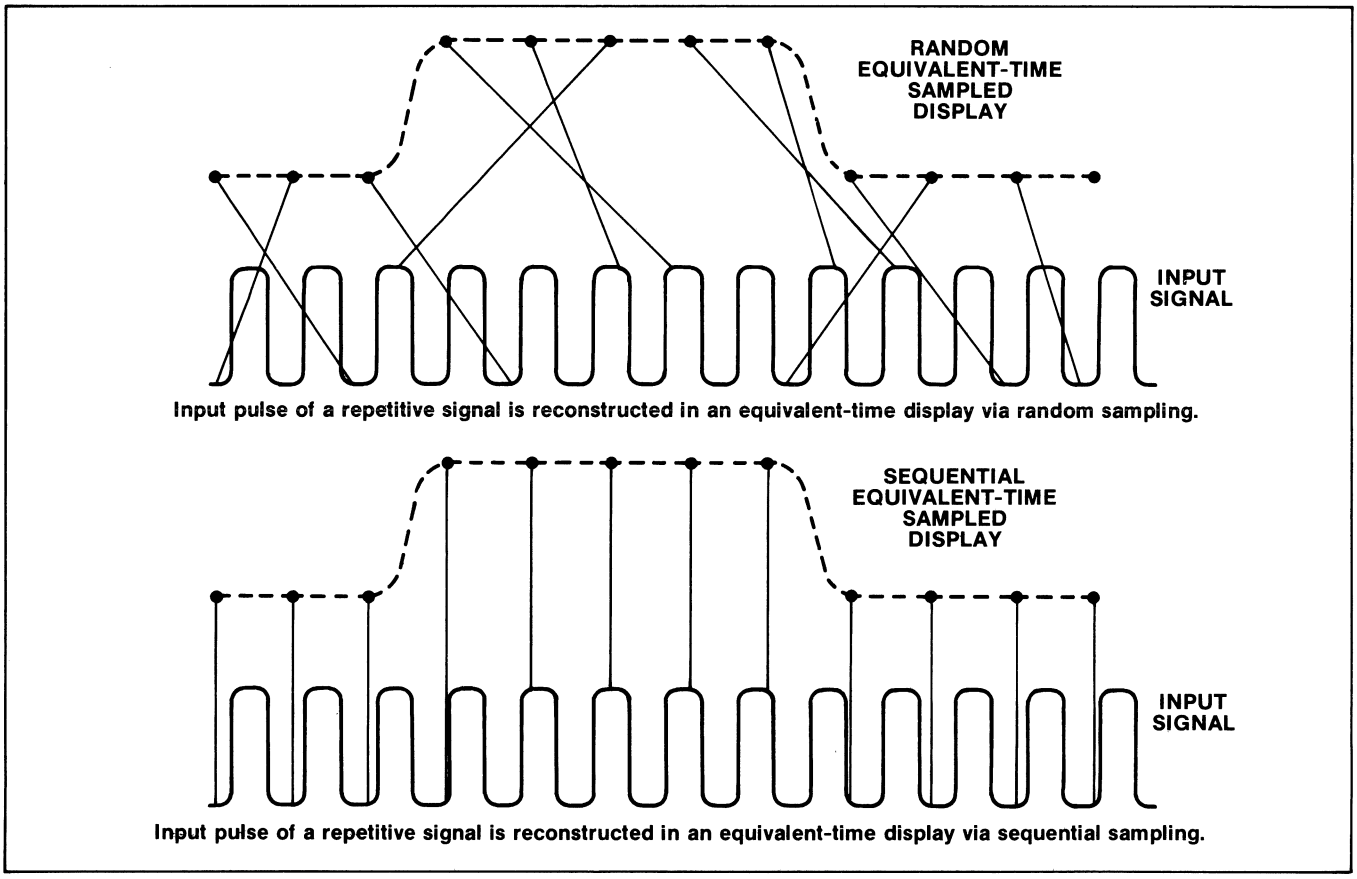


Figure 2. Equivalent-time sampling requires many sweeps of a repetitive signal to form a sampled display.

TYPICAL VERTICAL SAMPLING CONCEPTS

Figure 3 shows a basic block diagram of a sampling circuit such as used in Tektronix sampling oscilloscope systems. This vertical sampling technique allows displayed noise to be smoothed while also minimizing signal kickout into the input cable. With this circuit the sample output from the Memory to the CRT Vertical Amplifier is not reset to zero after each sample; instead, the Memory output remains at the sampled amplitude of the last sample until corrected by the next sample. Since the sample is always the difference between the instantaneous amplitude of the signal at sample time and the previously "memorized" amplitude, this error signal and subsequent kickout are much smaller in amplitude than if the Memory were reset to zero. The Memory output changes only when the error signal from the Sampling Bridge is present, and occurs only during the crt blanking pulse. This ensures that the transition is not visible on the display.

Assume that the output from the Sampling Bridge at sampling time is about 2% of the difference between the input signal voltage and the Memory output. (The actual percentage will vary depending on the input signal.) This 2% error signal is applied to the Preamplifier/Amplifier and is then ac-coupled to the Memory Gate. The Memory Gate, when gated on, couples the error signal to the Memory whose output voltage is changed to equal the signal voltage at the instant of sampling. These changes in Memory output occur while the crt is blanked, and do not show up in the display. The Memory output does not revert to zero, but remains as a fixed voltage until corrected by the next error signal. The percentage of response, or attenuation through the Sampling Bridge, is the sampling efficiency.

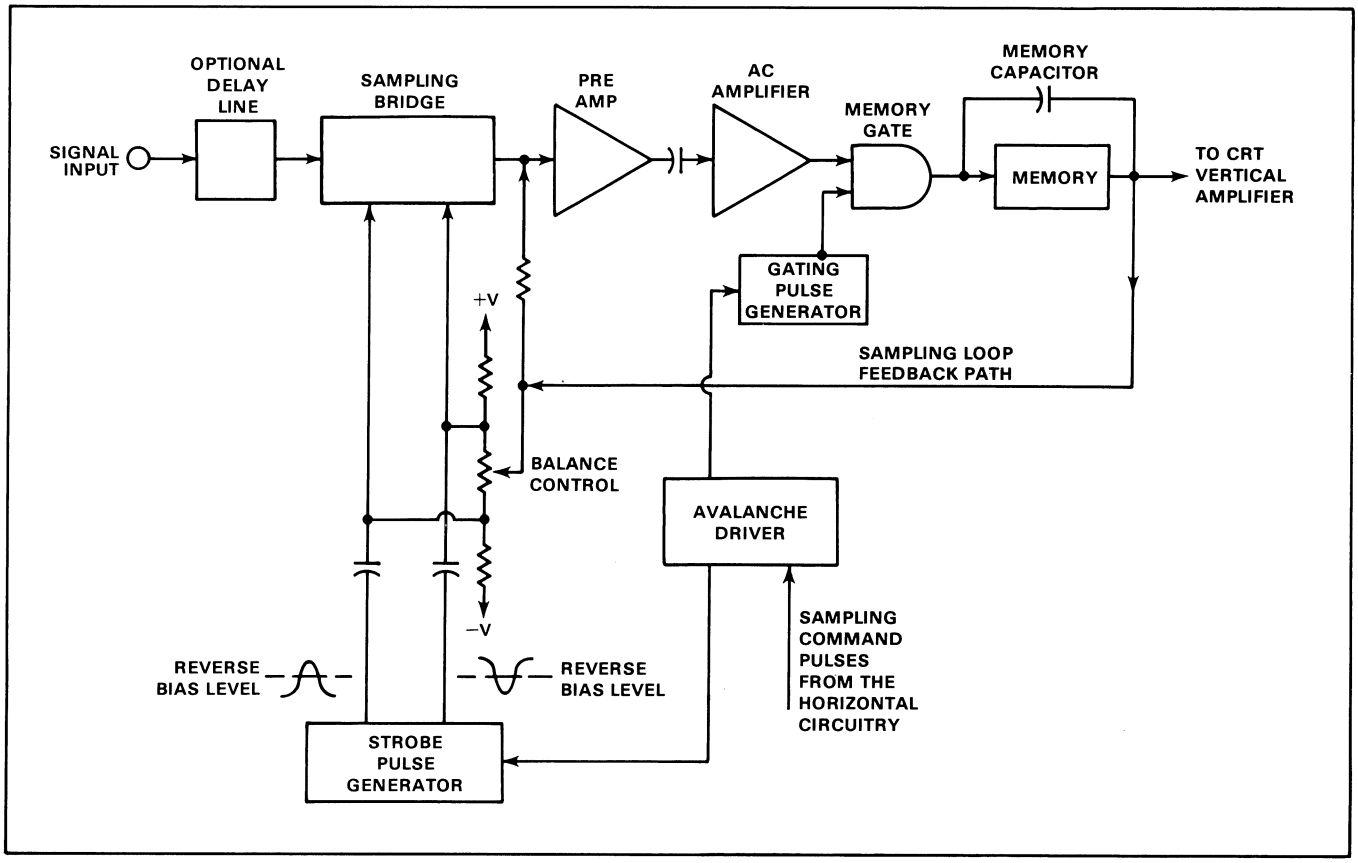


Figure 3. Block diagram of a typical error-sampled feedback system.

ERROR-SAMPLED FEEDBACK OPERATION

The Strobe Pulse Generator of an error-sampled feedback circuit (as shown in Figure 3) is usually driven by a blocking oscillator or a transistor operated in the fast-switching avalanche mode. In turn, this stage is driven by sampling command pulses which originate in the trigger and timing circuits of the sampling oscilloscope. When a sampling command pulse is generated, a strobe pulse is delivered to the Sampling Bridge. The sample is then taken and coupled through the Sampling Bridge, Preamplifier, and Amplifier to the Memory Gate. Typically, the Memory Gate will pass the amplified error signal for about one-third microsecond each time a sampling command pulse is received, compared to a third of a nanosecond, or less, when the Sampling Bridge passes the input signal. This allows a small step voltage (the sample) applied to the input of the Preamplifier to be amplified for a large portion of a microsecond before the Memory Gate is turned off.

The Memory is usually a dc-coupled inverting amplifier with the output fed back to the input through the Memory Capacitor. When the Memory Gate is open (and not allowing the error signal through), the input to the Memory Capacitor is disconnected, providing a very high impedance to ground at the input. This means that whatever voltage is stored in the Memory Capacitor remains essentially constant until another sample is taken. The Memory output applied to the CRT Vertical Deflection circuit is thus held at the sample level until the next sample is taken. The amplifier stages following the Memory are not unique to sampling oscilloscopes and will not be discussed here.

The output signal from the Memory is also fed back to the input of the Preamplifier through an attenuating resistive network. The signal path from the Memory output to the Preamplifier input is part of what is referred to as the Sampling Loop. The Sampling Loop also includes the Sampling Bridge and all amplifying and attenuating stages through to the Memory output. The amplification of the input signal through the Preamplifier/Amplifier and Memory is called "forward gain". The attenuation of the Memory output before it is reapplied to the Preamplifier is called "feedback attenuation". The product of sampling efficiency, forward gain, and feedback attenuation (expressed as gain) is called "sampling-loop gain" and is normally near unity (expressed as "1").

Figure 4 shows the input signal and Memory output voltages for six samples taken along the rising portion of a step waveform. At the time of sample 1, the input signal and the feedback voltage are equal; no change has occurred in the error signal level, so no change occurs in the Memory output. The crt is blanked until the circuit stabilizes after the end of the Memory Gate pulse.

At the time of sample 2 (in Figure 4) the input signal is 0.1 volt. The Memory output is still 0 volt. Assuming a sampling efficiency of 10%, the input of the Preamplifier/Amplifier receives 10% of the signal, or 0.01 volt. The 0.01 volt, times the gain of the Preamplifier/Amplifier stages (X10), corrects the Memory output to equal the 0.1 volt signal at sample time. Again, the crt is blanked during this change until the circuit is stabilized, and is then unblanked to display the new data point.

At the time of sample 3, the input signal voltage is 0.45 volt and the difference between the input signal and the feedback signal is 0.35 volt. The Preamplifier/Amplifier responds to 10% or 0.035 volt, and the gain of this stage changes the signal from the Memory to the new value of 0.45 volt. The Memory output again equals the signal at sampling time and the crt is blanked until the circuit stabilizes.

OPTIONAL DELAY LINE

The Delay Line, if used, is a specially constructed 50-ohm coaxial cable, about 30 to 50 feet long, inserted between the signal input and the Sampling Bridge. (See Fig 3.) Sampling systems with rise times below about 350 picoseconds do not use Delay Lines; but, systems with longer rise times will not always use a Delay Line either. The Delay Line usually delays the input signal about 45 to 75 nanoseconds and will degrade the system response to fast-rising signals. The purpose of the Delay Line is to delay the vertical signal with respect to the trigger signal. This allows the sampling system to sample the input signal prior to the triggering event.

EFFECTIVE SAMPLING TIME

The minimum displayable rise time of a sampling system is controlled by the time interval during which the Strobe Pulse Generator applies forward bias to the Sampling Bridge diodes. The duration of this forward bias is controlled by the time the strobe pulse exceeds a fixed reverse bias. Special circuitry is used to make the strobe duration as short as possible, consistent with noise and diode recovery time. The strobe pulse is often generated by a snap-off diode and a small section of shorted transmission line (called a clipping line) in the Strobe Pulse Generator. The effective bridge conduction time is adjusted primarily by controlling the amplitude and duration of the strobe pulse, thus controlling the time during which the strobe pulse exceeds the reverse bias. Adjusting the reverse bias is a secondary means of controlling the Sampling Bridge conduction time. The reverse bias level is shown by dashed lines through the strobe pulses on Figure 3.

LOOP GAIN

When loop gain is 1, the voltage fed back to the Preamplifier plus the voltage from the Sampling Bridge will equal the input voltage at the time of the sample. This allows the system to track the input signal as closely as possible, resulting in the least possible display distortion. If the loop gain is less than unity, the Memory output signal and the feedback to the Preamplifier is less than necessary to reduce the error voltage to zero. The Memory output and the feedback will then approach the signal level asymptotically. After several samples have been taken, the error voltage approaches zero (for a steady state signal). In the case of a loop gain less than unity, the feedback voltage is effectively a moving average of several preceding samples.

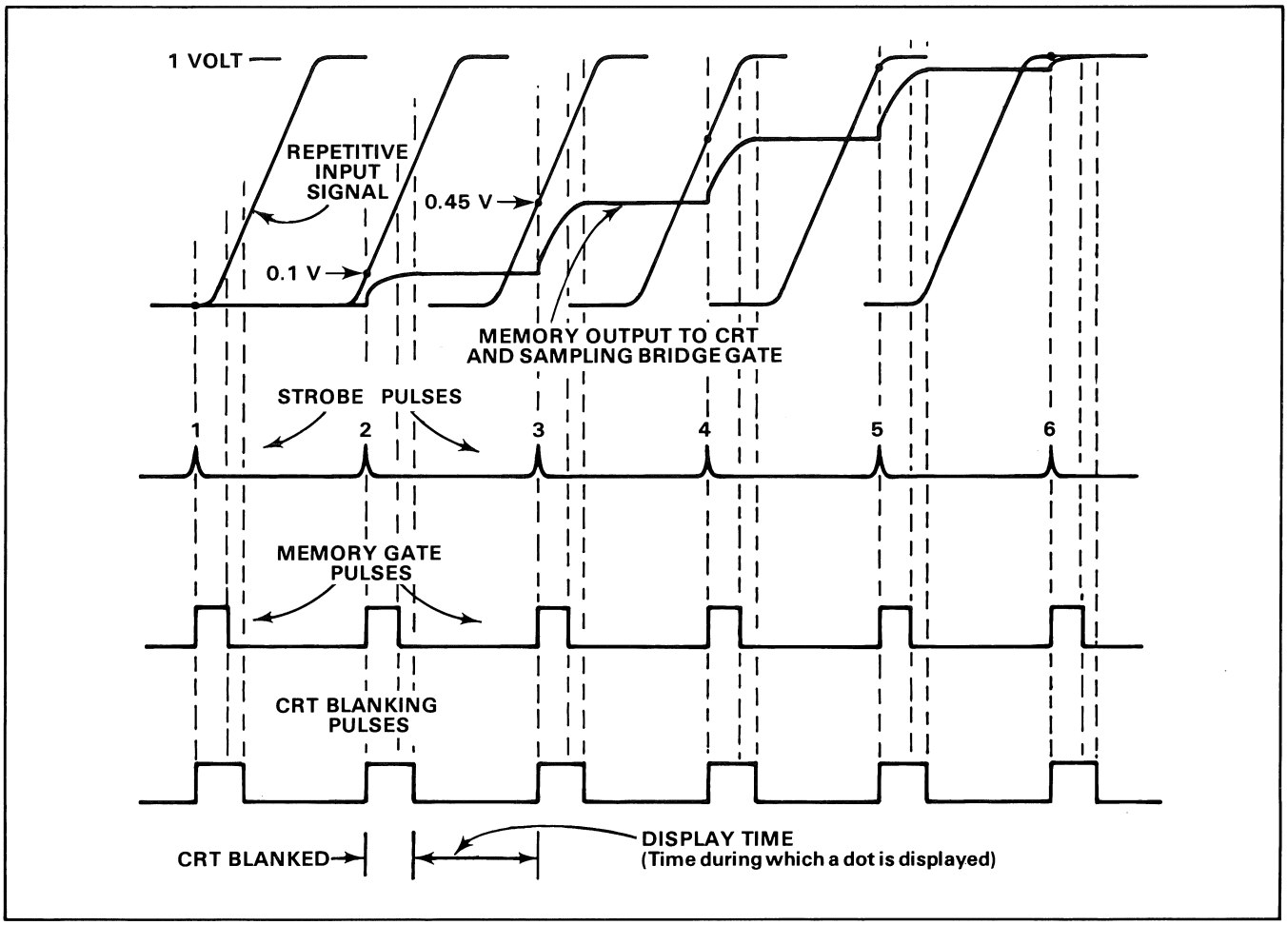


Figure 4. Representation of timing with an error-sampled feedback system.

If the loop gain is greater than unity, the feedback voltage will be greater than the error signal after each sample. The displayed dot sequence of a step signal will then alternately overshoot and undershoot for a few samples.

TRAVELING-WAVE SAMPLING GATE

The sampling system may use a Sampling Gate instead of the Sampling Bridge shown in Figure 3. Figure 5 shows a simplified schematic of a Traveling-Wave Sampling Gate. The input signal is connected to the Preamplifier only during the time a sample is taken. The six diodes form the traveling-wave Sampling Gate.

Step response is determined by the travel time of the strobe pulse through part of the Sampling Gate. In a Sampling Bridge, the step response is determined by the strobe pulse width.

In the traveling-wave gate, part of the input signal is temporarily stored between sampling gate diodes when the strobe pulse ends, and is then fed to the Preamplifier at a slower rate than the step response rise time. The environment is controlled at the input and Sampling Gate to minimize reflections of fast-pulse signals. The environment of following circuitry needs to pass only moderate rate-of-rise signals.

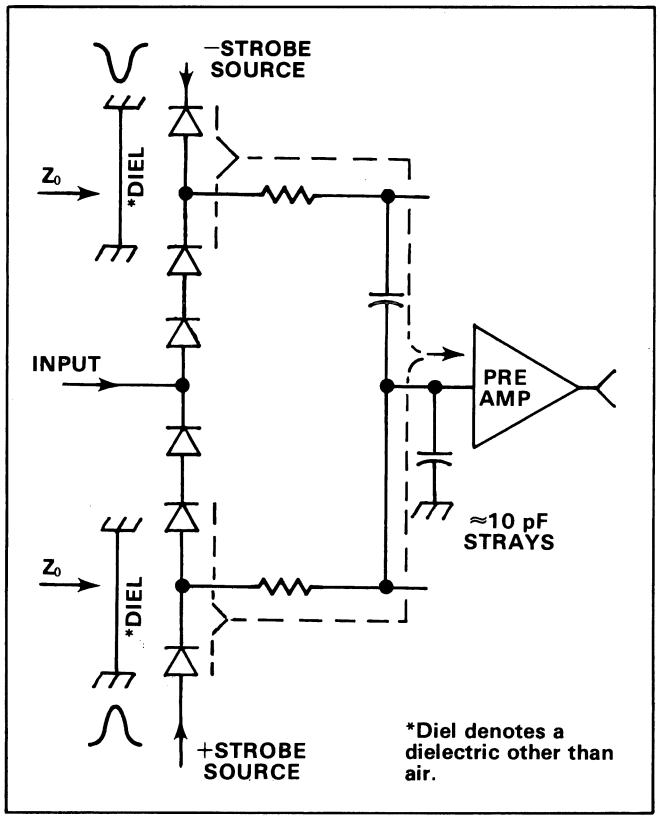


Figure 5. Error-signal source and path through a Sampling Gate.

MIMINIZING STROBE KICKOUT

A minor reason for using the error-sampled feedback circuit is to minimize energy being fed out of the vertical input connector from the strobe pulses that open (enable) the Sampling Bridge or Sampling Gate. How much energy is "kicked out" is partially determined by what the signal voltage is at the time of the sample compared to the voltage at the electrical center of the balanced Sampling Bridge (or Gate). When loop gain is unity, the voltage at electrical center of the Sampling Bridge is always the same as the voltage level of the input signal during the last sample. Most of the time, particularly when using the sequential mode of timing, successive samples represent very small differences in signal voltage level. Therefore, strobe pulse kickout is reduced by continually rebalancing the Sampling Bridge (or Gate) to match the last sampled signal level.

SMOOTHING

Random noise in the sampled display can be reduced by using a loop gain less than unity, resulting in several consecutive samples being averaged. However, this averaging (smoothing) may also slow down the fastest displayable rise time, requiring an increase in the number of dots contained in the pulse edge (step transition). By increasing the number of dots in the step transition, the display will follow the actual input signal more closely.

Figure 6 shows the usual effects of smoothing on a fixed rise-time, sequentially-sampled step display when two different loop gains are used. In Figure 6A, the actual rise time (between the 10% and 90% amplitude points) shows 4 dots for a unity loop gain; however, when operating at 0.3 loop gain, 7 dots are shown in the rise time. This shows a significant difference in the displayed rise time between the two loop gain settings. If the sampling density is increased as shown in Figure 6B, however, only one sample is lost from the step transition when the loop gain is changed from unity to 0.3 (smoothing). When the smoothed mode of a system uses a loop gain of 0.3 (as in the TEKTRONIX 7S11 Sampling Unit), 15 or more samples between the 10% and 90% amplitude points will result in minimum distortion between the smoothed and unsmoothed rise time displays. If the smoothed display contains 12 samples in the step transition, the smoothed rise time will be about 6% longer than for an

unsmoothed display. Always check for sufficient sampling density to warrant smoothing. This can usually be done by changing the dots/division or samples/division control on the timing unit and observing the effect of sampling density on the displayed rise time. Smoothing cannot be applied where the full amplitude of each sample is required, such as in the random sampling mode of the TEKTRONIX 7T11 Sampling Sweep Unit. In this mode the samples are not presented in time sequence and therefore cannot be averaged together.

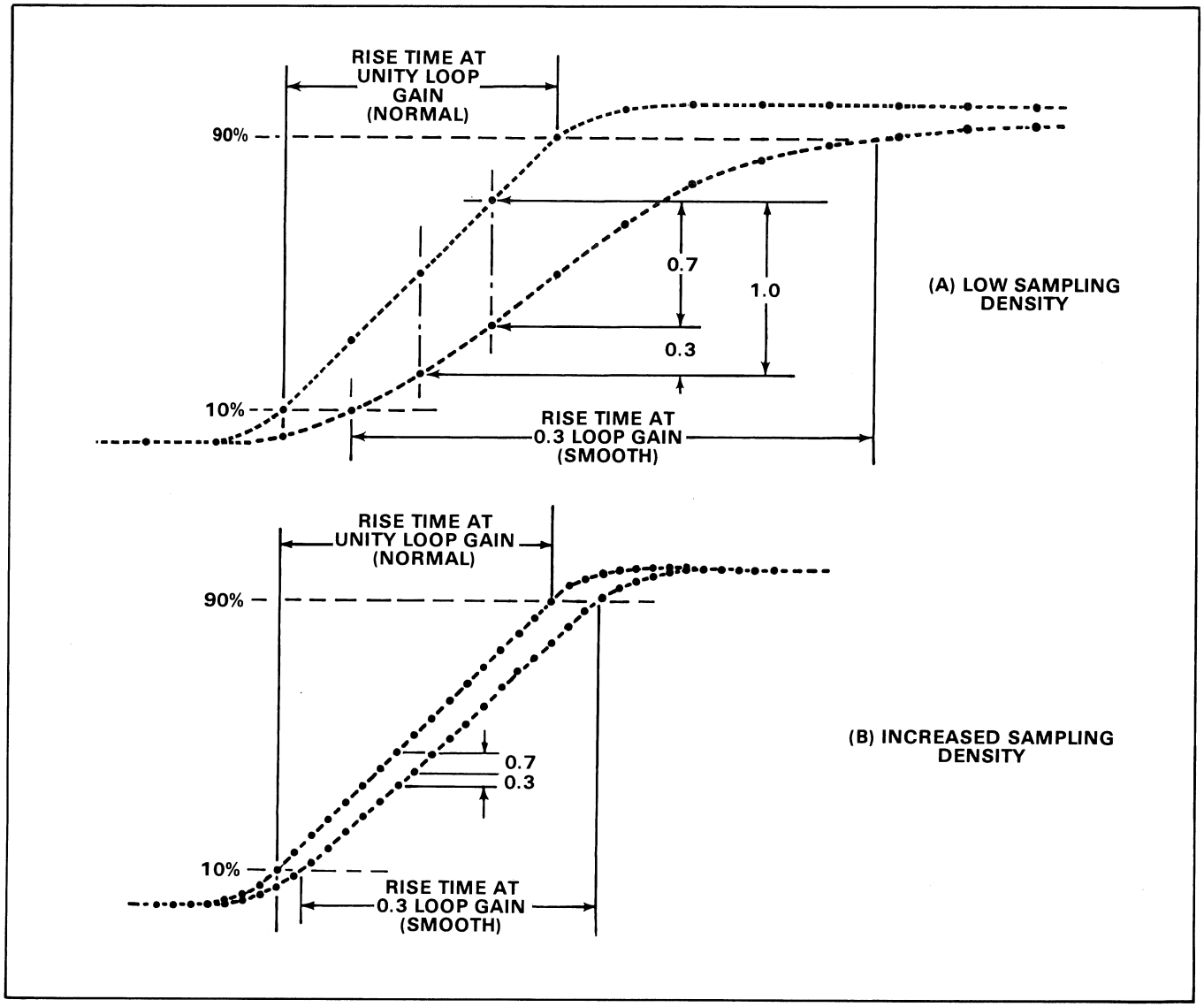


Figure 6. Displayed rise-time differences for smoothed and unsmoothed modes with two different sampling densities.

DC OFFSET

A sampling system which operates on the voltage difference from one sample to the next can inject an offset voltage which allows a small vertical "window" of the input signal to be displayed free from most of the aberrations which occur in overscanned displays associated with conventional oscilloscopes. Figure 7 shows the method used to add a dc offset voltage to the error-sampled memory feedback circuit. The error signal produced at sampling time is no longer referenced to ground. Instead, the error signal is now referenced to the dc offset voltage. This permits portions of the signal (other than ground) to be positioned to the crt center, without altering the selected deflection factor.

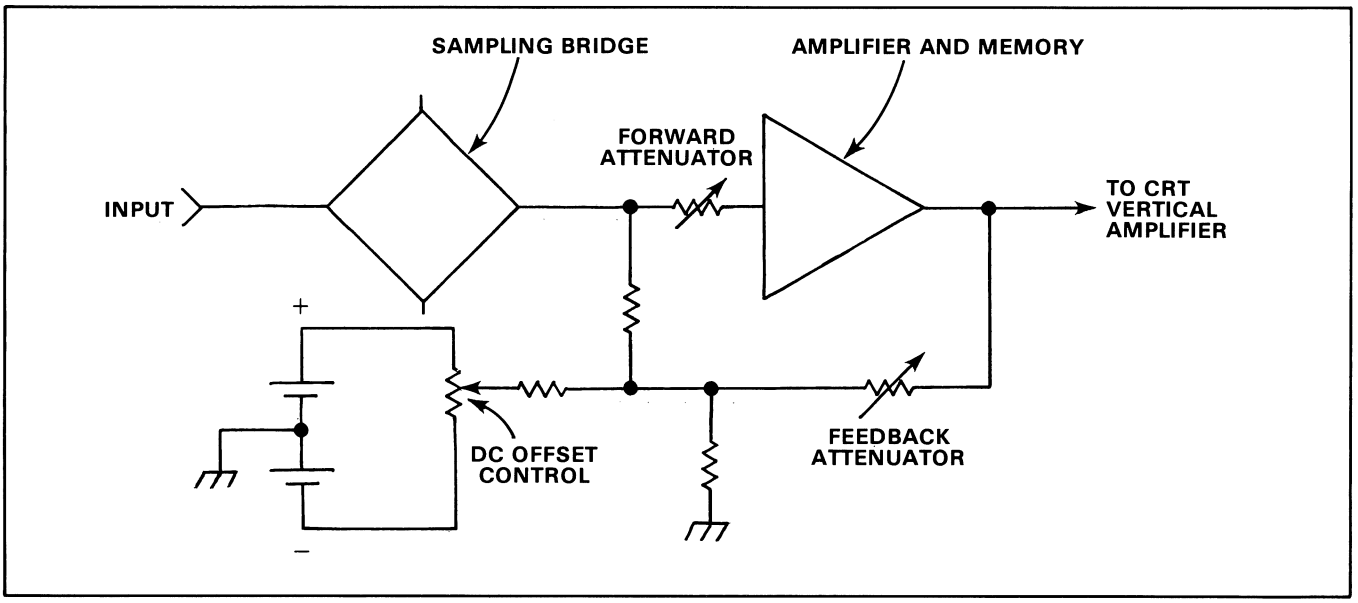


Figure 7. Method of adding dc offset to the sampling loop.

VERTICAL SAMPLING CONCEPTS QUIZ

Perform the following quiz by responding to the questions while you cover the shaded answer column. Then check your responses against the answers provided to the right of the questions.

1. Each displayed dot on a sampling oscilloscope reflects the _____ voltage level of the input signal at the time of sampling. a. average, in the smoothed display b. instantaneous, in nonsmoothed displays c. both a and b d. none of the above	1. (c) In the smoothed mode the average voltage level of the input signal is displayed, and in nonsmoothed modes the instantaneous voltage level of the input signal is displayed, by the sampling oscilloscope.
2. The type of sampling method used can be determined by the _____ between the samples. a. timing b. voltage difference c. signal frequency d. all of the above	2. (a) The type of sampling method being used is determined by the timing between samples. Real-time sampling is taken sequentially and the dots forming any given event in the display are generated by that unique event. Equivalent-time sampling is taken from a repetitive waveform and at successively later points on separate cycles of the signal.
3. Dot density is the number of dots per _____. a. graticule. b. vertical display division. c. horizontal display division.	3. (c) Dot density is the number of dots displayed per horizontal graticule division.
4. The higher the dot density, the _____ the displayed resolution and the _____ the time required to reconstruct the input signal (equivalent-time mode). a. worse, longer b. worse, better c. better, longer d. better, shorter	4. (c) In equivalent-time displays the higher the dot density is set, the better the displayed resolution will be. However, the oscilloscope will now require more time to reconstruct the display.
5. The _____ allows displayed noise to be smoothed and also minimizes the signal kickout. a. Strobe Pulse Generator b. Sampling Bridge c. Sampling Gate d. Error-Sampled Feedback Circuit	5. (d) Using an error-sampled feedback circuit to obtain the vertical sample will reduce the signal kickout and allow any noise on the signal to be smoothed.

6. The Memory output normally changes level while the crt is _____. a. unblanked. b. blanked.	6. (b) The output level of the Memory is only changed while the crt is blanked, this avoids the appearance of an unstable display.
7. Feedback through the _____ maintains the output of the Memory until the sample level changes. a. Memory Gate b. Sampling Loop c. Memory Capacitor d. Resistive Divider Network	7. (c) Whenever the Memory Gate is not allowing the error signal to pass, the input to the Memory Capacitor is disconnected. This provides a very high impedance to ground at the input to the Memory, maintaining the output level across the Memory and Memory Capacitor.
8. Sampling-loop gain is the product of: a. forward gain. b. feedback attenuation. c. sampling efficiency. d. all of the above.	8. (d) Sampling-loop gain is the product of forward gain through the Preamplifier/Amplifier and Memory, feedback attenuation from the Memory to the Preamplifier, and the sampling efficiency.
9. A Delay Line will _____ the response of fast-rising signals, as well as delay the input signal. a. improve b. degrade	9. (b) A Delay Line will degrade the system response to fast-rising signals.
10. The effective sampling time is controlled by adjusting: a. the duration of the strobe pulse. b. the reverse bias on the Sampling Bridge. c. the amplitude of the strobe pulse. d. all of the above.	10. (d) The effective sampling time is controlled directly by the time the Strobe Pulse applies forward bias to the Sampling Bridge diodes. Therefore, indirectly the amplitude of the Strobe Pulse and the setting of the reverse bias on the Sampling Bridge diodes also control the effective sampling time.
11. With a loop gain less than unity, signal _____ occurs. a. overshoot or ringing b. smoothing or averaging c. noise increase d. aberration prior to the rising edge	11. (b) When the loop gain is less than unity the voltage fed back to the Preamplifier from the Memory is not enough to reduce the error voltage to zero. The error voltage thus approaches zero only after several samples, effectively averaging or smoothing the signal.

12. Strobe pulse kickout is reduced by adjusting the Sampling Bridge output voltage to: a. equal the signal voltage at the time the first sample is taken. b. not equal the signal voltage at the time the first sample is taken. c. equal the signal voltage at the time the last sample is taken. d. not equal the signal voltage at the time the last sample is taken.	12. (c) Usually, successive samples represent very small differences in signal voltage level; therefore, kickout can be reduced by continually rebalancing the Sampling Bridge to match the level of the last sample taken.
13. _____ permits portions of the signal to be positioned to the crt center _____ altering the deflection factor. a. DC offset, by b. DC offset, without c. Error signals, by d. Error signals, without	13. (b) By applying a dc offset voltage, portions of the signal which would otherwise overscan the display can be positioned to the crt center without altering the selected deflection factor.

CHAPTER 3
TIMING METHODS

SEQUENTIAL-MODE TIMING

In the sequential mode of timing samples, each successively displayed dot is produced from left to right in a very orderly manner across the crt screen. Therefore, each new sample of the vertical signal should be from a successively later point on the repetitive vertical input signal.

A basic block diagram of the horizontal circuit of a sampling oscilloscope in the sequential sampling mode is shown in Figure 8. Shown in Figure 9 are the timing relationships important in this mode. Refer to these illustrations throughout the following discussion.

Sampling oscilloscopes, like conventional oscillosopes, require a triggering signal in order to form a coherent display from the input signal. The block diagram in Figure 8 shows a portion of the input signal diverted to the Trigger Recognition stage via the Trigger Slope Selection. However, most sampling systems make provisions for an external trigger to be applied to the Slope Selection stage instead of a portion of the vertical input signal. This permits greater flexibility in triggering requirements.

The Trigger Recognition circuit responds to a suitable trigger, whether the source is internal or external, and generates a fast step-signal which initiates a ramp. This ramp can be called a "fast ramp", "timing ramp", or "slewing ramp" and is similar to the sweep ramp produced in a conventional oscilloscope. However, an important difference between the slewing ramp of a sampling system and the timing ramp of a conventional oscilloscope is that the slewing ramp is not used, either directly or after amplification, to produce crt deflection. Nevertheless, the slewing ramp is a primary factor in determining the horizontal time/division in a sequential sampling time-base unit. If the slope of the slewing ramp is steepened, the time/division is reduced; any nonlinearities in the slewing ramp will produce a nonlinear time scale. The slewing-ramp process is analogous to sampling a section of the timing ramp of a conventional oscilloscope and using those samples to produce horizontal deflection. However, in the sequential sampling mode, even though the horizontal position of each displayed dot is not determined by a sample of a timing ramp, each sample does correspond to a different point on a timing ramp.

The Trigger Holdoff stage prevents the premature initiation of a new slewing ramp before the full recovery of the last one. By holding off the triggering signal each slewing ramp can fully recover and be ready to start again before a new one can possibly be triggered. Changing the setting of the Time/Division control may change one or several of the following:

1. The capacitance of the Slewed Ramp stage which determines the slope of the slewing ramp.
2. The capacitance of the Trigger Holdoff stage which, with the Recovery Time control, determines how much a given triggering signal will be counted down.
3. The setting of the Display Magnifier control for the horizontal amplifier.
4. The setting of the Time Magnification control inserted between the Staircase Inverter and the Attenuator.

Whenever the slewing ramp reaches the level of the attenuated and inverted voltage applied to the Comparator from the Staircase Inverter, a pulse is produced by the Comparator. These pulses are referred to as slewed pulses because each successive pulse is slightly later than the previous one with respect to any given point in a cycle of the trigger signal. As this implies, each successive pulse from the Comparator is delayed one increment more than the former pulse with respect to the beginning of each slewing ramp. Generally, these slewed pulses are referred to as "sampling command pulses". The sampling command pulses strobe the Sampling Bridge as previously described.

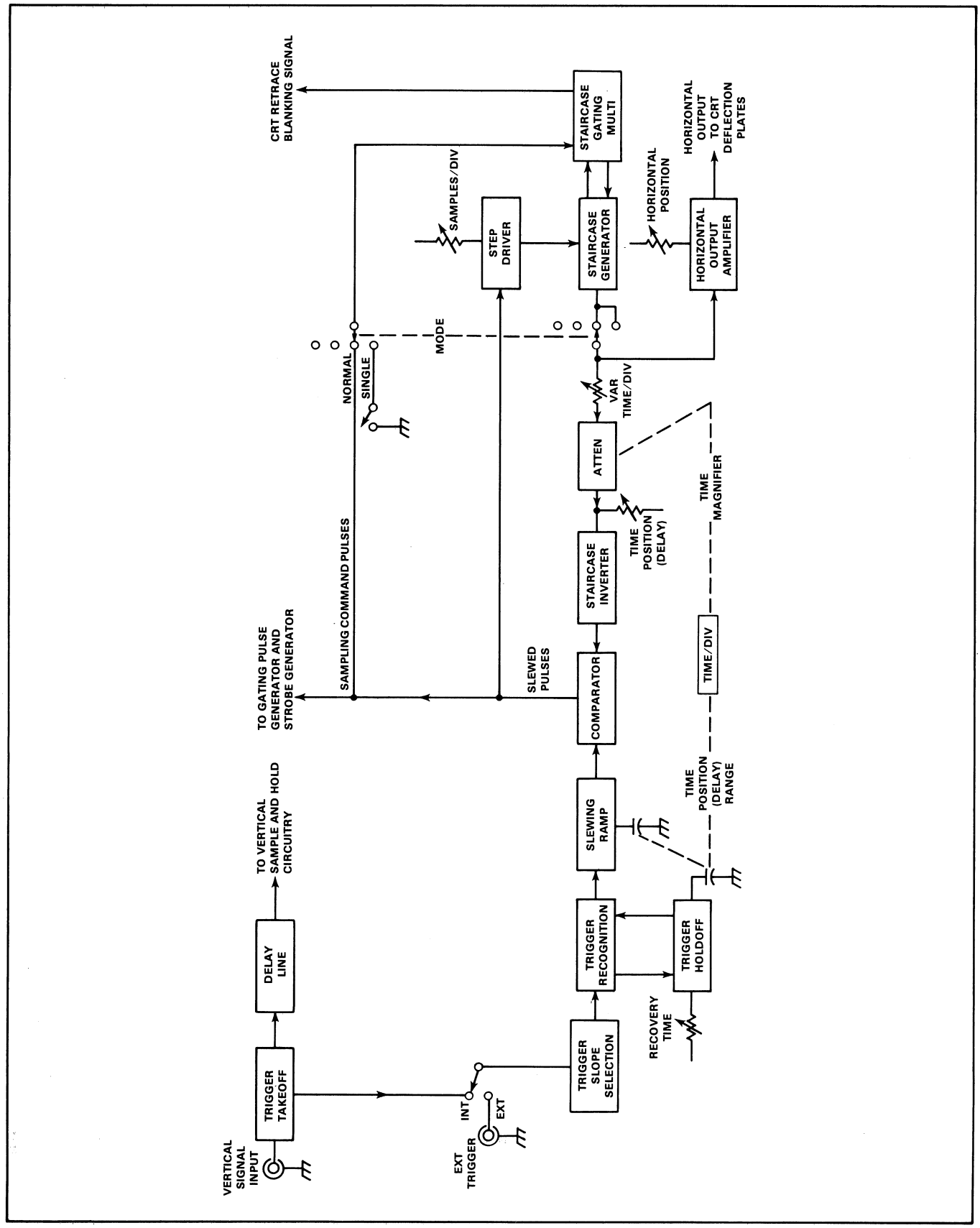
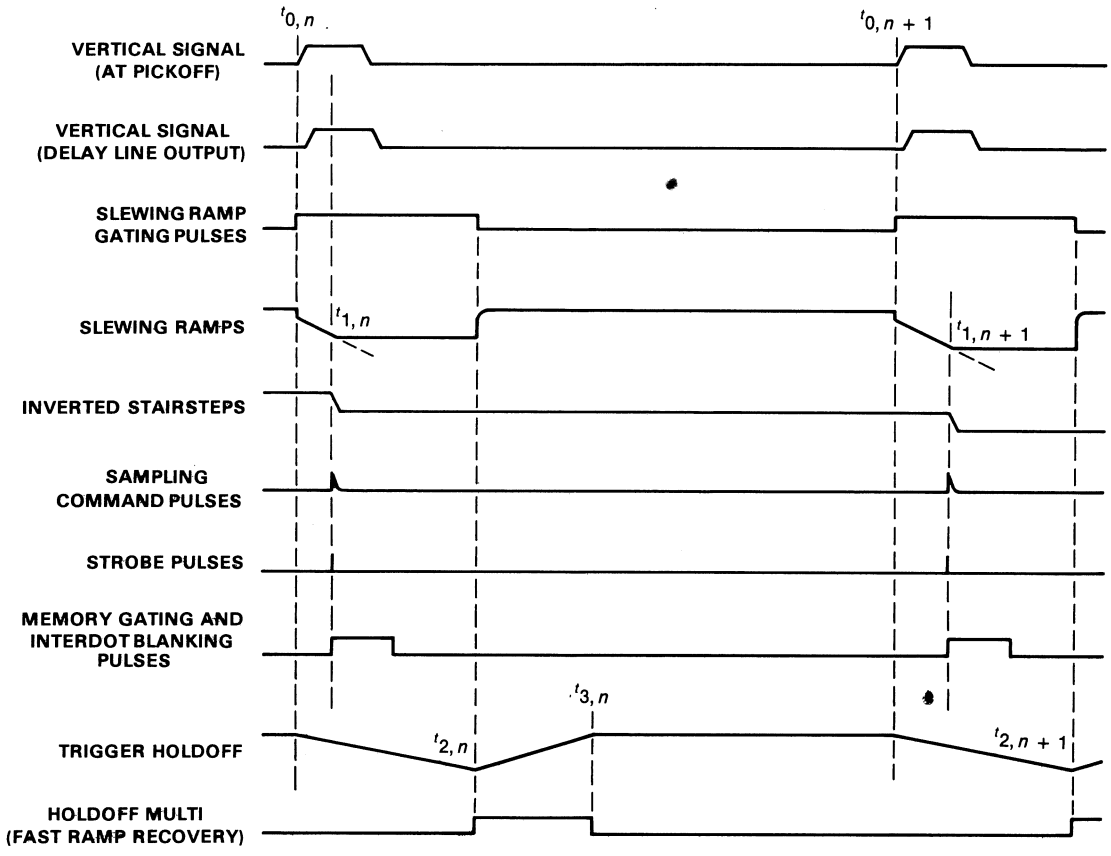


Figure 8. Horizontal block diagram of sequential-mode sampling.

The sampling command pulses are also applied to the Step Driver inside the horizontal deflection circuitry. The Staircase Gating Multi initiates a staircase voltage signal which is stepped once by each sample command of the Step Driver. After the staircase has reached sufficient amplitude, the Staircase Gating Multi stops the staircase and allows it to recover. The Staircase Generator, which is started and stopped by the Staircase Gating Multi, produces the positive-going horizontal deflection signal and an advancing set of comparison voltage levels which are attenuated and inverted before being applied to the Comparator.

A new lower staircase level is generated for the Comparator each time a slewing ramp voltage crosses the existing staircase level and retraces. (Refer to Fig 9.)

The instant when each ramp crosses a new staircase level is slightly later than the last since, because each staircase level into the Comparator is lower than the one before, the ramp must drop further to reach the new level. After the staircase voltage reaches the amplitude necessary to produce full-scale horizontal deflection, the Staircase Gating Multi turns off the Staircase Generator and allows it to recover. Any slewing ramps generated during the time the Staircase Generator is recovering will cause sampling command pulses to be produced. The samples taken as a result of these sampling command pulses will not be shown on the crt screen because the Staircase Gating Multi blanks the crt during this horizontal retrace period.



t_0 - The instant when the triggering signal initiates a slewing ramp. Each ramp runs down until it reaches the level of the existing inverted stairstep.

t_1 - The instant when a slewed ramp reaches the existing inverted stairstep level. At time t_1 a sampling command pulse, a strobe pulse, and a memory gating pulse are initiated, and the staircase advances one step.

t_2 - Slewing ramp starts to recover.

t_3 - Trigger holdoff interval ends.

Figure 9. Sequential-mode timing diagram.

RANDOM-MODE TIMING

Random sampling is one of the basic modes of timing used in sampling oscilloscopes and requires a previous understanding of the sequential mode. Figure 10 shows a basic block diagram of the horizontal deflection circuits and Figure 11 shows the signal timing involved in the random-timing mode. Refer to these illustrations throughout the following discussion.

In random sampling the sampling command pulses are not precisely synchronized with the input signal cycles, resulting in dots occurring on the display either to the left or right of the previous sample. The dots laid down on the display, therefore, appear to be at random compared to those produced in the sequential mode. The degree of randomness is a function of signal-period jitter and the inherent random-sampling circuitry jitter. The advantage of random sampling is in the way the signal can be viewed ahead of the trigger recognition point, usually on the leading edge of a pulse, without the use of vertical signal delay lines or an externally-applied pretrigger signal. Unlike conventional oscilloscopes, in random sampling oscilloscopes we use a system of automatically measuring the input signal repetition rate to produce delayed triggers which occur at the same, or a submultiple of the same, rate. Once the trigger signal repetition rate is known by the repetition-rate measuring circuitry (ratemeter), appropriate circuitry starts a timing ramp just prior to arrival of the next trigger. The start of this timing ramp corresponds to the start of the display, allowing the display to start before the actual trigger event.

The display is generated by sampling both the vertical signal and a triggered linear timing ramp each time a dot is to be displayed on the screen. Because each timing ramp is triggered by the same point in each cycle of the sampled signal, the proper X and Y coordinates for each dot are available at the output of the Vertical Memory and Horizontal Memory.

In the random mode, two kinds of sampling command pulses are generated. (Refer to Figure 10.) One kind goes to the vertical deflection circuit to cause the vertical signal to be sampled, the other (referred to as "ramp stop pulses") stays in the horizontal deflection circuit to cause the timing ramps to be sampled. In the sequential mode, only the vertical signal was sampled, not the timing ramp.

Two types of fast ramps are produced in the random mode: (1) The timing ramps which help determine the time per division of the horizontal scale, and (2) the slewing ramps which produce various increments of delay so that all portions of the signal are sampled and displayed. In both the sequential and the random mode, the instant when the timing-ramp triggering signal is recognized defines the trigger recognition point (t_0). Whether the timing-ramp triggering signal is a portion of the vertical input signal or an externally applied triggering signal is immaterial at this point.

The Trigger Recognition and Trigger Holdoff stages are common to the random and sequential modes of operation. The primary signal out of the Trigger Recognition stage is the step signal which initiates the timing ramp in the Timing Ramp Generator. (This also is common with the sequential mode of operation, except the timing ramp was referred to as the slewing ramp.) The Slewing Ramp Generator initiates the slewing ramp which drives the Slewing Ramp Comparator. The voltage levels against which the slewing ramps are compared are negative levels which arrived from the output of the Staircase Inverter. The Staircase Inverter is driven by a positive-going staircase, which is first attenuated before being applied to the Staircase Inverter. Unlike in sequential sampling, the Staircase Generator does not produce horizontal deflection in the random-sampling mode. The sole purpose of the Staircase Generator now is to help the slewing ramps produce sampling command pulses and ramp stop pulses to sample all portions of the vertical signal and timing ramps. The Staircase Gating Multi and Step Driver perform as previously described for the sequential mode.

The slewing ramp is a negative-going ramp which produces two pulses every time the slewing ramp occurs. The first pulse emerges from the Slewing Ramp Comparator and is called the sampling command pulse, and the second emerges from the Leadtime Comparator and is called the ramp stop pulse. The sampling command pulses always cause the vertical input signal to be sampled and the ramp stop pulses cause the timing ramp to be sampled. The pulse edge from the Lead time Comparator stops the timing ramp at whatever voltage the ramp had reached at the moment the pulse edge occurred. This level remains constant until the timing ramp gating pulse ends and the ramp starts to recover. The stopped amplitude of each timing ramp is a good sample of the amplitude that existed at the moment the stop ramp pulse arrived from the Lead time Comparator. The difference between the instant when each sampling command pulse is generated and the subsequent instant when each timing ramp stop pulse is generated determines the lead time. (Lead time is the amount of time ahead of the trigger recognition point that we may sample and display the vertical signal.) Adjustment of the Leadtime Offset control deter-

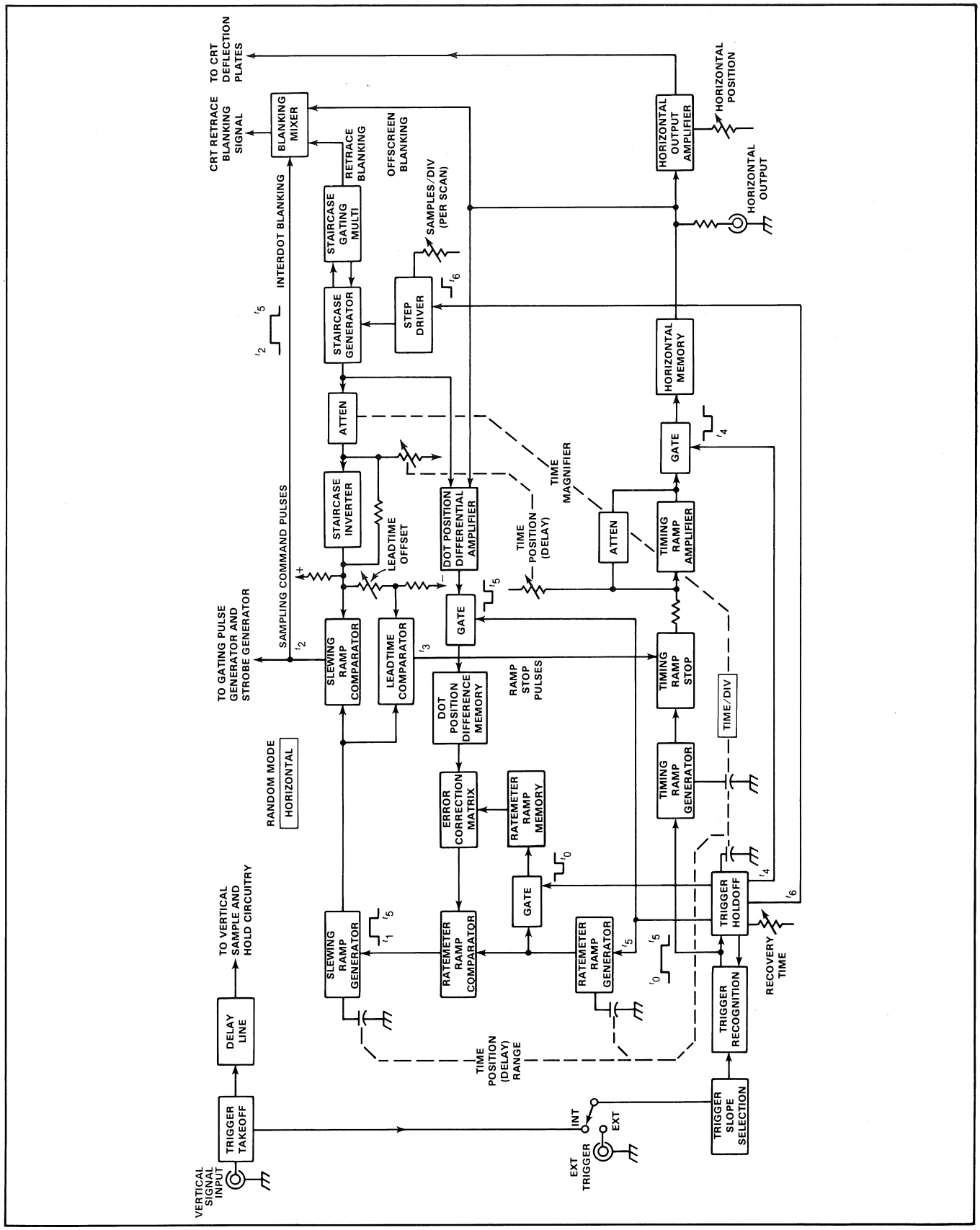


Figure 10. Horizontal block diagram of random-mode sampling.

mines the difference in time between the generation of a sampling command pulse and the generation of a ramp stop pulse.

Each stopped timing ramp is amplified and inverted by the Timing Ramp Amplifier and applied to the Horizontal Memory. The output of the Horizontal Memory, after being amplified by the Horizontal Output Amplifier, determines the horizontal position of any dot on the screen. Under ideal circumstances the dots simulate the appearance of the sequential mode, where they are laid down from left to right in equal steps from the output of the Staircase Generator. But the horizontal position of any dot in the random mode is controlled only by the voltage at the output of the Horizontal Memory.

When a sample of the vertical signal precedes a sample of the timing ramp signal by the same amount every time the two signals are sampled, the display will be as correct as if the pairs of samples always occurred simultaneously. The difference will be that a sample of the signal taken prior to the trigger recognition point on the vertical signal may now be displayed. (Samples taken after the trigger recognition point may also be part of the display.)

Six of the blocks shown in Figure 10 are concerned solely with the generation of presignal triggers. These six blocks are the Ratemeter Ramp Generator, Ratemeter Ramp Memory, Ratemeter Ramp Comparator, Error Correction Matrix, Dot Position Differ-

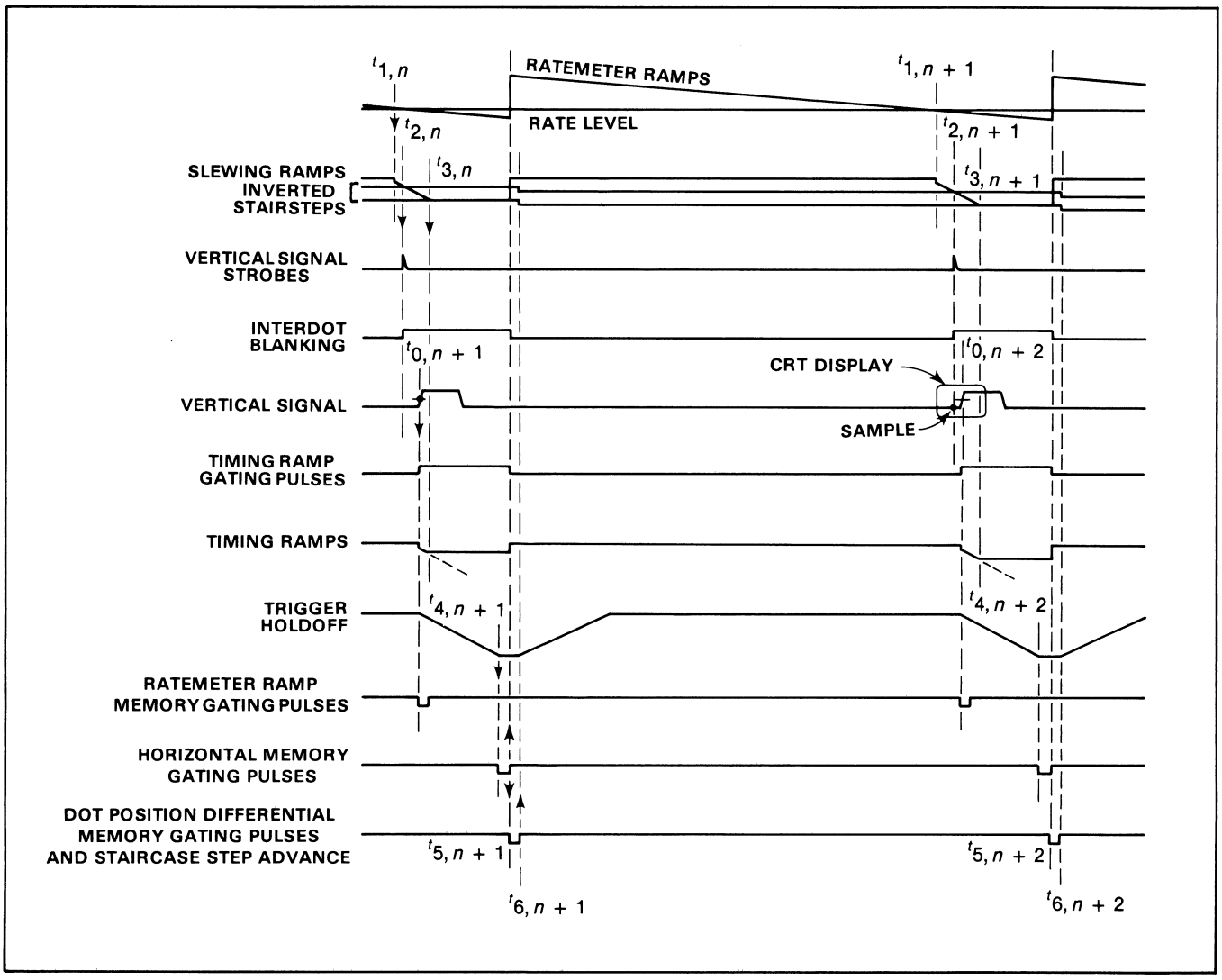


Figure 11. Random-mode timing diagram.

ence Memory, and the Dot Position Differential Amplifier. In every normal sampling cycle the order of events occurs at the times specified by t_0, t_1, t_2, t_3, t_4, t_5, and t_6 in both Figure 10 and 11. The order or occurrence of times t_1 through t_6 is always the same; however, t_0 may occur either before or after time t_1 in any sampling cycle. This means that all pulses generated at times t_1 through t_6 depend on the generation of the previous trigger recognition point (t_0). Time t_0 is the master time reference point for each sampling cycle. The pulse edge which occurs at time t_0 initiates a timing ramp and causes the existing ratemeter ramp level to be gated into the Ratemeter Ramp Memory.

At time t_1 the ratemeter ramp crosses the level applied from the Error Correction Matrix to the Ratemeter Ramp Comparator. The pulse edge initiated at this time causes a slewing ramp to be started. Ideally, time t_1 is a stable pretrigger point which occurs well before time t_0 in this particular sample cycle. (In the first sampling cycle, no events occur at t_1, t_2, or t_3.)

Time t_2 occurs when the slewing ramp crosses the level of the staircase signal applied to the Slewing Ramp Comparator from the Staircase Inverter. The pulse edge initiated at this time causes the vertical signal to be strobed and sampled.

When the slewing ramp crosses the lower negative offset level riding on the output of the Staircase Inverter, time t_3 occurs. At this time the pulse edge is generated to stop the timing ramp. This level is amplified and held until time t_4 occurs. At time t_4 the stopped level of the timing ramp is gated into the Timing Ramp Amplifier and into the Horizontal Memory. Time t_5 occurs in the middle of the holdoff cycle when the Timing Ramp Generator, Slewing Ramp Generator, and the Ratemeter Ramp Generator are reset. Also at time t_5 the voltage applied from the Dot Position Differential Amplifier is gated into the Dot Position Difference Memory. At time t_6 the Staircase Generator is advanced one step and the holdoff cycle is complete.

The ratemeter ramp range may last 1000 times as long as the time range of the time position control. Whenever a ratemeter ramp is initiated, as with the generation of a pulse edge at time t_5 from the Trigger Holdoff stage, the ramp starts a slow rundown until the next similar pulse edge at time t_5. At this time the ratemeter ramp resets and starts over again at the same slope. The Ratemeter Ramp Amplitude is a function of the trigger recognition rate. This rate may not be the same as that of the triggering signal if the triggering signal is a high-frequency signal and trigger countdown is occurring. The ratemeter ramp is applied to the Ratemeter Ramp Comparator and to the Ratemeter Ramp Memory. The amplitude of the ratemeter ramp at time t_0 is stored in the Ratemeter Ramp Memory. This amplitude will be an unchanging dc level if the trigger recognition rate is a very constant frequency. If the frequency decreases, the ramp amplitude increases and the rate level increases in the negative direction. The level out of the Ratemeter Ramp Memory is mixed with another level in the Error Correction Matrix and the combination is applied to the Ratemeter Ramp Comparator for its reference level.

Because the reference level to the Ratemeter Ramp Comparator is slightly higher than the output from the Ratemeter Ramp Memory, the negative-going ratemeter ramp will cross this reference level sooner than if it had to run all the way down to the level of the Ratemeter Ramp Memory.

When the ratemeter ramp reaches this reference level, an output pulse is generated by the Ratemeter Ramp Comparator which initiates a slewing ramp in the Slewing Ramp Generator. Since the level at the output of the Ratemeter Ramp Memory is the amplitude of the ratemeter ramp at time t_0, the pulse from the Ratemeter Ramp Comparator will normally occur ahead of each new time t_0. This is the pretrigger pulse.

The pretrigger pulse occurs at time t_1 and starts the slewing ramp. Remember that the pulse generated at time t_1 occurs as a result of events in the previous sampling cycle and, in this way, can occur prior to time t_0 in any particular sampling cycle.

The slewing ramp produces an output pulse at the Slewing Ramp Comparator and then at the Leadtime Comparator. Remember that the first pulse causes the vertical signal to be sampled, and the second pulse causes the timing ramp to be sampled. Because the Slewing Ramp Comparator and the Leadtime Comparator both have changing reference levels fed to them from the Staircase Inverter, each of the pairs of pulses produced by each slewing ramp occurs at a different point in each cycle. This slewing function follows the same pattern as previously described in the sequential mode of operation, the only difference being that now we start to slew from a point ahead of the trigger recognition.

The output of the Staircase Generator, which corresponds to a particular spot on the horizontal scale, is applied as one input to the Dot Position Differential Amplifier. The other input to the Dot Position Differential Amplifier is the output of the Horizontal Memory.

Typically, the horizontal position of any displayed dot may differ from the position that dot would have if it had been positioned by the Staircase Generator alone. Therefore, the polarity and the magnitude of the voltage from the Horizontal Memory will affect the dc level from the Dot Position Difference Memory and the Error Correction Matrix to correct for possible error caused by the pulse from the Staircase Generator alone. A change in the dc level applied as the reference voltage to the Ratemeter Ramp Comparator will cause the pretrigger signal to occur correspondingly earlier or later to minimize the error.

To avoid jitter in the display, the crt beam must be blanked at least between the time when a new sample is placed in the Vertical Memory and a corresponding sample is placed in the Horizontal Memory. Actually the beam is blanked a little longer than that. The beam is blanked from the vertical signal sampled at time t_2, through the last moment when the timing ramp is sampled (t_5), during the time the Staircase Generator is recovering, and any time when output from the Horizontal Memory would otherwise place a sample off the display screen.

REAL-TIME MODE TIMING

Real-time sampling extends the capabilities of sampling oscilloscopes so they may display slow-changing as well as fast-changing voltages. The time required for a complete horizontal sweep using either sequential or random sampling is invariably much longer than the time represented by 10 divisions at the selected time per division of the horizontal scale. Therefore, the sequential and random modes are referred to as equivalent-time sampling because the time per division of the horizontal scale is equivalent to a much shorter interval than actually taken for the crt beam to traverse one division. In the real-time mode the horizontal beam velocity equals the time per division of the horizontal scale.

The type of real-time sampling shown in Figure 12 requires an accurate gated clock. This method uses a staircase sweep and the time between steps is precisely clocked. Each step in the staircase sweep corresponds to one sample of the signal, the same as for equivalent-time sampling modes. However, real-time sampling permits us to sample many points in each signal cycle. Time intervals are measured by counting the dots between two points on the signal. A 1000-dot sweep corresponds to 100 dots per division.

By comparing Figures 8 and 12 we can see that a few circuit functions are the same in the real-time and sequential modes of operation. One difference is that the Trigger Holdoff interval does not expire in the real-time mode until a sweep is completed. Also, in the real-time mode we do not generate slewing ramps and we only trigger once per sweep.

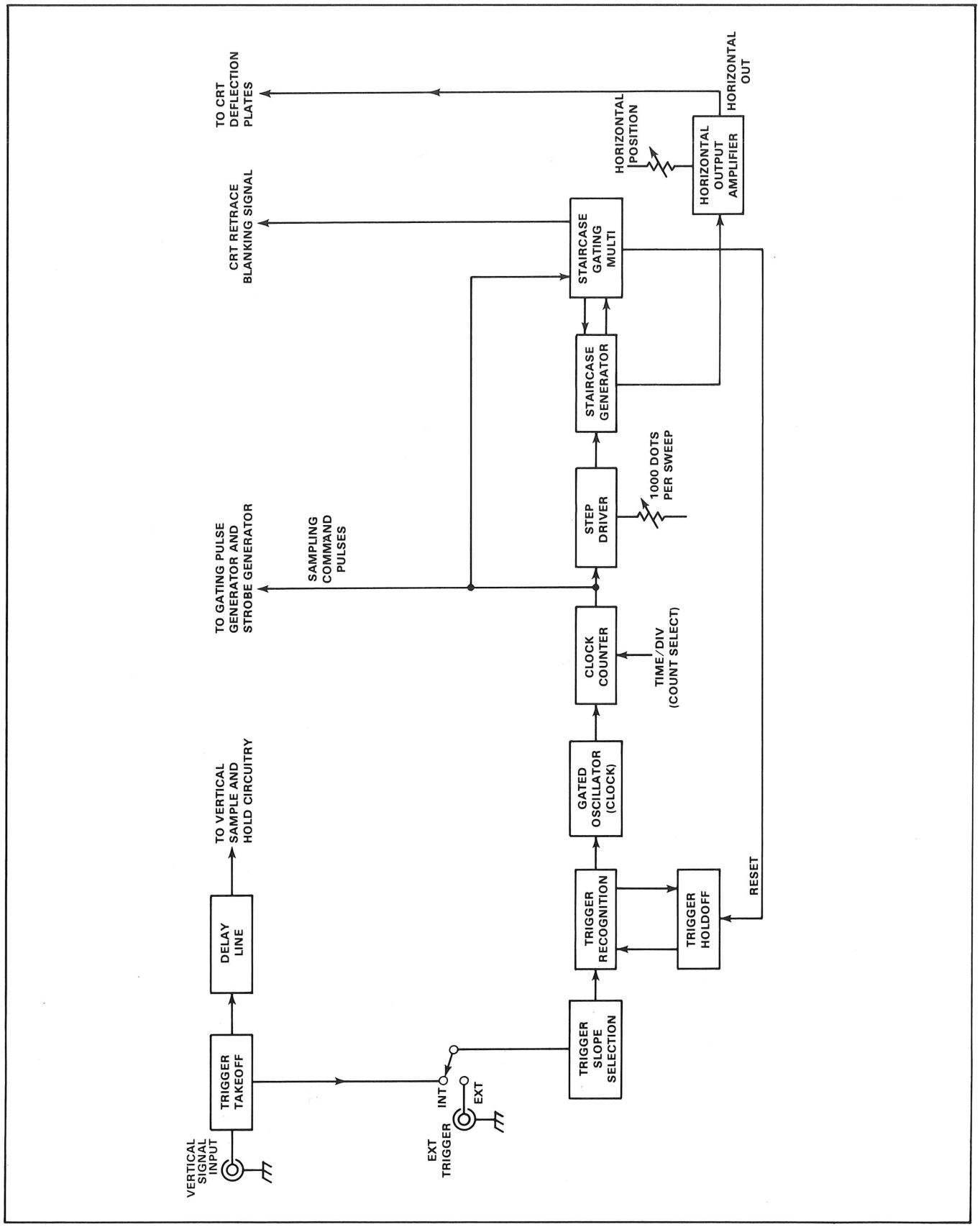


Figure 12. Horizontal block diagram of real-time sampling.

TIMING METHODS QUIZ

Perform the following quiz by responding to the questions while you cover the shaded answer column. Then check your responses against the answers provided to the right of the questions.

1. In the _____ mode of sampling, the displayed dots are produced successively from the left edge of the graticule to the right. a. random b. sequential c. real-time d. both b and c	1. (d) In all sampling modes but random the dots are displayed sequentially across the crt display screen from left to right.
2. To produce a coherent display, sampling oscilloscopes require _____ signals. a. input b. triggering c. both a and b d. ratemeter	2. (c) A coherent display can only be produced with a triggering signal and a vertical input signal.
3. One difference between a sampling oscilloscope slewing ramp and a conventional oscilloscope timing ramp is: a. the slewing ramp produces crt deflection before amplification. b. the slewing ramp does not determine the time per division in a sequential sampling mode. c. the slewing ramp does not produce crt deflection. d. none of the above.	3. (c) The slewing ramp of a sampling oscilloscope is never used to produce crt deflection.
4. When the slope of the sequential mode slewing ramp is _____, the time per division is _____. a. lowered, increased b. steepened, increased c. lowered, reduced d. steepened, reduced	4. (d) Steepening the slope of the slewing ramp will reduce the time per division by shortening the time required to reach the desired amplitude on the slewing ramp.

5. The Trigger Holdoff stage prevents the premature start of the: a. fast ramp. b. slewing ramp. c. timing ramp. d. all of the above.	5. (d) The slewing ramp can also be referred to as the fast ramp or the timing ramp. In any case, the Trigger Holdoff circuit prevents the slewing ramp from starting again until the last one has fully recovered.
6. In the sequential sampling mode, the time-of-sample is incremented through the input signal by the: a. staircase voltage. b. slewing ramp. c. blanking signal. d. none of the above.	6. (a) The staircase voltage effectively increments the time-of-sample through the vertical signal by delaying each slewing ramp a little more than the last one.
7. The degree of randomness in the random sampling mode display is a function of the: a. input signal amplitude. b. input signal repetition rate. c. timebase and signal jitter. d. none of the above.	7. (c) Jitter in the input signal and the jitter inherent in the Ratemeter are displayed as the randomness of the display.
8. In the random mode, the _____ pulses cause the vertical input signal to be sampled, and the _____ pulses cause the timing ramp to be sampled. a. ramp stop, staircase b. staircase, ramp stop c. sampling command, staircase d. sampling command, ramp stop	8. (d) The sampling command pulses always cause the sampling of the vertical level of the input signal and the ramp stop pulses cause the sampling of the timing ramp. Both must be sampled to produce an accurate reconstruction of the input signal.
9. The random mode allows lead time when viewing the input signal. Lead time is: a. the time between the generation of the sampling command pulse and the generation of the timing ramp stop pulse. b. the time ahead of the trigger recognition point that the signal can be sampled. c. both a and b. d. the time between the start of the display and the first sample.	9. (c) Lead time, the time difference between the sampling command pulse and the timing ramp stop pulse, also refers to the time ahead of the trigger recognition point that the signal can be sampled.

10. In real-time sampling, the horizontal beam velocity _____ the time per division of the horizontal scale. a. equals b. lags c. leads d. is determined by	10. (d) In real-time sampling, which is used primarily for single-sweep and low-speed waveforms, the horizontal velocity of the crt beam is determined by the time per division of the horizontal scale. The horizontal beam velocity is the reciprocal of the time per division.

CHAPTER 4
GLOSSARY OF TERMS

The terms listed in this glossary are commonly used in sampling discussions and are defined here for your convenience.

balanced sampling gate

A type of sampling gate arranged so that strobe currents are balanced to minimize kickout.

baseline drift

Vertical movement of the entire trace under constant signal conditions and control settings.

baseline shift

Vertical movement of the entire trace initiated by a change-of-signal condition or control setting; usually reaches an equilibrium state more rapidly than baseline drift.

blowby

A display aberration resulting from signal-induced displacement current through all capacitance shunting the sampling gate. Character of the aberration depends on the circuit time constants affecting redistribution of the displacement charge.

coherent display

A display in which the time sequence of signal events is preserved. A coherent display may be produced by either random or sequential sampling.

countdown

The process of responding to only every nth recurrence of the signal, in a circuit receiving a recurrent triggering signal, where "n" is an integer which may or may not be constant.

display magnifier

A control or circuit whose function is to decrease the sweep time-per-division of a display by increased gain in the horizontal amplification system.

display window

The particular time interval represented within the horizontal limits of the crt graticule.

dot

A displayed spot indicating the horizontal and vertical coordinates of a particular sample.

dot density

The number of dots per horizontal division.

dot slash

Dot elongation due to memory or staircase leakage.

dot transient response

The ability of a sampling oscilloscope to correctly display voltage change between any two successive samples. Good dot transient response requires unity loop gain.

dynamic range

The ratio of the specified maximum input-signal capability to the noise value.

equivalent time

The time scale represented in the display of a sampling oscilloscope operating in the equivalent-time sampling mode.

equivalent-time sampling

Sampling process in which at least one repetitive signal event is required for each sample taken. The time required for display construction is thus greater than the time represented in the display.

false display

A sampling display allowing faulty or ambiguous interpretation, usually caused by insufficient dot density or improper triggering.

feedback attenuation

In a sampling loop, the effective intersample attenuation in the signal path between memory output and input sampling gate.

feedback attenuator

A circuit causing feedback attenuation. In a sampling oscilloscope, the control which determines vertical deflection factor and, with the forward attenuator, maintains constant loop gain.

forward attenuator

A circuit which determines forward gain, normally ganged with the feedback attenuator.

forward gain

The effective gain in a sampling loop between the input sampling gate output and memory output.

kickout

A signal emanating from an input connector.

lead time

The maximum time interval which may be displayed prior to the trigger recognition point.

loop gain

The product of sampling efficiency, forward gain, and feedback attenuation in a sampling loop. Loop gain is normally unity, except in a smoothed display where it will be less than unity.

memory

A circuit which stores the vertical or horizontal coordinate value of the sample.

memory gate

Electronic switch between a memory and its driving amplifier.

offset monitor

A connector which provides an output voltage proportional to the internal dc offset voltage of a sampling system.

pretrigger

A trigger signal which occurs before a related signal event.

random sampling

A sampling process involving significant time-interval uncertainty between the signal and the sample-taking operation. Also the process of coherent display construction from such randomly-taken samples. This process may be employed by either real-time or equivalent-time sampling oscilloscopes.

random sampling oscilloscope

An oscilloscope employing the random sampling process together with means for constructing a coherent display from the randomly-taken samples.

real time

The time scale associated with signal events.

real-time sampling

A sampling process in which more than one sample is taken for each signal event. The time required for display construction is the same as the time represented in the display.

reflection coefficient (rho)

The ratio of peak amplitude of a particular reflection to the incident-step amplitude in time-domain reflectometry. In practice, the observed reflection coefficient may depend upon system rise time, losses in the associated transmission medium, and the nature of reflection-producing discontinuity.

sample distribution

In a random sampling oscilloscope, a function of equivalent time which describes how the density of randomly-placed samples varies across the signal.

sampling

A process of sensing and storing one or more instantaneous values of a signal for further processing or display.

sampling command

A trigger or other electrical signal intended to initiate or cause sampling.

sampling efficiency

The ratio of the voltage change between the instant before sampling (t^-) and the instant after sampling (t^+) at the output of a sampling gate to the difference between gate input voltage (E_i) and gate output voltage (E_o) at the instant before sampling.

$$\text{Sampling Efficiency} = \frac{E_o(t^+) - E_o(t^-)}{E_i(^-) - E_o(t^-)}$$

sampling gate

An electronic switch which conducts briefly upon command for the purpose of collecting and storing the instantaneous value of a signal.

sampling loop

Those circuits providing the main signal path through the input sampling gate, amplifiers, forward gain attenuator, memory gate, memory, feedback attenuator, and back to the sampling gate.

sampling oscilloscope

An oscilloscope which employs sampling together with means for constructing a coherent display of the samples taken.

scanning

The process by which slewing is controlled. In an equivalent/time sampling oscilloscope, usually governed by a relatively slow staircase or ramp, manual control, or externally-derived signal.

sequential sampling

A sampling process in which samples are taken at successively later times relative to the trigger-recognition point.

slewing

The process of causing successive samples to be taken at different instants relative to the trigger-recognition point.

slewing ramp

A linear ramp which acts with a slower staircase, ramp, or other changing voltage to cause slewing.

slideback

A measurement process by which the value of a known is varied and compared with an unknown until they are equal (null).

smoothed display

A display produced by a sampling loop employing smoothing.

smoothing

A process affecting dot transient response intended to reduce the effect of random noise or jitter in the display.

strobe

A pulse of short duration which directly operates the sampling gate.

tangentially-measured noise

A noise value determined by a tangential-noise measurement.

tangential-noise measurement

A procedure to determine displayed noise wherein a flat-top pulse or square-wave input signal is adjusted in amplitude until the two traces (or portions of two traces) thus produced appear to be immediately adjacent or contiguous. Measurement of the resulting signal amplitude determines a noise value which correlates closely with the value interpreted by the eye from a sampling display and is called the tangential noise value.

time domain reflectometry

The technique of launching a pulse or step signal into a transmission medium with subsequent analysis of any reflections thus produced.

time magnifier

A control which acts to alter the equivalent-time scale without an accompanying change in dot density.

time position

The equivalent-time relationship between the start of the time window and the trigger-recognition point.

time-position range

The equivalent-time interval over which the start of the time window may be positioned by the time-position control. The time-position range normally starts before the trigger-recognition point in a random-sampling oscilloscope and with, or shortly after, the trigger-recognition point in a sequential-sampling oscilloscope. (This assumes no delay line.)

time window

The particular equivalent-time interval over which signal events can be described by usable samples.

trigger pickoff

A device or circuit intended to extract a portion of the input signal for purposes of triggering the display.

trigger recognition

The process of responding to a suitable triggering signal.

trigger-recognition point

The point in time at which trigger recognition occurs, also that point on a displayed waveform representing the instant of trigger recognition.

usable samples

Those samples containing signal information which is within the operating range of the sampling loop.

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