Service Manual

Tektronix

2780 Series
Spectrum Analyzers

070-8244-02

This document supports the 2782 with serial numbers B020000 and above and the 2784 with serial numbers B010100 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

Please check for change information at the rear of this manual.

First Printing: September 1993
Revised: October 1993

Instrument Serial Numbers

Each instrument manufactured by Tektronix has a serial number on a panel insert or tag, or stamped on the chassis. The first letter in the serial number designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B010000	Tektronix, Inc., Beaverton, Oregon, USA
E200000	Tektronix United Kingdom, Ltd., London
J300000	Sony/Tektronix, Japan
H700000	Tektronix Holland, NV, Heerenveen, The Netherlands

Instruments manufactured for Tektronix by external vendors outside the United States are assigned a two digit alpha code to identify the country of manufacture (e.g., JP for Japan, HK for Hong Kong, IL for Israel, etc.).

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

Printed in U.S.A.

Tektronix®

REVISION INFORMATION

Manual Part No. 070-8244-02 **First Printing** SEP 1993

Product: 2780 Series Spectrum Analyzer **Revised** OCT 1993

Manual Insert Status

DATE	CHANGE REFERENCE	STATUS
FEB 92	M74830	Effective
FEB 92	M74994	Effective
FEB 92	M76047	Effective
FEB 92	M76442/M76592	Effective
JUN 92	M75651	Effective
JUN 92	M77752	Effective
MAR 93	M78775	Effective
MAY 93	M74839	Effective
MAY 93	M79172	Effective
AUG 93	M74844	Effective
AUG 93	M78548	Effective
AUG 93	M74844	Effective
AUG 93	M79321	Effective
SEP 93	M79897	Effective
OCT 93	M75640	Effective
OCT 93	M80134	Effective
OCT 93	M80269A	Effective

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MANUAL CHANGE INFORMATION

Date: 02-03-92 **Change Reference:** M74830

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBER: B020389

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

CIRCUIT NUMBER	PART NUMBER	DESCRIPTION
A24	670-9447-03	CIRCUIT BOARD ASSY:DIGITAL STORAGE

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MANUAL CHANGE INFORMATION

Date: 02-03-92 **Change Reference:** M74994

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBER: B020413

MECHANICAL PARTS LIST CHANGE

CHANGE TO:

FIGURE & INDEX	QTY	PART NUMBER	DESCRIPTION
2-42	1	333-3313-02	FRONT PANEL MARKER

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MANUAL CHANGE INFORMATION

Date: 02-03-92 **Change Reference:** M76047

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBER: B020267

MECHANICAL PARTS LIST CHANGE

CHANGE TO:

FIGURE & INDEX	QTY	PART NUMBER	DESCRIPTION
2-1	1	337-0925-02	SHIELD GASKET,ELEC

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MANUAL CHANGE INFORMATION

Date: 02-14-92 **Change Reference:** M76442/M76592

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBER: B020388

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

CIRCUIT NUMBER	PART NUMBER	DESCRIPTION
A12	119-2743-06	CONVERTER ASSY:MAGNETICALLY TUNED

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MANUAL CHANGE INFORMATION

Date: 06-01-92 **Change Reference:** M75651

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBERS:

2782 B020438
2784 B010119

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

CIRCUIT NUMBER	PART NUMBER	DESCRIPTION
A5	621-0038-07	POWER SUPPLY ASSEMBLY
A5A2	670-9451-03	CIRCUIT BOARD ASSY:SECONDARY POWER SUPPLY

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MANUAL CHANGE INFORMATION

Date: 06-03-92 **Change Reference:** M77752

Product: 2780-Series Service **Manual Part No:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE SERIAL NUMBER: 2782 B020425
2784 B010118

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

CIRCUIT NUMBER	PART NUMBER	DESCRIPTION
A41	670-9463-03	CIRCUIT BOARD ASSY:MAIN PROCESSOR ASSEMBLY

MECHANICAL PARTS LIST CHANGE

CHANGE TO:

FIG. & INDEX	PART NUMBER	DESCRIPTION
6-10	671-0727-01	CKT BOARD ASSY:PROCESSOR EXTENDER BOARD

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MANUAL CHANGE INFORMATION:

Date: 01–MAR–93 **Change Reference:** M78775

Product: 2780–Series Service **Manual Part No.:** 070-8244-02

DESCRIPTION **Product Group 2E**

EFFECTIVE FOR SERIAL NUMBERS:

2782	B020477 and up
2784	B010143 and up

Change Replaceable Mechanical Parts to:

REMOVE:

FIG. & INDEX	PART NUMBER	DESCRIPTION
2–39	131–4328–00	CONN,RF ADPT PLANAR CROWN:26.5 GHZ

ADD:

FIG & INDEX	PART NUMBER	DESCRIPTION
2–39	131–4328–01	CONN,RF ADPT PLANAR CROWN:40.0 GHZ

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MANUAL CHANGE INFORMATION

Date 13-MAY-93 Change Reference: M74839

Product: 2780-Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrum Analyzer B020477 and above
2784 Spectrum Analyzer B010149 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A28	672-0195-05	CKT BOARD ASSY:PERIOD COUNTER

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A28	672-0195-06	CKT BOARD ASSY:PERIOD COUNTER

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MANUAL CHANGE INFORMATION

Date 13–MAY–93 Change Reference: M79172

Product: 2780–Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrun Analyzer B020477 and above
2784 Spectrum Analyzer B010147 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A16	644–0631–16	VR MODULE ASSEMBLY

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A16	644–0631–17	VR MODULE ASSEMBLY

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MANUAL CHANGE INFORMATION:

Date: 01-AUG-93 **Change Reference:** M74844

Product: 2780-Series Service **Manual Part No.:** 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782	B020477 and up
2784	B010141 and up

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A17	119-2938-05	PHASE LOCK ASSY:MICROWAVE

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A17	119-2938-06	PHASE LOCK ASSY:MICROWAVE

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MANUAL CHANGE INFORMATION:

Date: 01-AUG-93 **Change Reference:** M78548

Product: 2780-Series Service **Manual Part No.:** 070-8244-02

DESCRIPTION **Product Group 2E**

EFFECTIVE FOR SERIAL NUMBERS:

2782	B020477 and up
2784	B010143 and up

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A22	670-9448-04	CKT BOARD ASSY:DISPLAY AMP

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A22	670-9448-05	CKT BOARD ASSY:DISPLAY AMP

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MANUAL CHANGE INFORMATION:

Date: 01-AUG-93 **Change Reference:** M74844

Product: 2780-Series Service **Manual Part No.:** 070-8244-02

DESCRIPTION **Product Group 2E**

EFFECTIVE FOR SERIAL NUMBERS:

2782	B020477 and up
2784	B010141 and up

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A17	119-2938-05	PHASE LOCK ASSY:MICROWAVE

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A17	119-2938-06	PHASE LOCK ASSY:MICROWAVE

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MANUAL CHANGE INFORMATION

Date 31-AUG-93 Change Reference: M79321

Product: 2780-Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrun Analyzer B020492 and above
2784 Spectrum Analyzer B010159 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A12	119-2743-06	CONVERTER ASSY:MAGNETICALLY TUNED (2782 ONLY)
A12	119-4249-00	CONVERTER ASSY:MAGNETICALLY TUNED (2784 ONLY)

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A12	119-2743-07	CONVERTER ASSY:MAGNETICALLY TUNED (2782 ONLY)
A12	119-4249-01	CONVERTER ASSY:MAGNETICALLY TUNED (2784 ONLY)

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MANUAL CHANGE INFORMATION

Date 15-Sept-93 Change Reference: M79897

Product: 2780-Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrum Analyzer B020493 and above
2784 Spectrum Analyzer B010171 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A24U11	160-5825-04	PRGM EPROM,27C1024,VER2.6
A41U63	160-5824-06	PRGM EPROM,27C1024,VER2.6
A41U63	160-7465-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A42U40	160-5826-03	PRGM EPROM,27C1024,VER2.6
A42U40	160-8501-03	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A43U10	160-5823-06	PRGM EPROM,27C1024,VER2.6
A43U10	160-7460-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A43U11	160-5819-06	PRGM EPROM,27C1024,VER2.6
A43U11	160-7461-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A43U12	160-5820-06	PRGM EPROM,27C1024,VER2.6
A43U12	160-7462-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A43U13	160-5821-06	PRGM EPROM,27C1024,VER2.6
A43U13	160-7463-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)
A43U14	160-5822-06	PRGM EPROM,27C1024,VER2.6
A43U14	160-7464-04	PRGM EPROM,27C1024,VER2.6 (OPTION 16 ONLY)

Product: 2782 & 2784 Service **Date:** 16–SEP–93 **Change Reference:** M79897

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A24U11	160-5825-05	PRGM EPROM,27C1024,VER2.7
A41U63	160-5824-07	PRGM EPROM,27C1024,VER2.7
A41U63	160-7465-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A42U40	160-5826-04	PRGM EPROM,27C1024,VER2.7
A42U40	160-8501-04	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U10	160-5823-07	PRGM EPROM,27C1024,VER2.7
A43U10	160-7460-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U11	160-5819-07	PRGM EPROM,27C1024,VER2.7
A43U11	160-7461-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U12	160-5820-07	PRGM EPROM,27C1024,VER2.7
A43U12	160-7462-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U13	160-5821-07	PRGM EPROM,27C1024,VER2.7
A43U13	160-7463-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U14	160-5822-07	PRGM EPROM,27C1024,VER2.7
A43U14	160-7464-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)

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MANUAL CHANGE INFORMATION:

Date: 01–Oct–93 **Change Reference:** M75640

Product: 2780–Series Service **Manual Part No.:** 070–8244–02

DESCRIPTION **Product Group 2E**

EFFECTIVE FOR SERIAL NUMBERS:

2782	B020492 and up
2784	B010165 and up

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A31	672-0190-04	CKT BOARD ASSY:PHASE LOCK

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A31	672-0190-05	CKT BOARD ASSY:PHASE LOCK

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MANUAL CHANGE INFORMATION

Date 01-OCT-93 Change Reference: M80134

Product: 2780-Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrun Analyzer B020492 and above
2784 Spectrum Analyzer B010165 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A5	621-0038-08	POWER SUPPLY
A5A1	670-9451-03	CIRCUIT BOARD ASSY:POWER SUPPLY SECONDARY

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A5	621-0038-09	POWER SUPPLY
A5A1	670-9451-04	CIRCUIT BOARD ASSY:POWER SUPPLY SECONDARY

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MANUAL CHANGE INFORMATION

Date 13-Oct-93 Change Reference: M80269A

Product: 2780 Series Spectrum Analyzers Manual Part No.: 070-8244-02

DESCRIPTION Product Group 2E

EFFECTIVE FOR SERIAL NUMBERS:

2782 Spectrum Analyzer B030101 and above
2784 Spectrum Analyzer B020101 and above

Change Replaceable Electrical Parts to:

REMOVE:

CIRCUIT #	PART NUMBER	DESCRIPTION
A24U11	160-5825-05	PRGM EPROM,27C1024,VER2.7
A41U63	160-5824-07	PRGM EPROM,27C1024,VER2.7
A41U63	160-7465-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A42U40	160-5826-04	PRGM EPROM,27C1024,VER2.7
A42U40	160-8501-04	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U10	160-5823-07	PRGM EPROM,27C1024,VER2.7
A43U10	160-7460-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U11	160-5819-07	PRGM EPROM,27C1024,VER2.7
A43U11	160-7461-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U12	160-5820-07	PRGM EPROM,27C1024,VER2.7
A43U12	160-7462-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U13	160-5821-07	PRGM EPROM,27C1024,VER2.7
A43U13	160-7463-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)
A43U14	160-5822-07	PRGM EPROM,27C1024,VER2.7
A43U14	160-7464-05	PRGM EPROM,27C1024,VER2.7 (OPTION 16 ONLY)

ADD:

CIRCUIT #	PART NUMBER	DESCRIPTION
A24U11	160-5825-06	PRGM EPROM,27C1024,VER2.8
A41U63	160-5824-08	PRGM EPROM,27C1024,VER2.8
A41U63	160-7465-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A42U40	160-5826-05	PRGM EPROM,27C1024,VER2.8
A42U40	160-8501-05	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A43U10	160-5823-08	PRGM EPROM,27C1024,VER2.8
A43U10	160-7460-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A43U11	160-5819-08	PRGM EPROM,27C1024,VER2.8
A43U11	160-7461-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A43U12	160-5820-08	PRGM EPROM,27C1024,VER2.8
A43U12	160-7462-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A43U13	160-5821-08	PRGM EPROM,27C1024,VER2.8
A43U13	160-7463-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)
A43U14	160-5822-08	PRGM EPROM,27C1024,VER2.8
A43U14	160-7464-06	PRGM EPROM,27C1024,VER2.8 (OPTION 16 ONLY)

PREFACE

This manual contains installation and performance verification information for the TEKTRONIX 2780-Series Spectrum Analyzer. A thorough knowledge of frequency domain analysis is assumed.

Manuals that describe other aspects of the product are:

- Operators Manual
- Programmers Manual
- Installation/Performance Verification

DOCUMENTATION STANDARDS

Most terminology and graphics follow ANSI standards. Refer to the following standards:

- ANSI Y1.1 — Abbreviations
- ANSI Y32.2 — Graphic Symbols
- IEEE 91 — Logic Symbols

CONTENTS

SAFETY SUMMARY

(Refer all servicing to qualified servicing personnel)

The safety information in this summary is for both operating and service personnel. Specific warnings and captions will be found through the manual where they apply, but may not appear in this summary.

CONFORMANCE TO INDUSTRY STANDARDS

The 2780-Series Spectrum Analyzer complies with the following Industry Safety Standards and Regulatory Requirements.

SAFETY

CSA: *Standard C22.2 No. 231 — Electrical and Electronic Measurement and Testing Equipment*

FM: *Electrical Utilization Standard Class 3810*

ANSI/ISA/S82 — *Safety Requirements for Electrical and Electronic Measuring and Controlling Instrumentation.*

IEC 348 (2nd edition) — *Safety Requirements for Electronic Measuring Apparatus.*

UL 1244 (2nd edition) — *Electrical and Electronic Measuring and Testing Equipment.*

REGULATORY REQUIREMENTS

VDE 0871 Class B — *Regulations for RFI Suppression of High Frequency Apparatus and Installations.*

FCC Part 15 Subpart J Class A — EMI Compatibility

(Germany) — RöV X-ray Decree, Section 5, March 1973

MILITARY

Mil-Std 461B, Part 4

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the instrument or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property, including the instrument itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL

This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — Refer to manual.

Certificate of the Manufacturer/Importer

We hereby certify that the 2780-Series Spectrum Analyzer with options complies with the RF Interference Suppression requirements of Amtsbl.-Vfg 1046/1984.

The German Postal Service was notified that the equipment is being marketed.

The German Postal Service has the right to re-test the series and to verify that it complies.

TEKTRONIX

Bescheinigung des Herstellers/Importeurs

Hiermit wird bescheinigt, daß der/die/das 2780 Series Spectrum Analyzer with options in Übereinstimmung mit den Bestimmungen der Amtsblatt-Verfügung 1046/1984 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprufüng der Serie auf Einhalten der Bestimmungen eingeräumt.

TEKTRONIX

NOTICE to the user/operator:

The German Postal Service requires that this equipment, when used in a test setup, may only be operated if the requirements of Postal Regulation, Vfg. 1046/1984, Par. 2, Sect. 1.7.1 are complied with.

HINWEIS für den Benutzer/Betreiber:

Dies Gerät darf in Meßaufbauten nur betreiben werden, wenn die Voraussetzungen des Par.2, Ziff. 1.7.1 der Vfg. 1046/1984 eingehalten werden.

NOTICE to the user/operator:

The German Postal Service requires that Systems assembled by the operator/user of this instrument must also comply with Postal Regulation, Vfg. 1046/1984, Par. 2, Sect. 1.

HINWEIS für den Benutzer/Betreiber:

Die vom Betreiber zusammengestellte Anlage, innerhalb derer dies Gerät eingesetzt wird, muß ebenfalls den Voraussetzungen nach Par.2, Ziff. 1 der Vfg. 1046/1984 genugen.

POWER SOURCE

The instrument is intended to operate from a power source that will not apply more than 250 V RMS between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

GROUNDING THE PRODUCT

The instrument is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting it to the power terminal. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for the instrument.

Use only a power cord that is in good condition.

International power cords (Tektronix Options A1, A2, A3, and A5) are approved for the country of use, and are not included in the CSA certification.

For detailed information on power cords and connectors, see the Options appendix in the Operators Manual.

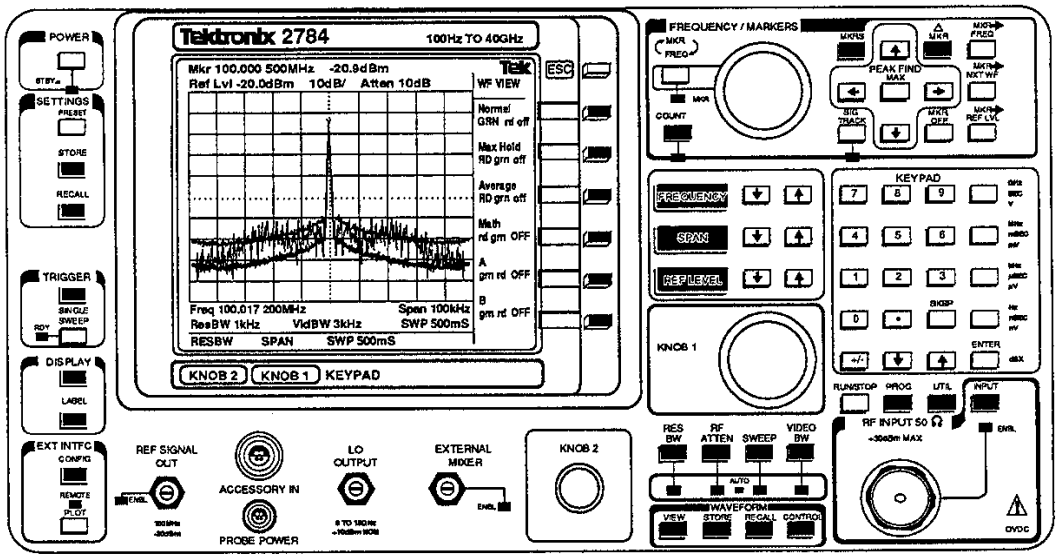
USE THE PROPER FUSE

To avoid fire hazard or equipment damage, use only the fuse of correct type, voltage rating, and current rating as marked on the instrument (as specified in the Replaceable Electrical Parts list of this manual).

OPERATIONAL PRECAUTIONS

Do Not Operate in Explosive Atmospheres — To avoid explosion, do not operate the instrument in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels — To avoid personal injury, do not remove the instrument covers or panels unless you are qualified to do so. *REFER ALL SERVICING TO QUALIFIED SERVICE PERSONNEL.*



Tektronix 2780-Series Portable Spectrum Analyzer

GENERAL INFORMATION

ABOUT THIS MANUAL

This manual includes module-level service information for the 2780-series Spectrum Analyzer. It is intended for use by qualified service technicians to aid in adjustment, troubleshooting, and repair. Technicians should have experience with spectrum analyzer service and should be familiar with RF and microwave circuits, analog and digital circuitry, microprocessors, and computer control.

This manual contains the following information:

Section One, General Information, describes this manual and other manuals for the 2780-series instruments, provides preliminary instructions for obtaining product service, and refers to module exchange information located elsewhere in this manual.

Section Two, Specification, consists of tables of instrument characteristics and performance statements.

Section Three, Adjustment, is a guide for performing regular instrument calibration.

Section Four, Maintenance, consists of information for preventive maintenance, troubleshooting, and corrective maintenance.

Section Five, Theory of Operation, consists of block descriptions to aid in servicing to the module level.

Section Six, Replaceable Electrical Parts, and Section Eight, Replaceable Mechanical Parts, are tables that list replaceable parts and assemblies. The Exploded View diagrams in Section Eight show part and assembly locations.

Section Seven, Diagrams, contains instrument interconnection information and an overall block diagram.

Appendix A, Service Related Error Messages, includes data useful in troubleshooting the instrument.

Appendix B, Service Kit Information, includes information on installing and using the Processor Extender board, which is part of the optional Service Kit. Appendix B also includes a list of the keyboard commands available in the Service mode when using a terminal with the RS-232 port on the Processor Extender board.

OTHER 2780-SERIES MANUALS

The Service Manual is one of several 2780-series manuals. The following manuals are standard accessories, and can also be ordered through the Tektronix product catalog:

Installation/Performance Verification Manual
Operators Manual
Operators Handbook
Programmers Manual
Programmers Reference Guide

The Installation/Performance Verification Manual includes installation information and a Performance Check procedure to check the instrument against its specifications. The Performance Check procedure uses PC-compatible computer-based programs to aid in checking instrument performance. The programs are included on the Performance Check disk and on the Flatness Check disks, included with the Installation/Performance Verification Manual.

The Operators Manual includes a complete product description, specifications, operating procedures, and a list of error and warning messages. The Operators Handbook is a condensed version of the Operators Manual.

The Programmers Manual includes complete programming information. The Programmers Reference Guide is a condensed version of the Programmers Manual.

PRODUCT SERVICE

To ensure adequate product service and maintenance for your instrument, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available.

For example, for a fixed fee, a maintenance agreement program provides maintenance and recalibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time. For more detailed information, refer to the Options Section of the 2780-series Operators Manual.

Tektronix emergency repair service provides immediate service when the instrument is urgently needed.

Contact your local Tektronix Service Center, representative, or sales engineer for details regarding product service.

MODULE EXCHANGE

Tektronix 2780-series instrument service is performed by identifying a faulty module and exchanging it with a properly functioning module. See Section 4, Maintenance, for module exchange information.

SPECIFICATION

DESCRIPTION

The following specification and features apply after a 30-minute warm up, except as noted.

The Performance Requirement column defines some characteristics in quantitative terms and in limit form. Statements in this column are considered to be guaranteed performance that can be verified. Procedures to verify performance requirements are provided in the Performance Check portion of the Installation/ Performance Verification manual.

The Supplemental Information column explains performance requirements or provides performance information. Statements in this column are not considered to be guaranteed performance, and are not ordinarily supported by a performance check procedure.

VERIFICATION OF TOLERANCE VALUES

When performing compliance tests of specified limits listed in the Performance Requirement column, use measurement instruments that do not affect the values measured. Measurements tolerance of test equipment should be negligible when compared to the specified tolerance. If the tolerance is not negligible, add the error of the measuring device to the specified tolerances.

Table 2-1

FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Center Frequency Range		2782 100 Hz to 33 GHz with internal mixer 8.0 GHz to 1200 GHz with external mixer 2784 100 Hz to 40 GHz with internal mixer 8.0 GHz to 1200 GHz with external mixer
Resolution		0.1% of Span
Accuracy Freq Span 10 Hz to ≤2 MHz	±[Freq*(RE + 10^{-10})]+(2% of Span or 20% of Res Bandwidth whichever is greater) +[N*(10 Hz)]	Where: Freq = Center or Marker Frequency RE = Reference Oscillator Error N = LO Harmonic
Freq Span >2 MHz	±[Freq*(RE + 10^{-10})]+(2% of Span or 20% of Res Bandwidth whichever is greater) +[N*(100 kHz)]	
Marker Frequency Counter Range		100 Hz to 1200 GHz
Resolution		Selectable from 1 GHz to 1 Hz
Accuracy All Frequency Spans except 1 MHz and 2 MHz	± [Freq*(RE + 10^{-10})] + [8 Hz*(N)] + 1 LSD	Where: Freq = Marker Frequency RE = Reference Oscillator Error LSD = Least Significant Digit N = LO Harmonic
1 MHz and 2 MHz Frequency Spans	± [Freq*(RE + 10^{-10})] + [15 Hz*(N)] + 1 LSD	
Sensitivity	20 dB above noise and no more than 80 dB below Ref Level	Smallest signal that can be counted

Table 2-1 (Continued)

FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Frequency Span Range		2782 10 Hz to 33 GHz, plus Max Span of 33 GHz. External Mixer Bands 10 Hz to 600 GHz. 2784 10 Hz to 40 GHz, plus Max Span of 40 GHz. External Mixer Bands 10 Hz to 600 GHz.
Resolution Frequency Spans ≥100 Hz Frequency Spans <100 Hz		 Selectable within ±1% Selectable within ±10%
Accuracy Frequency Spans >2 MHz >1 kHz and ≤2 MHz >100 Hz and ≤1 kHz ≥10 Hz and ≤100 Hz	 ±2% ±1% ±7%	 ±7.0%
* Resolution Bandwidth Range		2782 serial number <B030101 2784 serial number <B020101 6 dB bandwidths from 3 Hz to 10 MHz 2782 serial number ≥B030101 2784 serial number ≥B020101 Fast Sweep Mode off: 6 dB bandwidths from 3 Hz to 10 MHz Fast Sweep Mode on: 3 dB bandwidths 3 Hz to 1 kHz 6 dB bandwidths 3 kHz to 10 MHz All characteristics in Fast Sweep Mode are specified typical.
Resolution		1-3-10 sequence
Bandwidth Accuracy 10 MHz and 3 MHz 1 MHz to 100 Hz 30 Hz and 10 Hz 3 Hz	 ±20% ±15% ±20%	 +50% to –10%
Shape Factor	<10:1	60 dB/6 dB

* Fast Sweep Mode was added at B030101 for the 2782 and B020101 for the 2784.

Table 2-1 (Continued)

FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Stability		
Residual FM		
≤2 MHz Span	[1 Hz*(N)] p-p over 1s four out of five sweeps with instrument reference locked to source to remove drift from measurement.	Where N = LO Harmonic
>2 MHz Span	[25 kHz*(N)] p-p over 500 ms	
Center Frequency Drift (Maximum)		Where N = LO Harmonic
After 30 Minutes Warm Up		
≤2 MHz Span		<30 Hz*(N)/minute of sweep time
>2 MHz Span		<25 kHz*(N)/minute of sweep time
After 1 Hour Warm Up		
≤2 MHz Span	<5 Hz*(N)/minute of sweep time	
>2 MHz Span		<5 kHz*(N)/minute of sweep time
Frequency Reference Accuracy		
Aging Rate		<1*10^{-6} /year and <7*10^{-9} /day (The yearly rate applies after 14 days of continuous oven operation). The Reference Oscillator and oven receive standby power whenever the instrument is plugged in.
Warm Up		On standby: No warm-up time needed No power: After 24 hours off at room temperature, within 1*10^{-8} of frequency at turnoff within 30 minutes. Long Term aging rate reached in 3 hours.
Temperature Drift with respect to 25°C		<±5*10^{-7} over –10°C to +55°C
IF Frequency, LO Range, and Harmonic Number		

Band and Frequency Range	LO Harmonic (N)	IF (GHz)
2782 and 2784		
1 (100 Hz to 6.50 GHz)	1	–10.025
2 (6.30 GHz to 12.775 GHz)	1	–3.525
3 (12.40 GHz to 21.25 GHz)	1	+3.525
4 (21.05 GHz to 28.025 GHz)	1	+10.025
5 (26.30 GHz to 33.0 GHz)	3	–3.525
2784		
6 (32.0 GHz to 37.0 GHz)	3	–3.525
7 (36.0 GHz to 40.0 GHz)	3	–3.525

Table 2-1 (Continued)

FREQUENCY RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information	
		LO Harmonic (GHz)	IF
(Band and Frequency Range (continued) (N)			
2782 and 2784 External Mixer Bands:			
Odd LO Harmonic Bands Freq Range (GHz)			
8.0 to 12.5		1	–3.525
12.4 to 18.0		1	+3.525
18.0 to 21.525		1	+3.525[1]
21.225 to 26.5		3	–3.525[2]
26.5 to 40.0		3	–3.525
33.0 to 50.0		3	–3.525
40.0 to 60.0		5	–3.525
50.0 to 75.0		5	–3.525
60.0 to 90.0		5	+3.525
75.0 to 110.0		7	–3.525
90.0 to 140.0		9	–3.525
110.0 to 170.0		11	–3.525
140.0 to 220.0		13	–3.525
170.0 to 260.0		15	–3.525
220.0 to 325.0		19	–3.525
260.0 to 400.0		23	–3.525
325.0 to 500.0		29	–3.525
400.0 to 600.0		35	–3.525
500.0 to 750.0		43	–3.525
600.0 to 900.0		51	–3.525
750.0 to 1100.0		63	–3.525
600.0 to 1200.0		69	–3.525
Even LO Harmonic Bands Freq Range (GHz)			
18.0 to 26.5		2	–0.525
26.5 to 36.125		2	–3.525[3]
35.925 to 40.0		4	–3.525[4]
33.0 to 50.0		4	–3.525
40.0 to 60.0		4	–3.525
50.0 to 75.0		6	–3.525
60.0 to 90.0		6	–3.525
75.0 to 110.0		8	–3.525
90.0 to 140.0		8	–3.525
110.0 to 170.0		10	–3.525
140.0 to 220.0		14	–3.525
170.0 to 260.0		16	–3.525
220.0 to 325.0		20	–3.525
260.0 to 400.0		24	–3.525
325.0 to 500.0		28	–3.525
400.0 to 600.0		34	–3.525
500.0 to 750.0		42	–3.525
600.0 to 900.0		52	–3.525
750.0 to 1100.0		62	–3.525
600.0 to 1200.0		68	–3.525

[1]Lower part of 18.0 to 26.5 range (no IDENTIFY function available)
[2]Upper part of 18.0 to 26.5 range (no IDENTIFY function available)
[3]Lower part of 26.5 to 40 range
[4]Upper part of 26.5 to 40 range

Table 2-2

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
RF Input		2782 100 Hz to 33 GHz dc coupled, Planar crown system connector with K compatible and N type adapters standard accessories 2784 100 Hz to 40 GHz dc coupled, Planar crown system connector with K compatible and N type adapters standard accessories
Impedance		50 Ω
VSWR		With 10 to 70 dB RF Atten.
100 Hz to 6.5 GHz		<2.0:1
6.5 GHz to 28 GHz		<2.5:1
28 GHz to 33 GHz		<3.0:1
(2784 only) 33 GHz to 40 GHz		<3.5:1
Maximum Input Amplitude Without Damage AC		+30 dBm continuous, +47 dBm (50 W) peak with a pulse width of 1 µs or less with a maximum duty factor of <0.005, with a minimum of 50 dB RF attenuation +20 dBm continuous with 0 dB RF atten.
DC		<100 mA continuous
1 dB Gain Compression		
Amplitude		
9 kHz to 21 GHz	0 dBm	
21 GHz to 28 GHz	–3 dBm	
28 GHz to 33 GHz	–6 dBm	
33 GHz to 40 GHz	–6 dBm	
100 Hz to 9 kHz	0 dBm	Reference Level ≥0 dBm and Reference Level – RF Attenuation = 0 dBm
External Mixer Input		
Impedance		50 Ω with a vswr of <1.9:1 at 525 MHz and <2.2:1 at 3.525 GHz
Bias Voltage Range		–2 V to +2V
Amplitude		Approximately –40 dBm for full screen signal, with –20 dBm Reference Level and 20 dB mixer conversion loss
1 dB Compression Point		–15 dBm at 3.525 GHz
Equivalent Input Noise		–152 dBm typical at 10 Hz Resolution Bandwidth and 0 dB mixer conversion loss selected

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
External Mixer Input (continued)		
LO Output Power	+15 dBm minimum	8.105 to 17.9 GHz
Marker Amplitude Measurement		
Range		–140 dBm to +30 dBm
Resolution		0.1 dB at 10 dB/div to 0.01 dB at 1 dB/div
Amplitude Measurement		
Display Flatness and Frequency Response		Flatness is specified over the temperature range of 20°C to 30°C. This is an overall instrument specification, including the RF Attenuator.
0-50 dB RF Atten, 20°C to 30°C		With 60 dB RF Atten 20°C to 30°C
9 kHz to 6.50 GHz	±1.0 dB	±1.0 dB
6.30 GHz to 12.775 GHz	±4.0 dB	±4.0 dB
12.40 GHz to 21.25 GHz	±4.0 dB	±4.0 dB
21.05 GHz to 28.025 GHz	±4.0 dB	±4.0 dB
26.30 GHz to 33.0 GHz	±4.5 dB	±4.5 dB
32.0 GHz to 37.0 GHz	±5.0 dB	±5.0 dB
36.0 GHz to 40.0 GHz	±5.0 dB	±5.0 dB
100 Hz to 9 kHz	±1.0 dB	Reference Level ≥0 dBm and Reference Level – RF Attenuation = 0 dBm
Reference Level		
Range		–140 dBm to +30 dBm; range extends to +60 dBm in overdrive mode
Resolution		0.1 dB
Temperature Drift		±0.15 dB/°C A self-correction cycle can be initiated that will correct reference level errors. Temperature drift then occurs relative to the temperature at the time of the self correction.
Vertical Display Law		
Range		
Log		1 dB/div to 15 dB/div
Linear		5 nV to 22 V/div to two significant digits
Square Law		2 aW to 100 W/div to two significant digits, (1 aW = $1*10^{-18}$W)

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Vertical Display Law (continued)		
Temperature Drift		
10 dB/div		2%/10°C
1 dB/div		1.2%/10°C
Accuracy		The accuracy specifications apply for amplitude measurements done with the marker only, since marker measurements are corrected for logging errors.
Log	±0.2 dB/1 dB incremental	
	≤ ±1.5 dB cumulative over the 0 to 90 dB range at self-correction temperature	Typically: ≤ ±1.5 dB cumulative over the 0 to 90 dB range within ±5°C of self-correction temperature
	≤ +2/–3.5 dB cumulative over the 0 to 100 dB range at self-correction temperature	≤ +2 dB/–3.5 dB cumulative over the 0 to 100 dB range within ±5°C of self-correction temperature
	±1.67 dB cumulative over 60 dB in the 25 MHz path	
	±0.8 dB cumulative over 27 dB at 3 dB/div	
Linear	±5% of full scale	
Square Law	±8% of full scale	
RF Attenuator		
Range		0 dB to 70 dB
Resolution		10 dB
Accuracy at 100 MHz Center Frequency	±0.5 dB	
IF Gain		IF gain can be reduced to allow the RF input to be overdriven by 30 dB (that is, 0 dBm reference level with 0 dB RF attenuation). Note that only 10 dB of mixer overdrive is available with the 3 Hz resolution bandwidth.
Range		0 dB to 140 dB
Resolution		0.1 dB
Accuracy At self correction temp.		Typical Accuracy:
0 to 50 dB	≤ ±1.0 dB	≤ ±1.0 dB over the range of 0 to 50 dB and
0 to 100 dB	≤ ±1.5 dB	≤ ±1.5 dB over the range 0 to 100 dB within ±5°C of self-correction temperature
		Accuracy for input signals <9 kHz applies when Reference Level ≥0 dBm and Reference Level – RF Attenuation = 0 dBm

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Gain Variation Between Resolution Filters		Measured at –20 dBm reference level, 10 dB RF attenuation, Auto Video Bandwidth, Auto Sweep, Auto Resolution Bandwidth, and after two hour warm-up.
At Self-Correction Temperature		Typically within ±5°C of self-correction temperature. Resonator tracking self correction must be run before the following typical specification will be met.
		For input signals <9 kHz, specification applies when Reference Level ≥0 dBm and Reference Level – RF Attenuation = 0 dBm
10 MHz to 30 Hz	0.5 dB p-p	1.0 dB p-p
10 MHz to 10 Hz	0.75 dB p-p	1.5 dB p-p
10 MHz to 3 Hz	2 dB p-p	4.0 dB p-p
Error in Setting –20 dBm Reference Level		At –20 dBm reference level, 10 dB RF Attenuation, 3 MHz Resolution Filter, At self-correction temp.±0.25 dB 100 MHz Center Frequency, 2 MHz Span, 50 ms Sweep, 30 kHz Video Filter, sample acquisition mode using the Reference Signal Out as a source. This error is added to the Ref Signal Out Amplitude Accuracy Specification to arrive at the absolute amplitude accuracy at the above instrument settings. Typical: ±1.2 dB within ±5°C of self correction temperature.
Band Switching Uncertainty	±1.5 dB	Gain change when changing internal bands
Pulse Digitization Error		Typical: 4 dB Displayed pulse amplitude degradation versus actual pulse amplitude measured with a 200 ns wide pulse width 10 MHz resolution bandwidth, 10 MHz video bandwidth, and max or min/max acquisition mode
Dynamic Range Equivalent Input Noise		With 0 dB RF attenuation and 10 Hz resolution bandwidth
9 kHz to 50 kHz	–95 dBm	
50 kHz to 10 MHz	–105 dBm	
10 MHz to 2.5 GHz	–135 dBm	
2.5 GHz to 6.5 GHz	–132 dBm	
6.5 GHz to 21.25 GHz	–125 dBm	
21.25 GHz to 28 GHz	–120 dBm	
28 GHz to 33 GHz	–107 dBm	
33 GHz to 40 GHz	–107 dBm	
100 Hz to 9 kHz	–78 dBm	At –30 dBm Ref Level
10 MHz to 2.5 GHz		Typically –127 dBm at –30 dBm Ref Level

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Phase Noise Sideband (dBc/Hz)		Measured at frequency spans ≤2 MHz in dBc/Hz mode
	Offset: 100 Hz / 1 kHz / 10 kHz / 100 kHz / 1 MHz	
Center Frequency		
6.5 GHz	–85 / –97 / –105 / –105 / –112	
12 GHz	–80 / –95 / –105 / –105 / –112	
		Offset: 100 Hz / 1 kHz / 10 kHz / 100 kHz / 1 MHz
21 GHz		–75 / –90 / –105 / –105 / –112
33 GHz		–70 / –86 / –97 / –97 / –102
40 GHz (2784 only)		–65 / –81 / –94 / –94 / –99
Spurious Responses		Measured relative to (–30 dBm + RF Atten) signal amplitudes at the RF Input. All responses are less than (–80 +20 log N) dBc or (average noise level + 3 dB) whichever is greater. (N=harmonic number)
Residual Signals		Signals displayed by the instrument independent of input signals
100 Hz to 10 MHz (except at 2 MHz with 10 kHz and wider resolution bandwidth)	<–77 dBm	
	<–70 dBm	
10 MHz to 6.5 GHz	<–100 dBm	
6.5 GHz to 21.25 GHz	<–92 dBm	
21.25 GHz to 28.025 GHz	<–82 dBm	
28.025 GHz to 33 GHz	<–80 dBm	
33 GHz to 40 GHz (2784 only)	<–80 dBm	
Line Related Sidebands		
Center Frequency		
<28 GHz	<–75 dBc	
28 GHz to 33 GHz	<–65 dBc	
33 GHz to 40 GHz (2784 only)	<–65 dBc	

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Intermodulation Rejection Second Order Intercept Center Frequency 1 MHz to 6.5 GHz 6.5 GHz to 33 GHz 33 GHz to 40 GHz	≥+28 dBm	 ≥+70 dBm ≥+70 dBm (2784 only)
Third Order Intercept Signal Separation <150 MHz & >20 kHz Center Frequency 1 MHz to 6.5 GHz 6.5 GHz to 28 GHz	 ≥+15 dBm ≥+10 dBm	
Signal Separation <150 MHz & >20 kHz Center Frequency 28 GHz to 33 GHz 33 GHz to 40 GHz		 ≥+15 dBm ≥+15 dBm (2784 only)
Signal Separation >150 MHz Center Frequency 1 MHz to 6.5 GHz 6.5 GHz to 28 GHz 28 GHz to 33 GHz 33 GHz to 40 GHz		 ≥+15 dBm ≥+20 dBm ≥+20 dBm ≥+20 dBm (2784 only)
Second Harmonic Distortion Center Frequency 50 MHz to 6.5 GHz 6.5 GHz to 33 GHz 33 GHz to 40 GHz	 ≤–60 dBc 	Measured with –30 dBm input level ≤–100 dBc ≤–100 dBm (2784 only)
LO Emission Center Frequency 100 Hz to 6.5 GHz 6.5 GHz to 33 GHz 33 GHz to 40 GHz		At 0 dB RF attenuation ≤–75 dBm ≤–65 dBm ≤–65 dBm (2784 only)
IF/N Response Due to an input signal at 10.025 GHz/N, 3.525 GHz/N or 525 MHz/N		≤–90 dBc (except ≤–70 dBc with 5.0125 GHz input signal and center frequency in Band 1)

Table 2-2 (continued)

AMPLITUDE RELATED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Out of Band Responses Image Responses At input frequency of 100 Hz to 35 GHz and a center frequency of:		
100 Hz to 28 GHz	<–65 dBc	
28 GHz to 33 GHz	<–65 dBc	
33 GHz to 40 GHz	<–65 dBc	2784 only
At input frequency of 35 GHz to 40 GHz and a center frequency of:		2784 only
100 Hz to 28 GHz	<–60 dBc	
28 GHz to 33 GHz	<–50 dBc	
33 GHz to 40 GHz	<–65 dBc	
Harmonic Conversions		
100 Hz to 28 GHz		<–65 dBc
28 GHz to 33 GHz		<–55 dBc
33 GHz to 40 GHz		<–55 dBc (2784 only)

Table 2-3

DISPLAY CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Video Bandwidth Range		0.03 Hz to 300 kHz 3 dB bandwidth, in a 1-3-10 sequence and 7 MHz, each step nominally within ±25% Specific bandwidths in this sequence can be selected.
Digital Storage Maximum Sweep Rate With 10-bit Resolution		10 ms
With Reduced Horizontal Resolution		2 ms
Vertical Digitizer Uncertainty		±0.4%

Table 2-4

REAR PANEL INPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
FREQ REF (IN/OUT) Impedance		Nominally 50 Ω
Input Signal Frequency Allowed	10 MHz ±5 Hz	
Input Signal Amplitude Range	0 dBm to +15 dBm maximum	
Output Signal (when selected)		Nominally 0 dBm at 10 MHz (TTL-compatible)
Phase Noise Allowable		≤–100 dBc/Hz at 1 Hz offset, without degradation of instrument phase noise performance
TRIG/HORIZ IN Impedance/Coupling		Nominally 1 kΩ (trigger mode), or 8.25 kΩ (sweep mode) in parallel with 33 pF, dc coupled
Input Voltage Change Required for Triggering	0.5 V p-p	With selectable input frequency of 0 Hz to 5 MHz, or 0 Hz to 1.5 kHz (HF rejection)
Triggering Level		Adjustable between –5 V and +5 V with + or – slope selectable.
Input Voltage Required for Sweep		Selectable to between • 0 V left side of screen to +10 V right side of screen • –5 V left side of screen to +5 V right side of screen Do not exceed ±30 V (DC +peak AC) at the input. This selection is common with, but opposite of, the SWPOUT selection (that is, if SWPOUT is set for 0 to +10 V, TRIG/HORIZ IN is ±5 V).

Table 2-4 (continued)

REAR PANEL INPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Accessory Connector		A 15-pin connector for external inputs and outputs.
EXTBLANK (Pin 15) (Ext In Display Blanking)		External access to blanking of the CRT beam. TTL compatible — logic one blanks the screen.
EXTH+ (Pin 3) EXTH– (Pin 4) (Ext In Display Horiz) and EXTV+ (Pin 5), EXTV– (Pin 6) (Ext In Display Vert)		External access to the real time horizontal and vertical channels of the instrument.
Impedance/Coupling		>1.5 kΩ in parallel with 200 pF, DC coupled
Input Voltage Rating		Do not exceed ±5 V (DC + peak AC) at the inputs. Common mode offset not to exceed ±500 mV.
EXTH± Expanded Graticule		Differential voltage of –0.9 V, ±10% at left edge of graticule, to +0.9 V, ±10% at right edge of graticule.
Compressed Graticule		Differential voltage of –0.9 V, ±10% at left edge of graticule, to +0.55 V, ±10% at right edge of graticule.
EXTV±		Differential voltage of –0.6 V, ±10% at bottom edge of graticule, to +0.7 V, ±10% at top edge of graticule
Bandwidth (3 dB)		Approximately 5 MHz
SWPOUT (Pin 7) (Sweep Output)		The sweep voltage used to drive the frequency control and display systems.
Impedance		1 kΩ
Output Voltage		Selectable to between • 0 V left side of screen to +10 V right side of screen • –5 V left side of screen to +5 V right side of screen Do not exceed ±30 V (DC +peak AC) at the input. This selection is common with, but opposite of, the TRIG/HORIZ IN selection (that is, if SWPOUT is set for 0 to +10 V, TRIG/HORIZ IN is ±5 V).

Table 2-4 (continued)

REAR PANEL INPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Accessory Connector (continued)		
EXTVI+ (Pin 1), EXTVI– (Pin 2) (Ext In Video)		External access to the input of the video processing system. This system includes video filters, digital storage acquisition, and the storage bypass mode.
Impedance/Coupling		75 Ω
Input Voltage Range		Differential or single-ended voltage of –0.875 V bottom of screen to +0.875 V top of screen. When using single-ended, ground one input. Do not exceed ±5 V (DC + peak AC) at the inputs. Common offset not to exceed ±400 mV.
Bandwidth		Approximately 7.5 MHz
Penlift (Pin 8)		TTL level output to lift plotter pen.
External YIG Coil Tune Voltage (Pin 9) and Return (Pin 10)		An external output of the YTO coil tuning voltage and a return path.
Pins 11 and 12		Unused
Pins 13 and 14		Ground
Instrument Bus		Serial communications bus that the processors use to communicate with each other and the rest of the instrument modules Pin 1 Ground Pin 2 Status Line 0 (TTL output) Pin 3 Clock (TTL output) Pin 4 Data (TTL bi-directional) Pin 5 Service Request Line (TTL input) Pin 6 Status Line 1 (TTL output) Pin 7 Reset Line (TTL output) Pin 8 Data Direction Indicator (TTL input) Pin 9 Port Enable (TTL input)

Table 2-5

FRONT PANEL OUTPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
LO OUTPUT		Provides access to the output of the 1st local oscillator at >+4 dBm **This port must be terminated in 50 Ω at all times.**
PROBE POWER		Provides operating voltages for active probes Output voltages are • Pin 1 +5 V, ±5%, at 100 mA max • Pin 2 Ground • Pin 3 –15 V, ±5%, at 100 mA max • Pin 4 +15 V, ±5%, at 100 mA max
REF SIGNAL OUT Amplitude		–20 dBm
Amplitude Accuracy	±0.3 dB	
Frequency		100 MHz Phase locked to reference oscillator
ACCESSORY IN		General purpose serial data port for future accessory use

Table 2-6

REAR PANEL OUTPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
EXT V OUT (External Display Vertical Signal Output)		Jumper selectable between full deflection amplifier signal or the real time signal only. Factory set for real time only.
Amplitude		–1.25 V to +1.25 V for full screen deflection from bottom to top
Accuracy		±10%
Impedance		50 Ω

Table 2-6 (continued)

REAR PANEL OUTPUT CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
EXT H OUT (External Display Horizontal Signal Output)		Jumper selectable between full deflection amplifier signal or the real time signal only. Factory set for real time only.
Amplitude		–1.25 V to +1.25 V for full screen deflection from left to right
Accuracy		±10%
Impedance		50 Ω
EXT Z OUT (External Display Blanking Signal Output)		Use the Penlift output (Pin 8 of Accessory Connector) for Z-axis control if a real time display using VOUT and H OUT is desired.
Amplitude		0 V fully blanked to +1 V full intensity.
IF OUT Amplitude		+9 dBm, ±2 dB for full screen signal with –30 dBm reference level, 100 MHz center frequency, 1 kHz resolution bandwidth The output level may be different with different reference levels, center frequency or resolution bandwidth.
Impedance		50 Ω (VSWR ≤1.5:1)
Frequency 3 MHz or 10 MHz Res BW		25 MHz
≤1 MHz Res BW		4 MHz
External Interface Connectors		Two GPIB connectors are standard. Port 1 is a basic GPIB talker-listener port. Port 2 also has controller functions, allowing it to drive devices (such as a plotter) without an external controller.

Table 2-7

UNCATEGORIZED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
IEEE STD 488-1978 Port (GPIB) Interface Functions Port 1		SH1, AH1, T5, L3, SR1, RL0, PP0, DC1, DT1, C0
Port 2		SH1, AH1, T5, L3, SR0, RL0, PP0, DC0, DT0, C1, C2, C3, C27 (C0 is selectable)

Table 2-7 (continued)

UNCATEGORIZED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Sweep Generator Sweep Speed Range		200s to 2 µs in a 1-2-5 sequence
Accuracy ≥50 µs ≤20 µs	 ±5% ±10%	
Triggering		Adjustable trigger level and slope; HF Reject with 1.5 kHz cutoff frequency
Internal		AC coupled, frequency range from 10 Hz to 1 MHz; no more than two divisions of signal height required to trigger
External		DC coupled, frequency range from 0 Hz to 5 MHz and 0.5 V p-p required to trigger
Line		Copy of AC line
Non-Volatile Memory CMOS Battery Backup NVRAM		Stores waveforms, settings, macros, and key sequences
Battery Type		Lithium cells **WARNING** To avoid personal injury, observe proper handling and disposal procedures for lithium batteries. **Lithium Battery Handling** Improper handling of lithium batteries may cause fire, explosion, or severe burns. • Do not recharge batteries. • Do not crush or disassemble batteries. • Do not heat batteries above 302°F (150°C). • Do not incinerate batteries. • Do not expose battery contents to water. **Lithium Battery Disposal** Dispose of batteries in accordance with local, state, and national regulations. • Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill. • Larger quantities must be sent by surface transport to a hazardous waste disposal facility. Package the batteries individually, to prevent shorting, in a sturdy container that is clearly labeled as follows: *— Lithium Batteries —* *DO NOT OPEN*

Table 2-7 (continued)

UNCATEGORIZED CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Non-Volatile Memory (continued)		
Memory Retention		Guaranteed to –10°C ambient temperature
Battery Life		1.8 years at 20°C ambient temperature, with no connector to power source. 1 year at 50°C ambient temperature, with no connector to power source. Batteries are not used when the instrument is connected to a power source.
EEPROM		Stores instrument correction data.

Table 2-8

POWER REQUIREMENTS

Characteristic	Description
Input Voltage	90 to 132 VAC, 47 to 440 Hz 180 to 250 VAC, 47 to 63 Hz
Power	250 W maximum, 2.8 A at 115 VAC, 60 Hz
Leakage Current	3.5 mA maximum

Table 2-9

ENVIRONMENTAL CHARACTERISTICS

Meets the following MIL-T-28800C Type III, Class 3, Style C Specification

Characteristic	Description
Temperature	
Operating	–10°C to +55°C (tested to –15°C)
Non-Operating	–62°C to +85°C
Humidity	5 cycles per MIL STD 810D Procedure III (modified) To insure correct operation of the 3 kHz Resolution Bandwidth filter, the instrument should be powered-up for several hours after exposure to high humidity environments.

Table 2-9 (continued)

ENVIRONMENTAL CHARACTERISTICS

Meets the following MIL-T-28800C Type III, Class 3, Style C Specification

Characteristic	Description
Altitude Operating	15,000 feet (tested to 25,000 feet)
Non-Operating	40,000 feet (tested to 50,000 feet)
Vibration Operating	MIL STD 810D Procedure I (modified). Resonant searches in all three axes from 5 Hz to 15 Hz at 0.060-inch displacement for 7 minutes, 15 Hz to 25 Hz at 0.040-inch displacement for 3 minutes, and 25 Hz to 55 Hz at 0.020-inch displacement for 5 minutes (tested to 0.025 inch). Dwell for an additional 10 minutes in each axis at the frequency of the major resonance or at 55 Hz if none was found. Resonance is defined as twice the input displacement. Total vibration time is 75 minutes.
Shock Operating and Non-Operating	Three Guillotine-type shocks of 30 g, one-half sine, 11 ms duration each direction along each major axis. (Tested to 50 g.)
Transit Drop	8 inches, one per each of six faces and eight corners. Tested to 12 inches.
Electromagnetic Interference (EMI) MIL STD	Meets MIL STD 461C Part 4 as follows
Conducted Emissions	CE01 — 60 Hz to 15 kHz, 15 dB relaxation below 2 kHz CE03 — 15 kHz to 50 MHz power leads Narrowband - Full Limits (US Navy only) Broadband - Full Limits (US Navy only)
Conducted Susceptibility	CS01 — 30 Hz to 50 kHz power leads, full limits CS02 — 50 kHz to 400 MHz power leads, 10 dB relaxation at the IF frequencies CS06 — spike power leads, full limits
Radiated Emissions	RE01 — 30 Hz to 50 kHz magnetic field, 5 dB relaxation below 1 kHz and a 10 dB relaxation from 1 kHz to 50 kHz RE02 — 14 kHz to 1 GHz, meets MIL STD 461C Part 7 to full limits
Radiated Susceptibility	RS01 — 30 Hz to 50 kHz magnetic field, full limits RS02 — Magnetic Induction; 30 dB relaxation at 60 Hz, 20 dB relaxation at 440 Hz RS03 — Limited to 1V/meter from 14 kHz to 1 GHz with 20 dB relaxation at the IF frequencies

Table 2-9 (continued)

ENVIRONMENTAL CHARACTERISTICS

Meets the following MIL-T-28800C Type III, Class 3, Style C Specification

Characteristic	Description
VDE	Meets VDE 0871 Class B - Regulations for RFI Suppression of High Frequency Apparatus and Installations.
FCC	Meets FCC Part 15, Subpart J, Class A - EMI Compatibility.
German R8V	Meets German R8V, X-Ray Decree, Section 5, March 1973
Safety	Meets the following industry safety standards: CSA Standard C22.2 No. 231 - Electrical and Electronic Measurement and testing Equipment ANSI/ISA/S82 - Safety Requirements for Electrical and Electronic Measuring and Testing Instrumentation IEC 348, 2nd Edition - Safety Requirements for Electronic Measuring Apparatus FM - Electrical Utilization Standard Class 3810 UL 1244, 2nd Edition - Electrical and Electronic Measuring and Testing Equipment

Table 2-10

PHYSICAL CHARACTERISTICS

Characteristic	Description
Weight With cover and standard accessories, except manuals	44 pounds (22 kg)
Dimensions Without front cover, handle, or feet	8.05 X 12.90 X 18.59 inches (204.47 X 327.66 X 472.19 mm)
With front cover, handle folded back, and feet	8.40 X 15.75 X 21.64 inches (204.47 X 400.05 X 549.61 mm)
With front cover, handle fully extended	8.05 X 15.75 X 24.75 inches (204.47 X 394.97 X 624.28 mm)

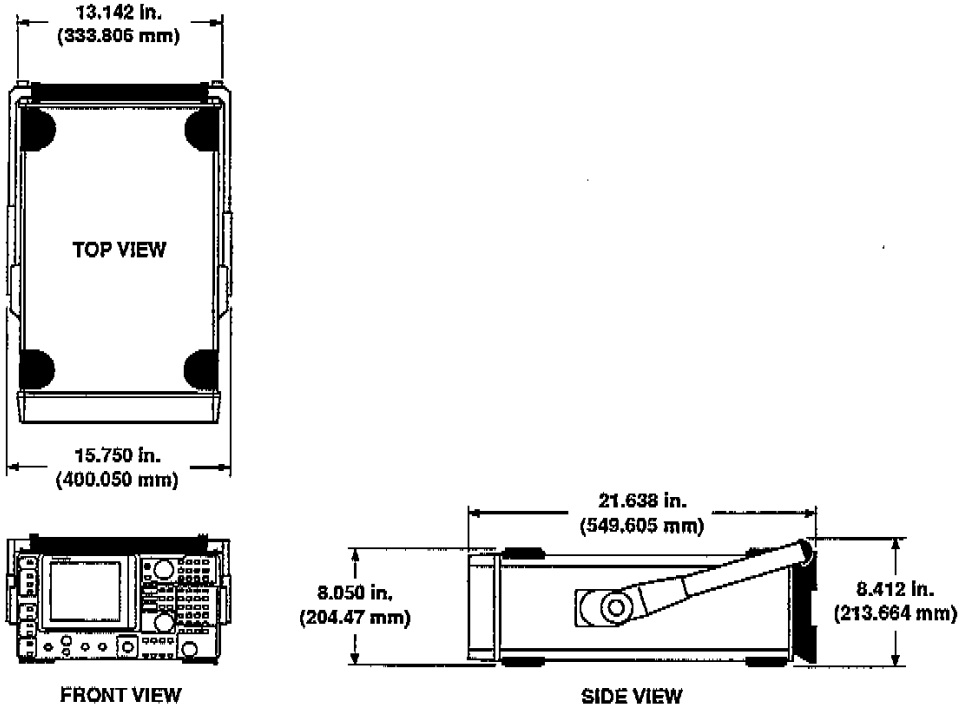


Figure 2-1. Dimensions.

ADJUSTMENTS/CORRECTIONS

This section provides adjustment/correction procedures for the instrument. It includes all the adjustments and self-corrections required to keep the instrument within specifications after repair or as part of routine maintenance.

Refer to Performance Tests, in the Installation/Performance Verification Manual, for instructions on checking the performance of the instrument after the adjustments have been made.

This section is divided into two parts. The first part details internal adjustments and the second part adjusts the flatness of the instrument. Software is included with this manual for flatness adjustment and other internal adjustments.

Before making any adjustment, allow the instrument to warm up for at least one hour in an ambient temperature of +20° C to +30° C. The waveform illustrations in this procedure are typical and may differ from one instrument to another. These waveforms do not necessarily represent specification tolerances.

Table 3-2 lists the adjustments and corrections necessary after repair or replacement of a specific module.

EQUIPMENT REQUIRED

Table 3-1 shows the equipment required for the flatness calibration and other adjustments.

Table 3-1. Equipment Required for Adjustments

Item	Characteristics	Recommended
Personal Computer	80286-based PC (IBM PC AT or equivalent), EGA or VGA graphics card and monitor, MS-DOS 3.1 or later.	
GPIB Interface Board	National PCIIA compatible.	National Instruments PCIIA
GPIB Interface Cable(s)	GPIB Interconnecting cable, 2 meters long NOTE: 4 or 5 cables are required to perform the Flatness checks (depending on generators used).	Tektronix Part No. 012-0630-01
RS-232-C Interface		Processor Extender board with RS-232 interface, supplied with Field Service Kit
RS-232-C Cable		Included with Field Service Kit
Communications Software	RS-232 communications and data transfer between computer and instrument.	Kermit - public domain communications program from Columbia University; or, any commercially available communications software with equivalent Kermit capabilities.
Test Software	278X Automated Tests Software 1-2-3 Spreadsheet V2.2 or greater but not V3. Measure for 1-2-3 278X Adjustment Software	Tektronix Part No. 063-1119-00 (Included with this manual) Lotus National Instruments Tektronix Part No. 063-0899-00 (Included with this manual)
Test Oscilloscope	100 MHz frequency range	Tektronix 2235A Oscilloscope
Test Spectrum Analyzer with Tracking Generator	Center Frequency range to 11 GHz	Hewlett-Packard HP3588A
Digital Voltmeter	Range 0 to ±200 volts; Accuracy 0.05%	Tektronix DM5110 or DM504A Digital Multi-meter
High-Voltage Probe	Range to 4500 volts	Tektronix Part No. 010-0277-00
Counter	9-digit accuracy; frequency range of 10 MHz to 100 MHz; and lockable to a 10 MHz reference signal	Hewlett-Packard HP5316B
Power Meter	Frequency range from 0 to 100 MHz (0 to 33 GHz for Flatness)	Hewlett-Packard HP438A or HP437B with HP8481D and HP11708A 50 MHz 30 dB Reference Attenuator. NOTE: For Flatness only, two additional power sensors are required: a Hewlett-Packard HP8487A and HP8482A

Table 3-1 (Continued). Equipment Required for Adjustments

Item	Characteristics	Recommended
Signal Generator	Frequency range of 10 kHz to 100 MHz, with less then –50 dBc of harmonic distortion, and lockable to 10 MHz external reference.	Hewlett-Packard HP8642A Synthesized Signal Generator, or equivalent.
Synthesizer (Low Frequency Flatness)	10 Hz to 20 MHz	Hewlett-Packard HP 3336C
Synthesizer/Sweep Generator (High Frequency Flatness and Fast Sweep Rate Tracking)	10 MHz to 40 GHz NOTE: 2 are required for 2nd and 3rd-order intercept measurements	Wiltron 6769B, or Hewlett-Packard HP 83640A
Frequency Standard	10 MHz, ± 0.01 Hz output	WWV receiver or other high-accuracy standard
Step Attenuators (2 Required)	1 dB/step within 0.1 dB at 100 MHz 10 dB/step within 0.5 dB at 100 MHz	Hewlett-Packard 355C Hewlett-Packard 355D
Fixed Attenuator	6 dB, 50 Ω, SMA connector (2 each) X10, 20 dB, 50 Ω	Tektronix Part No. 015-1001-00 Tektronix Part No. 011-0059-02
Coaxial Cable	BNC, 50 Ω, ±1% precision, 36 in. BNC, 50 Ω, 43 in. (2 each) SMA, 50 Ω, 28.5 in.(standard accessory)	Tektronix Part No. 012-0482-00 Tektronix Part No. 012-0057-01 Tektronix Part No. 012-0649-00
Coaxial Adapter	BNC male to BNC male BNC female to SMA male SMA male to SMA male	Tektronix Part No. 103-0029-00 Tektronix Part No. 015-1018-00 Tektronix Part No. 015-1011-00
High-Frequency Connectors, Pads, and Splitters	Power Divider/Combiner (dc to 40 GHz). 40 GHz flexible 50 Ω cable with K connectors. 3 dB attenuator (2 ea.) K male-to-male adapter N female-to-SMA male adapter SMA female-to-BNC male adapter BNC female-to-SMB female adapter 2.4 mm female-to-K male adapter K male-to-female adapter (2 ea. - optional) 50 Ω termination	Wiltron K240C WL Gore PD501501084.0 Wiltron 43KC-3 Wiltron K220 Tektronix 015-1009-00 Tektronix 015-0572-00 Hewlett-Packard 1250-1236 Hewlett-Packard 11904D Wiltron K224 Wiltron 28K50
Field Service Kit	Includes the following items: 9-pin RS-232-C cable 9-pin to 25-pin female RS-232-C adapter Power Supply cable BNC to 2 square pin cable VR Module Extender cable Plug to jack adapters (2 ea.) 50 Ω coax. cables (6 ea.) 0.2 - 250 MHz coupler, 20 dB Front Card Cage Extender Board Main Card Cage Extender Board Processor Extender Board	Tektronix Part No. 006-7334-00

REQUIREMENTS AFTER ASSEMBLY REPAIR OR REPLACEMENT

The following table lists replaceable assemblies and components, and the adjustments and/or corrections required when they are replaced.

Table 3-2. Adjustments/Corrections required after repair or replacement

Module	Name	Adjustments/Corrections Required
A1	Mother Board	None
A2A1	Front Panel #1	None
A2A2	Front Panel #2	None
A3	Flat Flex Interconnect	None
A5	LV Power Supply and Communications Interface	Power Supply Voltage Adjustment
A5B100	Fan	None
A5FL500	EMI Filter	None
A5W516	50 Ω Coaxial Cable	None
A5A1	Power Supply Primary	Power Supply Voltage Adjustment
A5A1F10	Thermal Fuse	Power Supply Voltage Adjustment
A5A2	Power Supply Secondary	None
A5A6	Communications Interface	None
A5A7	Rear Panel BNC	None
A10	RF Attenuator	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW Flatness
A11	YIG Tuned Oscillator (YTO)	Frequency Self Corrections Preselector Tracking Flatness
A11A2	YTO Driver	Frequency Self Corrections Preselector Tracking
A12	MTX	Preselector Tracking Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW External Mixer Corrections Flatness

Table 3-2 (Continued). Adjustments/Corrections required after repair or replacement

Module	Name	Adjustments/Corrections Required
A12A4	Low Pass Terminator	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW Flatness
A12A5	Low Pass Mixer	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW Flatness
A13	Microwave IF	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW External Mixer Corrections Flatness
A14	525 MHz IF	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW External Mixer Corrections Flatness
A15	Calibrator	100 MHz Calibrator Amplitude Adjustment
A15A3	RF Isolator	Spurious Response
A16	VR	Vertical Self Corrections: Display Law Gain Step VR Resonator ResBW Flatness
A17	Microwave Phase Lock	None
A18	Log Processor	Vertical Self Corrections: Display Law Log Corrections/Lin Adjustments Gain Step VR Resonator ResBW Flatness

Table 3-2 (Continued). Adjustments/Corrections required after repair or replacement

Module	Name	Adjustments/Corrections Required
A20	Video Processor	Real-Time Clamp Real-Time Horizontal Real-Time Vertical Vertical Self Corrections (all)
A22	Display Amplifiers	Intensity Real-Time Clamp Real-Time Horizontal Real-Time Vertical Vertical Display Gain and Offset Horizontal Display Gain and Offset
A23	High Voltage	CRT Cut-Off Intensity, Focus, and Astigmatism Geometry
A24	Digital Storage	Vertical Self Corrections (all)
A24U16	EPROM	None
A25	LO Module	Frequency Self Corrections Preselector Tracking Sweep Tracking Flatness
A28	Period Counter and 5X Multiplier	None
A29	Reference Oscillator	Reference Oscillator Adjustment Frequency Self Corrections
A31	565 MHz Synthesizer	Frequency Self Corrections
A33	Sweep/Span Attenuator	+10 Volt Reference Adjustment Frequency Self Corrections Preselector Tracking
A41	Main Processor	None
A41U63	EPROM	None
A42	I/O Interface	All adjustments/corrections in this procedure, including flatness.
A42BT10	Lithium Battery	None
A42BT11	Lithium Battery	None
A43	Memory	None *(if firmware version does not change)*
A43U10	EPROM	None *(if firmware version does not change)*
A43U11	EPROM	None *(if firmware version does not change)*
A43U12	EPROM	None *(if firmware version does not change)*
A43U13	EPROM	None *(if firmware version does not change)*
A43U14	EPROM	None *(if firmware version does not change)*
F10	Fuse	None

Table 3-2 (Continued). Adjustments/Corrections required after repair or replacement.

Module	Name	Adjustments/Corrections Required
FL100	Low Pass Filter	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW Flatness (Band 1 only)
P16	50 Ω Coaxial Terminator	
P18	50 Ω Coaxial Terminator	
V100	CRT	CRT Cut-Off Intensity, Focus, and Astigmatism Geometry Trace Rotation Vertical Display Gain and Offset Horizontal Display Gain and Offset
W100	Coaxial Cable (RF Atten-to-MTX)	Vertical Self Corrections: Attenuator Display Law Gain Step VR Resonator ResBW Flatness
W112	Coaxial Cable (YTO-to-1st LO OUTPUT)	None
W114	Coaxial Cable (YTO-to-Isolator)	None
W140	Coaxial Cable (525 MHz IF-to-VR)	None
W150	Coaxial Cable (Calibrator-to-Low Pass Termination)	None
W152	Coaxial Cable (Calibrator-to-REF SIG OUT)	None
W154	Coaxial Cable (Isolator-to-Microwave Phase Lock)	None
W166	Coaxial Cable (VR-to-IF OUT)	None
W250	Coaxial Cable (LO Module-to-Microwave Phase Lock)	None
W280	Coaxial Cable (X5 Mult-to-525 MHz IF)	None
W292	Coaxial Cable (Ref Osc-to-2nd LO Phase Lock)	None
W1280	Ribbon Cable (YTO Interface-to-YTO)	None
W1320	Coaxial Cable (Microwave IF-to-525 MHz IF)	None
W1334	Coaxial Cable (2nd LO-to-Calibrator)	None

PART I. ADJUSTMENTS/CORRECTIONS PROCEDURE

ENVIRONMENT REQUIREMENTS

The ambient temperature for the instrument should be within ±5° C of the temperature where self-correction of the instrument was performed. The ambient temperature during factory calibration is 25° C.

Before making any of these checks, allow the instrument to warm up for at least one hour.

Removing the Cabinet and Internal Covers

1. Disconnect the power cord.
2. Remove the cabinet. Put the front cover on the instrument and place the instrument on its face. Then, remove the four large screws that secure the rear feet, and remove the cabinet. Place the instrument in operating position again, and remove the front cover.
3. Remove the processor card-cage cover and the main card-cage cover.

CAUTION

To maintain adequate air flowing through the instrument, cover the card cage with a non-conductive material such as a large piece of paper when covers are removed.

4. Re-connect the power cord. The power supply fan will run for a few seconds, then stops. This is normal when power is first connected.
5. Press the POWER key. Wait approximately 5 seconds, while the internal processor initializes. During this period, the RF attenuators are set (a clicking sound). Let the instrument heat up for at least one hour before continuing this procedure.

A. POWER SUPPLY VOLTAGE ADJUSTMENT

1. Press PRESET to select the factory preset settings.
2. Press the SPAN key and enter 5 MHz with the keypad.
3. Press SINGLE SWEEP.
4. Using the digital voltmeter, measure the voltage between the +5VD test point on the mother board (see Figure 3-1) and chassis ground. The voltage should be +5 V, ±0.01 V. If the voltage is not within tolerance, adjust the +5D adjustment (see Figure 3-1). The fan speed may change when making this adjustment.

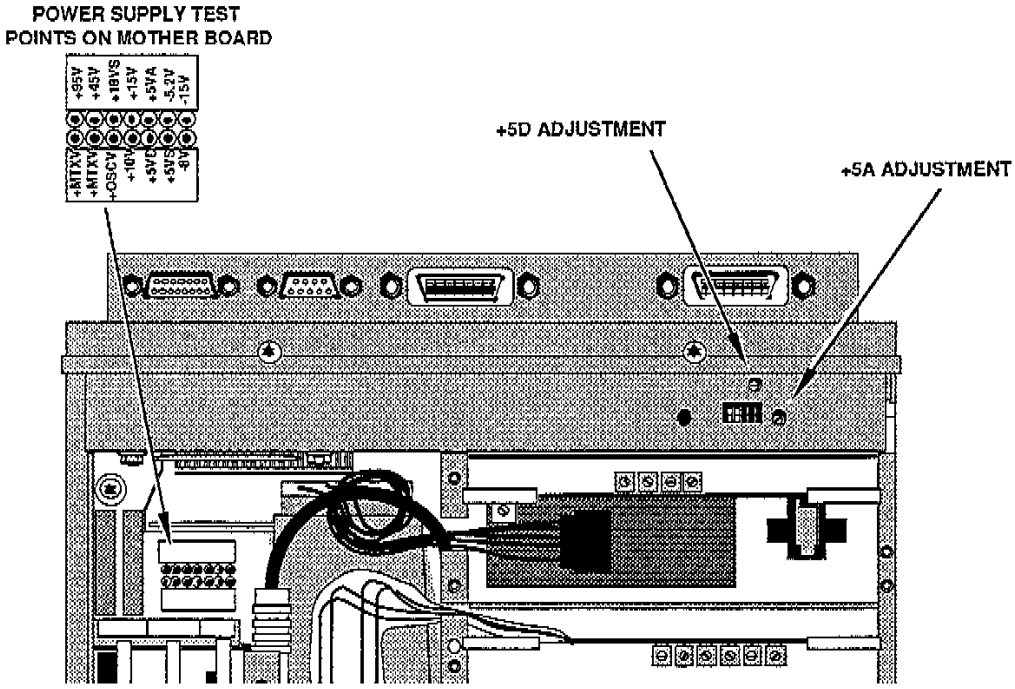


Figure 3-1. +5VD and +5VA Adjustment and Power Supply Test Points.

5. Measure the voltage between the +5VA test point on the mother board (see Figure 3-1) and chassis ground. This voltage should also be +5 V, ±0.01 V. If the voltage is not within tolerance, adjust the +5A adjustment (see Figure 3-1).

6. Repeat steps 3 and 4 until both the +5 VD and +5 VA voltages levels are within tolerance.

B. POWER SUPPLY VOLTAGE CHECK

1. Connect the digital voltmeter to the voltage listed in Table 3-3 (see Figure 3-1) and check that each is within its tolerance range.

Table 3-3. Power Supply Tolerances

Voltage	Tolerance Range
+5VD	4.80 V to 5.20 V
+5VA	4.95 V to 5.05 V
+5VS	4.92 V to 5.08 V
+10V	9.85 V to 10.15 V
+18VS	17.1 V to 20.7 V
+15V	14.70 V to 15.30 V
+45V	42.75 V to 47.75 V
+95V	90.25 V to 97.85 V
–5.2V	–5.14 V to –5.25 V
–15V	–14.70 V to –15.30 V
–8V	–7.88 V to –8.12 V

2. Press the TRIGGER key. Then, press the FREQUENCY key and enter 1 GHz from the instrument keypad. Press the SPAN key and enter 1 GHz from the keypad.

3. Connect the digital voltmeter to the MTXV test point on the Mother Board (see Figure 3-1) and check for approximately +0.5 volts as listed in Table 3-4.

Table 3-4. MTXV and OSCV Power Supply Tolerances

Test Point	Center Frequency	Test Point Voltage	Tolerance
MTXV	1 GHz	+0.5 V	Approximate
MTXV	7 GHz	+18 V	16.74 V to 19.26 V
MTXV	29 GHz	+26 V	24.18 V to 27.82 V
OSCV	29 GHz	+18 V	16.74 V to 19.26 V

4. Press the FREQUENCY key and enter 7 GHz via the keypad.

5. With the digital voltmeter still connected to the MTXV test point, check for the MTXV voltage of 16.74 V to 19.26 V

6. Press the FREQUENCY key and enter 29 GHz via the keypad.

7. Check for a voltage for the MTXV voltage of 24.18 V to 27.82 V.

8. Connect the digital voltmeter to the OSCV test point on the Mother Board (see Figure 3-1) and check for a voltage of 16.74 V to 19.26 V.

C. +10 VOLT REFERENCE ADJUSTMENT

1. Press the SINGLE SWEEP key.

2. Locate the two +10 V test points on the A33 Sweep/Span Attenuator board (see Figure 3-2). One test point provides access to the +10 V reference voltage, and the other test point provides access to a ground for the +10 V supply. This ground test point must be used when adjusting the +10 V reference.

3. Touch the ground lead of the digital voltmeter to the +10 V ground test point. Touch the other lead of the meter to the +10 V reference test point.

4. With the digital voltmeter set for the 20 V scale, adjust the +10 Volt Reference adjustment (see Figure 3-2) for a reading of 10.00 volts, ±0.01 volt.

5. Remove the digital voltmeter leads from the +10 V test points.

6. Press the TRIGGER key to set the instrument back to the continuous-sweep mode.

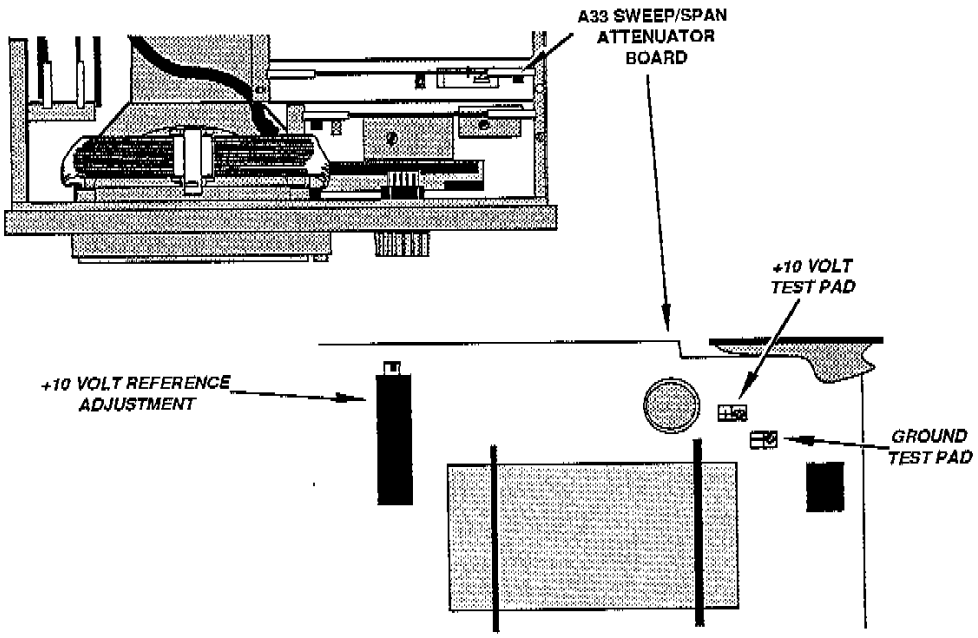


Figure 3-2. +10 Volt Reference Test Points and Adjustment.

D. HIGH VOLTAGE ADJUSTMENTS

During the adjustment steps of this procedure it will be necessary to discharge the CRT anode lead. Use the following procedure to discharge the CRT anode lead.

WARNING

The CRT anode lead retains a high voltage charge after the instrument is turned off. To avoid electrical shock or damage to other circuit components, discharge the anode lead as follows.

1. Disconnect the ceramic connector above the CRT; refer to Figure 3-3 (A).
2. Disconnect the connector by pulling on the CRT anode lead.
3. Insert the metal end of the male connector into one of the empty holes at the top of the card cage, refer to Figure 3-3 (B). Be certain the metal connector is touching the chassis.
4. Insert the blade of an insulated screwdriver into the female connector and short the blade to the chassis, refer to Figure 3-3 (B).

NOTE

Allow at least five minutes to discharge the male connector.

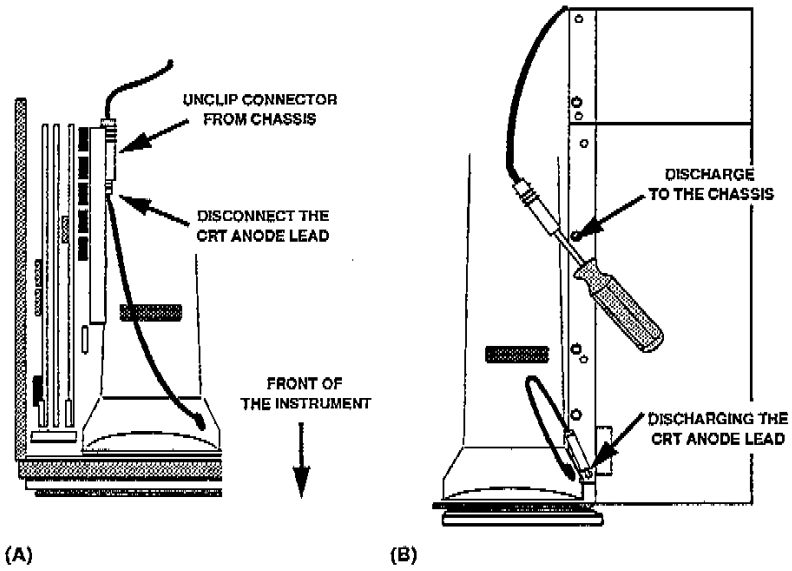


Figure 3-3. Discharging the CRT anode lead to the chassis.

HIGH VOLTAGE CATHODE POTENTIAL ADJUSTMENT

1. Turn the instrument POWER off.
2. Discharge the CRT anode to eliminate shock hazard as outlined at the start of this step.
3. Remove the card cage cover over the HV Power Supply assembly.
4. Remove the A23 HV Power Supply assembly, place on the Main Card Cage Extender board, and reinstall.
5. Remove the plug from J11 and place a jumper between pins 1 and 2 of J11 (use a jumper from one of the unused extender boards in the Field Service Kit). See Figure 3-4.
6. Apply POWER.
7. Connect Digital Multimeter with High Voltage probe to the Cathode adjustment test point and adjust the Cathode Adjust potentiometer for –4450 V ±45.5 V.

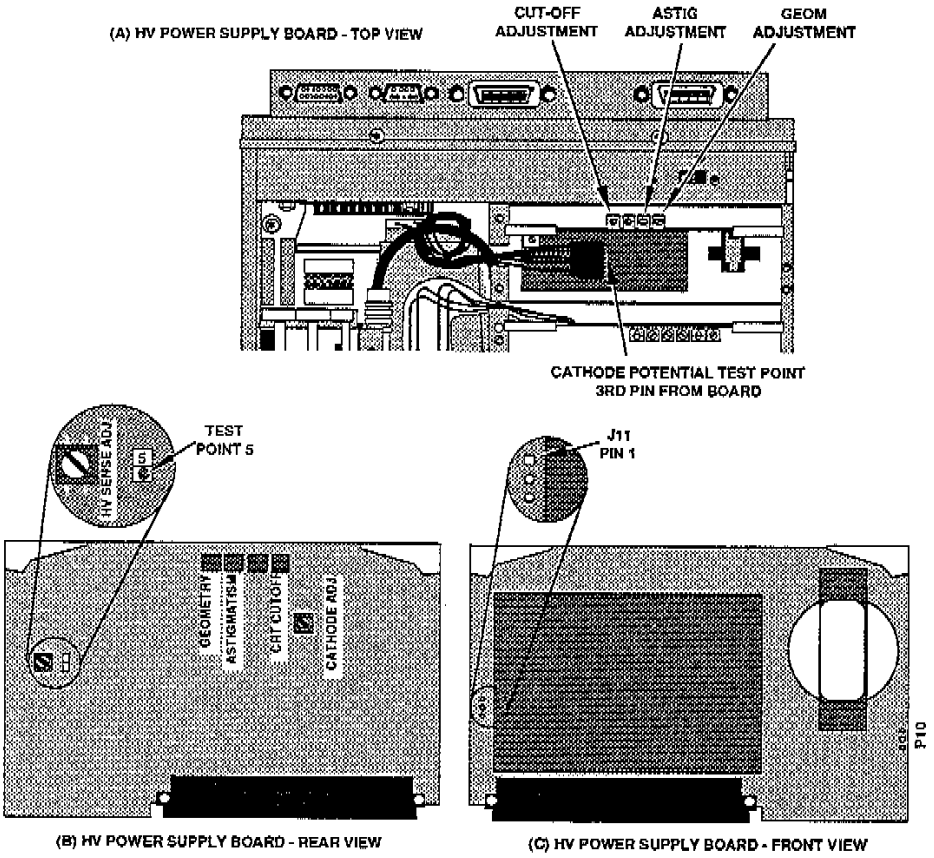


Figure 3-4. HV Power Supply adjustments.

HIGH VOLTAGE SENSE ADJUSTMENT

1. Measure TP5 with Digital Multimeter, and adjust HV Sense potentiometer for 50 mV, ±100 mV.
2. Turn the instrument POWER off.
3. Discharge the CRT anode to eliminate shock hazard as outlined at the start of this step.
4. Remove the HV Power Supply assembly and Main Card Cage Extender board.
5. Remove the jumper from J11 and re-connect the plug.
6. Reinstall the HV Power Supply assembly, anode connector, and the card cage shield.

CRT CUT-OFF ADJUSTMENT

1. A graticule should be displayed on the CRT screen. If there is no graticule display, press the PRESET key to reset the instrument to the factory preset settings.

CAUTION

In the next step of this procedure, do not remove the high voltage shield to make the CRT CUT-OFF adjustment. An access hole for the adjustment is provided in the shield.

2. Rotate CUT-OFF clockwise until the trace beam (dot) is visible at the upper left of the graticule. Adjust CUT-OFF counterclockwise to the point where the dot is no longer visible. Continue rotating the adjustment to a point ≈45° to 90° beyond where blanking first occurs.

E. INTENSITY, FOCUS, AND ASTIGMATISM ADJUSTMENTS

1. Press the DISPLAY key to bring up the Display Menu, and select the CRT Adjust Menu.
2. From the CRT Adjust Menu, select Set Brightness.
3. Adjust Knob 2 on the instrument front panel to increase the brightness of the display until there is no further change in display brightness (that is, until maximum display brightness is obtained). On the keypad, press ENTER to save this maximum brightness setting.
4. From the CRT Adjust Menu, select Set Focus.
5. Turn Knob 2 clockwise until there is no further change in display focus.
6. Adjust the INTEN adjustment on the Display Amplifier board (see Figure 3-5) until there is no degradation of character continuity (that is, until there are no tails or broken segments). This setting constitutes the maximum intensity level that can be set from the front panel.

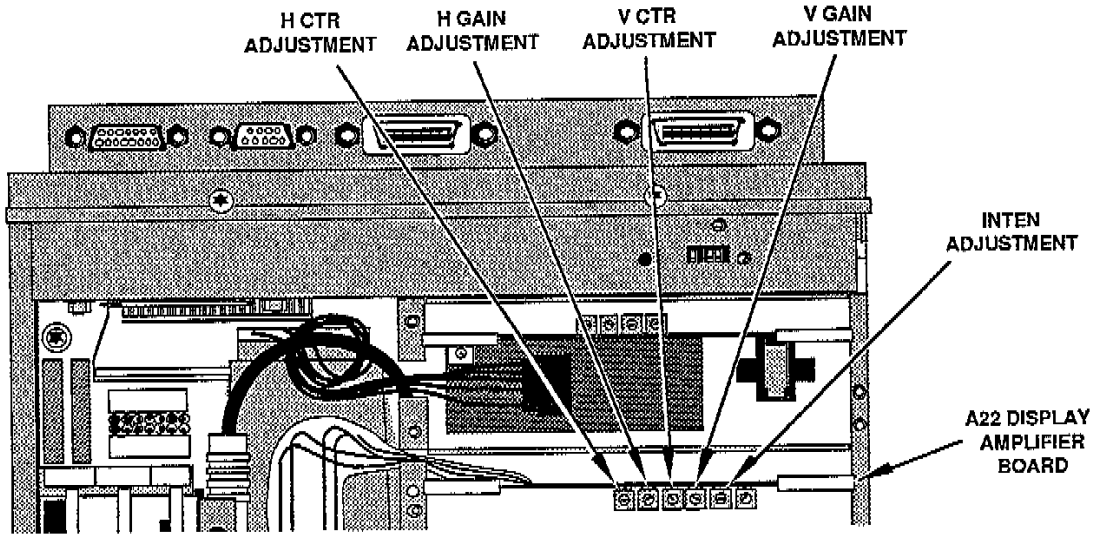


Figure 3-5. Display Amplifier Board adjustments.

CAUTION

In the next step of this procedure, do not remove the high voltage shield to make the Astigmatism adjustment. An access hole for the adjustment is provided in the shield.

7. Alternately adjust Knob 2 (set for Focus) and the Astigmatism adjustment on the A23 High Voltage assembly for optimum spot roundness on the CRT display. Press ENTER to save this setting.
8. From the CRT Adjust Menu, select Set Brightness.
9. Adjust Knob 2 for the desired brightness. Press ENTER to save the brightness setting.
10. From the CRT Adjust Menu, select Set Focus.
11. Adjust Knob 2 for optimum focus. Press ENTER to save the focus setting.
12. Press the front-panel ESC key twice to exit the Display menu.

F. GEOMETRY ADJUSTMENT

CAUTION

In the following procedure, do not remove the high voltage shield to make the GEOMETRY adjustment. An access hole for the adjustment is provided in the shield.

1. Adjust the GEOMETRY on the high voltage module (see Figure 3-4) for least bowing of the horizontal and vertical graticule lines. Bowing is most prominent at the edges of the display. When properly adjusted, no curvature of the graticule lines should be apparent.

G. TRACE ROTATION ADJUSTMENT

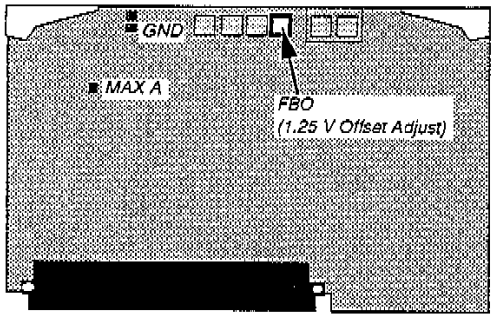
1. Press the DISPLAY key to bring up the Display Menu, and select the CRT Adjust Menu.
2. From the CRT Adjust Menu, select Set Trace Rot.
3. Adjust Knob 2 to align the graticule display evenly with the edges of the CRT bezel.
4. Press the ENTER key to save the trace-rotation-calibration settings. Then, press the ESC key twice to exit the Display Menu.

NOTE

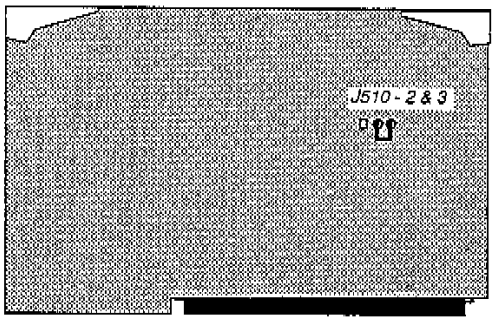
If it was necessary to adjust the Trace Rotation more than a few degrees, re-check the geometry adjustment as outlined in the previous procedure.

H. VIDEO PROCESSOR 1.25 VOLT OFFSET ADJUSTMENT

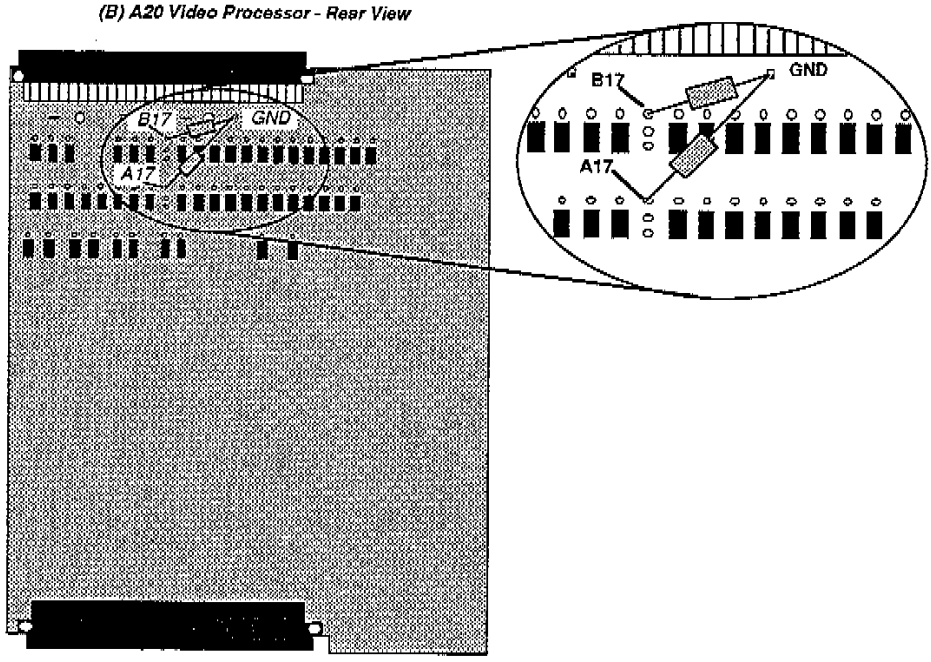
1. Turn the instrument POWER off, remove the A20 Video Processor, and place on the Main Card Cage Extender board. See Figure 3-6.
2. Move Video Processor jumper J510 to pins 2 and 3. See Figure 3-6B.
3. Remove jumpers on B17 and A17 of the Main Card Cage Extender board and connect two 75 Ω resistors on the Main Card Cage Extender board as shown in Figure 3-6C.
4. Re-apply instrument POWER and connect the Digital Multimeter positive lead to the MAX A test point and negative lead to the GND (ground) test point as shown in Figure 3-6A.
5. After the board has reached operating temperature (approximately 30 minutes), adjust the FBO potentiometer (1.25 V Offset adjustment, see Figure 3-6A) for 1.25 V, ± 2 mV.
6. Turn the POWER off, return the jumper on J510 to pins 1 and 2, reinstall the Video Processor, and remove the two 75 Ω resistors from the main card cage extender board.



(A) A20 Video Processor - Front View



(B) A20 Video Processor - Rear View



(C) Main Card Cage Extender - Video Processor test connections.

Figure 3-6. Video Processor 1.25 V Offset test setup.

I. VERTICAL DISPLAY GAIN AND OFFSET ADJUSTMENT

1. Press the WAVEFORM VIEW key to obtain a display that includes the graticule and the VIEW menu.
2. Adjust the VGAIN adjustment (vertical display width) and the V CRT adjustment (vertical display position) on the display amplifier board (see Figure 3-5) as follows:
   - So that the top and bottom of the CRT display extends just to the top and bottom of the CRT screen, without being cut off by the edge of the CRT.
   - So that the menu selections on the right side of the CRT match up with the menu keys on the CRT bezel, when viewed at a normal viewing angle (approx. 30-degree).

J. HORIZONTAL DISPLAY GAIN AND OFFSET ADJUSTMENT

1. Adjust the HGAIN adjustment (horizontal display width) and HCTR adjustment (horizontal display position) on the display amplifier board (see Figure 3-5) so that the left and right sides of the CRT display extend to within 0.125 inch (3.0 millimeters) of the left and right sides of the CRT screen, respectively.
2. Press the ESC key twice to obtain a full-screen graticule, without menu information. Check that the right side of the graticule does not extend beyond the right side of the CRT screen. If the graticule runs off the right side of the CRT screen, readjust the HGAIN and HCTR adjustments slightly to center the graticule horizontally on the CRT screen.

K. REAL TIME ADJUSTMENTS

BRIGHTNESS AND FOCUS

1. Press the PRESET key
2. Connect the REF SIGNAL OUT to the RF INPUT with a 50 Ω cable.
3. Press the FREQUENCY key, and enter a center frequency of 100 MHz from the keypad.
4. Press the SPAN key, and enter a span of 1 GHz from the keypad.
5. Press the WAVEFORM CONTROL key, select Real Time Menu. From the Real Time menu, select Real Time ON.
6. Select Set RT Brightness.
7. Adjust Knob 2 for a comfortable brightness level, then press the ENTER key to save the setting in NVRAM. When properly adjusted, the real time trace will be no brighter than the digital trace
8. Select Set RT Focus.
9. Adjust Knob 2 for a well-defined display, then press the ENTER key to save the setting in NVRAM.

CLAMP

1. Press the REF LEVEL key, and select the Vert Scale Menu. Then, select Knob 1 and set vertical scale to 1dB/ with KNOB 1.
2. Adjust the CLAMP adjustment on the A20 Video Processor board (see Figure 3-7) until the real time baseline is aligned with the digitized baseline.

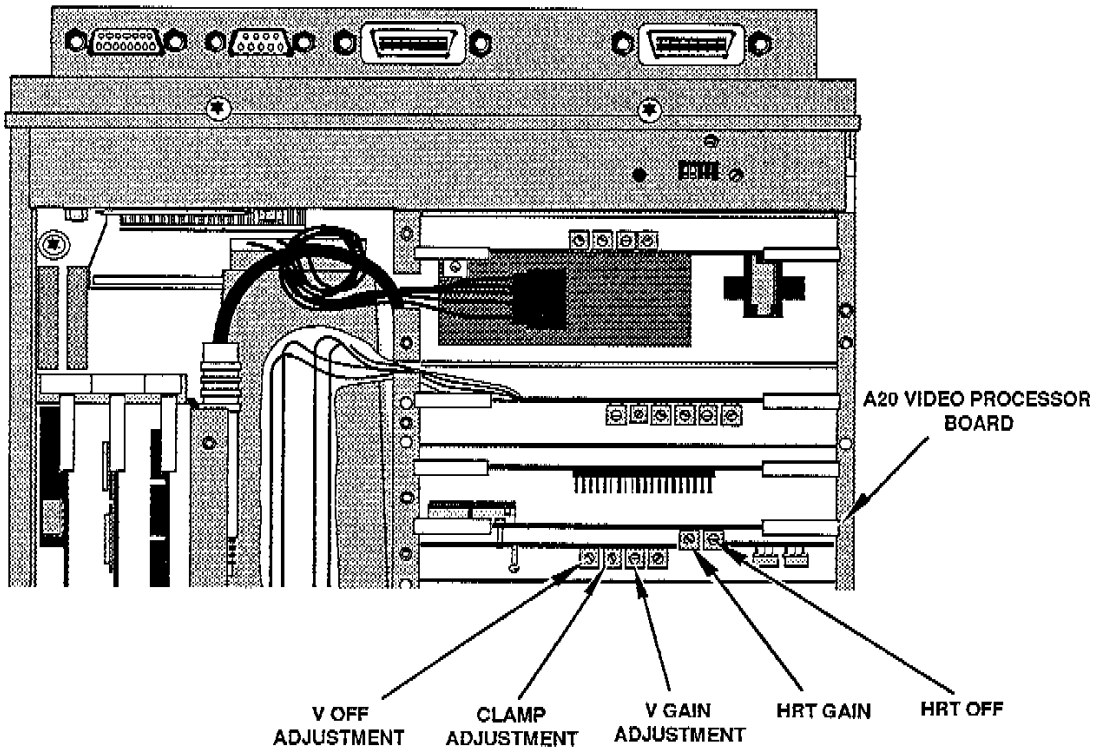


Figure 3-7. Video Processor Board.

HORIZONTAL

1. Press the SPAN key, and enter a span of 1 kHz from the keypad.
2. Press the RES BW key and enter a resolution bandwidth of 1 kHz.
3. Press the ESC key to exit the menu and display the full graticule.
4. Alternately adjust the HRT GAIN and HRT OFFSET adjustments on the Video Processor board (see Figure 3-7) until the real time display is positioned horizontally, directly over the digitized display.

VERTICAL

1. Press the SPAN key, and enter a span of 0 Hz from the keypad.
2. Press the ESC key to exit the menu and display the full graticule.
3. Using the REF LEVEL up and down arrows, and the FREQUENCY/MARKERS knob, position the signal near the top of the screen.
4. Alternately adjust the V GAIN and V OFF adjustments on the A20 Video Processor board (see Figure 3-7) until the real time display is positioned vertically, directly over the digitized display.
5. Using the REF LEVEL down arrow, and the FREQUENCY/MARKERS knob, position the signal to one division from the bottom graticule line, and repeat step 6.

6. Repeat steps 5 through 7 until the real time display vertically overlaps the digitized display when the signal is at the top of the screen and one division from the bottom of the screen.

7. Press the WAVEFORM CONTROL key, select REAL TIME menu, then Real Time OFF.

L. REFERENCE OSCILLATOR ADJUSTMENT

NOTE

The instrument must have had power applied to it, either in the standby mode (STBY light on) or the operating mode, for at least one hour before making the following adjustment.

An alternate procedure, using a frequency counter, is described in the note at the end of the procedure.

1. Connect the output of the rear-panel FREQ REF connector through a 50 Ω cable to a vertical channel input of the Test Oscilloscope, as shown in Figure 3-8.

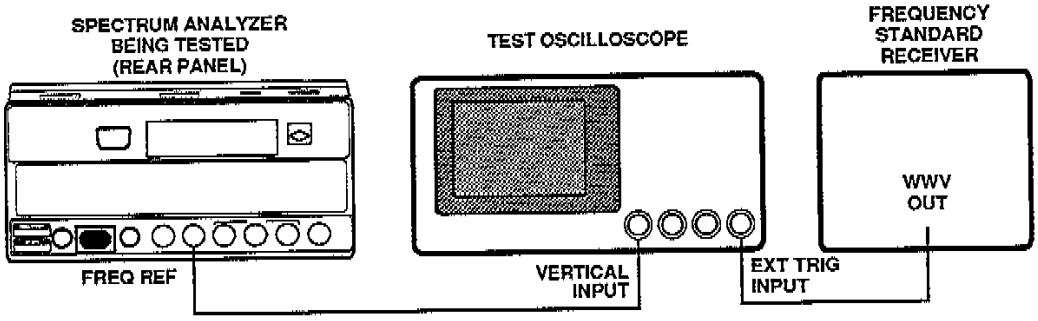


Figure 3-8. Test Equipment Connections for Reference Oscillator Check and Adjustment.

2. Tune the Frequency Standard Receiver to a frequency standard transmission (WWV), and connect the output to the external trigger input of the Test Oscilloscope.

3. Set the oscilloscope triggering for external triggering; the sweep speed for 0.05 microseconds/division; and the vertical gain for 1 volt/division.

4. Press the SETTINGS PRESET key, then press the FREQUENCY key to select the FREQUENCY menu.

5. Press the Configure Freq Menu key to select the CONFIGURE menu, then press the FreqRefOut key to select ON.

6. Observe the waveform on the test oscilloscope and adjust the trigger controls, if needed, for a stable display. The waveform may be stationary or drift slowly across the screen.

7. Adjust the Fine Reference Oscillator adjustment, R10, to stabilize the waveform on the test oscilloscope (see Figure 3-9).

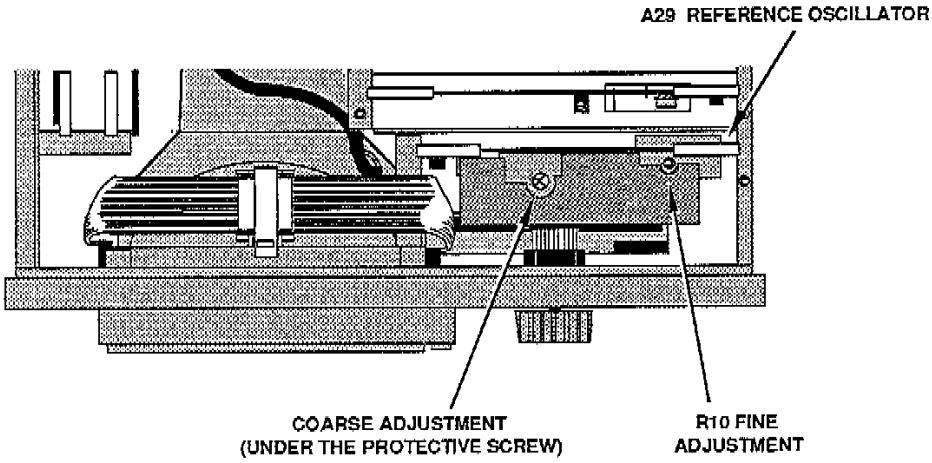


Figure 3-9. Reference Oscillator Adjustment.

NOTE

During this adjustment, the precision reference (WWV) triggers the oscilloscope sweep. When the oscillator frequency you are adjusting matches the reference, the displayed signal will no longer move across the display.

If the range of R10 is insufficient, mid-range R10 and adjust the coarse adjustment. See Figure 3-9.

8. Disconnect the cables from the instrument, the Test Oscilloscope, and the Frequency Standards receiver.

NOTE

Alternate Method Using A Frequency Counter

Substitute a frequency counter for the oscilloscope in the previous procedure. Connect the rear-panel FREQ REF to the counter's input and the Frequency Standard signal to the counter's external reference input. With the spectrum analyzer settings as described, adjust the Fine Reference Oscillator adjustment for a counted frequency of 10.000 000 MHz.

M. 5X MULTIPLIER OUTPUT ADJUSTMENTS

Set up the test Spectrum Analyzer as follows:

FREQ	500 MHz
SPAN	As necessary to view 500 MHz output
REF LEVEL	As necessary to view approximately 5 dBm

1. Turn the instrument POWER off.
2. Remove the main card cage covers and remove the A28 Period Counter and X5 Multiplier assembly. (Refer to the removal and replacement procedures in the Maintenance section.)
3. Remove the three shields by removing the six Torx T-6 screws as shown in Figure 3-10.

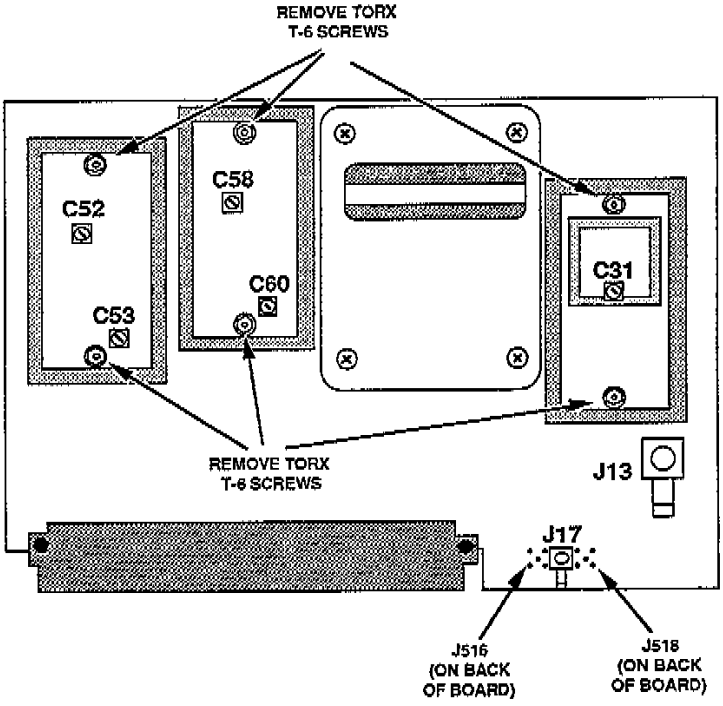


Figure 3-10. X5 Multiplier adjustment and test connector locations.

4. Connect the Period Counter and X5 Multiplier assembly to the Main Card Cage Extender, then connect J518 as indicated in Figure 3-11. The connection to J518 is on the rear of the extender and is made using one of the RF Cable Assemblies from the service kit.

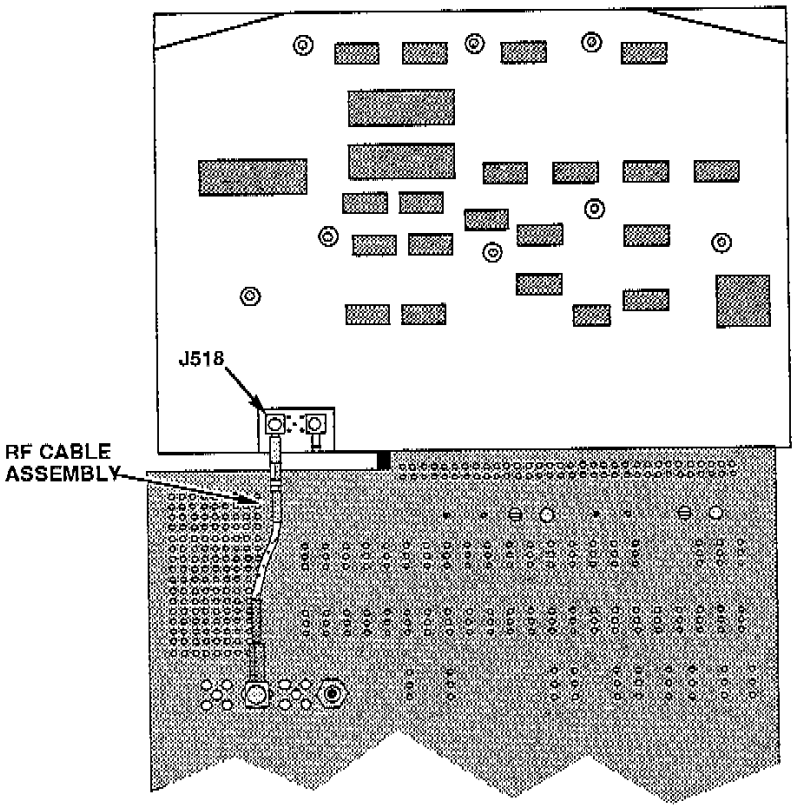


Figure 3-10. Connection on rear of Period Counter and X5 Multiplier assembly.

5. Install the Main Card Cage Extender, with the Period Counter and X5 Multiplier assembly attached, into the card cage.
6. Re-apply POWER.
7. Monitor J13 with the Test Spectrum Analyzer and adjust C31 for maximum amplitude of the 500 MHz signal. (Signal amplitude is approximately 6-10 dBm.)
8. Monitor J17 and adjust C58 and C60 for maximum amplitude. (Signal amplitude is approximately 4 dBm.)
9. Monitor J516 and adjust C52 and C53 for maximum amplitude. (Signal amplitude is approximately 4 dBm.)
10. Turn the POWER off, remove the test equipment, reinstall the shields removed in step 3, reinstall the assembly in the card cage, and replace the card cage covers.

N. VARIABLE RESOLUTION ASSEMBLY ADJUSTMENTS

The A16 Variable Resolution (VR) assembly adjustments should be performed as part of the overall instrument calibration. The adjustments are required to compensate for component aging, therefore they are not required when a replacement VR assembly is installed.

This procedure uses a software program to control the instrument through the GPIB port (PORT 1) on the instrument rear panel. The following equipment and software is required to provide GPIB control.

- IBM compatible personal computer (PC) with floppy disk drive and hard disk drive (C: drive)
- 278X Adjustment Software (included with this Service Manual)
- Lotus 1-2-3 spreadsheet software (version 2.2 or greater but not Version 3.X)
- National Instruments Measure for 1-2-3 software
- National Instruments GPIB interface card GPIB-PCII or GPIB-PCIIA

NOTE

During the following procedure, spreadsheet commands are executed by typing the first letter of the command. The notation to type "n" (next command) is n(ext).

INSTALLING THE PERSONAL COMPUTER HARDWARE

Use the following procedure to install the GPIB cards.

1. Set the base address for the PCIIA GPIB board and install it in the personal computer. Instructions for setting the base address, and for installing the board into the PC are contained in the instruction manual that comes with the board.

   The GPIB board must be given a base address that is used by the software to identify the board. The PCIIA board should come with its base address set to 02E1 (hex). Leave the board set at that address. Refer to the Switch Setting illustration for setting the switches

2. If conflicts occur with DMA or interrupts, refer to the manual provided with the National Instruments GPIB-PCIIA board.

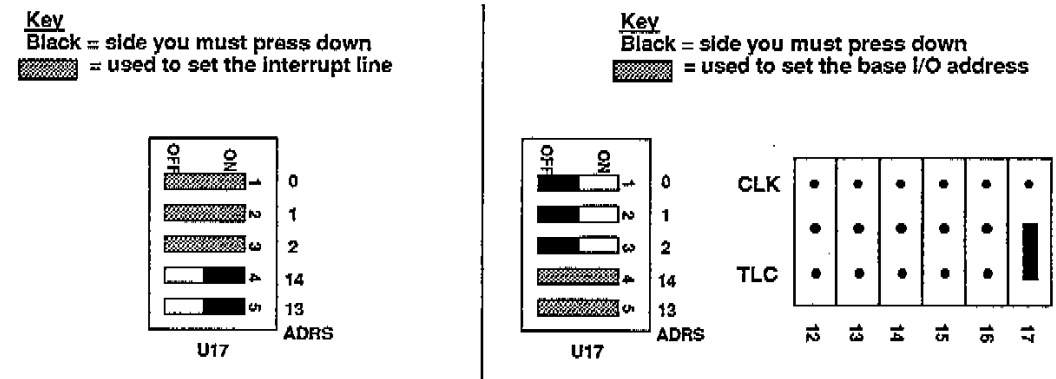


Figure 3-1. Default Switch Settings for the GPIB Controller Cards.

INSTALLING THE PERSONAL COMPUTER SOFTWARE

Prior to using this procedure be sure Lotus 1-2-3 software has been installed.

1. Place the 278X Adjustment Software disk in floppy drive and close the drive door.
2. Change the default drive to the floppy (for example a:).
3. To establish operating parameters for the 1-2-3 initialization program type:

   123init<RETURN>

4. Start the installation program by typing:

   install<RETURN>.

7. Follow the on-screen instructions to complete the installation. When prompted for path name for 1-2-3 program files, enter the path for the 1-2-3 program itself.

   Batch files to run VR Adjustment and RF Attenuator Correction are placed in the root directory of the hard drive. Your path environment variable must include root to run these programs from any directory (for example c:\).

SETTING UP THE TEST EQUIPMENT

1. Remove power from the instrument by disconnecting the power cord on the rear panel.
2. Remove VR assembly as per instructions in section 4.
3. Connect VR assembly test setup as illustrated in Figure 3-12. The Extender Cable from P507 on the mother board to the module is part of the optional Field Service Kit.

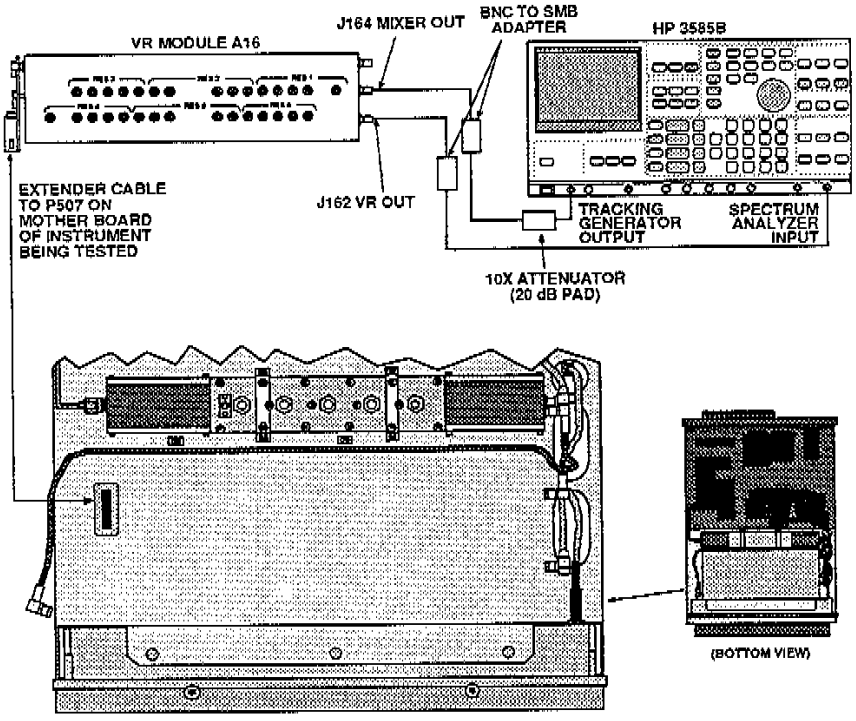


Figure 3-12. VR Module Test Setup.

4. Connect the PC GPIB interface port to the instrument PORT 1 on the rear panel.
5. Re-connect the power cord to the rear panel power connector.
6. Apply power to the instrument and test equipment.
7. Set the test equipment as follows:

HP 3585B Spectrum Analyzer

Center Frequency	4 MHz
Frequency Span	100 kHz
Reference Level	15 dBm
Vertical Display	2 dB/Div
REF LVL TRACK	on

Tracking Generator

Output	0 dBm

RUN THE 278X ADJUSTMENT SOFTWARE

NOTE

Be sure the computer software has been installed and the test setup connected before proceeding.

1. To start the VR Adjustment software on the PC type:

   VRCAL <RETURN>

NOTE

After power has been applied, allow the module 20 minutes to stabilize.

During the following procedure, four commands are available; Next, Previous, Step, and Quit. The commands are executed by typing the first letter of the command (n for next, p for previous, s for step, and q for quit.) Next and Previous commands allow moving forward and backward in the program. Step allows selecting a particular step number (4 through 14) out of sequence. Quit exits the program.

2. Using the S(tep) command select step number 4 to begin the adjustment procedure. Refer to Figure 3-13.

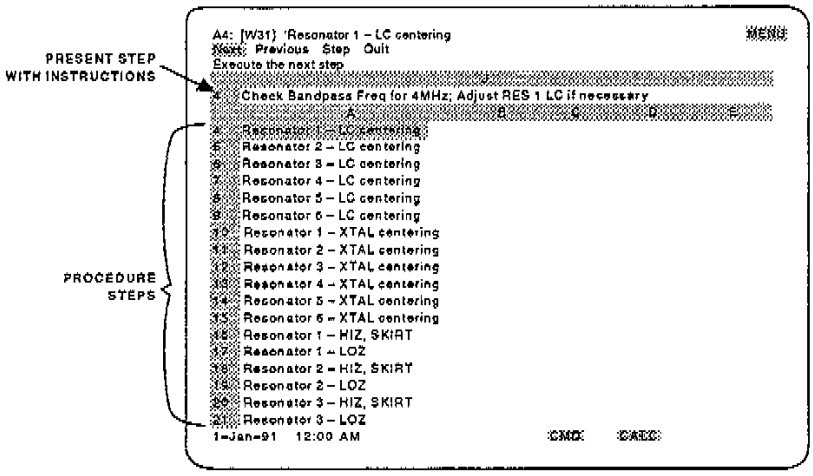


Figure 3-13. VR Adjustment spreadsheet display on the PC.

LC Centering Adjustment (Steps 4 – 9)

For the Resonator LC Centering adjustment steps 4 through 9, perform the adjustments indicated in the instruction area of the screen. See Figure 3-13 and Figure 3-14.

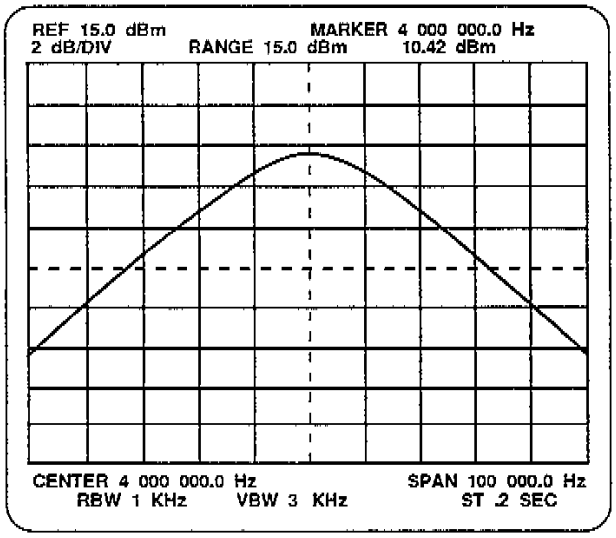


Figure 3-14. Resonator LC Centering properly adjusted.

XTAL Centering Adjustment (Steps 10 – 15)

1. Set the test spectrum analyzer span to 200 Hz, range to 0 dBm and check that the REF LVL TRACK is on.
2. For the XTAL Centering adjustment steps 10 through 15, perform the adjustments indicated in the instructions area of the screen. See Figure 3-15.

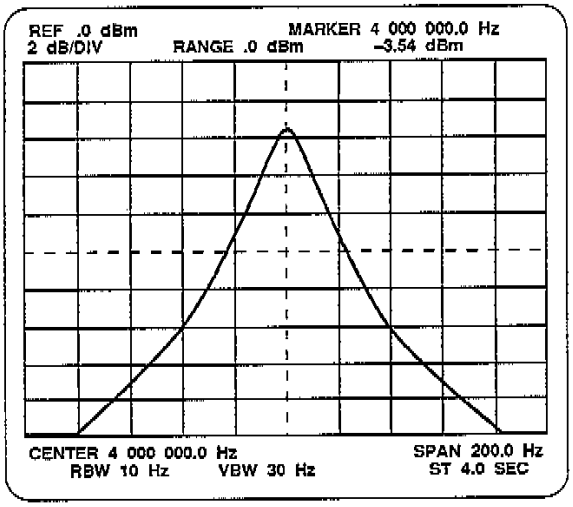


Figure 3-15. XTAL Centering properly adjusted.

HIZ SKIRT and LOZ Adjustment (Steps 16 – 27)

1. Set the test spectrum analyzer span to 50 kHz, vertical display to 2 dB/div, and range to 20 dBm.
2. Perform the adjustment indicated on screen for step 16.
3. Change the test spectrum analyzer span to 20 kHz and perform the adjustment indicated on screen for step 17.
4. Return to step 16. Repeat steps 16 and 17 to eliminate interaction. Refer to Figure 3-16 and Figure 3-17.

NOTE

Do not adjust the skirt of the signal during the LOZ steps.

When adjusting RES 6, set the test spectrum analyzer span to 5 kHz.

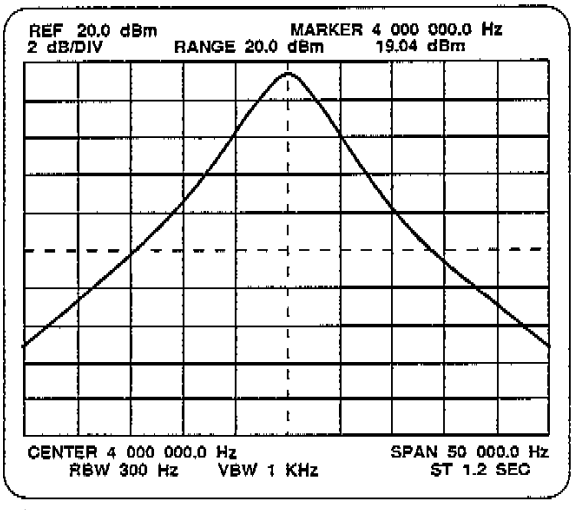


Figure 3-16. Proper adjustment of HIZ and SKIRT

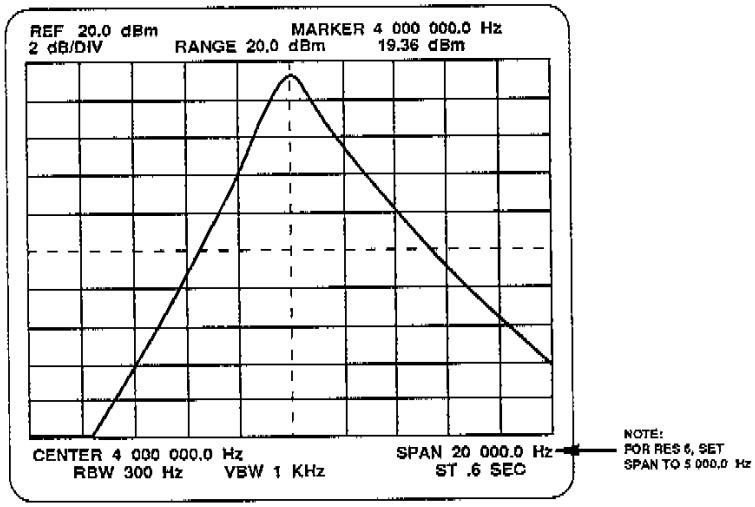


Figure 3-17. Proper adjustment of LOZ.

5. Continue with step 18 through 27 adjusting each as was done in steps 1 through 4.

3 MHz Filter Shape & Centering Adjustment (Step 28)

1. Remove the cover of the VR module by removing the six screws.
2. Move the tracking generator output from J164 (MIXER OUT) to J161 (25 MHZ RF). See Figure 3-18.
3. Set the test spectrum analyzer span to 5 MHz, vertical display to 2 dB/DIV, range to 0 dBm, and center frequency to 25 MHz.
4. Adjust as indicated in the instruction area of the screen. See Figure 3-19.

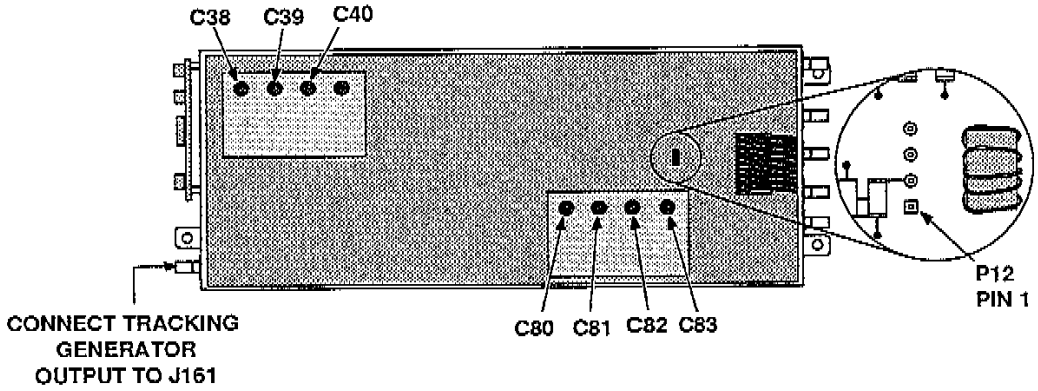


Figure 3-18. VR Module internal adjustments and test points.

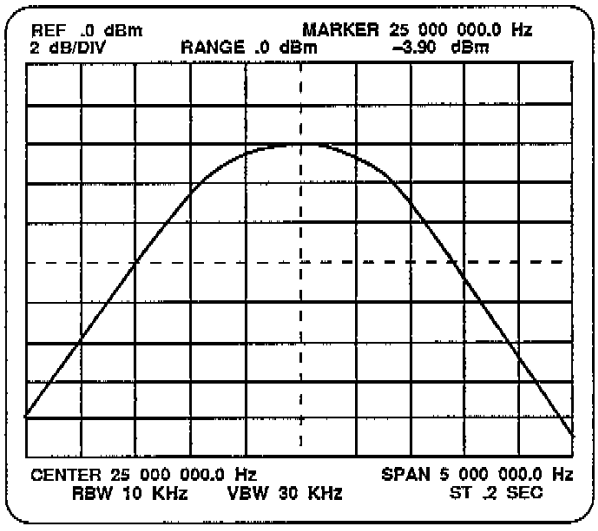


Figure 3-19. Proper 3 MHz filter shape and centering adjustment (C38, C39, and C40).

Bandpass and 33 MHz Notch Adjustment (Step 29)

1. Remove the jumper from pins 2 and 3 of P12. See Figure 3-18.
2. Connect the test spectrum analyzer input to pins 1 and 2 of P12 (ground to pin 1 and signal to pin 2) with the BNC to square pin cable (from the service kit).
3. Set the test spectrum analyzer span to 20 MHz, vertical display to 10 dB/division, and reference level to –25 dBm.
4. Tune the test spectrum analyzer center frequency to 33 MHz.
5. Adjust C81 for maximum null (notch) at 33 MHz. Refer to Figure 3-20.

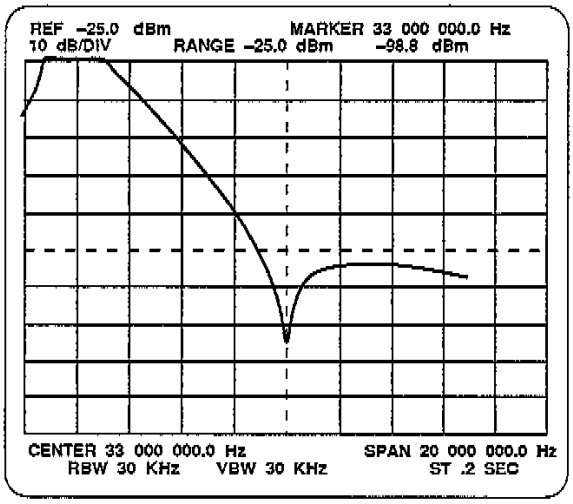


Figure 3-20. 25 MHz Bandpass and 33 MHz Notch filter.

6. Set the test spectrum analyzer center frequency to 25 MHz, frequency span to 5 MHz, vertical display to 2dB/DIV and range to –15 dBm.
7. Adjust C80, C82, and C83 for a signal centered at 25 MHz with flat-top response; refer to Figure 3-21.
8. Repeat step 5 (33 MHz notch) and readjust if necessary.

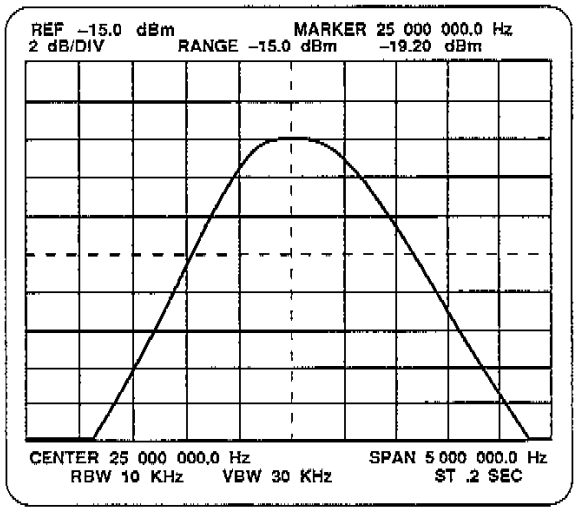


Figure 3-21. 25 MHz Bandpass properly aligned.

9. Remove the cable to P12 and re-connect the jumper to pins 2 and 3 (Figure 3-18).

25 MHz Osc Adjustment (Step 30)

NOTE

If the module you are adjusting does not have the 25 MHz OSC access hole in the cover, it will be necessary to remove the cover to make this adjustment. Keep the cover in place except when actually making the adjustment.

1. Install the VR assembly cover and allow five minutes warm-up.
2. Disconnect the tracking generator output then, connect the test spectrum analyzer input to J164 (MIXER OUT)
3. Set the test spectrum analyzer center frequency to 4 MHz, span to 5 kHz, range to –25 dBm, vertical display to 2dB/Div, and reference level to –36 dBm.
4. Use the n(ext) command on the computer to select step 30.
5. Adjust the 25 MHz Osc for an output (at J164) of 4 MHz ±20 Hz. Refer to Figure 3-22.

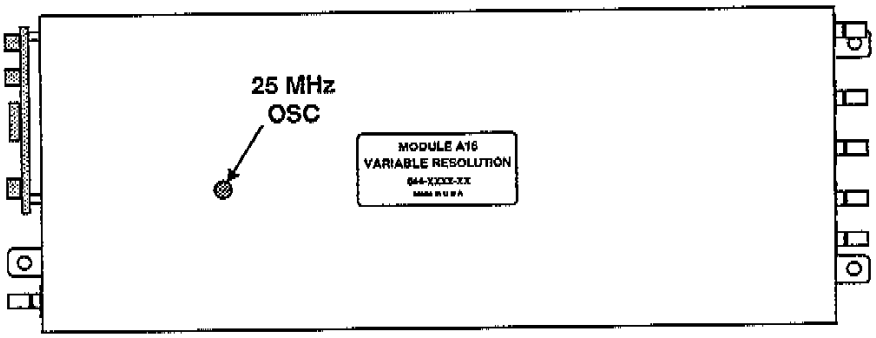


Figure 3-22. Location of 25 MHz Oscillator adjustment.

6. Observe the output for approximately 5 minutes and adjust the 25 MHz Osc to meet the ±20 Hz specification at the end of the five minute time period.
7. Disconnect the test equipment and reinstall the module.

O. RF ATTENUATOR CORRECTION

To successfully complete this procedure, the accuracy of the external step attenuator used must be known. Inaccuracy for the 10 dB steps must be ≤0.5 dB. These values will be requested during the installation procedure.

INSTALLING THE COMPUTER HARDWARE AND SOFTWARE

This procedure uses the same software program as was used for the previous (VR) adjustment procedure. If necessary, refer to the installation procedure of step *N. VARIABLE RESOLUTION ASSEMBLY ADJUSTMENTS* for instructions.

NOTE

During the following procedure, RF Attenuator spreadsheet commands are executed by typing the first letter of the command. The notation to type "n" (next command) is n(ext).

RUN THE RF ATTENUATOR CORRECTION SOFTWARE

1. Connect the test setup as shown in Figure 3-24.

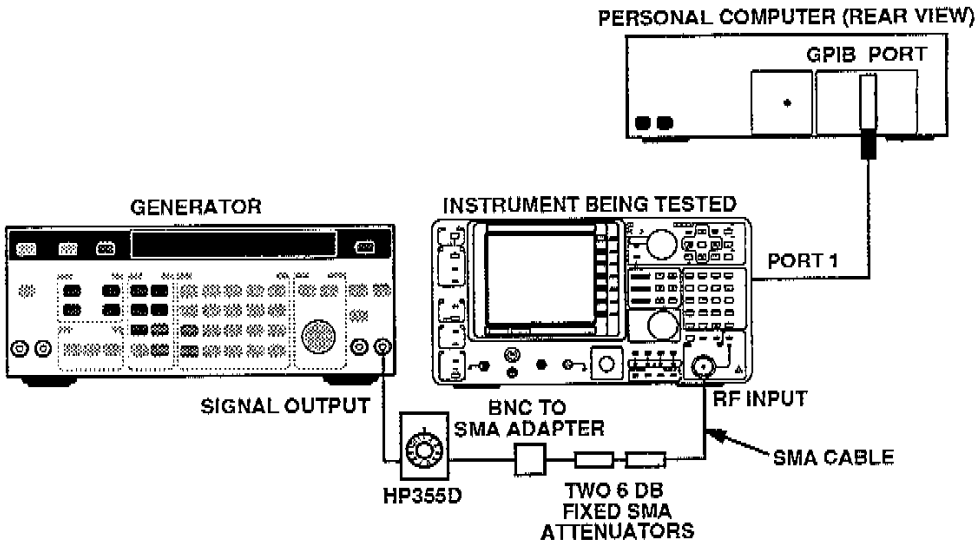


Figure 3-24. Test equipment connections for RF Attenuator Correction.

2. To start the RF Attenuator Correction software on the PC type:

   attencal<RETURN>

NOTE

During the correction procedure (steps 4-17) the Next and Previous commands allow moving forward and backward in the program. Step allows selecting a particular step number out of sequence. Quit exits the program.

3. Once the 1-2-3 spreadsheet is open enter the instrument serial number (for example B010231), then enter the external attenuator calibration factors (actual attenuation of test attenuators) as follows.

   - type o(ther) to go to the OtherMenu.
   - type e(xternal) to select Ext_Attenuation and enter the ID of the external attenuators. This will be a calibration number, poll number, or other number to uniquely identify the 10 dB attenuator.
   - follow the prompt to enter the ACTUAL attenuation of the external attenuators.
   - type o(ther) to go to the OtherMenu then s(ave) for Save_Atten.

NOTE

The last step in the above procedure saves the attenuator values to a file named with the ID of the attenuators. If attenuator values have been entered during a previous adjustment procedure, they can be recalled by using the OtherMenu and R(etrieve)_Atten commands.

4. Set the test equipment as indicated in the prompt. Refer to Figure 3-25.

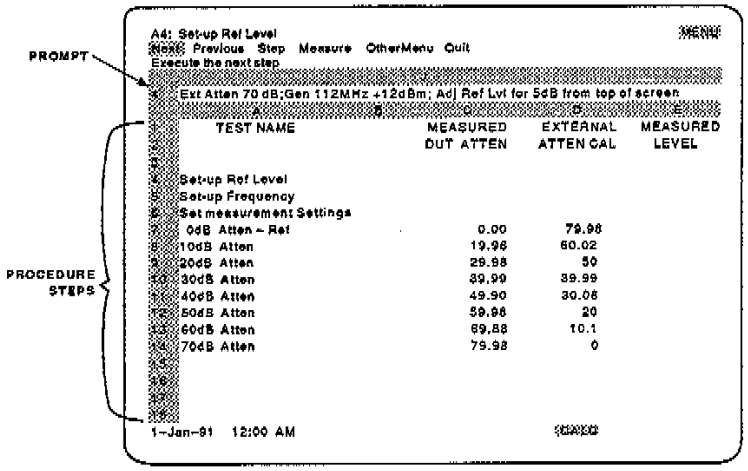


Figure 3-25. RF Attenuator Correction spreadsheet display on the PC.

5. Continue the test setup with steps 5 and 6 setting the test equipment as indicated in the prompt.

NOTE

During the following steps (7-14) ***do not use the PEAK FIND function*** *on the instrument being tested, or move the marker in any other way.*

6. For the RF Attenuator Correction steps 7 through 14, perform the actions indicated in the prompt. To enter the value measured for each step, type the M(easure) key on the PC before proceeding to the n(ext) step.
7. After step 14 is complete, check to see that the MEASURED DUT ATTEN at each step is no more than 1 dB in error. If so, either a measurement error or a DUT RF attenuator problem is indicated.
8. After successful completion of the measurements, type O(ther) and then D(own load) to store the correction data into instrument calibration EEROM.
9. Type q(uit) to exit the atten cal spreadsheet and disconnect the test equipment from the instrument.

P. SWEEP TRACKING ADJUSTMENT

This procedure requires that the personal computer (PC) be connected to the instrument through the RS-232 port on the Processor Extender board. Connect the PC as per the instructions in Appendix B *USING THE PROCESSOR EXTENDER.*

NOTE

The instrument must have had power applied to it, either in the standby mode (STBY light lit) or the operating mode, for at least one hour before making the following adjustment.

1. With the instrument connected to send/receive data through the RS-232 port, start the communication software (Kermit) on the PC.

2. Once the PC is displaying data from the instrument, press the SETTINGS PRESET key.
3. Press the UTIL key, then press the Service Menu key, followed by the Enter Keybd Mode key.
4. Type the command **prsw** <RETURN> from the PC keyboard.
5. Connect the digital voltmeter to pin 9 on the instrument's rear-panel ACCESSORY port. See Figure 3-26.

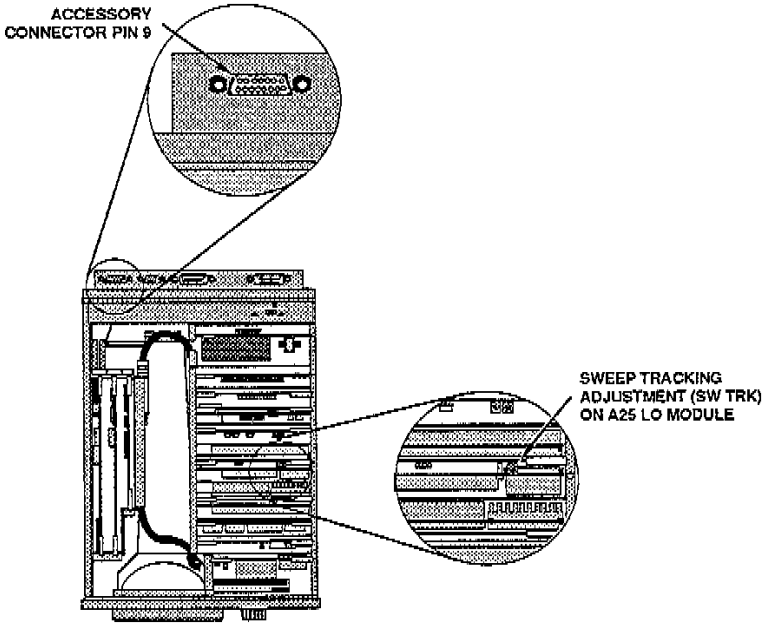


Figure 3-26. Location of Sweep Tracking Balance Test Points and Adjustment.

6. Observe the menu on the computer screen. Select the first item by typing 1 <RETURN> on the PC keyboard, and wait a few seconds to complete the step.
7. Measure and note the voltage at pin 9.
8. Select item two by typing 2 <RETURN> on the PC keyboard, and wait a few seconds to complete the step.
9. Adjust the Sweep Tracking adjustment located on the LO module (see Figure 3-26) so that the voltage measured at pin 9 is the same as was measured in step 7.
10. Repeat steps 6 through 9 until the voltage measured at pin 9 is the same for each step.
11. Remove the voltmeter from pin 9.
12. Type **fpan** <RETURN> from the PC keyboard to return control to the instrument front panel.
13. Exit the Kermit program on the PC.
14. Press the POWER key to remove power from the instrument. Then disconnect the instrument power cord from the power source.
15. Disconnect the RS-232 cable from between the Processor Extender board and the RS-232 port of the PC. Disconnect the Main Processor board from the Processor Extender board.

16. Open switch S11-3 on the A41 Main Processor to disable the Service Mode.
17. Remove the Processor Extender board and re-install the Main Processor board in the instrument.
18. Re-connect the power cord and push the POWER key.

Q. LIN BASELINE ADJUSTMENT

1. Press the PRESET key.
2. Using the FREQUENCY key and KEYPAD enter a frequency of 112 MHz, then using the SPAN key and KEYPAD enter a span of 10 MHz.
3. Press the REF LEVEL key, and press the Vert Scale Menu key. Then press the Scale DB v w menu key to select the V (voltage) scale.
4. Adjust the LIN offset adjustment on the Log Processor board (see Figure 3-27) by first rotating the adjustment counterclockwise until the baseline moves up from the bottom graticule line. Then, reverse rotation (clockwise) and adjust the baseline to a point where it reaches the bottom graticule line.

NOTE

When adjusting the LIN offset, a point will be reached where continued clockwise rotation no longer moves the baseline down. Once this point has been reached, do not continue rotating the adjustment. The proper adjustment is when this point is reached. This point should correspond to the bottom graticule line.

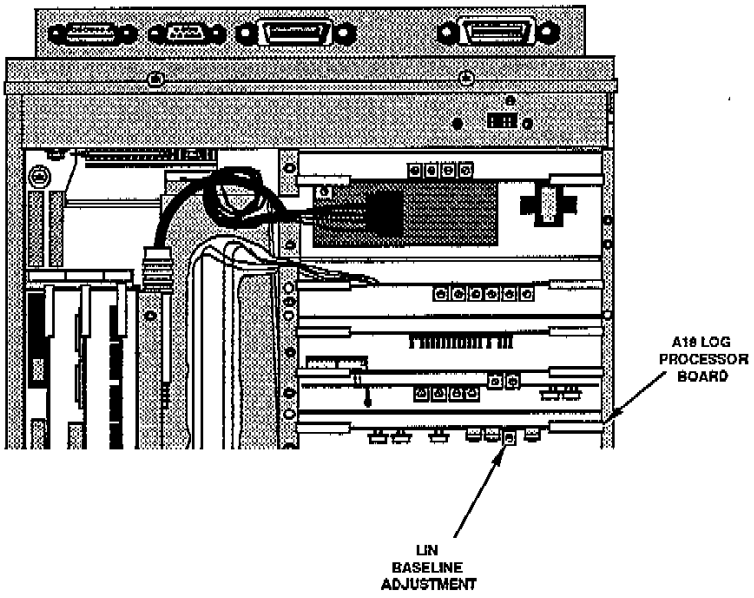


Figure 3-27. Lin Baseline Adjustment.

R. 100 MHZ CALIBRATOR AMPLITUDE ADJUSTMENT

1. Press the PRESET key.
2. Press the instrument's INPUT key, and press the RefSig Out single/COMB menu key to select SINGLE.
3. With the power meter turned off, connect the HP8481D Power Sensor Head to either channel of the Hewlett-Packard HP432A Power Meter, then turn the power meter on. (The power meter should be turned off when connecting the power sensor head to prevent damage.)
4. Connect a Hewlett-Packard HP11708 30 dB attenuator to the POWER REF connector of the power meter.
5. Press the power meter Channel A key (or Channel B if the power head is connected to channel B), and press the ZERO key. (Wait a few seconds for the zeroing routine to complete.)
6. Press the power meter CAL FACTOR key and, using the power meter keypad, enter the REF CF% value that is recorded on the power sensor head (for example, 97.0 ENTER).
7. Connect the HP8481D Power Sensor head to the HP11707 30 dB attenuator that is connected to the power meter Power Ref connector (as shown in Figure 3-28A).

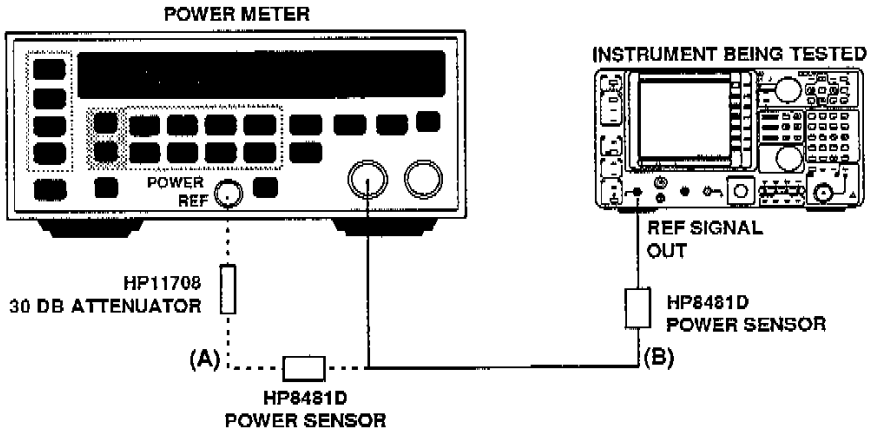


Figure 3-28. Test Equipment Connections for 100 MHz Calibrator Amplitude Adjustment.

8. Press the power meter OSC key, and press the CAL ADJ key. Then enter the REF CF% value entered in step 6 from the power meter keypad. The power meter should then read –30.00 dBm.
9. Connect the power sensor head to the REF SIGNAL OUT connector of the instrument under test (as shown in Figure 3-35B).
10. Adjust the 100 MHz Amplitude adjustment on the 100 MHz Calibrator module (see Figure 3-29) for –20.00 dBm on the power meter.
11. Disconnect the power sensor head (power off) and press the instrument SETTINGS PRESET key.

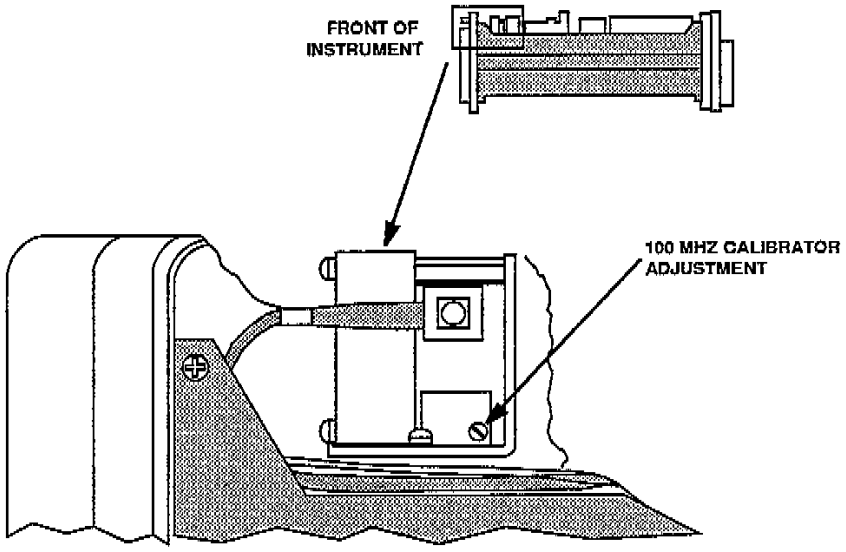


Figure 3-29. 100 MHz Amplitude Adjustment

S. PERFORM SELF-CORRECTION SEQUENCE

Perform the following self correction routines to complete the adjustment of the instrument.

NOTE

For proper operation, be sure to perform the corrections in the order given.

HORIZONTAL FREQUENCY SELF-CORRECTION

NOTE

The Instrument must have been operating for at least one hour before making the following correction.

1. Press the UTIL key to display the UTILITY menu, and press the Freq Corr Menu key to select the Frequency Correction menu.
2. Press the Run Freq Corr Cycle key to initiate the automatic frequency calibration routine. This routine takes approximately 3 minutes to complete.
3. When the Frequency Correction routine is complete, press the Store Data key to store the data in EEPROM.

VERTICAL SELF-CORRECTIONS

Peak Detectors Gain and Offset Self-Correction

1. Press the UTIL key, then press the Misc Corr Menu key. From the MISC CORR menu, press the Peak Dtect Menu key.
2. Press the Run Corr Cycle menu key.
3. When the peak-detector-correction routine is complete, press the Store Data key to store the data in EEPROM.

Resonator Tracking Self-Correction (first time)

1. Press the UTIL key, then press the Vert Corr Menu key. From the VERT CORR menu, press the VR Reson Menu key.
2. Press the Run Corr Cycle menu key to start the automatic resonator-tracking-correction routine.
3. When the resonator-tracking-correction routine is complete, press the Store Data key to store the data in EEPROM.

Display Law Self-Correction

1. Connect a 50 Ω cable between the REF SIGNAL OUT and the RF INPUT connectors.
2. Press the UTIL key, then press the Vert Corr Menu key. From the VERT CORR menu, press the Display Law Menu key. Then, press the Run Corr Cycle menu key to initiate execution of the automatic display-law-correction routine.
3. When the display-law-correction routine is complete, press the Store Data key to store the data in EEPROM.

Log Self-Corrections

1. Connect the signal generator to the instrument's RF INPUT connector through a pair of variable step attenuators (10 dB and 1 dB, respectively) and a pair of 6 dB fixed attenuators (as shown in Figure 3-30).

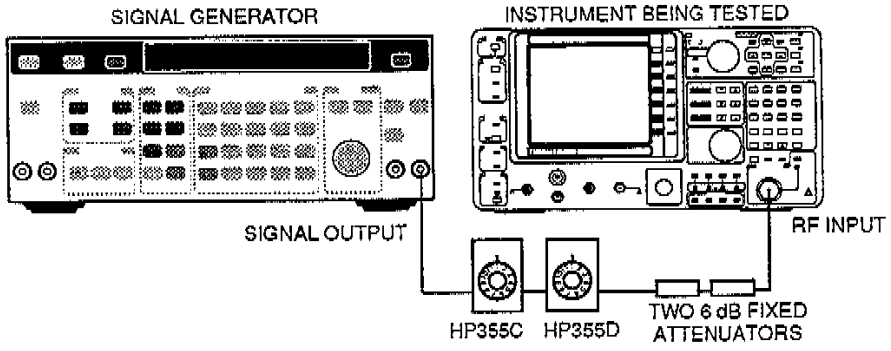


Figure 3-30. Log Self-Correction Test Setup.

2. Press the UTIL key, select Misc Corr Menu and then select Log Corr Menu.
3. To start the routine, press the Start Corr key and follow the on-screen instructions for the log-correction routine.
4. When the log-correction routine is complete, press the Store Data key to store the data in EEP-ROM.
5. Disconnect the signal generator and attenuators from the instrument.

Gain Steps Self-Correction

1. Press the UTIL key, then press the Vert Corr Menu key. From the VERT CORR menu, press the Gain Step Menu key.
2. Press the Run Corr Cycle menu key to start the gain step vertical-correction routine.
3. When execution of the gain-step-vertical-correction routine is complete, press the Store Data key to store the data in EEPROM.

Resonator Tracking Self-Correction (second time)

1. Press the UTIL key, then press the Vert Corr Menu key. From the VERT CORR menu, press the VR Reson Menu key.
2. Press the Run Corr Cycle menu key to start the automatic resonator-tracking-correction routine.
3. When the resonator-tracking-correction routine is complete, press the Store Data key to store the data in EEPROM.

Resolution Bandwidth Self-Correction

1. Press the UTIL key, then press the Vert Corr Menu key. From the VERT CORR menu, press the Res BW Menu key.
2. Press the Run Corr Cycle menu key to start the resolution bandwidth-correction routine.
3. When execution of the resolution-bandwidth-correction routine is complete, press the Store Data key to store the data in EEPROM.

External Mixer Input Self-Correction

1. Using the Power Meter, adjust the synthesizer for an output of –40 dBm at 3.525 GHz.
2. Using an appropriate 50 Ω cable, connect the synthesizer signal to the EXTERNAL MIXER input as shown in Figure 3-31.

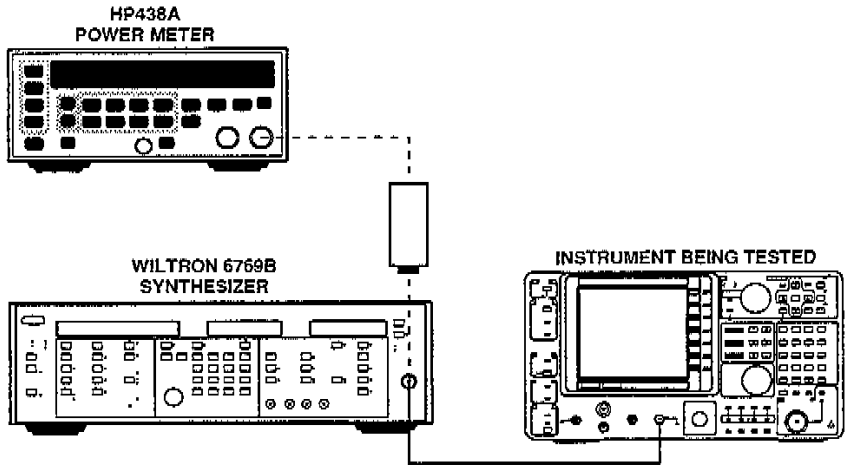


Figure 3-31. External Mixer Input Correction Equipment setup.

3. Adjust the instrument Center Frequency and Reference level to display the generator output. Then vary the generator frequency in, 100 kHz steps, to peak the on-screen signal.
4. Press the UTIL key, then press the Misc Corr Menu key. From the MISS CORR menu, press the ExtMx Corr Menu key.
5. Press the Run Corr Cycle menu key to start the external mixer input correction routine.
6. When the routine is complete, press the Store Data menu key.
7. Press the SETTINGS PRESET key.
8. Disconnect the signal generator from the EXTERNAL MIXER input.

T. FAST SWEEP RATE ADJUSTMENTS

YTO DRIVER BOARD FAST SWEEP ADJUSTMENT

This adjustment matches the First local Oscillator (YTO) static and dynamic frequencies.

1. Connect the test setup as shown in Figure 3-31 (previous step)
2. Adjust the generator output for –18 dBm at 9.5 GHz.
3. Set up the spectrum analyzer as follows:

FREQUENCY	9.5 GHz
Vert Scale	5 dB/
SPAN	6.0 GHz
RES BW	10 MHz
REF LEVEL	–15 dBm
VIDEO BW	10 MHz

4. Assign the SWEEP rate to KNOB 1 by pressing the SWEEP key then selecting Knob 1 from the SWEEP menu.
5. Change the sweep rate to 500 mS with KNOB 1.
6. Set R1 to mid-range (see Figure 3-32).

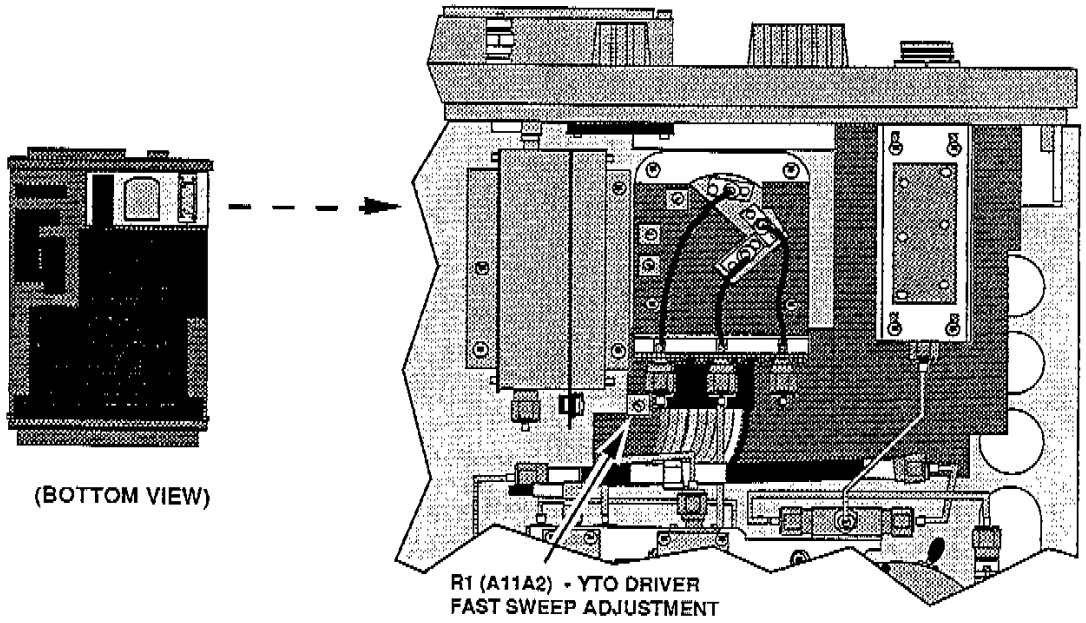


Figure 3-32. Location of YTO Driver Fast Sweep adjustment.

7. Press PEAK FIND and read the frequency of the signal. Note this value.
8. Change the sweep rate to 50 mS.
9. Press PEAK FIND and read the frequency of the signal.
10. Adjust the YTO Driver Fast Sweep control, R1 on the YTO driver board, until the frequency measured in step 9 matches the frequency noted in step 7.
11. Use KNOB 1 to step the sweep rate to 500 mS. At each step use the PEAK FIND function to check the frequency of the signal. If the frequency does not remain constant at each step, repeat steps 5 through 10 to eliminate interaction.

PRESELECTOR DRIVER FAST SWEEP ADJUSTMENT

This adjustment matches the static and dynamic insertion loss of the preselector by offsetting the preselector to place the signal on the preselector filter skirt.

1. Connect test setup as illustrated in Figure 3-33.

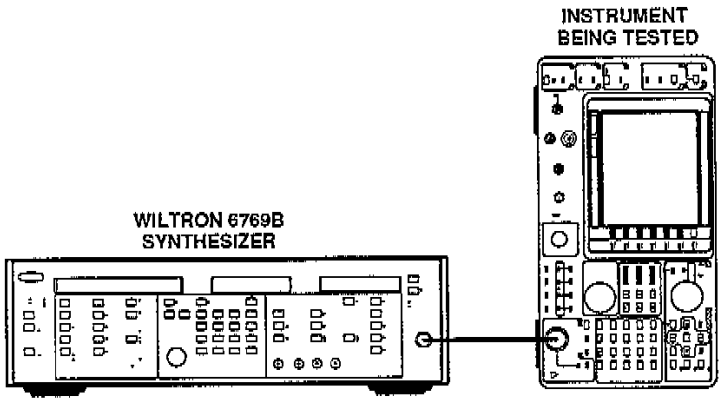


Figure 3-33. Fast Sweep Preselector Driver adjustment setup.

2. Connect the instrument GPIB interface to the personal computer (PC).

NOTE

For this adjustment, the 278X instrument is controlled by a personal computer using the GPIB interface. If necessary, refer to "INSTALLING THE PERSONAL COMPUTER HARDWARE" *in step* N. VARIABLE RESOLUTION ASSEMBLY ADJUSTMENT *to install the GPIB card into your personal computer.*

3. Set the generator output for –18 dBm at 9.5 GHz.

4. Set the spectrum analyzer as follows:

FREQUENCY	9.5 GHz (use FREQUENCY key and KEYPAD)
SPAN	200 MHz
REF LEVEL	–15 dBm
Vert Scale	5 dB/
RES BW	AUTO
VIDEO BW	AUTO
SWEEP	500 ms

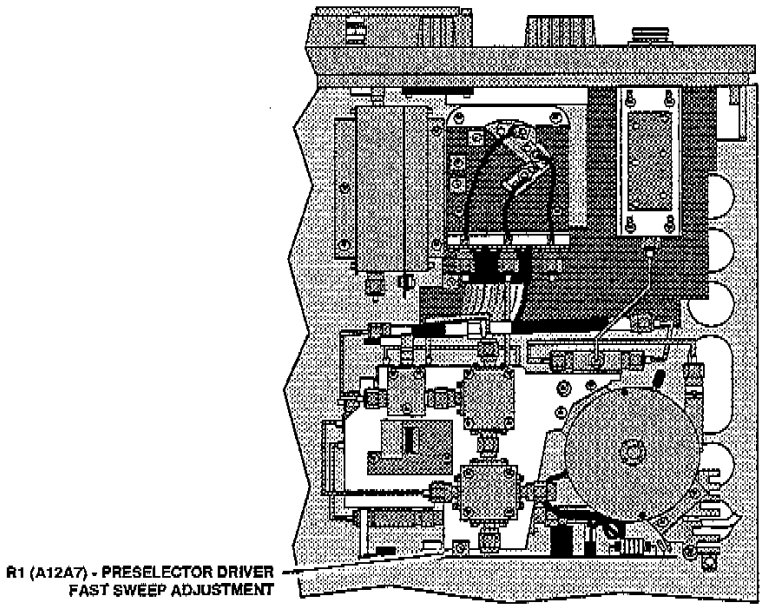


Figure 3-34. Fast Sweep adjustment and test point location.

5. With the 278X Adjustment Software installed as described earlier in the ***VARIABLE RESOLUTION ASSEMBLY ADJUSTMENT*** section type the following.

   presel 1<RETURN>.

NOTE

*In the example in the previous step, **presel** is the program to be run and **1** is the GPIB address of the instrument being tested. The address is required.*

6. Your PC should now display the slope and offset calibration data for the preselector in your instrument at this band.

NOTE

During this program the values for offset is varied using the arrow keys on the PC keyboard. Up arrow increases the value and down arrow decreases the value.

7. Using the up/down arrow keys, vary the offset until the amplitude of the 9.5 GHz signal displayed on the instrument, drops 1 division (5 dB).
8. Using the keypad enter a SPAN of 6 GHz.
9. Assign the SWEEP rate to KNOB 1 by pressing the SWEEP key then selecting Knob 1 from the SWEEP menu.
10. Adjust the Preselector Driver Fast Sweep Adjustment R1 (A12A7) until no change in amplitude occurs when the sweep speed is varied from 500 ms to 50 ms (with KNOB 1). Refer to Figure 3-34.
13. After the adjustment is complete, press UTIL, Freq Corr Menu, and Recall from Store keys to restore the offset value.
14. Exit the program by typing <Cntl>C.

PART II. AMPLITUDE FLATNESS ADJUSTMENT PROCEDURE

The following procedure measures the instruments response over the input frequency range to a constant amplitude input. Once this data is available, it is transferred to the instrument operating system. The operating system uses the data to generate corrections to maintain a constant amplitude over the input frequency range.

The following steps describe the adjustment process.

- Setup computer
- Track preselector and measure uncorrected flatness response
- Transfer data to instrument operating system
- Check corrected flatness

ADJUSTMENT ENVIRONMENT

The ambient temperature for the instrument should be within ±5° C of the temperature where self-correction of the instrument was performed. The ambient temperature during factory calibration is 25° C.

Before making any of these adjustments, allow the instrument to warm up for at least one hour.

A. COMPUTER SETUP AND SOFTWARE INSTALLATION

OVERVIEW OF THE INSTALLATION PROCEDURE

For this adjustment the 278X is controlled by a personal computer using the GPIB interface. If necessary, refer to *"INSTALLING THE PERSONAL COMPUTER HARDWARE"* in step *N. VARIABLE RESOLUTION ASSEMBLY ADJUSTMENT* to install the GPIB card into your personal computer.

The following steps describe the installation process.

- Install the test software.
- Run the system configuration program (CONFIG).
- Connect the personal computer to control the test instrument.
- Run the test equipment characterization program (CHAR).

NOTE

These steps are required for initial installation only. After the initial installation, it is not necessary to run CONFIG or CHAR as long as the system remains intact.

INSTALL THE FLATNESS AND RESIDUAL SIGNALS TEST SOFTWARE

The Flatness and Residual Signals Test software is contained on a set of 5¼" floppy disks supplied with this manual (278X Automated Tests). Use the following procedure to install the software onto the personal computer:

1. Install disk 1 in drive A of the personal computer.
2. Set the default drive for A by typing:

   `A:<ENTER>`

3. Type the following command to install the flatness software on your hard disk:

   `Install<ENTER>`

   A prompt will instruct you when to switch disks.

4. Re-boot your PC to incorporate the changes to the autoexec.bat file.

NOTE

INSTALL.BAT is a batch file that creates a directory on your hard disk (called TEKCATS) and several sub-directories. It then copies the automated tests software into these directories.

CONFIGURE THE TEST SYSTEM (CONFIG)

The CONFIG program generates a table that describes the test equipment being used and their respective GPIB addresses. It also creates a file for the power sensors, containing the calibration factors to be used at each frequency.

To start the program to configure the test system type:

`CONFIG<ENTER>`

The main menu will be displayed with the following selections.

```
Create a New System Configuration
List the New System Configuration
Exit to DOS
```

Select "`Create a New System Configuration`" and you will be asked to specify the following:

- Signal source below 10 MHz (limited to the Hewlett Packard HP 3336C generator).
- High frequency signal source. See Table 3-5.
- Power Meter used.
- Power Sensor identification number for power sensor above 50 MHz.. This is an arbitrary number of your choice.
- Power Sensor calibration factors from the data printed on the power sensor. Be sure to include 50 MHz reference power. Enter the data in increasing order of frequency.

NOTE

Be sure to include the 50 MHz reference cal factors.

The upper limit of the test range is determined by the high frequency generator and/or power sensor you specify. The test will terminate at the upper limit of the generator and/or power sensor range. See Table 3-5.

Table 3-5. Equipment supported by the 278X Automated Tests Software

Function	Range	Model
Signal Generators	100 Hz to 10 MHz	Hewlett-Packard HP 3336C
	10 MHz to 20 GHz	Hewlett-Packard HP 83620A
		Hewlett-Packard HP 8341A
	10 MHz to 26.5 GHz	Hewlett-Packard HP 8340A Wiltron 6759A/B
	10 MHz to 40 GHz	Hewlett-Packard HP 83640A Wiltron 6769A/B
	2 GHz to 40 GHz	Hewlett-Packard HP 83642A
	26.5 GHz to 40 GHz	Wiltron 6740A/B
Power Sensors	10 MHz to 18 GHz	Hewlett-Packard HP 8481A
	100 kHz to 4.2 GHz	Hewlett-Packard HP 8482A
	50 MHz to 26.5 GHz	Hewlett-Packard HP 8485A
	50 MHz to 50 GHz	Hewlett-Packard HP 8487A
Power Meters		Hewlett-Packard HP 438A Hewlett-Packard HP 437B

If you wish to examine the configuration you have just created, select List a New System Configuration. This will display the system configuration.

NOTE

When using the HP 438A power meter, connect the lower frequency sensor to Channel A, and the high frequency sensor to Channel B.

CHANGING SYSTEM CONFIGURATION

If you wish to change system configuration (different generators or power meter) you must re-run CONFIG and re-enter the test equipment being used. If the power sensor is not changed, when prompted for power sensor calibration factors, type <RETURN> and the existing file of data will be used. However, if power meter type is changed, power sensor cal factors should be re-entered.

CONNECT THE PERSONAL COMPUTER TO CONTROL THE TEST INSTRUMENTS

1. Connect the instrument to be tested, signal generators, and power meter to the computer through GPIB cables.
2. Apply power to the instrument and test equipment, then allow a warm up of at least one hour.
3. Set the GPIB address of the instrument to 1 as follows. On the instrument front panel, press the EXT INTFC CONFIG key, then press the Set Port1 Address menu key. Enter 1 from the KEYPAD, and press ENTER. Press the Set Port1 Address key a second time and check that the CRT readout indicates `PORT1 01`.

RUNNING THE TEST EQUIPMENT CHARACTERIZATION PROGRAM (CHAR)

The display flatness test uses a power divider and power meter to compensate for flatness variations in the generators, and for losses in the test system cabling. The flatness test performs this correction by measuring the signal amplitude at power divider Port #3 (refer to Figure 3-35), then calculating the amplitude present at the instrument's RF Input. The error in displayed flatness is then corrected according to the calculated power available at the RF Input.

The CHAR program is designed to measure and record the difference in amplitude between Port #3 and the instrument's RF Input (output of the 3 dB attenuator connected to power divider Port #2).

Test setups for characterizing the power divider output ports are shown in Figures 3-35 and 3-36. Port #3 of the power divider is characterized by measuring its output amplitude with a power meter across the frequency range while Port #2 is terminated with the 3 dB pad and 50 Ω termination. The power meter and termination connections are then swapped to determine the response of Port #2. The amplitude difference between Port #2 and Port #3 is then stored in a data file for later use by the flatness test.

The power divider characterization takes about 1½ hours. To maintain a traceable calibration standard, this characterization must be performed whenever the power divider or the 3 dB attenuator are replaced. We recommended dedicating these components to this test system to minimize characterization requirements.

To characterize the test setup, enter the following at the prompt on the PC type:

CHAR<ENTER>

Follow the on-screen instructions. You will be prompted to make the connections shown in Figure 3-35. Midway through the test you will be prompted to make the connections shown in Figure 3-36. The test will then run to completion.

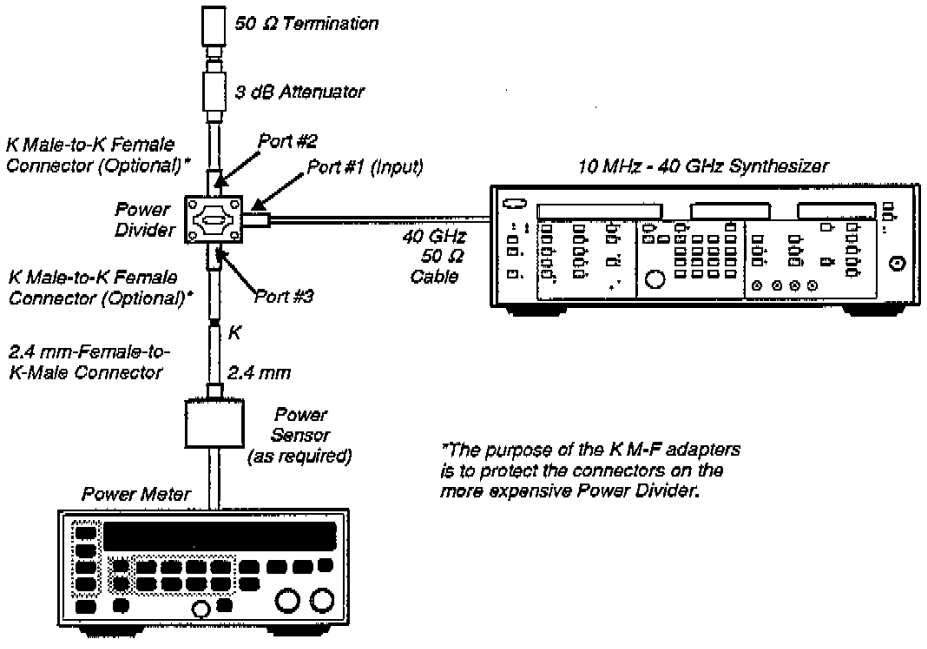


Figure 3-35. Test Equipment Characterization, Port #3

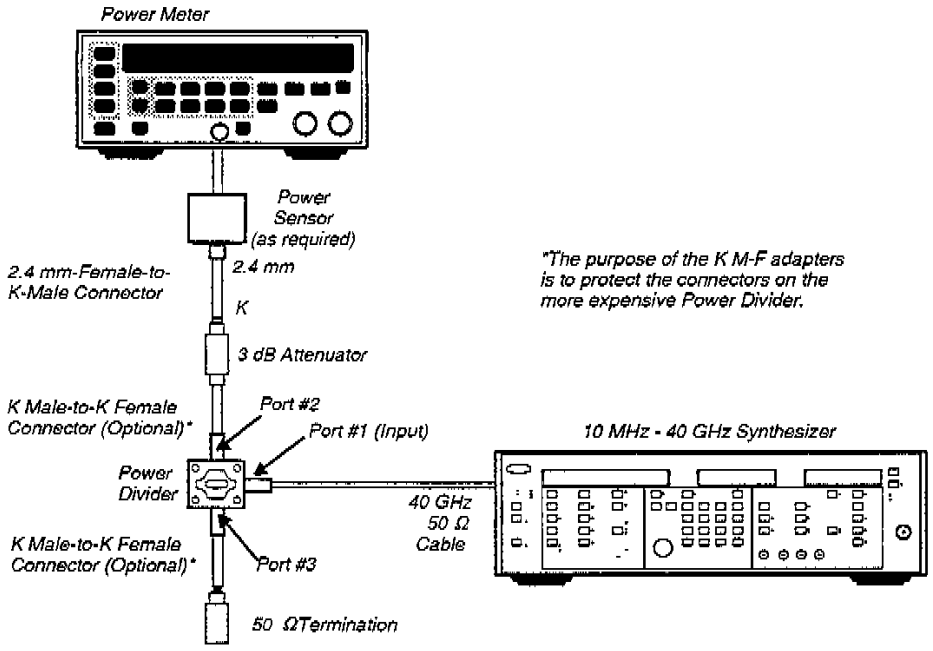


Figure 3-36. Test Equipment Characterization, Port #2

B. PRESELECTOR TRACKING AND FLATNESS MEASUREMENT

This section of the procedure contains two parts. In the first part, the preselector filter is adjusted to track the input frequency. Once the preselector is adjusted, the instruments uncorrected flatness response is measured over the input frequency range.

Allow the instrument to warm up for at least one hour before performing this procedure.

NOTE

During the following procedures, the test equipment you specify (with CONFIG) must cover the full frequency range of the instrument. Only a partial calibration will occur otherwise.

Do not press the help or interrupt keys during the test. Once a test is interrupted, it cannot be resumed at the point of interruption; it must be restarted.

RUN THE 278X PROGRAM

Type the following on the personal computer to begin the 278X program.

```
278X<ENTER>
```

The 278X program is menu driven and requires entry of test conditions. You will be prompted to enter the following during the test sequence:

1. Enter your name or your calibration labs name.
2. Verify the date and time.
3. Enter temperature and humidity information.
4. Select Device Under Test (DUT). Enter selection number to select the 278X model you are testing.
5. Select the CAL sequence from the "Select Sequence" menu.
6. Enter the DUT serial number and press <ENTER>. You will be asked to verify the serial number.

PRESELECTOR TRACKING

At the completion of this program, the tracking data will be automatically stored in the instrument operating system.

1. Enter 3 for Select Test(s) and then select the Preselector Tracking Test.
2. When prompted, connect the test setup as illustrated in Figure 3-38.
3. Select Full Cal from the menu.
4. The preselector tracking will now be run automatically and requires approximately ½ hour to complete.

FLATNESS MEASUREMENT

1. Select Flatness Test.
2. Select First Attenuator to be Tested – 0 dB; then select Last Attenuator to be Tested – 50 dB; Select Frequency Band(s) to be Tested – Full Test. This test requires approximately four hours for a 2782 and 5 hours for a 2784.
3. You will be prompted to make the connection shown in Figure 3-37. This test setup checks the low frequency range from 1 kHz to 10 MHz.

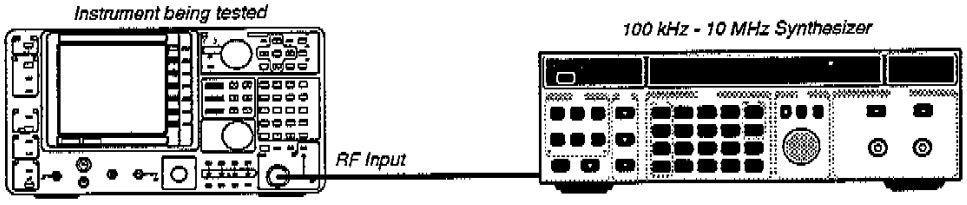


Figure 3-37. Flatness Test Set-up – 10 MHz and below.

4. Next you are prompted to make the connections shown in Figure 3-38, but with the low frequency sensor. After the low frequency test is complete, you will be prompted to make the connections in Figure 3-38, with the HF sensor, to test the range above 10 MHz.

NOTE

If you are using a single channel power meter, when you are prompted to connect another sensor, power down the power meter, switch sensors, power up the power meter and wait for self test to finish. ***Do Not*** *change sensors at any other time in the test, the power on SRQ generated by the power meter will abort the test.*

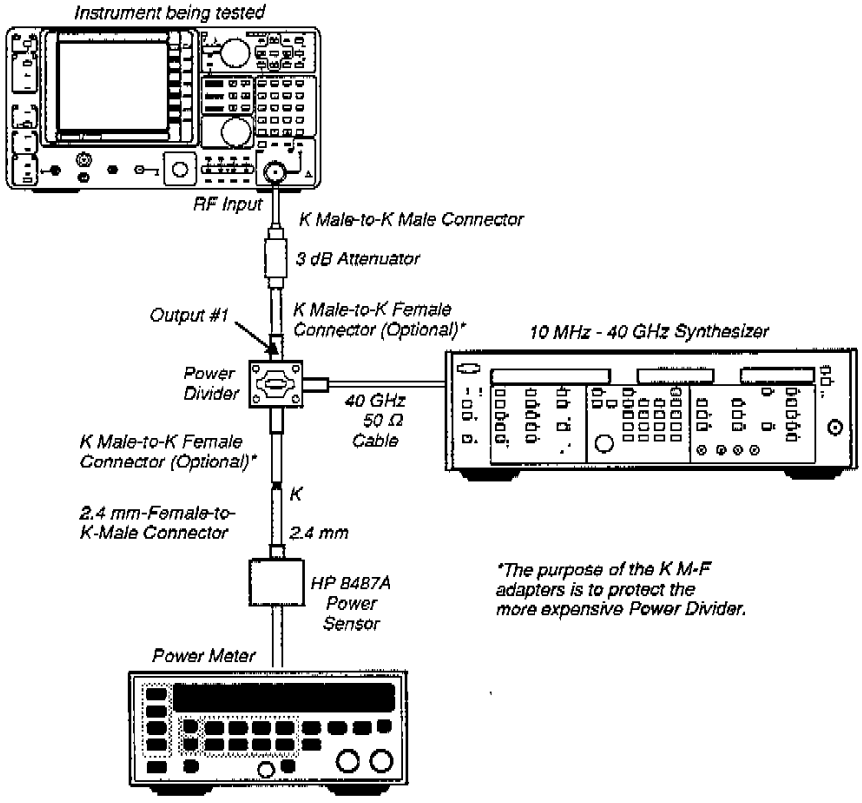


Figure 3-38. Flatness test setup – 50 MHz and above.

EXAMINE THE FLATNESS DATA (PLOTF)

This program draws a series of graphs on the PC monitor, each representing the flatness error data for each RF attenuation setting. The horizontal axis of the graphs represents frequency, with the lowest band on the left and the highest band on the right. The vertical axis shows the flatness response in dB. The vertical scale of the graphs is set automatically to fit all of the data in the window.

Keep in mind that the data you are viewing is un-corrected. After this data is transferred to the instrument, corrections will be generated to compensate for variations in the response.

C. PLOTTING THE FLATNESS TEST RESULTS (PLOTF).

Syntax for plotf is as follows: (entries in braces are optional)

```
plotf dut_type serial_number [-a atten][-b band][-u][-h]
```

`dut-type`: 2782 or 2784

`serial_number`: the full serial number as was entered during the flatness test.

`-a atten`: normally plotf will plot data from all attenuator settings tested. Specifying this option allows you to specify a plot of specified attenuator(s). The first digit of the attenuation should be entered here.

`-b band`: normally plotf will plot data for all frequency bands tested. Specifying this option allows you to specify a plot of specified band(s).

`-u`: specifying this option will cause plotf to plot results from the calibration (adjustment) flatness run for the DUT. This option is not used during performance verification

`-h`: this will cause plotf to automatically hard-copy each plot before plotting the next. If this option is not specified, plotf will pause after displaying each graph.

NOTE

This program requires an EGA or VGA monitor.

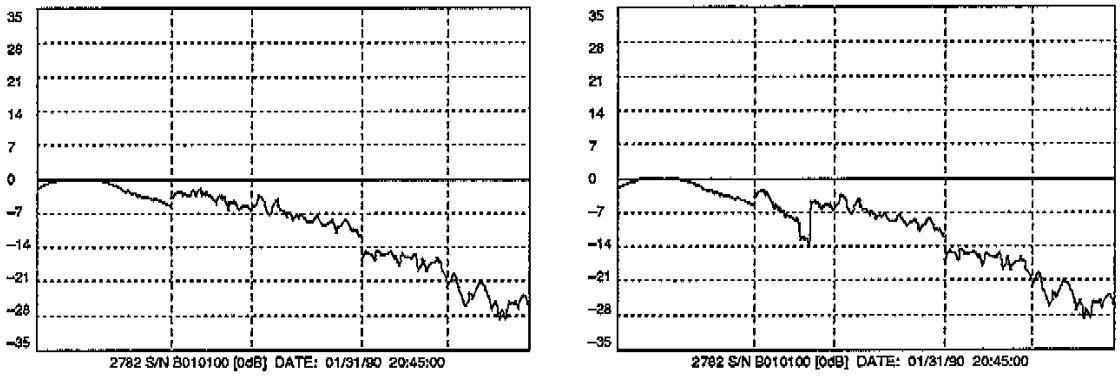
1. For example, to use the program PLOTF to plot the un-corrected flatness data for 2782 serial number B010100 on the personal computer monitor, use the following command:

```
plotf 2782 B010100 -u
```

2. As each graph is plotted, check that there are no abrupt changes in flatness (see plot below).

NOTE

An abrupt change indicates a problem with the instrument and must be resolved. See Figure 3-39 (B).



(A) Typical un-corrected flatness response. **(B) Flatness response indicating problem on band 2.**

Figure 3-39. Examples of PLOTF display.

D. TRANSFER FLATNESS DATA TO THE INSTRUMENT OPERATING SYSTEM (DOWNLOAD)

This step of the procedure transfers the flatness data stored in the file `\tekcats\flatness\278x\serial_number.unc*` and loads it into EEPROM in the 278X under test. The instrument uses this data to generate correction factors to assure flat response over its operating range.

To run the download program, type:

```
download dut_type serial_number
```

Where – dut_type is 2782 or 2784 and serial_number is the full serial number as was entered at the beginning of the test.

E. RUN THE FLATNESS VERIFICATION PROGRAM (278X)

This section measures the corrected display flatness, and frequency response, of the instrument.

Type the following on the personal computer to run 278X program.

```
278X<ENTER>
```

The 278X program is a menu driven program which requires entry of test conditions and test selections. Complete the following steps to run the flatness test (PERFORMANCE VERIFICATION) sequence:

1. Enter your name or your calibration labs name.
2. Verify the date and time.
3. Enter temperature and humidity information.
4. Select Device Under Test (DUT). Enter selection number to select the 278X model you are testing.
5. Select the PV sequence from the "Select Sequence" menu.
6. Enter the DUT serial number and press <ENTER>. You will be asked to verify the serial number.
7. Select the flatness test.
8. Select the First Attenuator to be Tested — 0 dB; then select the Last Attenuator to be Tested –50 dB; and select Frequency Band(s) to be Tested — Full Test. This test requires approximately two hours for the 2782 and 2½ hours for the 2784.
9. You will be prompted to make the connection shown in Figure 3-37. This test setup checks the low frequency range from 100 Hz to 10 MHz.

NOTE

When using the HP438A power meter, connect the low frequency sensor to Channel A, and the high frequency sensor to Channel B.

10. Next you are prompted to make the connections shown in Figure 3-38, but with the low frequency sensor. After the low frequency test is complete, you will be prompted to make the connections in Figure 3-38, with the HF sensor, to test the range above 10 MHz.

*In this example, `278x` is the instrument type being tested and `serial_number.unds` the serial number of that instrument with the extension .unc.

NOTE

*If you are using a single channel power meter, when you are prompted to connect another sensor, power down the power meter, switch sensors, power up the power meter and wait for self test to finish. **DO Not** change sensors at any other time in the test, the power on SRQ generated by the power meter will abort the test.*

F. EVALUATING THE FLATNESS VERIFICATION TEST

USING THE REPORT GENERATOR (RPT)

The RPT program generates a print out of the test results from data obtained by the 278X test. For example, to run RPT for a 2782 SN B010100 enter the following at the DOS prompt:

rpt 2782 B010100 PV<ENTER>

The full syntax for RPT are as follows: (Optional parameters are in [])

```
rpt [-pf][-t test] dut_type serial_number sequence
```

-p: or only those tests that passed – Optional
-f: or only those tests that failed – Optional
-t test: report only for the test named – Optional
for example –t flatness or –t residual

dut-type: 2782 or 2784 — Required

serial_number: DUT serial number for example B010100 — Required

sequence: PV or CAL — Required

Use PV for performance verification tests. Use CAL for the calibration test (flatness and preselector tracking).

Check that each band and attenuator passed for peak to peak flatness and that the band switching uncertainty specification passed for each attenuator and band.

PLOTTING THE FLATNESS TEST RESULTS (PLOTF).

If you wish to examine the plot of the flatness data, use the program PLOTF.

Syntax for plotf is as follows: (entries in braces are optional)

```
plot dut_type serial_number [-a atten][-b band][-u][-h]
```

dut-type: 2782 or 2784

serial_number: the full serial number as was entered during the flatness test.

`-a atten`: normally plotf will plot data from all attenuator settings tested. Specifying this option allows you to specify a plot of specified attenuator(s). The first digit of the attenuation should be entered here.

`-b band`: normally plotf will plot data for all frequency bands tested. Specifying this option allows you to specify a plot of specified band(s).

`-u`: specifying this option will cause plotf to plot results from the calibration (adjustment) flatness run for the DUT. This option is not used during performance verification

`-h`: this will cause plotf to automatically hard-copy each plot before plotting the next. If this option is not specified, plotf will pause after displaying each graph.

Examples using plotf:

To plot all flatness data for the performance verification test for 2784 serial number B010100:

```
plotf 2784 B010100
```

To plot only the data for bands 4 and 5, and attenuation setting of 0 and 10 dB for 2782 serial number B020300

```
plotf 2782 B020300 -a01 -b45
```

MAINTENANCE

This section describes preventive maintenance procedures, troubleshooting methods, corrective maintenance, and procedures for adjusting those assemblies that normally do not require routine calibration.

PREPARING THE INSTRUMENT FOR SERVICE

Refer to Figure 4-1 and prepare the instrument as follows:

1. Remove the power cord.
2. Install the protective front cover.
3. Set the instrument on a secure surface, face down.
4. Loosen the four slotted captive screws in the rear feet.
5. Remove the rear feet.
6. Remove the cabinet bezel.
7. Pull the cabinet up and off.
8. Place the instrument on the work bench, remove the front cover, and re-connect the power cord.

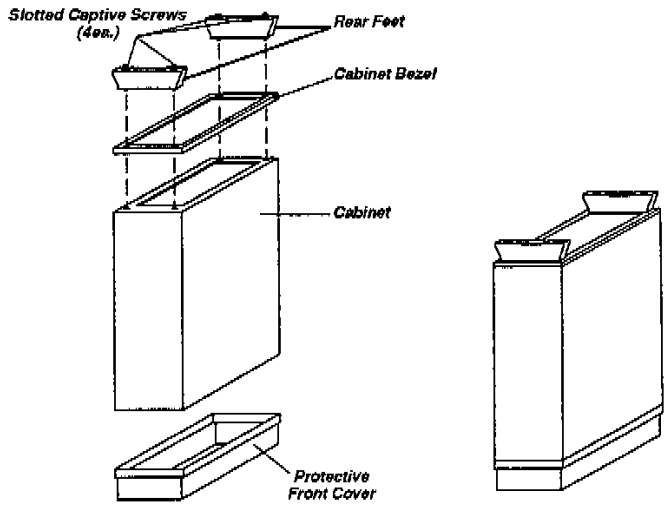


Figure 4-1. Removing the instrument from its cabinet.

STATIC-SENSITIVE COMPONENTS

This instrument contains electrical components that can be damaged by static discharge. See Table 4-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV can occur in unprotected environments.

CAUTION

Static discharge can damage any semiconductor component in this instrument. Surface mounted devices may be damaged by voltages as low as 30 Volts.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on metallized or conductive foam. Label packages that contains static-sensitive assemblies or components.
3. Wear a grounded wrist strap while handling these components. Static-sensitive assemblies or components should be handled and serviced only at static-free work stations by qualified service technicians.
4. Keep the workstation surface free of anything capable of generating or holding a static charge.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Do not handle components in areas that have a floor or work-surface covering that can generate a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only special anti-static suction type or wick type desoldering tools.

Table 4-1. Relative Susceptibility to Static Discharge Damage

Relative Semiconductor Classes	Susceptibility	Voltage Levels*
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1	100 to 500 V
ECL	2	200 to 500 V
Schottky signal diodes	3	250 V
Schottky TTL	4	500 V
High-frequency bipolar transistors	5	400 to 600 V
JFET devices	6	600 to 800 V
Linear microcircuits	7	400 to 1000 V (est)
Low-power Schottky TTL	8	900 V
TTL (Least Sensitive)	9	1200 V

*Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.

PREVENTATIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, performance check, and if needed, readjustment. Establish a preventive maintenance schedule that is based on the environment in which the instrument is operated and the amount of use. Under average conditions (laboratory situation) a preventive maintenance check should be performed every 2000 hours of instrument operation, with a cleaning and visual inspection every 500 hours.

CLEANING

Clean the instrument often enough to prevent dust or dirt from accumulating in or on it. Accumulation of dirt and grease acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high resistance electrical leakage paths between conductors or components in a humid environment.

EXTERIOR

Clean the dust from the outside of the instrument by wiping or brushing the surface with a soft cloth or small brush. The brush will remove dust from around the front-panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

The CRT faceplate is a glass cover over the liquid crystal color shutter. Use a soft, lint-free cloth dampened with a commercial glass cleaner. Do not use an alcohol-based cleaner, because the alcohol can dissolve the glue between the color shutter and the faceplate.

INTERIOR

Clean the interior by loosening accumulated dust with a dry soft brush, then remove the loosened dirt with low pressure air to blow the dust clear. (High velocity air can damage some components.) Hardened dirt or grease may be removed with a cotton tipped applicator dampened with a solution of mild detergent in water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used. If the circuit board assemblies need cleaning, remove the circuit board by referring to the instructions under ***Corrective Maintenance*** in this section.

After cleaning, allow the interior to thoroughly dry before applying power to the instrument.

CAUTION

Observe the following guidelines when cleaning to avoid instrument damage:

Do not allow water to get inside any enclosed assembly or components such as the hybrid assemblies, RF Attenuator assembly, potentiometers, etc. Instructions for removing these assemblies are provided in the ***Corrective Maintenance*** *part of this section.*

Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone or similar compounds because they may damage the plastic.

Do not clean the CRT faceplate with alcohol based cleaners.

MAINTENANCE FIXTURES AND TOOLS

Table 4-2 lists kits and fixtures that are used in servicing the spectrum analyzer.

Table 4-2. Service Kit and Tools.

Service Kit (See the Optional Accessories in the Replaceable Mechanical Parts List)

Processor Extender Board with RS-232 Cable and adapter
(See ***Appendix B - Using the Processor Extender***)
Main Card Cage Extender (Except A29 Ref Osc)
Card Cage Extender (Front Slot - A29 Ref Osc)
Extender Coaxial Cables (for Main Extender)
Extender Cables for Power Supply, VR, and Phase Lock modules
20 dB Coupler, 0.2 to 250 MHz

Tools

Large Slotted Screwdriver - for removing case
Posidrive #1 and #2 Screwdriver
Torx T-10 and T-15 Screwdrivers for removing most assemblies
(Minimum 2 inch long, narrow shaft T-10 driver required for A14 525 MHz IF and A16 VR)
Torque Wrench, 5/16-in open-end for SMA and K connectors
Torque Driver, adjustable, with tips for all screws.
IC Extraction Tool for 40-pin Firmware ROMs
Temperature-Controlled Soldering Iron or Hot Air Soldering Tool for removing batteries

VISUAL INSPECTION

After cleaning, carefully check the instrument for such defects as defective connections and damaged parts. If heat-damaged parts are discovered, try to determine the cause of overheating before the damaged part is replaced; otherwise, the damage may be repeated.

PERFORMANCE CHECK AND CORRECTIONS

The instrument performance should be checked after each 2000 hours of operation or every 12 months if the instrument is used intermittently. This schedule will ensure maximum performance and assist in locating defects that may not be apparent during regular operation. This schedule is also appropriate for replacing the NVRAM batteries, see that topic in the ***Corrective Maintenance*** part of this section. Instructions for conducting a performance check are provided in the *2780-Series Installation/Performance Verification Manual.*

Perform adjustments only as necessary to meet the Performance Requirements checked by the Performance Check procedure. Refer to ***Section 3 — Adjustment/Corrections*** in this manual.

Perform self-corrections as necessary when the operating environment changes, error messages are displayed or when directed by the performance check and adjustment procedures. Refer to the ***Correction Procedure*** later in the section, and ***Section 3 — Adjustments/Corrections*** for instructions for running the self-correction routines.

GENERAL DIAGNOSTICS

This section contains general information used to troubleshoot the instrument to a module level. It also provides procedures for implementing self-corrections that optimize the performance of many instrument parameters, and produce troubleshooting data.

RS-232 INTERFACE

The main troubleshooting tool is the RS-232 or keyboard interface. When the keyboard mode is active, the terminal will display the prompt:

```
Enter command:
```

Commands accepted by this prompt are in the form of a four letter command name followed by whatever arguments are appropriate to the particular command. Refer to ***Appendix B - Using the Processor Extender Board*** for details on setting up and using the RS-232 mode and for information on specific commands.

TRACE MODE

A trace mode is provided to print out information over the RS-232 interface that shows what is happening during corrections; the term trace does not refer to the trace on the instrument CRT. The trace mode *traces* the corrections and produces a report of measurements and calibration data taken during the self-correction cycle. This information is very useful for instrument level diagnostic.

The trace mode is enabled by setting switch S10 #3 on the A42 I/O Module to the CLOSED position (see ***Correction Procedure*** later in this section for details). A keyboard command is then used to invoke the desired trace. The trace mode for the vertical corrections is displayed by entering the `vrta 1` command, and disabled with the command `vtra 0`. Trace modes for reference level gain distribution and frequency corrections are also available. The command `rtra 1` (on) and `rtra 0` (off) control reference level gain distribution traces, and the command `ftra` followed by an argument invokes frequency correction traces. Refer to ***Frequency Control Diagnostics*** in this section for more information on the `ftra` arguments. Table 4-3 summarized the available trace modes.

A trace showing all frequency, vertical and reference level gain distribution activity appears on the terminal automatically when A42 S11 #3 is OPEN.

Table 4-3. Traces Modes available for diagnostics when A42 S11 #3 is CLOSED.

Parameter	Enable Trace	Disable Trace
Vertical Data	vtra 1	vtra 0
Frequency Control Data	ftra +(argument)	ftra –(argument)
Reference level Gain	rtra 1	rtra 0

ERROR LOG

An error log lists all errors recorded during instrument operation. To access the error log, press the UTIL key, select the Service Menu, and choose Error Msg Menu. Refer to ***Appendix B*** in the *2780-Series Operator's Manual* for additional information.

Errors are also listed on the terminal display as they occur when a trace mode is active. These messages are used to determine which step within a correction routine fails.

SIGNAL MEASUREMENTS

Signals use several different paths to travel between modules. These interconnect paths include the Mother board, a flat flex cable assembly located beneath the card cage, and 50 Ω coaxial cables. Mother board connections are generally limited to signals having frequencies below 250 kHz. The flat flex cable routes signals up to 25 MHz through Nanohex connectors. Coaxial cables with SMB connectors are typically used when frequencies exceed 25 MHz. Microwave frequencies such as the YTO signal travel through semi-rigid coax cables.

Most signals may be measured by placing modules on a Card Cage Extender (see ***Maintenance Fixtures and Tools*** in this section). Two rows of square pins labeled A1 – A22 and B1 – B25 provide access to signals that connect to the Mother board. SMB ports on the Card Extender also provide access to signals that travel through the flat flex cable assembly. Be sure to check the flat flex cable assembly for continuity when a missing signal is detected before replacing modules.

Microwave signals may be measured with a spectrum analyzer or power meter. We recommend using a spectrum analyzer, which provides a visual display that will detect subtle characteristics such as noise sidebands and frequency instability.

CORRECTION PROCEDURE

This section gives the procedure for performing corrections. The full correction is required whenever the A42 I/O Interface board is replaced, non-volatile memory is erased, or so many modules have been replaced that the existing correction data is totally invalid (see Table 3-2 in ***Section 3—Adjustments/Corrections*** for module replacement requirements). Final correction should only be performed on a fully warmed-up instrument which has the cabinet installed (at least 1 1/2 hour warm up) due to the temperature-sensitive nature of some circuitry. Partial corrections are used to optimize instrument performance during normal use, and for obtaining trace information during troubleshooting procedures.

CORRECTION DATA

Three sets of correction data reside within the instrument: default, store, and current.

- Default data resides in ROM and is used primarily as a starting point for the corrections.
- Store data resides in non-volatile memory. The correction routines acquire current data to be saved in non-volatile memory. Once saved, the data is referred to as store data.
- Current data is placed in RAM for use during normal instrument operation. Current data is read from the store data at instrument power-up and modified by the corrections routines.

STORING/RECALLING CORRECTION DATA

After a correction routine is completed, the resulting current data may be stored as follows:

- Service mode must be invoked (S10 #3 on the A41 Main Processor CLOSED) to enable the Store data menu selections.
- Follow the path UTIL, Misc Corr Menu, Correction (such as Peak Dtect Menu), Store Data for miscellaneous corrections.
- Follow the path UTIL, Vert Corr Menu, Correction (such as Total Vert Menu) Store Data for vertical corrections.
- Follow the path UTIL, Freq Corr Menu, Store Data for frequency self-corrections.

Each menu also contains Recall From Store and Recall Default selections. Recall From Store implements the last stored values, and Recall Default implements default data from ROM that is used as the beginning point for most corrections.

Several keyboard commands are provided to store and recall the correction data sets (Table 4-4). These commands are used for manipulating the correction data for troubleshooting and adjustment purposes.

Table 4-4. Store and recall commands.

Command	Action
rcgn *n*	copies default (generic) data set n into current data.
rcdf *n*	copies stored data set n into current data.
stcu *n*	stores current data set n into stored data. The value of n is from the Data ID Table 4-5

When storing default data, the previously acquired store data is replaced with the default data. The routine for which default data was stored must be performed again to obtain new store data.

ABORTING CORRECTIONS

The proper way to abort corrections during adjustment or troubleshooting procedures is to turn the instrument power off and back on. The correction can be re-run after power-up. *Correction routines should not be aborted by pressing the ESC key.* This can have undesirable side effects. Due to the length of some correction routines, which require several minutes to complete, we suggest aborting corrections as soon as the desired trace has been completed when using trace mode for fault isolation.

DEPENDENCIES

In general, the correction dependencies follow the sequence given in section *3 — Adjustments/Corrections.* That is, if a given correction needs to be performed, each of the following corrections in the sequence must also be performed. Two exceptions to this are the VR Resonator Correction and Peak Detector Correction, which may be performed at any time without affecting other corrections. The Peak Detector routine optimizes the trace width and may improve the results of subsequent routines which use the markers to measure amplitude.

Table 3-2 in ***Section 3 — Adjustment/Corrections.*** shows which corrections to preform when modules are replaced. If a module is repaired or replaced, all the corresponding adjustments and corrections must be performed.

FREQUENCY SELF-CORRECTION

A frequency self-correction is preformed as follows:

1. Press the UTIL key.
2. Select Freq Corr Menu.
3. Choose Run Freq Corr Cycle.
4. Following completion of the correction sequence, select Store Data to save this information in non-volatile memory.

NOTE

Do not store the resulting data if the self-correction is run for troubleshooting purposes, or if the instrument has not been running for 1 ½ hours..

FULL VERTICAL CORRECTIONS

A full vertical correction is performed as follows:

NOTE

Steps 1 through 6 may be omitted if the Attenuator Correction is not performed. The Attenuator Correction typically does not need to be invoked unless the A10 RF Attenuator has been replaced, or calibration data stored in the non-volatile memory is lost (the A42 I/O Interface board is replaced).

1. Install the Processor Extender board into the instrument (see ***Appendix B***).

2. Set the A42 I/O Interface switch S10 #3 to OPEN.

   This switch controls trace mode. When set to OPEN, all traces are turned off until invoked by commands discussed later in this procedure. When set to the CLOSED position, all trace information is automatically sent out the RS-232 interface to the terminal and printer, if connected.

3. Set the A41 Main Processor switch S11 #3 CLOSED. S11 is located directly above the crystal.

   This switch controls service mode, which allows individual access to the keyboard mode and all correction routines. It also enables the Save Results menu selection for storing new data.

4. Power up the instrument. S10 and S11 are only read during the power-up sequence.

5. Enable the vertical trace mode. Press UTIL, select the Service Menu, select Enter Keyboard Mode and enter the following command:

   ```
   vtra 1
   ```

   After entering vtra 1, the terminal responds:

   ```
   VCalTraceEnable = 1
   ```

   which is the code for the vertical trace. Trace reports will appear on the terminal when vertical correction routines are performed.

6. Enter the command:

   ```
   fpan
   ```

   to resume front panel control of the instrument.

7. Enter the UTIL menu and run the correction routine in the following order. When a routine completes without issuing errors, immediately save the calibration data with the Save Results menu key. If a correction routine fails, consult the following section for troubleshooting information.

   Peak Detector Correction
   Lin Baseline Adjustment (See ***Section 3 — Adjustments/Corrections***)
   VR Resonator Correction
   Display Law Correction
   Attenuator Correction
   Sweep Offset Adjustment (See ***Section 3 — Adjustments/Corrections***)

   NOTE

   At this point, remove the Processor Extender board, install the instrument in its cabinet, and allow 1 ½ hours to warm up before continuing.

   Reference Oscillator Frequency Check (***See Section 3 — Adjustments/Corrections***)
   Frequency Correction
   Peak Detector Correction (2nd time)
   VR Resonator Correction (2nd time)
   Display Law Correction (2nd time)
   Log Correction
   Display Law Correction (3rd time)
   Gain Step Correction
   VR Resonator Correction (3rd time)
   Res BW Correction
   External Mixer Correction

8. Check the instrument performance after the vertical corrections are complete.

PARTIAL VERTICAL CORRECTION

This section gives the sequence for performing a partial vertical correction. Use this sequence when an instrument's performance must be optimized during normal use, such as when the operating temperature changes more than 5°C. This procedure may also be used following repairs which do not require new attenuator or log correction data. New attenuator or log correction data are needed when the following modules are replaced: A10 RF Attenuator, A12 MTX, A13 Microwave IF, A16 VR, A29 Reference Oscillator, and A18 Log Processor.

Individual corrections may be run on cold instruments for troubleshooting purposes and to verify functionality, but the resulting data will have reduced accuracy. Final correction should only be performed on instruments which have had a minimum warm up period of 1 ½ hours.

NOTE

The instrument must be in its cabinet during this sequence unless the corrections are run for diagnostic purposes. Do not save data obtained during troubleshooting procedures.

1. Connect the front panel REF SIGNAL OUT to the RF INPUT.
2. Press the UTIL key.
3. Select the Vert Corr Menu.
4. Select Display Law Menu, VR Reson Menu, Gain step Menu or Res BW Menu.
5. Select Run Corr Cycle.
6. Press Store Data to save the correction data in non-volatile memory.

If a correction routine fails, consult the following section for troubleshooting information.

NOTE

An additional Vert Corr Menu selection called Total Vert Menu is available when operating in service mode (A41 Main Processor switch S11 #3 COSED). This selection runs all parameters listed in Step 4 in sequence.

Correction data is listed out using the **dcal** keyboard command:

EXAMINING CORRECTION DATA

VERTICAL CORRECTIONS

Correction data for vertical corrections may be listed out using the dcal keyboard commands follows:

dcal ***type id***

The two arguments indicate which set or subset of the data is to be listed, and whether generic, default, or current correction data is desired. The arguments are listed in Table 4-5 and 4-6.

Table 4-5. Data Type arguments for the dcal command.

Data Type	Data Type Listed
0	Generic data
1	Default or Stored data
2	Current data

Table 4-6. Data ID arguments for the dcal command.

Data ID	Data Set Listed
0	All correction data
1	VR Resonator Data
2	Display Law Data
3	Gain Step Data
4	ResBW Data
5	Attenuator Data
6	Peak Detector Data
7	Log Curve Correction Data

For example, **dcal 2 4** lists the current resolution bandwidth data, and **dcal 0 1** lists the generic VR resonator data. The first line of all data listings indicates both data type and which set of data is being listed. For example, the first line of the listing generated by **dcal 2 4** is:

```
CurrentCalData-> resbw_data:
```

while the one for **dcal 0 1** is:

```
GenericCalData-> vrres_data:
```

The term generic refers to the default data. Refer to the ***Vertical Diagnostics*** section for detailed explantations of the listings.

FREQUENCY CORRECTIONS

If the entire frequency self-correction cycle is allowed to run, the frequency self-calibration data may be examined by entering the command:

```
tabl
```

Refer to the ***Frequency Control Diagnostics*** section for detailed explanations of the listings.

The `scal` command produces a list of all sweep-related data, which is part of the frequency self-calibration data listed by the `tabl` command.

RF PATH DIAGNOSTICS

This section provides information for isolating amplitude related faults within the RF signal path. Typically symptoms of failures within this path are low signal amplitude on the screen and a high internal noise floor resulting in reduced sensitivity. Due to RF path switching, failures may only appear at some FREQUENCY settings. These symptoms may be used to isolate the faulty module. Following is a summary of the most common signal switching paths:

- All signals pass through the A10 RF Attenuator module.
- Signals between 0 and 6.5 GHz (frequency band 1) pass through the A12A4 Low Pass Termination and A12A5 Low Pass Mixer modules.
- Signals above 6.5 GHz (frequency bands 2, 3, 4, and 5) pass through a Preselector Filter and High Pass Mixer, which are part of the A12 MTX module.
- Signals between 0 to 6.5 GHz and 21 GHz to 28 GHz (frequency bands 1 and 4), produce a 10.025 GHz IF from the A12 MTX module.
- Signals between 6.5 GHz and 21 GHz, and 28 GHz to 33 GHz (frequency bands 2, 3, and 5), produce a 3.525 GHz IF from the A12 MTX module.
- The A13 Microwave IF contains a 9.5 GHz 2nd LO for converting the 10.025 GHz first IF to 525 MHz (frequency bands 1 and 4).
- The A13 Microwave IF contains a 3.0 GHz 2nd LO for converting the 3.525 GHz IF to 525 MHz (frequency bands 2, 3, and 5).

Refer to ***Section 5 — Theory of Operation*** for more information on signal path switching.

Table 4-7 provides a listing of the key RF signal ports, and Figure 4-2 shows each port location on the RF deck portion of the chassis. For each port, the expected signal amplitude and frequency characteristics are provided for frequency bands 1 and 2. Refer to the instrument level block diagram fold-out at the rear of this manual for signal levels for frequency bands 3, 4, and 5.

CAUTION

Use extreme caution when disconnecting the semi-rigid coaxial cables to prevent damage to the cable. Calibrated torque wrenches should be used to install K connectors (5 inch/lbs.) and SMA connectors (8 inch/lbs.).

SIGNAL INJECTION

CW signals may be injected into the RF path at specified frequencies and amplitudes to produce full-screen vertical deflection on the spectrum analyzer display. Under these conditions, the spectrum analyzer display is a flat, horizontal line. This method of fault isolation measures the signal gain of each module to determine which module has insufficient gain.

To perform signal injection:

1. Turn on the instrument and select 100 MHz FREQUENCY, Zero SPAN, and –30 dBm REF level. Leave remaining settings at their power-up condition.
2. Change the FREQUENCY as required if the fault only occurs within specified frequency ranges.
3. Apply signals to RF ports at the frequency and amplitude specified in Table 4-7.
4. Proper gain is indicated when the trace (flat, horizontal line) moves to the top graticule line.

RF SIGNAL MEASUREMENTS

The –20 dBm, REF SIGNAL OUT provides an input signal to trace gain characteristics through the RF path. A test spectrum analyzer is used to measure the resulting signals at specified points along the RF path.

To measure signals along the RF path:

1. Turn on the instrument and select 100 MHz FREQUENCY, Zero SPAN, and –20 dBm REF level. Leave remaining settings at their power-up condition.
2. Connect the REF SIGNAL OUT to the RF INPUT.
3. If the fault only occurs at frequencies other than 100 MHz, replace the REF SIGNAL OUT with an external, –20 dBm signal at the appropriate frequency.

NOTE

Refer to the instrument-level block diagram fold-out at the rear of this manual for signal levels for frequency bands 3, 4, and 5.

Table 4-7. RF path signal characteristics.

RF Port	0 to 6.5 GHz (Band 1)	6.5 to 12.7 GHz (Band 2)
A10 RF Attenuator Output	–30 to –31 dBm	–32 to –31.5 dBm
A11 YTO Output	+13 to +17 dBm 10 to 16.5 GHz for Band 1*	+13 to +17 dBm 10 to 16.2 GHz for Band 2*
A12 MTX IF Output	–41 to –51 dBm (–43 dBm nominal) 10.025 GHz	–48 to –60 dBm (–50 dBm nominal) 3.525 GHz
A13 Microwave IF Output	–35 to –52 dBm (–39 dBm nominal) 525 MHz	–32 to –51 dBm (–39 dBm nominal) 525 MHz
A14 525 MHz IF 3rd LO Input	–6 to –9 dBm, 500 MHz	+6 to +9 dBm, 500 MHz
A16 VR 25 MHz IF Input	–35 to –52 dBm (–39 dBm nominal) 25 MHz	–32 to –52 dBm (–29 dBm nominal) 25 MHz
A16 VR 25 MHz IF Output	+16 dBm 25 MHz (3 and 10 MHz RBW) +16 dBm, 4 MHz (3 Hz to 1 MHz RBW)	+16, 25 MHz (3 and 20 MHz RBW) +16 dBm, 4 MHz (3 Hz to 1 MHz RBW)

*Measure at front panel connector (+15 dBm minimum) or input to A12 MTX module.

CAUTION

Do not bend semi-rigid coaxial cables when disconnecting them for maintenance purposes. Some cables contain in-line filters which may be destroyed when cables are bent. In-line filters are identified by a black, plastic sleeve at the middle of the cable.

Mechanical damage to any semi-rigid cable may degrade frequency response performance. Replace all damaged cables.

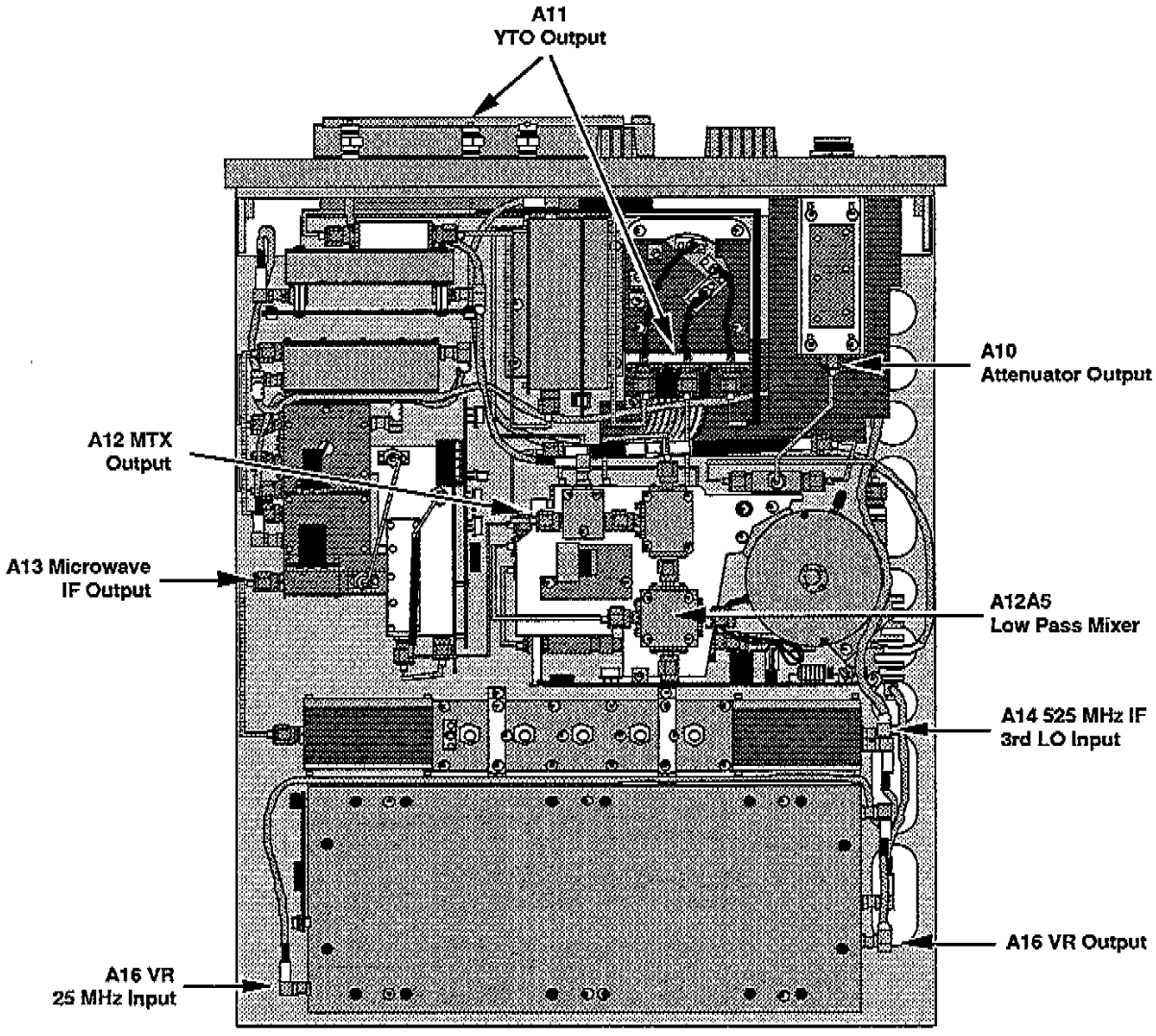


Figure 4-2. RF ports and signal injection and RF path measurements.

VERTICAL DIAGNOSTICS

This section contains detailed information that describes the individual vertical correction routines. Following the introductory information, each routine is described. This consists a summary of the actual routine, a description of the trace, a list of possible error messages.

SETTING UP THE VERTICAL TRACE

Follow these steps to trace individual vertical correction routines:

1. Install the Extender board and enter keyboard mode (see ***Appendix B*** for instructions).

   - Set S10 #3 on the A42 I/O Interface board to OPEN (disables automatic trace on all data).
   - Set S11 #3 on the A41 Main Processor to CLOSED (enable service mode).
   - Power-up the instrument.

2. Enter the command:

   ```
   vtra 1
   ```

3. Enter the command:

   ```
   fpan
   ```

4. Press the ESC key to return to the UTIL menu.

5. Run a vertical correction routine (select Misc Corr Menu, Peak Dtect Menu, and Run Corr Cycle for the Peak Detector correction).

The terminal will display trace data immediately as the routine begins. The following sections explain this trace data for each vertical correction routine. They also provide descriptions of error messages and troubleshooting procedures for use when a correction sequence fails.

PEAK DETECTOR CORRECTION

The A20 Video Processor module has four peak detectors that operate as sample and hold detectors. During waveform acquisition, the Video Processor alternates between the different peak detectors. Specific detectors are used for each acquisition mode. This correction has five steps which adjust the peak detectors so that each circuit produces the same digitized value when equal input signals are applied. The Peak Detector correction takes about 1 minute to complete. Tests are performed in this sequence:

- Peak Detector Display Setup
- MAX Peak Detector Correction
- MIN Peak Detector Correction
- SAMPLE Peak Detector Correction
- Gain and Offset Correction

NOTE

Repeat the Peak Detector correction at least twice before attempting to repair a fault. This routine may fail occasionally even though the instrument has no defective components.

LISTING OUT PEAK DETECTOR CORRECTION DATA

After the Peak Detector correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
dcal 2 6
```

The vertical trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command  :  vtra 1
Enter command  :  dcal  2  6
CurrentCalData->pkdet_data:
    gain  =  0x26
    offset  =  0xbe
    min_offset  =  0x8d
    max_offset  =  0x47
    min_smpl_offs  =  0x80
    max_smpl_offs  =  0x6a
```

`Gain` is the peak gain, `offset` is the peak offset, `min_offset` is the MIN offset, `max_offset` is the MAX offset, `min_smpl_offs` is not used and `max_smpl_offs` is the MAX offset used in SAMPLE mode. Following is a detailed explanation of this data.

PEAK DETECTOR DISPLAY SETUP

During this step the 4 MHz reference oscillator in the VR as the signal source The vertical height of the on screen display, a straight horizontal line, is adjusted using the log offset DAC on the A18 Log Processor module. The peak detector correction begins by adjusting the log offset until the signal is at mid-screen. The trace for the first part of the routine looks like this:

```
PeakDetCorr:
    setup_pkdet_corr: state=1
        Offset_To_Lvl: lvl=950 su  VertScale=10  dB/div
            LogOffset= 0.00  dB  ht= 837 su  err=-113 lsb
            LogOffset=11.30  dB  ht= 951 su  err=   1 lsb
        Offset_To_Lvl: lvl=500 su  VertScale=1  dB/div
            LogOffset=11.30  dB  ht=1023 su  err= 523 lsb
            LogOffset= 6.07  dB  ht=1023 su  err= 523 lsb
            LogOffset= 0.84  dB  ht=1023 su  err= 523 lsb
            LogOffset=-4.39  dB  ht= 624 su  err= 124 lsb
            LogOffset=-5.63  dB  ht= 497 su  err=  -3 lsb
```

The first two lines of the trace indicate that the instrument is being set up for peak detector correction. These lines never change. Offset_To_Lvl identifies a firmware routine used to adjust log offset until the desired vertical position, `950 su` (Screen Units) in this case as indicated by the display `lvl=950 su`. Screen units refer to the 1000 point vertical axis of the screen, where 0 su is at the baseline, `1000 su` is the reference level, and a maximum digitized value of `1023 su` is possible. `VertScale=10 dB/div` indicates the vertical scale factor in use. The following lines of the trace are the results of each iteration of the adjustment, showing the log offset in (`LogOffset= 0.00 dB`), the signal height in screen units (`ht= 837 su`), and the error with respect to the desired level (`err=-113 lsb`); the error is in screen units and is equal to the desired level minus the current level.

Toward the middle of this trace, the vertical scale is set to 1 dB/div. This is done because the Peak Detector correction is the first of the correction routines to be performed, so no assumptions can be made concerning the correction of the display law. Therefore, this two part signal adjustment is used to adjust the signal level quickly and reliability regardless of the instrument calibration.

PEAK DETECTOR DISPLAY SETUP ERROR MESSAGES

The following error can occur during this part of the correction:

Peak Detectors Not Corrected. This message is generated at the end of the Peak Detector correction if anything fails. Examine the preceding errors in the error log, (also found in the trace information,) to determine the cause of the failure.

Signal Offset Timed Out. The signal level could not be adjusted by the log offset DAC. This error is also generated when the reference signal is missing. Check for the 4 MHz reference oscillator before continuing as follows:

1. In keyboard mode, enter the command:

```
vpth 1000
```

2. Use a spectrum analyzer to measure the 4 MHz signal at J162 on the A16 VR module. Signal parameters are 4 MHz ±10%, and 16 dBm ±0.5 dB for a full-screen display (–20 dBm REF Signal Out applied when REF Level is –20 dBm).

The error message is often due to an unstable or missing signal. If the signal is missing, the instrument attempts to adjust its noise floor causing the noise level to change for each new sweep. The A20 Video Processor may cause this error message, producing an extremely noisy on-screen signal that may not be adjusted. Check the operation of the Video Processor for other symptoms, and replace if necessary.

Another possible cause for this error message is the log offset DAC on the A18 Log Processor module. To exercise the log offset DAC:

3. Select a 1 MHz resolution Bandwidth.

4. Inject a signal (4 MHz, +16 dBm for full-screen display) into the Log Processor module at P181.

5. Exercise the DAC with one of the following keyboard commands:

```
offs 1ff   (loads hex value 1ff into log offset DAC, other values from
    000 to fff                may be used to check range)

lofs 5.0   (loads DAC with value for 5.0  dB of log offset relative to the
    hinge               point)

ofsq       (prints out current value of log offset DAC)

swep       (Forces a sweep to update the display)
```

The **swep** command forces a sweep so on-screen signals change vertical position as the DAC is exercised. Replace the A18 Log Processor module if the DAC fails to respond.

MAX PEAK DETECTOR CORRECTION

After the signal level is adjusted, the two MAX peak detectors are corrected. To accomplish this, MAX acquisition mode (which alternates between the two max peak detectors) and a 10 ms sweep speed are selected. The minimum and maximum signal amplitudes for signals near center screen are measured; their differences represents the MAX peak detector mismatch. Next the MAX peak detector offset DAC is adjusted until this mismatch is minimized. On the instrument display, the waveform resembles a square wave that changes to a horizontal line with small noise spikes on it. The amplitude of the noise represents the difference between the two MAX peak detectors. A clean line with no noise is produced when the correction is complete.

A two-pass algorithm is used to determine the best DAC number. On the first pass the most significant DAC control bits are exercised to determine which setting produces the lowest noise amplitude. The second pass fine tunes the DAC using its least significant control bits until the lowest minimum value is found. The trace looks like this:

```
cal max peak detectors:
    pass 1:
          DAC=0x00  noise_ht=16 lsb
          DAC=0x10  noise_ht=12 lsb
          DAC=0x20  noise_ht= 9 lsb
          DAC=0x30  noise_ht= 5 lsb
          DAC=0x40  noise_ht= 2 lsb
          DAC=0x50  noise_ht= 3 lsb
          DAC=0x60  noise_ht= 6 lsb
          DAC=0x70  noise_ht=10 lsb
    pass 2:
          min_DAC=0x30  max_DAC=0x50
          DAC=0x30  noise_ht= 6 lsb
          DAC=0x31  noise_ht= 5 lsb
          DAC=0x3d  noise_ht= 3 lsb
          DAC=0x3e  noise_ht= 2 lsb
          DAC=0x3f  noise_ht= 2 lsb
          DAC=0x40  noise_ht= 2 lsb
          DAC=0x41  noise_ht= 2 lsb
          DAC=0x42  noise_ht= 2 lsb
          DAC=0x43  noise_ht= 1 lsb
          DAC=0x44  noise_ht= 1 lsb
          DAC=0x45  noise_ht= 1 lsb
          DAC=0x46  noise_ht= 2 lsb
          DAC=0x47  noise_ht= 2 lsb
          DAC=0x48  noise_ht= 1 lsb
          DAC=0x49  noise_ht= 2 lsb
          DAC=0x4a  noise_ht= 1 lsb
          DAC=0x4b  noise_ht= 2 lsb
          DAC=0x4c  noise_ht= 2 lsb
          DAC=0x4d  noise_ht= 3 lsb
          DAC=0x4e  noise_ht= 2 lsb
          DAC=0x4f  noise_ht= 3 lsb
          DAC=0x50  noise_ht= 3 lsb
    final DAC=0x43  min_ht=1 lsb
```

The trace indicates the DAC value, in this case the MAX offset DAC, and the corresponding **noise_ht** (peak detector mismatch) in LSB. The **0x** prefix on the DAC values indicates that the value is expressed in hexadecimal form. When the second pass is finished, the minimum noise height (**min_ht=1 lsb**) and the corresponding DAC value are listed. The minimum noise height must be ≤3 LSB, or the error message **Peak Detector Max Not Corrected** is generated. The correction proceeds to the MIN peak detector correction despite this error.

MAX PEAK DETECTOR CORRECTION ERROR MESSAGES

The following error can occur during this part of the correction:

Peak Detector Max Not Corrected. The MAX peak detector could not be matched to within 3 LSB of each other. The problem is often the results of faulty peak detector circuitry on the A20 Video Processor module. Symptoms include degraded or unusable MAX and MIN/MAX acquisition modes.

1. Set the MAX peak offset DAC and its corresponding correction data, by enabling keyboard mode and entering these commands:

   pkmx 2e (Loads DAC with Hex value 2e)

   swep (Forces a sweep to update the display)

   The instrument trace should become noisy and move vertically on the screen.

2. Observe the results and repeat the commands to exercise for DAC values between 00 and ff (Hex). If the DAC does not respond properly, replace the A20 Video Processor module.

MIN PEAK DETECTOR CORRECTION

This is identical to the max peak detector correction, except that MIN acquisition mode and the min offset DAC are used for the correction. The trace looks like this:

```
cal min peak detectors:
      pass 1:
            DAC=0x00  noise_ht=31 lsb
            ...
            DAC=0xb0  noise_ht= 8 lsb
      pass 2:
            min_DAC=0x70  max_DAC=0x90
            DAC=0x70  noise_ht= 6 lsb
            ...
            DAC=0x89  noise_ht= 1 lsb
            ...
            DAC=0x90  noise_ht= 2 lsb
      final DAC=0x89  min_ht=1 lsb
```

MIN PEAK DETECTOR CORRECTION ERROR MESSAGES

The following error can occur during this part of the correction:

Peak Detector Min Not Corrected — The MIN peak detectors could not be matched to within 3 LSB of each other. The problem is typically due to a faulty peak detector circuitry on the A20 Video Processor module. Symptoms will include degraded or unusable MIN and MIN/MAX acquisition modes.

1. Set the MIN peak offset DAC and its corresponding correction data, by enabling keyboard mode and entering these command:

   ```
   pkmn 2e       (loads DAC with hex value 2e)
   swep          (Forces a sweep to update the display)
   ```

2. Observe the results, and repeat the commands to exercise the DAC over the range of 00 to ff. (hex) If the DAC does not respond properly, replace the A20 Video Processor.

SAMPLE PEAK DETECTOR CORRECTION

The MAX peak detectors are used in SAMPLE acquisition mode, but with a different correction DAC value is required. This routine is identical to the MAX peak detector correction, except that SAMPLE mode is used. The trace looks like this:

```
cal sample max peak detectors:
      pass 1:
            DAC=0x00  noise_ht=25 lsb
            ...
            DAC=0x90  noise_ht=10 lsb
      pass 2:
            min_DAC=0x50  max_DAC=0x70
            DAC=0x50  noise_ht= 7 lsb
            ...
            DAC=0x65  noise_ht= 1 lsb
            ...
            DAC=0x70  noise_ht= 3 lsb
      final DAC=0x65  min_ht=1 lsb
```

SAMPLE PEAK DETECTOR CORRECTION ERROR MESSAGES

The following error can occur during this part of the correction:

Peak Detector Sample Not Corrected — The MAX peak detectors could not be matched to within 3 lsb of each other. The problem is typically due to faulty peak detector circuitry on the A20 Video Processor module. Symptoms will include degraded or unusual SAMPLE acquisition mode.

1. Set the MAX peak offset DAC and its corresponding correction data, by enabling keyboard mode and entering these commands:

   ```
   pkms 2e      (Loads DAC - sample mode - with hex value 2e)
   swep         (Forces a sweep to update he display)
   ```

   The instrument trace should become noisy and move vertically on the screen.

2. Observe the results, and repeat the commands to exercise the DAC values between 00 to ff (Hex). If the DAC does not respond properly, replace the A20 Video Processor module.

GAIN AND OFFSET CORRECTIONS

This correction adjusts the peak gain and peak offset DACs to match the MIN peak detectors. The routine alternates between offset and gain until both are corrected.

Initially the peak offset DAC is adjusted at center of screen. The signal is moved to this height and swept twice, once in MIN and once in MAX acquisition mode. The amplitude difference between the two sweeps represents the mismatch to be corrected. After the peak offset has been corrected, the signal is moved to full screen where the same correction is performed for the peak gain. The routine repeats these adjustments due to interaction until both parameters are corrected. The trace looks like this:

```
cal_gain_offs:
cal offset:
Offset_To_Lvl: lvl=500 su  VertScale=1 dB/div
                    LogOffset=-5.63 dB  ht= 495 su  err=  -5 lsb
                    LogOffset=-5.58 dB  ht= 499 su  err=  -1 lsb
               DAC=0x80  err=4 lsb
               DAC=0x7d  err=3 lsb
               DAC=0x7b  err=0 lsb
         cal gain:
               Offset_To_Lvl: lvl=990 su  VertScale=1 dB/div
                    LogOffset=-5.58 dB  ht= 499 su  err=-491 lsb
                    LogOffset=-0.67 dB  ht= 982 su  err=  -8 lsb
                    LogOffset=-0.59 dB  ht= 989 su  err=  -1 lsb
               DAC=0x80  err=22 lsb
               DAC=0x73  err=20 lsb
               DAC=0x67  err=9 lsb
               DAC=0x62  err=4 lsb
               DAC=0x5f  err=2 lsb
               DAC=0x5e  err=1 lsb
               DAC=0x5d  err=1 lsb
               DAC=0x5c  err=0 lsb
         cal offset:
               ...
         cal gain:
               ...
         cal offset:
               ...
```

```
            cal gain:
                  Offset_To_Lvl: lvl=990 su  VertScale=1 dB/div
                        LogOffset=-5.61 dB  ht= 501 su  err=-489 lsb
                        LogOffset=-0.72 dB  ht= 999 su  err=   9 lsb
                        LogOffset=-0.81 dB  ht= 991 su  err=   1 lsb
                  DAC=0x27  err=1 lsb
                  DAC=0x26  err=0 lsb
            cal offset:
                  Offset_To_Lvl: lvl=500 su  VertScale=1 dB/div
                        LogOffset=-0.81 dB  ht= 992 su  err= 492 lsb
                        LogOffset=-5.73 dB  ht= 488 su  err= -12 lsb
                        LogOffset=-5.61 dB  ht= 501 su  err=   1 lsb
                  DAC=0xc1  err=0 lsb
      setup_pkdet_corr: state=0
```

The **Offset_To_Lvl** lines indicate signal level on the screen. The **cal_offset** line identifies the peak offset correction, and the following lines provide peak offset DAC value (**dac=0x80**) and the related difference between the MIN and MAX acquisition sweeps (**err=4 lsb**). Error is the height of the MAX acquisition minus the height of the MIN acquisition. The correction repeats 20 times, or until the error reaches 0 LSB. A **Peak Detector Min-Max Timed Out** error is generated if the error exceeds 3 LSB after 20 tries causing the correction to terminate.

Next he signal is set to top of screen and the correction repeated for the peak gain DAC. The routine will alternate between gain and offset up to 20 times, or until the measured error for either gain or offset is zero. A **Peak Detector Min-Max Not Corrected** error is generated if both gain and offset error exceed 3 LSB after 20 tries.

GAIN AND OFFSET CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Peak Detector Min-Max Not Corrected. The overall peak gain and offset correction has timed out. Replace the A20 Video Processor Module.

Peak Detector Min-Max Timed Out. An individual peak gain or peak offset correction has failed. Replace the A20 Video Processor Module.

Refer to the trace to determine whether the gain or offset DAC has failed. The peak gain and peak offset DACs, and their corresponding correction data, may be manipulated with the following keyboard commands:

```
pkof 5d     (set the peak offset to hex value 5d, range is 00 to ff)
pkgn 2a     (set the peak gain to hex value 2a)
swep        (Forces a sweep to update the display)
```

VR RESONATOR TRACKING CORRECTION

The 4 MHz IF resolution bandwidth filters (i.e. - resolution bandwidths of 1 MHz or less) are composed of a series of six individual filters or resonators. Alignment of these resonators is critical for dynamic range, filter shape , amplitude accuracy, and center frequency accuracy. The 4 MHz IF frequency is achieved by mixing the 25 MHz IF coming into the VR with a DAC-tuned 29 MHz LO. Each resonator is also individually controlled by a tune DAC. The VR Resonator correction sets the 29 MHz LO to 29 MHz, sets the center frequency of each resonator to 4 MHz, and aligns the tracking of all six resonators. This routine takes about 30 seconds to complete. Tests are performed in this sequence:

- Setting 29 MHz LO
- Setting Up Crystal Resonator Ringdown
- Crystal Resonator Tracking
- Resonator Correction In Narrow Bandwidths (Automatic)

LISTING OUT VR RESONATOR TRACKING CORRECTION DATA

After the VR Resonator tracking correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
dcal 2 1
```

The vertical trace must be enabled in order to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 1
CurrentCalData-> vrres_data:
    lo29 = 0x4c7
    lo25 = 0x30b
    td_tbl =
          0xaa   0x56
          0xa3   0x64
          0xaf   0x65
          0xa1   0x50
          0xa2   0x62
          0xab   0x5c
```

`lo29` is the 29 MHz LO tune DAC setting, `lo25` is the 29 MHz LO tune DAC value used during the crystal resonator tracking , and `td_tbl` is the tune DAC values for each of the six resonators, listed in order from 0 to 5. The left column is the crystal mode, the right column is the LC mode. Following is a detailed explanation of this data.

SETTING 29 MHZ LO

The 29 MHz tune DAC is adjusted until the frequency is within 0.75 Hz of 29 MHz. The 11-bit DAC has a nominal resolution of 0.75 Hz/LSB. The corresponding trace looks like this:

```
VRResonatorCorr:
    set_vcor_stgs:
    set_DACs: td_freq=4000000.00  Hz  lo29_freq=29000000.00  Hz
          setting lo29
          set_lo29_to_freq: tune_freq=29000000.00  Hz
                DAC=0x400  freq=29000149.36  Hz  err=149.36  Hz
                DAC=0x2d6  freq=29000012.77  Hz  err=12.77  Hz
                DAC=0x2bd  freq=29000001.24  Hz  err=1.24  Hz
                DAC=0x2bb  freq=29000000.23  Hz  err=0.23  Hz
          lo29_actual=29000000.23  Hz  td_freq=4000000.23  Hz
```

The first four lines of the trace identify which routine is running. `set_lo29_to_freq` indicates that the 29 MHz LO is to be set to a specific `tune_freq`, in this case `29000000.00 Hz`. The following lines reflect activity of the 29 MHz LO correction. The `dac` column indicates the tune DAC value expressed in hexadecimal. `freq` shows the measured frequency of the LO, and `err` is the frequency difference from 29 MHz. After the 29 MHz LO has been corrected, the remaining error is incorporated into the tune DAC frequency `td_freq` which is the frequency that the resonators will be set to. The correction times out if the 29 MHz LO is not set in 10 tries.

SETTING 29 MHZ LO ERROR MESSAGES

The following errors may occur during this part of the correction:

29 MHz LO Set To Limit Value. The 29 MHz LO DAC has insufficient range to tune the LO frequency. This error can also be generated if there are problems counting the LO (see below). To count the LO frequency:

1. Select the 3 MHz resolution bandwidth (to select the 25 MHz log amp).

2. Enable keyboard mode and enter this path:

```
vpth 901   (Routes 29 MHz LO signal to output of VR)
ifen 1     (Enables count path through log amp)
log4 1     (Selects 25  MHz log amp)
lo29 4096  (Counts 29 MHz LO using period counter)
```

A typical count response would be:

```
29 MHz LO = 29000011.51
```

3. Check the resulting value against a precision frequency counter connected to J162 of the A16 VR module. The counter should agree with the frequency displayed on the terminal.

   - A discrepancy here may indicate a miss adjusted A29 Reference Oscillator module.
   - Replace the A16 VR module if the counted frequency matches the terminals's display.

4. The LO 29 DAC may be set using the `sllo xx` command where `xx` is the DAC value (Hex). Enter the extreme DAC values and count the 29 MHz LO frequency to check frequency range of the circuit:

```
sllo 0
lo29 4096 (result should be below 29 MHz)
sllo 7ff
lo29 4096 (result should be above 29 MHz)
```

29 MHz LO Does Not Converge. The 29 MHz LO tune DAC should be linear in terms of Hz per LSB. This error is generated if the 29 MHz LO correction does not converge. The cause may be the tune DAC or a faulty count path. Refer to the **29 MHz LO Set To Limit Value** error message for troubleshooting procedures.

29 MHz LO Count Terminated
29 MHz LO Count Data Unknown
29 MHz LO Not Set. These three errors can be generated if the 29 MHz LO cannot be counted due to a missing 29 MHz LO signal, or a problem in the count path. Fault symptoms are characterized by large frequency errors (≥100 kHz) in the `err` column of the trace. A weak signal results in smaller errors while missing signals produces larger ones. . The period counter requires that the signal be at least 20 dB above the noise floor for accurate counts; signals near the threshold will produce small frequency count errors.

To check the 29 MHz LO:

1. Set up the instrument for 1 MHz ResBW (turns on the 4 MHz path), and connect a spectrum analyzer to J168 LO Out on the A16 VR module.

1. Check for 29 MHz, 0 dBm, LO signal.

   - Replace the A16 VR module if the signal is weak or missing.

3. Check the count path sensitivity:

   - Connect an external 29 MHz signal to J181 on the A18 Log Processor module.

   - Set up the count path by enabling keyboard mode and entering these commands:

     ```
     vpth 901, ifen 1, log4 1, lo29 4096
     ```

   - Adjust the 29 MHz signal amplitude and repeat the l929 4996 command to determine the minimum signal amplitude required for repeatable counts. Replace the A16 VR module if this amplitude is greater than the 29 MHz output from J168 on the A16 VR module.

4. To isolate 29 MHz LO count problems caused by either the A18 Log Processor or A28 Period Counter:

   - Use an oscilloscope to measure the TTL level IFPC line at A18 Pin B9. IFPC is a square wave with a frequency equal to the 29 MHz divided by 1024 (28.3 kHz).

   - If IFPC is missing or noisy, replace the A18 Log Processor module. Replace the A28 Period Counter module if IFPC has the correct waveform.

SETTING UP CRYSTAL RESOLUTION RINGDOWN

Crystal resonator center frequency is determined by ringing down each resonator and counting its resonant frequency. To accomplish a ring down, each resonator is charged with energy from a 25 MHz ringdown oscillator located in the VR module. This 25 MHz signal is mixed with the 29 MHz LO to produce 4 MHz charging signal. The 29 MHz LO frequency is adjusted when the 25 MHz ring down oscillator is running to produce a precise 4 MHz IF (4 MHz ±5 Hz) for maximum efficiency. The range of the first crystal tune DAC is also checked to ensure functionality. The trace looks like this:

```
set_lo25:
    DAC=0x400  freq=3999926.76  Hz  err=-73.24  Hz
    DAC=0x492  freq=3999989.01  Hz  err=-10.99  Hz
    DAC=0x4a7  freq=3999997.25  Hz  err=-2.75  Hz
setup_rdown_vr:
    chk_td_slope: xlc_mode=0
          max_freq=4000041.50  Hz
          min_freq=3999952.70  Hz
          DAC range=88.81  Hz
```

To begin the trace **`set_lo25 dac`** is the 29 MHz LO tune DAC value used during ringdown, **`freq`** is the resulting 4 MHz IF, and **`err`** is the frequency difference between the IF and 4 MHz.

`setup_rdown_vr` indicates that the VR is being set for resonator ringdown. The **`chk_td_slope: xlc_mode=0`** line identifies the DAC range check for the first crystal resonator, and is followed by the measured minimum, maximum, and tune range of the resonator. The correction fails after 10 tries, causing the crystal resonators to charge to lower levels. This condition produces weaker signal, which may cause the crystal resonator tracking to fail.

SETTING UP CRYSTAL RESONATOR RINGDOWN CORRECTION ERROR MESSAGES

The following error can occur during this part of the correction:

29 MHz LO Out Of Range. The 29 MHz LO DAC has insufficient range to mix the 25 MHz ringdown oscillator to 4 MHz ±5 Hz. This error can also be generated if the 4 MHz IF produced during the ring down cannot be counted. To check the frequency range of the 4 MHz IF produced during the ring down process:

1. Select the 1 MHz resolution bandwidth (to select the 4 MHz log amp path).

2. Enable keyboard mode, and enter the following commands:

```
vpth 532      (Turns on 25 MHz signal and mix down to 4 MHz)
ifen 1        (Enables count path through log amp)
log4 0        (Selects 4 MHz log amp path)
eyef 4096     (Counts 4 MHz IF using period counter)
```

3. Compare the measured value of the 4 MHz frequency measured at J162 of the A16 VR module using a precise frequency counter.

   - The counted value should be similar to the value on the terminal.

   - If the counted values do not match, check the period counter path as describe for error messages in the Setting 29 MHz LO step located earlier in this section.

4. The LO 29 DAC can be exercised with the command **sllo xx**, where **xx** is the DAC value (Hex). Check the frequency range by entering the extreme DAC values:

```
sllo 0
eyef 4096     (result should be below 4 MHz)
sllo 7ff
eyef 4096     (result should be above 4 MHz)
```

- If this check fails, readjust the 25 MHz ringdown oscillator frequency or replace the A16 VR module.

25 MHz LO Count
4 MHz IF Count Bad Data
4 MHz Terminated
29 MHz LO Timed Out
25 MHz Ringdown Oscillator Not Set
29 MHz LO Out of Range. These six errors can all be generated if the 4 MHz IF produced by the 25 MHz ringdown oscillator cannot be counted due to a missing 25 MHz signal, or a problem in the count path. A missing 29 MHz LO will also generate these messages, but this fault is normally detected earlier in the correction. Large frequency errors (>100 kHz) in the **err** column of the trace indicate a weak or missing signal. Weak signals produce small errors while missing signals produce larger ones. The period counter requires that signals be at least 20 dB above the noise floor for accurate counts.

1. Check for a weak or missing 25 MHz ring down oscillator using the procedure from the 29 MHz LO Out Of Range error message.

   •Replace the A16 VR module if the signal is faulty.

2. To check the count path sensitivity:

   - Connect a 4 MHz, 0 dBm external signal to J181 on the A18 Log Processor module.
   - Select a 1 MHz resolution bandwidth.
   - Enable keyboard mode and enter the following commands:

```
vpth 532      (route LO 25 signal to output of VR)
ifen 1        (enable count path through log amp)
log4 0        (select 4  MHz log amp)
eyef 4096     (count 4  MHz IF using period counter)
```

   - Adjust the signal generator amplitude and repeat the **eyef 4096** command to determine the minimum signal amplitude required for repeatable counts.

   •Replace the A16 VR module if this amplitude exceeds the 4 MHz signal from the VR module.

3. Refer to the troubleshooting procedure for the **29 MHz LO Not Set** error message in the Setting 29 MHz LO step of this correction to isolate faults along the signal path (A18 Log Processor and A28 Period Counter modules).

CRYSTAL RESONATOR TRACKING

This step adjusts each crystal resonator to within 0.7 Hz of 4 MHz; the tune DACs have a resolution of 0.5 Hz/lsb. The frequency of each resonators is measured by charging it with an IF derived by mixing the 29 MHz LO and 25 MHz ringdown oscillator. The 4 MHz IF is then counted after the ringdown oscillator is turned off. When a signal source is removed from a charged resonator, the decaying output signal is at the natural frequency of the resonator. Thus the tune DAC is set to adjust the frequency produced by the decaying resonator to exactly 4 MHz. The resonator to be counted is set to MIN bandwidth crystal mode while the others are set to LC mode to ensure that each resonator is counted individually. The LC resonators decay much faster than the crystal resonator stage, so they discharge before the period counter is turned on. The correction times out if any resonator cannot set in 10 tries. The trace looks like this:

```
setting crystal tune_DAC 0:
set_xtal_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3999982.91  Hz  err=-17.32  Hz
    DAC=0x6f  freq=3999998.47  Hz  err=-1.76  Hz
    DAC=0x73  freq=4000000.31  Hz  err=0.07  Hz
setting crystal tune_DAC 1:
set_xtal_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3999982.61  Hz  err=-17.63  Hz
    DAC=0x6f  freq=3999998.78  Hz  err=-1.45  Hz
    DAC=0x72  freq=4000000.00  Hz  err=-0.23  Hz
setting crystal tune_DAC 2:
    ...
setting crystal tune_DAC 3:
    ...
setting crystal tune_DAC 4:
    ...
setting crystal tune_DAC 5:
set_xtal_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3999984.44  Hz  err=-15.80  Hz
    DAC=0x6b  freq=3999998.17  Hz  err=-2.06  Hz
    DAC=0x6f  freq=3999999.39  Hz  err=-0.84  Hz
    DAC=0x71  freq=4000000.31  Hz  err=0.07  Hz
```

The **dac** value is the crystal resonator tune DAC value, **freq** is the counted resonator frequency, and **err** equals **freq** minus the target frequency **tune_freq**. Failure to track the crystal resonators results in reduced dynamic range and/or loss of amplitude in the narrowest crystal bandwidths (3 Hz and 10 Hz).

CRYSTAL RESONATOR TRACKING CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Crystal Resonator Set To Limit Value. There is insufficient DAC range for one or more resonators. The **dac** number in the trace will indicate a value of **0x00** or **0xff** (from the **setting crystal tune_dac x** part of the trace), the minimum and maximum extremes to which each failed resonator is set. This error may also be generated if the ringdown signal cannot be counted. To check the ring down frequency:

1. Enable keyboard mode and enter the following commands:

```
vset          (Setup instrument for counting ringdown)
minb xx             (Set resonator to min bw mode; see below)
xlcm xx             (Set all other resonators to LC mode)
xfrq          (Count ringdown frequency)
```

   Arguments for **minb** and **xlcm** commands select between crystal (Min BW) and LC modes for the individual resonators labelled 0 through 5. Table 4-8 provides a summary of these arguments.

2. Repeat the **xfrq** command several times and look for counted results that are within 0.35 Hz of each other. Variations greater than 1 or 2 Hz indicate counting problems (see following error messages).

3. If the frequency counts are consistent, exercise the DAC by entering several DAC values:

```
stnd n xx     (Sets resonator n from Table 4-8 to Hex value XX)
xfrq          (Counts ring down frequency)
```

   - A DAC value of **00** produces a frequency below 4 MHz, **ff** produces a frequency above 4 MHz and **80** sets the frequency approximately midway between the two.

   - Refer to *Section 3 — Adjustment/Corrections* for an adjustment procedure if the tune DAC range does not center around 4 MHz.

   - Replace the A16 VR module if the tune DAC fails to respond to the **xfrq** command.

Table 4-7. Resonator Command Arguments.

Resonator	minb	xlcm
0 (1st)	01	3e
1	02	3d
2	04	3b
3	08	37
4	10	2f
5 (6th)	20	1f

Ringdown Count Terminated
4 MHz Terminated
Crystal Resonator Timed Out
Crystal Resonator Set To Limit Value. These four errors may indicate problems counting the ringdown frequency of the resonators, typically producing large (>100 kHz) count errors.

1. Refer to the **Crystal Resonator Set To Limit Value** troubleshooting procedure for a method of checking the ring down frequency of each resonator.

2. Count variations greater than 1 or 2 Hz indicate counting problems. The count system is checked out as follows:

   - Check the period counter by enabling keyboard command and entering these commands:

     ```
     vpth 532      (Turn on ringdown oscillator)
     eyef 256      (Count 4 MHz IF)
     ```

   - Repeat the **eyef 256** command several times and check for counted results consistent to within 0.5 Hz.
   - If counts are inconsistent, check the A16 VR module output at J162 with a spectrum analyzer for a stable 4 MHz, –20 dBm (minimum) signal. Replace the A16 VR module if the signal is unstable or missing.

3. Check the count path sensitivity if the 4 MHz signal amplitude is less than –20 dBm.

   - Connect a stable, external 4 MHz, 0 dBm signal to input connector P181 on the A18 Log Processor at P181.
   - Repeat the **eyef 256** command. Inconsistent counts indicate problems in the A18 Log Processor or A28 Period Counter modules.
   - If counts are consistent reduce the 4 MHz signal level in 10 dB steps, repeating the **eyef 256** at each step, and note the signal amplitude at which the count becomes inconsistent. Good counts should occur at levels as low as –72 dBm.
   - Count failure at amplitudes greater than –72 dBm indicate a faulty A18 Log Processor or A28 Period Counter module.
   - If the counting system functions properly, the A16 VR module is defective. Replace the A16 VR module, or proceed to determine if the 25 MHz ringdown oscillator requires adjustment.

4. To check the ringdown oscillator calibration:

   - Connect a spectrum analyzer to J162 at the A16 VR module output.
   - Enable keyboard mode and enter these commands to exercise the ringdown oscillator:

     ```
     vpth 532      (Turn on ringdown oscillator)
     vpth 522      (Turn off ringdown oscillator)
     ```

   - When the oscillator is enabled, a –20 dBm (or greater) 4 MHz signal should be present. This signal should disappear when the oscillator is turned off. Low signal amplitude is often due to failure of the ringdown oscillator frequency to align with the resonator, attenuating the signal amplitude by the resonator skirts. This fault may also be due to a defective 4 MHz oscillator.

5. To check the 4 MHz reference oscillator:

   - Connect a spectrum analyzer in count mode to J162 on the A16 VR module.
   - Use the **vpth 532** command to turn on the 4 MHz oscillator. The measured 4 Mhz IF should be 4 MHz ±5 Hz.
   - Connect the VR output to the A18 Log Processor.
   - Count the 4 MHz IF by entering the **eyef 4096** command. The resulting 4 MHz count should match that measured by the analyzer. If the results do not match, the instrument's 100 MHz internal reference must be readjusted.

6. If the IF is not 4 MHz ±5 Hz, the 25 MHz oscillator frequency must be readjusted. Refer to **Section 3 — Adjustment/Corrections** for an adjustment procedure.

7. If the 25 MHz ringdown oscillator frequency and corresponding 4 MHz IF amplitude are correct, try looking for anomalies in the ringdown signal.

   - Connect the output of the VR module at J162 to a spectrum analyzer set to zero span mode.
   - Use the xfrq keyboard command to initiate a ringdown.
   - Operate the test spectrum analyzer in single sweep mode to capture the ringdown curve; the resulting trace starts above –20 dBm and slopes linearly into the noise. Replace the A16 VR module if this test fails.

LC RESONATOR TRACKING CORRECTION

Each LC resonator is adjusted to within 500 Hz of 4 MHz; the tune DACs have a nominal resolution of 315 Hz/lsb. Resonator frequency is determined by setting each resonator in MIN bandwidth mode, one at a time, and executing a sweep. A marker locates the signal peak and measures the resonator frequency. To begin the measurement sequence, reference level and VR gain are adjusted to position the waveform in the upper half of the screen. Next, the range of the first LC tune DAC is checked. The correction fails if a resonator can not be set in 10 tries. The trace looks like this:

```
set_lc_lvl:
    Set_Filter_Rlv:
          Setting 10 dB/div level to 950 su
          pk_y=1004 su  err=  54 lsb
          pk_y= 948 su  err=  -2 lsb
    Set_Filter_Gain:
          Setting 1dB/div level to 800 su
          StepGain=29 dB  pk_y= 412 su  err=-388 lsb
          StepGain=33 dB  pk_y= 854 su  err=  54 lsb
    chk_td_slope: xlc_mode=1
          max_freq=4033400.00  Hz
          min_freq=3962000.00  Hz
          DAC range=71400.00  Hz
setting LC tune_DAC 0:
set_lc_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3989000.00  Hz  err=-11000.23  Hz
    DAC=0x68  freq=4000200.00  Hz  err=199.77  Hz
setting LC tune_DAC 1:
set_lc_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3990400.00  Hz  err=-9600.23  Hz
    DAC=0x64  freq=3999800.00  Hz  err=-200.23  Hz
setting LC tune_DAC 2:
    ...
setting LC tune_DAC 3:
    ...
setting LC tune_DAC 4:
    ...
setting LC tune_DAC 5:
set_lc_to_freq: tune_freq=4000000.23  Hz
    DAC=0x46  freq=3991600.00  Hz  err=-8400.23  Hz
    DAC=0x60  freq=3999400.00  Hz  err=-600.23  Hz
    DAC=0x61  freq=3999800.00  Hz  err=-200.23  Hz
```

The `dac freq`, and `err` columns contain the same information as was described during the ***Crystal Resonator Tracking*** trace. `chk_td_slope: xlc_mode=1` part of the trace identifies the DAC range check for the first LC resonator; `min_freq`, `max_freq`, and `dac range` are the minimum frequency, maximum frequency, and range of the tune DAC. Failure of this step results in reduced dynamic range and amplitude in the narrowest LC bandwidth (10 kHz and 30 kHz).

LC RESONATOR TRACKING CORRECTION MESSAGES

The following errors can occur during this part of the correction:

VR Resonator Internal Self-Corr Failed. There is insufficient DAC range; the DAC number in the trace will be set to minimum (0x00) or maximum (0xff). This error may also be generated by a missing or noisy signal (see LC Resonator Tracking Timed Out message).

1. Note the number of each failing resonator, then select these instrument front panel settings:

FREQUENCY	100 MHz
REF LEVEL	-50 dBm
SPAN	100 kHz
RES BW	10 kHz

   Internal calibrator ON (from INPUT menu)

2. Enable keyboard mode and enter the following command:

   ```
   minb xx      (Set resonator to min bw mode, select xx from table 4-8.)
   ```

3. Return to front panel mode (enter fpan) and adjust the reference level for an on-screen waveform in 1 dB/Div.

4. Enable keyboard mode and exercise the DAC by entering several DAC values and forcing a sweep with the following commands:

   ```
   stnd n xx    (Set tune DAC n to hex value xx, see Table 4-8)
   swep         (Force a sweep to update the display)
   ```

   - Enter DAC numbers of 00 (signal mover right, ff (signal moves left), and 80 (signal centered midway between 00 and ff positions.
   - Refer to Section 3 — Adjustments/Corrections for an adjustment procedure if the signal does not cross center of screen.
   - Replace the A16 VR module if the signal does not move or has a very limited range.

LC Resonator Tracking Timed Out
LC Resonator Set To Limit. These two errors may be due to a missing or unstable signal. If so, the instrument display will contain the noise floor instead of a signal peak.

1. Check for the signal by selecting the following front panel settings:

FREQUENCY	100 MHz
REF LEVEL	-50 dBm
SPAN	100 kHz
RES BW	10 kHz

   Internal calibrator ON (from INPUT menu)

2. The calibrator signal should be clearly visible and centered on the display. If not, check the Calibrator signal path or Frequency Control hardware.

Signal Level Timed Out. The signal level for LC resonator tracking could not be set using instrument reference level hardware. This failure usually indicates hardware problems in the A16 VR or A18 Log Processor module, although fault correction data for display law, gain step or log curve correction may also cause this error. Perform these corrections before replacing the A16 or A18 modules.

Signal Gain Timed Out. The signal level for LC resonator tracking could not be set using VR gain. Failure usually indicates a defective 25 MHz gain stage in the A16 VR module, although the error may also result from incorrect log curve data. This correction should always work with default log data. Check the current log data by reca lling the default data and running the correction again.

VR Gain Truncated. The signal level for LC resonator tracking could not be set using VR gain, indicating the VR does not have enough gain to achieve the desired signal level. The error results from too much or too little gain. Check signal levels from the A16 Calibrator, and along the RF path between the RF Input connector to the A18 Log Processor to isolate the fault.

VR Resonator Internal Self-Corr Failed. This message is generated at the end of the correction if anything went wrong. Examine the preceding errors in the error log, or trace information to determine the specific cause of failure.

RESONATOR CORRECTION IN NARROW BANDWIDTHS (AUTOMATIC)

A subset of the resonator tracking routine is performed automatically at 15 minute intervals, when operating in resolution bandwidths of 30 Hz or narrower, to maintain amplitude accuracy. This message appears on the instrument display: VR RESONATOR CORR: SETTING LO 29 when the routine begins. This routine compensates for normal circuit changes which occur as the temperature within the instrument changes. The automatic correction fails during the first hour of operation as the instrument warms up as the 29 MHz LO and 25 MHz IF frequencies drift.

The automatic resonator tracking routine corrects the 29 MHz LO and the crystal resonators using the same process as the full resonator tracking correction. It takes about 10 seconds to complete. The user may disable the automatic correction, but amplitude accuracy in bandwidth of 30 Hz or less cannot be guaranteed.

The automatic correction is only performed when the resolution bandwidth is 30 Hz or less and the last resonator tracking was performed more than 15 minutes ago, or a narrow resolution bandwidth is selected for the first time and the resonators have not been tracked recently. Under the latter condition, a correction begins as soon as the current sweep is completed.

DISPLAY LAW CORRECTION

The display law correction adjusts for hinge point and vertical scale calibration, primarily affecting the A18 Log Processor module. The hinge point is the top-of-screen reference for the vertical scaling in log mode, where signals position (top-of-screen) do not change with dB/div scaling. The hinge point correction determines DAC values needed to set the hinge point for each log scale setting. Vertical scale corrections produce DAC values used to calibrate the dB/div scaling in log mode, and correct for center-of-screen in linear (–6 dBc) and power (–3 dBc) modes. This routine also determines the log offset DAC resolution.

The REF SIGNAL OUT is used as a signal source, and must be connected to the RF INPUT connector. The correction takes about 90 seconds to complete. Test are performed in this sequence:

- Log Hinge Point Correction
- 10 dB/div Correction (4 MHz IF)
- Log Offset DAC Correction (4 MHz IF)
- 1 dB/div Correction (4 MHz IF)
- 10 dB/div Correction (25 MHz IF)
- Log Offset DAC Correction (25 MHz IF)
- 1 dB/div Correction (25 MHz IF)
- Internal Calibrator Correction
- Linear Scale Correction
- Power Scale Correction

LISTING OUT DISPLAY LAW CORRECTION DATA

After the Display Law correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
dcal 2 2
```

Vertical trace must be entered to view the data. The terminal will display the following:

```
Enter command  :  vtra  1
Enter command  :  dcal 2 2
CurrentCalData-> displ_data:
    zero_log_offs [0] = 0x1c1, zero_log_offs [1] = 0x1c1
    hg_pos [0] = 0x6c2, hg_pos [1] = 0x68b
    gm_log_slope [0] = 3094.4, gm_log_icept [0] = -132.4
    gm_log_slope [0] = 3026.7, gm_log_icept [0] = -132.7
    gm_lin [0] [0] = 172, gm_lin [0] [1] = 473
    gm_lin [1] [0] = 165, gm_lin [1] [1] = 459
    log_offs res [0] = 0.0397, log_offs_res[1] = 0.0388
```

zero_logoffs [0] and **zero_log_offs [1]** are the zero hinge power log offset DAC values for the 4 MHz and 25 MHz IFs, respectively. These two values are always the same, ranging from **0x000** to **0xfff**. **hg_posn [0]** and **hg_posn [1]** are the hinge position DAC values established for log and linear/power modes, respectively; with DAC values ranging from **0x000** to **0xfff**.

The log scale correction assumes a linear gilbert DAC, which controls the dB/div log scales. Thus the DAC values established for 10 dB/div and 1 dB/div DAC are used to compute slope and intercept values. The resulting **gm_log_slope[]** and **gm_log_incept[]** values are used to compute gilbert DAC values for the remaining dB/div settings.

The `gm_lin [] []` values are gilbert DAC values for linear and power modes. The left index indicates the IF path (0 for 4 MHz, 1 for 25 MHz); the right index selects between linear (`0`) or power (`1`) modes. `log_offset_res [0]` and `log_offset_res [1]` are the log offset DAC resolution values for the 4 MHz and 25 MHz IFs, respectively, expressed in dB/LSB. The internal –50 dBm calibrator signal level, `clalb_lvl` is expressed in dBm.

Several keyboard commands are available to modify the display law correction data. The following example illustrates how these commands are used (see ***Appendix B – Using the Processor Extender*** for descriptions of individual commands):

```
Enter command : hofs 222
Enter command : logh 500
Enter command : linh 600
Enter command : gmlg 1 3333.3 -222.2
Enter command : ofsr 0 0.555
Enter command : clvl -55.5
Enter command : dcal 2 2
CurrentCalData-> displ_data:
    zero_log_offs [0] = 0x222, zero_offs [1] = 0x222
    hg_posn [0] = 0x500, hg_pos [1] = 0x600
    gm_log_slope [0] = 3.94.4, gm_log_icept [0] = -132.4
    gm_log_slope [1] = 3333.3, gm_log_icept [1] = -111.1
    gm_lin [0] [0] = 172, gm_lin [0] [1] = 473
    gm_lin [1] [0] = 165, gm_lin [1] [1] = 459
    log_offs res [0] = 0.0555, log_offs_res [1] = 0.0388
    calib_lvl = -55.50
```

LOG HINGE POINT CORRECTION

The log scale correction begins by setting the hinge point. A 4 MHz reference oscillator in the A16 VR module is turned on to supply a known calibration signal. Next the log offset DAC is adjusted for equal on-screen levels when changing between 1 dB/div and 10 dB/div. For this measurement the hinge position DAC is set to `0x000` to ensure an on-screen display. Once this hinge point is established (by the log offset DAC), the hinge position DAC is adjusted for top-of-screen display. The trace looks like this:

```
DisplayLawCorr:
Calibrating 4 MHz path
     LogScaleCorr:
          hg_pwr_corr:
               log offs DAC=0x1c0  y10=773 su  y1=799 su  err=-26 lsb
               log offs DAC=0x1b9  y10=771 su  y1=773 su  err= -2 lsb
               zero_log_offs[0]=0x1b9
               zero_log_offs[1]=0x1b9
          hg_posn_log_corr:
               hg posn DAC=0x800  ht= 974 su  err=-26 lsb
               hg posn DAC=0x904  ht= 999 su  err= -1 lsb
```

The first three lines of the trace identify that the log scale correction step of the display law correction is being performed using the 4 MHz log path. `hg_pwr_corr` identifies the hinge power correction, which determines the zero offset value for the hinge point. It includes the log offset DAC value (`log ofs dac`), 10 dB/div signal height (`y10`), 1 dB/div signal height (`y1`), and amplitude difference between y1 and y10 (`err`), which cannot exceed 2 LSB. The zero offset DAC value, which is the final `log offs dac` value, is then listed for both 4 MHz (`zero_log_offs [0]`) and 25 MHz (`zero_log_offs [1]`) IFs.

The `hg_posn_log_corr` correction adjusts the hinge position DAC to set the hinge point signal from `hg_pwr_corr` to top of screen. For each iteration, the trace includes the hinge position DAC value (`hg pos dac`), signal height (`ht`), and the computed difference between the signal height and top-of-screen (`err`). This correction terminates when the error is 2 LSB or less.

LOG HINGE POINT CORRECTION ERROR MESSAGES

The following errors may occur during this part of the correction:

Hinge Point Data Unknown. This error occurs when large signal level errors are detected, such as off-screen signals when in 10 dB/div mode. A faulty A18 Log Processor or A16 VR module is likely. To isolate the defective module:

1. Turn on the 4 MHz reference oscillator in the VR by enabling keyboard mode and entering this command:

   ```
   vpth 1000    (Turns on 4 MHz VR reference oscillator)
   ```

2. Connect a spectrum analyzer to P162 on the A16 VR module.

   - This signal should measure 4 MHz ±10% at +16 dBm ±0.5 dB.
   - Replace the A16 VR module if the signal does not meet these specifications. Replace the A18 Log Processor module if the 4 MHz signal is correct.

The **Hinge Point Data Unknown** message may also be generated if the acquisition system fails to acquire a sweep indicating a problem in the A20 Video Processor or A24 Digital Storage modules. This failure mode is quite rare, since acquisition problems are usually noticed during normal operation.

Log Hinge Position Truncated. The hinge position DAC on the A18 Log Processor does not have enough range to move the hinge point to top of screen.

Check the 4 MHz reference oscillator signal as described for the **Hinge Point Data Unknown** error message, and replace the A18 Log Processor or A16 VR module.

Hinge Power Timed Out
Hinge Position Timed Out. These two errors indicate that the hinge point could not be set within two SU (screen units). A noisy signal during this step may be the cause.

1. Run the Peak Detector correction to minimize the noise.

2. Check the A18 Log Processor and A20 Video Processor modules for noise sources such as oscillations.

   - Replace the A18 Log Processor module if the signal is clean but the error message persists.
   - The **Hinge Power Timed Out** message indicates a log offset DAC failure, and **Hinge Position Timed Out** indicates a hinge position DAC failure.

10 DB/DIV CORRECTION (4 MHZ IF)

This step establishes gilbert DAC values that produce accurate 10 dB/div and 1 dB/div vertical scale factors. These values are used to compute gilbert DAC values for remaining vertical scale factors.

The instrument's RF attenuators serves as the calibration standard for this test. These attenuators are very stable with time and temperature, and their values are characterized during instrument calibration. The 40 dB excursion between the 10 dB and 50 dB attenuator settings is used to avoid inaccuracies caused by excessive return loss. A defective RF attenuator will produce faulty calibration data, so the attenuators are tested for functionality before the correction begins. The routine also confirms that the REF SIGNAL OUT is connected to the instrument input connector.

After the RF attenuator and signal source are validated, the test sets up for the 10 dB/div correction. A 10 dB RF attenuator step pads the input, log offset is set to 0.0 dB and VR gain is adjusted for a top-of-screen display. Now the RF attenuator is switched between the 10 and 50 dB settings while the gilbert DAC is adjusted for exactly 10 dB/div. The trace looks like this:

```
setup_att_lscl:
                    setting up 4 MHz path
                    Chk_Signal:
                          signal off: pk_y=182 su
                          signal on : pk_y=1023 su
                    Set_Filter_Lvl: lvl=1000  VertScale=10 dB/div
                          su_per_lsb=0.50  max_err=3 su
                          c_gain=0x22  f_gain=0x83  err= 100 su
                          c_gain=0x24  f_gain=0x80  err= -10 su
                          c_gain=0x24  f_gain=0x95  err=  -2 su
                          6-dB bw=104 Hz  bw_err=4.0%
                    Chk_Atten:
                          atten= 0  ht=998 su
                          atten=10 dB  ht=906 su  delta=0.92 div
                          atten=20 dB  ht=809 su  delta=0.97 div
                          atten=30 dB  ht=714 su  delta=0.95 div
                          atten=40 dB  ht=617 su  delta=0.97 div
                          atten=50 dB  ht=522 su  delta=0.95 div
                          atten=60 dB  ht=427 su  delta=0.95 div
                          atten=70 dB  ht=335 su  delta=0.92 div
adjusting signal level...
                    Gain_To_Lvl: lvl=1000  VertScale=10 dB/div
                          su_per_lsb=0.50  max_err=3 su
                          c_gain=0x24  f_gain=0x95  err= -95 su
                          c_gain=0x22  f_gain=0x8b  err=  -6 su
                          c_gain=0x22  f_gain=0x8b  err=  -6 su
                          c_gain=0x22  f_gain=0x97  err=  -2 su
                    Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
                          su_per_lsb=5.00  max_err=4 su
                          c_gain=0x22  f_gain=0x97  err=  20 su
                          c_gain=0x22  f_gain=0x8b  err= -25 su
                          c_gain=0x22  f_gain=0x8b  err= -25 su
                          c_gain=0x22  f_gain=0x90  err=  -6 su
                          c_gain=0x22  f_gain=0x91  err=  -2 su
               cal_log_scale: 10.00 dB/div:
                    gilbert DAC=0x08c  10.478 dB/div  err=  4.78%
                    gilbert DAC=0x098  10.030 dB/div  err=  0.30%
```

The first two lines indicate that the log scale correction of the 4 MHz IF path is being set. **Chk_Signal** is a routine that checks for a 100 MHz signal, measured in su, as the REF SIGNAL OUT is turned off (**pk_y=182 su**) and on (**pk_y=1023**). The signal height must be at least 400 su (4 divisions) above the noise floor when the reference is turned on, and no more than 6 dB above the noise floor when it is off.

After verifying the signal source, its level is adjusted to top-of-screen using VR gain (**Set_Filter_Lvl:**) when the log offset set to 0 dB. Next signal bandwidth is checked to further ensure signal validity. The check fails if the 6 dB bandwidth is not within ±50% of the resolution bandwidth (**6-dB bw=104 Hz bw_err=4.0%**). At this point the RF attenuator steps are checked (**Chk_Atten:**). at each setting to ensure that the signal amplitude decreases between 0.5 and 2.0 divisions for each 10 dB of attenuation. **atten** is attenuator setting, **ht** is the signal height, and **delta** is the amount of signal decrease since the previous attenuator step.

Gain_To_Lvl is a routine used to set the signal level using VR gain. **lvl** is the desired signal level, **VertScale** is the vertical scale, **su_per_lsb** is the fine gain DAC resolution, and **max_err** is the target error for the routine. The VR gain DAC values are printed out for each iteration of **Gain_To_Lvl**. **f_gain** is the fine gain DAC value, **c_gain** is the coarse gain DAC value, and **err** is the corresponding signal level error.

cal_log_scale: 10 dB/div: indicates when the 10 dB/div log scale setting is being corrected. The gilbert DAC value, corresponding dB/div, and percent of error appear for each iteration, which concludes when the dB/div is within 0.4% of its normal value.

10 DB/DIV CORRECTION (4 MHZ IF) ERROR MESSAGES

Error messages often indicate problems with the reference signal. Before proceeding with troubleshooting procedures, always check that the REF SIGNAL OUT is connected to the RF INPUT connector. If this connection is in order, check for a defective cable. The following errors may occur during this part of the correction:

Reference Signal Unknown A signal was detected when the reference was turned off. 100 MHz signals may leak into the instrument front end, due to a defective cable or A15 Calibrator module.

Reference Signal Missing. The signal is missing.

1. Check the REF SIGNAL OUT cabling.
2. If properly connected, check for a 100 MHz, –20 dBm signal from the A15 Calibrator module.

Attenuator Steps Broken The RF attenuator check failed. To check the RF attenuator steps:

1. Place a signal on the instrument display (100 MHz FREQUENCY, 500 kHz SPAN, –20 dBm REF Level, REF SIGNAL OUT connected to RF Input).
2. Establish keyboard mode and enter these commands:

```
satt val      (val is the desired attenuator setting in dB from
0 to 70)
swep          (Forces a sweep to update the display)
```

   - This command exercises the RF attenuator without affecting the reference level or gain distribution. Replace the A10 RF attenuator as required.

3. Severe compression at the top of screen may also cause this error. To check for compression:
   - Exercise the RF attenuators until observing signal behavior near the top of the screen.
   - Compression problems are often reported in the trace data as a small (<0.5 div, but >0), **delta** value for the first attenuator step. Faulty attenuator steps are indicated whenever the **delta** value is <0.05 div.

Signal Gain Timed Out Signal levels cannot be adjusted using the VR gain because the signal is noisy or missing. Noisy signals may result from uncorrected Peak Detectors or a fault in the Frequency Control system.

1. Run the Peak Detector correction.
2. If this does not correct the problem the noise is probably due to an unstable Frequency Control system (excessive FM or loss of phaselock).
   - Run the frequency self-correction routine.
   - Check the signal remaining on screen when switching from 5 MHz SPAN to 2 MHz SPAN to verify phaselock mode operation.
   - With REF SIGNAL OUT connected to RF Input and centered on screen, reduce SPAN to 10 MHz and turn on MAX HOLD to detect possible FM.

VR Gain Truncated — The VR does not have enough gain range to make the required adjustment. The instrument signal path has either too much or too little gain. Any module located between the RF Input connector and the A18 Log Processor module may be defective. To isolate the fault:

1. Apply a 100 MHz signal of known amplitude to the RF Input connector (100 MHz FREQUENCY, ZERO SPAN, –20 dBm REF Level, REF SIGNAL OUT connected to RF Input).

2. Use a spectrum analyzer to check the signal level present at the output of each module.

   - To simplify this process, check the 25 MHz signal level driving the A16 VR module at J161 first.
   - If signal amplitude is low the fault is prior to this module; if correct, the fault is either the A16 VR or A18 Log Processor module.

Log Scale Timed Out. The log scale did not meet specifications after 8 tries. This error often results from a noisy or missing signal.

1. Refer to the error message Signal Gain Timed Out for a troubleshooting procedure.

2. A defective gilbert DAC may also cause this message. To exercise the gilbert DAC, enable keyboard mode and enter the following commands:

   ```
   gilb dac    (dac is Hex value from 000 (>10 dB/div) to fff [< 1 dB/div])
   swep        (Forces a sweep to update the display)
   ```

   This command prints the current DAC value to the terminal.

   - The printed value reflects what the firmware thinks the DAC value is; the hardware on the module is not actually queried
   - Replace the A18 Log Processor if the gilbert DAC fails to respond to **gilb** ***dac*** command.

Maximin Vertical Scale Not Reachable. The gilbert DAC has insufficient range to correct the log 18 dB/div scale. Replace the A18 Log Processor module.

LOG OFFSET DAC CORRECTION (4 MHZ IF)

This step measures the resolution of the log offset DAC in dB/lsb. To accomplish this measurement, the log offset is set to zero (DAC loaded with zero value obtained during hinge point correction) and 40 dB of RF attenuation is switched in. The offset DAC value is then changed until the signal returns to its original height. During this correction the signal is located at the top of screen, and RF attenuator settings and screen position are the same as those used during the 10 dB/div correction, to ensure that no log error is introduced into the offset DAC correction. The trace looks like this:

```
cal_log_offset: VR_Path=0
                Gain_To_Lvl: lvl=1000  VertScale=10 dB/div
                     su_per_lsb=0.50  max_err=3 su
                     c_gain=0x22  f_gain=0x91  err=  -4 su
                     c_gain=0x22  f_gain=0x8b  err=  -7 su
                     c_gain=0x22  f_gain=0x8b  err=  -7 su
                     c_gain=0x22  f_gain=0x99  err=  -1 su
                Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
                     su_per_lsb=5.00  max_err=4 su
                     c_gain=0x22  f_gain=0x99  err=  23 su
                     c_gain=0x22  f_gain=0x8b  err= -26 su
                     c_gain=0x22  f_gain=0x8b  err= -26 su
                     c_gain=0x22  f_gain=0x90  err=  -7 su
                     c_gain=0x22  f_gain=0x91  err=  -3 su
                lo_bits=0x1b9  ht=997 su
```

```
Offset_To_Lvl: lvl=997 su  VertScale=1 dB/div
      LogOffset=30.00 dB  ht= 0 su  err=-997 lsb
      LogOffset=39.97 dB  ht= 748 su  err=-249 lsb
      LogOffset=42.46 dB  ht= 978 su  err= -19 lsb
      LogOffset=42.65 dB  ht= 993 su  err=  -4 lsb
      LogOffset=42.69 dB  ht= 996 su  err=  -1 lsb
hi_bits=0x5e4  ht=997 su
log_offs_res=0.0374 dB/lsb
```

cal_log_offset: VR_Path=0 indicates that log offset DAC correction for the 4 MHz path is being performed. The attenuator is set to 10 dB and the log offset set to zero. The **Gain_To_Lvl** routine sets the signal to top of screen, first in 10 dB/div, then in 1 dB/div; using VR coarse gain and VR fine gain steps. Next the offset DAC and corresponding signal level (**lo_bits=0x1b9 ht=997 su**) appear. At this point the RF attenuator is set to 50 dB. The **Offset_To_Lvl** routine returns the signal back to top of screen using the log offset DAC. **lvl=997** line is the desired signal level, and **VertScale= 1 dB/div** is the current vertical scale. For each iteration, **LogOffset** is the log offset value in dB, **ht** is the corresponding signal height, and **err** is the difference between **ht** and **Offset_To_Lvl**. **hi_bits=0x5e4** represents the new log offset DAC value and **log_offs_res=0.0374 dB/lsb** is the DAC resolution.

LOG OFFSET DAC CORRECTION (4 MHZ IF) ERROR MESSAGES

The following errors can occur during this part of the correction:

Signal Gain Times Out
VR Gain Truncated. Refer to ***10DB/DIV CORRECTION (4MHZ IF) ERROR MESSAGES*** for troubleshooting procedures.

Signal Offset Timed Out The log offset DAC cannot adjust signal levels due to a **noisy or missing signal.** Noisy signals may result from uncorrected Peak Detectors or a fault in the Frequency Control system.

1. Refer to the **Signal Gain Timed Out** error message in the ***10 DB/DIV CORRECTION (4MHZ IF) ERROR MESSAGES*** section for a troubleshooting procedure.

Signal Offset Truncated The log offset DAC does not have enough range to make the required adjustment. Normally the log offset DAC has more range than required, so this error often indicates a problem in the video system. Replace the A18 Log Processor or A20 Video Processor module.

Log Offset Resolution Data Out Of Range. The log offset DAC resolution is not meeting its specification of 0.030 to 0.050 dB/LSB. Replace the A18 Log Processor module.

1 DB/DIV CORRECTION (4 MHZ IF)

The 1 dB/div correction uses the log offset DAC correction results as a standard. Log offset is toggled between 0.0 and 9.0 dB, while measuring the resulting change in signal height. The correction terminates when the signal change is 9 divisions ±0.4%. The trace looks like this:

```
cal_log_scale: 1.00 dB/div:
                  gilbert DAC=0xa37 1.018 dB/div  err=  1.81%
                  gilbert DAC=0xa67 1.000 dB/div  err=  0.00%
            min vscale=0.66 dB/div
            max vscale=21.97 dB/div
```

cal_log_scale: 1 dB/div: indicates that the 1 dB/div log scale setting is being corrected. The gilbert DAC value, corresponding dB/div, and percent error are listed for each iteration. **min vscale** and **max vscale** are the vertical scale factor extremes that corresponding to DAC values of **0xfff** and **0x000**, respectively.

1 DB/DIV CORRECTION (4 MHZ IF) MESSAGES

The following errors can occur during this part of the correction:

Log Scale Timed Out — Refer to *10 DB/DIV CORRECTION (4 MHZ IF) ERROR MESSAGES* for a trouble-shooting procedure.

Minimum Vertical Scale Not Reachable — This error occurs when **`min vscale`** is greater than 0.80 dB/div. Replace the A18 Log Processor.

Maximum Vertical Scale Not Reachable — This error occurs when **`max vscale`** is less than 18.0 dB/div. Replace the A18 Log Processor.

10 DB/DIV CORRECTION (25 MHZ IF)

This step is essentially the same as that for the 10 dB/Div Correction (4 MHz IF) including error messages and troubleshooting procedures. During this step only 30 dB of attenuation is used (RF attenuator is switched between 10 dB and 40 dB) due to increased noise in the 25 MHz if path. An RF attenuator check is not performed because it was tested previously. The trace looks like this:

```
Calibrating 25 MHz path
     LogScaleCorr:
          setup_att_lscl:
               setting up 25 MHz path
               Chk_Signal:
                    signal off: pk_y=554 su
                    signal on : pk_y=1008 su
               Set_Filter_Lvl: lvl=1000  VertScale=10 dB/div
                    su_per_lsb=0.50  max_err=3 su
                    c_gain=0x09  f_gain=0x6e  err= 8 su
                    c_gain=0x09  f_gain=0x55  err=  -2 su
                    6-dB bw=2860000 Hz  bw_err=4.7%
               adjusting signal level...
               Gain_To_Lvl: lvl=1000  VertScale=10 dB/div
                    su_per_lsb=0.50  max_err=3 su
                    c_gain=0x09  f_gain=0x55  err= -14 su
                    c_gain=0x09  f_gain=0x6b  err=  -5 su
                    c_gain=0x09  f_gain=0x6b  err=  -5 su
                    c_gain=0x09  f_gain=0x75  err=  -1 su
               Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
                    su_per_lsb=5.00  max_err=4 su
                    c_gain=0x09  f_gain=0x75  err=  23 su
                    c_gain=0x09  f_gain=0x55  err=-104 su
                    c_gain=0x09  f_gain=0x6b  err=  -8 su
                    c_gain=0x09  f_gain=0x6d  err= 0 su
          cal_log_scale: 10.00 dB/div:
               gilbert DAC=0x07b  11.022 dB/div  err= 10.22%
               gilbert DAC=0x092  10.097 dB/div  err=  0.97%
               gilbert DAC=0x094  10.030 dB/div  err=  0.30%
```

LOG OFFSET DAC CORRECTION (25 MHZ IF)

This step is essentially the same as that for the 4 MHz IF, including error messages and troubleshooting procedures. During this step only 30 dB of attenuation is used (RF attenuator is switched between 10 dB and 40 dB) due to increased noise in the 25 MHz IF path. The trace looks like this:

```
cal_log_offset: VR_Path=1
               Gain_To_Lvl: lvl=1000  VertScale=10 dB/div
                    su_per_lsb=0.50  max_err=3 su
                    c_gain=0x09  f_gain=0x6d  err=  -4 su
                    c_gain=0x09  f_gain=0x6b  err=  -5 su
                    c_gain=0x09  f_gain=0x6b  err=  -5 su
                    c_gain=0x09  f_gain=0x75  err= 0 su
```

```
Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
      su_per_lsb=5.00  max_err=4 su
      c_gain=0x09  f_gain=0x75  err=  23 su
      c_gain=0x09  f_gain=0x55  err=-104 su
      c_gain=0x09  f_gain=0x6b  err=  -8 su
      c_gain=0x09  f_gain=0x6d  err= 0 su
lo_bits=0x1b9  ht=1000 su
Offset_To_Lvl: lvl=1000 su  VertScale=1 dB/div
      LogOffset=20.00 dB  ht=0 su  err=-1000 lsb
      LogOffset=30.00 dB  ht= 765 su  err=-235 lsb
      LogOffset=32.35 dB  ht= 968 su  err= -32 lsb
      LogOffset=32.67 dB  ht= 995 su  err=  -5 lsb
      LogOffset=32.72 dB  ht= 998 su  err=  -2 lsb
hi_bits=0x4eb  ht=998 su
log_offs_res=0.0368 dB/lsb
```

1 DB/DIV CORRECTION (25 MHZ IF)

This is identical to the 1 dB/div Correction (4 MHz I step, except for the IF signal path. The trace looks like this:

```
cal_log_scale: 1.00 dB/div:
               gilbert DAC=0x98d 1.068 dB/div  err=  6.76%
               gilbert DAC=0xa30 1.004 dB/div  err=  0.45%
               gilbert DAC=0xa3b 1.001 dB/div  err=  0.11%
          min vscale=0.65 dB/div
          max vscale=21.69 dB/div
```

INTERNAL CALIBRATOR CORRECTION

The instrument produces two reference signals. The REF SIGNAL OUT front panel produces a precision 100 MHz, –20 dBm frequency and amplitude reference signal. A menu-selectable internal calibrator introduces a –50 dBm signal directly into the first mixer. This calibrator provides a signal for most vertical corrections routines without requiring an external connection.

The internal calibrator amplitude is measured and corrected for optimum amplitude accuracy. Its level is compared to the external REF SIGNAL OUT signal amplitude. To begin this step the external calibrator is turned on and VR gain is set for a mid-screen signal. Log offset is 10 dB and an RF attenuator value of 30 dB is selected. The 30 dB of RF attenuation in series with the REF SIGNAL OUT produces an accurate –50 dBm reference to which the internal calibrator is compared. Next, the internal calibrator is turned on. Log offset is now adjusted to match the internal calibrator level to the mid-screen level established by the REF SIGNAL OUT. The trace looks like this:

```
Calib_Corr:
               Gain_To_Lvl: lvl=500  VertScale=1 dB/div
                     su_per_lsb=5.00  max_err=4 su
                     c_gain=0x09  f_gain=0xf4  err= 523 su
                     c_gain=0x09  f_gain=0xeb  err= 523 su
                     c_gain=0x09  f_gain=0xd5  err= 523 su
                     c_gain=0x09  f_gain=0x6c  err=  64 su
                     c_gain=0x09  f_gain=0x5f  err=2 su
          extern ht=502 su  offset=10.00 dB
               Offset_To_Lvl: lvl=502 su  VertScale=1 dB/div
                     LogOffset=10.00 dB  ht=0 su  err=-502 lsb
                     LogOffset=15.02 dB  ht=1023 su  err= 521 lsb
                     LogOffset= 9.81 dB  ht= 941 su  err= 439 lsb
                     LogOffset= 5.42 dB  ht= 496 su  err=  -6 lsb
                     LogOffset= 5.48 dB  ht= 503 su  err= 1 lsb
          intern ht=503 su  offset=5.48 dB
          ref_signal=-49.88 dB  offs_delta=-4.52 dB
          calib_lvl=-45.36 dBm
```

`Calib_Corr:` indicates that calibrator correction is being run. `Gain_To_Lvl` adjusts the signal height (external calibrator is on, 30 dB of attenuation) to center of screen (`lvl=500`) with VR gain while the log offset is fixed at 10 dB. `extern ht=502 su offset=10.0 dB` is the signal height and corresponding log offset for the external calibrator measurement. Next the internal calibrator is switched on and `Offset_To_Lvl` adjusts the signal height to match that of the external calibrator. `intern ht=503 su offset=5.48 dB` are the final signal height and log offset for the internal calibrator measurement.

The internal calibrator level is computed by subtracting the change in log offset from the attenuated external calibrator level. `ref_signal` is the nominal calibrator level (–20 dBm) minus the RF attenuation (using attenuator calibration data). `offs_delta` is the change in log offset between the internal and external calibrator measurements and `calib_lvl` is the internal calibrator level.

INTERNAL CALIBRATOR CORRECTION MESSAGES

The following errors can occur during this part of the correction:

Signal Gain Timed Out.
VR Gain Truncated. Refer to ***10 dB/DIV CORRECTION (4 MHZ IF) ERROR MESSAGES*** for a troubleshooting procedure.

Signal Offset Timed Out
Signal Offset Truncated. Refer to ***LOG OFFSET DAC CORRECTION 94 MHZ IF)*** for troubleshooting procedure.

Internal Calibrator Range Error. The final `calib_lvl` was not between –45 dBm and –55 dBm.

1. Turn the Internal Calibrator signal and use a spectrum analyzer to measure the 100 MHz, –20.8 dBm ±0.6 dB signal at J150 of the A15 Calibrator module.

   - Replace the A15 Calibrator module if the signal is low or missing.

2. Check for a 100 MHz, approximately –50 dBm signal at the A12A4 Low Pass Termination output driving the A12A5 Lowpass Mixer.

   - The Low Pass Termination should have a loss of 30 dB, ±3 dB.
   - Replace the A12A4 Low Pass Termination if low or missing.

LINEAR SCALE CORRECTION

Linear and power vertical scale modes are corrected at top, center, and bottom of screen. Top of screen is corrected using the hinge position DAC, bottom of screen correction is performed with a hardware adjustment on the A18 Log Processor module, and center of screen corrections use the gilbert DAC. The trace looks like this:

```
LinScaleCorr:
          hg_posn_lin_corr:
               hg posn DAC=0x800  ht= 963 su  err=-37 lsb
               hg posn DAC=0x821  ht= 999 su  err= -1 lsb
          offset_bits=0x118
          gilbert DAC=0x0a5  yval=499 su  err=-1 lsb
          4_mhz_slope=2790.0  25_mhz_slope=2745.6
          4_mhz_icept=-127.0  25_mhz_icept=-126.6
          gm_lin[0][0]=0x0a5
          gm_lin[1][0]=0x0a0
```

The linear scale correction is identified by `LinScaleCorr`. The correction starts by correcting the hinge position, or top-of-screen, for linear mode (`hg_posn_lin_corr:`). Each iteration shows the DAC value (`hg posn DAC`), signal height (`ht`), and difference between signal height and top of screen (`err`). The process stops when `err` is less than 2 LSB. `offset_bits` is the log offset DAC value that sets the signal level 6.02 dB below top of screen. Next a gilbert DAC is selected to position the signal precisely at center screen. `gilbert DAC` is the gilbert DAC value, `yval` is the corresponding signal height, and `err` is the distance from center screen. This process stops when `err` is less than 3 LSB.

After the correction is preformed using the 4 MHz IF, a 25 MHz IF gilbert DAC value is computed using the log scale correction results listed in the next two lines. `gm_lin[0][0]` is the gilbert DAC value from the 4 MHz IF correction, `gm_lin[1][0]` is the computed value for the 25 MHz IF.

LINEAR SCALE CORRECTION ERROR MESSAGES

The following errors may occur during this part of the correction:

Linear Hinge Position Truncated. The hinge position DAC on the A18 Log Processor does not have enough range to position the hinge point to top of screen.

1. In most instances, replace the A18 Log Processor module.
2. This error may also result from an incorrect 4 MHz reference oscillator signal from the A16 VR module. Refer to the **Hinge Point Data Unknown** error message under ***LOG HINGE POINT CORRECTION*** for a procedure to check the 4 MHz oscillator.

Linear Hinge Position Timed Out. The hinge point could not be set. A noisy waveform is often the cause of this error.

1. Refer to the **Signal Gain Timed Out** error message in the ***10DB/DIV CORRECTION (4MHZ IF) ERROR MESSAGES*** section for a troubleshooting procedure.
2. If the fault persists, check the A18 Log Processor and A20 Video Processor modules for noise and replace as needed.
3. Replace the A18 Log Processor module if this error persists and the signal is stable and clean.

Linear Scale Set To Limit Value. The gilbert DAC did not have enough range to position the signal at center of screen.

1. The LIN Baseline (bottom-of-screen) adjustment may be out of calibration. To check this condition:
   - Disconnect the signal input at P181 on the A18 Log Processor module.
   - Set FREQUENCY TO 112 MHz, SPAN to 10 MHz, and Ref Level/Scale to V (linear mode).
   - If the trace is not aligned with the bottom graticule, perform the LIN Baseline adjustment (refer to *Section 3 — Adjustments/Corrections*).
2. Connect the Log Processor input, and repeat the Display Law correction.
3. Replace the A18 Log Processor if the error persists after adjusting the LIN Baseline.

Linear Scale Timed Out. A center-of-screen signal could not be obtained. This is often due to a miss-adjusted LIN Baseline (bottom-of-screen).

1. Refer to **Linear Scale Set To Limit Value** for a troubleshooting procedure.

2. Replace the A18 Log Processor module if the LIN Baseline is adjusted properly and this error persists.

POWER SCALE CORRECTION

The power scale correction is nearly identical to that of the linear mode correction, as Log Processor module operation is similar for both modes. Power mode simply uses a different gilbert DAC value to obtain a display in watts rather than volts. Power mode is corrected by determining the gilbert DAC value for a 3.01 dB down center-of-screen; all other settings and computations are the same as for the linear mode. The trace looks like this:

```
PowScaleCorr:
            offset_bits=0x168
            gilbert DAC=0x1e0  yval=489 su  err=-11 lsb
            gilbert DAC=0x1ce  yval=499 su  err=-1 lsb
            4_mhz_slope=2790.0  25_mhz_slope=2745.6
            4_mhz_icept=-127.0  25_mhz_icept=-126.6
            gm_lin[0][1]=0x1ce
            gm_lin[1][1]=0x1c5
```

The power scale correction is identified by **`PowScaleCorr:. offset_bits`** is the log offset DAC value that reduces the signal to 3.01 dB below top-of-screen. Next a gilbert DAC value is determined to position the signal precisely at center screen. **`gilbert dac`** is the gilbert DAC value, **`yval`** is the corresponding signal height, and **`err`** is the distance from center screen, which must be less than 3 LSB.

The correction is performed using the 4 MHz IF. A 25 MHz IF gilbert DAC value is computed using the log scale correction results, which are listed in the next 2 lines of the trace. **`gm_lin[0][1]`** is the gilbert DAC value from the 4 MHz IF correction, and **`gm_lin[1][1]`** is the computed value for the 25 MHz IF.

POWER SCALE CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Power Scale Set To Limit Value. Refer to the **Linear Scale Set To Limit Value** error message for a trouble-shooting procedure.

Power Scale Timed Out. Refer to the **Linear Scale Timed Out** error message for a troubleshooting procedure.

ATTENUATOR CORRECTION

The A10 RF attenuator module is manufactured to very tight tolerances, but impedance mismatch between the RF attenuator and the First Converter may cause the attenuator steps to have different values when installed in the instrument. Incorrect attenuation values produce faulty dB/div correction data, which causes the log correction to function improperly. To ensure proper instrument calibration the RF attenuator steps are characterized after the module is installed into the instrument.

Unlike the other corrections, the attenuator characterization is a manual operation. It is important to avoid mistakes during the characterization and its related computations. The RF Attenuator Adjustment procedure located in *Section 3 — Adjustments/Corrections.*, is used to characterize the RF attenuator.

LISTING ATTENUATOR CORRECTION DATA

After the Attenuator correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
DCAL  2  5
```

The vertical trace must be enabled to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 5
CurrentCalData-> atten_data:
    atten[0]=0.0
    atten[1]=10.26
    atten[2]=20.11
    atten[3]=30.11
    atten[4]=40.07
    atten[5]=50.05
    atten[6]=59.96
    atten[7]=69.73
```

The number in the brackets indicates the attenuation index (equal to the nominal attenuation divided by 10), and the numbers to the right are the corresponding attenuation data. In this example, `atten[1]=10.26` indicates an actual value of 10.26 dB for the 10 dB step of the RF attenuator.

POTENTIAL PROBLEMS

The following conditions may cause problems during attenuator correction:

Noisy Signal. This is often caused by faulty connections or cables in the test setup. Check cables and connections. If the test setup is functional, this problem is probably due to a high instrument noise floor.

Unstable Signal. A signal with changing frequency or amplitude characteristics can introduce significant errors into the correction. A fault in the test setup (defective cable or signal generator) or the instrument may cause this problem.

TABLES

Tables 4-9 and 4-10 are provided to aid in computing the attenuator correction values. Table 4-9 is a completed example; Table 4-10 is a blank that may be copied for use during the correction.

Table 4-8. Attenuator Correction Table (Example)

1	2	3	4	5	6	7
Nominal Instr Atten	Nominal External Atten	Actual External Atten	External Atten Delta	External Atten Error	Marker Delta Amplitude	Actual Instr Atten
0	70	70.50	0.00	0.00	0.0	0.0
10	60	60.50	10.00	0.00	-0.1	10.1
20	50	50.50	20.00	0.00	-0.2	20.2
30	40	40.30	30.20	0.20	-0.5	30.3
40	30	30.20	40.30	0.30	-0.7	41.0
50	20	20.10	50.40	0.40	-0.4	50.8
60	10	10.10	60.40	0.40	-0.2	60.6
70	0	0.00	70.50	0.50	-0.2	70.7

Table 4-9. Attenuator Correction Table

1 Nominal Instr Atten	2 Nominal External Atten	3 Actual External Atten	4 External Atten Delta	5 External Atten Error	6 Marker Delta Amplitude	7 Actual Instr Atten
0	70		0.00	0.00	0.0	0.0
10	60					
20	50					
30	40					
40	30					
50	20					
60	10					
70	0	0.00				

LOG CORRECTION

The log transfer curve correction characterizes the non-linearities in the A18 Log Processor module. The resulting data is used to increase the accuracy of marker amplitude measurements and to correct the display law. The routine compares the log amplifier response to an external step attenuator which reduces signal amplitude in precise 1 dB steps. Corrections are performed individually for the 4 MHz and 25 MHz IFs. The procedure takes about 20 minutes. Tests are performed in this sequence:

- 4 MHz Log Correction
- Log Curve Measurement
- Screen Offset
- Step Attenuator Compensation
- 25 MHz Log Correction

NOTE

The instrument must be in its cabinet to obtain the most accurate results. Use of the RS-232 interface should be limited to diagnostics, Sweep Tracking, and Attenuator Corrections.

LISTING OF LOG CORRECTION DATA

After the Log correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
dcal 2 7
```

The vertical trace must be enabled to view the data. Following is a sample of data displayed on the terminal:

```
Enter command : vtra 1
Enter command : dcal 2 7
CurrentCalData-> lcurv_data:
     LogTbl_4MHz =
        0     9    19    29    39    49    59    69    79    89
       99   109   119   129   139   149   159   169   179   189

     . . .

LogTbl_25MHz =
        0    10    20    30    40    50    60    70    80    90
      100   110   120   130   140   150   160   170   180   190

     . . .

     11399 11409 11419 11429 11439 11449 11459 11469 11479 11489
     11499
```

The data consists of two 1151-element tables for the 4 MHz 25 MHz IFs. Each data table is formatted as a correction table, as opposed to an error table; table indices correspond to the log amplifier output, while table values correspond to the corrected log amplifier output. The indices are scaled to a 1000 point, 100 dB log amplifier, with an index of 0 at the bottom and an index of 1000 at the hinge point (nominally +16 dB into the log amplifier). The table values follow the same scale, but are multiplied by a factor of 10 to preserve data accuracy.

Only the top 85 dB of the 4 MHz log is characterized corresponding to elements 150 to 1000 of the 4 MHz table. In a similar manner, the top 50 dB of the 25 MHz log are characterized and mapped into elements 500 to 1000 of the 25 MHz table. The remaining table elements are generated by creating data corresponding to a straight line between the endpoints of the table and the nearest actual data.

During this correction the instrument displays prompts that indicate setting for both the 10 dB and 1 dB external step attenuators. Whenever a 10 dB step is changed, the 10 dB step value is compared to a 10 dB group of 1 dB steps and the VR gain adjusted to compensate for any difference. The on-screen attenuator prompt looks like this:

```
Set external attenuator to 10+3=13 dB.
```

The first number (10 in this example) is the 10 dB step attenuator setting, the second number (3) is the 1 dB step attenuator setting, and the last number (13) is the total value of external attenuation. The attenuation settings range from 0 to 85 dB for the 4 MHz log and 0 to 50 dB for the 25 MHz log. All waveforms should be clean and stable except for attenuator settings toward the end (final 10 dB) of the 4 MHz log correction.

4 MHZ LOG CORRECTION

Press the UTIL key and select Misc Corr Menu, Log Corr Menu, and Start Log Corr to begin the correction. The instrument displays this prompt for external attenuator settings:

```
Set external attenuator to 00+10=10 dB.
```

After the attenuators are set to the indicated values, press the ENTER key to continue. Instrument is automatically set up to the 100 Hz resolution bandwidth and a narrow span for the initial measurement. The log offset is set to 0.0 dB (top end of the log amp), and the VR gain adjusted until the signal is at the top graticule line with a 1 dB/ div vertical scale. The trace looks like this:

NOTE

The cabinet must be removed to view trace information with the RS-232 hookup. Normal correction requires installation of the instrument in its cabinet. During this step limit the use of the trace mode to diagnostics.

```
setup_lcorr: path=0
        Set_Filter_Lvl: lvl=1000  VertScale=10 dB/div
              su_per_lsb=0.50  max_err=3 su
              c_gain=0x22  f_gain=0x93  err= 100 su
              c_gain=0x24  f_gain=0x80  err= -34 su
              c_gain=0x24  f_gain=0xc0  err=  -3 su
              c_gain=0x24  f_gain=0xc6  err=  -1 su
        Set_Filter_Lvl: lvl=1000  VertScale=1 dB/div
              su_per_lsb=5.00  max_err=4 su
              c_gain=0x24  f_gain=0xab  err=-117 su
              c_gain=0x24  f_gain=0xc0  err= -15 su
              c_gain=0x24  f_gain=0xc3  err=  -1 su
  LogOffset=0.00  (0x1c1)
  gain=0x24 0xc3
```

Set_Filter_Lvl identifies the routine that sets signal levels using the VR gain. **lvl** is the desired signal level in screen units, **VertScale** is the current vertical scale, **su_per_lsb** is the resolution of the VR pin DAC resolution in screen units, and **max_err** is the accuracy to which the routine will set the level. For each iteration, **c_gain** is the coarse VR gain step setting, **f_gain** is the fine VR gain (pin DAC), and **err** is the measured signal level minus the desired **lvl** value.

When this step is completed, the log offset and final gain settings are displayed on the terminal. Next the display produces this prompt:

```
Set external attenuator to 00+1= 1 dB.
```

4 MHZ LOG CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Signal Level Too High.
Signal Gain Timed Out.
VR Gain Truncated. These three errors may be generated if the signal level is too high or missing.

1. Check the test setup for proper connections.
2. Reset the signal generator frequency if it has drifted form center screen.

LOG CURVE MEASUREMENT

NOTE

If the step attenuator is inadvertently changed during the remaining parts of this correction, the prompts will no longer line up with the attenuator settings. If this happens, cycle the instrument power and start over.

Once instrument setup is complete, the user proceeds in a repetitive cycle of waiting for the prompt, setting the attenuator, and pressing ENTER for each attenuator setting. The trace looks like this:

```
LC_Ref=1000  sig_ht=999  LC_Data[0]=-1
LC_Ref=900   sig_ht=908  LC_Data[1]=108
LC_Ref=800   sig_ht=806  LC_Data[2]=206
LC_Ref=700   sig_ht=701  LC_Data[3]=301
LC_Ref=600   sig_ht=600  LC_Data[4]=400
LC_Ref=500   sig_ht=498  LC_Data[5]=498
LC_Ref=400   sig_ht=399  LC_Data[6]=599
LC_Ref=300   sig_ht=307  LC_Data[7]=707
LC_Ref=200   sig_ht=216  LC_Data[8]=816
LC_Ref=100   sig_ht=131  LC_Data[9]=931
```

`LC_Ref` is the reference signal height. This value decreased by 100 (1 division on screen) for each attenuator step. `sig_ht` is the actual measured signal height and `LC_Data[]` is a table of log data as a function of attenuation.

LOG CURVE MEASUREMENT ERROR MESSAGES

The following error can occur during this part of the correction:

Incorrect Signal Level Encountered. This message is displayed if an unexpected signal level is detected. The instrument checks for the correct attenuator settings, and prompts the user to change the step attenuator settings, if between 0.5 to 1.5 dB is not detected for each 1 dB of attenuation.

1. This error results when the external step attenuator value is changed wild the instrument is adjusting signal levels. If this occurs the attenuator setting is out of step with the correction routine.
   - Cycle the instrument power and start over.
2. A noisy signal may also produce this error (the noise amplitude is large enough to appear as an amplitude error). If this occurs, cycle the instrument power and recall the store data with this command:

   rcdf 7 (or use Recall from Store in Vert Corr Menu)
3. Try the correction again. Do not proceed until this error condition is resolved.

SCREEN OFFSET

The signal level is adjusted before proceeding to the next measurement whenever the signal amplitude is within 1.5 division of the baseline. Log offset is set to increase the displayed amplitude by 8 divisions, placing the peak near the reference level. The trace looks like this:

```
moving signal level to 931...
          Set_Filter_Offs: lvl=931 su  VertScale=1 dB/div
                LogOffset= 0.00 dB  ht= 131 su  err=-800 lsb
                LogOffset= 8.00 dB  ht= 939 su  err=   8 lsb
                LogOffset= 7.92 dB  ht= 931 su  err=   0 lsb
    adj sig_ht=931 LogOffset=7.92 (0x289)
LC_Ref=800  sig_ht=839  LC_Data[10]=1039
```

`moving signal level to 931...` shows the screen location to which the signal is being moved. Next is the trace for the level-setting routine `Set_Filter_Offs: lvl=931 su  ...` which indicates the log offset (`LogOffset= 0.00 dB`), signal height (`ht=131 su`), and error (`err=-800`) for each iteration. When finished, the final signal height (`adj sig_ht=931`) and log offset (`LogOffset=7.92 (0x289)`) values are listed; the number in parenthesis is the log offset DAC value.

SCREEN OFFSET ERROR MESSAGES

The following error can occur during this part of the correction:

The Signal Offset Timed Out. This error is generated if a noisy signal is detected when positioning the signal with the log offset DAC. This condition often occurs due to a high instrument noise floor. If this occurs:

1. Cycle the instrument power and recall the store data with this command:

   rdcf 7 (or use Recall from Store in Vert Corr Menu)

2. Try the correction again. Do not proceed until this error condition is resolved.

STEP ATTENUATOR COMPENSATION

Whenever an external 10 dB attenuator step is changed, it is compared to 10 dB from the 1 dB step attenuator so that the 10 dB step value may be compensated to optimize accuracy. When making this check, the log amplifier is measured in the normal manner and this prompt appears:

```
Set external attenuator to 00+10=10 dB.
```

The corresponding trace looks like this:

```
LC_Ref=800  sig_ht=839  LC_Data[10]=1039
```

The signal level is measured (in this case 839), and this prompt to remove 10 dB of 1 dB steps and increase the 10 dB steps by 10 dB appears:

```
Set external attenuator to 10+0=10 dB.
```

Next the VR gain is adjusted to match the new signal level to that measured during the last step. The trace looks like this:

```
Set_Filter_Gain:
      Setting 1dB/div level to 839 su
      StepGain=17 dB  pk_y= 836 su  err=  -3 lsb
adj sig_ht=835  gain=0x24 0xc3
```

In this example, no adjustment was needed. Now the correction continues until the amplitude drops below 1.5 divisions, at which point a Screen Offset occurs.

STEP ATTENUATOR COMPENSATION ERROR MESSAGE

The following error can occur during this part of the correction:

Signal Gain Timed Out. This error can be generated if a noisy signal is present during VR gain adjustments. This condition often occurs due to a high instrument noise floor. If this occurs:

1. Cycle the instrument power and recall the store data with this command:

   rcdf 7 (or use Recall from Store in Vert Corr Menu)

2. Try the correction again. Do not proceed until this error condition is resolved.

SETTING-UP THE 25 MHZ LOG CORRECTION

This is identical to the 4 MHz correction, except that the measurements are made in zero span mode with a 3 MHz resolution bandwidth setting. All errors and prompts are the same as those for the 4 MHz log correction.

GAIN STEP CORRECTION

The gain step correction corrects the discrete gain steps used by the reference level firmware; these gain steps are located in the VR and microwave IF modules. The gain step correction assumes that display law and log corrections have been performed. The gain step correction takes about 30 seconds to complete.

The sequence performed by the firmware is as follows:

LISTING OF GAIN STEP CORRECTION DATA

After the Gain Step correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

dcal 2 3

The vertical trace must be enabled to view the data. The terminal will display the following:

```
Enter command : vtra 1
Enter command : dcal 2 3 CurrentCalData-> gstep_data:
   gs_tbl[ 0]=0x24 0x00    gs_tbl[ 1]=0x24 0x15    gs_tbl[ 2]=0x24 0x2b
   gs_tbl[ 3]=0x24 0x40    gs_tbl[ 4]=0x24 0x55    gs_tbl[ 5]=0x24 0x6b
   gs_tbl[ 6]=0x24 0x80    gs_tbl[ 7]=0x24 0x95    gs_tbl[ 8]=0x24 0xa7
   gs_tbl[ 9]=0x24 0xbc    gs_tbl[10]=0x24 0xd0    gs_tbl[11]=0x22 0x13
   gs_tbl[12]=0x22 0x28    gs_tbl[13]=0x22 0x3e    gs_tbl[14]=0x22 0x54
   gs_tbl[15]=0x22 0x68    gs_tbl[16]=0x22 0x7d    gs_tbl[17]=0x22 0x93
   gs_tbl[18]=0x22 0xa9    gs_tbl[19]=0x22 0xbd    gs_tbl[20]=0x12 0x05
   gs_tbl[21]=0x12 0x19    gs_tbl[22]=0x12 0x2c    gs_tbl[23]=0x12 0x41
   gs_tbl[24]=0x12 0x56    gs_tbl[25]=0x12 0x6e    gs_tbl[26]=0x12 0x85
   gs_tbl[27]=0x12 0x99    gs_tbl[28]=0x12 0xac    gs_tbl[29]=0x12 0xbf
   gs_tbl[30]=0x11 0x09    gs_tbl[31]=0x11 0x1e    gs_tbl[32]=0x11 0x33
   gs_tbl[33]=0x11 0x4a    gs_tbl[34]=0x11 0x61    gs_tbl[35]=0x11 0x79
   gs_tbl[36]=0x11 0x8d    gs_tbl[37]=0x11 0xa0    gs_tbl[38]=0x11 0xb4
   gs_tbl[39]=0x11 0xc6    gs_tbl[40]=0x09 0x04    gs_tbl[41]=0x09 0x1b
   gs_tbl[42]=0x09 0x31    gs_tbl[43]=0x09 0x48    gs_tbl[44]=0x09 0x5c
   gs_tbl[45]=0x09 0x71    gs_tbl[46]=0x09 0x85    gs_tbl[47]=0x09 0x99
   gs_tbl[48]=0x09 0xad    gs_tbl[49]=0x09 0xc1    gs_tbl[50]=0x09 0xd5
   gs_tbl[51]=0x09 0xe7    gs_tbl[52]=0x09 0xf7    gs_tbl[53]=0x09 0xff
   gs_tbl[54]=0x09 0xff    gs_tbl[55]=0x09 0xff    gs_tbl[56]=0x09 0xff
   gs_tbl[57]=0x09 0xff    gs_tbl[58]=0x09 0xff    gs_tbl[59]=0x09 0xff
   max_gs=52
   uwave_gain=4.53
   vr_out[0]=0.00
   vr_out[1]=9.27
   vr_out[2]=19.14
```

`gs_tbl [n]` is the correction data for the *[n'th]* gain step. Numbers in the left column are the coarse gain selections, decoded as shown in Table 4-11.

Table 4-10. Coarse Gain Values.

Coarse Gain	Gain Value
0x24	0 dB
0x22	9 dB
0x12	18 dB
0x11	27 dB
0x09	26 dB

Numbers in the right column are the fine gain DAC value. `max_gs` is the maximum gain step in dB, representing the last `gs_tbl[]` entry containing valid data. `uwave_gain` is the value of the microwave gain step. `vr_out[1]` and `vr_out[2]` are the measured value of the microwave gain step. `vr_out[0]` is the value of the 0 dB step, 0.00 by definition.

Several keyboard commands are available for manipulating the gain steps.

`ganc x`

sets the VR coarse gain, where *x* is a value from Table 4-11.

`ganf x`

sets the VR coarse gain, where *x* is the fine gain DAC value ranging from 00 to ff.

`uwif 0, 1`

turns the microwave IF step on (00) or off (1).

`gred n`

sets the VR output gain to 0, 10, and 20 dB for *n* values of 0, 1, and 2, respectively.

MICROWAVE IF GAIN STEP CORRECTION

The microwave IF gain step is a single switchable gain stage located in the A13 Microwave IF module. The correction measures the gain step value and stores this data for use when changing reference level settings. To begin this sequence the gain step is turned on, log offset is set to 0 dB, and VR gain adjusted for top-of-screen signal in 1 dB/div. Next the gain step is turned off to reduce the signal amplitude. The measured microwave IF gain step value is represented by the amplitude change from the top-of-screen reference. The trace looks like this:

```
meas_uwif_step:
      adjusting vr gain...
      LogOffset=0.00
            Gain_To_Lvl: lvl=990  VertScale=10 dB/div
                  su_per_lsb=0.50  max_err=3 su
                  c_gain=0x24  f_gain=0x00  err=-295 su
                  c_gain=0x12  f_gain=0xd5  err=   2 su
            Gain_To_Lvl: lvl=1000  VertScale=1 dB/div
                  su_per_lsb=5.00  max_err=4 su
                  c_gain=0x12  f_gain=0xd5  err= -73 su
                  c_gain=0x12  f_gain=0xd5  err= -73 su
                  c_gain=0x12  f_gain=0xd5  err= -72 su
                  c_gain=0x12  f_gain=0xe3  err=   5 su
                  c_gain=0x12  f_gain=0xe2  err=  -1 su
      top_ht=999 su  bot_ht=547 su  uw_gain=4.52 dB
```

`meas_uwif_step` identifies that the microwave IF step is being measured. `LogOffset=0.00` is the log offset setting of 0.0 dB. The `Gain_To_Lvl` routine sets the signal level using VR gain. First the signal is first set to a height of `990 su` in 10 dB/div, then to `1000 su` in 1 dB/div. Next the microwave step is turned off. `top_ht` is the signal level with the gain on, `bot_ht` is the signal level with the gain off, and `uw_gain` is the difference in dB.

MICROWAVE IF GAIN STEP CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Signal Gain Timed Out.
VR Gain Truncated. Refer to these error messages in the **10 dB/div Correction (4 MHz IF)** part of the *DISPLAY LAW CORRECTION* for troubleshooting procedures.

Microwave IF Gain Step Out Of Range. The microwave IF gain step does not measure between 3.0 and 10.0 dB. Due to this error, the instrument may not meet its gain specifications, but the correction does not abort. Instead, the measured value is recorded and used as it was correct.

Gain Step Internal Self-Corr Terminated. This error is generated at the end of the Gain Step correction if any other error occurs. Use the other error messages (in error log and trace data) to determine the cause of failure. This failure may also indicate a signal loss in the instrument front end.

VR OUTPUT GAIN STEP CORRECTION

The VR output gain consists of switchable gain stages with nominal values of 0, 10, and 20 dB. These steps are corrected by measuring their values and storing this data for use when changing reference level settings. The trace looks like this:

```
meas_vr_out:
      adjusting vr gain...
      LogOffset=0.00
            Gain_To_Lvl: lvl=910  VertScale=10 dB/div
                  su_per_lsb=0.50  max_err=3 su
                  c_gain=0x24  f_gain=0x00  err=-410 su
                  c_gain=0x09  f_gain=0x40  err=  20 su
                  c_gain=0x09  f_gain=0x15  err=  -1 su
            Gain_To_Lvl: lvl=100  VertScale=3 dB/div
                  su_per_lsb=1.67  max_err=3 su
                  c_gain=0x09  f_gain=0x15  err= 591 su
                  c_gain=0x12  f_gain=0x2b  err= -32 su
                  c_gain=0x12  f_gain=0x2b  err= -32 su
                  c_gain=0x12  f_gain=0x3e  err=  -6 su
                  c_gain=0x12  f_gain=0x42  err=   1 su
      top_ht=409 su  bot_ht=101 su  vr_out[1]= 9.24 dB
      top_ht=739 su  bot_ht=101 su  vr_out[2]=19.14 dB
```

`meas_vr_out` identifies when the VR output gain is being measured. First the log offset is set to 0 dB (`LogOffset=0.00`), and the signal level adjusted to a height 1 division above the baseline in 3 dB/div. At this time the VR output gain steps value is 0 dB. Next the 10 dB and 20 dB output gain steps are alternately turned on. Their dB value is determined by measuring the on-screen signal amplitude change. `top_ht` is the signal level with a step turned on and, `bot_ht` is the reference level signal level with no gain. `vr_out[1]` and `vr_out[2]` are the measured 10 dB and 20 dB step values.

VR OUTPUT GAIN STEP CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Signal Gain Timed Out.
VR Gain Truncated. Refer to these error messages in the **10 dB/div Correction (4 MHz IF)** part of the ***DISPLAY LAW CORRECTION*** for troubleshooting procedures.

VR Output Gain Out Of Range. The VR output gain steps do not meet specifications. The 10 dB step value must range between 8 and 11 dB, and the 20 dB step must range between 17 and 21 dB. Due to this error, the instrument may not met its gain specifications, but the correction does not abort. Instead, the measured values are recorded and used as if they were correct.

Gain Step Internal Self-Corr Terminated. Refer to this error message under **Microwave IF Gain Step Correction Error Messages** for a troubleshooting procedure.

1 DB GAIN STEP CORRECTION

The 1 dB gain steps are a combination of discrete (coarse) gain steps and fine gain from a pin DAC circuit located within the A16 VR module. The VR module contains two discrete coarse gain steps, each with nominal settings of 0, 9, and 18 dB, for a total of 36 dB. The 8-bit pin gain DAC with nominal gain range from 0 to 12 dB, in 0.05 dB steps. Each 1 dB gain step is corrected by determining the combination of coarse gain and fine gain that produces the desired 1 dB gain step values. These settings are sued to set the reference level.

The 1 dB steps are corrected in 1 dB/div, starting with the 0 dB (minimum gain) settings and increasing to maximum gain. When the signal level reaches the reference level, log offset is used to move the signal toward the baseline so the gain may increase. This correction terminates when either gain or log offset runs out of range. The trace looks like this:

```
cal_gain_steps:
      adjusting log offset...
            Offset_To_Lvl: lvl=910 su  VertScale=10 dB/div
                  LogOffset= 0.00 dB  ht= 456 su  err=-454 lsb
                  LogOffset=45.40 dB  ht= 912 su  err=   2 lsb
            Offset_To_Lvl: lvl=100 su  VertScale=1 dB/div
                  LogOffset=45.40 dB  ht=  99 su  err=  -1 lsb
      gs_tbl[1]:
      set_gain_to_lvl: lvl=200 su
            c_gain=0x24  f_gain=0x15  err= -4 su
      gs_tbl[2]:
      set_gain_to_lvl: lvl=300 su
            c_gain=0x24  f_gain=0x2b  err= -2 su
      gs_tbl[3]:
      set_gain_to_lvl: lvl=400 su
            c_gain=0x24  f_gain=0x40  err= -3 su
      ...
      gs_tbl[7]:
      set_gain_to_lvl: lvl=800 su
            c_gain=0x24  f_gain=0x95  err=  5 su
      gs_tbl[8]:
      set_gain_to_lvl: lvl=900 su
            c_gain=0x24  f_gain=0xab  err= 21 su
            c_gain=0x24  f_gain=0xa7  err=  1 su
      gs_tbl[9]:
      adjusting log offset...
            Offset_To_Lvl: lvl=100 su  VertScale=1 dB/div
                  LogOffset=45.40 dB  ht= 901 su  err= 801 lsb
                  LogOffset=37.39 dB  ht=  94 su  err=  -6 lsb
                  LogOffset=37.45 dB  ht= 102 su  err=   2 lsb
      set_gain_to_lvl: lvl=200 su
            c_gain=0x24  f_gain=0xc0  err= 21 su
            c_gain=0x24  f_gain=0xbc  err=  0 su
      gs_tbl[10]:
      set_gain_to_lvl: lvl=300 su
            c_gain=0x24  f_gain=0xd5  err= 28 su
            c_gain=0x24  f_gain=0xcf  err= -6 su
      ...
      gs_tbl[52]:
      set_gain_to_lvl: lvl=500 su
            c_gain=0x09  f_gain=0xff  err= 39 su
            c_gain=0x09  f_gain=0xf7  err=-10 su
            c_gain=0x09  f_gain=0xf8  err= -4 su
      gs_tbl[53]:
      set_gain_to_lvl: lvl=600 su
            c_gain=0x09  f_gain=0xff  err=-62 su
      max_gs=52 dB
```

`cal_gain_steps` identifies when the 1 dB gain steps are being corrected. Initially the coarse gain, fine gain, VR output and microwave IF gain are set to zero. Log offset is used to set the signal to a height of 100 su, 1 division up from the baseline in 1 dB/div (`Offset_To_Lvl...`). As each gain is corrected, a table entry `gs_tbl[n]`, where *n* is the gain step being corrected, is generated showing the coarse gain (`c_gain`) and fine gain (`f_gain`) settings. `set_gain_to_lvl: lvl=200 su` is the target signal height for the first step, 200 in this example, which is 100 su or 1 dB greater than the initial level setting. For each iteration, `err` is the difference between the measured and target signal height, with a 10 su maximum. The measured signal height has been corrected for the log curve, so level changes may not correspond to one division per step on the display.

When the target signal level reaches a height of 900 su (1 division below the reference level), log offset is used to return the signal level to 100 su (`Offset_To_Lvl...`). The correction terminates if the log offset goes negative or the VR module has no more gain. The former is indicated when the trace displays `c_gain=0x09 f_fain=0xff` with an `err` of 10 or more. When this happens the value of the previous gain step, which is the maximum valid one, is recorded (`max_gs=52`) and checked against the gain specifications.

1 DB GAIN STEP CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

Signal Offset Timed Out.
Signal Offset Truncated. Refer to these error messages in the **Log Offset DAC Correction (4 MHz IF)** part of the *DISPLAY LAW CORRECTION* for troubleshooting procedures.

Gain Step Correction Took Too Long. The correction of the current gain step did not succeed within 20 tries. This error is often due to a noisy signal trace or unstable instrument performance.

1. Run the Peak Detector correction.

2. Check for a stable Frequency Control system. Refer to the **Signal Gain Timed Out** error message in the *10 dB/div CORRECTION (4 MHZ IF) ERROR MESSAGES* section for a troubleshooting procedure.

Gain Step Correction Terminated Hardware Failure Indicated. The correction required a negative gain setting to correct the current gain step. The instrument is unable to correctly measure signal levels, indicating a serious instrument-level malfunction, because an apparent increase to the reference signal level occurred since a zero-gain level was measured. An unstable signal amplitude may be caused by a variety of failures including Frequency Control phase lock and sweep acquisition. Look for additional symptoms to isolate the fault.

VR 25 MHz Gain Out Of Range. The maximum VR gain (`vr_gs`) is not between 45 and 58 dB. Although the instrument may not meet its gain specifications, this correction does not abort. The low gain is compensated for with increased log offset, reducing the dynamic range for lower RefLevel values. If the log offset runs out of range, lower RefLevel values may not be available. Replace the A16 VR module.

Gain Step Internal Self-Corr Terminated. Refer to this error message under *MICROWAVE IF GAIN STEP CORRECTION ERROR MESSAGES* for a troubleshooting procedure.

RESOLUTION BANDWIDTH AND REFERENCE LEVEL CORRECTION

The resolution bandwidth correction adjusts the bandwidth of most resolution bandwidth filters, and sets the gain of each filter for accurate reference levels on the display. A "negative resistance" correction is performed to maximize the VR module's dynamic range. This routine is the last vertical corrections sequence. It assumes that all other vertical corrections have been successfully completed. Most failures are related to the A16 VR module. The correction takes approximately 15 minutes to complete.

NOTE

To successfully perform the Resolution Bandwidth step for final correction, the instrument must run for at least 1 ½ hours with its cabinet installed. Resonator Tracking must be performed immediately before this routine.

A VBW (Variable Bandwidth) DAC located within the A16 VR module provides fine control of the resolution bandwidth for all filter settings of 1 MHz or less. The 3 MHz and 10 MHz bandwidths are fixed filters that are calibrated with hardware adjustments. After a filter is corrected for bandwidth, the reference level is corrected for optimum amplitude accuracy. Reference level correction occurs for the full range of bandwidths. A negative resistance amplifier is adjusted to provide coarse bandwidth amplitude leveling before any other resolution bandwidth corrections are performed.

Table 4-12 lists control parameters that correspond to the fourteen available resolution bandwidth ranges. Several of these are currently unused. **MinBW Mode** shows which resonators are operating in minimum bandwidth (**MinBW**) and normal mode. **RS1-RS2** shows which of two switchable resistors (**RS1 and RS2**) that load the resonators and set bandwidth range are used. **0x2** selects RS1, **0x1** selects RS2, and **0x3** selects both. **Z** is another bandwidth setting variable that selects between narrow bandwidth (**0, Low Z**) and wide bandwidth (**1, High Z**) modes. LC/Crystal Mode shows the type of resonator being used. VRPath Bits direct signal through the switching circuits path within the VR module. Pre/Post Filter Gain selects an internal gain value for optimum filter performance at various settings. The procedure takes about 15 minutes. Tests are performed in this sequence:

- Negative Resistance Correction
- ResBW and Reference Level Correction

Table 4-11. Bandwidth Range Settings

Range Number	ResBW Range	MinBW Mode	RS1 RS2	Z	LC/Crystal Mode	VRPath Bits	Pre/Post Filter Gain
0	3Hz- 33Hz	MinBW	0x2	0	Crystal	0x322	0x04
1	33Hz- 47Hz	Normal	0x2	0	Crystal	0x322	0x02
2	47Hz- 230Hz	Normal	0x0	0	Crystal	0x322	0x01
3	230Hz- 190Hz	Normal	0x3	1	Crystal	0x322	0x02
4	190Hz- 370Hz	Normal	0x1	1	Crystal	0x322	0x02
5	370Hz- 680Hz	Normal	0x2	1	Crystal	0x322	0x02
6	680Hz-5300Hz	Normal	0x0	1	Crystal	0x322	0x01
7	5 kHz- 12 kHz	MinBW	0x2	0	LC	0x342	0x04
8	12 kHz- 83 kHz	MinBW	0x2	0	LC	0x542	0x04
9	83 kHz-120 kHz	Normal	0x2	0	LC	0x542	0x02
10	120 kHz-580 kHz	Normal	0x0	0	LC	0x542	0x01
11	580 kHz-630 kHz	Normal	0x3	1	LC	0x542	0x02
12	630 kHz-920 kHz	Normal	0x1	1	LC	0x542	0x02
13	920 kHz-1.7 MHz	Normal	0x2	1	LC	0x542	0x02

LISTING OF RESOLUTION BANDWIDTH CORRECTION DATA

After the Resolution Bandwidth and Reference Level correction is complete, a summary of the resulting current data may be listed and examined when keyboard mode is enabled by entering the command:

```
dcal 2 4
```

The vertical trace must be enabled to view the data. The terminal will display the following:

```
Enter command : dcal 2 4
CurrentCalData-> resbw_data:
     ResBW  VRPath MinBW  RS  Neg_R  VBW  RFGain  Z   XLC  Range   Refl_Corr
          3  0x0322 0x3f  0x2  0xef  0x6e   0x4   0  0x00    0     20.37 dB
         10  0x0322 0x3f  0x2  0xef  0xce   0x4   0  0x00    0     22.01 dB
         30  0x0322 0x3f  0x2  0xef  0xf5   0x2   0  0x00    0     22.48 dB
        100  0x0322 0x00  0x0  0xef  0xb7   0x1   0  0x00    2     22.14 dB
        300  0x0322 0x00  0x1  0x74  0xf4   0x2   1  0x00    4     21.12 dB
       1000  0x0322 0x00  0x0  0x74  0x9d   0x1   1  0x00    6     21.27 dB
       3000  0x0322 0x00  0x0  0x74  0xf3   0x1   1  0x00    6     21.25 dB
      10000  0x0342 0x3f  0x2  0xc7  0x9e   0x4   0  0x3f    7     37.20 dB
      30000  0x0542 0x3f  0x2  0xc7  0xdd   0x2   0  0x3f    8     19.15 dB
     100000  0x0542 0x00  0x0  0xc7  0x50   0x2   0  0x3f   10     19.39 dB
     300000  0x0542 0x00  0x0  0xc7  0xc5   0x1   0  0x3f   10     19.14 dB
    1000000  0x0542 0x00  0x2  0x70  0x91   0x2   1  0x3f   13     18.49 dB
    3000000  0x0844 0x00  0x0  0x00  0x00   0x0   0  0x00   14     38.99 dB
   10000000  0x0884 0x00  0x0  0x00  0x00   0x0   0  0x00   14     38.81 dB
```

Table 4-12. VR Path Bit Map

Bit	(Hex)	Function
bit 0	(0001)	29 MHz Count (VR 1)
bit 1	(0002)	4 MHz Path (VR 1)
bit 2	(0004)	25 MHz Path (VR 1)
bit 3	(0008)	NBW for 25 MHz Ringdown (VR 1)
bit 4	(0010)	25 MHz Source (VR 1)
bit 5	(0020)	10 kHz Xtal Filter (VR 1)
bit 6	(0040)	3 MHz Filter (VR 1)
bit 7	(0080)	10 MHz Filter (VR 1)
bit 8	(0100)	29 MHz Osc On/Off (VR 2)
bit 9	(0200)	Bandpass Filter Path (VR 3)
bit 10	(0400)	Low Pass Filter Path (VR 3)
bit 11	(0800)	25 MHz Path (VR 3)
bit 12	(1000)	4 MHz Source (VR 3)

`ResBW` is the resolution bandwidth for the row of data. `VRPath` defines signal paths through the switchable circuits within the A16 VR module. Table 4-13 summarizes the bit mapping. These paths may be set up (by adding the Hex values) to isolate failures within the A16 VR module, and to route signals through the VR module to other destinations within the instrument (such as the A18 Log Processor module) for diagnostic testing. For example, the value `0x0322` sets this VR signal path:

0002 4 MHz Path (VR 1)
0020 10 kHz Xtal Filter (VR 1)
0200 Bandpass Filter (VR 3)
0100 29 MHz Osc On (VR 2)
0322 VR Path bit map

Following are other settings that could be implemented using data from the `dcal 2 4` printout.

0002 4 MHz Path (VR 1)
0040 3 MHz Filter (VR 1)
0100 29 MHz Osc On (VR 2)
0200 Bandpass Filter Path (VR 3)
0342 VR Path bit map

0002 4 MHz Path (VR 1)
0040 3 MHz Filter (VR 1)
0100 29 MHz Osc On (VR 2)
0400 Low Pass Filter Path (VR 3)
0542 VR Path bit map

0004 25 MHz Path (VR 1)
0040 3 MHz Filter (VR 1)
0000 29 MHz Osc Off (VR 2)
0800 25 MHz Path (VR 3)
0844 VR Path bit map

0004 25 MHz Path (VR 1)
0080 10 MHz Filter (VR 1)
0000 29 MHz Osc Off (VR 2)
0800 25 MHz Path (VR 3)
0884 VR Path bit map

These paths are especially useful for instrument-level diagnostics:

0001 29 MHz Count (VR 1)
0100 29 MHz Osc On (VR 2)
0800 25 MHz Path (VR 3)
0901 29 MHz Osc Count VR Path bit map

1000 4 MHz Source (VR 3)
1000 4 MHz Source VR Path bit map

0004 25 MHz Path (VR 1)
0010 25 MHz Source (VR 1)
0020 10 kHz Xtal Filter (VR 1)
0000 29 MHz Osc Off (VR 2)
0800 25 MHz Path (VR 3)
0834 25 MHz Source VR Path bit map

The VR Path bits can be set over the RS-232 Interface with the `vpath` command or with the **VR Cal program** for the VR module adjustment procedure (refer to ***Section — 3 Adjustment/Corrections***).

`MinBW` indicates whether the resonators are in minimum bandwidth mode; `0x3f` sets all 6 to minimum bandwidth mode, `0x00` sets them to normal mode. `RS` is the state of RS1 and RS2; `0x2` selects RS1, `0x1` selects RS2, and `0x3` selects both. `Neg_R` is the Negative R DAC value for each filter, while `VBW` is the VBW DAC value and `PFGain` is the pre-filter and post-filter gain selections. Table 4-14 summarizes the available pre-filter and post-filter selections. `Z` is 1 for High Z and 0 for Low Z operation. `XLC` selects LC (`0x3f`) or Crystal (`0x00`) resonator mode. Range is one of fourteen resolution bandwidth range from Table 4-12. `Refl_Corr` is the reference level correction factor.

Table 4-13. VR Path Switch Bit Maps

PFGain Value	Pre-Filter Gain	Post-Filter Gain
0x0	off	off
0x1	+6 dB	-6 dB
0x2	0 dB	0 dB
0x4	-6 dB	+6 dB

NEGATIVE RESISTANCE CORRECTION

The A16 VR module contains a negative resistance (Negative R) amplifier that levels the bandwidths filter amplitudes for each High Z/Low Z and LC/Crystal combination. A Negative R DAC value is determined to set the bandwidths within that combination to about the same amplitude. For each combination of bandwidth ranges, the correction begins by making initial amplitude and bandwidth measurements at the minimum and maximum bandwidths. These results are used to compute an amplitude where the negative R is optimized.

The Negative R DAC is highly non-linear, so a binary search algorithm is used to determine the desired amplitude. This search technique begins with a measurement at the midpoint of the DAC range. One half of the DAC range is then eliminated by checking whether the signal level is too high or too low. The next measurement is taken at the midpoint of the remaining range to again divide the DAC range in half. This process continues until the search range is reduced to one LSB. Once the best value is obtained, the corresponding error is checked to make sure it is within tolerance. The trace looks like this:

```
ResBWCorrection :
cal_neg_res:
 cal_neg_res: Lo Z  Crystal
       measure_y0:
             min_rng= 0  min_rbw=10 Hz      min_vbw=0x60
             max_rng= 2  max_rbw=100 Hz     max_vbw=0xf0
             ResBWLvl=0xd0
             y2=805 su  rt2= 432.80 ohms
             y1=147 su  rt1=  18.25 ohms
             y0 (final) = 877 su
       bw_lvl=0x80  lvl_err=-82.80 dB
       bw_lvl=0xbf  lvl_err=-78.50 dB
       bw_lvl=0xdf  lvl_err=-56.80 dB
       bw_lvl=0xef  lvl_err= 14.10 dB
       bw_lvl=0xe7  lvl_err=-33.60 dB
       bw_lvl=0xeb  lvl_err=-15.00 dB
       bw_lvl=0xed  lvl_err= -3.90 dB
       bw_lvl=0xee  lvl_err=  2.50 dB
       bw_lvl=0xee (final)
 cal_neg_res: Hi Z  Crystal
       ...
 cal_neg_res: Lo Z  LC
       ...
 cal_neg_res: Hi Z  LC
       ...
```

cal_neg_res: Lo Z Crystal identifies that the negative R is being corrected for the low Z crystal combination. **measure_y0** dotes when the target amplitude determination begins. **min_rng= 0 min_rbw=10 Hz min_vbw=0x60** shows the range number, nominal resolution bandwidth, and specific VBW DAC value used for the narrow bandwidth portion of the measurement. **max_rng= 2 max_rbw=100 Hz max_vbw=0xf0** is the same information for the wide bandwidth measurement. **ResBWLvl** is the Negative R DAC value at which the measurements are made. The next two lines (**y2=805 ... y1=147 ...**) are the results of the wide (**y2**) and narrow (**y1**) bandwidth measurements. **rt2** and **rt1** are termination resistances computed from the measured bandwidth values, and **y0 (final)** is the target amplitude.

The DAC value and signal level error is listed for each iteration of the binary searches also listed. **bw_lvl** is the Negative R DAC value, and **lvl_err** is the difference between the measured level and **y0**. The final DAC value (**bw_lvl=0xee (final)**) appears when the search is finished. An error is generated if the **err** exceeds 5.0 dB.

NEGATIVE RESISTANCE CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

VR Negative Resistance DAC Too Coarse. This error is generated if any of the Negative R corrections fails. The specific correction is identified by one or more of the following errors.

Low Z, Crystal Neg R DAC Too Coarse
High Z, Crystal Neg R DAC Too Coarse
Low Z, LC Neg R DAC Too Coarse
High Z, LC Neg R DAC Too Coarse. Each of these errors identifies a specific High Z/Low Z LC/Crystal combination whose level could not be calibrated to within 5 dB of target. Refer to ***Section 3 — Adjustment/ Corrections*** for an adjustment procedure to replace the A16 VR module.

Measure Bandwidth Found Bad Waveform. There was an unsuccessful attempt to make a bandwidth measurement due to an invalid waveform. The signal may be missing or severely distorted. The A16 VR module is the cause most often.

1. Check for a stable Frequency Control system. Refer to the **Signal Gain Time Out** error message in the ***10 DB/DIV CORRECTION (4 MHZ IF) ERROR MESSAGES*** section for a way to do this.

2. Replace the A16 VR module if the Frequency Control system is operating properly.

ResBW and Reference Level Correction

During this step each resolution filter is corrected for bandwidth (except for 3 MHz and 10 MHz filters), and amplitude. A nominal setting for each bandwidth is selected using the default correction data and the appropriate Negative R value. First a coarse reference level correction is performed to position the signal peak two divisions from the reference level in 1 dB/div. Next the bandwidth is corrected to within 4% of its nominal value. A final reference level correction is now performed to produce a signal level of –20 dBm that is accurate to within ± 0.05 dB.

The 3 Hz, 3 MHz, and 10 MHz filters are only corrected for amplitude. Self-correction bandwidth adjustments are not available for the 3 MHz and 10 MHz bandwidths; they are set by hardware adjustments. The 3 Hz bandwidth is adjustable, but its bandwidth is not corrected due to stability limitations of the Frequency Control system.

ResBW and Reference Level Correction trace information is highly repetitive, so much data has been ;omitted from this document. Traces for the 3 Hz and 10 bandwidths are included as examples of amplitude-only and full bandwidth correction. The trace for the 3 Hz bandwidth looks like this:

```
Calibrating ResBW=3 Hz
 cal_bw_lvl: 10 dB/div
       lvl=1000 su  max_err=20 lsb
       ResBWLvlCorr=30.00  gain=43 dB  offset=0.39 dB  err= 200su
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err= -5 su
 cal_bw_lvl: 1 dB/div
       lvl=1000 su  max_err=5 lsb
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err= -58 su
       ResBWLvlCorr=10.58  gain=23 dB  offset=0.97 dB  err= -8 su
       ResBWLvlCorr=11.24  gain=24 dB  offset=0.63 dB  err= 1 su
```

`Calibrating ResBW=3 Hz` identifies when the 3 Hz bandwidth is being corrected. **cal_bw_lvl** is a routine used to correct the reference level for the current bandwidth. The reference level is corrected first in 10 dB/div, then in 1 dB/div for maximum accuracy. `lvl` is the height to which the signal is adjusted, and `max_err` is the accuracy to which it is set. For each iteration, `ResBWLvlCorr` is the resolution bandwidth reference level correction factor, `gain` and `offset` are the corresponding VR gain and log offset settings. `err` is the reference level error in screen units.

The trace for the 10 Hz bandwidth looks like this:

```
Calibrating ResBW=10 Hz
 cal_bw_lvl: 10 dB/div
       lvl=980 su  max_err=20 lsb
       ResBWLvlCorr=30.00  gain=43 dB  offset=0.39 dB  err= 200su
       ResBWLvlCorr=10.00  gain=23 dB  offset=0.39 dB  err= -39 su
       ResBWLvlCorr=13.90  gain=27 dB  offset=0.29 dB  err=  -1 su
 cal_bw_lvl: 1 dB/div
       lvl=920 su  max_err=20 lsb
       ResBWLvlCorr=13.90  gain=27 dB  offset=0.29 dB  err=-158su
       ResBWLvlCorr=15.48  gain=28 dB  offset=0.87 dB  err=  -5 su
 range=0  vbw=0xc9  bw_err=-1.74 Hz (-17.4 %)
 range=0  vbw=0xd3  bw_err=0.74 Hz (7.4 %)
 range=0  vbw=0xcf  bw_err=-0.07 Hz (-0.7 %)
 cal_bw_lvl: 1 dB/div
       lvl=1000 su  max_err=5 lsb
       ResBWLvlCorr=15.48  gain=28 dB  offset=0.87 dB  err=-101su
       ResBWLvlCorr=16.49  gain=29 dB  offset=0.88 dB  err=  -6 su
       ResBWLvlCorr=16.55  gain=29 dB  offset=0.94 dB  err= 0 su
```

This reference level correction is divided into two parts because filter bandwidth correction causes small changes in signal amplitude. The `cal_bw_lvl` routine adjusts the signal level to 2 divisions below top-of-screen in 1 dB/div. This trace for this part is the same as that for the 3 Hz bandwidth. During the bandwidth correction `range` is the bandwidth range, `vbw` is the VBW DAC value, and `bw_err` is the bandwidth error expressed in Hz and percentage. Each bandwidth is corrected to within 4%. After the bandwidth correction, the reference level is adjusted in the same manner as the 3 Hz filter.

RESBW AND REFERENCE LEVEL CORRECTION ERROR MESSAGES

The following errors can occur during this part of the correction:

BW Correction Timed Out; Terminated. The bandwidth could not be corrected. Refer to ***Section 3 — Adjustments/Corrections*** for an adjustment procedure or replace the A16 VR module.

Bandwidth Correction Reached Limit. A bandwidth (normally the 1 MHz and 10 Hz filters) could not be corrected because the hardware has insufficient range. Refer to ***Section 3 — Adjustments/Corrections*** for an adjustment procedure or replace the A16 VR module.

BW Level Correction Timed Out. The bandwidth could not be corrected, typically due to incorrect correction data for the Display Law, Gain Step, or Log corrections, or a combination of these. Run these corrections before proceeding.

This error is often intermittent and difficult to isolate. If module replacement is required, replace the A16 VR or A18 Log Processor modules and run the ResBW correction at least 3 times to ensure that the error condition has been repaired.

Resolution Bandwidth Self-Corr Failed. This error is generated at the end of the ResBW correction if any other errors occur. Use the other error messages (in error log and trace data) to determine the cause of failure.

EXTERNAL MIXER CORRECTION

The External Mixer Correction compensates for internal losses by measuring the EXTERNAL MIXER input signal level and calculating a correction value that is added to the reference level and marker amplitude readouts. An external 3.525 GHz, –40 dBm signal is connected to the EXTERNAL MIXER port before running the correction. Use a precision power meter to establish this level. The user should peak the on-screen amplitude by adjusting the generator frequency before beginning this correction.

This routine sets the instrument to an external mixer band and measures the signal level being applied to the EXTERNAL MIXER port. The instrument's gain distribution is then adjusted to produce an on-screen display. Several sweeps are averaged to determine the final signal level.

EXTERNAL MIXER CORRECTION ERROR MESSAGES

The following errors may occur during this part of the correction:

Signal Level Does Not Converge.
Signal no set to specified level. These two messages indicate that a signal was not found. They will be followed by one or more the following messages.

External Mixer Level Not Corrected.
Internal correction routine failed.
Refer to Self-Corr Appendix in Op Manual. Perform the following checks if any of these three messages occur:

1. Check the frequency and level of the signal generator.
2. Check all cables and connections (especially the cable located between the front panel EXTERNAL MIXER port and the A12 MTX assembly), then run the correction again.
3. If error messages persist, check the A12 MTX assembly for proper connections and replace if necessary.

DISPLAY SYSTEM DIAGNOSTICS

This section provides troubleshooting information for isolating faults within the Display System. This system contains the A20 Video Processor, A22 Display Amplifiers, A23 High Voltage, D24 Digital Storage, and Color Shutter modules.

VIDEO PROCESSOR TROUBLESHOOTING

This section provides a list of failure symptoms that indicate that the A20 Video Processor module may need to be replaced. Basic module operation can be verified by checking for input and output signals listed below. Connect the REF SIGNAL OUT to the RF Input and select these front panel settings, when measuring inputs and outputs:

FREQUENCY	100 MHz
SPAN	500 kHz
REF LEVEL	–20 dBm

VIDEO PROCESSOR INPUT SIGNALS

- LAVI+ (video) at A20 pin B17 is 60 mV/div.
- LAVI– (video) at A20 pin A17 is 60 mV/div;
- SWEEP+ at A20 pin A25 is 0 to +10 Volt ramp (SWEEP– is ground).

VIDEO PROCESSOR OUTPUT SIGNALS

- INTV+ (analog video) at A20 pin B21 is 60 mV/div.
- INTV– (analog video) at A20 pin A21 is 60 mV/div.
- INTH+ (analog sweep) at A20 pin B19 is 1.5 Volt ramp for normal display and 1.2 Volt ramp for menu displays.
- SDAV at A20 pin B11 is TTL-level, serial vertical data for digital storage displays.
- SDAH at A20 pin B12 is TTL-level, serial horizontal data for digital storage displays.
- PSG at A20 pin B8 is TTL-level, Sweep Gate signal.
- SDASE at A20 pin A12 is TTL-level pulse used to shift serial data onto the A24 Digital Storage module.
- SDAHSE at A20 pin A13 is a TTL-level pulse used to shift horizontal data onto the A24 Digital Storage module.

VIDEO PROCESSOR FAILURE MODES

NOTE

Always run the Peak Detector correction before replacing the module.

Switch Channel Not Selectable. Cannot select between the internal and external video sources.

General Circuit Failure. There is a straight, horizontal line somewhere on the display, usually at the top or bottom of the screen.

Video Filter Failure. When a Video Filter is turned on there is no change, or an inconsistent change, in the peak-to-peak height of the displayed noise, or the display becomes a straight horizontal line.

Gain or Offset DAC Failure. The Peak Detector Correction fails when calibrating the Minimum Peak Detector to match the Maximum Peak Detector.

Vin Multiplexor Failure. The noise floor peaks at some screen locations remain at the same value.

Analog Max/Min Detector Failure. Narrow pulses are not displayed at the correct amplitude in successive sweeps while in the Max/Min Acquisition Mode.

Clamp Circuit Failure. The real time signal cannot be adjusted, or the real time signal is a flat line at the bottom of the screen.

Vertical Real-Time Circuit Failure. Cannot adjust the real time gain and offset to match the digitized signal.

Serial Interface Chip Failure. An error is displayed on screen by the Microprocessor.

Decoding Circuit Failure. Not able to change acquisition modes, video filter, and so forth, from the front panel.

Horizontal Acquisition Failure. The sweep is not digitized and the Self-Correction routines fail.

Data Output Failure. On the display one axis of the digitized data remains stationary while the other axis moves with the incoming digitized data (if the vertical data failed and the horizontal axis would sweep normally and the vertical axis would remain stationary).

Acquisition Mode Failure. The display is not consistent with the expected display for the selected acquisition mode.

Horizontal Real-Time Circuit Failure. The real-time display does not sweep, does not appear on the screen, or the Horizontal Real-Time display gain and offset cannot be adjusted.

Compressed Real-Time Screen Failure. The display is compressed when it includes a real-time display and menu, or the display fails to compress when a menu is turned on.

DIGITAL STORAGE TROUBLESHOOTING

This section provides levels for the major input and output signals related to the A24 Digital Storage module. The typical symptom for a failure module is a disabled digitized display., but the real-time display is operational. This module also generates all CRT readouts, markers, the graticule, and Color Shutter control signals in addition to the Video Processor module's acquisition clock.

Basic Digital Storage module operation can be verified by checking for the signals listed below. Connect the REF SIGNAL OUT to the RF Input and select these front panel settings, when measuring module inputs and outputs:

FREQUENCY	100 MHz
SPAN	500 kHz
REF LEVEL	–20 dBm

DIGITAL STORAGE INPUT SIGNALS

- DAAV at A24 pin B11 is TTL-level, serial vertical data for digital storage displays.
- SDAH at A24 pin B12 is TTL-level, serial horizontal data for digital storage displays.
- SDASE at A24 pin A12 is TTL-level pulse used to shift serial data onto the module.
- SDAHSE at A24 pin A13 is a TTL-level pulse used to shift horizontal data onto the module.
- /DIGINH at A24 pin A7 is a TTL-level pulse used for Color Shutter timing.

DIGITAL STORAGE OUTPUT SIGNALS

- DSV (digitized video with graticule and readout) at A24 pin B3 is 1.5 Volt p-p centered around 0 volts.
- DSH (digitized sweep with graticule and readout) at A24 pin B5 is 1.5 Volts p-p centered around 0 Volts.
- ACQCLK at A24 pin A10 is a TTL-level signal that controls CRT blanking.
- BOD at A24 pin B2 is a TTL-level, hand-shaking signal that synchronizes Color Shutter switching.
- DIGBLANK at A24 pin A10 is a TTL-level signal that controls CRT blanking.
- DIGCLK at A24 pin A9 is a TTL-level, 4.608 MHz clock.
- DIGCOLOR at A24 pin A8 is a TTL-level signal that controls the Color Shutter switching between red (Low) and green (High).
- EOC at A24 pin A11 is a TTL-level signal that controls readout and trace display sequencing for analog displays.

LED INDICATORS

Eight red LEDs located at the top, right corner of the module provide a visual indicator that the Main Processor was able to reset the Digital Storage Register at power-up. Beginning from the left, the first three LEDs are normally off, the next four are turned on, and the last one is off (Figure 4-3). If the instrument fails to set up this LED pattern, a problem with the instrument bus or A24 Digital Storage module is indicated.

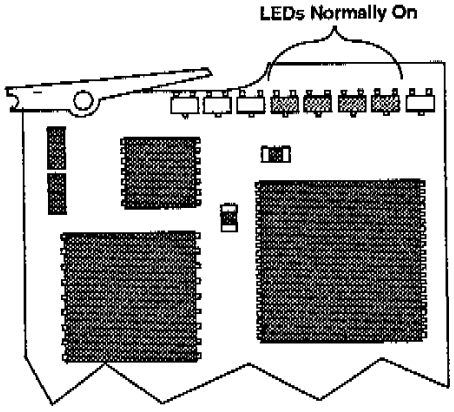


Figure 4-3. LEDs on the Digital Storage module.

DISPLAY AMPLIFIER TROUBLESHOOTING

This section provides levels for the major input and output signals related to the A24 Digital Storage module. This module drives the vertical and horizontal deflection plates of the CRT, and generates signals to control the CRT intensity level, focus and blanking. It also produces the Color Shutter drive signal. Refer to the ***Display Troubleshooting*** section in this manual for a list of failure symptoms that may be related to this module.

Basic Display Amplifier module operation can be verified by checking for the signals listed below. Connect the REF SIGNAL OUT to the RF Input, and select these front panel settings, when measuring module inputs and outputs:

FREQUENCY	100 MHz
SPAN	500 kHz
REF LEVEL	–20 dBm

DISPLAY AMPLIFIER INPUT SIGNALS

- DSV (digitized video with graticule readout) at A22 pin B3 is 1.5 Volts p-p centered around 0 Volts.
- INTV+ (analog video) at A22 pin B21 is 60 mV/div.
- INTV– (analog video) at A22 pin A21 is 60 mV/div.
- INTH+ (analog sweep) at A20 pin B19 is 1.5 Volt ramp for normal displays and 1.2 Volt ramp for menu displays.
- DSH (digitized sweep with graticule and readout) at A22 pin B5 is 1.5 Volts p-p centered around 0 Volts.
- PSG at A22 pin B8 is TTL-level Sweep Gate signal.
- BOD at A22 pin B2 is TTL-level, hand-shaking signal that synchronizes Color Shutter switching.
- DIGBLANK at A22 pin A10 is TTL-level signal the controls CRT blanking.
- DIGCLK at A22 pin A9 is a TTL-level, 4.608 MHz clock.
- EOC at A22 pin A11 is a TTL-level signal that controls readout and trace display sequencing for analog displays.

DISPLAY AMPLIFIER OUTPUT SIGNALS

- /DIGINH at A22 pin A7 is a TTL-level pulse used for Color Shutter timing control.
- COLOR+ at A22 pin A25 is a 45 Volt p-p signal (centered around 0 Volts) that controls Color Shutter switching between red (0 Volts) and green.
- ACFOC at A22 pin 12 is a –0.5 to +4.7 Volt p-p (centered at +2.5 Volt level), variable amplitude focus control signal for analog displays.
- DCFOC at A22 pin A22 is a 0 to 2 Volt DC, variable focus control signal for digitized displays.
- HDEF+ and HDEF–, +10 to +65 Volt horizontal deflection drive signals measured at first and second pins of harmonica connector on the left side of the module.
- VDEF+ and VDEF–, +10 to +65 Volt vertical deflection drive signal measured at the third and forth pins of harmonica connector on the left side of the module.
- VZ, +5 to +75 Volt p-p (variable with intensity) Z-Axis control signal measured at the seventh (orange wire) pin of harmonica connector on the left side of the module.
- TROT+ and TROT–, ±12 Volt DC level used to set race rotation, measured at 2-pin harmonica connector at upper left corner of module.

HIGH-VOLTAGE SUPPLY TROUBLESHOOTING

This section provides levels for the major input and output signals related to the A23 High-voltage Supply module. This module drives the anode, cathode, and control elements of the CRT. Basic High-voltage Supply module operation can be verified by checking for signals listed below.

WARNING

To avoid dangerous electrical shock, use extreme caution when measuring signals at the A23 High-voltage Supply module. Potentials in excess of 15 kV are present on this module.

The high-voltage charge on the anode lead can damage other circuits in this instrument. Be sure to fully discharge the anode lead to the main chassis by placing the leads against the chassis for at least five minutes.

An overvoltage protection circuit turns off the supply if the cathode potential exceeds –4715 Volts. This condition is indicated by a red LED (Figure 4-4) which turns on when the cathode potential is too high.

HIGH-VOLTAGE SUPPLY INPUT SIGNALS

- VZ, +5 to +75 Volts p-p (variable with intensity) Z-Axis control signal measured at the 3-pin harmonica connector (orange wire) located at the lower, left corner of the module.
- ACFOC at A22 pin B12 is a –0.5 to +4.7 Volt p-p (centered at +2.5 Volt level), variable amplitude focus control signal for analog displays.
- DCFOC at A23 pin A22 is a 0 to 2 Volt DC, variable focus control signal for digitized displays.

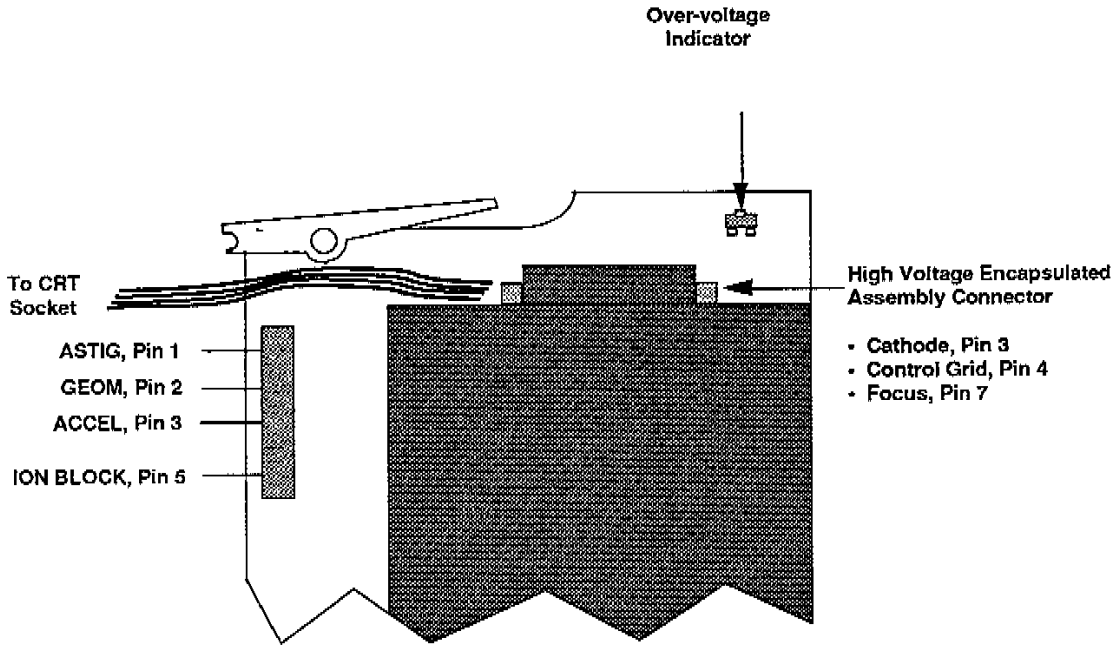


Figure 4-4. High-Voltage Supply module connectors and over-voltage indicator.

HIGH-VOLTAGE SUPPLY OUTPUT SIGNALS

- ASTIG, a 0 to +94 Volt, variable DC level that controls display astigmatism, measured at J10 pin 1 (white/purple wire).
- GEOM, a 0 to 95 Volt, variable DC level that controls display geometry, measured at J10 pin 2 (white/gray wire).
- ACCEL, a +50 Volt ±10% DC level for the accelerator grid, measured at J10 pin 3 (white wire).
- ION BLOCK, a +140 Volt ±20% DC level for CRT control, measured at J10 pin 5 (black/brown/white wire).
- –4450 Volt DC cathode supply, measured at pin 3 of high voltage encapsulated module connector (red/white/wire).
- –3150 to –3400 Volt variable DC focus potential (varies with focus control), measured at pin 4 of the high voltage encapsulated module connector (orange/white wire).
- –4450 to –4550 Volt variable DC control grid potential (varies with intensity control), measured at pin 7 of high voltage encapsulated module connector (yellow/white wire).

DISPLAY TROUBLESHOOTING

This section provides a list of common symptoms and probable causes for faults that are directly related to the CRT display.

Display Blank.	Over-Voltage shutdown condition in HV Power Supply. Check for illuminated red LED on A23 High Voltage module. Replace the A23 High Voltage module. Shorted +95 Volt secondary supply. Isolate and replace the defective module. Disconnected cable to CRT socket. Connect Cable. Z-axis IC failure. Replace the A22 Display Amplifier module. Faulty blanking input to Display Amplifiers. Check for TTL-level PSG signal from the A20 Video Processor module, and TTL-level signals BOD, EOC, DIGBLANK, and DIGCLK from A24 Digital Storage module. Replace the A20 Video Processor A22 Display Amplifier, or A24 Digital Storage modules as required.
No Color.	Disconnected or shorted cable to Color Shutter module. Repair or replace as needed. Color Shutter driver failure. Replace the A22 Display Amplifier module. No TTL-level DIGCOLOR signal. Replace the A24 Digital Storage module. Color Shutter failure. Replace Color Shutter module.
Color Smearing.	Color Shutter driver failing to send the TTL-level /DIGINH signal to the Digital Storage module. Replace the A22 Display Amplifier module. Digital Storage not responding to the /DIGINH signal. Replace the A24 Digital Storage module.
Display Out of Focus.	Failed Focus Amplifier on Display Amplifiers module. Replace the A22 Display Amplifier module. Failed Focus Amplifier on High Voltage Power Supply. Replace the A23 High Voltage module. High Voltage encapsulated assembly failure. Replace the A23 High Voltage module. Oscillation on Deflection Amplifier output. Replace the A22 Display Amplifier module.

Dot in Middle of Screen.	Shorted deflection/z-axis cable causing +85 V regulator to fold-back. Repair or replace cable. Deflection cable unplugged. Reinstall cables. Failed Deflection Amp/Z-axis IC causing +85 V regulator to fold back. Replace the A22 Display Amplifier module. Missing +95 Volt supply. Check for illuminated red LED on A5 Power Supply module. Replace the A5 LV Power Supply module or A5A2 Power Supply Secondary board.
Dot in Corner of Screen.	No Digital Storage deflection signals due to a consciously inhibited state. Check the TTL-level /DIGINH signal from the A22 Display Amplifiers module. Digital Storage display control program execution error. Replace the A24 Digital Storage module. Extreme overdrive of Deflection Amplifier inputs. Check DSV (1.5 V p-p for full screen) and DSH (2.5 V p-p) signals from A20 Video Processor module. Replace the A20 Video Processor or A22 Display Amplifiers modules.
Readouts Distorted or Missing.	Check for normal instrument control. If control is normal, replace the A24 Digital Storage module. If control is not normal check for faults on instrument data or control bus.
Insufficient Gain Range.	Both axes of display too small. HV Power Supply is in an over-voltage condition. Replace the A23 High Voltage module. Bot axes of display too large. HV Power Supply is in an under-voltage condition. Replace the A23 High Voltage module. Condition limited to one display axis. Check DSV (1.5 V p-p for full screen) and DSH (1.5 V p-p) signals from A20 Video Processor module. Replace the A20 Video Processor or A22 Display Amplifiers modules.
Distortion on Display.	Possible of Deflection Amplifier inputs. Check DSV (1.5 V p-p for full screen) and DSH (1.5 V p-p) signals from A20 Video Processor module. Replace the A20 Video Processor or A22 Display Amplifiers modules. +85 V regulator on Display Amplifiers going into current limit. Replace the A22 Display Amplifiers Module. Bit stuck on Digital Storage DAC (only affects digitized displays). Replace the A24 Digital Storage module. Oscillation on Deflection Amplifier outputs. Replace the A22 Display Amplifiers module.

FREQUENCY CONTROL DIAGNOSTICS

This section describes the frequency self-correction of the spectrum analyzer. Following the introductory information, each routine is described in detail. This consists of a summary of the actual routine, a description of the trace, a list of possible error messages, and troubleshooting procedures that apply to the error messages. The correction takes about four minutes to complete unless trace mode is active. The sequence requires more time in trace mode because data is sent to the terminal. Tests are performed in this sequence:

- CAL SWEEP Routine
- CAL 13 LO Routine
- CAL LO 129 Routine
- CAL YIG Routine
- CAL SWEEP OFFSET Routine
- CAL SPAN Routine
- CAL SPAN FM Routine
- CAL SPAN YIG Routine
- CAL TIME SWEEP Routine

NOTE

The frequency self-correction consists of nine routines which automatically run in order. This sequence always begins with CAL SWEEP and ends with CAL SWEEP TIME. It is not possible to begin the frequency self-correction at a point within the sequence.

SETTING UP THE FREQUENCY TRACE

Follow these steps to trace a frequency correction routine:

1. Install the Extender board, and enter keyboard mode (see Appendix B for instructions).
2. Enter the command:

   ftra +n

   when n is an argument from Table 4-15 that selects which step within the correction will be traced.
3. Enter the command:

   recl (Begins a correction cycle; could also be started manually from the UTIL menu)

The frequency self-correction begins immediately. Trace information will appear on the terminal screen as soon as the step for the selected trace begins. The following sections explain this trace data for each correction routine. They also provide descriptions of error messages and troubleshooting procedures for use when a correction sequence fails.

Multiple traces may be enabled during a frequency correction sequence to receive information on more than one parameter. For example, to receive reports on sweep and LO Low activity, enter the command:

ftra +sweep +lolo

then enter the command:

recl

to begin the trace.

Table 4-15. Keyboard arguments for frequency traces:

Argument	Syntax	Trace Information
lolo	ftra +lolo	Traces 10-16 MHz LO in A25 LO module
yig	ftra +yig	Traces A11 YIG-Tuned Oscillator (YTO)
count	ftra +count	Traces counter on A28 Period Counter module
span	ftra +span	Traces decade attenuator on A33 Sweep/Span Attenuator module
sweep	ftra +sweep	Traces sweep calibration on A33 Sweep/Span Attenuator module
29	ftra +29	Traces 29 MHz LO in the A16 VR module
pres	ftra +pres	Traces the preselector tracking calibration routine

To display a frequency trace, turn the instrument off and back on again or enter the command:

```
ftra -n
```

where n is the argument from Table 4-15 which was used previously to turn the trace on. Refer to the *General Diagnostics* section for more details.

LISTING OUT FREQUENCY CORRECTION DATA

After the frequency self-correction is complete, a summary of the resulting data may be listed out and examined by entering the command:

```
tabl
```

The terminal will display the following:

```
Enter command : tabl
GratSlope = 3.257295   GratOffset = 107.071548
LOloMin = 8.962605e+006 Hz    LOloMax = 1.703152e+007 Hz
LOloSlope = 8.132099e-001     LOlo_Offset = -7.347683e+006
LOlo DAC_Weight = 1623
LOlo_Slope_Factor =
    0      3.731383e-004      1.097582e+007
    1      3.061668e-003      1.270786e+006
    2      2.873771e-002      1.358750e+005
    3      2.852073e-001      1.364175e+004
Preselector
    Band   Slope  Offset
    1      1828   995
    2      1836   976
    3      1782   2704
    4      1716   1080
YIGMin = 6.638937e+009 HzYIGMax = 2.106364e+010 Hz
YIGSlope = 4.877195e.004 YIGOffset = -3.237939e+006
```

```
YIG_Span_Factor =
    0      3.590189e-007              1.140748e+010
    1      3.595464e-006       1.139074e+009
    2      3.714492e-005       1.133078e+008
FM_Span_Factor =
    0      7.150907e005 6.658368e+007
    1      6.159944e-004       7.748599e+006
    2      7.192544e-003       7.713599e+005
LO129Mix = 1.270771e+008 Hz
LO129Max = 1.314070e+008 Hz
LO129Step = 2.707823e+005 Hz
10129 freqDAC    DAC slope
1.270761e+008    0      0.000904
1.273459e+008    f4     0.000897
    .      .      .
    .      .      .
1.3027i2i+008    db9    0.0011057
1.3111359e+008   ed7    0.001092
SweepOffsetSlope + 0.174494  SweepOffsetOffset  =  35.603642
TimeRange  min time (Sec)
    0      2.36238.e+001
    1      2.703265e+000
    2      2.964390e+001
    3      4.091900e+002
    4      4.782346e+003
    5      5.134642e+004
    6      6.719834e-005
    7      7.689480e+007
    8      8.43.255e+007
```

GratSlope and **GratOffset** are results of the CAL SWEEP routine. The following three lines list the CAL 13 LO results. **LOlo_Span_Factor** lists the LO Low Span factors determined during the CAL SPAN routine. **0** is +1, **1** is +10, **2** is +100, and **3** is +1000. The **Preselector data (Band, Slope**, and **Offset)** are results of the PRESELECTOR TRACKING routine. **YIGMin, YIGMax, YIGSlope**, and **YIGOffset** are the YTO frequency extremes and calibration results from the CAL YIG routine. **YIG_Span_Factor** and **FM_Span_Factor** are the YTO decade attenuator calibration data established during the CAL YIG and CAL SPAN FM routines, respectively. 0 is +1, 1 is +10, 2 is +100. Lines that begin with **LO129** are CAL 129 routine results indicating the 129 MHz LO characteristics. **LO129 freq**, and the following data is a list of sixteen 129 MHz LO frequency steps and their corresponding DAC values. **SweepOffsetSlope** and **SweepOffsetOffset** are results from the CAL SWEEP OFFSET routine and **TimeRange min time (Sec)** is a summary of the CAL SWEEP TIME routine results.

NOTE

The PRESELECTOR TRACKING routine is a separate sequence used when adjusting the instrument's frequency response. Although data from this routine is listed by the tabl command, PRESELECTOR TRACKING does not run when the frequency self-correction sequence is invoked.

CAL SWEEP ROUTINE

To begin the first of nine routines, the instrument display indicates

CAL SWEEP

This routine establishes marker DAC values that equate to specific sweep positions. A marker DAC on the A33 Sweep/Span Attenuator module is set to a series of sequential values, and the resulting screen position for each value is measured and reported by the A20 Video Processor module. Using the resulting calibration table, the Main Processor can calculate the DAC value needed to produce any specific on screen position.

This is the first of nine frequency self-correction routines so trace data appears immediately on the terminal. The trace consists of a list of marker and screen values. Following the list are the measurement conclusions. The routine is complete when CAL 13 LO appears on the instrument screen. The trace, enabled by **ftra +sweep**, looks like this:

```
Enter command : ftra +sweep
FreqTraceEnable = 0001

Enter Command  :  recl
CalibrateSweep
sweep      reg   105    sweep DAC    448
sweep      reg   159    sweep OAC    623
sweep      reg   213    sweep DAC    798
sweep      reg   266    sweep DAC    973
    .      .     .
    .      .     .
sweep      reg   802    sweep DAC    2723
sweep      reg   856    sweep DAC    2898
sweep      reg   909    sweep DAC    3073
sweep      reg   973    sweep DAC    3248
    GrtSlope + 3.265339 GrtOffset = 103.540543
```

CalibrateSweep indicates when the CAL SWEEP routine is being performed. **sweep reg** is the horizontal screen location; this screen has 1000 points where the left graticule is point 0 and the right graticule is point 1000. **sweep DAC** is a Marker DAC value that generates the corresponding sweep position. The trace concludes with the calculated sweep offset slope (**GratSlope**) and sweep offset offset (**GratOffset**).

CAL SWEEP ERROR MESSAGES

The following errors may occur during this part of the correction:

Display Position Does Not Converge. The A24 Digital Storage module was unable to determine the sweep position. The routine continues with the next sample despite the error message.

Sweep Position Slope Out Of Range. The Sweep Position Slope deviates more than 10.7% from the desired value of 3.2777. The routine continues with the next measurement despite the error message.

Sweep Position Offset Out Of Range. The Sweep Position Offset deviates more than 16.9% from the desired value of 101.6112. The routine continues with the next measurement despite the error message.

Sweep Position Correction Terminated. Not enough samples could be collected to properly calculate the sweep position. Span calibration will not be performed.

CAL SWEEP TROUBLESHOOTING PROCEDURE

Failures detected during this step indicate the instrument is unable to produce, calibrate, or digitize a horizontal sweep signal. These errors are typically due to faults in the A33 Sweep/Span Attenuator, A20 Video Processor, or A24 Digital Storage modules. Perform the following steps to isolate the defective module:

1. Use an oscilloscope to measure the SWEEP+ signal at pin A25 and the SWPGATE signal at pin A22, of the A33 Sweep/Span Attenuator.

   - SWEEP+ should be a 10 Volt p-p, positive going ramp ranging from 0 to +10 Volts.
   - SWPGATE should be a TTL-level pulse that is High during sweep and Low during holdoff.
   - Replace the A33 Sweep/Span Attenuator module if these signals are weak or missing.

2. Monitor the SWEEP+ signal at pin A25 and the A33 Sweep/Span Attenuator with an oscilloscope while running the CAL SWEEP portion of the frequency self-correction routine.

   - The signal should be 0 Volts DC level that increases to +10 Volts in a series of steps, then returns to about +5 Volts.
   - Replace the A33 Sweep/Span Attenuator module if the sweep voltage fails to change levels or return to +5 Volts.

3. Measure the SDAH signal at pin B12 on the A20 Video Processor.

   - SDAH is a TTL-level pulse string that provides the Digital Storage circuit with analog sweep location data. The pulse string period is proportional to the sweep rate.
   - Replace the A20 Video Processor module if SDAH is weak or missing, and the correct signals from steps 1 and 2 are measured.

4. Replace the A24 Digital Storage module if correct signals from steps 1, 2, and 3 are measured.

CAL 13 LO ROUTINE

To begin the second of nine routines, the instrument display indicates

CAL 13 LO

This routine calibrates the 10.1 MHz to 16.1 MHz LO low oscillator (nominally 13 MHz), which is part of the First Local Oscillator Phaselock Loop.

The routine begins by setting the sweep to center screen and the span attenuator DAC on the Sweep/Span Attenuator to 0 (+1). Next the coarse and fine tuning DACs in the A25 LO module are set to a series of combinations that produce frequencies that are measured to determine the minimum and maximum oscillator frequency, and the slope, offset, and relative weight of each DAC.

This is the second of nine frequency self-correction routines, so trace data appears within a few seconds on the terminal. The trace consists of a summary of the measurement, followed by continuous iterations of LO Low activity. The routine is complete when CAL 129 LO appears on the instrument screen. The trace enabled by **ftra +lolo**, looks like this:

```
Enter command : ftra +lolo
FreeTraceEnable = 0010
Enter Command : recl
Set_LOlo (14457325, 5000.00)
    precision + 4828.000000
    CountPeriods = 17
MinCount = 29001932
MaxCount = 29021309
hiDAC      IoDAC Delay PeriodFrequency
Oacl       07e5  0     29012480     14456896
MakeLOloTable
    hi fine free =          1.312839ee+007 Hz
    lo fine free =          1.312363e+007 Hz
    hi coarse free =   1.553462e+007 Hz
    lo coarse free =   1.067218e+007 Hz
    min free =         9.208732e+006 Hz
    max free =         1.689380e+007 Hz
    center free =           1.312602e+007 Hz
    LOloMin +    9.208732e+006
    LoloMax =    1.689380e+007
    LOloSloFe =  8.604281e+001
    LOloOffset = -7.945516e+006
    Lolo_DAC_Weight = 1634
    .      .      .
    .      .      .
```

`Set_LOlo` indicates when this routine begins, including its target LO frequency (`14457325`) and precision (`5000.00`) in Hz. The following lies indicate the mincing number of count periods (`16`) required to achieve the desired precision, and the actual precision (`4828.00`) `MinCount` and `MaxCount` are the actual count periods recorded when the LO is set to its extremes. `hiDAC` and `LODAC` are the coarse and fine tune DAC settings that produce an LO `Frequency`. `Delay` is the number of software delay intervals between measurements, and Period is the number of 100 MHz reference cycles recorded during the measurement. `MakeLOloTable` is a summary of the LO Low frequency tune DAC parameters. `LOlo_DAC_Weight` is the number of fine tune DAC bits required to change the LO frequency an amount equal to the frequency an amount equal to the frequency change that results when the coarse DAC is incriminated by one LSB.

Following this summary, the trace continues to record LO Low activity during subsequent routines.

CAL 13 LO ERROR MESSAGES

The following errors may occur during this part of the correction:

LO Low Will Not Tune Low Enough. The LO Low oscillator will not tune to the minimum frequency, which is 10.1 MHz. The firmware continues with the next measurement despite the error message.

LO Low Will Not Tune High Enough. The LO Low oscillator will not tune to the maximum frequency, which is 16.1 MHz. The firmware continues with the next measurement despite the error message.

LO Low Tune Slope Out Of Range. The LO Low oscillator tune offset value deviates more than 20% from the desired value of –0.8649. The firmware continues with the next measurement despite the error message.

LO Low Tune Offset Out Of Range. The LO Low oscillator tune offset value deviates more than 30% from the desired value of –8.087E6. The firmware continues with the next measurement despite the error message.

LO Low DAC Weight Out Of Range. The LO Low oscillator fine-tune DAC weight deviates more than 12% from the desired value of 1650. The firmware continues with the next measurement despite the error message.

LO Low Tuning Correction Terminated. Report To Qualified Service Person. The firmware failed to calibrate the tune curve for the LO Low oscillator. YTO (YIG Tuned Oscillator) and Span calibrations will not be performed.

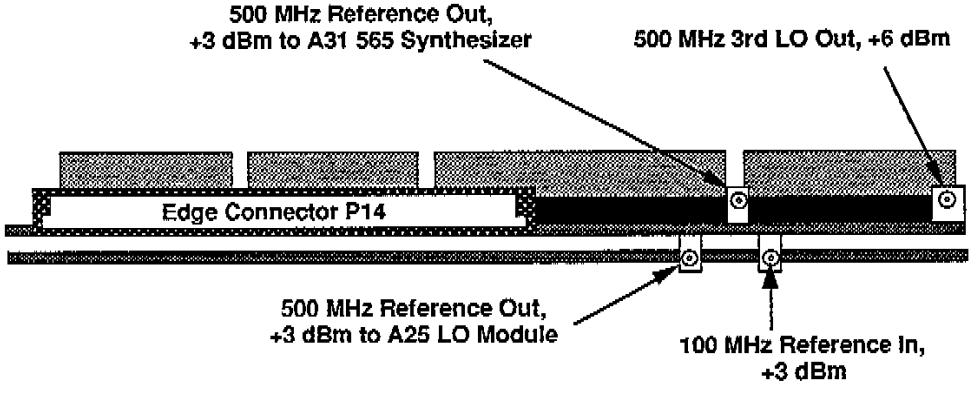


Figure 4-5. A28 Period Counter module connector locations (bottom view of module).

CAL 13 LO TROUBLESHOOTING PROCEDURE

Failures detected during this step indicate the instrument is unable to calibrate the 10.1 to 16.1 MHz LO Low signal. These errors are typically due to faults in the A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter. Perform the following steps to isolate the defective module:

1. To isolate the A28 Period Counter enter this command:

   lo29 1024

   The terminal should respond with the 29 MHz LO frequency.

   - Measure the +3 dBm, 100 MHz Reference period Counter input (Figure 4-5) if the terminal fails to respond with the 29 MHz LO frequency.
   - Replace the A29 Reference Oscillator module if the 100 MHz Reference is weak or missing, and replace the A28 Period Counter module if the 100 MHz signal is present.

2. If step 1 operates correctly enter the command:

   lolo

   - The terminal will respond with the current LO Low frequency, which must be within the 10.1 MHz to 16.2 MHz range.
   - If the count is outside the 10.1 MHz to 16.1 MHz range, replace the A25 LO module.
   - If no count is returned, proceed to the next step.

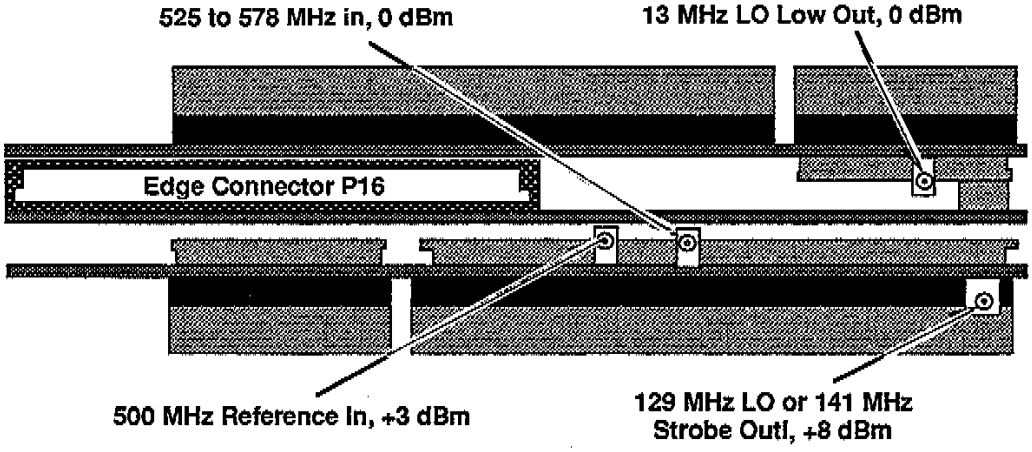


Figure 4-6. A25 LO module connector location (bottom view of module).

3. Use an oscilloscope to measure the FREQSWP+ signal at pin B19 of the A25 LO module.

   - FREQSWP+ is a positive-going sweep ramp, centered around 0 Volts, that changes amplitude with Frequency Span settings. This ramp combines with decade attenuator steps to set the span. Normal range is about 10 Volts p-p to 200 mV p-p at 10 Hz Frequency Span
   - Replace the A33 Sweep/Span Attenuator if the FREQSWP+ signal is faulty or missing.
   - Replace the A25 LO module if the FREQSWP+ signal is correct.

4. Measure the LO Low amplitude (0 dBm) and exercise the oscillator tuning circuit:

   - Connect a spectrum analyzer to measure the 0 dBm, LO Low output on the A25 LO module (Figure 4-6)
   - Enter keyboard mode and enter the command:

     slol 10.1e6 100

     to set the LO Low frequency to 10.1 MHz. The frequency change should be measured by the test spectrum analyzer.

   - Enter the command:

     slol 16.1e6 100

   to set the LO Low frequency to 16.1 MHz. The frequency change should be measured by the test spectrum analyzer. Replace the A25 LO module if the LO Low amplitude is less than 0 dBm, or if the LO fails to tune.

CAL 129 LO ROUTINE

To begin the third of nine routines, the instrument display indicates

CAL 129 LO

This routine checks the range of the 129 MHz LO located within the A25 LO module and determines tune DAC settings that divide the total LO tune range into sixteen equal steps.

To begin this routine tune DAC is alternately set to its extremes, producing the 129 MHz oscillator's minimum and maximum frequencies. From these measurements, sixteen intermediate tuning steps are calculated to construct a tune table. A DAC value for the first intermediate tune step is then implemented followed by a count of the resulting 129 MHz LO frequency. The tune DAC value is then adjusted and the resulting frequency counted until the tune step is calibrated. This process is repeated for each intermediate step until all sixteen have been calibrated.

This is the third of nine frequency self-correction routines, so trace data appears n the terminal within approximately 12 seconds. The trace consists of the measured minimum and maximum 129 MHz LO frequencies, followed by sixteen groups of tune DAC values and their resulting frequencies. Each group represents the adjustment of one tune step. The routine is complete when CAL YIG HI DAC MID F appears on the instrument screen. The trace enabled by **ftra +129**, looks like this:

```
Enter command  :  ftra  +129
FreqTraceEnable  =  0040

Enter Command  : recl
Make129Table
          1.313375e+008  fff
          1.269972e+008 000
          LO129Min = 1.269972e+008 Hz; LO129Max = 1.313375e+008 Hz
          frequency    DAC
          1.272881e+008      Off
          1..72678e+008      Oed
--> 1.272685e+008 0ed

          1.275404e+008      ldb
```

```
-> 1.275397e+008 1db

          1.278115e+008      2c7
-> 1.278110e+008 2c7
     .      .      .
     .      .      .
          1.305162e+008      c88
          1.305231e+008      c8f
-> 1.305237e+008 c8f

          1.307860e+008      da1
          1.307947e+008      daa
-> 1.307949e+008 daa

          1.310569e+008      ec5
          1.310660e+008      ecf
-> 1.310762e+008 ecf

Prelock_LO129
```

Make129Table indicates when the routine begins. **LO129Min = 1.269972e+008 Hz** and **LO129Max = 1.313375e+008 Hz** are the measured frequency extremes of the LO for tune DAC settings of **000** and **fff**, respectively. The following groups of frequency and DAC settings are iterations used to calibrate each intermediate tune step. An arrow (—>) highlights the fine settings for each tune step. The routine concludes by tuning off the 129 MHz LO using the **Prelock_129** statement.

CAL 129 LO ERROR MESSAGES

The following errors may occur during this part of the corrections:

129 MHz Tuning Correction Terminated. Report To Qualified Service Person. The firmware failed to calibrate the tune curve for the 129 MHz oscillator. This usually indicates a failure to count the oscillator frequency.

129 MHz Tuning Range Unknown. Report To Qualified Service Person. The measured tuning range of the 29 MHz oscillator is incorrect. The problem is most likely the A25 LO Module.

CAL 129 LO TROUBLESHOOTING PROCEDURE

Failures detected during this step indicate that the instrument is unable to measure the 129 MHz LO frequency or control its tuning DAC. These errors are typically due to faults in the A25 LO Module or A28 Period Counter. Perform the following steps to isolate the defective module:

1. Refer to the *CAL 13 LO TROUBLESHOOTING PROCEDURE* located earlier in this section for a procedure to isolate the A28 Period Counter.

2. If the period counter is functional, measure the 129 MHz LO frequency with this command:

   f129

   - The terminal should return the 129 MHz LO frequency, which must be within the 128 MHz to 130 MHz range. Replace the A25 LO module if the frequency is outside of this range.

3. Use a test spectrum analyzer to measure the A25 LO module inputs:

   - Check for a 500 MHz, +3 dBm input from the A28A1 X5 Multiplier (part of the A28 Period Counter module). See Figure 4-6 for the test point location. This 500 MHz signal is generated by the A29 Reference Oscillator, and is routed through the A28 Period Counter module to the A25 LO module.
   - Begin the frequency self-correction routine while measuring the 565 MHz input to the A25 LO module (Figure 4-6). Check for a 0 dBm signal that sweeps slowly from 578 MHz to 525 MHz.

4. Connect a test spectrum analyzer to the 129 MHz LO Out port (Figure 4-6) to check the 129 MHz LO amplitude and tune control circuitry:

   - Normal amplitude is about +8 dBm; replace the A25 LO module if weak or missing.
   - To check the tune control circuit, enable keyboard mode and enter this command:

     s129 128e6

   The LO frequency should change to 128 MHz.

   - Enter the command:

     s129 130e6

   The LO frequency should change to 130 MHz.

   - Replace the A25 LO module if the 129 MHz LO fails to tune properly.

CAL YIG ROUTINE

To begin the fourth of nine routines the instrument display indicates:

CAL YIG HI DAC MID F

This routine determines the A11 YIG Tuned Oscillator (YTO) tuning curve, producing a calibration table that indicates which coarse-tune DAC and fine-tune DAC settings are required to generate specific YTO frequencies. This routine is only invoked if the CAL 13 LO routine is successful.

Several measurements are performed using a tunable, 138 to 145 MHz Strobe signal produced by the A31 565 MHz Synthesizer and A25 LO modules. This Strobe is locked to the LO Low oscillator signal, so its frequency changes as the LO Low Oscillator is tuned. During this routine the Strobe and YTO signals are applied to a harmonic mixer to produce beat frequencies (difference between YTO and nearest Strobe harmonic) that are counted to determine the strobe harmonic number N. Once N is determined, the firmware uses the beat frequencies to determine the YTO frequency:

YTO frequency = (Strobe x N) + Beat Frequency

A subroutine called FindYIG verifies which Strobe harmonic (N) is producing the beat frequencies. During the FindYIG process, the Strobe frequency is changed and the resulting beat frequency is measured. Because the beat frequency is directly related to the frequency of the Strobe harmonic, changes to the Strobe frequency will produce a proportional change to the beat frequency. For instance, if the Strobe frequency is changed by 1 kHz, a 10 kHz change to the beat frequency will result when mixing on the tenth harmonic. In this example, the beat frequency produced when mixing with the ninth harmonic would change 9 kHz.

To begin this routine, the YTO tune DACs located within the A25 LO module are set to mid-range and the resulting frequency is measured. Next the coarse tune DAC increases the YTO frequency by approximately 100 MHz and the resulting frequency is measured. From the measurement in this and the previous step, the approximate slope of the tune curve is determined.

Next the YTO frequency is set to 16.5 GHz (based upon the approximate tune curve slope), then to 9.5 GHz, and for each setting the resulting frequency is measured. These two measurements are sued to determine the tune curve of the coarse tune DAC.

After setting the coarse tune DAC to mid-range and the fine tune DAC to maximum, the resulting frequency is measured. Next the fine tune DAC is set minimum and the resulting frequency determined. Using all of these measurements, the Main Processor calculates the YTO maximum frequency, minimum frequency, frequency range, tuning slope, tuning offset, and DAC weight.

This is the forth of nine frequency self-correction routines, so trace data appears on the terminal within approximately 15 seconds. FindYIG routines are performed for each frequency setting of the YTO, producing a trace that contains a report of the iterations required to set the YTO frequency. The routine is completed when CAL SWEEP OFFSET appears on the instrument screen. The trace is enabled by **ftra +yig**. A sample of this repetitive trace that includes a complete FindYIG sequence looks like this:

```
Enter command : ftra +yig
FreqTraceEnable = 0080

Enter Command : recl
Set_YIG (1.327500e+010)
    dacoffset = -12670
    Strobe =  1.426075e+008
    Target Beatnote =  12.500
hiDAC     IoDAC Delay Beatnote
0743      0349  0           12.962
0741      0a56  2           12.614
MakeYlGTable
FindYIG (1.325000e+010)
    traceSize = 92

Set Strobe CoDnt Strobe CoDnt Beat   i     d     statcs
143.450000 143.449976   0.000       0     0
143.395548 143.395547   0.000       0     0
143.341095 143.341112   0.000       0     0
143.286643 143.286744   0.000       0     0
143.232190 143.232219   0.000       0     0
143.177738 143.177729   0.000       0     0
143.123285 143.1.3300   0.000       0     0
143.078833 143.078816   0.000       0     0
143.014380 143.014397   0.000       0     0
142.959928 142.959908   0.000       0     0
14..905476 142.905474   0.000       0     0
142.851023 142.851046   0.702       0     0
142.796571 142.797564   27.685      0     0
142.742118 142.74.140   22.723      0     0
142.787666 142.687757   17.768      0     0
142.733213 142.733232   12.820      1     0
142.578761 142.578745   7.B7B       2     0
142.524308 142.5.4324   2.913       3     0
142.469856 142.469834   2.043       4     0
142.415404 142.415408   6.993       5     0
142.370951 142.360979   11.944      0     1     x
141.271902 141.271908   17.201      0     1
141.217450 141..17438   25.2.6      0     1
141.162997 141.173011   20.215      0     1
141.108545 141.108514   15.192      1     1
141.054092 141.054095   10.180      2     1
140.999740 140.999655   5.174       3     1
140.945188 140.945185   0.000       4     1
140.890735 140.890756   4.842       5     1
140.836283 140.836276   9.854       0     2     x
```

```
    strobe1 = 1.427332e+008 Hz; beat1 = 1.282043e+007 Hz
    strobe2 = 1.411085e+008 Hz beat2 = 1.519231e+007 Hz
    delta fnYIG =  0.98
    fnYIG =  90.99
    YIG free =  1.297780e+010 Hz
dflt slope = 3.216713e+007; offeet =  -2.128435e+003
FindYIG (1.30668e+010)
    tracesize + 100
    .     .     .
    .     .     .
```

To begin this routine, a **Set_YGI** routine attempts to set the YTO frequency to 13.275 GHz. The coarse and fine-tune DACs (**dacOffset + –12660**) are set to values that will produce a Beatnote frequency near the **Target Beatnote = 12.500 MHz** when mixed with the harmonic of the Strobe (**1.426075e+800**). The YTO frequency is then fine-tuned with new tune DAC values until the resulting Beatnote is within limits. Delay indicates how many 4 ms waiting periods are required for tune setting before a measurement is attempted. This value is logarithmically proportional to the YTO frequency step, increasing for larger frequency changes.

MakeYIGTable automatically begins the **FindYIG** routine, which determines the YTO frequency when it is not known. **FindYIG** generates a table that indicates when two valid Strobe frequencies are located. This table records data as a series of Strobe signals (**Set Strobe**) are mixed with the YTO signal. Each Strobe frequency is counted (**Count Strobe**) for increased precision. The resulting Beatnotes are then counted (**Count Beat**). Results are recorded in columns labeled **i, j,** and **status. traceSize = 92** is the maximum number of Strobe frequencies that may be used before a failure is indicated.

The number **1** appears in the **i** column when a Beatnote frequency falls within certain limits. The next four Strobe frequencies are then set to produce predictable Beatnote frequencies, and are recorded by listing **2, 3, 4** and **5** in the **i** column if the resulting Beatnotes are within expected limits. This process identifies which harmonic of the Strobe is mixing with the YTO so the YTO frequency may be calculated. A **1** appears in the column when a group of five valid Beatnotes are recorded. An **x** also appears in the **status** column to indicate that a valid Strobe setting has been established. This process is repeated a second time on the next Strobe harmonic to verify the measurement results, producing a **2** in the **j** column. An **a** or **b** in the **status** column indicates an invalid Strobe setting when a group of five Strobes do not produce the expected Beatnote frequencies.

The **FindYIG** routine concludes by listing the Strobes (**strobe1** and **strobe2**) and Beatnote frequencies (**beat1** and **beat2**) that were first in each grouping. **delta fnYIG** is a number close to 1; significant deviation indicates an unstable Strobe or YTO signal. **fnYIG** is the Strobe harmonic used for mixing; deviation from an integer value also indicates an unstable Strobe or YTO signal. The actual YTO frequency is then listed (**YIG freq = 1.296680e+010 Hz**), followed by the tune DAC settings.

The **Set_YIG** and **FindYIG** routines are repeated for each YTO frequency as the YTO tuning curve is determined.

CAL YIG ERROR MESSAGES

The following errors may occur during this part of the correction:

YTO DAC Weight Out Of Range. The YTO DAC weight deviates more than 12% from the desired value of 1783. The firmware continues with the next measurement despite the error message.

YTO Tune Slope Out Of Range. The YTO tune slope deviated more than 25.5% from the desired value of 5.1945E–4. The firmware continues with the next measurement despite the error message.

YTO Tune Offset Out Of Range. The YTO tune offset deviates more than 24.1% from the desired value of –3.6955E6. The firmware continues with the next measurement despite the error message.

YTO Tuning Correction Terminated. Report To Qualified Service Person. The firmware failed to calibrate the tune curve for the YTO. The problem results from failure to determine the YTO frequency. Span calibration will not be performed.

LO Low Will Not Set. The firmware was unable to set the LO Low oscillator (nominally 13 MHz) to a frequency that allows the Strobe to be set as needed. to produce beat notes. Repeated failures will result in termination of the entire YTO tuning correction routine. Refer to ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure.

CAL YIG TROUBLESHOOTING PROCEDURE

Most failures detected during this step indicate the instrument is unable to count or calibrate the tune range of the A11 YTO. These errors are typically due to faults in the A11, YTO, A11A2 YTO Driver, A17 Microwave Phase Lock, A32 565 MHz Synthesizer, A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter. Perform the following steps to isolate the defective module:

1. Refer to the ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate the A28 Period Counter and A33 Sweep Span/Attenuator modules, and replace as needed.

2. Check the Main Coil Spans (>50 MHz) sweep and tune volts signals from the A25 LO module:

   - Set the SPAN to 100 MHz and use an oscilloscope to check for a 50 mV p-p ramp at A25 pin A25 (LODR+). This ramp increases to about 2.5 Volts p-p as the SPAN increases to 6.5 GHz. Replace the A25 LO module if the sweep is missing or distorted.
   - Measure the LODR– signal (Center Frequency Tune Voltage) with a volt meter at A25 pin A24. This voltage should change from –2.4 Volts at 0 MHz CENTER FREQUENCY to –4.2 Volts at 6.5 GHz CENTER FREQUENCY. Replace the A25 LO module if missing.

3. Measure the Main Coil Spans (>50 MHz) drive signal to the A11 YTO module:

   - Set the CENTER FREQUENCY to 0 MHz and measure the DC voltage at pin 10 (white wire) of the A11 YTO ribbon cable. Voltages of +1.9 Volts at 0 MHz CENTER FREQUENCY and +3.1 Volts at 6.5 GHz CENTER FREQUENCY should be present. Replace the A11A2 YTO Driver if this voltage does not change with CENTER FREQUENCY settings.
   - Set the SPAN to 6.5 GHz and measure the sweep ramp at pin 10 of the A11 YTO ribbon cable. This ramp should measure about 1.8 Volts p-p, and change DC level as the FREQUENCY control is rotated. Replace the A11A2 YTO Driver if the ramp is not present.

4. Connect a test spectrum analyzer to the front panel LO OUTPUT connector and measure the A1 YTO frequency and amplitude. The frequency is 10.025 GHz at 0 MHz CENTER FREQUENCY and 16.525 GHz at 6.5 GHz CENTER FREQUENCY. Amplitude is approximately +10 dBm.

NOTE

The YTO signal is applied to the A17 Microwave Phaselock module by a separate cable. If the YTO cannot be counted, check for the YTO signal at the A17 modules input.

- Check for a +18 Volt DC level at pin 4 (yellow wire) of the A11 YTO ribbon cable.
- Replace the A11 YTO if drive signals are present but the output frequency is incorrect or weak.

5. Refer to the *CAL 129 LO TROUBLESHOOTING PROCEDURE* located earlier in this section for a troubleshooting procedure to isolate the A25 LO module, and replace as needed.

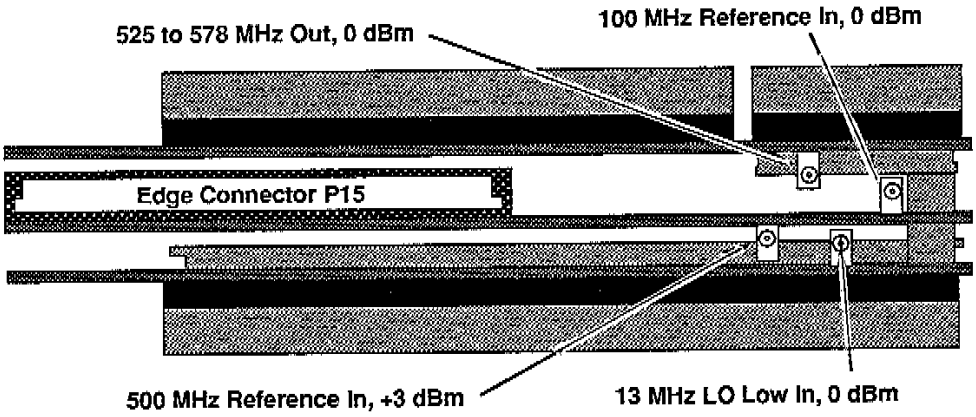


Figure 4-7. A31 565 MHz Synthesized module connector locations.

6. Check the A31 565 MHz Synthesizer module performance:
   - Connect a test spectrum analyzer to the 565 MHz output (Figure 4-7). Set the 565 MHz CENTER FREQUENCY, 5 MHz SPAN/DIV, and 0 dBm REF Level.
   - Enable keyboard mode and enter the command:

     fyig 13e9

   - A 0 dBm signal should appear on the test spectrum analyzer display. The signal frequency will sweep slowly from 578 MHz to 552 MHz as the instrument attempts to set the YTO frequency.
   - Replace the A32 565 MHz Synthesizer module if the signal is weak or missing.
   - Check for proper module inputs if the 565 MHz signal does not tune. Use a test spectrum analyzer to measure 100 MHz (+0 dBm) and 500 MHz (+3 dBm) references from the A29 Reference Oscillator module. Refer to step 1 to measure the LO Low input signal.

7. To check the A17 Microwave Phaselock module, measure the TTL-level PLLPC signal at pin B11 on the A28 Period Counter module. This is the beat frequency (difference between the YTO and nearest 141 MHz Strobe harmonic, up to 25 MHz) divided by 32.
   - Connect an oscilloscope to pin B11 on the A28 Period Counter module.
   - Run the frequency self-correction routine. The PLLPC line should be active whenever the YTO is counted (during CAL YIG, CAL SPAN, and so forth).
   - Check for 141 MHz Strobe and YTO inputs at the A17 module using steps 4 and 5. Replace the A17 Microwave Phaselock module if PLLPC is missing when input signals are present.

CAL SWEEP OFFSET ROUTINE

To begin the fifth of nine routines, the instrument display indicates

CAL SWEEP OFFSET

This routine establishes sweep offset DAC (located within the A33 Sweep/Span Attenuator module) values so the sweep may be positioned anywhere on the screen. During this routine, the LO Low oscillator is used as a voltage-to-frequency converter so each sweep offset DAC setting can be measured. Each time the sweep offset DAC is incriminated, the LO Low frequency is counted. The marker DAC is then used to return the sweep voltage, and thus the LO Low frequency, to the previous value.

To begin this routine the LO Low frequency is measured with the tune DACs at center value and the FREQSWP+ line at 0 volts. This LO Low frequency is the target value for subsequent measurements. The marker DAC and sweep offset DAC are then set to 0. The sweep offset DAC is then incriminated, followed by a count of the LO Low frequency. To complete the first measurement, the marker DAC is adjusted by using a successive approximation method to zero the FREQSWP+ signal, returning the LO Low to its target frequency. The sweep offset DAC is incriminated again, and this process repeats for each sweep offset DAC setting until the marker DAC exceeds its range.

Marker DAC values that could be used to successfully adjust the FREQSWP+ signal to zero are used to relate the sweep offset DAC values to the horizontal sweep position. The calculated slope and offset are stored to represent Sweep Offset Slope and Sweep Offset Offset. At the conclusion of this routine, the marker DAC is set to center the sweep on the screen.

This is the fifth of nine frequency self-correction routines. Trace data appears on the terminal within approximately 30 seconds, listing the comparison of offset, marker, and screen values set by the routine. The routine is complete when CAL SPAN appears on the instrument screen. The trace, established by **ftra +sweep,** looks like this:

```
Enter command : ftra +sweep
FreqTraceEnable = 0001

Enter Command : recl
Set_YIG (1.327500e+010)
    .       .       .
    .       .       .
sweep reg 909    sweep DAC    3073
sweep reg 963    sweep DAC    3248
          GratSlope = 3.275339 GratOffset = 103.540543
CalibrateSpan
    zero span LOlo = 13305438
Offset    Marker Screen
    32    31     -22.22
    33    72     -12.72
    34    77     -8.13
    35    100    -1.08
    36    115    3.51
    .     .      .
    .     .      .
    247   4046   1207.37
    248   4077   1.16.86
    249   4092   1221.45
SweepOffsetSlope = 0.174904        SweepOffsetOffset = 35.419144
```

Set_YIG, GratSlope, and **GratOffset** are results from previous steps within the **+sweep** trace. **CalibrateSpan** indicates when the CAL SWEEP OFFSET routine begins. **zero span LOlo** is the target LO Low frequency. **Offset, Marker,** and **Screen** are the sweep offset DAC and marker DAC values, and their corresponding screen locations with reference to the 1000 point horizontal axis. Negative screen values indicate sweep positions that extend beyond the left edge of the screen, while values greater than 1000 extend beyond the right graticule. **SweepOffsetSlope** and **SweepOffsetOffset** are the calculated slope and offset values.

CAL SWEEP OFFSET ERROR MESSAGES

The following errors may occur during this part of the correction:

Sweep Offset Offset Out Of Range. The sweep offset offset deviates more than 33.5% from the desired value of 34.4549. The routine continues with the next measurement despite the error message.

Sweep Offset Slope Out Of Range. The sweep offset slope deviates more than 15.8% from the desired value of 0.1770. The routine continues with the next measurement despite the error message.

Sweep Offset Correction Terminated. Report To Qualified Service Person. The routine failed to complete the measurement.

CAL SWEEP OFFSET TROUBLESHOOTING PROCEDURE

Failure detected during this step indicate the instrument is unable to offset the sweep voltage with either the marker or offset DAC, or the LO Low signal cannot be counted. These errors are typically due to faults in the A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter. Perform the following steps to isolate the defective module:

1. Refer to ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate the A28 Period Counter module and replace as needed.

2. Use this procedure to check the A33 Sweep/Span Attenuator:

   - Connect an oscilloscope to pin B19 (FREQSWP+).
   - Run the frequency self-correction routine while observing the scope display.
   - When the CAL SWEEP OFFSET routine begins the DC level at pin B19 should be 0 Volts. This voltage toggles between ±50 mV as the sweep offset and marker DACs are incremented.
   - Replace the A33 Sweep/Span Attenuator if the FREQSWP+ signal does not respond correctly.

3. Refer to the ***CAL 129 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate the A25 LO module, and replace as needed. The LO Low signal must meet amplitude, frequency, and tune control requirements.

CAL SPAN ROUTINE

To begin the sixth of nine routines, the instrument display indicates

CAL SPAN

This routine calibrates the LO Low frequency span factors for each setting of a decade attenuator within the A25 LO Module: 0 (÷1), 1 (÷10), and 3 (÷1000). The 10.1 MHz to 16.1 MHz LO Low is swept for SPAN settings from 2 MHz to
10 Hz when the A11 YTO operates in its phaselock mode. The routine is complete when CAL SPAN FM 0 appears on the instrument.

To set up for this routine, the span attenuator DAC is set to 1865 and the decade attenuator is set to 0 attenuation (÷1). The LO Low frequency is then measured after the sweep is positioned at the first and ninth graticule lines. The LO Low span factor is calculated from these two frequencies.

Next the span attenuator DAC is set to 2945. The LO Low frequency is again measured after the sweep is positioned at the first and ninth graticule line. The LO Low span factor for each of the three remaining attenuator decades is calculated from these two frequencies.

This is the sixth of nine frequency self-correction routines. Trace data appears on the terminal within approximately70 seconds, listing the value for LO Low span cal factors 0 (+1), 1 (+10), 2 (+100), and 3 (+1000). The routine is complete when CAL SPAN FM 0 appears on the instrument screen. The trace, enabled by **ftra +span**, looks like this:

```
Enter command : ftra +span
FreeTraceEnable = 0002

Enter Command : recl
SetSgeeFAttn (0)
Set Decade Attn : 4
Set+YIG Dqsae Attn (2)
CalIbriCeBFan -
SetseeeFAttn (0)
Set Decade Atbly : 4
    zero span LOlo = 137452.7
SetSweepAttn (4095)
Set Decade Attn : 1
SetSweepAtfn (1875)
Set_Decade_Attn : 0
Set_Decade_Attn (2945)
Set_Decade_Attn : 1
Set_Decade_Attn : 2
Set_Decade_Attn : 3
Set_Decade_Attn : 1
Set_Decade_Attn : 2
Set_Decade_Attn : 3
    LOlo span cal factor [0] = 3.947581e-004
    LOlo span cal factor [1] = 3.285885e-003
    LOlo span cal factor [2] = 3.083868e-002
    LOlo span cal factor [3] = 3.059705e-001
Set_YIG_Decade_Attn (0)
```

The first lines of this trace are results form previous steps within the frequency self-correction. **SetSweepAtten (1865)** and **Set_Decad_Atten : 0** indicates the initial span attenuator DAC and decade attenuation (+1) settings for LO Low span calibration. **SetSweepAtten (2945)** indicates when the span attenuator DAC value is changed. Next, three **Set_Decade_Atten :** lines represent when the beam is positioned at the first graticule for the +10, 100, and 1000 decade steps. The remaining **Set_Decade_Atten :** lines represent when the beam is at the 9th graticule for the +10, 100, and 1000 decade steps. Calibration results for each decade attenuator setting (**LOlo span cal factor** []) are listed at the end. **LOlo span cal factors** equate to these decade attenuator settings: 0=+1, 1=+10, 2=+100, and 3=+1000. **Set_YIG_Decade_Atten (0)** begins the next frequency self-correction step.

SPAN CAL ERROR MESSAGES

The following errors may occur during this part of the correction:

LO Low Span Correction Out Of Range. One or more of the LO Low span factors deviated more than the allowed percentage from the desired values:

- Span cal factor 0: 3.349595E–4 ±53.5%
- Span cal factor 1: 2.735503E–3 ±55.5%
- Span cal factor 2: 2.525079E–2 ±55.5%
- Span cal factor 3: 2.525079E–1 ±55.5%

The firmware continues with the next measurement despite the error message

LO Low Span Correction Terminated. Report To Qualified Service Person. The firmware failed to complete the measurement.

CAL SPAN TROUBLESHOOTING PROCEDURE

Failures detected during this step indicate the instrument is unable to count or sweep the LO Low, or to calibrate its range. These errors are typically due to faults in the A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter module. Perform the following steps to isolate the defective module:

1. Refer to ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate the A28 Period Counter module and replace as needed.

2. Refer to step 3 and 4 of ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section to check for a functional A33 Sweep/Span Attenuator module.

   - Typical FREQSWP+ amplitudes are 5 Volts p-p at 2 MHz Span, 10 Volts p-p at 50 kHz Span, and 200 mV p-p at 10 Hz Span.
   - Replace the A33 Sweep/Span Attenuator module if the FREQSWP+ signal is missing or fails to change amplitude with Span settings.

3. Refer to ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to measure the LO Low.

   - Span Factor 0, 1, 2, and 3 refer to a decade attenuator located within the A25 LO module. Replace this module if only one of these factors is out of tolerance.

4. If steps 1, 2, and 3 do not reveal any failures, check for an operational 1st LO Phaselock Loop:

   - Connect the REF Signal Out to the RF Input and select 100 MHz CENTER FREQUENCY, 5 MHz SPAN, and –20 dBm REF Level (signal centered on the spectrum analyzer screen).
   - Reduce the SPAN to 2 MHz. If the signal disappears, the 1st LO Phaselock Loop has failed indicating a defective A25 LO Module, A31 565 MHz Synthesize, or A17 Microwave Phaselock.

5. Refer to steps 5 and 6 of the ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to check the A25 LO module (129 MHz output) and A31 565 MHz Synthesizer (525 MHz to 578 MHz output).

   - If these signals are functional, the 1st LO Phaselock failure is probably due to a defective A17 Microwave Phaselock module.
   - Check the 129 MHz and YTO inputs to the A17 module before replacing.
   - Check for close to 0 Volts DC on the FMRD signal line at pin A13 on the A25 LO module. If 129 MHz and YTO inputs are correct, but this signal is not close to 0 Volts (+5 Volts is typical when A17 is faulty), replace the A17 Microwave Phaselock module.

CAL SPAN FM ROUTINE

To begin the seventh of nine routines, the instrument display indicates:

CAL SPAN FM 0

This routine calibrates the FM Span settings (50 MHz to >2 MHz) for YTO frequencies between 8 GHz and 18 GHz at 50 MHz intervals.

To begin this routine the span attenuator DAC is set to 2945, the YTO decade attenuator is set to 0 (+1), the YTO is set to 13 GHz, and the frequency control loop is closed. The measurement will not proceed if this lop does not close. Next the sweep is positioned at the first and ninth graticule lines and the YTO frequency is counted at each location. This process is repeated for YTO frequencies from 8 GHz though 18 GHz at 50 MHz intervals. A calibration table is constructed from the results. The FM span factors for 0 attenuation (+1) is calculated by averaging the values collected in the table. A span factor for the remaining two attenuation decades is calculated from the ratios measured in the ***CAL SPAN YIG*** routine (which follows) and the span factor determined in this routine.

This is the seventh of nine frequency self-correction routines. Trace data appears on the terminal almost immediately to track the YTO activity, but data from the CAL SPAN FM routine appears in approximately 75 seconds. This trace slows the frequency self-correction routine due to the amount of information reported to the terminal. The routine is complete when CAL SPAN YIG 2 LO appears on the instrument screen

Successive interaction of the YTO occur as it tunes from 8 GHz to 50 MHz steps appear. A sample of the race enabled by **ftra +yig**, that shows how the sequence begins (8.00 GHz) and ends (18.00 GHz) YTO settings look like this:

```
Enter command : ftra +yig
FreeTraceEnable = 0080

Enter Command : recl
Set_YIG (1.327500e+010)
    dacOffset = -12660
    Strobe = 1.426075e+008
    Target Beatnote = 12.500
hiDAC      loDAC Delay Beatnote
0743             0349  0     12. 962
0741             0a56  2     12. 614
    .      .      .
    .      .      .
    strobe1 = 1.427332e+008 Hz;  beat1 = 1.28.043e+007 Hz
    strobe2 = 1.411085+008 Hz;  beat2 = 1.519231e+007 Hz
    delta fnYIG = 0.98
    fnYIG = 90.99
    YIG freq = 1.300722e+010 Hz
    .      .      .
    .      .      .
Prelock_YIG
Set_YIG= (1.299465e+010)
    dacOffset = -71
    Strobe = 1.426610e+008
    Target Beatnote = 12.500
hiDAC      loDAC Delay Beatnote
0724             093d  3     22.255

quickFindYIG (1.299475e+010,   1.426710e+008,   91)
    Strobe          Beat          lowYIG          highYIG
    1.4.6610e+008   2.077643e+007 1.296148e+010   1.300283e+010
    1.427984e+008   1.770860e+007 1.297694e+010   1.301237e+010
    1.425237e+008   0.000000e+000 0.000000e+000   0.000000e+000
    1.4.9357e+008   5.217901e+010 1.300194e+010   1.301.37e+010
    YIG freq = 1.301237e+010 Bz
    Strobe = 1.426610e=008
    Target Beatnote = 12.501
hiDAC      loDAC Delay Beatnote
071f             08ca  3     12.427
071f             08ee  2     12.497
Set_YIG (8.000000e+009)
    dacOffset = -71
    Strobe = 1.427339e+008
    Target Beatnote = 12.500
hiDAC      loDAC Delay Beatnote
0185             0acb  4     12.5.6
```

```
quickFindYlG (7.98.767e+009y 1.423.72e+00Bf 57)
 Strobe            Beat            Low YIG          High YIG
 1.423272e+008     1.119472e+007   7.959073+009     7.981462+009
 1.425494e+008     1.307874e+006   7 .981460e+009   7.984075e+009
YIG freq = 7.981460e+009 Hz

quickFindYlG (8.017233e+009y 1.429417e+008F 57)
Strobe             Beat            Low YIG          High YIG
1.429417e+008      1.374451e+007   7.990988+009     8.018477+00g
1.431649e+008      1..45765e+006   8.015987e+009    8.018478e+009
YIG freq = 8.018478e+009 Hz

Set_YIG (8.050000e+009)
    .      .      .
    .      .      .
Set_YIG (1.800000e+010)
    dacOffset = -71
    Strobe = 1.4.7597e+008
    Target Beatnote = 1..499
hiDAC      loDAC Delay Beatnote
OcbB              0850  3     11.806
OcbB              09a5  2     12,539

quickFindYlG (1.798277e+010, 1.4.6.1.e+008F 127)
Strobe              Beat             Low YIG          High YIG
1+426212e+008       1.091578e+007    1.795935e+010    1.798118e+010
1.427204e+008       1.577132e+007    1.798119e+010    1.798435e+010
YIG freq = 1.798119e+010 Hz

quickFindYlG (1.801723e+010, 1.428947e+008y 126)
Strobe              Beat             Low YIG          High YIG
1.428947e+008       1.393814e+007    1.799079e+010    1.801877e+010
1.429939e+008       1.428970e+006    1.801580e+010    1.801876e+016
YIG freq = 1.801866e+010 Hz
```

The initial portion of this trace represents results from previous routines. To begin the CAL SPAN FM routine, a **Prelock_YIG** routine closes the frequency control loop to check basic functionality. The desired YTO frequency is selected by **Set_YIG (1.299465e+010)**.

A **quickFindYIG** routine fine-tunes the YTO frequency if it is not within tolerance (beatnote is not close to **Target Beatnote = 12.500**). Data listed after quickFindYIG includes the expected YTO frequency (**1.299465e+010**), beginning Strobe frequency (**1.426610e+008**), and the Strobe harmonic (**91**) used to generate Beatnotes. This routine varies the **Strobe** frequency and measures the resulting **Beat** frequency. Calculated YTO values are then listed for each mixing product that could have generated the **Beat** frequency; **Low YIG** = –YTO + (Strobe x N) and **High YIG** = YTO – (Strobe x N) **quickFindYIG** concludes by listing the actual YTO frequency (**YIG freq = 1.301237e+010 Hz**)

The CAL SPAN FM routine is now ready to adjust the FM Span settings over the 8 to 18 GHz YTO frequency range. The first correction occurs at **Set_YIG (8.000000e_009)**. Additional information for this setting includes the **dacOffset = –71, Stobe = 1.426339e+008**, and **Target Beatnote = 12.500**. A **quickFindYIG** will follow if the YTO frequency is not within the required tolerance. After the YTO frequency is set, two **quickFindYIG** routines occur to measure the YTO frequency when the sweep is positioned at the firs and ninth graticules. **quickFindYIG (7.982767e+009, 1.423263e+008, 56)** determines the YTO frequency at the first graticule, and **quickFindYIG (8.017233e+009, 1.429417e+008, 56)** determines the YTO frequency at the ninth graticule. The results of these two measurements are then used to calculate the FM span factor for this 50 MHz span. The routine continues to the next YTO frequency **Set_YIG (8.050000e+009)** where the next FM SPAN calibration will occur. The YTO frequency steps in 50 MHz increments until the 8 to 18 GHz range is calibrated.

CAL SPAN FM ERROR MESSAGES

The following errors may occur during this part of the correction:

FM Span Correction Terminated. Report To Qualified Service Person. The firmware failed to complete the measurement.

FM Span Correction Out Of Range. One or more of the FM Span factors deviated more than the allowed percentage from the desired value:

- Span cal factor 0 (÷1): 6.5442E–5 ±24.4%
- Span cal factor 1 (÷10): Span cal factor 0 x 10 ±2%
- Span cal factor 2 (÷100): Span cal factor 0 x 100 ±2%

CAL SPAN FM TROUBLESHOOTING PROCEDURE

Most failures detected during this step indicate the instrument is unable to count the A11 YTO frequency, or calibrate the FM Spans (50 MHz to >2 MHz). These errors are typically due to faults in the A11 YTO, A17 Microwave Phase Lock, A31 565 MHz Synthesizer, A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter. Perform the following steps to isolate the defective module:

1. Refer to the ***CAL 13 LO TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate the A28 Period Counter and A33 Sweep/Span Attenuator modules.

   - Be sure to check that the FREQSWP+ ramp changes amplitude as the SPAN setting is changed.
   - Replace the A28 Period Counter and A33 Sweep Span/Attenuator modules as needed.

2. Check the FM Spans (50 MHz to >2 MHz) sweep path from the A25 LO module:

   - Set the SPAN to 50 MHz and check for a 9 Volt p-p ramp at A25 pin B21 (FMCSWP). This ramp decreases to about 900 mV p-p as the SPAN is decreased to 5 MHz.
   - Replace the A25 LO module if missing or distorted.

3. Measure the FM Spans (50 MHz to > 2 MHz) drive to the A11 YTO:

   - Set the SPAN to 50 MHz and check for a 4 Volt p-p, negative-going ramp at pins 1 and 2 of the A11 YTO ribbon cable (brown and red wires). This ramp decreases to 500 mV p-p at 5 MHz SPAN.
   - Replace the A17 Microwave Phaselock module if missing or distorted, but the signal from step 2 is correct.

4. Use a test spectrum analyzer to measure the A11 YTO frequency when the FM Coil is swept. The frequency change should equal the SPAN setting (50 MHz change when the SDPAN is 50 MHz).

   - Replace the A11 YTO if the drive signal from step 3 is correct but the YTO frequency does not sweep.

5. Refer to steps 5 and 6 of the ***CAL YIG TROUBLESHOOTING PROCEDURE*** located earlier in this section for procedures to check the A25 LO and A31 565 MHz Synthesizer modules. Replace these modules as needed.

CAL SPAN YIG ROUTINE

To begin the eighth of nine routines, the instrument display indicates

CAL SPAN YIG 2 LO

This routine calibrates the Main Coil span factors (>50 MHz) for the +100, +10, and +1 decade attenuator steps (span factor 2, 1, and 0 respectively).

To begin this step YTO is set to 13 GHz, the span attenuator DAC is set to 2945, and the YTO decade attenuator is set to +100. The YTO frequency is then measured after the sweep is positioned at the first and ninth graticule lines to determine the frequency span. Span factor 2 is adjusted using this data and the correction table produced from the CAL SPAN FM routine. The YTO decade attenuator is then set to +10 and +1, and this process is repeated, to determine values for span factors 1 and 0.

This is the eight of nine frequency self-correction routines. Trace data appears on the terminal almost immediately to track the YTO activity, but data from the CAL SPAN YIG routine appears in approximately 6 minutes when the screen indicates CAL SPAN YIG 2 LO. Span factor values for each decade attenuator setting in Main Coil and FM Span settings are listed at the conclusion of this trace. The frequency self-correction routines run slowly due to the amount of information reported to the terminal. The routine is completed when CAL SWEEP TIME appears on the instrument screen. A sample of the trace, enabled by **ftra +yig +span,** looks like this:

```
Enter command : ftra +yig +span
FreqTraceEnable = 0082

Enter Command : recl
Set_YIG (1.327500e+010)
    dacOffset = .12660
    Strobe = 1.426075e+008
    Target Beatnote = 12.500
hiDAC      loDAC Delay Beatnote
0743             0349  0     12.972
0741             0a56  2     12.614
    .      .      .
    .      .      .

Set_YIG (1.800000e+010)
    dacOffset = -71
    Strobe = 1.427597e+008
    Target Beatnote = 1..499
hiDAC      loDAC Delay Beatnote
0cb8             0850  3     11.806
0cb8             09a5  2     12.539

quickFindYIG (1.798277e+010, 1.426212e+008, 126)
    .      .      .
    .      .      .
Prelock YIG
Set_YIG_Decade_Attn (2)
Set_YIG (1.300000e+010)
    dacOffset = -143
Strobe = 1.427198e+008
Target Beatnote = 12.498
hiDAC      IoDAC Delay Beatnote
0722             0a8e  4     12.538

FindYIG (1.297003e+010)
    .      .      .
    .      .      .
    YIG freq = 1.296680e+010 Hz
    .      .      .
    .      .      .
```

```
FindYIG (1.302997e+010)
    .     .     .
    .     .     .
    YIG freq = 1.303332e+010 Hz
    .     .     .
    .     .     .
Set_YIG_Decade_Attn (1)
findYIG (1.267866e+010)
    .     .     .
    .     .     .
    YIG freq = 1.267240e+010 Hz
FindYIG (1.332934e+010)
    .     .     .
    .     .     .
    YIG freq =1.33.971e+010 Hz
    .     .     .
    .     .     .
Set_YIG_Decade_Attn (0)
FindYIG (9.719965e+009)
    .     .     .
    .     .     .
    YIG freq = 9.717364e+009 Hz
FindYIG (1. 62800e+010)
    .     .     .
    .     .     .
    YIG freq = 1.624767e+010 Hz
    YIG span cal factor [0] = 3.607250e-007
    YIG span cal factor [1] = 3.591426e-006
    YIG span cal factor [2] = 3.576837e-005
    FM span cal factor [0] = 6.253768e-005
    FM span cal factor [1] = 6.226334e-004
    FM span cal factor [2] = 6.201042e-003
```

The first data listed in this trace are results from previous steps. To begin the CAL SPAN YIG routine, **Prelock_YIG** closes the frequency control loop. Next the YTO decade attenuator is set to ÷100 (**Set_YIG_Decade_Atten** (2)), and the YTO frequency is set to 13 GHz (**Set_YIG** (**1.300000e+010**)). A quickFindYIG routine may follow if the YTO frequency is not within tolerance (beatnote not close to **Target Beatnote** = **12.500**).

The sweep is positioned at the firs and ninth graticule lines, and the YTO frequency is counted at each location using a **FindYIG** routine, to determine the frequency span. In this example, the YTO frequency is **1.296680e+010 Hz** at the first graticule, and **1.303332e+010 Hz** at the ninth graticule. From these measurements, the YIG span cal factor 2 (÷100) calibration data is determined.

The routine proceeds by setting the YTO decade attenuator to ÷10 (**Set_YIG_Decade_Atten** (1)). Two FindYIG routines follow to determine the YTO frequency when the sweep is positioned at the first and ninth graticule lines. These measurements are used to determine the YIG scan cal factor 1 (÷10) calibration data. The process repeats once more for YIG span cal factor 0 (**Set_YIG_Decade_Atten** (0)). At the conclusion of this trace span cal factors for each Main Coil (**YIG span cal factor** []) and FM (**FM span cal factor** []) YTO decade attenuator setting are listed.

CAL SPAN YIG ERROR MESSAGES

The following errors may occur during this part of the correction:

YTO Span Correction Terminated. Report To Qualified Service Person. The firmware failed to complete the measurement.

YTO Span Cal Out Of Range. One or more of the Main Coil Span factors deviates more than the allowed percentage from the desired value:

- YIG span cal factor 0 (÷1): 37190E–7 ±21.2%
- YIG span cal factor 1 (÷10): YIG span cal factor 0 x 10 ±2%
- YIG span cal factor 2 (÷100): YIG span cal factor 0 x 100 ±2%

CAL SPAN YIG TROUBLESHOOTING PROCEDURE

Most failures detected during this step indicate the instrument is unable to count the A11 YTO frequency, or calibrate its sweep range for Main Coil Spans (>50 MHz). These errors are typically due to faults in the A11 YTO< A11A2 YTO Driver, A17 Microwave Phase Lock, A31 565 MHz Synthesizer, A33 Sweep/Span Attenuator, A25 LO Module, or A28 Period Counter. Perform the following steps to isolate the defective module:

1. Refer to the ***CAL YIG TROUBLESHOOTING PROCEDURE*** located earlier in this section for a troubleshooting procedure to isolate each module.

   - The decade attenuators are located within the A25 LO Module and the span attenuator DAC is located on the A33 Sweep/Span Attenuator module.
   - The span attenuator DAC is tested during the CAL SPAN FM routine.

CAL SWEEP TIME ROUTINE

To begin this last of nine routines, the instrument display indicates

CAL SWEEP TIME

This routine calibrates the sweep time. The period of the SLZS signal (sweep time equal to about 11 horizontal divisions) is counted and compared to the PSG (Precision Sweep Gate) signal period. PSG represents the 1000 point digitized display. Both signals are applied to the Period Counter which is gated by a special 1 MHz reference from the A29 Reference Oscillator. Sweep timing is calibrated by adjusting a Miller Integrator (within the A33 Sweep/Span Attenuator module) to change the SLZS period. The Miller Integrator has nine selectable timing resistor and capacitor combinations (Ranges 0 to 8).

To begin this step the Sweep/Span Attenuator and Period Counter are set up to measure sweep time. Next the SLZS and PSG signals for timing resistor/capacitor ranges 2 and 3 are measured, and a ratio is established between the two. The SLZS for ranges 4 through 6 are then measured, and the PSG time for each is calculated, using the ratio established from the previous measurement. The remaining ranges are calculated from the ratios of the measured sweep ranges.

This is the last of nine frequency self-correction routines. Trace data appears on the terminal immediately to track the CAL SWEEP and CAL SWEEP OFFSET routine activities, but data from the CAL SWEEP TIME routine appears in approximately 4 minutes. Included in the data are measurement results of the SLZS and PSG signals, and an average ratio between them (Ranges 2 and 3). Computed PSG values based upon the measured ratio are then listed. The routine is complete when the frequency self-correction routine is finished. The trace, enabled by **ftra +sweep**, looks like this:

```
Enter command : ftra +sweep
FreeTraceEnable = 0001

Enter Command : recl
CalibrateSweep
sweep reg 105    sweep DAC    448
sweep reg 159    sweep DAC    623
```

```
    .      .      .
    .      .      .
    248    40171  11216.86
    249    4092   1221.45
SweepOffsetSlope = 0.174904  SweepOffsetSlope = 35.419144
Range 2: Measured sweep gate is 0.334487 sec
    Measured precision sweep gate is 0.287457 sec
Range 3: Measured sweep gate is 0.045467 sec
    Measured precision sweep gate is 0.039076 sec
    Average ratio is 0.859415
Range 4: Measured sweep gate is 0.005189 sec
    Computed precision sweep gate is 0.004460 sec
Range 5: Measured sweep gate is 0.000571 sec
    Computed precision sweep gate is 0.000491 sec
Range 6: Measured sweep gate is 0.000078 sec
    Computed precision sweep gate is 0.000077 sec
Range 0: Computed precision sweep gate is 22.889822 sec
Range 1: Computed precision sweep gate is 2.612.75 sec
Range 7: Computed precision sweep gate is 0.000008 sec
Range 8: Computed precision sweep gate is 0.000000 sec
```

The first part of this trace provides results from the previous steps. **Range 2: Measured sweep gate** is the measured value for SLZS with a specific timing resistor/capacitor combination, and is followed by **Measured precision sweep gate**, the measured PSG period for the same range. **Average ratio** is the average measured ratio of SLZS and PSG from Ranges 2 and 3. This ratio is then used to compute PSG values for the remaining ranges. Following these are a list of measured SLZS values for other timing resistor/capacitor combinations, and calculated values for the PSG signal period. **Range 8** always has a value of **0.000000 sec** due to display resolution limitations.

CAL SWEEP TIME ERROR MESSAGES

The following errors may occur during this part of the correction:

Sweep Time Correction Terminated. Report To Qualified Service Person. The firmware was unable to count a sweep period.

CAL SWEEP TIME TROUBLESHOOTING PROCEDURE

Most failures detected during this step indicate the instrument is unable to count the SLZS or PSG signals, or adjust the sweep rate to specified limits. This error is typically due to faulty A33 Sweep/Span Attenuator. A29 Reference Oscillator, A29 Video Processor, A24 Digital Storage, or A28 Period Counter modules. Perform the following steps to isolate the defective module:

1. Refer to the *CAL 13 LO TROUBLESHOOTING PROCEDURE* located earlier in this section for a troubleshooting procedure to isolate the A28 Period Counter, and replace if needed.

2. Use an oscilloscope to measure the TTL-level SLZS signal at pin B2 of the A28 Period Counter module.

   - The signal is High during active sweep time; its period should be about 10% greater than the selected sweep time.
   - Replace the A33 Sweep/Span Attenuator module if the SLZS signal is missing or distorted.

3. Use an oscilloscope to measure the TTL-level PSG signal at pin B22 of the A28 Period Counter module.

- The signal is High during active sweep time; its period should equal the selected sweep time.
- If PSG is missing, check for the TTL-level SWPGATE signal at pin A22 on the A20 Video Processor module.
- Replace the A33 Sweep/Span Attenuator module if the SWPGATE signal is missing or distorted. Replace the A20 Video Processor module if the SWPGATE signal is correct but PSG is missing or distorted.

4. Use an oscilloscope to measure the TTL-level 1 MHz Reference signal at pin B1 on the A28 Period Counter module.

   - Enable keyboard mode and enter the common:

     ```
     rmhz 1
     ```

     The 1 MHz signal should appear on the oscilloscope.
   - Replace the A29 Reference Oscillator module if the 1 MHz signal is missing or distorted, and replace the A28 Period Counter if signals from step 1, 2, and 3 are correct.

DIGITAL CONTROL SYSTEM DIAGNOSTICS

There are two levels of diagnostics for the Digital Control system, which include the A41 Main Processor and A43 Memory modules. Power-up Diagnostics are a form of automatic testing to quickly verify Digital Control system performance before operation begins. Advanced Diagnostics are available for more detailed and time consuming check required for fault isolation. The Advanced Diagnostics tests are initiated by setting switches on the Main Processor board.

Each Advanced Diagnostics test has two modes of operation: single pass and looping. Single pass mode stops the diagnostic test and displays an error message whenever an error is encountered. Other wise, normal operation resumes when the single pass test completes. The looping test mode continues to run diagnostics until a failure occurs. An error message indicates the detected failure.

POWER-UP DIAGNOSTICS

This section describes the power-up diagnostics for the instrument. Sixteen LEDs on the A41 Main Processor board, CR10 – CR25 (Figure 4-8), display predictable patterns to indicate test information. Each step within the power-up sequence is identified by a 4-digit Hexadecimal (Hex) equivalent combination of the sixteen LEDs. An un-lit LED represents a binary "0" and an illuminated LED represents a binary "1". During normal operation, many of the LEDs are actively exercised.

CR 10 – CR13 form the most significant Hex digit (MSB), CR14 – CR17 form the next group, CR18 – CR21 form one group, and CR22 – CR25 form the least significant (LSB) digit. LEDs are read from left to right. Table 4-16 shows how to convert groups of four LEDs to a Hex value. For example, and LED display of 0000/0000/0000/0001 (only CR25 is lit) represents the Hex value **0001**, and LED pattern of 1001/1100/0001/1111 is the Hex value **9C1F**.

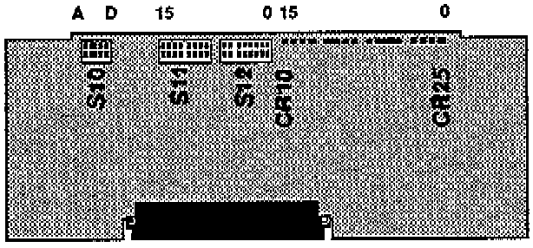


Figure 4-8. Main Processor board switches and LEDs.

Table 4-16. Binary to Hex conversion for LEDs.

LED Pattern	Hex Value	LED Pattern	Hex Value
0000 (all off)	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	B
0100	4	1100	C
0101	5	1101	D
0110	6	1110	E
0111	7	1111 (all on)	F

MICROPROCESSOR SELF TEST

This is the first test within the power-up diagnostics sequence. It turns all LEDs off (Hex value 0000), sets the internal flags for the processor chip, then checks that each flag has been set. If there are no errors the internal flags are cleared and checked once more, followed by a quick check of all available internal registers. An error stops the program.

INITIALIZE PROCESSOR I/O

Entering this test the LED pattern displayed the Hex value 0001. This routine sets up various controller chips that make up the system. After the setup is completed switches S11 and S12 are checked to see if the advanced diagnostics test are selected, or if normal operation should proceed.

CHECK SYSTEM ROM

Entering this test the LED pattern displays the Hex value 0002. This is a check of System ROM U63. A failure is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed, the expected checksum, and the actual checksum.

RAM TEST

Entering this test, the LED pattern displays the Hex value 0004. Initially all RAM locations are loaded with logic highs. Each location is then checked for correct data. The test is then repeated after loading the RAM with logic lows. If a failure is detected, all sixteen LEDs are flashed followed by a pattern indicating the module and test that failed. This display if followed by the specific address that failed, the expected data, and the incorrect data.

REMAINING ROM TEST

Entering this test the LED pattern displays a Hex pattern for each ROM as it is checked (Table 4-17). If an error occurs all sixteen LEDs are flashed, followed by a Hex pattern indicating the module and test that failed. This display is followed by the expected and actual checksums.

Table 4-17. LED patterns for ROM identification.

ROM	Location	LED Hex Value
ROM 4	U11	0008
ROM 6	U12	0009
ROM 8	U13	000A
ROM A	U14	000B
ROM C	U10	000C

INTERRUPT CONTROLLER TEST SETUP

Entering this test the LED pattern displays the Hex value **0010**. The first step sets up the instrument vectors and initializes the stack area. Next a check is made for any pending interrupts, then all interrupts are disabled.

INITIALIZE INTERRUPT VECTORS

Entering this test the LED pattern displays the Hex value **0011**. This routine initializes the vectors that are used to drive functions defined by the interrupts.

TIMER TESTS

Entering this test the LED pattern displays the Hex value **0020**. This test checks each of the timers used for bus tests and performs a simple functional test of one timer.

DMA INITIALIZATION

Entering this test the LED pattern displays the Hex value **0040**. This step performs a simple bus test of the DMA controller and then sets it up for normal operation.

POWER SUPPLY CONTROL

Entering this test the LED pattern displays the Hex value **0080**. This test is a write-read test of the power supply and YIG control bits. Upon test completion the LED pattern displays 0081, indicating that the system is waiting for the power supply to turn on and reach proper operating voltage.

NON-VOLATILE MEMORY CONTROL CHECKS

Entering this test the LED pattern displays the Hex value **0100**. This step checks the control circuits on the A24 I/O Interface Board.

INSTRUMENT BUS CHECK

Entering this test the LED pattern displays the Hex value **0200**. This test checks for access to the control bus interface (SCL and SDA signal paths).

DIGITAL BUS CHECK

Entering this test the LED pattern displays the Hex value **0201**. This test checks for access to the display bus interface (SDAHSE and SDASE signal paths).

INITIALIZE RAM VALUES

Entering this test the LED pattern displays the Hex value **8000**. This routine copies data from the ROMs into RAM before beginning to execute he normal operating system.

ADVANCED DIAGNOSTIC

GENERAL INFORMATION

The advanced Diagnostics tests are used for fault isolation on the A41 Main Processor and A43 Memory boards. These test are defined by setting switches on the Main Processor board.

Two test modes, Single Pass and Looping, are available. Selected test run one time in Single Pass mode, while Looping mode runs test continuously until a failure is detected.

MAIN PROCESSOR SWITCH SETTINGS

Switches S11 and S12 located on the A41 Main Processor (Figure 4-8) enable the Advanced Diagnostic mode, choose between Single Pass or Looping modes, and select which module will be tested. These switches also determine whether to execute all available test, or only one specific test, on the selected module.

Figure 4-9 shows how to set S11 and S12 for Advanced Diagnostics. **Switch #15** selects between normal operation (power-up diagnostics) and Advanced Diagnostics. This switch is OPEN (0) for normal operation. **Switch #14** chooses Single Pass (0) or Looping (C). **Positions 8 – 13** select which module is tested and **positions 0 – 7** select the test to be performed. Table 4-18 summarizes the switch definitions.

Table 4-19 shows how to set position 8 – 13 to select the Main Processor Memory board. A "0" indicates open and "C" indicates a closed switch. The exact function of test-selection switches 0 through 7 varies for each module. These switch settings are defined as individual tests are described later in this section.

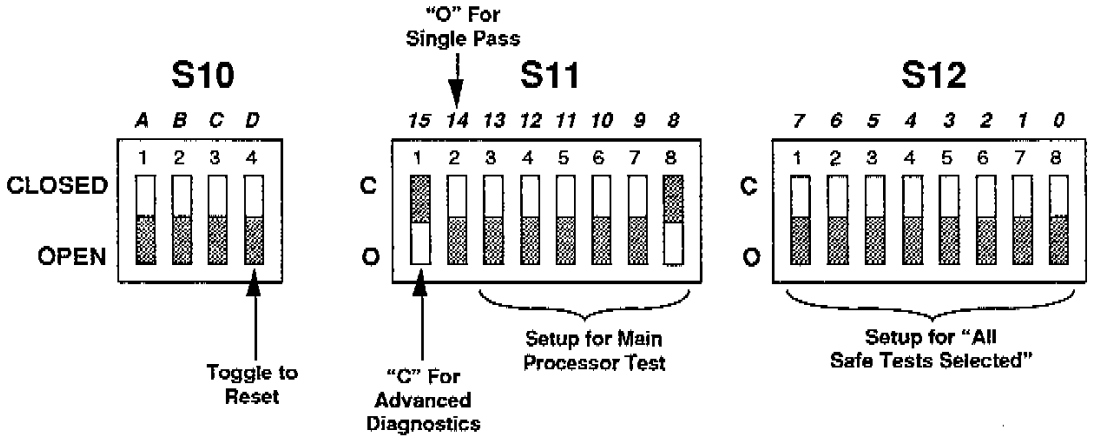


Figure 4-9. Switch settings for Main Processor, Single Pass, All Safe Tests.

Table 4-18. Advanced Diagnostics switch configuration.

Switch Number	Location	Function
15	Main Processor S11	Normal Diagnostics/ADVANCED DIAGNOSTICS (closed)
14	Main Processor S11	Single Pass/CONTINUOUS LOOPING (closed)
8-13	Main Processor S11	Module Selections
0-7	Main Processor S12	Test Selections

Table 4-19. Advanced Diagnostics module selections.

Switch Number						Module Selected
13	12	11	10	9	8	
0	0	0	0	0	C	Main Processor
0	0	0	0	C	0	Memory Board

RUNNING THE TESTS

NOTE

Write down the current settings before starting Advanced Diagnostics.

Advanced Diagnostics tests are initiated by the following sequence. Each module and test selection is described in detail later in this section.

1. Close **S11 #15** to enable Advanced Diagnostics.
2. Select Single Pass or Looping mode with **S11 #14**.
3. Select module to be tested with **S11 #8 – 13**.
4. Choose test with **S12 #0 – 7**.
5. Toggle **S10 #D** to begin the test.

NOTE

The instrument behaves differently when Single Pass mode tests for the Main Processor and Memory board execute successfully. A normal power-up occurs following successful completion of Main Processor tests, while the LEDs display Hex 0081 (CR18 and CR25 lit) at the end of successful Memory board tests.

Looping mode causes the selected tests to run continuously until a failure is detected.

MAIN PROCESSOR USER FEEDBACK

The Advanced Diagnostics provide feedback to the user through LED indicators on the Main Processor Board, shown in Figure 4-3. The sixteen LEDs form a 16-bit digital word that shows the current test and module; CR10 is a bit 15 (MSB) to the data word and CR25 is bit 0 (LSB). In addition, CR10 lights to indicate when a long test is running. The indicators also display patterns when a test fails. Specific LED patterns for each test are described later in this section.

INVALID MODULE OR TEST SELECTIONS

A fault sequence is shown before normal operation continues if S11 and S12 on the Main Processor board are set to test undefined modules or module tests.

When an undefined module is selected (S11 # 8 – 13 see Table 4-19), CR10 – CR17 are flashed on and off, followed by patterns indicating the maximum valid module value and the actual module value. This pattern repeats several times before continuing normal operation. The selected module test is ignored until a valid module is chosen.

When an undefined test is selected (S12 # 0 – 7, see Tables 4-19 and 4-20), CR18 – CR25 are flashed on and off followed by patterns indicating the maximum valid test value and the actual test value. This pattern repeats several times before continuing normal operation.

TEST FAILURE REPORTING

Test failures are reported differently for Single Pass and Looping modes. Single Pass mode failures are reported by first flashing all sixteen LEDs. Next a pattern is generated that shows which module and test failure, and if possible, the component that failed. This sequence repeats until the test is terminated. If the display system is working, the current status is displayed along with any related error messages.

Continuous Looping failures are reported as described for Single Pass mode, but testing continues until the main processor is reset.

MAIN PROCESSOR ADVANCED DIAGNOSTICS

This section describes each Advanced Diagnostics test for the A41 Main Processor board. The Main Processor board is a self-contained module, requiring only a power supply to run these tests. Several built-in fault isolation tools are also available to further isolate faults on this board. Use the All Safe Test (25 seconds) and Module Verification Test (7 minutes) to isolate failures to the A41 Main Processor board, and the remaining tests for on-board fault isolation.

Table 4-20 shows how to select individual Advanced Diagnostic test for the A41 Main Processor board. Close S11 #8 to enable these tests. "0" indicates an open switch and "C" indicates a closed switch.

Table 4-20. Main Processor test selections.

Switch Number								
7	6	5	4	3	2	1	0	Test Selected
0	0	0	0	0	0	0	0	All Safe Tests Selected
0	0	0	0	0	0	0	C	LED Tests
0	0	0	0	0	0	C	0	Switch Test
0	0	0	0	0	0	C	C	System ROM Test
0	0	0	0	0	C	0	0	RAM Test 1st Bank XOR
0	0	0	0	0	C	0	C	RAM Test 1st Bank LONG
0	0	0	0	0	C	C	0	RAM Test 1st Bank SOAK
0	0	0	0	0	C	C	C	RAM Test 2nd Bank XOR
0	0	0	0	C	0	0	0	RAM Test 2nd Bank LONG
0	0	0	0	C	0	0	C	RAM Test 2nd Bank SOAK
0	0	0	0	C	0	C	0	Interrupt Controller Bus Test
0	0	0	0	C	0	C	C	Timer Controller Bus Test
0	0	0	0	C	C	0	0	Timer Controller Functional Test
0	0	0	0	C	C	0	C	Interrupt Controller Functional Test
0	0	0	0	C	C	C	0	DMA Controller Bus Test
0	0	0	0	C	C	C	C	Power Supply, YIG Control Test
C	C	C	C	C	C	C	C	Module Verification Test

ALL SAFE TEST SELECTED

This test performs all non-destructive tests available for the Main Processor board. Each test executes once and then continues to the next test. RAM is tested by the short, non-destructive XOR test. If a failure occurs it is indicated by first turning all the LEDs on followed by a Hex pattern indicating which module and test failed. This test is competed in about 25 seconds.

LED TEST

All LEDs turn off for a short time, then each LED is turned on individually. Following this sequence is a pattern that turns on alternate LEDs (one is on, the next is off, and so forth). The data pattern is then reversed. Failures must be determined visually. This test is completed in about 5 seconds.

SWITCH TEST

This test provides and LED display of the data read from switches S11 and S12. The LED associated with each switch is off for a closed (C) switch and on for an open (O) switch. Failures must be determined visually. For bets results use Looping mode so switch settings are displayed continuously, and LED patterns change as switches are toggled.

SYSTEM ROM TEST

This test performs a checksum of System ROM U63 located on the Main Processor board. Failures are indicated by first tuning all the LEDs on, followed by a Hex pattern indicating which module and test failed, the expected checksum, and the actual checksum. This test is completed in about 5 seconds.

RAM TESTS

These tests check one of the two RAM banks located on the Main Processor board. Bank 1 consists of U39 (bits 15-8) and U60 (bits 7-0). Bank 2 consists of U29 (bits 15-8) and U49 (bits 7-0). Three types of tests may be performed: XOR, LONG, and SOAK.

NOTE

The LONG and SOAK tests change data in RAM, which includes the Current Correction data. Valid corrections data is restored from non-volatile memory when the power is turned of and on again.

The XOR test is a non-destructive RAM test (memory contents is unchanged after the test). This test reads the data from the first memory location and stores this value. The data is then exclusive-OR'ed (XOR'ed) with the first value and is written to the same location. Finally the data is verified to ensure that the new value matches the original. If no errors occur a second XOR test is performed for this location. Again, if no errors occur, a third XOR test is done which restores the original value. This sequence repeats until each RAM location is tested. During this test the LEDs indicate the selected module and test. This test is completed in about 5 seconds.

The LONG test is a destructive test of the data stored in memory (it changes the values in memory when executed). This is a long test so CR10 blinks on and off to indicate when the test is running. The remaining LEDs identify the current test and module. This test is completed in about 150 seconds.

The SOAK test is also a destructive test. It stores a pattern into RAM, waits almost a minute, and checks for the correct data. Three patterns are tested this way. This is a long test so CR10 blinks on and off to indicate when the test is running. The remaining LEDs identify the current test and module. This test is completed in about 150 seconds.

If a failure is detected during any RAM test, all sixteen LEDs are flashed followed by a pattern indicating the module and test that failed. This display is followed by the specific address that failed, the expected data, and the incorrect data. If Looping is active the program will attempt to read and write from the failed address until the system resets.

INTERRUPT CONTROLLER BUS TEST

There are two tests from the Interrupt Controller chip. The first verifies operation of the data bus to and from the Interrupt Controller chip; the second checks for pending interrupts after the test is complete. This test is completed in about 5 seconds.

Failures are indicated by flashing all sixteen LEDs on, followed by a Hex pattern indicating the module and test. Next the failed address that failed is displayed, followed by the expected and actual data.

TIMER CONTROLLER BUS TEST

This test check the bus interface to the Timer Controller chip. If a failure is detected, all sixteen LEDs are flashed followed by a pattern indicating the module and test that failed. This display is followed by the specific address that failed, the expected data, and the incorrect data. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed. This test is completed in about 5 seconds.

TIMER CONTROLLER FUNCTIONAL TEST

This test causes the three timers to produce square waves at different frequencies. The first timer divides the processor bus clock by 2, the second timer by 4, and the third timer by 8. These TTL-level signals can be viewed at TP11, TP12, and TP13; large, square pads located on the Main Processor board near the Mother board connector.

INTERRUPT CONTROLLER FUNCTIONAL TEST

This test checks that the Interrupt Controller receives the Timer Controller output. If a failure occurs it is indicated by first turning all the LEDs on followed by a Hex pattern indicating which module and test failed. This test is completed in about 5 seconds.

DMA CONTROLLER BUS TEST

This a basic write and verify test for three of the internal registers on the DMA Controller Chip that write every possible bit pattern to each of the registers. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed. This test is completed in about 5 seconds.

POWER SUPPLY YIG CONTROL TEST

This is a basic write and verify test for a latch and buffer that control the fan speed, YIG power supply, and the power supply control lines. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed. This test is completed in about 5 seconds.

MODULE VERIFICATION TEST

This selection executes all tests described in this section except for the RAM XOR and SOAK tests. The RAM LONG test is performed, so this is a destructive test. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed. This test is completed in about 7 minutes.

BUILT-IN DIAGNOSTIC TOOLS

The following built-in tools help to isolate faults on the Main Processor board:

- Clock Generator
- Processor Address Testing
- Processor Reset

Clock Generator. The clock generator circuit may be defective if there is no clock for the Microprocessor. An external clock may be sued to check this circuit as follows:

1. Close Main Processor switch S10 #B to select the external clock mode.
2. Apply an external TTL-level clock between 6 MHz and 22 MHz to J10, a two-pin harmonica connector located just below S11.
3. If the processor system runs, the clock generator is defective.

Processor Address Testing. The microprocessor has a self-test mode to exercise the lowest sixteen address bits, LA0 and LA15. This is how to enter the self-test mode:

1. Close Main Processor switch S10 #A.

2. Reset the microprocessor by toggling S10 #D.

3. Use an oscilloscope to check address lines LA0 to LA15 for TTL signal levels at A41 pin A2 (LA)), B2, C2, A3, B3, C3, A4, B4, C4, A5, B5 C5, A6, B6, C6, and A7 (LA15) respectively. Each line should have a TTL-level square wave at twice the frequency of the preceding line. The MSB (LA15) has the longest period, measuring about 23 ms.

Processor Reset. If the power-up reset circuit is in question, reset the microprocessor by toggling Main Processor switch S10 #D. This will restart the microprocessor unless the supply monitor circuit located within the A5 LV Power Supply module is preventing the system reset.

MEMORY BOARD ADVANCED DIAGNOSTICS

This section describes each Advanced Diagnostics test for the A43 Memory board. The Main Processor board and LV Power Supply module must be functioning to execute these tests.

Table 4-21 shows how to select individual Advanced Diagnostic test for the A43 Memory board. Close S11 #7 to enable these tests (Figure 4-10). "0" indicates an open switch and "C" indicates a closed switch.

Table 4-21. Memory board test selections.

Switch Number								
7	6	5	4	3	2	1	0	Test Selected
0	0	0	0	0	0	0	0	All Safe Tests Selected
0	0	0	0	0	0	0	C	RAM Test 3rd Bank XOR
0	0	0	0	0	0	C	0	RAM Test 3rd Bank LONG
0	0	0	0	0	0	C	C	RAM Test 3rd Bank SOAK
0	0	0	0	0	C	0	0	RAM Test 4th Bank XOR
0	0	0	0	0	C	0	C	RAM Test 4th Bank LONG
0	0	0	0	0	C	C	0	RAM Test 4th Bank SOAK
0	0	0	0	0	C	C	C	ROM 4 Test
0	0	0	0	C	0	0	0	ROM 6 Test
0	0	0	0	C	0	0	C	ROM 8 Test
0	0	0	0	C	0	C	0	ROM A Test
0	0	0	0	C	0	C	C	ROM C Test
C	C	C	C	C	C	C	C	Module Verification Test

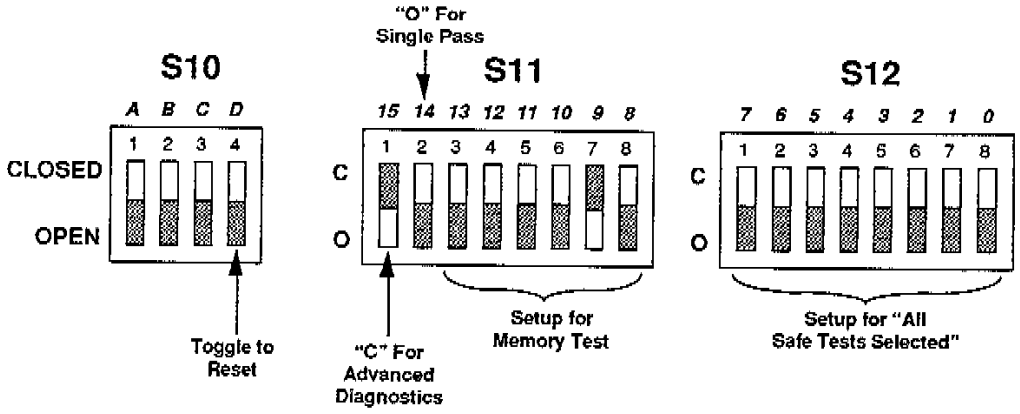


Figure 4-10. Switch settings for Memory board, Single Pass, All Safe Tests

ALL SAFE TESTS SELECTED

This test performs all non-destructive tests available for the Memory board. Each test executes once and then continues to the next test. RAM is tested by the short, non-destructive XOR test. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test failed. This test is completed in about 5 seconds.

RAM TESTS

These tests check one of the two RAM banks located on the A43 Memory board. Bank 3 consists of U16 (bits 15-8) and U20 (bits 7-0). Bank 4 consists of U15 (bits 15-8) and U19 (bits 7-0). Three types of tests are performed including XOR, LONG, and SOAK. These tests are described in detail in the ***Main Processor Advanced Diagnostics*** section.

NOTE

The LONG and SOAK tests change data in RAM, which includes the Current Correction data. Valid corrections data is restored from non-volatile memory during power-up.

If a failure is detected during any RAM test, all sixteen LEDs are flashed followed by a pattern indicating the module and test that failed. This display is followed by the specific address that failed, the expected data, and the incorrect data. If Looping is active the program will attempt to read and write from the failed address until the system resets.

ROM TESTS

These tests perform a checksum of the system EPROM banks on the Memory Board shown in Table 4-11. If an error occurs all sixteen LEDs are flashed, followed by a Hex pattern indicating the module and the test that failed. This display is followed by the expected and actual checksums.

Table 4-22. Memory Board EPROM locations.

EEPROM Bank	Location
ROM 4	U11
ROM 6	U12
ROM 8	U13
ROM A	U14
ROM C	U10

MODULE VERIFICATION TEST

This selection executes all tests described in this section except for the RAM XOR and SOAK tests. The RAM LONG test is performed, so this is a destructive test. If a failure occurs it is indicated by first turning all the LEDs on, followed by a Hex pattern indicating which module and test filed. This test is completed in about 5 minutes.

LOW-VOLTAGE POWER SUPPLY DIAGNOSTICS

WARNING

The A5 Low-voltage Power Supply module contains hazardous voltages. To avoid serious injury due to electrical shock, always remove the AC power before removing this module for service.

This section provides information to assist in the isolation of failures within the A5 Low-voltage Power Supply module, which contains the A5A1 Power Supply Primary and A5A2 Power Supply Secondary boards. This module produces several DC power supplies for distribution throughout the instrument, including auxiliary supplies which run whenever power is applied to maintain a stable internal temperature. Switchable supplies for the A11 YTO Main Coil and the Preselector Filter coil (part of the A12 MTX assembly) are also produced.

This module contains a digital interface that informs the Main Processor of supply status, and enables or disables the main supply section after the front panel POWER button is pressed. The A5A6 Communications Interface board, which contains the IEEE-488 GPIB connector, is mounted onto the rear of the module housing.

OPEN FUSES

The power supply contains two fuses: F10 is the main power line fuse and A5A1F10 is a thermal fuse. Refer to the ***Replaceable Electrical Parts*** section to obtain the proper replacement for these fuses.

MAIN POWER LINE FUSE

F10 is located within a fuse cartridge on the instrument rear panel. Replace the A5A1 Power Supply Primary board if this fuse opens when the power cord is connected to a power source, or when the POWER button is pressed.

THERMAL FUSE

A5A1F10 is located on the A5A1 Power Supply Primary board next to the AC line filter capacitors. This fuse opens when the operating temperature within the instrument exceeds 98°C. If this fuse opens:

- Check for proper ventilation around the air intake and exhaust paths from the cabinet. External air enters through holes on the bottom of the cabinet, and is exhausted through holes on the rear panel.
- Check that the A5B100 fan assembly is operating properly. The fan runs briefly when power is first applied (standby mode), and continuously when the instrument is in use.

SECONDARY SUPPLIES

SUPPLY FAIL SENSOR

A green Supply Fail Sensor LED indicates when one or more secondary supplies are significantly out of tolerance (Figure 4-11). The LED is normally illuminated, and turns off when a defective supply is detected. The LED may be viewed through a hole in the module casting.

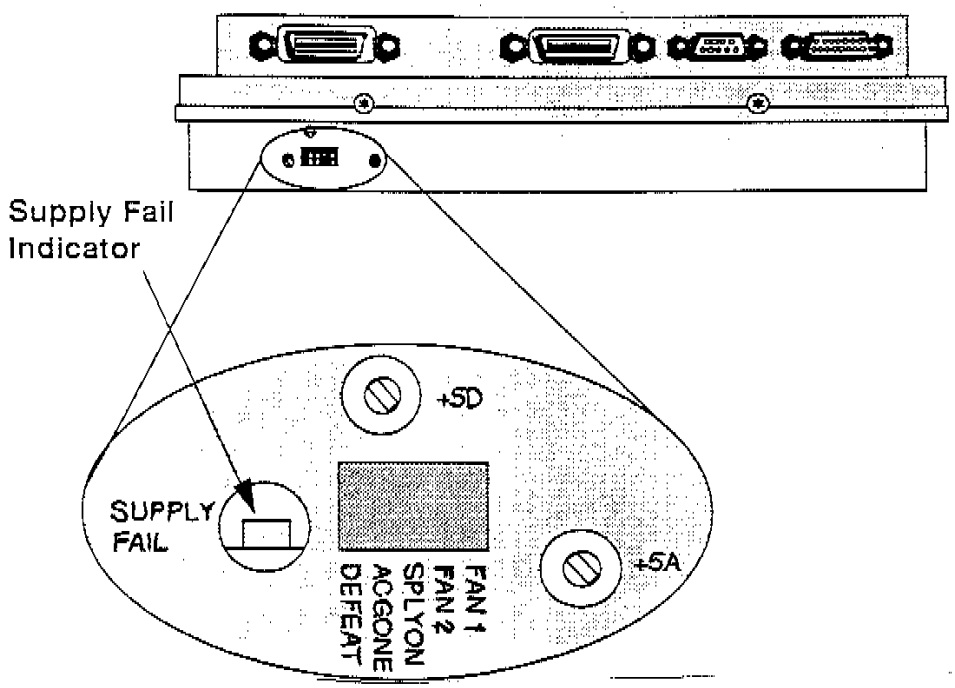


Figure 4-11. Green LED supply fail sensor location.

SUPPLY CHARACTERISTICS

Secondary supplies are measured at test points on the Mother Board, located directly behind the A43 Memory board. Refer to Table 4-23 for voltage tolerances, typical p-p ripple, and resistance to ground for each supply. Supply ripple increased during the sweep retrace period due to increased loading.

NOTE

Do not measure supply voltages when the A5 Low-voltage Power Supply module is disconnected form the Mother board. The supply requires a load to produce the correct secondary voltages.

The power supply may shut down if the +5A or +5D supplies are too high. Adjust these supplies before attempting repairs.

Table 4-23. Power supply secondary characteristics.

Supply	Tolerance	P-P Ripple (Sweep)	P-P Ripple (Retrace)	Ω To Ground
+MTXV (+18, 26 or 32 V)	7%	30 mV	200 mV	200 kΩ*
+OSCV (+18 or 26 V)	7%	30 mV	200 mV	7 kΩ
+10V	1.5%	1 mV	2 mV	20 Ω
+5VD	4%	11 mV	13 mV	5 Ω
+5VS	1.5%	0.4 mV	1.5 mV	250 Ω
–8V	1.5%	0.4 mV	2 mV	80 Ω
+95V	+3%, –5%	300 mV	300 mV	11 kΩ
+45	7%	620 mV	650 mV	11 kΩ
+18VS	–5%, +15%	25 mV	200 mV	1.3 kΩ
+15V	2%	0.5 mV	3 mV	350 Ω
+5VA	1%	0.5 mV	2 mV	80 Ω
-5.2V	1%	1.5 mV	2 mV	100 Ω
–15V	2%	0.5 mV	3 mV	400 Ω

*Wait 20 seconds after power is removed before measuring resistance.

DIGITAL CONTROL SIGNALS

The A5A2 Power Supply Secondary produces or receives several TTL-level digital control signals. The purpose of each signal, along with applicable truth tables, are provided below.

/ACGONE. Transitions low to notify the Main Processor when AC power has been removed.

- Measured at A41 pin C30.
- Failure of this line may prevent the instrument from storing data such as power-down settings into non-volatile memory when power is removed.

OSC1. Controls the voltage source to the A11 YTO Main Coil.

- Measure at A42 I/O Interface board pin B13
- Low produces +18 Volts (most common condition), High produces +26 Volts.

MTX1 AND MTX2. Produced by Main Processor to control the Preselector Filter Coil (part of A12 MTX assembly) voltage source.

- Measure at A41 pin A26 (MTX1) and pin A27 (MTX2).
- Voltage selections are 0, +18, +26, and +32 Volts DC (Table 4-24).

Table 4-24. Truth table for MTX1 and MTX2.

MTX1	MTX2	+MTXV Voltage
Low	Low	0 Volts
Low	High	+18 Volts
High	Low	+26 Volts
High	High	+32 Volts

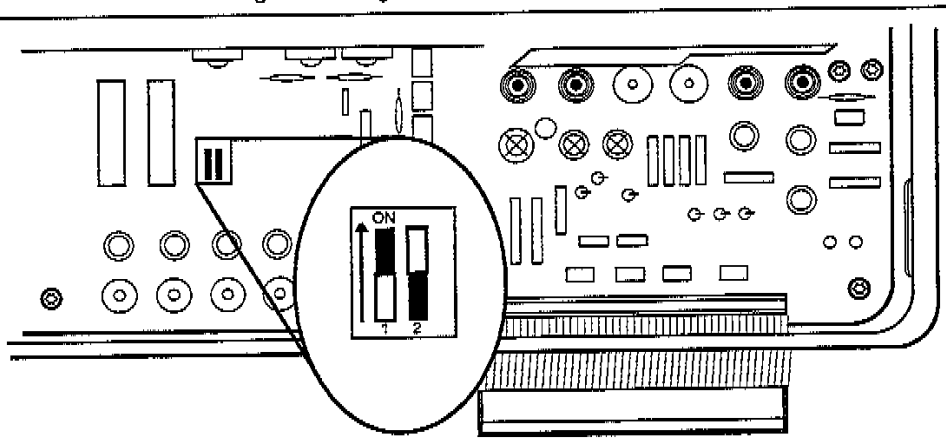


Figure 4-12. Location of defeat switch for /SPLYON signal.

/SPLYON. Produced by the Main Processor, this signal transitions Low to enable the main section of the Low-voltage Power Supply when the POWER button is pressed.

- Measure at A41 pin C27
- Failure of this line may prevent the instrument from turning on.
- This signal may be defeated for troubleshooting purposes by closing position #1 of a 2-section switch located on the A5A1 Primary Power supply board (Figure 4-12).

FAN1 and FAN2. Produced by Main Processor to control the fan speed (currently set for +30 Volts to produce maximum fan speed at all times).

- Measure at A41 pin B26 (FAN1) and pin B27 (FAN2).
- Voltage selections are +1, +17, +25, and +30 Volts DC (Table 4-25).

Table 4-25. Truth table for FAN1 and FAN2.

FAN1	FAN2	Fan Supply
Low	Low	+30 Volts
Low	High	+25 Volts
High	Low	+17 Volts
High	High	+1 Volt (Fan Off)

ISOLATING FAULTS TO PRIMARY OR SECONDARY BOARD

This power supply contains data links between the primary and secondary circuits for improved regulation. As a result, it is often difficult to determine which board has failed. Following are two methods for isolating faults to either the A5A1 Primary Power Supply or the A5A2 Secondary Power Supply board.

1. Replace one of the boards with a working circuit board.

   - If the supply fails to run, the unchanged circuit board is at fault.

2. Open the module and unplug the main switching transformer connector (Figure 4-13). Be sure to position the connector so it cannot short to surrounding parts.

   - With this connector unplugged, assemble the module, connect it to the instrument, and apply power.
   - If the auxiliary supplies (+5VS, +18VS, +MTXV, and OSCV) are present, the A5A1 Primary Power Supply board is probably functioning. This step verifies the functionality of all A5A1 circuits except the main transformer switching circuits.
   - If the auxiliary supplies do not function, and there are no short circuits on the secondary test points, replace the A5A1 Primary Power Supply board.

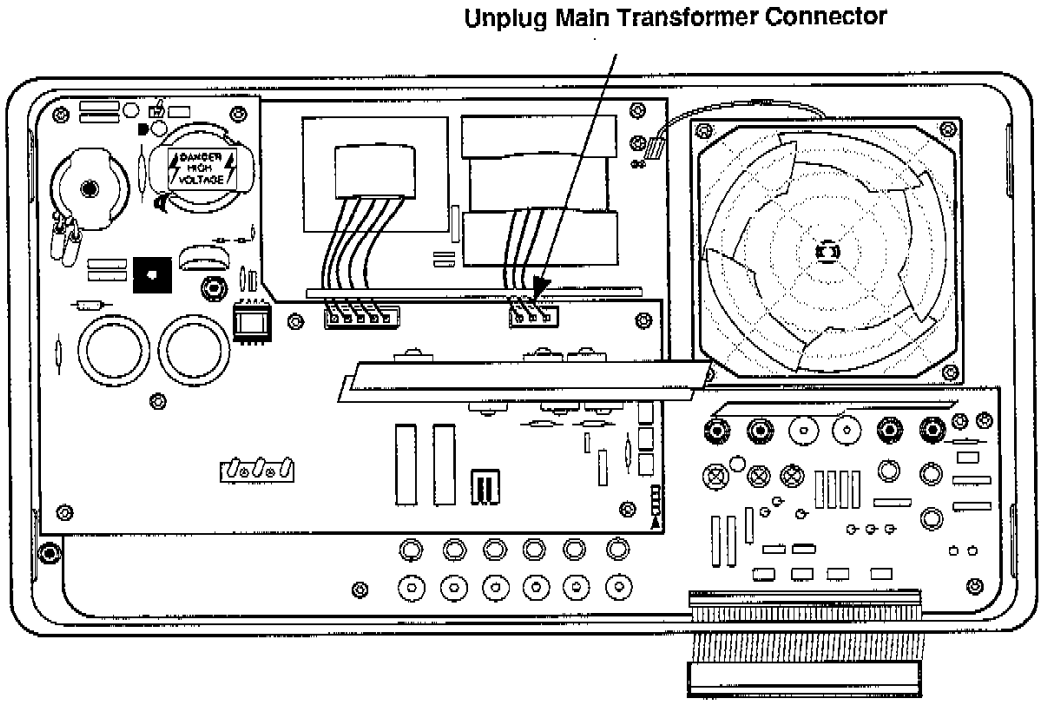


Figure 4-13. Main transformer connector location.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques and procedures that may be required to remove and replace assemblies and/or components in this instrument are described here.

STATIC-SENSITIVE COMPONENTS

Most semiconductor types, both separately and in assemblies, are susceptible to damage by static discharge. See Table 4-1, at the start of this section, for voltage levels. Use static-discharge protection whenever handling semiconductors or assemblies containing them.

OBTAINING REPLACEMENT PARTS

Replacement assemblies and parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts. Also see the following Module Exchange information.

Where applicable, an improved part will be substituted when a replacement is ordered. If the change is complex, your local Field Office or representative will contact you concerning the change.

MODULE EXCHANGE PROGRAM

This instrument was designed with a module exchange service approach. Service is performed by identifying a faulty module and exchanging it with a properly functioning module. This information details the process for obtaining a properly operating module from Tektronix. A list of the exchangeable modules is contained in the Replaceable Electrical Parts List.

NOTE

Module service and exchange should be performed by qualified service personnel only.

Module Exchange Service (US Customers)

To exchange a module, call Tektronix between the hours of 7:00 AM and 5:00 PM (Pacific Time) Monday through Friday, at the following telephone number:

(503) 627-7880 (for Service Assistance)
(800) 835-9433 (if unable to use the above number)

Please have the following information ready when you call:

- Instrument type
- Instrument serial number (located on the rear panel)
- Module part number
- Your shipping address
- Your billing address
- Resale number (for sales tax purposes)
- Preferred method of shipment
- Preferred shipper
- Is the instrument under warranty?

Module shipment will be made by your choice of carrier (for example, priority, express, one-day, overnight delivery, or common carrier service). After you receive the replacement module, the faulty module must be returned immediately to Tektronix via prepaid common carrier freight. Use the packaging material from the replacement module to prepare the faulty module for return shipment. A return shipping label will be furnished with the replacement module.

A standard fee is charged for each out-of-warranty module exchanged and will be quoted when the exchange module is requested. If the faulty module is not received at the Module Exchange Center within 30 days after the original request, the full price of the module will be charged.

Full price will also be charged for modules returned that do not qualify for the exchange rates. A module is not eligible for the exchange rates if it is

- damaged from repair attempts (other than by Tektronix),
- damaged from improper use or connection to incompatible equipment,
- modified by the customer,
- custom modified by Tektronix (by customer order).

Module Exchange Service (Outside the US)

Customers outside the United States should contact their local Tektronix sales subsidiary or distributor for details on servicing.

FIRMWARE VERSION AND ERROR MESSAGE READOUT

This feature provides readout of the firmware version when the power is cycled on and off. During the initial power-up cycle, the instrument firmware version is displayed on the screen for a short time. Firmware may be updated by replacing the ROMs. (Also see the information in this section titled 'Updating Firmware'.)

When an error occurs, a message appears on the screen describing the nature of the error. Status messages or prompts are also displayed when running a diagnostic test or self-correction routine. Descriptions of the on-screen messages are included in the Operators Manual. Descriptions and suggested corrective actions for service-related error messages are included in the troubleshooting part of this section.

REMOVING OR REPLACING SEMI-RIGID COAXIAL CABLES

Performance of the instrument may be degraded if the connectors on semi-rigid cables are loose, dirty, or damaged. The following procedure will help ensure that the connection is good enough to maintain proper performance.

1. Use a 5/16" open-end wrench to loosen or tighten the connectors. Use a second wrench to hold the rigid (receptacle) portion of the connector to prevent bending or twisting the cable.

2. Ensure that the plug and receptacle are clean and free of any foreign matter.

3. Insert the plug connector fully into the receptacle before screwing the nut on. Tighten the connection to 8 in-lbs. for SMA connectors and 5 in-lbs. for K connectors. Over-tightening will damage the connector.

NOTE

Removal of any assembly with K or SMA connectors in the signal path requires checking and re-adjusting flatness. If you do not have the equipment required to check flatness, we recommend returning the instrument to Tektronix for repair and adjustment.

TORQUE SPECIFICATION

Use the following torque specifications for connectors and screws to prevent instrument damage. Also, see the removal and replacement procedures for exceptions.

- SMA connectors are tightened to 8 in-lbs.
- K connectors are tightened to 5 in-lbs.
- Torx T-10 screws are tightened to 5 in-lbs unless otherwise noted.
- Pozidriv screws are tightened to 10 in-lbs unless otherwise noted.

REPLACING ASSEMBLIES

When replacing assemblies, prepare the instrument for service, and use Figures 4-14 and 4-15 as a guide to locate the assembly locations.

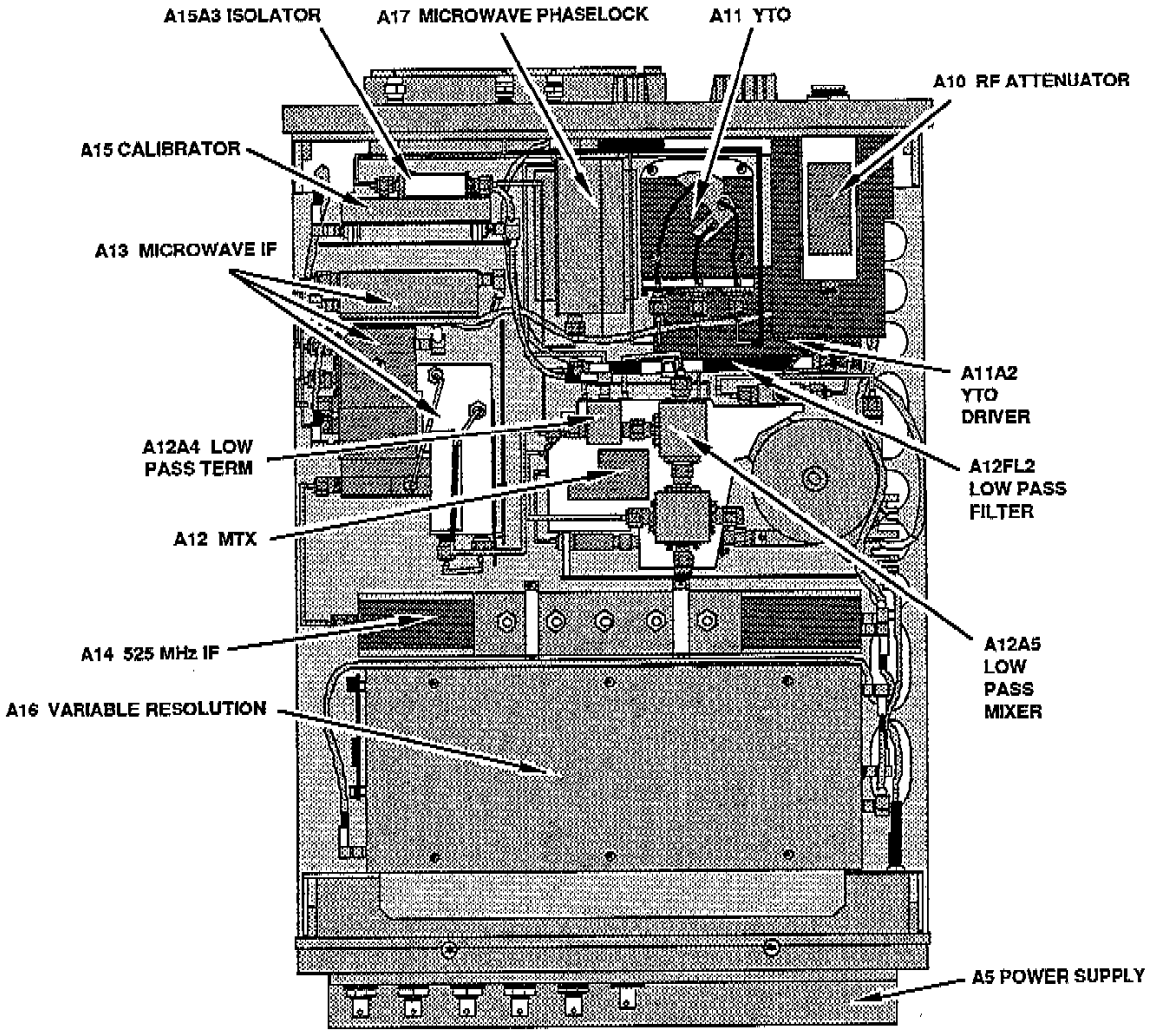


Figure 4-14. Bottom Deck (RF Assemblies).

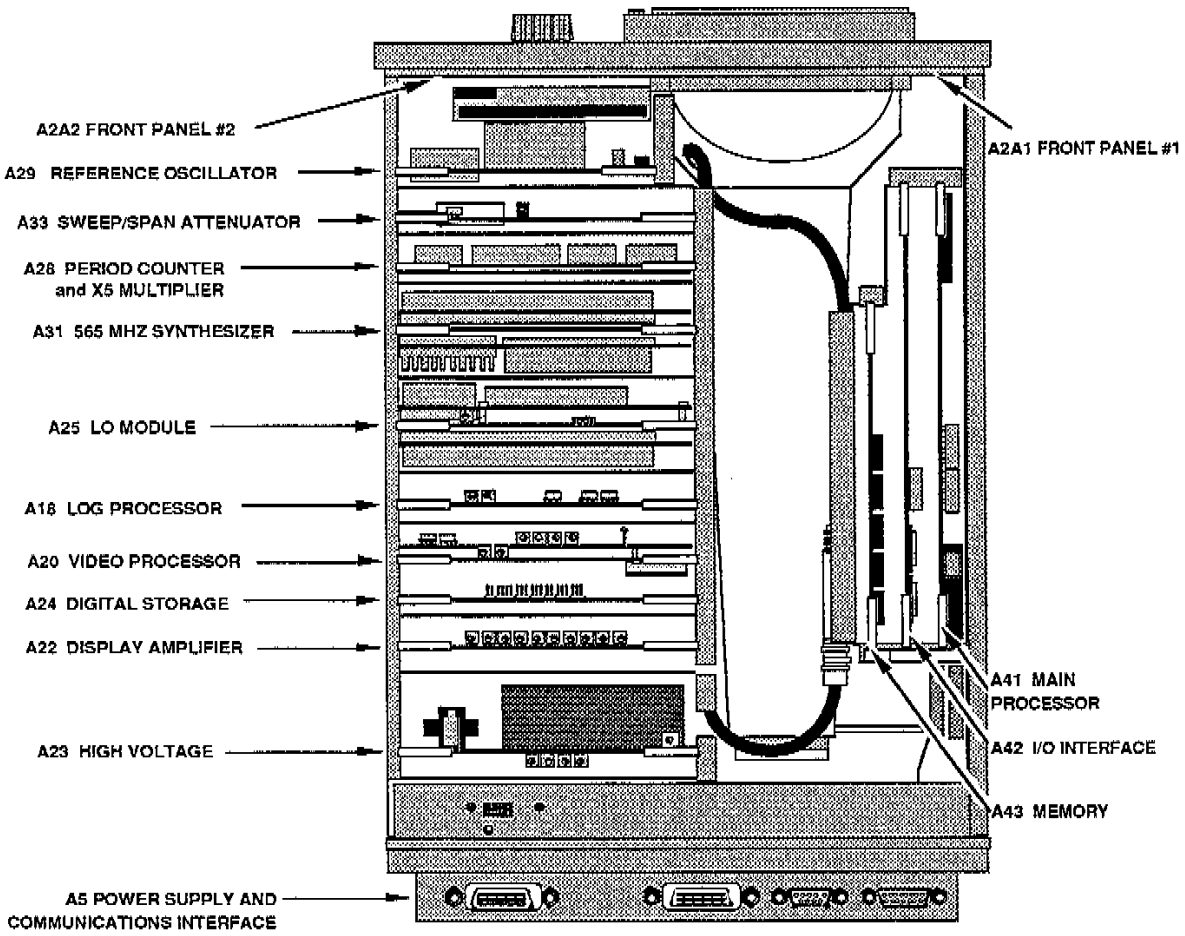


Figure 4-15. Top Deck assembly locations.

REPLACING THE RF ATTENUATOR (A10)

Removing the RF Attenuator

Refer to Figure 4-16 and remove the cable connecting the RF Attenuator to the Switched Diplexer as follows:

1. Disconnect the 5/16" K connector on the top of the Switched Diplexer.
2. Disconnect the K connector at the rear of the RF Attenuator and remove the cable.
3. Remove the ¾" nut from the front-panel RF INPUT 50 Ω connector. Then, gently pull the Attenuator assembly backwards to disconnect the circuit board connector from the Front-panel circuit board assembly. If needed, apply slight pressure on the corner of the Front-panel assembly. Be careful to not damage the YTO Driver assembly (A11A2) beneath the RF Attenuator.

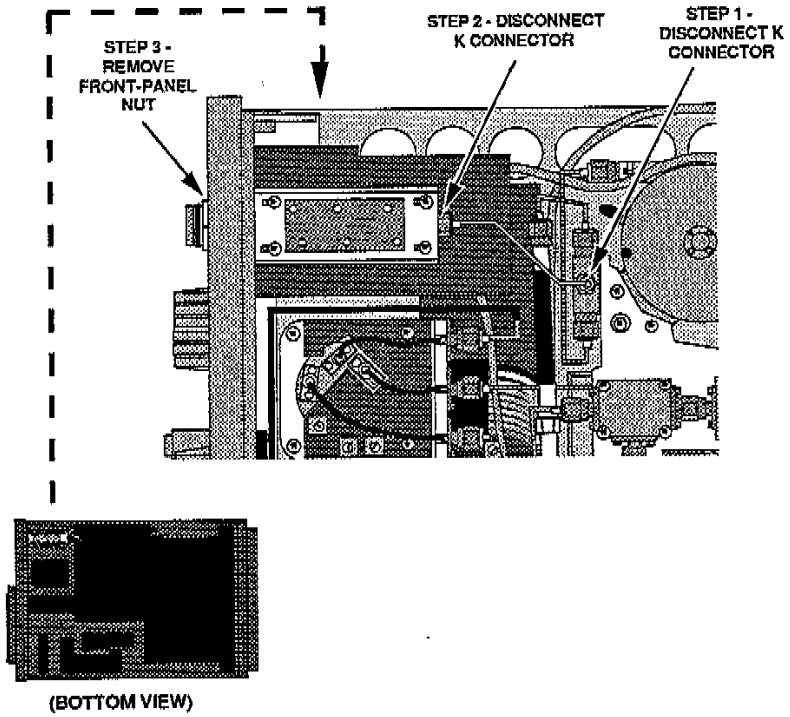


Figure 4-16. Steps to replace the RF Attenuator.

Installing the RF Attenuator

Reverse the removal procedure. Tighten the K connectors to 5 in-lbs. Do not over tighten.

Adjustment or correction is required after replacing the attenuator. Refer to Table 3-2, titled *Adjustments/ Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE MTX ASSEMBLY (A12)

Removing the MTX Assembly

The MTX assembly can be replaced as a unit. Individual subassemblies that may be replaced are the Low Pass Termination (A12A4), Low Pass Mixer (A12A5), and Low Pass Filter (A12FL2). Procedures for removing these items follow the main MTX removal procedure. Refer to Figures 4-14 and 4-15.

Use the following procedure to remove the MTX Assembly:

1. Disconnect the 5/16" K connector of the cable from the RF Attenuator (A10) to the MTX, and remove the cable.

2. Disconnect the SMA connector from the YTO (A11) at the YTO end.

3. Disconnect the K connector of the Low Pass Filter, FL100, from the Microwave IF at the MTX end.

NOTE

FL100 is an in-line filter contained in the semi-rigid cable from the 1st Converter to the Microwave IF. The filter area is near the connector attached to the Microwave IF and is indicated by black tubing on the cable. Do not bend this area when removing the cable.

4. Disconnect the External Mixer Input cable at the rear of the front-panel.

5. Disconnect the SMB connector from the Calibrator (A15) at the MTX end.

6. Remove the six Torx T-10 and two T-15 screws as shown in Figure 4-17. Use a T-10 screwdriver or bit with 3" clearance to reach the screws next to the 525 MHz IF (A14).

7. Remove the MTX assembly from the chassis. Be careful to not bend any semi-rigid coaxial cables. If necessary, loosen or remove connectors at their associated assemblies to provide clearance for the MTX assembly.

Installing the MTX Assembly

1. Reverse the removal procedure. Tighten SMA connectors to 8 in-lbs and K connectors to 5 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

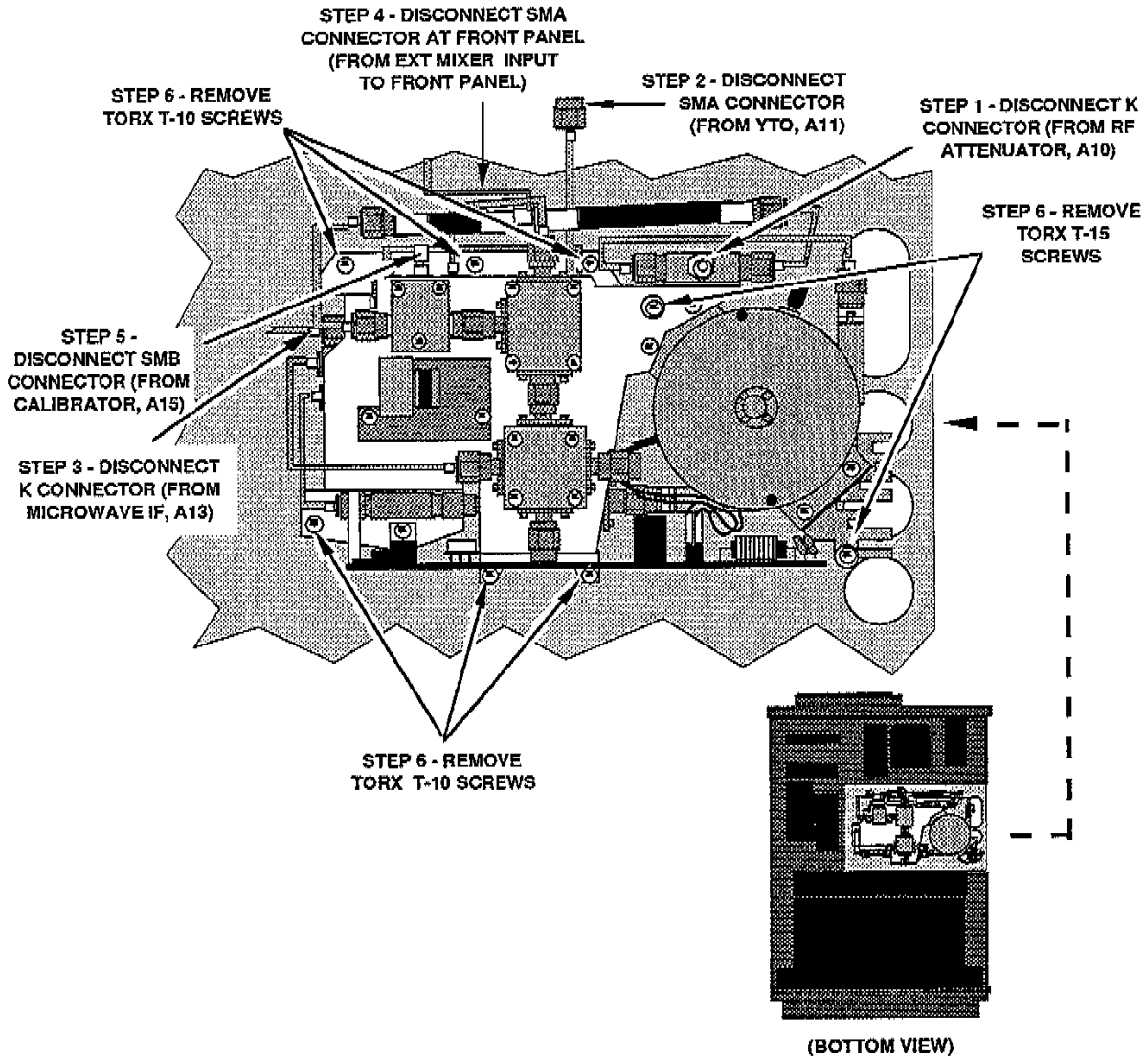


Figure 4-17. Steps to replace the MTX Assembly (A12).

Removing the MTX Low Pass Termination Assembly (A12A4)

1. Remove the three Pozidriv P1 screws from the top of the assembly.
2. Disconnect the two 5/16" SMA and one SMB connectors from the assembly.
3. Remove the assembly.

Installing the MTX Low Pass Termination Assembly

1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

Removing the MTX Low Pass Mixer Assembly (A12A5)

1. Remove the four Pozidriv P1 screws from the top of the assembly.

2. Disconnect the three 5/16" SMA connectors from the assembly.

3. Remove the assembly.

Installing the MTX Low Pass Mixer Assembly

1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

Removing the Low Pass Filter (A12FL2)

1. Disconnect the two 5/16" SMA connectors from the assembly.

2. Remove the assembly.

Installing the Low Pass Filter Assembly

1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE YTO ASSEMBLY (A11)

The YIG Tuned Oscillator (YTO), Assembly (A11) is replaceable as two units; the YTO with its interface board (A11) and the YTO Driver (A11A2). Refer to Figures 4-14 and 4-18.

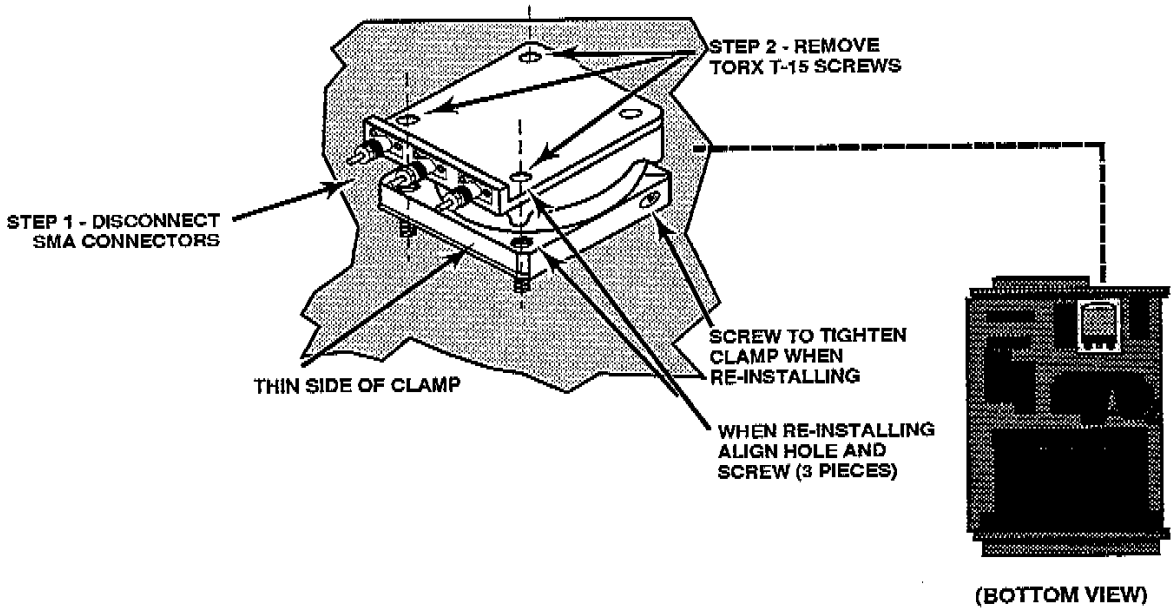


Figure 4-18. Steps to replace the YTO Assembly (A11).

Removing the YTO Assembly

1. Disconnect the three 5/16" SMA connectors from the YTO Assembly.
2. Remove the three Torx T-15 screws from the YTO Assembly.
3. Gently pull the YTO Assembly away from the chassis and disconnect the harmonica connector to the YTO Driver Assembly (A11A2).

Installing the YTO Assembly

1. Reverse the removal procedure. Tighten all SMA connectors to 8 in-lbs. Do not over tighten.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

Removing the YTO Driver Assembly (A11A2)

1. Remove the YTO (A11) and RF Attenuator (A10) assemblies using the previously described procedure.
2. Remove the five Torx T-10 screws mounting the YTO Driver Assembly circuit board.
3. Gently pull the YTO Driver Assembly away from the chassis to disconnect it from the Mother Board Assembly (A1).

Installing the YTO Driver Assembly

1. Reverse the removal procedure. When replacing the YTO and Attenuator assemblies, tighten all SMA connectors to 8 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE MICROWAVE IF ASSEMBLY (A13)

The Microwave IF Assembly (A13) is replaceable as a single item. The assembly consists of two sub-assemblies connected by cables. Both sub-assemblies must be replaced as a unit. Refer to Figure 4-19 for the steps to replace the assembly.

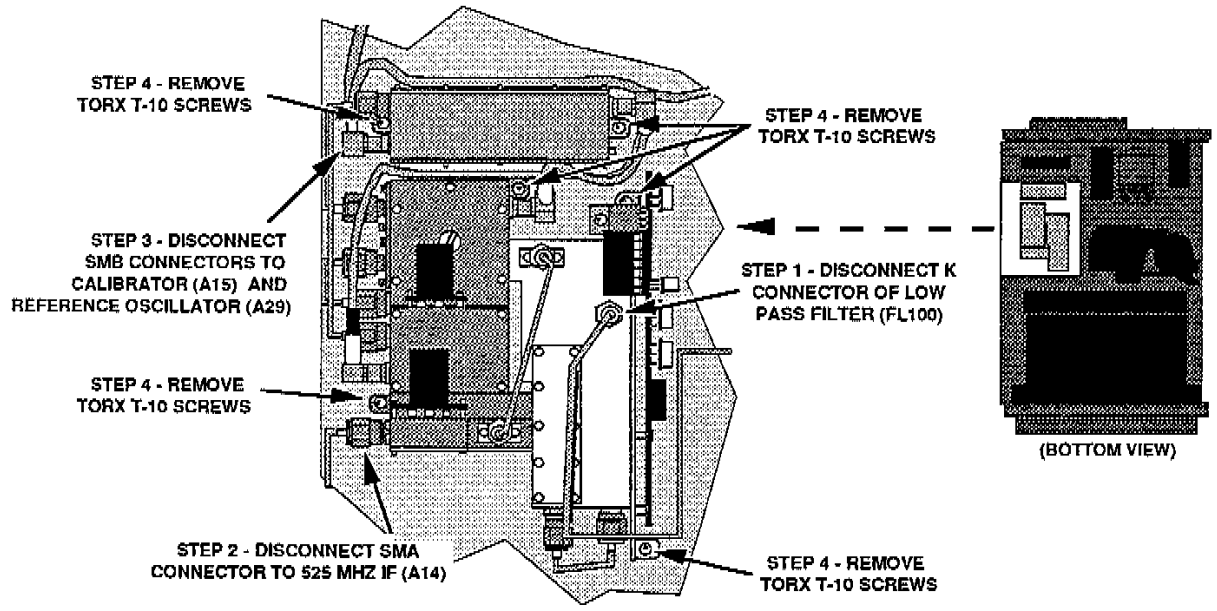


Figure 4-19. Steps to replace the Microwave IF Assembly.

Removing the Microwave IF Assembly

1. Disconnect the 5/16" K connector on the Low Pass Filter (FL100) connected to the assembly.

NOTE

FL100 is an in-line filter contained in the semi-rigid cable from the 1st Converter to the Microwave IF. The filter area is near the connector attached to the Microwave IF and is indicated by black tubing on the cable. When removing the cable do not bend this area.

2. Disconnect the SMA connector on the cable to the 525 MHz IF at the Microwave IF end.

3. Disconnect the two SMB connectors going to the Calibrator (A15) and Reference Oscillator (A29) at the Microwave IF end.

4. Remove the six Torx T-10 screws indicated in Figure 4-19.

5. Gently lift the main assembly by the circuit board to disconnect the connector from the Mother Board (A1), and remove the assembly with the remaining cables attached.

Installing the Microwave IF Assembly

1. Reverse the removal procedure. Tighten the SMA connectors to 8 in-lbs and the K connectors to 5 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE CALIBRATOR (A15) AND ISOLATOR ASSEMBLY (A15A3)

The Calibrator (A15) and Isolator (A14A3) are removed together. Refer to Figure 4-20.

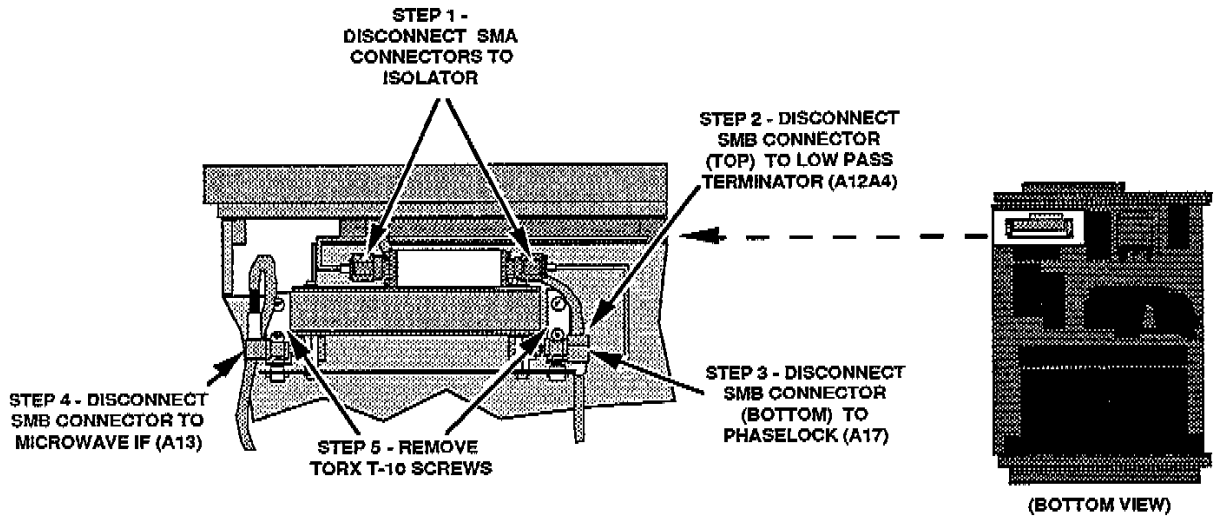


Figure 4-20. Steps to replace the Calibrator and Isolator.

Removing the Calibrator and Isolator

1. Disconnect the two SMA connectors to the Isolator Assembly.

2. Disconnect the SMB connector (top) to the Low Pass Terminator Assembly (A12A4) at the Calibrator end.

3. Disconnect the SMB connector (bottom) to the Microwave Phase lock Assembly (A17) at the Calibrator end.

4. Disconnect the SMB connector to the Microwave IF Assembly (A13) at the Calibrator end.
5. Remove the four Torx T-10 screws.
6. Gently lift the assembly to disconnect the connector from the Mother Board (A1).
7. Remove the four screws holding the Isolator (A15A3) to the Calibrator.

Installing the Calibrator and Isolator

1. Reverse the removal procedure. Tighten the SMA connectors to 8 in-lbs. Do not over tighten.
2. No adjustments or corrections are required after replacing this assembly.

REPLACING THE MICROWAVE PHASE LOCK ASSEMBLY (A18)

Refer to Figure 4-21 for the steps to replace the microwave phase lock assembly.

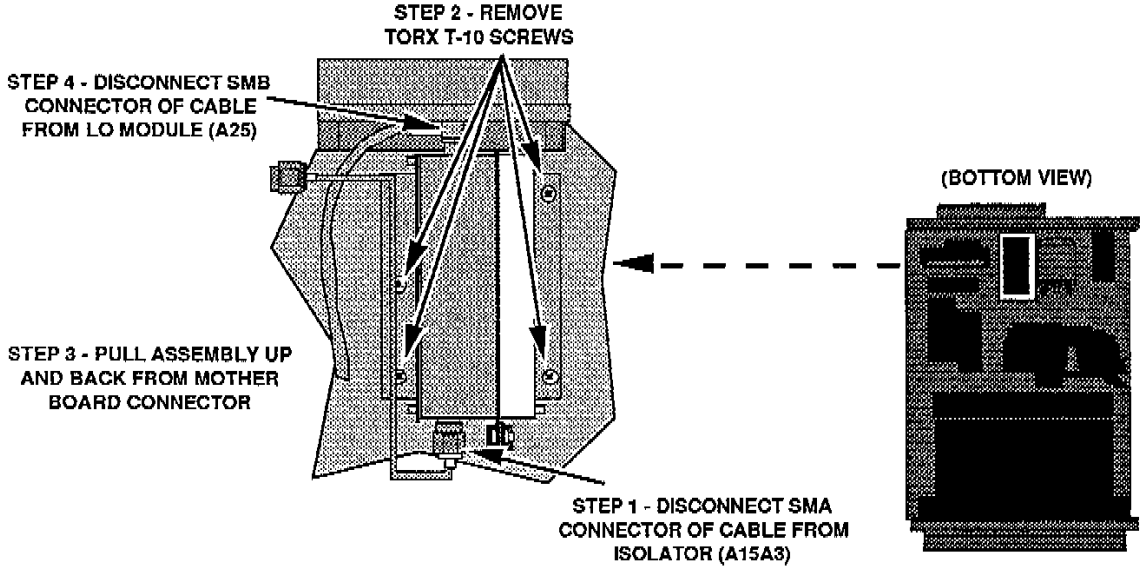


Figure 4-21. Steps to replace the Microwave Phase lock.

Removing the Microwave Phase lock

1. Disconnect the 5/16" SMA connector from the Isolator Assembly (A15A3) at the Microwave Phase lock end.
2. Remove the four Torx T-10 screws.
3. Gently lift the assembly up and then back to disconnect the connector from the Mother Board (A1).
4. Disconnect the SMB connector from the LO Module (A25) at the Microwave Phase lock end.

Installing the Microwave Phase lock

1. Reverse the removal procedure. Tighten the SMA connector to 8 in-lbs. Do not over tighten.

2. No adjustments or corrections are required after replacing this assembly.

REPLACING THE 525 MHZ IF (A14)

Refer to Figure 4-22 for the steps to replace the 525 MHz IF assembly.

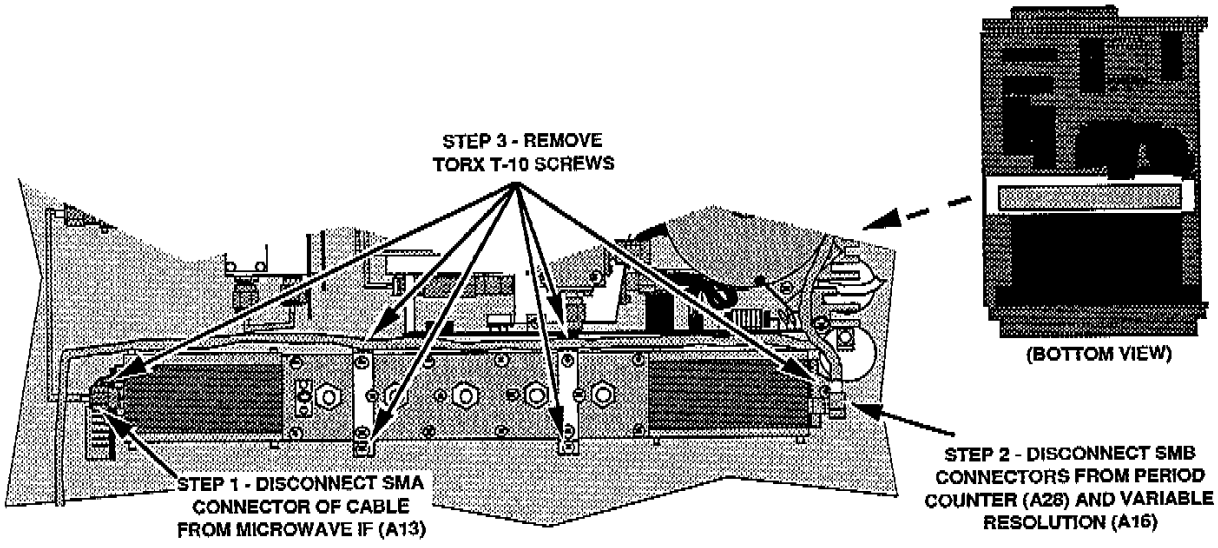


Figure 4-22. Steps to replace the 525 MHz IF.

Removing the 525 MHz IF

1. Disconnect the 5/16" SMA connector from the Microwave IF assembly (A13) at the 525 MHz IF end.

2. Disconnect the SMB connectors from the Period Counter Assembly (A28) and Variable Resolution Assembly (A16) at the 525 MHz IF end.

3. Remove the six Torx T-10 screws. Use a screwdriver with 3" long tip to reach the screws.

4. Gently lift the assembly to disconnect the connector from the Mother Board (A1).

Installing the 525 MHz IF

1. Reverse the removal procedure. Tighten the SMA connector to 8 in-lbs. Do not over tighten.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE VARIABLE RESOLUTION (VR) ASSEMBLY (A16)

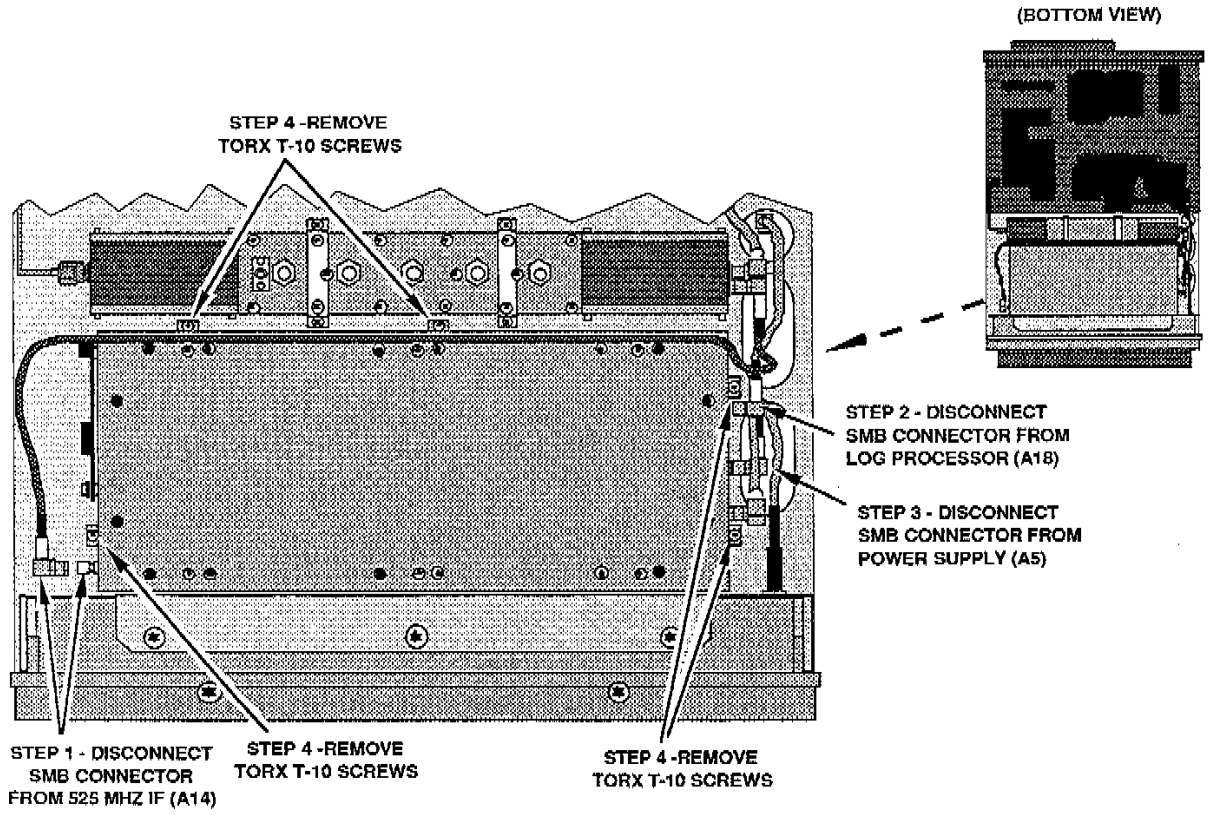


Figure 4-23. Removing the VR Assembly (A16).

Removing the VR Assembly

1. Disconnect the SMB connector from the 525 MHz IF Assembly (A14) at the VR end.
2. Disconnect the SMB connector from the Log Processor Assembly (A18) at the VR end.
3. Disconnect the SMB connector from the Power Supply (A5) at the VR end.
4. Remove the five Torx T-10 screws. Use a screwdriver with 3" long tip to reach the screws next to the 525 MHz IF (A14).
5. Gently lift the assembly to disconnect the connector from the Mother Board (A1).

Installing the VR Assembly

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REMOVING THE CARD CAGE COVERS

Circuit cards on the top side of the instrument are covered with metal shields. Separate shields cover the main card cage, the High Voltage assembly, and the processor system card cage. The main card cage shield and the High Voltage assembly shield hook over the outside edge of the card cage and are held by Torx T-10 screws on the inside edge of the card cage. The processor system shield is similar, but is secured with screws on both sides. The following figure shows the card cage covers and screw location.

CAUTION

When you remove the covers from the top deck, place a sheet of paper over the exposed assemblies to maintain proper air flow.

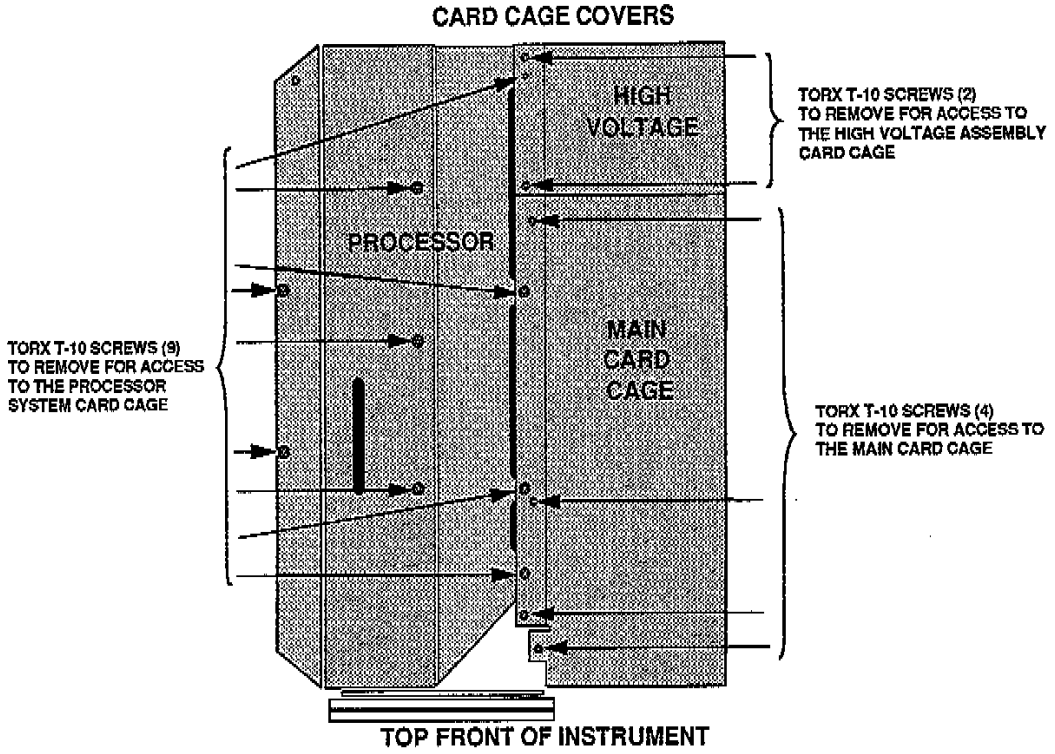


Figure 4-24. Removing the Card Cage covers.

NOTE

After removal of any of the boards, be sure the connector is properly aligned before seating the board. Improper alignment can result in damage to the connector.

REPLACING THE REFERENCE OSCILLATOR (A29)

Removing the Reference Oscillator

1. Remove the main card cage cover.
2. Disconnect the SMB connector on the bottom of the assembly, through the chassis hole on the RF deck side of the instrument.
3. Remove the assembly from the card cage using the circuit board levers.

Installing the Reference Oscillator

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE SWEEP/SPAN ATTENUATOR (A33)

Removing the Sweep/Span Attenuator

1. Remove the main card cage cover.
2. Remove the assembly from the card cage using the circuit board levers.

Installing the Sweep/Span Attenuator

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE PERIOD COUNTER (A28)

Removing the Period Counter

1. Remove the main card cage cover.
2. Disconnect the SMB connector on the bottom of the assembly, through the chassis hole on the RF deck side of the instrument.
3. Remove the assembly from the card cage using the circuit board levers.

Installing the Period Counter

1. Reverse the removal procedure.
2. No adjustments or corrections are required after replacing this assembly.

REPLACING THE 565 MHZ SYNTHESIZER (A31)

Removing the 565 MHz Synthesizer

1. Remove the main card cage cover.
2. Remove the assembly from the card cage using the circuit board levers.

Installing the 565 MHz Synthesizer

1. Reverse the removal procedure.
2. No adjustments or corrections are required after replacing this assembly.

REPLACING THE LO MODULE (A25)

Removing the LO Module

1. Remove the main card cage cover.
2. Disconnect the SMB connector on the bottom of the assembly, through the chassis hole on the RF deck side of the instrument.
3. Remove the assembly from the card cage using the circuit board levers.

Installing the LO Module

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE LOG PROCESSOR (A18)

Removing the Log Processor

1. Remove the main card cage cover.
2. Disconnect the SMB connector on the bottom of the assembly, through the chassis hole on the RF deck side of the instrument.
3. Remove the assembly from the card cage using the circuit board levers.

Installing the Log Processor

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE VIDEO PROCESSOR (A20)

Removing the Video Processor

1. Remove the main card cage cover.
2. Remove the assembly from the card cage using the circuit board levers.

Installing the Video Processor

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE DIGITAL STORAGE (A24)

NOTE

Firmware ROMs can be ordered separately from the boards. If only ROMs are needed, order the replacement set. ROMs are included with a replacement board.

Removing the Digital Storage

1. Remove the main card cage cover.
2. Remove the assembly from the card cage using the circuit board levers.
3. Remove the firmware ROM from the board using an IC extraction tool. See *Updating Firmware*, later in this section, for ROM locations.

Installing the Digital Storage

1. Reverse the removal procedure.
2. If you are replacing the Digital Storage firmware ROM, U11 see *Updating Firmware*, later in this section, for the ROM location.
3. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE DISPLAY AMPLIFIER (A22)

Removing the Display Amplifiers

1. Remove the main card cage cover.
2. Remove the two harmonica connectors on the left side of the board through the opening in the card cage.
3. Remove the assembly from the card cage using the circuit board levers.

Installing the Display Amplifiers

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE HV POWER SUPPLY (A23)

During the adjustment steps of this procedure it will be necessary to discharge the CRT anode lead. Use the following procedure to discharge the CRT anode lead.

WARNING

The CRT anode lead retains a high voltage charge after the instrument is turned off. To avoid electrical shock or damage to other circuit components, discharge the anode lead as follows.

1. Disconnect the ceramic connector above the CRT, refer to Figure 4-25 (A).
2. Separate the connector by pulling on the male (plastic) connector.
3. Insert the metal end of the male connector into one of the empty holes at the top of the card cage, refer to Figure 4-25 (B). Be certain the metal connector is touching the chassis.
4. Insert the blade of an insulated screwdriver into the female connector and short the blade to the chassis, refer to Figure 4-25 (B).

NOTE

Allow at least five minutes to discharge the male connector.

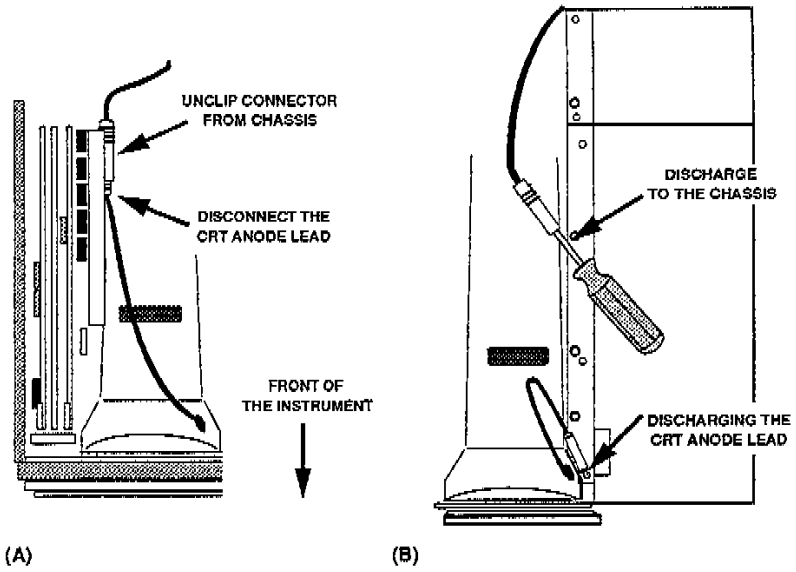


Figure 4-25. Discharging the CRT anode lead to the chassis.

Removing the HV Power Supply

1. Disconnect the multi-pin connector from the top of the assembly.
2. Unseat the assembly from the Mother Board connector using the two board levers, and gently lift out of the card cage until two more multi-pin connectors on the CRT side of the assembly are accessible.
3. Disconnect the two remaining multi-pin connectors.
4. Remove the assembly from the card cage.

Installing the HV Power Supply

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE MAIN PROCESSOR SYSTEM BOARDS (A41, A42, and A43)

The Main Processor System consists of the Main Processor (A41), the I/O Interface (A42), and the Memory (A43) – all located in the Main Processor card cage and the Communications Interface (A5A6), which is physically located in the Power Supply assembly (A5). This procedure is for the card cage assemblies only. A separate procedure for replacing the Communications Interface is described with the Power Supply assemblies.

CAUTION

Check the position of jumper J10 before installing a replacement module. Replacement modules are stored with the jumper in the Secure position (pins 2 & 3) to extend the battery life. The jumper must be in the Normal position (pins 1 & 2) to activate storage.

NOTE

Firmware ROMs must be ordered separately from the boards. ROMs are not included with a replacement board.

Saving Operating System Data

Instrument data is stored in NVRAM and in EEPROM. The calibration data is in EEPROM, while user settings, and waveforms are in NVRAM.

If the A42 I/O Interface module is replaced during servicing, the data stored in NVRAM and EEPROM must be transferred from the old module to the new one. Two software programs (Dump and Restore) are provided to transfer this data.

If necessary, refer to *SECTION 3 COMPUTER SETUP AND SOFTWARE INSTALLATION* in *PART II. AMPLITUDE FLATNESS ADJUSTMENT PROCEDURE* for information concerning connecting and using the personal computer with these programs.

To use these programs when replacing the A42 I/O Interface module, with the old I/O Interface module installed, type the following on the personal computer:

278X<ENTER>

The 278X program is a menu driven program which requires entry of test conditions and test selections. Complete the following steps to run the Dump/Restore program.

1. Enter your name or your cal labs name.
2. Verify the date and time.
3. Enter temperature and humidity information.
4. Select Device Under Test (DUT). Enter selection number to select the 278X model you are testing.
5. Enter the selection number 3 for TS (Troubleshooting).
6. Enter the DUT serial number and press <ENTER>. You will be asked to enter this a second time to verify correct entry of the serial number.
7. Choose which tests are to be performed in the sequence. Enter 3 for Select Test(s).
8. Specify Test: select "Dump NVRAM/EEPROM Files".
9. Select "1. ALL FILES". This will create a new directory \tekcats\dump\278x\1 (where 278x is the instrument being tested) and creates a file for each type of data.

10. After replacing the A42 I/O Interface module run "Restore NVRAM/EEPROM Files" and select "1. ALL FILES". The data on disk will be restored into NVRAM and EEPROM on the new I/O Interface module.

NOTE

In addition to this application, Dump can be used to backup NVRAM and EEPROM data so that data can be restored in event of a future problem that results in loss of NVRAM and/or EEPROM data.

Removing the Main Processor System Boards

1. Remove the processor card cage cover.
2. Remove the desired assembly from the card cage using the circuit board levers.
3. If the ROMs are to be replaced, remove the old ROMs from the board using an IC extraction tool. See *Updating Firmware*, later in this section, for locations.

Installing the Main Processor System Boards

1. Reverse the removal procedure.
2. Duplicate the switch settings from old to new board. See *Switches and Jumpers* later in this section.
3. Replace the firmware ROMs to their proper sockets. See *Updating Firmware*, later in this section, for ROM locations.
4. No adjustments or corrections are required after replacing the A41 Main Processor or A43 Memory assemblies. However, because the A42 I/O Interface contains the correction data, the entire adjustment/correction procedure, including flatness, must be performed if that assembly is replaced. Refer to the Adjustment/Correction section of this manual.

REPLACING THE LOW VOLTAGE POWER SUPPLY AND COMMUNICATIONS INTERFACE (A5)

Removing the LV Power Supply

1. Remove the three Torx T-10 screws attaching the Power Supply to the bottom rear chassis bracket as per Figure 4-26.
2. Remove the four Pozidriv screws attaching the Power Supply to the side rails at the rear of the chassis.
3. With the instrument right side up, move the assembly away from the chassis, then disconnect the three multi-conductor cables from the Mother Board (A1) at locking connectors A1J22, A1J23, and A1J24.
4. Disconnect the SMB connector as illustrated in Figure 4-26 and remove the Power Supply assembly.

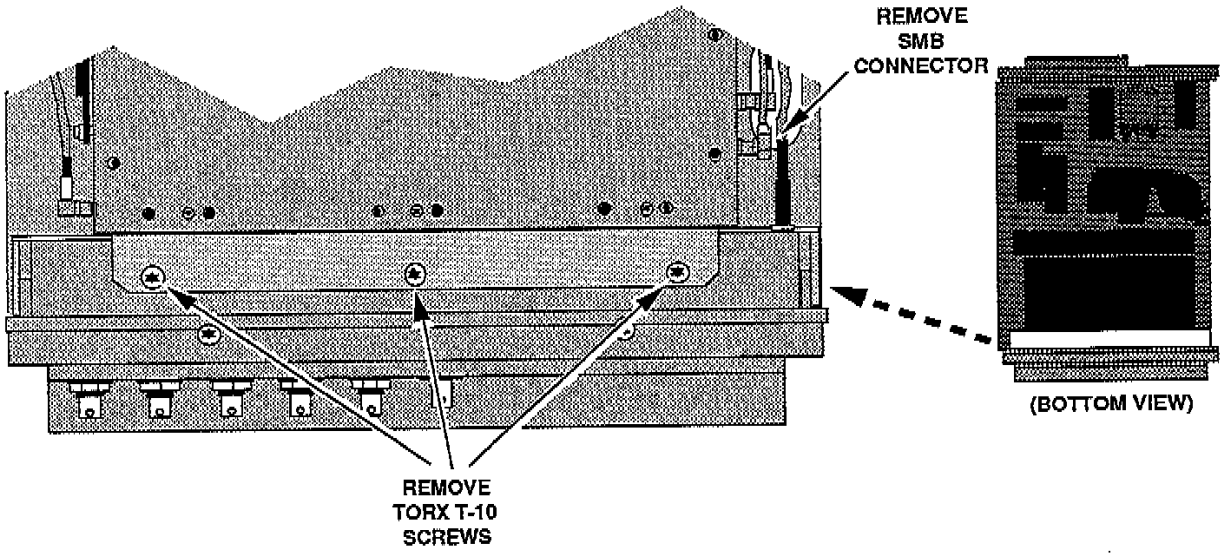


Figure 4-26. Power Supply removal.

Installing the LV Power Supply

Reverse the removal procedure.

Disassembling the LV Power Supply Halves

1. Open the Power Supply assembly by removing the four Torx T-10 screws from the top and bottom of the assembly.

2. Disconnect the SMB connector on the end of the IF OUT coaxial cable, A5W516.

NOTE

Note the routing of the IF OUT cable for reassembly.

Assembling the LV Power Supply Halves

Reverse the disassembly procedure keeping in mind the routing of the IF OUT cable.

Replacing the Thermal Fuse (A5A1F10)

WARNING

The Thermal Fuse opens at a temperature of approximately 98° C. Let the instrument cool to a safe temperature before replacing the Thermal Fuse.

1. Disassemble the Power Supply halves using the previously described procedure.

2. Use pliers to remove the Thermal Fuse (A5A1F10). See Figure 4-27.

3. Install the replacement fuse in the socket.

4. Re-assemble the Power Supply halves.

5. Re-install the Power Supply.

6. No adjustments or corrections are required after replacing this assembly.

CAUTION

To avoid instrument damage, determine why the instrument overheated before re-applying power for long periods. Check for sufficient clearance around the air vents or electrical problems that might be causing the temperature rise.

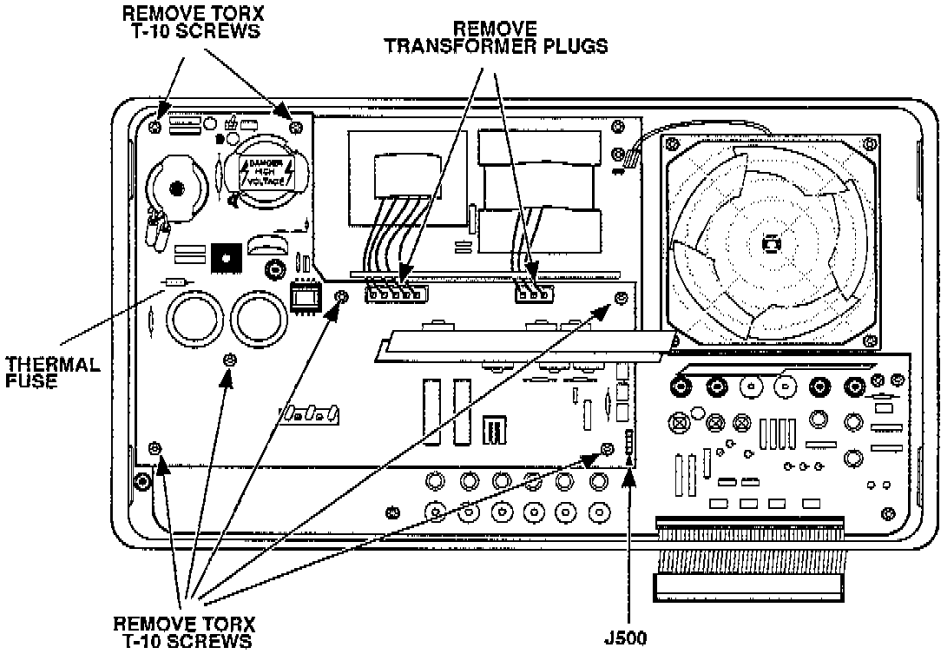


Figure 4-27. Removing the Power Supply Primary board and location of the thermal fuse.

Removing the Primary Board (A5A1)

1. Remove the Low Voltage Power Supply and Communications Interface assembly (A5) from the instrument as described earlier in this section.

2. Disassemble the Power Supply halves as previously described.

3. Remove the seven Torx T-10 screws from the Primary board.

3. Disconnect the two multi-pin transformer plugs.

4. Gently lift the Primary board at the end nearest the fan to disconnect connector J500 from the Secondary board (J500 is between the two boards). See Figure 4-27.

5. Continue lifting on the fan end until the board clears the heat sink on the Secondary board. Then remove the Primary board.
6. Remove the plastic insulating sheet from the bottom of the assembly.
7. Note the switch positions for re-installation.

Installing the Primary Board (A5A1)

1. Replace the plastic insulator sheet on the standoffs.
2. Place the wide end of the Primary board under the indents at the end of the Power Supply chassis.
3. Connect the fan end of the Primary board to connector J500 on the Secondary board.
4. Replace the seven Torx T-10 screws.
5. Connect the two transformer multi-pin connector cables.
6. Set the switches to the positions noted when removing the board.
7. Assemble the Power Supply halves (separate procedure).
8. Install the Power Supply in the instrument (separate procedure).
9. No adjustments or corrections are required after replacing this assembly.

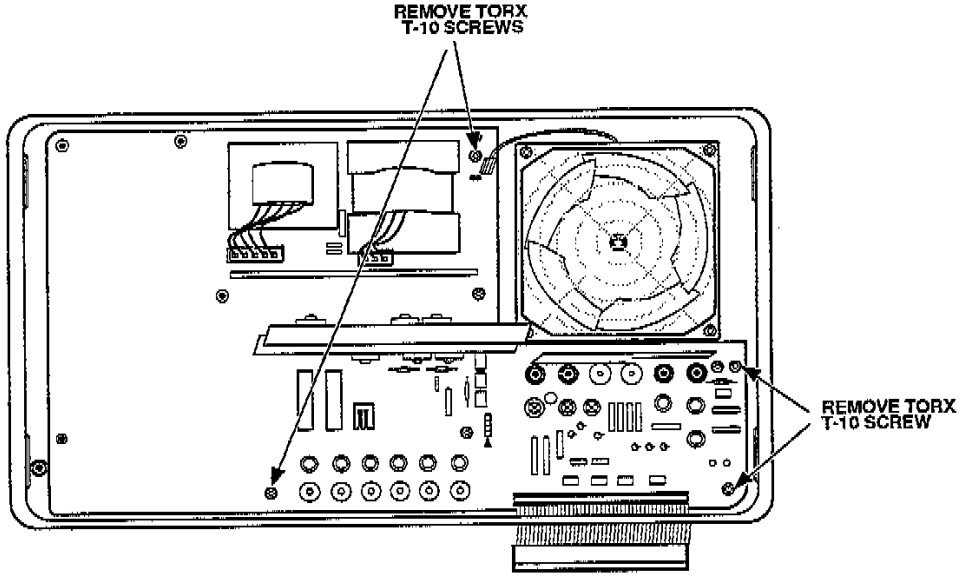


Figure 4-28. Removal of the Power Supply Secondary board.

Removing the Secondary Board (A5A2)

1. Remove the Power Supply assembly (A5) from the instrument (see separate procedure).
2. Disassemble the Power Supply halves (see separate procedure).
3. Remove the Primary board (see separate procedure).
4. Disconnect the Fan connector.
5. Remove the four Torx T-10 screws as shown in Figure 4-28.

Installing the Secondary Board (A5A2)

1. Replace the Secondary board and the four Torx T-10 screws in the positions shown in the illustration.
2. Connect the Fan connector. Note that pin 1 is indicated with an arrow.
3. Replace the Primary board (separate procedure).
4. Assemble the Power Supply halves (separate procedure).
5. Install the Power Supply in the instrument (separate procedure).
6. No adjustments or corrections are required after replacing this assembly.

Removing the Communications Interface (A5A6)

1. Remove the Low Voltage Power Supply and Communications Interface assembly (A5) from the instrument as described earlier in this section.
2. Disassemble the Power Supply halves (see separate procedure).
3. Disconnect the multi conductor cable connector from the rear panel BNC Interface board (A5A7). See Figure 4-29.
4. Remove the four 5/32" nuts from the PORT 1 and PORT 2 connectors at the top of the frame.
5. Remove the four 3/16" nuts from the INSTRUMENT BUS and ACCESSORY connectors at the top of the frame.
6. Remove the two Torx T-10 screws from the board.
7. Remove the Communications Interface board.

Installing the Communications Interface (A5A6)

1. Reverse the removal procedure.
2. No adjustments or corrections are required after replacing this assembly.

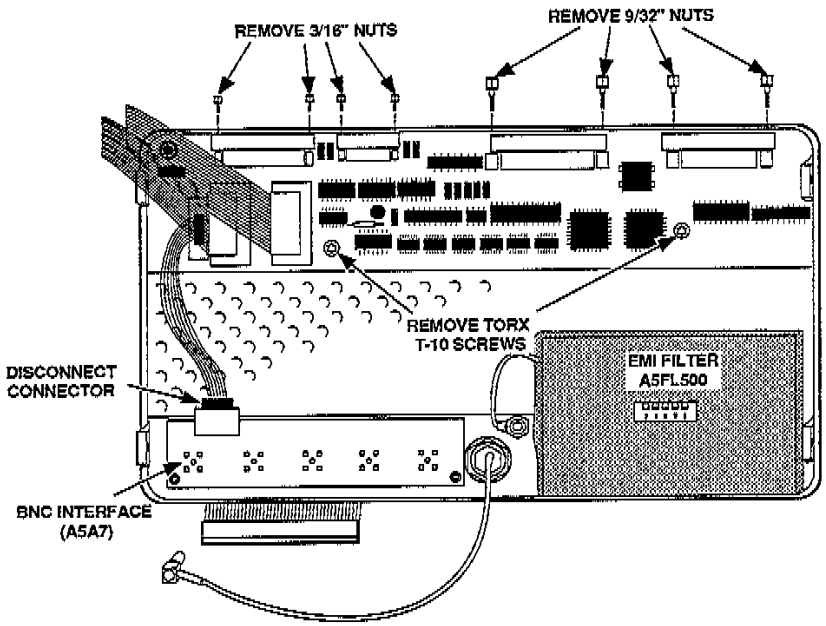


Figure 4-29. Communications Interface removal.

Removing the Rear Panel BNC Interface (A5A7)

1. Remove the Low Voltage Power Supply and Communications Interface assembly (A5) from the instrument as described earlier in this section.
2. Disassemble the Power Supply halves as previously illustrated in this section.
3. Disconnect the multi conductor cable connector. See Figure 4-29.
4. Remove the nuts from the five BNC connectors.
5. Remove the BNC Interface board.

Installing the Rear Panel BNC Interface (A5A7)

1. Reverse the removal procedure.
2. No adjustments or corrections are required after replacing this assembly.

Removing the Fan (A5B100)

1. Remove the Low Voltage Power Supply and Communications Interface assembly (A5) from the instrument (see separate procedure).

2. Disassemble the Power Supply halves as previously illustrated in this section.

3. Remove the Primary board as previously illustrated in this section.

4. Disconnect the fan power multi-pin connector to the Secondary board. Note the wire positions.

5. Remove the four 7/64" Allen head screws holding the fan housing and remove the fan.

Installing the Fan (A5B100)

1. Reverse the removal procedure making sure the fan is positioned with the label facing the inside of the assembly.

2. No adjustments or corrections are required after replacing this assembly.

Removing the EMI Filter (A5FL500)

1. Remove the Low Voltage Power Supply and Communications Interface Assembly (A5) from the instrument and separate the halves (see previous procedures).

2. Remove the nut from the green-yellow ground wire.

3. Remove the two Torx T-10 screws at the sides of the power input connector as indicated on Figure 4-30.

4. Remove the EMI filter.

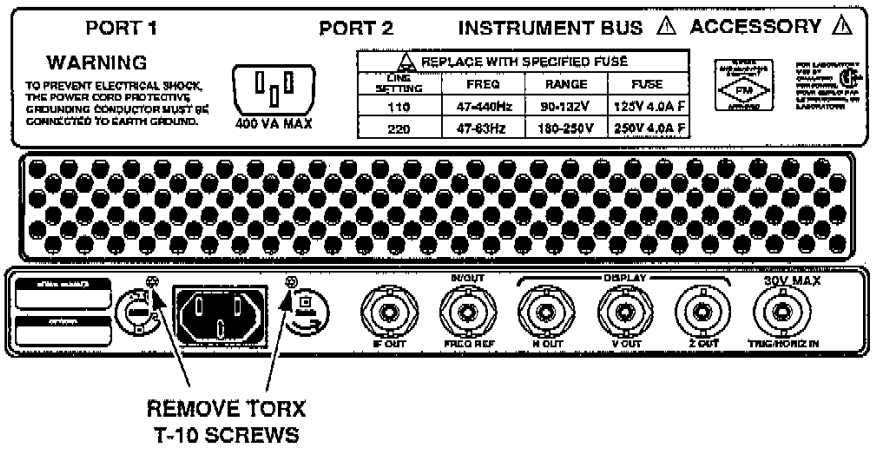


Figure 4-30. Line filter removal.

Installing the EMI Filter (A5FL500)

1. Reverse the removal procedure.

2. Check that the Line Selector position and fuse are set to the correct voltage.

3. No adjustments or corrections are required after replacing this assembly.

REPLACING THE COLOR SHUTTER, CRT BEZEL, AND CRT ASSEMBLY

Removing the Color Shutter and CRT Bezel

1. Remove the two Torx T-10 screws from the bottom of the CRT bezel.
2. Lift the bezel away from the CRT and disconnect the multi-pin connector.

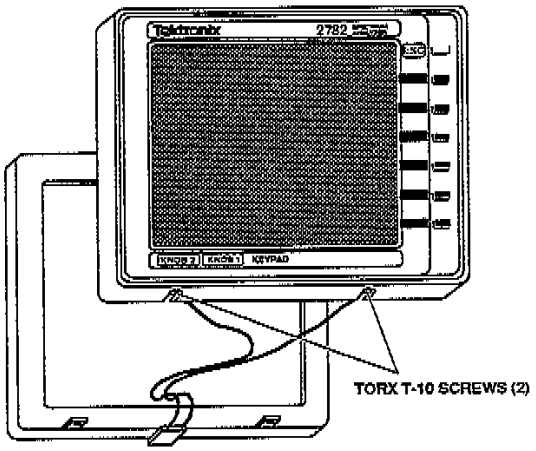


Figure 4-31. Removing the Color Shutter and CRT Bezel.

Installing the Color Shutter and CRT Bezel

1. Connect the multi-pin connector.
2. Hook the top of the bezel over the indents in the frame and align the push-button into position.
3. Push the bezel into position while checking for proper clearance for the wires and push-button.
4. Install the two Torx screws.
5. No adjustments or corrections are required after replacing this assembly.

Replacing the CRT

WARNING

The CRT anode lead retains a high voltage charge after the instrument is turned off. To avoid electrical shock or damage to other circuit components, discharge the anode lead as follows.

1. Disconnect the ceramic connector above the CRT, refer to Figure 4-32 (A).
2. Separate the connector by pulling on the male (plastic) connector.
3. Insert the metal end of the male connector into one of the empty holes at the top of the card cage, refer to Figure 4-32 (B). Be certain the metal connector is touching the chassis.

4. Insert the blade of an insulated screwdriver into the female connector and short the blade to the chassis, refer to Figure 4-32 (B).

NOTE

Allow at least five minutes to discharge the male connector.

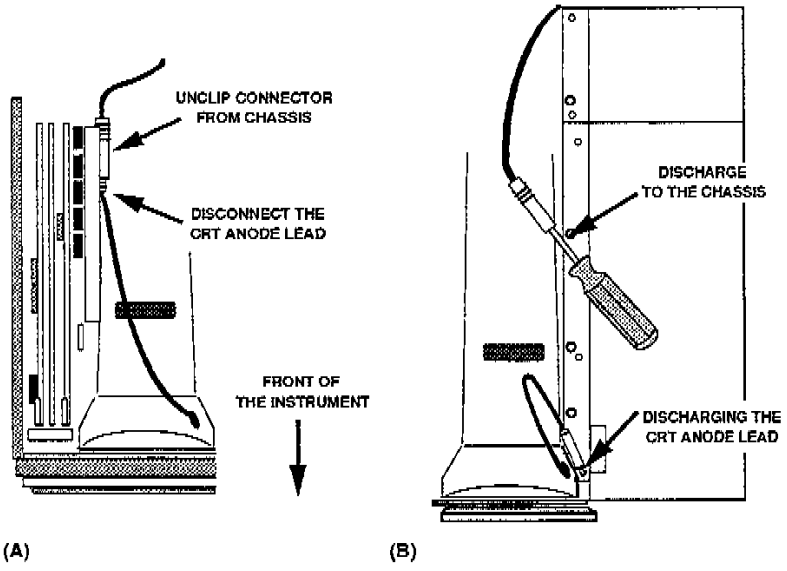


Figure 4-32. Discharging the CRT anode lead to the chassis.

Removing the CRT and Trace Rotation Coil

Refer to Figures 4-33, and 4-34 while performing this procedure.

1. Remove the Processor System card cage cover to gain access to the CRT anode connector, and then discharge the CRT anode connector as described in Figure 4-32.

2. Remove the Low Voltage Power Supply and Communications Interface assembly (A5) as previously described. This gives access to the CRT socket.

3. Remove the CRT socket. Be careful to not bend the CRT pins. This could result in an implosion or loss of vacuum in the CRT.

4. If replacing the Trace Rotation Coil, disconnect its multi-pin connector from the side of the Display Amplifier assembly. Note the location of pin 1 for use when re-installing the CRT.

5. Remove the horizontal and vertical deflection connectors from the CRT neck. Note the location of the red connector for use when re-installing the CRT. Be careful to not bend the CRT neck pins.

6. Remove the Color Shutter and CRT Bezel assembly as was described earlier in this procedure.

7. To remove CRT, remove the eight screws from the CRT frame. Then, remove the CRT frame, polycarbonate window, and mylar shim from the CRT. Then, remove the CRT from the shield. The CRT retainers will come out of the shield with the CRT. Place the CRT retainers aside.

NOTE

The upper left and lower right CRT retainers are different from the upper right and lower left retainers. Two are black and two are gray. During re-assembly, be sure they are returned to their proper location for correct alignment

8. If replacing the Trace Rotation coil, remove it from inside the CRT shield.

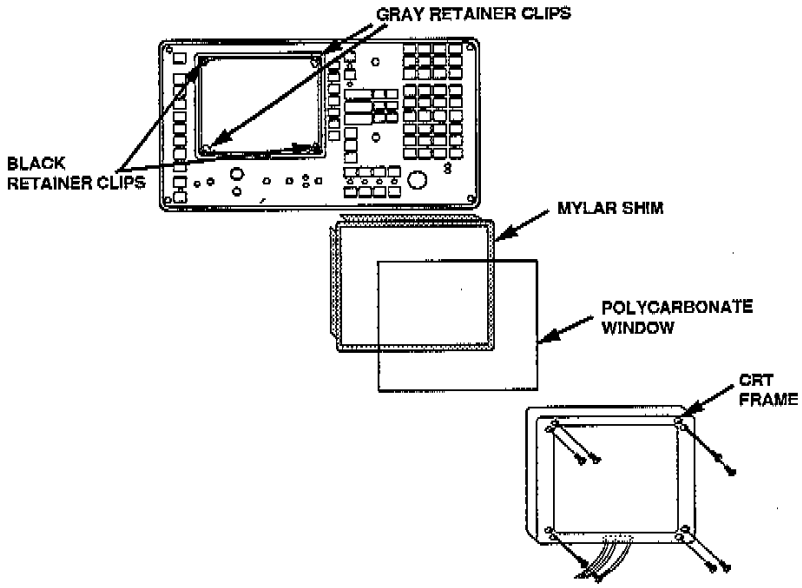


Figure 4-33. CRT Front-panel assembly sequence.

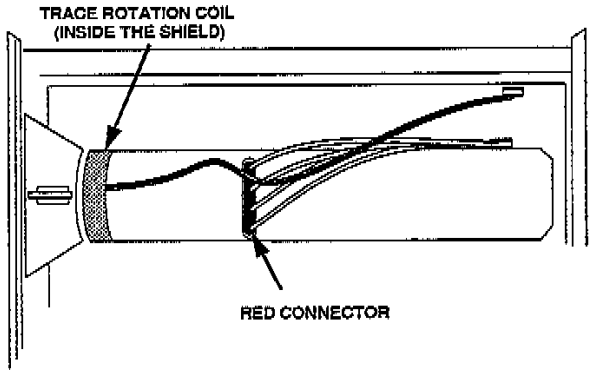


Figure 4-34. Location of the Trace Rotation coil.

Installing the CRT and Trace Rotation Coil

Observe the same precautions as when removing the CRT.

1. Reverse the removal procedure, except when replacing the CRT frame and retainers, make sure the retainers are in the proper places, and use the following procedure:

   Center the polycarbonate window in the CRT frame, and tighten the four inner Torx screws to 10 in-lbs each.

   Adjust the retainers screws in a diagonal pattern around the frame to bring the retainers into place to keep the CRT properly aligned and mechanically stable. Tighten the screws to 10 in-lbs. Do not over-tighten.

   NOTE

   Be sure that all optical surfaces are clean and lint-free before re-installing the CRT and color shutter.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

REPLACING THE FRONT-PANEL ASSEMBLIES

Removing the Front-panel (with CRT Attached)

1. Remove the RF Attenuator (A10) and the cable attaching it to the 1st Converter (A12 MTX). (See separate procedure for replacing the Attenuator.)

   CAUTION

   Removing the RF Attenuator is recommended to avoid possible damage to the attenuator and cable while replacing the front-panel.

2. Disconnect the three 5/16" SMA connectors from the cables to the front-panel REF SIGNAL OUT, LO OUTPUT, and EXTERNAL MIXER connectors.

3. Remove the two Torx T-10 screws that attach through the chassis bottom to the CRT frame.

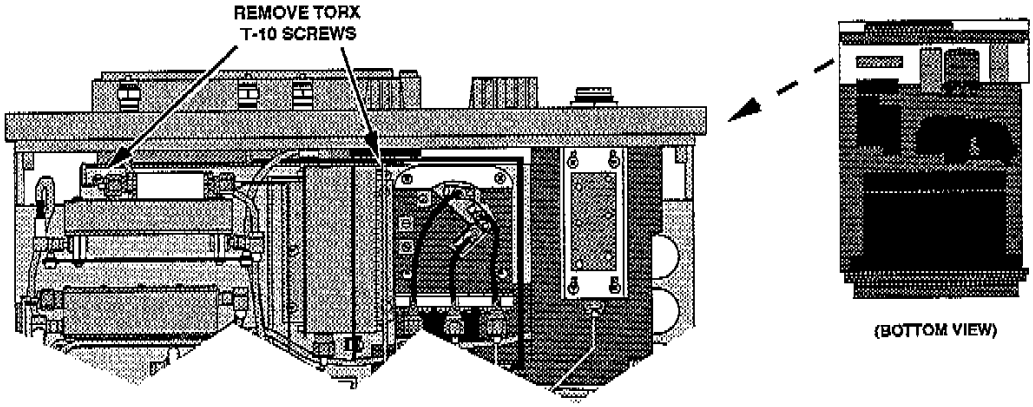


Figure 4-35. Removing the screws from the CRT shield.

4. Turn the instrument as necessary to work on the top side of the instrument (card cage side).

5. Remove the Processor System card cage cover to allow disconnecting the anode lead connector.

6. Disconnect the CRT anode lead and immediately discharge it to the main chassis as follows:

WARNING

The CRT anode lead retains a high voltage charge after the instrument is turned off. To avoid electrical shock or damage to other circuit components, discharge the anode lead.

•Disconnect the ceramic insulator above the CRT; refer to Figure 4-32 (A).

•Separate the connector by pulling on the male (plastic) connector.

•Insert the metal end of the male connector into one of the empty holes at the top of the card cage, refer to Figure 4-32 (B). Be certain the metal connector is touching the chassis.

•Insert the blade of an insulated screwdriver into the female connector and short the blade to the chassis, refer to Figure 4-32 (B).

NOTE

Allow at least five minutes to discharge the male connector.

7. Remove the High Voltage card cage cover and disconnect the multi-pin connectors that go to the CRT socket from the High Voltage assembly.

8. Disconnect the two top multi-pin connectors on the side (through the card cage) of the Display Amplifier assembly (A22). All CRT leads should now be disconnected.

9. Disconnect the SMB connector on the bottom of the assembly, through the chassis hole, from the RF deck side of the instrument.

10. Disconnect the connector from the Mother board to the front-panel, see Figure 4-36.

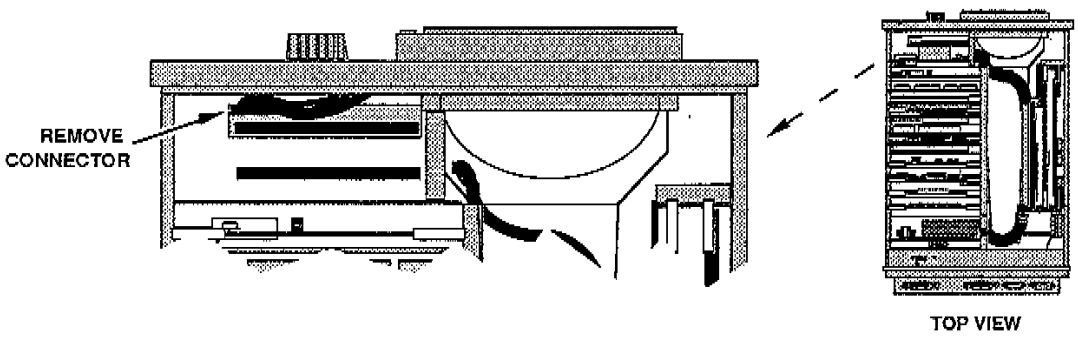


Figure 4-36. Removing the connector from Mother board to Front-panel.

11. Disconnect the multi-conductor connector from the right front of the Mother Board (A1). The other end of this cable is soldered to the Right Front-panel assembly (A2A2). This is to gain access to the screw at the top of the CRT shield. See Figure 4-37.

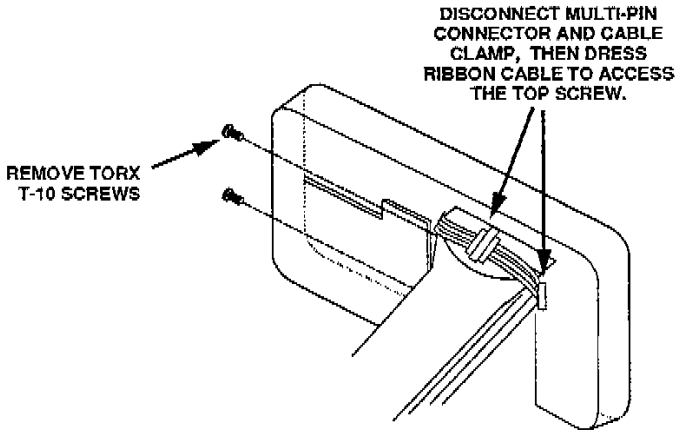


Figure 4-37. Removing the screws from the CRT shield and chassis.

12. Undo the multi-conductor cable clamp on the top of the CRT shield, then disconnect the end of the multi-conductor cable going to the smaller (Left) Front-panel assembly (A2A1).

13. Move this multi-conductor cable to the right to provide access to the two Torx T-10 screws going through the card cage side to the right side of the CRT frame.

14. Remove the two screws, using a long shaft or right angle driver.

15. Remove the four Pozidriv screws from the main chassis side rail where they attach to the front-panel frame, two from each side.

16. Pull the assembly up and forward to remove the Front-panel assembly (A2).

Removing the Left (small) Front-panel Assembly (A2A1)

1. Remove the front-panel assembly as discussed above.
2. Make sure the multi-conductor cable between the two front-panel boards is disconnected from the smaller assembly. (It should already be disconnected after the previous procedure.)
3. Remove the five Torx T-10 screws from the assembly as shown in Figure 4-38.
4. Place the assembly face down (CRT up) and remove the board (A2A1) from the assembly. Do not disturb the front-panel frame or push-button while the board is removed.

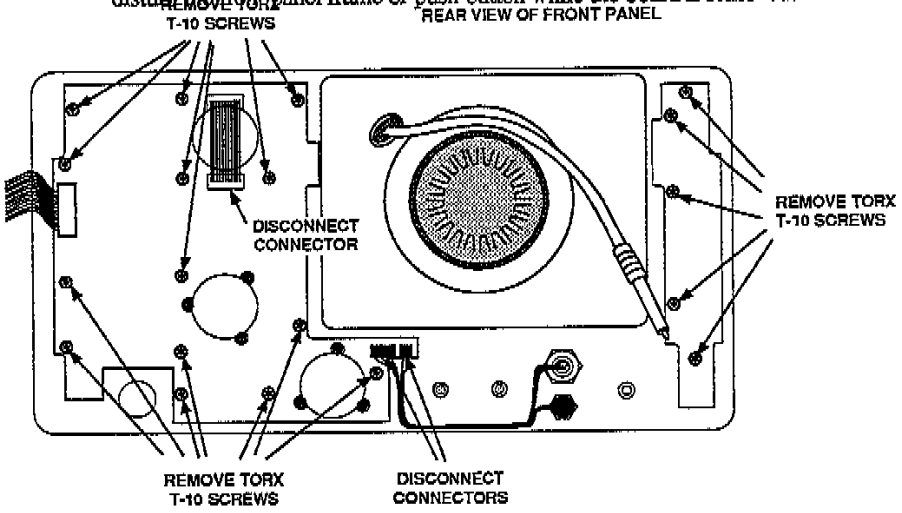


Figure 4-38. Front-panel board removal.

Installing the Left Front-panel Assembly (A2A1)

1. Reverse the removal procedure.
2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

Removing the Right (large) Front-panel Assembly (A2A2)

1. Remove the entire Front-panel assembly as previously described.
2. Remove the knobs from the KNOB 1 and KNOB 2 controls. KNOB 1 has two 1/16 inch Allen set-screws, and KNOB 2 has one set-screw.
3. Disconnect the multi conductor cable going over the CRT shield from the clamp on the CRT shield and from the multi-pin connector on the Left Front-panel (A2A1). The multi-conductor cable is soldered to this assembly, and is replaced as part of the assembly.
4. Disconnect the multi-pin connector that connects the FREQUENCY/MARKERS control to the board as shown in Figure 4-38.
5. Disconnect the multi-pin connectors to the ACCESSORY IN and PROBE POWER connectors.

6. Place the assembly face down (CRT up) on a flat surface for the rest of this procedure. This keeps the buttons in place until the replacement assembly is installed to provide support.

7. Remove 14 Torx T-10 screws holding the board to the front-panel frame.

8. Remove the board. Also, remove the two ground springs around the shafts of the KNOB 1 and KNOB 2 controls, or from the frame if they cling there. Keep the springs and knobs to use when installing the replacement board.

Installing the Right Front-panel Assembly (A2A2)

1. Reverse the removal procedure.

2. Adjustments or corrections are required after replacing this assembly. Refer to Table 3-2, titled *Adjustments/Corrections required after repair or replacement* located in the *Adjustments/Corrections* section of this manual.

Installing the Front-panel Assembly

1. Reverse the removal procedure. Tighten the SMA connectors to 8 in-lbs. Do not over tighten.

2. Check flatness after re-installing the Front-panel Assembly. (Flatness checks should be performed any time SMA connectors are changed in the front end signal path.)

REPLACING THE NVRAM BATTERIES

The batteries that power the non-volatile RAM (NVRAM) must be replaced once a year under normal use. The procedure replaces one battery at a time, so that the other battery can supply the NVRAM during the replacement process. If both batteries are disconnected, stored waveforms, settings, and instrument display adjustments will be lost.

CAUTION

Check the position of jumper J10 before installing a replacement module. Replacement modules are stored with the jumper in the Secure position (pins 2 & 3) to extend the battery life. The jumper must be in the Normal position (pins 1 & 2) to activate storage.

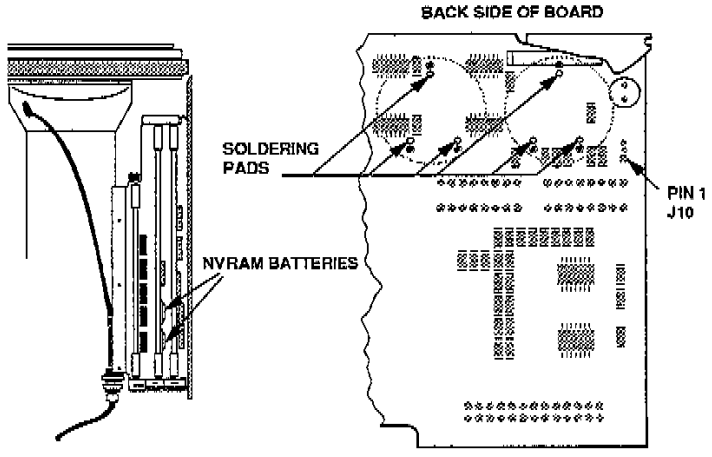


Figure 4-39. NVRAM Battery locations.

Battery Replacement Procedure

1. Disconnect the power cord from the instrument.
2. Remove the I/O Interface (A42) from the instrument.
3. Determine which battery to replace first by measuring the levels of the two batteries with a volt meter. Replace the batteries according to the following criteria

   If both batteries measure over 2 V, replace the higher voltage battery first.

   If one battery is under 2 V, replace the lower voltage battery first.

   If both batteries are under 2 V, data is probably already lost, and you can replace either battery first.
4. Unsolder the first battery to be replaced, being careful to not overheat the circuit board pads. Use desoldering tools to aid the process. Carefully remove the battery. Refer to the *LITHIUM BATTERY DISPOSAL AND FIRST AID* section following this section.
5. Install the first replacement battery by soldering it into the empty battery pads. Be sure to not overheat the pads.
6. Repeat steps 4 and 5 to replace the remaining battery, and re-install the I/O Interface assembly.
8. No adjustments or corrections are required after replacing the batteries if no data is lost. If data is lost, the entire adjustment/correction procedure, including flatness, must be performed. Refer to the *Adjustments/Corrections* section of this manual.

LITHIUM BATTERY DISPOSAL AND FIRST AID

WARNING

Improper handling may cause fire, explosion, or severe burns. *To avoid personal injury, observe proper procedures for the handling of lithium batteries. Do not recharge, crush, disassemble, heat the battery above 302°F (150°C), incinerate, or expose the contents to water.*

Lithium Battery Disposal

Dispose of the battery according to local, state, and federal agencies.

NOTE

Typically, small quantities (less than 20) can be safely disposed of with ordinary garbage in a sanitary landfill.

Larger quantities must be sent by surface transport to a hazardous waste disposal facility. The batteries should be individually packaged to prevent shorting. Then, pack them into a sturdy container that is clearly labeled:

Lithium Batteries – DO NOT OPEN

Lithium Battery Emergency and First Aid Information

Manufacturer: Catalyst Research or Sanyo

Battery Type: Lithium

Table 4-26 lists the emergency procedures to follow should you come in contact with battery solvent.

Table 4-26. Lithium Battery Emergency Procedures

Area of Contact	Emergency Procedure
Skin	Wash promptly with plenty of water.
Eyes	Flush immediately with plenty of water and use an emergency eye wash, if available. Report to a medical professional for treatment.
Inhalation	Leave the area and get fresh air. Report to a medical professional for treatment.
Ingestion	Non-toxic according to laboratory testing. How ever, report to a medical professional for advice.

In case of venting, clear the immediate area. Venting will usually last only a few seconds.

UPDATING FIRMWARE

Firmware is updated in this instrument by replacing Read Only Memory (ROM). The ROMs are located on four boards described in Table 4-27. There are three sets of replaceable firmware in the instrument. The boards and their respective firmware are:

Table 4-27. Firmware Locations

Board	Function	Contained In
A24 Digital Storage	Digital Storage firmware	U11
A42 I/O Interface	Main Processor firmware (I/O Interface portion)	U37, U38, U39, and U40
A41 Main Processor	Main Processor firmware	U63
A43 Memory	Main Processor firmware	U10, U11, U12, U13, U14

All ROMs listed in Table 4-27 must be ordered separately from the boards they reside on. The Main Processor firmware on the Main Processor (A41) and Memory (A43) boards must be replaced as a set. The I/O Interface portion of the Main Processor firmware may be replaced independently of the rest of the Main Processor firmware. The Digital Storage firmware is replaced independently.

Option 16 — Option 16 firmware is unique and must be replaced with the appropriate part number. Refer to the replaceable electrical parts list for the proper part number for your instrument.

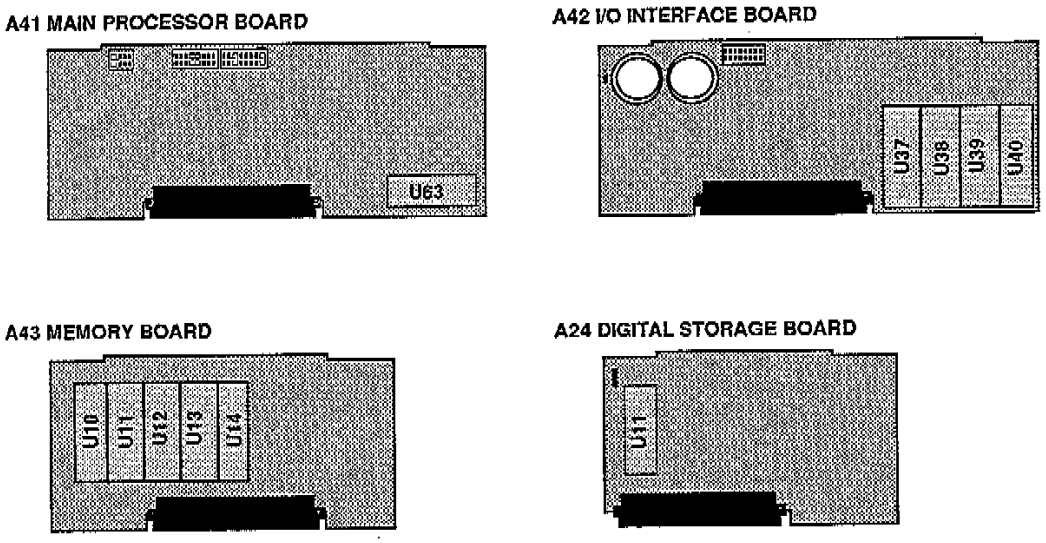


Figure 4-40. Firmware ROM locations.

SWITCHES AND JUMPERS

The following information gives the switch and jumper positions. Factory-set default settings are in ALL CAPITAL letters.

I/O Interface

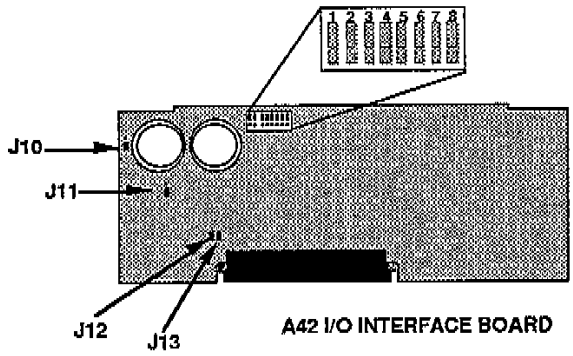


Figure 4-41. I/O Interface jumpers and switch locations.

Table 4-28. I/O Interface Switch Functions and Positions

Switch Number and Function	Position	
	Open	Closed
1. Sweep Board version	Old (-00)	NEW (>-01)
2. Ref Osc version	Old (-00)	NEW (>-01)
3. Trace Mode	DISABLED	Enabled
4. Span Compensation	ENABLED	Disabled
5. Frequency Control Loop	Open Loop	CLOSED LOOP
8. MTX version	Old (X0304)	NEW (> X0304A)

CAUTION

Check the position of jumper J10 before installing a replacement module. Replacement modules are stored with the jumper in the Secure position (pins 2 & 3) to extend the battery life. The jumper must be in the Normal position (pins 1 & 2) to activate storage.

Table 4-29. I/O Interface Jumpers

Jumpers	Positions	
J10 Secure Mode	Pins 1 and 2 NORMAL (Data Saved)	Pins 2 and 3 Secure (Data Erased)
J11	Pins 1 and 2 Only NORMAL	Pins 2 and 3 (Not Supported)
J12 Interrupt 4	Shorted ENABLED	Open Disabled
J13 Interrupt 3	Shorted ENABLED	Open Disabled

Main Processor

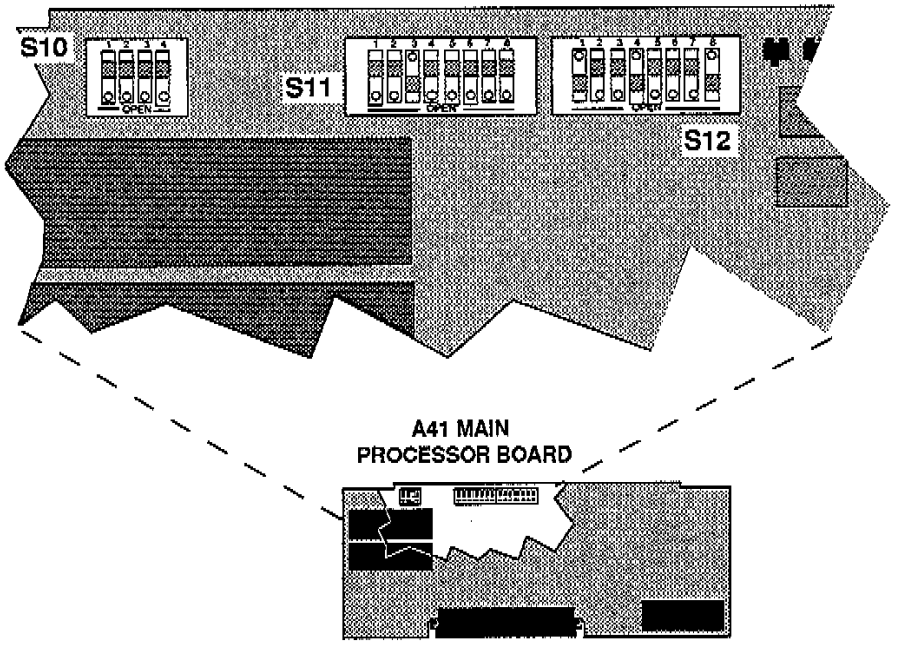


Figure 4-42. Main Processor Switch Locations.

Table 4-30. Main Processor Switch Functions - S10 (Figure 4-42)

S10 Switch Number and Function	Position Open	Closed
1. Power-up Self Test	DISABLED	Enabled
2. Clock Source	INTERNAL	External
3. Not Used	———	———
4. System Reset	NORMAL	Close, then open to reset System

Table 4-31. Main Processor Switch Functions - S11 (Figure 4-42)

S11 - (Left Switch) Switch Number and Function	Position Open	Closed
1. Advanced Diagnostics	Enabled	DISABLED
2. Power Up ROM (Checksum test)	ENABLED	Disabled
3. Service Mode	DISABLED	Enabled
4. Error Reporting	ENABLED	Disabled
5. Not Used	———	———
6. Not Used	———	———
7. FP Version	NEW	Old
8. FP Standby Switch	ENABLED	Disabled

Table 4-32. Main Processor Switch Functions - S12 (Figure 4-42)

S12 - (Right Switch) Switch Number and Function	Position	
	Open	Closed
1. NMI Enable	ENABLED	Disabled
2. Not Used	———	———
3. Not Used	———	———
4. Not Used	———	———
5. Force Recall of Default Settings	ENABLED	Disabled
6. Periodic Calibration	ENABLED	Disabled
7. Overdrive limit for 10 kHz BW	Disabled	ENABLED
8. Power Supply version	OPEN	Closed

Power Supply

Table 4-33. A5A1 Power Supply Primary Switches (Figure 4-43)

Number	Function	Normal Position
S10 - 1	Main Chopper Control	OFF
S10 - 2	Pulse Width Modulator Sense Voltage	OFF

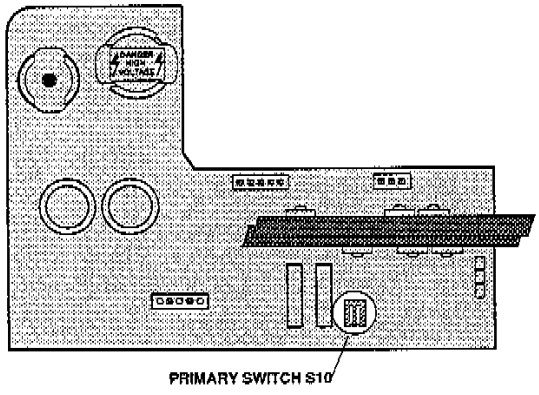


Figure 4-43. Power Supply Primary Switches S10 location.

Table 4-34. A5A2 Power Supply Secondary Switch (Figure 4-44)

Number	Function	Normal Position
S10 - 1	/ACGONE Defeat	OFF (ACTIVE)
S10 - 2	Main Chopper Control	OFF
S10 - 3 and 4	Fan Speed Control	These switches function only if power is disconnected from the Processor. See Table 4-38.

Table 4-35. Fan Switch Positions

Fan Speed	S10-3 Fan 2	S10-4 Fan 1
OFF (Normal)	OFF	OFF
Low	On	Off
Medium	Off	On
High	On	On

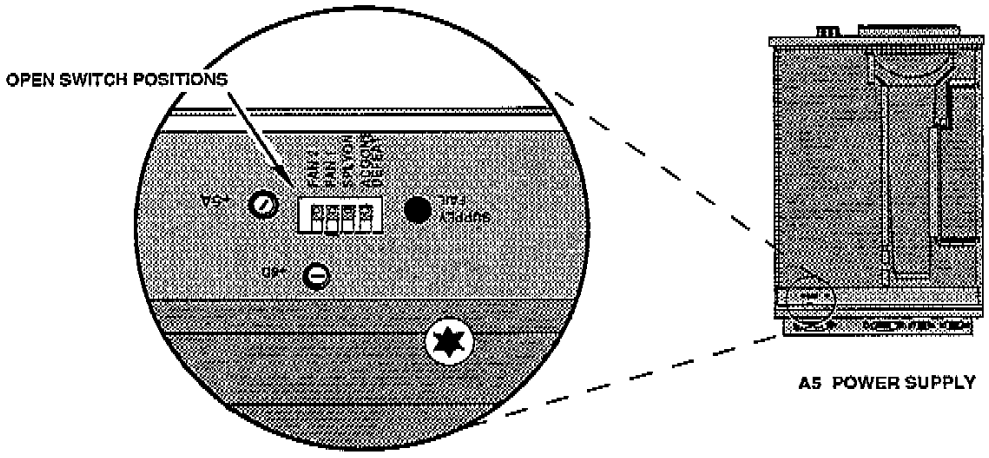


Figure 4-44. S10 Location on the Power Supply Secondary.

Video Processor

Table 4-36. Video Processor Jumper (Figure 4-45)

A20 Video Processor Jumper	
Pins 1 & 2	NORMAL
Pins 2 & 3	Test/Cal

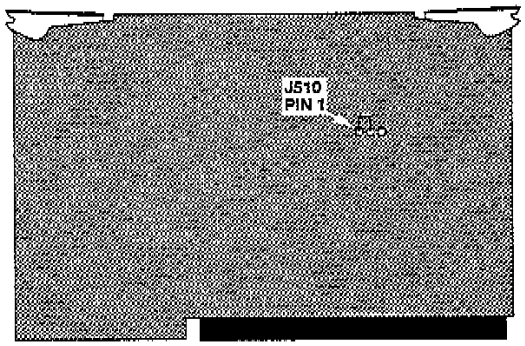


Figure 4-45. Video Processor test jumper location.

Display Amplifier

The jumpers on the A22 Display Amplifier board select either real-time signal or composite signal to the rear-panel H OUT and V OUT connectors. The normal operating mode is real-time signals. The composite signal includes signal, readout information in addition to the normal vertical and horizontal information.

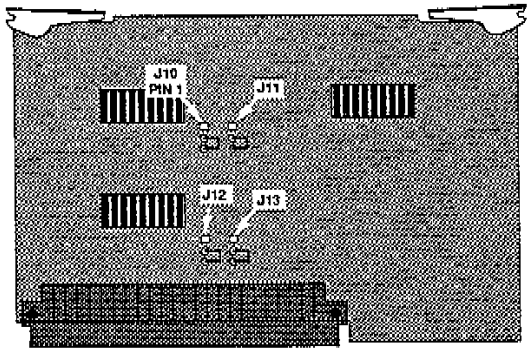


Figure 4-46. Display Amplifier jumper locations.

Table 4-37. Display Amplifier Jumpers J10, J11, J12, and J13 (Figure 4-46)

Pins	Function
1 & 2	REAL-TIME
2 & 3	Composite

Sweep/Span Attenuator

The jumper on the A33 Sweep/Span board is used for troubleshooting purposes. It allows breaking the gate control loop and inserting an external pulse to gate the sweep rather than the internal gate. The normal jumper position is between pins one and two.

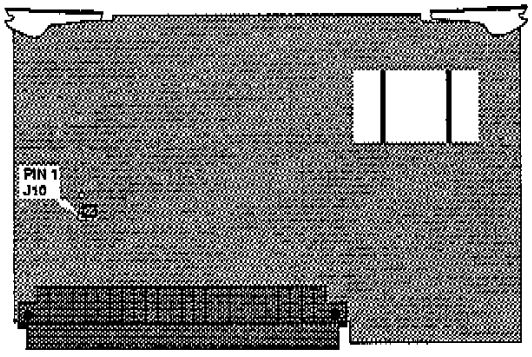


Figure 4-47. Sweep/Span Attenuator jumper location.

THEORY OF OPERATION

This section describes the 2780-series spectrum analyzer circuitry. The section begins with a brief description of the major circuits and follows with a module-level description of each block.

While reading this description, refer to figures within this section that apply to the particular circuit under discussion and to the overall block diagram in ***Section 7—Diagrams***. Refer also to ***Section 4—Maintenance***, for a detailed discussion of the self-correction routines.

FUNCTIONAL DESCRIPTION

The 2780-series Spectrum Analyzer is a four-conversion receiver that displays electrical signals on a CRT. The horizontal display axis is calibrated in units of frequency, and the vertical axis is calibrated in units of power or voltage.

Refer to Figure 5-1, which is a block diagram of the 2780-series instrument. The spectrum analyzer consists of the following major components:

- The 1st Converter (MTX) mixes the input signal (100 Hz to the maximum input coaxial frequency) with an 8 to 16 GHz swept local oscillator signal to produce an intermediate frequency (IF) signal of either 3.525 GHz or 10.025 GHz, depending on the band selected. If an internal mixer is used, either a preselector (6.5 GHz and above) or low-pass filter is placed in the signal path to reject unwanted signals.

  NOTE

  2780-Series frequency bands are not obvious to the user. The instrument does use internal frequency bands, so very wide spans may consist of two separate sweeps that are joined by the Main Processor.

  When the instrument is sweeping over an internal band break in very wide spans, the Main Processor takes two sweeps. A sweep is made in each band, then the two are joined. To avoid missing a signal at the juncture, the sweeps are intentionally overlapped. Thus, a signal at the juncture may appear as two signals, but becomes one if the span is narrowed to less than 500 MHz.

  If an external waveguide mixer is used (8 GHz to 1200 GHz), the incoming IF signal (usually 3.525 GHz) is neither filtered nor attenuated by the 1st Converter, but is passed through this stage to the 2nd Converter. A single front-panel connector conveys the external mixer IF signal in and the local oscillator signal out; an internal diplexer separates the two signals.

- The 2nd Converter (Microwave IF) filters and amplifies the first IF signal, then mixes it with the second local oscillator signal to produce the second IF signal, nominally 525 MHz. The 2nd converter contains two mixers and two local oscillators (9.5 GHz and 3 GHz) so that the input signal and first IF signal do not overlap when switching bands. Both local oscillators are locked to a 100 MHz reference signal from the Frequency Control section. The IF output signal is applied to the 3rd Converter.

- The 3rd Converter (525 MHz IF) filters the incoming second IF signal, then mixes it with a 500 MHz local oscillator signal to produce the third IF signal, nominally 25 MHz. This signal is applied to the Variable Resolution Module.

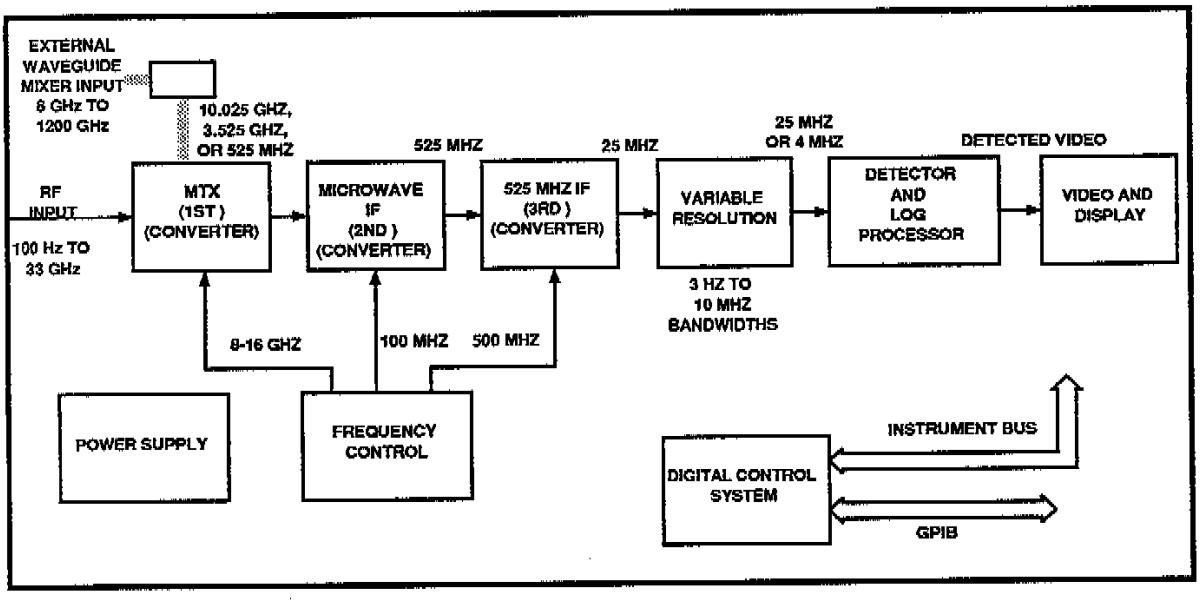


Figure 5-1. 2780-series Spectrum Analyzer Block Diagram.

- The Variable Resolution circuits amplify and filter the third IF signal through a bandwidth filter section, and in most bandwidths, convert it down to the 4 MHz fourth IF signal. Bandwidth filter selections range from 3 Hz to 10 MHz in 1-3-10 sequential steps. (Most of the variable gain stages that control the reference level are in this section.) The 25 MHz third IF is used only with the 10 MHz and 3 MHz bandwidths. When one of the other twelve bandwidths is selected, a 29 MHz local oscillator signal and the incoming 25 MHz IF signal are mixed to produce a 4 MHz IF signal. From this section, the filtered IF signal is passed to the Log Processor.
- The Detector and Log Processor logarithmically amplifies the incoming IF signal, detects the signal, converts the signal for a linear display if required, and provides vertical scale adjustment. This section also performs necessary flatness corrections to maintain a flat response over the entire frequency range. The video signal from this block is applied to the Video and Display section.
- The Video and Display section consists of three major circuits:
  1) The Video Processor filters and amplifies the incoming video signal, selects video bandwidth, digitizes the video signal (using one of four acquisition modes: MAX, MIN/MAX, MIN, or SAMPLE), and sends the digitized video signal to the Digital Storage section. If a real-time (analog) display is selected, the analog video signal is sent to the Display section.
  2) The Digital Storage section produces a vector graphics display of waveforms, graticules, and text. This section also performs the Max Hold, Average, Math, and Marker functions (primary, secondary delta, and bandwidth). Color shutter control signals are generated here and sent to the Display Section.
  3) The Display Section amplifies the X, Y, and Z-axis signals for application to the CRT. It also drives the color shutter.
- The Frequency Control section consists of five major elements:

1) The Yig-Tuned Oscillator (YTO) produces the local oscillator signal to mix with the RF input signal in the 1st Converter. A swept-frequency synthesizer locks the YTO to reduce drift.

2) The Reference Oscillator produces the 100 MHz signal that is multiplied by five to become the 500 MHz third local oscillator signal. The 100 MHz signal is also used for the calibrator signal and as a reference signal to stabilize the two local oscillators in the 2nd Converter and the 1st local oscillator via the Swept-frequency Synthesizer.

3) The Sweep/Span Attenuator produces a scanning signal to drive the LO Module and the sweep signal to drive the horizontal display circuits.

4) The LO Module produces the tuning voltages to drive the YTO and Preselector across the input frequency range .

4) The Microwave Phase Lock Module controls the YTO to reduce frequency drift.

5) The Period Counter measures signals from the Log Processor, LO Module, Reference Oscillator, and Microwave Phase Lock.

- The Digital Control section processes front-panel control inputs, including knob, key, and menu selections to select the appropriate operating modes and functions. This section also communicates over two rear-panel GPIB connectors. Digital control of other sections is via an internal serial bus.
- The Power Supply section provides regulated DC power and forced-air cooling for all circuits in the instrument.

BLOCK DESCRIPTION

1ST CONVERTER

The 1st Converter is the front end of the spectrum analyzer (see Figure 5-2). It mixes the radio frequency (RF) input signal with a tunable local oscillator signal to produce the first intermediate frequency (IF) signal, which is either 10.025 GHz or 3.525 GHz, depending on the frequency band being analyzed. When an external waveguide mixer is used, the 1st Converter furnishes a local oscillator signal to the EXTERNAL MIXER port, and multiplexes that local oscillator signal with the incoming 3.525 GHz or 525 MHz IF signal. The 1st Converter consists of RF Attenuator A10, Magnetically Tuned Converter (MTX) A12, and First Local Oscillator (YTO) A11.

RF ATTENUATOR

The RF signal enters the instrument through the RF INPUT connector, a Planar Crown connector system. RF Attenuator A10 attenuates the incoming RF signal from 0 dB to 70 dB in 10 dB steps, then applies it to the MTX. Nominal mixer input level is –30 dBm, but in mixer overdrive applications, attenuation decreases 10 dB for each 10 dB of overdrive.

MTX

The A12 MTX assembly contains the main body of the 1st Converter. The signal from the RF Attenuator is applied to a switched diplexer that selects the low-pass path for frequencies under 6.5 GHz, or the high-pass path for signals above 6.5 GHz. A different mixer is used for each path.

Signals from waveguide sources can be converted by external waveguide mixers. The external waveguide mixer output passes through the EXTERNAL MIXER input connector to the Ext Mixer Multiplexer, which frequency-multiplexes the local oscillator signal (used to drive the external mixer) with the incoming signal.

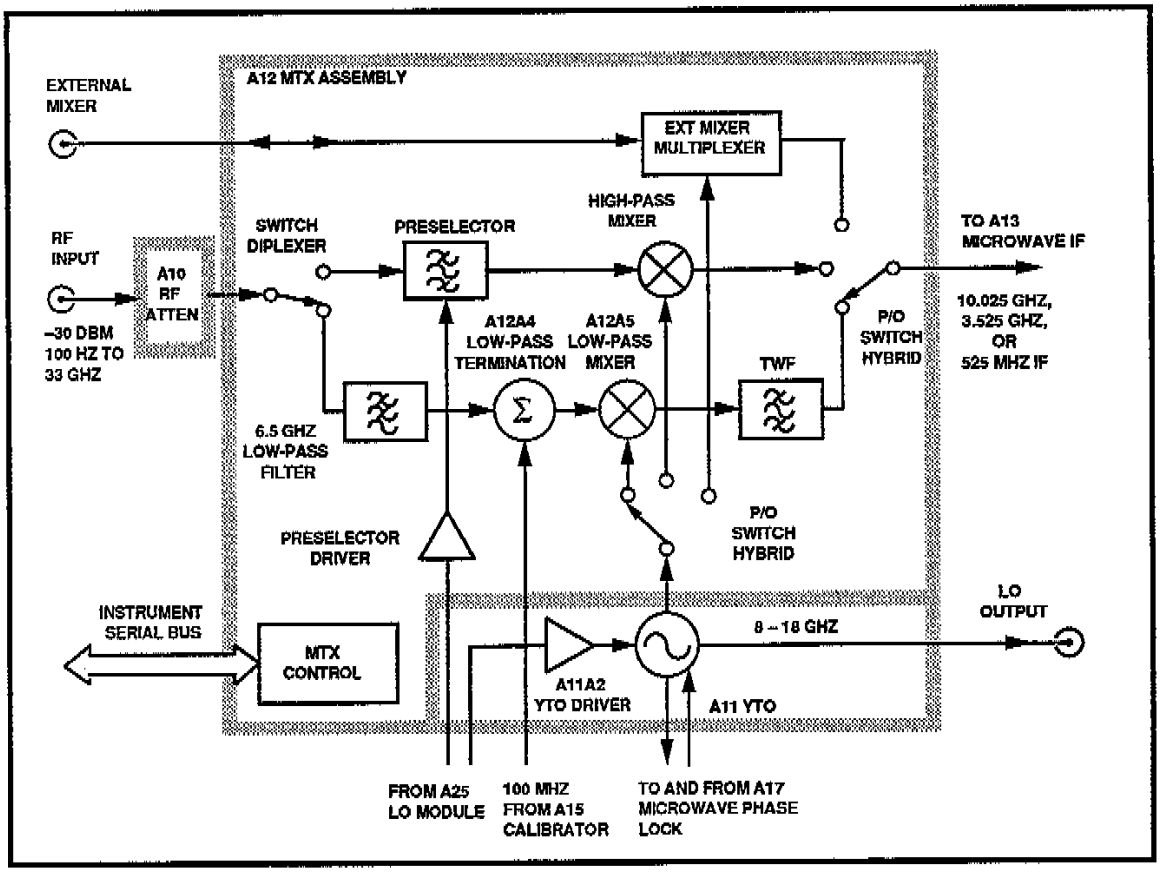


Figure 5-2. 1st Converter Block Diagram

Low-pass Path

The Low-pass path converts signals under 6.5 GHz. The signal goes through a Low-pass Filter, Low-pass Termination, Low-pass Mixer, Traveling-wave Filter (TWF), and Switch Hybrid circuit.

The 6.5 GHz Low-pass Filter blocks higher frequency signals from entering the Low-pass path. This removes higher order conversions and the image response. The filter also prevents the local oscillator signal from passing back to the RF input connector.

Low-pass Termination A12A4 terminates the Low-pass filter and the Low-pass Mixer RF input. When the Input Menu selects the internal calibrator, a 100 MHz signal is applied to the termination. A 30 dB attenuator reduces the 100 MHz signal level to approximately –50 dBm at the mixer input.

Low-pass Mixer (A12A5) mixes the RF input signal with the first local oscillator signal to produce a 10.025 GHz IF signal. The balanced mixer design reduces local oscillator signal feedthrough. Conversion loss is approximately 13 dB at 100 MHz.

The TWF is a 10.025 GHz bandpass filter. The desired 10.025 GHz signal passes to the output switching circuit; unwanted signals are blocked by the TWF. Filter bandwidth is approximately 300 MHz.

High-pass Path

The High-pass path converts RF input signals above 6.5 GHz. The path consists of the Preselector and Preselector Driver, and the High-pass Mixer. The signal is automatically preselected by a tunable bandpass filter before driving the High-pass Mixer. The mixer output signal is passed to the Switch Hybrid circuit.

The Preselector is a wide-range tunable bandpass filter. Tuning range is from 6.5 GHz to the maximum coaxial input frequency of the instrument.

The Preselector Driver receives a swept tuning voltage from the A25 LO Module. The driver in turn supplies the tuning current to the Preselector coil. This tuning current corresponds with the sweep to synchronize the displayed signal frequency with that of the Preselector.

The High-pass Mixer combines the preselected input signal with the local oscillator signal to produce the first IF signal (3.525 MHz for 6.5 to 21 GHz and above 28 GHz, and 10.025 GHz for 21 to 28 GHz.). This signal is passed to the Switch Hybrid, where it is filtered and sent to the 2nd Converter.

Switch Hybrid

The Switch Hybrid assembly provides local oscillator signal amplification, switching, filtering, and signal multiplexing. The local oscillator signal is applied to the Switch Hybrid, where it is amplified to provide a high-level drive for the mixers. PIN diodes direct the local oscillator signal to the Low-pass, High-pass, or External Mixer path.

The signal from the Low-pass path arrives at the Switch Hybrid through the TWF. A PIN diode switch connects the signal to the converter output. A low-pass filter prevents the local oscillator signal from entering the IF path.

The signal from the High-pass path comes directly from the High-pass Mixer. A PIN diode switch connects the signal to the converter output.

In the External Mixer path, a multiplexer allows the local oscillator signal and the External Mixer IF signal to share the same line. This allows using two-port waveguide mixers. The local oscillator signal is tunable from 8 GHz to 18 GHz, and the IF output from the External Mixer is primarily at 3.525 GHz. Refer to ***Section Two—Specification***, for the external waveguide mixer bands and the corresponding IF and local oscillator harmonic numbers.

MTX Control

The MTX Control circuit interfaces to the instrument serial bus and provides power supply filtering. Control signals from the instrument bus direct the PIN diode switches, local oscillator signal switching, and bias for external mixers.

FIRST LOCAL OSCILLATOR

The First Local Oscillator provides a high-level signal that is tunable over an 8 GHz to 18 GHz range. The local oscillator can be phase-locked to the instrument Reference Oscillator to provide stability and low phase noise when operating within narrow sweep spans. The First Local Oscillator consists of the A11 YTO (YIG-Tuned Oscillator) and the A11A2 YTO Driver.

YTO

The A11 YTO is a magnetically-tuned YIG oscillator. Current through the magnet coils tunes the resonant frequency. The A11A2 YTO Driver and the A17 Microwave Phase Lock assembly supply the tuning current. The oscillator has three outputs; one drives the MTX, another is part of the Microwave Phase Lock loop, and the third is to the front-panel LO OUTPUT.

YTO Driver

The YTO Driver (A11A2) converts drive voltage into coil current, switches a noise filter across the coil, clamps the coil during retrace, and provides power supply filtering.

The drive voltage from the LO Module (A25) is converted to a current to drive the main YIG coil. This current is proportional to the drive voltage.

The noise filter is a low-pass filter that reduces noise current across the main coil and optimizes transient response. An additional RC network is switched in when the main coil is not swept.

2ND CONVERTER

The 2nd Converter (A13 Microwave IF Assembly) amplifies, filters, and converts signals from the 1st Converter to produce the 525 MHz second IF signal. See Figure 5-3. The 2nd Converter consists of the Input Amplifier and Filter, Mixer and Local Oscillator, Phase Lock, and Microwave IF Controller.

INPUT AMPLIFIER AND FILTER

The Input Amplifier and Filter consists of two diplexers, three amplifier stages, and two filters. The input signal is applied to the input diplexer, where any frequency components under 600 MHz are sent directly to the converter output. Frequency components over 3 GHz are sent through the converter.

The first and third amplifiers remain in the signal path in all bands of operation (except Identify Mode). An additional amplifier is switched into the signal path when Band 2 or above is selected and when Band 1 requires additional IF gain (REF levels below –30 dBm). This extra gain step overcomes increased insertion losses that occur in the 1st Converter at higher frequencies. The output signal from the third amplifier is applied to the output diplexer, which separates the 3.525 GHz and 10.025 GHz signals and applies each to the appropriate filter.

Two bandpass filters (one with a center frequency of 3.525 GHz and the other of 10.025 GHz) reject images from the active mixer. Filter bandwidth is 100 MHz.

MIXER AND LOCAL OSCILLATOR

This circuit consists of two mixers, a 3 GHz local oscillator, a 9.5 GHz local oscillator, and the IF Selector. The signal from each bandpass filter is applied to the appropriate mixer. Each mixer is driven by a separate local oscillator, one that converts the 3.525 MHz IF signal and another that converts the 10.025 GHz IF signal. Both conversions produce a 525 MHz second-IF signal. Only the selected oscillator has power applied. Each oscillator is phase-locked to a harmonic of the 100 MHz Reference Oscillator signal.

Both mixers feed the IF Selector, which selects the appropriate mixer output signal for the band in use. The IF Selector selects the 525 MHz path through the Isolation Switch in some External Mixer Bands, or when the external mixer Identify mode is used.

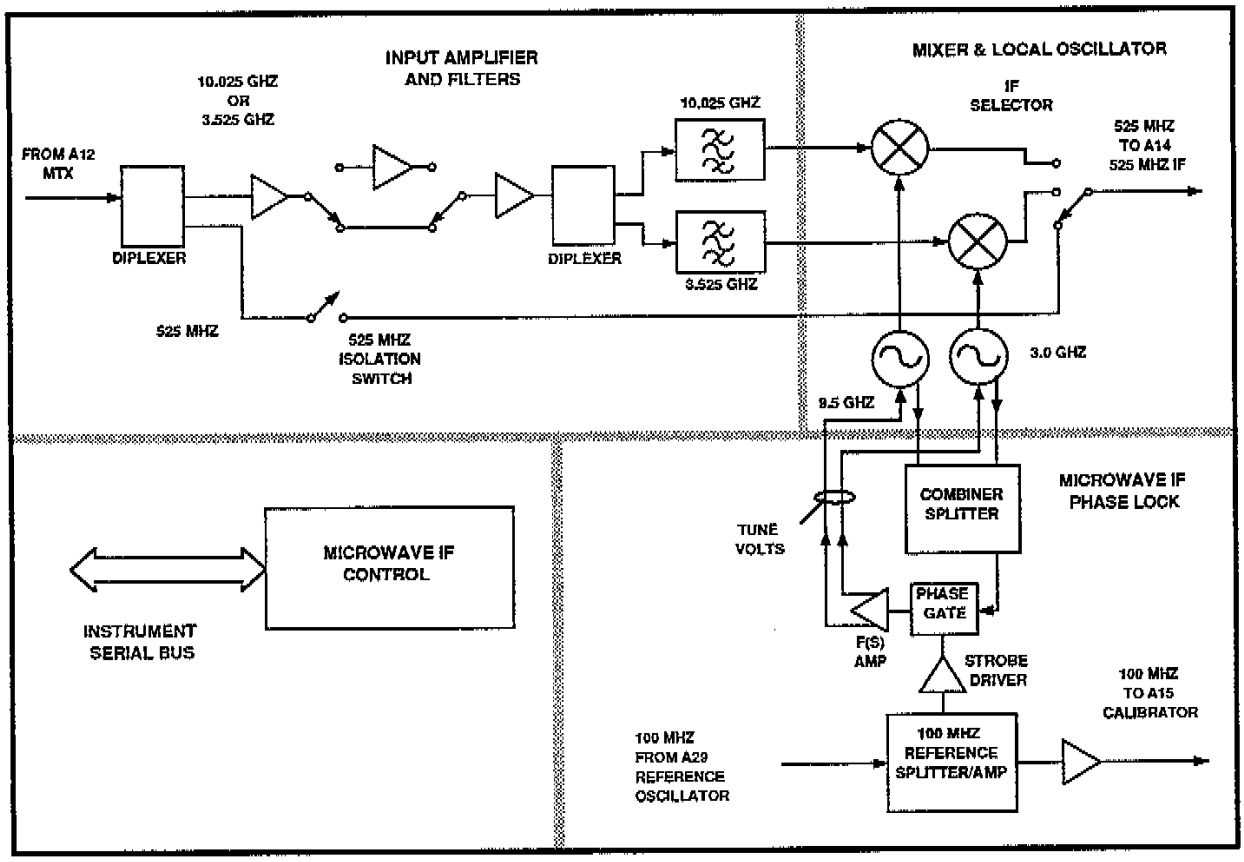


Figure 5-3. 2nd Converter (A13 Microwave IF) Block Diagram.

PHASE LOCK

The Phase Lock circuit consists of the 100 MHz Reference Splitter-Amplifier, Strobe Driver, Combiner Splitter, Phase Gate, and F(s) Amplifier. The circuit locks the active local oscillator to a harmonic of the 100 MHz Reference signal.

The output signal from the active local oscillator enters the Phase-lock section through the Combiner Splitter to drive the Phase Gate. The 100 MHz reference signal strobes the Phase Gate, producing a difference signal. This signal drives the F(s) amplifier, where it is filtered to produce a tune voltage, which is fed to the local oscillators as a control signal.

100 MHz Reference Splitter-Amplifier

The 100 MHz Reference Oscillator output signal is applied to the Splitter-Amplifier at approximately +3.5 dBm; the signal is amplified to approximately +10 dBm and applied to the Strobe Driver. The 100 MHz signal is also split off at a +3.5 dBm level and applied to the Calibrator module. The serial bus interface on the Microwave IF controller shuts off the signal to the calibrator when not in use, if so directed by the Main Processor.

The Strobe Driver accepts the +10 dBm signal from the splitter board and amplifies it to drive the snap-off diode in the Phase Gate.

Combined Splitter

The Combiner Splitter is a hybrid that accepts and isolates local-oscillator power from the 3 GHz local oscillator and 9.5 GHz local oscillator and provides the proper signal level to the Phase Gate.

Phase Gate

The local-oscillator signal from the Combiner Splitter is applied to the Phase Gate at a reduced power level. The Phase Gate produces a comb of harmonics of the 100 MHz reference signal and samples the local-oscillator signal from the Combiner Splitter with the appropriate harmonic (30th or 95th) of the reference signal, producing a beat note that is proportional to the frequency difference between the reference harmonic and the local-oscillator signal. The beat note is applied to the F(s) Amplifier for filtering and integrating.

F(s) Amplifier

The F(s) amplifier filters and integrates the beat note from the Phase Gate, producing a tune voltage to drive the active local oscillator. When the local oscillator locks, the beat note becomes a DC voltage. The F(s) Amplifier isolates the tune voltage from the Phase Gate and removes offset voltages coming from that stage.

Microwave IF Controller

The Microwave IF Controller is the interface between the serial bus and the modules that make up the 2nd Converter. The controller receives instructions from the Main Processor that determine intermediate-frequency gain, which module should receive power, and which band of frequencies is to be converted or passed by the module. The controller also filters incoming supply voltages.

3RD CONVERTER

Refer to Figure 5-4. The 3rd Converter (A14 525 MHz IF module) consists of the Pre-filter, Input Amplifier, 525 MHz Bandpass Filter, LO Amplifier, and Mixer. This module mixes the 500 MHz signal from the X5 Multiplier in the A28 Period Counter with the incoming 525 MHz second IF signal to produce the 25 MHz third IF signal, which is applied to the Variable Resolution (VR) circuits. The 3rd Converter also fixes the bandwidth of the incoming 525 MHz signal at 10 MHz.

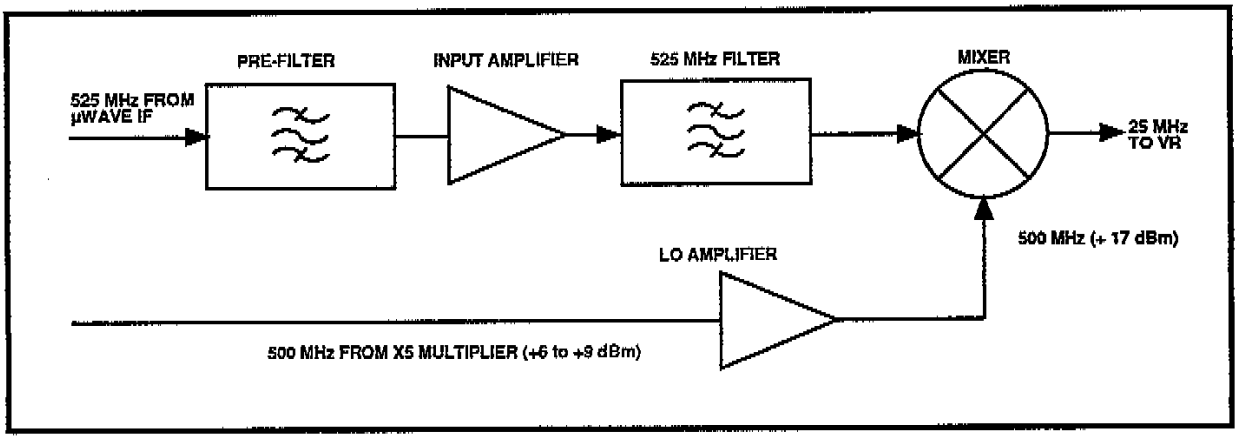


Figure 5-4. 3rd Converter (A14 525 MHz IF) Block Diagram.

The Pre-filter rejects the 475 MHz image conversion from the 2nd Converter.

The Input Amplifier isolates the 2nd and 3rd Converter from one another. It produces approximately +9 dB gain to compensate for conversion losses.

The 525 MHz Bandpass Filter has an approximate 10 MHz bandwidth and works with filters in the VR circuit to produce the 10 MHz resolution bandwidth.

The reference signal is amplified in the LO Amplifier to produce a high level (approximately +17 dBm) to drive the Mixer.

The 525 MHz signal and the 500 MHz signal from the X5 Multiplier (described in the Reference Oscillator description further on in this section) are combined in the Mixer to produce a 25 MHz mixer output signal, which is applied to the VR module. A low-pass filter in the Mixer rejects harmonics from the LO amplifier, reducing harmonic distortion in the mixer.

VARIABLE RESOLUTION

The A16 Variable Resolution (VR) module amplifies and filters the incoming 25 MHz IF signal from the 3rd Converter. When conversion is selected (narrower twelve bandwidths), the VR circuits also convert the incoming IF signal to the 4 MHz fourth IF signal and filter the signal through selected bandwidth resonators to produce an IF signal bandwidth of 3 Hz to 1 MHz. The VR circuits also produce a 4 MHz signal for calibrating the Log Processor during self-correction. See Figure 5-5. The VR circuit consists of the Input Amplifier and Filters, 25 MHz path, 4 MHz path, 29 MHz Oscillator, 4 MHz Oscillator, Output Amplifier, and Interface.

INPUT AMPLIFIER AND FILTERS

This section provides initial amplification, filtering, and the 25 MHz oscillator signal that is used to set the resonator center frequency during self-correction routines. The section consists of an Input Amplifier, 25 MHz Crystal Oscillator, Switching, Bandpass Filters, and Gain Step Amplifiers.

Input Amplifier

The 25 MHz IF signal is applied to the Input Amplifier at a level of approximately –39 dBm (for a full-screen signal with the 100 MHz reference signal applied, a REF level of –20 dBm, and RF attenuation of 10 dB). The signal is amplified approximately 18 dB and applied to one of two paths through a bandwidth selector switch.

Filters

Selectable filters control input bandwidth. When 10 MHz bandwidth is selected, the signal is passed directly to the Gain Step Amplifiers (some 10 MHz bandwidth filtering has already occurred in the 3rd Converter). When a RES BW of 10 kHz to 3 MHz is selected, the incoming signal is passed through a 3 MHz filter and applied to the Gain Step Amplifiers. When a RES BW of 3 Hz to 3 kHz is selected, the incoming signal is passed through a 10 kHz crystal filter to reduce noise, then applied to the Gain Step Amplifiers. When the OSC switch is closed by the Processor, the 10 kHz filter and related circuits produces a 25 MHz signal to excite the resonators when the self-correction routine is invoked.

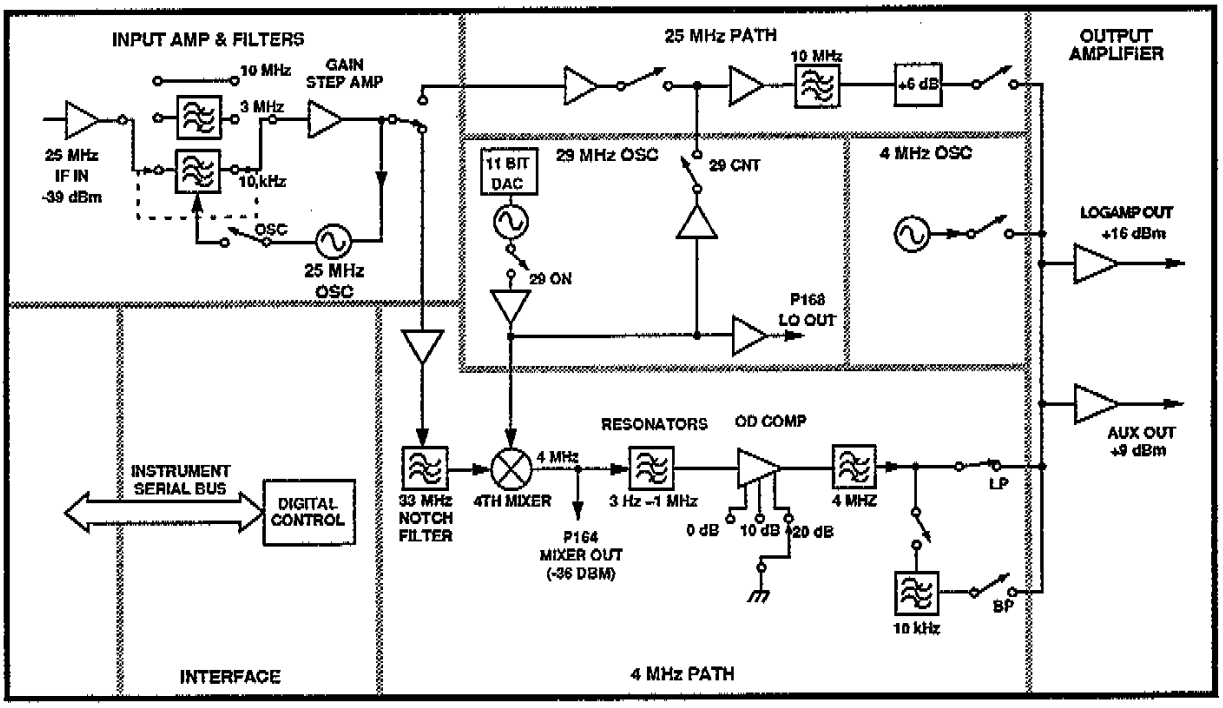


Figure 5-5. A16 Variable Resolution Module Block Diagram.

Gain Step Amplifiers

The Gain Step Amplifiers consist of three stages, the First Gain Step Amplifier, the PIN Amplifier, and the Second Gain Step Amplifier (see Figure 5-6). These stages compensate for variations in conversion losses that occur in the front end, provide variable gain for REF LEVEL switching, and reduce overall IF gain by 10 dB when the 30 dB Mixer Overdrive mode is selected. Each Gain Step Amplifier has three selectable gain settings, –9.5 dB, 0 dB, and +9.5 dB. All settings are for REF levels between –30 dBm and –60 dBm. The PIN Amplifier, the gain of which is controlled by a DAC, provides the fine gain adjustment for the section. Gain range is approximately 12 dB. From the output of the Second Gain Step Amplifier, the amplified 25 MHz signal is applied through the IF path selector switch to one of the two IF paths for further amplification by fixed-gain amplifiers.

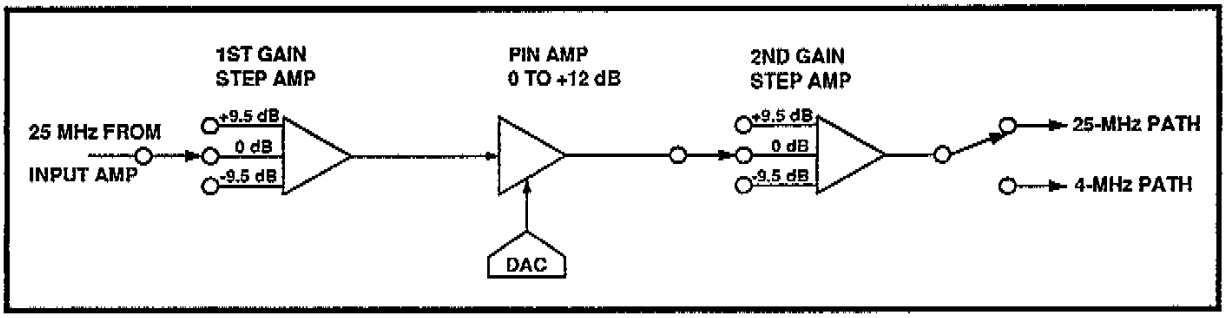


Figure 5-6. Gain Step Amplifiers.

25 MHZ PATH

See Figure 5-5. The 25 MHz path is used with the two widest bandwidths, 3 MHz and 10 MHz. The IF signal from the Gain Step Amplifiers is amplified and filtered through this path. The path is also used by the 29 MHz oscillator signal to allow the Main Processor to measure the oscillator frequency. The 25 MHz Path consists of two fixed-gain amplifiers, a bandpass filter, and a step-up transformer that produces 6 dB gain.

The 25 MHz IF signal is applied to the two fixed-gain amplifiers, each of which amplifies the signal by approximately 8.5 dB. A switch between the two amplifiers breaks the signal path to allow the 29 MHz signal to be applied to the second stage.

The second fixed-gain amplifier applies the IF signal through a 10 MHz bandpass filter. (The shape of IF signals that have passed through the 3 MHz filter in the Input Amplifier are not affected by this filter.) In the 10 MHz RES BW position, the observed response curve comes from the combined effects of the Helical filter in the 3rd Converter and this 10 MHz filter.

The filtered output is applied to a step-up transformer, which provides approximately 6 dB gain. The IF signal from the transformer secondary is applied to the Output Amplifier through a switch that is opened when the 4 MHz Path is in use, or when the 4 MHz Oscillator signal is used for correction routines.

4 MHZ PATH

The 4 MHz Path is used when one of the twelve narrower resolution bandwidths are selected. This path converts the 25 MHz third IF to the 4 MHz fourth IF, then filters and amplifies that signal for application to the Output Amplifier. A bank of synchronously-tuned filters is automatically tracked to a common center frequency, producing one of twelve resolution bandwidths ranging from 3 Hz to 1 MHz. The 4 MHz Path consists of a Fixed-gain Amplifier, Notch Filter, Mixer, Resonators, Band-pass Filter, and Noise Filter.

Fixed-gain Amplifier

The 25 MHz signal from the bandwidth selector switch passes through a Fixed-Gain Amplifier that produces approximately 3 dB gain. The amplifier output drives the Notch Filter.

Notch Filter

The amplified 25 MHz IF signal is applied to the Notch Filter, which has a center frequency of 25 MHz and a attenuation quality of approximately –85 dBc at 33 MHz. This filter blocks the 33 MHz image of the frequency conversion in the next section. The filtered IF signal is applied to the Mixer.

Mixer

The 25 MHz third IF signal is mixed with the 29 MHz Local Oscillator signal to produce a 4 MHz fourth IF signal. Test connector P164 provides a –36 dBm level when there is a full-screen display.

Resonators

The Resonators consist of Pre-filter Gain, six resonator elements, three Fixed-gain stages, and Post-filter Gain. See Figure 5-7, which illustrates the resonator arrangement.

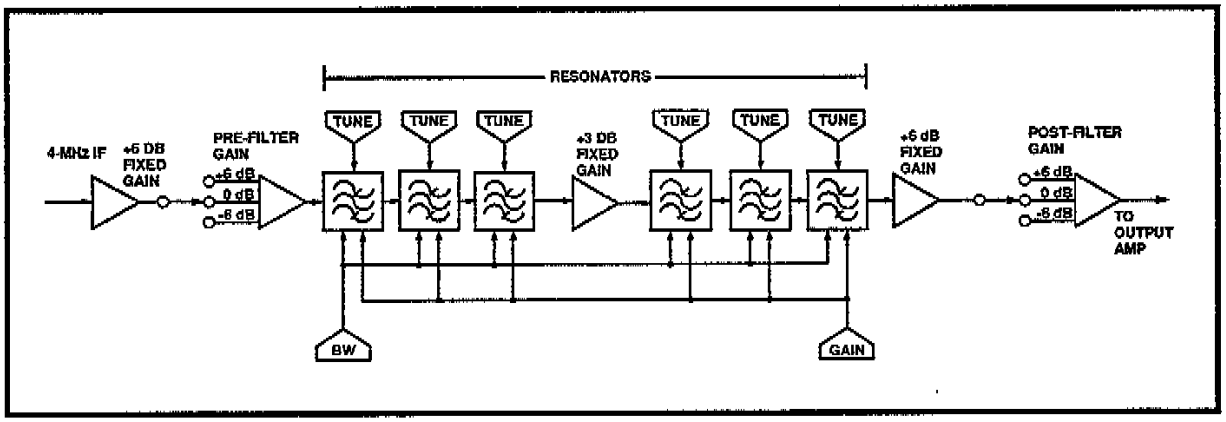


Figure 5-7. Resonator Section.

The Fixed-gain Amplifier produces a gain of approximately 6 dB. The amplified IF is then applied to the Pre-filter Gain Amplifier.

The gain of the Pre-filter and Post-filter Gain stages is set, depending on the selected bandwidth, to –6 dB, 0 dB, or +6 dB. The input gain selection is made to permit the resonators to operate at optimum dynamic range. Typically, medium-bandwidth filters use 0 dB gain settings, wide-bandwidth filters use +6 dB Pre-filter gain and –6 dB Post-filter gain, and narrow-bandwidth filters use –6 dB Pre-filter gain and +6 dB Post-filter gain. Overall gain of the Resonator section is always approximately 0 dB.

The Resonators consist of two banks of three filters connected in series. Each filter consists of a crystal resonator that provides filtering for the narrower seven bandwidths (3 Hz to 3 kHz) and an LC resonator that is used for the next five bandwidths (10 kHz to 1 MHz). The bandwidth of all six resonators, variable from 3 Hz to 1 MHz, is controlled by a single DAC. Another DAC controls the gain of all six resonators. The Resolution Bandwidth self-correction routine adjusts the gain and bandwidth of all resonators.

The center frequency of each resonator (4 MHz) is tuned by a separate DAC, allowing precise control of resonator tracking. The Resonator Tracking self-correction routine adjusts the center frequency of each filter. A fixed-gain amplifier between the first and last set of resonators produces 3 dB of gain to drive the last three sections.

The resonators are tuned as follows.

1. The OSC switch is closed, placing the 25 MHz crystal oscillator in operation. The 4 MHz path is chosen, so the 25 MHz oscillator signal passes to the mixer to produce a precise 4 MHz IF signal.
2. The first of the six resonators is set to narrow bandwidth; the remaining five are set to wide bandwidth. The 4 MHz IF signal excites the resonators at the input frequency.
3. The 25 MHz oscillator is turned off. The wide-bandwidth resonators decay in oscillation very rapidly, but the narrow-bandwidth resonator rings at its resonant frequency for a longer period. This signal frequency is routed through the Log Processor to be counted by the Period Counter, discussed later in this section under Frequency Control.
4. The Tune DAC for the narrow-bandwidth resonator cell is adjusted to compensate for the difference between the actual resonant frequency and the 4 MHz IF signal.

5. The first cell is repeatedly excited and its output frequency measured and tuned until it is precisely on center frequency.

6. Successively, each of the remaining cells is tuned through the process described for the first resonator cell.

Overdrive Compensation Amplifier

From the Post-filter Gain stage, the 4 MHz IF is applied to the Overdrive Compensation Amplifier. This amplifier maintains the signal level applied to the Log Processor within its dynamic range when mixer overdrive is selected. When 0 dB Mixer Overdrive is selected, the stage has 20 dB gain. When 10 dB mixer overdrive is selected (increasing the overall signal to noise ratio in the instrument), the stage has 10 dB gain and signal levels up to this point in the instrument are increased 10 dB by reducing RF attenuation 10 dB, increasing the signal to noise ratio. When 20 dB mixer overdrive is selected (RF attenuation reduced by 20 dB), the stage has 0 dB gain, resulting in 20 dB higher signal levels through the instrument up to this point. When 30 dB mixer overdrive is selected, the stage still has 0 dB gain, but the Gain Step Amplifier gain is reduced by 10 dB. Thus, although the front end receives 30 dB of overdrive, the 4 MHz path receives only 20 dB overdrive. Note that mixer overdrive is not available when 3 Hz bandwidth is selected.

The Overdrive Compensation Amplifier drives two filters, both having a center frequency of 4 MHz. The first, which is always in the 4 MHz path, has a bandwidth of 1.8 MHz to limit noise. The second is a 10 kHz bandpass filter that is switched into the path for additional noise limiting when the RES BW is from 3 Hz to 10 kHz.

29 MHZ OSCILLATOR

The 29 MHz Oscillator provides a tunable 29 MHz signal to mix with the incoming 25 MHz third IF signal. A DAC (controlled by the Main Processor) sets the 29 MHz by counting the oscillator output. The 25 MHz and 4 MHz paths are broken and the 29 CNT switch is closed to allow the oscillator output signal to pass through to the Output Amplifier. This signal is divided in the Log Processor, then applied to the Period Counter module for measurement.

4 MHZ OSCILLATOR

The 4 MHz Oscillator is connected into the output path to establish the top-screen level for the Display Law self-correction routine. It is also used for the Peak Detector self-correction routine. When the 4 MHz oscillator signal is connected into the signal path, the signal amplitude at the Log Processor input is +16 dBm, which corresponds to a full-screen vertical display.

OUTPUT AMPLIFIER

The Output Amplifier consists of a preamplifier that drives two output stages. The first furnishes a +16 dBm signal to drive the Log Processor input. The second output is the +9 dBm rear-panel IF OUT signal.

DIGITAL CONTROL

The Digital Control circuits set the proper gain factors to match the operating mode, provide switching to route the 29 MHz or 4 MHz oscillator signals for self-correction and resonator tracking routines, and select the proper filters for the resolution bandwidth setting.

LOG PROCESSOR

The A18 Log Processor module provides display scaling, amplitude calibration, video amplification and detection, flatness compensation, and an IFPC output signal for the Period Counter. Refer to Figure 5-8. The module consists of four major circuits: Log Amplifier and Detector, Video Preprocessor, Frequency Divider, and Digital Control.

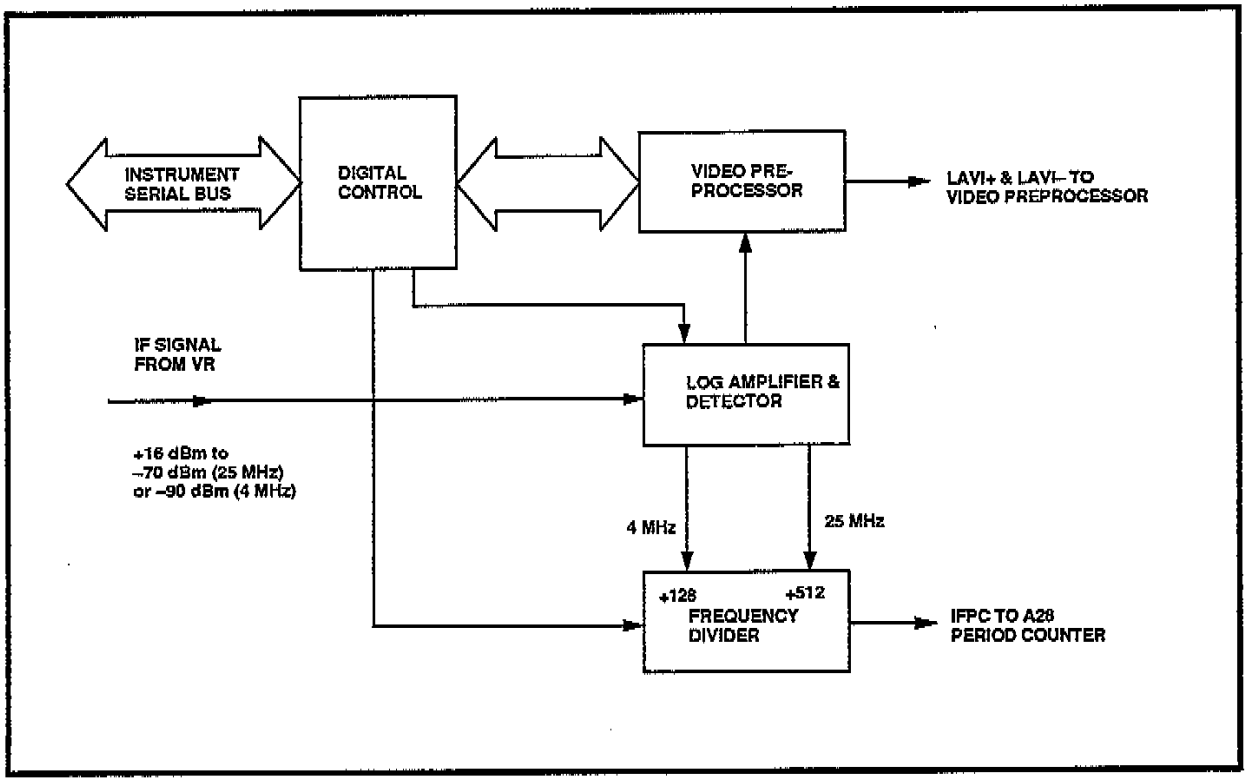


Figure 5-8. Log Processor module block diagram.

LOG AMPLIFIER

The Log Amplifier and Detector, which occupies the front side of the A18 Log Processor Module, provides logarithmic amplification of the incoming IF signal over a wide range of input amplitudes and detects the signal envelope to produce a video signal that is applied to the Video Preprocessor (located on the rear side of A18). This section consists of the 25 MHz Low-pass Filter, First Log Amplifiers, 4 MHz Low-pass Filter, Second Log Amplifiers, Reference Current Source, Summing Network, and Noise Filters. See Figure 5-9.

The incoming IF signal from the VR circuit (25 MHz or 4 MHz) first passes through the 30 MHz Low-pass Filter. From there it is applied to the first of a chain of ten detector-limiter cells, each having a small-signal gain of 10 dB. The limited signal at each limiter output is detected and passed to a summing point, producing the overall effect of a logarithmic output. The inset in Figure 5-9 illustrates the connection arrangement of three of the ten cells to the summing point. Each stage is a 10 dB amplifier with a sharp limiting characteristic.

The sum of signals from the Log Amplifier is the detected video signal. It is sent through one of two ripple filters to remove the IF frequency component from the video signal. If the IF signal is 4 MHz, a 1 MHz Low-pass filter removes the ripple. If the signal is 25 MHz, the 10 MHz Low-pass filter removes the ripple. From the Summing Network, the signal is sent through a 1 MHz bandpass filter to reduce noise. From there, the video signal is fed to the Video Preprocessor.

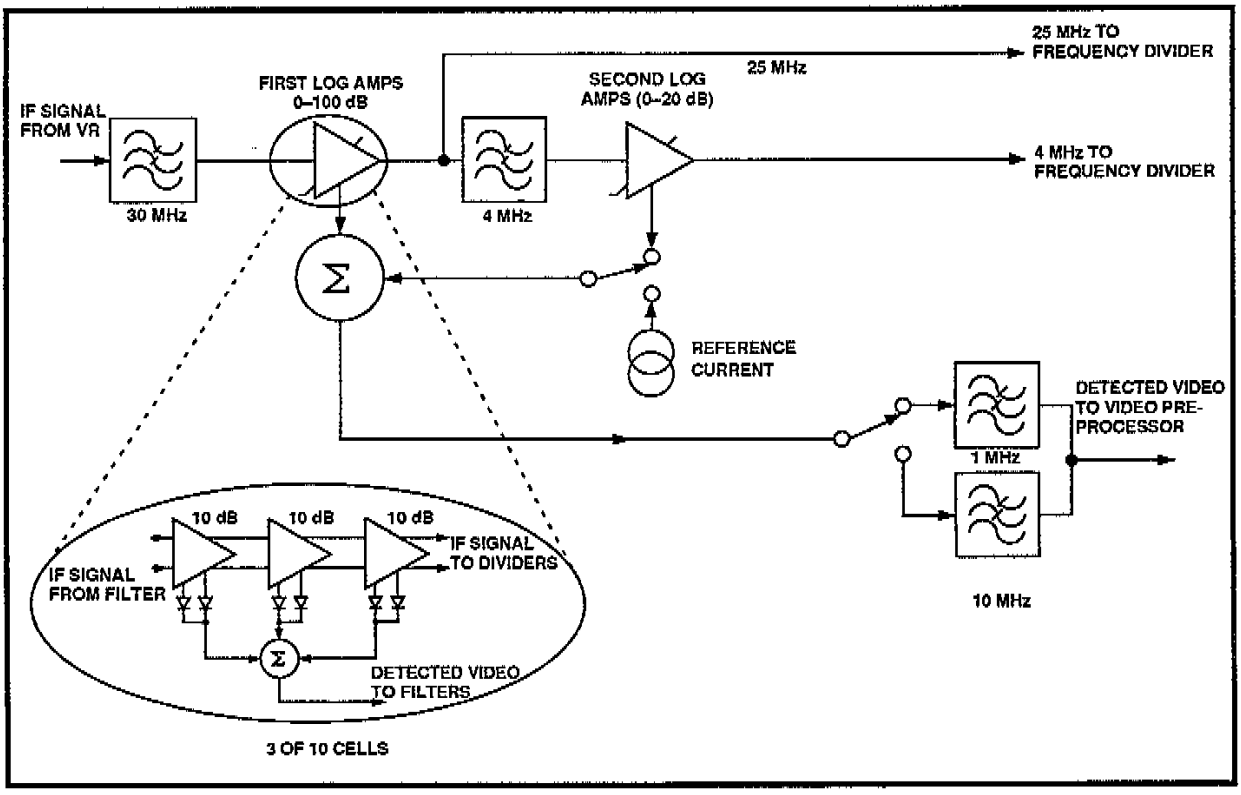


Figure 5-9. Log Amplifier block diagram.

The Second Log Amplifier is identical to the First Log Amplifiers, except that it consists of two 10 dB amplifier cells and is switched into the circuit only when the 4 MHz IF signal is used. This provides an additional 20 dB of log dynamic range to compensate for the additional loss caused by the fourth conversion. The output signal from this amplifier is sent to the Summing Network and to the Frequency Divider.

When the IF signal is 25 MHz, the signal is fed to the Frequency Divider and the Summing Network. A Reference Current source is switched into the circuit to maintain a constant level out of the Summing Network. From the Summing Network, the detected video signal is sent through a 10 MHz ripple filter to reduce noise, then to the Video Preprocessor.

VIDEO PREPROCESSOR

The Video Preprocessor amplifies and processes the signal to provide proper scaling, offset, screen position, and the selected display mode (Lin, Square Law, or Log display.) The section (see Figure 5-10) consists of the Current Converter, the Variable Gain Amplifier, the Exponential Amplifier, and the Current to Voltage Converter.

The single-ended video signal from the Log Amplifier is converted by the Current Converter to a differential signal. The offset of this stage is controlled by the 12-bit Log Offset DAC. The Log Offset data increases the video level for REF level settings between –40 dBm and –140 dBm, depending on the active path and the selected frequency band. The flatness data, which is determined during self-correction and stored in EEPROM memory, has a correction range of 0 to 12 dB. The differential video signal is fed to the Variable Gain Amplifier.

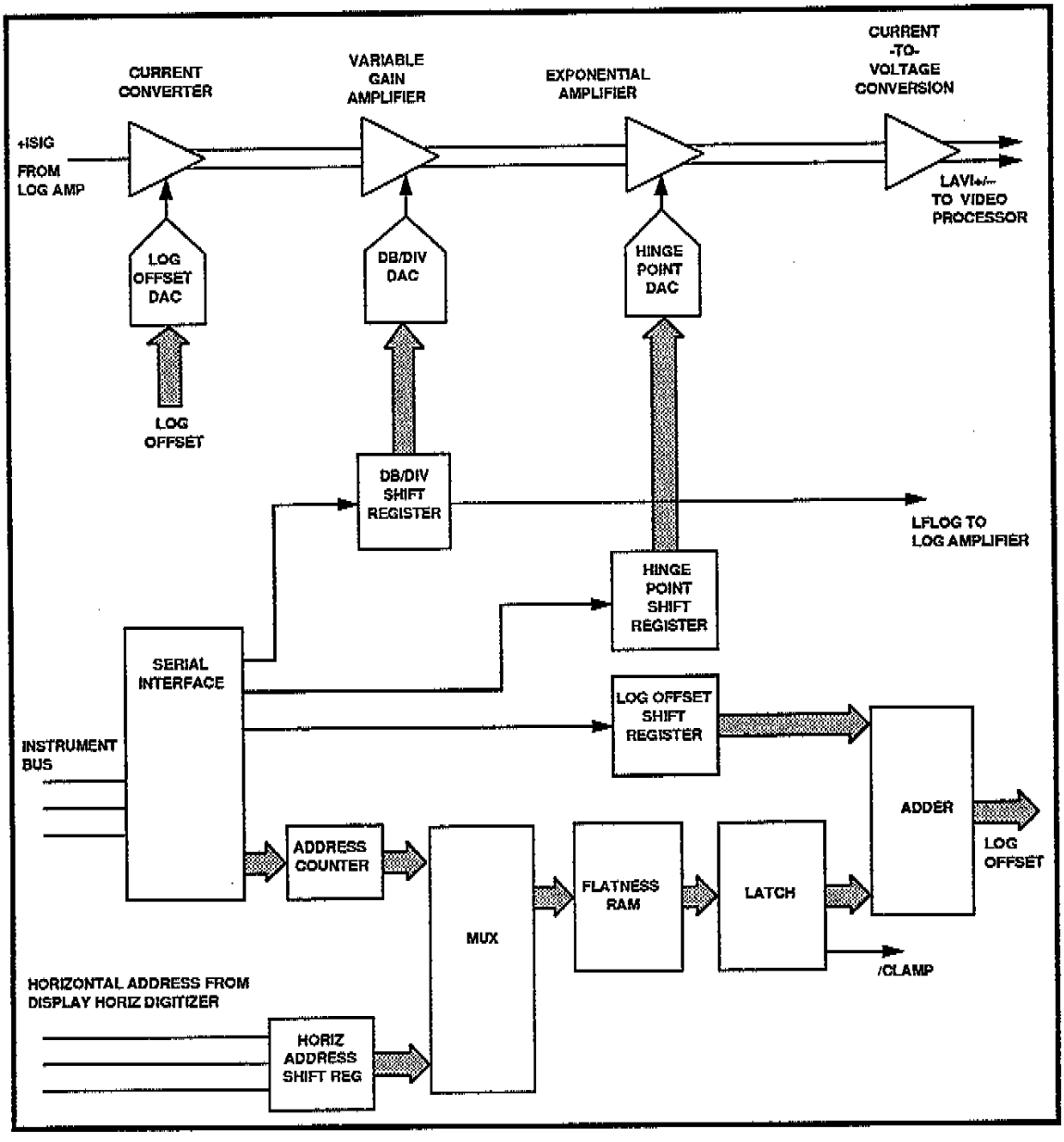


Figure 5-10. Video Preprocessor block diagram.

The Variable Gain Amplifier provides calibrated scales that range from 1 dB/Div to 15 dB/Div. The amplifier is controlled by the 12-bit dB/Div DAC, which allows the Processor to control the gain. This DAC ordinarily sets the control current based on Log scaling ratios. When Lin mode is selected, 10 dB/Div scaling is used. When Square Law mode is selected, 5 dB/Div scaling is used.

The Exponential Amplifier converts the signal back to linear-scale mode when a LIN display is selected. It is also used in the Square Law mode. The Lin Baseline adjustment sets the baseline for 0 volts. The Exponential Amplifier is controlled by the 12-bit Hinge Point DAC, which sets the hinge point to the top of the screen for whichever vertical scale mode and setting is selected. (The hinge point is the top-of-screen reference for vertical scaling in log mode, where signals at top-of-screen do not change amplitude with dB/div scale changes.

The Current to Voltage Converter transforms the differential current into differential voltage signals (LAVI+ and LAVI–) to drive the Video Processor.

Digital Interface

Serial data from the Serial Interface is applied to the dB/Div Shift Register, which drives the dB/Div DAC; the Hinge Point Shift Register, which drives the Hinge Point DAC; and to the Address Counter and Log Offset Shift Register. The Address Counter and the Horizontal Address Shift Register both feed a Multiplexer that determines the timing for inserting the Flatness RAM data into the Latch, for combination with the Log Offset data in the Adder. The flatness data is added at every fourth sweep position. The Main Processor loads flatness data that has been stored in EEPROM during calibration into specific flatness RAM addresses by incrementing the Address Counter.

Clamping occurs when sweeping outside the selected frequency range, at which point the RAM output is all ones. This activates the /CLAMP line, the second output of the Latch. This signal is fed to the Video Processor to indicate when that circuit must initiate the baseline clamping circuit.

Frequency Divider

A TTL-level squared signal from the Log Amplifier is applied to the Frequency Divider, which divides the 4 MHz signal by a factor of 128 or the 25 MHz signal by a factor of 512. The output of the divider is then sent as the IFPC signal to the Period Counter.

VIDEO AND DISPLAY SECTION

The Video and Display Section performs the following functions:

- Digitizes the Log Processor output; that is, generates the digitized data from the Log Processor output signal.
- Transforms digitized data into signals for the display.
- Processes the detected Log Processor output signal for display.
- Amplifies internal or external signals to drive the deflection plates.
- Controls display sequencing.
- Drives the color shutter.
- Produces CRT voltages.

See Figure 5-11. The Video and Display section consists of the A20 Video Processor module, A24 Digital Storage module, A22 Display Amplifier module, A23 High-voltage module, A4 Color Shutter, and the CRT.

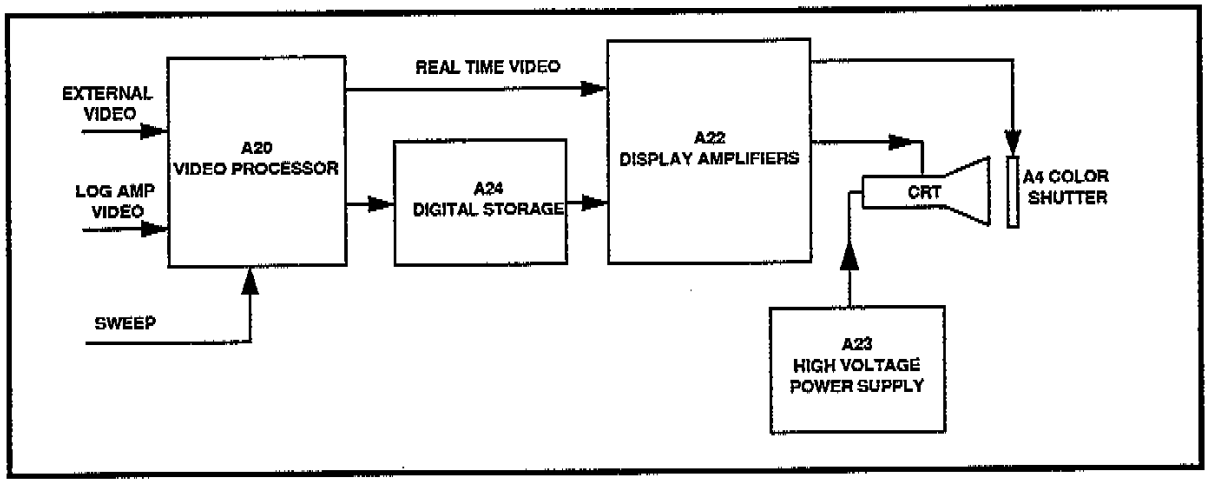


Figure 5-11. Display System Block Diagram.

VIDEO PROCESSOR

The A20 Video Processor filters, amplifies, and digitizes the incoming video signal from either the Log Amplifier video or the rear-panel external video input. Digitizing of the video signal is performed in one of four acquisition modes (MAX, MIN/MAX, MIN, and SAMPLE). The digitized video signal is then sent to the Digital Storage section. If a real-time (analog) display is selected, the analog video signal is amplified and sent to the Display Amplifiers. Out-of-range clamping is also initiated by this section. Refer to Figure 5-12. The Video Processor consists of the Video Select circuit, Video Filters, Peak Detectors, Video Buffer and Clamp, Internal Trigger Buffer, Analog Max/Min Detectors, 10-Bit A to D Converter, 10-Bit Tracking A to D Converter, Vertical Data Processor, Horizontal Data Sequencer, and Horizontal Real-time Amplifier.

Video Select

The differential LAVI signals from the Log Processor are applied to the Video-Select circuits. Input amplitude for a full-screen display is approximately ±0.375 volts. The Video Select circuits allow selecting between the LAVI signal from the Log Processor or the EXTVI signals from the rear-panel Accessory connector. The selected signal drives the Video Filters. A bandwidth and amplitude limiter on the EXTVI input protects the Video Processor circuits.

Video Filters

The video signal from the Video Select circuit is fed through low-pass filtering that ranges from 0.03 Hz to 300 kHz in 1-3-10 sequential steps, controlled via the menu display. The differential signal from the filter output is applied to the Peak Detectors, Video Buffer and Clamp, Internal Trigger Buffer, and Analog Min/Max Detectors.

Internal Trigger Buffer

The internal trigger buffer samples the filtered video signal to produce the TRIG signal for triggering internal sweeps. Output amplitude is approximately ±0.5 volts centered at a –4.5 volt offset level.

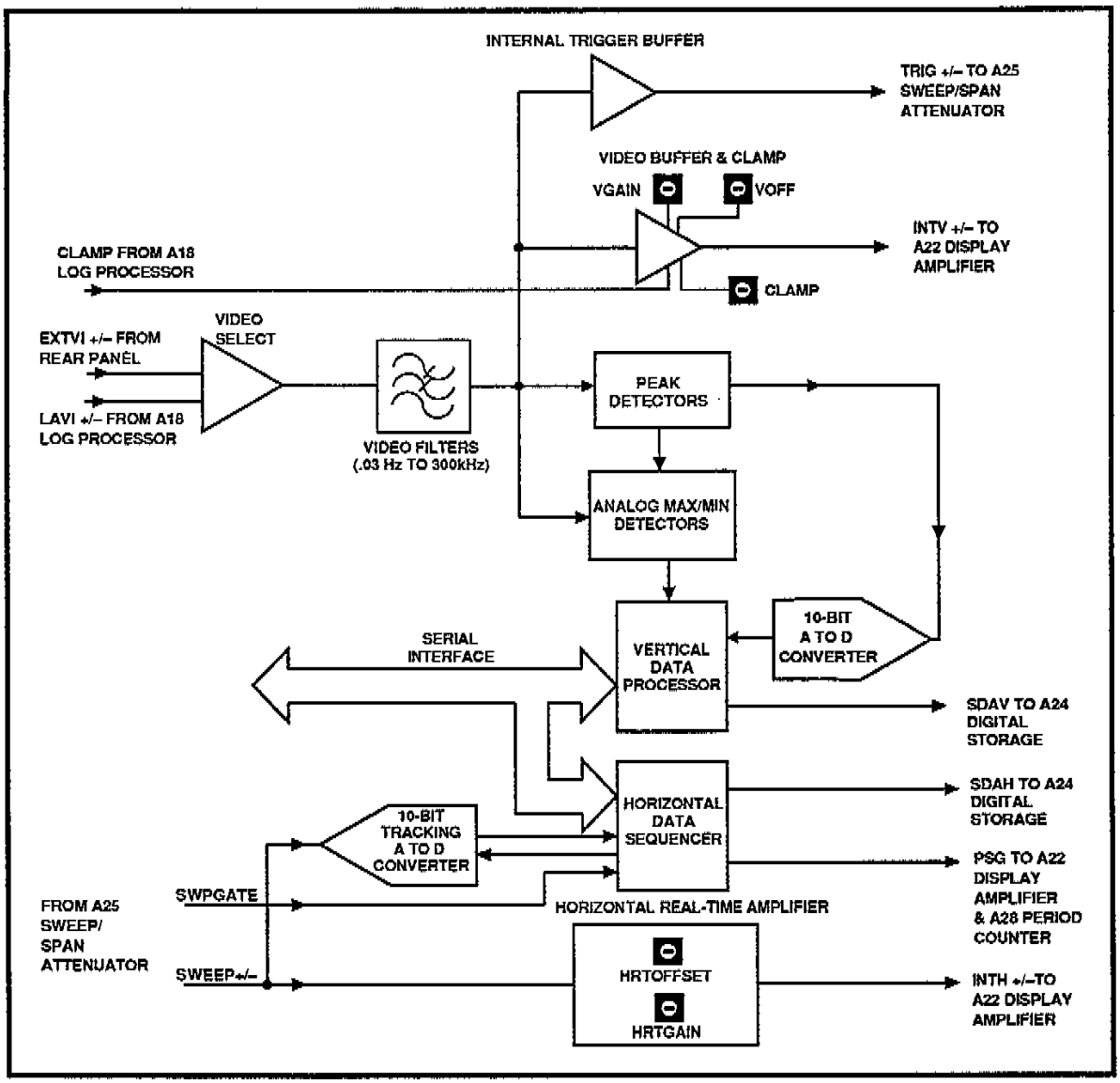


Figure 5-12. Video Processor Block Diagram.

Peak Detectors

The filtered video signal from the Filter Selector is applied to four sample-and-hold circuits, two for the negative signal excursion, and two for the positive signal excursion. The detector pairs operate alternately to ensure that a signal peak is not missed. The peak detector operates in one of three modes: 1) Peak-detect the video signal; 2) Sample or track the signal; 3) Hold the current signal amplitude. This allows the stage to sample and hold the signal or peak-detect and hold the signal. The four output signals, which are sampled representations of the analog video signal, successively appear at the input of the 10-bit A to D Converter and the Analog Max/Min Detectors. Output amplitude is 0 to +2.5 volts for a full-screen display.

Analog Max/Min Detectors

The Analog Max/Min Detectors are a set of four high-speed comparators that compare the Peak Detector output with the video signal. This stage is used when the MAX/MIN display mode is selected. A strobe signal that is generated by the Main Processor is used to select stored samples of the filtered video signal for comparison with the current Peak Detector value.

Internal Video Buffer and Clamp

The filtered video signal is amplified to produce a ± .375 volt signal for application to the Display Amplifier. The clamping signal from the Log Processor pulls the video signal to the baseline amplitude when out-of-band displays occur. The VGAIN, VOFF, and CLAMP adjustments set the vertical gain, offset, and clamping level, respectively.

10-Bit A to D Converter

As each sample is taken by the Peak Detectors and applied to the 10-bit A to D Converter, this circuit converts that signal value to a 10-bit parallel word, which is passed to the Vertical Data Processor.

Vertical Data Processor

The Vertical Data Processor acts as a vertical acquisition circuit. It converts the 10-bit samples from the 10-bit A to D Converter to a 10-bit serial word that represents vertical signal amplitude. This word is sent via the SDAV line to the Digital Storage module. Storage registers hold samples for comparison with the Peak Detector output signal when MAX/MIN, MAX hold, or MIN display mode is selected.

10-Bit Tracking A to D Converter

The 10 volt SWEEP ramp signal from the Sweep/Span Attenuator module is applied to the 10-bit Tracking A to D Converter, where it is converted into a 10-bit parallel word whose value corresponds to input signal amplitude. Internal up-down comparators determine the direction of sweep movement. The parallel word is applied to the Horizontal Data Sequencer.

Horizontal Data Sequencer

The digitized sweep from the tracking A to D Converter is converted into a serial 10-bit word that represents the horizontal location of the analog sweep. Each word becomes the RAM address for the corresponding vertical data. The serial data is fed to the Digital Storage Module via the SDAH line.

Horizontal Real-time Amplifier

The 10 volt SWEEP signal is also applied to the Horizontal Real-Time Amplifier, where it is amplified by a factor of 0.15. Offset and gain adjustments permit setting the sweep signal for proper amplitude and centering before application to the Display Amplifier module. Full-screen display amplitude is approximately 1.5 volt p-p.

DIGITAL STORAGE

The Digital Storage module generates video and sweep signals for digitized displays. It consists of the Acquisition Section, Display µProcessor, and Vector Processor. Status LED indicators on the module reveal Digital Storage module operating condition. See Figure 5-13.

Acquisition Section

The Acquisition Section receives the serial SDAV and SDAH serial data from the Video Processor and stores this data in RAM. As each vertical word is clocked into a register, the corresponding horizontal word is used to generate a RAM address for acquisition memory. The Acquisition Section consists of the Acquisition Data Shift Register, Acquisition Address Shift Register, Acquisition Location Shift Register, Acquisition & CPU RAM, and Acquisition Control Logic.

The 4.608 MHz DIGCLK signal clocks the data (SDAV and SDAH) from the Video Processor into the shift registers. SDASE is the Serial Data Shift Enable signal from the Video Processor, which enables the data shifting. SDASHE is the Serial Data Horizontal Shift Enable signal, also from the Video Processor, which enables the shifting of horizontal data into the Acquisition Location Shift Register.

The Acquisition Control Logic arbitrates between the RAM requirements of the Acquisition Section and the CPU. Since the RAM is shared by both these circuits, handshaking logic in the Acquisition Control Logic prevents simultaneous access attempts by these two circuits.

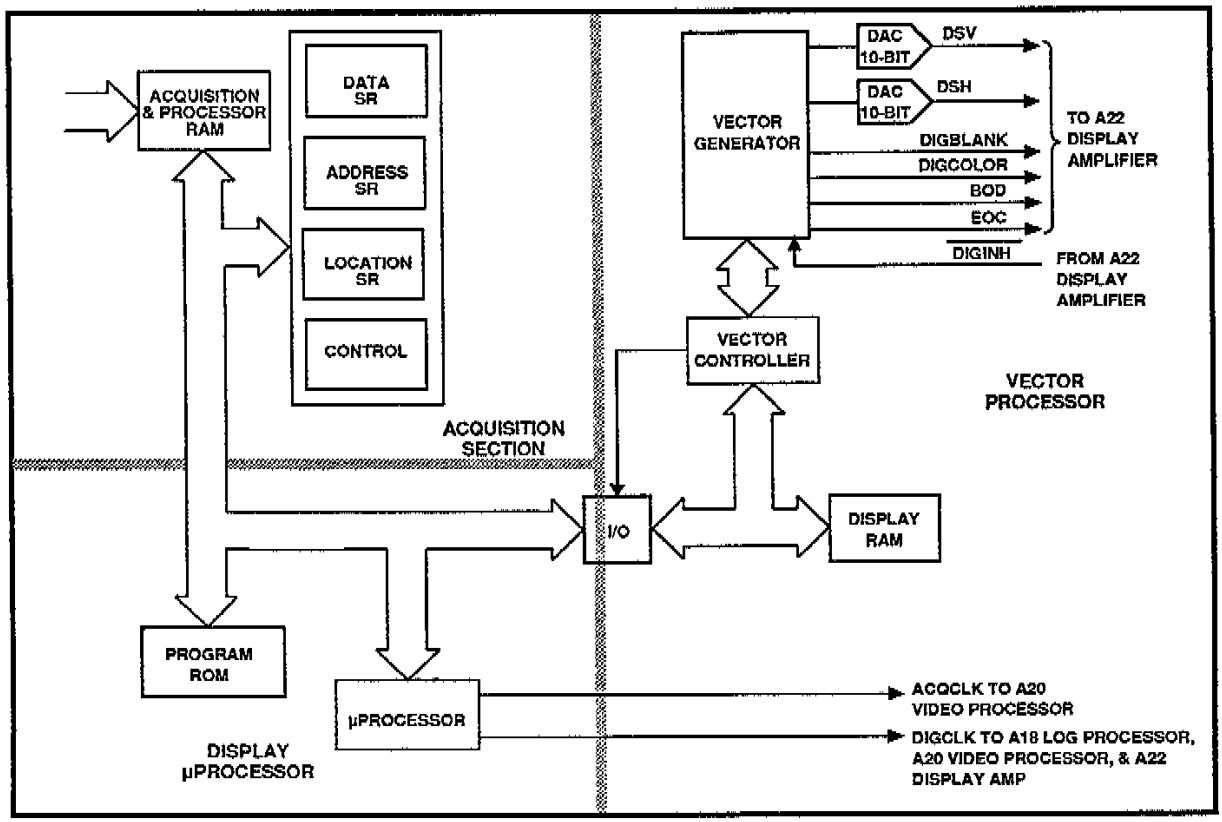


Figure 5-13. Digital Storage module block diagram.

The Acquisition Section operates in the following manner.

1. The Acquisition Data Shift Register latches vertical data for storage in RAM:
   a. The serial SDAV data is clocked into the shift register by the DIGCLK signal.
   b. SDASE latches the serial data into parallel latches.
2. Simultaneously, the Acquisition Address Shift Register accepts the horizontal data to generate RAM addresses that correspond to the current screen location:
   a. The serial SDAH data is clocked into the shift register by the DIGCLK signal.
   b. SDASE enables the shift register output lines, presenting a parallel address word for storage in the RAM for acquisition memory.
3. The Acquisition Location Shift Register manipulates the horizontal sweep location data to accommodate sweep update, marker and frequency calibration:
   a. The serial SDAH data is clocked into the shift register by the DIGCLK signal.
   b. SDAHSE enables the shift register output lines, presenting a parallel address word that can be sent directly to the Display Section Vector Controller.

Display µProcessor

The Display µProcessor consists of the 80C186 microprocessor, Program ROM, and I/O port. The Display Processor converts acquired data into move or draw commands for use by the Vector Processor, performs math functions as directed by the Main Processor, modifies the display control program as required to update the screen readout, and generates the 9.216 MHz ACQCLK and 4.608 MHz DIGCLK signals that synchronize signal acquisition.

The I/O Port provides arbitration between the Display Microprocessor bus and the Vector Processor bus. As a result, the Display RAM is dual-ported between the two. The Display Microprocessor generates and loads the display program into display RAM. The Vector Processor executes the display program stored in display RAM.

Vector Processor

The Vector Processor consists of the Vector Controller, Vector Generator, Display RAM, part of the I/O, and two 10-bit digital-to-analog converters. The circuit executes the display program, produces video and sweep signals (including readouts and graticules), and produces handshaking signals for display sequencing, blanking, and Color Shutter operation.

Handshaking signals include the following:

DIGCOLOR controls the color state of the Color Shutter.

DIGBLANK provides display blanking data for intensity control.

BOD is a handshaking signal between the Digital Storage and Display Amplifier modules to indicate display color change activity.

EOC informs the Display Amplifier of the end of a character, for purposes of chopping between real-time and digital storage displays (if a real-time waveform is being viewed).

Vector Controller

The Vector Controller executes a display program that consists of move-draw commands stored in the Display RAM by sending ΔX, ΔY, and ΔZ data to the Vector Generator. The ΔX and ΔY information is converted into equal incremental steps between points on the screen. This ensures that displayed trace intensity remains constant. During Color Shutter transition periods, display mode changes, and real-time displays, Vector Controller activity is suspended by the /DIGINH signal.

Vector Generator

The Vector Generator converts ΔX data and ΔY data into 10-bit parallel data words. The horizontal data word is converted by a 10-bit DAC to a horizontal signal (DSH). An interpolation filter smooths the DSH output signal, which is sent to the Horizontal Deflection Amplifier in the Display Amplifier module.

The 10-bit parallel vertical data word is also converted by a 10-bit DAC to a vertical signal (DSV). An interpolation filter smooths the DSV output signal, which is sent to the Vertical Deflection Amplifier in the Display Amplifier module.

DISPLAY AMPLIFIER

The A22 Display Amplifier module produces the CRT deflection signals, produces the CRT control signals, generates the COLOR+ signal that regulates Color Shutter operation, selects the signal source for horizontal and vertical deflection, and controls display sequencing. The module consists of the Deflection Amplifiers, Display Sequencer, Color Shutter Driver, Z-axis Control, and five Digital-to-analog converters that decode the focus, intensity, and trace rotation data from the Main Processor. See Figure 5-14.

Deflection Amplifiers

The Vertical and Horizontal Deflection Amplifiers provide voltage amplification to drive the CRT deflection plates. A multiplexer in each amplifier allows the Main Processor to select from three signal sources, digitized, internal real-time, or external real-time.

Vertical Deflection Amplifier. Three signal sources are available at the input of the Vertical Deflection Amplifier:

1. The INTV (Internal Vertical real-time) signal from the Video Processor, which is a ±600 mV INTV differential drive signal for full-screen deflection.
2. The EXTV (External Vertical real-time) signal from the rear-panel accessory connector. An amplitude and bandwidth limiter on the EXTV line protects the amplifier from externally-applied signals that are out of specified frequency or amplitude range. The EXTV input can be driven differentially or single-ended. Sensitivity is ±750 mV for full-screen deflection.
3. The DSV (Digital Storage Vertical) signal from the Digital Storage module. The DSV signal is approximately 1.5V p-p for full-screen deflection, since it also contains graticule and readout data and is single-ended.

A multiplexer within the Vertical Deflection Amplifier selects one of the three signals for amplification. VGAIN and VCTR adjustments set the amplifier gain and display centering. Differential output voltage from the Vertical Deflection Amplifier is approximately ±60 volts full deflection with a common-mode output level of +40 volts.

Horizontal Deflection Amplifier. Three signal sources are available at the input of the Horizontal Deflection Amplifier:

1. The single-ended INTH (Internal Horizontal real-time) signal from the Video Processor is applied to the Horizontal Deflection Amplifier. Input signal amplitude varies depending on the selection of expanded or compressed display mode. When expanded mode is selected, no menu appears on the display and the entire CRT screen is available for signal display. In this instance, the INTH signal is approximately ±750 mV to produce full-screen deflection.

   When compressed mode is selected, display area is reserved at the right side of the display for the menu. In this instance, the INTH signal is approximately ±600 mV to produce full-screen deflection. The INTH signal is slightly offset to accommodate the menu on the right side of the display.)

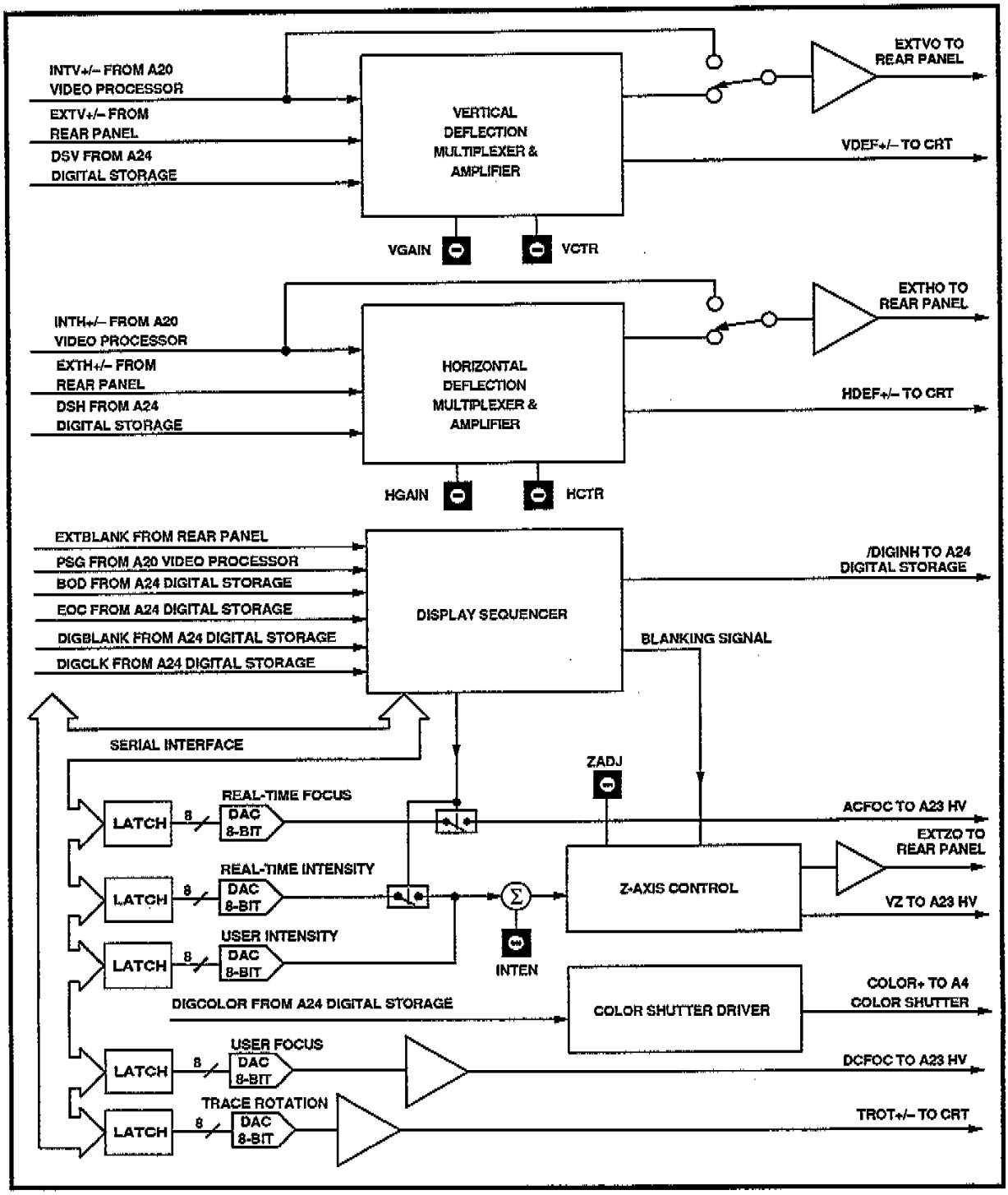


Figure 5-14. A22 Display Amplifier Module Block Diagram.

2. The EXTH (External Horizontal real-time) signal from the rear-panel accessory connector. An amplitude and bandwidth limiter on the EXTH line protects the amplifier from externally-applied signals that are out of specified frequency or amplitude range. The EXTH input can be driven differentially or single-ended. Sensitivity is ±750 mV for full-screen deflection.

3. The DSH (Digital Storage Horizontal) signal from the Digital Storage module. The DSH signal is approximately 1.5V p-p, since it also contains graticule and readout data and is single-ended.

A multiplexer within the Horizontal Deflection Amplifier selects one of the three signals for amplification. HGAIN and HCTR adjustments set the amplifier gain and display centering. Differential output voltage from the Horizontal Deflection Amplifier is approximately ±60 volts full deflection with a common-mode output level of +40 volts.

Rear-panel output selection. The following applies to both amplifiers:

Jumpers on the Display Amplifier module select the sources for the signals to be applied to the rear-panel output signal buffers. One jumper position connects the internal real-time signal to the output buffer, by-passing the multiplexer. The other position connects to an amplifier output that has unity gain, allowing a sample of the composite display to be routed to the rear panel. The jumpers allow the user to exclude readout and graticule signals when a chart recorder or other such application is connected to the rear-panel connector and only the analog signal is desired. The jumpers are normally set at the factory for real-time signal output. Refer to ***Section 4—Maintenance*** for directions on changing the jumper setting.

Display Sequencer

The Display Sequencer manages the CRT display. Input signals are:

EXTBLANK, a rear-panel input that allows CRT blanking from an external source.

PSG from the Video Processor, which is the real-time precision sweep gate signal.

BOD is a handshaking signal between the Digital Storage and Display Amplifier modules to indicate display color change activity.

EOC informs the Display Amplifier of the end of a character, for purposes of chopping between real-time and digital storage displays (if a real-time waveform is being viewed).

DIGBLANK from the Digital Storage module, which blanks digital displays.

DIGCLK from the Digital Storage module, which synchronizes display sequencing with the Digital Storage operations.

Serial Interface control data from the Main Processor.

Output signals are:

Vertical and Horizontal select signals, which drive the deflection amplifier multiplexers.

/DIGINH, which shuts down the Digital Storage Vector Generator when switching shutter colors, during display mode changes, and during real-time displays.

A blanking signal that drives the Z-axis Control.

Real-time focus and intensity switch control.

The Display Sequencer permits simultaneous display of digitized and real-time traces. At slow sweep rates, the two displays are chopped. At sweep rates faster than 50 µs, the entire digitized trace and readout information is alternately displayed with multiple real-time sweeps.

Digital-to-analog Converters

Five Digital-to analog converters control the CRT focus, intensity, and trace rotation. The Serial Interface loads the selected latch with data from the Main Processor. The parallel latch output lines drive the respective DAC, producing a voltage that corresponds to the data applied to the latch. The Display Sequencer controls two of these circuits: the Real-time Focus circuit, which provides a path for fast focus changes, and the Real-time Intensity path, which alters the intensity when a real-time display is selected. The additional current from the Real-time Intensity path is summed with the User Intensity path and current from the INTEN adjustment. The output of the summing network provides drive current for the Z-axis Control.

Two other converters control CRT functions. The User Focus path provides a DC focus control voltage, ranging from 0 to 2 volts, that is amplified to drive the High-voltage DC Focus Restorer. The Trace Rotation path provides a ±12 volt level to drive the trace rotation coil in the CRT.

Z-axis Control

The Z-axis control circuit amplifies the variable current from the summing network and interrupts that current under the control of the blanking signal from the Display Sequencer. The resulting VZ output signal is a rectangular blanking pulse that ranges from approximately +5 volts to +75 volts. The VZ signal is applied via the High-Voltage module to the CRT control grid to blank the display during the negative signal excursion. A sample of the VZ signal is fed to the rear-panel accessory connector through a buffer; the output voltage is a pulse that ranges from approximately 0 volt to +1 volt.

Color Shutter Driver

The Color Shutter Driver consists of a delay generator and an oscillator that operates at 2 to 4 kHz (typically 3 kHz). The DIGCOLOR signal from the Digital Storage module switches at the display refresh rate (nominally 70 Hz), depending on the content of the display. This signal selects between the red and green shutter states. The delay generator selects delay times between Color Shutter on and off periods by gating the oscillator signal. Green switching delay is 350 µs, red switching delay is 3.2 ms, and phosphor decay time delay is 1.5 ms for each color. The resulting output signal, COLOR+, is approximately 42 volts p-p centered about 0 volts in 3 kHz bursts, which corresponds to green display periods; and 0 volt, which corresponds to red display periods.

HIGH-VOLTAGE POWER SUPPLY

The A23 High Voltage Power Supply provides the bias and control voltages required to operate the CRT. The module contains an oscillator that converts power from a low-voltage unregulated supply to a voltage level usable by the CRT and related circuitry. Because of the high voltages present, a portion of the circuitry is encapsulated.

WARNING

The CRT anode lead retains a high voltage charge after the instrument is turned off. To avoid dangerous electrical shock, short both of the anode leads to the main chassis by placing the leads against the chassis for at least five minutes to fully discharge the anode.

CAUTION

The high-voltage charge on the anode lead can damage other circuits in this instrument. Be sure to fully discharge the anode lead to the main chassis, as described above.

Refer to Figure 5-15. The High-voltage module accepts the low-level AC and DC focus signals (ACFOC and DCFOCUS) from the Display Amplifiers module, amplifies, level-shifts, and sums them together to form the FOCUS signal, which sets the potential on the focus barrel in the CRT. It also receives the grid drive signal (VZ) from the Display Amplifiers module, which it level-shifts and references to the cathode potential.

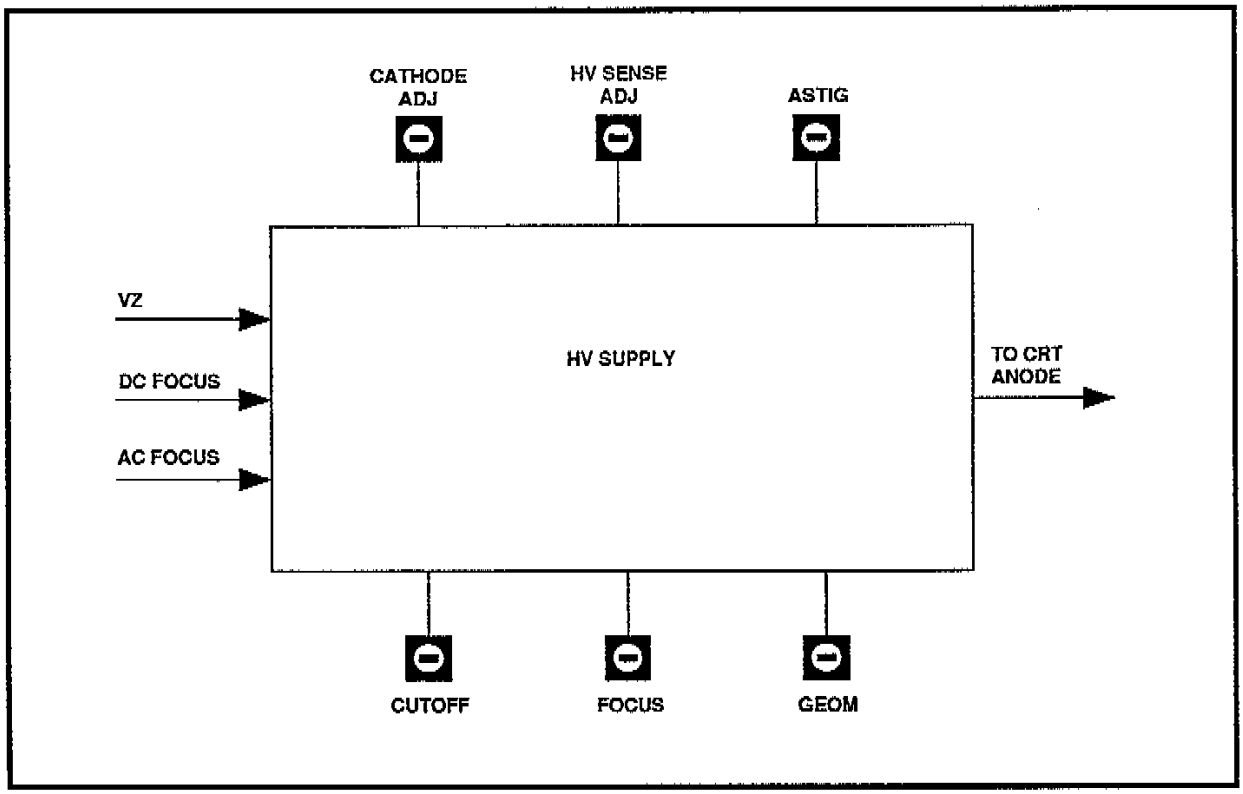


Figure 5-15. A23 High-voltage Module block diagram.

Adjustments on the module allow setting the cathode potential, over-voltage shutdown point, cut-off, focus, astigmatism, and geometry.

The secondary voltage in the supply is monitored by a circuit that shuts down the oscillator whenever the voltage level exceeds its nominal value by more than 7% to prevent excessive x-radiation emission from the CRT.

CRT AND COLOR SHUTTER

The CRT and Color Shutter provide the visual display to the user. The CRT provides the light output of the display, and the color shutter in front of the CRT provides the color information.

WARNING

Use extreme care when handling the CRT. If the CRT breaks, an implosion may result, causing glass fragments to scatter at high velocity. Wear protective clothing and safety glasses when handling the CRT. Do not allow the CRT to strike against anything that might cause it to crack or implode. When storing a CRT, place it in a protective carton if available, or set the CRT face down on a soft mat in a protected location that has a smooth surface.

The CRT is an electrostatically-deflected, post-deflection accelerated tube. The tube has a dispenser cathode, which gives the tube extremely long life even under high duty, high drive operating conditions. The tube uses a special phosphor with a spectral emission optimized for use with the "red-green" Liquid Crystal Color Shutter (LCCS).

The Color Shutter is an electrically-operated optical bandpass filter. Polarizing screens positioned between the CRT face and the filter polarize the red and green light to be 90° apart. The CRT light output passes through the Color Shutter. In the driven state, the color shutter allows transmission of the green spectral component of the phosphor, while the red component is suppressed. In the off (or semi-relaxed) state, the red spectral component of the phosphor is transmitted, while the green component is suppressed. To give the appearance of a multi-color display, the shutter is switched between its "green" and "red" transmission states with each display frame. The color of the waveforms and characters on the screen is determined by the state of the color shutter when they are drawn. A display drawn once in the "green" state and again in the "red" state appears yellow. The states are controlled by the Digital Storage Module.

FREQUENCY CONTROL

Refer to Figure 5-16. The Frequency Control section consists of six major elements:

- The Reference Oscillator produces a 100 MHz signal, which is multiplied by five to become the 500 MHz third local oscillator signal. The 100 MHz signal is also used for the calibrator signal and as a reference signal to stabilize the two local oscillators in the 2nd Converter and the 1st local oscillator via the Swept-frequency Synthesizer.
- The Sweep/Span Attenuator produces a scanning signal to drive the LO Module and the sweep signal to drive the horizontal display circuits.
- The 565 MHz Synthesizer generates a tunable signal (565 MHz ±13 MHz) that drives the LO Module for phase-locked frequency spans.
- The LO Module produces the voltages that tune the YTO and Preselector across the input frequency range, the LO low tuning signal that is used by the 565 MHz Synthesizer for phase lock operation, and the 129 MHz strobe signal for locking to the YTO.
- The Microwave Phase Lock Module locks the YTO to a harmonic of the 129 MHz strobe signal.
- The Period Counter measures signals from the Log Processor, LO Module, Reference Oscillator, and Microwave Phase Lock.

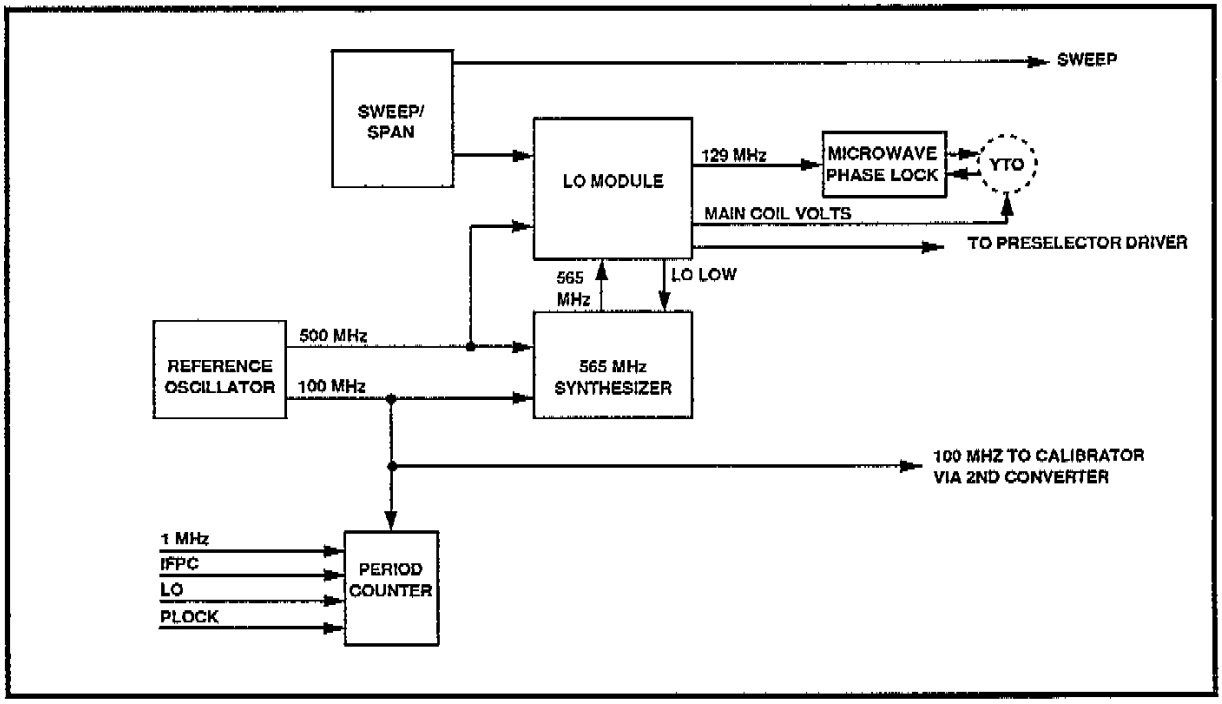


Figure 5-16. Frequency Control Section Block Diagram.

The Frequency Control section operates in three major span modes:

- Phase-lock Span, which is 2 MHz and below.
- FM Coil Span, which is from 2 MHz to 50 MHz.
- Main Coil Span, which is from 50 MHz to the maximum RF input frequency.

Figure 5-17 is a block diagram of the Frequency Control section, showing signal paths for the different span configurations. The switches are positioned for the phase-lock span operating mode.

PHASE-LOCK SPANS

This configuration is used when Phase-lock Span operation is selected; that is, the span is 2 MHz and narrower. A scaled ramp voltage from the Sweep/Span Attenuator is applied through a decade attenuator to a summing network. The other input to the network is the LO Low Tune DAC voltage. This allows Main Processor control of the LO Low frequency for calibration purposes. The voltage from the summing network is applied to the LO Low Oscillator, which has a frequency range of 10.1 to 16.1 MHz. The oscillator output is applied to the 565 MHz Synthesizer, where it controls the 565 MHz Synthesizer frequency. (In spans below 20 kHz, a decade divider reduces the signal frequency by a factor of ten.) This signal drives the LO Module, which produces the 129 MHz Strobe signal for the Microwave Phase Lock Module. A sample of the YTO output and harmonics of the 129 MHz strobe are combined in a phase gate to produce a beat note that is proportional to the phase error between the two signals. This phase error voltage drives the YTO FM Coil, tuning the YTO until the beat note is zero.

Although the Main Coil Spans path is blocked, the Center Frequency DAC allows the Main Processor to adjust the center frequency of the YTO in this configuration.

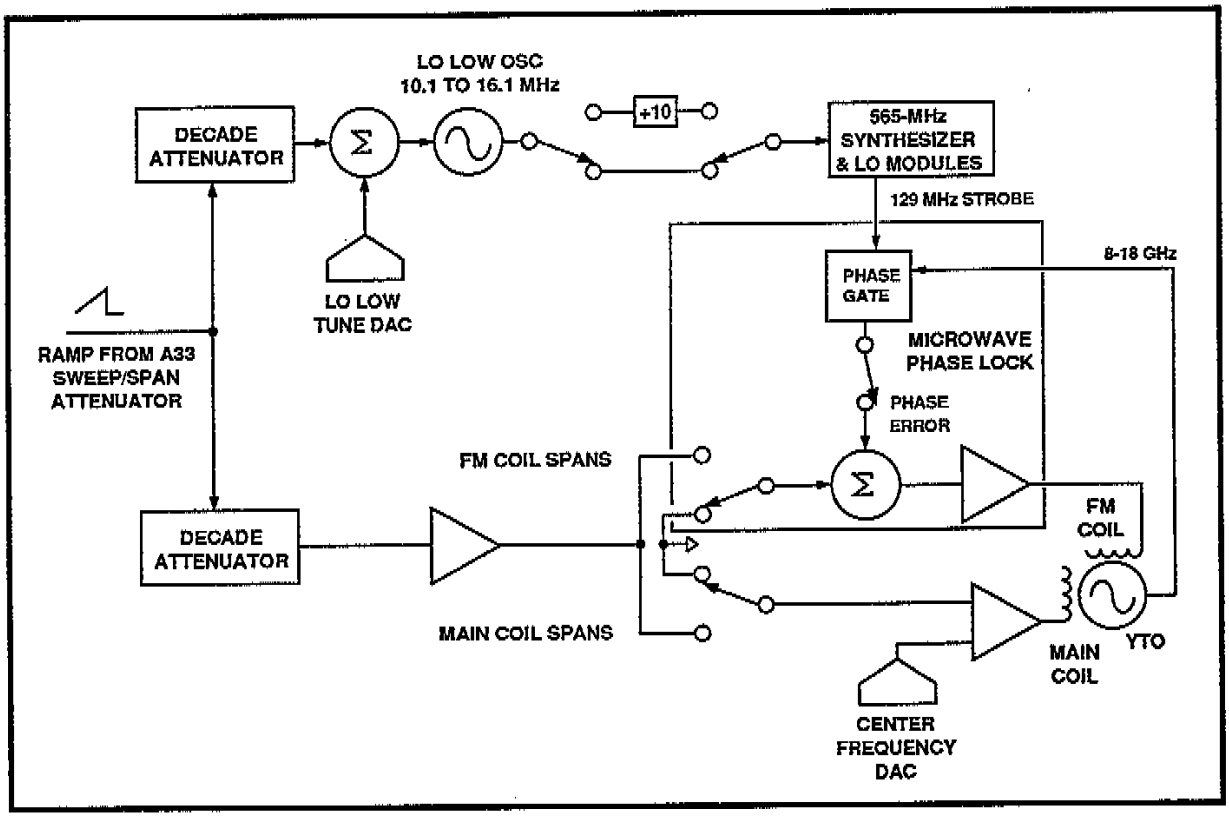


Figure 5-17. Frequency Span block diagram.

FM COIL SPANS

This configuration is selected when FM Coil Span operation is selected; that is, the span is from more than 2 MHz to 50 MHz. In this configuration, the FM Coil Spans switch in Figure 5-17 is changed to the up position, the Main Coil Spans path is blocked, and the Phase Error path is blocked.

A scaled ramp voltage from the Sweep/Span Attenuator is applied through a decade attenuator, amplified, then passed through the switch through a summing network, which is not used in this configuration. The signal is amplified to drive the FM Coil, tuning the YTO. Although the Main Coil Spans path is blocked, the Center Frequency DAC allows the Main Processor to adjust the YTO center frequency in this configuration.

MAIN COIL SPANS

This configuration is selected when Main Coil Span operation is selected; that is, the span is from more than 50 MHz to maximum frequency span. In this configuration, the Main Coil Spans path in Figure 5-17 is active, the FM Coil Spans path is blocked, and the Phase Error path is blocked.

A scaled ramp voltage from the Sweep/Span Attenuator is applied through a decade attenuator, amplified, then passed through the switch to an amplifier. The other input to the amplifier is from the Center Frequency DAC, allowing the Main Processor to adjust the center frequency. The combination of the ramp signal and center frequency offset (if any) is amplified to drive the Main Coil, tuning the YTO.

REFERENCE OSCILLATOR

The A29 Reference Oscillator provides the instrument frequency reference. An internal 100 MHz oven-compensated crystal oscillator provides an accurate and stable frequency source. A Reference Lock circuit allows locking the 100 MHz source to an external 10 MHz source. A 10 MHz output signal, derived from the 100 MHz source, can be selected in place of the external input. The X5 Multiplier produces the 500 MHz signal for application to the 3rd Converter and Frequency Control circuits. Refer to Figure 5-18.

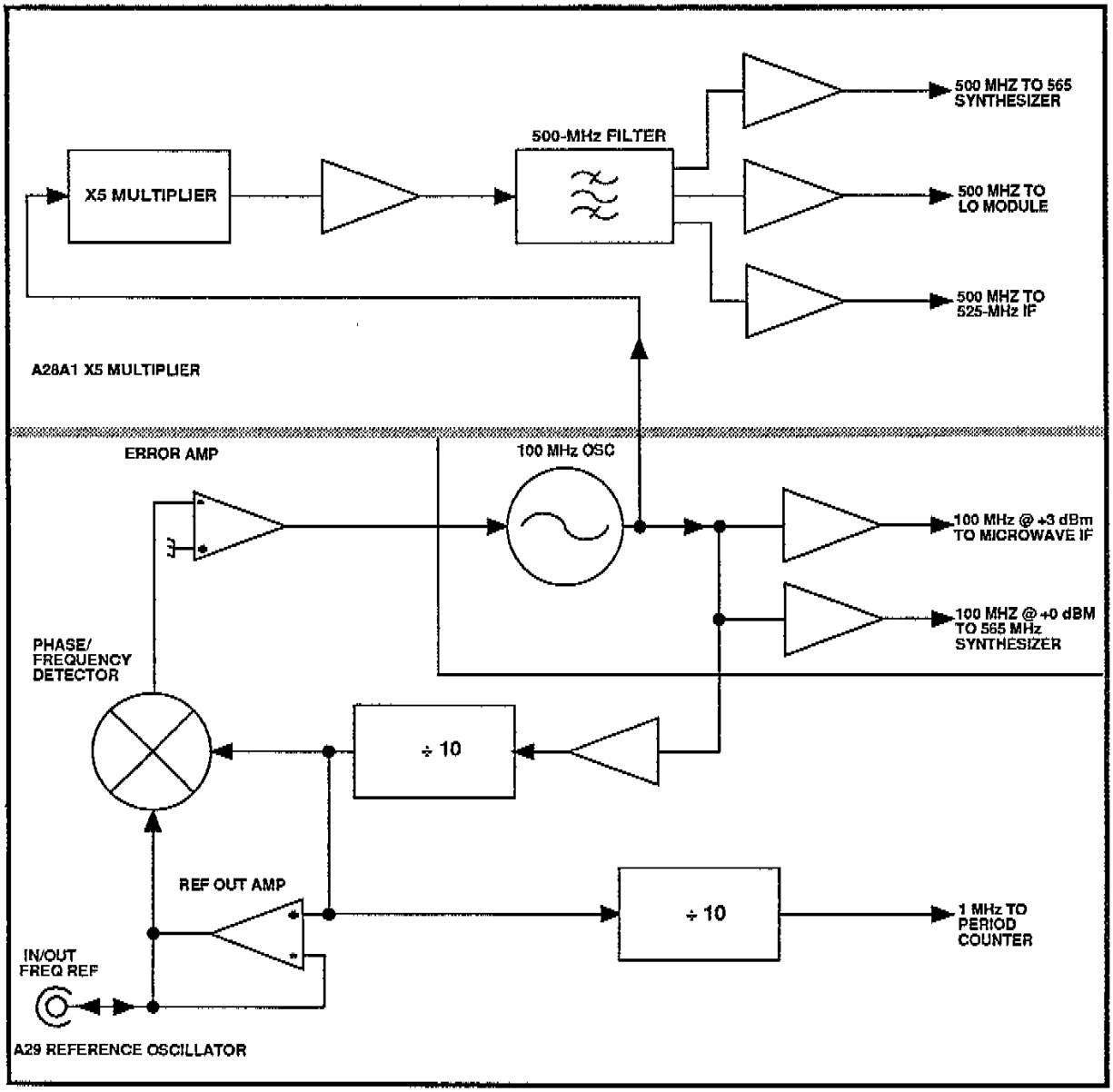


Figure 5-18. Reference Oscillator Block Diagram.

100 MHz Oscillator

The 100 MHz oscillator is powered from regulated standby voltage so that both the oscillator and the oven operate whenever the line cord is plugged in (Standby Mode) to reduce warm-up frequency error. The oscillator has a tune input that is used for fine adjustment or to phase-lock to an external reference.

The oscillator output is applied to four buffers that isolate the oscillator from the loads and the loads from one another. One buffer drives the X5 Multiplier, the second drives the 2nd Converter, the third drives the 565 MHz Synthesizer, and the fourth drives a decade divider to furnish 10 MHz to the Reference Lock circuit.

Reference Lock

The Reference Lock circuit allows locking the Reference Oscillator to an external source. It also divides the reference signal to provide a 10 MHz signal (used for internal frequency control and as a reference frequency output) and a 1 MHz signal (applied to the Period Counter).

The Reference Lock Circuit consists of two Decade Dividers, the Error Amplifier, the Phase/Frequency Detector, and the Reference Output Amplifier. A frequency configuration menu allows the operator to select an internal or external reference or to turn the output reference signal (FreqRefOut) on or off.

When the 10 MHz reference frequency output is used, the Reference Output Amp is switched into the circuit, furnishing a TTL-level 10 MHz reference signal to the rear-panel IN/OUT FREQ REF connector.

When the instrument is using an external reference to regulate oscillator frequency, the Error Amplifier is switched into the loop, allowing the Phase/Frequency Detector output (derived from the difference between the external reference signal and the divided oscillator output frequency) to control oscillator operation.

The lock circuit has a very narrow lock bandwidth, which causes the loop to take nearly 30 seconds to reach lock and stabilize. The narrow bandwidth reduces external reference phase noise and sidebands to the reference signal.

X5 Multiplier

The A28A1 X5 Multiplier module is the source of 500 MHz signals used in the instrument. Three 500 MHz signals are derived from a common 100 MHz input, which comes from the A29 Reference Oscillator through the A3 Flat-Flex Interconnect assembly.

The X5 Multiplier output passes through a buffer and is sent through a 500 MHz bandpass filter. The filter drives three output amplifier buffer stages. The first produces a +6 dBm to +9 dBm signal for the 3rd Converter, the second produces a +0 dBm to +3 dBm signal for the 565 MHz Synthesizer, and the third produces a +0 dBm to +3 dBm signal for the LO Module.

SWEEP/SPAN ATTENUATOR

The A33 Sweep/Span Attenuator processes trigger inputs from external, internal, and line-voltage sources, and produces a ramp voltage that is applied to the display through the Video Processor, to the rear-panel Accessory connector, and to the LO Module to sweep the YTO. See Figure 5-19. The Sweep/Span Attenuator consists of the Trigger Circuits, the Ramp Generator, the Marker Control, and Output Amplifiers.

Trigger Circuits

The Trigger circuits select from three sources, internal, external, or line. An eight-bit DAC furnishes the trigger level to establish the triggering point on the signal. Gate logic circuitry produces gating signals that are used for blanking and timing in other modules, and controls sweep start in the Ramp Generator.

Marker Control

A twelve-bit DAC produces a voltage that clamps the ramp voltage when the ramp voltage equals the sweep value. This stops the sweep to allow the YTO frequency to be measured at that point. This function is used in counter mode and in dB/Hz noise-measurement mode. The Marker DAC is set by the Main Processor to the horizontal address of the Marker location on the display.

Ramp Generator

The Ramp Generator is a Miller integrator that produces a 0 to ±10 volt linear ramp. Slope of the ramp is varied by selection of RC combinations for coarse changes and by an eight-bit DAC for fine changes. A clamping circuit allows stopping the ramp to measure YTO frequency at that point. The output ramp voltage is applied to the Output Amplifiers.

Output Amplifiers

The output of the Ramp Generator, SWEEP, is applied directly to the Video Processor and two buffer stages. Current can be switched in and out of one of the buffers by the Main Processor to offset the output signal, which is applied to the rear-panel Accessory connector as SWPOUT. Depending on the offset, the rear panel SWPOUT signal is –5 to +5 volts or 0 to +10 volts.

The other buffer produces the FREQSWP signal that is applied to the LO Module. A Twelve-bit DAC at the buffer input allows the Main Processor to set span values in between the decade steps by attenuating the output signal. This also permits keypad entry of non-standard values. The DAC is also used for self-correction routines.

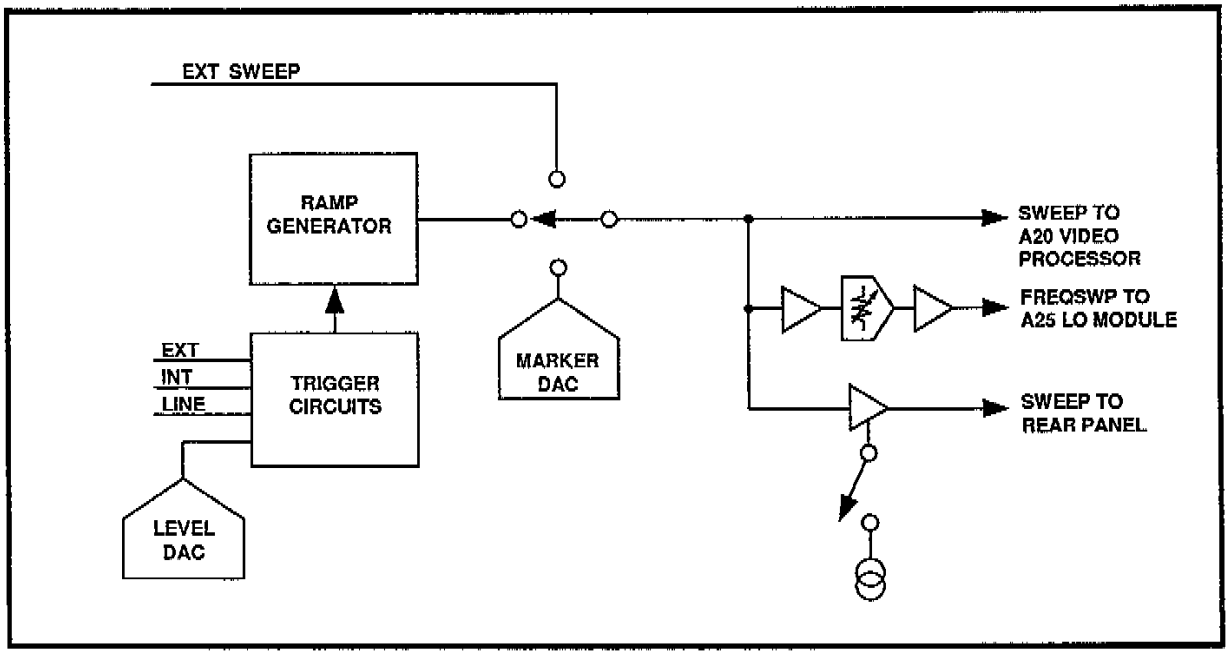


Figure 5-19. Sweep/Span Attenuator block diagram.

565 MHZ SYNTHESIZER

The A31 565 MHz Synthesizer module generates a 565 MHz control signal for the LO Module. See Figure 5-20. The module consists of the Frac N Synthesizer, the 113 MHz Synthesizer, and the 565 Phase Detector, the Mixers, and the 565 MHz Oscillator.

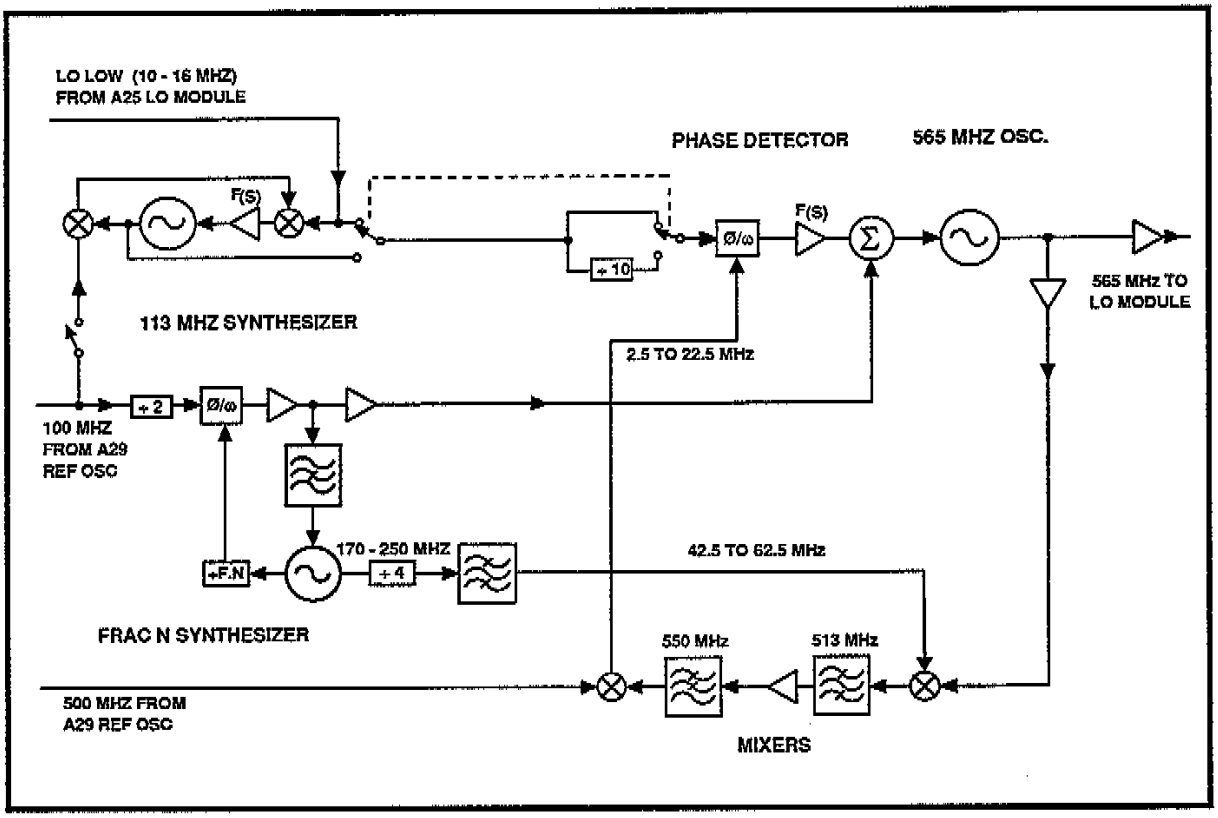


Figure 5-20. 565 Synthesizer block diagram.

Frac N Synthesizer

The Frac N Synthesizer consists of a VCO that is controlled by the Main Processor, allowing the 565 MHz Synthesizer to be tuned in 392 kHz steps. The VCO tuning range is 170 to 250 MHz.

The 100 MHz reference signal from the Reference Oscillator is applied to the Frac N Synthesizer input, where it is first divided by two. The 50 MHz divider output is then applied to a phase/frequency comparator, where the signal is used as the frequency reference for the loop. Comparison of this reference with the Frac N Synthesizer output produces an error voltage that is fed back through a band-reject filter to regulate the VCO operating frequency. The VCO output signal is applied to a Fractional Divider, which is controlled by the Main Processor. Division range is from 3 13/32 to 5.

A sample of the phase error voltage is sent to the 565 MHz VCO as a pretuning signal. The Frac N Synthesizer signal is applied to a divide-by-four stage, then sent through a bandpass filter to the Mixers.

Mixers

The Mixers consist of two mixers, two bandpass filters, and an amplifier. The 565 MHz signal from the 565 MHz VCO is fed to the first mixer, where it combines with the 42.5 to (62.5 MHz signal (nominally 52 MHz) from the Frac N Synthesizer. The output is fed through a bandpass filter that has a center frequency of 513 MHz. The signal is amplified, filtered again, then mixed with the 500 MHz reference signal from the Reference Oscillator to produce a difference frequency of 2.5 to 22.5 MHz (nominally 13 MHz). The mixer output is fed to the Phase Detector.

Phase Detector

The output of the mixers (nominally 13 MHz) is applied to the Phase Detector, where the signal is combined with the LO Low oscillator signal from the LO Module. The resulting beat note is converted to an error voltage by the F(s) amplifier and applied through a summing network to drive the 565 MHz VCO.

113 MHz Synthesizer

The 113 MHz Synthesizer is the frequency reference loop for spans narrower than 20 kHz. The circuit consists of two mixers, an F(s) amplifier, a decade divider, and the VCO.

The 10.1 to 16.1 MHz LO Low signal from the LO Module is applied to the input of the 113 MHz Synthesizer, where for spans from 20 kHz to 2 MHz, the LO Low signal is coupled directly to the Phase Detector input. When a span narrower than 20 kHz is selected, the switches close to insert the decade divider, to divert the LO Low signal to the 113 MHz Synthesizer, and to apply the 100 MHz reference to the 113 MHz Synthesizer.

The 100 MHz reference signal is combined with the 113 MHz VCO to produce a difference frequency of 13 MHz, which is applied to a mixer that combines the 13 MHz signal with the 10.1 to 16.1 MHz LO Low signal. The resulting beat note is converted into a phase error voltage that drives the oscillator frequency toward producing a zero beat note.

The oscillator output, nominally 113 MHz, is sent through a decade divider to the Phase Detector.

LO MODULE

See Figure 5-21. The A25 LO Module produces the voltages that tune the YTO and Preselector across the input frequency range, the LO Low tuning signal that is used by the 565 MHz Synthesizer for phase-lock operation, and the 129 and 141 MHz strobe that drives the Microwave Phase Lock Module. The LO Module consists of the Microwave Control, the LO Control, and the 129 MHz Synthesizer.

The sweep ramp from the Sweep/Span Attenuator is combined in a summing network with the tuning voltage from a Center-frequency DAC, then applied to the Preselector Driver and YTO Driver.

The sweep ramp from the Sweep/Span Attenuator is combined in a summing network with the LO Low Tune DAC tuning voltage and applied to the LO Low Oscillator. The tuning voltage is set by the Main Processor.

The 500 MHz reference signal from the X5 Multiplier is applied to the 500 MHz Mixer. The output of the 129 MHz Oscillator is multiplied four times (to 516 MHz), then combined with the 500 MHz signal to produce a 16 MHz difference. This signal is applied to the Harmonic Mixer, where the 26th to 48th harmonic is combined with the 565 MHz signal from the A31 565 MHz Synthesizer. The beat note is applied to an Error amplifier to produce a phase-error voltage. The voltage is combined in a summation network with the tuning voltage from the 129 MHz Tune DAC, then applied to drive the 129 MHz oscillator. When the First Local Oscillator is counted by the Main Processor rather than phase-locked, the 565 MHz signal is routed through a divide-by-four circuit to produce the 141 MHz strobe signal. This is sent through a divide by 100 circuit to the Period Counter.

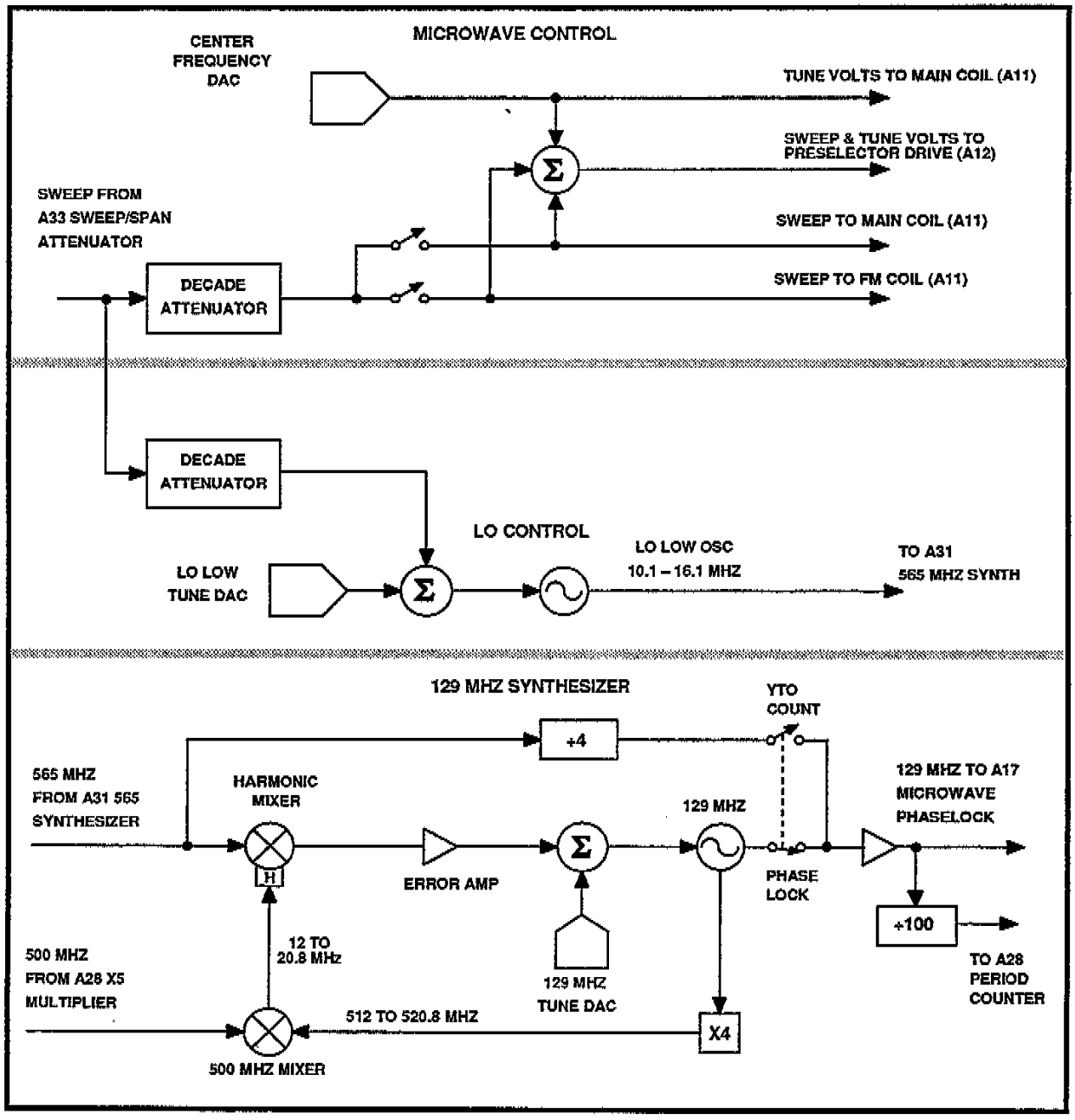


Figure 5-21. LO Module block diagram.

MICROWAVE PHASE LOCK

See Figure 5-22. The A17 Microwave Phase Lock Module generates a phase error voltage to sweep the First Local Oscillator in phase-lock spans, stabilizes the YTO FM coil in phase-lock spans (2 MHz and narrower), and generates a beat note for measuring First Local Oscillator frequency by the Period Counter. The Microwave Phase Lock consists of the Leveling Bandpass Hybrid, Phase Gate Hybrid, Strobe Driver, and F(s) Driver.

The 1st LO signal from the YTO (8-18 GHz) is fed to a PIN Attenuator and through a filter having a 12 GHz bandpass and a 13 GHz center frequency. The Detector samples a small portion of the RF signal and sends it to the Error Amplifier. The signal amplitude is controlled by the Leveling Bandpass Hybrid to improve flatness of the beat note from the Phase Gate. The Error Amplifier controls the PIN Attenuator, fixing overall gain for the section. The leveled output is applied to the Phase Gate Hybrid.

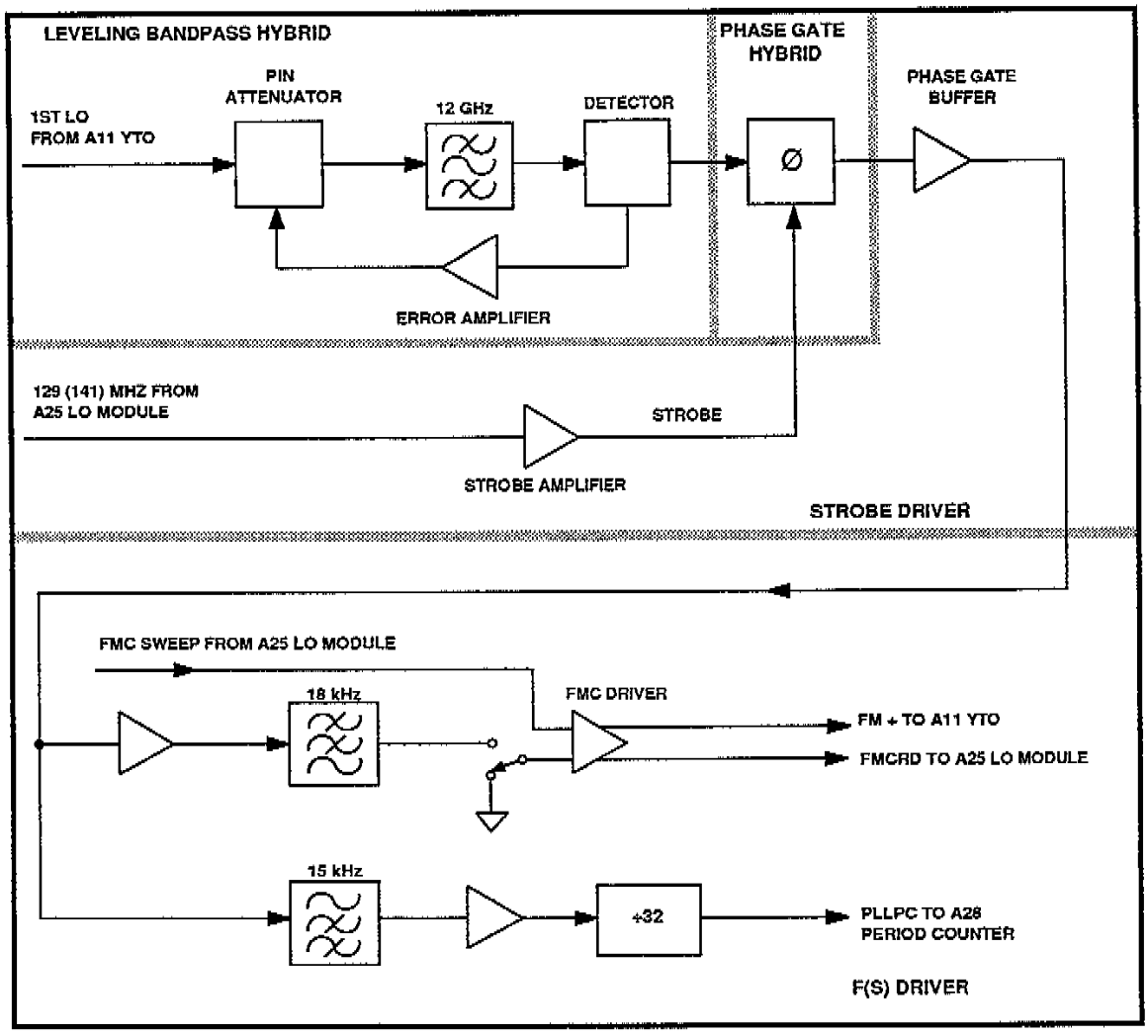


Figure 5-22. Microwave Phase Lock block diagram.

The 129 MHz Strobe from the LO Module is amplified, then applied to the Phase Gate Hybrid, where a harmonic of the strobe and the detected RF combine to produce a phase error voltage that is proportional to the frequency difference between the strobe harmonic and the incoming RF signal. The phase-error voltage is applied to the F(s) Driver.

The phase-error voltage from the Phase Gate Buffer is applied through a buffer to a low-pass filter. Half-power point of the filter is 18 kHz, but the filter response flattens at 300 kHz to counteract the effects of the overall circuit. The filtered output is applied to the FMC Driver during phase-lock operations, which combines with the FMC SWEEP signal to drive the YTO FM Coil. An attenuated version of the FM+ signal is sent as FMCRD to the LO Module to indicate when the FM Coil is tuned outside the selected frequency span.

The phase-error voltage from the Phase Gate Buffer is also applied to a high-pass filter that is nominally 15 MHz. However, in combination with the Phase Gate, the filter acts as a bandpass filter with the upper frequency cutoff at 30 MHz. The output of the filter is amplified, then divided by 32 and sent to the Period Counter. This is the signal that is counted when the Main Processor determines First Local Oscillator frequency.

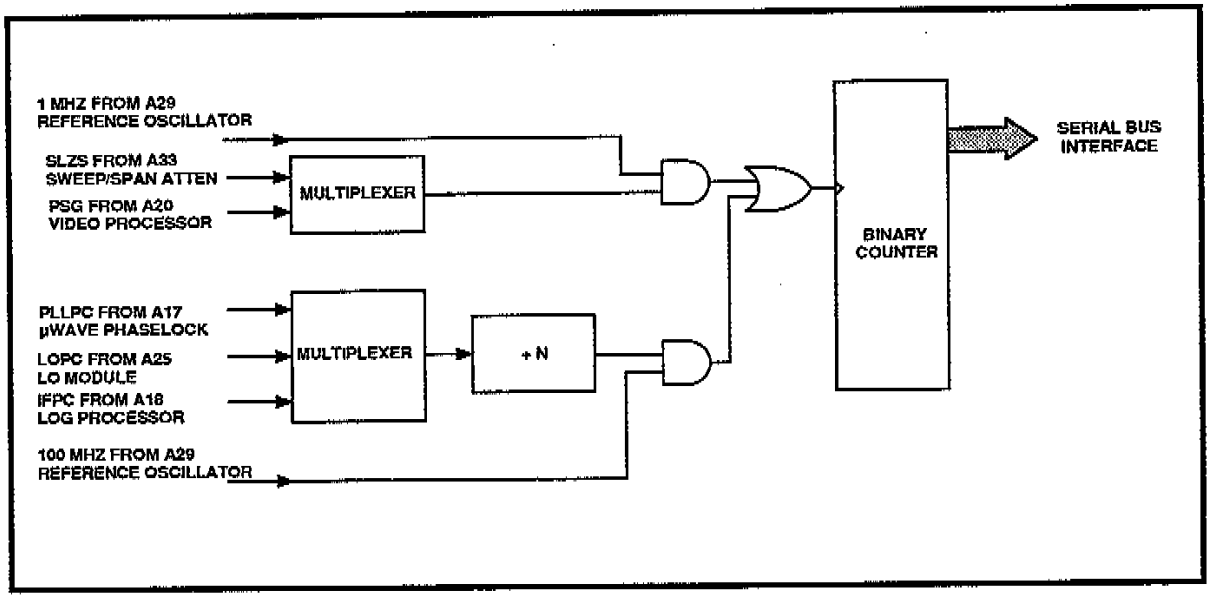


Figure 5-23. Period Counter block diagram.

Period Counter

The A28 Period Counter measures one of several signals as determined by the Main Processor. See Figure 5-23. Period Counter input signals are:

- LOPC from the LO Module, which is the LO Low signal (divided by 128), the 129 MHz strobe signal (divided by 800), or the 565 MHz signal (divided by 3200).
- PLLPC, which is the beat-frequency note from the Microwave Phase Lock Module divided by 32.
- IFPC signal, which is the signal from the Log Processor. This can be the 4 MHz IF signal (divided by 128), 25 MHz IF signal (divided by 512), or 29 MHz LO signal (divided by 512).
- 100 MHz, the reference signal from the Reference Oscillator.
- 1 MHz, the divided 100 MHz signal from the Reference Oscillator.

- PSG, the precision sweep gate from the Video Processor.
- SLZS, the sweep length zero span signal from the Sweep/Span Attenuator.

The Period Counter consists of a Source Multiplexer, ÷N Circuit, Binary Counter, Gate Multiplexer, and gating circuitry.

One of three signal sources (PLLPC, LOPC, or IFPC) is selected by the Main Processor to be applied to the ÷N circuit. The divider ratio of this circuit is set by the Main Processor for best measurement resolution. The output of the ÷N circuit is used to gate the 100 MHz signal applied to the Binary Counter, which counts the 100 MHz reference signal for the ÷N circuit output signal period.

When a sweep duration measurement is made, the SLZS or PSG signal is selected to gate the 1 MHz reference signal, and the sweep period is measured. In this measurement, the Main Processor resets the sweep, issues a count signal, then starts the sweep.

CALIBRATOR

The A15 Calibrator Module supplies a reference signal for front-panel use and for internal use in the self-correction mode of operation. See Figure 4-24.

The Calibrator receives the 100 MHz reference signal from the Reference Oscillator via the Microwave IF Module, where a +3.5 dBm sample of the reference signal is taken from the splitter.

The Calibrator produces two outputs from the same input. The first is a clean 100 MHz signal that is applied to the A12 MTX assembly, where it is used in self-correction routines. The second is the 100 MHz signal or a summation of the 100 MHz signal plus harmonics. The amplitude of this output is precisely controlled at -20 dBm. This output signal is applied to the front-panel REF SIGNAL OUT connector. Calibrator Module operation is controlled by the Main Processor, as follows:

- Calibrator power can be shut off by the Main Processor.
- The signal to the MTX can be turned off while the front-panel output remains in operation.
- The front-panel output signal is selectable to be the 100 MHz signal only or the 100 MHz signal plus harmonics.

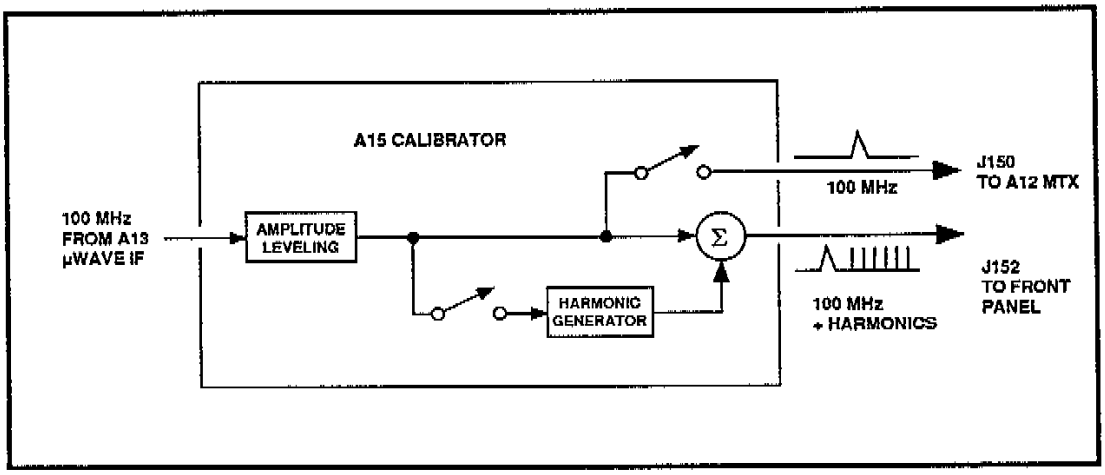


Figure 4-24. Calibrator block diagram.

DIGITAL CONTROL SYSTEM

Introduction

The Digital Control System consists of three assemblies (A41 Main Processor, A42 I/O Interface, and A43 Memory) that are connected by a local bus. This local bus is made available to the assemblies bus via a 96-pin edge connector. See Figure 5-25.

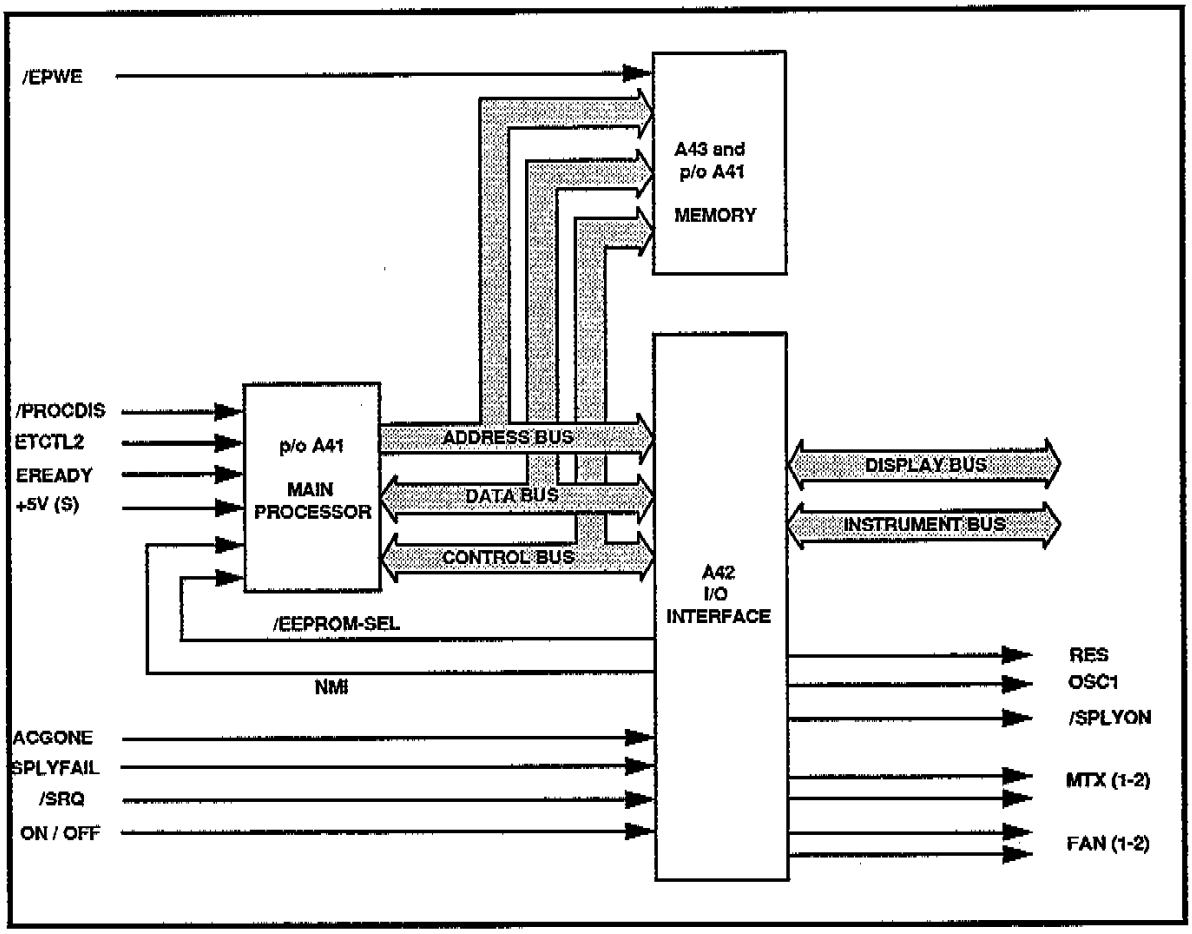


Figure 5-25. CPU System Block Diagram.

All three modules have a separate bus extension. These are isolated from the local bus for three reasons:

1. The processor buffers can be tri-stated, allowing an external programmer to write data directly into the EPROM's through the edge connector. This function is only performed at the factory).
2. To reduce the number of actual loads seen by the other modules that interface with the local bus.
3. The large memory array is protected from fault conditions that may occur on the local bus.

Several switches on the Main Processor Board are used for diagnostic purposes and to control some of the specific hardware functions. Table 5-1 lists the purpose of each switch.

Table 5-1. Control Processor Switch Descriptions.

Bank	Number	Purpose
S10	A	Enables/disables the bus self test when the Main Processor system boots.
S10	B	Enables/disables the external clock to the clock generator chip.
S10	C	Not used .
S10	D	When closed, then opened, causes the processor system to halt and reset as if a power up reset has occurred.
S11	Bit 15	Enables (closed) or disables (open) advanced diagnostics for the Processor System.
S11	Bit 8 to 14	Firmware-defined.
S12	Bit 0 to 7	Firmware-defined.

NOTE

Closing S11 bit 15 re-defines S12 and the rest of S11. See Section 4—Maintenance for information on switches and jumpers for further details.

Processor System

The Processor System consists of the following major circuits:

- Clock Generator.
- Main Processor/Math Coprocessor.
- Interrupt Controller.
- Self Test/Control Hardware.
- Timer Controller.
- DMA Controller.
- Wait State Generators.

Clock Generator. The clock generator creates the clock signal for the Processor system, either from the internal crystal oscillator or from an external signal via J10. It also synchronizes the processor ready and processor reset signals to the clock.

Switch S10B selects the clock source. An open switch selects the internal oscillator; a closed switch selects an external signal source. The external signal must be between 6 MHz and 21.1122 MHz. The clock frequency from either source is divided by three to create the processor bus clock. The clock generator outputs are the processor clock, processor ready signal, and system reset signal.

The reset signal source is the power supply control circuit. The processor can also be reset by closing and opening S10D.

Main Processor/Math Coprocessor. The Main Processor and Math Coprocessor (called the processor block) work in tandem to form the heart of the processor system. The Math Coprocessor increases the speed of math operations.

The processor block uses a common ready signal, a common clock, and a common reset signal source. (The Main Processor also uses two interrupt pins for servicing external hardware.) Non-Masked Interrupt signal NMI notifies the Main Processor if the standby supply voltage levels are below the recommended operating tolerance. The masked interrupt is driven from the interrupt controller.

The bus controller (considered part of the Processor block) generates timing signals for reading and writing data to memory or I/O locations and control signals that prevent output of timing signals during direct memory access (DMA) transfers. Output signals are synchronized with the system clock.

Interrupt Controller. The interrupt controller expands the single masked interrupt input to the Main Processor.

Self Test. In normal operation, switch S10A is open and the self-test circuit does not affect the data bus. If the switch is closed, two data bits are held low, the processor system is reset, and the Main Processor begins a loop that tests the lower address lines only. The loop continues until the switch is reopened and the processor system is reset.

Timer Controller. The timer controller has three internal 16-bit counters that can be programmed in any one of six different modes of operation. The firmware can change the mode of operation as needed to perform the necessary timing functions.

DMA Controller. The DMA (Direct Memory Access) controller transfers data between memory locations and peripheral I/O locations. The Control Transfer and Disable circuit prevents bus contention during control transfer. The DMA controller requests the use of the external bus by asserting the signal "HOLD". The DMA controller then waits until a "HOLDACK" is returned before controlling the external bus.

Wait State Generators. There are two wait state generators for the main processor system, one for the main processor controller and one for the DMA controller. This is required due to the different timing relationships between the two controllers.

Memory. The Memory resides on both the A41 Main Processor board and the A43 Memory board. The Memory and some of the local I/O on the Main Processor board share the same address and data buffers. This reduces the number of CMOS loads on the external processor bus. These data buffers and control circuits, and other gates are common to both the Memory and the local I/O locations.

Processor I/O. The local I/O for the processor is made up of the three function blocks that are part of the processor system: the DMA, Interrupt, and the Timer controllers. Each of these controllers have unique addresses for internal registers that control the various functions.

DMA programming uses the address and data buffers also used by the DMA controller. The chip select for the DMA controller is used to enable the data, address, and control buffers.

Timer programming uses the same address and data buffers as the DMA controller. The only valid address for the timer controller are on even boundaries, so the chip select is qualified with address line 0.

Interrupt programming uses the internal processor system bus, which allows the processor access to the interrupt controller when responding to an interrupt vector call. The only valid address for the interrupt controller is on even boundaries so the chip select is qualified with address line 0.

System I/O. The remaining I/O on the Main Processor Module is for diagnostics and power control, which facilitates Main Processor board testing. The diagnostic aids consist of sixteen switches and sixteen LED's. The switches and the LED's are at the same I/O location to write data to the LED's and read data from the switches. The power supply control consists of the fan speed control, MTX voltage control, Power supply on-off control, and AC power supply monitor control. Each of these functions are controlled by controlling the bits and reading the byte at the power supply control I/O location. Each function controls part of the processor control of the power supply and related functions.

FAN SPEED—The fan speed control consists of the lower two bits, 0 and 1. Changing the bit pattern changes the fan speed from off to one of three speeds.

MTX VOLTAGE CONTROL—Bits 2 and 3 are the MTX voltage control. They control the power supply +MTXV voltage supplied to the A12 MTX for Preselector control.

POWER SUPPLY ON-OFF—Bit 4 is the power supply on-off control. This allows the Main Processor to turn the power supply outputs on or off when the user presses the front panel power button.

POWER SUPPLY STATUS—There is also a status line from the power supply board that indicates when a power supply has improper voltage.

POWER SUPPLY MONITOR—The AC power supply monitor alerts the Main Processor when the AC power source is removed. If so, a non-maskable interrupt is presented to the processor system. (Switch S10D on the A41 Main Processor board tests this function. The switch, when closed and then opened, causes a power-up reset of the processor system.) The AC power supply monitor also monitors the +5 V standby voltage and resets the Main Processor after the power supply reaches 4.5 V or higher for at least 375 ms.

COMMUNICATIONS INTERFACE

The A5A6 Communications Interface is functionally part of the processor system and the I/O for the processor system. The following functions are supported by the Communications Interface:

- Processor Interface.
- GPIB Port 1 and GPIB Port 2.
- Interface Control/Status.
- External Serial Bus Interface.
- Interface Analog Input and Outputs.

This board is part of the Power Supply Module and is connected to the Mother Board by two forty-conductor cables. Refer to Diagram 3 in ***Section 7—Diagrams*** for connection details.

Processor Interface

The A5A6 Communications Interface is an extension of the A42 I/O Interface, which supplies address lines, data lines, and control lines to the Communications Interface. The data, address, and most of the control lines are isolated by buffers between the Communications Interface and the I/O Interface.

GPIB Port 1 and GPIB Port 2

The GPIB bus interface contains two transceiver chips. One is used to buffer the IEEE-488 data lines. Either push-pull outputs or open-collector outputs are automatically selected by the hardware as needed. The other chip isolates the management lines from the IEEE-488 bus.

External Serial Bus Interface

NOTE

This function is not used in the instrument; it is intended for future use. The description is included for troubleshooting purposes because circuit failure may affect the SDA and SCL lines.

The External Serial Bus interface allows the processor to control the interface as well as determining when an External Serial Bus is present. The data is bidirectional, and is controlled by the External Serial Bus.

Interface Analog Input and Outputs

The Communications Interface also routes many of the analog signals from the Mother Board to the rear panel. These signals do not control any functions on the Communications Interface, but are routed to connectors on the A5A7 Rear Panel BNC assembly.

FRONT PANEL

The A2 Front Panel Module is the interface between the user and the instrument. These circuits translate operator actions on front-panel controls into data for the Main Processor to read and implement. The circuits output data showing current operating modes to the user via LED's (light emitting diodes). See Figure 5-26. Also refer to Diagram 4 in ***Section 7—Diagrams*** for connection details.

The circuits consist of a Communications Port to interface with the rest of the instrument, a Processor System to process the data to and from the user, an LED Matrix to display data to the user, and a Key Matrix to read data from the user.

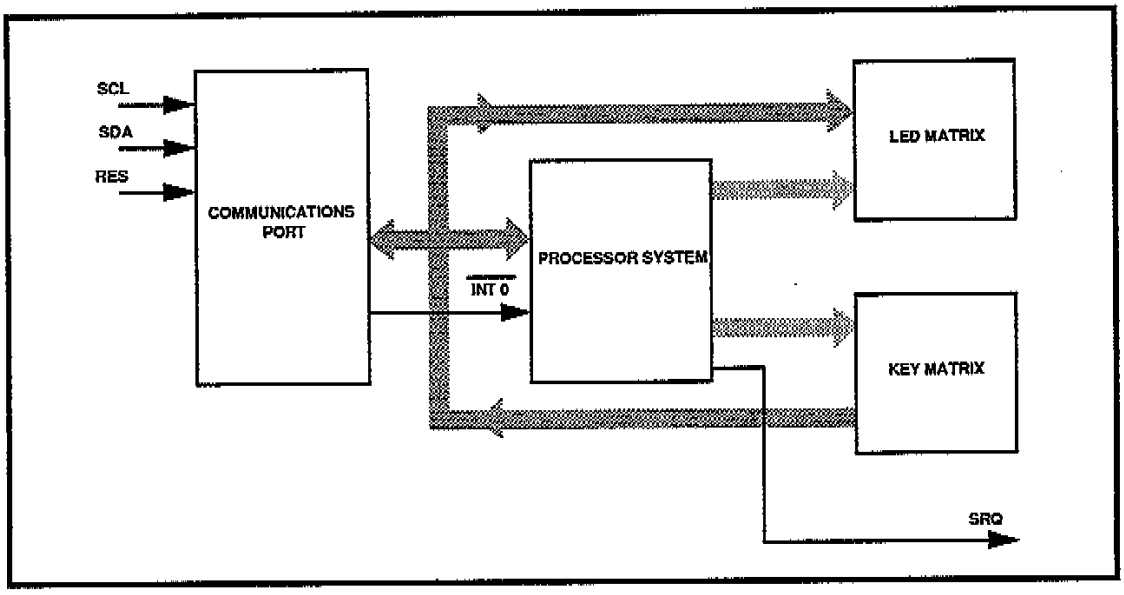


Figure 5-26. A2 Front Panel Processor Module Block Diagram.

Key Matrix

The Key Matrix reads the front panel push buttons and knobs to determine the operating conditions. The front panel keys push against switches on the board. The knobs are optical encoders that convert knob rotation into digital numbers. The FREQUENCY/MARKER knobs takes the speed of rotation into account as well.

LED Matrix

The LED Matrix lights the front panel indicators to show the selected buttons and conditions of operation.

Communications Port

The Communications Port interfaces the Front Panel circuits with the instrument serial bus. This circuit issues interrupts to the front panel processor when a key or knob requests service.

Processor System

The Processor System consists of a one-chip computer, complete with RAM and ROM on the chip. The processor provides fast implementation of the knob and button requests. The circuit also issues an SRQ (Service Request) signal as necessary to the rest of the instrument.

LOW-VOLTAGE POWER SUPPLY

The Low-voltage Power Supply provides regulated low-voltage power to the instrument. The assembly uses switching circuitry to provide high power, low ripple, and good regulation with a minimum of weight and space. The supply is contained in a metal enclosure that reduces Electromagnetic Interference (EMI). See Figure 5-27. The Low-voltage Power Supply consists of the A5FL500 EMI Filter, A5A1 Primary assembly, A5A2 Secondary assembly, A5B100 Fan, A5A6 Communications Interface assembly, and A5A7 Rear Panel BNC assembly.

NOTE

The Communications Interface is part of the Digital Control System, and is described in that part of this section.

The 125 VDC primary voltage is chopped and coupled to the secondary through two power transformers. Secondary power is rectified, filtered, and in some cases regulated. Current is delivered from the Secondary Assembly to the Mother board and distributed throughout the instrument.

EMI Filter

The EMI filter has two main purposes. First, it is a power entry module that provides voltage selection, over-current protection, and voltage surge protection. Second, it attenuates high-frequency noise generated in the instrument that otherwise would be injected onto the power bus.

Protection circuits included in the EMI filter are the input fuse, two surge protectors, and two thermistors. The surge protectors clamp input voltage to 230 V for the 110 V selection and 460 V for the 220 V selection. If the line input receives a high-energy voltage spike, the surge-protector clamps and blows the fuse. The thermistors limit current when line power is first applied.

Primary Supply

Power is delivered to the Primary Supply assembly at 110 VAC or 220 Vac . An input rectifier converts the power to approximately 300 VDC. At this point there is about 15 volts of 120 Hz ripple. A flyback regulator converts this noisy DC voltage to steady 125 VDC. There are some EMI filtering components on the primary board. This filtering prevents switching-frequency noise generated in the flyback regulator and power transformers from being injected onto the power bus.

On the Primary Assembly, a 98°C thermal fuse (A5A1F10) prevents instrument overheating. (Actual range is 94°C to 98°C.) This fuse does not reset when the temperature decreases; if it opens, it must be replaced. (See *Section 4–Maintenance* for details.)

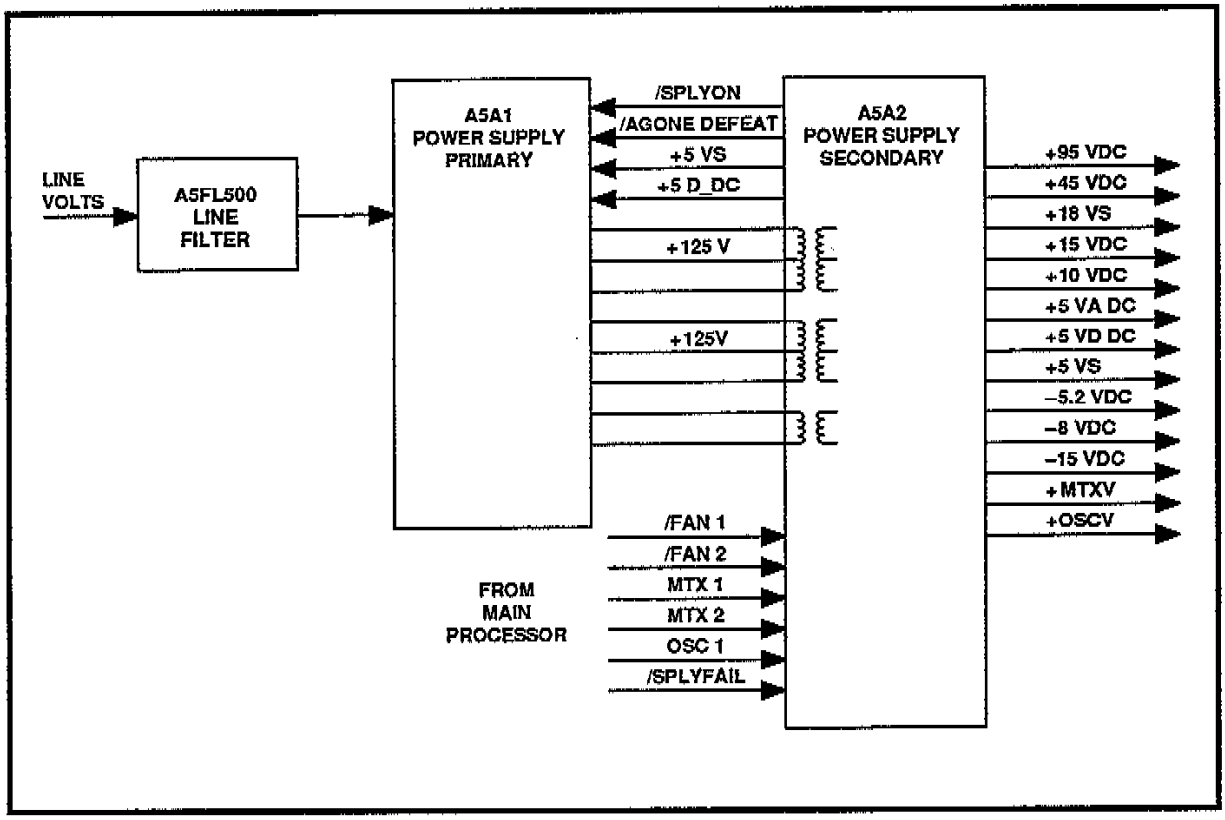


Figure 5-27. A5 Low-voltage Power Supply block diagram.

A pre-regulator provides over-current and over-voltage protection. If the output of the pre-regulator increases above 158 VDC, a pulse-width modulator circuit senses the over-voltage, sets an error latch, and turns off the FET switches. The error latch is set when the current reaches approximately 3.8 A.

Whenever the error latch is set (as a result of a fault condition), control voltage drops until the error latch resets. Input voltage then increases. If the fault condition still exists, the error latch will set again, input voltage will drop, and the error latch resets. This cycle continues until the fault is corrected or the supply is unplugged. An audible ticking at a 4 to 10 Hz rate can be heard when supply is cycling in the fault mode.

To protect against short-circuit output conditions on unregulated power supplies, current-sensing resistors sense the main and auxiliary push-pull power return current and trigger the protection cycle just described if a short-circuit occurs.

Secondary Supply

The secondary has seven regulated outputs, two switchable unregulated outputs (not including the fan voltage), and four other unregulated outputs. All seven regulators use high-gain amplifiers with pass transistors and current foldback to protect against short-circuits. Each supply uses one or two low-pass pi filters to reduce high-frequency noise. Most of the outputs to the Mother Board are decoupled at the Mother Board connector to further reduce noise on the outputs.

The +5 VS reference is the main reference voltage for the Secondary Supply. Six other reference voltages are derived from this reference using voltage dividers. The ground for each references is sensed at the Mother board to avoid the voltage drop that would occur between the Mother Board ground and the power supply ground. The reference circuit operates in standby mode to allow the main power supplies to turn on quickly (typically 20 to 40 milliseconds).

Auxiliary Supplies

When line voltage is applied to the Low-voltage Supply, the Auxiliary Supply converter begins to operate. Eleven rectifier pairs are powered by the Auxiliary Supply: one pair for the fan, three for +MTXV, two for +OSCV, one for +18 VS, one for –18 VS (used internally), and three for +5 VS. All of these rectifiers drive highly-capacitive filters as well as loads.

The fan has its own rectifier to help keep noise from other outputs. Since the fan motor can be a major noise source, the fan voltage is also decoupled. The fan speed is controlled by the Main Processor through the /FAN1 and /FAN2 lines. Switches on the Power Supply Module allow control of fan speed when the Main Processor is disabled. See ***Section 4–Maintenance*** for details.

Table 5-2. Fan Control Logic.

/FAN1	/FAN2	FAN SPEED
0 (Low)	0 (low)	High
0 (low)	1 (high)	Medium
1 (high)	0 (low)	Low
1 (high)	1 (high)	Off

Two supplies have switchable output voltages: +MTXV and +OSCV. The +MTXV signal drives the preselector. The +MTXV output is set by decoding MTX1 and MTX2 from the Main Processor. Table 5-3 lists the input line state vs. the output voltage.

Table 5-3. MTXV Control Logic.

MTX2	MTX1	+MTXV
0 (Low)	0 (low)	0V
0 (low)	1 (high)	18V
1 (high)	0 (low)	26V
1 (high)	1 (high)	32V

The +OSCV is switched between 18 VDC and 26 VDC under the direction of the Main Processor. Table 5-4 lists the input line state vs. the output voltage.

Table 5-4. OSCV Control Logic.

OSC1	OSCV
0 (Low)	18V
1 (high)	26V

+18 VS and –18 VS are two unregulated un-switchable auxiliary supplies. +18 VS is used internally on the Secondary Supply and to power a heater for the Reference Oscillator oven. The –18 VS is used only as an internal power source for the Secondary Supply.

The +5 VS supply powers the Main Processor system as well as the Communications Interface. A shunt regulator provides over-voltage protection to protect these sensitive loads. When +5 VS increases above +5.5 V, the shunt regulator latches and sends a signal to the Primary assembly through the RESET opto-coupler to reduce the pre-regulator duty cycle and output voltage.

Main Supply

The Main Supply has three unregulated outputs and six regulated outputs. The +5D (+5 V digital) has a separate current return to prevent digital noise from being induced into other supplies. The +5D supply is kept from exceeding approximately 10 A by sensing the voltage drop across filter inductors. The +5D supply also has over-voltage protection using the same type of circuit described above for the +5 VS supply.

The regulated supplies (+15 V, +10 V, +5 VA, –5.2 V, –8 V, and –15 V) are all controlled in a manner similar to that for the +5 VS supply. The +5 VA and –5.2 V output voltages are sensed at the mother board to keep a low tolerance on these supplies. The +95 V and +45 V supplies are low-current unregulated supplies used in display circuits.

If line power shuts off, the /ACGONE DEFEAT line switches low and signals the Main Processor that the instrument lost line power. The Main Processor then turns off the main supply and completes all shut-down routines before auxiliary power collapses.

The combined output of all the regulated supplies (and the +95 V and +45 V unregulated supplies) is sensed by the supply fail circuit. A current sum circuit senses the combined voltage. Thus, if one supply exceeds limits, the /SPLYFAIL line goes low and the green LED (DS10) on the Secondary assembly turns off.

Protection Circuits

Several protection circuits are included on the Secondary assembly. These are the +5 VS and +5 VD over-voltage circuits, and the +5 VD over-current circuit.

When one of the protection circuits detects out-of-tolerance conditions, the supply begins to shut down. The supply does not shut down entirely, but the +125 V pre-regulator amplitude will reduce substantially. Oscillation between low-output and fault states can occur with these fault conditions and is noticeable by an audible whine or buzz. (It is easily seen on an oscilloscope by probing the +5D output.)

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

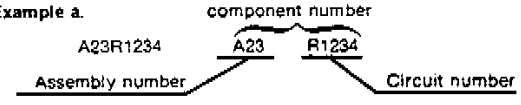
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

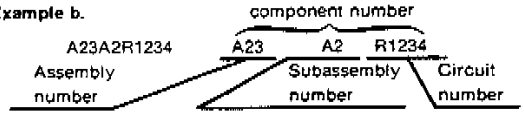
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00681	MINE SAFETY APPLIANCE CO CATALYST RESEARCH DIV	1421 CLARKVIEW RD	BALTIMORE MD 21209-2103
09772	WEST COAST LOCKWASHER CO INC	16730 E JOHNSON DRIVE P O BOX 3588	CITY OF INDUSTRY CA 91744
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125-4632
14482	WATKINS-JOHNSON CO	3333 HILLVIEW AVE	PALO ALTO CA 94304-1204
18565	CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801-1039
27012	MICRO DEVICES CORP SUB OF EMERSON ELECTRIC CO	1320 S MAIN ST PO BOX 3538	MANSFIELD OH 44907-2516
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
72228	AMCA INTERNATIONAL CORP CONTINENTAL SCREW CO DIV	459 MT PLEASANT	NEW BEDFORD MA 02742
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
77900	ILLINOIS TOOL WORKS SHAKEPROOF DIV	ST CHARLES RD	ELGIN IL 60120
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
83385	MICRODOT MFG INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
TK0435	LEWIS SCREW CO	4300 S RACINE AVE	CHICAGO IL 60609-3320
TK0858	STAUFFER SUPPLY CO (DIST)		
TK1302	MOUNTAIN MOLDING	606 SECOND STREET	BERTHOUD CO 80513
TK1312	LEMO USA INC	335 TESCONI CIR PO BOX 11006	SANTA ROSA CA 95406
TK1375	ESAM		
TK1543	CAMCAR/TEXTRON	600 18TH AVE	ROCKFORD IL 61108-5181

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A1	670-9439-01			CIRCUIT BD ASSY:MOTHER	80009	670-9439-01
A2A1	670-9466-01			CIRCUIT BD ASSY:FRONT PANEL #1	80009	670-9466-01
A2A2	670-9465-01			CIRCUIT BD ASSY:FRONT PANEL #2	80009	670-9465-01
A3	012-1283-00			CABLE ASSEMBLY:FLAT FLEX COAX	80009	012-1283-00
A4	119-2939-00			COLOR SHUTTER A:RED/GREEN 5 INCH DIAGONAL	80009	119-2939-00
A5	621-0038-04	B020000	B020293	PWR SPLY ASSY:	80009	621-0038-04
A5	621-0038-05	B020294	B020385	POWER SUPPLY:	80009	621-0038-05
A5	621-0038-06	B020386	B020437	POWER SUPPLY:	80009	621-0038-06
A5	621-0038-07	B020438		POWER SUPPLY: (2782 ONLY)	80009	621-0038-07
A5	621-0038-06	B010100	B010118	POWER SUPPLY:	80009	621-0038-06
A5	621-0038-07	B010119		POWER SUPPLY: (2784 ONLY)	80009	621-0038-07
A5B100	119-2222-03			FAN,TUBEAXIAL:24V,2.6W,3450RPM,36CFM,BRUSHLESS W/CONNECTORS	80009	119-2222-03
A5FL500	119-3127-01			FILTER ASSEMBLY:EMI,ENCAPSULATED	80009	119-3127-01
A5W516	174-0372-00			CABLE ASSY,RF:50 OHM COAX,8.5 L	80009	174-0372-00
A5A1	670-9450-02	B020000	B020293	CIRCUIT BD ASSY:POWER SUPPLY PRIMARY	80009	670-9450-02
A5A1	670-9450-03	B020294		CIRCUIT BD ASSY:POWER SUPPLY PRIMARY (2782 ONLY)	80009	670-9450-03
A5A1	670-9450-03			CIRCUIT BD ASSY:POWER SUPPLY PRIMARY (2784 ONLY)	80009	670-9450-03
A5A1F10	159-0321-00			FUSE,TERMINAL:15A,98DRG C MAX OPENING TEMP	27012	4204A1
A5A2	670-9451-02	B020000	B020437	CIRCUIT BD ASSY:POWER SUPPLY SECONDARY	80009	670-9451-02
A5A2	670-9451-03	B020438		CIRCUIT BD ASSY:POWER SUPPLY SECONDARY (2782 ONLY)	80009	670-9451-03
A5A2	670-9451-02	B010100	B010118	CIRCUIT BD ASSY:POWER SUPPLY SECONDARY	80009	670-9451-02
A5A2	670-9451-03	B010119		CIRCUIT BD ASSY:POWER SUPPLY SECONDARY (2784 ONLY)	80009	670-9451-03
A5A6	671-0082-02	B020000	B020385	CIRCUIT BD ASSY:COMMUNICATIONS INTERFACE	80009	671-0082-02
A5A6	671-0082-03	B020386		CIRCUIT BD ASSY:COMMUNICATIONS INTERFACE (2782 ONLY)	80009	671-0082-03
A5A6	671-0082-03			CIRCUIT BD ASSY:COMMUNICATIONS INTERFACE (2784 ONLY)	80009	671-0082-03
A5A7	670-9495-01			CIRCUIT BD ASSY:REAR PANEL BNC	80009	670-9495-01
A10	119-2675-01	B020000	B020413	ATTENUATOR:33GHZ-70DB	80009	119-2675-01
A10	119-4248-00	B020412		ATTENUATOR:40GHZ-70DB (2782 ONLY)	80009	119-4248-00
A10	119-4248-00			ATTENUATOR:40GHZ-70DB (2784 ONLY)	80009	119-4248-00
A11	119-2496-02	B020000	B020329	YIG OSC ASSY:8-18GHZ	80009	119-2496-02
A11	119-2496-03	B020330		YIG OSC ASSY:8-18GHZ (2782 ONLY)	80009	119-2496-03
A11	119-2496-03			YIG OSC ASSY:8-18GHZ (2784 ONLY)	80009	119-2496-03
A11A2	671-0242-03			CIRCUIT BD ASSY:YTO DRIVER	80009	671-0242-03
A12	119-2743-04	B020000	B020387	CONVERTER ASSY:MAGNETICALLY TUNED	80009	119-2743-04
A12	119-2743-06	B020388	B020413	CONVERTER ASSY:MAGNETICALLY TUNED	80009	119-2743-06
A12	119-4249-00	B020414		MIX CONV ASSY:40GHZ-70DB,MAGNETICALLY TUNED (2782 ONLY)	80009	119-4249-00
A12	119-4249-00			MIX CONV ASSY:40GHZ-70DB,MAGNETICALLY TUNED (2784 ONLY)	80009	119-4249-00
A12A4	119-2742-00			TERMINATOR ASSY:LOW PASS	80009	119-2742-00
A12A5	119-2876-00			MIXER,LOW PASS:CONVERTS IF SIGNAL OF 20 HZ TO 6.5 GHZ TO RF FREQ OF	14482	M52DC-1
A12FL2	119-2942-00			FILTER:LOW PASS	80009	119-2942-00
A13	119-2887-04	B020000	B020421	MWIF ASSEMBLY:MICROWAVE IF	80009	119-2887-04
A13	119-2887-05	B020422		MWIF ASSEMBLY:MICROWAVE I/F (2782 ONLY)	80009	119-2887-05
A13	119-2887-04	B010100	B010126	MWIF ASSEMBLY:MICROWAVE IF	80009	119-2887-04
A13	119-2887-05	B010127		MWIF ASSEMBLY:MICROWAVE I/F (2784 ONLY)	80009	119-2887-05

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14	119-2285-02	B020000	B020367	INTMD FREQ ASSY:525 IF MODULE	80009	119-2285-02
A14	119-2285-03	B020368	B020461	INTMD FREQ ASSY:525 FF MODULE	80009	119-2285-03
A14	119-2285-04	B020462		INTMD FREQ ASSY:525 FF MODULE (2782 ONLY)	80009	119-2285-04
A14	119-2285-03	B010100	B010129	INTMD FREQ ASSY:525 FF MODULE	80009	119-2285-03
A14	119-2285-04	B010130		INTMD FREQ ASSY:525 FF MODULE (2784 ONLY)	80009	119-2285-04
A15	119-3072-00	B020000	B020330	CALIBRATOR ASSY:	80009	119-3072-00
A15	119-3072-01	B020331		CALIBRATOR ASSY: (2782 ONLY)	80009	119-3072-01
A15	119-3072-01			CALIBRATOR ASSY: (2784 ONLY)	80009	119-3072-01
A15A3	119-3676-00			ISOLATOR,RF:WIDE BAND,8-18GHZ	80009	119-3676-00
A16	644-0631-08	B020000	B020242	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-08
A16	644-0631-09	B020243	B020245	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-09
A16	644-0631-10	B020246	B020250	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-10
A16	644-0631-11	B020251	B020255	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-11
A16	644-0631-12	B020256	B020270	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-12
A16	644-0631-13	B020271	B020285	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-13
A16	644-0631-14	B020286	B020403	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-14
A16	644-0631-15	B020404	B020461	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-15
A16	644-0631-16	B020462		VR ASSEMBLY:VARIABLE RESOLUTION (2782 ONLY)	80009	644-0631-16
A16	644-0631-15	B010100	B010129	VR ASSEMBLY:VARIABLE RESOLUTION	80009	644-0631-15
A16	644-0631-16	B010130		VR ASSEMBLY:VARIABLE RESOLUTION (2784 ONLY)	80009	644-0631-16
A17	119-2938-03	B020000	B020386	PHASELOCK ASSY:MICROWAVE	80009	119-2938-03
A17	119-2938-04	B020387	B020421	PHASE LOCK ASSY:MICROWAVE	80009	119-2938-04
A17	119-2938-05	B020422		PHASE LOCK ASSY:MICROWAVE (2782 ONLY)	80009	119-2938-05
A17	119-2938-04	B010100	B010126	PHASE LOCK ASSY:MICROWAVE	80009	119-2938-04
A17	119-2938-05	B010127		PHASE LOCK ASSY:MICROWAVE (2784 ONLY)	80009	119-2938-05
A18	670-9438-08	B020000	B020315	CIRCUIT BD ASSY:LOG PROCESSOR	80009	670-9438-08
A18	670-9438-09	B020316	B020330	CIRCUIT BD ASSY:LOG PROCESSOR	80009	670-9438-09
A18	670-9438-10	B020331	B020465	CIRCUIT BD ASSY:LOG PROCESSOR	80009	670-9438-10
A18	670-9438-11	B020466		CIRCUIT BD ASSY:LOG PROCESSOR (2782 ONLY)	80009	670-9438-11
A18	670-9438-10	B010100	B010130	CIRCUIT BD ASSY:LOG PROCESSOR	80009	670-9438-10
A18	670-9438-11	B010131		CIRCUIT BD ASSY:LOG PROCESSOR (2784 ONLY)	80009	670-9438-11
A19	119-4386-00			MODULE:25MHZ IF (OPTION 04 ONLY)	80009	119-4386-00
A20	672-0257-03	B020000	B020281	CIRCUIT BD ASSY:DIGITAL/VIDEO PROCESSOR	80009	672-0257-03
A20	672-0257-04	B020282	B020304	CIRCUIT BD ASSY:DIG/VIDEO PROCESSOR	80009	672-0257-04
A20	672-0257-05	B020305	B020410	CIRCUIT BD ASSY:DIG/VIDEO PROCESSOR	80009	672-0257-05
A20	672-0257-06	B020411		CIRCUIT BD ASSY:DIG/VIDEO PROCESSOR (2782 ONLY)	80009	672-0257-06
A20	672-0257-06			CIRCUIT BD ASSY:DIG/VIDEO PROCESSOR (2784 ONLY)	80009	672-0257-06
A22	670-9448-03	B020000	B020468	CIRCUIT BD ASSY:DISPLAY AMP	80009	670-9448-03
A22	670-9448-04	B020469		CIRCUIT BD ASSY:DISPLAY AMP (2782 ONLY)	80009	670-9448-04
A22	670-9448-03	B010100	B010131	CIRCUIT BD ASSY:DISPLAY AMP	80009	670-9448-03
A22	670-9448-04	B010132		CIRCUIT BD ASSY:DISPLAY AMP (2784 ONLY)	80009	670-9448-04
A23	670-9449-02	B020000	B020457	CIRCUIT BD ASSY:HIGH VOLTAGE	80009	670-9449-02
A23	670-9449-03	B020458		CIRCUIT BD ASSY:HIGH VOLTAGE (2782 ONLY)	80009	670-9449-03
A23	670-9449-02	B010100	B010127	CIRCUIT BD ASSY:HIGH VOLTAGE	80009	670-9449-02
A23	670-9449-03	B010128		CIRCUIT BD ASSY:HIGH VOLTAGE (2784 ONLY)	80009	670-9449-03

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A24	670-9447-02	B020000	B020388	CIRCUIT BD ASSY:DIGITAL STORAGE	80009	670-9447-02
A24	670-9447-03	B020389		CIRCUIT BD ASSY:DIGITAL STORAGE (2782 ONLY)	80009	670-9447-03
A24	670-9447-03			CIRCUIT BD ASSY:DIGITAL STORAGE (2784 ONLY)	80009	670-9447-03
A24U11	160-5825-01	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5825-01
A24U11	160-5825-02	B020210	B020403	MIROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27C 1024,DIP40	80009	160-5825-02
A24U11	160-5825-04	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5825-04
A24U11	160-5825-04			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5825-04
A25	672-1269-05	B020000	B020244	CIRCUIT BD ASSY:LO CONTROL	80009	672-1269-05
A25	672-1269-07	B020245	B020313	CIRCUIT BD ASSY:LO CONTROL	80009	672-1269-07
A25	672-1269-08	B020314	B020414	CIRCUIT BD ASSY:LO CONTROL	80009	672-1269-08
A25	672-1269-09	B020415	B020470	CIRCUIT BD ASSY:L.O. CONTROL	80009	672-1269-09
A25	672-1269-10	B020471		CIRCUIT BD ASSY:L.O. CONTROL (2782 ONLY)	80009	672-1269-10
A25	672-1269-09	B010100	B010131	CIRCUIT BD ASSY:L.O. CONTROL	80009	672-1269-09
A25	672-1269-10	B010132		CIRCUIT BD ASSY:L.O. CONTROL (2784 ONLY)	80009	672-1269-10
A28	672-0195-05			CIRCUIT BD ASSY:PERIOD COUNTER	80009	672-0195-05
A29	670-9461-07	B020000	B020327	CIRCUIT BD ASSY:REF OSC	80009	670-9461-07
A29	670-9461-08	B020328	B020403	CIRCUIT BD ASSY:REF OSC	80009	670-9461-08
A29	670-9461-09	B020404		CIRCUIT BD ASSY:REFERENCE (2782 ONLY)	80009	670-9461-09
A29	670-9461-09			CIRCUIT BD ASSY:REFERENCE (2784 ONLY)	80009	670-9461-09
A31	672-0190-04			CIRCUIT BD ASSY:PHASE LOCK	80009	672-0190-04
A33	670-9459-01	B020000	B020311	CIRCUIT BD ASSY:SWEEP/SPAN ATTEN	80009	670-9459-01
A33	670-9459-02	B020312		CIRCUIT BD ASSY:SWEEP/SPAN ATTEN (2782 ONLY)	80009	670-9459-02
A33	670-9459-02			CIRCUIT BD ASSY:SWEEP/SPAN ATTEN (2784 ONLY)	80009	670-9459-02
A41	670-9463-01	B020000	B020416	CIRCUIT BD ASSY:MAIN PROCESSOR	80009	670-9463-01
A41	670-9463-02	B020417	B020424	CIRCUIT BD ASSY:MAIN PROCESSOR	80009	670-9463-02
A41	670-9463-03	B020425		CIRCUIT BD ASSY:MAIN PROCESSOR (2782 ONLY)	80009	670-9463-03
A41	670-9463-02	B010100	B010130	CIRCUIT BD ASSY:MAIN PROCESSOR	80009	670-9463-02
A41	670-9463-03	B010118		CIRCUIT BD ASSY:MAIN PROCESSOR (2784 ONLY)	80009	670-9463-03
A41U63	160-5824-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5824-03
A41U63	160-5824-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5824-04
A41U63	160-5824-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5824-06
A41U63	160-5824-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5824-06
A41U63	160-7465-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6 (2782 & 2784 OPTION 16 ONLY)	80009	160-7465-04
A42	670-9464-01	B020000	B020438	CIRCUIT BD ASSY:I/O INTERFACE	80009	670-9464-01
A42	670-9464-02	B020439		CIRCUIT BD ASSY:I/O INTERFACE (2782 ONLY)	80009	670-9464-02
A42	670-9464-01	B010100	B010123	CIRCUIT BD ASSY:I/O INTERFACE	80009	670-9464-01
A42	670-9464-02	B010124		CIRCUIT BD ASSY:I/O INTERFACE	80009	670-9464-02

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(2784 ONLY)		
A42BT10	146-0044-00			BATTERY,DRY:3V,0.17AH @ 0.85MA,BUTTON CELL, LITHIUM-MANGANESE DIOXIDE	00681	ORDER BY DESCR
A42BT11	146-0044-00			BATTERY,DRY:3V,0.17AH @ 0.85MA,BUTTON CELL, LITHIUM-MANGANESE DIOXIDE	00681	ORDER BY DESCR
A42U40	160-5826-00	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM	80009	160-5826-00
A42U40	160-5826-01	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5826-01
A42U40	160-5826-03	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5826-03
A42U40	160-5826-03			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5826-03
A42U40	160-8501-03			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6,OPT 16 (2782 & 2784 OPTION 16 ONLY)	80009	160-8501-03
A43	670-9462-00	B020000	B020457	CIRCUIT BD ASSY:ROM	80009	670-9462-00
A43	670-9462-01	B020458		CIRCUIT BD ASSY:ROM (2782 ONLY)	80009	670-9462-01
A43	670-9462-00	B010100	B010127	CIRCUIT BD ASSY:ROM	80009	670-9462-00
A43	670-9462-01	B010128		CIRCUIT BD ASSY:ROM (2784 ONLY)	80009	670-9462-01
A43U10	160-5823-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5823-03
A43U10	160-5823-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5823-04
A43U10	160-5823-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5823-06
A43U10	160-5823-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5823-06
A43U10	160-7460-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6,OPT 16 (2782 & 2784 OPTION 16 ONLY)	80009	160-7460-04
A43U11	160-5819-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5819-03
A43U11	160-5819-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5819-04
A43U11	160-5819-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5819-06
A43U11	160-5819-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5819-06
A43U11	160-7461-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6 (2782 & 2784 OPTION 16 ONLY)	80009	160-7461-04
A43U12	160-5820-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5820-03
A43U12	160-5820-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5820-04
A43U12	160-5820-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5820-06
A43U12	160-5820-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5820-06
A43U12	160-7462-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6 (2782 & 2784 OPTION 16 ONLY)	80009	160-7462-04

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A43U13	160-5821-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5821-03
A43U13	160-5821-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5821-04
A43U13	160-5821-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5821-06
A43U13	160-5821-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5821-06
A43U13	160-7463-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6 (2782 & 2784 OPTION 16 ONLY)	80009	160-7463-04
A43U14	160-5822-03	B020000	B020209	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,27C1024 ,DIP40	80009	160-5822-03
A43U14	160-5822-04	B020210	B020403	MICROCKT,DGTL:CMOS,65536 X 16 EPROM,PRGM,27 C1024,DIP40	80009	160-5822-04
A43U14	160-5822-06	B020404		IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2782 ONLY)	80009	160-5822-06
A43U14	160-5822-06			IC,DIGITAL:CMOS,65536 X 16,EPROM,PRGM,27C10 24,DIP40,VER2.6 (2784 ONLY)	80009	160-5822-06
A43U14	160-7464-04			IC,DIGITAL:CMOS,EPROM;65536 X 16 PRGM,156-3 566-00,27C1024,DIP40.6 (2782 & 2784 OPTION 16 ONLY)	80009	160-7464-04
F10	159-0319-00			FUSE,CARTRIDGE:4A,125V,5.2 X 20MM,FAST BLOW	71400	GMA-4A
F10	159-0320-00			FUSE,CARTRIDGE:4A,250V,FAST (OPTIONS A1, A2, A3, A4, A5 ONLY)	80009	159-0320-00
FL100	119-4023-00			FILTER:LOW PASS,12.4GHZ	80009	119-4023-00
L10	108-1335-00			COIL,TUBE DEFL:FXD,TRACE ROTATOR	80009	108-1335-00
P16	015-0567-00			TERMN,COAXIAL:50 OHM 0.5W DC TO 18.0GHZ	34078	2444MC-032
P18	015-0567-00			TERMN,COAXIAL:50 OHM 0.5W DC TO 18.0GHZ	34078	2444MC-032
V100	154-0891-00			ELECTRON TUBE:T6630,CRT FINISHED	80009	154-0891-00
W100	174-1112-01			CABLE ASSY,RF:50 OHM COAX,SEMI RIGID	80009	174-1112-01
W112	174-0355-00			CABLE ASSY,RF:SEMIRIGID,50 OHM COAX	80009	174-0355-00
W114	174-1863-00			CABLE ASSY,RF:50 OHM SEMI RIGID	80009	174-1863-00
W140	174-0380-00			CABLE ASSY,RF:50 OHM COAX,17.0 L	80009	174-0380-00
W150	174-0357-00			CABLE ASSY,RF:50 OHM COAX,7.25 L	80009	174-0357-00
W152	174-0373-00			CABLE ASSY,RF:50 OHM COAX,5.0 L	80009	174-0373-00
W154	174-1864-00			CABLE ASSY,RF:50 OHM SEMI RIGID	80009	174-1864-00
W162	174-0361-00			CABLE ASSY,RF:50 OHM COAX,5.5 L	80009	174-0361-00
W166	174-0361-00			CABLE ASSY,RF:50 OHM COAX,5.5 L	80009	174-0361-00
W250	174-0374-00	B020100	B020407	CABLE ASSY,RF:50 OHM COAX,17.5 L	80009	174-0374-00
W250	174-0376-00	B020408		CABLE ASSY,RF:50 OHM COAX,17.5 L (2782 ONLY)	80009	174-0376-00
W250	174-0376-00			CABLE ASSY,RF:50 OHM COAX,17.5 L (2784 ONLY)	80009	174-0376-00
W280	174-0375-00			CABLE ASSY,RF:50 OHM COAX,8.75 L	80009	174-0375-00
W292	174-0376-00			CABLE ASSY,RF:50 OHM COAX,17.5 L	80009	174-0376-00
W1220	174-1057-00			CABLE ASSY,RF:50 OHM COAX,2.18 L	80009	174-1057-00
W1232	174-1059-00			CABLE ASSY,RF:50 OHM COAX,2.48 L	80009	174-1059-00
W1235	174-0354-00			CABLE ASSY,RF:SEMIRIGID,50 OHM COAX,6.428 L	80009	174-0354-00
W1270	174-0377-00			CA ASSY,SP,ELEC:10,26 AWG,4.0 L,RIBBON	80009	174-0377-00
W1320	174-0356-00	B020000	B020461	CABLE ASSY,RF:SEMIRIGID,50 OHM COAX	80009	174-0356-00
W1320	174-0356-01	B020462		CABLE ASSY,RF:SEMIRIGID,50 OHM COAX (2782 ONLY)	80009	174-0356-01
W1320	174-0356-00	B010100	B010129	CABLE ASSY,RF:SEMIRIGID,50 OHM COAX	80009	174-0356-00
W1320	174-0356-01	B010130		CABLE ASSY,RF:SEMIRIGID,50 OHM COAX (2784 ONLY)	80009	174-0356-01

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
W1334	174-0378-00			CABLE ASSY,RF:50 OHM COAX,5.5 L	80009	174-0378-00

DIAGRAMS

INTRODUCTION

This section consists of the following:

- Mother board signal titles, including source and destination. See Table 7-1.
- Overall Block Diagram.
- Layout diagrams to locate connectors and individual connections on the Mother Board.
- Intermodule interconnection diagrams.

STANDARDS

With the exception of the symbols in Fig. 7-1, graphic symbols and class designation letters comply with ANSI Standard Y32.2–1975.

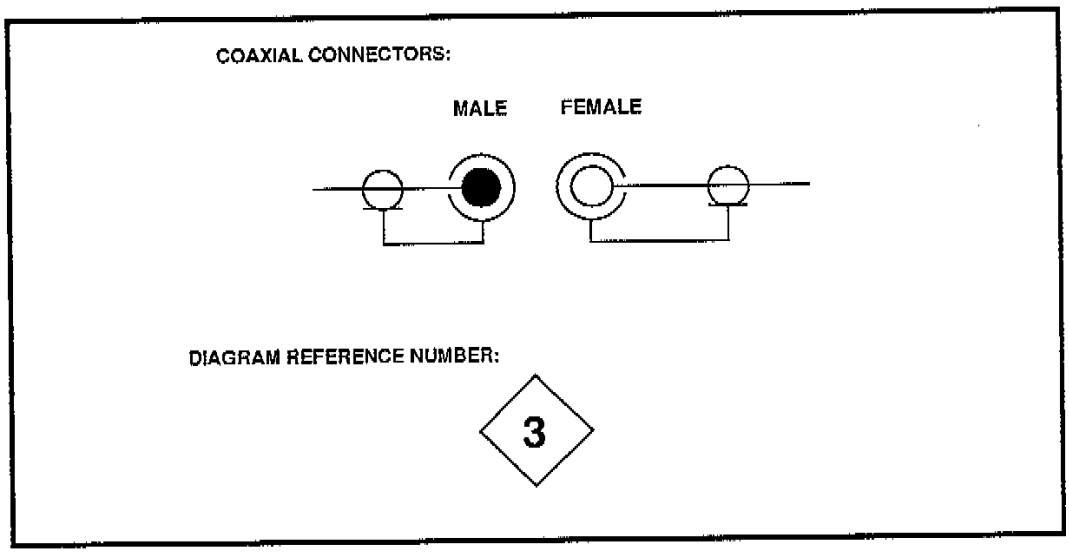


Figure 7–1. Graphic Symbols.

Other ANSI standards used in this section are:

Y1.1–1972	Abbreviations.
Y10.5–1975	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.
Y14.2–1973	Line Conventions and Lettering.
Y14.15–1966	Drafting Practices.

ASSEMBLY NUMBERING

Each replaceable assembly is assigned an assembly number. Refer to the Replaceable Electrical Parts List for ordering information.

Table 7-1
Conductor Definitions

Title	Definition	Source	Destination
+10V	+10V supply	LV POWER SUPPLY (J22: A12, B12)	1ST LO (P502: B5) 565 SYNTHESIZER (J15: A16, B16) CALIBRATOR (P508: B3) DIGITAL STORAGE (J19: A16, B16) DISPLAY AMPLIFIER (J20: A16, B16) HIGH VOLTAGE (J21: A16, B16) LO MODULE (J16: A16, B16) LOG PROCESSOR (J17: A16, B16) MICROWAVE IF (P501: B1) MTX CONTROL (P504: A10, B10) PERIOD COUNTER (J14: A16, B16) PRESELECTOR DRIVER (P505: A5) REFERENCE OSCILLATOR (J12: A16, B16) SPARE (J11: A16, B16) SWEEP/SPAN ATTEN (J13: A16, B16) VIDEO PROCESSOR (J18: A16, B1
+10VREF	+10-volt reference	SWEEP/SPAN ATTEN (P13: B27)	565 SYNTHESIZER (J15: B27) CALIBRATOR (P508: B5) DIGITAL STORAGE (J19: B27) DISPLAY AMPLIFIER (J20: B27) HIGH VOLTAGE (J21: B27) LO MODULE (J16: B27) LOG PROCESSOR (J17: B27) MICROWAVE IF (P501: B9) MTX CONTROL (P504: A10, A5) PERIOD COUNTER (J14: B27) REFERENCE OSCILLATOR (J12: B27) SPARE (J11: B27) VIDEO PROCESSOR (J18: B27) VR ASSEMBLY (P507: A1)
+10VRRET	+10V reference return	SWEEP/SPAN ATTEN (P13: A27)	565 SYNTHESIZER (J15: A27) CALIBRATOR (P508: A5) DIGITAL STORAGE (J19: A27) DISPLAY AMPLIFIER (J20: A27) HIGH VOLTAGE (J21: A27) LO MODULE (J16: A27) LOG PROCESSOR (J17: A27) MICROWAVE IF (P501: B10) MTX CONTROL (P504: B5) PERIOD COUNTER (J14: A27) REFERENCE OSCILLATOR (J12: A27) SPARE (J11: A27) VIDEO PROCESSOR (J18: A27) VR ASSEMBLY (P507: A3)

Table 7-1 continued

Title	Definition	Source	Destination
+15V	+15V supply.	LV POWER SUPPLY (J22: A10, A11, B11)	1ST LO (P502: A4) 525 IF (P506: B3) 565 SYNTHESIZER (J15: A26, B26) CALIBRATOR (P508: A5) DIGITAL STORAGE (J19: A26, B26) DISPLAY AMPLIFIER (J20: A26, B26) FRONT PANEL (P10: A7) HIGH VOLTAGE (J21: A26, B26) LO MODULE (J16: A26, B26) LOG PROCESSOR (J17: A26, B26) MICROWAVE IF (P501: B10) MICROWAVE PHASE-LOCK (P500: B6) MTX CONTROL (P504: B5) PERIOD COUNTER (J14: A26, B26) PRESELECTOR DRIVER (P505: A4) REFERENCE OSCILLATOR (J12: A26, B26) SPARE (J11: A26, B26) SWEEP/SPAN ATTENUATOR (J13: A26, B26) UNUSED (P503: B3) VIDEO PROCESSOR (J18: A26, B26) VR ASSEMBLY (P507: A3)
+18VS	+18V standby supply.	LV POWER SUPPLY (J22:A21)	REFERENCE OSCILLATOR (J12: B21)
+45V	+45V supply.	LV POWER SUPPLY (J22:B21)	565 SYNTHESIZER (J15: A15, B15) DIGITAL STORAGE (J19: A15, B15) DISPLAY AMPLIFIER (J20: A15, B15) HIGH VOLTAGE (J21: A15, B15) LO MODULE (J16: A15, B15) LOG PROCESSOR (J17: A15, B15) PERIOD COUNTER (J14: A15, B15) REFERENCE OSCILLATOR (J12: A15, B15) SPARE (J11: A15, B15) SWEEP/SPAN ATTEN (J13: A15, B15) VIDEO PROCESSOR (J18: A15, B15)
+5VA	+5V analog supply.	LV POWER SUPPLY (J22: A15, B15)	1ST LO (P502: A3) 565 SYNTHESIZER (J15: A28, B28) CALIBRATOR (P508: B6) DIGITAL STORAGE (J19: A28, B28) DISPLAY AMPLIFIER (J20: A28, B28) HIGH VOLTAGE (J21: A28, B28) LO MODULE (J16: A28, B28) LOG PROCESSOR (J17: A28, B28) MICROWAVE IF (P501: B5) MICROWAVE PHASE-LOCK (P500: A4) MTX CONTROL (P504: A4,B4) PERIOD COUNTER (J14: A28, B28) PRESELECTOR DRIVER (P505: A3) REFERENCE OSCILLATOR (J12: A28, B28) SPARE (J11: A28, B28) SWEEP/SPAN ATTEN (J13: A28, B28) UNUSED (P503: A7) VIDEO PROCESSOR (J18: A28, B28) VR ASSEMBLY (P507: B2)

Table 7-1 continued

Title	Definition	Source	Destination
+5VAsens	+5V analog supply sense line.	LV POWER SUPPLY (J22: B16)	HIGH VOLTAGE (J21: A20)
+5VD	+5V digital supply.	LV POWER SUPPLY (J22: A22, A23, A24, A25)	1ST LO (P502: A1) 565 SYNTHESIZER (J15: A32, B32) CALIBRATOR (P508: B10) DIGITAL STORAGE (J19: A32, B32) DISPLAY AMPLIFIER (J20: A32, B32) FRONT PANEL (P10: A1) HIGH VOLTAGE (J21: A32, B32) I/O INTERFACE 1 (P27: C32) LO MODULE (J16: A32, B32) LOG PROCESSOR (J17: A32, B32) MAIN PROCESSOR (P26: C32) MICROWAVE IF (P501: A1) MICROWAVE PHASE-LOCK (P500: B1) MTX CONTROL (P504: B1) PERIOD COUNTER (J14: A32, B32) PRESELECTOR DRIVER (P505: A1) MEMORY (J28: C32) REFERENCE OSCILLATOR (J12: A32, B32) SPARE (J11: A32, B32) SWEEP/SPAN ATTEN (J13: A32, B32) VIDEO PROCESSOR (J18: A32, B32)
+5VS	+5V standby supply.	LV POWER SUPPLY (J22: B1, B2, B3, B4)	COMM INTERFACE 2 (J24: 35, 36) COMM INTERFACE 1 (J23: 17, 18, 19) FRONT PANEL (J10: B5) I/O INTERFACE 1 (P27: A32, B32, C10) MAIN PROCESSOR (P26: A32, B32, C10) MEMORY (J28: A32, B32, C10)
+95V	+95V supply.	LV POWER SUPPLY (J22: B9)	DISPLAY AMPLIFIER (J20: A1) HIGH VOLTAGE (J21: A1)
-15V	-15V supply	A5 LV POWER SUPPLY (J22: A16)	1ST LO (P502: A8) 565 SYNTHESIZER (J15: A23, B23) CALIBRATOR (P508: A4) DIGITAL STORAGE (J19: A23, B23) DISPLAY AMPLIFIER (J20: A23, B23) FRONT PANEL (J10: A6) HIGH VOLTAGE (J21: A23, B23) I/O INTERFACE 1 (P27: C32) LO MODULE (J16: A23, B23) LOG PROCESSOR (J17: A23, B23) MAIN PROCESSOR (P26: C32) MICROWAVE IF (P501: A8,B8) MICROWAVE PHASE-LOCK (P500: A6) MTX CONTROL (P504: A7) NOT USED (P503: B7) PERIOD COUNTER (J14: A23, B23) PRESELECTOR DRIVER (P505: B5) MEMORY (J28: C32) REFERENCE OSCILLATOR (J12: A23, B23) SPARE (J11: A23, B23) SWEEP/SPAN ATTEN (J13: A23, B23) VIDEO PROCESSOR (J18: A23, B23) VR ASSEMBLY (P507: B7)

Table 7-1 continued

Title	Definition	Source	Destination
-5.2sens	-5.2V supply sense line	LV POWER SUPPLY (J22: B13)	HIGH VOLTAGE (J21: A20)
-5.2V	-5.2V supply	LV POWER SUPPLY (J22: A14,B14)	1ST LO (P502: B4) 565 SYNTHESIZER (J15: A20, B20) CALIBRATOR (P508: A3) DIGITAL STORAGE (J19: A20, B20) DISPLAY AMPLIFIER (J20: A20, B20) FRONT PANEL (J10: B6) HIGH VOLTAGE (J21: A20, B20) LO MODULE (J16: A20, B20) LOG PROCESSOR (J17: A20, B20) MICROWAVE IF (P501: A9) MICROWAVE PHASE-LOCK (P500: A3) MTX CONTROL (P504: B7) PERIOD COUNTER (J14: A20, B20) PRESELECTOR DRIVER (P505: B4) REFERENCE OSCILLATOR (J12: A20, B20) SPARE (J11: A20, B20) SWEEP/SPAN ATTEN (J13: A20, B20) VIDEO PROCESSOR (J18: A20, B20)
-8V	-8V supply	LV POWER SUPPLY (J22: A19, B19)	1ST LO (P502: B8) 565 SYNTHESIZER (J15: A4, B4) CALIBRATOR (P508: A2) DIGITAL STORAGE (J19: A4, B4) DISPLAY AMPLIFIER (J20: A4, B4) FRONT PANEL (J10: A5) HIGH VOLTAGE (J21: A4, B4) LO MODULE (J16: A4, B4) LOG PROCESSOR (J17: A4, B4) MICROWAVE IF (P501: A10) NOT USED (P503: B5) PERIOD COUNTER (J14: A4, B4) PRESELECTOR DRIVER (P505: B3) REFERENCE OSCILLATOR (J12: A4, B4) SPARE (J11: A4, B4) SWEEP/SPAN ATTEN (J13: A4, B4) VIDEO PROCESSOR (J18: A4, B4) VR ASSEMBLY (P507: B6)
1 MHZ	(TTL) 1/100th of the 100-MHz reference frequency (sent to the Period Counter).	REFERENCE OSCILLATOR (J12: B1)	PERIOD COUNTER (J14: B1)
ACFOC	The portion of total focus signal that keeps display focused despite sudden intensity changes.	DISPLAY AMPLIFIER (J20: B12)	HIGH VOLTAGE (J22: B12)
ACFOCRET	Return for ACFOC.	DISPLAY AMPLIFIER (J20: B11)	HIGH VOLTAGE (J22: B11)
/ACGONE	Control line that signals imminent power loss due to ac line voltage failure.	I/O INTERFACE 1 (P27: C30)	MAIN PROCESSOR (P26: C30) LV POWER SUPPLY (J22: A8) MEMORY (J28: C30)

Table 7-1 continued

Title	Definition	Source	Destination
ACQCLK	(TTL) A 9.216-MHz internal clock from the Digital Storage board that is divided down in the Video Processor and used to run the digitizer.	DIGITAL STORAGE (J19: B9)	VIDEO PROCESSOR (J18: B9)
/ATEST	(TTL) This signal disables the memory and ROM during processor self-test.	I/O INTERFACE 1 (J27: B12)	MEMORY (J28: B12) MAIN PROCESSOR (J26: B12)
/BDDIR	(TTL) Buffered Data DIRection signal that indicates comm. interface data flow direction. HIGH => from the comm. interface, and LOW => to the comm. interface.	I/O INTERFACE 2 (J25: A7)	COMM INTERFACE 1 (J23: 39)
/BDMAAK1	(TTL) Buffered DMA Acknowledge signal from processor to peripheral (GPIB0) that allows the peripheral to proceed with the programmed operation.	I/O INTERFACE 2 (J25: B2)	COMM INTERFACE 1 (J23: 4)
/BDMAAK2	(TTL) Buffered DMA Acknowledge signal from processor to peripheral (GPIB1) that allows the peripheral to proceed with the programmed operation.	I/O INTERFACE 2 (J25: A2)	COMM INTERFACE 1 (J23: 5)
/BEIORD	(TTL) Buffered External IO ReaD signal to the COMM interface (active LOW).	I/O INTERFACE 2 (J25: A8)	COMM INTERFACE 1 (J23: 38)
/BEIOWR	(TTL) Buffered External IO WRite signal to the COMM interface (active LOW).	I/O INTERFACE 2 (J25: B8)	COMM INTERFACE 1 (J23: 37)
BLA1	(TTL) Buffered Latched Address 1.	I/O INTERFACE 2 (J25: B5)	COMM INTERFACE 1 (J23: 11)
BLA2	(TTL) Buffered Latched Address 2.	I/O INTERFACE 2 (J25: A5)	COMM INTERFACE 1 (J23: 12)
BLA3	(TTL) Buffered Latched Address 3.	I/O INTERFACE 2 (J25: B6)	COMM INTERFACE 1 (J23: 13)
BLA4	(TTL) Buffered Latched Address 4.	I/O INTERFACE 2 (J25: A6)	COMM INTERFACE 1 (J23: 14)
BLA5	(TTL) Buffered Latched Address 5.	I/O INTERFACE 2 (J25: B7)	COMM INTERFACE 1 (J23: 15)

Table 7-1 continued

Title	Definition	Source	Destination
BOD	(TTL) Beginning Of Display handshaking signal between Digital Storage and Display Amplifier Module. Signal is pulsed high to indicate that a color change has just occurred.	DIGITAL STORAGE (J19: B2)	DISPLAY AMPLIFIER (J20: B2)
BPD0	(TTL) Buffered processor data bit 1 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: B9)	COMM INTERFACE 1 (J23: 21)
BPD1	(TTL) Buffered processor data bit 2 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: A9)	COMM INTERFACE 1 (J23: 23)
BPD2	(TTL) Buffered processor data bit 3 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: B10)	COMM INTERFACE 1 (J23: 25)
BPD3	(TTL) Buffered processor data bit 4 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: A10)	COMM INTERFACE 1 (J23: 27)
BPD4	(TTL) Buffered processor data bit 5 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: B11)	COMM INTERFACE 1 (J23: 29)
BPD5	(TTL) Buffered processor data bit 6 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: A11)	COMM INTERFACE 1 (J23: 31)
BPD6	(TTL) Buffered processor data bit 7 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: B12)	COMM INTERFACE 1 (J23: 33)
BPD7	(TTL) Buffered processor data bit 8 of 8-bit data bus (LSB).	I/O INTERFACE 2 (J25: A12)	COMM INTERFACE 1 (J23: 35)
/CLAMP	(TTL) Causes video processor to clamp display to baseline when sweep is outside scan range. (Active LOW.)	LOG PROCESSOR (J17: B7)	VIDEO PROCESSOR (J18: B7)
COLOR+	Color shutter drive signal (approx. 40V, 2-kHz square wave).	DISPLAY AMPLIFIER (J20: A25)	FRONT PANEL (J10: A4)
COLOR-	Return for COLOR+.	DISPLAY AMPLIFIER (J20: A24)	FRONT PANEL (J10: B4)
/COMSEL	(TTL) Communications interface select signal (Active LOW). When active, the I/O devices on the communications interface are selected and can transfer data to/from the main processor.	I/O INTERFACE 2 (J25: A4)	COMM INTERFACE 1 (J23: 9)
D0	(TTL) Bit 1 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C12)	I/O INTERFACE 1 (J27: C12) MEMORY (J28: C12)
D1	(TTL) Bit 2 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: A13)	I/O INTERFACE 1 (J27: A13) MEMORY (J28: A13)

Table 7-1 continued

Title	Definition	Source	Destination
D2	(TTL) Bit 3 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: B13)	I/O INTERFACE 1 (J27: B13) MEMORY (J28: B13)
D3	(TTL) Bit 4 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C13)	I/O INTERFACE 1 (J27: C13) MEMORY (J28: C13)
D4	(TTL) Bit 5 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: A14)	I/O INTERFACE 1 (J27: A14) MEMORY (J28: A14)
D5	(TTL) Bit 6 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: B14)	I/O INTERFACE 1 (J27: B14) MEMORY (J28: B14)
D6	(TTL) Bit 7 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C14)	I/O INTERFACE 1 (J27: C14) MEMORY (J28: C14)
D7	(TTL) Bit 8 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: A15)	I/O INTERFACE 1 (J27: A15) MEMORY (J28: A15)
D8	(TTL) Bit 9 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: B15)	I/O INTERFACE 1 (J27: B15) MEMORY (J28: B15)
D9	(TTL) Bit 10 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C15)	I/O INTERFACE 1 (J27: C15) MEMORY (J28: C15)
D10	(TTL) Bit 11 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: A16)	I/O INTERFACE 1 (J27: A16) MEMORY (J28: A16)
D11	(TTL) Bit 12 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: B16)	I/O INTERFACE 1 (J27: B16) MEMORY (J28: B16)
D12	(TTL) Bit 13 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C16)	I/O INTERFACE 1 (J27: C16) MEMORY (J28: C16)
D13	(TTL) Bit 14 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: A17)	I/O INTERFACE 1 (J27: A17) MEMORY (J28: A17)
D14	(TTL) Bit 15 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: B17)	I/O INTERFACE 1 (J27: B17) MEMORY (J28: B17)
D15	(TTL) Bit 16 of the 16-bit processor data bus.	MAIN PROCESSOR (J26: C17)	I/O INTERFACE 1 (J27: C17) MEMORY (J28: C17)
DCFOC	DC portion of the focus signal sent to the High-voltage Power Supply.	DISPLAY AMPLIFIER (J20:A22)	HIGH VOLTAGE (J22: A22)
DCFOCRET	Return for DCFOC	DISPLAY AMPLIFIER (J20: B22)	HIGH VOLTAGE (J22: B22)
DIGBLANK	(TTL) Digital Storage blanking signal (HIGH ==> blank).	DIGITAL STORAGE (J19: A10)	DISPLAY AMPLIFIER (J20: A10)

Table 7-1 continued

Title	Definition	Source	Destination
DIGCLK	(TTL) A 4.608-MHz internal clock generated on the Digital Storage board that runs the acquisition system and the display sequencer.	DIGITAL STORAGE (J19: A9)	DISPLAY AMPLIFIER (J20: A9) LOG PROCESSOR (J17: A9) VIDEO PROCESSOR (J18: A9)
DIGCOLOR	(TTL) Controls display color (HIGH ==> green, LOW ==> red).	DIGITAL STORAGE (J19: A8)	DISPLAY AMPLIFIER (J20: A8)
/DIGINH	(TTL) Disables the vector generator.	DISPLAY AMPLIFIER (J20: A7)	DIGITAL STORAGE (J19: A7)
DSCL	(TTL) High speed serial bus clock line: Controls the movement of data between the Log Processor and Digital Storage modules, and the Main Processor System.	MAIN PROCESSOR (J26: C28)	DIGITAL STORAGE (J19: B30) I/O INTERFACE 1 (J27: C28) LOG PROCESSOR (J17: B30) MEMORY (J28: C28)
DSDA	(TTL) High speed serial bus data line for the master IC bus linking the Log Processor, Digital Storage, and the Main Processor System.	MAIN PROCESSOR (J26: A28)	DIGITAL STORAGE (J19: B29) I/O INTERFACE 1 (J27: A28) LOG PROCESSOR (J17: B29) MEMORY (J28: A28)
DSH	(ANALOG) Digital Storage Horizontal Deflection signal. A single-ended low-level deflection signal having a sensitivity of 1.5V for full-screen deflection, and a nominal range of +/- 750mV.	DIGITAL STORAGE (J19: B5)	DISPLAY AMPLIFIER (J20: B5)
DSHRET	Return for DSH	DIGITAL STORAGE (J19: A5)	DISPLAY AMPLIFIER (J20: A5)
DSV	(ANALOG) Digital Storage Vertical Deflection signal. A single-ended low-level deflection signal having a sensitivity of 1.5V for full-screen deflection, and a nominal range of +/- 750mV.	DIGITAL STORAGE (J19: B3)	DISPLAY AMPLIFIER (J20: B3)
DSVRET	Return for DSV	DIGITAL STORAGE (J19: A3)	DISPLAY AMPLIFIER (J20: A3)

Table 7-1 continued

Title	Definition	Source	Destination
DSZ	(ANALOG) Digital Storage Z-Axis (Intensity) signal. A single-ended signal that allows Digital Storage to modulate the intensity of the display to allow for markers, high-lighted zones, intensified readout, etc. (Not used at this time.)	DIGITAL STORAGE (J19: A6)	DISPLAY AMPLIFIER (J20: A6)
DSZRET	Return for DSZ	DIGITAL STORAGE (J19: B6)	DISPLAY AMPLIFIER (J20: B6)
ECLKOUT	(TTL) Processor system synchronized clock.	MAIN PROCESSOR (J26: C26)	I/O INTERFACE 1 (J27: C26) MEMORY (J28: C26)
/EDMAAK0	(TTL) DMA Acknowledge from processor to peripheral (Instrument Serial Bus) that allows peripheral to proceed with the programmed operation.	MAIN PROCESSOR (J26: C20)	I/O INTERFACE 1 (J27: C20) MEMORY (J28: C20)
/EDMAAK1	(TTL) DMA Acknowledge from processor to peripheral (GPIB0) that allows peripheral to proceed with the programmed operation.	MAIN PROCESSOR (J26: A21)	I/O INTERFACE 1 (J27: A21) MEMORY (J28: A21)
/EDMAAK2	(TTL) DMA Acknowledge from processor to peripheral (GPIB1) that allows peripheral to proceed with the programmed operation.	MAIN PROCESSOR (J26: B21)	I/O INTERFACE 1 (J27: B21) MEMORY (J28: B21)
/EDMAAK3	(TTL) DMA Acknowledge from processor to peripheral (High Speed Serial Bus) that allows peripheral to proceed with programmed operation.	MAIN PROCESSOR (J26: C21)	I/O INTERFACE 1 (J27: C21) MEMORY (J28: C21)
/EDMARQ1	(TTL) DMA ReQuest #1 from communications interface (Active LOW).	COMM INTERFACE 1 (J23: 2)	I/O INTERFACE 2 (J25: B1)
/EDMARQ2	(TTL) DMA ReQuest #2 from communications interface (Active LOW).	COMM INTERFACE 1 (J23: 3)	I/O INTERFACE 2 (J25: A1)
EDMARQ0	(TTL) DMA request input line 0 (Instrument Serial Bus).	I/O INTERFACE 1 (J27: A22)	MAIN PROCESSOR (J26: A22) MEMORY (J28: A22)
EDMARQ1	(TTL) DMA request input line 1 (GPIB0)	I/O INTERFACE 1 (J27: B22)	MAIN PROCESSOR (J26: B22) MEMORY (J28: B22)

Table 7-1 continued

Title	Definition	Source	Destination
EDMARQ2	(TTL) DMA request input line 2 (GPIB1)	I/O INTERFACE 1 (J27: C22)	MAIN PROCESSOR (J26: C22) MEMORY (J28: C22)
EDMARQ3	(TTL) DMA request input line 3 (High Speed Serial Bus)	I/O INTERFACE 1 (J27: A23)	MAIN PROCESSOR (J26: A23) MEMORY (J28: A23)
/EINTP3	(TTL) Inverted (active LOW) processor interrupt 3 (GPIB0)	COMM INTERFACE 1 (J23: 7)	I/O INTERFACE 2 (J25: A3)
/EINTP4	(TTL) Inverted (active LOW) processor interrupt 4 (GPIB1)	COMM INTERFACE 1 (J23: 6)	I/O INTERFACE 2 (J25: B3)
EINTP2	(TTL) Processor interrupt 2 (High Speed Serial Bus)	I/O INTERFACE 1 (J27: C23)	MAIN PROCESSOR (J26: C23) MEMORY (J28: C23)
EINTP3	(TTL) Processor interrupt 3 (GPIB1)	I/O INTERFACE 1 (J27: A24)	MAIN PROCESSOR (J26: A24) MEMORY (J28: A24)
EINTP4	(TTL) Processor interrupt 4 (GPIB2)	I/O INTERFACE 1 (J27: B24)	MAIN PROCESSOR (J26: B24) MEMORY (J28: B24))
EINTP5	(TTL) Processor interrupt 5 (Instrument Serial Bus)	MAIN PROCESSOR (J26: C24)	I/O INTERFACE 1 (J27: C24) MEMORY (J28: C24)
EINTP6	(TTL) Processor interrupt 6 (Service request SRQ)	MAIN PROCESSOR (J26: A25)	I/O INTERFACE 1 (J27: A25) MEMORY (J28: A25)
EINTP7	(TTL) Processor interrupt 7 (On/Standby)	MAIN PROCESSOR (J26: B25)	I/O INTERFACE 1 (J27: B25) MEMORY (J28: B25)
/EIORD	(TTL) Indicates an IO read cycle (active LOW).	MAIN PROCESSOR (J26: B19)	I/O INTERFACE 1 1 (J27: B19) MEMORY (J28: B19)
/EIOWR	(TTL) Indicates an IO write cycle (active LOW).	MAIN PROCESSOR (J26: B20)	I/O INTERFACE 1 (J27: B20) MEMORY (J28: B20)
/EMR	(TTL) Indicates a memory read cycle (active LOW).	MAIN PROCESSOR (J26: A19)	I/O INTERFACE 1 (J27: A19) MEMORY (J28: A19)
/EMWR	(TTL) Indicates a memory write cycle (active LOW).	MAIN PROCESSOR (J26: A20)	I/O INTERFACE 1 (J27: A20) MEMORY (J28: A20)
EOC	(TTL) End Of Character. Hand-shaking signal used in real-time modes to show that Digital Storage just drew a character.	DIGITAL STORAGE (J19: A11)	DISPLAY AMPLIFIER (J20: A11)
EPROMVCC	EPROM programming voltage for VCC. Normally tied to +5VD by a jumper on the Digital Storage Board.	None	DIGITAL STORAGE (J19: A25)

Table 7-1 continued

Title	Definition	Source	Destination
EPROMVPP	EPROM programming voltage for VPP. Normally tied to +5VD by a jumper on the Digital Storage Board.	None	DIGITAL STORAGE (J19: A24)
/EPWE	(TTL) Disables EPROM write-protect circuitry controlling the data buffers to allow for external programming. (Active LOW)	MAIN PROCESSOR (J26: B10)	I/O INTERFACE 1 (J27: B10) MEMORY (J28: B10)
EREADY	(TTL) Allows peripheral devices to lengthen a bus cycle by forcing processor to insert wait states (when the signal is LOW).	MEMORY (J28: C19)	I/O INTERFACE 1 (J27: C19) MAIN PROCESSOR (J26: C19)
/ERESOUT	(TTL) Active low system reset function; internally synchronized with CLKOUT.	I/O INTERFACE 2 (P25: B4)	COMM INTERFACE 1 (J23: 8)
ERESOUT	(TTL) Active high system reset function; internally synchronized with CLKOUT.	MAIN PROCESSOR (J26: C9) MEMORY (J28: C9)	I/O INTERFACE 1 (J27: C9)
ETCTL2	(TTL) Timer 2 control line.	I/O INTERFACE 1 (J27: B28)	MAIN PROCESSOR (J26: B28) MEMORY (J28: B28)
ETOUT2	(TTL) Timer 2 output (internal timer output).	MAIN PROCESSOR (J26: B23)	I/O INTERFACE 1 (J27: B23) MEMORY (J28: B23)
EXT:T/H+	External trigger and horizontal input (positive).	COMM INTERFACE 2 (J23: 25)	SWEEP/SPAN ATTENUATOR (J13: A5)
EXT:T/H-	External trigger and horizontal input (negative).	COMM INTERFACE 2 (J23: 26)	SWEEP/SPAN ATTENUATOR (J13: B5)
EXTBLANK	(TTL) External blanking input accessible from rear panel. (HIGH ==> blank).	COMM INTERFACE 2 (J23: 22)	DISPLAY AMPLIFIER (J20: B9)
EXTH+	(ANALOG) External Horizontal Deflection input (positive): A low-level deflection signal having a sensitivity of approximately 90 mV/div when driven differentially by EXTH-.	COMM INTERFACE 2 (J23: 14)	DISPLAY AMPLIFIER (J20: B14)
EXTH-	(ANALOG) External Horizontal Deflection input (negative): A low-level deflec- of approximately 90 mV/div when driven differentially by EXTH+.	COMM INTERFACE 2 (J23: 16	DISPLAY AMPLIFIER (J20: A14)

Table 7-1 continued

Title	Definition	Source	Destination
EXTHO	(ANALOG) Single-ended horizontal deflection signal having a range of -1.25V to +1.25V.	DISPLAY AMPLIFIER (J20: A13)	COMM INTERFACE 2 (J23: 27)
EXTPSDR	Scaled version of preselector drive voltage sent to rear panel.	LO MODULE (J16: B14)	COMM INTERFACE 2 (J23: 7)
EXTPSRET	Return for EXTPSDR	LO MODULE (J16:A14)	COMM INTERFACE 2 (J23: 6)
EXTREF	External reference signal	COMM INTERFACE 2 (J23: 2)	REFERENCE OSCILLATOR (J12: A19)
EXTV+	(ANALOG) External Vertical Deflection input (positive): A low-level deflection signal having a sensitivity of approximately 65 mV/div when driven differentially by EXTV-.	COMM INTERFACE 2 (J23: 18)	DISPLAY AMPLIFIER (J20: B17)
EXTV-	(ANALOG) External Vertical Deflection input (negative): A low-level deflection signal having a sensitivity of approximately 65 mV/div when driven differentially by EXTV+.	COMM INTERFACE 2 (J23: 20)	DISPLAY AMPLIFIER (J20: A17)
EXTVI+	(ANALOG) External Video input(positive): An external video signal (capable of being filtered and digitized) having a sensitivity of approximately 87 mV/div when driven differentially by EXTVI-.	COMM INTERFACE 2 (J23: 10)	VIDEO PROCESSOR (J18: B5)
EXTVI-	(ANALOG) External Video input (negative): An external video signal (capable of being filtered and digitized) having a sensitivity of approximately 87 mV/div when driven differentially by EXTVI+.	COMM INTERFACE 2 (J23: 12)	VIDEO PROCESSOR (J18: A5)
EXTVO	(ANALOG) Single-ended vertical deflection signal having a range of -1.25V to +1.25V.	DISPLAY AMPLIFIER (J20: B13)	COMM INTERFACE 2 (J23: 29)
EXTZO	(ANALOG) External monitor Z-axis modulation signal having a range of 0 to 1V.	DISPLAY AMPLIFIER (J20: A12)	COMM INTERFACE 2 (J23: 31)
FAN1	(TTL) LSB fan speed control bit.	MAIN PROCESSOR (J26: B26)	I/O INTERFACE 1 (J27: B26) LV POWER SUPPLY (J22: A20) MEMORY (J28: B26)

Table 7-1 continued

Title	Definition	Source	Destination
FAN2	(TTL) MSB fan speed control bit.	MAIN PROCESSOR (J26: B27)	I/O INTERFACE 1 (J27: B27) LV POWER SUPPLY (J22: B20) MEMORY (J28: B27)
FM+	FM Coil tune (positive): The amplified sum of the FM coil sweep voltage (FMCSWP) and the filtered phase error voltage (1st LO) during locked modes, and equals the amplified FM coil sweep voltage (FMCSWP) during unlocked modes.	MICROWAVE PHASE-LOCK (P501: A5)	1ST LO (P502: A10)
FM-	FM Coil tune (negative): Return for FM+	MICROWAVE PHASE-LOCK (P501: B5)	1ST LO (P502: B9)
FMCRET	Return for FMCSWP	LO MODULE (J16: A21)	MICROWAVE PHASE-LOCK (P501: A7)
FMCSWP	FM coil sweep voltage	LO MODULE (J16:B21)	MICROWAVE PHASE-LOCK (P501: B7)
FMCRD	(ANALOG) FM coil Rail Detect; Senses FM coil bias and causes the bias on the main YIG coil to be adjusted if the FM coil is tuned beyond range.	MICROWAVE PHASE-LOCK (P501: B4)	LO MODULE (J16: A13)
FR	Divide by R counter output; internally connected to the phase detector input in the Reference Oscillator frequency synthesizer. This signal is thus locked to the 100-MHz reference frequency, and is typically 250 kHz.	REFERENCE OSCILLATOR (J12: A12)	PERIOD COUNTER (J14: A12)
FREQSWP+	(ANALOG) Frequency sweep voltage (positive).	SWEEP/SPAN ATTENUATOR (J13: B19)	LO MODULE (J16: B19)
FREQSWP-	(ANALOG) Frequency sweep voltage (negative).	SWEEP/SPAN ATTENUATOR (J13: A19)	LO MODULE (J16: A19)
FV	Divide by N counter output; internally connected to phase detector input in the Reference Oscillator frequency synthesizer. This signal is thus locked to the 100-MHz reference frequency, and is typically 250 kHz.	REFERENCE OSCILLATOR (J12: A13)	PERIOD COUNTER (J14: A13)

Table 7-1 continued

Title	Definition	Source	Destination
GND	Common return	LV POWER SUPPLY (J22: A1, A2, A3, A4, B10, A13, A17, B17, B22, B23, B24, B25)	1ST LO (P502: A5, B10) 525 IF (P506: A3) 565 SYNTHESIZER (J15: A2, B2, A3, B3, A6, B6, A8, A9, B9, A18, B18, B24, B25, A31, B31) CALIBRATOR (P508: A6) COMM INTERFACE 1 (J23: 1, 10, 16, 20, 22, 24, 26, 28, 30, 32, 34, 36, 40 COMM INTERFACE 2 (J23: 1, 3, 8, 9, 11, 13, 15, 17, 19, 21, 23, 28, 30, 32, 34) DIGITAL STORAGE (J19: A18, B18, B24, B25, A31, B31) DISPLAY AMPLIFIER (J20: A18, B18, B24, B25, A31, B31) FRONT PANEL (J10: B1) HIGH VOLTAGE (J21: A18, B18, B24, B25, A31, B31) I/O INTERFACE 1 (J27: A1, B1, C1, A11, B11, C11, A18, B18, C18, A31, B31, C31) LO MODULE (J16: A2, B2, A3, B3, A6, B6,A8, A9, B9, A18, B18, B24, B25, A31, B31) LOG PROCESSOR (J17: A18, B18, B24, B25, A31, B31) MAIN PROCESSOR (J26: A1, B1, C1, A11, B11, C11, A18, B18, C18, A31, B31, C31) MICROWAVE IF (P501: A2, B4, A5, A7, B7) MICROWAVE PHASE-LOCK (P501: B3) MTX CONTROL (P504: A3, B3, A9, B9) NOT USED (P503: A5) PERIOD COUNTER (J14: A18, B18, B24, B25, A31, B31) PRESELECTOR DRIVER (P505: A2) MEMORY (J28: A1, B1, C1, A11, B11, C11, A18, B18, C18, A31, B31, C31) REFERENCE OSCILLATOR (J12: A18, B18, B19, B24, B25, A31, B31) SPARE (J11: A18, B18, B24, B25, A31, B31) SWEEP/SPAN ATTENUATOR (J13: A18, B18, B24, B25, A31, B31) VIDEO PROCESSOR (J18: A18, B18, B24, B25, A31, B31) VR ASSEMBLY (P507: B4)
HVOFF	(TTL) An active HIGH signal that can be used to turn off the high-voltage power supply. (For now, this signal is grounded through a resistor on the Display Amplifier board.)	DISPLAY AMPLIFIER (J20: B10)	
IFG	(TTL)Turns calibrator or tracking generator off. (Unused)	PERIOD COUNTER (J14: B7)	CALIBRATOR (P508: A7)

Table 7-1 continued

Title	Definition	Source	Destination
IFPC	(TTL) IF output to period counter.	LOG PROCESSOR (J17: B9)	PERIOD COUNTER (J14: B9)
INTH+	(ANALOG) Internal real-time horizontal deflection signal: A low-level deflection signal having a sensitivity of 150 mV/div (expanded mode) and 120 mV/div (compressed mode).	VIDEO PROCESSOR (J18: B19)	DISPLAY AMPLIFIER (J20: B19)
INTH-	Return for INTH+	VIDEO PROCESSOR (J18: A19)	DISPLAY AMPLIFIER (J20: A19)
INTV+	(ANALOG) Internal real-time vertical deflection signal (positive): Low-level deflection signal with sensitivity of approx. 60 mV/div when driven differentially by INTV-.	VIDEO PROCESSOR (J18: B21)	DISPLAY AMPLIFIER (J20: B21)
INTV-	(ANALOG) Internal real-time vertical deflection signal (negative): Low-level deflection signal with sensitivity of approx. 60 mV/div when driven differentially by INTV+.	VIDEO PROCESSOR (J18: A21)	DISPLAY AMPLIFIER (J20: A21)
LA0	(TTL) Bit 1 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A2)	I/O INTERFACE 1 (J27: A2) MEMORY (J28: A2)
LA1	(TTL) Bit 2 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B2)	I/O INTERFACE 1 (J27: B2) MEMORY (J28: B2)
LA2	(TTL) Bit 3 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C2)	I/O INTERFACE 1 (J27: C2) MEMORY (J28: C2)
LA3	(TTL) Bit 4 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A3)	I/O INTERFACE 1 (J27: A3) MEMORY (J28: A3)
LA4	(TTL) Bit 5 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B3)	I/O INTERFACE 1 (J27: B3) MEMORY (J28: B3)
LA5	(TTL) Bit 6 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C3)	I/O INTERFACE 1 (J27: C3) MEMORY (J28: C3)
LA6	(TTL) Bit 7 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A4)	I/O INTERFACE 1 (J27: A4) MEMORY (J28: A4)
LA7	(TTL) Bit 8 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B4)	I/O INTERFACE 1 (J27: B4) MEMORY (J28: B4)
LA8	(TTL) Bit 9 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C4)	I/O INTERFACE 1 (J27: C4) MEMORY (J28: C4)

Table 7-1 continued

Title	Definition	Source	Destination
LA9	(TTL) Bit 10 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A5)	I/O INTERFACE 1 (J27: A5) MEMORY (J28: A5)
LA10	(TTL) Bit 11 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B5)	I/O INTERFACE 1 (J27: B5) MEMORY (J28: B5)
LA11	(TTL) Bit 12 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C5)	I/O INTERFACE 1 (J27: C5) MEMORY (J28: C5)
LA12	(TTL) Bit 13 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A6)	I/O INTERFACE 1 (J27: A6) MEMORY (J28: A6)
LA13	(TTL) Bit 14 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B6)	I/O INTERFACE 1 (J27: B6) MEMORY (J28: B6)
LA14	(TTL) Bit 15 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C6)	I/O INTERFACE 1 (J27: C6) MEMORY (J28: C6)
LA15	(TTL) Bit 16 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A7)	I/O INTERFACE 1 (J27: A7) MEMORY (J28: A7)
LA16	(TTL) Bit 17 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B7)	I/O INTERFACE 1 (J27: B7) MEMORY (J28: B7)
LA17	(TTL) Bit 18 of 20-bit latched address bus.	MAIN PROCESSOR (J26: C7)	I/O INTERFACE 1 (J27: C7) MEMORY (J28: C7)
LA18	(TTL) Bit 19 of 20-bit latched address bus.	MAIN PROCESSOR (J26: A8)	I/O INTERFACE 1 (J27: A8) MEMORY (J28: A8)
LA19	(TTL) Bit 20 of 20-bit latched address bus.	MAIN PROCESSOR (J26: B8)	I/O INTERFACE 1 (J27: B8) MEMORY (J28: B8)
LAVI+	(ANALOG) Log Amp Video (positive): A low-level video signal having a sensitivity of 75 mV/div (when driven differentially with LAVI-), centered about ground.	LOG PROCESSOR (J17: B17)	VIDEO PROCESSOR (J18: B17)
LAVI-	(ANALOG) Log Amp Video (negative): A low-level video signal having a sensitivity of 75 mV/div (when driven differentially with LAVI+), centered about ground.	LOG PROCESSOR (J17: A17)	VIDEO PROCESSOR (J18: A17)
LBS1	(TTL) Latched bus status signal 1: Indicates type of bus cycle being performed by the processor. 1 ⟹ WRITE : 0 ⟹ READ.	MAIN PROCESSOR (J26: B9)	I/O INTERFACE 1 (J27: B9) MEMORY (J28: B9)

Table 7-1 continued

Title	Definition	Source	Destination
LBS2	(TTL) Latched bus status signal 2: Indicates type of bus cycle being performed by the processor. 1 ==> WRITE : 0 ==> READ.	MAIN PROCESSOR (J26: A9)	I/O INTERFACE 1 (J27: A9) MEMORY (J28: A9)
LINEV	(ANALOG) A low-level 60Hz signal for line triggering.	LV POWER SUPPLY (J22: A9)	SWEEP/SPAN ATTENUATOR (J13: A14)
LOCNT	(TTL) Enables output of divide-by-32 counter in the Microwave phase-lock module, allowing the period counter to count beat frequency between 1st LO and 565/4 output.	LO MODULE (J16: B8)	MICROWAVE PHASE-LOCK (P501: A2)
LODR+	(ANALOG) YIG center frequency tune voltage (positive).	LO MODULE (J16: A25)	1ST LO (P502: A7)
LODR-	(ANALOG) YIG center frequency tune voltage (negative).	LO MODULE (J16: A24)	1ST LO (P502: B7)
LOFLT	(TTL) Controls main YIG coil bandwidth reduction.	LO MODULE (J16: B7)	1ST LO (P502: B1)
LOFRQ	Rear-panel scaled version of main YIG coil tune voltage.	LO MODULE (J16: B5)	COMM INTERFACE 2 (J23: 4)
LOFRQRTN	Return for LOFRQ	LO MODULE (J16: A5)	COMM INTERFACE 2 (J23: 5)
LOPC	(TTL) Period counter LO output.	LO MODULE (J16: B10)	PERIOD COUNTER (J14: B10)
/LUBE	(TTL) Latched Upper Byte Enable. A LOW indicates that the upper byte of the 16-bit data bus has valid data.	MAIN PROCESSOR (J26: C8)	I/O INTERFACE 1 (J27: C8) MEMORY (J28: C8)
MTX1	(TTL) LSB control bit for +MTXV supply.	MAIN PROCESSOR (J26: A26)	I/O INTERFACE 1 (J27: A26) LV POWER SUPPLY (J22: A18) MEMORY (J28: A26)
MTX2	(TTL) MSB control bit for +MTXV supply.	MAIN PROCESSOR (J26: A27)	I/O INTERFACE 1 (J27: A27) LV POWER SUPPLY (J22: B18) MEMORY (J28: A27)
+MTXV	Processor variable voltage supply used by preselector in Preselector Driver module. Nominal values are 0, 18V, 26V and 32V.	LV POWER SUPPLY (J22: A5)	PRESELECTOR DRIVER (P505: B6)

Table 7-1 continued

Title	Definition	Source	Destination
ON/OFF	(TTL) Connected to POWER switch, and is used to request changes between the standby and normal power supply modes.	FRONT PANEL (J10: B7)	I/O INTERFACE 1 (J27: C25) MAIN PROCESSOR (J26: C25) MEMORY (J28: C25)
OSC1	(TTL) Control bit for +OSCV supply.	I/O INTERFACE 2 (P25: B13)	LV POWER SUPPLY (J22: B7)
+OSCV	Processor variable voltage supply used in the 1st LO module. Nominal values are 18V and 26V.	LV POWER SUPPLY (J22: B5)	1ST LO (P502: B6)
PENLIFT	(TTL) Rear-panel output to lift plotter pen during sweep retrace. Can also be used as real-time blanking signal in external monitor mode.	VIDEO PROCESSOR (J18: A7)	COMM INTERFACE 2 (J23: 24)
PLLPC	(TTL) Output of 1st LO phase-lock to period counter. Output of +32 counter that counts beat frequency between 1st LO and 565/4 output.	MICROWAVE PHASE-LOCK (P501: A1)	PERIOD COUNTER (J14: B11)
/PLO	(TTL) Phase Lock On; used to turn on 1st LO Phase-lock (active LOW).	LO MODULE (J16: B13)	MICROWAVE PHASE-LOCK (P501: B2)
PROCDIS	(TTL) Disables the processor from system bus; allows using multiple processors.	MAIN PROCESSOR (J26: A10)	I/O INTERFACE 1 (J27: A10) MEMORY (J28: A10)
PSDR+	(ANALOG) Preselector positive drive voltage.	LO MODULE (J16: B17)	PRESELECTOR DRIVER (P505: A7)
PSDR-	(ANALOG) Preselector negative drive voltage.	LO MODULE (J16: A17)	PRESELECTOR DRIVER (P505: B7)
PSFLT	(TTL) Preselector coil bandwidth control signal.	MTX CONTROL (P504: B8)	PRESELECTOR DRIVER (P505: B1)
PSG	(TTL) Precision Sweep Gate: Indicates when sweep voltage is within digitizing limits of horizontal acquisition system.	VIDEO PROCESSOR (J18: B8)	DISPLAY AMPLIFIER (J20: B8) PERIOD COUNTER (J14: B22)
RDTRIG	(TTL) Initiates resonator ring-down during calibration to synchronize horizontal digitizer with beginning of ring-down.	VIDEO PROCESSOR (J18: B22)	VR ASSEMBLY (P507: A5)

Table 7-1 continued

Title	Definition	Source	Destination
RES	(TTL) Serial bus reset line.	MAIN PROCESSOR (J26: A30)	525 IF (P506: B4) 565 SYNTHESIZER (J15: A30) CALIBRATOR (P508: A9) COMM INTERFACE 2 (J23: 40 DIGITAL STORAGE (J19: A30) DISPLAY AMPLIFIER (J20: A30) FRONT PANEL (J10: A3) HIGH VOLTAGE (J22: A30) I/O INTERFACE 1 (J27: A30) LOG PROCESSOR (J17: A30) LO MODULE (J16: A30) MICROWAVE IF (P501: B3) MTX CONTROL (P504: B2) NOT USED (P503: A1) PERIOD COUNTER (J14: A30) MEMORY (J28: A30) REFERENCE OSCILLATOR (J12: A30) SWEEP/SPAN ATTENUATOR (J13: A30) SPARE (J11: A30) VIDEO PROCESSOR (J18: A30) VR ASSEMBLY (P507: B5)
/RESET	(TTL) Inverted system reset pulse; Initializes over-voltage protection circuitry in the High Voltage Power Supply.	DISPLAY AMPLIFIER (J20: B7)	HIGH VOLTAGE (J22: B7)
SCL	(TTL) Serial bus clock line: A serial clock that controls the movement of data on the serial bus.	MAIN PROCESSOR (J26: B30)	525 IF (P506: A4) 565 SYNTHESIZER (J15: B30) CALIBRATOR (P508: B9) COMM INTERFACE 2 (J23: 39) DIGITAL STORAGE (J19: B30) DISPLAY AMPLIFIER (J20: B30) FRONT PANEL (J10: B2) HIGH VOLTAGE (J22: B30) I/O INTERFACE 1 (J27: B30) LOG PROCESSOR (J17: B30) LO MODULE (J16: B30) MICROWAVE IF (P501: A4) MTX CONTROL (P504: A1) NOT USED (P503: B1) PERIOD COUNTER (J14: B30) MEMORY (J28: B30) REFERENCE OSCILLATOR (J12: B30) SWEEP/SPAN ATTENUATOR (J13: B30) SPARE (J11: B30) VIDEO PROCESSOR (J18: B30) VR ASSEMBLY (P507: B3)

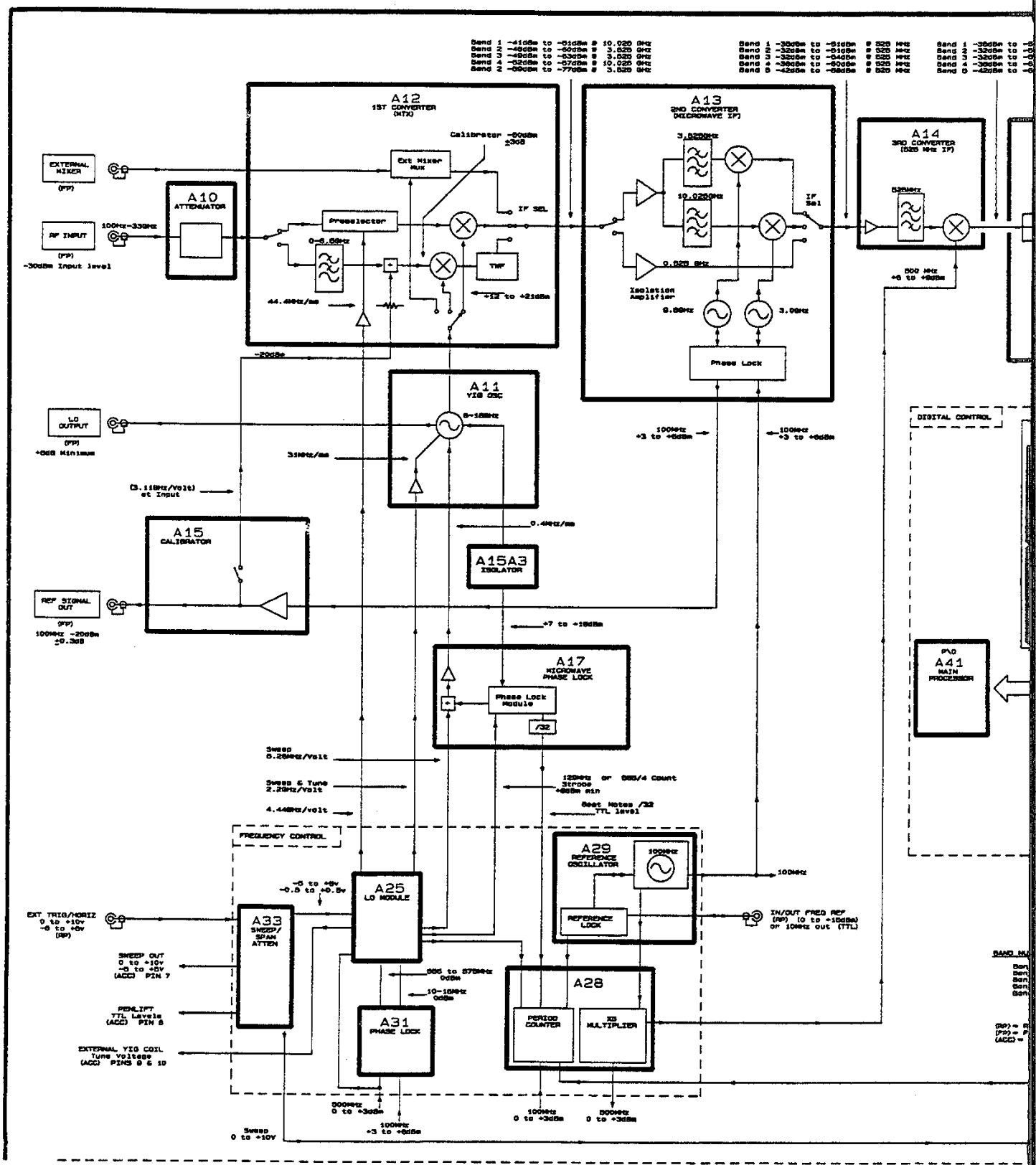
Table 7-1 continued

Title	Definition	Source	Destination
SDA	(TTL) Serial bus data line.	MAIN PROCESSOR (J26: B29)	525 IF (P506: A5) 565 SYNTHESIZER (J15: B29) CALIBRATOR (P508: A10) COMM INTERFACE 2 (J23: 38) DIGITAL STORAGE (J19: B29) DISPLAY AMPLIFIER (J20: B29) FRONT PANEL (J10: A2) HIGH VOLTAGE (J22: B29) I/O INTERFACE 1 (J27: B29) LOG PROCESSOR (J17: B29) LO MODULE (J16: B29) MICROWAVE IF (P501: A3) MTX CONTROL (P504: A2) NOT USED (P503: B1) PERIOD COUNTER (J14: B29) MEMORY (J28: B29) REFERENCE OSCILLATOR (J12: B29) SWEEP/SPAN ATTENUATOR (J13: B29) SPARE (J11: B29) VIDEO PROCESSOR (J18: B29) VR ASSEMBLY (P507: A2)
SDAH	(TTL) Serial data line for the digitized horizontal data.	VIDEO PROCESSOR (J18: B12)	DIGITAL STORAGE (J19: B12) LOG PROCESSOR (J17: B12)
SDAHSE	(TTL) Serial DAta Horizontal Shift Enable: Enables shifting of only horizontal data into acquisition shift register on Digital Storage board.	VIDEO PROCESSOR (J18: A13)	DIGITAL STORAGE (J19: A13)
SDASE	(TTL) Serial DAta Shift: Enable: Enables shifting serially transmitted vertical and horiz-ontal digitized data into acquisit ion acquisition shift registers on Digital Storage board.	VIDEO PROCESSOR (J18: A12) LOG PROCESSOR (J17: A12)	DIGITAL STORAGE (J19: A12)
SDAV	(TTL) Serial data line for the digitized vertical data.	VIDEO PROCESSOR (J18: B11)	DIGITAL STORAGE (J19: B11)
SLZS	Sweep Length Zero Span: Counted by the period counter to define an 11-division window.	SWEEP/SPAN ATTENUATOR (J13: B2)	PERIOD COUNTER (J14: B2)
SPLYFAIL	(TTL) Indicates loss of power supply regulation due to current limit, short circuit, etc.	LV POWER SUPPLY (J22: B8)	I/O INTERFACE 1 (J27: C29) MAIN PROCESSOR (J26: C29) MEMORY (J28: C29)
/SPLYON	(TTL) Control bit that enables the power supply output.	MAIN PROCESSOR (J26: C27)	I/O INTERFACE 1 (J27: C27) LV POWER SUPPLY (J22: A7) MEMORY (J28: C27)

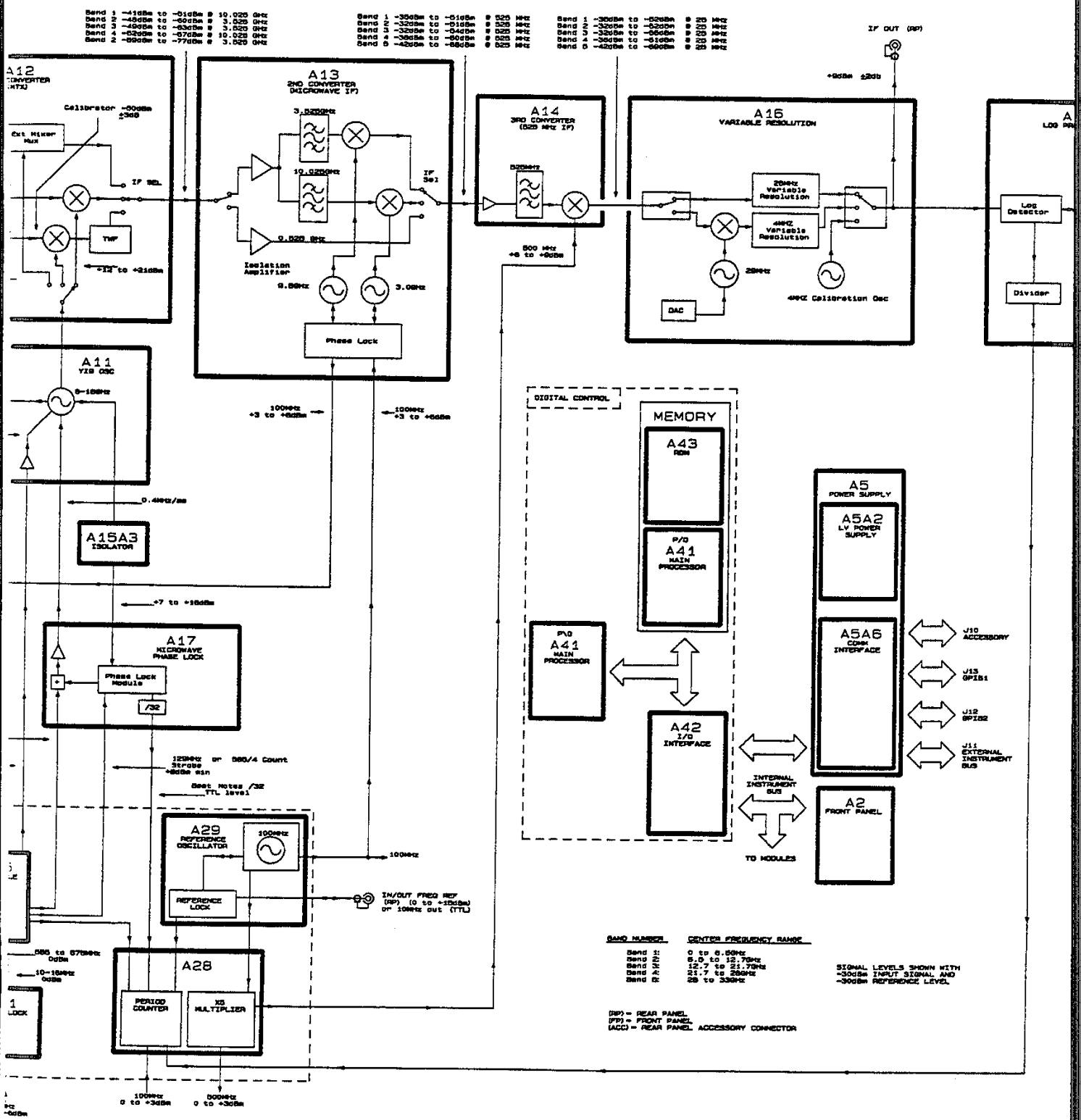
Table 7-1 continued

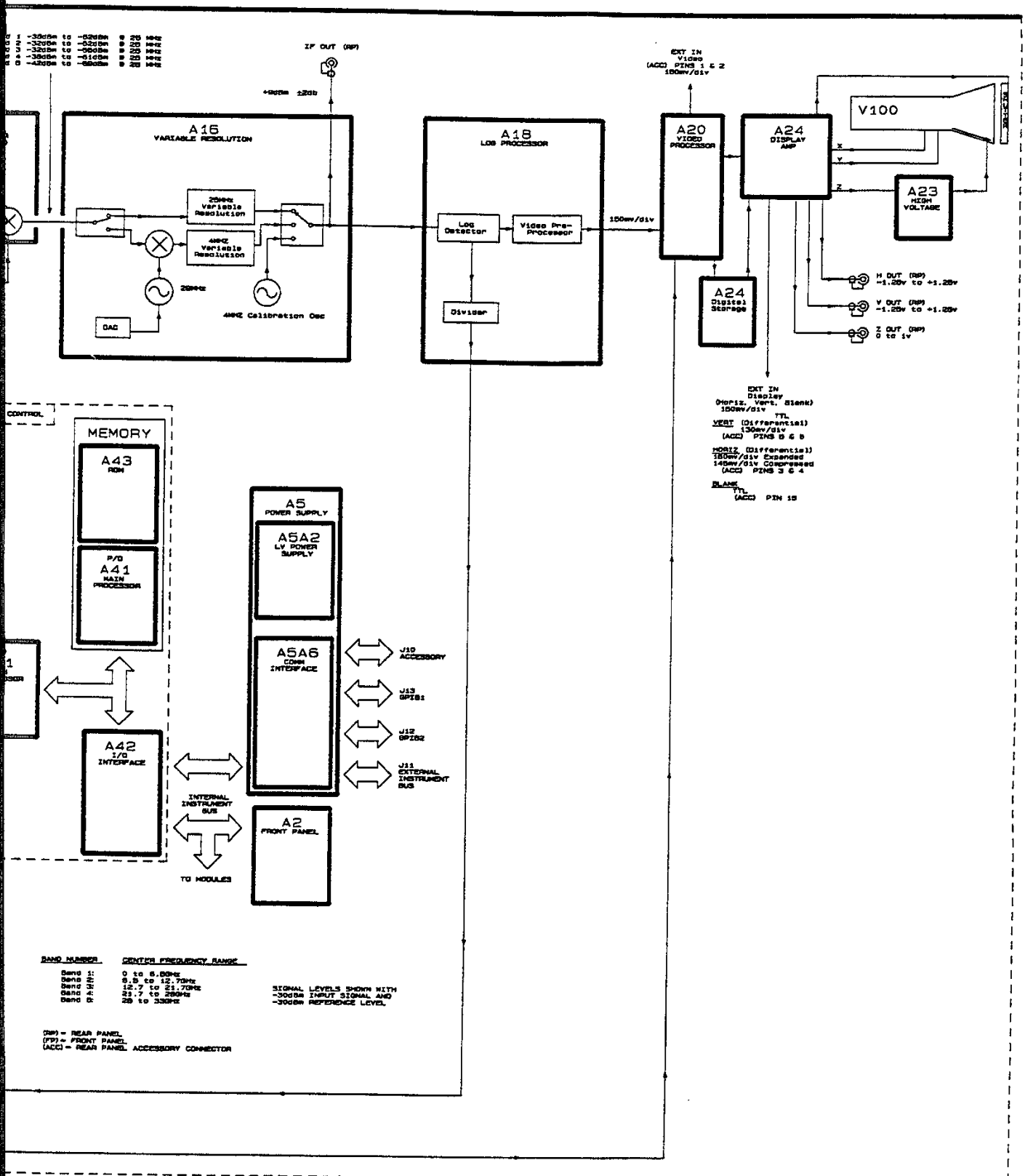
Title	Definition	Source	Destination
/SRQ	(TTL) Serial bus service request line (Active LOW). Notifies processor of module service requests.	MAIN PROCESSOR (J26: A29)	525 IF (P506: B5) 565 SYNTHESIZER (J15: A29) CALIBRATOR (P508: A8) COMM INTERFACE 2 (J23: 37) DIGITAL STORAGE (J19: A29) DISPLAY AMPLIFIER (J20: A29) FRONT PANEL (J10: B3) HIGH VOLTAGE (J22: A29) I/O INTERFACE 1 (J27: A29) LOG PROCESSOR (J17: A29) LO MODULE (J16: A29) MICROWAVE IF (P501: B2) PERIOD COUNTER (J14: A29) MEMORY (J28: A29) REFERENCE OSCILLATOR (J12: A29) SWEEP/SPAN ATTENUATOR (J13: A29) SPARE (J11: A29) VIDEO PROCESSOR (J18: A29) VR ASSEMBLY (P507: A6)
SWEEP+	(ANALOG) 0 to 10V sweep signal that drives acquisition system.	SWEEP/SPAN ATTENUATOR (J13: A25)	VIDEO PROCESSOR (J18: A25)
SWEEP-	Return for SWEEP+	SWEEP/SPAN ATTENUATOR (J13: A24)	VIDEO PROCESSOR (J18: A24)
SWPGATE	(TTL) Indicates valid sweep by going HIGH when sweep is active and LOW during retrace and hold-off.	SWEEP/SPAN ATTENUATOR (J13: A22)	LOG PROCESSOR (J17: A22) VIDEO PROCESSOR (J18: A22)
SWPOUT	Sweep voltage output to rear panel. Selectable ranges of 0 to 10V, or -5V to +5V (corresponds to sweep input).	SWEEP/SPAN ATTENUATOR (J13: A6)	COMM INTERFACE 2 (J23: 33)
TRIG+	Internal TRIGger (positive): A differential signal provided for internal triggering. Ranges from +1V to -1V.	VIDEO PROCESSOR (J18: B3)	SWEEP/SPAN ATTENUATOR (J13: B3)
TRIG-	Internal TRIGger (negative): A differential signal provided for internal triggering. Ranges from +1V to -1V.	VIDEO PROCESSOR (J18: A3)	SWEEP/SPAN ATTENUATOR (J13: A3)
WBD	(TTL) Waveform Being Drawn: When HIGH, indicates a digitally stored waveform is being drawn. This differentiates the waveform from readout and graticule information.	DIGITAL STORAGE (J19: A2)	DISPLAY AMPLIFIER (J20: A2)
YIGRET	Return line for +MTXV and +OSCV supplies	LV POWER SUPPLY (J22: A6, B6)	1ST LO (P502: A6) PRESELECTOR DRIVER (P505: A6)
UNUSED	Not used.	CALIBRATOR (P508: B7)	PERIOD COUNTER (J14: B8)

1 Sht 1 of 3


A12
1ST CONVERTER
(MTX)
A13
2ND CONVERTER
(MICROWAVE IF)
A14
3RD CONVERTER
(525 MHz IF)
A10
ATTENUATOR
A11
YIG OSC
A15
CALIBRATOR
A15A3
ISOLATOR
A17
MICROWAVE
PHASE LOCK
A25
LO MODULE
A29
REFERENCE
OSCILLATOR
A33
SWEEP/
SPAN
ATTEN
A28
A31
PHASE LOCK
A41
MAIN
PROCESSOR
EXTERNAL
MIXER
RF INPUT
LO
OUTPUT
REF SIGNAL
OUT
Ext Mixer
Mux
Preselector
TWT
Isolation
Amplifier
Phase Lock
Phase Lock
Module
/32
REFERENCE
LOCK
PERIOD
COUNTER
X5
MULTIPLIER
DIGITAL CONTROL
FREQUENCY CONTROL
Calibrator -60dBm
±3dB
3.025GHz
10.025GHz
0.525 GHz
525MHz
800 MHz
+6 to +8dBm
9.5GHz
3.0GHz
IF SEL
IF
Sel
100MHz
+3 to +6dBm
100MHz
+3 to +6dBm
-20dBm
+7 to +10dBm
0.4MHz/mm
51MHz/mm
(3.11MHz/Volt)
at Input
44.4MHz/mm
+12 to +21dBm
100MHz -20dBm
±0.3dB
+0dB Minimum
-30dBm Input level
100MHz-33GHz
(PP)
0-8.5GHz
Sweep
8.25MHz/Volt
Sweep & Tune
2.22Hz/Volt
4.44MHz/volt
128MHz or 655/4 Count
Strobe
+8dBm min
Sent Notes /32
TTL level
-5 to +5V
-0.5 to +0.5V
EXT TRIG/HORIZ
0 to +10V
-5 to +5V
(RP)
SWEEP OUT
0 to +10V
-5 to +5V
(ACC) PIN 7
PENLIFT
TTL Levels
(ACC) PIN 8
EXTERNAL YIG COIL
Tune Voltage
(ACC) PINS 9 & 10
500 to 575MHz
0dBm
10-18MHz
0dBm
500MHz
0 to +3dBm
100MHz
+3 to +6dBm
100MHz
0 to +3dBm
500MHz
0 to +3dBm
Sweep
0 to +10V
100MHz
IN/OUT FREQ REF
(RP) (0 to +10dBm)
or 10MHz out (TTL)
Band 1 -41dBm to -51dBm @ 10.020 GHz
Band 2 -48dBm to -60dBm @ 3.020 GHz
Band 3 -49dBm to -63dBm @ 3.020 GHz
Band 4 -62dBm to -67dBm @ 10.020 GHz
Band 5 -68dBm to -77dBm @ 3.020 GHz
Band 1 -30dBm to -51dBm @ 525 MHz
Band 2 -32dBm to -51dBm @ 525 MHz
Band 3 -32dBm to -54dBm @ 525 MHz
Band 4 -36dBm to -50dBm @ 525 MHz
Band 5 -42dBm to -58dBm @ 525 MHz
Band 1 -30dBm to
Band 2 -32dBm to
Band 3 -32dBm to
Band 4 -30dBm to
Band 5 -42dBm to

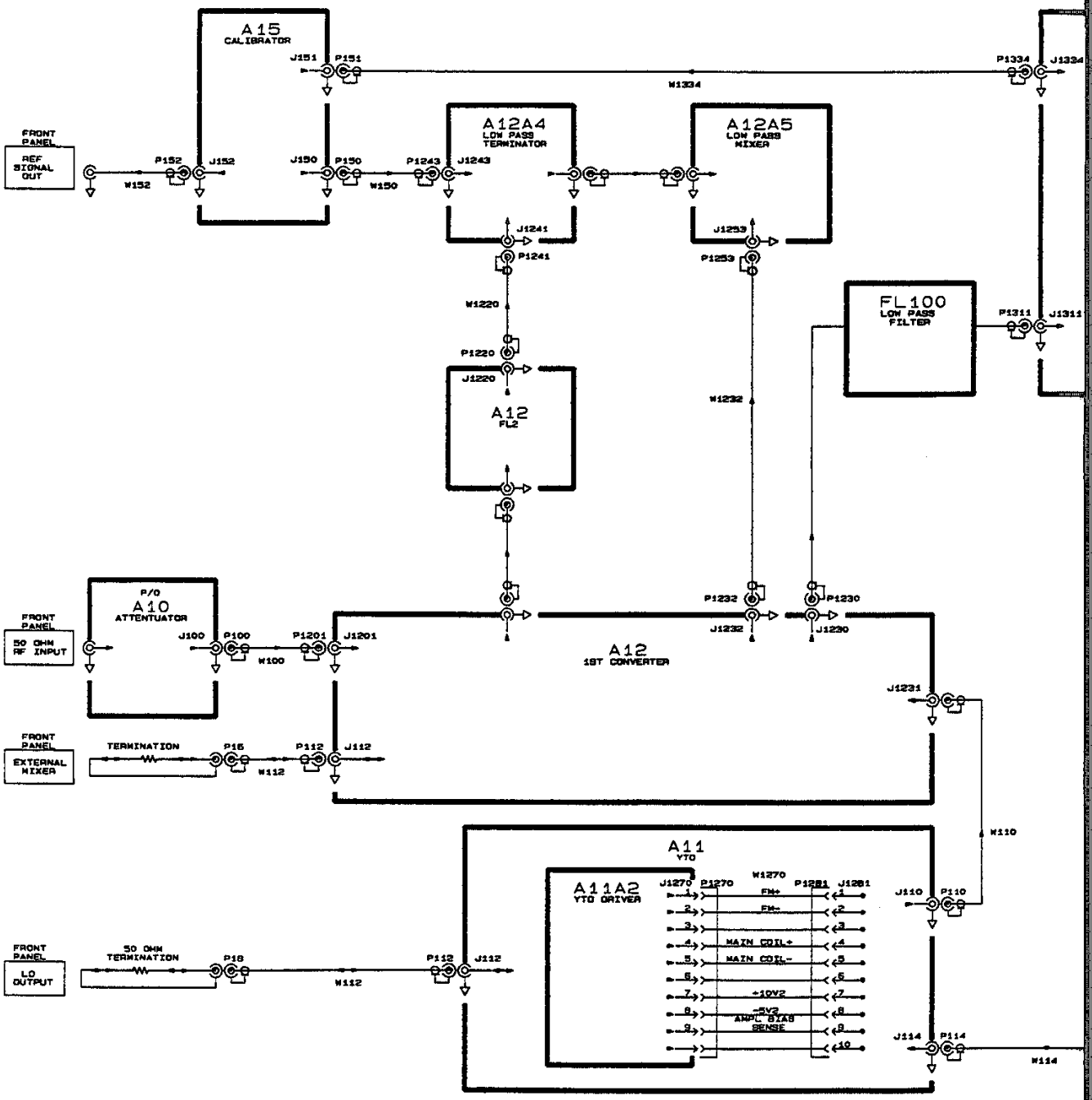
(1) Sht. 2 of 3


A12
A13
2ND CONVERTER
(MICROWAVE IF)
A14
3RD CONVERTER
(620 MHz IF)
A16
VARIABLE RESOLUTION
IF OUT (RP)
+9dBm ±2db
Calibrator -50dBm ±3dB
Ext Mixer Mux
IF SEL
YIG
+12 to +21dBm
3.5200MHz
10.020GHz
0.520 GHz
IF Sel
Isolation Amplifier
8.5GHz
3.0GHz
Phase Lock
620MHz
800 MHz +6 to +9dBm
20MHz Variable Resolution
4MHz Variable Resolution
DAC
25MHz
40MHz Calibration Osc
LOG Detector
Divider
A11
YIG OSC
8-18GHz
100MHz +3 to +6dBm
100MHz +3 to +6dBm
0.4MHz/ms
A15A3
ISOLATOR
+7 to +16dBm
A17
MICROWAVE PHASE LOCK
Phase Lock Module
/32
12MHz or 560/4 Count Strobe +4dBm min
Gate Notes /32 TTL level
DIGITAL CONTROL
MEMORY
A43
ROM
P/O
A41
MAIN PROCESSOR
P\O
A41
MAIN PROCESSOR
A42
I/O INTERFACE
A5
POWER SUPPLY
A5A2
LV POWER SUPPLY
A5A6
COMM INTERFACE
J10 ACCESSORY
J13 GPIB1
J12 GPIB2
J11 EXTERNAL INSTRUMENT BUS
INTERNAL INSTRUMENT BUS
TO MODULES
A2
FRONT PANEL
A29
REFERENCE OSCILLATOR
100MHz
REFERENCE LOCK
100MHz
IN/OUT FREQ REF (RP) (0 to +15dBm) or 10MHz out (TTL)
560 to 670MHz 0dBm
10-18GHz 0dBm
A28
PERIOD COUNTER
X5 MULTIPLIER
100MHz 0 to +3dBm
500MHz 0 to +3dBm
BAND NUMBER
CENTER FREQUENCY RANGE
Band 1: 0 to 8.5GHz
Band 2: 8.5 to 12.7GHz
Band 3: 12.7 to 21.7GHz
Band 4: 21.7 to 26GHz
Band 5: 26 to 33GHz
SIGNAL LEVELS SHOWN WITH -30dBm REFERENCE LEVEL
(RP) = REAR PANEL
(FP) = FRONT PANEL
(ACC) = REAR PANEL ACCESSORY CONNECTOR

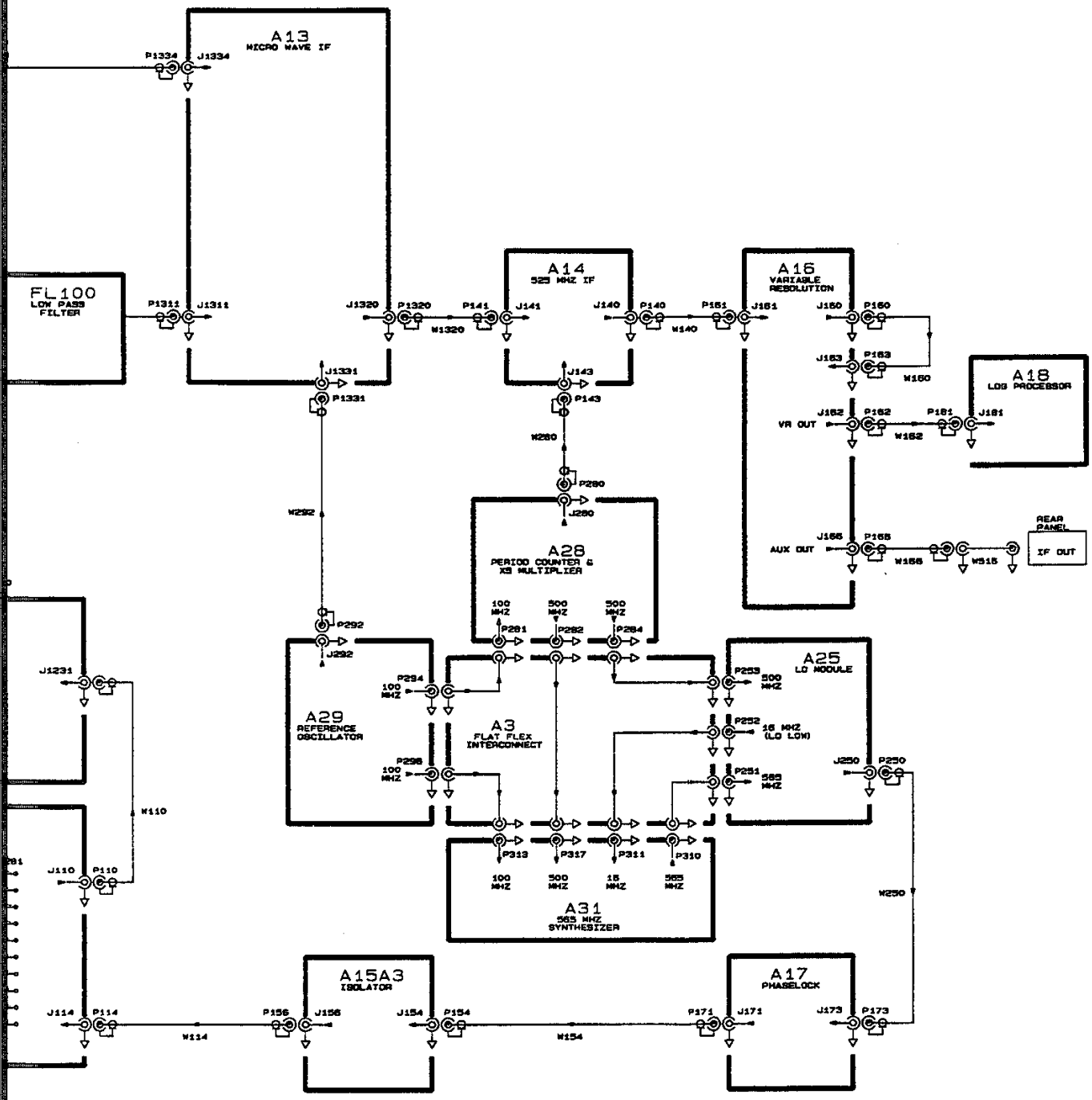


BLOCK DIAGRAM 1

9 Sht. 1 of 2

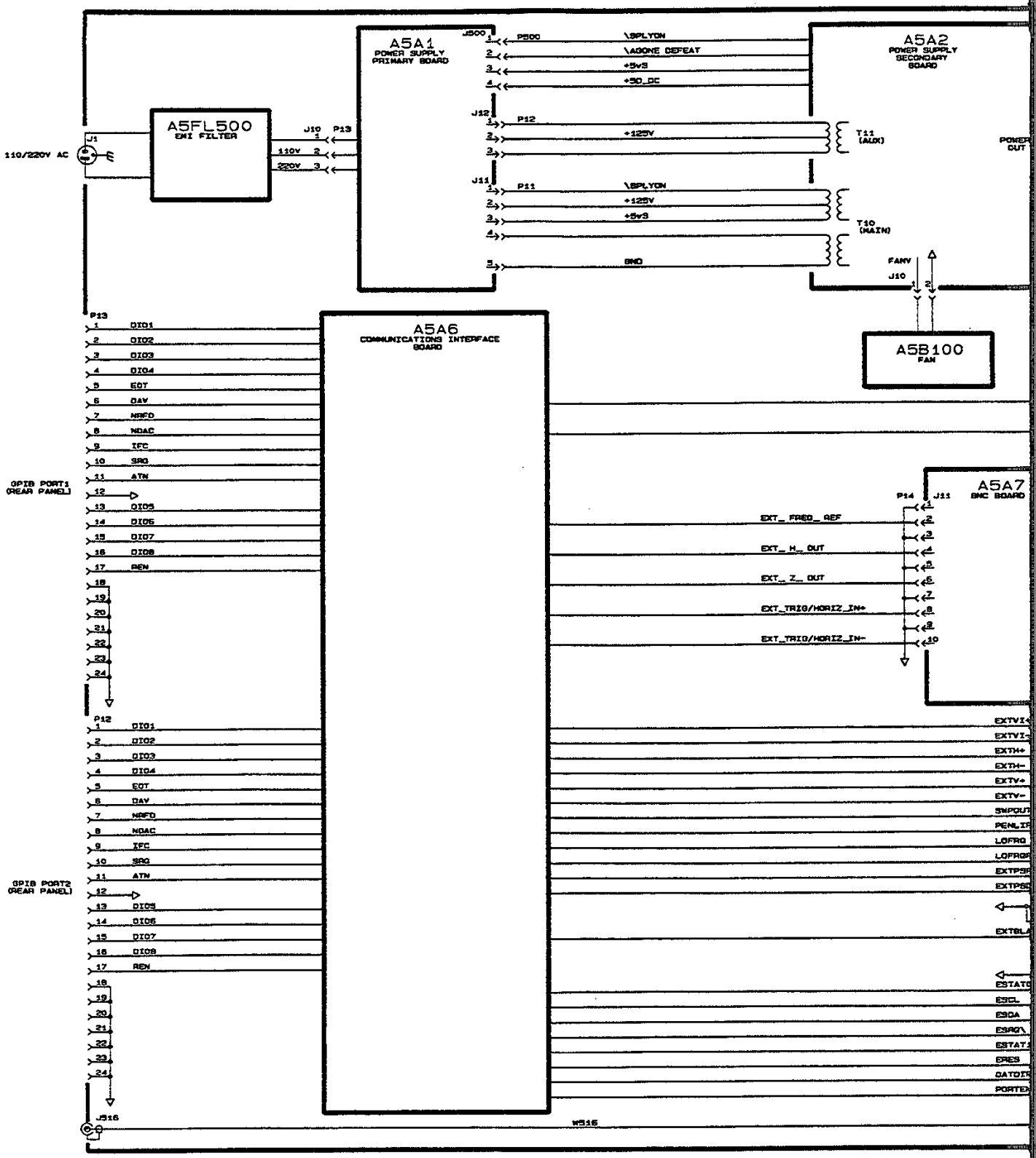

A15
CALIBRATOR
J151
P151
W1334
P1334
J1334
FRONT PANEL
REF SIGNAL OUT
P152
J152
W152
J150
P150
W150
P1243
J1243
A12A4
LOW PASS TERMINATOR
A12A5
LOW PASS MIXER
J1241
P1241
J1253
P1253
W1220
P1220
J1220
A12
FL2
W1232
FL100
LOW PASS FILTER
P1311
J1311
P/O
A10
ATTENTUATOR
FRONT PANEL
50 OHM RF INPUT
J100
P100
P1201
J1201
W100
P1232
J1232
P1230
J1230
A12
1ST CONVERTER
J1231
FRONT PANEL
EXTERNAL MIXER
TERMINATION
P16
P112
J112
W112
W110
A11
YTO
A11A2
YTO DRIVER
J1270
P1270
W1270
P1281
J1281
FM+
FM-
MAIN COIL+
MAIN COIL-
+10V2
-5V2
AMPL BIAS SENSE
J110
P110
FRONT PANEL
LO OUTPUT
50 OHM TERMINATION
P18
P112
J112
W112
J114
P114
W114

2 Sht. 2 of 2



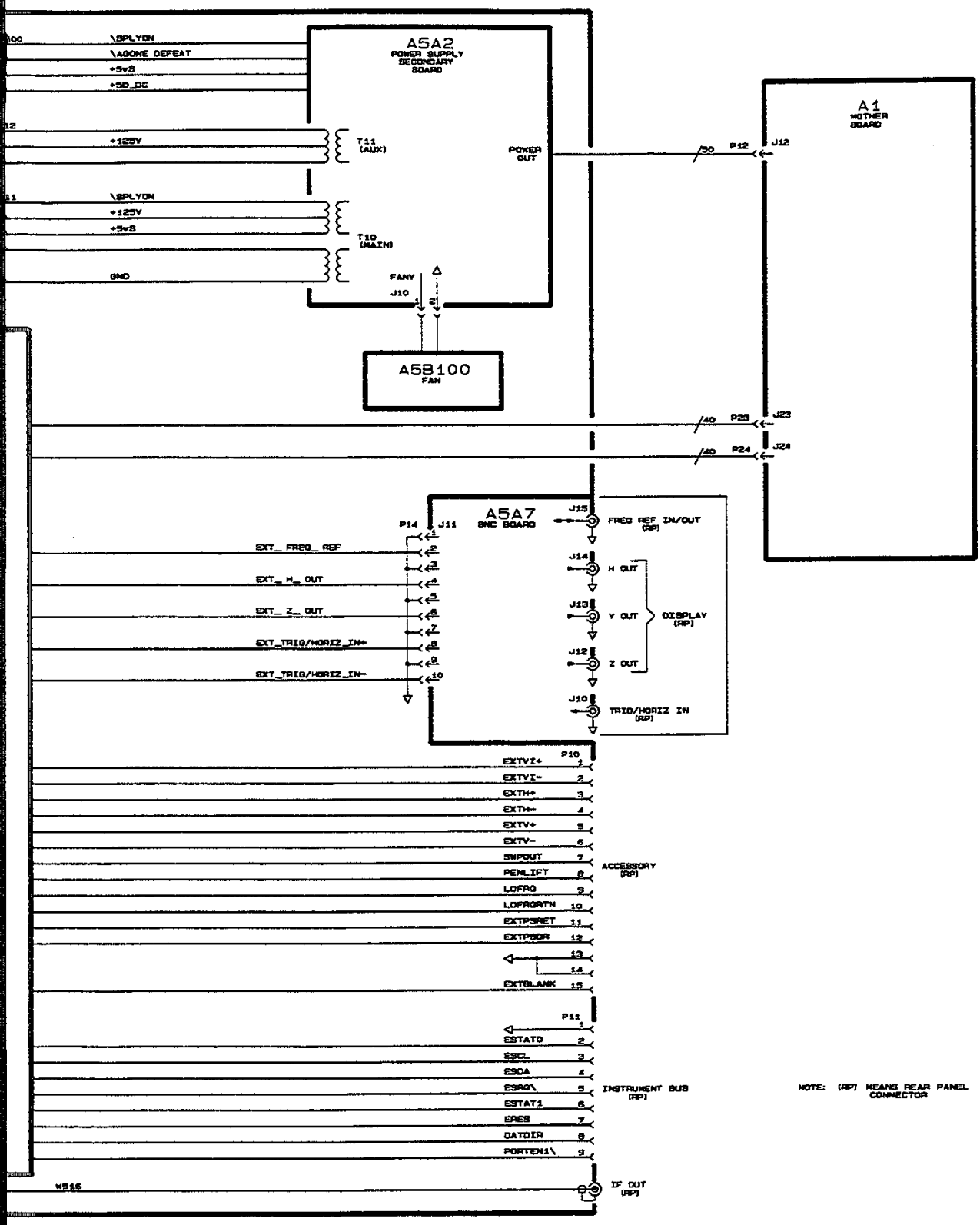
RF DECK INTERCONNECTIONS

3 Sht. 1 of 2



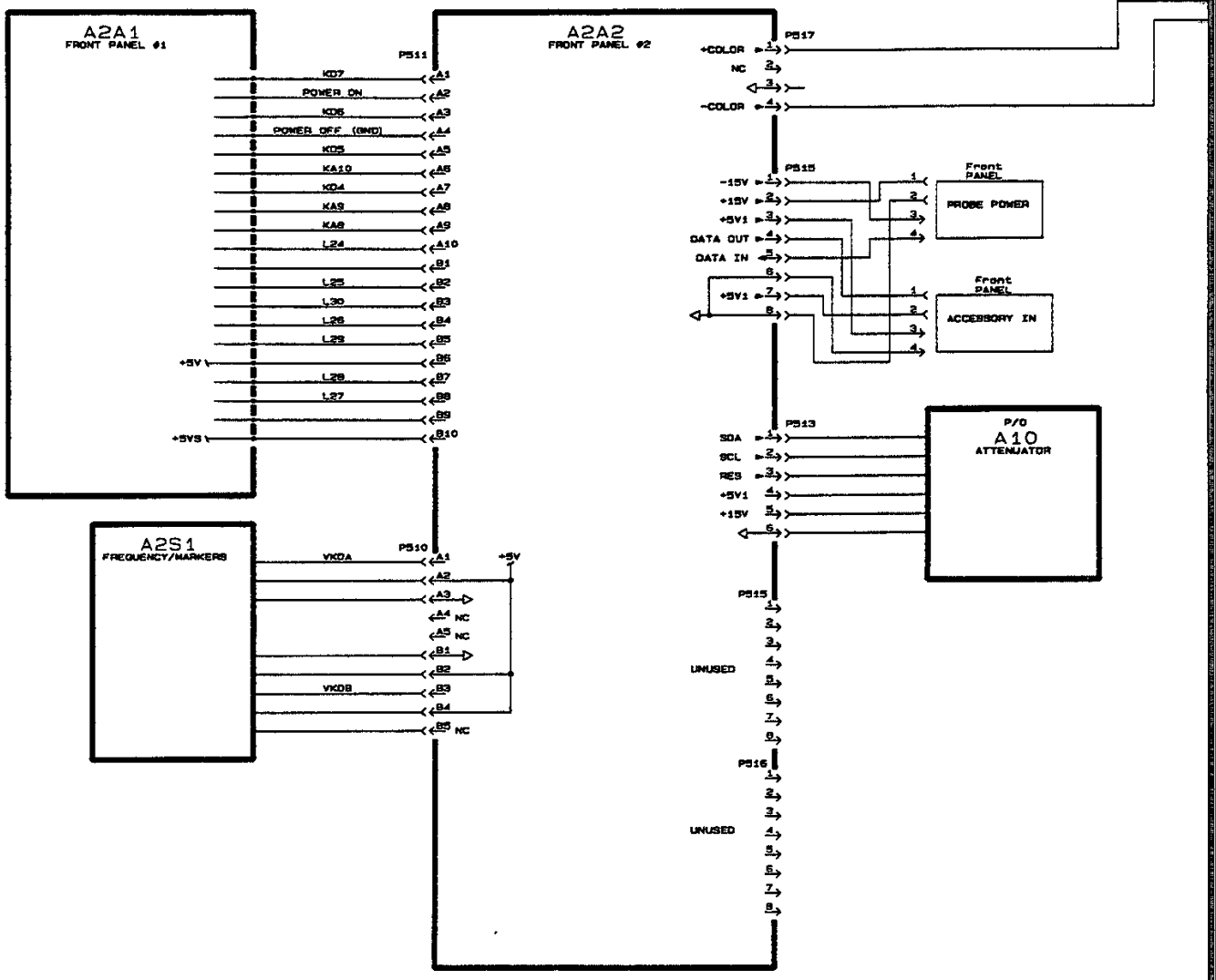
REAR PANEL AND L

3 Sht. 2 of 2

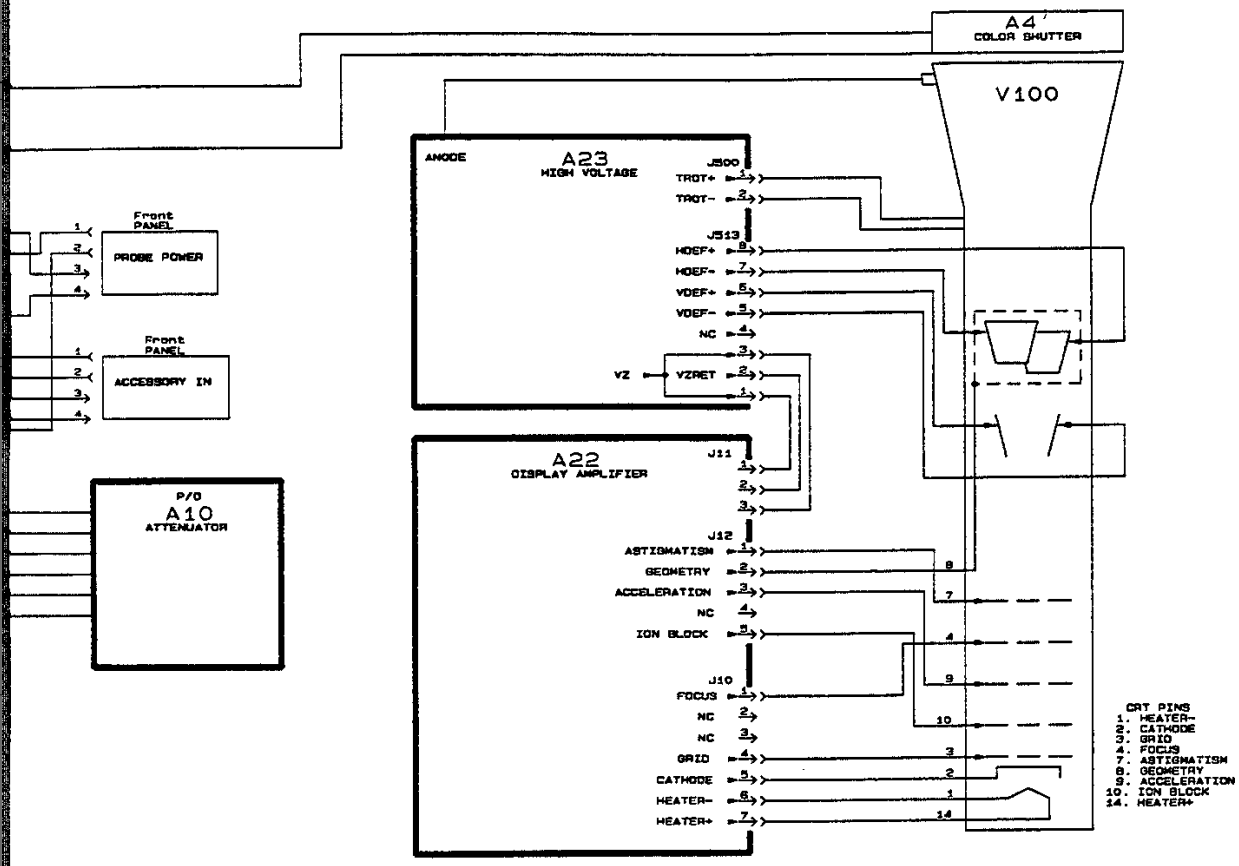


REAR PANEL AND LV SUPPLY INTERCONNECTIONS 3

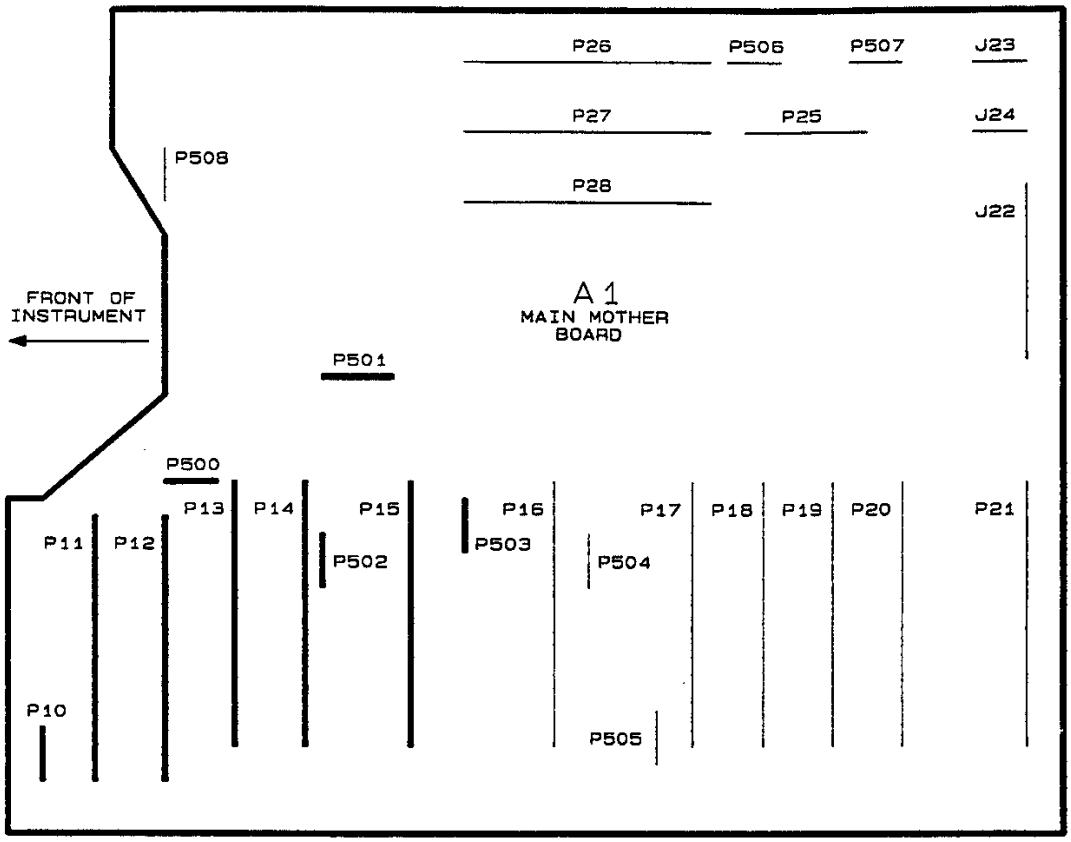
4 Sht. 1 of 2


A2A1
FRONT PANEL #1
P511
KD7
POWER ON
KD6
POWER OFF (GND)
KD5
KA10
KD4
KA9
KA8
L24
L25
L30
L26
L29
+5V
L28
L27
+5VS
A2A2
FRONT PANEL #2
P517
+COLOR
NC
-COLOR
P515
-15V
+15V
+5V1
DATA OUT
DATA IN
+5V1
Front PANEL
PROBE POWER
Front PANEL
ACCESSORY IN
P513
SDA
SCL
RES
+5V1
+15V
P/O
A10
ATTENUATOR
A2S1
FREQUENCY/MARKERS
P510
VKDA
+5V
NC
NC
VKDB
NC
P515
UNUSED
P516
UNUSED

4 Sht. 2 OF 2



FRONT PANEL & DISPLAY INTERCONNECTIONS

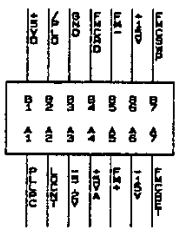


NOTE: P500 SERIES #'S ARE ON BACK OF BOARD.

FIG. 7-1. MOTHER BOARD CONNECTOR LOCATIONS 1

(5) Sht. 1 of 2

P550
TO A17 MICROWAVE PHASE LOCK



P11
SPARE

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	NC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	NC
NC	B12	A12	NC
NC	B11	A11	NC
NC	B10	A10	NC
NC	B9	A9	NC
NC	B8	A8	NC
NC	B7	A7	NC
NC	B6	A6	NC
NC	B5	A5	NC
-8V	B4	A4	-8V
NC	B3	A3	NC
NC	B2	A2	NC
NC	B1	A1	XX

P12
TO A29 REFERENCE OSCILLATOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	NC
+16V8	B21	A21	NC
-5.2V	B20	A20	-5.2V
GND	B19	A19	EXTREF
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	FV
NC	B12	A12	FR
NC	B11	A11	NC
NC	B10	A10	NC
NC	B9	A9	NC
NC	B8	A8	NC
NC	B7	A7	NC
NC	B6	A6	NC
NC	B5	A5	NC
-8V	B4	A4	-8V
NC	B3	A3	NC
NC	B2	A2	NC
1MHz	B1	A1	XX

P13
TO A33 SWEEP/SPAN ATTENUATOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	SWEEP+
GND	B24	A24	SWEEP-
-15V	B23	A23	-15V
NC	B22	A22	SWPGATE
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
FREQSWP+	B19	A19	FREQSWP-
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	LINEV
NC	B13	A13	NC
NC	B12	A12	NC
NC	B11	A11	NC
NC	B10	A10	NC
NC	B9	A9	NC
NC	B8	A8	NC
NC	B7	A7	NC
NC	B6	A6	SWPOUT
EXT: T/H-	B5	A5	EXT: T/H+
-8V	B4	A4	-8V
TRIG+	B3	A3	TRIG-
SLZS	B2	A2	NC
NC	B1	A1	XX

P14
TO A28 PERIOD CO

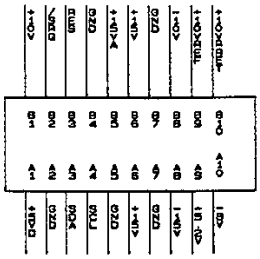
+5VD	B32	A32	
GND	B31	A31	
SCL	B30	A30	
SDA	B29	A29	
+5VA	B28	A28	
+10VREF	B27	A27	
+15V	B26	A26	
GND	B25	A25	
GND	B24	A24	
-15V	B23	A23	
PSG	B22	A22	
NC	B21	A21	
-5.2V	B20	A20	
NC	B19	A19	
GND	B18	A18	
NC	B17	A17	
+10V	B16	A16	
+45V	B15	A15	
NC	B14	A14	
NC	B13	A13	
NC	B12	A12	
PLLPC	B11	A11	
LOPC	B10	A10	
IFPC	B9	A9	
RF/TG-PC	B8	A8	
IFG	B7	A7	
NC	B6	A6	
NC	B5	A5	
-8V	B4	A4	
NC	B3	A3	
SLZS	B2	A2	
1MHz	B1	A1	

J10
TO A2A1 & A2A2 FRONT PANEL

ON/OFF	B7	A7	+15V
-5.2V	B6	A6	-15V
+5VS	B5	A5	-8V
COLOR-	B4	A4	COLOR+
/SRQ	B3	A3	RES
SCL	B2	A2	SDA
GND	B1	A1	+5VD

5 Sht. 2 of 2

P501
TO A13 MICRO WAVE IF



P13
TO A33 SWEEP/SPAN ATTENUATOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	SWEEP+
GND	B24	A24	SWEEP-
-15V	B23	A23	-15V
NC	B22	A22	SWPGATE
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
FREQSWP+	B19	A19	FREQSWP-
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	LINEV
NC	B13	A13	NC
NC	B12	A12	NC
NC	B11	A11	NC
NC	B10	A10	NC
NC	B9	A9	NC
NC	B8	A8	NC
NC	B7	A7	NC
NC	B6	A6	SWPOUT
EXT: T/H-	B5	A5	EXT: T/H+
-8V	B4	A4	-8V
TRIG+	B3	A3	TRIG-
SLZS	B2	A2	NC
NC	B1	A1	XX

P14
TO A28 PERIOD COUNTER

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
PSO	B22	A22	NC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	FV
NC	B12	A12	FR
PLLPC	B11	A11	NC
LOPC	B10	A10	NC
IFPC	B9	A9	NC
RF/TG-PC	B8	A8	NC
IFO	B7	A7	NC
NC	B6	A6	NC
NC	B5	A5	NC
-8V	B4	A4	-8V
NC	B3	A3	NC
SLZS	B2	A2	NC
1MHz	B1	A1	XX

P502
TO A11 YIG OSC

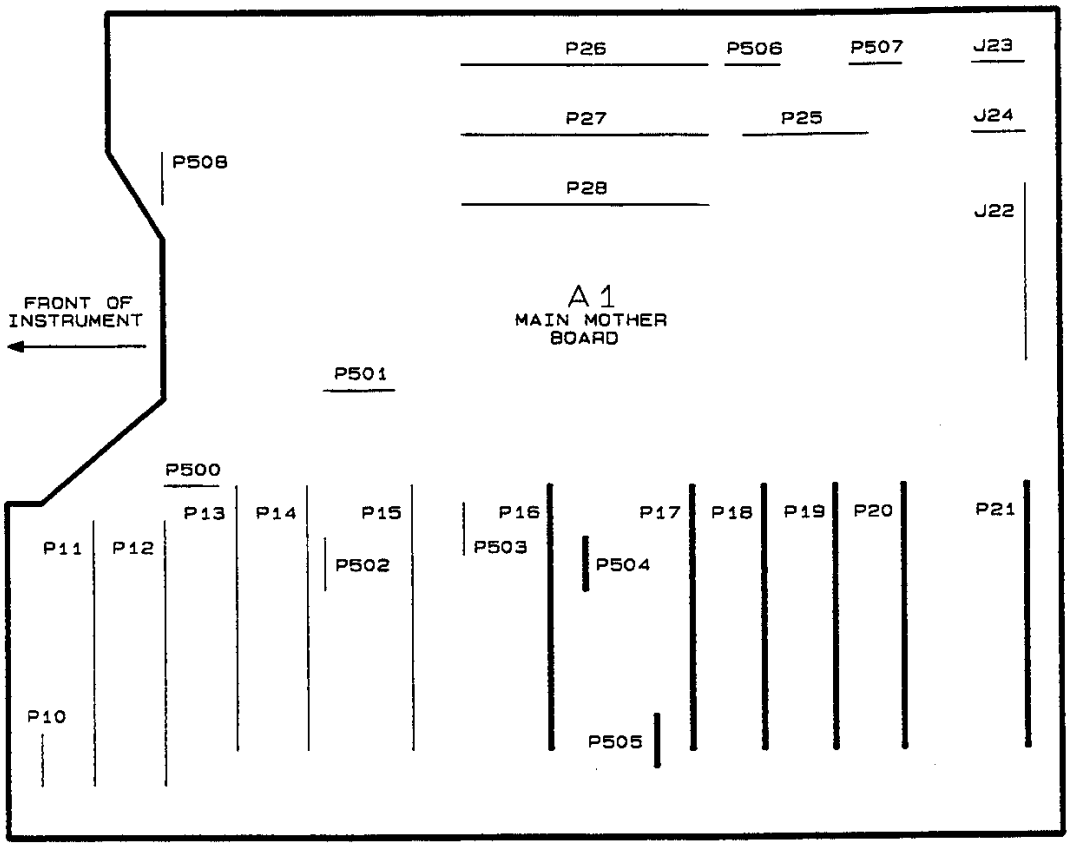
+5VD	A1	B1	LOFLT
NC	A2	B2	NC
+5VA	A3	B3	NC
+15V	A4	B4	-5.2V
GND	A5	B5	+10V
YIGRET	A6	B6	+OSCV
LODR+	A7	B7	LODR-
-15V	A8	B8	-8V
NC	A9	B9	FM-
FM+	A10	B10	GND

P15
TO A31 PHASE LOCK

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	NC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	NC
NC	B12	A12	NC
NC	B11	A11	NC
NC	B10	A10	NC
GND	B9	A9	GND
NC	B8	A8	GND
NC	B7	A7	NC
GND	B6	A6	GND
NC	B5	A5	NC
-8V	B4	A4	-8V
GND	B3	A3	GND
GND	B2	A2	GND
NC	B1	A1	XX

P503
UNUSED

SCL	B1	A1	RES
NC	B2	A2	NC
+15V	B3	A3	SDA
NC	B4	A4	NC
-8V	B5	A5	GND
NC	B6	A6	NC
-15V	B7	A7	+5VA



NOTE: P500 SERIES #'S ARE ON BACK OF BOARD.

FIG. 7-2. MOTHER BOARD CONNECTOR LOCATIONS 2

(6) Sht. 1 of 2

P16
TO A25 LO MODULE

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	LODR+
GND	B24	A24	LODR-
-15V	B23	A23	-15V
NC	B22	A22	NC
FMCSWP	B21	A21	FMCRET
-5.2V	B20	A20	-5.2V
FREQSWP+	B19	A19	FREQSWP-
GND	B18	A18	GND
PSDR+	B17	A17	PSDR-
+10V	B16	A16	+10V
+45V	B15	A15	+45V
EXTPSDR	B14	A14	EXTPSRET
/PLO	B13	A13	FMCRD
NC	B12	A12	NC
NC	B11	A11	NC
LOPC	B10	A10	NC
GND	B9	A9	GND
LOCNT	B8	A8	GND
LOFLT	B7	A7	NC
GND	B6	A6	GND
LOFRQ	B5	A5	LOFRQATN
-8V	B4	A4	-8V
GND	B3	A3	GND
GND	B2	A2	GND
NC	B1	A1	XX

P504
TO A12A5 LOW PASS MIXER

SCL	A1	B1	+5VD
SDA	A2	B2	RES
GND	A3	B3	GND
+5VA	A4	B4	+5VA
+10VREF	A5	B5	+10VRRET
+15V	A6	B6	NC
-15V	A7	B7	-8.2V
NC	A8	B8	PSFLT
GND	A9	B9	GND
+10V	A10	B10	+10V

P505
TO A11A2 YTO DRIVER

+5VD	A1	B1	PSFLT
GND	A2	B2	NC
+5VA	A3	B3	-8V
+15V	A4	B4	-5.2V
+10V	A5	B5	-15V
YIGRET	A6	B6	+MTXV
PSDR+	A7	B7	PSDR-

P17
TO A18 LOG PROCESSOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
OSCL	B30	A30	RES
OSDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	SWPGATE
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
LAVI+	B17	A17	LAVI-
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	NC
SDAH	B12	A12	SDASE
NC	B11	A11	NC
NC	B10	A10	NC
IFPC	B9	A9	DIGCLK
NC	B8	A8	NC
/CLAMP	B7	A7	NC
NC	B6	A6	NC
NC	B5	A5	NC
-8V	B4	A4	-8V
NC	B3	A3	NC
NC	B2	A2	NC
NC	B1	A1	XX

P18
TO A20 VIDEO PROCESSOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	SWEEP+
GND	B24	A24	SWEEP-
-15V	B23	A23	-15V
RCTRIG	B22	A22	SWPGATE
INTV+	B21	A21	INTV-
-5.2V	B20	A20	-5.2V
INTH+	B19	A19	INTH-
GND	B18	A18	GND
LAVI+	B17	A17	LAVI-
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	SDAHSE
SDAH	B12	A12	SDASE
SDAV	B11	A11	NC
NC	B10	A10	NC
ACQCLK	B9	A9	DIGCLK
PSQ	B8	A8	NC
/CLAMP	B7	A7	PEN_IFT
NC	B6	A6	NC
EXTVI+	B5	A5	EXTVI-
-8V	B4	A4	-8V
TRIG+	B3	A3	TRIG-
NC	B2	A2	NC
NC	B1	A1	XX

P19
TO A24 DIGITAL STORAGE

+5VD	B32	A32	+5VD
GND	B31	A31	GND
OSCL	B30	A30	RES
OSDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VRRET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	NC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	SDAHSE
SDAH	B12	A12	SDASE
SDAV	B11	A11	EOC
NC	B10	A10	DIGBLANK
ACQCLK	B9	A9	DIGCLK
NC	B8	A8	DIGCOLOR
NC	B7	A7	/DIGINH
DSZRET	B6	A6	DSZ
DSH	B5	A5	DSHRET
-8V	B4	A4	-8V
DSV	B3	A3	DSVRET
BOD	B2	A2	WBO
NC	B1	A1	XX

P18
TO A20 VIDEO PROCESSOR

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VARET
+15V	B26	A26	+15V
GND	B25	A25	SWEEP+
GND	B24	A24	SWEEP-
-15V	B23	A23	-15V
DTRIG	B22	A22	SWPGATE
INTV+	B21	A21	INTV-
-5.2V	B20	A20	-5.2V
INTH+	B19	A19	INTH-
GND	B18	A18	GND
LAVI+	B17	A17	LAVI-
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	SDAHSE
SDAH	B12	A12	SDASE
SDAV	B11	A11	NC
NC	B10	A10	NC
DCCLK	B9	A9	DIGCLK
PSG	B8	A8	NC
CLAMP	B7	A7	PENLIFT
NC	B6	A6	NC
EXTVI+	B5	A5	EXTVI-
-8V	B4	A4	-8V
TRIG+	B3	A3	TRIG-
NC	B2	A2	NC
NC	B1	A1	XX

P19
TO A24 DIGITAL STORAGE

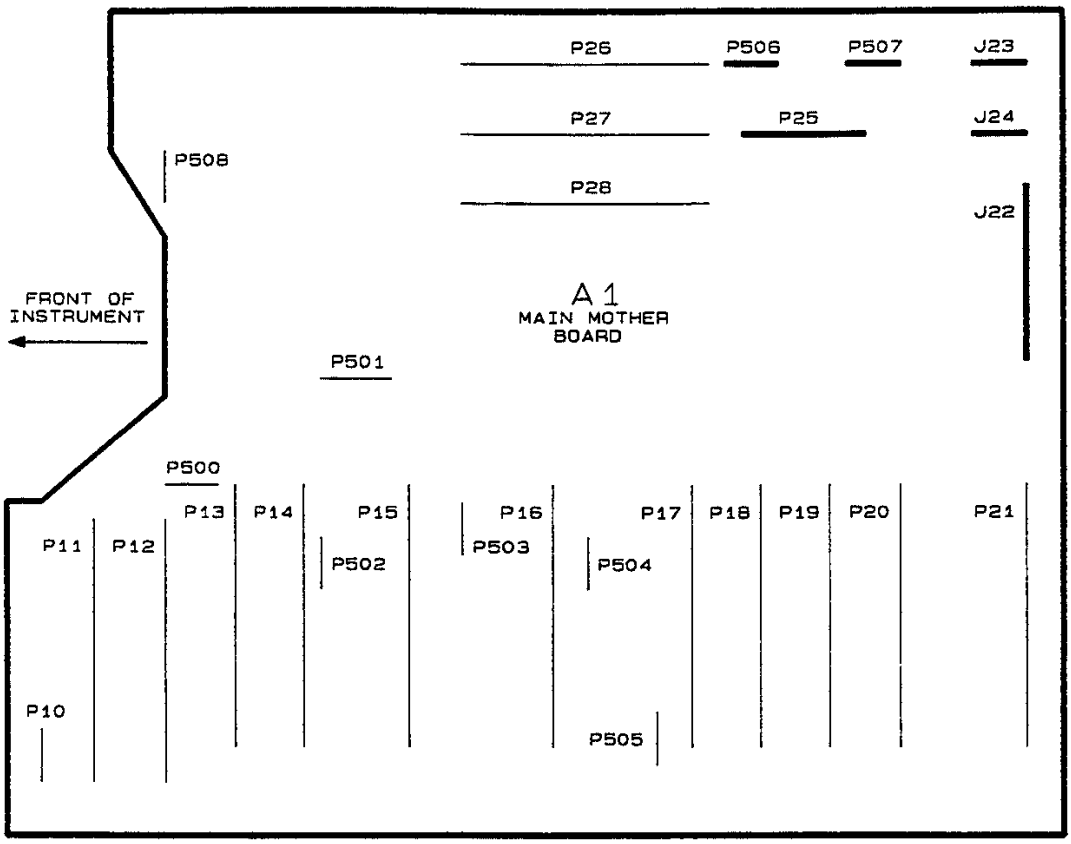
+5VD	B32	A32	+5VD
GND	B31	A31	GND
DSCL	B30	A30	RES
DSDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VARET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
NC	B22	A22	NC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	SDAHSE
SDAH	B12	A12	SDASE
SDAV	B11	A11	EOC
NC	B10	A10	DIGBLANK
ACQCLK	B9	A9	DIGCLK
NC	B8	A8	DIGCOLOR
NC	B7	A7	/DIGINH
DSZRET	B6	A6	DSZ
DSH	B5	A5	DSHRET
-8V	B4	A4	-8V
DSV	B3	A3	DSVRET
BOD	B2	A2	WBO
NC	B1	A1	XX

P20
TO A22 DISPLAY AMPLIFIER

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VARET
+15V	B26	A26	+15V
GND	B25	A25	COLOR+
GND	B24	A24	COLOR-
-15V	B23	A23	-15V
DCFOCRET	B22	A22	DCFOC
INTV+	B21	A21	INTV-
-5.2V	B20	A20	-5.2V
INTH+	B19	A19	INTH-
GND	B18	A18	GND
EXTV+	B17	A17	EXTV-
+10V	B16	A16	+10V
+45V	B15	A15	+45V
EXTH+	B14	A14	EXTH-
EXTVO	B13	A13	EXTHO
ACFOC	B12	A12	EXTZO
ACFOCRET	B11	A11	EOC
HVOFF	B10	A10	DIGBLANK
EXTBLANK	B9	A9	DIGCLK
PSG	B8	A8	DIGCOLOR
/RESET	B7	A7	/DIGINH
DSZRET	B6	A6	DSZ
DSH	B5	A5	DSHRET
-8V	B4	A4	-8V
DSV	B3	A3	DSVRET
BOD	B2	A2	WBO
NC	B1	A1	+95V

P21
TO A23 HIGH VOLTAGE

+5VD	B32	A32	+5VD
GND	B31	A31	GND
SCL	B30	A30	RES
SDA	B29	A29	/SRQ
+5VA	B28	A28	+5VA
+10VREF	B27	A27	+10VARET
+15V	B26	A26	+15V
GND	B25	A25	NC
GND	B24	A24	NC
-15V	B23	A23	-15V
DCFOCRET	B22	A22	DCFOC
NC	B21	A21	NC
-5.2V	B20	A20	-5.2V
NC	B19	A19	NC
GND	B18	A18	GND
NC	B17	A17	NC
+10V	B16	A16	+10V
+45V	B15	A15	+45V
NC	B14	A14	NC
NC	B13	A13	NC
ACFOC	B12	A12	NC
ACFOCRET	B11	A11	NC
HVOFF	B10	A10	NC
NC	B9	A9	NC
NC	B8	A8	NC
/RESET	B7	A7	NC
NC	B6	A6	NC
NC	B5	A5	NC
-8V	B4	A4	-8V
NC	B3	A3	NC
NC	B2	A2	NC
NC	B1	A1	+95V



NOTE: P500 SERIES #'S ARE ON BACK OF BOARD.

FIG. 7-3. MOTHER BOARD CONNECTOR LOCATIONS 3

◇7 Sht. 1 of 2

P506
TO A14 825 MHZ IF

P507
TO A16 VARIABLE RESOLUTION

J23
TO COMM1 REAR PANEL

J24
TO COMM2 REAR PANEL

P25
TO A42 I/O INTERFACE

POWER SUPPLY TEST POINTS

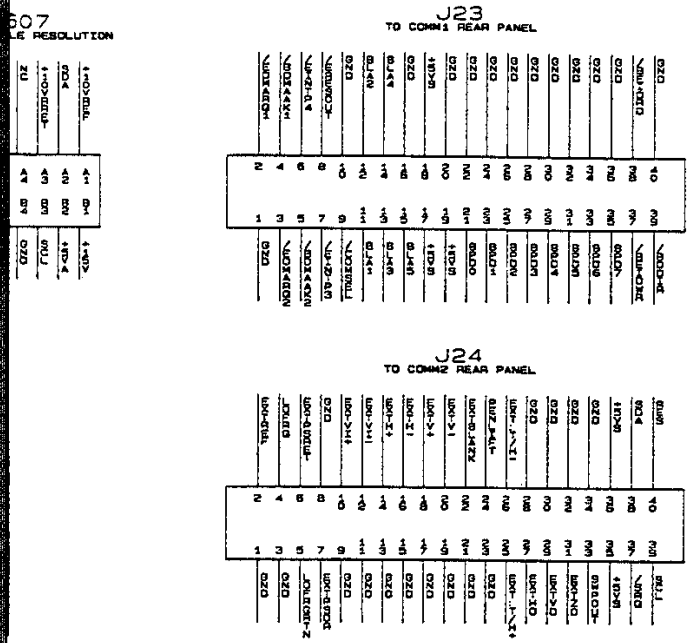
+MTXV
+09CV
+10V
+5VD
+5VS
-8V

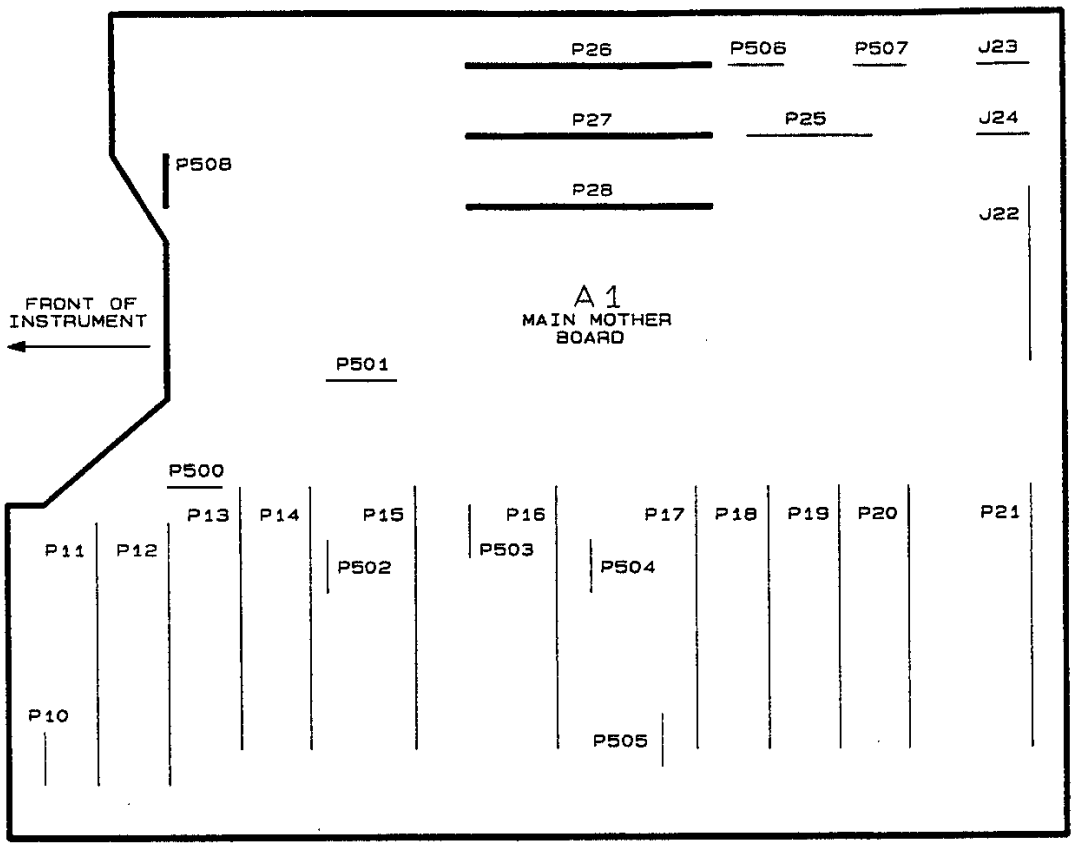
+95V
+45V
+18VS
+15V
+5VA
-5.2V
-15V

J2
POWER

GND	A1
GND	A2
GND	A3
GND	A4
+MTXV	A5
YIGRET	A6
/SPLYON	A7
/ACGONE	A8
LINEV	A9
+15V	A10
+15V	A11
+10V	A12
GND	A13
-5.2V	A14
+5VA	A15
-15V	A16
GND	A17
MTX1	A18
-8V	A19
FAN1	A20
+18VS	A21
+5VD	A22
+5VD	A23
+5VD	A24
+5VD	A25

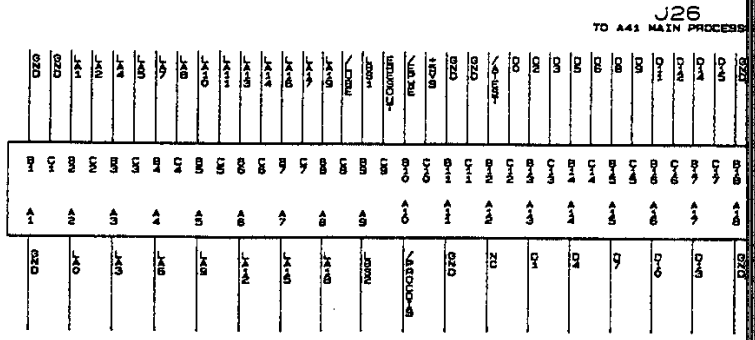
MOTHER BOARD

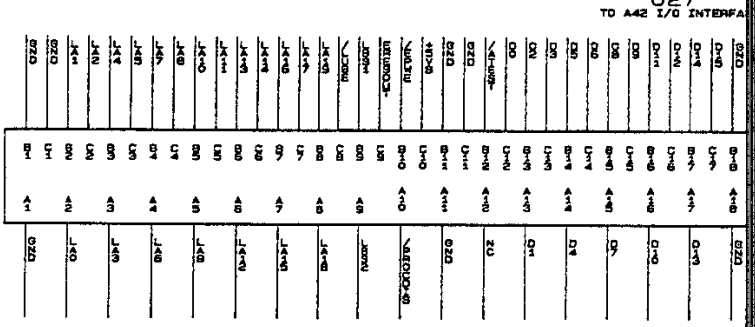

J23
TO COMM1 REAR PANEL
J24
TO COMM2 REAR PANEL
J22
POWER SUPPLY
POWER SUPPLY TEST POINTS
+NTXV
+OSCV
+10V
+5VD
+5VS
-8V
+95V
+45V
+18VS
+15V
+5VA
-5.2V
-15V
GND
-5.2sens
+5Asens
MTX1
MTX2
FAN1
FAN2
OSC1
SPLYFAIL
YIGRET

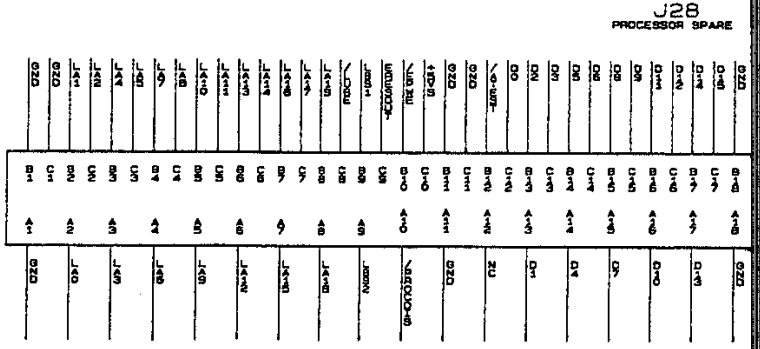


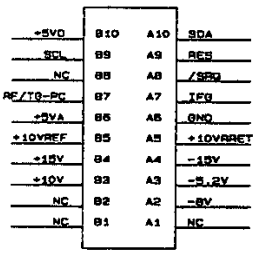
NOTE: P500 SERIES #'S ARE ON BACK OF BOARD.

FIG. 7-4. MOTHER BOARD CONNECTOR LOCATIONS 4

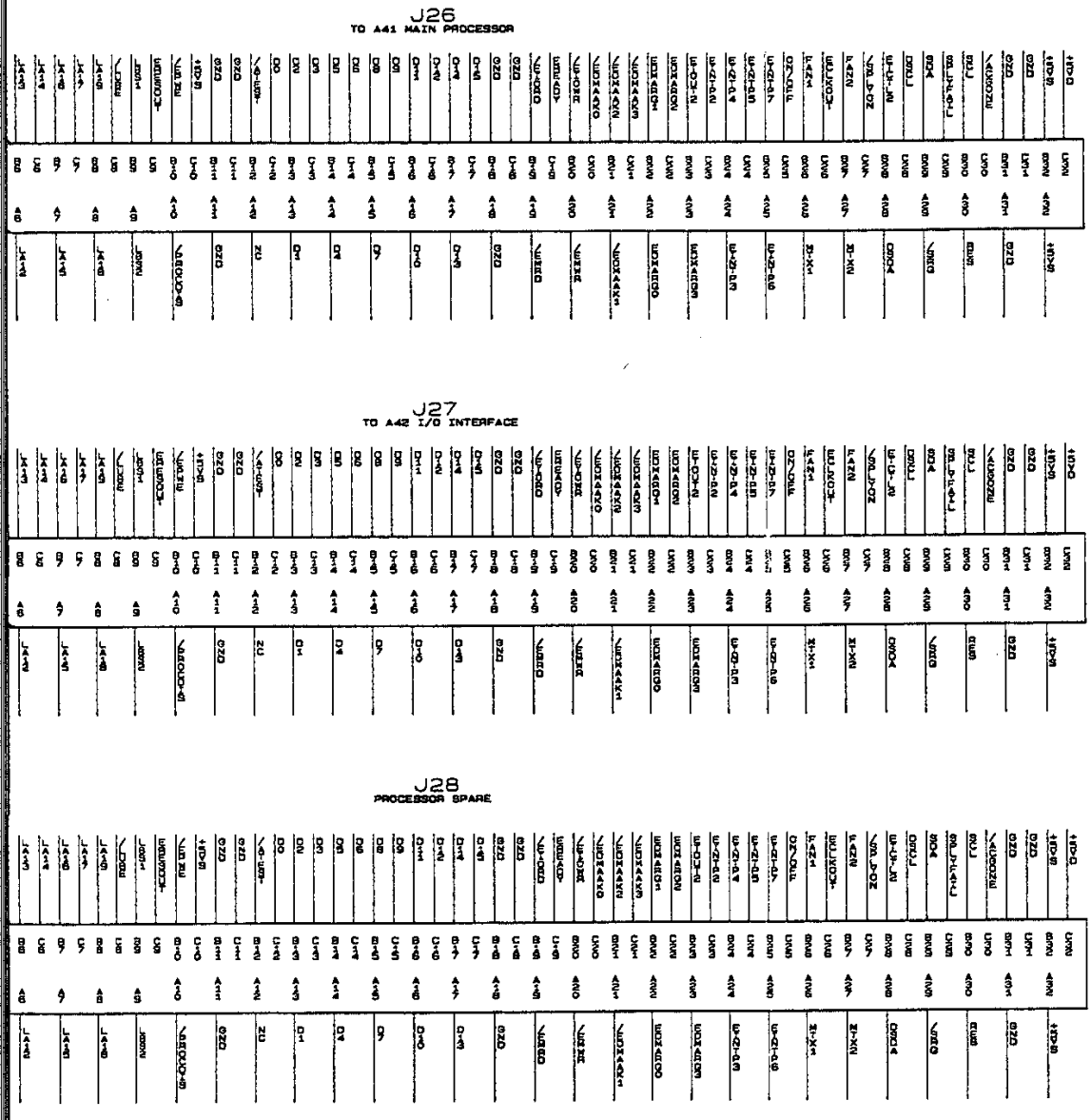

J26
TO A41 MAIN PROCESS


J27
TO A42 I/O INTERFA


J28
PROCESSOR SPARE


P508
TO A15 CALIBRATOR
+5VD
SCL
NC
RF/TG-PC
+5VA
+10VREF
+15V
+10V
NC
NC
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
SDA
RES
/SRQ
IFG
GND
+10VRRET
-15V
-5.2V
-8V
NC

8 Sht. 2 of 2



MOTHER BOARD CONNECTIONS 4

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
        - - - * - - -
  Detail Part of Assembly and/or Component
  Attaching parts for Detail Part
        - - - * - - -
    Parts of Detail Part
    Attaching parts for Parts of Detail Part
        - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC CAMCAR DIV SEMS PRODUCTS UNIT	1818 CHRISTINA ST	ROCKFORD IL 61108
09772	WEST COAST LOCKWASHER CO INC	16730 E JOHNSON DRIVE P O BOX 3588	CITY OF INDUSTRY CA 91744
12327	FREEWAY CORP	9301 ALLEN DR	CLEVELAND OH 44125-4632
16428	COOPER BELDEN ELECTRONIC WIRE AND CA SUB OF COOPER INDUSTRIES INC		
18565	CHOMERICS INC	77 DRAGON COURT	WOBURN MA 01801-1039
19505	APPLIED ENGINEERING PRODUCTS	1475 WHALLEY AVE PO BOX A-D	NEW HAVEN CT 06525
24931	SPECIALTY CONNECTOR CO INC	2100 EARLYWOOD DR PO BOX 547	FRANKLIN IN 46131
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
53217	TECHNICAL WIRE PRODUCTS INC DBA TECKNIT INC	320 N NOPAL ST	SANTA BARBARA CA 93103-3225
70903	COOPER BELDEN ELECTRONICS WIRE AND C SUB OF COOPER INDUSTRIES INC		
71400	BUSSMANN DIV OF COOPER INDUSTRIES INC	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
72228	AMCA INTERNATIONAL CORP CONTINENTAL SCREW CO DIV	459 MT PLEASANT	NEW BEDFORD MA 02742
73743	FISCHER SPECIAL MFG CO	111 INDUSTRIAL RD	COLD SPRING KY 41076-9749
77900	ILLINOIS TOOL WORKS SHAKEPROOF DIV	ST CHARLES RD	ELGIN IL 60120
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIV	ST CHARLES ROAD	ELGIN IL 60120
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
83385	MICRODOT MFG INC GREER-CENTRAL DIV	3221 W BIG BEAVER RD	TROY MI 48098
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
93459	WEINSCHEL ENGINEERING CO INC	1 WEINSCHEL LANE	GAITHERSBURG MD 20877
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61108-5181
98291	SEALECTRO CORP BICC ELECTRONICS	40 LINDEMAN DR	TURNBULL CT 06611-4739
S3109	FELLER	72 Veronica Ave Unit 4	Summerset NJ 08873
TK0433	PORTLAND SCREW CO		
TK0858	STAUFFER SUPPLY CO (DIST)		
TK1302	MOUNTAIN MOLDING	606 SECOND STREET	BERTHOUD CO 80513
TK1312	LEMO USA INC	335 TESCONI CIR PO BOX 11006	SANTA ROSA CA 95406
TK1375	ESAM		
TK1543	CAMCAR/TEXTRON	600 18TH AVE	ROCKFORD IL 61108-5181

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	200-3475-00			1	COVER,FRONT:POLYCARBONATE	80009	200-3475-00
-2	348-1011-00			4	FOOT,CABINET:TOP	80009	348-1011-00
					(ATTACHING PARTS)		
-3	211-0674-00			4	SCREW,MACHINE:6-32 X 0.312,TRH,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-4	386-5719-00			4	PLATE,FOOT:TOP,ALUMINUM	80009	386-5719-00
-5	348-1012-00			4	FOOT,CABINET:BOTTOM	80009	348-1012-00
					(ATTACHING PARTS)		
-6	211-0674-00			4	SCREW,MACHINE:6-32 X 0.312,TRH,STL	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	386-5718-00			4	PLATE,FOOT:BOTTOM,ALUMINUM	80009	386-5718-00
-8	366-0579-00			2	PUSH BUTTON:ALUMINUM	80009	366-0579-00
-9	129-1108-00			2	SPACER,POST:0.1 L,6-32 THD BOTH ENDS,PLSTC	80009	129-1108-00
-10	367-0384-00			1	HANDLE ASSEMBLY:PLASTIC/ALUMINUM/RUBBER	80009	367-0384-00
					(ATTACHING PARTS)		
-11	212-0560-00			6	SCREW,MACHINE:10-32 X 0.312,FLH,100 DEG	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-12	380-0668-00			2	HOUSING,INDEX:	80009	380-0668-00
					(ATTACHING PARTS)		
-13	213-0858-00			8	SCREW,TPG,TR:6-32 X 0.5 L,TAPTITE,FLH	83385	ORDER BY DESCR
					(END ATTACHING PARTS)		
-14	386-5625-00			2	PLATE,HANDLE:ALUMINUM	80009	386-5625-00
-15	200-2694-00			2	COVER,INDEX:ALUMINUM	80009	200-2694-00
					(ATTACHING PARTS)		
-16	213-0918-00			6	SCREW,TPG,TR:8-32 X 0.625,FLH,82 DEG,POZ	72228	ORDER BY DESCR
					(END ATTACHING PARTS)		
-17	214-3200-00			2	SPRING,HLCPS:0.798 OD X 1.1 L,CLE,MUW	80009	214-3200-00
-18	105-0893-00			2	INDEX RLSE,HDL:	80009	105-0893-00
-19	105-0894-00			2	INDEX STOP,HDL:	80009	105-0894-00
-20	214-3198-00			2	INDEX,HANDLE:	80009	214-3198-00
-21	200-3624-01			1	COVER,REAR:POLYCARBONATE	80009	200-3624-01
-22	348-1017-00			2	FOOT,CABINET:REAR	80009	348-1017-00
					(ATTACHING PARTS)		
-23	212-0630-01			4	SCREW,SPCL MACH:10-24 X 1.55 L,FLH,45 DEG	TK0858	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	426-2220-01	B020000	B020254	1	FRAME,REAR:ALUMINUM	80009	426-2220-01
	426-2220-02	B020255		1	FRAME,REAR:ALUMINUM	80009	426-2220-02
					(2782 ONLY)		
	426-2220-02	B010100		1	FRAME,REAR:ALUMINUM	80009	426-2220-02
					(2784 ONLY)		
-25	334-7025-00	B020000	B020387	1	MARKER,IDENT:MKD 2782 SPECTRUM ANALYZER	80009	334-7025-00
	334-8349-00	B020388		1	MARKER,IDENT:MKD 2784	80009	334-8349-00
					(2782 ONLY)		
	334-8349-00	B010100		1	MARKER,IDENT:MKD 2784	80009	334-8349-00
					(2784 ONLY)		
-26	334-7700-00			1	MARKER,IDENT:MKD CAUTION	80009	334-7700-00
-27	437-0355-00			1	CABINET,SA:	80009	437-0355-00

Fig. 1
Sht. 1 of 2

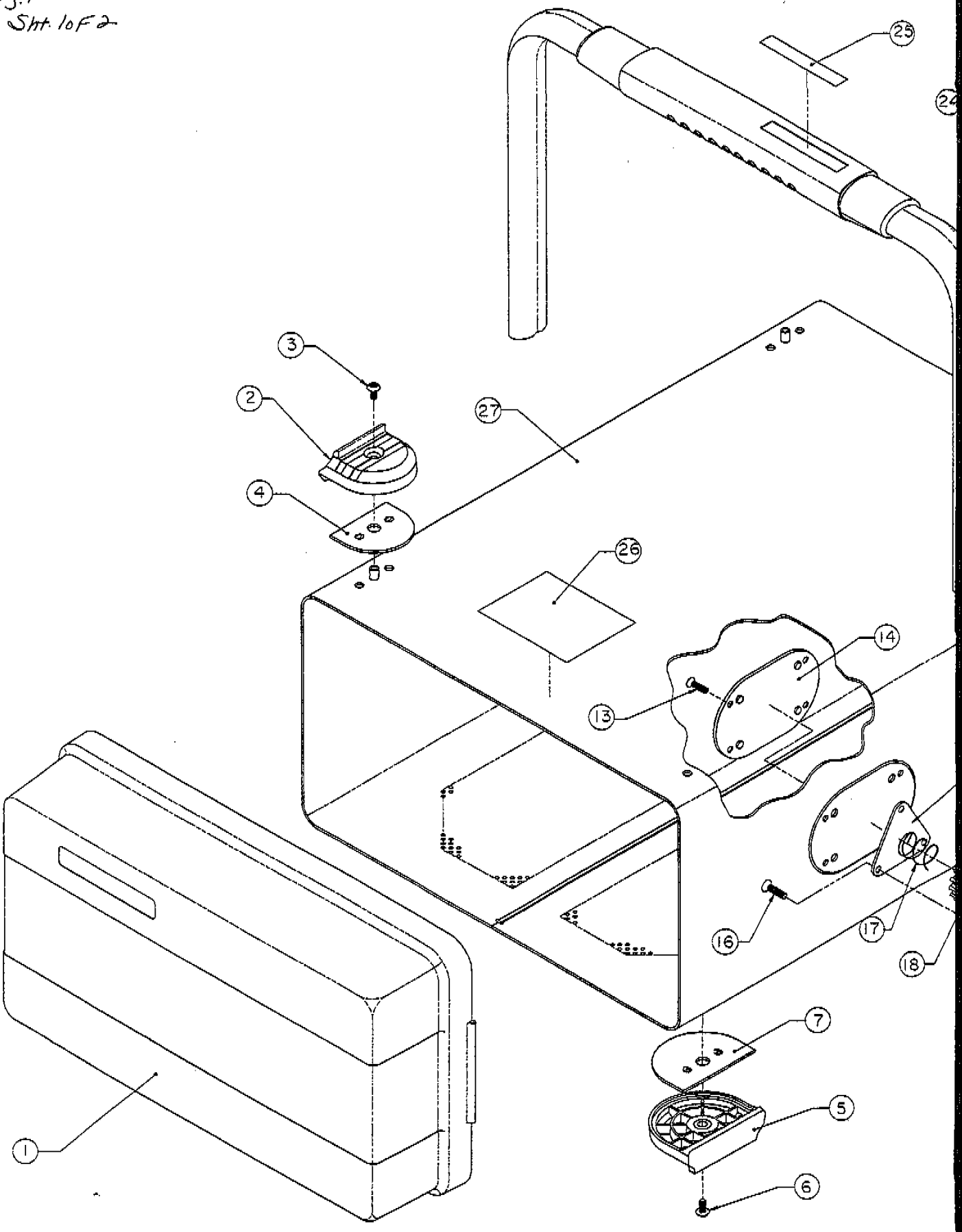


Fig. 1
Sht. 2 of 2

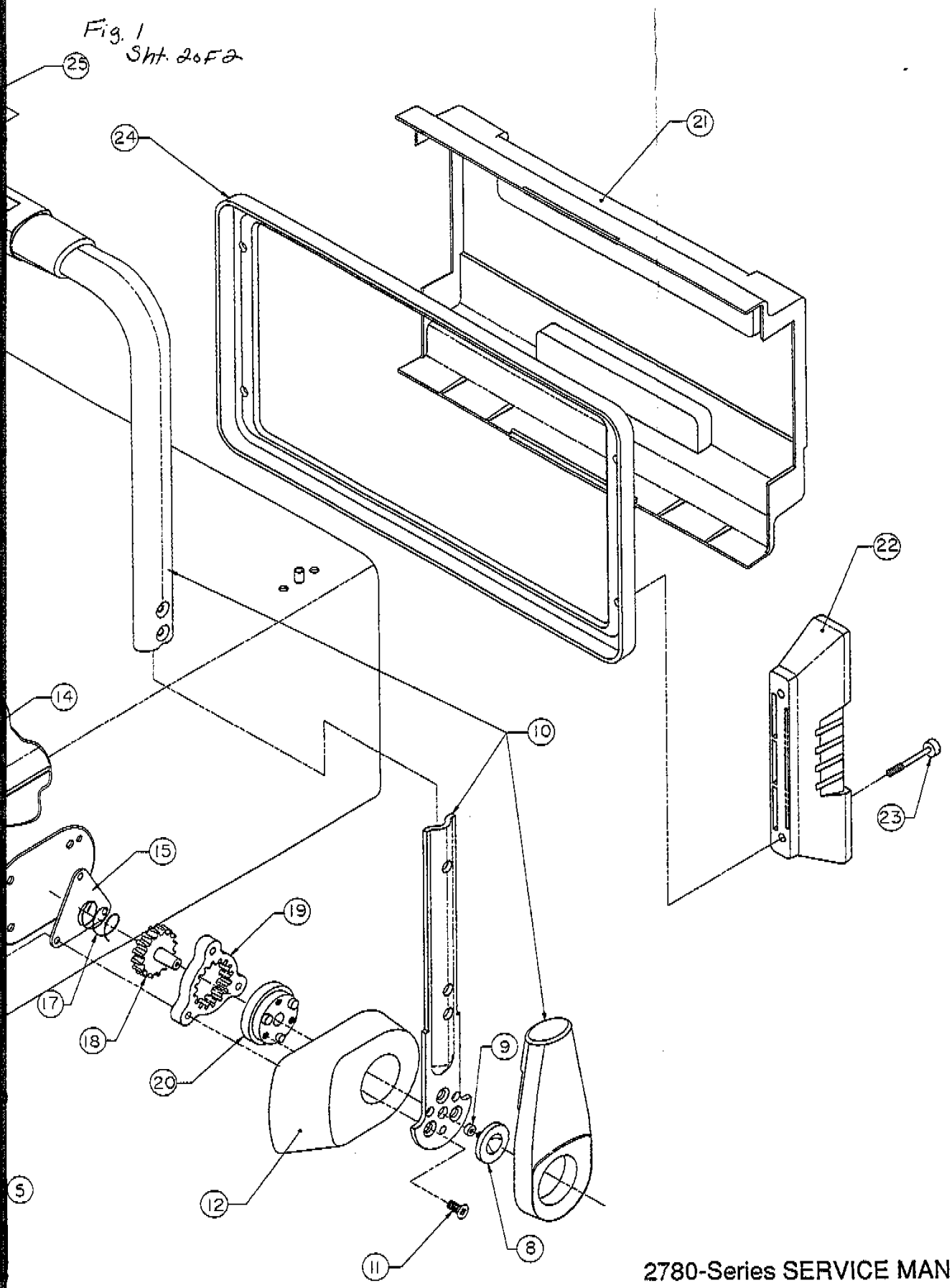
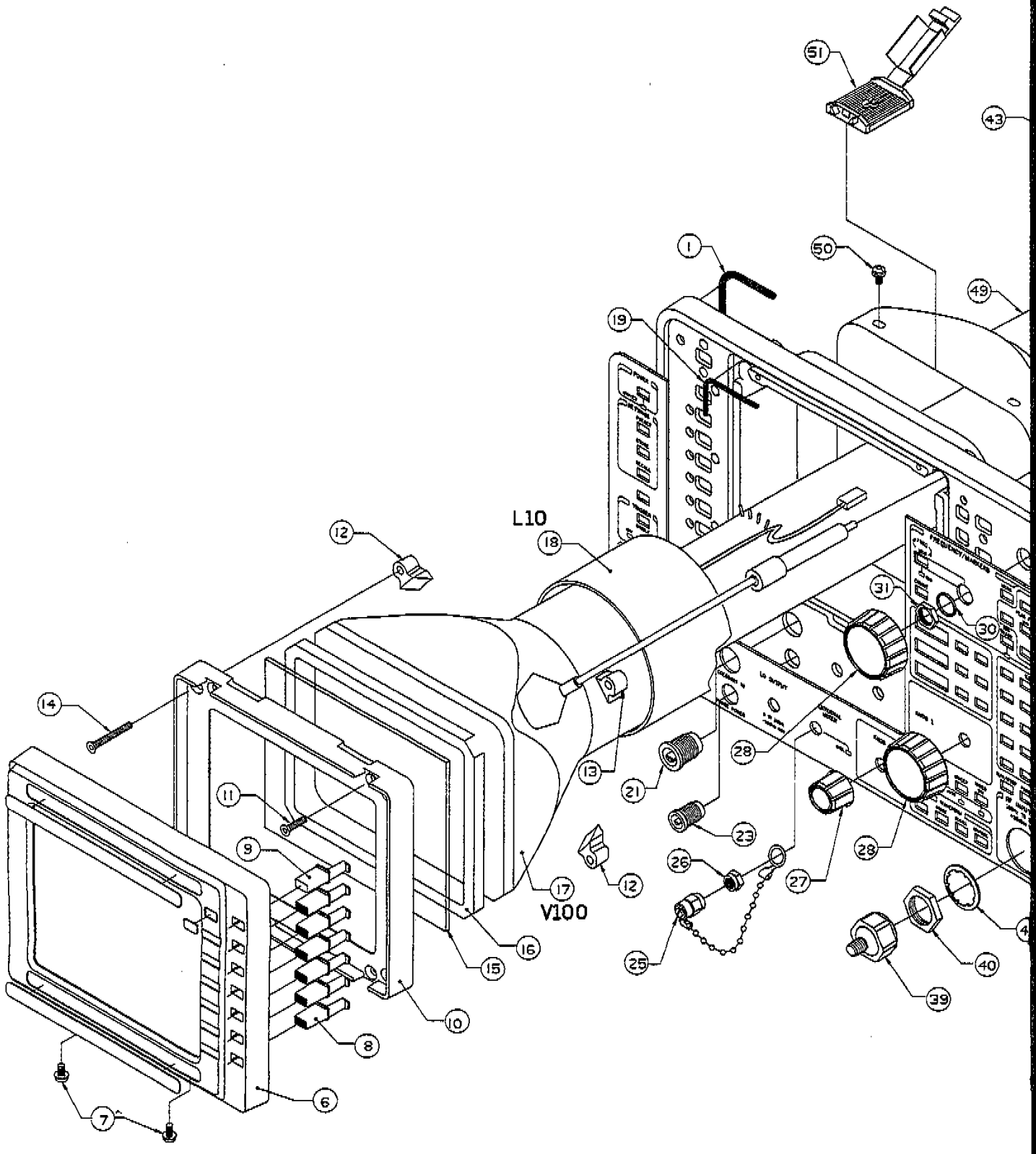


FIG. 1 CABINET ASSY.

Fig. 2
Sht. 1 of 2



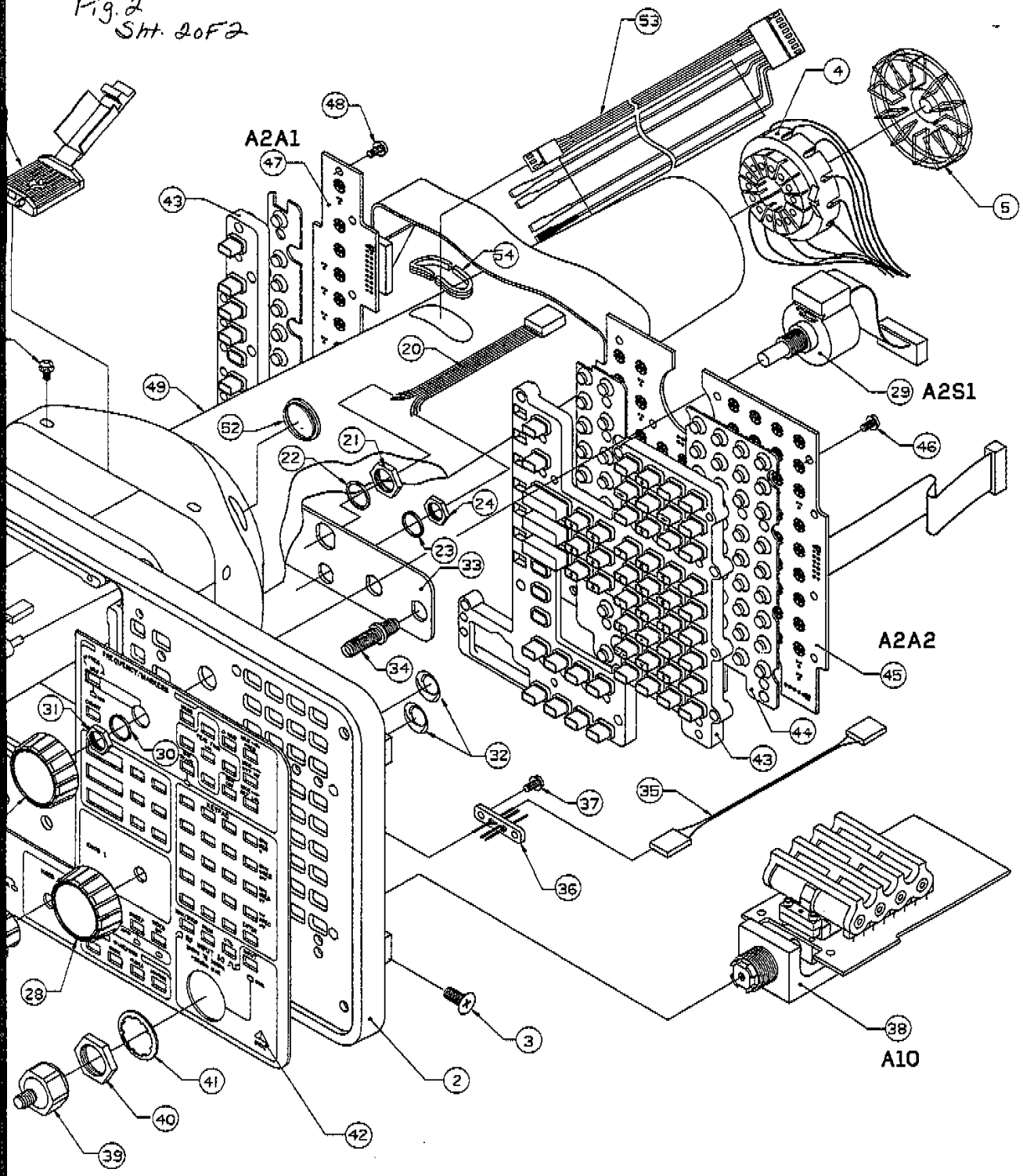


FIG. 2 FRONT PANEL AND CRT

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	337-0925-04	B020000	B020266	1	SHLD GSKT,ELEK:37.0 L	TK1375	ORDER BY DESCR
	337-0925-02	B020267		1	SHLD GSKT,ELEK:BULK (2782 ONLY)	53217	21-00352
	337-0925-02	B010100		1	SHLD GSKT,ELEK:BULK (2784 ONLY)	53217	21-00352
-2	386-5381-00	B020000	B020254	1	SUBPANEL,FRONT:	80009	386-5381-00
	386-5381-01	B020255		1	SUBPANEL,FRONT:2782 (2782 ONLY)	80009	386-5381-01
	386-5381-01	B010100		1	SUBPANEL,FRONT:2782 (2784 ONLY)	80009	386-5381-01
					(ATTACHING PARTS)		
-3	212-0650-00			4	SCREW,MACHINE:10-32 X 0.437,FLH,100 DEG,SST	83486	ORDER BY DESCR
					(END ATTACHING PARTS)		
-4	136-0935-00			1	SKT,PL-IN ELEK:ELECTRON TUBE,W/LEADS	80009	136-0935-00
-5	200-0917-01			1	COVER,CRT SKT:2.052 OD X 0.291 H,PLASTIC	80009	200-0917-01
-6	----- -----			1	COLOR SHUTTER A:RED/GREEN 5 INCH DIAGONAL (SEE A4 REPL)		
					(ATTACHING PARTS)		
-7	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-8	366-0609-00			6	PUSH BUTTON:MENU	80009	366-0609-00
-9	366-0730-00			1	KEYCAP:MENU APPEARANCE BEZEL	80009	366-0730-00
-10	426-2129-00			1	FRAME,CRT:	80009	426-2129-00
					(ATTACHING PARTS)		
-11	211-0777-00			4	SCREW,MACHINE:6-32 X 0.5,FH TORX	80009	211-0777-00
					(END ATTACHING PARTS)		
-12	343-1354-00			2	RETAINER,CRT:LOWER RIGHT,UPPER LEFT,PLASTIC	80009	343-1354-00
-13	343-1355-00			2	RETAINER,CRT:UPPER RIGHT,LOWER LEFT,PLASTIC	80009	343-1355-00
					(ATTACHING PARTS)		
-14	211-0778-00			4	SCREW,MACHINE:6-32 X 1.0,FH TORX	80009	211-0778-00
					(END ATTACHING PARTS)		
-15	331-0492-00			1	WINDOW,CRT:EMI,OPTICAL POLYCARBONATE	80009	331-0492-00
-16	361-1537-00			1	SHIM:0.25 THK X 3.39 X 4.24,MYLAR	80009	361-1537-00
-17	----- -----			1	ELECTRON TUBE:FINISHED(SEE V100 REPL)		
-18	----- -----			1	COIL,TUBE DEFL:FXD,TRACE ROTATOR (SEE L10 REPL)		
-19	348-1016-00			1	GASKET,RF:CRT FRAME,0.1 DIA	80009	348-1016-00
-20	174-0359-00			1	CA ASSY,SP,ELEC:8,26 AWG,5.0 L	80009	174-0359-00
-21	131-1011-00			1	CONN,CIRC::PNL,LEMO;4 POS,2 MALE,2 FEMALE,1 7.5 MM L,10 MM DIA,M9X0.6 THD,SLDR CUP;,,	TK1312	ERA.0S.304.CNL
					(ATTACHING PARTS)		
-22	210-0021-00			1	WASHER,LOCK:0.476 ID,INTL,0.018 THK,STL	78189	1222-01
					(END ATTACHING PARTS)		
-23	131-0771-00			1	CONN,CIRC::	80009	131-0771-00
					(ATTACHING PARTS)		
-24	220-0551-00			1	NUT,PLAIN,HEX:9 MM X 1.00,BRS NP	73743	ORDER BY DESCR
					(END ATTACHING PARTS)		
-25	----- -----			2	TERMN,COAXIAL:(SEE P16,P18 REPL)		
					(ATTACHING PARTS)		
-26	220-0531-02			3	NUT,PLAIN,HEX:0.25-36 X 0.312 HEX,BRS NP	80009	220-0531-02
	210-0940-00			1	WASHER,FLAT:0.25 ID X 0.375 OD X 0.02,STL	12327	ORDER BY DESCR
					(END ATTACHING PARTS)		
-27	366-0670-00			1	SHELL,KNOB:SILVER GRAY	80009	366-0670-00
-28	366-0685-00			2	SHELL,KNOB:SILVER GRAY	80009	366-0685-00
-29	260-2412-00			1	SWITCH ASSEMBLY:OPTICAL,ROTARY,256 POS	50434	QEDS-7189
					(ATTACHING PARTS)		
-30	210-0590-00			1	NUT,PLAIN,HEX:0.375-32 X 0.438 BRS CD PL	73743	28269-402
-31	210-0012-00			1	WASHER,LOCK:0.384 ID,INTL,0.022 THK,STL	09772	ORDER BY DESCR
					(END ATTACHING PARTS)		
-32	214-2617-00			2	SPRING,GROUND:0.248 ID,COPPER BERYLLIUM	80009	214-2617-00
-33	386-5824-01			1	PLATE,CONNECTOR:ALUMINUM	80009	386-5824-01
-34	131-2343-00			3	CONN,JACK,RF::	80009	131-2343-00
-35	174-0381-00			1	CA ASSY,SP,ELEC:2,26 AWG,4.0 L,RIBBON	80009	174-0381-00
-36	119-3557-00			1	FILTER ASSEMBLY:FRONT PANEL	80009	119-3557-00
					(ATTACHING PARTS)		
-37	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-38	----- -----			1	ATTENUATOR:33GHZ-70DB(SEE A10 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-					(ATTACHING PARTS)		
-39	131-4328-00			1	CONN,RCPT,ELEC:ADAPT,SMA FEMALE TO PLANAR C ROWN,0.810 L	80009	131-4328-00
-40	210-0579-00			1	NUT,PLAIN,HEX:0.625-24 X 0.75,BRS CD PL	73743	48046-402
-41	210-0049-00			1	WASHER,LOCK:0.65 ID INTL,0.022 THK,STL	77900	128-02-00-0541C
					(END ATTACHING PARTS)		
-42	333-3313-00	B020000	B020255	1	PANEL,FRONT:	80009	333-3313-00
	333-3313-01	B020256	B020412	1	PANEL,FRONT:2782	80009	333-3313-01
	333-3313-02	B020413		1	PANEL,FRONT:2782 (2782 ONLY)	80009	333-3313-02
	333-3313-02	B010100		1	PANEL,FRONT:2782 (2784 ONLY)	80009	333-3313-02
-43	260-2317-00	B020000	B020358	1	SWITCH ASSEMBLY:W/2 BEZELS	80009	260-2317-00
	366-0746-00	B020359		1	PUSH BUTTON AS:FRONT PANEL (2782 ONLY)	80009	366-0746-00
	366-0746-00	B010100		1	PUSH BUTTON AS:FRONT PANEL (2784 ONLY)	80009	366-0746-00
-44	260-2461-00			1	SWITCH ASSEMBLY:ELASTOMER KEYPAD	80009	260-2461-00
-45	----- -----			1	CKT BOARD ASSY:FRONT PANEL #2 (SEE A2A2 REPL)		
					(ATTACHING PARTS)		
-46	211-0408-00			14	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-47	----- -----			1	CKT BOARD ASSY:FRONT PANEL #1 (SEE A2A1 REPL)		
					(ATTACHING PARTS)		
-48	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-49	337-3308-00			1	SHIELD,CRT:	80009	337-3308-00
					(ATTACHING PARTS)		
-50	211-0408-00			3	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
	211-0324-00			1	SCR,ASSEM WSHR:4-40 X 0.188,PNH,T9 TORX DR	01536	829-06780-024
					(END ATTACHING PARTS)		
-51	343-1370-00			1	CLAMP,CABLE:1.27 L,PLASTIC	80009	343-1370-00
-52	348-0762-00			1	GROMMET,PLASTIC:NATURAL,ROUND,0.54 ID	TK1302	ORDER BY DESCR
-53	174-0382-00			1	CA ASSY,SP,ELEC:7,26 AWG,10.75 L,RIBBON	80009	174-0382-00
-54	348-0085-00			2	GROMMET,PLASTIC:GRAY,U-SHAPE,0.48 ID	80009	348-0085-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
3-	----- -----			1	POWER SUPPLY:(SEE A5 REPL) (ATTACHING PARTS)		
-1	212-0650-00			4	SCREW,MACHINE:10-32 X 0.437,FLH,100 DEG,SST	83486	ORDER BY DESCR
-2	211-0734-00			3	SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL (END ATTACHING PARTS)	83486	ORDER BY DESCR
					POWER SUPPLY INCLUDES:		
-3	426-2148-00			1	.FRAME SECTION:REAR PANEL	80009	426-2148-00
-4	334-6977-00			1	.MARKER,IDENT:POLYCARBONATE FILM,REAR PNL,LO .WER	80009	334-6977-00
-5	----- -----			1	.CKT BD ASSY:REAR PANEL BNC(SEE A5A7 REPL) (ATTACHING PARTS)		
-6	220-0497-00			5	.NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
-7	210-1039-00			5	.WASHER,LOCK:0.521 ID,INT,0.025 THK,SST (END ATTACHING PARTS)	24931	ORDER BY DESCR
-8	334-6978-00			1	.MARKER,IDENT:POLYCARBONATE FILM,REAR PNL,UP .PER	80009	334-6978-00
-9	----- -----			1	.CABLE ASSY,RF(SEE A5W516 REPL)		
-10	131-4293-00			1	.CONN,RCPT,ELEC:PANEL MOUNT,SMB	98291	51-075-0000
-11	----- -----			1	.CKT BD ASSY:COMM INTERFACE(SEE A5A6 REPL) (ATTACHING PARTS)		
-12	020-1612-00			2	.ACCESSORY KIT:W/BRACKET & SCREWS	00779	553638-2
-13	131-0890-01			4	.LOCK,CONNECTOR:4-40 X 0.312 L,HEX HD,STL	00779	205818-2
-14	211-0408-00			2	.SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX (END ATTACHING PARTS)	93907	ORDER BY DESCR
-15	342-0891-00	B020000	B020293	1	.INSULATOR:POWER SUPPLY	80009	342-0891-00
	342-0891-01	B020294		1	.INSULATOR:POWER SUPPLY .(2782 ONLY)	80009	342-0891-01
	342-0891-01	B010100		1	.INSULATOR:POWER SUPPLY .(2784 ONLY)	80009	342-0891-01
-16	----- -----			1	.FILTER ASSY:EMI(SEE A5FL500 REPL) (ATTACHING PARTS)		
-17	211-0409-00			2	.SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
-18	210-0457-00			1	.NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL (END ATTACHING PARTS)	78189	511-061800-00
-19	342-0798-00			1	.INSUL,PWR SPLY:POLYESTER	80009	342-0798-00
-20	----- -----			1	.CKT BD ASSY:PRIMARY POWER SUPPLY .(SEE A5A1 REPL) (ATTACHING PARTS)		
-21	211-0302-00			7	.SCR,ASSEM WSHR:4-40 X 0.75,PNH,STL,TORX DR (END ATTACHING PARTS)	01536	ORDER BY DESCR
-22	----- -----			1	.CKT BD ASSY:SECONDARY POWER SUPPLY .(SEE A5A2 REPL) (ATTACHING PARTS)		
-23	211-0408-00			4	.SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX (END ATTACHING PARTS)	93907	ORDER BY DESCR
-24	----- -----			1	.FAN,TUBEAXIAL:(SEE A5B100 REPL) (ATTACHING PARTS)		
-25	211-0702-00			4	.SCREW,CAP:6-32 X 0.375,HEX SKT,SST	TK0433	ORDER BY DESCR
-26	211-0711-00			3	.SCR,ASSEM WSHR:6-32 X 0.25,PNH,STL,TORX,T15 (END ATTACHING PARTS)	01536	ORDER BY DESCR
-27	378-2049-01			1	.GRILLE,FAN:3.07 DIA,2782	80009	378-2049-01
-28	348-1157-00			1	.GROMMET:SHOCK MOUNT,2782	80009	348-1157-00
-29	441-1735-02			1	CHAS,PWR SPLY:ALUMINUM,2782 (ATTACHING PARTS)	80009	441-1735-02
-30	211-0734-00			4	.SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL (END ATTACHING PARTS)	83486	ORDER BY DESCR

Fig. 3
Sht. 1 of 2

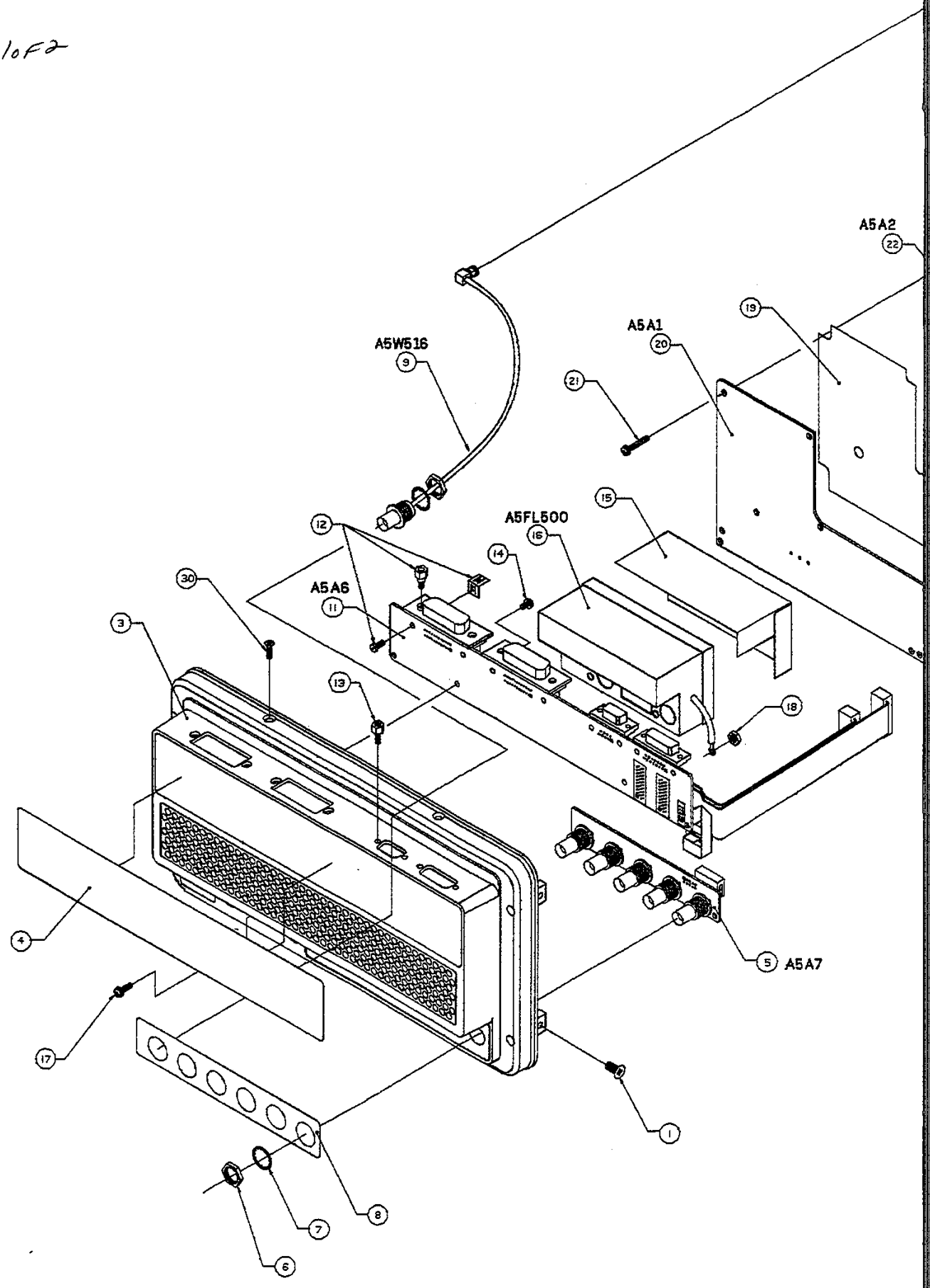
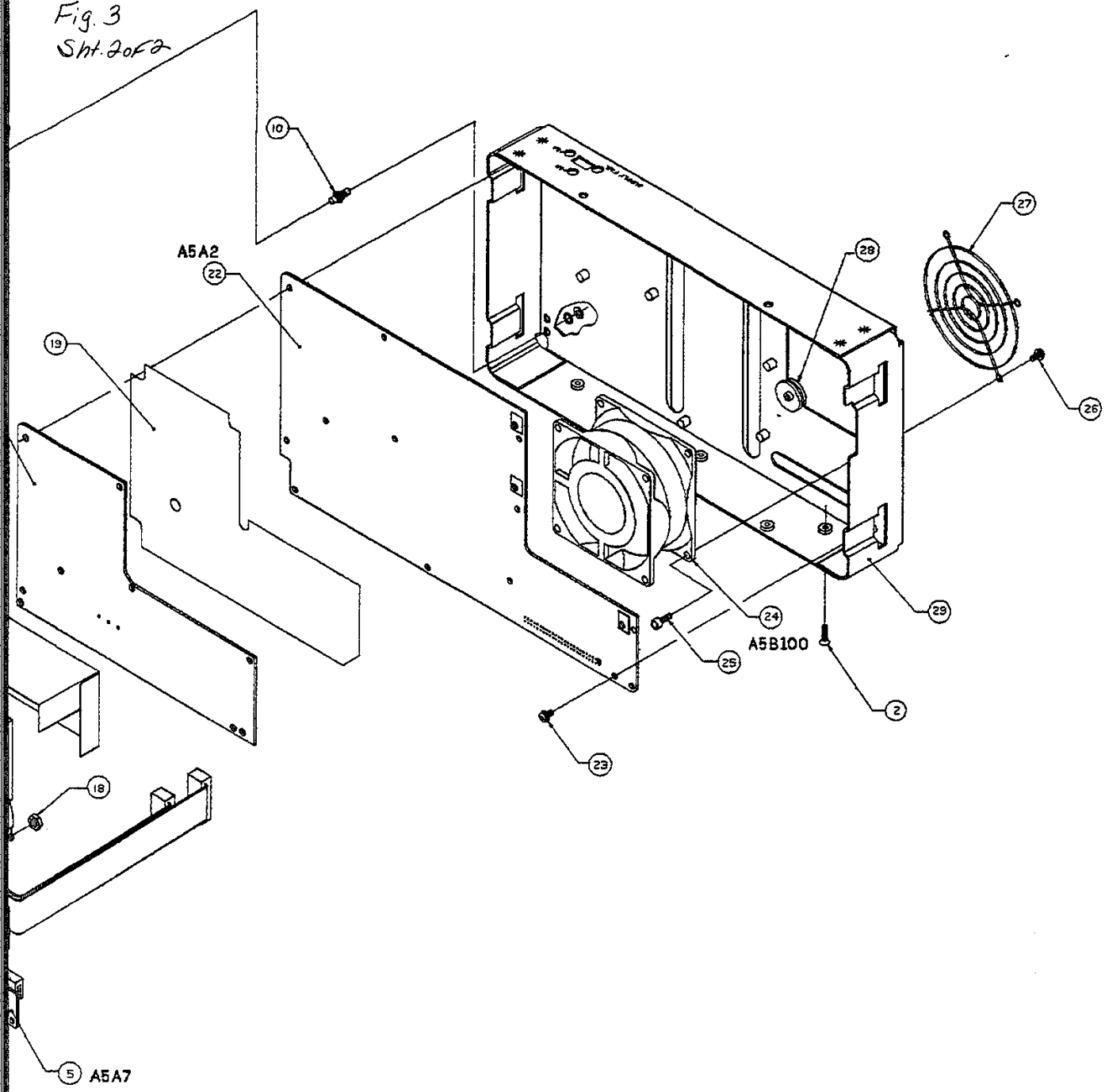


Fig. 3
Sht. 2 of 2



2780-Series SERVICE MANUAL
FIG. 3 POWER SUPPLY ASSY

Fig. 4
Sht. 1 of 2

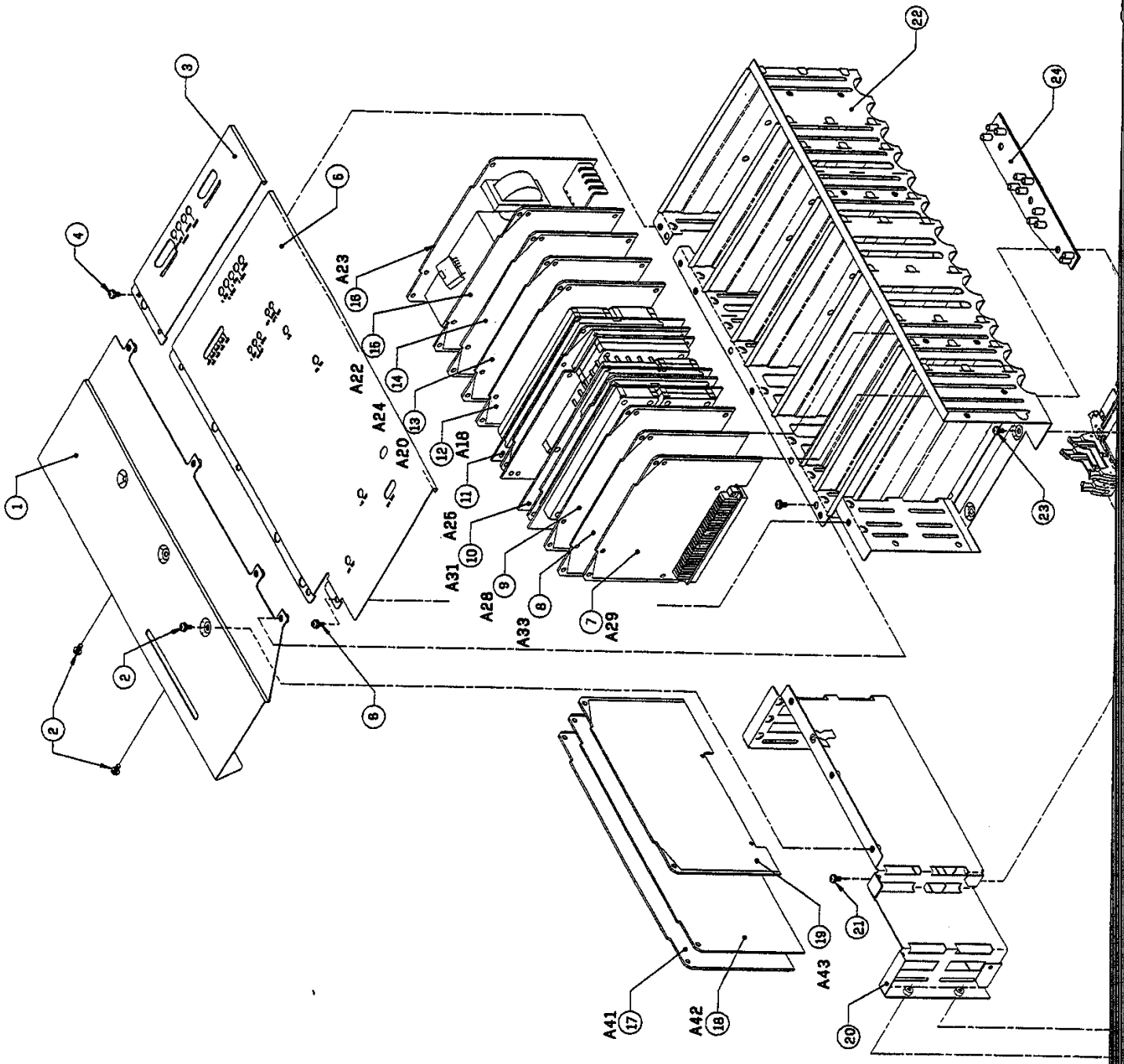


Fig. 4
Sht. 2 of 2

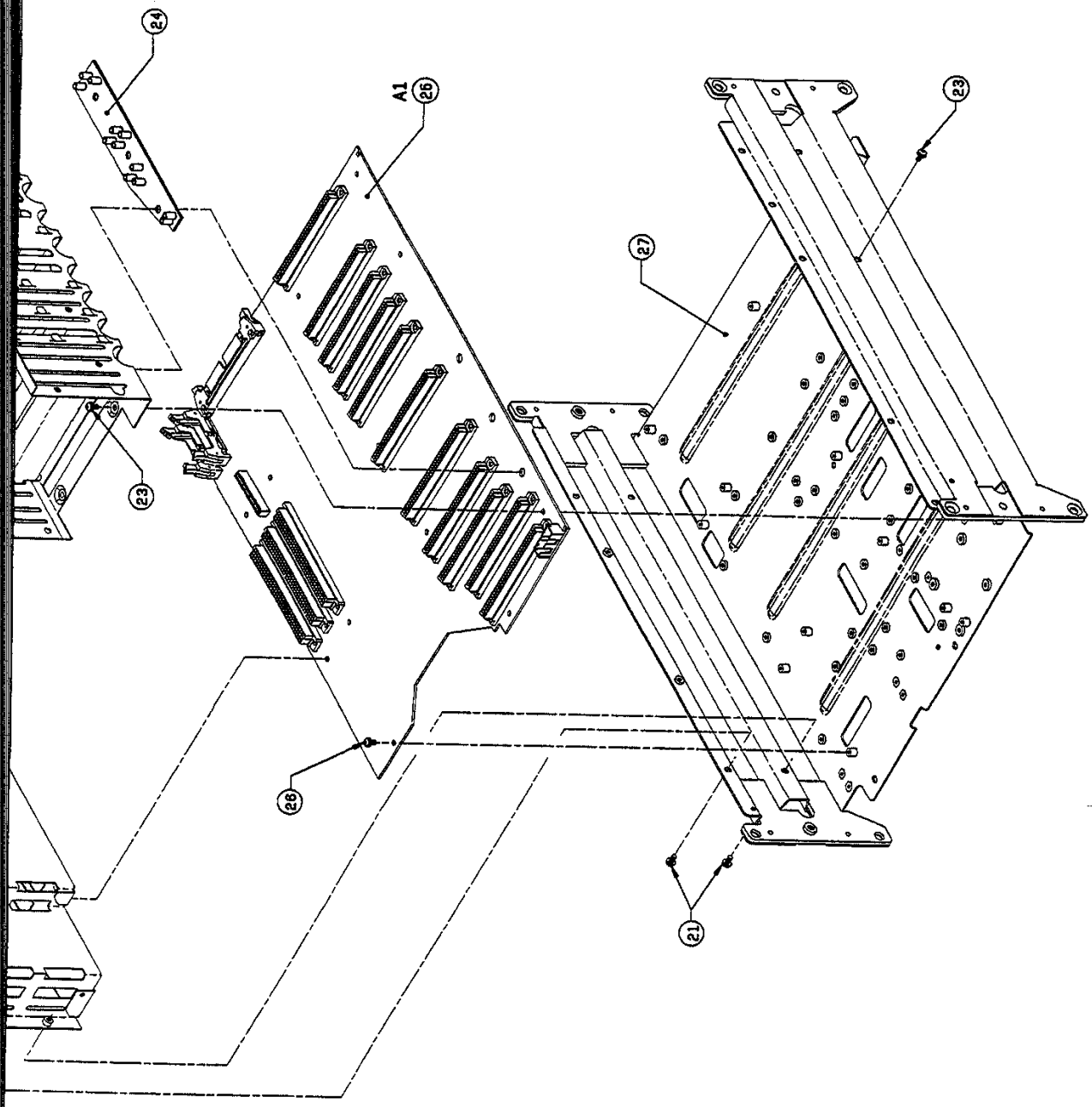


FIG. 4 CHASSIS (TOP)

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
4-1	200-3438-01			1	COVER,CARD CAGE:AL,PROCESSOR	80009	200-3438-01
					(ATTACHING PARTS)		
-2	211-0408-00			9	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-3	200-3654-01			1	COVER,CARD CAGE:AL,HIGH VOLTAGE	80009	200-3654-01
					(ATTACHING PARTS)		
-4	211-0408-00			2	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-5	200-3655-01	B020000	B020329	1	COVER,CARD CAGE:AL,MAIN	80009	200-3655-01
	200-3655-02	B020330		1	COVER,CARD CAGE:AL,MAIN	80009	200-3655-02
					(2782 ONLY)		
	200-3655-02	B010100		1	COVER,CARD CAGE:AL,MAIN	80009	200-3655-02
					(2784 ONLY)		
-6	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	----- -----			1	CKT BOARD ASSY:REFERENCE OSCILLATOR		
					(SEE A29 REPL)		
-8	----- -----			1	CKT BOARD ASSY:SWEEP/SPAN ATTENUATOR		
					(SEE A33 REPL)		
-9	----- -----			1	CKT BOARD ASSY:PERIOD COUNTER		
					(SEE A28 REPL)		
-10	----- -----			1	CKT BOARD ASSY:PHASE LOCK		
					(SEE A31 REPL)		
-11	----- -----			1	CKT BOARD ASSY:LO MODULE		
					(SEE A25 REPL)		
-12	----- -----			1	CKT BOARD ASSY:LOG PROCESSOR		
					(SEE A18 REPL)		
-13	----- -----			1	CKT BOARD ASSY:DIGITAL VIDEO PROCESSOR		
					(SEE A20 REPL)		
-14	----- -----			1	CKT BOARD ASSY:DIGITAL STORAGE		
					(SEE A24 REPL)		
-15	----- -----			1	CKT BOARD ASSY:DISPLAY AMP		
					(SEE A22 REPL)		
-16	----- -----			1	CKT BOARD ASSY:HIGH VOLTAGE		
					(SEE A23 REPL)		
-17	----- -----			1	CKT BOARD ASSY:MAIN PROCESSOR		
					(SEE A41 REPL)		
-18	----- -----			1	CKT BOARD ASSY;I/O INTERFACE		
					(SEE A42 REPL)		
-19	----- -----			1	CKT BOARD ASSY:MEMORY		
					(SEE A43 REPL)		
-20	441-1736-00	B020000	B020451	1	CARD CAGE ASSY:ALUMINUM	80009	441-1736-00
	441-1736-01	B020452		1	CARD CAGE ASSY:ALUMINUM,WELDED	80009	441-1736-01
					(2782 ONLY)		
	441-1736-00	B010100	B010127	1	CARD CAGE ASSY:ALUMINUM	80009	441-1736-00
	441-1736-00	B010128		1	CARD CAGE ASSY:ALUMINUM	80009	441-1736-00
					(2784 ONLY)		
					(ATTACHING PARTS)		
-21	211-0408-00			8	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-22	441-1784-01			1	CHAS,CARD CAGE:AL,MAIN	80009	441-1784-01
					(ATTACHING PARTS)		
-23	211-0408-00			19	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	----- -----			1	CABLE ASSEMBLY:FLAT FLEX COAX		
					(SEE A3 REPL)		
-25	----- -----			1	CKT BOARD ASSY:MOTHER		
					(SEE A1 REPL)		
					(ATTACHING PARTS)		
-26	211-0408-00			3	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-27	441-1748-00			1	CHASSIS,MAIN:ALUMINUM	80009	441-1748-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
5-1	----- -----			1	PHASELOCK ASSY:MICROWAVE(SEE A17 REPL)		
					(ATTACHING PARTS)		
-2	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-3	----- -----			1	CALIBRATOR ASSY:(SEE A15 REPL)		
					(ATTACHING PARTS)		
-4	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-5	407-3902-00			1	BRACKET,MTG:ALUMINUM	80009	407-3902-00
					(ATTACHING PARTS)		
-6	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	----- -----			1	ISOLATOR,RF:WIDE BAND,8-18GHZ		
					(SEE A15A3 REPL)		
					(ATTACHING PARTS)		
-8	211-0390-00			2	SCREW,MACHINE:2-56 X 0.188,FH,STL CD PL	80009	211-0390-00
					(END ATTACHING PARTS)		
-9	----- -----			1	MICROWAVE IF ASSY:(SEE A13 REPL)		
					(ATTACHING PARTS)		
-10	211-0408-00			6	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-11	----- -----			1	VR ASSEMBLY:(SEE A16 REPL)		
					(ATTACHING PARTS)		
-12	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-13	----- -----			1	INTMD FREQ ASSY:525MHZ(SEE A14 REPL)		
					(ATTACHING PARTS)		
-14	211-0408-00			4	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
-15	211-0409-00			2	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-16	----- -----			1	TERMINATION AS:LOW PASS(SEE A12A4 REPL)		
-17	----- -----			1	MIXER,LOW PASS:(SEE A12A5 REPL)		
-18	----- -----			1	CONVERTER ASSY:(SEE A12 REPL)		
					(ATTACHING PARTS)		
-19	211-0754-00			2	SCR,ASSEM WSHR:6-32 X 1.375,PNH,STL	93907	ORDER BY DESCR
-20	211-0408-00			6	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
					(END ATTACHING PARTS)		
-21	343-1447-00			1	CLAMP,MTG:YTO,INSTR,ALUMINUM	80009	343-1447-00
					(ATTACHING PARTS)		
-22	211-0732-00			3	SCR,ASSEM WSHR:6-32 X 0.75,PNH,STL,CD PL,TO	TK1543	ORDER BY DESCR
					RX T15		
					(END ATTACHING PARTS)		
-23	----- -----			1	YIG OSC ASSY:(SEE A11 REPL)		
					(ATTACHING PARTS)		
-24	211-0730-00			1	SCR,ASSEM WSHR:6-32 X 0.375,PNH,STL CD PL,T	80009	211-0730-00
					ORX T15		
					(END ATTACHING PARTS)		
-25	----- -----			1	CKT BOARD ASSY:YIG OSC DRIVER		
					(SEE A11A2 REPL)		
					(ATTACHING PARTS)		
-26	211-0408-00			5	SCR,ASSEM WSHR:4-40 X 0.250,PNH,STL TORX	93907	ORDER BY DESCR
-27	211-0409-00			1	SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL	93907	ORDER BY DESCR
-28	210-1291-01			1	WASHER,SHLDR:0.118 ID X 0.202 OD X 0.1 THK	80009	210-1291-01
					(END ATTACHING PARTS)		
-29	342-0563-00			1	INSULATOR,PLATE:TRANSISTOR,FIBERGLASS REINF	18565	69-11-8805-1674
					ORCED SILICON RUBBER		
-30	441-1748-00			1	CHASSIS,MAIN:ALUMINUM	80009	441-1748-00

Fig. 5
Sht. 1 of 2

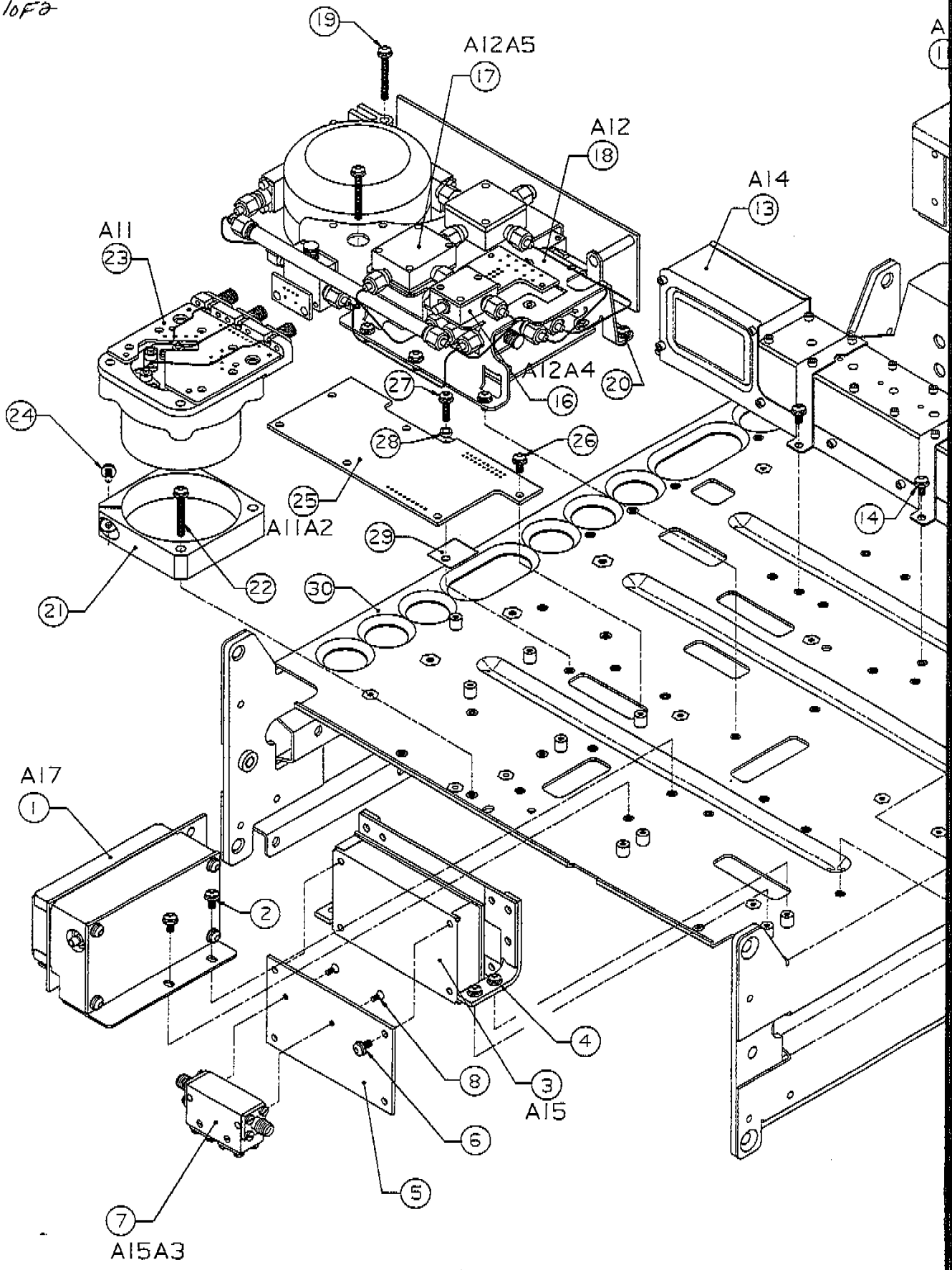


Fig. 5
Sht. 2 of 2

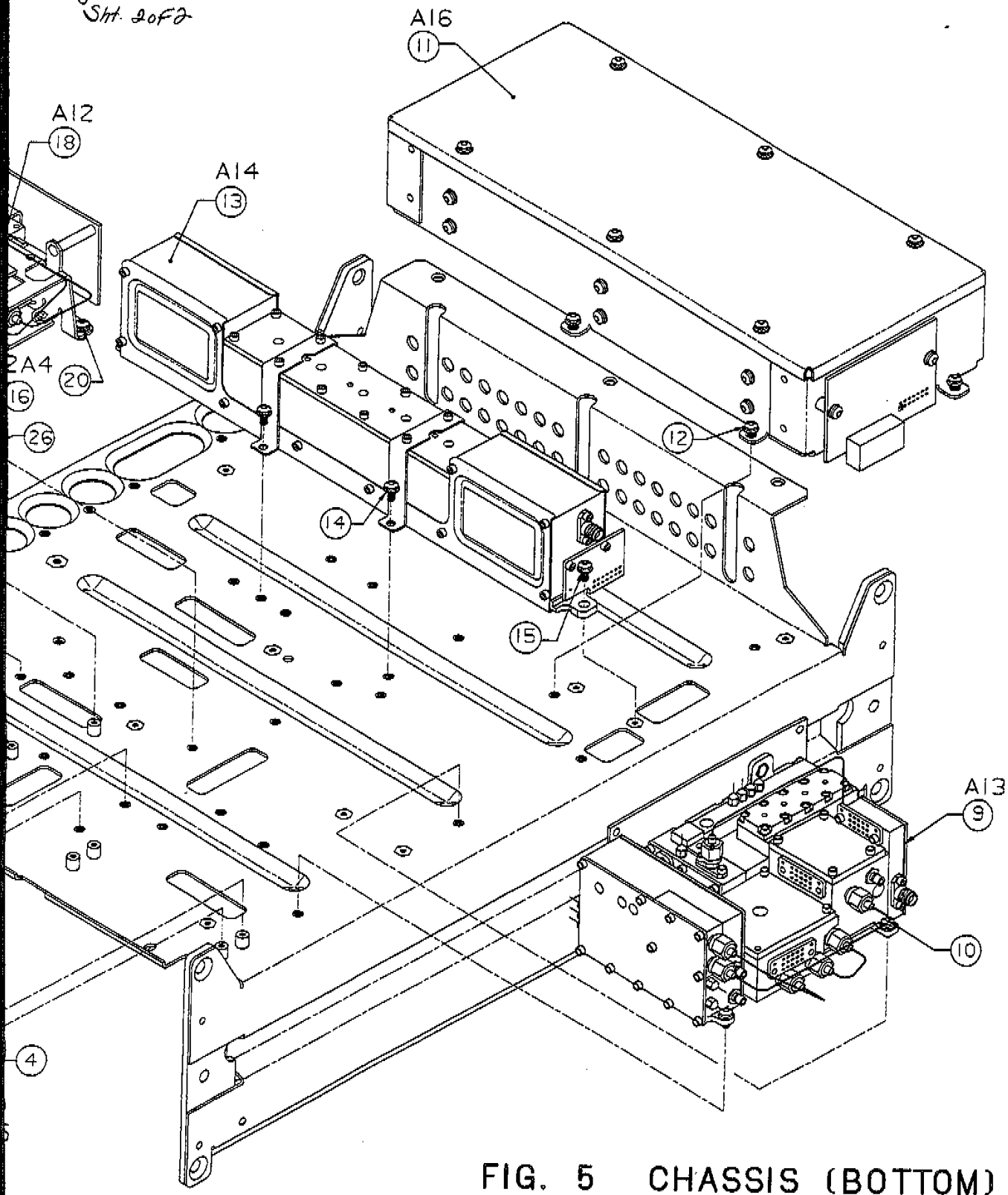
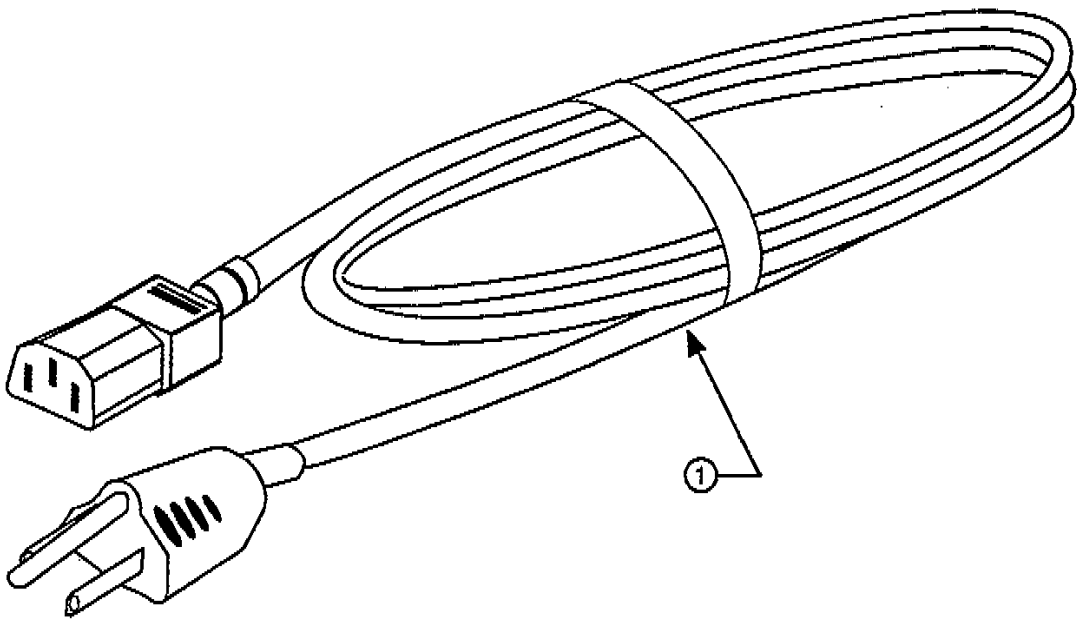
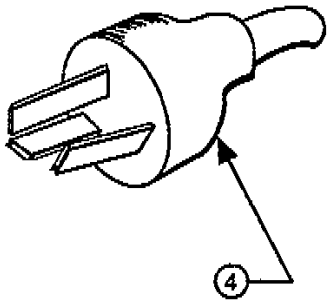
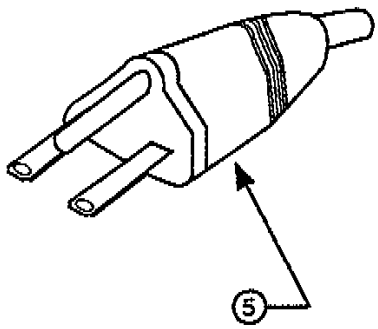


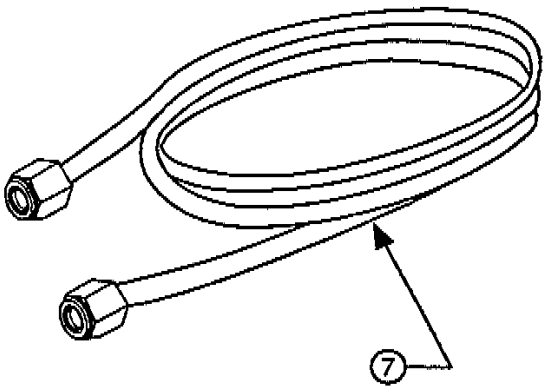
FIG. 5 CHASSIS (BOTTOM)

Fig. 6
Sht. 1 of 2









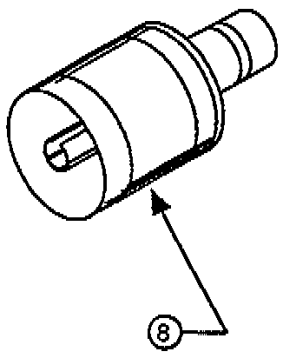


Fig. 6
Sht. 2 of 2

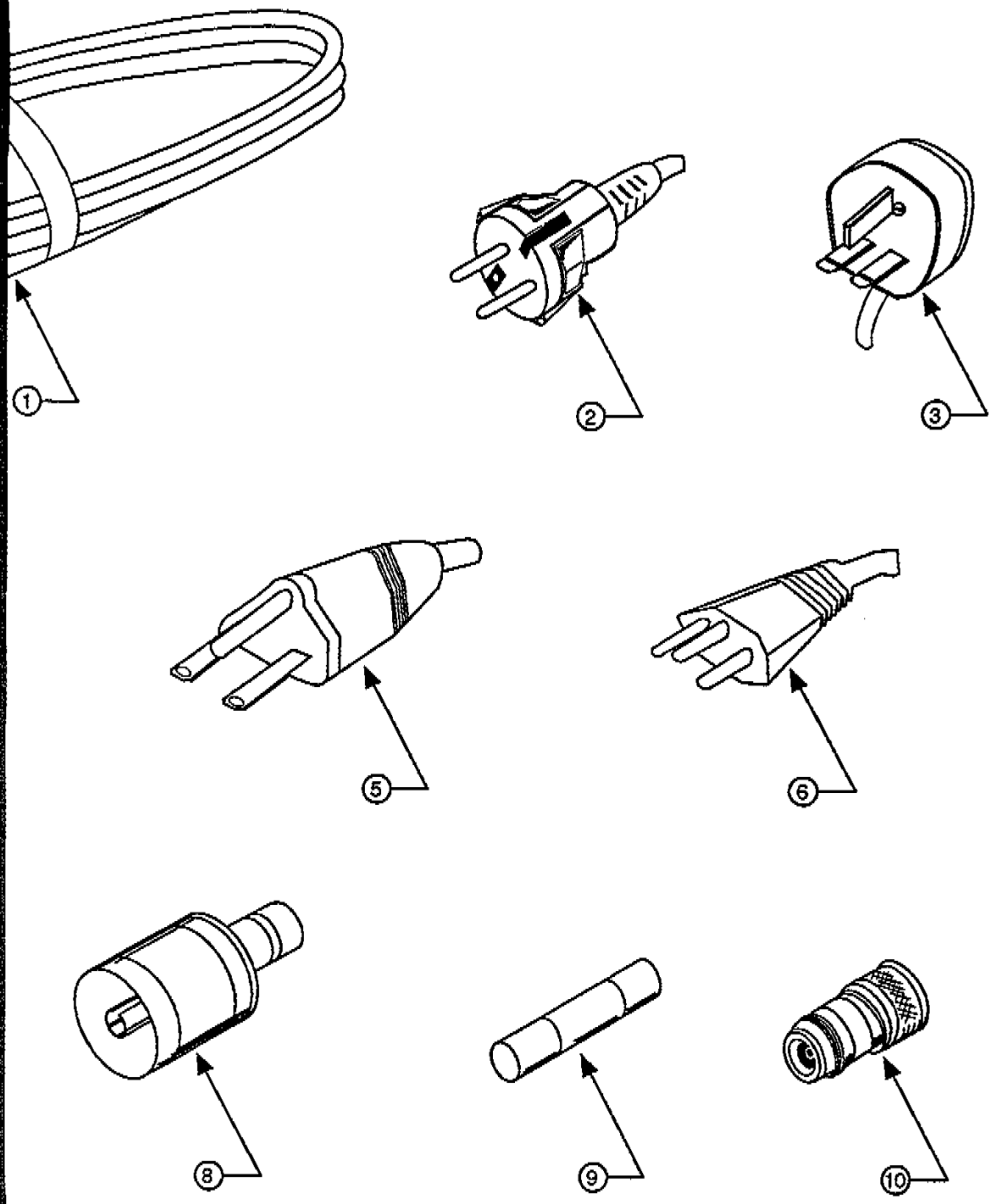


FIG.6 ACCESSORIES

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
6-1	161-0104-00			1	CABLE ASSY,PWR,:3,18 AWG,98 L,SVT,GREY/BLK, 60 DEG C,BME X RTANG IEC,RECPT,10A/250V;,,	16428	CH8352, FH-8352
-2	161-0104-06			1	CABLE ASSY,PWR,:3 X 0.75MM SQ,220V,98.0 L (OPTION A1 EUROPEAN ONLY)	S3109	
-3	161-0104-07			1	CABLE ASSY,PWR,: (OPTION A2 UNITED KINGDOM ONLY)	80009	161-0104-07
-4	161-0104-05			1	CABLE ASSY,PWR,:3,18 AWG,240V,98.0 L (OPTION A3 AUSTRALIAN ONLY)	S3109	
-5	161-0134-00			1	CABLE ASSY,PWR,:3,18 AWG,240V,120.0 L (OPTION A4 NORTH AMERICAN ONLY)	70903	ORDER BY DESCR
-6	161-0167-00			1	CABLE ASSY,PWR,:3.0 X 0.75,6A,240V,2.5M L (OPTION A5 SWISS ONLY)	80009	161-0167-00
-7	012-0649-00			1	CABLE ASSY,RF:50 OHM COAX,28.5 L	19505	80-9902-201
-8	103-0045-00			1	ADAPTER,CONN:N MALE TO BNC FEMALE	24931	29 JP104-3
-9	159-0319-00			2	FUSE,CARTRIDGE:4A,125V,5.2 X 20MM,FAST BLOW	71400	GMA-4A
	159-0320-00			2	FUSE,CARTRIDGE:4A,250V,FAST (OPTION A1,A2,A3,A4,A5 ONLY)	80009	159-0320-00
-10	131-4329-00			1	CONN,RCPT,ELEC:THREADED,N-TYPE,FEMALE	80009	131-4329-00
	070-8220-00			1	MANUAL,TECH:PROGRAMMERS,2782,OPTION 16 2780 SERIES	80009	070-8220-00
	070-8240-01			1	MANUAL,TECH:OPERATORS,2780 SERIES	80009	070-8240-01
	070-8566-01			1	MANUAL,TECH:INSTALLATION,2780 SERIES,PERFOR MANCE VERIFICATION	80009	070-8566-01
	063-0632-02			1	SOFTWARE PKG:278X PERFORMANCE VERIFICATION (THIS IS INCLUDED WITH 070-8566-00)	80009	063-0632-02
	063-1119-01			1	SOFTWARE PKG:2782 AUTO TEST SOFTWARE V1.4 (THIS IS INCLUDED WITH 070-8566-00)	80009	063-1119-01
	070-8241-02			1	MANUAL,TECH:PROGRAMMERS,2780 SERIES,W/8566 LANGUAGE	80009	070-8241-02
	070-8242-01			1	MANUAL,TECH:PROGRAMMERS REF GUIDE,2780 SERI ES	80009	070-8242-01
	070-8249-01			1	MANUAL,TECH:OPERATORS HANDBOOK,2780 SERIES	80009	070-8249-01
					OPTIONAL ACCESSORIES		
	015-0509-00			1	ADAPTER ASSY:N MALE TO N FEMALE 50 OHM,10KH Z TO 21GHZ,50V	93459	5201
	016-1019-01			1	RACK ADPTR KIT:PART SPECTRUM ANALYZER	80009	016-1019-01
	070-8244-02			1	MANUAL,TECH:SERVICE,2780 SERIES,VOL 1	80009	070-8244-02
	063-0899-00			1	SOFTWARE PKG:278X ADJUSTMENT SOFTWARE V1.1 (THIS IS INCLUDED WITH 070-8244-01)	80009	063-0899-00
	063-1119-01			1	SOFTWARE PKG:2782 AUTO TEST SOFTWARE V1.4 (THIS IS INCLUDED WITH 070-8244-01)	80009	063-1119-01
	006-7334-00			1	FIELD SVC KIT:2782	80009	006-7334-00
	012-1243-00			1	.CABLE,INTCON:CRIMP,MONITOR;MALE TO MALE,STR .,DB9 BOTH ENDS,1 METER	80009	012-1243-00
	012-1347-00			1	.CABLE ASSEMBLY:2782 SERVICE KIT,POWER SUPPL .Y	80009	012-1347-00
	013-0260-00			2	.ADAPTER ELEC:RF,SMA PLUG TO SMB JACK,0.766 .L	98291	050-674-6303-310
	015-0599-00			1	.ADAPTER,CONN:9 TO 25 FEMALE	80009	015-0599-00
	174-2013-00			6	.CABLE ASSY,RF:50 OHM COAX,3.1 L	80009	174-2013-00
	376-0243-00			1	.COUPLER:20DB,0.2-250MHZ	80009	376-0243-00
	671-0725-00			1	.CIRCUIT BD ASSY:CARD CAGE EXTENDER	80009	671-0725-00
	671-0726-00			1	.CIRCUIT BD ASSY:MAIN CARD CAGE EXTENDER	80009	671-0726-00
	671-0727-00			1	.CIRCUIT BD ASSY:PROCESSOR EXTENDER	80009	671-0727-00

SERVICE-RELATED ERROR MESSAGES

The following table contains service-related error messages that might appear on the instrument screen. Along with the messages are a brief description of the message and possible corrective action. Use this information along with normal troubleshooting methods to isolate a faulty module.

Table A-1. Error Messages

Message	Description	Corrective Action
129 MHz Count Timed Out	The LO129 count failed.	Check the A28 Period Counter and A25 LO Module.
129 MHz Tuning Correction Terminated	Correction of the LO129 tune DACs failed.	Check the A25 LO Module.
129 MHz Tuning Range Unknown	The tuning range of the LO129 does not match the expected range.	Check the A25 LO Module.
25 MHz IF Timed Out Count never finished	The IF25 count failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
25 MHz LO Count 4 MHz IF count bad data	The 4 MHz IF count failed while attempting to set the 29 MHz LO in the VR to convert the 25 MHz ringdown oscillator to 4 MHz.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Count Data Unknown	The LO29 count failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Count Terminated Count never finished	The LO29 count failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Does Not Converge Resonator tracking failed	The 29 MHz LO in the VR does not converge.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Not Set Resonator tracking failed	The 29 MHz LO in the VR can not be set to a specified frequency.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Out Of Range	The 29 MHz LO in the VR has insufficient range to convert the 25 MHz ringdown oscillator frequency to 4 MHz.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
29 MHz LO Set To Limit Value Resonator tracking failed	The 29 MHz LO in the VR has insufficient range for resonator tracking.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
9 MHz LO Timed Out 25 MHz ringdown oscillator not set	The 29 MHz LO in the VR not able to convert the 25 MHz oscillator to 4 MHz properly.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
2nd LO Not Locked	The 2nd LO (in the microwave IF assembly) will not lock in the time allowed.	Check the A13 Microwave IF module and A29 Reference Oscillator.
4 MHz Terminated Count never finished	The IF4 count failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
565 MHz Count Timed Out	The LO565 count failed.	Check the A31 565 MHz Synthesizer and A29 Period Counter.
Action Code Unknown Unknown error action argument received.	The error log action selection function received an unknown argument.	Indicates a possible firmware error. ****Please notify the factory.****
Attenuator Steps Broken	The attenuator changing did not result in the correct change in signal amplitude.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Bandwidth Offset Data In Memory Unknown Band offset correction data unknown.	The non-volatile memory contains unknown band offset correction data.	Check A42 I/O Interface, NVRAM batteries, and Flatness data on all attenuator settings.
Bandwidth Correction Reached Limit. Resolution bandwidth correction failed	Resolution bandwidth correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Bandwidth Type Unexpected Resolution bandwidth correction failed. Firmware error.	Resolution bandwidth correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
BuildMessage NULL Pointer.	The "BuildMessage" routine has failed.	Indicates a possible firmware error. ****Please notify the factory****
BuildResponse NULL Pointer.	The "BuildResponse" routine has failed.	Indicates a possible firmware error. ****Please notify the factory****
BW Correction Timed Out; Terminated. Resolution bandwidth correction failed.	Resolution bandwidth correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
BW Level Correction Timed Out; Terminated. Resolution bandwidth correction failed.	Resolution bandwidth correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Calibrator Not Responsive.	The calibrator SIC does not respond.	Check A15 Calibrator and A42 I/O interface.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Channel Not Open. Internal Firmware Error.	An operation was attempted on non-volatile memory that requires a file to be open on the channel being used when there was no open file for that channel.	Indicates a possible firmware error. **** Please notify the factory.****
Counter Board Not Responsive.	The Counter board SIC does not respond.	Check A28 Period Counter and A42 I/O Interface.
Crystal Resonator Set To Limit Value. Resonator tracking failed.	One of the resonator tune DACs in the VR has insufficient range for resonator tracking.	Refer to the Vertical Correction Information in the Troubleshooting portion of the Maintenance Section of this manual.
Crystal Resonator Timed Out. Resonator tracking failed.	Resonator tracking failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Data Not Stored - Service Mode Required. Instrument uses current data in RAM.	An attempt was made to store current RAM internal correction data into EEPROM. The instrument must be in the service mode to be able to write correction data to EEPROM.	Enable Service Mode and re-run tests.
Data Source Unknown.	The information data source is unknown.	Indicates a possible firmware error. **** Please notify the factory.****
Data State Cannot Be Used.	The requested data state cannot be used. No action was taken.	Indicates a possible firmware error. **** Please notify the factory.****
Data Stored In Memory Not Valid NVRAM contains non-valid information.	The non-volatile memory contains non-valid data.	Check A42 I/O Interface and NVRAM batteries.
Data Stored In Memory Unknown.	The non-volatile memory contains unknown file system data.	Check A42 I/O Interface and NVRAM batteries.
Delta-X Measurement Terminated. Waveform not of required type.	An unexpected waveform was found. The waveform must be a single filter shape with exactly two crossings at the specified y-value.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Digital Storage Comm Not Responsive.	An attempt to communicate with the display processor has failed.	Indicates a possible firmware error. **** Please notify the factory.****
Digital Storage Data Number Unknown.	The Digital Storage did not return the data number that corresponds with the data requested.	Indicates a possible firmware error. **** Please notify the factory.****
Digital Storage MIC Not Responsive.	The Digital Storage MIC does not respond.	Check A24 Digital Storage and A42 I/OInterface.
Display Amplifier Timed Out. signal not produced	The display sequencer has not produced a "ready signal in".	Check A24 Digital Storage and A42 I/O Ready Interface.
Display Law Correction Terminated. Internal correction routine failed. Refer to Self-Correction in the Op Manual.	The display law correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Display Position Does Not Converge.	The instrument cannot converge to the requested display position.	Check A20 Video Processor.
Error Message Overflow. Discarding overflowed messages.	The system has too many messages queued up and is running out of memory.	Probably related to excess GPIB traffic. Review program to reduce commands coming in, or program is producing too many errors.
External Mixer Loss Data Unknown.	The non-volatile memory contains unknown external mixer loss data.	Check A42 I/O Interface.
File Already Open. Internal firmware error.	An attempt was made to open a file more than once.	Indicates a possible firmware error. ****Please notify the factory.****
File Mode Unknown. Internal firmware error.	An unknown file mode was specified.	Indicates a possible firmware error. ****Please notify the factory.****
File Not Found.	The file specified was not found.	Indicates a possible firmware error. ****Please notify the factory.****
File Seek Not Possible. Internal firmware error.	An attempt was made to seek outside of the defined file size.	Indicates a possible firmware error. ****Please notify the factory.****
File Specification Unknown.	An unknown file specification string was passed to the file system.	Indicates a possible firmware error. ****Please notify the factory.****
Flatness Data In Memory Unknown.	The non-volatile memory contains unknown flatness correction data.	Check flatness data.
Flatness Not Responsive. Flatness SIC does not answer.	The flatness RAM on the Log Processor is not responsive.	Check A28 Log Processor and A42 I/O Interface.
Focus Step Size Increase Unknown. Memory failed.	The focus increment mode is not valid.	Indicates a possible firmware error. ****Please notify the factory.**** .
FM Span Correction Out Of Range.	The X1 FM decade span attenuator correction factor is out of range.	Re-run Frequency Self-Corrections. Check Frequency Control system.
FM Span Correction Out Of Range.	The calibration of the FM spans failed.	Re-run Frequency Self-Corrections.
Frequency Data In Memory Unknown.	The non-volatile memory contains unknown frequency correction data.	Check A42 I/O Interface.
Frequency Uncorrected.	The frequency control firmware is operating open-loop.	Re-run Frequency Self-Corrections. Check Frequency Control system.
Front Panel Data Not Responsive.	The front-panel data SIC does not respond.	Check A2 Front Panel and A42 I/O Interface.
Front Panel Not Responsive.	The front-panel control SIC does not respond.	Check A2 Front Panel and A42 I/O Interface.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Front Panel State Unknown.	A known front panel state was not found.	Indicates a possible firmware error. ****Please notify the factory.****
Front Panel Timed Out.	The front panel does not respond.	Check A2 Front Panel.
Gain Step Correction Terminated. Hardware failure indicated.	Data during gain step correction indicates a hardware failure.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Gain Step Correction Took Too Long. Terminated. Gain step correction failed.	The Gain Step correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Gain Step Internal Self-Corr Terminated. Internal correction routine failed. Gain steps not corrected. Refer to Self-Corrections in the Op Man.	The gain step correction routine failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Gain Step Unknown. Memory failed.	The gain step request is unknown.	Refer to the Vertical Correction information in the Troubleshooting portion of this Maintenance Section of this manual.
High Z, Crystal Neg R DAC Too Coarse. Resolution bandwidth correction failed.	The Resolution bandwidth level DAC on the VR has insufficient resolution to correct the VR.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
High Z, LC Neg R DAC Too Coarse. Resolution bandwidth correction failed.	The resolution bandwidth level DAC in the VR has insufficient resolution to correct the VR.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Hinge Point Data Unknown. Bad data found during correction.	Data found during hinge point correction is unknown. Hardware problems are indicated.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Hinge Position Timed Out. Hinge position not set.	An attempt to set the hinge position did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Hinge Power Timed Out. Hinge power not set.	An attempt to set hinge power did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Identify Request Unknown.	The identify mode has been requested with unknown instrument settings.	Indicates a possible firmware error. ****Please notify the factory.****
Input Handler Message Building Failed. Memory failed during message building.	Memory allocation failed during the building of a message.	Indicates a possible firmware error. ****Please notify the factory.****
Instrument Type Unknown.	The variable "Instrument Type" has been found to have an unknown value.	Indicates a possible ;firmware error. ****Please notify the factory.****

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Intensity Increase Mode Unknown. Memory failed.	The intensity increment mode is not valid, but was previously validated.	Possible RAM failure - run advanced diagnostic (information in this section), or possible firmware error. ****Please notify the factory.****
Internal Calibrator Out Of Range. Signal level not within expected range.	The internal calibrator signal level is not within the range of expected values.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Internal Frequency Standard Warming Up. Frequency may be inaccurate.	The internal frequency standard takes a few minutes to warm up. Until it does, the reference loop cannot lock internally and the instrument may not meet its frequency accuracy specifications.	Allow one-hour warm-up time. If the message persists, check the A29 Reference Oscillator.
Internal Reference Not Standard. Reference loop cannot lock.	No signal was found at the loop reference input when using the internal standard.	Check the A29 Reference Oscillator.
Key Code Input Not Recognized. No action taken.	The attempted key code input was not recognized and no action was taken.	Indicates a possible firmware error. ****Please notify the factory.****
Key Code Selection Unknown. No action taken.	An unknown front-panel key code was sent. No action taken.	Indicates a possible firmware error. ****Please notify the factory.****
KEYPAD Terminator Unknown.	The KEYPAD terminator is not known. The valid KEYPAD terminator selections are: GHz MHz kHz Hz SEC mSEC µSEC nSEC V mV V nV	Indicates a possible firmware error. ****Please notify the factory.****
Knob Code Selection Unknown. No action taken.	An unknown front-panel knob code was sent. No action taken.	Indicates a possible firmware error. ****Please notify the factory.****
LC Resonator Set To Limit. Resonator tracking failed.	One of the LC tune DACs in the VR has insufficient range for resonator tracking.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
LC Resonator Tracking Timed Out. Resonator tracking failed.	An attempt to set one of the LC resonators in the VR did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Linear Hinge Position Timed Out. Linear hinge position not set.	An attempt to set the linear hinge position did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Linear Hinge Position Truncated. Set to limit value.	The linear hinge position DAC has insufficient range.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Linear Scale Set To Limit . Linear scale correction failed.	Linear scale correction found insufficient range in the gilbert multiplier DAC on the Log Processor module, and the DAC was set to its limit. This corrects the center of the screen to have zero vertical error in linear scale.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
LO Low Count Timed Out.	The LO low count failed.	Check the A25 LO Module.
LO Low DAC Weight Out Of Range.	The tune DACs relative value is outside of the expected range.	Check the A25 LO Module.
LO Low Span Correction Out Of Range.	One of the LO low decade span attenuator correction factor is out of range.	Check the A25 LO Module.
LO Low Span Correction Terminated.	The correction of the LO low spans failed.	Check the A25 LO Module.
LO Low Tune Offset Out Of Range.	The offset relating LO low frequency to the tune DACs is outside of the expected range.	Check the A25 LO Module.
LO Low Tune Slope Out Of Range.	The slope relating LO low frequency to the tune DACs is outside of the expected range.	Check the A25 LO Module.
LO Low Tuning Correction Terminated.	The calibration of the LO low tune DACs failed.	Check the A25 LO Module.
LO Low Will Not Set.	The LO low will not set to the desired frequency.	Check the A25 LO Module and A24 I/O Interface.
LO Low Will Not Tune High Enough.	The LO low is not tuning high enough.	Check the A25 LO Module.
LO Low Will Not Tune Low Enough.	The LO low is not tuning low enough.	Check the A25 LO Module.
Linear Scale Timed Out. Linear scale correction failed.	An attempt to set linear scale did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Local Oscillator Not Responsive.	The LO module SIC does not respond.	Check the A25 LO Module and A24 I/O Interface.
Log Correction Terminated. Internal correction routine failed. Refer to Self-Correction in Op Man.	The log curve characterization failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Log Hinge Position Truncated. Set to limit value.	The log hinge position DAC has insufficient range.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Log Offset Resolution Data Out Of Range. Log offset corrections failed.	The measured value of the resolution of the log offset DAC is not within the expected range.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Log Scale Correction Data Unknown. Internal correction routine failed.	Data found during the log scale correction routine was unknown.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Log Scale Timed Out. Log scale not set.	An attempt to set the log scale factor did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Log/Lin Mode Selection Unknown. Memory failed.	The log/lin selection is unknown.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section. Also indicates a possible firmware error. ****Please notify the factory.****
Low Z, Crystal Neg R DAC Too Coarse. Resolution bandwidth correction failed.	The resolution bandwidth level DAC on the VR has insufficient resolution.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Low Z, LC Neg R DAC Too Coarse. Resolution bandwidth correction failed.	The resolution bandwidth level DAC on the VR has insufficient resolution.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Maximum Vertical Scale Not Reachable.	The maximum vertical scale factor is not reachable with the current log scale correction data.	Check A18 Log Processor, and refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Measure Bandwidth Found Bad Waveform.	An unknown waveform has been found.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Memory Allocation Error.	Memory allocation has returned a null pointer.	Indicates a possible firmware error. ****Please notify the factory.****
Memory Failed During Message Building.	Memory allocation failed in building a message.	Indicates a possible firmware error. ****Please notify the factory.****
Memory Register List Data Unknown.	The register list is unknown because of non-volatile memory problems.	Check A42 I/O Interface and NVRAM batteries.
Menu Selection Unknown.	The requested memory selection is unknown.	Indicates a possible firmware error. ****Please notify the factory.****
Microwave IF Gain Step Out Of Range. Gain step self-correction failed.	The measured Microwave IF gain step is not within the range of expected values.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Microwave IF Not Responsive.	The Microwave IF SIC does not respond.	Check A13 Microwave IF and A24 I/O Interface.
Minimum RF Atten Increment Unknown. Memory failed	The minimum RF attenuation increment selection is unknown.	Indicates a possible firmware error. ***Please notify the factory.***
Minimum Vertical Scale Not Reachable. Vertical scale factor failed.	The minimum vertical scale factor is not reachable with the current log scale correction data.	Check A18 Log Processor, and refer to the Vertical Correction information in the Trouble-shooting portion of the Maintenance Section of this manual.
Mixer Overdrive Increment Mode Unknown. Memory failed	The mixer overdrive increment is unknown.	Indicates a possible firmware error. *** *Please notify the factory.***
Multiplexer Not Responsive.	The multiplexer SIC does not respond.	Check A12 MTX and A42 I/O Interface.
Non-Volatile Memory Can't Be Formatted.	The firmware was unable to format non-volatile memory.	Check A42 I/O Interface.
Non-Volatile Memory Channel Unknown. Internal firmware error.	An unknown channel number was passed to the non-volatile memory.	Indicates a possible firmware error. *** *Please notify the factory.***
Non-Volatile Memory Full.	The non-volatile memory is full and there is no available memory for more data.	Indicates a possible firmware error. *** *Please notify the factory.***
Non-Volatile Memory Function Unknown.	An unknown or un-implemented function was attempted on the file system.	Indicates a possible firmware error. *** *Please notify the factory.***
Non-Volatile Memory Not Formatted.	The non-volatile memory specified was not properly formatted.	Check A42 I/O Interface.
Non-Volatile Memory Not Specified. Internal firmware error.	The non-volatile memory type was not specified in the firmware specification.	Indicates a possible firmware error. *** *Please notify the factory.***
Non-Volatile Memory Unknown. Internal firmware error.	An unknown non-volatile memory type was passed to the firmware.	Indicates a possible firmware error. *** *Please notify the factory.***
Peak Detector Max Not Corrected.	The peak detector maximum offset correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Peak Detector Min Not Corrected.	The peak detector minimum offset correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Peak Detector Min-Max Not Corrected.	The peak detector offset and gain correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Peak Detector Min-Max Timed Out. Peak detector correction failed.	The peak detector offset and gain correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Peak Detector Sample Not Corrected. Peak detector correction failed.	The peak detector sample mode maximum offset correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Peak Detectors Not Corrected. Internal correction routine failed Refer to Self-Correction in Op Man.	The video processor peak detector correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Plot Buffer Display Unknown. Missing menu or waveform display.	The screen stored in the plot buffer is an unknown display.	Indicates a possible firmware error. ***Please notify the factory.****
Plot Menu Selection Unknown. Menu key number unrecognized.	An unrecognized plot menu selection was made.	Indicates a possible firmware error. ***Please notify the factory.****
Plot Size Change Unrecognized.	An attempt was made to select a non-valid plot size.	Indicates a possible firmware error. ***Please notify the factory.****
Plotter Pen Color Unknown. Select red, green, or yellow.	An unknown color selection was saved into the plot buffer.	Indicates a possible firmware error. ***Please notify the factory.****
Plotter Will Not Start. Check connections and power switch.	The plotter initialization failed; probably due to the GPIB port being unconnected.	If the problem persists, check A42 I/O Interface and A5A6 Communications Interface.
Power Down.	Power was just turned off.	No Action
Power On.	Power turned on with the front-panel POWER key.	No action.
Power Scale Set To Limit Value. Power scale correction failed.	The power scale correction found insufficient range in the gilbert multiplier DAC on the log processor module.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Power Scale Timed Out. Power scale correction failed	An attempt to set the linear scale did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Power-Up Data In Memory Unknown.	The non-volatile memory contains unknown power-up data.	Check A42 I/O Interface.
Read Only File - Cannot Be Opened. Internal firmware error.	An attempt was made to open a file to write on a read only silicon disk drive.	Indicates a possible firmware error. ***Please notify the factory.****
Ref Level Correction Out Of Range. Correction not within expected range.	The measured reference level correction is not within the range of expected values.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Ref Oscillator Divider Out Of Range. Hardware cannot be set to this value.	The Reference Oscillator was requested to set to a divider value outside the limits of the hardware.	Indicates a possible firmware error. ****Please notify the factory.****
Reference Level Increment Unknown. Memory failed.	The reference level increment mode is unknown.	Indicates a possible firmware error. ****Please notify the factory.****
Reference Level Units Unknown. Memory failed.	The reference level units are unknown.	Indicates a possible firmware error. ****Please notify the factory.****
Reference Loop Cannot Lock. Internal reference frequency incorrect.	The measured internal reference frequency is not a proper multiple of the loop reference frequency.	Check A29 Reference Oscillator.
Reference Loop Will Not Lock.	The reference oscillator module lock loop will not lock, even though a loop reference is present.	Check A29 Reference Oscillator.
Reference Oscillator Count Timed Out. Count never finishes.	The Reference Oscillator count failed.	Check A29 Reference Oscillator and A28 Period Counter.
Reference Oscillator Not Responsive.	The Reference Oscillator is not responding.	Check A29 Reference Oscillator and A42 I/O Interface.
Reference Signal Missing. Connect REF SIGNAL OUT to input.	An attempt to find the reference signal was not successful.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual..
Reference Signal Unknown. Connect REF SIGNAL OUT to input.	The reference signal does not appear to be the instrument reference signal.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Register List Data In Memory Unknown.	The non-volatile memory contains an unknown register list.	Check A42 I/O Interface.
Register List Type Unknown.	The register list initiating function received an unknown list type.	Indicates a possible firmware error ****Please notify the factory.****
Resolution Bandwidth Self-Corr Failed. Internal correction routine failed.	The resolution bandwidth self-correction routine has failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Resolution BW Increment Unknown. Memory failed.	The resolution bandwidth increment is not valid.	Indicates a possible firmware error. ****Please notify the factory.****
Resonator Frequency Unknown. Resonator tracking failed.	Bad data found during VR resonator correction routine.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
RF Attenuation Unknown. Memory failed.	The RF attenuation increment mode is unknown.	Indicates a possible firmware error. ****Please notify the factory.****

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
RF Attenuator Not Responsive.	The RF attenuator SIC does not respond.	Check A10 RF Attenuator and A42 I/O Interface.
Ringdown Count Terminated. VR resonator frequency not counted.	An attempt to count the VR resonator frequency during ring-down was unsuccessful.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
RS-232 Terminator Selection Unknown. Select CR/LF, CR, or LF.	The terminator setting function for RS-232 port configuration received data that is not valid.	Indicates a possible firmware error. ****Please notify the factory.****
Sets Register Data In Memory Unknown. Settings register data unknown.	The non-volatile memory contains non-valid instrument settings register data.	Check A42 I/O Interface. Also indicates a possible firmware error. ****Please notify the factory.****
Signal Gain Timed Out. Signal level not set.	An attempt to set the signal level with the VR gain did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Signal Level Does Not Converge. Signal not set to specified level.	Setting the signal to a specific level does not converge.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Signal Level Timed Out. Signal level not set.	An attempt to set the signal level with the reference level did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Signal Offset Timed Out. Signal level not set.	An attempt to set the signal level did not succeed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Signal Offset Truncated. Set to limit value.	The log offset is not sufficient to set the signal to the desired level.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Sweep Not Responsive.	The Sweep board SIC does not respond.	Check A33 Sweep/Span Attenuator and A42 I/O Interface.
Sweep Offset Correction Terminated.	The correction of the frequency sweep offset DAC failed.	Check A33 Sweep/Span Attenuator and A20 Video Processor.
Sweep Offset Out Of Range.	The offset relating screen position to the frequency sweep offset DAC is outside of the expected range.	Check A33 Sweep/Span Attenuator and A20 Video Processor.
Sweep Offset Slope Out Of Range.	The slope relating screen position to the frequency sweep offset DAC is outside of the expected range.	Check A33 Sweep/Span Attenuator and A20 Video Processor.
Sweep Position Correction Terminated.	The correction of the sweep marker DAC in relation to horizontal acquisition failed.	Check A33 Sweep/Span Attenuator and A20 Video Processor.

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
Sweep Position Offset Out Of Range.	The offset relating screen position to sweep marker DAC is outside of the expected range.	Check A33 Sweep/Span Attenuator and A20 Video Processor.
Sweep Position Slope Out Of Range.	The slope relating screen position to sweep marker DAC is outside of the expected range.	Check A33 Sweep/Span Attenuator and A20 Video Processor.
Synthesizer Not Responsive.	The 565 Synthesizer SIC is not responding.	Check A31 565 MHz Synthesizer and A42 I/O Interface.
Text Too Long - Exceeded 40 Characters. Text string truncated.	The text string was too long to put on one line. On-screen text can only be 40 characters long.	Indicates a possible firmware error. ****Please notify the factory.****
Trace Rotation Increment Unknown.	The trace rotation increment mode is not valid.	Indicates a possible firmware error. ****Please notify the factory.****
Vertical Data In Memory Unknown. Vertical correction data unknown.	The non-volatile memory contains unknown vertical correction data.	Check A42 I/O Interface and NVRAM batteries.
Vertical Display Change Was Valid. Memory failed or firmware problem.	The vertical display mode change was valid, but has resulted in an unsuitable value.	Indicates a possible firmware error. ****Please notify the factory.****
Vertical Scale Mode Unknown. Memory failed.	The vertical scaling mode is unknown.	Indicates a possible firmware error. ****Please notify the factory.****
Vertical Scale Unexpected. Hardware or firmware problem.	The vertical scale setting has returned an unexpected error number.	Indicates a possible firmware error. ****Please notify the factory.****
Video Bandwidth Increase Unexpected. Memory failed.	The video bandwidth increment mode is unexpected.	Indicates a possible firmware error. ****Please notify the factory.****
Video Bandwidth Index Not Possible.	The video bandwidth index is not possible.	Indicates a possible firmware error. ****Please notify the factory.****
Video Pre-Processor Not Responsive.	The video pre-processor SIC, on the Log Processor board, does not respond.	Check A18 Log Processor and A42 I/O Interface.
Video Processor Not Responsive.	The Video Processor SIC does not respond.	Check A20 Video Processor and A42 I/O Interface.
VR 25 MHz Gain Out Of Range. Gain step not within expected values.	The measured maximum VR gain (25 MHz gain) is not within the range of expected values.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
VR Gain Truncated. Set to limit value.	The VR has insufficient gain range.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
VR Internal Self-Corr Routine Failed. Could Not Set VR Self-Cor Settings.	The attempt to set the instrument to VR self-correction setting has failed.	Indicates a possible firmware error. ****Please notify the factory.****

Table A-1. Error Messages (continued)

Message	Description	Corrective Action
VR Module Not Responsive.	The VR module SIC does not respond.	Check A16 VR and A42 I/O Interface.
VR Negative Resistance DAC Too Coarse. Resolution bandwidth correction failed.	The resolution bandwidth level DAC on the VR does not have fine enough resolution to correct the VR.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
VR Output Gain Out Of Range. Gain step not within expected values.	The measured VR output gain step is not within the range of expected values.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
VR Resonator Internal Self-Corr Failed. Refer to Self-Correction in Op Man.	The VR resonator tracking correction failed.	Refer to the Vertical Correction information in the Troubleshooting portion of the Maintenance Section of this manual.
Waveform Register Memory Data Unknown.	The non-volatile memory contains unknown waveform register data.	Check A42 I/O Interface.
YIG Not Responsive.	The YIG control SIC does not respond.	Check A25 LO Module and A42 I/O Interface.
YTO DAC Weight Out Of Range.	The weighting factor relating the relative weights of the tune DACs is outside of the expected range.	Check A25 LO Module, A11 YTO, and A11A2 YTO Driver.
YTO Span Cal Out Of Range.	One of the YIG decade span attenuator correction factors is out of range.	Check A25 LO Module.
YTO Span Correction Terminated.	The correction of the YIG main coil spans failed.	Check A25 LO Module, A11 YTO, and A11A2 YTO Driver.
YTO Tune Offset Out Of Range.	The offset relating YIG frequency to the tune DACs is outside the expected range.	Check A25 LO Module, A11 YTO, and A11A2 YTO Driver.
YTO Tune Slope Out Of Range.	The slope relating YIG frequency to the tune DACs is outside of the expected range.	Check A25 LO Module, A11 YTO, and A11A2 YTO Driver.
YTO Tuning Correction Terminated.	The correction of the YIG tune DACs failed.	Check AZ25 LO Module, A11 YTO, and A11A2 YTO Driver.
Zero Length Text Was Attempted. No action taken.	An attempt was made to make a zero length data entry. No action was taken.	Operator error. If the message persists, a firmware error is indicated. ****Please notify the factory.****

USING THE PROCESSOR EXTENDER

The Processor Extender board is part of the instrument Service Kit and allows extending any of the processor system boards (including the Communications Interface) and provides access to the signals that interface between the system board and the Mother board. The extender board also provides an RS-232 interface that allows external control of the instrument for calibration and troubleshooting.

Jumpers on each signal line allow attaching a logic analyzer or scope probe. This also allows isolating any signal by removing jumpers from the Processor Extender board. Test points for power supply voltages and ground references are included, and a set of LEDs indicate power supply control line status.

INSTALLING THE PROCESSOR EXTENDER TO INTERFACE RS-232

The Processor Extender can be used with up to two Processor System boards at a time. Two parallel connectors are provided, one vertical and another horizontal. The A42 I/O Interface must be used in the horizontal position to connect J11. A typical use would extend the A42 I/O Interface in the right angle connectors and the A41 Main Processor in the vertical connectors.

Connect the Processor system to interface RS-232 as follows. (Modify the procedure as necessary for extending any of the other Processor System boards.)

- 1. Remove the instrument power cord.

NOTE

It is necessary to remove the power cord because standby power is applied to the processor whenever the power cord is connected.

- 2. Remove the instrument cover.
- 3. Remove the Processor card cage shield.
- 4. Remove the A41 Main Processor board[1].
- 5. Refer to Figure B-1 and set the Processor Extender board jumpers as follows:

  J30 RS-232 Enabled
  J40 Interrupt 4 Selected

- 6. Remove the Torx T-10 screw from the motherboard as shown in Figure B-2. This prevents J11 on the Processor Extender from shorting.

NOTE

After using the extender, be sure to reinstall the screw removed in this step.

- 7. Install the Processor Extender board in the Main Processor slot.
- 8. Install the Main Processor in the vertical connector on the Processor Extender board.

[1]The Processor Extender board can be used with any of the boards in the Processor card cage, and the Communications Interface board in the Power Supply module. If the Memory board is extended, Interrupt 4 must be set on J12 of the A42 I/O Interface board instead of on the Processor Extender board. When the Processor Extender board is inserted in the A41 Main Processor or A43 Memory board slots, a corresponding Mother board screw must be temporarily removed to avoid contact with connector J11 on the Processor Extender. See Figure B-2.

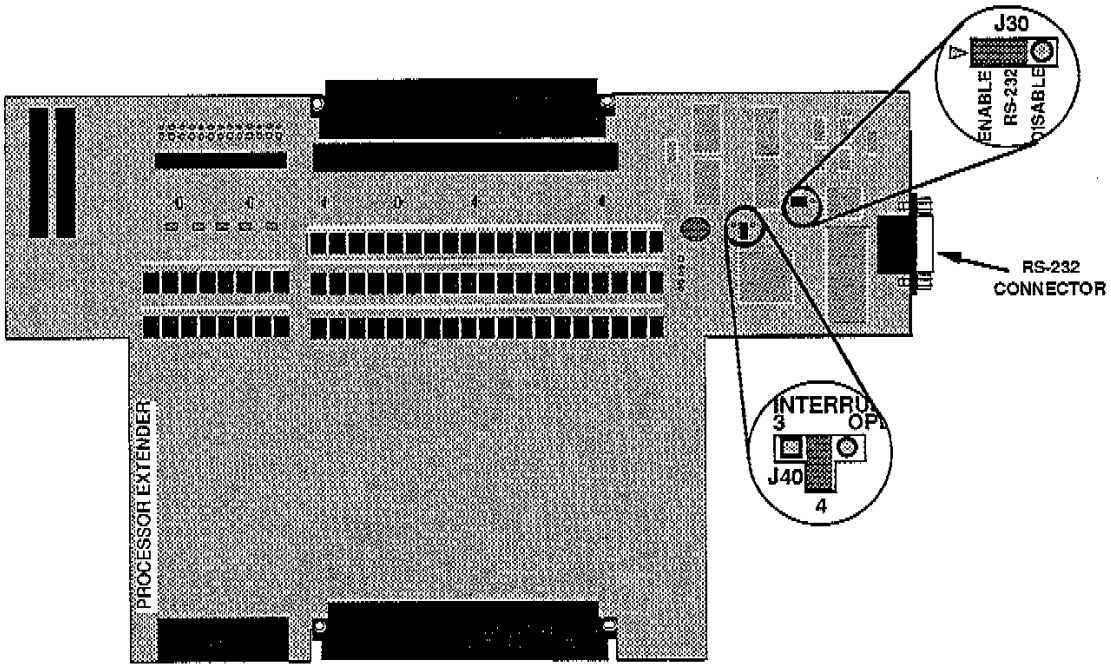


Figure B-1. Processor Extender board setup for RS232 operation.

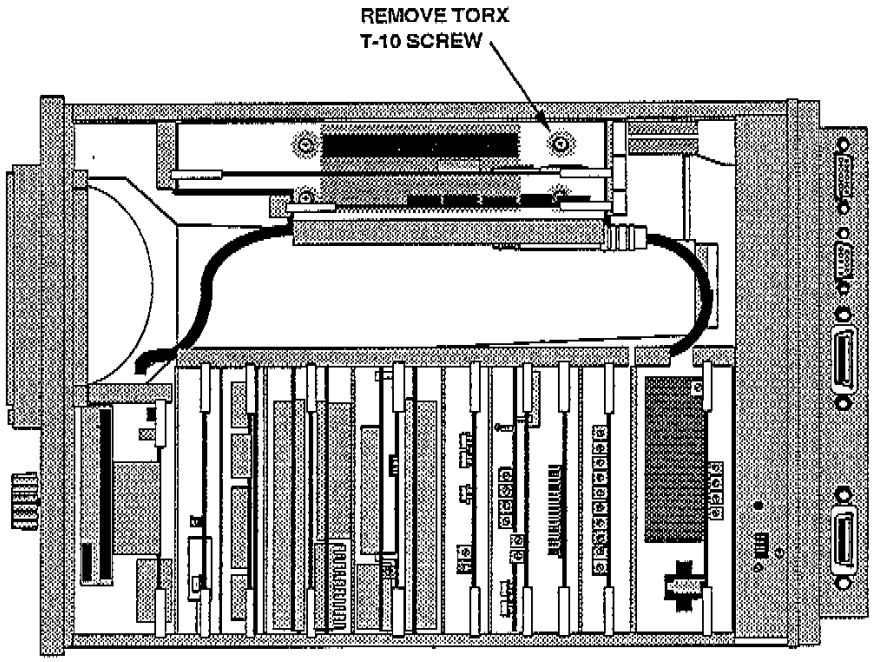


Figure B-2. Screw removal.

CONNECTING A PERSONAL COMPUTER

- 1. Connect an RS-232 terminal to the 9-pin connector, J20, on the Processor Extender board. This connector simulates an AT-style personal computer port. (A 9-pin-to-25 pin adapter is included in the Service Kit with the Processor Extender board.)

- 2. Install communications interface software[1] and set as follows:

Baud Rate	9600
Bits per Character	8
Parity	None

- 3. Set the instrument for the Service Mode by setting switch S11-3 on the A41 Main Processor to the closed position.

- 4 Re-connect the power cord and press the instrument POWER key.

ENTERING THE KEYBOARD MODE

Press the instrument UTIL key and select the Service Menu and then **Enter Keybd Mode** from the menu soft keys. The instrument must be in the Service Mode (S11-3 closed) to enable the Enter Keyboard soft key.

CAUTION

*Do not enter the Keyboard Mode without an appropriate terminal connected. If a terminal is not connected, front panel control cannot be restored without resetting the instrument's Main Processor, possibly losing data. See **EXITING THE KEYBOARD MODE.***

EXITING THE KEYBOARD MODE

Issue the **fpan** keyboard command to exit the Keyboard Mode.

This command returns control to the front panel. If you have entered the Keyboard Mode without having a terminal connected, you must either connect a terminal to exit properly, or you must reset the instrument's Main Processor by toggling S10-D on the Main Processor board or by unplugging and re-connecting the instrument power cord. Resetting the Main Processor may cause loss of data.

[1]We recommend use of the Public Domain software *Kermit* to provide interface with the instrument.

KEYBOARD SERVICE COMMAND DICTIONARY

The following commands are available in the RS-232 keyboard command mode using the Processor Extender Board (part of the Service Kit). Bold faced characters are keyboard commands, and those in italics are arguments and variables that may be selected for the command.

achp *0|1*	Select whether chop/alt display is automatically selected. 1 selects auto chop/alt, 0 selects manual chop/alt.
acun *0|1*	Turn unconditional acquisition on (1) or off (0).
adel *time*	Set alt delay, in seconds.
atda *att_idx atten*	Enter atten cal data value. "att_idx" is the attenuation index (0-7); "atten" is the attenuation in dB.
beat	Count the beat note from the phase gate, using 1024 as the period counter prescale value.
bofs *band att_idx offset*	Enter band offset value. "band" is the current instrument band number (0-4); "att_idx" is the attenuation index (0-7); "offset" is the offset in dB. Offset for band 0 should always be 0.0 dB. Also sets the hardware.
boli	Print list of band offset values.
bost	Store band offset values into NVRAM.
bswe *0|1*	Enable (1) or disable (0) backward sweep acquisitions. (BSPD bit on video processor).
bwfg *bw_idx gain*	Enter the fine gain level into the resbw cal data. "bw_idx" is the resbw table index; "gain" is the gain, in dB, required to make the reflvl come out right. Also sets the hardware.
bwlv *bw_idx bw_lvl*	Enter the bw level dac value into the resbw cal data. "bw_idx" is the resbw table index; "bw_lvl" is the dac value in hex. Also sets the hardware.
bwrs *bw_idx rs*	Enter RS value into resbw cal data. "bw_idx" is the resbw table index. "rs" is hex number equal to 2*rs1 + rs2; i.e the 2's bit is rs1 and the 1's bit is rs2. Also sets the hardware.
bwvr *bw_idx vbw*	Enter the hex "vbw" dac value into the resbw cal data. "bw_idx" indicates the resbw table index. Also sets the hardware.
cdel *min max*	Select min and max chop delay times. "min" and "max" have values ranging from 0 to 3. See display amp EMS for details.
cler	Clears all errors by running NoErrorReport().
clvl *lvl*	Enter internal calibrator signal level into current cal data. "lvl" is the signal level at the input connector, in dB, that is equivalent to the internal calibrator level.
cmem	Returns the amount of memory used.
cntv *0|1*	Set continuous vertical data out bit on video processor. "1" to enable, "0" to disable.

`cnvr reflvl old_units new_units`

Converts "reflvl" in "old_units" to the equivalent value in "new_units." "old_units" and "new_units" are as follows:

0	dBm
1	dBmV
2	Volts
3	Watts
4	User (Not implemented)
5	dBV
6	dBuV
7	dBuW
8	dBuV
9	Current instrument units

`ctps pos1 pos2`	Set the signal counter positions to "pos1" and "pos2".
`dcal source data_id`	Print (list) cal data. Vertical cal trace must have been enabled ("vtra 1). "source" indicates where the data to be printed comes from: 0 Generic cal data (ROM) 1 Default cal data (NVRAM) 2 Current cal data (RAM) "data_id" indicates which data is to be printed: 0 All data 1 Resonator tracking data 2 Display law data 3 Gain step data 4 ResBW data 5 Attenuator and calibrator data 6 Acquisition peak detector data 7 Log correction data
`dscr 0|1`	Disable/enable frequency corrections. A 0 argument will enable frequency corrections (closed loop). A 1 argument will disable frequency corrections (open loop).
`dsen 0|1`	Set display amp display enable; 1 enables display, 0 disables display.
`dsrc vert_src hor_src`	Select vertical and horizontal source for the real time display. Source selections are: 0 ground 1 internal 2 external
`echp`	Execute auto chop/alt routine.
`erde 0|1`	BDisplayErrors - Turns on or off the display of errors.
`erdm 0|1 mask`	BErrDispMask - Turns mask bits on or off, effects display of errors and warnings by instrument functional section. "mask" is a bits8 value.

erdw *0|1*	BDisplayWarnings - Turns on or off the display of warnings.
erep *error_number*	Report a error specified by the decimal argument "error_number".
erle *0|1*	BLogErrors - Turns on or off the logging of errors.
erlm *mask 0|1*	BErrLogMask - Turns mask bits on or off, effects logging of errors and warnings by instrument functional section. "mask" is a bits8 value.
erlw *0|1*	BLogWarnings - Turns on or off the logging of warnings.
eyef *periods*	Count the 4 MHz IF. "periods" specifies the period counter prescale value to use.
f129	Count the 129 MHz synthesizer, using 1024 as the period counter prescale value.
f565	Count the 565 MHz synthesizer, using 1024 as the period counter prescale value.
facc *file*	See if the specified NVRAM, EEPROM, or EPROM file is accessible. Argument "file" specifies what file to check. To see if NVRAM file "abc" is accessible, enter "facc RAM/abc". To see if EEPROM file "def" is accessible, enter "facc EEPROM/def". To see if EPROM file "ghi" is accessible, enter "facc EPROM/ghi".
fcat *file*	Dump the contents of a NVRAM, EEPROM, or EPROM file in hex format. Argument "file" specifies what file to dump. To dump NVRAM file "abc", enter "fcat RAM/abc". To dump EEPROM file "def", enter "fcat EEPROM/def". To dump EPROM file "ghi", enter "fcat EPROM/ghi".
fclo *file_descriptor*	Close a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt".
fcrt *file*	Create a silicon disk file for reading and writing in NVRAM or EEPROM and return a file descriptor of the created file. The file to be created is specified by the argument "file". To open a NVRAM file "abc", enter "fopn RAM/abc". To open a EEPROM file "def", enter "fopn EEPROM/def".
fdfo *0|1*	Enable/disable the strobe to the phase gate. A 0 argument will disable the strobe. A 1 argument will enable the strobe. To obtain a strobe, the fractional N should be set to the proper value for the desired strobe frequency.
fdir *file_system*	Do a directory list of the specified file system. If argument file_system is "RAM" the contents of the NVRAM silicon disk is displayed. If argument file_system is "EEPROM" the contents of EEPROM silicon disk is displayed. If argument file_system is "EPROM" the contents of EPROM silicon disk is displayed.
fldz	Fill the EEPROM flatness tables with zeros.
flgn *bits*	Set the pre- and post-filter gain bits on the VR. "bits" simultaneously sets both pre- and -post filter gain as follows: 1 -6 dB pre-filter, +6 dB post-filter 2 -6 dB pre-filter, +6 dB post-filter 4 -6 dB pre-filter, +6 dB post-filter
fltz *0|1*	Set the termination resistance Z on the VR. 0 selects low Z; 1 selects high Z.
fnuk *file_system*	Delete all files in the specified file system. If file_system = 0, all NVRAM files will be removed. If file_system = 1, all EEPROM files will be removed.

`fopn file`	Open a file for reading and writing in NVRAM, EEPROM, of EPROM (read only). and return a file descriptor of the opened file. The file to be opened is specified by the argument "file". To open a NVRAM file "abc", enter "fopn RAM/abc". To open a EEPROM file "def", enter "fopn EEPROM/def". To open a EPROM file "ghi", enter "fopn EPROM/ghi".
`fpan`	Returns instrument control to the front panel.
`fpos position`	Set the frequency reference position to "position"
`fred file_descriptor bytes`	Read data from a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". The argument "bytes" specifies how many bytes to read from the file.
`fren from to`	Rename a silicon disk file. The argument "from" is the name of the file to be renamed. The argument "to" is the name the file will be moved to.
`fsck file_system`	Run a file system consistency check on the specified file system. If argument file_system is "RAM" the NVRAM drive is checked. If argument file_system is "EPROM" the EPROM drive is checked. If argument file_system is "EEPROM" the EEPROM drive is checked.
`fsdf file_system`	Show the amount of free space left for the specified file system. If argument file_system is "RAM" the contents of the NVRAM silicon disk is displayed. If argument file_system is "EEPROM" the contents of EEPROM silicon disk is displayed. If argument file_system is "EPROM" the contents of EPROM silicon disk is displayed.
`fsek file_descriptor mode offset`	Seek to a position in a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". If argument "mode" is 0, the file pointer is set to "offset" bytes. If argument "mode" is 1, the file pointer is set to the current location plus "offset" bytes. If argument "mode" is 2, the file pointer is set to the size of the file plus "offset" bytes. The argument "offset" is the number of bytes to move within the file.
`fswp 0|1`	Enable (1) or disable (0) fast sweep mode of video processor.
`ftra [+-]source...`	Enable/disable tracing of the specified frequency control "source(s)". A leading "+" will enable the "source" while a leading "-" will disable the "source". More than one "source" may be specified, each with its own leading "+" or "-". The allowable values for "source" are: 129 29 count lohi lolo pres span sweep yig
`fwrt file_descriptor string`	Write a string to a silicon disk file. The argument "file_descriptor" is what was previously returned from "fopn" or "fcrt". The argument string is a quoted string of the text to write to the file.
`fyig frequency`	Perform a FindYIG. FindYIG assumes that the YTO is at "frequency".

`ganc dac`	Set the coarse gain dac on the VR to the hex value "dac." The dac is actually a set of bits, each of which selects a gain setting. The bits are decoded as follows: bits 0-2 1st gain stage of VR1 bits 3-5 3rd gain stage of VR1 Meaningful values are: 24 0 dB 22 9 dB 12 18 dB 11 27 dB 09 36 dB
`ganf dac`	Set fine gain dac on VR. This is the 2nd gain stage on VR1. "dac" is a hex value corresponding to a 12 dB gain range.
`gilb dac`	Set the gilbert (dB/div) dac on the log processor. "dac" is a 12 bit hex value (000-fff).
`glbq`	Print current value of the gilbert multiplier (dB/div) dac, in hex.
`gmax max_step`	Enter max VR gain step into current cal data. "max_step" is an integer value with units of dB.
`gmlg path slope icept`	Enter dB/div data into current cal data. "path" is the log IF frequency: 0 for 4 MHz; 1 for 25 MHz. "slope" and "icept" are the slope and offset parameters characterizing the dB/div vs gilbert dac relationship: dac = (dB/div)/slope + icept.
`gnuw gain`	Set the value of the microwave IF gain step value to "gain".
`gred gain`	Set the output gain steps on VR 3. "gain" selects the gain as follows: 0 0 dB 1 10 dB 2 20 dB
`hgpt dac`	Set the hinge position dac in the log preprocessor. "dac" is the dac value in hex (000-fff).
`hofs path dac`	Enter the zero hinge power dac value into the current display law cal data, and set the corresponding hardware. "path" is 0 for 4 MHz log amp, 1 for 25 MHz. "dac" is the log offset dac in hex (000-fff).
`ifen 0|1`	Enable/disable the IF. A 0 argument will disable the IF. A 1 argument will enable the IF.
`lll29`	Lock the 129 MHz synthesizer to the 565 MHz synthesizer.
`lacq 0|1`	Set log acquisition bit on video processor. A log acquisition is acquired when the bit is changes from 0 to 1. The bit is normally set to 0.
`lcen 0|1`	Enable (1) or disable (0) log correction.
`lcev 0|1`	Sets log correction evaluation mode; "1" enables eval mode, "0" disables eval mode.
`lifd band att_idx`	List flatness data for "band" and "att_idx"
`linh dac`	Enter the hinge position dac number for lin mode into current display law data. "dac" is in hex (000-fff). Also sets the hardware.
`litd`	Print current lo29 and tune dac values for VR.

`livr`	Print contents of the VR registers.
`lo29` *periods*	Count the 29 MHz LO. "periods" specifies the period counter prescale value to use.
`lofs` *val*	Sets log offset to "val" in dB.
`log4` *0|1*	Set the 4 MHz mode of the log processor. An argument of 0 indicates 4 MHz mode; 1 indicates 25 MHz mode.
`logh` *dac*	Enter the hinge position dac number for log mode into current display law data. "dac" is in hex (000-fff). Also sets the hardware.
`lolo`	Count LOlo using a period counter prescale value of 512.
`minb` *bits*	Set the VR resonators to minimum bandwidth mode. "bits" is a hex number, each bit of which sets a single resonator to minbw mode; a high bit (1) selects minbw mode, while a low bit (0) selects normal mode. The bits are decoded as follows: bit 0 resonator 0 bit 1 resonator 1 bit 2 resonator 2 bit 3 resonator 3 bit 4 resonator 4 bit 5 resonator 5
`mono` *0|1*	Set monochrome display on (1) or off (0).
`nres` *rs*	Set RS1/RS2 on the VR. "rs" equals 2*rs1 + rs2; i.e. rs1 is the 2's bit while rs2 is the 1's bit.
`nsge` *0|1*	Enable (1) or disable (0) min/max noise signal in acquisition data. (NSGE bit on video processor).
`offs` *dac*	Set the log offset dac on the log processor. "dac" is a 12-bit hex value (000-fff).
`ofsq`	Print contents of log offset dac on log processor.
`ofsr` *path offset_res*	Enter resolution of the log offset dac ("offset_res") in dB/lsb. "path" indicates the log IF: 0 for 4 MHz; 1 for 25 MHz.
`otda`	Performs a sweep and prints out level of signal in screen units (0-1023). Signal is assumed to be of constant level.
`pkgn` *dac*	Enter peak detector gain dac value into cal data. "dac" is in hex. Also sets the hardware.
`pkmn` *dac*	Enter min peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.
`pkms` *dac*	Enter max sample peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.
`pkmx` *dac*	Enter max peak detector dac value into cal data. "dac" is in hex. Also sets the hardware.
`pkof` *dac*	Enter peak detector offset dac value into cal data. "dac" is in hex. Also sets the hardware.
`prod`	Calculate the preselector slope and offset DAC values for the bands for which sample peaks have been taken with the "prfo" command.

`prfl`	Flush the current list of preselector peak samples taken with the "prfo" command.
`prfo`	Find the line equation relating the preselector slope and offset DACs at the current frequency and reference level. If the line is successfully found, save the line for use by the "prcd" command.
`prio` *task_number task_priority*	Prioritize a task. The argument "task_number" specifies which task to re-prioritize. Valid values are listed in Task.h. The argument "task_priority" specifies the new priority for the task. A task of "0" is the lowest priority, "255" is the highest priority.
`prsl` *band slope offset*	Set the preselector slope and offset DACs for band "band" to "slope" and "offset" respectively. "band" specifies a preselected coax band, and ranges from 1 through 5.
`prsw`	Enter the preselector sweep adjustment mode. Follow the menu presented.
`rblv` *dac*	Set the resbw level dac on the VR. "dac" is the dac value in hex.
`rcnt` *div*	Count the frequency of the selected reference source. "Div" is the value which will be loaded into the divider in the reference oscillator module.
`rcpc`	Recall preselector cal data from NVRAM.
`recl`	Re-calibrate the frequency control system.
`refl` *reflvl*	Set the reference level to "reflvl." Units are whatever the current instrument units are.
`relt` *mode*	Select real time mode: 0 selects digital storage display, 1 or 2 selects double channel real time display.
`rflt`	Read contents of flatness RAM on log processor.
`rlck` *0|1*	Lock or unlock the reference oscillator loop. 0 unlocks, 1 locks.
`rmhz` *0|1*	Turn the 1 MHz output from the reference oscillator module to the period counter on or off. 0 turns on, 1 turns off.
`rord`	Read and report the locked/unlocked and external power detected/not detected status of the reference oscillator module.
`rstr` *SIC_address num_of_bytes*	Receive data from a SIC. The hex argument "SIC_address" specifies which SIC address to read from. The decimal argument "num_of_bytes" specifies how many bytes to read.
`rtra` *0|1*	Enable or disable the reflvl trace. 0 disables trace; 1 enables trace.
`rver`	Determine the hardware version of the reference oscillator which is installed.
`s129` *frequency*	Turn on and set the 129 MHz synthesizer to "frequency".
`satt` *atten_val*	Set the attenuator to "atten_val," in dB. This command sets only the attenuator, bypassing the reference level firmware entirely. Use of this command results in incorrect reference level and marker readouts.
`scal` *0|1*	Calibrate the sweep. "0" does not print results, "1" does.
`schp` *0|1*	Select chop (0) or alt (1) display mode.

`sdbg` *reg1 reg2 reg3*	Set the debug registers in the display amp. "reg1-3" are the registers in hex (0000-ffff).
`sfrn` *N*	Set the fractional N synthesizer value to "N". This control the 565 MHz synthesizer frequency.
`sllo` *value*	Set the "Last LO" bit pattern to "value"
`slol` *frequency precision*	Set LOlo to "frequency" within "precision" Hz.
`stgn` *gain*	Set the VR 1 dB gain steps to "gain," in dB.
`stnd` *type res_num dac*	Enter tune dac value into resonator tracking cal data. "type" is 0 for crystal resonators, 1 for LC. "res_num" is the resonator number (0-5). "dac" is the tune dac value in hex (00-ff). Also sets the hardware.
`svpc`	Save preselector cal data in NVRAM.
`swep`	Do a single sweep.
`swrc` *range mintime*	Set the minimum sweep time for sweep range "range" to "mintime"
`syig` *frequency*	Set the YTO to "frequency".
`tabl` *(FW Vers. 2.1 and earlier)*	Display the current frequency calibration table.
`tabl` *1(FW Vers. 2.2 and later)*	With no argument, display the current frequency calibration table except for the FM Span corrections. With an argument of *1*, includes the FM Span corrections calculated at 50 MHz intervals.
`ttst` *time*	Test the processor timer by delaying "time" seconds between two printed messages.
`tund` *bits*	Load tune dacs with appropriate values from resonator cal data for the specified "bits" value. "bits" is the LC/crystal control byte as defined in the "xlcm" command.
`ul29`	Unlock and turn off the 129 MHz synthesizer.
`unlk` *file*	Remove a file from NVRAM or EEPROM. The file to be removed is specified by the argument "file". To remove NVRAM file "abc", enter "unlk RAM/abc". To remove EEPROM file "def", enter "unlk EEPROM/def".
`uwif` *0|1*	Insert/remove the microwave IF attenuation
`vbws` *source*	Select the source for the video processor; 0 selects internal, 1 selects external.
`vers`	Print the FW version string.
`vout` *type*	Select rear panel video output type: 0 for real time, 1 for composite.

`vpth path_bits`

Set the VR path bits. "path_bits" is a collection of VR switches that the firmware treats as a single register on the VR. "path_bits" is decoded as follows:

0001	29 MHz count (VR 1)
0002	4 MHz path (VR 1)
0004	25 MHz path (VR 1)
0008	NBW for ringdown filter (VR 1)
0010	25 MHz ringdown oscillator (VR 1)
0020	XTAL filter (VR 1)
0040	3 MHz filter (VR 1)
0080	10 MHz filter (VR 1)
0100	29 MHz oscillator on/off (VR 1)
0200	BP filter (VR 3)
0400	LP filter (VR 3)
0800	25 MHz path (VR 3)
1000	4 MHz oscillator (VR 3)

Useful values include:

vpth 901 Route LO 29 signal to output of VR
vpth 532 Turn on ringdown oscillator
vpth 522 Turn off ringdown oscillator

`vpts 0|1` — Set the test bit on the video processor. 1 turns on test mode, 0 turns it off.

`vres dac` — Set the variable bw dac (VBW) on the VR. "dac" is an 8-bit hex number (00-ff).

`vset` — Set up instrument for "xfrq" command.

`vtra 0|1` — Enable or disable vertical cal trace. 0 disables trace, 1 enables trace.

`xfrq` — Count ringdown frequency of xtal resonator. Assumes instrument and VR have been properly set up with the "vset" command.

`xlcm bits`

Set the VR resonators to LC or crystal mode. "bits" is a hex number, each bit of which sets a single resonator to the desired mode; a high bit (1) selects LC mode, while a low bit (0) selects crystal mode. The bits are decoded as follows:

bit 0	resonator 0
bit 1	resonator 1
bit 2	resonator 2
bit 3	resonator 3
bit 4	resonator 4
bit 5	resonator 5

`xstr address num_bytes hex_byte...`

Send hex bytes to a SIC. The SIC address is specified by the hex argument "address". The number of bytes to be transmitted is specified by the decimal argument "num_bytes". The actual data to be sent is entered as hex numbers. The number of hex digits should match the argument "num_bytes". For example; to send hex digits 0x10, 0x43, 0xfe, and 0x32, to SIC address 0xde, enter "xstr de 4 10 43 fe 32"