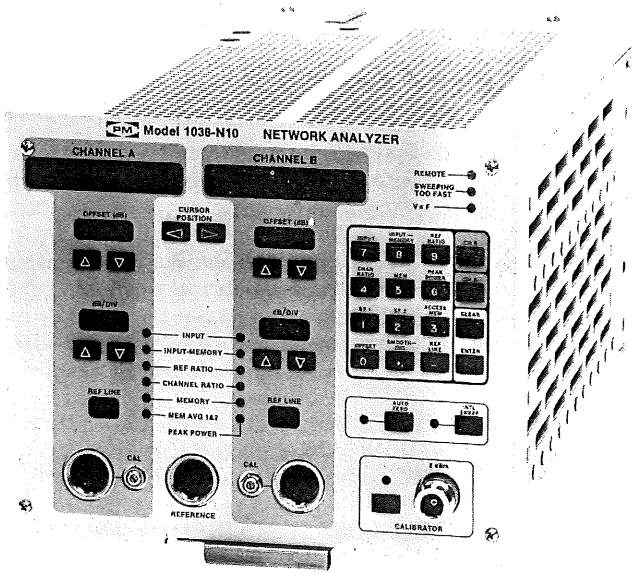
OPERATING AND MAINTENANCE MANUAL



NETWORK ANALYZER MODEL 1038-N10

SERIAL NUMBER 663

WAVETEK PACIFIC MEASUREMENTS, INC

488 TASMAN DRIVE, SUNNYVALE, CALIFORNIA 94089
TEL: (408) 734-5780 TWX: 910-339-9273

1499-15126 Code 18(5-83)

CERTIFICATION

WAVETEK PACIFIC MEASUREMENTS INC. ("WPM") certifies that this instrument was thoroughly tested and inspected and found to meet all its published specifications when it was shipped from the factory. WPM further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

ONE YEAR LIMITED WARRANTY

WAVETEK PACIFIC MEASUREMENTS INC. ("WPM") warrants to the original purchaser, and only the original purchaser, that this instrument will be free from defects in material and workmanship, under normal recommended use and operating conditions, for a period of one year after the date of delivery to the original purchaser.

WPM's obligation under this Warranty is limited to (1) repairing or replacing, at WPM's option, any part or parts (excluding RF diodes, RF connectors, batteries, and fuses) which are returned to WPM in the manner specified below and which, upon inspection by WPM's personnel, are determined to be defective as described above; and (2) calibrating the repaired instrument to current published specifications. If it is determined that the instrument is not defective, a nominal inspection charge will be charged and the instrument will be returned with transportation charges collect. If it is determined that the defect has been caused by misuse and/or abnormal operating conditions or that the instrument is not under Warranty, an estimate will be submitted prior to the commencement of necessary repair and calibration work. If the purchaser does not authorize WPM to commence such repairs within fifteen days after such estimate is submitted, the instrument will be returned to the purchaser transportation charges collect.

WPM's OBLIGATION TO REPAIR OR REPLACE DEFECTIVE PARTS, AS DESCRIBED ABOVE, SHALL BE THE PURCHASER'S EXCLUSIVE REMEDY AND NO OTHER REMEDY SHALL BE AVAILABLE (INCLUDING, BUT NOT LIMITED TO, INCIDENTAL OR CONSEQUENTIAL DAMAGES FOR LOST PROFITS, LOST SALES, OTHER ECONOMIC LOSS, INJURY TO PERSON OR PROPERTY, OR ANY OTHER INCIDENTAL OR CONSEQUENTIAL LOSS SUSTAINED BY THE ORIGINAL PURCHASER OR ANY OTHER PERSON).

THE WARRANTY DESCRIBED ABOVE IS THE ONLY WARRANTY APPLICABLE TO THIS WPM INSTRUMENT AND IS MADE EXPRESSLY IN LIEU OF ANY AND ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR INFRINGEMENT.

WARRANTY PROCEDURE AND SHIPPING INSTRUCTIONS

If any fault develops, the following steps should be taken:

a. Notify WPM immediately, giving model number, serial or part number, code number, and a detailed description of the nature and/or conditions of failure. On receipt of this information, service, operating or shipping instructions will be supplied to you.

b. On receipt of shipping instructions, ship the instrument transportation prepaid to WPM. The instrument should be shipped in the original shipping carton or, if damaged or not available, in a suitable rigid container with the instrument wrapped in paper or plastic and surrounded with at least four inches of cushioning material on all sides. If under Warranty, the instrument will be repaired and returned transportation prepaid.

RECEIVING INSTRUCTIONS

The instrument must be thoroughly inspected immediately upon receipt. All material in the shipping container should be checked against the enclosed packing list. WPM will not be responsible for shortages against the packing list unless notified immediately. Upon receipt of shipment, if there is any visible evidence of damages, make a notation on the way bill of such damage and immediately contact the nearest office of the carrier in your city. If there is evidence of damage after the goods are unpacked, contact the nearest office of the carrier, request an inspection, and save all packing and materials therein until the inspection has been completed. A full report of the damage should be obtained by the carrier's claim agent, and a copy of this report forwarded to WPM. Upon receipt of this report, you will be advised of the disposition of the equipment for repair or replacement. WPM shall have no responsibility for damaged instruments if the above inspection requirements are not complied with. Time is of the essence regarding the above instructions.

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LIST OF ILLUSTRATIONS (Tables and Figures)

1. GENERAL INFORMATION

1.1 Wavetek Pacific Measurements Model 1038-N10 Network Analyzer Plug-In

The Model 1038-N10 Network Analyzer is a microprocessor-based plug-in unit capable of fully automating all scalar measurements of insertion loss/gain, return loss, and absolute power (dBm) measurements. It is designed to be used with the Wavetek Pacific Measurements Model 1038-D14A Mainframe.

All data and function inputs are digital, and can be entered either through the General Purpose Interface Bus (GPIB) or, manually, via the keypad on the front of the unit. The N10 has a self-contained Automemory® for calibration data storage, and also has automatic zero adjustment for accurate low level measurements. Automatic horizontal sweep controls provide an automatic on-screen adjustment to the ramp voltage generated by most sweep generators. A detector calibrator is built into the unit. The unit's reference and channel ratio modes are digitally selectable. Positioning of the reference line on the display is also selectable. The N10 provides a cursor indication on the 1038-D14A display. The cursor can be positioned so that selected numeric readout of measured power can be accomplished for any desired point on the display trace. The readout is independent of the vertical scaling or vertical sensitivity (dB/DIV) factor of whatever channel is being displayed.

1.2 Performance Specifications

Frequency Range	100 kHz to 40 GHz, depending on the detector used (expandable to above 200 GHz with mm band detectors and the Wavetek Pacific Measurements adapter cable).
Input Power Range	76 dB dynamic range, +16 dBm to -60 dBm, available on A & B Channels when the instrument is used with WPM Balanced Detectors. With WPM Single Diode Detectors, the dynamic range is 70 dB. The Single Diode Coaxial Detector's range is +16 dBm to -54 dBm. The range of the Waveguide Detector is +10 dBm to -60 dBm. The dynamic range for the reference channel is from +16 dBm to -30 dBm.
Instrument Accuracy	When coaxial detectors are used, measurement uncertainty will be constant at ±0.2 dB between 15° and 35°C. When the waveguide detector is used, measurement uncertainty will be constant at ±0.5 dB between +3 dBm and -38 dBm at 15° to 35°C ambient temperature. See Figures 1-1 and 1-2 for instrument uncertainty at other input levels and temperatures. Smoothing is available through the keypad for levels below -30 dBm.

Data Resolution: (full range)

Channel A	0.04 dB
Channel B	0.006 dB

Horizontal Memory Resolution:

2048 addressable horizontal points for each channel. (Frequency resolution is dependent upon the range of the sweep generator being used)

Front Panel LED Readout Resolution:

Channel A	0.1 dB
Channel B	0.01 dB

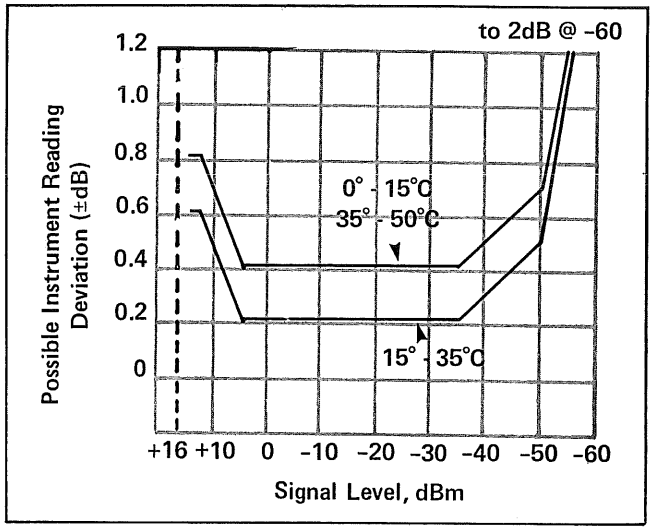


Figure 1-1 N10 Measurement Accuracy with Coaxial Detectors to 26.5 GHz

(An additional 0.2 dB is added to the deviation reading for operation below 30 MHz.)

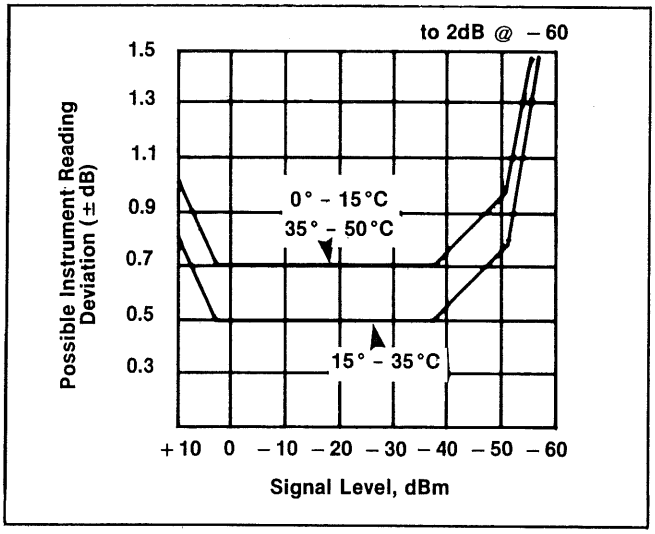


Figure 1-2 N10 Measurement Accuracy with Waveguide Detector from 26.5 to 40 GHz.

IEEE Bus Resolution: Data read out through the IEEE-488 Bus is limited by the bus interface to the following resolutions:

Vertical	0.02 dB on A & B channels when reading plug-in
Horizontal	500 points

CRT Display Controls: (Data can be displayed on the CRT with the following selections available either by direct selection through the data entry keypad or through the IEEE Bus)

Offset	+40 dB to -60 dB (in 0.1 dB increments)
Offset Accuracy	±0.04 dB
Sensitivity	Channel A - 8 steps: 20, 10, 5, 2, 1, 0.5, 0.2, and 0.1 dB/DIV Channel B - 9 steps: 20, 10, 5, 2, 1, 0.5, 0.2, 0.1, and 0.05 dB/DIV

Reference Line	±4 major graticule lines (on the D14A CRT) from the center line.
Cursor	Positioned directly to any of the 500 points available in display memory, or through the keypad or bus to any of 1000 points.

Sweep Inputs

External Sweep

Negative Peak (Sweep Start)	-12 to +2V
P-P Amplitude	5 - 20V
Forward Sweep Time	20 msec to 30 sec
Retrace Time	5 msec to 10 sec
Internal Sweep	60 Hz, nominal
V∝F	From 0 to +2V to 0 to +20V

Calibrator:

Signal Level	0 dBm (1 mW) ±0.06 dB
Frequency	50 MHz ± 2%
Harmonics	< -50 dBc
Source Impedance	50 ohms
Output Match	Better than -30 dB return loss
Connector	Type N Jack Option 02, APC-7

Design and Construction:

To the intent of MIL-T-28800, Type III, Class 5, Style E or F, Color R

Temperature:

Operating	0°C to 50°C (+32°F to +122°F)
Storage	-40°C to +70°C (-40°F to +158°F)

Note

N10 Plug-Ins used in older D14 Mainframes (code 07 and earlier) have the following operating limits:

Unmodified	*0° to 40°C (+32° to +104°F)*
*Modified**	*0° to 45°C (+32° to +113°F)*

**Contact factory for modification details.*

Power Requirements: (for D14A Mainframe and N10 system)

Approximately 100 VA at 50-440 Hz, and 100, 120, 220, 240 VAC ± 10%

Dimension and Weight: (H x W x D)

168 x 203 x 324 mm
(6-5/8 x 8 x 12-3/4 in)

Net Weight	4.5 kg (10 lbs)
Shipping Weight	7.3 kg (16 lbs)

1.2.1 Detector Specifications

Three types of detectors are available from Wavetek Pacific Measurements for use with the 1038-N10 and 1038-NS20 systems. These include the balanced or dual diode type, the single diode type, and the balanced element waveguide type. All of the detectors have 50 ohm impedance, and 50 to 75 ohm adapters are available for low frequency applications with the coaxial detectors. Coaxial detectors cover frequency ranges from 1MHz to 18.5GHz or from 1MHz to 26.5 GHz (useful to 34.0GHz), and can be ordered with type N, APC7, or APC3.5 connectors. Frequencies down to 100kHz are available on special order. The waveguide detector has a UG-599/U (WR28) connector, and covers the frequency range from 26.5 to 40.0GHz. See Table 1-A for part numbers and general characteristics of the seven available detectors. If a diode replacement is ever required, Table 1-A also lists the specific Diode Replacement Kit part number that should be ordered.

Included in the detector characteristics and operating parameters are the following:

Balanced – Balanced detectors provide 76 dB dynamic range, attenuate even order harmonics, have low thermal drift, and are temperature compensated. Low level dc signals at the detector input are zeroed out automatically due to the differential output. See Figure 1-1 for linearity from 30MHz to 26.5GHz, Table 1-B for flatness (maximum total variation), and Table 1-C for return loss specifications.

Single Diode – The single diode coaxial detector provides 70 dB of dynamic range and is temperature compensated. See Figure 1-1 for linearity from 30MHz to 26.5GHz, Table 1-B for flatness (maximum total variation), and Table 1-C for return loss specifications.

Balanced Element Waveguide – The balanced element waveguide detector is similar to the single diode coaxial detector in that it has 70 dB of dynamic range and is temperature compensated. The waveguide detector also contains a linear-

Table 1-A
General Detector Characteristics

Part Number	Frequency Range	Absolute Maximum Power Input Without Damage (Peak or CW)	Connector	Type	Diode Replacement Kits
15176	1MHz to 18.5GHz	200 mW	Type N	Balanced	15360
15177	1MHz to 18.5GHz	200 mW	APC7	Balanced	15360
15181	1MHz to 26.5GHz*	200 mW	APC3.5**	Single Diode	15363
15237	1MHz to 18.5GHz	200 mW	Type N	Single Diode	15362
15284	1MHz to 18.5GHz	200 mW	APC7	Single Diode	15362
15285	1MHz to 26.5GHz	200 mW	APC3.5**	Balanced	15361
15882	26.5 to 40.0GHz	100 mW	UG-599/U (WR28)	Waveguide	Not Field Replaceable

*Information to 34.0GHz provided on special order. **Compatible with SMA connector.

ity resistor when used with the N10 or NS20 systems. See Figure 1-2 for linearity from 26.5 to 40.0GHz, Table 1-B for flatness (maximum total variation), and Table 1-C for return loss specifications.

Additional Specifications

Frequency Response
Curve Data Accuracy:

Coaxial Detectors: The uncertainty of calibration at 1 mW (0 dBm) is 3% to 18.5GHz and 5% to 26.5GHz.

Waveguide Detectors: The relative calibration curve uncertainty is 5% from 26.5 to 40.0GHz.

Physical Specifications:

Cable Length: 1.5m (3 ft.)
Weight: Approx. 230 gm (8 oz.)

Temperature Range:

Operating: 0° to 50°C (+32° to +122°F)
Storage: -40° to +65°C (-40° to +149°F)

1.2.1.1 Detector Performance Evaluation

In most cases, any deterioration in detector performance will result in improper tracking with changes in signal level (i.e., a deficiency in linearity). In rare cases, there can be a change in return loss (VSWR). The test described here will check for linearity or VSWR degradation.

Standard procedures can be used to check return loss. The measurement of return loss up to a frequency of 34.0GHz requires considerable care if measurement errors are to be avoided. It is highly recommended that a slotted line be used, or to use couplers or bridges with open/short calibration and an air line during the measurement procedure.

To check linearity, the power meter or analyzer compatible with the detectors must be within proper calibration. To supply power to the detector, a source with a power output between 0 and 16 dBm must be used. For coaxial detectors, this is usually a 30 to 50MHz source of 40 mW. For waveguide detectors, a 10 mW source in the frequency band of the waveguide will be required. The source must have harmonics down at least 50 dB, and a well matched step attenuator (10 dB steps, return loss greater than 20 dB, and a 70 dB range). Due to the tightness of the linearity specification for coaxial detectors, the coaxial attenuator must have a correction chart. This chart must show the attenuation within 0.03 dB down to -40 dBm, and within 0.1 dB below -40 dBm.

Connect the attenuator between the detector and the source. Starting with 0 attenuation, step the attenuator in 10 dB steps, and check the resultant power meter readings against the linearity curves (Figures 1-1 and 1-2) shown on the preceding pages. Use Figure 1-1 if checking coaxial detectors, or Figure 1-2 if checking waveguide detectors.

Table 1-B
Detector Flatness (Maximum Total Variation)

	To 18.5GHz	To 26.5GHz	To 34.0GHz	To 40.0GHz
Single Diode APC3.5	1.0dB	2.0dB	3.0dB	–
Single Diode Type N or APC7	1.0dB	2.0dB	–	–
Balanced (any connector below 18.5GHz. APC3.5 above 18.5GHz)	1.5dB	2.0dB	–	–
Waveguide	–	–	4.0dB	4.0dB

Table 1-C
Detector Return Loss Specifications (in dB):

	To 2 GHz	To 12.4 GHz	To 18 GHz	To 26.5 GHz	To 34 GHz	To 40 GHz
Balanced (any connector below 18.5GHz. APC3.5 above 18.5GHz.)	20	18	16	10	–	–
Single APC3.5	25	20	16	14	10	–
Single Type N or APC7	25	20	18	–	–	–
Waveguide	–	–	–	–	10	10

2. INITIAL INSTRUCTIONS

2.1 Receiving Instructions

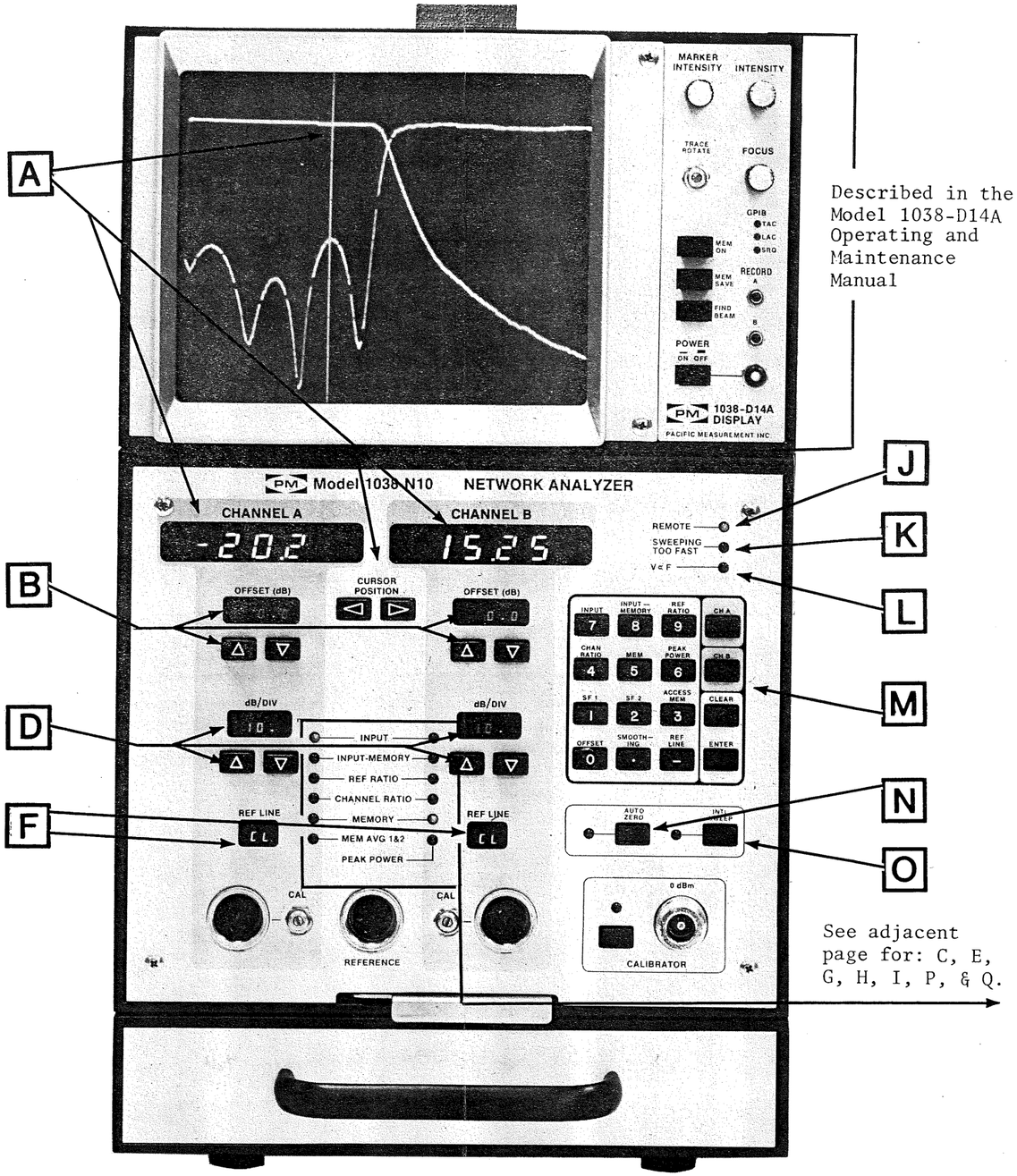
Inspect the Plug-In and any detectors for shipping damage. Also see the "Receiving Instructions" Section of the Warranty statement on page i (located on the back of the front page of this manual).

CAUTION: Be sure that all portions of the shipment are located and removed before discarding the shipping containers.

The Performance Verification Tests of Section 6 of this manual can be used for receiving inspection testing if required.

2.2 Returning the Plug-In or Detectors

If it is felt that the Plug-In and/or any detectors should be returned to Wavetek Pacific Measurements for any reason, it is mandatory that the Wavetek Pacific Measurements Customer Service Department be contacted prior to returning to receive a Warranty Return Authorization. The telephone number is (408) 734-5780 extension 260 or Telex (910) 339-9273. See the shipping instructions on the Warranty statement on page i at the front of this manual.



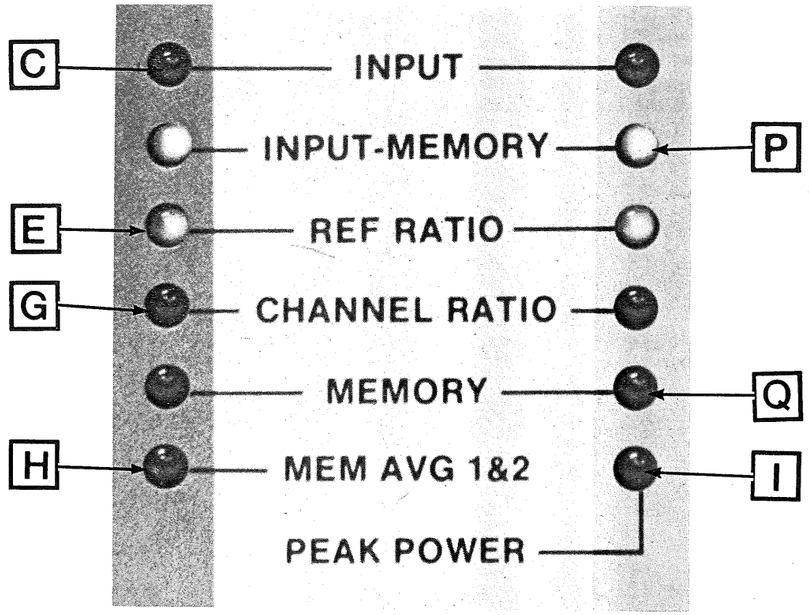


Figure 3-1 Model 1038-N10 Network Analyzer Installed in the Model 1038-D14A Mainframe
(See paragraph 3.5.2 for description of the above delineated controls and indicators.)

3. OPERATION

3.1 Introduction

The Model 1038-N10 Network Analyzer Plug-In is designed to be used in the Model 1038-D14A or D14 Mainframe. The purpose of this section of the manual is to provide detailed operating instructions only for the N10 Plug-In. A separate instruction manual contains operating instructions for the Model 1038-D14A or D14 Mainframe and CRT display.

3.2 Installation

WARNING: DO NOT INSTALL OR REMOVE THE N10 PLUG-IN WHILE THE D14A POWER IS TURNED ON.

Prior to installation, it should be ascertained what tests are to be conducted and what basic test parameters are to be used. This is necessary because there are two internal switches in the N10 unit that must be preset before making certain measurements. These switches are labeled on the top of the N10 housing, and are accessible through holes in the cover as indicated by the labels.

If a sweep generator is used wherein the RF is turned off (zero power) during the sweeper retrace period, the external Auto Zero function can be disabled if desired. (The internal Auto Zero is always on.) If the sweep generator has a voltage proportional to frequency (V ∝ F) capability and it is desired to use this function (described in Section 3.5.2.L), the N10 must be switched to be able to accept this input. Switch A11S1 is used to preset both the Auto Zero and V ∝ F functions. Figure 3-2 depicts the label affixed to the top of the N10 housing.

SWITCH POS.	DET. AMP. AUTO ZERO MODE	MEMORY MODE
0	FRONT PANEL	V ~ F
1	*INTERNAL	V ~ F
2	FRONT PANEL	V ~ SWEEP
3	*INTERNAL	V ~ SWEEP

*RF MUST BE < −75dBm DURING RETRACE

(to sw. A11S1)

Figure 3-2. Auto Zero and V ∝ F Switch Settings

The function of each switch position is defined as follows:

"0" – Turns ON the external Auto Zero and V ∝ F

"1" – Turns OFF the external Auto Zero and leaves ON the V ∝ F

"2" – Turns ON the external Auto Zero and turns OFF the V ∝ F

"3" – Turns OFF the external Auto Zero and turns OFF the V ∝ F

See Section 3.9.3, third paragraph, for a further definition of the usage of the V ∝ F input feature.

The second switch to be considered prior to installing the N10 plug-in is the Peak Power Sensitivity setting (A10S1). Figure 3-3 depicts the label affixed to the top of the N10 housing.

PEAK POWER SENSITIVITY

SWITCH POS.	mV/dB
2	10
4	100

A CHAN (to sw. A9S1) B CHAN (to sw. A10S1)

Figure 3-3. Power Sensitivity Settings When Using 1018B Input

If it is planned to use the output of the Pacific Measurements Model 1018B Peak Power Meter when making measurements, switch A10S1 must be set to the desired mV/dB sensitivity, as shown. Since Peak Power is measured only through channel B of the N10, only the "B CHAN" switch is of interest at this time. The "A CHAN" switch (A9S1) is used later when accomplishing certain internal calibration procedures within the N10 unit.

3.2.1 V ∝ F Sensitivity Selection Considerations

When the instrument is shipped from the factory, the sensitivity of the V∝F input is set to allow voltages up to 20 V to be used for memory reference. Since there are 2000 memory locations, a new location will be accessed for each 10 mV that the voltage increases. In most cases this will provide sufficient resolution. However, if a smaller voltage will be used during memorization, it is possible to select greater sensitivity. This should be done if the memory resolution is found to be insufficient for the application. (Note that most applications do not require the maximum memory resolution.) In order to select the sensitivity, remove the instrument from the mainframe and remove the top cover. At the upper left hand corner of board A8 there is a switch (S1). Using this switch, select the desired sensitivity by reference to Table 3-A below:

SWITCH NUMBER				MAXIMUM VOLTAGE RANGE
1	2	3	4	VOLTS
X	OPEN	OPEN	CLOSED	20
X	CLOSED	CLOSED	CLOSED	10
X	CLOSED	OPEN	CLOSED	5
X	CLOSED	CLOSED	OPEN	3.3
X	CLOSED	OPEN	OPEN	2.5

Note: X means that either position is acceptable.

Table 3-A. V∝F Sensitivity Settings

Example:

Suppose that a swept signal source will be adjusted to cover the range from 1.5 GHz to 9 GHz during the calibration memorization process, and that the source has an output voltage of 1V/GHz. Its maximum voltage will be 9V, corresponding to the top end of the band (9 GHz). In this case, either the 10 or 20 volt range could be selected for the memory to work properly. The best memory resolution will be obtained by selecting the 10V range; this is accomplished by setting switches 2, 3 and 4 closed. In most cases, using the normal 20V range would give sufficient resolution and resetting the switches would be unnecessary.

3.2.2 Physical Installation

After the switch positions have been selected and it is desired to physically install the N10 unit into the 1038-D14A Mainframe, locate the latching lever at the bottom center of the N10 unit. This lever must be pulled straight out before the plug-in is pushed all of the way into the Mainframe. After the plug-in can be pushed no further, the lever is moved to the right. This mates the plug-in unit into the connector at the rear and locks it into place. Use care in inserting the plug-in and be sure that the connector in the rear lines up with the connector on the back of the plug-in. This is particularly important when the 1038-N10 configuration is first set up, because shipping damage could cause a misalignment situation.

3.3 Operating Limitations

Care should always be exercised when using or storing the 1038-N10 unit, that it is kept within the temperature range specified in Section 1.2 (Performance Specifications). Attempting to use or store the instrument where the temperature might fall outside of the specified range could cause erratic readings or a complete failure of the instrument. Adequate ventilation should always be considered when using the instrument. If a rack mount configuration is used, there should be at least one inch of open space left above and below the unit. If the instrument is used on a bench or in any enclosed area, sufficient clearance for air flow should always be left on the sides and back of the unit.

3.4 Detector Connection

WARNING: ANY DETECTOR CAN BE EASILY DAMAGED IF TOO MUCH RF POWER IS APPLIED TO IT. BE SURE TO OBSERVE THE WARNING AFFIXED TO THE DETECTOR REGARDING ITS MAXIMUM POWER HANDLING CAPABILITY.

In order to use the N10 Plug-In, one to three detectors are required. These connect to the three front panel female multi-pin receptacles. The connectors on the detector cables have keys on the plastic portion of the connector. These keys must mate with the keyways in the front panel receptacles before pushing the connectors into the receptacles. Once the detector cable connectors are seated in the front panel receptacles, the outer portion of the male connector can be screwed in to provide a good mechanical connection.

3.5 Front Panel Controls and Indicators

3.5.1 General

The various displays on the front of the Model 1038-N10 Network Analyzer Plug-In unit are designed to provide information at a glance regarding instrument status, as well as sharp, clear readout of measurement data. When all displays pertaining to a particular channel are out, it means that that channel is turned off. When any of the channel displays are flashing, it indicates that the N10 is waiting for further action by the operator to complete a general command sequence. If a single indicator is flashing (such as "MEM AVG 1&2"), it means that a particular function is in progress and requires operator action (such as changing from a short to an open condition during calibration of a test set-up) to complete the function. Additionally, the instrument will tell the operator if an improper or out of sequence entry has been made by displaying an "ERROR" indication in the appropriate LED display window.

3.5.2 Description of Controls & Indicators

(See Figure 3-1 for the location of the following controls and indicators.)

A. Digital readouts indicate the magnitude of the displayed signal at the Cursor location. If the N10 unit is used with a D14A Mainframe, it will be noted upon initial turn-on of the instrument that the Cursor (a full-screen-height vertical line) is located approximately one-half of a division in from the right side of the CRT display. If the N10 is installed in a 1038-D14 (no suffix) Mainframe, the Cursor will be a ½ division, negative-going pulse. The start-up location will be about ½ division in from the right side of the CRT display. When measurements are taken, the cursor can be moved to wherever it is desired to take a power reading on the CRT display by depressing the CURSOR POSITION (◁ ▷) buttons. The channel LED readouts will then display the dB or dBm level at that point. If the Cursor is moved off either edge of the CRT display, it will reappear on the trace at the opposite side of the display.

B. The Offset function permits the input signal to be moved to the reference line, with the amount of polarity of the required offset indicated by the OFFSET (dB) LED display. This reading is an indication of the difference (in dB) between the signal and the reference. For example, if 0 dBm is used as a reference and an offset of -12 dB moves the signal to the zero reference line, the level is -12 dBm. Offset △ and ▽ buttons allow movement of the offset in 0.1 dB increments (Note that these buttons indicate the direction of movement of the CRT display, *not* increasing or decreasing offset.) Holding the button down causes the trace to move with increasing speed to the desired location. Positioning of the Offset is also controllable through use of the keypad, as will be described in Section 3.6.2.d.

C. The "Input" indication shows that a channel is receiving data from its associated detector. This data is displayed in dBm. The channel is indicated by the illumination of the light on the A or B channel side of the listing.

D. The dB/DIV LED display indicates the vertical sensitivity of signals being displayed on the CRT. The N10 initially presents a display of 10 dB per major CRT graticule, but this can be reset down to 0.1 dB/DIV for channel A and 0.05 dB/DIV for channel B using the increment/decrement buttons (△ ▽) located beneath the dB/DIV LED display. For channel A, the available sensitivity settings are:

20, 10, 5, 2, 1, 0.5, 0.2, and 0.1 dB/DIV

The channel B sequence is similar, except that the sensitivity of channel B will go to 0.05 dB/DIV.

When using the GPIB interface, channel A sensitivity will go to 0.05 dB/DIV.

E. The "Ref Ratio" indication shows that the signal from the reference channel is being subtracted from the input measurement. For example, if the Input indicator is on and the Ref Ratio indicator is also on, it means that the unit is displaying the Input signal minus the Reference signal. If just the Ref Ratio indication is on, the channel display is showing the negative of the Reference Channel (-Ref).

F. The Reference Line (REF LINE) function enables the selection of a major horizontal line on the CRT graticule that will serve as a 0 dB reference for a particular measurement. That is, if a 0 dB signal were applied to the input, it would lie on the line indicated by the REF LINE readout. Any offset is in relation to the selected position of the REF LINE. The reference line is also the line about which the CRT trace expands as successively greater display sensitivities are selected. The initial location of the reference line on the CRT graticule is the center line (CL), and wherever the REF LINE is positioned is considered zero. The REF LINE LED display shows the number of horizontal lines that the reference is displaced from center. Since the Reference Line location is continuously indicated, it is not necessary to try and remember its location. (A minus [-] indication means below the center line.) The "Ref Line" button on the keypad is used to position the reference, and will be described in Section 3.6.2.e.

G. The "Channel Ratio" indication (similar to the Ref Ratio) shows that the opposite channel's signal is being sub-

tracted from the measurement when both input lights are on. If the Channel Ratio indicator is the only light that is illuminated, the negative of the opposite channel (whose input light is on) is being displayed.

H. The "Mem Avg 1&2" indication shows that the channel A (only) access memory operation is in progress. When the change is made from a short to an open condition while calibrating a test set-up, "ENTER" must be pressed again to place into memory the result of the automatic averaging of the open and short conditions.

I. The "Peak Power" indication (channel B only) shows (when lighted) that the Peak Power mode has been selected. The Peak Power mode allows the analog output of a Model 1018B Power Meter to be used instead of the front panel detector input of channel B. The 1018B input can be memorized or ratioed similar to any other input and swept peak power measurements can be made. The 1018B is connected to the Aux 3 BNC connection at the rear of the 1038-D14A Mainframe.

J. The "Remote" light shows that the operation of the 1038-N10 is under IEEE Bus (GPIB) control.

K. "Sweeping Too Fast". At each detected signal level, the N10 generates a voltage proportional to the maximum allowable sweep speed that will not distort the input signal. This voltage is compared with a voltage proportional to the actual sweep speed. If the actual sweep voltage is higher than the maximum allowable voltage, this indicates a "Sweeping Too Fast" condition and the light will turn on.

Since this function is strongly level dependent, it is particularly necessary to slow the sweep at low signal levels.

L. The "V $\propto$ F" light indicates that the voltage proportional to frequency mode has been selected. This mode can be utilized when a sweep generator with a V $\propto$ F output is used. Using the V $\propto$ F capability, frequency response can be memorized over a very broad range (e.g., 2 - 18 GHz), and then a device tested over a very narrow portion of that range (e.g., 3.7 - 4.2 GHz). This gives the operator the ability to change the sweep end points at will and still preserve calibration. To use the V $\propto$ F feature, it is necessary to set a switch inside the N10 as described in Section 3.2.

M. The Keypad allows rapid selection of each channel's function, control of the memory, and precise entry of Offset Reference Line, and Cursor positioning information. These and other functions will be described in detail in Section 3.6 of this manual.

N. The Automatic Zero (AUTO ZERO) feature is available whenever it becomes necessary to command the N10 to re-zero itself. As previously described in Section 3.2, an internal switch (A11S1) is used if it is desired to disable the external Auto Zero during the course of a test. (Note that the RF must be < -75dBm during the retrace period to use this Auto Zero mode.) If the internal switch has been used to turn off the external Auto Zero, this also disables the front panel switch and only the internal Auto Zero will be operative until the switch has been reset. As long as A11S1 is set to positions 0 or 2, the Auto Zero will be activated and can be accessed externally whenever the front panel switch is pressed. The Auto Zero function operates automatically, regardless of switch settings, whenever the N10 is first turned on. The light next to the front panel switch will come on for about 8 seconds and then go out. This is to allow the N10 to automatically calibrate itself with a zero input. No RF should be applied at this time. (The Auto Zero sequence will not terminate and the "Auto Zero" light will begin to flash if there is any RF present at turn-on.)

The purpose of the Auto Zero feature is to remove any offsets caused by thermal EMF's external to the N10 unit. When working at very low signal levels (< -30 dBm), the Auto Zero switch should be used frequently to prevent possible measurement errors from accumulating.

O. The Internal Sweep (INTL SWEEP) function should be ON when no sweep signal is being received from an external source. The Internal Sweep can be used when it is desired to view the contents of the memory in real time. The Internal Sweep is also useful when the input signal is a CW signal and the N10 is being used as a power meter.

P. The "Input-Memory" indication shows that the memory is being subtracted (in dB) from the input signal of the channel under which the light is illuminated.

Q. The "Memory" indication shows that the contents of memory are being displayed. It also flashes after the ACCESS MEMORY key has been pressed to indicate that the unit is ready to memorize.

3.6 Keypad Functions

3.6.1 General

Use of the Keypad (Figure 3-4) allows the operator to easily, rapidly, and precisely manually select and control all of the functions of the N10. This is largely due to the fact that a logical progression is always followed when entering a command sequence. First the desired channel is selected, then the desired function, then any numbers that may be required to be used with the desired function, and finally the ENTER command to initiate the selected function. As previously described in paragraph 3.5.1, the N10 keeps the operator informed, at each step of the command sequence, that further action is required (flashing displays) or that a command has been improperly entered (ERROR indication on the appropriate display). Although most of the keys are multi-functional, a "second function" key is not required due to the manner in which the N10 is programmed.

This section will describe how to implement each of the functions capable of being controlled through use of the keypad. All of these functions are also remotely controllable through the GPIB, as defined in Section 4 of this manual.

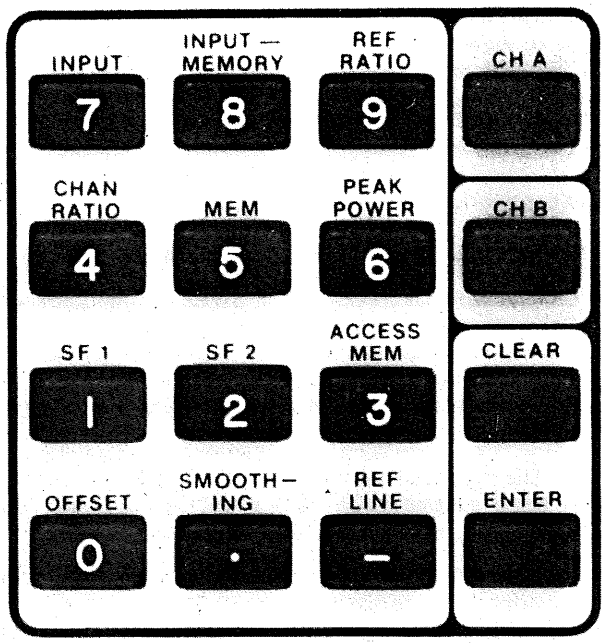
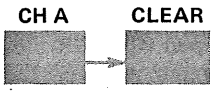


Figure 3-4 N10 Front Panel Keyboard

3.6.2 Description of Keypad Functions

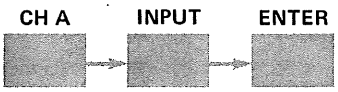
a. **CLEAR.** The Clear button will stop any function that is in process and that it is desired to terminate. The Clear button is also used as an "off" button when the N10 is first turned on if only one channel is being used and the other channel has no detector attached. The unused channel *must* be turned OFF to allow the N10 to properly Auto Zero itself. Assuming that only channel B is to be used, channel A would be turned OFF as soon as the N10 is turned on. This is accomplished on the keypad as follows:



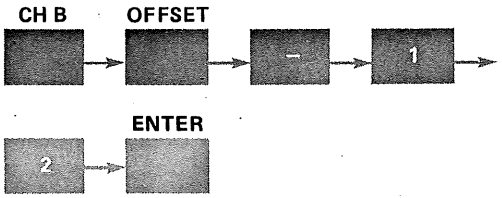
(It is not necessary to use the "ENTER" command when performing the CLEAR function.)

b. **ENTER.** The Enter button is depressed as a final action to actuate any of the keypad commands other than Clear, Ref Line, or SF2.

c. **INPUT.** The Input button is used to display the incoming signal (in dBm) from the detector associated with either channel. For channel A, the keypad sequence would be:



d. **OFFSET.** The Offset function has been described in paragraph 3.5.2.B. To control this function from the keypad using the example given in paragraph 3.5.2.B, the sequence would be (assuming channel B):

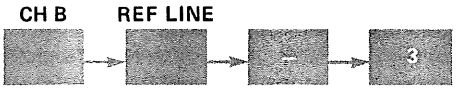


The Offset will follow the dB/DIV (see paragraph 3.5.2.D) in its positioning on the CRT display. For instance, if the dB/DIV were set to 0.05 and an offset of -0.1 were entered, the signal displayed would move upward (positive) two major divisions (0.1/0.05 = 2).

e. **REF LINE.** The Reference Line function has been described in paragraph 3.5.2.F. To change the location of the Reference Line using the keypad, the following operations are performed (assume 3 divisions of positive displacement of channel B):

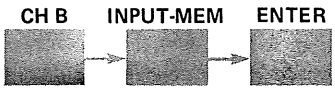
(It is not necessary to use the "ENTER" command when performing the REF LINE function.)

If it were desired to move the Reference Line down (negative), the keypad action would be:

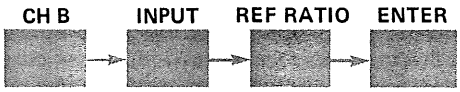


f. **INPUT-MEMORY.** The Input minus Memory button will cause the display of the input signal with the contents of the memory subtracted (in dB).

To display the Input minus Memory function, perform the following keypad operations (assume channel B):



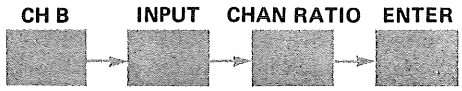
g. **REF RATIO.** When testing at signal levels of -30 dBm or higher, the Reference Ration function can be used to cause the reference detector input to be ratioed to the input signal of the desired channel. This function is generally used as an aid in calibrating the swept measurement system. For channel B, the keypad sequence is:



The "Ref Ratio" and "Input-Memory" lights will turn on to indicate that the input is being ratioed (subtracted in dB) to the reference signal and the memory.

h. **CHAN RATIO.** The Channel Ratio function is similar to the reference ratio function except, instead of ratioing to the reference channel input, the signals being applied to channel A or B can be ratioed to each other. For instance, channel B can be ratioed to channel A (i.e., display dB = 10 log B/A). Channel A has more sensitivity (-60 dBm versus -30 dBm) than the reference channel, so this would be a useful function at low signal levels. The ratioed channel (A in the above case) becomes an accurate power meter, so

that the input power levels to a device are easily set. The keypad sequence is:



The ratio of A/B can also be performed by substituting channel A for channel B.

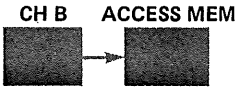
i. **MEM.** Use of the Memory button will cause the display of the contents of the memory of the selected channel. The memory is independent of the dB/DIV sensitivity setting and records over the entire dynamic range of the instrument. To display the contents of channel B memory, the keypad sequence is:

j. **PEAK POWER.** The Peak Power function has been described in paragraph 3.5.2.I. To cause the display of the Peak Power input on the CRT, perform the following keypad operations (channel B only):

Note:

Peak Power can be substituted for the input in the REF RATIO, CHAN RATIO, and the MEMORIZE functions.

k. **ACCESS MEM.** Use of the Access Memory function prepares the unit for storing an input signal in the memory of either channel. To prepare the N10 to memorize in channel B:



The "Memory" LED will start flashing.

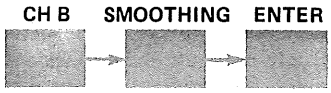
Note:

If one channel is turned off (no detector attached), the cursor data reading will appear on that channel. This is normal, and the reading will disappear as soon as the memorizing is completed.

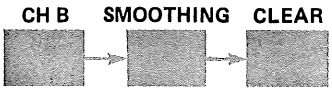
Pressing will then cause the instrument to memorize during the next *full* sweep. When the information is memorized, the flashing "Memory" LED will go out and the "Input-Memory" LED will light. When calibrating Channel A, the "Mem Avg 1&2" light will flash the first time "ENTER" is pressed. After changing from the open to the short condition, "ENTER is pressed again and "Input-Memory" will light.

l. **SMOOTHING.** The Smoothing button will cause the reduction of the bandwidth of the log amplifier on all dB/DIV settings. At low signal levels (below -30 dBm), there are random variations in signal amplitude due to noise. The Smoothing function reduces the bandwidth of the log amplifier for signals below -30 dBm causing the response to be slower at these low signal levels. This means that the displayed amplitude will be incorrect if rapid variations are displayed at excessive sweep speeds.

Excessive sweep speed will be indicated by the illumination of the "Sweeping Too Fast" light on the front panel, and can be checked by slowing the sweep rate of the sweep generator and observing whether the shape of the display changes. The speed of the sweeper must be such that there is no distortion in the displayed signal. The keypad sequence to utilize the smoothing function is:

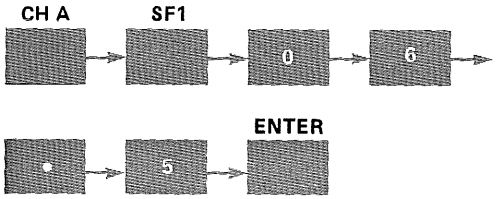


To terminate the smoothing function:

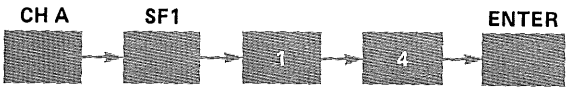


m. **SF1.** The Special Function One button will allow the initiation of ten different sub-functions. These consist of the following:

0 – Used for positioning of the cursor. For example, pressing "6.5" after pressing "SF1" and "0" would move the cursor 6.5 divisions to the right from the left side of the CRT graticule. The keypad sequence would be (assume channel A):

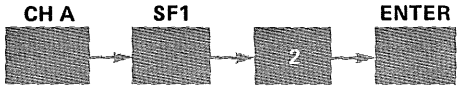


1 – Used for selection of vertical sensitivity. Nine sensitivity settings are available (0 through 8) to cover the dB/DIV increments of both channel A and channel B. A "0" will select 0.05 dB/DIV on either channel. "1" will select 0.1 dB/DIV on either channel, "2" will select 0.2 dB/DIV on either channel, "3" will select 0.5 dB/DIV on either channel, and so on (as listed in paragraph 3.5.2.D) up to "8" which will select 20 dB/DIV on either channel. For example, if 1 dB/DIV is desired as the sensitivity for channel A, the keypad sequence would be:

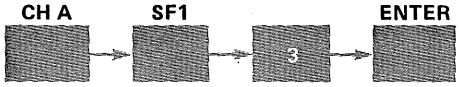


2 – Special function One – 2 Initiates a self-test function within the 1038-N10 unit. The general condition of the analog circuitry associated with the channel of interest is tested. A healthy condition is indicated by a reading of 3 to 9 dBm on the channel LED display. Both channels must be in the "Input" mode as described in Section 3.6.2.c. If it were desired to check

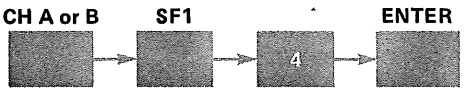
the condition of the electronics associated with channel A, the keypad sequence would be:



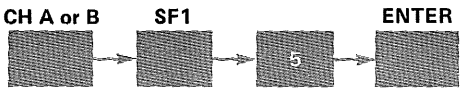
3 – Special Function One – 3 is used to terminate the self-test function. The keypad sequence is:



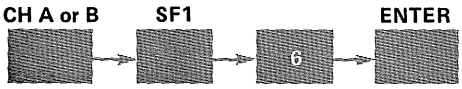
4 – Special Function One – 4 is used to enable the input from the GPIB interface or, if option 04 has not been installed, to enable external ratio inputs. All other inputs are disabled. The keypad sequence is:



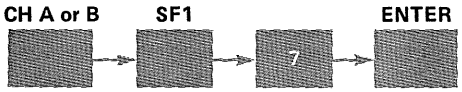
5 – Special Function One – 5 is used to disable the external sweep scaling circuitry. It is to be used only after the sweep width has become stable, and can be used for a period of several minutes of testing before re-enabling. The keypad sequence is:



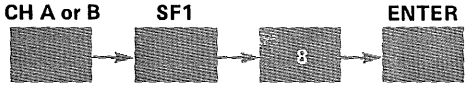
6 – Special Function One – 6 re-enables the automatic sweep scaling circuitry. The keypad sequence is:



7 – Special Function One – 7 is used essentially as the opposite of SF1 – 4 in that it disables the input from the GPIB interface or from external ratio inputs and enables all other inputs. The keypad sequence is:



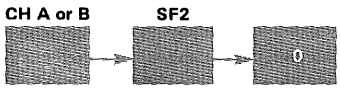
8 – Special Function One – 8 causes the disconnection of all inputs from the display circuits. It also allows the selection of any combination of inputs. The keypad sequence is:



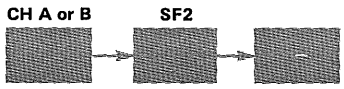
9 – Special Function One – 9 is used to manually lock out all of the controls on the N10 with the exception of the cursor and the numbers 0 through 9 on the keypad. When "CH B" then "SF1" then "9" are pressed, any 0 through 9 digit pressed after that will go through the GPIB and signal for an SRQ (operator action). As a part of the SRQ, the number of the key (0 - 9) is presented to the computer and can be used to call up any of 10 test programs for example. SF1-9 is used when the N10 is interconnected to the GPIB or if it is desired to lock out the front panel in a production application.

n. SF2. Use of the Special Function Two button initiates two different sub-functions. These consist of the following:

0 – Used to toggle the cursor. SF2-0 will either cause the cursor to appear on the display if it is not already there, or to disappear if it is present. The keypad sequence is:



– – The "minus" function is used when it is desired to completely reset the instrument. All functions are reset to the same condition as when the N10 was first turned on. The keypad sequence is:



3.7 Front Panel Reference Connection and Calibrator Output Functions

The REFERENCE detector is connected to a coupler or some other system reference point. The detector is used to sense any variation in the power at the coupler or reference point. The purpose of the reference is to correct for unwanted sweeper drift and any other undesired characteristics that might distort the reading. It does this by tracking variations in the output power level of the sweep generator and other components of the system. As a result, the 1038-N10 display will not show any variations in level which might come before the reference point, but display only the difference between the reference signal and the input signal.

The CALIBRATOR connection provides an accurate 0 dBm output for detector calibration. It is switch controlled and should always be OFF when not in use to prevent any interference from its output. Use of the CALIBRATOR will be described in Section 3.9.2 of this manual.

3.8 Detector Characteristics

Three types of RF detectors are available for use with the N10 Plug-In. These are the Balanced (dual diode) detector, the Single Diode detector (SDD), and the Balanced Element Waveguide detector. Balanced detectors are used for power measurements where it is expected to be measuring very low power levels (–60 dBm). This is because it is far more responsive, has 3 dB more output, and is less sensitive to even harmonics and thermal offsets than the SDD.

The SDD has better frequency response and better return loss performance than the Balanced detector. For this reason, the SDD is generally used where gain and sensitivity are not as important, such as the sensor for the reference channel of the instrument when performing a calibration routine.

All RF detectors used with the N10 are equipped with RF connectors for connection to sources of RF power. Depending on the connector type and the characteristics of

the detector, the maximum frequency for each detector will be different. Be sure to check the specifications for the detector before using it at the highest RF frequencies. Each detector has slightly different detection characteristics from another. Due to the unique compensation circuitry of the N10 unit, *detectors can be interchanged at will and published accuracy specifications will be met.*

An adapter cable is available for connecting detectors or devices with built-in detectors having BNC or SMC output connections (i.e., waveguide detectors or autotesters) to any of the detector inputs of the N10. The use of the special cable is recommended because it contains a low-pass filter to isolate the cable from the RF signal. It also has a temperature compensation sensor. The temperature sensor is close to the BNC connector in the brass block to which the connector is mounted. Care should always be taken to keep the adapter temperature the same as the detector to which it is attached. This will ensure that temperature variations in the detector can be compensated by the N10 Plug-In.

3.9 Operating Procedures

3.9.1 Initial Turn-On Procedure

Connect detector(s) to Channel A, Channel B, or A and B for simultaneous measurement. (Also REFERENCE if required for the particular measurement to be made.) As a general rule, when making individual or simultaneous measurements, Channel A is used for return loss and Channel B is used for insertion loss/gain.

There must not be any RF power applied to the detectors, or the instrument will not be able to Auto Zero itself.

Note:

Be sure that a sweep signal (external or internal) is present or the LED readouts will not give a steady indication.

Turn the mainframe power ON. If only one channel is to be used and there is no detector attached to the other channel, the unused channel must be turned OFF (i.e., if channel A is not used, press CH A then CLEAR keys) to allow the N10 to properly Auto Zero. The AUTO ZERO light will stay on for 8 seconds while the N10 automatically calibrates itself with a zero input. The AUTO ZERO light will turn off when the unit is ready for operation.

Note:

If at any time the unit must be turned OFF, be sure to wait at least 10 seconds before turning it on again. This is required to assure proper readings when usage of the N10 is resumed.

As the unit warms up, all traces will disappear from the bottom of the display screen. This happens because, without any RF input to the detector, the system is looking at nothing but noise (-65 to -70 dBm) and the trace is following the noise level (down approximately six to seven divisions from the center line reference).

After initial warm-up (Auto Zero) and with no RF applied, the LED displays on the N10 should have the following indications: (If both channels have detectors attached, both channels will indicate. If only one channel has a detector, that channel will indicate and the other channel should be turned OFF, as previously stated.)

CHANNEL A and/or B LED	-65 to -70 dB
OFFSET	0.0
dB/DIV	10.0
REF LINE	CL

3.9.2 Calibration Check

When the 1038-N10 system is first set up, the detector exchanged, the temperature of the room substantially changed, or there is any reason to question the calibration, use the following procedure for each active channel and its associated detector:

Allow the instrument to warm up for at least 10 minutes – longer if it has been stored in a cold place. Connect the detector to the CALIBRATOR on the front of the N10. Turn ON the Calibrator and the INT SWEEP (above the Calibrator). Set the OFFSET to read 00.0, the dB/DIV to 0.1 dB, and be sure that the REF LINE reads CL. Press the desired channel and then "Input" and "Enter" on the keypad. The trace should be in the center of the screen and the channel LED readout should read 0.0. If the trace is not centered and the readout reads anything other than 0.0, adjust the CAL pot next to the detector input on the face of the N10 until the channel LED display reads 0.0.

3.9.3 Absolute Power Display

If power is to be displayed against another variable, typically frequency, connect the X-axis (horizontal) ramp from the sweeper to the Aux 1 connection at the rear of the 1038-D14A Mainframe. Set the sweeper to produce a repetitive sweep. To obtain the display, connect the detector to the device under test (or sweeper output) and be sure the OFFSET LED display reads 00.0. The REF LINE should be in the center of the CRT graticule, and the dB/DIV should be adjusted so that its LED readout indicates 10 dB/DIV. Press the desired channel and then "Input" and "Enter" on the keypad and the signal should appear on the CRT display. Having obtained a display, set the REF LINE, OFFSET, and dB/DIV to whatever position is desired. If smoothing is desired, press the channel of interest, then the "Smoothing" then the "Enter" buttons on the keypad. Check to see that the smoothing function does not change the shape of the displayed signal. If it does, slow the sweep until the signal appears normal. (Note the "Sweeping Too Fast" light.)

In order to see small signal variations across a band of frequencies, greater display sensitivity (smaller number of dB/DIV) can be used. To do this, the portion of the display of interest must be moved to the reference line by using the OFFSET adjustment. The display is then expanded using the desired dB/DIV sensitivity setting. The reading on the OFFSET LED readout is the power (in dBm) at the point where the trace crosses the reference line. The channel LED readout will indicate the power wherever the CURSOR is located. The CURSOR can be moved to any desired location on the display trace using the "Cursor Position" controls.

If a sweep generator with a voltage proportional to frequency ($V \propto F$) output is used, system errors can be memorized over a very broad range, and then readings taken from the device under test over a very narrow portion of that range. This function essentially does for frequency

what the dB/DIV sensitivity function does for amplitude, and gives the operator the ability to change the sweep end points at will and still preserve calibration. To use the V ∝ F function (indicated, when in use, by the illumination of the "V ∝ F" light on the face of the N10), the sweep generator's "Frequency Reference" output is connected to the Aux 2 input on the back of the 1038-D14A Mainframe. Then, if it has not already been pre-set per Section 3.2 of this manual, the A11S1 switch inside the N10 unit must be reset to place the V ∝ F function in an "ON" condition. This switch also controls the turning on or off of the Auto Zero function, and was previously described in Section 3.2.

3.9.4 Use of the Memory

a. **Single Reference.** To store any single reference signal in the memory of either channel, the ACCESS MEMORY function is used as described in Section 3.6.2.k of this manual. To check the contents of the memory of either channel, follow the instructions given in Section 3.6.2.i. When the INPUT-MEMORY function is used, as described in Section 3.6.2.f, a straight line should result. This is because the calibration curve just recorded is subtracted (in dB) from the input curve. When a device under test is inserted, the data displayed will be just the characteristics of the RF device. This is because the apparent calibration curve is a straight line corresponding to the reference line.

b. **Average of Two References.** When making return loss measurements, there is the possibility of storing an error during calibration. The error is due to the interaction of the directional device's source mismatch with the total reflection of the short or open circuit used during calibration. The magnitude of the error depends upon the match of the output port of whatever directional device is used. In practice, errors on the order of one-half to one dB are frequently seen for a broadband measurement. This error will be added or subtracted (in dB) to any measured value subsequent to calibration.

To substantially avoid this error, two reference curves can be averaged; the first made using an open circuit and the second using a short circuit. Since the phase of the two reflected signals are opposite in both cases, the resultant curve will have equal and opposite errors. By averaging the curves, the final calibration curve will be correct.

The Model 1038-N10 accomplishes this on channel A through use of the MEMORY and MEM AVG·1&2 functions, as described in Sec. 3.5.2.H. After "Enter" is pressed the second time, the characteristics of the open condition are added to the characteristics of the short condition at each of 2000 points along the curve. The result is divided by two and the dividend placed in memory replacing the data from the first curve. Unlike the straight line obtained with a single reference, the memorized average typically is not a straight line. The deviation from a straight line is the error that would have been in the measurement if only a short or open had been used for the 0 dB calibration.

4. IEEE BUS INTERFACE

4.1 D14A or D14 GPIB Data

As detailed in Section 7 of the 1038-D14A or D14 Operating and Maintenance Manuals, option 04 provides for connection to a remote calculator/controller. Assuming that this option is included in the mainframe when interfaced with the N10 unit, the following bus commands can be integrated with any specific program designed by the user. See Table 7-1 in Section 7 of the D14A or D14 Instruction Manual for a listing of all of the Refresh Display commands and bus functions pertaining to the D14A or D14.

Application Note AN21, "Programming the Model 1038-D14A/N10 Swept Measurement System", will give the user more detailed information on other commands and programming methods."

4.2 N10 Bus Commands

4.2.1 N10 Bus Commands used with a D14A Mainframe

The bus commands for the N10 are passed through the D14A by using a "minor" address which is one plus the D14A address. For example, if the D14A address is 4, then the N10 address is 5.

Note: This means that the 1038-D14A/N10 system has two (2) addresses.

The minor address is not preceded by a "P" as with the D14 (no suffix).

4.2.2 N10 Bus Commands used with a D14 (no suffix) Mainframe

The bus commands for the N10 Plug-In unit (Table 4-A) are passed through the D14 by prefixing a "P" (for plug-in) in front of the N10 commands. For example: to access channel A, a "PA" command would be sent through the bus to the D14. To turn off channel B, a "PBC" command would be sent through the bus.

Commands can be listed in series, but the user is cautioned that any "P" following the first "P" in a string will be interpreted as a "Cursor Position" command instead of the plug-in access. In other words, only the first letter of any command string for the plug-in must be a "P".

The commands for the N10 follow the key-strokes almost one for one, so learning to program the unit should be a simple process. Table 4-A identifies the keypad commands and indicates the bus functions that do the same things.

Tone Generation Function

The intention of the tone generation function is to allow audio tones to be programmed, as desired, into a testing sequence. This allows the operator to hear audible prompts at any desired time during the testing.

To set the tone generation mode, a lower case "m" is sent first, followed by the notes as shown in Table 4-B.

Table 4-A N10 Bus Commands

Channel A	A
Channel B	B
Enter	E
Clear	C
Auto Zero	Z
Internal Sweep	I
	X for external sweep
Calibrator	K for calibrator ON
	J for calibrator OFF
Secondary Functions:	
Offset	0
SF1	1
SF2	2
SF2-0	Toggle cursor ON/OFF
SF2-–	Reset to "Power-On" status
Access Memory	3
Channel Ratio	4
Memory	5
Peak Power	6
Input	7
Input-Memory	8
Reference Ratio	9
Smoothing	•
Reference Line	–
Indirect Functions:	
Sensitivity	S followed by a number from 0 to 8.
	0 = 0.5dB/DIV
	1 = 0.1dB/DIV
	2 = 0.2dB/DIV
	3 = 0.5dB/DIV
	4 = 1.0dB/DIV
	5 = 2.0dB/DIV
	6 = 5.0dB/DIV
	7 = 10.0dB/DIV
	8 = 20dB/DIV
Cursor Position	P followed by the desired position in CRT display divisions e.g., P5.00E for center screen. (The "E" is required to ENTER the data)
Local Lockout	G to lockout
	H to return keypad to use
Remote	R to remote (light lamp)
	L to return to local
Auto Zero Mode	M for RF on during retrace
	N for RF off during retrace
Self Test	T for SELF TEST ON
	W for normal working mode
V ∝ F	V for using proportional memory
	F for using full memory each sweep
Device Clear	D to reset unit

Example

To program channel A for a –20.5dB offset:

P (to access the plug-in)
A (for channel A)
0 (Offset – second function)
–
2
0
.
5
E (to enter the data)

Table 4-B Tone Generation Commands

Note	Command
A	A
B	B
C	C
D	D
E	E
F	F
G	G
A (second octave)	I
B	J
C	K
D	L
E	M
F	N
G	O

The tone mode is exited by sending a lower case "q" following the notes.

5. ELECTRICAL DESCRIPTIONS OF PC BOARDS

5.1 Introduction

This section of the manual contains a functional description of the electrical circuits contained on the PC boards and front panel assembly of the 1038-N10 plug-in unit. Table 5-A lists the circuit assemblies by reference designation, and includes the Schematic Diagram (SD) and assembly number for each board.

There is one electrical characteristic that is common to all of the PC boards in the N10 unit. This is the method used to provide the proper grounding configuration throughout the unit.

Each PC board contains both input and output isolator stages. This is to transfer the ground reference from the Reference or Ratio Common Ground used when signals are passing between the PC boards, to an on-board 15V Common Ground. When signals leave the boards, they pass through another isolator stage which transfers them back to the between-the-boards Reference Ground.

5.2 Block Diagram Description

(Use Figure 5-1, N10 Block Diagram, for a better understanding of the following discussion.)

Low level signals from the detectors are received by the respective Preamp and Log boards (both A and B channel Preamp & Log boards are identical), and then converted to logarithmic equivalents. The result is amplified to a voltage which varies between +1.6 and -6.0V (corresponding with the +16 to -60 dBm dynamic range of the N10). This voltage is then applied to the CRT Driver Board along with the reference channel voltage (if a reference is being used). The Reference Preamp and Log circuit board operation is basically similar to that of channels A and B with the exception that the reference output voltage will vary between +1.6 and -3.0V (+16 to -30 dBm).

The CRT Driver combines signals received from the other N10 components (see Block Diagram) according to whatever command the N10 has been given. The Driver can thus cause the ratioing of any input signal to any other input signal (including signals received through the GPIB). The Channel B (only) CRT Driver also has the capability of displaying a peak power input (interfaced through the Aux 3 connection on the rear of the 1038-D14A Mainframe). The Driver circuitry takes the 100 mV/dB that it receives from the Log & Preamp circuitry, offsets it by whatever amount of offset has been selected, then amplifies or attenuates the voltage according to the desired dB/DIV sensitivity setting. The positioning of the reference line is also controlled by the CRT Driver.

Absolute outputs from the Driver boards go to the Memory boards, the Cursor display circuitry, and the D14A Mainframe to be available on the GPIB. The Cursor display circuitry also operates in conjunction with the Horizontal board. When there is a coincidence between the selected cursor horizontal address and the 0 to 10V ramp input, a display will appear on the front panel LED readout. This display will indicate the power reading at whatever position the cursor is located on the CRT trace.

Upon command, the Memory boards will memorize the information received from the CRT Driver boards. Signal data memorized is independent of any scale settings, and both positive and negative memory is available. Using the Input-Memory and channel (A or B) memory controls, it is possible to see what has just been memorized.

The Horizontal board accepts the ramp input of the sweep generator (within the limits of -5 and +20V) and converts it to a 0 to 10V ramp voltage. The board also generates the cursor pulse and the addresses for the A and B channel memories. There are eleven data lines physically available for the production of addresses. These lines allow access to 2048 horizontal points. The full sweep (V ∝ Sweep) mode uses the 0 to 10V ramp to produce horizontal addresses for the whole memory. If the voltage proportional to frequency (V ∝ F) mode is desired, memory storage will be proportional to the frequency of the input signal. This means that any desired part of the total frequency band of interest can be selected and examined. This is useful, for example, in the evaluation of a bandpass filter. The broad band can be examined for possible spurious outputs, and then the passband can be closely examined to locate ripples. This can be done without any changes required in the testing setup or loss of any memorized data. This also means re-calibration in the V ∝ F mode is not necessary if frequency limits are altered.

The CPU (Central Processing Unit) board provides outputs to control the keypad operation and all front panel displays. It controls the processing of the V ∝ F, Auto Zero, and Memory functions and furnishes an input for the signals received through the PMIB (Pacific Measurements Interface Bus). The PMIB is the interface between the N10 and the external GPIB. The CPU also controls the Calibrator, which provides the 0 dBm at 50 MHz signal used to calibrate the detectors.

Table 5-A N10 Circuit Assemblies

Ref. Desig.	Nomenclature	Ass'y. No.	SD No.
A1	Digital Display Driver Board	14950	14951
A2	Display and Calibration Board	14953	14954
A3/A4	Input Preamplifier & Log A (or B) Circuit	15834	15835
A5	Reference Channel Preamp & Log Circuit	15227	15228
A6	A Channel Memory	14879	14880
A7	B Channel Memory	14887	14888
A8	Horizontal & Cursor Board	15187	15188
A9/A10	CRT Display (A or B Channel)	15330	15331
A11	CPU Board	14963	14964
A12	N10 Interconnect Board	15005	15006
A13	Front Panel Assembly	14968	15003
A14	Horizontal Finger Board	15023	15034
A15	A Channel Finger Board	15064	15034

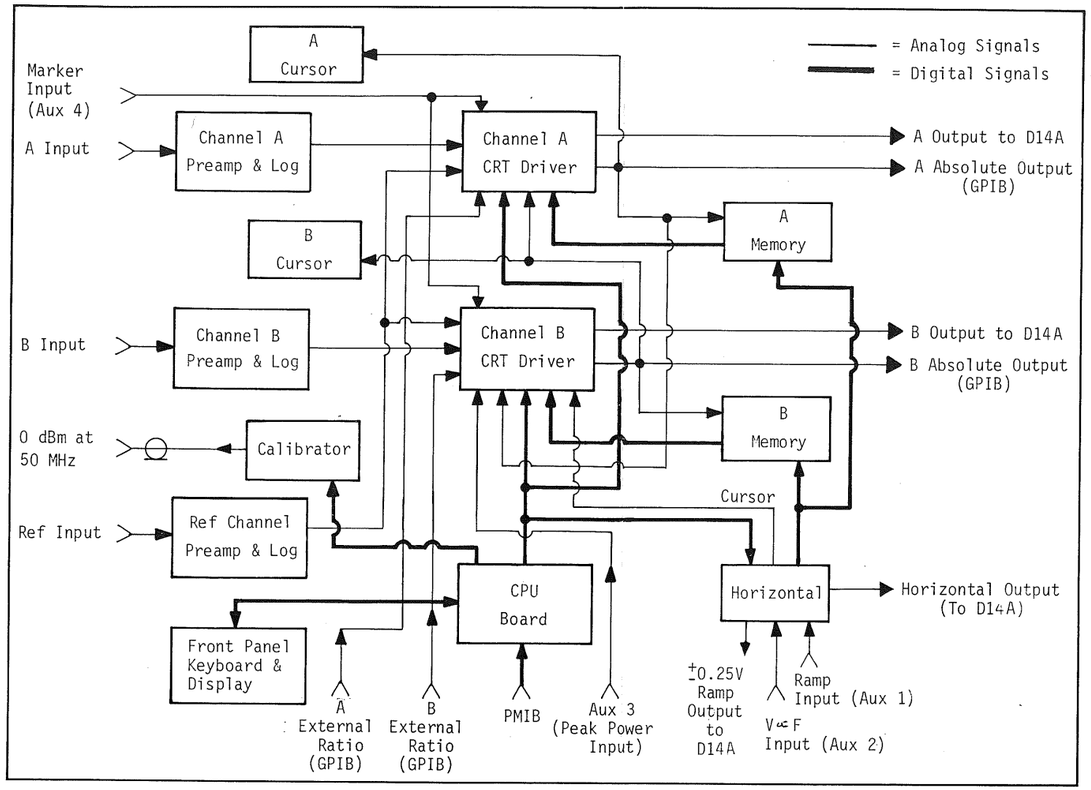


Figure 5-1 N10 Block Diagram

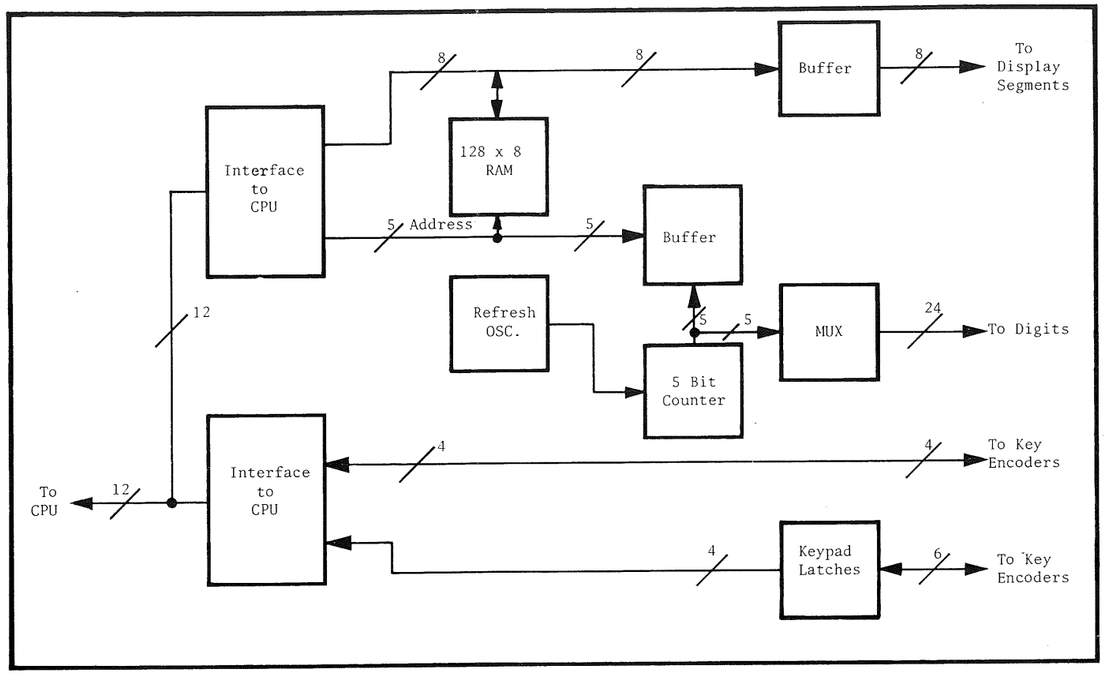


Figure 5-2 Digital Display Driver Board (Bd # A1-SD 14951)

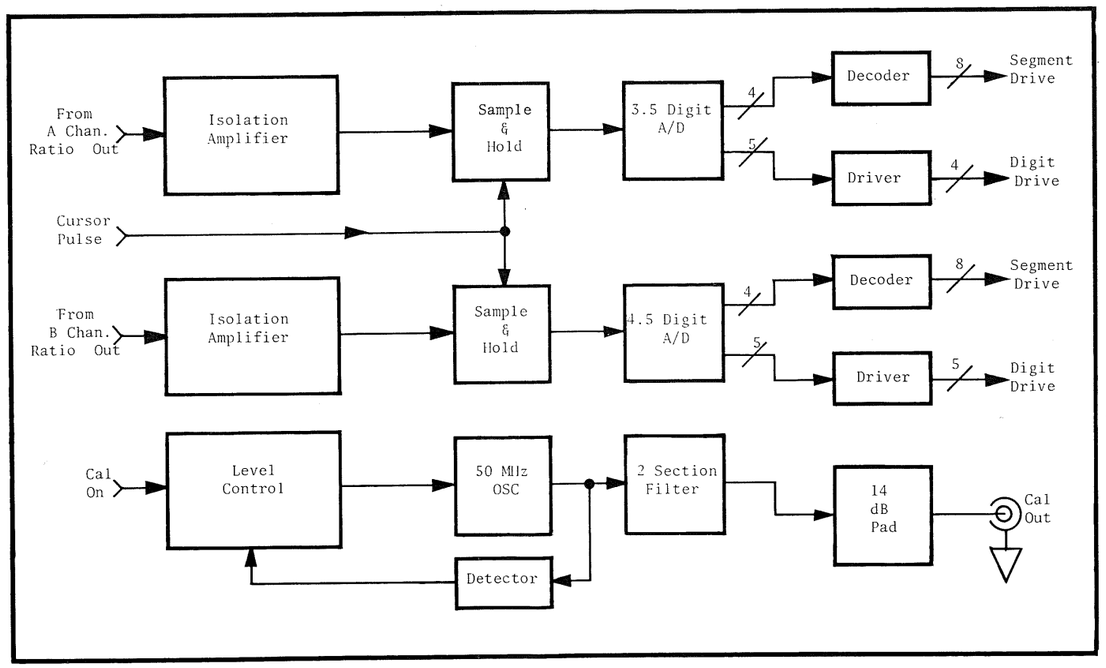


Figure 5-3 Display and Calibration Board (Bd # A2-SD 14954)

5.3 Printed Circuit Board Descriptions

5.3.1 *Digital Display Driver Board* (SD 14951 Bd # A1)

The Digital Display Driver PC Board (Assembly #14950) is used to provide the required signals to illuminate all of the N10 unit's front panel LED displays except the cursor display (channel readouts). This includes the single LED's used to indicate what mode is in use. The board also provides an input interface for commands sent from the front panel keypad. (Use Fig. 5-2 – Block Diagram on page 5-3, and SD14951 as aids to better understand the following discussion.)

5.3.1.1 LED Display Circuitry

The LED's are driven using a standard seven segment display format. That is, each lamp is driven from one of the segment outputs so that, as far as the CPU is concerned, it causes them to be lit similar to the seven segment format. All of the seven segment LED's on the front panel have their segments tied in parallel; all a's together, b's together, etc. Segment drive lines a through g (shown in the upper right corner of SD 14951) are used to input the segment information. Line dp is the decimal point, and is also common to all of the LED's. To determine which light is to be lit at any one time, separate cathodes are brought into the PC board and tied to cathode or digit drivers. They are split into the A and B channel displays, and the A and B channels are divided into individual LED signal readout lines from the PC board. For instance, connector J1's (channel A) outputs are labeled Offset 1, 2, 3, 4, and 5. These go to the Offset display on the N10's front panel, and read from the left (looking at the panel from the front). This means that line number one is connected to the farthest digit to the left on the display, and line number five is the farthest to the right. The Sensitivity (dB/DIV) display has a similar interconnect configuration.

The overall display format is operated by first individually decoding which digit is to be lit, and then which segments of that digit are to be lit. That information is kept in the 128 byte RAM, U19. In U19, two sections of 24 bytes each are used. These sections are called banks. One bank contains the segment information to be displayed, and the other bank contains either the same information or all zeros. If all zeros are contained in the bank being displayed, no segments are lit (LED will be blank). This function is used to cause the flashing action of the LED's. By having segment data in one bank, all zeros in the other, and then automatically switching back and forth, the light will flash on and off. To cause the LED's to light in the proper sequence, a multiplexing procedure is used. At each address of U19, there is a byte of data that represents the segments to be lit to cause the display of a particular digit. All of U19's addresses are cycled through by using an oscillator, a set of dividers, and a decoder. The oscillator is U20, operating at approximately 3.5 kHz. The dividers are U21 and U22 which divide by 24. U18 is the buffer amplifier between the divider and U19. The outputs of the dividers feed the input side of U18, and the U18 output feeds the address lines of U19. Since the address lines are being driven from a counter, they increment from 0 to 24. The bank switching on U19 is taken care of by the next two address lines, A5 and A6, which are controlled by the CPU through the Parallel Peripheral Interface (PPI) device, U24. Thus, the CPU can directly control U19 to tell it from which bank it should be operating.

To load data into U19, the data lines become inputs rather than outputs and are driven by U25. The eight lines of the A port of U25 will transmit the correct data for a particular location (specific front panel LED) to U19. The B port of U25 has the address information for the data, and it activates the write-select line of U19 to write the address into the RAM. The read/write line (pin 16) of U19 is controlled from U24. If the line is high, it is in the read mode, and if it is low it is in the write mode. The CPU can arbitrarily write to any digit position on the front panel by loading information into the U19 RAM, releasing it, and then allowing the refresh oscillator to keep displaying everything in the RAM. The data does not have to be a number; it could be any alphanumeric character (such as ERROR). The RAM keeps cycling through all available locations and displaying the information over and over again. The disconnect for the refresh oscillator is through the U18 buffer. Pins 1 and 15 of U18 are the enable lines and, if these lines go low, U18's tri-state outputs will take control of the bus. If the enable lines are high, U18 is disconnected and U25 writes directly to U19. The enable lines are controlled from U24 (labeled Not-Counter Active).

5.3.1.2 Keypad Interface Circuitry

Keypad data is supplied from a separate decoder board through two sets of lines. One set of four lines is the actual data corresponding to the key that was pressed. The other set of lines correspond to the particular bank of keys containing the depressed key. The keys are divided into data groups 1, 2, and 3, with the data from each group brought into the Digital Display Driver PC Board separately. This means that when a front panel key is pressed, data comes in from the A, B, C, and D lines through connector J1. These lines form a nibble of data telling what key was pressed. A separate set of lines labeled DA (Data Available) 1, DA2, and DA3 come from the same decoders and tell in which bank of keys the particular key that was depressed is located. The three data available bus lines are connected to three separate latches, U26A, U26B, and U28. If data from the keypad is available, one of the latches will trigger. The triggered latch will then cause the Q-bar output to go low (having been set high by a clearing pulse). The low output is fed to an enable line (active low), and will go back to the keypad decoding circuit and enable the data from the particular bank of keys to go to the four data lines. The ABCD data lines are fed to the A port of U24 (low nibble of the A byte). The high nibble of the A byte, lines 4, 5, 6, and 7, are derived from the output of the latches with the exception of bit 7, the MSB (most significant bit). Bit 7 is derived directly from the data available line, DA2, on the middle bank. The middle bank comes from the jog buttons (cursor and offset controls) on the front panel. If a cursor or an offset control button is pressed, the cursor will continue to move or the offset continue to change until the button is released. By taking the DA2 line directly to the MSB of the A port of U24, the circuit can constantly monitor the MSB to determine if the button is being held closed. When the operator releases the button, the line will go low (will be sensed as bit 7, the MSB on the byte going low), and the CPU will respond by stopping the jogging action.

In a normal operating mode, if the DA1 line is set true, it will toggle the U26B latch. U26B's Q output will then go high and be delivered by bit 6 to the A port of U24. The CPU senses that bit 6 is high, and then knows that it is the first bank (DA1) of data that is being requested. It will then decode the ABCD data lines (least significant nibble

of the byte) according to the bank one data. Having done that, the output from the B port of U24 (B0) is supplied directly to the clear line of U26B and will clear the latch to its normal condition. In other words, if the button is pushed, the data will be looked at and, as soon as it is no longer needed, the latch will be cleared. At the same time, when the clear pulse is applied to U26B, the active low line is pulled low. One input to and gate U27C also goes low, forcing the output to be low, which clears the next latch, U26A. The low pulse is also applied to the "and" input of U27D, which clears the third latch, U28. This means that, when any latch receives the "clear" command, it clears all three latches.

Another function that occurs when any of the Data Available lines are activated, is that one of the outputs will go to a true (high) condition (conversely, another output will go low), and the complement outputs will be "or'd" together. When this happens, the keypad interrupt output (TP4) will come true. The not-interrupt goes low (comes true because it is an active low), and interrupts the CPU. The CPU will cease processing whatever function it is currently involved with, and determine what is being asked for on the keypad. It will then process the keypad data.

5.3.1.3 Sweep Error Indication, Alarm and Zero Lamp Lines

Another output of the Digital Display Driver Board is the Sweep Error indication. If the CPU detects that the sweep is too fast to memorize, it will (through U24, port B, bit 3) cause the Sweep Error lamp to illuminate. The output of U24 is through nand-gate U23A. The Sweep Error lamp is also operated from the Input Preamplifier PC Board (SD 15073), so that if the sweep generator is sweeping too fast for the power level (low level) to handle, the light will also turn on.

The Alarm input (from J2, pins 23 and 24) goes to pins 19 and 20 (the B port) of U24, and are toggled in opposition. This produces a differential signal which will activate the alarm transducer. The timing is software controllable so that the audio pitch is selectable by the programmer. Tones can be generated to provide any desired combination, including music.

The Zero Lamp off line is merely a feed-through connection, used as a convenience relating to the overall design format of the system.

5.3.1.4 CPU Address Interface

Parallel Peripheral Interfaces (PPI's) U24 and U25 are driven by the CPU, and need to have the various addresses decoded so that the CPU knows where to reach them. U29 is the address decoder, and receives address information from the CPU through address lines A2, A3, A4, A5, and the not-bus enable line. The not-bus enable line comes from the CPU and will be true at address 7000 and above. As long as the CPU is asking for peripheral data, U29 will be active and looking at the four address lines. The address lines are decoded into two outputs of U29 (not-4 and not-5) which are active low. The not-4 line is brought to the not-chip select input of U25, and the not-5 line goes to the not-chip select input of U24. U25 is decoded at 7010H (H = Hex) and U24 is decoded at 7014H. U24 and U25 both operate with four addresses. U25 is controlled from addresses 7010, 7011, 7012, and 7013, and U24 is controlled from addresses 7014, 7015, 7016, and 7017.

5.3.1.5 Test Point Indications

TP1 – Refresh Clock output (operates at about 3.5 kHz – the speed of the refresh oscillator U20)

TP2 – CPU Interrupt line

TP3 – PC Board Ground

TP4 – +5V

TP5 – All Displays Off. If the panel is completely blank, TP5 can be checked to see if the panel has been commanded to be off. If TP5 is low, the panel is supposed to be off.

5.3.2 *Display & Calibration Board* (SD 14954 Bd #A2)

The Display and Calibration Board (Assembly #14953) has two major functions. The first function is to provide a 50 MHz, 0 dBm reference for external detector calibration. The other function furnishes the signal required to activate the cursor display LEDs on the N10 front panel. (Use Figure 5-3 on page 5-3 and SD 14954 as aids to better understanding the following discussion.)

5.3.2.1 Calibrator Circuitry

The Calibrator signal generation circuitry (shown along the bottom of SD 14954) primarily consists of a 50 MHz oscillator with a leveller-loop attached to control the output power. The output of the oscillator is filtered (to eliminate harmonics) and padded before it reaches the output connector. This assures a 0dBm (1mW) into 50 ohm at 50 MHz output with almost no harmonics and excellent source match.

Q1 is a 50 MHz Colpitts oscillator whose output is supplied to the filters through a 50 ohm resistance. The 50 ohm is used to ensure that the source impedance will match the filter impedance. The circuit is designed to allow an external swept RF source to be used to test the filter in order to optimize the filter's response before it is connected to the calibrator. This is done through J4, pins 3 and 4, which allow connection of the swept source into the front of the filter. In order to test the filters with the swept source, it is necessary to lift one end of R80 so that the impedance that the source is looking into will be close to 50 ohms. The output of the filter is then padded through a single-section pi pad rated at 14 dB. The pi pad is used to provide a 0 dBm output that can be controlled to maintain a return loss in excess of 30 dB. In this way, the source impedance is almost completely independent of the filter characteristics.

As the output of the Q1 oscillator is applied to R80, it is monitored by CR7. The resulting voltage is used in a feedback loop to control the power output from the oscillator. The feedback loop is composed of CR7, U16A, and peripheral components. The loop will supply current to the emitter of the oscillator through Q2. The only purpose of Q2 is to turn the oscillator on and off from a specific logic level by way of level shifter Q3. The input of Q3 is TTL and the output side is CMOS type logic (runs positive enough to turn the control switch on). Q1's output power is controlled through a voltage supplied by a separate voltage controlled reference diode, CR6. CR6 supplies a 6V reference without being effected by variations in the 15V power supply. The 6.2V from CR6 is supplied to the oscillator reference resistor, R69, through the temperature compensating diode, CR5, CR5 compensates for any tem-

perature variations that may affect the diode detector, CR7. In this way, the reference voltage will stay constant when there is any change in temperature because the voltage drop across CR7 will maintain the correct value. The oscillator adjust pot., R71, provides the means for a small adjustment to assure an exact 0 dBm output. The pot. will only adjust within about a 1 dB range, but this is sufficient to take care of any circuit variations that might be present.

5.3.2.2 Cursor Display Circuitry

The cursor display consists of the large power readout digits at the top of each channel section on the front panel of the N10 unit. There is a separate circuit path to drive each of the channel readouts. Both A and B channel circuit paths are identical except that A channel displays 3.5 digits while B channel displays 4.5 digits. Channel A has a resolution of 10 mV and channel B resolves to 1 mV. This means that the decimal point on the displays is positioned to show 0.1 dB resolution on channel A and 0.01 dB resolution on channel B.

The conversion from analog to digital data is accomplished in chip set U3 and U4 for channel A and U11 and U12 for channel B. The chip sets process an analog voltage input to deliver a BCD digital output. This output will be processed to eventually drive the LEDs of the front panel displays. Since the BCD numbers cannot directly drive the display LEDs, the numbers must be converted to the 7-segment mode through a decoder. U5 and U13 do this for channels A and B respectively. The outputs of the decoders are fed through current limiting resistor networks R28, R29 and R55, R56 to the cathodes of the respective channel LEDs. To cause the LEDs to turn on, the anodes of each LED must be activated as required. This is done using a multiplex (light one digit at a time) system. The "D" outputs of U4 and U12 control the actual anode activation, and are fed through isolators U6 and U14 which supply the anodes of the LEDs, and allow them to be strobed.

Decoder drivers U5 and U13 are also used to suppress any leading zeros. This means that if any unwanted zeros are in front of the numbers to be read out, they will be eliminated before the display digits are activated. Only the active or significant digits will be displayed. The polarity indication and positioning of the decimal point on the display are controlled and driven through separate driver transistors. Two sets of transistor arrays, U7 and U8, are used for individual channel logic control (as shown on SD 14954).

The dBm or dB inputs for both channels are supplied through a sample and hold technique. Sample and hold circuits are used to ensure that the signal input to the PC board is only processed at a specific point in time. That point is the exact instant that the cursor appears on the CRT display trace. In this way, the display will show what the power level is exactly at the cursor location. Coupling switches U2A (for channel A) and U2B (for channel B) are used to ensure that this timing takes place at the correct instant. U2 is switched when the cursor pip (the voltage pulse that is generated when the cursor appears on the CRT display) comes into the PC board. The cursor pip will close the switches and charge the hold capacitors (C5 for A channel and C21 for B channel) for the very short segment of the trace displayed by the cursor. The cursor is about 1% of the sweep width, so it will be about 0.1 msec wide at the maximum sweep speed of 10 msec. With a sweep speed of 1 second, the cursor would occupy about 10 msec of sweep width. The hold capacitors are connected to isolation amplifiers U1C (for A channel) and U10D (for B channel). The amplifiers supply the DACs through voltage divider networks (R12, R13 and R45, R57) since the full scale input to the DACs are only 10% of what is required for the input signal.

The input to both channels is through isolation amplifiers U1A and U10A for the A and B circuit paths respectively. Isolation amplifiers must be used whenever a signal enters or leaves a PC board in the N10 unit to allow for the changing of grounds. Ratio or reference grounds are used between the PC boards and a 15V common ground is used on the boards. Therefore, a change from ratio to 15V ground must be made at the PC board input and then transferred back to ratio common ground when the signal leaves the board.

Another signal used in the Display and Calibration PC board circuitry is the +10V Reference. The +10V reference must also be transferred from the ratio ground to the 15V common ground on the board, and this is done through U10C. U10C also divides the 10V down to 1.1V to give an internal reference of 1.1V. The 1.1V is used to supply each of the A to D convertors. U4 and U12 receive the 1.1V through gain adjust pots R21 and R64 so that the full scale level of each channel can be individually set. The 0 level can also be set for each channel by offset trim pots R9 and R40. The trim pots are required to supply a dc offset adjustment. This adjustment is used to ensure that the readout will indicate 0V when a 0V input is present at a particular channel.

5.3.2.3 Test Point Indications

TP1 – Ratio Common Ground

TP2 – Lamp Test. Channel A

TP3 – Lamp Test. Channel B

TP4 – -15V

TP5 – 5V Common

TP6 – 15V Common

TP7 – +5V

TP8 – +15V

TP9 – Calibrator Oscillator Drive (Approximately ±8V)

5.3.3 *Input Preamplifier and Log A (and B) Circuit* (SD 15835 Bd #A3/A4)

The Input Preamplifier and Log Circuit board (Assembly #15834) is identical for both channel A or channel B. The board is designed to accept the signal input from both balanced (dual diode) and single diode detectors. The board contains a linear preamplifier that can initially process both the input from a balanced detector and a single diode detector. The amplified output of the Preamp (the name of the board will be shortened to "Preamp" for the rest of this discussion), after further processing, will then be used by the 1038-D14A Mainframe to cause precise power indications on the CRT and the N10 LED displays.

The positive and negative signals received from the balanced and single diode detectors are processed through two separate circuit paths, theoretically similar to the absolute value circuit operation of a digital voltmeter. The detected signal enters electronic switch U30 and, during the normal CRT trace period, the signal is applied to the differential amplifiers U20 and U21 for low levels or U13 and U12 for high level signals. During the retrace period, U30 is switched and grounds the amplifier input. The Preamp recognizes this ground condition and adjusts itself to 0V at the output

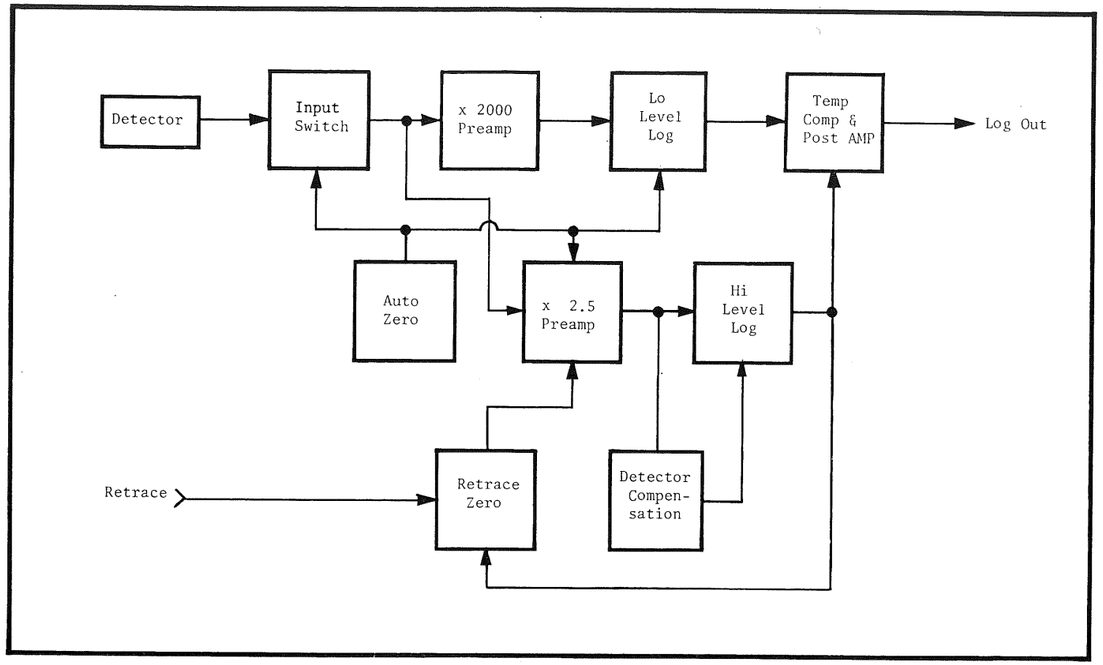


Figure 5-4 Input Preamplifier and Log A (or B) Circuit (Bd # A3/A4-SD 15835)

(Autobalances). (Use Fig. 5-4 on page 5-7 and SD 15835 as aids to better understand the following description.)

5.3.3.1 Low Level Signals

Since U20 and U21 are differential amplifiers, the signal input from the detectors is brought in differentially as a pair. This means that either positive or negative single diode detectors can be used. In the balanced detector, both inputs are used.

U20 and U21 amplify the signal by a factor of 200, and then send it on to U19C. In U19C, the balanced signal is converted to an unbalanced signal and amplified by a factor of 10. This total gain of 2000 (relative to the front end detector input) can be checked at TP9. The signal then proceeds to the input of log amplifier U19D. U19D is a summing amplifier whose positive side is grounded. During the retrace period, this places a virtual ground at pin 6 due to feedback action (normal inverting operational amplifier) so that the input resistance going into U19D from U19C consists of R26 and R33. (C11 is inactive except during the Auto Zero mode. This will be discussed later in this section.) The Preamp is adjusted to 0, and TP9 will read a voltage proportional to the RF input, up to -27 dBm with a single diode detector, or to -30 dBm with a balanced detector. At -30 dBm with the balanced detector, the voltage at TP9 would be 2.8V. At -30 dBm, there should be about 2.8V or 1.4V depending upon whether a balanced or single diode detector is in use. If the power input dropped to -40 dBm, the signal level would be 1/10th or 0.28/0.14V; at -50 dBm, it would go down another 1/10th, etc.

In the normal (forward trace) mode, U19D receives its feedback from U4A's collector which is connected to a summing junction. The current coming into the summing junction through R33 will be logged by the system so that the voltage at pin 4 of U4A will look like the log of the input with a coefficient of 60 mV per decade. For every 10 dB change of the detector input, there will be about 60 mV change at the emitter of U4A. Q1 is in the circuit to provide feedback in case the zero offset is slightly negative.

The signal coming from pin 4 of U4A (Log Direct) goes through R41 to U11B. R53 is an adjustment on the feedback divider which consists of R34 (in the feedback circuit of U11B) and R41. The signal output from U11B is called "Log Low". It is multiplied by 16.6 and equals 100 mV/dB (will equal 0V at -27 dBm for a single diode detector and at -30 dBm for a balanced detector). The log amplifier is temperature sensitive in that the leakage current in the transistor is a function of temperature and doubles every 10°C. This causes the voltage between the emitter and base to change. To compensate for this, there is a temperature compensation circuit consisting of U11A (with feedback through U4B) which is an inverting amplifier with fixed current coming from a fixed 10V reference (R44). The reference causes a voltage to appear between the base and emitter of U4B due to the feedback action of U11A (another log amplifier). In U11A, the collector current feeds back from pin 14 of U4B to pin 9 of U11A. The result is that the emitter-to-base potential of U4B has the same temperature variation as the emitter-to-base potential of U4A at the same current. Since the current is equal to the -27 dBm current, U11B (Log Low) will now have a 0V output. The only purpose of U4B and U11A is temperature compensation. With the above process in effect for low level signals, the signals are now proportional to the log of the input all the way from -70 dBm up to -27 dBm (single diode), at which point U11B, pin 14, goes positive, CR5 disconnects, and the high level signal path takes over.

5.3.3.2 High Level Signal Path

Differential amplifiers U12 and U13 are connected to the same point (output of U30) as U20 and U21. They operate (along with U5) to provide the same function as U20, U21, and U19C only for signals above -27 dBm (single diode detector). U13 has very low gain (5, as against 200 for the low level path), and U5B has a gain of one-half. This equals an overall gain of 2.5. At the highest power level (+16 dBm), a single diode detector will have a maximum output of about 1.7V and a balanced detector will deliver about 3.4V. With a gain of 2.5 this equals 8.5V which is close to the power supply voltage on U17. The ouput of U11D goes through R141 to log amplifier U5, which gets its feedback from the collector of U4D. Q4 is used similar to Q1 (in the low level path) for a reverse clamp. The signal goes through U11C and is amplified by a factor of 16.6 so that the "Log High" signal equals about 100 mV/dB.

Both the log high and log low signals are output through diodes. The low signal from U11B will always be negative due to the fact that CR5 disconnects at 0V preventing the low signal from going above 0V. The log high signal from U11C is always positive because CR13 prevents it from going below 0V. As the low RF signal starts to increase, the log low voltage goes toward zero until it reaches -27 dBm (0V). Just above -27 dBm, the log high voltage, which has been at 0V, takes over. The log low voltage remains at 0V and the log high voltage continues to increase as the RF input signal increases. Both log low and log high signals are summed at U9. One of the inputs to U9 is always adding zero to the signal, so only the active signal is passed to U10D. Temperature compensation is accomplished through RT1, R59, and R58. These components provide a linear temperature coefficient to compensate for the log circuit so that the output of U10D will always be exactly 100 mV/dB, regardless of temperature. U10D furnishes both isolation and a place to sum in a correction signal which compensates for the temperature coefficient of the detector diode. The performance of the entire signal path can be checked at TP2.

Compensation circuitry is included in the Preamp for use with high level signals. The purpose of the compensation amplifier (active only above -30 dBm) is to maintain a constant upward slope to the detector output level. At about -30 dBm, a detector will start to divert from square law (steady upward slope) to the peak-detector voltage law (smaller slope) as the RF power of the signal increases. To circumvent this and maintain the steady upward slope, the output of U11D (pin 1) is tied into a compensation circuit through potentiometer R142 and resistor 143 to U8. U8 is another log amplifier and receives its feedback through U14B The voltage output from U14B is through pin 2. Q5 prevents the signal from locking up in a reverse direction. The signal leaves U14B through R151 to U7. U7 has a gain of 2, so the de-logged signal is squared. The signal is de-logged at U14C so that U14C's current (not voltage) output will be proportional to the current at U8 pin 2. TP11 will allow measurement of the voltage output of this section of the Preamp. U14A compensates the log transistor junction so that U19D and U14A provide a fixed current. Along with the fixed current is a voltage that will be a function of temperature, as will the voltage from U8. U14A, U14B, and U14C have the same temperature dependence. U14A will furnish compensation for these components.

Current from U14C (monitored by U32 pin 2) goes into U14D and U14E. The purpose of U14D, U14E, and U32 is to produce a current mirror. In other words, the same current is present at pin 12 of U14E, except that it must be of reverse polarity. The current is applied to the input of the Log High circuit and summed in U5 to form the log of the total composite signal. The composite signal consists of the signal through R141 and U14D pin 12. The sum of the currents is linear with power from -30 dBm to +16 dBm, thus maintaining the steady upward (square law) curve rather than starting to level off (peak detector law). The compensation must be different depending on whether the detector uses a balanced or single diode. This means that the same compensation that occurred at one voltage for the single diode detector will have to occur at twice the voltage if the balanced detector is used. U22D causes the reference current to double in U14A whenever a balanced detector is used. The single diode detector will read the same voltage at the output as the balanced detector due to the fact that additional current is summed into U31A. This changes the voltage enough to offset the output at TP2 by 3 dB. Since the balanced detector generates twice the output of the single diode, this 3 dB change will produce an equal voltage for either detector. Pin 25 (Detector ID) at the input of the Preamp is used to recognize whether a balanced or single diode detector is in use. The balanced detector contains a jumper which causes 0V to be present at pin 25. The single diode detector has no jumper and allows 5V to be present at pin 25. The voltage goes through U27D, is inverted by U26F, and sent to U22D. Thus, the N10 "knows" what type of detector is in use without any adjustment required by the operator.

5.3.3.3 Thermal Compensation

At low signal levels, the detector voltage will vary considerably with changes in temperature. A detector's output at low levels is an inverse function of temperature. Therefore, it is necessary to monitor the temperature of the detector to be able to provide the proper compensation. This is done by means of a thermistor located inside the detector. The thermistor becomes part of a bridge that includes the input circuitry to U31B. U31B puts out a temperature compensation signal that is just proportional to the temperature change sensed by the thermistor. This signal is fed as a reference to U14A to cause the compensation circuit to correct for any detector temperature variations. The reference signal also goes to U31A to cause a slight offset on the output.

The signal that goes to the temperature compensation circuit will compensate for errors in the curvature of the correction circuit, but will still leave the possibility of an absolute level shift (as the temperature goes up, the output will appear as if there were less RF). To offset that, additional compensation is added through U31A. The result is that, as measured at TP2, the output is independent of the temperature of the detector.

Inside the detector assembly, there is a selected resistor which allows a slight adjustment on the reference voltage at U31B pin 7. This detector compensation resistor interfaces with the Preamp at pin BB of the input connector, and its value will depend on the individual characteristics of the diode in the detector. If the diode in the detector element is replaced, the resistor must also be replaced. The correct value resistor for the replacement diode is included in the replacement kit.

5.3.3.4 Auto Zero Circuitry

There are two methods used to assure that the N10 unit automatically zeros itself. If the RF is *completely* turned off (zero power) during the retrace period of the sweep generator (oscillators are off), electronic switch U30 in the Preamp can be selected so that it will never be activated and the signal will always go directly to the differential amplifiers. U30 would always be in the position as shown on SD 15073.

The second method is employed if a sweep generator is used wherein the RF cannot be turned off during the retrace period. In that case, U30 is activated and the signal is sent to ground. This allows the Preamp and N10 internal circuitry to zero, but still does not compensate for the detector. Regardless of which way U30 is switched, during the sweep retrace period the Preamp is set so that the log feedback is disabled. The feedback from U19D goes to the switch portion of U29 and the log feedback is eliminated by opening pins 9 and 8 of U29. Then, the linear feedback is supplied through pin 3 of U29. This feeds through R37 to C13 and through R72 to C72. C13 is necessary to stabilize the feedback loop during the Auto Zero interval. C72 is a sample-and-hold capacitor that stores the required voltage to cause the Preamp to be adjusted to 0V at the input. The constant C72 voltage is applied through voltage follower U28B and R19 back to the input of U19D. When the retrace cycle is completed, U29 pin 3 opens, U29 pin 11 closes, and the circuit goes back to the log feedback mode. Just enough current continues to flow through R19 to guarantee that the Preamp will produce a 0V output with a 0V input. The action described above takes place every retrace interval. This means that approximately 10% of the time the instrument is zeroing itself.

If the RF is not turned off during retrace, it becomes necessary to take into account the parasitic thermal potentials of the detector diode. As said before, if the RF is off the system will automatically zero itself without adjustment on the part of the operator. In the event that the RF remains on or partially on during retrace, it becomes necessary for the operator to periodically turn off the RF manually. This can be done through the bus or by physically turning off the power from the sweeper. Then, the Auto Zero button on the front of the N10 unit is pressed. This causes the N10 to go through a cycle of events to read the dc voltage on the detector. When the Auto Zero button is pressed, the circuitry performs a normal retrace zero (just discussed) wherein the voltage on capacitor C72 is updated and the N10 is properly zeroed with U30 switched to ground. The cycle is then repeated with the detector in the circuit so that the second zero will take into account any parasitic thermal voltage from the detector. In order to do this, the first part of the cycle is a course zero which makes use of successive approximation register U2 and DAC (Digital to Analog Convertor) U3. U3 is fed through U10A (part of the DAC) and then back through switch U18 and R34 to correctly zero the Preamp in the coarse mode. U2 is triggered and goes through a successive approximation (normal A to D conversion) with U1B monitoring the voltage at the output of U19D through R74. (C74 eliminates noise spikes.) The successive approximation goes rather slowly, with each step taking 1/16th of a second. (See Figure 5-5 for the Timing Diagram.) All of the above occurs after the Auto Zero button has been pressed. A signal comes into the Preamp through pin 6 from the N10 microprocessor that says an Auto Zero is required. When the

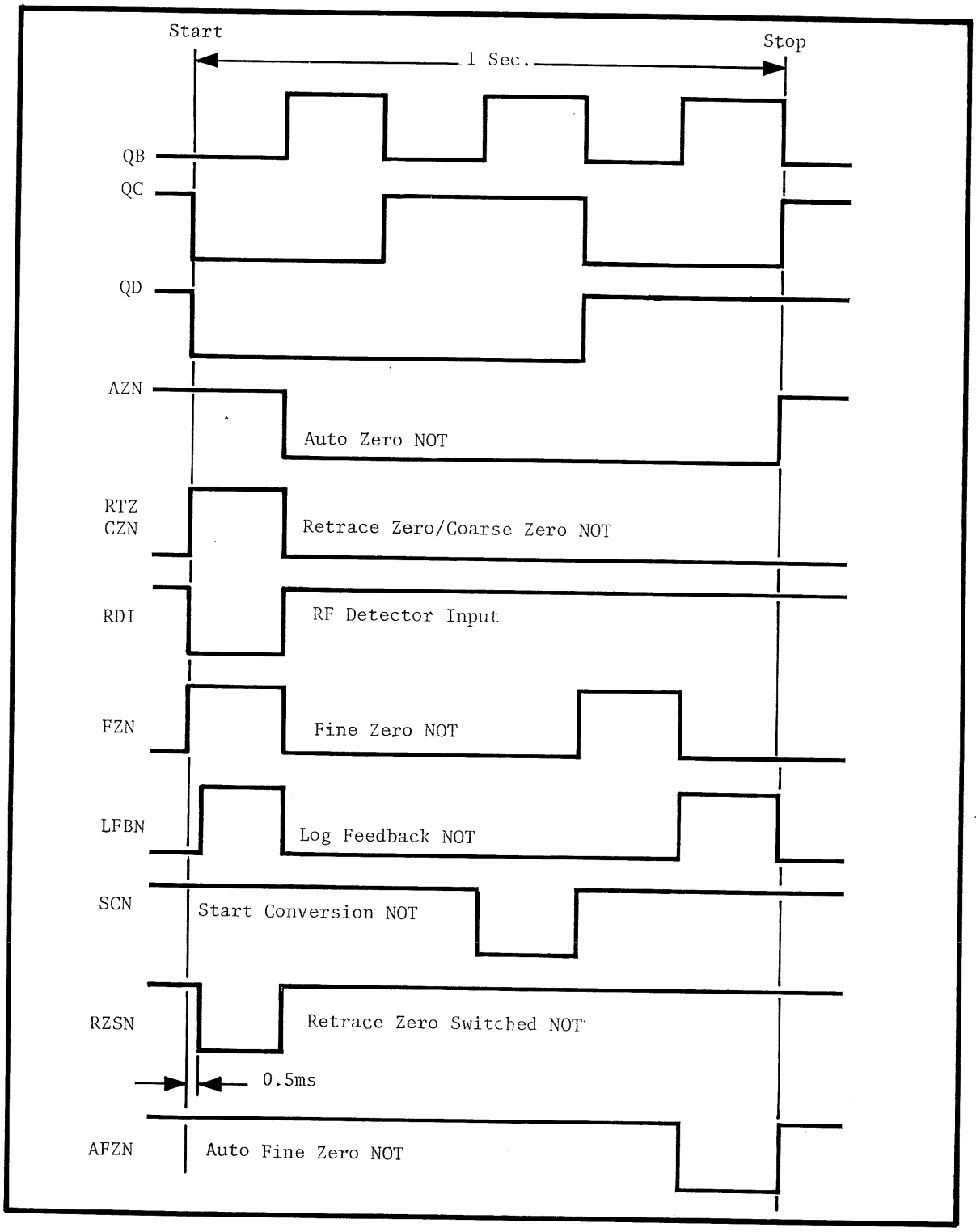


Figure 5-5 Auto Zero Timing Diagram

Auto Zero button is pressed, all of the logic circuits (U15, U23, U24, U17, U16, and U25) take over and cause the Auto Zero cycle to start. U2 generates a series of clocks, causing the output of U10 to be forced to drive the voltage on pin 7 of U19D to as near zero as possible. This is a normal successive approximation technique using U1B as a comparator, U2 for the successive approximation, and U3 as the DAC.

The course zero is fed back through pin 2 of U18 but, since this is only a course adjustment, residual voltage must be considered and eliminated. The DAC has 8 bits equalling a resolution of one part in 256. This is not sufficient to zero as accurately as is required, so there will always be residual voltage at pin 7 of U19D that must be eliminated after the coarse zero cycle is completed. This is done by another sample and hold circuit consisting of U28B and C12. This circuit is fed from the output of U19D through pin 6 of U18. The voltage at pin 1 of U28B is forced to the correct value with feedback supplied through R35 and U18 pin 11. This completes the coarse and residual (fine) zeroing process.

To briefly recap the preceding discussion, whatever voltage is present during the coarse and fine zeroing cycles is connected to the amplifier during the normal (trace) interval of display. During the retrace interval, the voltage is disconnected after the zeroing process is completed. The signal from the coarse and fine zero is only connected during the display mode. During the retrace mode, it is not connected because then the Preamp is zeroed with the input (shorted through U30). The coarse and fine zero signals are used to make up the *difference* between what is done during the retrace period and what the detector is sensing. The whole purpose of the coarse and fine zero modes is to apply to the Preamp a signal proporational to the difference.

Refer to Figure 5-5, Auto Zero Timing Diagram, for the logic associated with the Auto Zero function. The logic is basically a clocking sequence which is counted down through U15A and U15B (a 16 Hz signal is used as the trigger frequency to operate the successive approximation register). A series of signals are derived that allow various events to take place. U15A & B are counters, and U23 is a state decoder which selects three modes of operation. U23 allows: (1) retrace zero, then (2) the time interval for the coarse zero cycle, then (3) a one second time interval for the fine zero cycle. U16A, B, and C comprise a three bit comparator. The output of this array is true if the three most significant bits of U2 are equal. This will happen if the correction called for is at the extreme limits of either end. In other words, if it is desired to have one polarity of correction to equal an all true (1's) condition out of U10A, the opposite polarity of correction would equal an all false condition (0's). This indicates that the DAC is at the farthest limit of its ability to correct. This logic signal is fed to pin 12 of U17A (Zero Error). A Zero Error would be indicated if the operator left the RF on when trying to zero the N10 and the signal was too large for the instrument to correct or, if an unused channel were left on that did not have a detector attached. Then the zeroing process would have to be repeated after the RF was removed or the unused channel turned off. The final output of U23 (pin 6 – indicates zeroing process is over) will clock U17A. This means that the "Zero Error" will set U17 to produce an output that does two things: (1) connects an output signal called "Zero Lamp Off" (pin 9 at the input of the Preamp) through U8C and D to a 4 kHz clock from U15A. This causes the front panel "Auto Zero" lamp to start flashing to indicate an improper zero to the operator, and (2) guarantees that there is a signal at U25A to keep the clock running. As long as the clock is running, the lamp will continue to flash and the circuitry will continue to try to zero itself. When the cause of the Zero Error is removed then, at the end of the fine zero cycle when the clock comes from pin 6 of U23, there will be a "zero" at pin 12 of U17. This will go through and cause U8 to shut off the Auto Zero lamp and stop the zeroing cycle.

Normally, when the Auto Zero button is pressed, the lamp goes on and stays on until the zeroing is complete. If there is an error, the lamp will go on steadily during the first zeroing cycle, then the circuit will sense the error, and the lamp will flash until the error condition is cleared.

C11 and R29, as previously mentioned, are part of the Auto Zero circuitry. They function to cause a drastic reduction in the bandwidth of the entire front end system. The reason for this is that, when the front panel Auto Zero control is activated, it is necessary that the N10 be as insensitive to noise as possible along with having zero RF power applied. External RF and noise will cause the instrument to zero incorrectly, so it is important that the bandwidth be as narrow as possible. Thus, pin 14 of U18 is on during the entire Auto Zero cycle to reduce the bandwidth to a point where as much noise as possible is filtered out of the system.

5.3.3.5 Smoothing and Excessive Sweep Speed Functions

The Smoothing function is used when it is desired to obtain high resolution at very low power levels. This is done by sweeping very slowly and adding additional noise filtering. A signal from the microprocessor (activated by the "Smoothing" button on the front panel keypad) enters the Preamp at pin E (Smoothing Off) and proceeds to U29 pin 16. U29 switches and connects pins 14 and 15, which turns on C15 and provides higher capacitance for sweep error detection. The circuit is looking at low level log signals only. The signal coming from U4A pin 4 (Log Direct) goes to U4C which takes the anti-log, thus producing a current output from pin 9 of U4C that is proportional to the input signal level. The anti-log must be taken at U4C because there is no other place in the specific circuit configuration where the signal is available for use. A slight offset is provided by R86 to be sure that the circuit does not lock up or give excessive indications at low signal levels. The signal from U4C into amplifier U10C combines with the current coming through R86. Remember that the current from U4C is proportional to the signal level. The current from C22 and C21 (C22 only if Smoothing is OFF) comes from the horizontal ramp input from the sweep generator. The faster the sweep speed of the ramp, the greater the current flow through the capacitor. If this current exceeds the current from U4C, then U10A will output an error indication. For this reason, when there is very little current from pin 9 of U4C (very low signal levels), the sweep must be slower than at high signal levels where there is a lot of current. U1D is a comparator to convert the level from U10C into a logic level capable of driving U8. U8 is a pair of gates connected as an RS flip-flop so that, if the signal on pin 8 of U8A is driven low (indicating a sweep error), U8A will latch and the signal will be fed to pin 11 of the Preamp edge connector. This error indication will cause the "Sweeping Too Fast" light to turn on. The light will stay on until the "Fwd Trace" signal comes in through pin 3 of the edge connector. When the forward trace goes negative (during retrace), it will reset U8 causing the light to go out. The light will remain out until

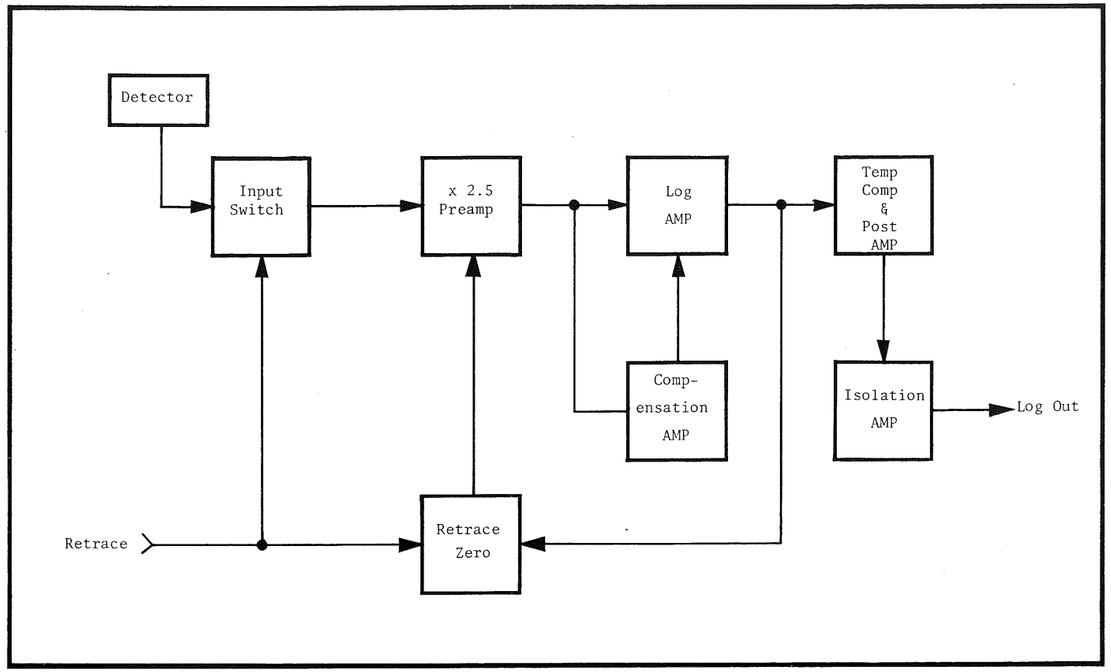


Figure 5-6 Reference Channel Preamp and Log Circuit (Bd # A5-SD 15228)

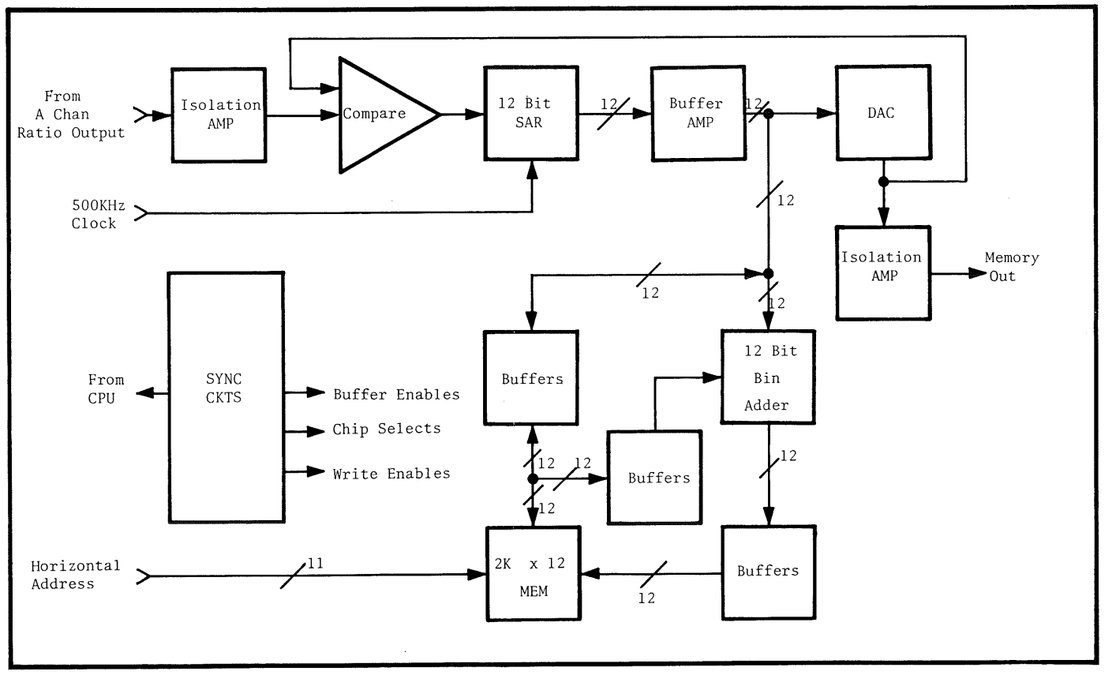


Figure 5-7 A Channel Memory (Bd # A6-SD 14880)

the portion of the signal is reached where the level is low enough to again light the lamp. The lamp will turn on and stay on for the remainder of the sweep, until it is again reset by the forward trace going low. This action makes it possible for the lamp to remain on long enough to be seen. Otherwise, the lamp might just flash on once or twice and not be seen. CR19 (connected to pin 2 – "A/B ON") is in the circuit to assure that the only time the above action takes place is when the Preamp is ON. This is necessary to be sure that the channel A board does not cause the light to go on when only channel B is in use, or vice versa. A signal must come in through the A/B ON connection to activate the board. U8A & B are both open collector devices with pull-up resistors R88 and R89, and allow the signal to enter and lock in only if the Preamp is on.

5.3.3.6 Test Point Indications

TP1 – +5V Power Supply. (Can be used for logic probe if necessary)

TP2 – Indicates the final output of the Preamp (100mV/dB)

TP3 – Logic (5V) Ground

TP4 – Log Low Signal. Will read 100 mV/dB up to -27 dBm.

TP5 – Log High Signal. Will read 100 mV/dB from -30 dBm up to +16 dBm.

TP6 – +10V Reference. Fed through U5A (Diff. Amp) to be sure that 10V is properly referenced to ground on this (Preamp) PC board.

TP7 – 0 ± 10 mV. Used to inject current into U19B to calibrate the log amplifier and check for proper operation.

TP8 – Reference Ground

TP9 – Output of the Low Level section of the Preamp (< -27 dBm)

TP10 – Output of the High Level section of the Preamp (> -30 dBm)

TP11 – Ratio (off board) Common

TP12 – +15V

TP13 – Grounded during part of the calibration procedure to remove detector compensation.

TP14 – -15V

5.3.4 *Reference Channel Preamplifier & Log Circuit* (Bd # A5 Schematic Diagram SD 15228)

(Use Figure 5-6 on page 5-12 and SD 15228 as aids to better understand the following discussion.)

The general operation of the Reference Channel Preamplifier and Log PC board (Assembly #15227) is almost exactly the same as the high level signal path of the Input Preamplifier and Log A (or B) Circuit board, as described in Section 5.3.3.2 of this manual. The Ref Chan Preamp has no low level section because the reference channel is used only for ratioing and will not be sensing signals below -30 dBm. Signal flow from the detector input, through the circuitry, to the Log R (100 mV/dB) output is exactly like that described in Section 5.3.3.2 with one exception. Since there are no low level signals involved, there is no signal combining stage required in what would be the combining amplifier, U5, on this board. U5 is a simple gain control stage that aids in compensating for temperature variations.

The compensation amplifier (shown along the bottom of the SD) is exactly like the A and B channel Preamp (as discussed in Section 5.3.3.3).

The self-test input of the Ref Chan board is also exactly the same as the A/B Preamp except that there is no low level channel that has to be turned off. This eliminates the necessity for an auxilliary output of the self-test circuit, as is required on the A/B Preamp board.

There is no necessity for an Auto Zero circuit on the Ref Chan board since the Auto Zero is only for low level signals (< -30 dBm). The Ref Chan board does have a retrace zeroing feature, but it too is almost identical to the A/B Preamp. There are some slight differences in implementation of the circuit, but the operation is essentially the same as described in Section 5.3.3.4.

5.3.4.1 Test Point Indications

TP1 – 5V Common Ground

TP2 – +5V

TP3 – Log Output. (100 mV/dB)

TP4 – +10V Reference

TP5 – On-Board Common Ground

TP6 – On-Board Preamp Output. This is the detector signal after being amplified by 2.5.

TP7 – Output of the Compensation Amplifier

5.3.5 *A Channel Memory* (Bd # A6 SD 14880

The A Channel Memory PC Board (Assembly #14879) has the capability of storing 2048 12-bit words. The 2048 words correspond to the 2048 addresses generated by the Horizontal and Cursor Board (SD 15188). The addresses are sent directly to the six 1K x 4 RAMs, U27 through U32. (Use Figure 5-7 – Block Diagram – on page 5-12 and SD 14880 as aids to better understand the following discussion.)

When a new address pulse enters the PC board through pin D of connector J6, the trailing edge triggers the 2 μsec 1-shot, U6A, which starts the conversion timing. Conversion is actually accomplished in Successive Approximation Register (SAR) U8 operating in conjunction with Digital to Analog Converter (DAC) U9. Both of these devices are 12 bit components. The output of U9 is converted from current to voltage by U25B. This voltage is then fed back to the input comparator, U24, where it is compared to the voltage which has been applied to the board at pin A (Ratio A) and passed through the isolating operational amplifier, U25A. Since U25A is an inverting op. amp., the signal is inverted and applied to comparator U25. The output of the comparator is the data input to SAR U8. U8 drives DAC U9 through the hex bus drivers U1 and U2. U1 and U2 are enabled by a signal called Memorize 1 or Memorize 2. That signal is generated by an and-gate from two signals, so that if the circuit is going through the Memorize 1 or Memorize 2 cycle, the Memory 1 or 2 will enable the hex bus drivers. Thus, anytime a memorizing sequence is in progress, the bus drivers are simply a connection from the output of U8 to the input of U9.

At the same time that U9 is being driven, the U27 through U32 RAMs are also driven from the U21 and U14 hex bus drivers. In this way, all 12 bits of information are applied to the RAMs at the same time that U9 is completing the conversion in conjunction with U8. When U8 produces a conversion complete signal, the write and the chip select lines of all of the RAMs are cycled through, and the digital word that is present at the DAC at that time is stored in the RAMs.

The process of keeping track of the status of the cycle is done by the U26 counter and the U17 decoder devices. When a signal comes into the circuitry that tells it to "memorize", the cycle starts with the U26 counter being set to contain all 1's. This is done through the master reset (MR) line of U26. A count down is then initiated, using the down-count clock input to U26. The action will start from a full count and then count towards zero.

While the count is regressing, U8 is being clocked by the same 0.5 MHz clock. Nothing is happening at first at the decoder (U17) because only three outputs are used, corresponding to count 3, count 2, and count 1. As the down count proceeds, it will eventually get down to count 3. At that time, pin 4 of U17 will go low and produce a load (clock) pulse which goes to the U12 and U19 hex latches. That action causes whatever digital word is present at U8 at that point to be loaded (all 12 bits) into U12 and U19. U12 and U19 will hold the word until it is needed. As the counting cycle continues, the next pulse will decrease the decoder down to count 2. This releases the line at pin 4 of U17 and grounds the line at pin 3. The line at pin 3 is an active low, and grounding it will have several enabling effects. The pin 3 output feeds the output enable of U20 and U13 (hex bus drivers that pass averaged information to the memories) but, to be fully enabled, output enable 1 (labeled not-output enable) of U20 and U17 also has to go low. At this point in the cycle, output enable 1 is not yet low since the cycle has not proceeded far enough to enable both outputs.

At the same time the above action is taking place, the 1 μsec timer, U6B, is clocked. The clocking will product a 1 μsec pulse at both the Q and Q-bar outputs of U6B. The Q-bar output, monitored at TP3, will appear at the input of or-gate U23A. The output of U23A is the write-enable input to all of the RAMs. Write-enable means that whatever data word is available at the inputs to the RAMs at that point will be written into the RAMs when the line is pulled low. Also, the Q output of the U6B timer is driven through a set of gates to produce the necessary bank select. The correct bank will be chip-selected for whatever address is present at the moment. The 1 μsec pulse is used to both write-enable and chip-select the RAMs. The write-enable will only be active if the system is in a write mode. This means that the circuitry must actually be converting and writing data into the RAMs. When data is read from the RAMs, only the chip select function will be active; the write-enable output of the U6B timer will not be used.

The preceding description has covered what happens when count 2 (on the way down to zero) is arrived at in the cycle. When count 1 is reached, the pin 2 line of U17 will go low (monitored at TP2). This line is called Not-Start Conversion and goes to the not-start input of U8. The line going low will stop the conversion process and also stop the counting in U26. The U10A gate is disabled so that the clock pulses can no longer get to the counter. If the counter can no longer be clocked, the cycle will stop at that point.

All of the above process will be repeated anytime that there are two conditions present. One of these is, if the beam on the CRT has moved far enough to go from one address to the next, the new address will be digitized at the new horizontal position. The other condition is the generation of the signal that will tell the circuitry to memorize. This is actually two signals, since the A channel memory memorizes twice. The first memory pulse commands the memory to store the signal that appears at the input. The second pulse commands the circuitry to memorize and average the second signal with the first signal. The end result is the storing of the average of the two memorized sequences in the A channel memory. This function is useful for return loss measurements where the average of short and open calibration signals needs to be taken and stored. The commands to memorize come from the CPU. The first memorized signal is applied to U18A. U18A will latch and wait until the signal can be passed to the following latch, U18B. U18B will then be clocked when the retrace pulse appears. The reason for this sequence is that the circuitry must not attempt to memorize during the retrace period of the CRT. This is assured by memorizing everything from the point where retrace stops until the next retrace starts. This allows memorizing only during the forward trace of exactly one sweep. To accomplish this, U18B is clocked from the positive edge of the retrace signal. This means that as soon as retrace begins, the U18B input information will be transferred to its two outputs. The Q output is used to enable two of the hex bus drivers, and the Q-bar output is used to enable the opposite two hex bus drivers that connect the output of U9 to the memories. The U18B Q output going high will disable U22 and U15. The Q-bar output going low will enable U21 and U14. This means that, since U21 and U14 will be enabled, it is now possible to drive or load the memories from the data lines on the output of U8. The Q-bar output of U18B (monitored by TP5) is called the Not-Memorize 1 line. When this line becomes active it clears input latch U18A, and then is ready for the next memorize signal. At this point, nothing has happened until a new address signal is received (after retrace is complete and the CRT is ready to start the forward trace). The address signal must wait for the end of retrace because U6A (Clear Direct) input is driven from the retrace, and inverted by U7A. Then, a new address signal will produce (at U6A) a master reset for the conversion counter, U26, and start the conversion cycle over again. After the first conversion has been completed (when the operator signals that the set-up has been changed from a short to an open), the CPU sends a memorize 1 and 2 divided by 2 command. The second memory pulse is latched in U11A to be used by U11B when required. U11B will transfer its data into an active state at the next retrace pulse. The Q output will disable hex bus drivers U21 and U14. The Q-bar output going low will enable U20 and U13. U20 and U13 will connect the outputs of a set of adders, U3, U4, and U5. These are connected so that the RAM memory can be loaded from the adders. The adders are then fed from the data already memorized and held in the U19 and U12 hex latches. That information is then added to the new data acquired when the second memory signal was digitized. The resulting data is shifted to the right once which divides it by two. This average is then loaded into the RAM.

Another output that appears on the PC board during the memorize 1 or 2 cycles, or during the interval when the circuit is waiting for the retrace signal to activate the memorize 1 or 2 cycle, is a signal called Not-Busy. This signal will go low, signifying that the memory circuits are

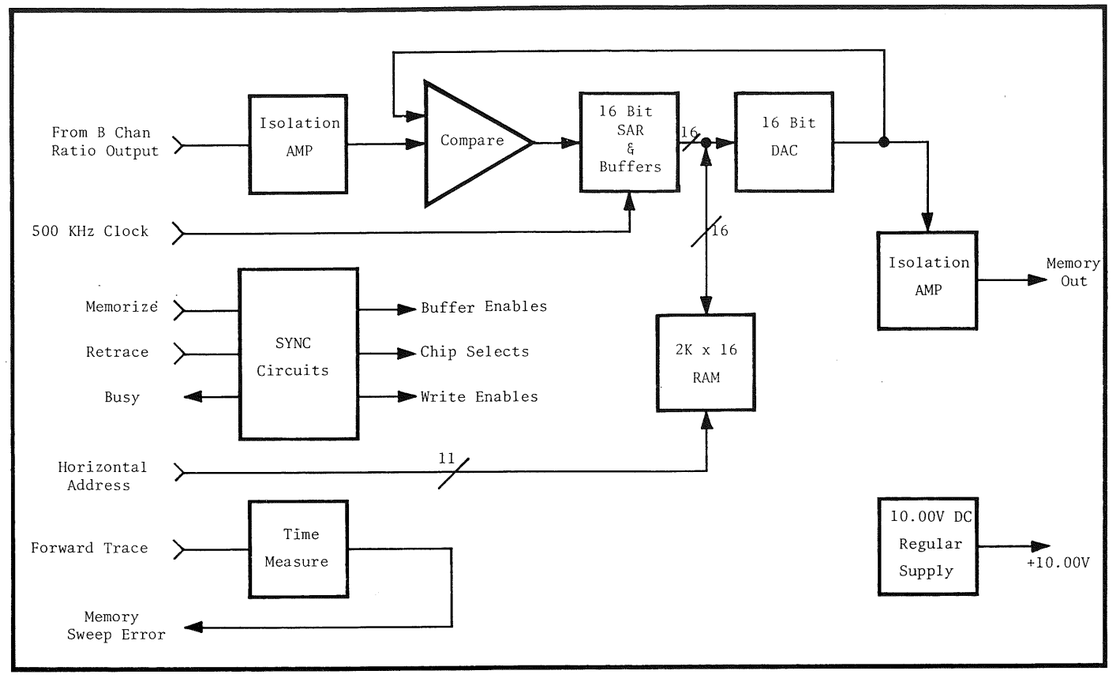


Figure 5-8 B Channel Memory (Bd # A7 - SD 14888)

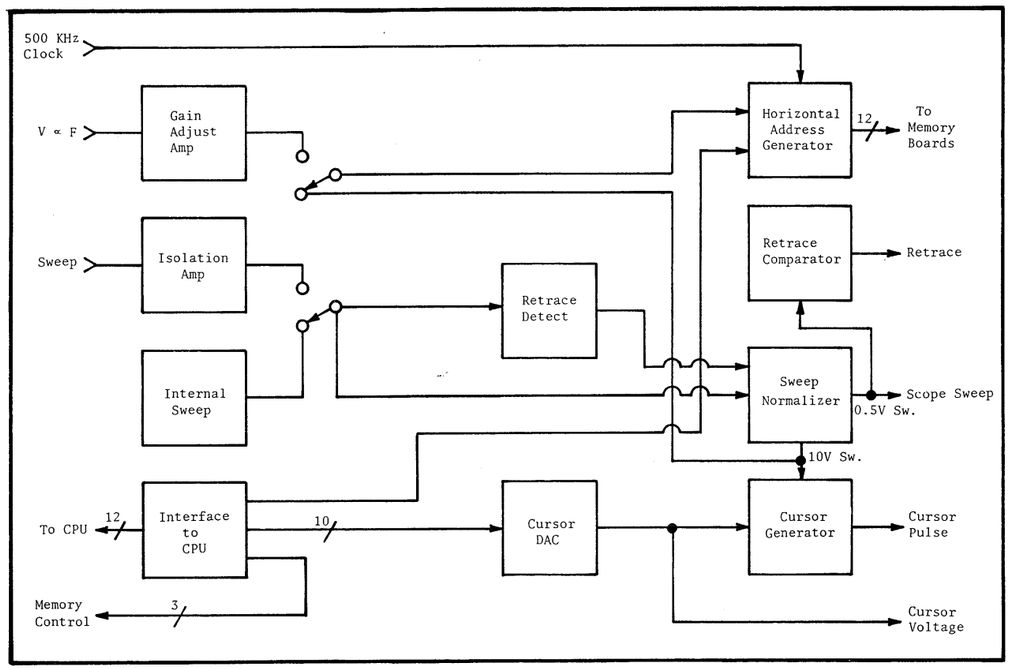


Figure 5-9 Horizontal Cursor Board (Bd # A8 - SD 15188)

busy and not able to accept additional commands. Anytime that the circuits have been commanded to memorize, they will stay busy until asked to memorize twice. In this way, they are able to go completely through the memorizing cycle.

The output of the A Channel Memory board is at J6, pin B (monitored by TP9). The output is produced through isolating op. amp. U25C so that grounds can be transferred.

5.3.5.1 Test Point Indications

TP1 – 5V Logic Voltage

TP2 – Start Conversion. Goes low when count 1 of countdown is reached.

TP3 – 1 μsec Pulse when U6B is clocked. Used to write-enable the RAMs.

TP4 – When low, connects the adders. End result is placing of averaged data into the RAMs.

TP5 – Enable Signal to hex drivers. Connects DAC to RAMs.

TP6 – +15V Supply Voltage

TP7 – Master Reset. (2.2 μsec pulse) Starts new conversion cycle.

TP8 – -15V Supply Voltage

TP9 – Memory Board Output

TP10 – 15V Common Ground (On-board signal common)

TP11 – Ratio Common Ground

5.3.6 *B Channel Memory* (Bd # A7 SD 14888)

The operations performed by the B Channel Memory board (Assy. #14887) can be divided into five different functions. Included in these are: (1) Memory Control, (2) A to D Conversion, (3) Random Access Memory (RAM), (4) Reference Voltage Supply and, (5) Sweeping Too Fast signal initiation. (Use Figure 5-8 – Block Diagram – and SD 14888 as aids to better understand the following discussion.)

5.3.6.1 Memory Control

The dual latch device, U8, is used to sense the presence of a memorize pulse from the CPU. The pulse will set the latch of U8A so that the Q output will go high. Then, at the arrival of the first retrace pulse, that will be transferred to the U8B latch output. The active low (Q-bar) output of U8B is applied to the clear input of U8A so that, as soon as data has been sensed by U8B, the information is cleared. The signal is then transferred through U9C and the CR1 diode, to a line called Not-Busy. This line will become true (go low, since it is an active low), and will tell the CPU that something is happening in the memory circuit and not to disturb it. Data from the Q-bar output of U8B is also used, through U9A and U10A, to steer the write-enable and chip select pulses to the correct RAMs.

New address information from the CPU enters the board at J7, pin D. This signal originates at the Horizontal and Cursor PC board, and indicates that the trace has moved far enough from the left to the right to arrive at a new address. The new address signal will activate timer U3A to produce a 3 μsec pulse from its Q-bar output. The 3 μsec pulse is called the Not-Start Conversion pulse and is an active low line that can be monitored at TP10. It is used as the start pulse for both Successive Approximation Registers (SAR) U2 and U1 in the A to D conversion process. Pin 3 of U3A is the reset direct and makes sure that U3A is reset during retrace. The end of the retrace will cause the start of the memorizing process. One additional timer, U3B, provides a 1 μsec pulse that is used to produce a vrite-enable signal for the RAMs at the correct point in time during the conversion process. This assures that, once converted, the data is stored in the RAMs.

5.3.6.2 A to D Conversion Process

Analog data is applied through the Ratio B input at J7, pin 1, to isolator U19A and appears as one input to comparator U21. The other input to U21 is derived from the output of the two DACs, U13 and U14. Since a feedback loop is formed from the output of the DACs back to the analog input (compared with the analog input), the closed loop causes the DACs to become A to D convertors. The outputs of the DACs are constantly being compared with the analog input to ensure that the DAC outputs will try to be equal to the analog input voltage. In the process of becoming equal to the analog voltage, the digital word required to produce that condition will appear at the inputs to U13 and U14. U13 and U14 are driven by a pair of Successive Approximation Registers, U1 and U2, through two data buffers, U6 and U7. U6 and U7 are needed because the data that feeds the two DACs will arrive either from U1 and U2 during tthe memorize cycle, or from the RAMs during the readback cycle. Hence, the DACs are always busy performing one function or the other.

When the N10 unit is first turned on, information in the RAMs is totally random and appears at the output of the DACs as a very large noise signal. It is possible that there could be enough noise to allow some to leak through to the CRT display and cause a slightly noisy display (only after turn on). This condition can be cleared by placing anything into the memory (go through memory cycle).

The output of the DACs U14 and U13 are applied to U20A and U20B which convert from current to voltage. U20A has a large feedback resistor (R13), 4.02K, and U20B has a small feedback resistor (R34), 511 ohms. Also, the voltage from U20A is fed through a 10K resistor (R14), while the output of U20B is fed to the same point through a 127K resistance (R35) which is 12.7 times as large as U20A. The combination of the two resistive changes produces a total output from U20B that is 1/100th the size of U20A. The reason for all of this is to produce a vernier adjustment of U14 by U13. U14 and U13 are both 8 bit counters (16 bit total), but they overlap so that only 15 bits of true data are available from the DACs. A full 16 bits would give, roughly, one part in 65,000 of resolution, whereas 15 bits gives one part in 32,000. In actuality, what is really produced is one part in 26,000, so the 15 bit resolution is not quite achieved. The DAC output data is combined at the U20C input and appears buffered at the U20C output. The pin 8 output of U20C is the point at which the feedback to U21 occurs. This means that this is the point where the signal is forced to be equal to the Ratio B input. From U20C, the signal goes through the U19B isolator stage to the output of the PC board, MEM B, and is monitored by TP3.

5.3.6.3 Random Access Memory (RAM) Storage and Function

There are two banks of RAM containing a total of 4K bytes of storage capacity. This capacity is necessary because there are 16 bits (2 bytes) of data (from the DACs) to store for 2048 locations, therefore 4K bytes of RAM are required. U15 through U18 and U22 through U25 store 1K x 4 bits

in each chip, adding up to a full 4K bytes of data storage.

Data from the RAMs are applied to the DACs if the DACs are in a read mode, or is stored from the buffers feeding the DACs during a write cycle. Bus contention is avoided by having the buffers from U1 and U2 that feed the RAMs' data during a write cycle, operated from the same circuitry that switches the write enable and chip select lines of the RAMs. This is controlled, as mentioned earlier, through U9A and U10A.

5.3.6.4 Reference Voltage Supply

This PC board (B Channel Memory) is the only point in the N10 unit where the reference and 15V common grounds are tied together (shown at the middle of the right side of the SD). This circuitry constitutes the analog voltage reference supply, and produces an exact, very stable, carefully adjusted 10V reference. This reference is adjusted by R39 to 10 ±0.002V. This ±0.02% deviation means that a precise 10V can be delivered, as required, to other PC boards in the system that require the analog reference voltage. The 10V reference is derived from U12. U12 is a very stable Zener diode located on a chip that also has a heater. The heater is tied between the positive and negative 15V supplies, and is thermostatically controlled. This assures that the temperature of the Zener is kept very close to a constant value. The Zener is rated at 7V and is multiplied to 10V by U19C.

5.3.6.5 Sweeping-Too-Fast Error Signal Production

The sweep cannot be too fast while memorizing or the DACs will not have enough time to go completely through their conversion process. Bits of data will be lost. If the sweep is too fast, this will be indicated by the instrument through the flashing of the Sweeping Too Fast error light, audible beeping, and a lock-up of all of the instrument's functions (except CLEAR) until the sweep generator is slowed down sufficiently to allow accurate recording.

The memory sweep error monitoring circuit is composed of both sections of U5, U11A, and peripheral components. U5 is a twin timer, with U5B generating a very short 1 μsec pulse and U5A producing a very long 120 msec pulse. The two timers are sequentially triggered by a signal coming into the board at J7, pin 3, called Forward Trace. The forward trace signal comes from the Horizontal and Cursor PC board, and will be high when the CRT spot is moving from left to right (during memorization).

When the forward trace cycle is initiated and the spot just starts to move to the right, the line will go high. At that point, U5A is triggered and raises its Q output line, pin 13. The Q output is applied to the D pin of the U11A latch. Nothing happens at U11A at this point except that the D input is in a high condition. If, before the 120 msec delay time is completed, there is a termination of the forward trace (gets all the way across the CRT screen and starts retrace), the forward trace signal will drop. The signal going low will trip U5B which will produce a 1 μsec pulse that will clock the U11A latch. If this happens before the 120 msec is up on the timer, the Q output of U11A will go high. This will send a signal to the CPU, via the interconnection through the mother board, that the sweep is moving too fast for the memory to properly capture it. The CPU will then stop all further action, will not attempt to memorize, will keep the keypad dead, will flash the Sweeping Too Fast light, and will give an audio indication through the sounder on the front of the instrument. This condition will continue until the sweep generator is slowed or unless the CLEAR button is pressed. Then the CPU will go back to reset and be ready for another command.

5.3.6.6 Test Point Functions

TP1 – 15V Common Ground

TP2 – 15V and Reference (Ratio) Common Ground Junction

TP3 – Output of the B Channel Memory board

TP4 – 10V Reference Output

TP5 – -15V

TP6 – +15V

TP7 – 5V Common Ground

TP8 – +5V

TP9 – Write Enable Signal to the RAMs

TP10 – Start Conversion Signal to the DACs

5.3.7 *Horizontal and Cursor Board* (Bd # A8 - SD 15188)

(Use Figure 5-9 – Block Diagram – and SD 15188 as aids to better understand the following discussion.)

5.3.7.1 Horizontal Sweep Circuitry

The Horizontal Sweep Circuitry portion of PC Board Assembly 15187 performs three functions. The first is to receive the ramp signal from the sweep generator and properly scale it. The second purpose is to generate horizontal address information so correction values can be located in the N10 memory. The third function provides an internal sweep if no sweep generator is available and CW power is to be measured.

The sweep from the sweep generator can be applied to the N10 in either symmetrical or asymmetrical form. Symmetrical would be evenly spaced above and below zero (e.g., -5 to +5V), and asymmetrical would be unevenly spaced (e.g., 0 to 20V). The circuitry will scale it so that almost any sweep input is turned into an exact 0 to 10V ramp for internal use.

The scaling circuit regulates the bottom and top levels of the sweep input. An auxiliary circuit is used to detect when the sweep has ended and retrace has started. With the sweep input at U11A of the auxiliary circuit, a retrace signal will be generated at the start of the retrace, and terminated when the retrace stops again. Thus the auxiliary circuit, composed of U11A, U1, U9A, and U6B, tells the scaling circuitry when to look at the sweep to adjust the amplitude at both the top and the bottom.

The ramp voltage from the sweep generator comes into the N10 as a sawtooth waveform through the Aux 1 connection of the back of the D14 Mainframe. The voltage is then applied to buffer amplifier U26B. R9 and R10 divide the voltage by two. This is necessary because the level from the sweep generator could come in as high as 20V, which would be beyond the dynamic range of the circuit. From U26B, the external sweep goes to analog switch U25B. Depending on the command it has received from the N10 microprocessor through U24, U25B will select either the external sweep from U26B or the internal sweep generated by U18A and U26C. Whichever sweep has been selected then goes into U11B for scaling and to U11A to determine the starting point of the retrace cycle. U11B is an amplifier which allows an offset to be used so that the sweep will always start from a -2V reference point. The sweep will

then go down to some arbitrary level depending on the magnitude of the sweep coming in from the sweep generator. U9B and C form a precision peak detector with feedback, looking at the output of U11B. This peak voltage is compared with the -2V standard reference level and any difference is amplified by U9D. U9D provides a current source through R82, with the magnitude and polarity determined by how far away the voltage on pin 8 of U9C is from the -2V reference. The reference is applied from voltage divider R76 and R80. If pin 8 of U9C is exactly equal to the reference, U9D will adjust itself to produce no current at all.

At the start of the retrace cycle, C24 is reset for an 880 μsec interval. This is caused by a current switch in U19A at pin 3 which discharges C24 to prepare for a new cycle. This guarantees that, to whatever point C24 was charged through CR8 for a specific sweep cycle, it will reach an accurate new peak value on the next cycle. Each cycle is completely independent.

At the end of the retrace cycle, U8 will trigger to close switch U4A for a period of 880 μsec. During the time the switch is closed, C22 will charge either positive, negative, or not at all depending on the relationship between the reference level and the level from U9C. The voltage on C22 will either increase, decrease, or remain constant. This will cause the voltage at pin 7 of U3A to shift to a level sufficient to set U11B to exactly -2V.

U3B operates exactly like U3A, U10B operates like U9B, U10D like U9C, and U12C like U9D, previously described. When the zero level (start of sweep) was set, it was only necessary to apply a straight dc offset to the input to bring it to the correct value. To scale the ramp voltage to the correct level at the end of the sweep, a multiplying procedure must be used. U2 is connected as a transconductance multiplier controlled by U19C. U11C feeds U19C with a properly scaled control signal. U19C is an exponential amplifier whose function is to provide a constant loop gain independent of the amplitude of its input.

The voltage output of U19C goes from pin 15 into pins 2 and 9 of U2. The only function of U19B is to supply, through potentiometer R96, a constant current level to U2. The usage of switch S2 will be discussed in the calibration procedure section of this manual. S2 is used to switch the circuit to a known state so adjustments can be made using potentiometers R96, R77, and R103 during the calibration procedure. It is very important that the proper, step by step, calibration procedure (as detailed in the manual) be used or the circuit will be temperature sensitive, even if it were working properly after some kind of informal, unspecified calibration was performed. The differential current coming from pins 7, 8, 1, and 14 of U2 is converted to a single ended signal by U10A. The 5V output of U10A goes into a control circuit similar to that previously described for the start of the sweep. The 5V output of pin 14 of U10A is multiplied by two in U10C. R109 is used to adjust the voltage to exactly 10V. The 10V ramp is applied to the unity gain differential amplifier U26D along with the +5V reference from U12B (measurable at TP6). This offsets the 10V ramp so that the output at U26D pin 8 is ±5V. This is attenuated 20:1 by R140 and R146. The final output at pin A (Horiz [+] Signal) is exactly 0.5 ±0.25V (measurable at TP10), which is the correct amount to properly operate the D14 Mainframe interface circuitry.

5.3.7.2 Cursor Control Circuitry

The Cursor Control circuitry portion of PC Board Assembly 15187 is composed of U23, U12A, U12B, U5B, U5C, U7B and associated components. U23 is a DAC. U12A converts output current into voltage with a full scale capability of 10V (0 to 10V scale). U23 is controlled by the Central Processing Unit (CPU) of the N10 through Parallel Peripheral Interface (PPI) U24. The "A" port and a section of the "B" port of U24 comprise the output lines to U23. Through this connection, the CPU can control the analog voltage measurable at TP13. This voltage is compared with the ramp voltage by twin comparators U5B and U5C. These two comparators sense the analog voltage coming from the DAC and compare it with the 0 to 10V ramp. U5B triggers first and, as the ramp crosses the threshold of U5B, the output will go positive. The positive transition will cause the U7B latch to be set. This means that the cursor output voltage level goes up and will stay up until the ramp sweeps about 1% beyond. Then U5C will cross its threshold and produce a negative-going output. This clears the U7B latch and terminates the cursor pulse. In this way, the position of the cursor pulse is dependent upon the voltage generated by the DAC which, in turn, is controlled by the CPU. U18C will change the 0 to +10V cursor voltage produced by the DAC to a -5 to +5V. This voltage is used by the D14A for positioning the full-screen height, vertical line cursor at any desired location on the CRT screen.

5.3.7.3 Horizontal Address Generator

Another segment of PC Board Assembly 15187 is used to produce horizontal addresses for memory storage. This circuitry can take either of two inputs and generate a digital address corresponding to the position of the sweep at any particular instant. The inputs can be either the scope sweep through the 0 to 10V ramp, or a separate external input used for V ∝ F sweep. This V ∝ F sweep comes from a sweep generator that produces voltages that are directly proportional to the instantaneous frequency of the sweep.

In either of the above cases, the address generator works essentially the same.

If the internal 10V ramp is used as the input, it is applied through U25A to a sample and hold circuit. This circuit, composed of U17, U18B, and C5, is used to form the bottom end of the sweep. This voltage could be 0V or slightly above or below, but the sample and hold circuit will always set the correct level. The purpose is to assure a reference point which will establish the correct starting level in relation to the total excursion of the ramp. Therefore, with one end of the address coming from the sample and hold circuit, the upper end of the ramp excursion is applied directly as sweep voltage to the comparator pair, U13B and U13D. These have latches U15A and U15B on their outputs. The latches are clocked by the 500 kHz system clock and cleared by timer U16. This latching and clearing action is necessary to fix the maximum speed at which the address generator is clocked. The clocking cannot get ahead of the A and B channel memory circuits which are speed limited. The timer, U16, has two separate timing outputs. The memorizing or slow mode is about 18 μsec, and the readback or fast mode is about 1.6 μsec. The purpose of the timer is to set the maximum clock speed into the address generator.

The other inputs of comparators U13B & D go to the DAC, U27 and U12D. U27 is a 12 bit DAC and U12D converts from current to voltage. Offsets are supplied on both ends

during this conversion process to allow the production of slightly more voltage range than is required. When the 0 to 10V ramp is fed into the system, it is very important that the voltage handling capability of the DAC is not exceeded. For this reason, the DAC has the ability to handle more than 10V. It can go slightly below 0V on the low end and slightly above 10V on the high end, by about 3%. The output of the DAC is compared with the 10V input ramp and, depending on whether it is larger or smaller than the input ramp, the digital word input of the DAC will either increase or decrease. This is done by applying clock pulses to either an up or down input in the 4 bit up/down counters U20, 21, 22, 28, 29, and 30. These counters have direct load capability. During the up/down phase (forward sweep), the up/down pulse inputs are supplied from the latches at the output of the comparators. The comparator decides whether an increase or a decrease is required, and applies the proper voltage to the latches. The clock pulse from the 500 kHz system clock puts the timing information into the latch. This appears as either an up-count or a down-count input to the counter. If the circuit is operating in the normal mode (counting up), an up pulse is required. The U15A latch will trip and produce a low at its output. This will produce a negative transition at the count-up line of U28. The high to low transition will also be applied through U14C to the timer, U16. A clearing pulse is then produced at the output of U16 as soon as the timing information is transferred from the latch to the timer. U16 generates the clearing pulse just long enough to clear the information and is then terminated because the clear line will be pulled down by the timer.

A sharp, narrow pulse comes from the comparators to the counters to keep the counters tracking the input ramp voltage. As the counting-up function progresses, a larger binary word is fed into the DAC (U27), and the voltage will increase along with the incoming ramp voltage. When the top of the ramp is reached, a Retrace and Not-Retrace signal is generated. One of the functions of the not-retrace pulse is to change the mode of the up/down counters. U28, U29, and U30 will go into a parallel load mode, and the 4 bit inputs to the counters are fed directly to their outputs. In other words, they become simple connectors and are transparent to the signal. The 4 bit inputs from U20, U21, and U22 will feed the digital word into the DAC to force it to go to the start voltage. The up/down pulses for U20, U21 and U22 come from nand-gates U14A & B. These gates are enabled by the retrace signal and clocked by the 500 kHz system clock. The clock pulse is steered to the up/down inputs by comparators U13A & C. The retrace comparators are fed from a held dc voltage that corresponds to the bottom end of the 0 to 10V ramp. As soon as the retrace mode becomes active, the comparators immediately attempt to force the DAC to a low level. This means that the DAC will be rapidly counted down and, as soon as the low level voltage is stable (held by the sample and hold circuit), the output of the DAC will not change until the retrace cycle is completed. The action will then transfer back to a normal counting mode, as previously described. One of the things that happens in the transition from the trace to retrace state or vice versa is a change in the ramp at the bottom end ($\approx$ 0V ± a few millivolts). A small hysteresis is applied to the comparator (U5A) that tracks the bottom end of the ramp. As soon as the ramp starts its voltage increase (moves a few millivolts up) the hysteresis of U5A will be overcome and a signal will be produced called Not-Start of Trace. The production of this signal means that the trace has started forward and, to indicate this, a sudden change is produced that clears the latch of U7A. When the sweep starts forward again, the forward trace is generated and is used on the input boards to enable the circuit that will detect the "Sweeping Too Fast" condition. When the U7A latch is cleared, its Q output (called Retrace) is reset, and the address generator will begin to follow the sweep toward +10V. The forward trace will be high only during the time that the trace is actually moving from left to right, and will be low at any other time. The purpose of this function is to have a signal available that will sense when memorizing can take place within the readable portion of the trace. The start of the forward trace also triggers the sample and hold switch and loads the bottom end sampler (U17) so that the bottom level of the input ramp is held. This is done because the external sweep may never come into the N10 exactly at zero; it could be 5 - 6V or some other odd range. For precise address generation, the circuitry must always know where the bottom level of the ramp will correspond to specific positions on the scope forward. At the bottom end of the trace, the comparator is set until it crosses the hysteresis level on the way up. During this time, it is sampling the input level at the bottom of the trace. When the hysteresis level is overcome, the circuit knows that the trace has started forward. The Not-Start of the Trace pulse is then terminated.

5.3.7.4 V ∝ F Circuitry

When the V ∝ F mode is to be used, the external input from the sweep generator is connected to the Aux 2 input on the rear of the D14 Mainframe. (It should be remembered that the Aux 1 input – Scope Sweep – is *always* required.) The signal comes into the Horizontal and Cursor PC Board through input connection pin B and goes to an isolating 2:1 divider. This divider consists of a pair of 1 meg resistors, R1 and R2, and provides a 2 meg input impedance plus isolation to prevent damage in case of an improper signal input. The signal is then applied to U26A. U26A is a variable gain amplifier whose gain is set by switch S1. S1 makes it possible to set the gain to either unity, 2. 4. 6. or 8. By the time the 2:1 input divider is added, a net gain of 0.5, 1, 2, 3, or 4 will be realized. A small sweep signal can be fed in and it will cause the generation of a large digital ramp. The ramp will correspond to specific positions on the scope sweep, similar to the 0 to 10V internal ramp. The gain will be set according to the maximum voltage input at the Aux 2 connection. Otherwise, the system works just the same as the internal sweep circuitry previously described. It should be remembered that the horizontal address generator is not capable of going negative, so care should be taken never to apply a negative voltage.

5.3.7.5 Test Point Indications

TP1 – 15V Common

TP2 – +15V

TP3 – -15V

TP4 – 0 to 10V Ramp

TP5 – Bottom of internal 0 to 10V ramp. (0V ± a few millivolts)

TP6 – +5V Reference. This is a dc reference established by U12B from an external 10V reference which comes from the B channel memory board. It should be accurate to within 0.25%.

TP7 – Not Used

TP8 – Cursor Pip

TP9 – Sweep (internal or external) Input to the scaling circuitry

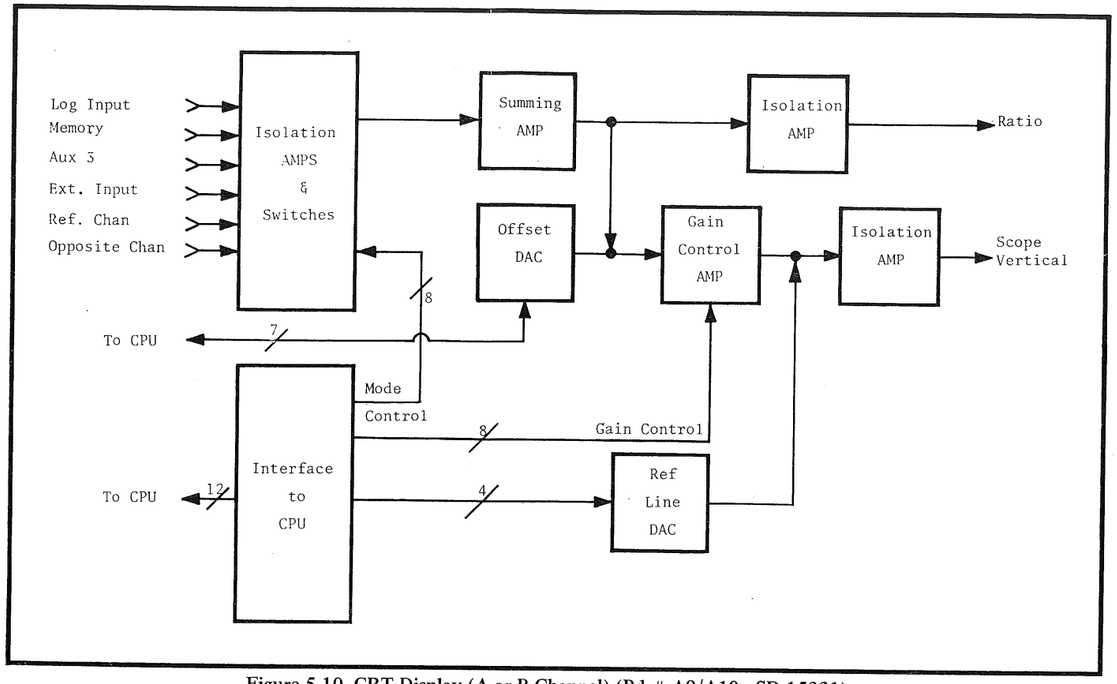


Figure 5-10 CRT Display (A or B Channel) (Bd # A9/A10 - SD 15331)

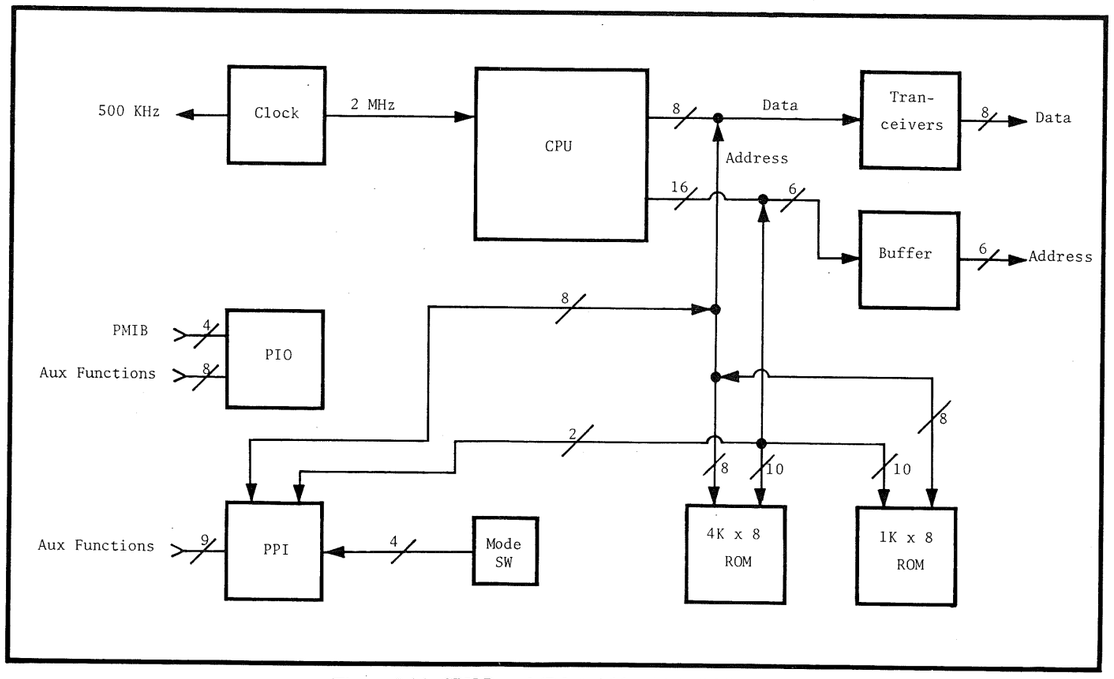


Figure 5-11 CPU Board (Bd # A11 - SD 14964)

TP10 – Horizontal Output (-0.25 to +0.25V)

TP11 – 5V Common

TP12 – Forward Trace

TP13 – Cursor Voltage

TP14 – +5V

5.3.8 *A & B Channel CRT Display Driver* (SD 15331 Bd #A9/A10)

The CRT Display board combines all analog signals for display on the D14A Mainframe CRT, for use in ratioing, and for display of the cursor digits on the front panel of the N10 unit. The signals to be combined are the A and B channel inputs from the detectors, the memory data from the A or B channel memory, the ratio signals from the auxiliary inputs which can either be external or from the GPIB, the channel ratio signals from the opposite channel, and the ratio signal from the center or reference channel. Also processed by the board are offset and reference line positioning information (controlled by the CPU), the marker and cursor pip signals, and the Aux 3 (Peak Power) input from the rear panel of the D14A Mainframe.

The CRT Display PC board (assembly #15330) is identical for both A and B channels. When the board is plugged into receptacle A9 of the N10 unit, it will process information for channel A (as shown on the SD). When inserted into receptacle A10, it will process information for channel B. (Use Figure 5-10 – Block Diagram – on page 5-20 and SD 15331 as aids to better understand the following discussion.)

5.3.8.1 Signal Combining Controls

All potential combinations are controlled by a set of analog switches, U8 and U9. These switches are controlled through the A port of the Peripheral Interface adapter, U18, which is controlled by the CPU. The A port is the mode control port, and it is what determines the settings of switches U8 and U9. U8 and U9 select what signals will be combined at the summing junction of U2.

The input from the detector (Log A) is applied to the ground isolator, U14A. The signal then goes to the top switch of U8A which is controlled from the 1 line of U18. The line is pulled low causing the switch to close, thus connecting the output of U14 A to the input of U2. U2 is a unity gain amplifier whose output will be similar to the Log A input. If the Log A input is positive, then the output of U2 (measured at TP2) will also be positive. The U2 output goes to another isolating stage, U3, which supplies the signal from the A or B channel input to the gain control switches, U4 and U10. These switches control the input and feedback resistors for the gain control stage, U11. The output from U11 goes through ground isolator U12B and then leaves the board to supply the A or B channel CRT outputs. The CRT outputs are the deflection signals that will cause the beam to move on the CRT.

U3 is also a combiner stage that not only supplies signals to the switches, but also combines the CPU controlled offsets to be used at the output. This offset is accomplished through the 12 bit DAC register, U6. A digital word is supplied to the input of U6 from the CPU. The output of U6 is buffered by U5 and produces an output that feeds U12. At U12, the signal is offset and the gain is adjusted so that U12's output will appear as 1V per 10 dB of signal (60 dB would appear as 6V at U12A). If the offset is set to 0 dB on the front panel of the N10 unit, then the offset voltage at pin 14 of U12A will be zero. However, the offset at the DAC buffer U5, pin 6, will be about -6V. The U6 DAC is supplied with a 10V reference at pin 15 which comes from the 10V isolator stage, U12C, pin 8. The 10V reference from U12C also goes through R82 to U17, and as an offset voltage to U12A through R42. In this way, all of the circuitry is tracking with the very stable +10V reference.

The output voltage from U5 is supplied, through U12A, to the combiner stage at U3. U3 combines this voltage with signals from the A or B input or other ratio signals as selected by the front panel controls. The output of U3 is gain adjusted through U4, U10, and the corresponding amplifier, U11, so that any available dB/DIV is selectable from the front panel. The output of U12B is then scaled to 50 mV/DIV which is sent to the D14 interface board. U12B also receives signals from the reference line DAC, U17. U17 has discrete levels that are selected by the reference line controls on the front panel of the N10. Any desired offset can be set to select one of the CRT display graticule lines to be the reference line for the display. The voltage from U17 is buffered by U12D and, at the input of U12D, appears at a 1V/DIV level. This level is divided down by U12D so that, at U12B, it appears as 50 mV/DIV.

Also combined in U17, along with the reference information, are the cursor pip and Aux 4 external inputs. The cursor pip is supplied to the 8 bit input (pin 9) of U17 so that it will produce exactly one-half of a division deflection on the CRT display trace. The cursor pip is not normally required when the N10 is used with a D14A Mainframe, as the cursor is a vertical line. If an X-Y plot of the CRT display is to be made, then the cursor pip may be wanted so it will show on the plot. For this reason, the cursor (bit 8) is gated with a line controlled by the CPU through pin 37 of U18. In order for the N10 to recognize whether or not it is plugged into a D14 or D14A Mainframe, pin 13 of U18 is brought out to the rear connector of the plug-in. It will be pulled high by R128 if it is installed in a D14 (no suffix).

The Aux 4 external input comes from the BNC connector at the rear of the D14A or D14 Mainframe and supplies marker information when the marker function has been connected to the instrument. The marker input is a TTL pulse that arrives at pin 10 of U17. Pin 10 is the 4-bit input and will produce a one-quarter division deflection on the CRT display. The signals to produce the deflection for both the cursor pip and the marker are completely independent of the gain setting of U11 (dB/DIV). Since the marker input is an external connection, it is isolated by a 1K resistor (R79) and clamped to +5V and ground with two diodes (CR1 and CR2) so that the voltage feeding U17 cannot exceed normal TTL levels.

If the next switch below the top switch of U8A is selected by the CPU through U18, this connects U15A to the U2 input. U15A is fed from the memory (A or B channel), and the contents of the memory will be displayed directly on the CRT. If the third switch down is selected, the memory signal is inverted by U15B and displayed. This inverted memory signal would be the minus memory (as used in the Input-Memory function), and is comprised of the data that would be subtracted from the input signal. If the fourth switch down (top switch of U9A) is selected by the CPU, it will connect U16B to U2. U16B is a stage of amplification and has either unity gain or times 10 gain, selected by S1A. S1 is a small rotary switch accessible through the top,

rear, of the N10 housing by removing the N10 from the Mainframe. S1A makes it possible to select either 10 mV or 100 mV per dB of gain depending on the signal applied to the external Aux 3 connection. The Aux 3 connection is used to receive the output signal from a Model 1018B Peak Power Meter. The signal is fed in through an isolator, U16A, to swap grounds.

The next switch down is connected to U16C. The signal input to U16C is an external ratio signal, applied either through a rear panel BNC connection or as a voltage supplied through the GPIB interface on the Mainframe (for A/X or B/X display). The next lower switch, connected to U16D, is fed from the opposite channel for ratioing with information contained in the opposite channel. This makes it possible to produce an A/B or B/A display. If this were the only switch of the array that were closed, the opposite channel would be inverted and displayed as such. The inverted display would show what is to be subtracted from the input signal to provide a ratioed display.

The U8B switch is fed from U14B (ground isolator) which, in turn, receives the signal from the Log Reference input. Log R comes from the center or reference channel and, when the switch is closed, the signal being sensed by the reference detector will be displayed.

If more than one of the switches in the U8A, U9A, and U8B switch array are closed, a ratio will be produced. Since all of the signals are in dB (logarithmic), the ratio is supplied by simple subtraction. For example, if the top switch which connects the signal from the detector to the display were closed along with the bottom switch that allows viewing of the signal from the opposite channel, the two signals would be combined. This would cause the display of A over B (or B/A in case of the opposite channel). If all of the switches are left open, it is possible to display only the balanced condition of the operational amplifiers of the CRT Display board. This makes it possible to adjust the input zero pot., and other balance pots on the board.

5.3.8.2 Address Controls

U7, in conjunction with U13A, is used to properly decode the address lines that enable either U6 or U18 so that U6 or U18 can be loaded by the CPU. U6 and U18 are enabled by either the zero or the 1 output of U7. U13A is an exclusive or-gate, one input of which is connected to an external line called Select A. Since both A and B channel CRT Display boards are identical, when the PC board is to be used for channel A (plugged into the A9 receptacle position in the N10 Unit), the Select A pin is left open (ungrounded). When the board is plugged into the A10 receptacle, Select A is grounded. In this way, the open or grounded state of the Select A line will tell the board whether it is processing A or B channel information. An open condition (channel A) will make the line high (pulled up by R8 connected to +5V) which causes U13A to invert the signal from the A5 line of the address bus. The inverted A5 address signal is then applied to the not-enable 1 line of U7. If the Select A line is grounded (B channel), this will cause a zero to appear at pin 2 of U13A so that the exclusive or-gate will not invert the signal on pin 1. Therefore, there will be an opposite address condition for the B channel. Whether the board is to function as A channel or B channel is thus determined by the normal or inverted condition of address line A5.

5.3.8.3 Test Point Indications and Usage

TP1 – Ratio Output. This TP looks at the output of the ground isolator state that sends the ratioed signal out to the cursor display and sends ratio information to the opposite channel. Data from this TP location is also sent to the GPIB when the current signal condition for each channel is requested.

TP 2 – Looks at the output of U2. U2 combines all input signals into a single signal that goes either to the ratio output or to the CRT output.

TP3 – Reference (Ratio) Common Ground

TP4 – Used to calibrate the offset voltage. Switch S1B, placed in a grounded position, will eliminate the input signal from U2, leaving only the offset. The signal at TP4 can then be used to set the DAC offset. The TP4 signal can also be fed to the gain control stage U11.

TP 5 – Looks at the A or B channel plus (+) output to the D14A Mainframe. 50 mV/DIV voltage is supplied to the CRT deflection amplifiers from this point.

TP6 – -15V

TP7 – +15V

TP8 – 15V Common Ground

TP9 – 5V

TP10 – +5V

5.3.9 *CPU Board* (SD 14964 Bd #A11)

The CPU (Central Processing Unit) Board (assy. #14963) controls all of the functions of the N10 unit. Using SD 14964 as a guide, the CPU circuitry can be broken into four sections. The clock and CPU itself can be seen in the center of the SD. At the top of the SD are shown the RAMs, and at the bottom are the EPROMs. At the right and left edges of the SD are shown the I/O interface components.

(Figure 5-11, Block Diagram, on page 5-20 can also be used as an aid to better understand the following discussion.)

5.3.9.1 Clock and CPU Controls

The 16 MHz crystal clock (U4) divides down to provide a 2 MHz clock for the CPU and a 500 kHz clock that is used by other PC boards. Binary counter U9 and U5, respectively, are the dividers for the 2 MHz and 500 kHz clocks. The output of U9 is fed to a transistor circuit (Q1, Q2, and peripheral components) to produce the necessary clock waveform for the CPU, U16. Transistor Q3 and its peripheral components comprise the power-on reset circuit. When power is first applied to the N10 unit, pin 26 of U16 (Not-Reset) is held low, keeping the CPU in a reset condition for the approximate one second that it takes the 5V power supply to stabilize. During this one second, the power-on circuit holds everything in a static condition. As soon as the reset circuit lets go, the CPU begins executing instructions at address zero. Address zero is decoded from the address lines by U2 and U8. U2 is a decoder that only feeds one of the I/O chips, and U8 decodes all else. At address zero, the zero comes from the U8 decoder and is used as an enable for EPROM U3. U3 is the low address EPROM and U12 is the high address EPROM. U3 occupies addresses from 0 to 7FF. U12 occupies addresses from

1000 to 17FF and is also decoded by U8. U8 outputs 0, 1, 2, 3, and 4 are active low lines and will pull down on individual chip select lines to accomplish the enabling of desired functions. The CPU, starting at zero and reading instructions from the U3 EPROM, will begin executing the instructions at address zero. After it starts executing, the entire CPU becomes controlled from the program in U3 and U12.

5.3.9.2 Random Access Memory (RAM) Functions

The RAM block (1K x 4 bits per RAM) consists of U1 and U7. These are chip selected by U8 at address group 2000 hex. Since they are chip selected at the same address, they will work together. U1 is the memory for the low nibble and U6 is the memory for the high nibble. The data lines for U1 and U7 are connected directly to the data bus for the rest of the instrument. The bus has a set of switches which allow the data bus from the CPU to be disconnected from the rest of the N10 unit. In opening the switches, a specific code is generated which will force the CPU to strobe all of its addresses. The purpose of this is to make it possible to use troubleshooting methods that utilize signature analysis equipment. All of the temporary storage (scratch pad memory) used by the CPU is contained in U1 and U7. This is only a small portion of the N10 unit's total memory capacity, and is used only by the CPU.

5.3.9.3 Input/Output (I/O) Functions

There are three separate ways for signals to enter and leave the CPU board. Referring to the right side of SD 14964, there are two sets of bi-directional buffers (U14 and U17), and one set of uni-directional buffers (U10). The reason that a uni-directional buffer can be used is because it interfaces only address lines. The CPU generates all of the addresses used by the PC boards in the N10 unit, and individual interfaces on the other PC boards will be addressed and enabled under the control of the CPU.

Referring to the left side of SD 14964, there are two additional chips used to interface the I/O signals with the CPU. Chip U11 is called a PIO (Peripheral Input/Output) and is a data line buffer for the CPU to allow data to be sent or received to or from peripheral equipment. This device has 16 data lines split into two 8-bit ports (A and B). The A port (four lines) is used to control the PMIB (Pacific Measurements Interface Bus). This bus interfaces, through the 1038-D14A Mainframe, the GPIB interface board and the N10 plug-in unit. The four lines of the A port form a handshaking, bit-serial interface. All data to and from the CPU board is sent in the bit-serial format (one bit at a time). All eight lines of port B are used for I/O functions as indicated on SD 14964. Some of these lines are inputs and some are outputs, but all of them are fully controllable by the CPU and also allow peripheral equipment to interrupt the CPU operation to cause the CPU to start a new function. One example of this interrupt function, applied to bit 0 of port B, is the Keyboard Interrupt. If the operator presses a front panel key, the line will pulse and cause the CPU to stop whatever function it is performing at the moment and go into an interrupt service routine. The CPU is vectored to the correct service routine and, in this case, will go out to the keypad, sense what data was entered, and store that data. The CPU will then go back to whatever operation it was performing before it was interrupted. This process is accomplished at a hardware level, therefore it is very rapid.

U11 is enabled by its chip select line. Decoding is done by address lines from the CPU through U2. U2 uses its zero decode line to select U11 as the I/O port, address 0 through 31, as selected here.

The other I/O port is PPI (Parallel Peripheral Interface) U15. U15 has three ports (eight lines per port), but only a portion of these are used. U15 is addressed as a portion of memory (similar to addressing a RAM) rather than as an I/O port. The address is decoded by U8. It is in the 4000 hex group that chip selects U15. U15 has four registers. These are the I/O registers for the A, B, and C ports, and the control register. The four ports are selected by address lines A1 and A0 of U15 on pins 8 and 9. These address lines are separate, distinct, and should be distinguished from the A port lines of pins 3 and 4. Pins 3 and 4 are peripheral I/O lines as opposed to address lines. The two least significant address bits control which of U15's four registers are actually being controlled. The C port of U15 has two outputs (C1 and C2) that control a transistor array. This array interfaces with two output lines labeled Not-Display A and Not-Display B. Both lines are active low, and are connected to the D14A Mainframe mother board. Through these lines, the CPU has control over what is being presented on the D14A CRT display.

Switch S1 (above U15 on the SD) is a rotary, screwdriver-adjustable, 16 position switch. The switch is physically labeled for positions 0 – 9, A – F, and is used for selection of specific operating characteristics of the N10. Only four of the positions are currently used for selection of Auto Zero and V ∝ F functions as defined in Section 3.2 of this manual. The switch is connected to the A port of U15 which determines what function is being requested by the operator. S1 can only be adjusted when the N10 unit is removed from the D14A Mainframe, as discussed in Section 3.2

5.3.9.4 Test Point Indications

TP1 – Not-Interrupt Line of U11. Allows monitoring of whatever condition has caused the CPU to stop its normal routine and go into an interrupt service routine. There are a number of functions that can cause an interrupt, so this TP is useful when troubleshooting. Checking at this point can assist in locating a malfunctioning component.

TP2 – +5V

TP3 – 5V Common

TP4 – Clock drive to the U16 CPU. It is a 2 MHz symmetrical square wave at +5V amplitude.

5.3.10 *N10 Interconnect Board* (SD 15006 Bd #A12)

The N10 Interconnect Board (Assembly # 15005) is the PC board that interconnects all of the signals traveling between the various functional circuit boards. Boards A1 through A11 plug into the Interconnect Board. Besides routing signals between the functional circuit boards, the Interconnect Board also provides the interface to the finger boards which, in turn, interface with the D14A Mainframe unit.

5.3.11 *Front Panel Assembly* (Bd # A13 - SD 15003

The Front Panel (Assembly #14968) contains all of the push button and LED readout controls and displays that allow the operator to interface with the N10 unit. The buttons that control the operation of the N10 are connected as

three groups. Each group is connected through an individual 16 key encoder. The three groups consist of: (1) the select buttons (Ch. A, Ch. B, Enter, Clear, Auto Zero, Int. Sweep, and Cal), encoded by U17; (2) the jog button group (Offset, dB/DIV, and Cursor), encoded by U13; and (3) the numeric group (0 through 9, minus sign, and decimal point), encoded by U14. The numeric buttons are actually double function keys because they activate specific functions as well as numbers. This is controlled by timing within the software program.

The 4 bit outputs of each encoder are all connected in parallel and supplied to the Display Driver board. From the Driver board, information is fed to an interface chip where it is read by the CPU. A data available line is also supplied from each encoder. All three encoders (U17, U13, and U14) operate similarly, so just U17 will be discussed here.

If one of the channel select or other buttons associated with U17 are pressed, U17 will encode from its X and Y input, and also raise the data available line on pin 12. The data available appears as the DA1 line to the keypad data, and is sent to the Digital Display Driver board. As soon as the DA1 line is raised, the information from the Driver board will pull the Not-Enable 1 line low. This will connect the tri-state output lines (A, B, C, and D) at the U17 encoder. This means that the A, B, C, and D outputs will appear at the Driver board and be available to be read by the CPU. Also available to the CPU is the fact that it was group one of the switches (group two is encoded by U13 and U14 encodes group three) which was encoded on the ABCD lines, and the CPU can determine which individual button is being pressed. This entire section (U17, U13, and U14) of the Front Panel is separate and distinct from all of the display functions.

All of the display readouts and indicators are LEDs. They are operated as seven-segment displays with all of the segment lines tied in parallel. Individual common lines are brought out so that it is possible to strobe (individually energize) each of the digits and produce a multiplexed display with a single seven-segment encoder. The individual LEDs that indicate the various input modes (dB, dBm, Input, Input-Memory, Ref Ratio, Channel Ratio, Memory, and Mem 1&2) are treated exactly like seven-segment displays. Each occupies a position on the segment encoder as if each were one segment of a seven-segment LED. In this way it is possible to use any single encoder to light any single digit or individual LED on the front panel.

All of the front panel LEDs are continually strobed at a frequency of 100 Hz. This means that, about every 10 msec, all of the lights will be cycled through and pulsed once (multiplexed) and another cycle started. All of the multiplexing is handled by the Digital Display Driver board, physically located next to the Front Panel.

The individual LEDs for the input mode indicators are returned to a common panel called A Common or B Common, depending on which channel the LED is associated with. Certain other functions (V ∝ F, Int Sweep, Remote, and Cal) are returned to a separate point called Miscellaneous Common, and each of these will be strobed separately by the Driver board. Each of the groups (input indicators and miscellaneous indicators) are strobed separately.

The circuitry is designed to make it possible to turn off any group of LEDs or any single LED. This makes is possible to flash that group or single LED. Flashing of LEDs or groups of LEDs will take place any time that action on the part of the operator is pending, to alert the operator that another step is required while performing a command input sequence.

5.3.12 *Horizontal Finger Board* (SD 15034 Bd #A14)

The Horizontal Finger Board (Assembly #15023) provides an interface between the Interconnect Board and the horizontal drive stage of the D14A Mainframe unit. Other signals, as shown on SD 15034, also are interfaced through this board.

5.3.13 *A Channel Finger Board* (SD 15034 Bd #A15)

The A Channel Finger Board (Assembly #15064) interfaces the signals from the A and B channels of the N10 unit to the D14A Mainframe unit. Other signals, as shown on SD 15034, are also interfaced between the N10 and the D14A through this board.

SECTION 6. PERFORMANCE VERIFICATION TESTS

6.1 Purpose

Information in this section is useful for periodic evaluation of the performance of the Model 1038-N10 Network Analyzer Plug-In. It can also be used for inspection testing when the instrument is first received. (The N10 Plug-In must be inserted into a Model 1038-D14A Mainframe for it to be able to function.) If the 1038-D14A/N10 system fails to meet one or more of the performance criteria listed here, refer to Section 7 for detailed instructions on making the necessary adjustments. Be sure that the 1038-D14A Mainframe is within proper calibration specifications prior to testing with the 1038-N10 Plug-In unit.

6.2 Equipment Required

Qty.	Description		Ref. Desig.
1	Model 1038-D14A Mainframe		MAINFRAME
1	Standard Swept RF Source	Power Output -10 to +16 dBm Sweep retrace time must be > 5 ms Sweep forward trace time must be > 20 ms	SWP SRC
1	Low Voltage Power Supply	2.5 to 5V @ 1 mA or higher	PWR SUP
1	Attenuator	10 dB to within ±0.02 db accuracy	FIX ATTEN
1	Attenuator	70 dB in accurate (within 0.03 dB) 10 dB steps (to check detectors)	VAR ATTEN
1	Source	30 to 50 MHz with an output of 10 mW ±0.5% and a source VSWR better than 1.07. Harmonics at -50 dBc or better.	PWR SRC

6.3 Test Procedures

(Prior to performing the Verification Tests, connect detectors to both A and B channels. Connect SWP SRC to drive the horizontal input – Aux 1 on the rear of the MAINFRAME. Be sure CALIBRATOR (on the front panel of the N10 unit) is always OFF when it is not actually in use.)

6.3.1 Auto Zero

A. Turn ON both channels
   1. Press CH A → CH B → ENTER

B. Apply zero input to both channels (RF = < -70 dBm)

C. Press CH A, AUTO ZERO
   1. Verify that only channel A is auto zeroing. (Cursor display varying)
   2. Wait for end of auto zero cycle (approximately 8 seconds)

D. Press CH B, AUTO ZERO
   1. Verify that only channel B is auto zeroing
   2. Wait for the end of the auto zero cycle

6.3.2 Power Tracking

A. Set the SWP SRC for at least 0.5 seconds
   1. Be sure retrace time is greater than 50 msec
   2. Press CH A → SF1 → 0 → 5 → ENTER
   3. Be sure that the CALIBRATOR light is OFF
   4. Activate SMOOTHING for Channels A & B by pressing CH A → SMOOTHING → ENTER and then CH B → SMOOTHING → ENTER

B. Check tracking of both channels from +10 to -60 dBm
   1. Connect channel A detector to the PWR SRC through the VAR ATTEN
   2. Set the VAR ATTEN to 10 dB (0 dBm output)
   3. Press CH A → INPUT → ENTER
   4. Adjust channel A CAL for exactly 0 dBm (00.0 on Cursor LED)
   5. Set the power level at each 10 dB level from +10 dBm to -50 dBm for a single diode detector, or -60 dBm for dual diode detectors
   6. Verify that the error is less than the maximum spec value as shown in Figure 1-1 of Section 1.2 of this manual
   7. Repeat 1 through 6 above using channel B (in Step 4, Cursor LED is set to 00.0)

The reference channel performance can be evaluated and verified as follows:

   8. Connect the detector to the Reference channel input
   9. Press CH B → REF RATIO → ENTER
   10. Set the VAR ATTEN to 10 dB (0 dBm output)
   11. Connect the detector input to the VAR ATTEN
   12. Note the reading on the channel B cursor display
   13. Set the power level to each 10 dB level from +10 to -30 dBm and subtract the reading noted in Step 12. Verify that the indicated power is within ±0.2 dB from +5 to -30 dBm and within ±0.4 dB at +10 dBm. *(Note: The polarity displayed will be reversed during this test.)*

6.3.3 Self Test

A. Press CH A → INPUT → CH B → INPUT → ENTER

B. Press CH A → SF1 → 2 → ENTER

C. Verify that both displays are reading between +3 and +9 dBm

D. Press CH A → REF RATIO → ENTER

E. Verify that channel A, which is now displaying the Reference channel with the sign reversed, indicates -4.5 to -7.5 dB

F. Press CH A → SF1 → 3 → ENTER to exit the self test mode

6.3.4 Calibrator

A. Connect the detector from channel B to the PWR SRC through the FIX ATTEN

B. Adjust channel B CAL for 0.00 dB (be sure the CALIBRATOR light is OFF)

C. Connect the detector to the CALIBRATOR and turn on the CALIBRATOR by pressing the button next to the CALIBRATOR

D. Channel B should indicate 0 dBm ±0.06 dB plus error limit of PWR SRC & FIX ATTEN

E. Disconnect the detector and turn OFF the CALIBRATOR

6.3.5 Cursor Check

A. Press CH B → SF1 → 0 → 1 → ENTER and verify that the cursor is one major division from the left end of the graticule ±1 minor division

B. Press CH B → SF1 → 0 → 5 → ENTER and verify that the cursor is at the center of the graticule ±1 minor division

C. Press CH B → SF1 → 0 → 9 → ENTER and verify that the cursor is 1 major division from the right side of the graticule ±1 minor division

6.3.6 Peak Power Input

A. Connect the HORIZONTAL OUT BNC to the Aux 3 input BNC connector on the rear of the MAINFRAME

B. Press CH B → PEAK POWER → ENTER

C. This should produce a ±50 dB or ±5 dB ramp on the display, depending on the setting of switch A10S1 on the channel B CRT Display board (A10) (See Section 3.2 of this manual)

6.3.7 Memory Functions

A. Press CH B → ACCESS MEM → ENTER

B. Note that after one full sweep, the "Input-Memory" and "Peak Power" lights are on, and the display is a straight line on the center line of the CRT graticule

C. Connect the channel B detector to the SWP SRC

D. Press CH B → INPUT → ENTER

E. To make this measurement, a variation of 2 to 6 dB is required. It may be necessary to connect a device in the line that will give the desired pattern

F. Press CH B → ACCESS MEM → ENTER and wait for the "Input-Memory" light to come on.

G. Press CH B → SF1 → 1 → 0 → ENTER and note that the channel B sensitivity is 0.05 dB/DIV

H. The display should be a straight line at the center line of the CRT. The resolution of the memory should be about 0.01 dB

I. Repeat from C, above, using channel A. Note the resolution is about 0.04 dB. (It will be necessary to press ENTER twice at Step F to complete the memorization for channel A.)

6.3.8 Marker Input

A. Press CH A → SF1 → 1 → 7 → ENTER

B. Apply +2.5V to 5V to Aux 4 at the rear of the MAINFRAME and note that the trace moves down ¼ division

SECTION 7 MAINTENANCE

7.1 Introduction

This section of the manual defines maintenance practices and troubleshooting procedures required for fault isolation down to, in most cases, PC board level.

It should be remembered that problems can occur that might be produced by equipment or components peripheral to the N10 unit. Preliminary checks should be made to be sure that external equipment or components are not causing what appears to be a malfunction within the N10 unit. Section 6 of the Model 1038-D14A Mainframe Instruction Manual will give checks that can assist in locating any problems within the Mainframe housing of the N10 Plug-In.

7.2 Periodic Maintenance

The following maintenance procedures should be performed once each year unless the Plug-In is operated in an extremely dirty or chemically contaminated environment, or is subjected to severe abuse (such as being dropped). In such cases, more frequent maintenance (immediate, if the Plug-In is dropped or severely abused in some way) is required.

A. Blow out all accumulated dust and dirt with forced air under moderate pressure.

B. Inspect the Plug-In for any loose wires or damaged components. Check to see that the Plug-In PC boards are properly seated in their receptacles, and that all wire lead connectors are properly attached to their PC board pins.

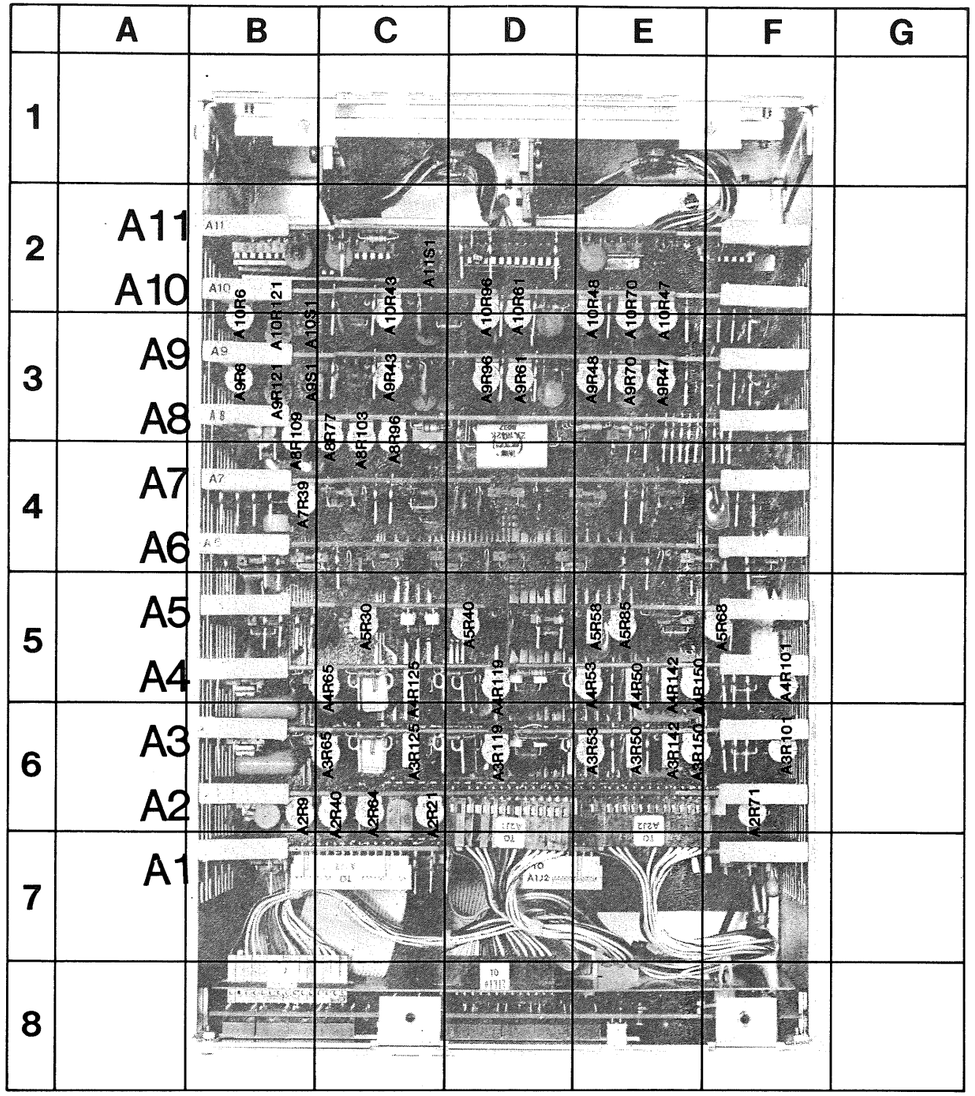
C. Using a cloth dampened in a mild detergent solution, clean the front panel of the N10. Do not use abrasive cleaners, scouring powders, or harsh chemicals. Wipe the soap residue off with a clean damp cloth, then dry with a clean dry cloth.

D. Make a performance verification check in accordance with the procedures found in Section 6 of this manual. If the performance is within the required specifications, no further service is required.

7.3 Calibration

Using all solid state components, the Model 1038-N10 unit is extremely rugged and reliable. Consequently, there is very little drift due to component aging, and adjustments to the Plug-In are rarely required. If measurements indicate that an adjustment is set within the stated range, do not attempt to put it "right on". It is often the case that variations in the equipment used to make the test account for small differences in measured values. Since some adjustments can be interactive, *BE ABSOLUTELY SURE THAT AN ADJUSTMENT IS REALLY REQUIRED BEFORE MAKING IT.*

Figure 7-1 Location of N10 Calibration Components



CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
A2R9	B-6	A3R125	C-6	A4R65	C-5	A4R101	F-5	A7R39	B-4	A9R6	B-3	A9R70	E-3	A10R96	D-2
A2R40	C-6	A3R119	D-6	A4R125	C-5					A9R121	B-3	A9R47	E-3	A10R61	D-2
A2R64	C-6	A3R53	E-6	A4R119	D-5	A5R30	C-5	A8R109	B-4	A9S1	B-3			A10R48	E-2
A2R21	C-6	A3R50	E-6	A4R53	E-5	A5R40	D-5	A8R77	C-4	A9R43	C-3	A10R6	B-2	A10R70	E-2
A2R71	F-6	A3R142	E-6	A4R50	E-5	A5R58	E-5	A8R103	C-4	A9R96	D-3	A10R121	B-2	A10R47	E-2
		A3R150	F-6	A4R142	E-5	A5R85	E-5	A8R96	C-4	A9R61	D-3	A10S1	B-3		
A3R65	C-6	A3R101	F-6	A4R150	E-5	A5R68	F-5			A9R48	E-3	A10R43	C-2	A11S1	C-2

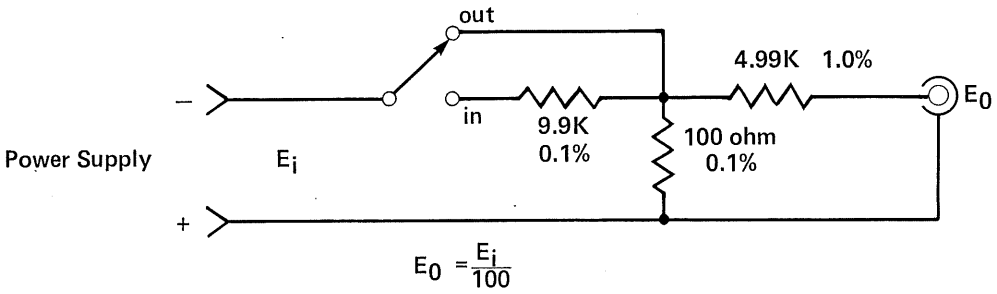
7.3.1 Test Equipment Required

(All test equipment must be within calibration limits as specified in the instruction manual or calibration procedures pertaining to the particular equipment.)

Qty.	Description		Ref. Desig.
1	Model 1038-D14A Mainframe.	(calibrated)	MAINFRAME
1	Digital Voltmeter	0.01% accuracy 5½ digits.	DVM
1	Oscilloscope (Dual Channel)	1 mV and 1 MHz. Must have calibrated offset capability.	SCOPE
1	Frequency Counter	to 50 MHz	FREQ CNTR
1	Power Source	10mW @ 30 to 50 MHz	PWR SRC
1	Sweep Source	40 ms to 1 sec. Retrace time > 10 ms. Amplitude adjustable from 5 to 20V p-p	SWP SRC
1	Precision Power Supply	10 mV to 10V Digitec Model 3110 or equivalent	PWR SUP
1	Detector Calibration Cable	Pacific Measurements P/N 15636	CAL CBL
1	Detector Simulator – DC Source	Pacific Measurements P/N 15484	DET DC

or

use the PWR SUP with the following divider box and 15238 Detector Cable



Then use the following table of values to match the applied voltage with the equivalent RF level:

RF Level (dB)	mV	
+10	.844	
0	.228	
-10	.48.6	
-20	.6.66	(Use divider box from this
-27	.1.40	point on down. The divider
-30	.0.70	box input would be 100 times
-40	.0.07	the numbers shown.)

7.3.1.1 N10 Preset Conditions

To establish the correct instrument parameters for performing the calibration routines, the following conditions must be preset on the N10 and D14A units:

A. Display A channel only

B. Set A channel OFFSET to 0 dB

C. Set A channel REF LINE to CL

D. Set A channel dB/DIV to 10

E. Switch CALIBRATOR to OFF

F. Connect external 100 ms sweep ramp to Aux 1 (at the rear of the MAINFRAME) and be sure INT SWEEP on the N10 unit is OFF.

G. Connect the D14 Horizontal Output to Aux 3 (at the rear of the MAINFRAME)

7.3.2 Procedures

(Prior to performing the calibration of the N10 Plug-In, the user should be sure that the D14A Mainframe has been calibrated per the instructions given in paragraph 6.2 of the D14A Operating and Maintenance Manual.)

(Figure 7-1 is provided as a fold-out sheet that can be used to locate the various components required for adjusting purposes during the calibration routines. Figure 7-1 is located on page 7-2.) Seven calibration routines will be described in this section. These routines should be performed whenever the instrument is due for routine calibration or when it is felt that calibration is required. Section 7.4, Troubleshooting, will also specify the performance of one or more of the calibration routines when a malfunctioning PC board is tested.

All of the tests require that the N10 be removed from the D14A Mainframe (attached through the extender cables) if a standard vertical D14 is being used for calibration. The rack mount (option 1) horizontal configuration of the D14A will allow the N10 to be bench calibrated by removing the right hand top cover. All test points and adjustments are labeled and are accessible at the top of the PC boards. It

is not necessary to remove any individual boards from the unit for these calibration procedures.

7.3.2.1 10V Reference Supply Calibration

A. On Bd #A7 (B Channel Memory), locate A7TP4 (+), A7TP2 (Com.,) and A7R39 (10V ADJ)

B. Attach DVM across the TPs, observing polarity

C. Adjust R39 for 10.00V ±1 mV

D. Disconnect the DVM

7.3.2.2 Horizontal Board (A8) Calibration

A. Connect SCOPE vertical to A8 TP4, SCOPE trigger to A8TP12 (negative slope), and SCOPE common to A8TP1

B. Monitor SWP SRC at Aux 1 (at rear of MAINFRAME), and set SWP SRC for 5V p-p output at 10 sweep/sec

C. Switch A8S2 is not numerically labeled. For the purposes of this procedure, assign numbers to the switch positions as shown in Figure 7-2 below.

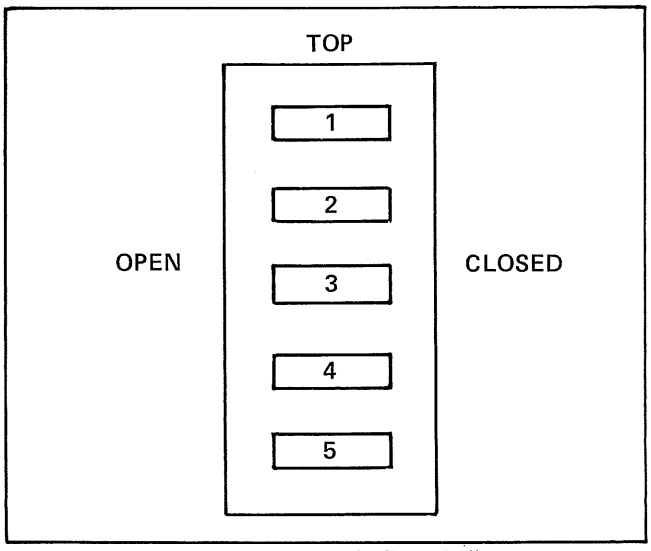


Figure 7-2 Switch A8S2 Labeling

Set S2 as follows:
S2-1: Open
S2-2: Closed
S2-3: Open
S2-4: Closed
S2-5: Closed

D. Adjust A8R77 (A BAL) for a reading of 0V ±20 mV at TP4

E. Open S2-2 and close S2-3

F. Adjust A8R103 (B BAL) for a reading of 0V ±20 mV at TP4

G. Open S2-3 and make a note of the voltage

H. Open S2-5 and adjust A8R96 (CUR BAL) to cause a reading equal to the reading obtained in G above

I. Open S2-4 and close S2-1

J. Note the voltage at the minus (-) peak while changing the input sweep amplitude from 5 to 20V. Adjust A8R96 (CUR BAL) slightly to maintain a constant 0V ±20 mV.

K. Using the calibrated offset feature of the SCOPE, set the plus (+) peak of the displayed trace at 10V ±25 mV using A8R109 (10V RAMP)

L. Verify that the sweep amplitude remains constant when the input sweep amplitude is varied from 5 to 20 V

7.3.2.3 A/B Channel CRT Display Board Calibration

(Calibration of both the A and B channel CRT display boards is exactly the same. The A channel is board #A9 and the B channel is board #A10, therefore references to component designations such as A9S1 would become A10S1 when calibrating the B channel board.)

Note:

All voltages are measured using A9/A10TP3 as common.

A. Set A9S1 to position 1

B. Set the N10 A channel OFFSET to 0.0 dB
   1. Adjust A9R47 (OFFSET ZERO) for 0V ±1 mV at A9TP4

C. Set N10 A channel OFFSET to +40 dB
   1. Adjust A9R48 (OFFSET CAL) for -4.00V ±1 mV at A9TP4

D. Set N10 A channel OFFSET to -60 dB
   1. If the voltage at A9TP4 is more than 4 mV on either side of 6.00V, the linearity of U6 may be bad and should be replaced.
   2. Repeat B, C, and D as required to get as close to -4.00V, 0V, and +6.00V as possible.
   3. Set N10 A channel OFFSET to 0 dB

E. Set A9S1 to 0 and key the following sequence into the N10 through the keypad: CH A → SF1 → 8 → ENTER
   1. Adjust A9R96 (INPUT ZERO) for 0V ±1 mV at A9TP2
   2. Adjust A9R61 (RATIO ZERO) for 0V ±1 mV at A9TP1
   3. Adjust A9R70 (OUTPUT ZERO) for 0V ±0.5 mV at A9TP5

F. Set A9S1 to position F (then move to bd #A2 for the following)
   1. Adjust A2R9 (A OFFSET TRIM) for 0.0 on the A channel LED power display
   2. Set A channel OFFSET to +40 dB
   3. Adjust A2R21 (A GAIN ADJ) for 40.0 dB on the A channel LED power display
   4. Set the A channel OFFSET to 0 and (moving back to bd #A9) set A9S1 to position 0

G. Key the following sequence into the N10 through the keypad:
   CH A → SF1 → 8 → ENTER → CH A → 3 → ENTER → ENTER (second ENTER only req'd on channel A)
   (Wait until end of memorizing, then continue)
   CH A → 5 → ENTER

H. Set SWP SRC to 10 seconds
   1. Adjust A9R43 (MEM ZERO) for 0V ±1 mV reading at A9TP1

I. Key the following sequence into the N10 through the keypad:
   CH A → SF1 → 8 → 8 → ENTER
   1. Adjust A9R6 (-MEM ZERO) for 0V ±1 mV reading at A9TP1
   2. Set SWP SRC to approximately 200 msec

J. Key the following sequence into the N10:

CH A → SF1 → 8 → 6 → ENTER → CH A → 3 → ENTER → ENTER

1 Adjust A9R21 (MEM GAIN) so that the CRT display has no slope. Increase channel A sensitivity to 0.1 dB/DIV for final adjustment.

K. Turn OFF channel A and turn ON channel B

L. Repeat the above procedure from Step A through Step K using channel B (Bd #A10). Remember to substitute "B" for "A" channel wherever mentioned in the procedure, and to use the B channel controls. In Step F, A2R40 is the "B OFFSET TRIM" pot and A2R64 is the "B ADJ GAIN" pot.

7.3.2.4 A/B Channel Input Preamplifier and Log Circuit Board Calibration

(Refer to Figure 7-3 on page 7-6 for test set-up.)

(Calibration of both the A and B channel Input boards is exactly the same. The A channel is board #A3 and the B channel is board #A4, therefore references to component designations such as A3TP9 would become A4TP9 when calibrating the B channel board.)

Note:

All voltage readings will change during retrace.

A. Turn ON channel A, turn OFF channel B. Set sweep to external and adjust for 2 to 10 second sweep speed. Preset channel A as follows:

OFFSET = 0
REF LINE = CL
CURSOR to center screen
SMOOTHING is OFF
INPUT mode

B. This procedure is written assuming the use of the DET DC. If the alternate (PWR SUP) method is used, refer to the equivalent input versus voltage chart shown in Section 7.3.1.

C. Connect the DET DC output to the channel A input through the CAL CBL

1. Set the DET DC to DUAL and OFF

D. Turn OFF channel A. Connect the DVM to A3TP9 (connect DVM LO to A3TP8, which is the common for this board) and set the DVM for the 10V range.

E. Adjust A3R190 (PREAMP BAL) for zero volts ±25 mV. Turn ON channel A.

F. Connect the DVM to A3TP2

G. Set the DET DC to OFF

1. Press AUTO ZERO and wait approximately 6 seconds for the AUTO ZERO light to go off.
2. The DVM should indicate -6 to -8V

H. Connect the SCOPE to A3TP5 and set the detector input to -30 dBm. Adjust the SCOPE for 100 mV/DIV vertical and 5 ms/DIV horizontal, using line sync.

Note

If you are using a substitution d.c. source for the DET D.C., a DUAL mode is not possible. Therefore, the input level should be set to -27 dBm for making the HI level and LO level REF adjustments.

1. Adjust A3R125 (HI LEVEL REF) so that the average voltage of the SCOPE is about zero volts.
2. Connect the SCOPE to A3TP4. Adjust A3R50 (LO LEVEL REF) so that the average voltage on the SCOPE is about zero.
3. Disconnect the SCOPE

I Set the DET DC to -30 dBm

1. Adjust A3R65 (CAL CENTER) for -3.000V ±1 mV on the DVM

J. Set the DET DC to -40 dBm

1. Adjust A3R53 (LO LEVEL LOG CAL) for -4.000V ±3 mV on the DVM
2. Repeat from H as required
3. Check with DET DC OFF for a reading of about -6 to -8V. If not, press AUTO ZERO, wait for the light to go out, and repeat from H.

WARNING: In Step K below, small, well-insulated clip leads must be used and great care taken that either TP is not shorted to an adjacent TP when the connection is made. Possible destruction of an IC (usually A3U14) can result if a short is accidentally introduced.

K. Connect A3TP13 to A3TP8. Press AUTO ZERO and wait for the light to turn off

L. Set the DET DC to 72 mV

1. Adjust A3R65 (CAL CENTER) for -1.000V ±1 mV on the DVM

M. Set the DET DC to 720 mV

1. Adjust A3R119 (HI LEVEL LOG CAL) for OV ±1 mV. Repeat K and L as required.

N. Set the DET DC to 7.2 mV

1. If the output is not -2.000V ±3 mV, repeat from Step J.
2. Disconnect A3TP13 from A3TP8 and continue

O. Set the DET DC to -30 dBm and DUAL

1. Adjust A3R65 (CAL CENTER) for -3.000V ±1 mV on the DVM

P. Set the DET DC to 0 dBm

1. Adjust A3R142 (0 dBm COMP) for 0V ±1 mV on the DVM

Q. Set the DET DC to -10 dBm

1. Adjust A3R150 (-10 dBm COMP) for 1.000V ±1 mV on the DVM

R. 1. Adjust A3R142 (0 dBm COMP) for 0V ±1 mV on the DVM.
2. Repeat from Step Q as required.

S. Check tracking from +10 to -40 dBm in 10 dB steps

1. All readings should be within ±0.1 dB of the applied power (±10 mV)

T. Set the DET DC to +16 dBm

1. The DVM should indicate +1.600V ±20 mV

U. On the N10 keypad, press CH A → SF1 → 2 → ENTER to activate the self-test function.

1. The DVM should indicate +0.6V ±0.07V
2. Press CH A → SF1 → 3 → ENTER to turn off the self-test

V. Turn OFF channel A, turn ON channel B, and repeat the procedure for channel B from Step C.

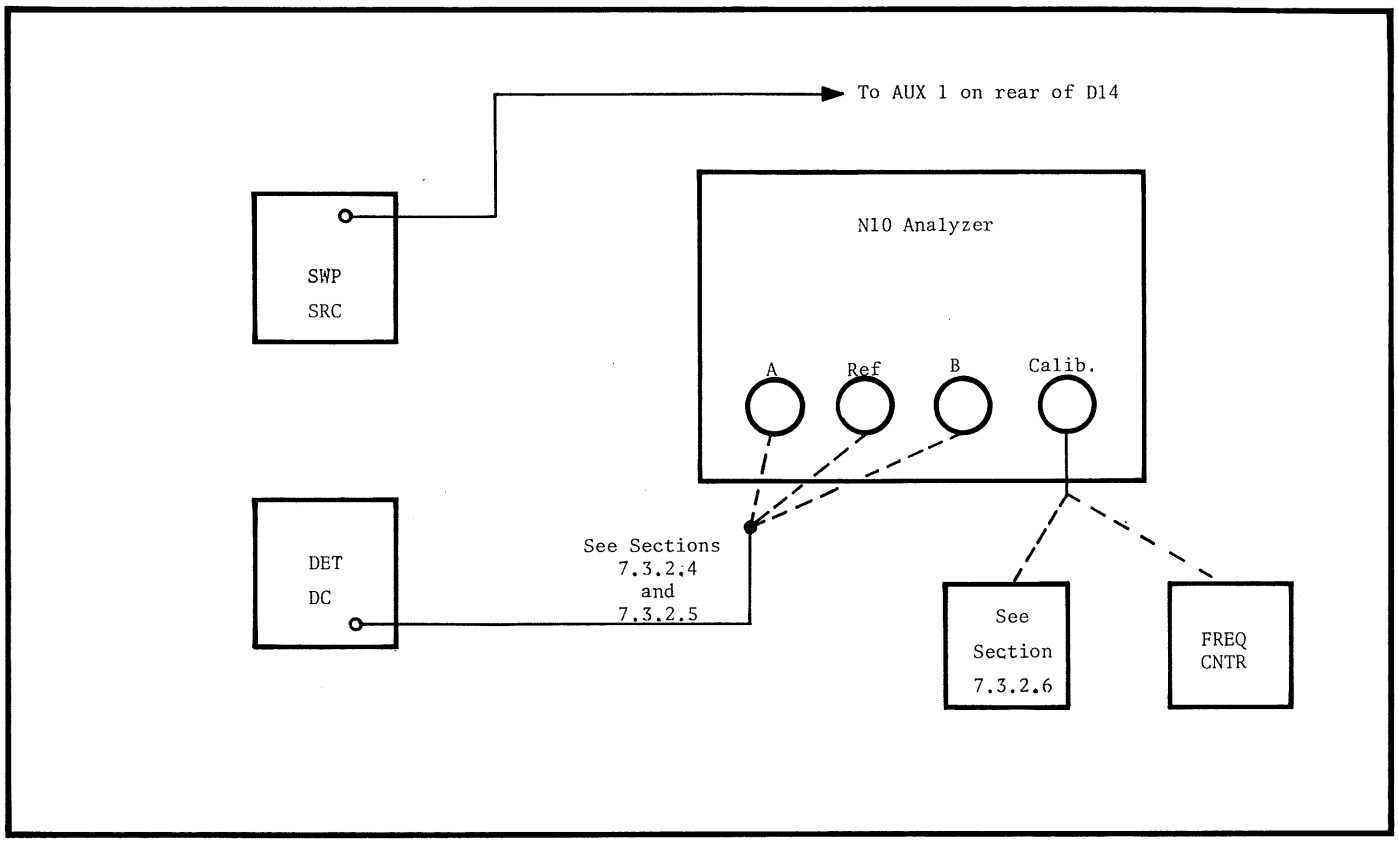


Figure 7-3 Calibration Test Set-Up

7.3.2.5 Reference Channel Calibration (Bd #A5)

(Refer to Figure 7-3 on page 7-6 for Test Set-Up.)

A. Connect DET DC to the reference channel using the CAL CBL. Set the N10 as though B channel were to be calibrated, except that the reference channel will be displayed by keying the following into the keypad: CH B → 9 → ENTER

B. A5TP5 will be the common point for all measurements in this section. Connect A5TP7 to A5TP5 and connect the DVM to A5TP3.

1. Set DET DC to -72 mV input to the reference channel
2. Adjust A5R30 (CAL CENTER) for -1.000V ±1 mV reading
3. Set DET DC to -720 mV input to the reference channel
4. Adjust A5R40 (HI LEVEL LOG CAL) for 0V ±1 mV reading
5. Repeat from Step 1 as required
6. Remove connection from A5TP5 to A5TP7

C. Set DET DC for -30 dBm into the reference detector input

1. Adjust A5R30 (CAL CENTER) for a -3.000V ±2 mV reading

D. Set DET DC for 0 dBm into the reference detector input

1. Adjust A5R58 (0 dBm COMP) for a 0V ±1 mV reading

E. Set DET DC for -10 dBm into the reference detector input

1. Adjust A5R65 (-10 dBm COMP) for -1.000V ±1 mV

F. Set DET DC for +10 dBm into the reference detector input

1. Note the difference between the DVM reading and +1.000V

G. Set DET DC for 0 dBm into the reference detector input

1. Adjust A5R68 (+10 dBm COMP) so that the DVM indicates about twice the difference noted in F-1 above (e.g., if the voltage at Step F-1 was +1.010, then R68 should be set for a reading of +0.020)
2. Adjust A5R58 (0 dBm COMP) for 0V ±1 mV
3. Repeat from Step E as required

H. Check tracking from +10 to -30 dBm in 10 dB steps

1. All readings should be within ±0.1 dB (±10 mV) of the applied power

I. Set DET DC for +16 dBm into the detector input

1. The DVM should indicate +1.600V ±20 mV

J. Activate the self-test feature by pressing CH B → SF1 → 2 → ENTER

1. The DVM should indicate 0.06V ± 0.15V
2. Turn OFF self-test feature by pressing CH B → SF1 → 3 → ENTER

7.3.2.6 50 MHz Calibrator Calibration (Bd #A2)

(Refer to Figure 7-3 on page 7-6 for Test Set-Up.)

A. Connect FREQ CNTR to the CALIBRATOR output and turn the CALIBRATOR on.

1. The frequency must be within 49 to 51 MHz

Note:

If a reading outside of the 49 to 51 MHz limit is noted, the accuracy of the FREQ CNTR should be verified, as it is highly unusual for this precision setting to slip or drift. It is possible, in an emergency, to change the frequency by removing board #A2 from the N10 housing and physically adjusting the length of the open-wound coil A2L1, but this is not recommended. It is recommended that the PC board (A2) be returned to the factory for repair and recalibration in the highly unusual case that this out-of-limit situation should ever occur.

Note:

To set the CALIBRATOR power output properly requires either of the following sets of equipment:

1. *A 30 to 50 MHz source of 1 mW power. The level should be known to an accuracy of ±0.5%, and the source VSWR should be better than 1.07. The harmonic content should be better than -50 dBc. This source should be interfaced with a detector for the N10 that is known to be good.*

or

2. *A 50 MHz power measuring device such as a thermal convertor, with an error limit better than ±0.5% and a VSWR of <1.07 @ 50 MHz.*

B. Using the 1 mW source, proceed as follows:

1. Connect the detector to the B channel input of the N10 and place channel B into the input mode. Turn ON the internal sweep.
2. Connect the detector to the 1 mW source and turn the N10 CALIBRATOR OFF.
3. Adjust the B channel CAL for a reading of 0.00 dBm on the B channel digital display.
4. Remove the detector from the 1 mW source and connect it to the N10 CALIBRATOR. Turn the CALIBRATOR ON.
5. Adjust A2R71 (OSC ADJ) for a reading of 0.00 ± 0.01 dBm on the B channel digital LED display.
6. Repeat Step 2 to be sure that there has been no drift.

C. Using the power measuring device, proceed as follows:

1. Connect the power measuring device to the N10 CALIBRATOR output and turn the CALIBRATOR ON.
2. Adjust A2R71 (OSC ADJ) for exactly 1 mW ±2 μW.

7.4 Troubleshooting

Information provided in this section should enable a technician to locate a malfunction and determine specifically which PC board is causing the trouble. The Troubleshooting Flow Charts of this section are used to trace a problem to a

specific board. Then, the electrical description and schematic diagram (SD) for that board (located by referring to the Table of Contents at the front of the manual) can be employed to assist the technician in circuit tracing the bad board. Note that the procedures outlined are confined to troubleshooting of the N10 only. Insure that the D14 Mainframe or IEEE interface board are not the source of the problem before starting.

In general, troubleshooting of the N10 unit is divided into three preliminary categories. First, the displays (CRT and LED readouts) are observed to determine in what general area the fault might lie. Second, a known and specific signal is applied and varied as required to allow a general determination of the severity and parameters of the trouble. Third, suspect PC boards are placed on extenders and waveforms and dc voltage indications are traced and checked. Following this initial philosophy, the subsequent steps given in this section can be used to isolate and locate the particular PC board responsible for a particular problem.

7.4.1 Equipment Required

The following items are required for the testing and servicing of a malfunctioning N10 unit:

Qty.	Description		Ref. Desig.
1	Oscilloscope	1mV, 1MHz except for logic circuits which require 2V, 50 MHz	SCOPE
1	Logic Probe	HP 545A or equivalent	LOG PR
1	Digital Volt Meter	5½ digit, 0.01%	DMV
1	Detector Simulator	Wavetek Pacific Measurements P/N 15484	DET DC
1	Extender Kit	Wavetek Pacific Measurements P/N 15387	EXT
1	1038-D14A Mainframe	with option 04 (if problem involves bus operation)	MAINFRAME
1	Detector Calibration Cable	Wavetek Pacific Measurements P/N 15636	CAL CBL

7.4.2 Initial Set-Up and Preliminary Checks

A. Connect detectors to channel A and the Reference channel. Connect the DET DC through the CAL CBL to channel B. Set the DET DC to -10 dBm. Connect the channel A detector to the CALIBRATOR. Turn the CALIBRATOR ON.

B. Set both A and B channels on INPUT

C. Set the OFFSET to 0.0 dB on both channels

D. Set REF LINE to CL on both channels

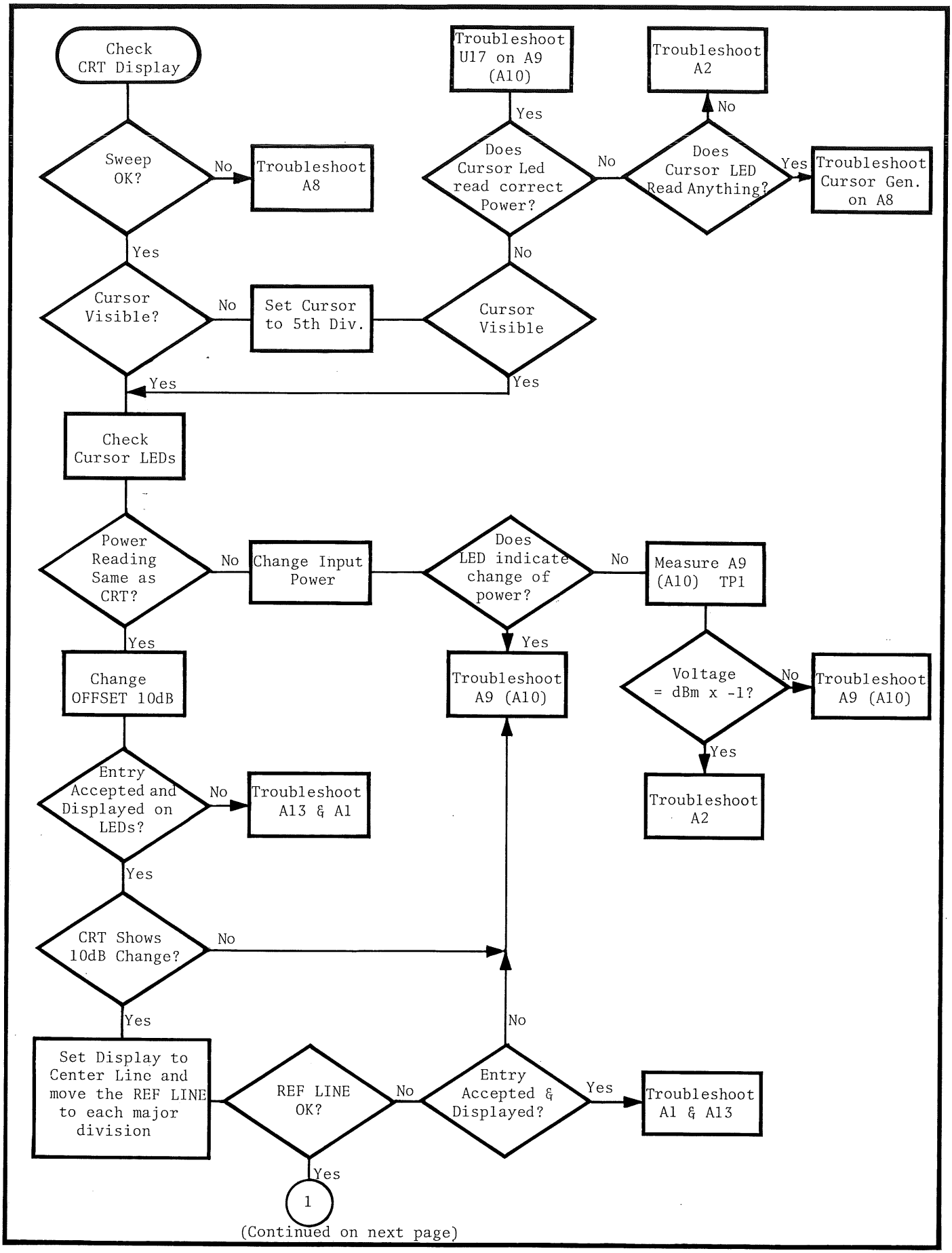
E. Set the sensitivity of both channels to 10 dB/DIV

F. Supply a ramp of 5 to 20V p-p to Aux 1 on the rear of the D14A, and set it for approximately 0.25 seconds forward time. Be sure that the retrace time is longer than 10 msec. Set the N10 for external sweep (INT SWEEP OFF). Connect the HORIZ OUT to Aux 3 on the rear of the D14A.

At this point, the CRT should show two horizontal lines. One line (A channel) should be at the center line of the graticule, and one line (B channel) should be located one division below the center graticule line. The lines should extend exactly to the ends of the graticule ±1 minor division. The A channel power display should be adjusted to 0.0 dBm using the CAL adjustment next to the detector input connectors. The B channel power display should be adjusted to -10 dBm with the CAL adjustment. The OFFSET LED display for both channels should show 0.0 dB. The sensitivity LEDs for both channels should show 10.0 dB/DIV. The REF LINE LEDs for both channels should show CL. The "Input" mode light for both channels should be ON. The CALIBRATOR light should be ON, the INT SWEEP light should be OFF, and the AUTO ZERO light should be OFF. If the AUTO ZERO light is on or blinking, turn OFF both channels and wait for the AUTO ZERO light to go out. If the light fails to go off after about 15 seconds, it will be necessary to find out which channel is causing the trouble. This can best be done by turning OFF the N10/D14A unit, removing one of the input boards (A3 or A4), and then turning the system ON again to see if the remaining board will work. After turn on, it will be necessary to press AUTO ZERO to start the function. After locating the faulty board, troubleshooting can proceed by placing the bad board on an extender and circuit tracing, referring to the circuit description (Section 5.3.3) and schematic diagram #15073.

If any portion of the above procedure could not be completed satisfactorily, refer to the troubleshooting flow charts for further help. If all characteristics seem to have a small error, recheck the setting of the +10.0V reference supply. See Section 7.3.2.1.

7.4.3 N10 Troubleshooting Flow Chart



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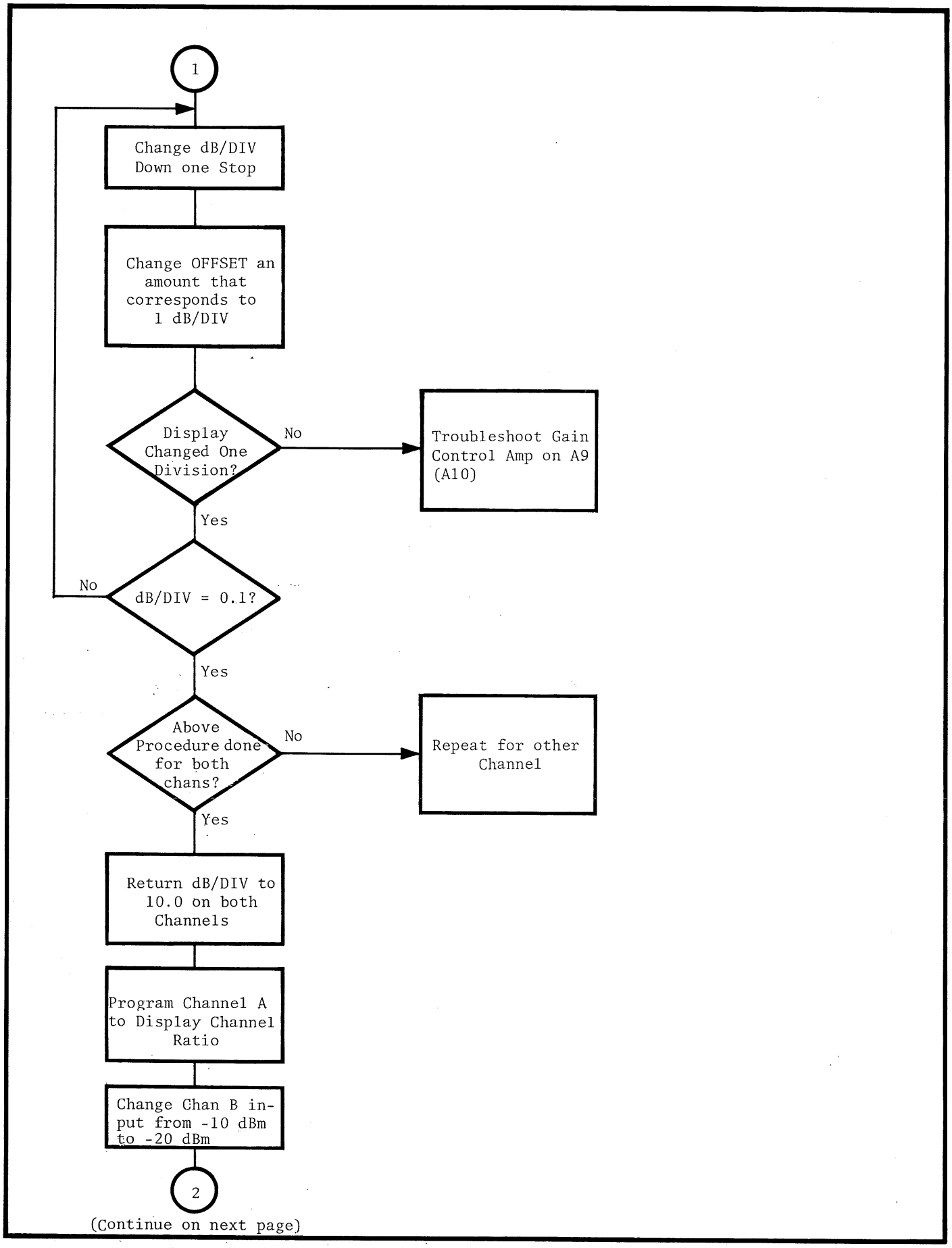

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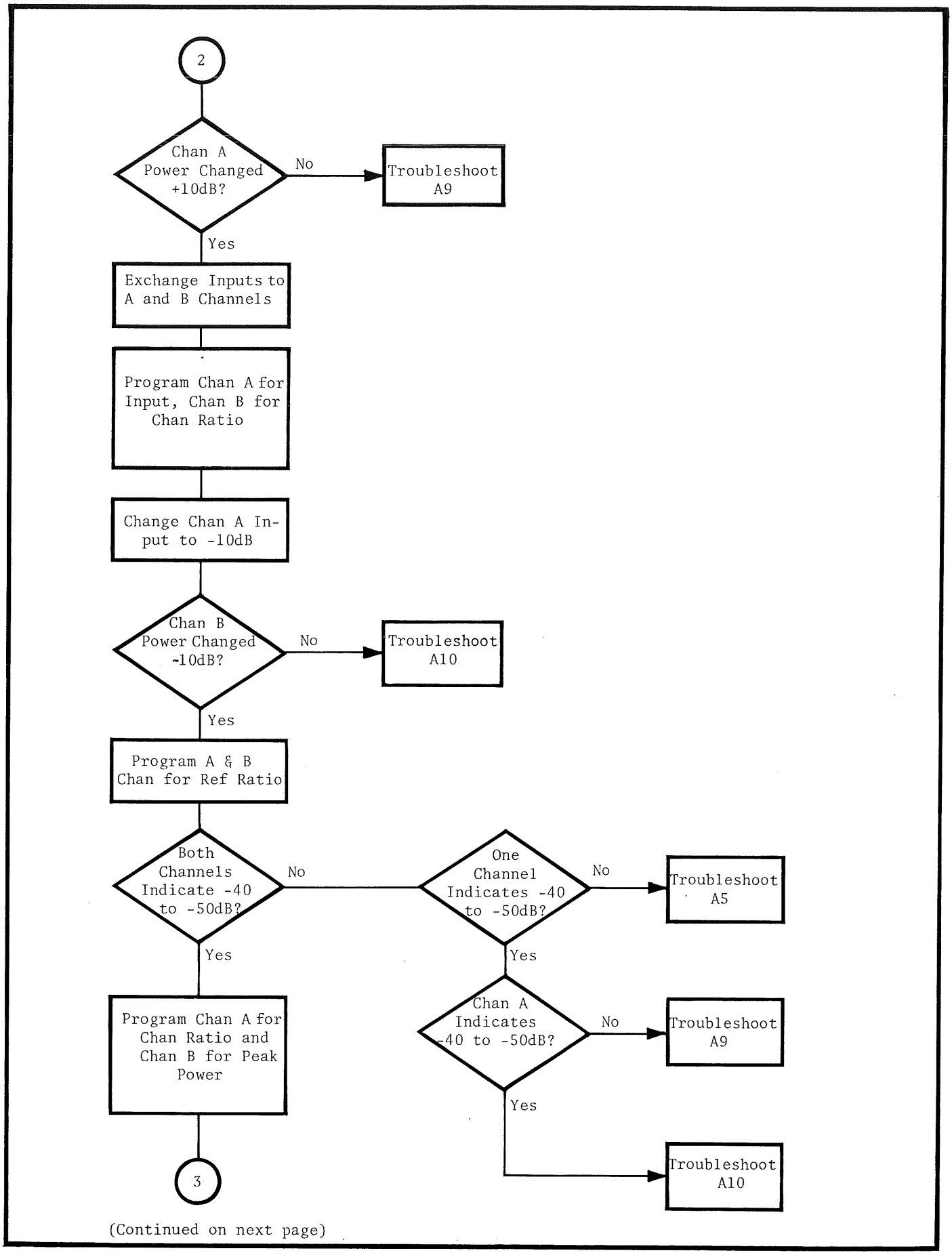

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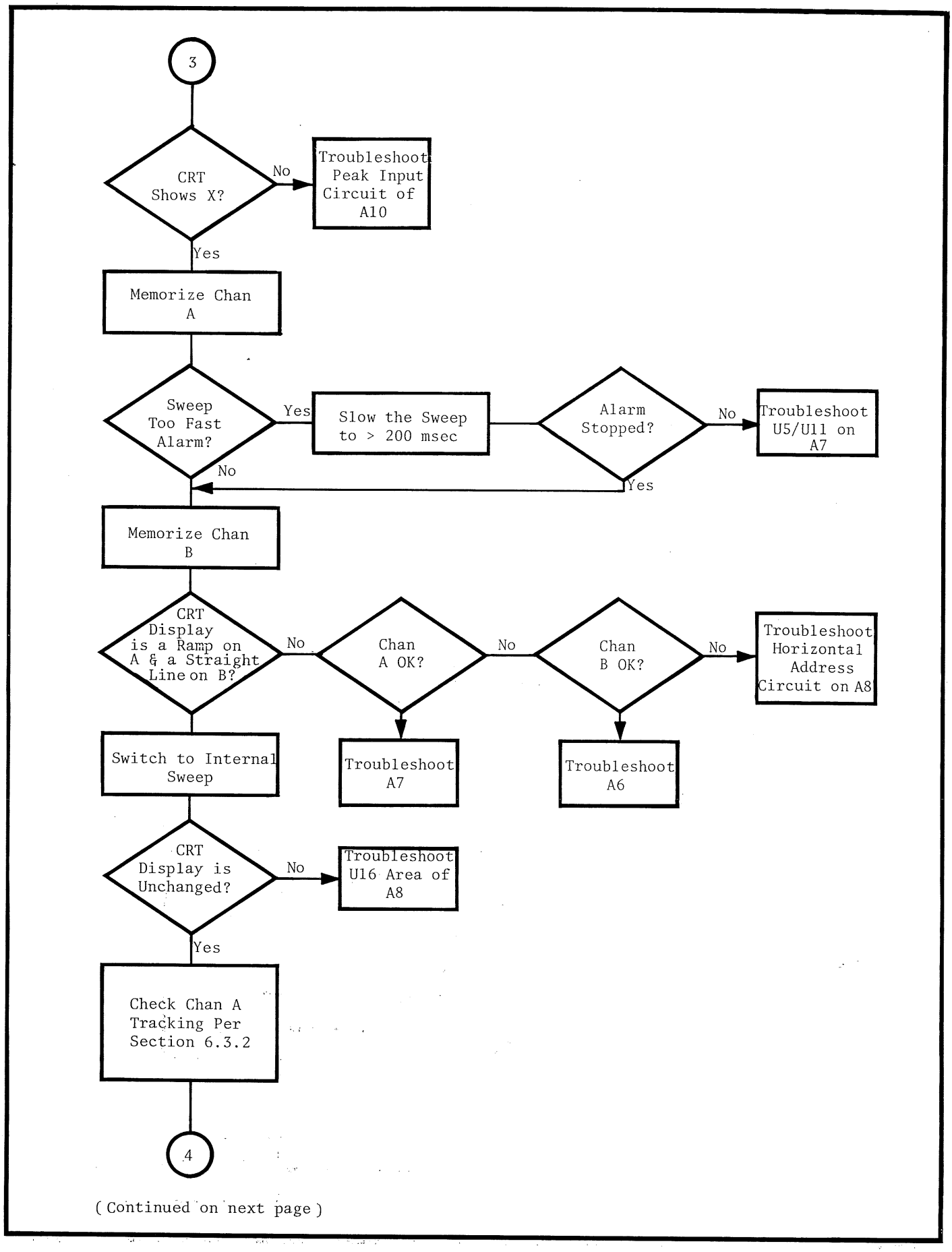

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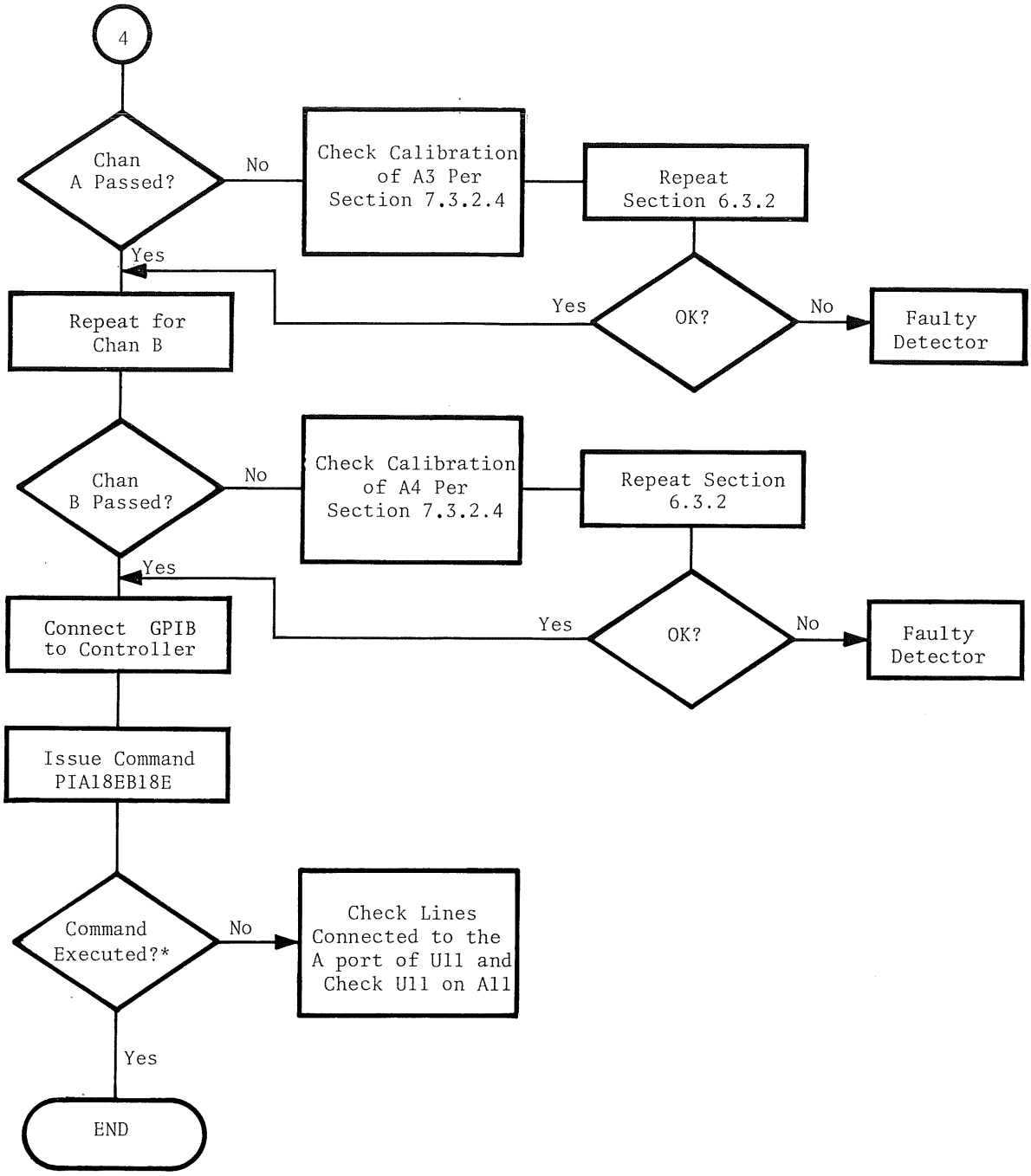
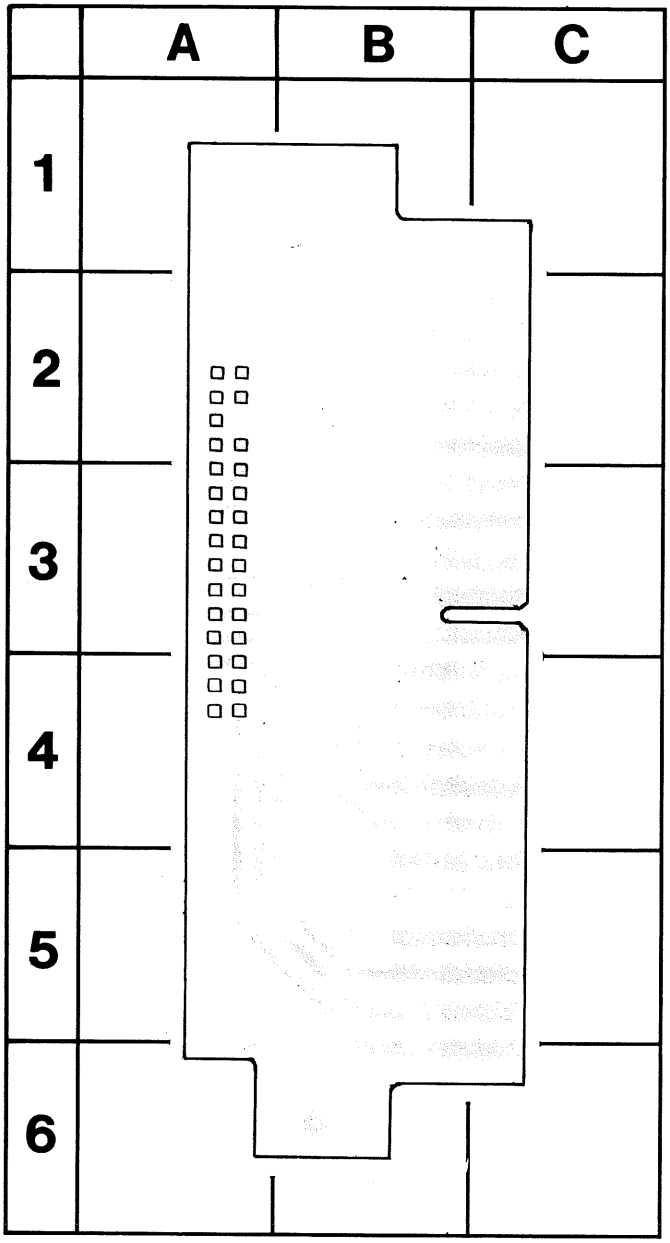


*"Command Executed" is indicated by all mode lights OFF, Chan A and B power displays indicating 0.0 dB ±0.1 dB, and internal sweep.

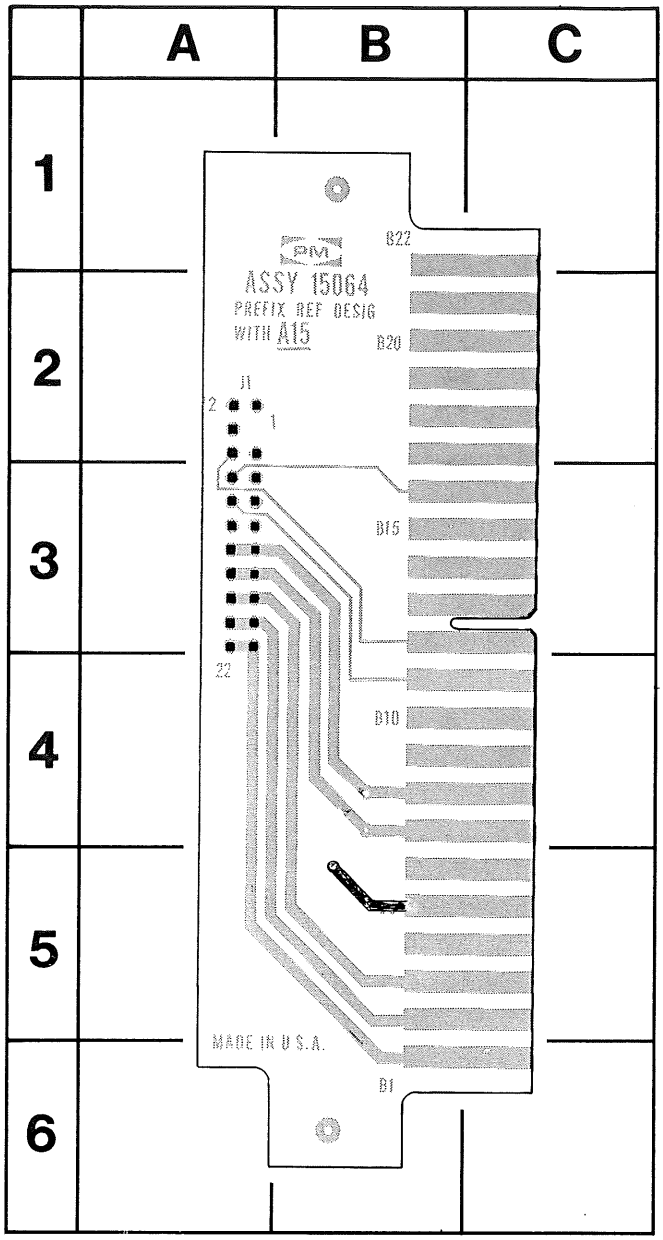
SECTION 8

BLOCK AND SCHEMATIC DIAGRAMS



CKT REF	GRID LOC
J1	A-3

FIGURE 8-1 HORIZONTAL FINGER PCB ASSEMBLY



CKT REF	GRID LOC
J1	A-3

FIGURE 8-2 A CHANNEL FINGER PCB ASSEMBLY

A 15
ASSEMBLY 15064
A CHANNEL
FINGER BOARD

J1 — W1 — J13

A1	BR-W	+15V
B1	BR-W	
A2	BK	-15V
B2	BK	
A3	W	15V COM
B3	W	
A7	GY	+5V
B7	GY	
A8	PR	5V COM
B8	PR	
A11	BL	'A' CHAN (+)
B11	G	'A' CHAN (-)
A12	Y	'B' CHAN (+)
B12	O	'B' CHAN (-)
A18	BR	RATIO A/X
A14	G	RATIO B/X
B16	Y	RATIO A
A15	O	RATIO B
A17	BR	RATIO COM
A5	BL	AUX 4 (TTL MARKER)
B5	R	AUX 4 COM
		NOT USED

A 12
ASSEMBLY 15005
INTERCONNECT BOARD

W7 — J14

4		+15V CAL POT 'A'
1		
3		CAL POT A R1 100K
5		CAL POT B R2 100K
7		CAL POT 'B' -15V
6		

CALIBRATOR OUTPUT

J1 — W8 — J2 — J3

A 14
ASSEMBLY 15023
HORIZONTAL
FINGER BOARD

J1 — W12 — J12

B4		DIAG I.D.
B6		CURSOR
A1		+15V
B1		
A2		-15V
B2		
A3		15V COM
B3		
A7		+5V
B7		
A8		5V COM
B8		
A4		-30V
B9		HORIZ. (+) SIGNAL
A9		HORIZ. (-) SIGNAL
A10		AUX 1
B11		AUX 2
A5		AUX 3
B10		AUX 1 & 2 COM
B5		AUX 3 COM
B18		DISPLAY A
B20		DISPLAY B
B12		DATA BUS Ø
B13		DATA BUS 1
B14		DATA BUS 2
B15		DATA BUS 3
B19		CHOPPER ACT. (DATA BUS 4)
A13		RETRACE
A12		PLUG-IN I.D.
B16		5V COM

A 1
ASSEMBLY 14950
DISPLAY DRIVER BOARD

J1 — W3 — J3

		OFFSET 1
		OFFSET 2
		OFFSET 3
		OFFSET 4
		OFFSET 5
		SENS. 1
		SENS. 2
		SENS. 3
		REF. LINE 1
		REF. LINE 2
		MODE COM.
		5V COM
		+5V
		A
		B
		C
		D
		DA1
		DE1
		DA2
		DE2
		DA3
		DE3

'A'

J2 — W4 — J4

		OFFSET 1
		OFFSET 2
		OFFSET 3
		OFFSET 4
		OFFSET 5
		SENS. 1
		SENS. 2
		SENS. 3
		REF. LINE 1
		REF. LINE 2
		MODE COM.
	R	MISC. COM.
	a	SEGMENTS
	b	
	c	
	d	
	e	
	f	
	g	
	dp	
		SWEEP ERROR
		ZERO LAMP OFF
		ALARM
		NOT USED

'B'

A 13
ASSEMBLY 14968
FRONT PANEL

A 2
ASSEMBLY 14953
DISPLAY & CALIBRATION BOARD

J1 — W5

a	PR	
b	Y	
c	GY	
d	R-W	
e	BL	
f	BK	
g	BR-W	
	5Vdp	
'1'	O-W	
'2'	BR	
'3'	PR	
'4'	BK	
	Y-W	POLARITY DRIVE '-'
	BL	NOT USED

J2 — W6

a	PR	
b	Y	
c	GY	
d	R-W	
e	G	
f	BK	
g	BR-W	
'1'	BL	
'2'	BK	
'3'	W	
'4'	O-W	
'5'	G-W	
	O	POLARITY DRIVE '-'
	5Vdp	
	Y-W	

A 3
ASSEMBLY 15072
INPUT PREAMP AND
LOG CIRCUIT

A 5
ASSEMBLY 15227
REF. CHAN. PREAMP
AND LOG CIRCUIT

A 4
ASSEMBLY 15072
INPUT PREAMP AND
LOG CIRCUIT

CHANNEL A — W9 — J3

	O	'A' DET. COM.
	R	'A' DET. COMP R
	BK	'A' DET. I.D.
	W	'A' DET. THERM.
	G	'A' DET. (+)
	BL	'A' DET. (-)
	—	COM.

S2

REFERENCE — W10 — J4

	O	'R' DET. COM.
	R	'R' DET. COMP R
	BK	'R' DET. I.D.
	W	'R' DET. THERM.
	G	'R' DET. (+)
	BL	'R' DET. (-)
	—	COM.

S2

CHANNEL B — W11 — J5

	O	'B' DET. COM.
	R	'B' DET. COMP R
	BK	'B' DET. I.D.
	W	'B' DET. THERM.
	G	'B' DET. (+)
	BL	'B' DET. (-)
	—	COM.

S2

NOTE:
1. PIN #2 ON ALL AMP CONNECTORS ARE KEYING PINS.

DRAWN	J. Bauer	DATE	9-11-80
APPD	S. Wetenkamp		6-2-81

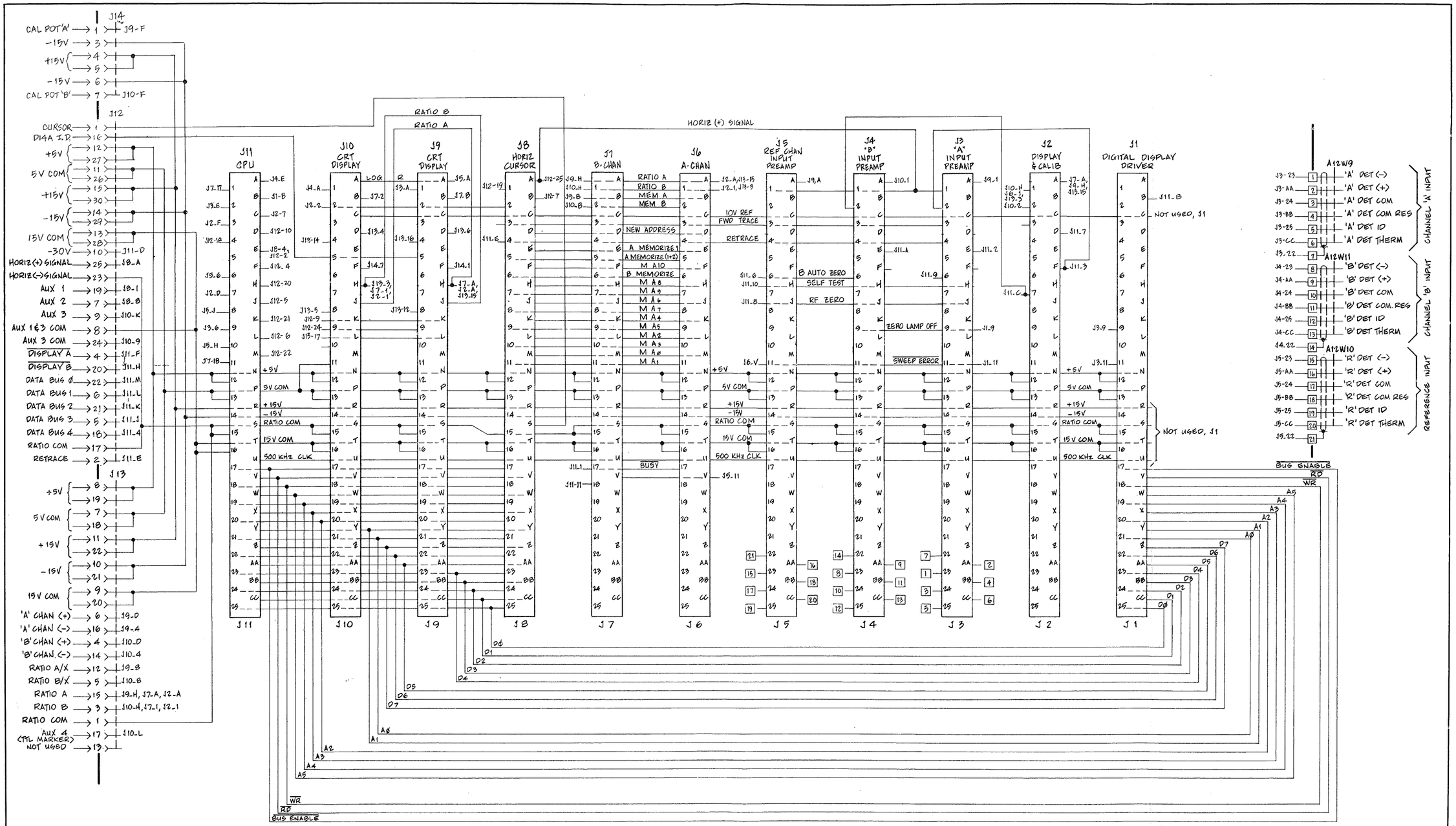
PM PACIFIC MEASUREMENTS INCORPORATED
SUNNYVALE, CALIFORNIA

N10 OVERALL SCHEMATIC

DRAWING NO. 15034 REV D
SHEET 1 OF 1

CKT REF	GRID LOC
J1	B-5
J2	C-5
J3	D-5
J4	E-5
J5	E-5
J6	F-5
J7	G-5
J8	H-5
J9	H-5
J10	I-5
J11	J-5
J12	K-4
J13	K-6
J14	B-4

FIGURE 8-3 INTERCONNECT PCB ASSEMBLY



ASSEMBLY 15005

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A 12

DRAWN TIEN	DATE 12.10.80	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
ENG S Watenkamp	6-2-81	NIO INTERCONNECT BD.	
PROD		DRAWING NO. 15006	REV D
		SHEET 1 OF 2	

P1 PIN NO.	J1 DISPLAY DRIVER BD (14951)	J2 DISPLAY & CALIBR BD (14954)	J3 PREAMP & LOG CKT (15073)	J4 PREAMP & LOG CKT (15073)	J5 REF CHAN PREAMP & LOG CKT	J6 'A' CHAN MEMORY (14880)	J7 'B' CHAN MEMORY (14888)	J8 HORIZ CURSOR BD (14911)	J9 CRT DISPLAY BD (14907)	J10 CRT DISPLAY BD (14907)	J11 CPU BOARD (14964)	P1 PIN NO.
A 1		RATIO 'A' RATIO 'B'	LOG 'A' HORIZ (+) SIGNAL	LOG 'B' HORIZ (+) SIGNAL	LOG 'R' HORIZ (+) SIGNAL	RATIO 'A' RATIO 'B'	RATIO 'A' RATIO 'B'	HORIZ (+) SIGNAL AUX 1	LOG 'R' LOG 'A'	LOG 'R' LOG 'B'	B' SMOOTHING OFF $\overline{\text{BUSY}}$	1 A
B 2	KEYBD INTERRUPT	CURSOR PIP	'A' ON	'B' ON		MEM 'A' MEM 'B'	MEM 'A' MEM 'B'	AUX 2 CURSOR PIP	MEM 'A' CURSOR PIP	MEM 'B' CURSOR PIP	KEYBD INTERRUPT 'A' SMOOTHING OFF	2 B
C 3	10V REF	10V REF	10V REF FWD TRACE	10V REF FWD TRACE	10V REF FWD TRACE	10V REF FWD TRACE	10V REF FWD TRACE	10V REF FWD TRACE	10V REF	10V REF	'B' ON 'A' ON	3 C
D 4		CAL	RETRACE	RETRACE	RETRACE	NEW ADDRESS RETRACE	NEW ADDRESS RETRACE	NEW ADDRESS RETRACE	'A' CHAN (+) 'A' CHAN (-)	'B' CHAN (+) 'B' CHAN (-)	-30V CHOPPER ACT (DATA BUS 4)	4 D
E 5			'A' SMOOTHING OFF	'B' SMOOTHING OFF		'A' MEMORIZE 1 'A' MEMORIZE (1+2)	'A' MEMORIZE 1 'A' MEMORIZE (1+2)	'A' MEMORIZE 1 'A' MEMORIZE (1+2)	D14A I.D.	D14A. I.D.	RETRACE SPARE	5 E
F 6		'A' ON	'A' AUTO ZERO	B' AUTO ZERO	'B' AUTO ZERO	M A10 'B' MEMORIZE	M A10 'B' MEMORIZE	M A10 'B' MEMORIZE	CAL POT 'A'	CAL POT 'B'	$\overline{\text{DISPLAY 'A'}}$ B' AUTO ZERO	6 F
H 7		B' ON	SELF TEST	SELF TEST	SELF TEST	M A8 M A9	M A8 M A9	M A8 M A9	RATIO 'A'	RATIO 'B'	$\overline{\text{DISPLAY 'B'}}$ CAL	7 H
J 8			RF ZERO	RF ZERO	RF ZERO	M A6 M A7	M A6 M A7	M A6 M A7	RATIO 'B' RATIO 'A'/X	RATIO 'A' RATIO 'B'/X	DATA BUS 3 RF ZERO	8 J
K 9	ZERO LAMP OFF		ZERO LAMP OFF	ZERO LAMP OFF		M A4 M A5	M A4 M A5	M A4 M A5	AUX 3 AUX 3 COM	AUX 3 AUX 3 COM	DATA BUS 2 'A' AUTO ZERO	9 K
L 10						M A2 M A3	M A2 M A3	M A2 M A3	AUX 4 (TTL MARKER)	AUX 4 (TTL MARKER)	DATA BUS 1 SELF TEST	10 L
M 11	SWEEP ERROR		SWEEP ERROR	SWEEP ERROR	SWEEP ERROR	M AØ M A1	M AØ M A1	M AØ M A1		SELECT 'B'	DATA BUS 0 SPARE	11 M
N 12	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	+5V +5V	12 N
P 13	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	5V COM 5V COM	13 P
R 14	+15V -15V	+15V -15V	+15 V -15 V	+15 V -15 V	+15 V -15 V	+15 V -15 V	+15 V -15 V	+15 V -15 V	+15 V -15 V	+15V -15V	+15V -15V	14 R
S 15	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	CURSOR RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	RATIO COM RATIO COM	15 S
T 16	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	15V COM 15V COM	16 T
U 17	500 KHZ CLK BUS ENABLE	500 KHZ CLK	500 KHZ CLK	500 KHZ CLK	500 KHZ CLK	500 KHZ CLK $\overline{\text{BUSY}}$	500 KHZ CLK $\overline{\text{BUSY}}$	500 KHZ CLK $\overline{\text{BUS ENABLE}}$	500 KHZ CLK $\overline{\text{BUS ENABLE}}$	500 KHZ CLK $\overline{\text{BUS ENABLE}}$	500 KHZ CLK $\overline{\text{BUS ENABLE}}$	17 U
V 18	RD WR					$\overline{\text{SWEEP ERROR}}$	$\overline{\text{SWEEP ERROR}}$	RD WR	RD WR	RD WR	RD WR	18 V
W 19	A5 A4							A5 A4	A5 A4	A5 A4	A5 A4	19 W
X 20	A3 A2							A3 A2	A3 A2	A3 A2	A3 A2	20 X
Y 21	A1 AØ							A1 AØ	A1 AØ	A1 AØ	A1 AØ	21 Y
Z 22	D7 D6							D7 D6	D7 D6	D7 D6	D7 D6	22 Z
AA 23	D5 D4		'A' DET + 'A' DET -	'B' DET + 'B' DET -	'R' DET + 'R' DET -			D5 D4	D5 D4	D5 D4	D5 D4	23 AA
BB 24	D3 D2		'A' DET COMP R 'A' DET COM	'B' DET COMP R 'B' DET COM	'R' DET COMP R 'R' DET COM			D3 D2	D3 D2	D3 D2	D3 D2	24 BB
CC 25	D1 DØ		'A' DET THERM 'A' DET 10	'B' DET THERM 'B' DET 10	'R' DET THERM 'R' DET 10			D1 DØ	D1 DØ	D1 DØ	D1 DØ	25 CC

PIN NO.'S FOR AMP CONNECTOR	J12 HORIZONTAL FINGER PCB (15023)	J13 A-CHAN FINGER PCB (15064)	J14 CAL POT A & B	PIN NO.'S FOR AMP CONNECTOR
1	CURSOR	RATIO COM	CAL POT 'A'	1
2	RETRACE	KEYING PIN	KEYING PIN	2
3	KEYING PIN	RATIO B	-15 V	3
4	DISPLAY A	'B' CHAN (+)	+15V	4
5	DATA BUS 3	RATIO 'B'/X	+15V	5
6	DATA BUS 1	'A' CHAN (+)	-15V	6
7	AUX 2	5V COM	CAL POT 'B'	7
8	AUX 1&2 COM (15V COM)	+5V		8
9	AUX 3	15V COM		9
10	-30 V	-15V		10
11	5V COM	+15V		11
12	+5V	RATIO 'A'/X		12
13	15V COM	NOT USED		13
14	-15V	'B' CHAN (-)		14
15	+15V	RATIO 'A'		15
16	D14A I.D.	'A' CHAN (-)		16
17	+RATIO COM	AUX 4 (TTL MARKER)		17
18	DATA BUS 4	5V COM		18
19	AUX 1	+5V		19
20	$\overline{\text{DISPLAY B}}$	15V COM		20
21	DATA BUS 2	-15V		21
22	DATA BUS Ø	+15V		22
23	+HORIZ (-) SIGNAL			23
24	AUX 3 COM			24
25	HORIZ (+) SIGNAL			25
26	5V COM			26
27	+5V			27
28	15V COM			28
29	-15V			
30	+15V			

DRAWN B. Owen	DATE 5/28/81	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
CHECKED		NIO INTERCONNECT BD.	
ENG S. Wetenkamp	6-2-81	DRAWING NO 15006	REV D
MFG ENG		SHEET 2 OF 2	
QA			

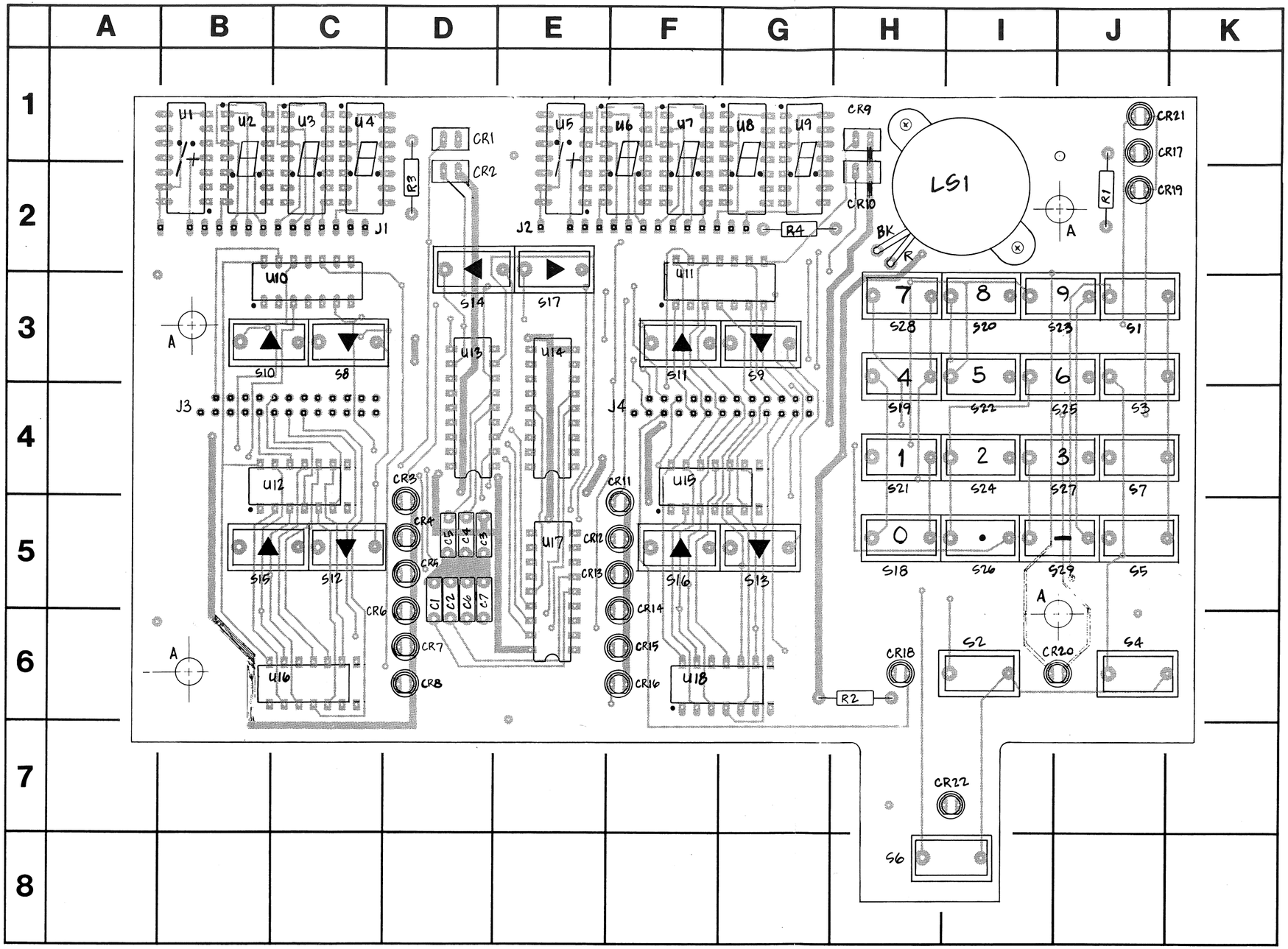
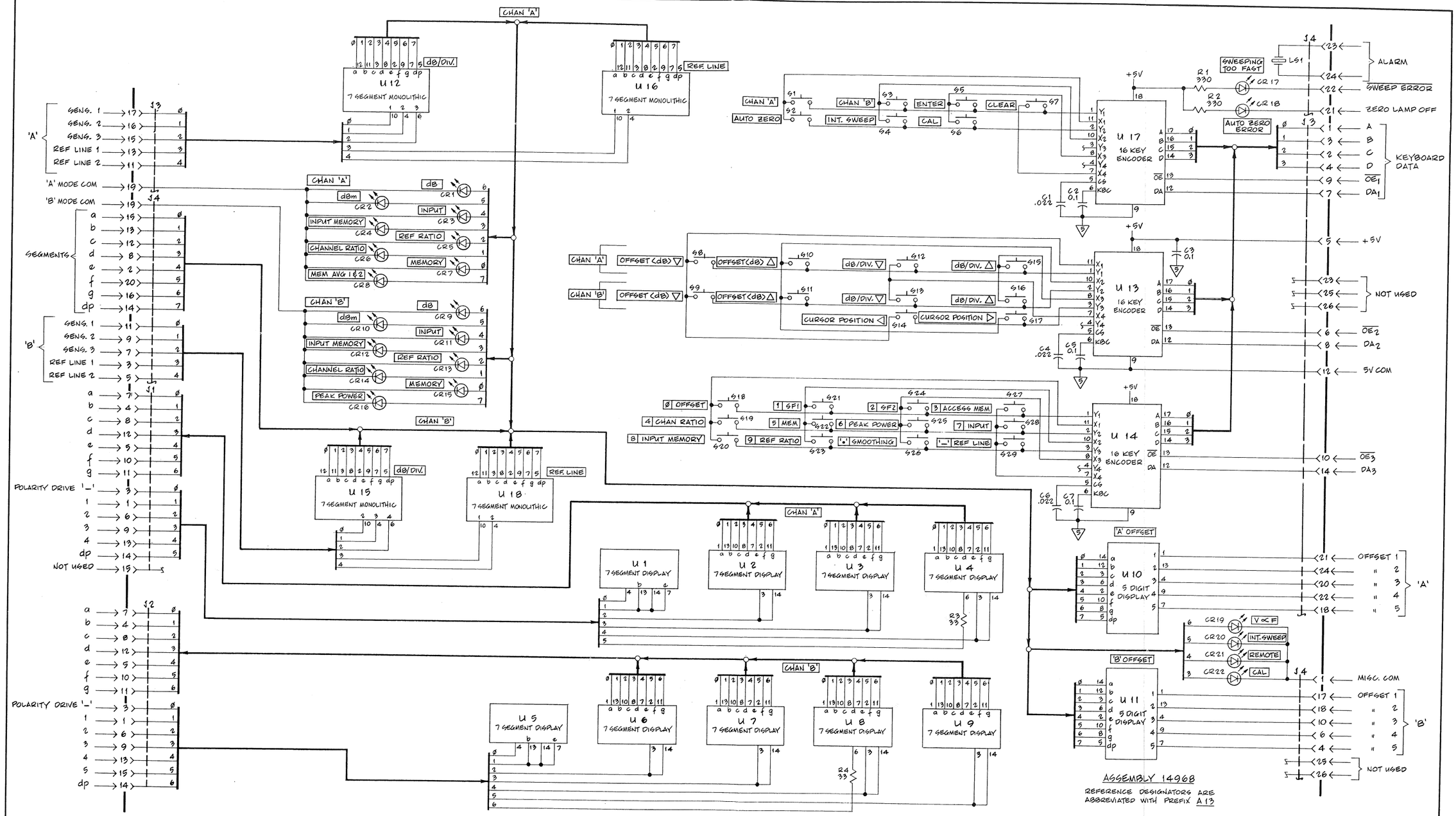


FIGURE 8-4 FRONT PANEL PCB ASSEMBLY

CKT REF	GRID LOC
C1	D-5
C2	D-5
C3	D-5
C4	D-5
C5	D-5
C6	D-5
C7	D-5
CR1	D-1
CR2	D-2
CR3	D-5
CR4	D-5
CR5	D-5
CR6	D-6
CR7	D-6
CR8	D-6
CR9	H-1
CR10	H-2
CR11	F-5
CR12	F-5
CR13	F-5
CR14	F-6
CR15	F-6
CR16	F-6
CR17	J-1
CR18	H-6
CR19	J-2
CR20	J-6
CR21	J-1
CR22	I-7
J1	B-2
J2	F-2
J3	B-4
J4	F-4
LS1	I-2
R1	J-2
R2	H-6
R3	D-2
R4	G-2
S1	J-3
S2	I-6
S3	J-3
S4	J-6
S5	J-5
S6	I-8
S7	J-4
S8	C-3
S9	G-3
S10	B-3
S11	F-3
S12	C-5
S13	G-5
S14	D-3
S15	B-5
S16	F-5
S17	E-3
S18	H-5
S19	H-3
S20	I-3
S21	H-4
S22	I-3
S23	J-3
S24	I-4
S25	J-3
S26	I-5
S27	J-4
S28	H-3
S29	J-5
U1	B-1
U2	B-1
U3	C-1
U4	C-1
U5	E-1
U6	F-1
U7	F-1
U8	G-1
U9	G-1
U10	C-3
U11	F-3
U12	C-4
U13	D-4
U14	E-4
U15	F-4
U16	C-6
U17	E-5
U18	G-6



ASSEMBLY 14968

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A13

RBF DESIG.	TYPE
U13, U14, U17	MM74C922
U12, U15, U16, U18	5082-7402
U10, U11	5082-7403
U2, U3, U4, U6 U7, U8, U9	5082-7610
U1, U5	5082-7616

NOTES:
1. UNLESS OTHERWISE SPECIFIED, REGISTORS VALUES ARE IN OHMS, 1/4 W, ± 5% AND CAPACITORS VALUES ARE IN MICROFARADS.

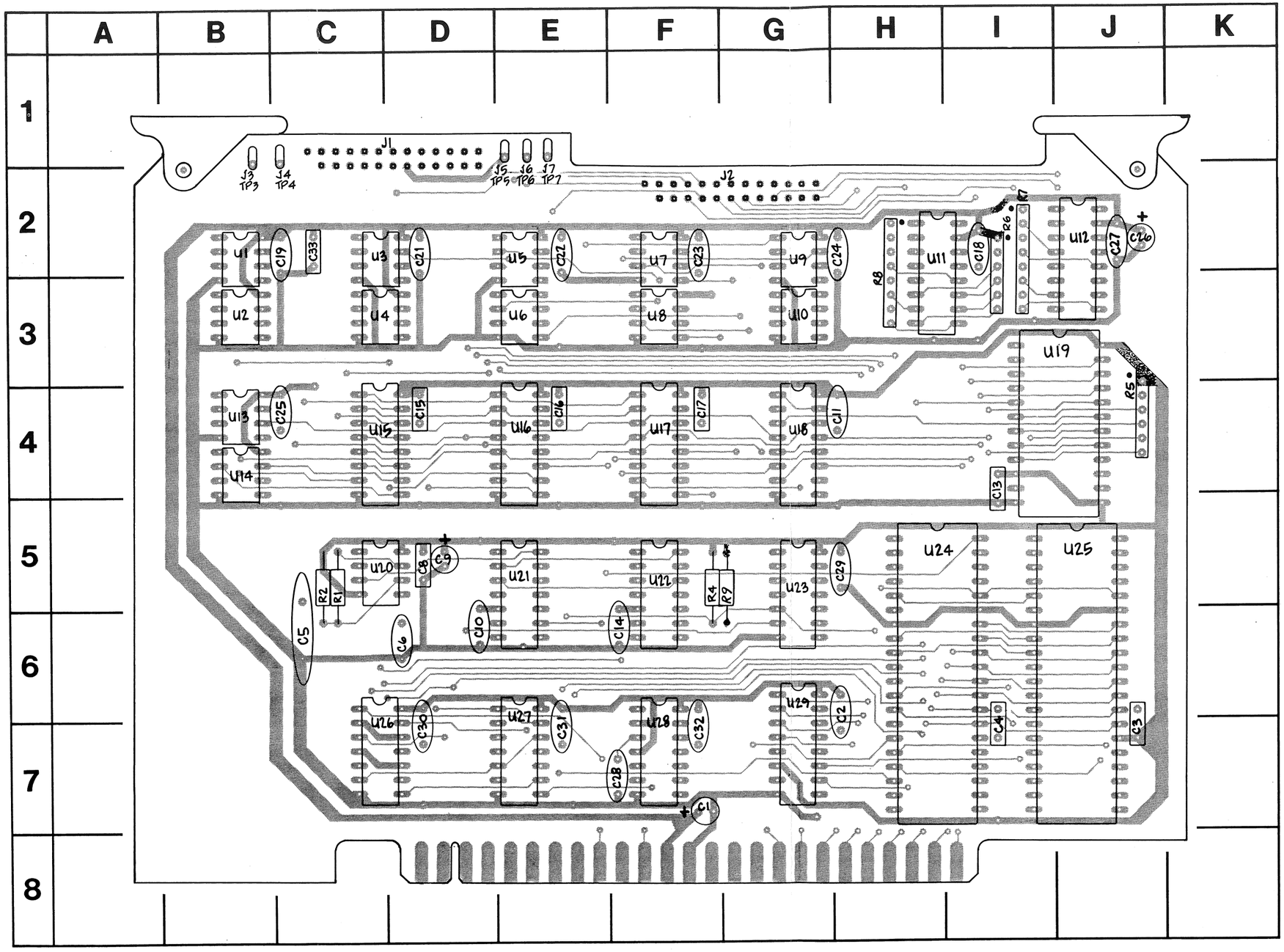
DRAWN	TIEN	DATE	2.11.81
ENG	S Watenkamp		6-2-81
PROD			

PACIFIC MEASUREMENTS INCORPORATED
SUNNYVALE, CALIFORNIA

FRONT PANEL

DRAWING NO. 15003 REV A

SHEET 1 OF 1



CKT REF	GRID LOC	CKT REF	GRID LOC
C1	F-7	U1	B-2
C2	H-6	U2	B-3
C3	J-7	U3	C-2
C4	I-7	U4	C-3
C5	C-6	U5	E-2
C6	D-6	U6	E-3
C7	---	U7	F-2
C8	D-5	U8	F-3
C9	D-5	U9	G-2
C10	D-6	U10	G-3
C11	H-4	U11	H-2
C12	---	U12	J-2
C13	I-4	U13	B-4
C14	F-6	U14	B-4
C15	D-4	U15	C-4
C16	E-4	U16	E-4
C17	F-4	U17	F-4
C18	I-2	U18	G-4
C19	C-2	U19	J-4
C20	---	U20	C-5
C21	D-2	U21	E-5
C22	E-2	U22	F-5
C23	F-2	U23	G-5
C24	H-2	U24	I-6
C25	C-4	U25	J-6
C26	J-2	U26	C-7
C27	J-2	U27	E-7
C28	F-7	U28	F-7
C29	H-5	U29	G-7
C30	D-7		
C31	E-7		
C32	F-7		
C33	C-2		
J1	C-1		
J2	G-2		
R1	C-5		
R2	C-5		
R3	---		
R4	G-5		
R5	J-4		
R6	I-2		
R7	I-2		
R8	H-2		
R9	G-5		
TP1	---		
TP2	---		
TP3	B-1		
TP4	C-1		
TP5	E-2		
TP6	E-2		
TP7	E-2		

FIGURE 8-5 DIGITAL DISPLAY DRIVER PCB ASSEMBLY

ASSEMBLY 14950

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A1

REF. DESIG	TYPE	REF. DESIG	TYPE
U19	MCM 6810	U27	74LS08N
U18	74LS365N	U26, U28	74LS74N
U15, U16, U17, U29	74LS138N	U24, U25	8255A
U11, U12	CA 3082	U23	74LS01N
U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U13, U14	DS3611N	U21, U22	74LS93N
		U20	LM555CN

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTORS VALUES ARE IN OHMS, ± 5%, 1/4 W AND CAPACITORS VALUES ARE IN MICROFARADS.

DS3611N CONNECTION DIAGRAM

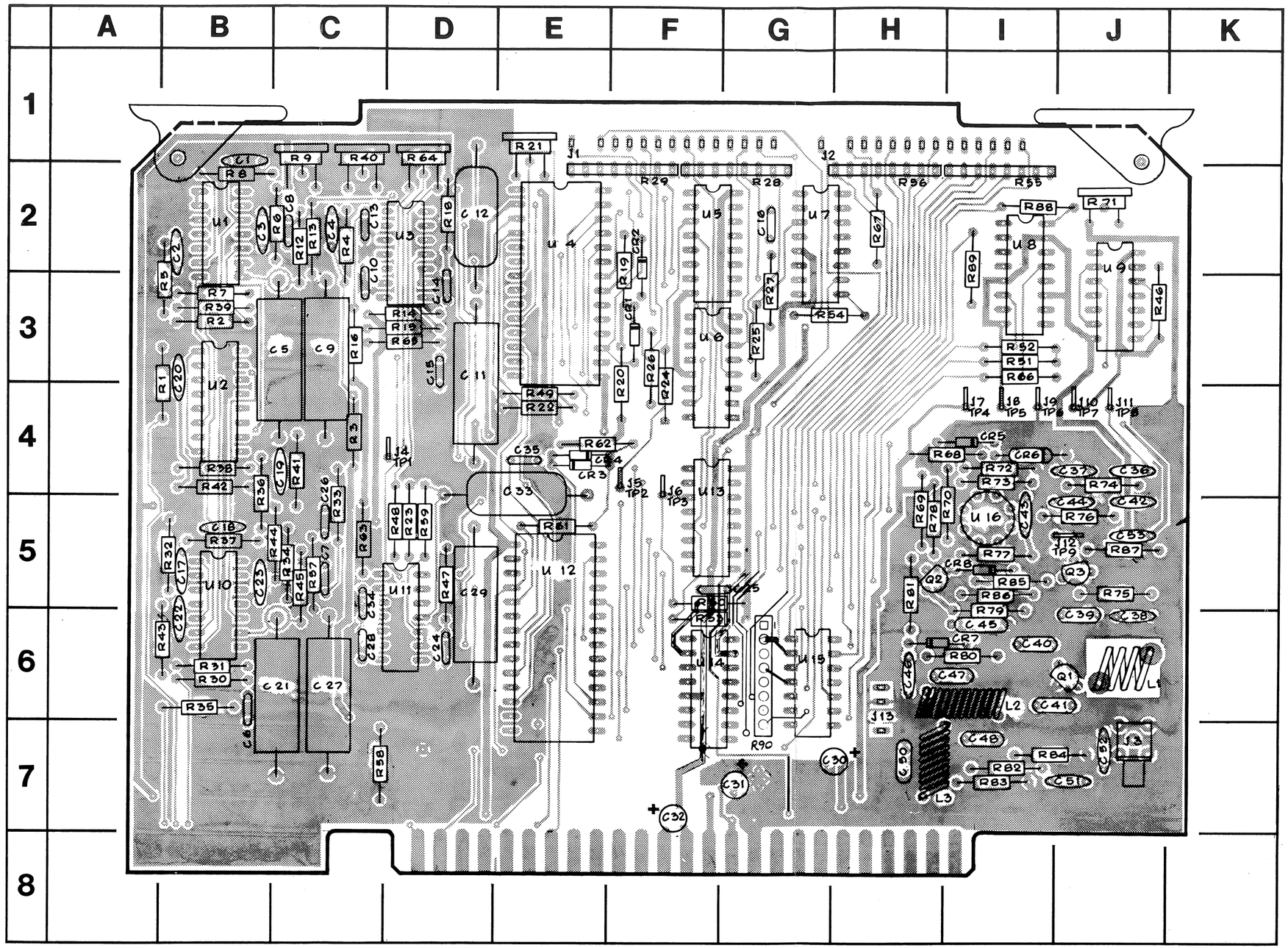
DRAWN	TIEN	DATE	1.12.81
ENG	S. Wetenkamp		6-2-81
PROD			

PACIFIC MEASUREMENTS INCORPORATED
SUNNYVALE, CALIFORNIA

DIGITAL DISPLAY DRIVER

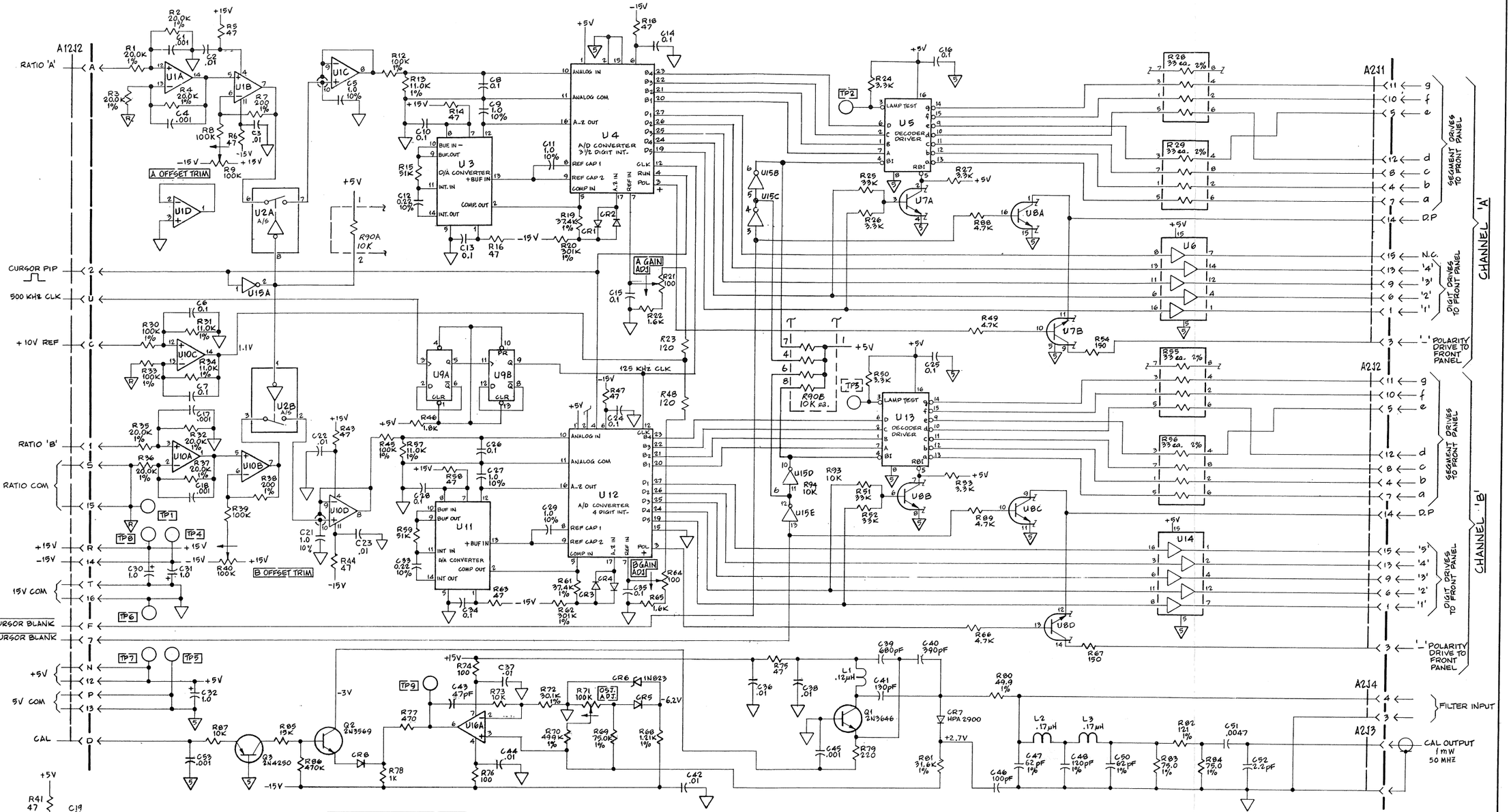
DRAWING NO. 14951 REV A

SHEET 1 OF 1



CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	B-1	CR1	F-3	R22	E-4	R78	H-5
C2	B-2	CR2	F-3	R23	D-5	R79	J-6
C3	B-2	CR3	E-4	R24	F-4	R80	I-6
C4	C-2	CR4	E-4	R25	G-3	R81	H-5
C5	B-3	CR5	I-4	R26	F-3	R82	I-7
C6	B-6	CR6	I-4	R27	G-3	R83	I-7
C7	C-5	CR7	H-6	R28	G-2	R84	I-7
C8	C-2	CR8	I-5	R29	F-2	R85	I-5
C9	C-3			R30	B-6	R86	I-5
C10	C-3			R31	B-6	R87	J-5
C11	D-4	J1	F-1	R32	B-5	R88	I-2
C12	D-2	J2	H-1	R33	C-5	R89	I-2
C13	C-2	J3	J-7	R34	C-5	R90	G-6
C14	D-3	J4	---	R35	B-6		
C15	D-4	J5	---	R36	B-5	TP1	C-4
C16	G-2	J6	---	R37	B-5	TP2	F-4
C17	B-5	J7	---	R38	B-4	TP3	F-4
C18	B-5	J8	---	R39	B-3	TP4	I-4
C19	B-4	J9	---	R40	C-1	TP5	I-4
C20	B-3	J10	---	R41	C-4	TP6	I-4
C21	B-6	J11	---	R42	B-4	TP7	J-4
C22	B-6	J12	---	R43	A-6	TP8	J-4
C23	B-5	J13	H-6	R44	C-5	TP9	J-5
C24	D-6			R45	C-5		
C25	F-5			R46	J-3		
C26	C-5	L1	J-6	R47	D-5	U1	B-2
C27	C-6	L2	I-6	R48	D-5	U2	B-4
C28	C-6	L3	H-7	R49	E-4	U3	D-2
C29	D-6			R50	F-6	U4	E-3
C30	H-7			R51	I-3	U5	F-2
C31	G-7	Q1	J-6	R52	I-3	U6	F-3
C32	F-7	Q2	H-5	R53	F-6	U7	G-2
C33	E-5	Q3	J-5	R54	G-3	U8	I-2
C34	C-6			R55	I-2	U9	J-3
C35	E-4			R56	H-2	U10	B-6
C36	J-4	R1	A-3	R57	C-5	U11	D-6
C37	J-4	R2	B-3	R58	C-7	U12	E-6
C38	J-6	R3	C-4	R59	D-5	U13	F-5
C39	J-6	R4	C-2	R60	---	U14	F-6
C40	I-6	R5	A-3	R61	E-5	U15	G-6
C41	J-6	R6	B-2	R62	E-4	U16	I-5
C42	J-5	R7	B-3	R63	C-5		
C43	I-5	R8	B-2	R64	D-1		
C44	J-5	R9	C-1	R65	D-3		
C45	I-6	R10	---	R66	I-3		
C46	H-6	R11	---	R67	H-2		
C47	I-6	R12	C-2	R68	I-4		
C48	I-7	R13	C-2	R69	H-5		
C49	---	R14	D-3	R70	I-5		
C50	H-7	R15	D-3	R71	J-2		
C51	J-7	R16	C-3	R72	I-4		
C52	J-7	R17	---	R73	I-4		
C53	J-5	R18	D-2	R74	J-4		
		R19	F-3	R75	J-5		
		R20	F-4	R76	J-5		
		R21	E-1	R77	I-5		

FIGURE 8-6 DIGITAL DISPLAY AND CALIBRATION PCB ASSEMBLY



U16	741 HC
U15	SN74LS05N
U11	ICL 8052A
U9	SN74LS74N
U7, U8	CA 3083
U6, U14	CA 3082
U5, U13	DM 7447 AN
U4, U12	ICL7103 CDI
U3	ICL 8052
U2	DG 201 CJ
U1, U10	TL 064 CN
REF. DESIG	TYPE

NOTES:
UNLESS OTHERWISE SPECIFIED,
1. RESISTORS VALUES ARE IN OHMS, ±5%, 1/4W
2. CAPACITORS VALUES ARE IN MICROFARADS
3. DIODES ARE IN4148
4. ⏚ 15V COM.

ASSEMBLY 14953

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A2

DRAWN TIEN	DATE 12.17.80	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
ENG S. Wetzenkamp	6-2-81	DISPLAY & CALIBRATION BD	
		DRAWING NO. 14954	REV C
		SHEET 1 OF 1	

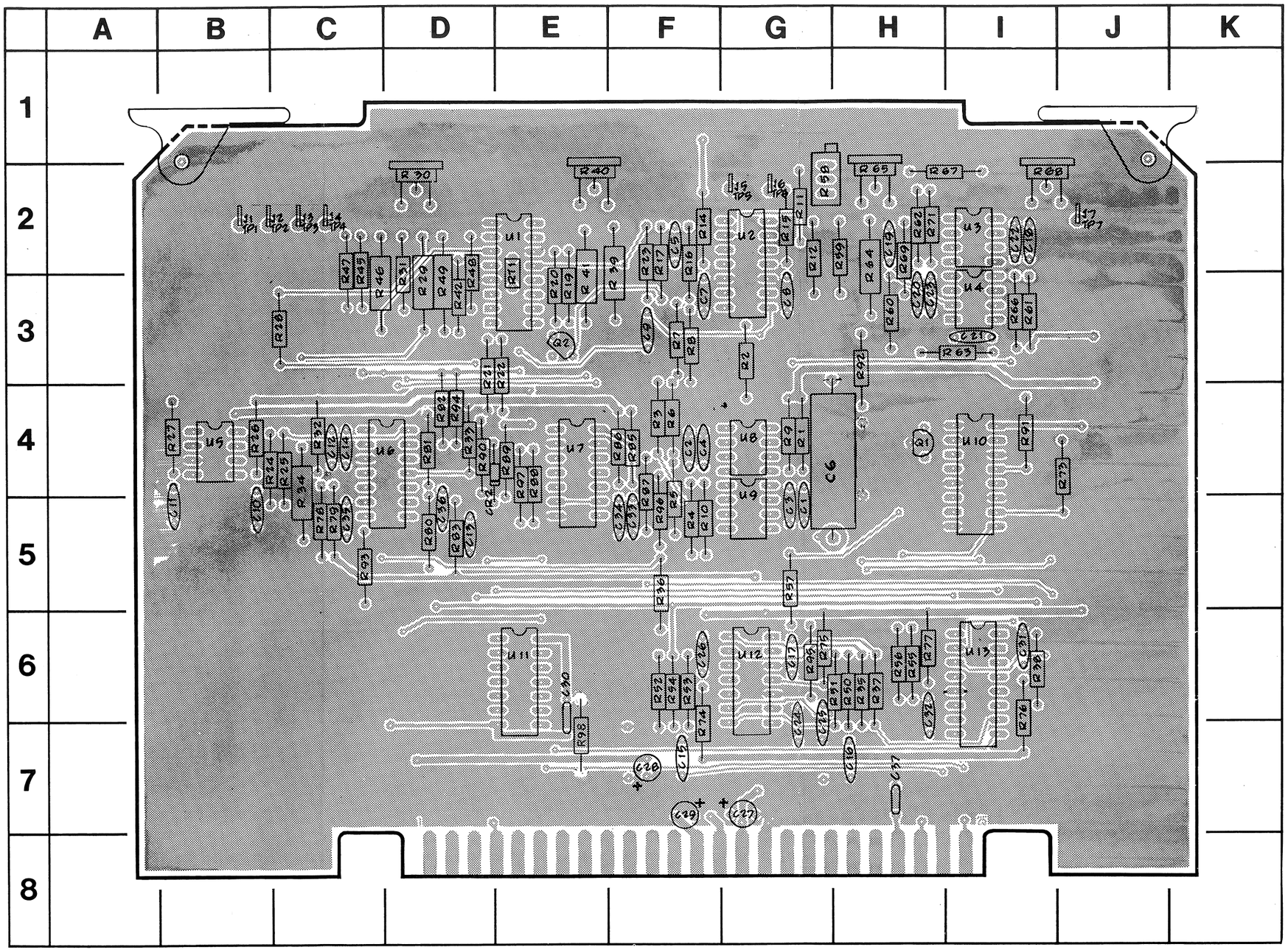


FIGURE 8-7 REFERENCE CHANNEL PREAMP LOG PCB ASSEMBLY

CKT REF	GRID LOC
C1	G-5
C2	F-4
C3	G-5
C4	F-4
C5	F-2
C6	G-4
C7	F-3
C8	G-3
C9	F-3
C10	B-5
C11	B-5
C12	C-4
C13	D-5
C14	C-4
C15	F-7
C16	H-7
C17	G-6
C18	I-2
C19	H-2
C20	H-3
C21	I-3
C22	I-2
C23	H-3
C24	G-7
C25	G-7
C26	F-6
C27	G-7
C28	F-7
C29	F-7
C30	E-7
C31	I-6
C32	H-7
C33	F-5
C34	F-5
C35	C-5
C36	D-5
C37	H-7
CR1	---
CR2	D-4
Q1	H-4
Q2	E-3
R1	G-4
R2	G-3
R3	F-4
R4	F-5
R5	F-5
R6	F-4
R7	F-3
R8	F-3
R9	G-4
R10	F-5
R11	G-2
R12	G-2
R13	---
R14	F-2
R15	G-2
R16	F-2
R17	F-3
R18	---
R19	E-3
R20	E-3
R21	D-3
R22	E-3
R23	F-3
R24	B-4
R25	C-4
R26	B-4
R27	B-4
R28	C-3
R29	D-3
R30	D-2
R31	D-3
R32	C-4
R33	D-4
R34	C-5
R35	H-6
R36	F-5
R37	H-6
R38	I-6
R39	E-3
R40	E-2
R41	E-3
R42	D-3
R43	---
R44	---
R45	C-3
R46	C-3
R47	C-3
R48	D-3
R49	D-3
R50	H-6
R51	H-6
R52	F-6
R53	F-6
R54	F-6
R55	H-6
R56	H-6
R57	G-5
R58	G-2
R59	G-2
R60	H-3
R61	I-3
R62	H-2
R63	H-3
R64	H-2
R65	H-2
R66	I-3
R67	H-2
R68	I-2
R69	H-2
R70	---
R71	H-2
R72	---
R73	I-4
R74	F-7
R75	G-6
R76	I-6
R77	H-6
R78	C-5
R79	C-5
R80	D-5
R81	D-4
R82	D-4
R83	D-5
R84	---
R85	F-4
R86	F-4
R87	F-4
R88	E-4
R89	E-4
R90	D-4
R91	I-4
R92	H-3
R93	C-5
R94	D-4
R95	G-6
R96	F-5
R97	E-4
R98	E-7
RT1	E-3
TP1	B-2
TP2	B-2
TP3	C-2
TP4	C-2
TP5	G-2
TP6	G-2
TP7	J-2
U1	E-3
U2	G-3
U3	I-2
U4	I-3
U5	B-4
U6	D-4
U7	E-4
U8	G-4
U9	G-5
U10	I-4
U11	E-6
U12	G-6
U13	I-6

A12J5 DET(-) 23 DET(+) AA 22

C33 .01 R85 47 +15V
R96 1K R87 2.2K R88 2.2K R97 1K R86 47 -15V
U7 DG303
C34 .01
C37 0.1

U9 U8 U2A U2B U2C U2D
R1 47 C1 .01 R2 4.99K 1% R3 4.02K 1% R4 47 C2 .01 R5 2.00K 1% R6 4.02K 1% R7 4.99K 1% R8 2.49K 1% R9 47 C3 .01 R10 47 C4 .01
R11 2.49K 1% R12 69.8K 1% R14 47 C7 .01 C8 .01 R15 47
TP5
R16 1M C5 330PF R17 17.8K 1% Q2 2N4250 R19 10K R20 100K C6 1.0 10% R21 4.7K R22 10K
U13A U13B U13C C9 47PF R23 3.9K R92 220
RD1

A12J5 SELF-TEST H RETRACE 4 DET I.D (Lo= Bal. det.) 25 DET THERM (10K @ 25°C) CC DET COMP. R (162K Nom.) BB DET COM 24 10V REF C + 15 V R - 15 V 14 15V COM T 16 +5V N 12 5V COM P 13 RATIO COM S 15

U11D U11B U11C
R98 3.3K +5V
R50 10.0K 1% R51 6.81K 1% +2.47V R56 143K 1% R55 143K 1% + 1.85V R52 249 K 1% R53 127 K 1% R54 499 K 1% +10V
U12B
C15 .01 C16 .01
TP4
R80 100K 1% R81 100K 1% R82 100K 1% R83 100K 1% R84 220 .001 +10V
U6D
C27 1.0 C28 1.0 C29 1.0 +15V -15V +5V
TP2 TP1

ASSEMBLY 15227

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A5

NOTE: UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 5% AND CAPACITOR VALUES ARE IN MICROFARADS.

REF. DESIG.	TYPE
U13	DG 201 CJ
U11	SN74LS02
U7	DG 303 CJ
U6, U12	TL064 CN
U3, U4, U5, U8, U9	OP-07CP
U2	TL074 CN
U1, U10	CA 3096 AE

U11A U11 C30 0.1 +5V

U1C LOG U1D CLAMP
R39 10.00K 0.1% R40 1K HIGH LEVEL LOG CAL

U10A C17 .01 R57 10K U12C R58 20K 20 TURNS Ø dBm COMP TP6 .57V@ Ø dBm R59 19.6K 1%
R60 100K C21 100pF R63 10K Q1 2N4250 R62 47 C19 .01 C20 .01 U4 U10B
U13 C31 .01 C32 .01 R76 47 R77 47 -15V U20

CAL CENTER +10V 300μA R30 5K R31 30.9 K 1%
R24 13.3K 1% R25 16.2K 1% R26 47 C10 .01 R28 9.11K 1% RT1 10K R29 10.00K 0.1% C35 470PF R32 47 C12 .01 R34 10.00K 0.1% TP3 R33, 470 C13 .01 R27 47 C11 .01 R78 5.90K 1% R79 10.0K 1%
U5 U6A
A12J5 A LOG 'R' (100 mV/dB)

R35 10.0K 1% R36 8.87K 1% R37 10.0K 1% R38 110K 1% +10V
U12A U13D 1.22 V
DET ID + SELF TEST

R89 15.0K 1% R90 1.00K 1% (-47 dBm Clamp) CR2 IN4148 U6B R42 174K 1% R41 169.0K 0.1%
R45 97.6K 1% R46 10.0M 1% 0.5V R47 5.11K 1% U6C C14 .01 R40 10K R49 10.00K 0.1% U1E

-10 dBm COMP R65 1K R64 10.00K 0.1% R66 47 R67 9.53K 1% C22 .01 U3 R69 4.99K 1% C23 .01 R71 47 R61 47 C18 .01
TP7 R73 4.99K 1% R68 2K R91 4.99K 1% +10 dBm COMP
U10C U10D U10E R95 220 C24 100pF 5% U12D C25 .01 C26 .01 R74 47 R75 47

DRAWN TIEN 8.22.80 REV
ENG. S. Wetenkamp 6-2-81
PROD
PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA
REF CHAN PREAMP & LOG CKT
DRAWING NO 15228 REV J
SHEET 1 OF 1

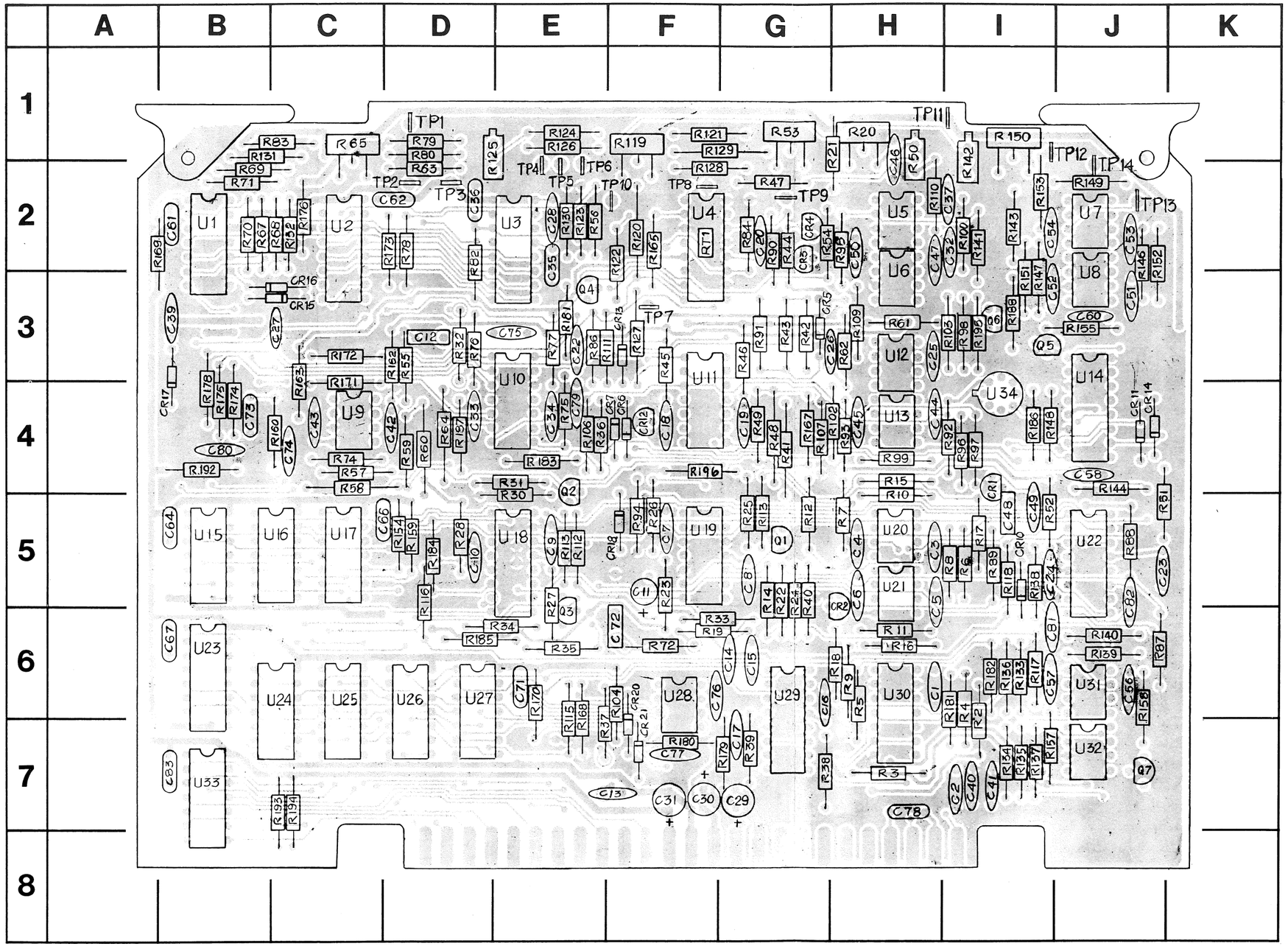


FIGURE 8-8 INPUT PREAMP PCB ASSEMBLY

CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	H-6	C58	J-4			R40	G-5
C2	I-7	C59	---			R41	G-4
C3	H-5	C60	J-3			R42	G-3
C4	H-5	C61	B-2			R43	G-3
C5	H-5	C62	D-2			R44	G-2
C6	H-5	C63	---			R45	F-3
C7	F-5	C64	B-5	Q1	G-5	R46	G-3
C8	G-5	C65	---	Q2	E-5	R47	G-2
C9	E-5	C66	C-5	Q3	E-6	R48	G-4
C10	D-5	C67	B-6	Q4	E-3	R49	G-4
C11	F-5	C68	---	Q5	I-3	R50	H-1
C12	D-3	C69	---	Q6	I-3	R51	J-5
C13	E-7	C70	---	Q7	J-7	R52	I-5
C14	G-6	C71	E-6			R53	G-1
C15	G-6	C72	F-5			R54	G-2
C16	G-7	C73	B-4			R55	D-3
C17	G-7	C74	C-4			R56	E-2
C18	F-4	C75	E-3			R57	C-4
C19	G-4	C76	F-6	R1	---	R58	C-4
C20	G-2	C77	F-7	R2	I-7	R59	D-4
C21	---	C78	H-7	R3	H-7	R60	D-4
C22	E-3	C79	E-4	R4	I-6	R61	H-3
C23	J-5	C80	B-4	R5	H-6	R62	H-3
C24	I-5	C81	I-6	R6	I-5	R63	D-2
C25	H-3	C82	J-5	R7	H-5	R64	D-4
C26	G-3	C83	B-7	R8	I-5	R65	C-1
C27	C-3			R9	H-6	R66	---
C28	E-2			R10	H-5	R67	B-2
C29	G-7			R11	H-6	R68	B-2
C30	F-7			R12	G-5	R69	B-2
C31	F-7			R13	G-5	R70	B-2
C32	I-2			R14	G-5	R71	B-2
C33	D-4			R15	H-4	R72	F-6
C34	E-4			R16	H-6	R73	---
C35	E-2			R17	I-5	R74	C-4
C36	D-2			R18	G-6	R75	E-4
C37	I-2	CR1	I-4	R19	F-6	R76	D-3
C38	---	CR2	G-5	R20	H-1	R77	E-3
C39	B-3	CR3	G-2	R21	H-1	R78	D-2
C40	I-7	CR4	G-2	R22	G-5	R79	D-1
C41	I-7	CR5	G-3	R23	F-5	R80	D-1
C42	D-4	CR6	F-4	R24	G-5	R81	E-3
C43	C-4	CR7	F-4	R25	G-5	R82	D-2
C44	H-4	CR8	---	R26	F-5	R83	C-1
C45	H-4	CR9	---	R27	E-5	R84	G-2
C46	H-2	CR10	I-5	R28	D-5	R85	---
C47	H-2	CR11	J-4	R29	---	R86	E-3
C48	I-5	CR12	F-4	R30	E-5	R87	J-6
C49	I-5	CR13	F-3	R31	E-5	R88	J-5
C50	H-2	CR14	J-4	R32	D-3	R89	I-5
C51	J-3	CR15	B-3	R33	F-6	R90	G-2
C52	I-3	CR16	B-3	R34	D-6	R91	G-3
C53	J-2	CR17	B-3	R35	E-6	R92	H-4
C54	I-2	CR18	F-5	R36	E-4	R93	H-4
C55	---	CR19	---	R37	E-7	R94	F-5
C56	J-6	CR20	F-7	R38	G-7	R95	H-2
C57	H-6	CR21	F-7	R39	G-7	R96	I-4

U17	SN74LS74N		
U16	SN74LS266N	U11	HA4741-5
U15	SN74LS393N	U33	SN74LS01N
U10,	TL064CN	U31	TL072CP
U6, U28	CA3240E	U30	DG303CJ
U5, U7, U8, U9, U12, U13, U20, U21, U32	HA-5135-5	U27	SN74LS02N
		U26	SN74LS04N
U4, U14 (MATCHED PAIR)	CA3083E	U24, U25	SN74LS00N
U3	DAC-08C	U23	SN74LS42N
U2	DM2503N	U19	TL074CN
U1	LM339	U18, U22, U29	DG201CJ
REF DESIGNATOR	TYPE	REF DESIGNATOR	TYPE

ASSEMBLY 15834

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A3 OR A4

NOTE: 1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, 1/4W, ±5% AND CAPACITOR VALUES ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE IN4148.
3. TRANSISTOR 2N3565 IS USED AS A DIODE.

EXAMPLE: NOT USED = ANODE / CATHODE

DRAWN	J. Bauer	DATE	4-19-82
ENG	TB		6-3-82
PROG			

PACIFIC MEASUREMENTS INCORPORATED, SUNNYVALE, CALIFORNIA

INPUT PREAMP AND LOG PCB

DRAWING NO 15835 REV E

SHEET 1 OF 1

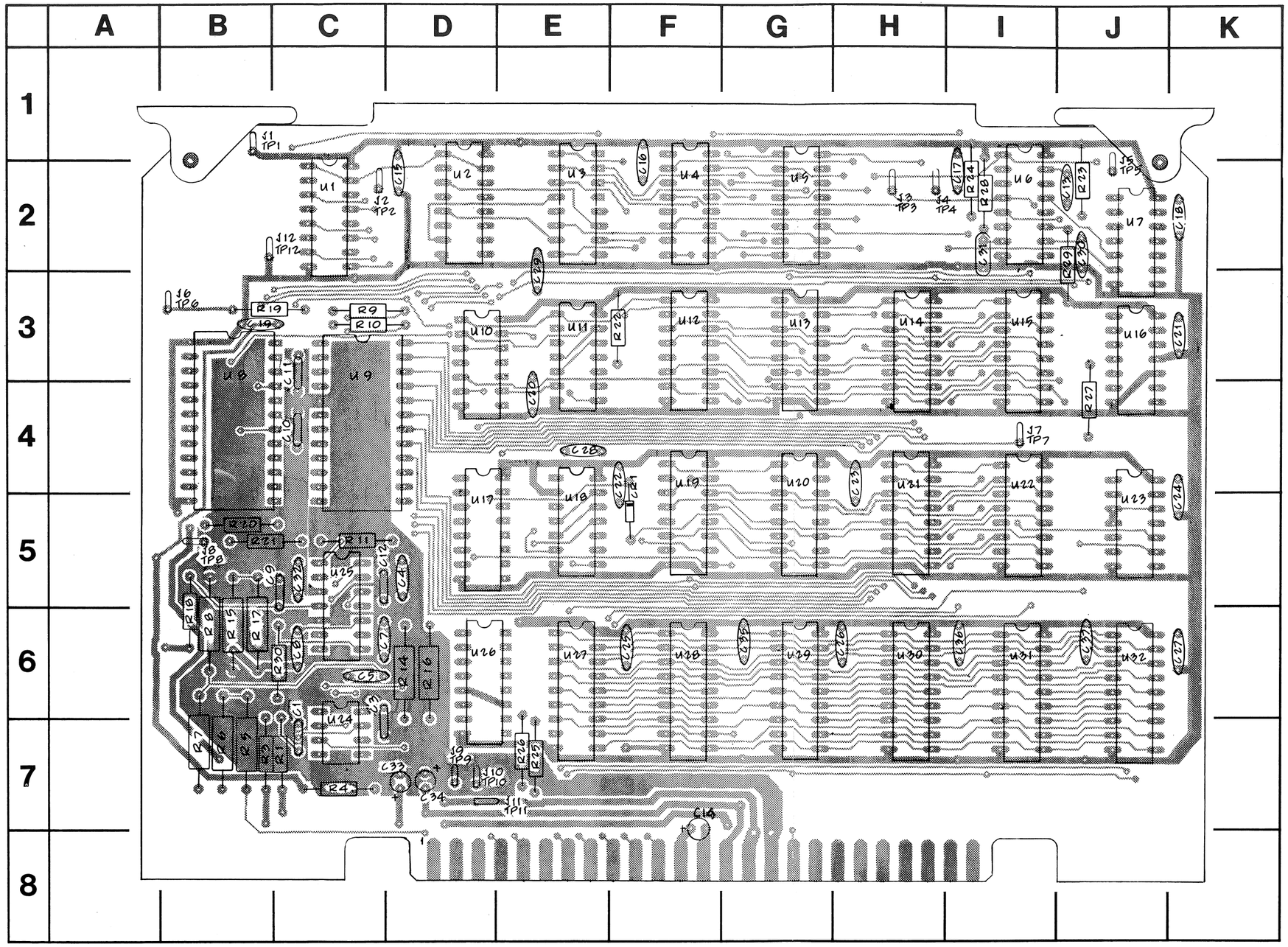
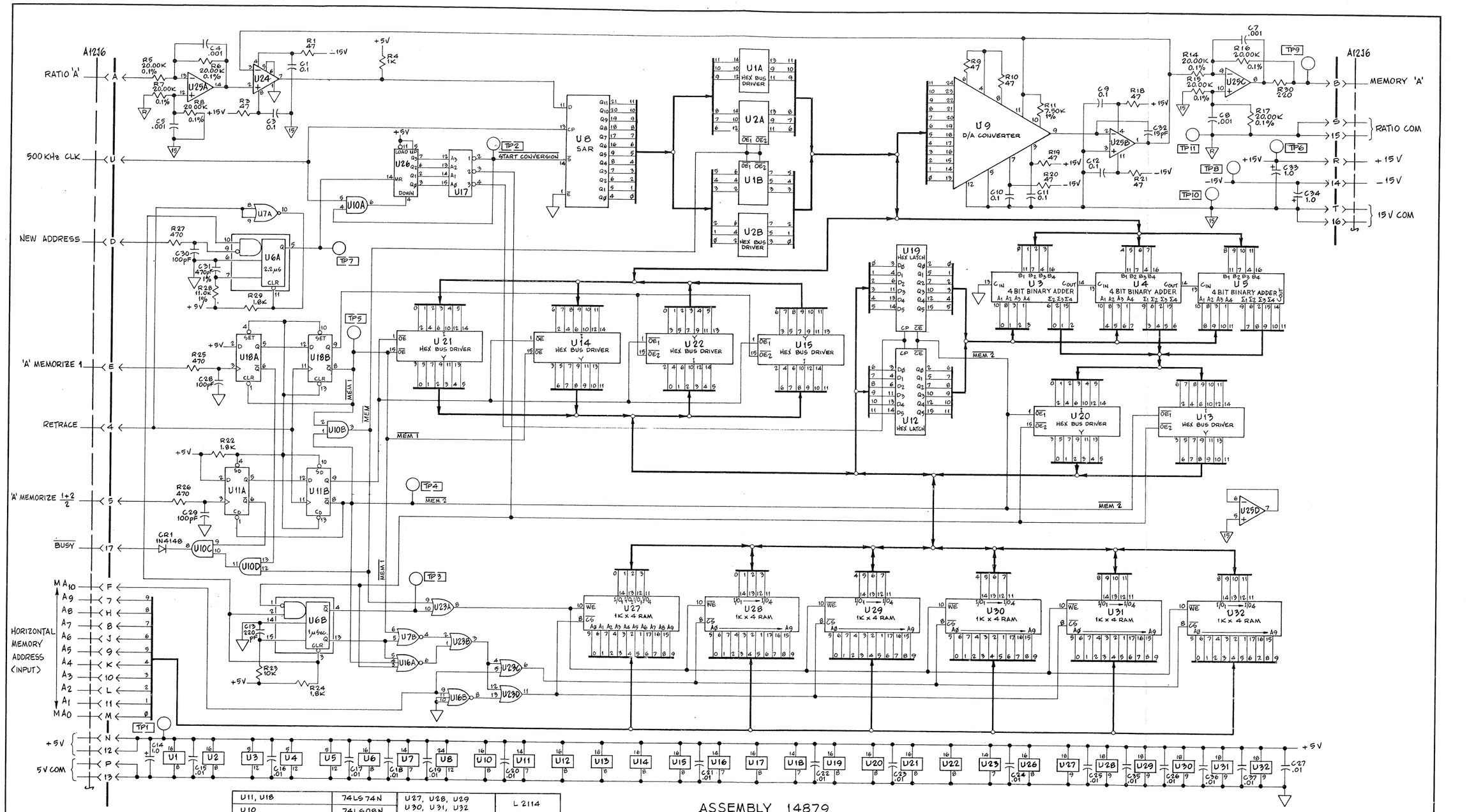


FIGURE 8-9 A CHANNEL MEMORY PCB ASSEMBLY

CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	C-7	R15	B-6	U25	C-5
C2	---	R16	D-6	U26	D-6
C3	C-6	R17	B-6	U27	E-6
C4	D-5	R18	B-6	U28	F-6
C5	C-6	R19	B-3	U29	G-6
C6	---	R20	B-5	U30	H-6
C7	C-6	R21	B-5	U31	I-6
C8	C-6	R22	F-3	U32	J-6
C9	C-5	R23	J-2		
C10	C-4	R24	I-2		
C11	C-3	R25	E-7		
C12	C-5	R26	E-7		
C13	J-2	R27	J-4		
C14	F-7	R28	I-2		
C15	D-2	R29	J-2		
C16	F-2	R30	C-6		
C17	I-2				
C18	K-2				
C19	B-3	TP1	B-1		
C20	E-4	TP2	C-2		
C21	K-3	TP3	H-2		
C22	F-4	TP4	H-2		
C23	H-4	TP5	J-2		
C24	K-4	TP6	B-3		
C25	F-6	TP7	I-4		
C26	H-6	TP8	B-5		
C27	K-6	TP9	D-7		
C28	E-4	TP10	D-7		
C29	E-3	TP11	D-7		
C30	J-2	TP12	B-2		
C31	I-2				
C32	C-5				
C33	D-7	U1	C-2		
C34	D-7	U2	D-2		
C35	G-6	U3	E-2		
C36	I-6	U4	F-2		
C37	J-6	U5	G-2		
		U6	I-2		
		U7	J-2		
CR1	F-5	U8	B-4		
		U9	C-4		
		U10	D-3		
R1	C-7	U11	E-3		
R2	---	U12	F-3		
R3	B-7	U13	G-3		
R4	C-7	U14	H-3		
R5	B-7	U15	I-3		
R6	B-7	U16	J-3		
R7	B-7	U17	D-5		
R8	B-6	U18	E-5		
R9	C-3	U19	F-5		
R10	C-3	U20	G-5		
R11	C-5	U21	H-5		
R12	---	U22	I-5		
R13	---	U23	J-5		
R14	D-6	U24	C-7		



U11, U18	74LS74N	U27, U28, U29 U30, U31, U32	L 2114
U10	74LS08N	U26	74LS193N
U9	AD565JD	U25	TL074CN
U8	DM2504N	U24	LM311N
U7	74LS33N	U23	74LS32N
U6	74LS123N	U17	74LS42N
U3, U4, U5	74LS83N	U16	74LS27N
U1, U2, U13, U14 U15, U20, U21, U22	74LS365N	U12, U19	74LS378N
REF DESIG	TYPE	REF DESIG	TYPE

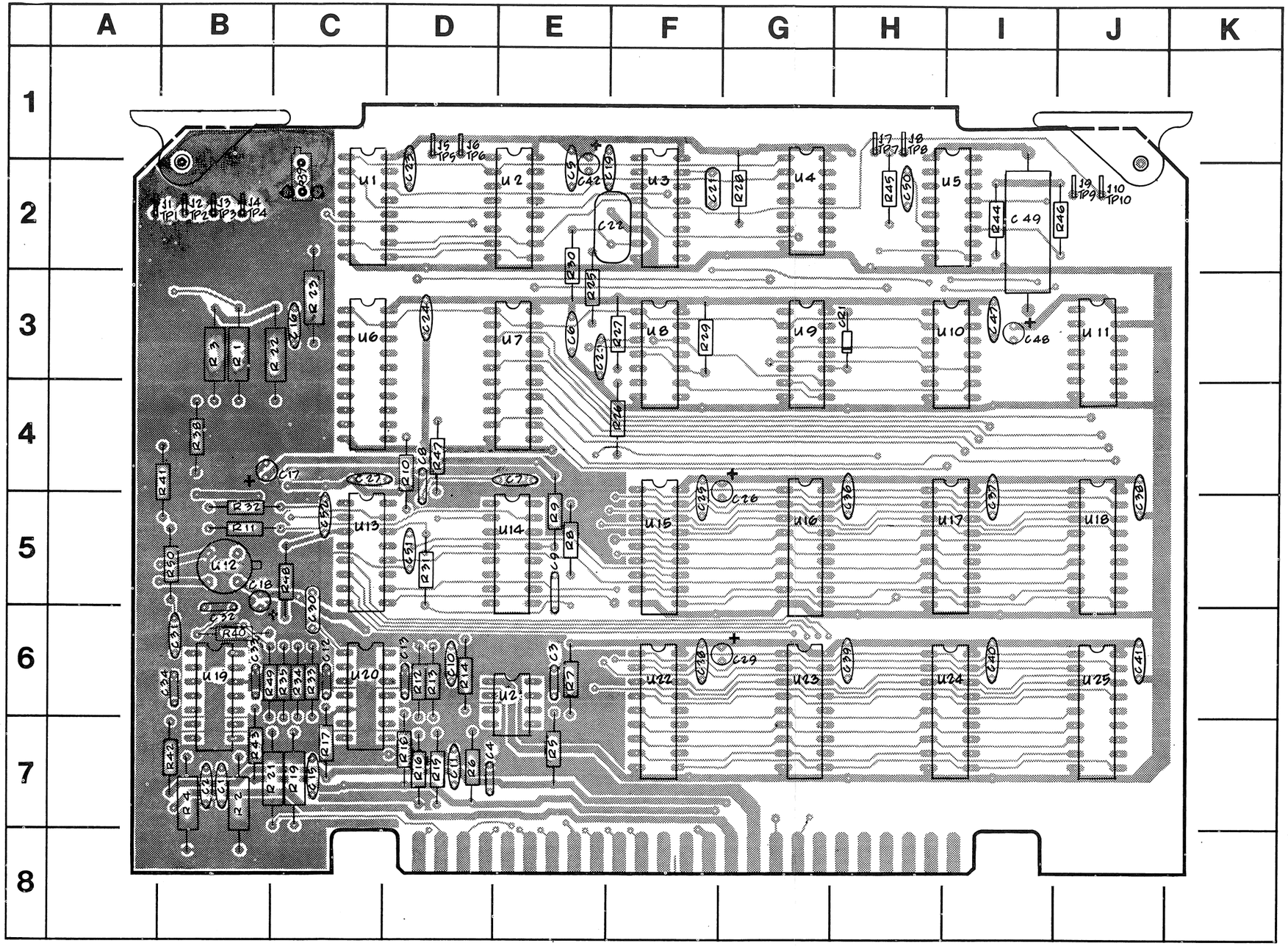
ASSEMBLY 14879

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A6

NOTES: 1. UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W AND CAPACITOR VALUES ARE IN MICROFARADS.

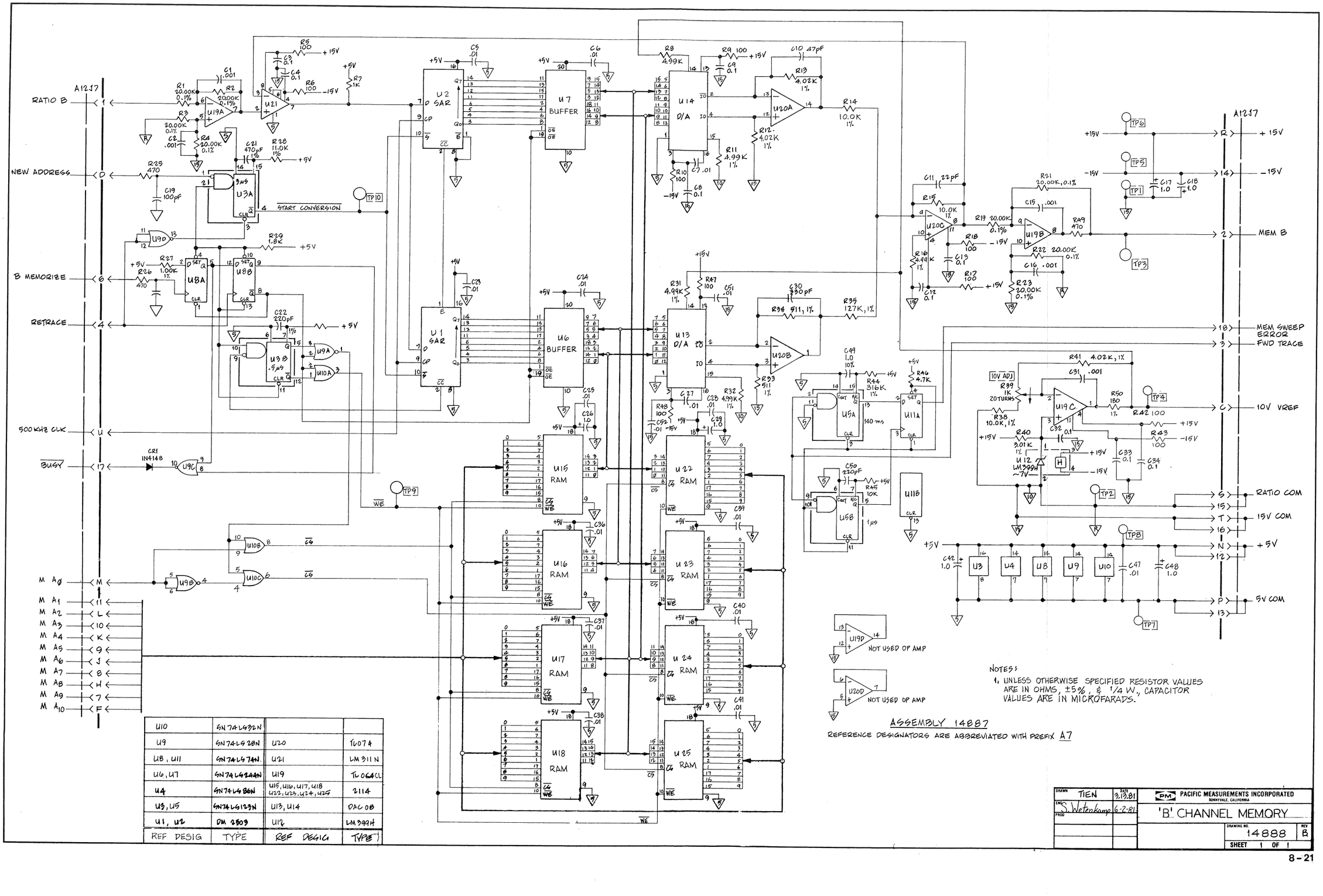
2. ▽ IS 5V COM.

DRAWN TIEN	DATE 1.5.81	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
ENG S. Wetenkamp	6-2-81	'A' CHANNEL MEMORY	
PROD		DRAWING NO. 14880	REV B
		SHEET 1 OF 1	



CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	B-7	C48	I-2	R30	E-2	U1	C-2
C2	B-7	C49	I-2	R31	D-5	U2	E-2
C3	E-6	C50	H-2	R32	B-5	U3	F-2
C4	D-7	C51	D-5	R33	C-6	U4	G-2
C5	E-2	C52	C-5	R34	C-6	U5	I-2
C6	E-3			R35	C-6	U6	C-3
C7	E-4			R36	---	U7	E-3
C8	D-4			R37	---	U8	F-3
C9	E-5			R38	B-4	U9	G-3
C10	D-6			R39	C-2	U10	I-3
C11	D-7			R40	B-6	U11	J-3
C12	C-6	CR1	H-3	R41	B-4	U12	B-5
C13	D-6			R42	B-7	U13	C-5
C14	---			R43	B-7	U14	E-5
C15	C-7			R44	I-2	U15	F-5
C16	C-3			R45	H-2	U16	G-5
C17	B-4			R46	J-2	U17	I-5
C18	B-5			R47	D-4	U18	J-5
C19	F-2	R1	B-3	R48	C-5	U19	B-6
C20	E-3	R2	B-7	R49	C-6	U20	C-6
C21	F-2	R3	B-3	R50	B-5	U21	E-6
C22	F-2	R4	B-7			U22	F-6
C23	D-2	R5	E-7			U23	G-6
C24	D-3	R6	D-7			U24	I-6
C25	F-5	R7	E-6			U25	J-6
C26	G-5	R8	E-5				
C27	C-4	R9	E-5				
C28	F-6	R10	D-4				
C29	G-6	R11	B-5				
C30	C-6	R12	D-6				
C31	B-6	R13	D-6	TP1	A-2		
C32	B-6	R14	D-6	TP2	B-2		
C33	B-6	R15	D-7	TP3	B-2		
C34	B-6	R16	D-7	TP4	B-2		
C35	---	R17	C-7	TP5	D-1		
C36	H-5	R18	D-7	TP6	D-1		
C37	I-5	R19	C-7	TP7	H-1		
C38	J-5	R20	---	TP8	H-1		
C39	H-6	R21	C-7	TP9	J-2		
C40	I-6	R22	C-3	TP10	J-2		
C41	J-6	R23	C-3				
C42	E-2	R24	---				
C43	---	R25	E-3				
C44	---	R26	F-4				
C45	---	R27	F-3				
C46	---	R28	G-2				
C47	I-3	R29	F-3				

FIGURE 8-10 B CHANNEL MEMORY PCB ASSEMBLY



U10	SN74LS32N	U20	TL074
U9	SN74LS28N	U21	LM311N
U8, U11	SN74LS74N	U19	TL064CL
U6, U7	SN74LS244N	U15, U16, U17, U18 U22, U23, U24, U25	2114
U4	SN74LS86N	U13, U14	DAC08
U3, U5	SN74LS123N	U12	LM399H
U1, U2	DM 2503		

REF DESIG	TYPE	REF DESIG	TYPE

NOTES:
1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, ±5%, & 1/4 W., CAPACITOR VALUES ARE IN MICROFARADS.

ASSEMBLY 14887

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A7

DRAWN TIEN	DATE 9.19.81	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
ENG S. Wetenkamp	6-2-81	'B' CHANNEL MEMORY	
PROD		DRAWING NO. 14888	REV B
		SHEET 1 OF 1	

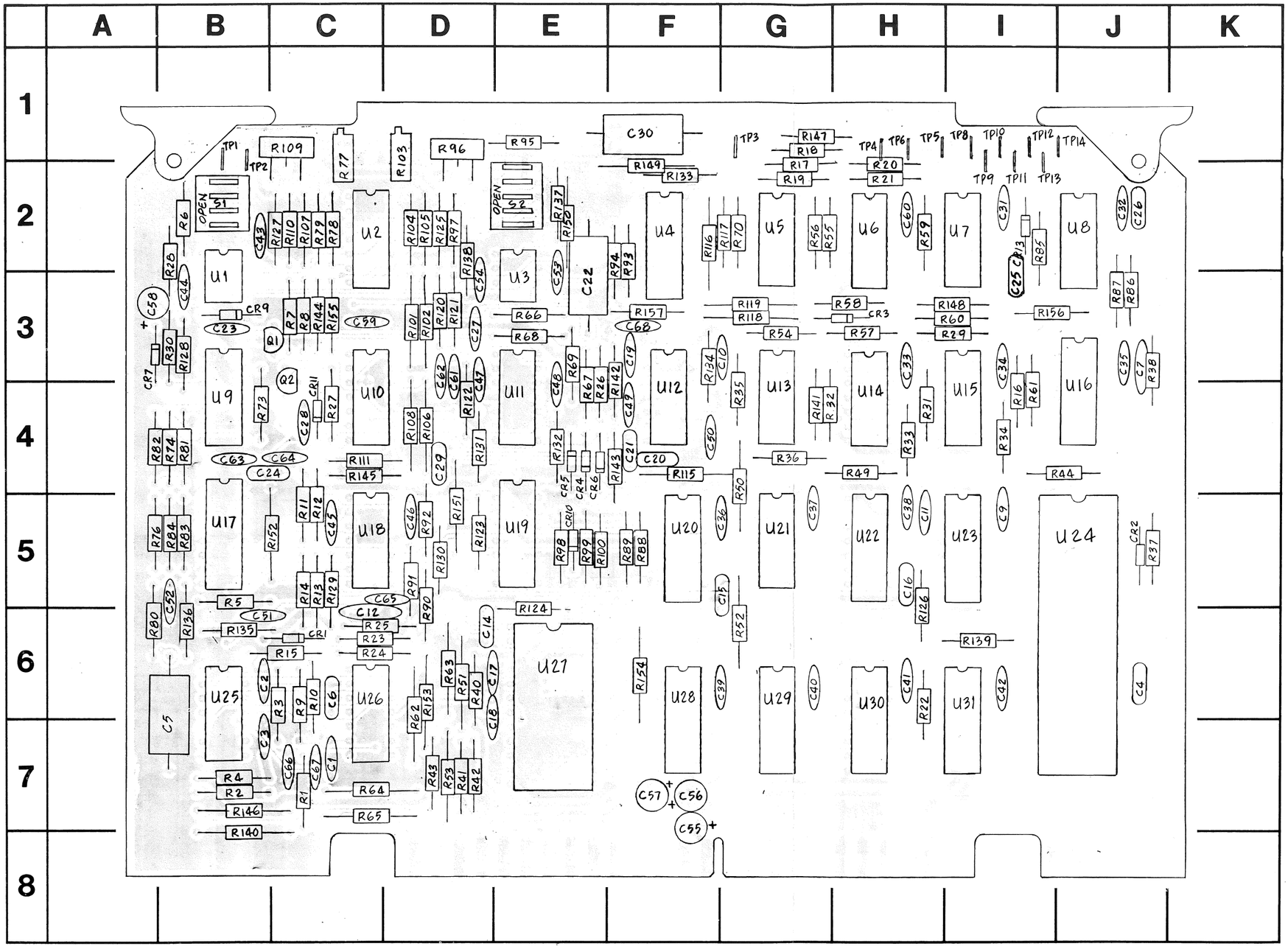
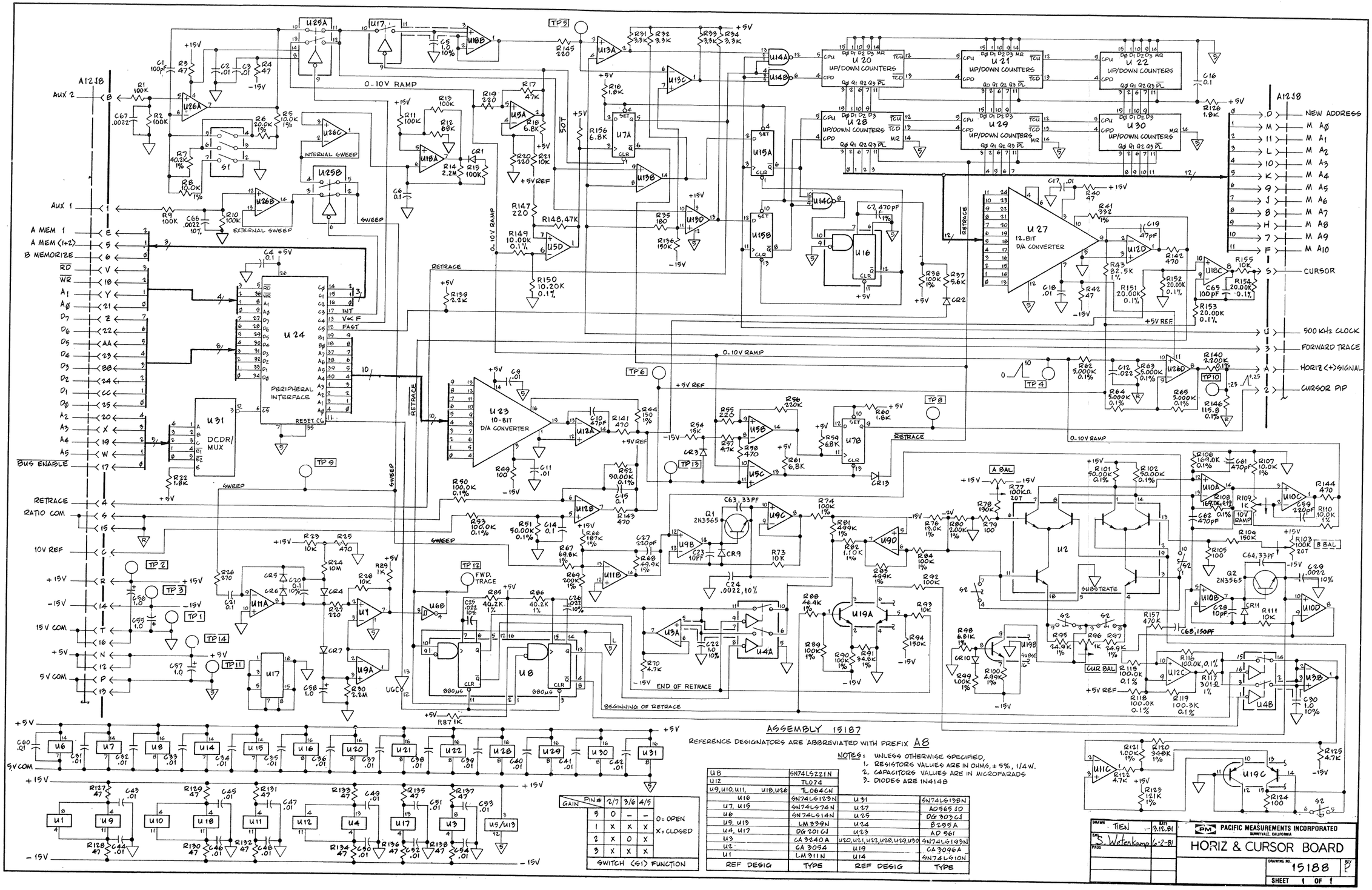


FIGURE 8-11 HORIZONTAL AND CURSOR PCB ASSEMBLY

CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	C-7	C58	B-3	R18	G-1	R75	---
C2	B-6	C59	C-3	R19	G-2	R76	A-5
C3	B-7	C60	H-2	R20	H-2	R77	C-1
C4	J-6	C61	D-4	R21	H-2	R78	C-2
C5	B-7	C62	D-4	R22	H-6	R79	C-2
C6	C-6	C63	B-4	R23	C-6	R80	A-6
C7	J-3	C64	C-4	R24	C-6	R81	B-4
C8	---	C65	D-4	R25	C-6	R82	A-4
C9	I-5	C66	C-7	R26	E-4	R83	B-5
C10	G-4	C67	C-7	R27	C-4	R84	B-5
C11	H-5	C68	F-3	R28	B-2	R85	I-2
C12	C-6			R29	I-3	R86	J-3
C13	---			R30	B-3	R87	J-3
C14	D-6			R31	H-4	R88	F-5
C15	G-5			R32	H-4	R89	F-5
C16	H-5			R33	H-4	R90	D-5
C17	D-6			R34	I-4	R91	D-5
C18	D-7			R35	G-4	R92	D-5
C19	F-3			R36	G-4	R93	F-2
C20	F-4			R37	J-5	R94	F-2
C21	F-4			R38	J-3	R95	E-1
C22	E-2	CR1	C-6	R39	---	R96	D-1
C23	B-3	CR2	J-5	R40	D-6	R97	D-2
C24	C-4	CR3	H-3	R41	D-7	R98	E-5
C25	I-3	CR4	E-4	R42	D-7	R99	E-5
C26	J-2	CR5	E-4	R43	D-7	R100	E-5
C27	D-3	CR6	E-4	R44	J-4	R101	D-3
C28	C-4	CR7	A-3	R45	---	R102	D-3
C29	D-4	CR8	---	R46	---	R103	D-1
C30	F-2	CR9	B-3	R47	---	R104	D-2
C31	I-2	CR10	E-5	R48	---	R105	D-2
C32	J-2	CR11	C-4	R49	H-4	R106	D-4
C33	H-3	CR12	---	R50	G-4	R107	C-2
C34	I-3	CR13	I-2	R51	D-6	R108	D-4
C35	J-3			R52	G-6	R109	C-1
C36	G-5			R53	D-7	R110	C-2
C37	G-5	Q1	C-3	R54	G-3	R111	C-4
C38	H-5	Q2	C-4	R55	G-2	R112	---
C39	G-6			R56	G-2	R113	---
C40	G-6			R57	H-3	R114	---
C41	H-6	R1	C-7	R58	H-3	R115	F-4
C42	I-6	R2	B-7	R59	H-2	R116	F-2
C43	B-2	R3	C-6	R60	I-3	R117	G-2
C44	B-3	R4	B-7	R61	I-4	R118	G-3
C45	C-5	R5	B-5	R62	D-7	R119	G-3
C46	D-5	R6	B-2	R63	D-6	R120	D-3
C47	D-4	R7	C-3	R64	C-7	R121	D-3
C48	E-4	R8	C-3	R65	C-7	R122	D-4
C49	F-4	R9	C-6	R66	E-3	R123	D-5
C50	F-4	R10	C-6	R67	E-4	R124	E-6
C51	B-6	R11	C-5	R68	E-3	R125	D-2
C52	B-5	R12	C-5	R69	E-3	R126	H-5
C53	E-3	R13	C-5	R70	G-2	R127	C-2
C54	D-3	R14	C-5	R71	---	R128	B-3
C55	F-7	R15	C-6	R72	---	R129	C-5
C56	F-7	R16	I-4	R73	C-4	R130	D-5
C57	F-7	R17	G-2	R74	B-4	R131	D-4



ASSEMBLY 15187

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A8

NOTES:
1. UNLESS OTHERWISE SPECIFIED,
2. RESISTORS VALUES ARE IN OHMS, ± 5%, 1/4 W.
3. CAPACITORS VALUES ARE IN MICROFARADS
4. DIODES ARE IN4148

REF DESIG	TYPE	REF DESIG	TYPE
U8	6N74LS221N		
U12	TL074		
U9, U10, U11, U18, U26	TL064CN		
U16	6N74LS123N	U31	6N74LS138N
U7, U13	6N74LS74N	U27	AD565 SD
U6	6N74LS14N	U25	DG 303 CJ
U5, U13	LM339N	U24	8255A
U4, U17	DG 201 CJ	U23	AD 561
U3	CA 3240 A	U20, U21, U22, U28, U29, U30	6N74LS193N
U2	CA 3054	U19	CA 3096A
U1	LM 311N	U14	6N74LS10N

GAIN \ PIN #	2/7	3/6	4/5
5	0	–	–
1	X	X	X
2	X	0	X
3	X	X	X

SWITCH (S1) FUNCTION

0 = OPEN
X = CLOSED

DRAWN	TIEN	DATE	3.12.81
ENG	S. Wetenkamp		6-2-81
PROD			

PACIFIC MEASUREMENTS INCORPORATED
SUNNYVALE, CALIFORNIA

HORIZ & CURSOR BOARD

DRAWING NO. 15188 REV P
SHEET 1 OF 1

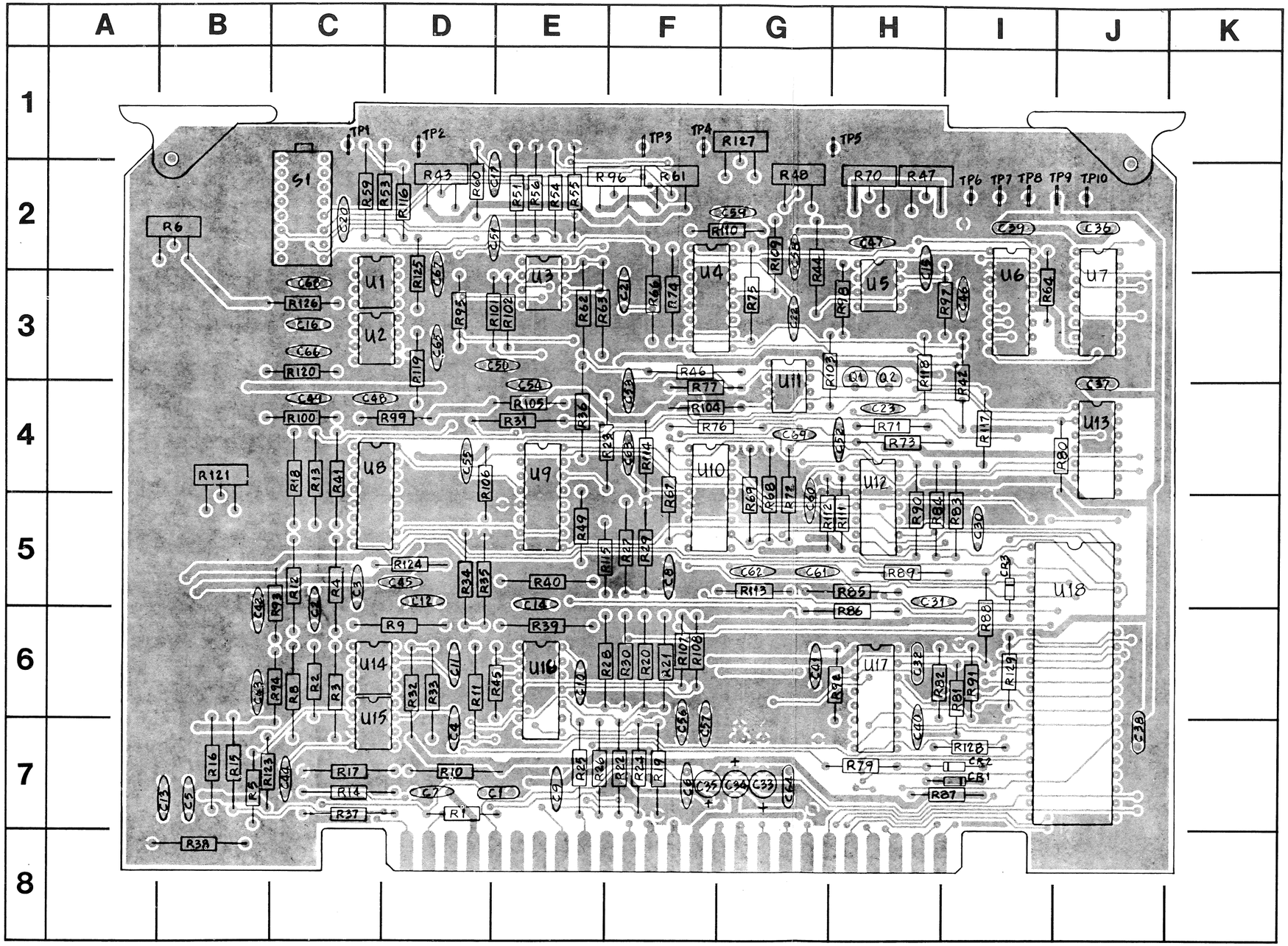


FIGURE 8-12 CRT DISPLAY PCB ASSEMBLY

CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC	CKT REF	GRID LOC
C1	E-7	C57	G-7	R34	D-5	R90	H-5
C2	C-6	C58	G-2	R35	D-5	R91	I-6
C3	C-5	C59	G-2	R36	E-4	R92	H-6
C4	D-7	C60	G-5	R37	C-7	R93	C-6
C5	B-7	C61	G-5	R38	B-8	R94	C-6
C6	F-7	C62	G-5	R39	E-6	R95	D-3
C7	D-7	C63	F-4	R40	E-5	R96	F-2
C8	F-5	C64	G-7	R41	C-4	R97	I-3
C9	E-7	C65	D-3	R42	I-4	R98	H-3
C10	E-6	C66	C-3	R43	D-2	R99	D-4
C11	D-6	C67	D-3	R44	G-2	R100	C-4
C12	D-6	C68	C-3	R45	E-6	R101	E-3
C13	B-7	C69	G-4	R46	F-3	R102	E-3
C14	E-6			R47	H-2	R103	H-3
C15	H-2			R48	G-2	R104	F-4
C16	C-3	CR1	I-7	R49	E-5	R105	E-4
C17	E-2	CR2	I-7	R50	---	R106	D-5
C18	---	CR3	I-5	R51	E-2	R107	F-6
C19	---			R52	---	R108	F-6
C20	C-2	Q1	H-3	R53	D-2	R109	G-2
C21	F-3	Q2	H-3	R54	E-2	R110	G-2
C22	G-3			R55	E-2	R111	H-5
C23	H-4			R56	E-2	R112	H-5
C24	---	R1	D-7	R57	---	R113	G-5
C25	---	R2	C-6	R58	---	R114	F-4
C26	---	R3	C-6	R59	C-2	R115	F-5
C27	---	R4	C-5	R60	D-2	R116	D-2
C28	---	R5	B-7	R61	F-2	R117	I-4
C29	---	R6	B-2	R62	E-3	R118	H-3
C30	I-5	R7	---	R63	F-4	R119	D-3
C31	I-5	R8	C-6	R64	J-3	R120	C-3
C32	H-6	R9	D-6	R65	---	R121	B-4
C33	G-7	R10	D-7	R66	F-3	R122	---
C34	G-7	R11	D-6	R67	F-5	R123	C-7
C35	F-7	R12	C-5	R68	G-5	R124	D-5
C36	J-2	R13	C-4	R69	G-5	R125	D-3
C37	J-3	R14	C-7	R70	H-2	R126	C-3
C38	J-7	R15	B-7	R71	H-4	R127	G-1
C39	I-2	R16	B-7	R72	G-5	R128	I-7
C40	H-7	R17	C-7	R73	H-4	R129	I-6
C41	G-6	R18	C-4	R74	F-3	S1	C-2
C42	B-6	R19	F-7	R75	G-3		
C43	B-6	R20	F-6	R76	F-4	TP1	C-1
C44	C-7	R21	F-6	R77	F-4	TP2	D-1
C45	D-5	R22	F-7	R78	---	TP3	F-1
C46	I-3	R23	F-4	R79	H-7	TP4	F-1
C47	H-2	R24	F-7	R80	J-4	TP5	H-1
C48	D-4	R25	E-7	R81	I-6	TP6	I-2
C49	C-4	R26	F-7	R82	I-6	TP7	I-2
C50	E-3	R27	F-5	R83	I-5	TP8	I-2
C51	E-2	R28	F-6	R84	H-5	TP9	J-2
C52	H-4	R29	F-5	R85	H-5	TP10	J-2
C53	F-4	R30	F-6	R86	H-6		
C54	E-4	R31	E-4	R87	I-7		
C55	D-4	R32	D-6	R88	I-6	U1	C-3
C56	F-7	R33	D-6	R89	H-5	U2	C-3

ASSEMBLY 15330

REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A9 / A10

REF DESIG	TYPE
U18	8259A
U17	DAC-08EQ
U14, U15	TL062
U13	SN74LS86N
U12, U16	TL064CN
U7	SN74LS138N
U6	AD7542AD
U4, U8, U9, U10	DG201CJ
U1, U2, U3, U5, U11	OP-07CP

NOTES:
1. UNLESS OTHERWISE SPECIFIED, RESISTORS VALUES ARE IN OHMS, ±0.1%, 1/4 W AND CAPACITORS VALUES ARE IN MICROFARADS.
2. ⏚ ARE 15V COM.

DRAWN	TIEN	9.3.81	PACIFIC MEASUREMENTS INCORPORATED, SUNNYVALE, CALIFORNIA
ENG	S. Wetenkamp	6-281	CRT DISPLAY
PROD			DRAWING NO. 15331, REV J
			SHEET 1 OF 1

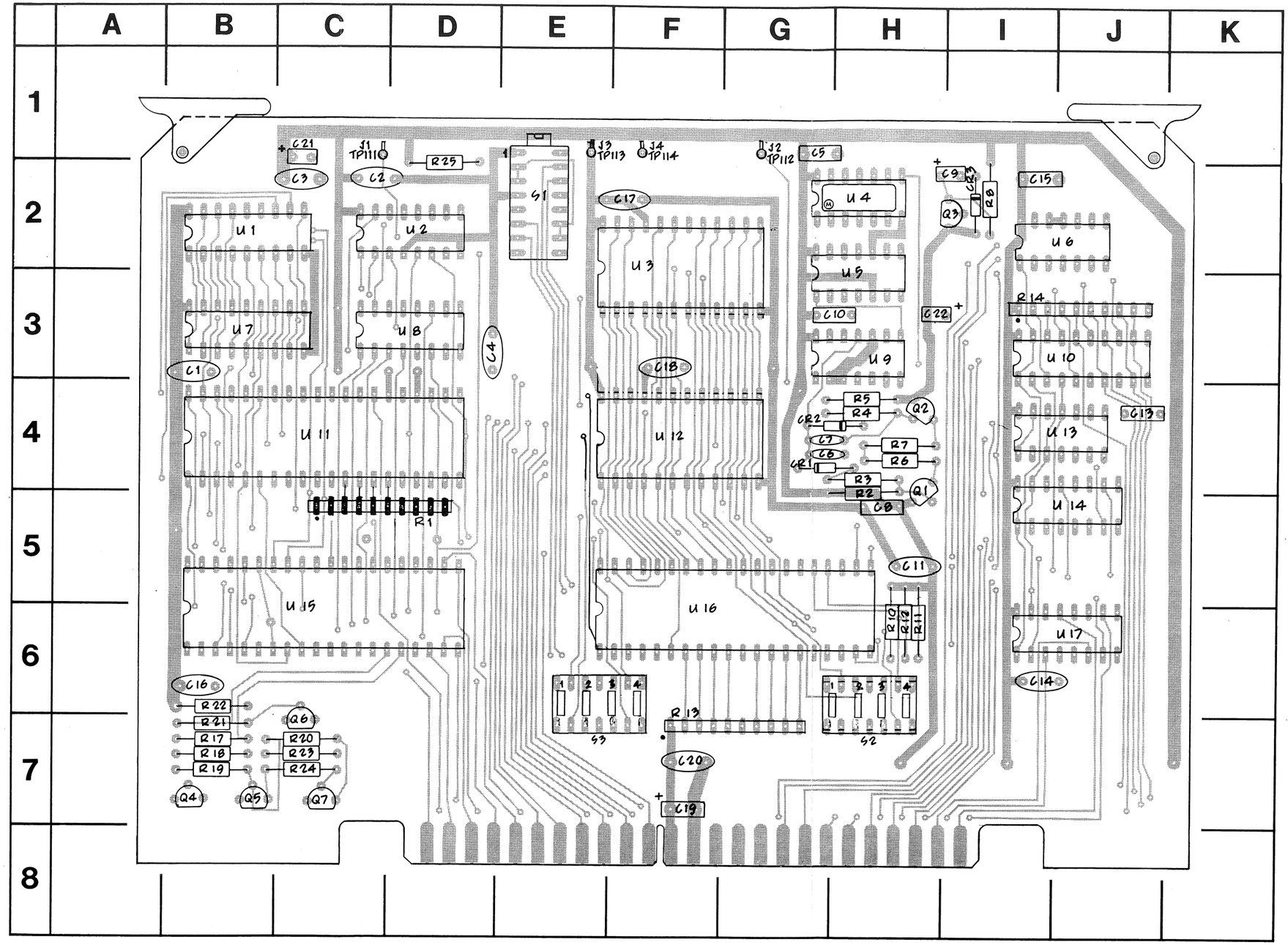


FIGURE 8-13 CPU PCB ASSEMBLY

CKT REF	GRID LOC
C1	B-3
C2	C-2
C3	C-2
C4	D-3
C5	G-2
C6	G-4
C7	G-4
C8	H-5
C9	I-2
C10	G-3
C11	H-5
C12	---
C13	J-4
C14	I-6
C15	I-2
C16	B-6
C17	F-2
C18	F-3
C19	F-7
C20	F-7
C21	C-1
C22	H-3
CR1	G-4
CR2	G-4
CR3	I-2
J1	C-1
J2	G-1
J3	E-1
J4	F-1
Q1	H-5
Q2	H-4
Q3	I-2
Q4	B-7
Q5	C-7
Q6	C-7
Q7	C-7
R1	C-5
R2	H-5
R3	H-5
R4	H-4
R5	H-4
R6	H-4
R7	H-4
R8	I-2
R9	---
R10	H-6
R11	H-6
R12	H-6
R13	G-7
R14	J-3
R15	---
R16	---
R17	B-7
R18	B-7
R19	B-7
R20	C-7
R21	B-7
R22	B-7
R23	C-7
R24	C-7
R25	D-2
S1	E-2
S2	H-6
S3	E-6
TP111	C-1
TP112	G-1
TP113	E-1
TP114	F-1
U1	B-2
U2	D-2
U3	F-3
U4	H-2
U5	H-3
U6	J-2
U7	B-3
U8	D-3
U9	H-3
U10	J-3
U11	C-4
U12	F-4
U13	J-4
U14	J-5
U15	C-6
U16	G-6
U17	J-6

REF. DESIG.	TYPE
U16	Z 80 CPU
U15	8255A
U14, U17	8216
U13	74LS32N
U11	Z80 PIO
U10	74LS244N
U6	74LS14N
U5, U9	74LS93
U4	K1148
U3, U12	2732
U2, U8	74LS138N
U1, U7	P2114

U6: 1 SPARE GATE

ASSEMBLY 14963
REFERENCE DESIGNATORS ARE ABBREVIATED WITH PREFIX A11

NOTE: UNLESS OTHERWISE SPECIFIED, RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W AND CAPACITOR VALUES ARE IN MICROFARADS.

DRAWN TIEN	DATE 8.19.80	PACIFIC MEASUREMENTS INCORPORATED SUNNYVALE, CALIFORNIA	
ENG S. Wetenkamp	6-2-81	CPU BOARD	
PROD		DRAWING NO. 14964	REV B
		SHEET 1 OF 1	

SECTION 9

REPLACEABLE PARTS LIST

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
		CHASSIS ASSEMBLY-14719
A1	14950	Digital Display Driver PCB Assy
A2	14953	Digital Display/Calibrator PCB Assy
A3	15834	Input Preamp & Log PCB Assy
A4	15834	Input Preamp & Log PCB Assy
A5	15227	Ref Channel Preamp & Log PCB Assy
A6	14879	'A' Channel Memory PCB Assy
A7	14887	'B' Channel Memory PCB Assy
A8	15187	Horizontal & Cursor PCB Assy
A9	15330	CRT Display Driver PCB Assy
A10	15330	CRT Display Driver PCB Assy
A11	14963	CPU PCB Assy
A12	15005	Interconnect PCB Assy
A13	14968	Front Panel PCB Assy
A14	15023	Horizontal Finger PCB Assy
A15	15064	'A' Channel Finger PCB Assy
C1	11501-2	Ceramic 0.1µF ±20% 50V
C2	11501-2	Ceramic 0.1µF ±20% 50V
C3	11501-2	Ceramic 0.1µF ±20% 50V
J3	13257	Audio 7 Pin
J4	13257	Audio 7 Pin
J5	13257	Audio 7 Pin
R1	11676-1	Variable 100KΩ ±20% 1/2W
R2	11676-1	Variable 100KΩ ±20% 1/2W
W1	15129	Cable Assy
W2	15130	Cable Assy
W3	15165	Cable Assy
W4	15166	Cable Assy
W5	15156	Cable Assy
W6	15157	Cable Assy
W7	15132	Cable Assy
W8	13289	RF Cable Assy
		DIGITAL DISPLAY DRIVER PC BOARD ASSEMBLY-14950
A1C1	10787-2	Tantalum 12µF ±20% 20V
A1C2	10000-11	Ceramic .01µF ±20% 100V
A1C3	11501-2	Ceramic 0.1µF ±20% 50V
A1C4	11501-2	Ceramic 0.1µF ±20% 50V
A1C5	10000-8	Ceramic .022µF ±20% 500V
A1C6	10000-11	Ceramic .01µF ±20% 100V
A1C7	--------	Not Used
A1C8	11501-2	Ceramic 0.1µF ±20% 50V
A1C9	10787-11	Tantalum 1.0µF ±20% 35V
A1C10	10000-11	Ceramic .01µF ±20% 100V
A1C11	10000-11	Ceramic .01µF ±20% 100V
A1C12	--------	Not Used
A1C13	11501-2	Ceramic 0.1µF ±20% 50V
A1C14	10000-11	Ceramic .01µF ±20% 100V
A1C15	11501-2	Ceramic 0.1µF ±20% 50V
A1C16	11501-2	Ceramic 0.1µF ±20% 50V
A1C17	11501-2	Ceramic 0.1µF ±20% 50V
A1C18	10000-11	Ceramic .01µF ±20% 100V
A1C19	10000-11	Ceramic .01µF ±20% 100V
A1C20	--------	Not Used
A1C21	10000-11	Ceramic .01µF ±20% 100V
A1C22	10000-11	Ceramic .01µF ±20% 100V
A1C23	10000-11	Ceramic .01µF ±20% 100V
A1C24	10000-11	Ceramic .01µF ±20% 100V
A1C25	10000-11	Ceramic .01µF ±20% 100V
A1C26	10787-2	Tantalum 12µF ±20% 20V
A1C27	10000-11	Ceramic .01µF ±20% 100V
A1C28	10000-4	Ceramic .001µF ±20% 1000V
A1C29	10000-11	Ceramic .01µF ±20% 100V
A1C30	10000-11	Ceramic .01µF ±20% 100V
A1C31	10000-11	Ceramic .01µF ±20% 100V
A1C32	10000-11	Ceramic .01µF ±20% 100V
A1C33	11501-2	Ceramic 0.1µF ±20% 50V
A1J1	14514-1	Post .025 Square
A1J2	14514-1	Post .025 Square
A1J3	14320-2	Test Jack
A1J4	14320-2	Test Jack
A1J5	14320-2	Test Jack
A1J6	14320-2	Test Jack
A1J7	14320-2	Test Jack
A1R1	10013-81	Carbon Film 4.3KΩ ±5% 1/4W
A1R2	10013-37	Carbon Film 10KΩ ±5% 1/4W
A1R3	--------	Not Used
A1R4	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A1R5	15098-1	Network 1K ±2% 125mW
A1R6	15098-1	Network 1K ±2% 125mW
A1R7	14881-3	Network 33Ω ±2% 125mW
A1R8	14881-3	Network 33Ω ±2% 125mW
A1R9	10013-31	Carbon Film 3.3K ±5% 1/4W
A1U1	15101	DS3611N
A1U2	15101	DS3611N
A1U3	15101	DS3611N
A1U4	15101	DS3611N
A1U5	15101	DS3611N
A1U6	15101	DS3611N
A1U7	15101	DS3611N
A1U8	15101	DS3611N
A1U9	15101	DS3611N
A1U10	15101	DS3611N
A1U11	15100	CA3082
A1U12	15100	CA3082
A1U13	15101	DS3611N
A1U14	15101	DS3611N
A1U15	13470-44	SN74LS138N
A1U16	13470-44	SN74LS138N
A1U17	13470-44	SN74LS138N
A1U18	13470-42	SN74LS365N
A1U19	15175	MCM6810P
A1U20	13871	LM555CN
A1U21	13470-48	SN74LS93N
A1U22	13470-48	SN74LS93N
A1U23	13470-2	SN74LS01N
A1U24	14641	8255A
A1U25	14641	8255A
A1U26	13470-13	SN74LS74N
A1U27	13470-5	SN74LS08N
A1U28	13470-13	SN74LS74N
A1U29	13470-44	SN74LS138N
		DISPLAY/CALIBRATOR PC BOARD ASSEMBLY-14953
A2C1	10000-4	Ceramic .001µF ±20% 1000V
A2C2	10000-11	Ceramic .01µF ±20% 100V
A2C3	10000-11	Ceramic .01µF ±20% 100V
A2C4	10000-4	Ceramic .001µF ±20% 1000V
A2C5	13979-1	Polycarbonate 1.0µF ±10% 200V
A2C6	11501-2	Ceramic 0.1µF ±20% 50V

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A2C7	11501-2	Ceramic	0.1µF	±20%	50V
A2C8	11501-2	Ceramic	0.1µF	±20%	50V
A2C9	10011-2	Mylar	1.0µF	±10%	200V
A2C10	11501-2	Ceramic	0.1µF	±20%	50V
A2C11	10011-2	Mylar	1.0µF	±10%	200V
A2C12	10007-8	Mylar	.22µF	±10%	200V
A2C13	11501-2	Ceramic	0.1µF	±20%	50V
A2C14	11501-2	Ceramic	0.1µF	±20%	50V
A2C15	11501-2	Ceramic	0.1µF	±20%	50V
A2C16	11501-2	Ceramic	0.1µF	±20%	50V
A2C17	10000-4	Ceramic	.001µF	±20%	1000V
A2C18	10000-4	Ceramic	.001µF	±20%	1000V
A2C19	10000-11	Ceramic	.01µF	±20%	100V
A2C20	10000-11	Ceramic	.01µF	±20%	100V
A2C21	13979-1	Polycarbonate	1.0µF	±10%	200V
A2C22	10000-11	Ceramic	.01µF	±20%	100V
A2C23	10000-11	Ceramic	.01µF	±20%	100V
A2C24	11501-2	Ceramic	0.1µF	±20%	50V
A2C25	11501-2	Ceramic	0.1µF	±20%	50V
A2C26	11501-2	Ceramic	0.1µF	±20%	50V
A2C27	10011-2	Mylar	1.0µF	±10%	200V
A2C28	11501-2	Ceramic	0.1µF	±20%	50V
A2C29	10011-2	Mylar	1.0µF	±10%	200V
A2C30	10787-11	Tantalum	1.0µF	±20%	35V
A2C31	10787-11	Tantalum	1.0µF	±20%	35V
A2C32	10787-11	Tantalum	1.0µF	±20%	35V
A2C33	10007-8	Mylar	.22µF	±10%	200V
A2C34	11501-2	Ceramic	0.1µF	±20%	50V
A2C35	11501-2	Ceramic	0.1µF	±20%	50V
A2C36	10000-11	Ceramic	.01µF	±20%	100V
A2C37	10000-11	Ceramic	.01µF	±20%	100V
A2C38	10000-11	Ceramic	.01µF	±20%	100V
A2C39	10585-4	Ceramic	680pF	±5%	1000V
A2C40	10677-12	Mica	390pF	±5%	500V
A2C41	10677-10	Mica	130pF	±5%	500V
A2C42	10000-11	Ceramic	.01µF	±20%	100V
A2C43	10001-6	Ceramic	47pF	±5%	1000V
A2C44	10000-11	Ceramic	.01µF	±20%	100V
A2C45	10585-5	Ceramic	.001µF	±5%	1000V
A2C46	10000-1	Ceramic	100pF	±20%	1000V
A2C47	10909-11	Mica	62pF	±1%	500V
A2C48	10909-12	Mica	120pF	±1%	500
A2C49	--------	Not Used			
A2C50	10909-11	Mica	62pF	±1%	500V
A2C51	10000-6	Ceramic	0047µF	±20%	500V
A2C52	10001-1	Ceramic	2.2pF	±5%	1000V
A2C53	10000-4	Ceramic	.001µF	±20%	1000V
A2CR1	10043	1N4148			
A2CR2	10043	1N4148			
A2CR3	10043	1N4148			
A2CR4	10043	1N4148			
A2CR5	10043	1N4148			
A2CR6	10045	1N823			
A2CR7	11345	HPA2900			
A2CR8	10043	1N4148			
A2J1	14514-1	Post .025 Square			
A2J2	14514-1	Post .025 Square			
A2J3	15112	SMB, Coaxial			
A2J4	14320-2	Test Jack			
A2J5	14320-2	Test Jack			
A2J6	14320-2	Test Jack			
A2J7	14320-2	Test Jack			
A2J8	14320-2	Test Jack			
A2J9	14320-2	Test Jack			
A2J10	14320-2	Test Jack			
A2J11	14320-2	Test Jack			
A2J12	14320-2	Test Jack			

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A2J13	14514-1	Post .025 Square			
A2L1	15292	R.F. .12µH 3.5 Turns			
A2L2	15293	R.F. .17µH 13.5 Turns			
A2L3	15293	R.F. .17µH 13.5 Turns			
A2Q1	10018	2N3646			
A2Q2	10017	2N3569			
A2Q3	11119	2N4250			
A2R1	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R2	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R3	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R4	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R5	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R6	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R7	10015-195	Metal Film 200Ω		±1%	1/8W
A2R8	10013-49	Carbon Film 100KΩ		±5%	1/4W
A2R9	13584-7	Variable Comp. 100KΩ		±20%	1/2W
A2R10	-------	Not Used			
A2R11	-------	Not Used			
A2R12	10015-13	Metal Film 100KΩ		±1%	1/8W
A2R13	10015-230	Metal Film 11.0KΩ		±1%	1/8W
A2R14	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R15	10013-95	Carbon Film 51KΩ		±5%	1/4W
A2R16	10013-9	Carbon Film 47KΩ		±5%	1/4W
A2R17	--------	Not Used			
A2R18	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R19	10015-242	Metal Film 37.4KΩ		±1%	1/8W
A2R20	10015-266	Metal Film 301KΩ		±1%	1/8W
A2R21	13584-2	Variable Comp 100Ω		±20%	1/2W
A2R22	10013-77	Carbon Film 1.6KΩ		±5%	1/4W
A2R23	10013-14	Carbon Film 120Ω		±5%	1/4W
A2R24	10013-31	Carbon Film 3.3KΩ		±5%	1/4W
A2R25	10013-43	Carbon Film 33KΩ		±5%	1/4W
A2R26	10013-43	Carbon Film 33KΩ		±5%	1/4W
A2R27	10013-31	Carbon Film 3.3KΩ		±5%	1/4W
A2R28	14881-3	Network 33Ω		±2%	125mW
A2R29	14881-3	Network 33Ω		±2%	125mW
A2R30	10015-13	Metal Film 100KΩ		±1%	1/8W
A2R31	10015-230	Metal Film 11.0KΩ		±1%	1/8W
A2R32	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R33	10015-13	Metal Film 100KΩ		±1%	1/8W
A2R34	10015-230	Metal Film 11.0KΩ		±1%	1/8W
A2R35	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R36	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R37	10015-207	Metal Film 20.0KΩ		±1%	1/8W
A2R38	10015-195	Metal Film 200Ω		±1%	1/8W
A2R39	10013-49	Carbon Film 100KΩ		±5%	1/4W
A2R40	13584-7	Variable Comp. 100KΩ		±20%	1/2W
A2R41	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R42	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R43	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R44	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R45	10015-13	Metal Film 100KΩ		±1%	1/8W
A2R46	10013-28	Carbon Film 1.8KΩ		±5%	1/4W
A2R47	10013-9	Carbon Film 47Ω		±5%	1/4W
A2R48	10013-14	Carbon Film 120Ω		±5%	1/4W
A2R49	10013-33	Carbon Film 4.7KΩ		±5%	1/4W
A2R50	10013-31	Carbon Film 3.3KΩ		±5%	1/4W
A2R51	10013-43	Carbon Film 33KΩ		±5%	1/4W
A2R52	10013-43	Carbon Film 33KΩ		±5%	1/4W
A2R53	10013-31	Carbon Film 3.3KΩ		±5%	1/4W
A2R54	10013-15	Carbon Film 150Ω		±5%	1/4W
A2R55	14881-3	Network 33Ω		±2%	125mW
A2R56	14881-3	Network 33Ω		±2%	125mW
A2R57	10015-230	Metal Film 11.0KΩ		±1%	1/8W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A2R58	10013-9	Carbon Film	47Ω	±5%	1/4W
A2R59	10013-95	Carbon Film	51KΩ	±5%	1/4W
A2R60	---------	Not Used			
A2R61	10015-242	Metal Film	37.4KΩ	±1%	1/8W
A2R62	10015-266	Metal Film	301KΩ	±1%	1/8W
A2R63	10013-9	Carbon Film	47Ω	±5%	1/4W
A2R64	13584-2	Variable Comp	100Ω	±20%	1/2W
A2R65	10013-77	Carbon Film	1.6KΩ	±5%	1/4W
A2R66	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A2R67	10013-15	Carbon Film	150Ω	±5%	1/4W
A2R68	10015-217	Metal Film	1.21Ω	±1%	1/8W
A2R69	10015-114	Metal Film	75.0KΩ	±1%	1/8W
A2R70	10015-45	Metal Film	499KΩ	±1%	1/8W
A2R71	13584-7	Variable Comp	100KΩ	±20%	1/2W
A2R72	10015-116	Metal Film	30.1KΩ	±1%	1/8W
A2R73	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R74	10013-13	Carbon Film	100Ω	±5%	1/4W
A2R75	10013-9	Carbon Film	47Ω	±5%	1/4W
A2R76	10013-13	Carbon Film	100Ω	±5%	1/4W
A2R77	10013-21	Carbon Film	470Ω	±5%	1/4W
A2R78	10013-25	Carbon Film	1KΩ	±5%	1/4W
A2R79	10013-17	Carbon Film	220Ω	±5%	1/4W
A2R80	10015-3	Metal Film	49.9Ω	±1%	1/8W
A2R81	10015-188	Metal Film	33.2KΩ	±1%	1/8W
A2R82	10015-181	Metal Film	121Ω	±1%	1/8W
A2R83	10015-113	Metal Film	75.0Ω	±1%	1/8W
A2R84	10015-113	Metal Film	75.0Ω	±1%	1/8W
A2R85	10013-39	Carbon Film	15KΩ	±5%	1/4W
A2R86	10013-57	Carbon Film	470KΩ	±5%	1/4W
A2R87	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R88	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A2R89	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A2R90	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R91	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R92	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R93	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2R94	10013-37	Carbon Film	10KΩ	±5%	1/4W
A2U1	15249	TL064CN			
A2U2	15119	DG201CJ			
A2U3	15109	8052			
A2U4	15110	7103CDI			
A2U5	15108	7447AN			
A2U6	15100	CA3082			
A2U7	15111	CA3083			
A2U8	15111	CA3083			
A2U9	13470-13	SN74LS74N			
A2U10	15249	TL064CN			
A2U11	14232	8052A			
A2U12	15110	7103CDI			
A2U13	15108	7447AN			
A2U14	15100	CA3082			
A2U15	13470-36	SN74LS05N			
A2U16	11539	741HC			
		INPUT PREAMP AND LOG PC BOARD ASSEMBLY - 15834			
A3C1	10000-11	Ceramic	.01µF	±20%	100V
A3C2	10000-11	Ceramic	.01µF	±20%	100V
A3C3	10000-11	Ceramic	.01µF	±20%	100V
A3C4	10000-11	Ceramic	.01µF	±20%	100V
A3C5	10000-11	Ceramic	.01µF	±20%	100V
A3C6	10000-11	Ceramic	.01µF	±20%	100V
A3C7	10000-11	Ceramic	.01µF	±20%	100V
A3C8	10000-11	Ceramic	.01µF	±20%	100V
A3C9	10000-11	Ceramic	.01µF	±20%	100V
A3C10	10000-11	Ceramic	.01µF	±20%	100V
A3C11	10787-2	Tantalum	12µF	±20%	20V
A3C12	16258-1	Mylar	1.0µF	±10%	50V
A3C13	15776-5	Ceramic	0.1µF	±10%	50V
A3C14	10000-2	Ceramic	220pF	±20%	1000V
A3C15	10000-11	Ceramic	.01µF	±20%	100V
A3C16	10000-11	Ceramic	.01µF	±20%	100V
A3C17	10000-11	Ceramic	.01µF	±20%	100V
A3C18	10000-11	Ceramic	.01µF	±20%	100V
A3C19	10000-11	Ceramic	.01µF	±20%	100V
A3C20	10000-11	Ceramic	.01µF	±20%	100V
A3C21	--------	Not Used			
A3C22	10001-7	Ceramic	100pF	±5%	1000V
A3C23	10000-11	Ceramic	.01µF	±20%	100V
A3C24	10000-11	Ceramic	.01µF	±20%	100V
A3C25	10000-11	Ceramic	.01µF	±20%	100V
A3C26	10000-11	Ceramic	.01µF	±20%	100V
A3C27	15776-1	Ceramic	.01µF	±10%	50V
A3C28	10000-11	Ceramic	.01µF	±20%	100V
A3C29	10787-11	Tantalum	1.0µF	±20%	35V
A3C30	10787-11	Tantalum	1.0µF	±20%	35V
A3C31	10787-11	Tantalum	1.0µF	±20%	35V
A3C32	10001-6	Ceramic	47pF	±5%	1000V
A3C33	10000-11	Ceramic	.01µF	±20%	100V
A3C34	10000-11	Ceramic	.01µF	±20%	100V
A3C35	11501-2	Ceramic	0.1µF	±20%	50V
A3C36	11501-2	Ceramic	0.1µF	±20%	50V
A3C37	10001-13	Ceramic	12pF	±5%	1000V
A3C38	--------	Not Used			
A3C39	15776-5	Ceramic	0.1µF	±10%	50V
A3C40	10000-11	Ceramic	.01µF	±20%	100V
A3C41	10000-11	Ceramic	.01µF	±20%	100V
A3C42	10000-11	Ceramic	.01µF	±20%	100V
A3C43	10000-11	Ceramic	.01µF	±20%	100V
A3C44	10000-11	Ceramic	.01µF	±20%	100V
A3C45	10000-11	Ceramic	.01µF	±20%	100V
A3C46	10000-11	Ceramic	.01µF	±20%	100V
A3C47	10000-11	Ceramic	.01µF	±20%	100V
A3C48	16258-1	Mylar	1.0µF	±10%	50V
A3C49	10001-6	Ceramic	47pF	±5%	1000V
A3C50	15776-1	Ceramic	.01µF	±10%	50V
A3C51	10000-11	Ceramic	.01µF	±20%	100V
A3C52	10000-11	Ceramic	.01µF	±20%	100V
A3C53	10000-11	Ceramic	.01µF	±20%	100V
A3C54	10000-11	Ceramic	.01µF	±20%	100V
A3C55	--------	Not Used			
A3C56	10000-11	Ceramic	.01µF	±20%	100V
A3C57	10000-11	Ceramic	.01µF	±20%	100V
A3C58	10000-11	Ceramic	.01µF	±20%	100V
A3C59	--------	Not Used			
A3C60	10000-1	Ceramic	100pF	±20%	1000V
A3C61	11501-2	Ceramic	0.1µF	±20%	50V
A3C62	11501-2	Ceramic	0.1µF	±20%	50V
A3C63	--------	Not Used			
A3C64	11501-2	Ceramic	0.1µF	±20%	50V
A3C65	--------	Not Used			
A3C66	11501-2	Ceramic	0.1µF	±20%	50V
A3C67	11501-2	Ceramic	0.1µF	±20%	50V
A3C68	--------	Not Used			
A3C69	--------	Not Used			
A3C70	--------	Not Used			
A3C71	11501-2	Ceramic	0.1µF	±20%	50V
A3C72	16258-1	Mylar	1.0µF	±10%	50V
A3C73	11501-7	Ceramic	0.1µF	±20%	100V
A3C74	10000-11	Ceramic	.01µF	±20%	100V
A3C75	10000-3	Ceramic	470pF	±20%	1000V
A3C76	10000-11	Ceramic	.01µF	±20%	100V
A3C77	10000-11	Ceramic	.01µF	±20%	100V
A3C78	11501-2	Ceramic	0.1µF	±20%	50V
A3C79	10001-6	Ceramic	47pF	±5%	1000V
A3C80	10000-4	Ceramic	.001µF	±20%	1000V
A3C81	10000-5	Ceramic	.0022µF	±20%	500V
A3C82	15776-5	Ceramic	0.1µF	±10%	50V
A3C83	11501-2	Ceramic	0.1µF	±20%	50V
A3CR1	10018	2N3646			
A3CR2	10018	2N3646			
A3CR3	10018	2N3646			
A3CR4	10018	2N3646			

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A3CR5	10043	1N4148
A3CR6	10043	1N4148
A3CR7	10043	1N4148
A3CR8	--------	Not Used
A3CR9	--------	Not Used
A3CR10	10043	1N4148
A3CR11	10043	1N4148
A3CR12	10019	2N3565
A3CR13	10043	1N4148
A3CR14	10043	1N4148
A3CR15	10043	1N4148
A3CR16	10043	1N4148
A3CR17	10043	1N4148
A3CR18	10043	1N4148
A3CR19	--------	Not Used
A3CR20	10043	1N4148
A3CR21	10043	1N4148
A3TP1	14320-2	Test Jack
A3TP2	14320-2	Test Jack
A3TP3	14320-2	Test Jack
A3TP4	14320-2	Test Jack
A3TP5	14320-2	Test Jack
A3TP6	14320-2	Test Jack
A3TP7	14320-2	Test Jack
A3TP8	14320-2	Test Jack
A3TP9	14320-2	Test Jack
A3TP10	14320-2	Test Jack
A3TP11	14320-2	Test Jack
A3TP12	14320-2	Test Jack
A3TP13	14320-2	Test Jack
A3TP14	14320-2	Test Jack
A3Q1	11119	2N4250
A3Q2	11119	2N4250
A3Q3	10019	2N3565
A3Q4	11119	2N4250
A3Q5	11119	2N4250
A3Q6	12591	E112
A3Q7	10018	2N3646
A3R1	--------	Not Used
A3R2	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R3	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R4	10013-29	Carbon Film 2.2KΩ ±5% 1/4W
A3R5	10013-29	Carbon Film 2.2KΩ ±5% 1/4W
A3R6	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R7	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R8	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R9	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R10	10015-13	Metal Film 100KΩ ±1% 1/8W
A3R11	10015-13	Metal Film 100KΩ ±1% 1/8W
A3R12	10015-19	Metal Film 1.00KΩ ±1% 1/8W
A3R13	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R14	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R15	10013-25	Carbon Film 1KΩ ±5% 1/4W
A3R16	10013-25	Carbon Film 1KΩ ±5% 1/4W
A3R17	10013-39	Carbon Film 15KΩ ±5% 1/4W
A3R18	10013-39	Carbon Film 15KΩ ±5% 1/4W
A3R19	10013-65	Carbon Film 2.2MΩ ±5% 1/4W
A3R20	13584-7	Variable Comp 100KΩ ±20% 1/2W
A3R21	10013-67	Carbon Film 3.3MΩ ±5% 1/4W
A3R22	12449-88	Metal Film 103.1KΩ ±0.1% 1/8W
A3R23	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R24	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R25	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A3R26	10015-133	Metal Film 49.9KΩ ±1% 1/8W
A3R27	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R28	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R29	--------	Not Used
A3R30	10013-25	Carbon Film 1KΩ ±5% 1/4W
A3R31	10013-55	Carbon Film 330KΩ ±5% 1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A3R32	10013-25	Carbon Film 1KΩ ±5% 1/4W
A3R33	10015-133	Metal Film 49.9KΩ ±1% 1/8W
A3R34	10013-69	Carbon Film 4.7MΩ ±5% 1/4W
A3R35	10013-61	Carbon Film 1MΩ ±5% 1/4W
A3R36	10013-49	Carbon Film 100KΩ ±5% 1/4W
A3R37	10013-37	Carbon Film 10KΩ ±5% 1/4W
A3R38	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R39	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R40	10013-33	Carbon Comp 4.7KΩ ±5% 1/4W
A3R41	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R42	10015-87	Metal Film 15.0KΩ ±1% 1/8W
A3R43	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A3R44	10015-270	Metal Film 357KΩ ±1% 1/8W
A3R45	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R46	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R47	10013-69	Carbon Comp 4.7MΩ ±5% 1/4W
A3R48	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R49	10015-233	Metal Film 174KΩ ±1% 1/8W
A3R50	15142-2	Variable Comp 100KΩ ±10% 1/2W
A3R51	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R52	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R53	13584-4	Variable Comp 1KΩ ±20% 1/2W
A3R54	10015-213	Metal Film 178KΩ ±1% 1/8W
A3R55	10013-33	Carbon Comp 4.7KΩ ±5% 1/4W
A3R56	10015-100	Metal Film 16.9KΩ ±1% 1/8W
A3R57	10015-100	Metal Film 16.9KΩ ±1% 1/8W
A3R58	12449-6	Metal Film 13.617KΩ ±0.1% 1/8W
A3R59	10015-36	Metal Film 5.11KΩ ±1% 1/8W
A3R60	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R61	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R62	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R63	10015-253	Metal Film 30.9KΩ ±1% 1/8W
A3R64	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A3R65	13584-9	Variable Comp 5KΩ ±20% 1/2W
A3R66	--------	Not Used
A3R67	10015-261	Metal Film 2.26KΩ ±1% 1/8W
A3R68	10015-13	Metal Film 100KΩ ±1% 1/8W
A3R69	10015-13	Metal Film 100KΩ ±1% 1/8W
A3R70	10015-13	Metal Film 100KΩ ±1% 1/8W
A3R71	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A3R72	10013-49	Carbon Film 100KΩ ±5% 1/4W
A3R73	--------	Not Used
A3R74	10013-49	Carbon Film 100KΩ ±5% 1/4W
A3R75	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A3R76	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R77	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R78	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A3R79	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A3R80	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A3R81	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R82	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R83	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A3R84	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A3R85	--------	Not Used
A3R86	10013-49	Carbon Film 100KΩ ±5% 1/4W
A3R87	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A3R88	10013-51	Carbon Film 150KΩ ±5% 1/4W
A3R89	10013-73	Carbon Film 10MΩ ±5% 1/4W
A3R90	10013-39	Carbon Film 15KΩ ±5% 1/4W
A3R91	10013-23	Carbon Film 680Ω ±5% 1/4W
A3R92	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R93	10142-8	Carbon Comp 47Ω ±5% 1/4W
A3R94	10013-16	Carbon Film 180Ω ±5% 1/4W
A3R95	10013-69	Carbon Film 4.7MΩ ±5% 1/4W
A3R96	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A3R97	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A3R98	10015-47	Metal Film 2.49KΩ ±1% 1/8W
A3R99	10015-74	Metal Film 2.00KΩ ±1% 1/8W
A3R100	10013-61	Carbon Film 1MΩ ±5% 1/4W
A3R101	--------	Not Used
A3R102	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A3R103	10015-65	Metal Film 4.99KΩ ±1% 1/8W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A3R104	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R105	--------	Not Used			
A3R106	10015-100	Metal Film	16.9KΩ	±1%	1/8W
A3R107	10015-47	Metal Film	2.49KΩ	±1%	1/8W
A3R108	--------	Not Used			
A3R109	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R110	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R111	10013-32	Carbon Film	3.9KΩ	±5%	1/4W
A3R112	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R113	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R114	--------	Not Used			
A3R115	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R116	10015-118	Metal Film	28.7KΩ	±1%	1/8W
A3R117	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R118	10015-91	Metal Film	90.9KΩ	±1%	1/8W
A3R119	13584-4	Variable Comp	1KΩ	±20%	1/2W
A3R120	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A3R121	10015-233	Metal Film	174KΩ	±1%	1/8W
A3R122	10015-213	Metal Film	178KΩ	±1%	1/8W
A3R123	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A3R124	10013-69	Carbon Film	4.7MΩ	±5%	1/4W
A3R125	15142-2	Variable Comp	100KΩ	±10%	1/2W
A3R126	10015-94	Metal Film	97.6KΩ	±1%	1/8W
A3R127	15144-1	Metal Film	10.0MΩ	±1%	1/8W
A3R128	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R129	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A3R130	10015-36	Metal Film	5.11KΩ	±1%	1/8W
A3R131	10015-210	Metal Film	150KΩ	±1%	1/8W
A3R132	10015-210	Metal Film	150KΩ	±1%	1/8W
A3R133	10015-45	Metal Film	499KΩ	±1%	1/4W
A3R134	10015-258	Metal Film	127KΩ	±1%	1/4W
A3R135	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R136	10015-102	Metal Film	249K	±1%	1/4W
A3R137	10015-106	Metal Film	6.81KΩ	±1%	1/8W
A3R138	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R139	10015-67	Metal Film	143KΩ	±1%	1/8W
A3R140	10015-67	Metal Film	143KΩ	±1%	1/8W
A3R141	10015-120	Metal Film	69.8KΩ	±1%	1/8W
A3R142	15142-1	Variable Comp	20KΩ	±10%	1/2W
A3R143	10015-60	Metal Film	19.6KΩ	±1%	1/8W
A3R144	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R145	--------	Not Used			
A3R146	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R147	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R148	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R149	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R150	13584-3	Variable Comp	500Ω	±20%	1/2W
A3R151	10015-65	Metal Film	4.99KΩ	±1%	1/8W
A3R152	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R153	10142-8	Carbon Comp	47Ω	±1%	1/4W
A3R154	10013-25	Carbon Film	1KΩ	±5%	1/4W
A3R155	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R156	--------	Not Used			
A3R157	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R158	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R159	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R160	10015-114	Metal Film	75.0KΩ	±1%	1/8W
A3R161	--------	Not Used			
A3R162	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R163	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R164	--------	Not Used			
A3R165	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R166	--------	Not Used			
A3R167	10013-47	Carbon Film	68KΩ	±5%	1/4W
A3R168	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A3R169	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R170	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R171	10015-189	Metal Film	5.90KΩ	±1%	1/8W
A3R172	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A3R173	10015-13	Metal Film	100KΩ	±1%	1/8W
A3R174	10015-13	Metal Film	100KΩ	±1%	1/8W
A3R175	10015-13	Metal Film	100KΩ	±1%	1/8W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A3R176	10015-13	Metal Film	100KΩ	±1%	1/8W
A3R177	--------	Not Used			
A3R178	10013-17	Carbon Film	220Ω	±5%	1/4W
A3R179	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R180	10142-8	Carbon Comp	47Ω	±5%	1/4W
A3R181	10013-25	Carbon Film	1KΩ	±5%	1/4W
A3R182	10013-25	Carbon Film	1KΩ	±5%	1/4W
A3R183	10013-65	Carbon Film	2.2MΩ	±5%	1/4W
A3R184	10013-49	Carbon Film	100KΩ	±5%	1/4W
A3R185	10013-25	Carbon Film	1KΩ	±5%	1/4W
A3R186	10013-13	Carbon Film	100Ω	±5%	1/4W
A3R187	10013-21	Carbon Film	470Ω	±5%	1/4W
A3R188	10015-62	Metal Film	200KΩ	±1%	1/8W
A3R189	--------	Not Used			
A3R190	--------	Not Used			
A3R191	--------	Not Used			
A3R192	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R193	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R194	10013-37	Carbon Film	10KΩ	±5%	1/4W
A3R195	10013-61	Carbon Film	1MΩ	±5%	1/4W
A3R196	10015-214	Metal Film	374KΩ	±1%	1/8W
A3RT1	13914	Thermister			
A3U1	15141	LM339			
A3U2	14636	DM2503N			
A3U3	14644	DAC-08			
A3U4	15111-3	CA3083F			
A3U5	15135	HA-5135-5 (OP-07CP)			
A3U6	15233	CA3240E			
A3U7	15135	HA-5135-5 (OP-07CP)			
A3U8	15135	HA-5135-5 (OP-07CP)			
A3U9	15135	HA-5135-5 (OP-07CP)			
A3U10	15249	TL064CN			
A3U11	15739	HA-4741-5			
A3U12	15135	HA-5135-5 (OP-07CP)			
A3U13	15135	HA-5135-5 (OP-07CP)			
A3U14	15111-3	CA3083F			
A3U15	13470-56	SN74LS393N			
A3U16	13470-22	SN74LS266N			
A3U17	13470-13	SN74LS74N			
A3U18	15119	DG210CJ			
A3U19	14226	TL074CN			
A3U20	15135	HA-5135-5 (OP-07CP)			
A3U21	15135	HA-5135-5 (OP-07CP)			
A3U22	15119	DG201CJ			
A3U23	13470-12	SN74LS42N			
A3U24	13470-1	SN74LS00N			
A3U25	13470-1	SN74LS00N			
A3U26	13470-4	SN74LS04N			
A3U27	13470-3	SN74LS02N			
A3U28	15233	CA3240E			
A3U29	15119	DG201CJ			
A3U30	15120	DG303CJ			
A3U31	14624	TL072CP			
A3U32	15135	HA-5135-5 (OP-07CP)			
A3U33	13470-2	SN74LS01N			
A3U34	16161	LF441			
		REF. CHAN PREAMP - LOG PC BOARD ASSEMBLY - 15227			
A5C1	10000-11	Ceramic	.01μF	±20%	100V
A5C2	10000-11	Ceramic	.01μF	±20%	100V
A5C3	10000-11	Ceramic	.01μF	±20%	100V
A5C4	10000-11	Ceramic	.01μF	±20%	100V
A5C5	10585-2	Ceramic	330pF	±5%	1000V
A5C6	10011-2	Mylar	1.0μF	±10%	200V
A5C7	10000-11	Ceramic	.01μF	±20%	100V
A5C8	10000-11	Ceramic	.01μF	±20%	100V
A5C9	10001-6	Ceramic	47pF	±5%	1000V
A5C10	10000-11	Ceramic	.01μF	±20%	100V
A5C11	10000-11	Ceramic	.01μF	±20%	100V
A5C12	10000-11	Ceramic	.01μF	±20%	100V
A5C13	10000-11	Ceramic	.01μF	±20%	100V
A5C14	15776-1	Ceramic	.01μF	±10%	50V

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION			
A5C15	10000-11	Ceramic	.01µF	±20%	100V
A5C16	10000-11	Ceramic	.01µF	±20%	100V
A5C17	10000-11	Ceramic	.01µF	±20%	100V
A5C18	10000-11	Ceramic	.01µF	±20%	100V
A5C19	10000-11	Ceramic	.01µF	±20%	100V
A5C20	10000-11	Ceramic	.01µF	±20%	100V
A5C21	10001-7	Ceramic	100pF	±5%	1000V
A5C22	10000-11	Ceramic	.01µF	±20%	100V
A5C23	10000-11	Ceramic	.01µF	±20%	100V
A5C24	10001-7	Ceramic	100pF	±5%	1000V
A5C25	10000-11	Ceramic	.01µF	±20%	100V
A5C26	10000-11	Ceramic	.01µF	±20%	100V
A5C27	10787-11	Tantalum	1.0µF	±20%	35V
A5C28	10787-11	Tantalum	1.0µF	±20%	35V
A5C29	10787-11	Tantalum	1.0µF	±20%	35V
A5C30	11501-2	Ceramic	0.1µF	±20%	50V
A5C31	10000-11	Ceramic	.01µF	±20%	100V
A5C32	10000-11	Ceramic	.01µF	±20%	100V
A5C33	10000-11	Ceramic	.01µF	±20%	100V
A5C34	10000-11	Ceramic	.01µF	±20%	100V
A5C35	10000-3	Ceramic	470pF	±20%	1000V
A5C36	10000-4	Ceramic	.001µF	±20%	1000V
A5C37	11501-2	Ceramic	0.1µF	±20%	50V
A5CR1	-------	Not Used			
A5CR2	10043	1N4148			
A5J1	14320-2	Test Jack			
A5J2	14320-2	Test Jack			
A5J3	14320-2	Test Jack			
A5J4	14320-2	Test Jack			
A5J5	14320-2	Test Jack			
A5J6	14320-2	Test Jack			
A5J7	14320-2	Test Jack			
A5Q1	11119	2N4250			
A5Q2	11119	2N4250			
A5R1	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R2	10015-65	Metal Film	.99KΩ	±10%	1/8W
A5R3	10015-80	Metal Film	4.02KΩ	±1%	1/8W
A5R4	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R5	10015-74	Metal Film	2.00KΩ	±1%	1/8W
A5R6	10015-80	Metal Film	4.02KΩ	±1%	1/8W
A5R7	10015-65	Metal Film	4.99KΩ	±1%	1/8W
A5R8	10015-47	Metal Film	2.49KΩ	±1%	1/8W
A5R9	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R10	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R11	10015-47	Metal Film	2.49KΩ	±1%	1/8W
A5R12	10015-120	Metal Film	69.8KΩ	±1%	1/8W
A5R13	--------	Not Used			
A5R14	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R15	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R16	10013-61	Carbon Film	1MΩ	±5%	1/4W
A5R17	10015-9	Metal Film	17.8KΩ	±1%	1/8W
A5R18	-------	Not Used			
A5R19	10013-37	Carbon Film	10KΩ	±5%	1/4W
A5R20	10013-49	Carbon Film	100KΩ	±5%	1/4W
A5R21	10013-33	Carbon Film	4.7KΩ	±5%	1/4W
A5R22	10013-37	Carbon Film	10KΩ	±5%	1/4W
A5R23	10013-32	Carbon Film	3.9KΩ	±5%	1/4W
A5R24	10015-98	Metal Film	13.3KΩ	±1%	1/8W
A5R25	10015-11	Metal Film	16.2KΩ	±1%	1/8W
A5R26	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R27	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R28	10015-36	Metal Film	5.11KΩ	±1%	1/8W
A5R29	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A5R30	13584-9	Var. Comp.	5KΩ	±20%	1/2W
A5R31	10015-253	Metal Film	30.9KΩ	±1%	1/8W
A5R32	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R33	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R34	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A5R35	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A5R36	10015-118	Metal Film	28.7KΩ	±1%	1/8W
A5R37	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A5R38	10015-54	Metal Film	110KΩ	±1%	1/8W
A5R39	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A5R40	13584-4	Var. Comp.	1KΩ	±20%	1/2W
A5R41	12449-77	Metal Film	169.0KΩ	±0.1%	1/8W
A5R42	10015-233	Metal Film	174KΩ	±1%	1/8W
A5R43	--------	Not Used			
A5R44	--------	Not Used			
A5R45	10015-94	Metal Film	97.6KΩ	±1%	1/8W
A5R46	15144-1	Metal Film	10MΩ	±1%	1/8W
A5R47	10015-36	Metal Film	5.11KΩ	±1%	1/8W
A5R48	10013-37	Carbon Film	10KΩ	±5%	1/4W
A5R49	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A5R50	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A5R51	10015-106	Metal Film	6.81KΩ	±1%	1/8W
A5R52	10015-102	Metal Film	249KΩ	±1%	1/8W
A5R53	10015-258	Metal Film	127KΩ	±1%	1/8W
A5R54	10015-451	Metal Film	499KΩ	±1%	1/8W
A5R55	10015-67	Metal Film	143KΩ	±1%	1/8W
A5R56	10015-67	Metal Film	143KΩ	±1%	1/8W
A5R57	10013-37	Carbon Film	10KΩ	±5%	1/4W
A5R58	15142-1	Var. Comp.	20KΩ	±10%	1/2W
A5R59	10015-60	Metal Film	19.6KΩ	±1%	1/8W
A5R60	10013-39	Carbon Film	100KΩ	±5%	1/4W
A5R61	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R62	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R63	10013-37	Carbon Film	10KΩ	±5%	1/4W
A5R64	12449-21	Metal Film	10.00KΩ	±0.1%	1/8W
A5R65	13584-4	Var. Comp.	1KΩ	±20%	1/2W
A5R66	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R67	10015-66	Metal Film	9.53KΩ	±1%	1/8W
A5R68	13584-5	Var. Comp.	2KΩ	±20%	1/2W
A5R69	10015-65	Metal Film	4.99KΩ	±1%	1/8W
A5R70	--------	Not Used			
A5R71	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R72	-------	Not Used			
A5R73	10015-65	Metal Film	4.99KΩ	±1%	1/8W
A5R74	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R75	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R76	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R77	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R78	10015-189	Metal Film	5.90KΩ	±1%	1/8W
A5R79	10015-7	Metal Film	10.0KΩ	±1%	1/8W
A5R80	10015-13	Metal Film	100KΩ	±1%	1/8W
A5R81	10015-13	Metal Film	100KΩ	±1%	1/8W
A5R82	10015-13	Metal Film	100KΩ	±1%	1/8W
A5R83	10015-13	Metal Film	100KΩ	±1%	1/8W
A5R84	--------	Not Used			
A5R85	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R86	10013-9	Carbon Film	47Ω	±5%	1/4W
A5R87	10013-29	Carbon Film	2.2KΩ	±5%	1/4W
A5R88	10013-29	Carbon Film	2.2KΩ	±5%	1/4W
A5R89	10015-87	Metal Film	15.0KΩ	±1%	1/8W
A5R90	10015-19	Metal Film	1.00KΩ	±1%	1/8W
A5R91	10015-65	Metal Film	4.99KΩ	±1%	1/8W
A5R92	10013-17	Carbon Film	220Ω	±5%	1/4W
A5R93	10013-21	Carbon Film	470Ω	±5%	1/4W
A5R94	10013-17	Carbon Film	220Ω	±5%	1/4W
A5R95	10013-17	Carbon Film	220Ω	±5%	1/4W
A5R96	10013-25	Carbon Film	1KΩ	±5%	1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A5R97	10013-25	Carbon Film 1KΩ ±5% 1/4W
A5R98	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A5RT1	13914	Thermistor 10KΩ
A5U1	15143	CA3096AE
A5U2	14226	TL074CN
A5U3	15135	OP-07CP
A5U4	15135	OP-07CP
A5U5	15135	OP-07CP
A5U6	15249	TL064CN
A5U7	15120	DG303CJ
A5U8	15135	OP-07CP
A5U9	15135	OP-07CP
A5U10	15143	CA3096AE
A5U11	13470	SN74LS02N
A5U12	15249	TL064CN
A5U13	15119	DG201CJ
		'A' CHANNEL MEMORY PC BOARD ASSEMBLY - 14879
A6C1	11501-2	Ceramic 0.1µF ±20% 50V
A6C2	-------	Not Used
A6C3	11501-2	Ceramic 0.1µF ±20% 50V
A6C4	10000-4	Ceramic .001µF ±20% 1000V
A6C5	10000-4	Ceramic .001µF ±20% 1000V
A6C6	-------	Not Used
A6C7	10000-4	Ceramic .001µF ±20% 1000V
A6C8	10000-4	Ceramic .001µF ±20% 1000V
A6C9	11501-2	Ceramic 0.1µF ±20% 50V
A6C10	11501-2	Ceramic 0.1µF ±20% 50V
A6C11	11501-2	Ceramic 0.1µF ±20% 50V
A6C12	11501-2	Ceramic 0.1µF ±20% 50V
A6C13	10000-2	Ceramic 220pF ±20% 1000V
A6C14	10787-11	Tantalum 1.0µF ±20% 35V
A6C15	10000-11	Ceramic .01µF ±20% 100V
A6C16	10000-11	Ceramic .01µF ±20% 100V
A6C17	10000-11	Ceramic .01µF ±20% 100V
A6C18	10000-11	Ceramic .01µF ±20% 100V
A6C19	10000-11	Ceramic .01µF ±20% 100V
A6C20	10000-11	Ceramic .01µF ±20% 100V
A6C21	10000-11	Ceramic .01µF ±20% 100V
A6C22	10000-11	Ceramic .01µF ±20% 100V
A6C23	10000-11	Ceramic .01µF ±20% 100V
A6C24	10000-11	Ceramic .01µF ±20% 100V
A6C25	10000-11	Ceramic .01µF ±20% 100V
A6C26	10000-11	Ceramic .01µF ±20% 100V
A6C27	10000-11	Ceramic .01µF ±20% 100V
A6C28	10000-1	Ceramic 100pF ±20% 1000V
A6C29	10000-1	Ceramic 100pF ±20% 1000V
A6C30	10000-1	Ceramic 100pF ±20% 1000V
A6C31	10909-2	Mica 470pF ±1% 500V
A6C32	10001-8	Ceramic 15pF ±5% 1000V
A6C33	10787-11	Tantalum 1.0µF ±20% 35V
A6C34	10787-11	Tantalum 1.0µF ±20% 35V
A6C35	10000-11	Ceramic .01µF ±20% 100V
A6C36	10000-11	Ceramic .01µF ±20% 100V
A6C37	10000-11	Ceramic .01µF ±20% 100V
A6CR1	10043	1N4148
A6J1	14320-2	Test Jack
A6J2	14320-2	Test Jack
A6J3	14320-2	Test Jack
A6J4	14320-2	Test Jack
A6J5	14320-2	Test Jack
A6J6	14320-2	Test Jack
A6J7	14320-2	Test Jack
A6J8	14320-2	Test Jack
A6J9	14320-2	Test Jack
A6J10	14320-2	Test Jack
A6J11	14320-2	Test Jack
A6J12	14320-2	Test Jack
A6R1	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R2	-------	Not Used
A6R3	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R4	10013-25	Carbon Film 1KΩ ±5% 1/4W
A6R5	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R6	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R7	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R8	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R9	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R10	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R11	10015-206	Metal Film 7.50KΩ ±1% 1/8W
A6R12	---------	Not Used
A6R13	---------	Not Used
A6R14	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R15	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R16	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R17	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A6R18	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R19	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R20	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R21	10013-9	Carbon Film 47Ω ±5% 1/4W
A6R22	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A6R23	10013-37	Carbon Film 10KΩ ±5% 1/4W
A6R24	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A6R25	10013-21	Carbon Film 470Ω ±5% 1/4W
A6R26	10013-21	Carbon Film 470Ω ±5% 1/4W
A6R27	10013-21	Carbon Film 470Ω ±5% 1/4W
A6R28	10015-230	Metal Film 11.0K ±1% 1/8W
A6R29	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A6R30	10013-17	Carbon Film 220Ω ±5% 1/4W
A6U1	13470-42	SN74LS365N
A6U2	13470-42	SN74LS365N
A6U3	13470-53	SN74LS83N
A6U4	13470-53	SN74LS83N
A6U5	13470-53	SN74LS83N
A6U6	13470-17	SN74LS123N
A6U7	13470-52	SN74LS33N
A6U8	14670	DM2504N
A6U9	14671	AD565JD
A6U10	13470-5	SN74LS08N
A6U11	13470-13	SN74LS74N
A6U12	13470-55	SN74LS378N
A6U13	13470-42	SN74LS365N
A6U14	13470-42	SN74LS365N
A6U15	13470-42	SN74LS365N
A6U16	13470-9	SN74LS27N
A6U17	13470-12	SN74LS42N
A6U18	13470-13	SN74LS74N
A6U19	13470-55	SN74LS378N
A6U20	13470-42	SN74LS365N
A6U21	13470-42	SN74LS365N
A6U22	13470-42	SN74LS365N
A6U23	13470-47	SN74LS32N
A6U24	14634	LM311N
A6U25	14226	TL074CN
A6U26	13470-54	SN74LS193N
A6U27	14640	P2114
A6U28	14640	P2114
A6U29	14640	P2114

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A6U30	14640	P2114
A6U31	14640	P2114
A6U32	14640	P2114
		'B' CHANNEL MEMORY PC BOARD ASSEMBLY - 14887
A7C1	10000-4	Ceramic .001µF ±20% 1000V
A7C2	10000-4	Ceramic .001µF ±20% 1000V
A7C3	11501-2	Ceramic 0.1µF ±20% 50V
A7C4	11501-2	Ceramic 0.1µF ±20% 50V
A7C5	10000-11	Ceramic .01µF ±20% 100V
A7C6	10000-11	Ceramic .01µF ±20% 100V
A7C7	10000-11	Ceramic .01µF ±20% 100V
A7C8	11501-2	Ceramic 0.1µF ±20% 50V
A7C9	11501-2	Ceramic 0.1µF ±20% 50V
A7C10	10001-6	Ceramic 47 pF ±5% 1000V
A7C11	10001-4	Ceramic 22 pF ±5% 1000V
A7C12	11501-2	Ceramic 0.1µF ±20% 50V
A7C13	11501-2	Ceramic 0.1µF ±20% 50V
A7C14	-------	Not Used
A7C15	10000-4	Ceramic .001µF ±20% 1000V
A7C16	10000-4	Ceramic .001µF ±20% 1000V
A7C17	10787-11	Tantalum 1.0µF ±20% 35V
A7C18	10787-11	Tantalum 1.0µF ±20% 35V
A7C19	10000-1	Ceramic 100 pF ±20% 1000V
A7C20	10000-1	Ceramic 100 pF ±20% 1000V
A7C21	10909-2	Mica 470 pF ±1% 500V
A7C22	10677-2	Mica 220 pF ±1% 500V
A7C23	10000-11	Ceramic .01µF ±20% 100V
A7C24	10000-11	Ceramic .01µF ±20% 100V
A7C25	10000-11	Ceramic .01µF ±20% 100V
A7C26	10787-11	Tantalum 1.0µF ±20% 35V
A7C27	10000-11	Ceramic .01µF ±20% 100V
A7C28	10000-11	Ceramic .01µF ±20% 100V
A7C29	10787-11	Tantalum 1.0µF ±20% 35V
A7C30	10585-2	Ceramic 330 pF ±5% 1000V
A7C31	10000-4	Ceramic .001µF ±20% 1000V
A7C32	11501-2	Ceramic 0.1µF ±20% 50V
A7C33	11501-2	Ceramic 0.1µF ±20% 50V
A7C34	11501-2	Ceramic 0.1µF ±20% 50V
A7C35	-------	Not Used
A7C36	10000-11	Ceramic .01µF ±20% 100V
A7C37	10000-11	Ceramic .01µF ±20% 100V
A7C38	10000-11	Ceramic .01µF ±20% 100V
A7C39	10000-11	Ceramic .01µF ±20% 100V
A7C40	10000-11	Ceramic .01µF ±20% 100V
A7C41	10000-11	Ceramic .01µF ±20% 100V
A7C42	10787-11	Tantalum 1.0µF ±20% 35V
A7C43	--------	Not Used
A7C44	--------	Not Used
A7C45	--------	Not Used
A7C46	--------	Not Used
A7C47	10000-11	Ceramic .01µF ±20% 100V
A7C48	10787-11	Tantalum 1.0µF ±20% 35V
A7C49	10011-2	Mylar 1.0µF ±20% 200V
A7C50	10000-2	Ceramic 220 pF ±20% 1000V
A7C51	10000-11	Ceramic .01µF ±20% 100V
A7C52	10000-11	Ceramic 0.1µF ±20% 100V
A7CR1	10043	1N4148
A7J1	14320-2	Test Jack
A7J2	14320-2	Test Jack
A7J3	14320-2	Test Jack
A7J4	14320-2	Test Jack
A7J5	14320-2	Test Jack
A7J6	14320-2	Test Jack
A7J7	14320-2	Test Jack
A7J8	14320-2	Test Jack
A7J9	14320-2	Test Jack
A7J10	14320-2	Test Jack
A7R1	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R2	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R3	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R4	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R5	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R6	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R7	10013-25	Carbon Film 1KΩ ±5% 1/4W
A7R8	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A7R9	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R10	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R11	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A7R12	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A7R13	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A7R14	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A7R15	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A7R16	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A7R17	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R18	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R19	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R20	--------	Not Used
A7R21	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R22	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R23	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A7R24	--------	Not Used
A7R25	10013-21	Carbon Film 470Ω ±5% 1/4W
A7R26	10013-21	Carbon Film 470Ω ±5% 1/4W
A7R27	10015-19	Metal Film 1.00KΩ ±1% 1/8W
A7R28	10015-230	Metal Film 11.0KΩ ±1% 1.8W
A7R29	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A7R30	10013-37	Carbon Film 10KΩ ±5% 1/4W
A7R31	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A7R32	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A7R33	10015-17	Metal Film 511Ω ±1% 1/8W
A7R34	10015-17	Metal Film 511Ω ±1% 1/8W
A7R35	10015-258	Metal Film 127KΩ ±1% 1/8W
A7R36	---------	Not Used
A7R37	---------	Not Used
A7R38	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A7R39	15142-3	Var. Comp. 1KΩ ±10% 1/2W
A7R40	10015-110	Metal Film 3.01KΩ ±1% 1/8W
A7R41	10015-80	Metal Film 4.02KΩ ±1% 1/8W
A7R42	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R43	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R44	10015-141	Metal Film 316KΩ ±1% 1/8W
A7R45	10013-37	Carbon Film 10KΩ ±5% 1/4W
A7R46	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A7R47	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R48	10013-13	Carbon Film 100Ω ±5% 1/4W
A7R49	10013-21	Carbon Film 470Ω ±5% 1/4W
A7R50	10013-16	Carbon Film 180Ω ±5% 1/4W
A7U1	14636	DM2503
A7U2	14636	DM2503
A7U3	13470-17	SN74LS123N
A7U4	13470-51	SN74LS86N
A7U5	13470-17	SN74LS123N
A7U6	13470-49	SN74LS244N
A7U7	13470-49	SN74LS244N
A7U8	13470-13	SN74LS74N
A7U9	13470-50	SN74LS28N
A7U10	13470-47	SN74LS32N
A7U11	13470-13	SN74LS74N
A7U12	15093	LM399H

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A7U13	14644	DAC08
A7U14	14644	DAC08
A7U15	14640	P2114
A7U16	14640	P2114
A7U17	14640	P2114
A7U18	14640	P2114
A7U19	15249	TL064CL
A7U20	14226	TL074
A7U21	14634	LM311N
A7U22	14640	P2114
A7U23	14640	P2114
A7U24	14640	P2114
A7U25	14640	P2114
		HORIZ & CURSOR PC BOARD ASSEMBLY - 15187
A8C1	10000-1	Ceramic 100pF ±20% 100V
A8C2	10000-11	Ceramic .01µF ±20% 100V
A8C3	10000-11	Ceramic .01µF ±20% 100V
A8C4	11501-2	Ceramic 0.1µF ±20% 50V
A8C5	10011-2	Mylar 1.0µF ±10% 200V
A8C6	11501-2	Ceramic 0.1µF ±20% 50V
A8C7	10909-3	Ceramic 390pF ±1% 1000V
A8C8	-------	Not Used
A8C9	10000-11	Ceramic .01µF ±20% 100V
A8C10	10001-6	Ceramic 47pF ±5% 1000V
A8C11	10000-11	Ceramic .01µF ±20% 100V
A8C12	10000-8	Ceramic .022µF ±20% 500V
A8C13	-------	Not Used
A8C14	11501-2	Ceramic 0.1µF ±20% 50V
A8C15	11501-2	Ceramic 0.1µF ±20% 50V
A8C16	11501-2	Ceramic 0.1µF ±20% 50V
A8C17	10000-11	Ceramic .01µF ±20% 100V
A8C18	10000-11	Ceramic .01µF ±20% 100V
A8C19	10001-6	Ceramic 47pF ±5% 1000V
A8C20	15776-5	Ceramic 0.1µF ±10% 50V
A8C21	11501-2	Ceramic 0.1µF ±20% 50V
A8C22	15788-1	Metal Mylar 1.0µF ±10% 50V
A8C23	10001-3	Ceramic 10pF ±20% 500V
A8C24	15776-4	Ceramic .0022µF ±10% 50V
A8C25	15776-3	Ceramic .022µF ±10% 50V
A8C26	15776-3	Ceramic .022µF ±10% 50V
A8C27	10000-2	Ceramic 220pF ±20% 1000V
A8C28	10001-3	Ceramic 10pF ±20% 500V
A8C29	15776-4	Ceramic .0022µF ±10% 50V
A8C30	10011-2	Mylar 1.0µF ±10% 200V
A8C31	10000-11	Ceramic .01µF ±20% 100V
A8C32	10000-11	Ceramic .01µF ±20% 100V
A8C33	10000-11	Ceramic .01µF ±20% 100V
A8C34	10000-11	Ceramic .01µF ±20% 100V
A8C35	10000-11	Ceramic .01µF ±20% 100V
A8C36	10000-11	Ceramic .01µF ±20% 100V
A8C37	10000-11	Ceramic .01µF ±20% 100V
A8C38	10000-11	Ceramic .01µF ±20% 100V
A8C39	10000-11	Ceramic .01µF ±20% 100V
A8C40	10000-11	Ceramic .01µF ±20% 100V
A8C41	10000-11	Ceramic .01µF ±20% 100V
A8C42	10000-11	Ceramic .01µF ±20% 100V
A8C43	10000-11	Ceramic .01µF ±20% 100V
A8C44	10000-11	Ceramic .01µF ±20% 100V
A8C45	10000-11	Ceramic .01µF ±20% 100V
A8C46	10000-11	Ceramic .01µF ±20% 100V
A8C47	10000-11	Ceramic .01µF ±20% 100V
A8C48	10000-11	Ceramic .01µF ±20% 100V
A8C49	10000-11	Ceramic .01µF ±20% 100V
A8C50	10000-11	Ceramic .01µF ±20% 100V
A8C51	10000-11	Ceramic .01µF ±20% 100V
A8C52	10000-11	Ceramic .01µF ±20% 100V
A8C53	10000-11	Ceramic .01µF ±20% 100V
A8C54	10000-11	Ceramic .01µF ±20% 100V
A8C55	10787-11	Tantalum 1.0µF ±20% 35V
A8C56	10787-11	Tantalum 1.0µF ±20% 35V
A8C57	10787-11	Tantalum 1.0µF ±20% 35V
A8C58	10787-11	Tantalum 1.0µF ±20% 35V
A8C59	10000-2	Ceramic 220pF ±20% 1000V
A8C60	10000-11	Ceramic .01µF ±20% 100V
A8C61	10909-2	Ceramic 470pF ±1% 1000V
A8C62	10909-2	Ceramic 470pF ±1% 1000V
A8C63	10001-5	Ceramic 33pF ±5% 1000V
A8C64	10001-5	Ceramic 33pF ±5% 1000V
A8C65	10000-1	Ceramic 100pF ±20% 1000V
A8C66	15776-4	Ceramic .0022µF ±10% 50V
A8C67	15776-4	Ceramic .0022µF ±10% 50V
A8C68	10000-12	Ceramic 150pF ±20% 1000V
A8CR1	10043	1N4148
A8CR2	10043	1N4148
A8CR3	10043	1N4148
A8CR4	10043	1N4148
A8CR5	10043	1N4148
A8CR6	10043	1N4148
A8CR7	10043	1N4148
A8CR8	--------	Not Used
A8CR9	10043	1N4148
A8CR10	10043	1N4148
A8CR11	10043	1N4148
A8CR12	--------	Not Used
A8CR13	10043	1N4148
A8J1	14320-2	Test Jack
A8J2	14320-2	Test Jack
A8J3	14320-2	Test Jack
A8J3	14320-2	Test Jack
A8J4	14320-2	Test Jack
A8J5	14320-2	Test Jack
A8J6	14320-2	Test Jack
A8J7	--------	Not Used
A8J8	14320-2	Test Jack
A8J9	14320-2	Test Jack
A8J10	14320-2	Test Jack
A8J11	14320-2	Test Jack
A8J12	14320-2	Test Jack
A8J13	14320-2	Test Jack
A8J14	14320-2	Test Jack
A8Q1	10019	2N3565
A8Q2	10019	2N3565
A8R1	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R2	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R3	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R4	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R5	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A8R6	10015-207	Metal Film 20.0KΩ ±1% 1/8W
A8R7	10015-218	Metal Film 40.2KΩ ±1% 1/8W
A8R8	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A8R9	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R10	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R11	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R12	10013-47	Carbon Film 68KΩ ±5% 1/4W
A8R13	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R14	10013-65	Carbon Film 2.2MΩ ±5% 1/4W
A8R15	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R16	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A8R17	10013-45	Carbon Film 47KΩ ±5% 1/4W
A8R18	10013-35	Carbon Film 6.8KΩ ±5% 1/4W
A8R19	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R20	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R21	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R22	10013-28	Carbon Film 108KΩ ±5% 1/4W
A8R23	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R24	10013-73	Carbon Film 10MΩ ±5% 1/4W
A8R25	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R26	10013-18	Carbon Film 270Ω ±5% 1/4W
A8R27	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R28	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R29	10013-25	Carbon Film 1KΩ ±5% 1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A8R30	10013-65	Carbon Film 2.2MΩ ±5% 1/4W
A8R31	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A8R32	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A8R33	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A8R34	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A8R35	10013-16	Carbon Film 180Ω ±5% 1/4W
A8R36	10013-51	Carbon Film 150KΩ ±5% 1/4W
A8R37	10013-34	Carbon Film 5.6KΩ ±5% 1/4W
A8R38	10015-13	Metal Film 100KΩ ±1% 1/8W
A8R39	--------	Not Used
A8R40	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R41	10015-152	Metal Film 332Ω ±1% 1/8W
A8R42	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R43	10015-33	Metal Film 92.5KΩ ±1% 1/8W
A8R44	10015-224	Metal Film 150Ω ±1% 1/8W
A8R45	--------	Not Used
A8R46	--------	Not Used
A8R47	--------	Not Used
A8R48	--------	Not Used
A8R49	10013-13	Carbon Film 100Ω ±5% 1/4W
A8R50	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A8R51	12449-53	Metal Film 50.00KΩ ±0.1% 1/8W
A8R52	12449-53	Metal Film 50.00KΩ ±0.1% 1/8W
A8R53	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A8R54	10013-39	Carbon Film 15KΩ ±5% 1/4W
A8R55	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R56	10013-53	Carbon Film 220KΩ ±5% 1/4W
A8R57	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A8R58	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R59	10013-35	Carbon Film 6.8KΩ ±5% 1/4W
A8R60	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A8R61	10013-35	Carbon Film 6.8KΩ ±5% 1/4W
A8R62	12449-26	Metal Film 5.000KΩ ±0.1% 1/8W
A8R63	12449-26	Metal Film 5.000KΩ ±0.1% 1/8W
A8R64	12449-26	Metal Film 5.000KΩ ±0.1% 1/8W
A8R65	12449-26	Metal Film 5.000KΩ ±0.1% 1/8W
A8R66	10015-239	Metal Film 187KΩ ±1% 1/8W
A8R67	10015-120	Metal Film 69.8KΩ ±1% 1/8W
A8R68	10015-133	Metal Film 49.9KΩ ±1% 1/8W
A8R69	10015-62	Metal Film 200KΩ ±1% 1/8W
A8R70	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A8R71	--------	Not Used
A8R72	--------	Not Used
A8R73	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R74	10015-13	Metal Film 100KΩ ±1% 1/8W
A8R75	--------	Not Used
A8R76	10015-190	Metal Film 13.0KΩ ±1% 1/8W
A8R77	15142-2	Variable Comp 100KΩ ±10% 1/2W
A8R78	10013-51	Carbon Film 150KΩ ±5% 1/4W
A8R79	10013-13	Carbon Film 100Ω ±5% 1/4W
A8R80	10015-74	Metal Film 2.00KΩ ±1% 1/8W
A8R81	10015-45	Metal Film 499KΩ ±1% 1/8W
A8R82	10015-20	Metal Film 1.10KΩ ±1% 1/8W
A8R83	10015-45	Metal Film 499KΩ ±1% 1/8W
A8R84	10015-13	Metal Film 100KΩ ±1% 1/8W
A8R85	10015-218	Metal Film 40.2KΩ ±1% 1/8W
A8R86	10015-218	Metal Film 40.2KΩ ±1% 1/8W
A8R87	10013-25	Carbon Film 1KΩ ±5% 1/4W
A8R88	10015-24	Metal Film 46.4KΩ ±1% 1/8W
A8R89	10015-13	Metal Film 100KΩ ±1% 1/8W
A8R90	10015-13	Metal Film 100KΩ ±1% 1/8W
A8R91	10015-119	Metal Film 34.8KΩ ±1% 1/8W
A8R92	10013-49	Carbon Film 100KΩ ±5% 1/4W
A8R93	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R94	10013-51	Carbon Film 150KΩ ±5% 1/4W
A8R95	10015-90	Metal Film 24.9KΩ ±5% 1/4W
A8R96	13584-4	Variable Comp 1KΩ ±20% 1/2W
A8R97	10015-90	Metal Film 24.9KΩ ±1% 1/8W
A8R98	10015-106	Metal Film 6.81KΩ ±1% 1/8W
A8R99	10015-19	Metal Film 1.00KΩ ±1% 1/8W
A8R100	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A8R101	12449-53	Metal Film 50.00KΩ ±0.1% 1/8W
A8R102	12449-53	Metal Film 50.00KΩ ±0.1% 1/8W
A8R103	15142-2	Variable Comp 100KΩ ±10% 1/2W
A8R104	10013-51	Carbon Film 150KΩ ±5% 1/4W
A8R105	10013-13	Carbon Film 100Ω ±5% 1/4W
A8R106	12449-77	Metal Film 169.0KΩ ±0.1% 1/8W
A8R107	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A8R108	12449-77	Metal Film 169.0KΩ ±0.1% 1/8W
A8R109	13584-4	Variable Comp 1KΩ ±20% 1/2W
A8R110	10015-7	Metal Film 10.0KΩ ±1% 1/8W
A8R111	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R112	--------	Not Used
A8R113	--------	Not Used
A8R114	--------	Not Used
A8R115	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A8R116	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A8R117	10015-123	Metal Film 301Ω ±1% 1/8W
A8R118	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A8R119	12449-86	Metal Film 100.3KΩ ±0.1% 1/8W
A8R120	10015-109	Metal Film 348KΩ ±1% 1/8W
A8R121	10015-19	Metal Film 1.00KΩ ±1% 1/8W
A8R122	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A8R123	10015-43	Metal Film 121KΩ ±1% 1/8W
A8R124	10013-13	Carbon Film 100Ω ±5% 1/4W
A8R125	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A8R126	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A8R127	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R128	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R129	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R130	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R131	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R132	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R133	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R134	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R135	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R136	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R137	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R138	10013-9	Carbon Film 47Ω ±5% 1/4W
A8R139	10013-29	Carbon Film 2.2KΩ ±5% 1/4W
A8R140	12449-65	Metal Film 2.200KΩ ±0.1% 1/8W
A8R141	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R142	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R143	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R144	10013-21	Carbon Film 470Ω ±5% 1/4W
A8R145	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R146	12449-82	Metal Film 115.8KΩ ±0.1% 1/8W
A8R147	10013-17	Carbon Film 220Ω ±5% 1/4W
A8R148	10013-45	Carbon Film 47KΩ ±5% 1/4W
A8R149	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A8R150	12449-73	Metal Film 10.20KΩ ±0.1% 1/8W
A8R151	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A8R152	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A8R153	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A8R154	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A8R155	10013-37	Carbon Film 10KΩ ±5% 1/4W
A8R156	10013-35	Carbon Film 6.8KΩ ±5% 1/4W
A8R157	10013-57	Carbon Film 470KΩ ±5% 1/4W
A8S1	15122	Switch, DIP, SPST (4 rocker arms)
A8S2	14677	Switch, DIP, SPST (5 rocker arms)
A8U1	14634	LM311N
A8U2	11332	CA3054
A8U3	15233	CA3240AE1
A8U4	15119	DG210CJ
A8U5	15141	LM339N
A8U6	13470-7	SN74LS14N
A8U7	13470-13	SN74LS74N
A8U8	13470-18	SN74LS221N
A8U9	15249	TL064CN
A8U10	15249	TL064CN
A8U11	15249	TL064CN
A8U12	14226	TL074CN
A8U13	15141	LM339N

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A8U14	13470-6	SN74LS10N
A8U15	13470-13	SN74LS74N
A8U16	13470-17	SN74LS123N
A8U17	15119	DG210CJ
A8U18	15249	TL064CN
A8U19	15143	CA3096A
A8U20	13470-54	SN74LS193N
A8U21	13470-54	SN74LS193N
A8U22	13470-54	SN74LS193N
A8U23	14645	AD561JD
A8U24	14641	8255A
A8U25	15120	DG303CJ
A8U26	15249	TL064CN
A8U27	14671	AD565J
A8U28	13470-54	SN74LS193N
A8U29	13470-54	SN74LS193N
A8U30	13470-54	SN74LS193N
A8U31	13470-44	SN74LS138N
		CRT DISPLAY PC BD ASSY - 15330
		(Note: A9 and A10 are common PC Board Assemblies. Prefix reference designators with A9 or A10)
A9C1	11501-2	Ceramic 0.1µF ±20% 50V
A9C2	10000-4	Ceramic .001µF ±20% 1000V
A9C3	10000-4	Ceramic .001µF ±20% 1000V
A9C4	10000-4	Ceramic .001µF ±20% 1000V
A9C5	10000-4	Ceramic .001µF ±20% 1000V
A9C6	10000-4	Ceramic .001µF ±20% 1000V
A9C7	10000-4	Ceramic .001µF ±20% 1000V
A9C8	10000-4	Ceramic .001µF ±20% 1000V
A9C9	10000-4	Ceramic .001µF ±20% 1000V
A9C10	10000-4	Ceramic .001µF ±20% 1000V
A9C11	10000-4	Ceramic .001µF ±20% 1000V
A9C12	10000-4	Ceramic .001µF ±20% 1000V
A9C13	10000-4	Ceramic .001µF ±20% 1000V
A9C14	10000-4	Ceramic .001µF ±20% 1000V
A9C15	10000-4	Ceramic .001µF ±20% 1000V
A9C16	10000-4	Ceramic .001µF ±20% 1000V
A9C17	10000-4	Ceramic .001µF ±20% 1000V
A9C18	--------	Not Used
A9C19	--------	Not Used
A9C20	10000-4	Ceramic .001µF ±20% 1000V
A9C21	10000-4	Ceramic .001µF ±20% 1000V
A9C22	10001-3	Ceramic 10pF ±5% 1000V
A9C23	10000-11	Ceramic .01µF ±20% 1000V
A9C24	--------	Not Used
A9C25	--------	Not Used
A9C26	--------	Not Used
A9C27	--------	Not Used
A9C28	--------	Not Used
A9C29	--------	Not Used
A9C30	10000-4	Ceramic .001µF ±20% 1000V
A9C31	10000-4	Ceramic .001µF ±20% 1000V
A9C32	11501-2	Ceramic 0.1µF ±20% 50V
A9C33	10787-11	Tantalum 1.0µF ±20% 35V
A9C34	10787-11	Tantalum 1.0µF ±20% 35V
A9C35	10787-11	Tantalum 1.0µF ±20% 35V
A9C36	11501-2	Ceramic 0.1µF ±20% 50V
A9C37	11501-2	Ceramic 0.1µF ±20% 50V
A9C38	11501-2	Ceramic 0.1µF ±20% 50V
A9V39	11501-2	Ceramic 0.1µF ±20% 50V
A9C40	10000-11	Ceramic .01µF ±20% 100V
A9C41	10000-11	Ceramic .01µF ±20% 100V
A9C42	10000-11	Ceramic .01µF ±20% 100V
A9C43	10000-11	Ceramic .01µF ±20% 100V
A9C44	10000-11	Ceramic .01µF ±20% 100V
A9C45	10000-11	Ceramic .01µF ±20% 100V
A9C46	10000-11	Ceramic .01µF ±20% 100V
A9C47	10000-11	Ceramic .01µF ±20% 100V
A9C48	10000-11	Ceramic .01µF ±20% 100V
A9C49	10000-11	Ceramic .01µF ±20% 100V
A9C50	10000-11	Ceramic .01µF ±20% 100V

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A9C51	10000-11	Ceramic .01µF ±20% 100V
A9C52	10000-11	Ceramic .01µF ±20% 100V
A9C53	10000-11	Ceramic .01µF ±20% 100V
A9C54	10000-11	Ceramic .01µF ±20% 100V
A9C55	10000-11	Ceramic .01µF ±20% 100V
A9C56	10000-11	Ceramic .01µF ±20% 100V
A9C57	10000-11	Ceramic .01µF ±20% 100V
A9C58	10000-11	Ceramic .01µF ±20% 100V
A9C59	10000-11	Ceramic .01µF ±20% 100V
A9C60	10000-11	Ceramic .01µF ±20% 100V
A9C61	10000-11	Ceramic .01µF ±20% 100V
A9C62	10000-11	Ceramic .01µF ±20% 100V
A9C63	10000-11	Ceramic .01µF ±20% 100V
A9C64	11501-2	Ceramic 0.1µF ±20% 50V
A9C65	10000-11	Ceramic .01µF ±20% 100V
A9C66	10000-11	Ceramic .01µF ±20% 100V
A9C67	10000-11	Ceramic .01µF ±20% 100V
A9C68	10000-11	Ceramic .01µF ±20% 100V
A9CR1	10043	1N4148
A9CR2	10043	1N4148
A9Q1	11119	2N4250
A9Q2	10019	2N3565
A9R1	10015-45	Metal Film 499KΩ ±1% 1/8W
A9R2	10015-45	Metal Film 499KΩ ±1% 1/8W
A9R3	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R4	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R5	10013-73	Carbon Film 10MΩ ±5% 1/4W
A9R6	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R7	--------	Not Used
A9R8	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R9	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R10	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R11	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R12	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R13	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R14	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R15	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R16	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R17	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R18	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R19	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R20	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R21	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A9R22	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R23	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R24	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R25	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R26	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R27	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R28	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R29	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R30	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R31	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R32	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R33	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R34	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R35	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R36	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R37	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R38	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R39	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R40	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R41	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R42	12909-15	Wire Wound 16.70KΩ ±0.1% 1/8W
A9R43	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R44	12909-9	Wire Wound 10.00KΩ ±0.1% 1/8W
A9R45	10013-69	Carbon Film 4.7MΩ ±5% 1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A9R46	12449-14	Wire Wound 10.20KΩ ±0.1% 1/8W
A9R47	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R48	13584-2	Var. Comp. 100Ω ±20% 1/2W
A9R49	10015-60	Metal Film 19.6KΩ ±1% 1/8W
A9R50	--------	Not Used
A9R51	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R52	--------	Not Used
A9R53	12499-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R54	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R55	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R56	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R57	--------	Not Used
A9R58	--------	Not Used
A9R59	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R60	10142-2	Carbon Film 15MΩ ±5% 1/4W
A9R61	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R62	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R63	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R64	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A9R65	--------	Not Used
A9R66	12449-78	Metal Film 1.000MΩ ±0.1% 1/8W
A9R67	12449-79	Metal Film 500.0KΩ ±0.1% 1/8W
A9R68	12449-80	Metal Film 200.0KΩ ±0.1% 1/8W
A9R69	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R70	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R71	10013-73	Carbon Film 10MΩ ±5% 1/4W
A9R72	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R73	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A9R74	12449-33	Metal Film 100.0KΩ ±0.1% 1/8W
A9R75	12449-21	Metal Film 10.00KΩ ±0.1% 1/8W
A9R76	12449-53	Metal Film 50.00KΩ ±0.1% 1/8W
A9R77	10013-37	Carbon Film 10KΩ ±5% 1/4W
A9R78	--------	Not Used
A9R79	10013-25	Carbon Film 1KΩ ±5% 1/4W
A9R80	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A9R81	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A9R82	10015-65	Metal Film 4.99KΩ ±1% 1/8W
A9R83	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R84	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R85	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R86	12449-37	Metal Film 20.00KΩ ±0.1% 1/8W
A9R87	10013-37	Carbon Film 10KΩ ±5% 1/4W
A9R88	12449-55	Metal Film 4.000KΩ ±0.1% 1/8W
A9R89	12449-55	Metal Film 4.000KΩ ±0.1% 1/8W
A9R90	12449-80	Metal Film 200.0KΩ ±0.1% 1/8W
A9R91	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R92	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R93	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R94	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R95	10013-71	Carbon Film 6.8MΩ ±5% 1/4W
A9R96	13584-7	Var. Comp. 100KΩ ±20% 1/2W
A9R97	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R98	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R99	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R100	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R101	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R102	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R103	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R104	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R105	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R106	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R107	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R108	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R109	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R110	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R111	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R112	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R113	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R114	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R115	10013-17	Carbon Film 220Ω ±5% 1/4W
A9R116	10013-17	Carbon Film 220Ω ±5% 1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A9R117	10013-21	Carbon Film 470Ω ±5% 1/4W
A9R118	10013-65	Carbon Film 2.2MΩ ±5% 1/4W
A9R119	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R120	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R121	13584-3	Var. Comp. 500Ω ±20% 1/2W
A9R122	-------	Not Used
A9R123	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R124	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R125	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R126	10013-9	Carbon Film 47Ω ±5% 1/4W
A9R127	13584-4	Var. Comp. 1KΩ ±10% 1/2W
A9S1	15091	Rotary, BCD
A9TP1	14320-2	Test Jack
A9TP2	14320-2	Test Jack
A9TP3	14320-2	Test Jack
A9TP4	14320-2	Test Jack
A9TP5	14320-2	Test Jack
A9TP6	14320-2	Test Jack
A9TP7	14320-2	Test Jack
A9TP8	14320-2	Test Jack
A9TP9	14320-2	Test Jack
A9TP10	14320-2	Test Jack
A9U1	15135	OP-07CP
A9U2	15135	OP-07CP
A9U3	15135	OP-07CP
A9U4	15119	DG201CJ
A9U5	15135	OP-07CP
A9U6	15214	AD7542AD
A9U7	13470-44	SN74LS183N
A9U8	15119	DG201CJ
A9U9	15119	DG201CJ
A9U10	15119	DG201CJ
A9U11	15135	OP-07CP
A9U12	15249	TL064CN
A9U13	13470-51	SN74LS86N
A9U14	15343	TL062CP
A9U15	15343	TL062CP
A9U16	15249	TL064CN
A9U17	14644	DAC08EQ
A9U18	14641	8255A

CPU PC BOARD ASSEMBLY 14963

A11C1	11501-2	Ceramic 0.1μF ±20% 50V
A11C2	10000-11	Ceramic .01μF ±20% 100V
A11C3	10000-11	Ceramic .01μF ±20% 100V
A11C4	10000-11	Ceramic .01μF ±20% 100V
A11C5	10000-11	Ceramic .01μF ±20% 100V
A11C6	10001-11	Ceramic 25 pF ±5% 1000V
A11C7	10001-11	Ceramic 25 pF ±5% 1000V
A11C8	11501-2	Ceramic 0.1μF ±20% 50V
A11C9	10787-11	Tantalum 1.0μF ±20% 35V
A11C10	11501-2	Ceramic 0.1μF ±20% 50V
A11C11	11501-2	Ceramic 0.1μF ±20% 50V
A11C12	-------	Not Used
A11C13	11501-2	Ceramic 0.1μF ±20% 50V
A11C14	11501-2	Ceramic 0.1μF ±20% 50V
A11C15	11501-2	Ceramic 0.1μF ±20% 50V
A11C16	10000-11	Ceramic .01μF ±20% 100V
A11C17	11501-2	Ceramic 0.1μF ±20% 50V
A11C18	11501-2	Ceramic 0.1μF ±20% 50V
A11C19	10787-11	Tantalum 1.0μF ±20% 35V
A11C20	11501-2	Ceramic 0.1μF ±20% 50V
A11C21	10787-11	Tantalum 1.0μF ±20% 35V

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A11C22	10787-11	Tantalum 1.0µF ±20% 35V
A11CR1	10043	1N4148
A11CR2	10043	1N4148
A11CR3	10043	1N4148
A11J1	14320-2	Test Jack
A11J2	14320-2	Test Jack
A11J3	14320-2	Test Jack
A11J4	14320-2	Test Jack
A11Q1	10398	2N4917
A11Q2	10018	2N3646
A11Q3	11507	TIS97
A11Q4	15092	TIS93
A11Q5	11507	TIS97
A11Q6	15092	TIS93
A11Q7	11507	TIS97
A11R1	14882-1	Network 10KΩ ±2% 125MW
A11R2	10013-18	Carbon Film 270Ω ±5% 1/4W
A11R3	10013-25	Carbon Film 1KΩ ±5% 1/4W
A11R4	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A11R5	10013-33	Carbon Film 4.7KΩ ±5% 1/4W
A11R6	10013-5	Carbon Film 22Ω ±5% 1/4W
A11R7	10013-5	Carbon Film 22Ω ±5% 1/4W
A11R8	10013-31	Carbon Film 3.3KΩ ±5% 1/4W
A11R9	--------	Not Used
A11R10	10013-37	Carbon Film 10KΩ ±5% 1/4W
A11R11	10013-37	Carbon Film 10KΩ ±5% 1/4W
A11R12	10013-37	Carbon Film 10KΩ ±5% 1/4W
A11R13	14882-1	Network 10KΩ ±2% 125MW
A11R14	14882-1	Network 10KΩ ±2% 125MW
A11R15	--------	Not Used
A11R16	--------	Not Used
A11R17	10013-32	Carbon Film 3.9KΩ ±5% 1/4W
A11R18	10013-32	Carbon Film 3.9KΩ ±5% 1/4W
A11R19	10013-43	Carbon Film 33KΩ ±5% 1/4W
A11R20	10013-43	Carbon Film 33KΩ ±5% 1/4W
A11R21	10013-32	Carbon Film 3.9KΩ ±5% 1/4W
A11R22	10013-32	Carbon Film 3.9KΩ ±5% 1/4W
A11R23	10013-43	Carbon Film 33KΩ ±5% 1/4W
A11R24	10013-43	Carbon Film 33KΩ ±5% 1/4W
A11R25	10013-28	Carbon Film 1.8KΩ ±5% 1/4W
A11S1	15091	Rotary, BCD
A11S2	15090	DIP, SPDT (2 Rocker Arms)
A11S3	15090	DIP, SPDT (2 Rocker Arms)
A11U1	14640	P2114
A11U2	13470-44	SN74LS138N
A11U3	15635-12	2732
A11U4	15039	K1148
A11U5	13470-48	SN74LS93N
A11U6	13470-7	SN74LS14N
A11U7	14640	P2114
A11U8	13470-44	SN74LS138N
A11U9	13470-48	SN74LS93N
A11U10	13470-49	SN74LS244N
A11U11	15088	Z80 PIO
A11U12	15635-13	2732
A11U13	13470-47	SN74LS32N
A11U14	15087	8216
A11U15	14641	8255A
A11U16	14675	Z80 CPU

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A11U17	15087	8216
		INTERCONNECT PC BOARD ASSEMBLY - 15005
A12J1	12440-3	P.C. Edge, 50 Contact
A12J2	12440-3	P.C. Edge, 50 Contact
A12J3	12440-3	P.C. Edge, 50 Contact
A12J4	12440-3	P.C. Edge, 50 Contact
A12J5	12440-3	P.C. Edge, 50 Contact
A12J6	12440-3	P.C. Edge, 50 Contact
A12J7	12440-3	P.C. Edge, 50 Contact
A12J8	12440-3	P.C. Edge, 50 Contact
A12J9	12440-3	P.C. Edge, 50 Contact
A12J10	12440-3	P.C. Edge, 50 Contact
A12J11	12440-3	P.C. Edge, 50 Contact
A12J12	14514-1	Post, .025 Square
A12J13	14514-1	Post, .025 Square
A12J14	14514-1	Post, .025 Square
		FRONT PANEL PC BOARD ASSEMBLY - 14968
A13C1	11501-1	Ceramic .022µF ±20% 50V
A13C2	11501-2	Ceramic 0.1µF ±20% 50V
A13C3	11501-2	Ceramic 0.1µF ±20% 50V
A13C4	11501-1	Ceramic .022µF ±20% 50V
A13C5	11501-2	Ceramic 0.1µF ±20% 50V
A13C6	11501-1	Ceramic .022µF ±20% 50V
A13C7	11501-2	Ceramic 0.1µF ±20% 50V
A13CR1	14006	LED, Red MV57124
A13CR2	14006	LED, Red MV57124
A13CR3	15077	LED, Red AND124R
A13CR4	15077	LED, Red AND124R
A13CR5	15077	LED, Red AND124R
A13CR6	15077	LED, Red AND124R
A13CR7	15077	LED, Red AND124R
A13CR8	15077	LED, Red AND124R
A13CR9	14006	LED, Red MV57124
A13CR10	14006	LED, Red MV57124
A13CR11	15077	LED, Red AND124R
A13CR12	15077	LED, Red AND124R
A13CR13	15077	LED, Red AND124R
A13CR14	15077	LED, Red AND124R
A13CR15	15077	LED, Red AND124R
A13CR16	15077	LED, Red AND124R
A13CR17	15077	LED, Red AND124R
A13CR18	15077	LED, Red AND124R
A13CR19	15077	LED, Red AND124R
A13CR20	15077	LED, Red AND124R
A13CR21	15077	LED, Red AND124R
A13CR22	15077	LED, Red AND124R
A13J1	14514-1	Post, .025 Square
A13J2	14514-1	Post, .025 Square
A13J3	14514-1	Post, .025 Square
A13J4	14514-1	Post, .025 Square
A13LS1	15164	Piezo-Alarm
A13R1	10013-19	Carbon Film 330Ω ±5% 1/4W
A13R2	10013-19	Carbon Film 330Ω ±5% 1/4W
A13R3	10013-7	Carbon Film 33Ω ±5% 1/4W
A13R4	10013-7	Carbon Film 33Ω ±5% 1/4W

CIRCUIT REFERENCE	PM PART NO.	DESCRIPTION
A13S1	15083-15	Pushbutton, Plain
A13S2	15083-15	Pushbutton, Plain
A13S3	15083-15	Pushbutton, Plain
A13S4	15083-15	Pushbutton, Plain
A13S5	15083-15	Pushbutton, Plain
A13S6	15083-15	Pushbutton, Plain
A13S7	15083-15	Pushbutton, Plain
A13S8	15083-13	Pushbutton, 'Δ'
A13S9	15083-13	Pushbutton, 'Δ'
A13S10	15083-13	Pushbutton, 'Δ'
A13S11	15083-13	Pushbutton, 'Δ'
A13S12	15083-13	Pushbutton, 'Δ'
A13S13	15083-13	Pushbutton, 'Δ'
A13S14	15083-14	Pushbutton, ' '
A13S15	15083-13	Pushbutton, 'Δ'
A13S16	15083-13	Pushbutton, 'Δ'
A13S17	15083-14	Pushbutton, ' '
A13S18	15083-10	Pushbutton, '0'
A13S19	15083-4	Pushbutton, '4'
A13S20	15083-8	Pushbutton, '8'
A13S21	15083-1	Pushbutton, '1'
A13S22	15083-5	Pushbutton, '5'
A13S23	15083-9	Pushbutton, '9'
A13S24	15083-2	Pushbutton, '2'
A13S25	15083-6	Pushbutton, '6'
A13S26	15083-11	Pushbutton, '.'
A13S27	15083-3	Pushbutton, '3'
A13S28	15083-7	Pushbutton, '7'
A13S29	15083-12	Pushbutton, '-'
A13U1	15079	Display LED ±1 Red
A13U2	15080	Display LED Numeric Red
A13U3	15080	Display LED Numeric Red
A13U4	15080	Display LED Numeric Red
A13U5	15079	Display LED ±1 Red
A13U6	15080	Display LED Numeric Red
A13U7	15080	Display LED Numeric Red
A13U8	15080	Display LED Numeric Red
A13U9	15080	Display LED Numeric Red
A13U10	15081-2	Display LED 5 Digit Red
A13U11	15081-2	Display LED 5 Digit Red
A13U12	15081-1	Display LED 3 Digit Red
A13U13	15076	MM74C922N
A13U14	15076	MM74C922N
A13U15	15081-1	Display LED 3 Digit Red
A13U16	15081-1	Display LED 3 Digit Red
A13U17	15076	MM74C922N
A13U18	15081-1	Display LED 3 Digit Red
		HORIZONTAL FINGER PC BOARD ASSEMBLY - 15023
A14J1	14514-1	Post, .025 Square
		'A' CHANNEL FINGER PC BOARD ASSEMBLY - 15064
A15J1	14514-1	Post, .025 Square

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
10000-1	56289	5GA-T10
10000-2	56289	5GA-T22
10000-3	56289	5GA-T47
10000-4	56289	5GA-D10
10000-5	56289	5GA-D22
10000-6	56289	5GA-D47
10000-8	56289	5GAS-S20
10000-11	72982	805-000-X5V0-103Z
10001-1	56289	10TCC-V22
10001-2	56289	10TCC-V47
10001-3	56289	10TCC-Q10
10001-4	56289	10TCC-Q22
10001-5	56289	10TCC-Q33
10001-6	56289	10TCC-Q47
10001-7	56289	10TCC-T10
10001-8	56289	10TCC-Q15
10001-11	56289	10TCC-Q25
10001-14	56289	10TCC-O68
10007-2	80031	711D1AA222PK601AX
10007-3	80031	711D1AC472PK601AX
10007-5	80031	711D1AA223PK201AX
10007-7	80031	711D1AC104PK201AX
10007-8	80031	711D1AF224PX201AX
10011-2	27556	ZA1652K
10013-5	80031	B803104NB220
10013-7	80031	B803104NB330
10013-9	80031	B803104NB470
10013-13	80031	B803104NB101
10013-14	80031	B803104NB121
10013-15	80031	B803104NB151
10013-16	80031	B803104NB181
10013-17	80031	B803104NB221
10013-18	80031	B803104NB271
10013-19	80031	B803104NB331
10013-21	80031	B803104NB471
10013-22	80031	B803104NB561
10013-23	80031	B803104NB681
10013-25	80031	B803104NB102
10013-28	80031	B803104NB182
10013-29	80031	B803104NB222
10013-31	80031	B803104NB332
10013-32	80031	B803104NB392
10013-33	80031	B803104NB472
10013-34	80031	B803104NB562
10013-35	80031	B803104NB682
10013-37	80031	B803104NB103
10013-39	80031	B803104NB153
10013-43	80031	B803104NB333
10013-45	80031	B803104NB473
10013-47	80031	B803104NB683
10013-49	80031	B803104NB104
10013-51	80031	B803104NB154
10013-53	80031	B803104NB224
10013-55	80031	B803104NB334
10013-57	80031	B803104NB474
10013-59	80031	B803104NB684

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
10013-61	80031	B803104NB105
10013-65	80031	B803104NB225
10013-69	80031	B803104NB475
10013-71	80031	B803104NB685
10013-73	80031	B803104NB106
10013-77	80031	B803104NB162
10013-81	80031	B803104NB432
10013-95	80031	B803104NB513
10015-3	24546	RN55D 49.9 Ohm 1%
10015-6	24546	RN55D 464K Ohm 1%
10015-7	24546	RN55D 10.0K Ohm 1%
10015-9	24546	RN55D 17.8K Ohm 1%
10015-12	24546	RN55D 9.09K Ohm 1%
10015-13	24546	RN55D 100K Ohm 1%
10015-14	24546	RN55D 31.6K Ohm 1%
10015-17	24546	RN55D 511 Ohm 1%
10015-19	24546	RN55D 1.00K Ohm 1%
10015-24	24546	RN55D 46.4K Ohm 1%
10015-27	24546	RN55D 56.2K Ohm 1%
10015-33	24546	RN55D 82.5K Ohm 1%
10015-36	24546	RN55D 5.11K Ohm 1%
10015-45	24546	RN55D 499K Ohm 1%
10015-47	24546	RN55D 2.49 Ohm 1%
10015-54	24546	RN55D 110K Ohm 1%
10015-60	24546	RN55D 19.6K Ohm 1%
10015-62	24546	RN55D 402K Ohm 1%
10015-65	24546	RN55D 4.99K Ohm 1%
10015-66	24546	RN55D 9.53K Ohm 1%
10015-67	24546	RN55D 143K Ohm 1%
10015-74	24546	RN55D 2.00K Ohm 1%
10015-80	24546	RN55D 4.02K Ohm 1%
10015-87	24546	RN55D 15.0K Ohm 1%
10015-90	24546	RN55D 24.9K Ohm 1%
10015-94	24546	RN55D 97.6K Ohm 1%
10015-98	24546	RN55D 13.3K Ohm 1%
10015-100	24546	RN55D 16.9K Ohm 1%
10015-106	24546	RN55D 6.81K Ohm 1%
10015-110	24546	RN55D 3.01K Ohm 1%
10015-113	24546	RN55D 75.0K Ohm 1%
10015-114	24546	RN55D 75.0K Ohm 1%
10015-116	24546	RN55D 30.1K Ohm 1%
10015-118	24546	RN55D 28.7K Ohm 1%
10015-119	24546	RN55D 34.8K Ohm 1%
10015-120	24546	RN55D 69.8K Ohm 1%
10015-133	24546	RN55D 49.9K Ohm 1%
10015-152	24546	RN55D 332 Ohm 1%
10015-181	24546	RN55D 121 Ohm 1%
10015-188	24546	RN55D 33.2K Ohm 1%

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
10015-189	24546	RN55D 5.90K Ohm 1%
10015-190	24546	RN55D 13.0K Ohm 1%
10015-191	24546	RN55D 66.5K Ohm 1%
10015-195	24546	RN55D 200 Ohm 1%
10015-206	24546	RN55D 7.50K Ohm 1%
10015-207	24546	RN55D 20.0K Ohm 1%
10015-210	24546	RN55D 150K Ohm 1%
10015-214	24546	RN55D 374K Ohm 1%
10015-217	24546	RN55D 1.21K Ohm 1%
10015-218	24546	RN55D 40.2K Ohm 1%
10015-230	24546	RN55D 11.0K Ohm 1%
10015-233	24546	RN55D 174K Ohm 1%
10015-239	24546	RN55D 187K Ohm 1%
10015-242	24546	RN55D 37.4K Ohm 1%
10015-261	24546	RN55D 226K Ohm 1%
10015-266	24546	RN55D 301K Ohm 1%
10017	07263	2N3569
10018	07263	2N3646
10019	07263	2N3565
10043	01002	1N4148
10045	12954	1N823
10142-2	01121	CB1565
10142-8	01121	RC07GF470J
10398	07263	PN4917
10585-2	56289	CO28B102F331J
10585-4	56289	CO28B102F681J
10585-5	56289	562C-X5E-AA102AJ102J
10677-2	84171	DM15F221J500V
10677-10	84171	DM15F131J500V
10677-12	84171	DM15F391J500V
10787-2	56289	196D126X9020JA1
10787-11	56289	196D105X9035HA1
10909-2	84171	CM06FD471F03
10909-8	84171	CM05FD560F03
10909-11	84171	CM05FD620F03
10909-12	84171	CM06FD121J03
11119	07263	2N4250
11332	02735	CA3054

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
11501-1	72982	8131-050-W5R-223K
11501-2	72982	8131-050-651-104M
11501-7	72982	8131-050-X7R0-103K
11507	01295	TIS97
11539	07263	741HC
11676-1	01121	WA1N024S104MZ
11845-4	24546	FP-2 15 Ohm 2W 10%
11845-5	24546	FP-2 36K Ohm 2W 10%
12440-3	02660	225-22523-110
12449-21	14298	EE 1/8 C2 10.00KΩ 0.1%
12449-22	14298	EE 1/8 C2 2.500KΩ 0.1%
12449-26	14298	EE 1/8 C2 5.000KΩ 0.1%
12449-33	14298	EE 1/8 C2 100.0KΩ 0.1%
12449-37	14298	EE 1/8 C2 20.00KΩ 0.1%
12449-53	14298	EE 1/8 C2 50.00KΩ 0.1%
12449-55	14298	EE 1/8 C2 4.000KΩ 0.1%
12449-57	14298	EE 1/8 C2 33.33KΩ 0.1%
12449-65	14298	EE 1/8 C2 2.200KΩ 0.1%
12449-73	14298	EE 1/8 C2 10.20KΩ 0.1%
12449-77	14298	EE 1/8 C2 169.0KΩ 0.1%
12449-78	14298	EE 1/8 C2 1.000MΩ 0.1%
12449-79	14298	EE 1/8 C2 500.0KΩ 0.1%
12449-80	14298	EE 1/8 C2 200.0KΩ 0.1%
12449-81	14298	EE 1/8 C2 128.0KΩ 0.1%
12449-82	14298	EE 1/8 C2 115.8Ω 0.1%
12449-83	14298	EE 1/8 C2 16.70KΩ 0.1%
12449-88	14298	EE 1/8 C2 103.1KΩ 0.1%
12591	17856	E11Z2
13470-1	01295	SN74LS00N
13470-2	01295	SN74LS01N
13470-3	01295	SN74LS02N
13470-4	01295	SN74LS04N
13470-5	01295	SN74LS08N
13470-6	01295	SN74LS10N
13470-7	01295	SN74LS14N
13470-9	01295	SN74LS27N
*12909-9	18235	535, 10.00KΩ
*12909-14	18235	535, 10.20KΩ
13470-12	01295	SN74LS42N
13470-13	01295	SN74LS74N
*12909-15	18235	535, 16.70KΩ
13470-17	01295	SN74LS123N
13470-22	01295	SN74LS266N
13470-36	01295	SN74LS05N
13470-42	01295	SN74LS365N
13470-44	01295	SN74LS138N
13470-47	01295	SN74LS32N

* = Out of Sequence

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
13470-48	01295	SN74LS93N
13470-49	01295	SN74LS244N
13470-50	01295	SN74LS28N
13470-51	01295	SN74LS86N
13470-52	01295	SN74LS33N
13470-53	01295	SN74LS83N
13470-54	01295	SN74LS193N
13470-55	01295	SN74LS378N
13470-56	01295	SN74LS393N
13584-2	71450	375x101B
13584-3	71450	375x501B
13584-4	71450	375x102B
13584-5	71450	375x202B
13584-7	71450	375x104B
13584-9	71450	375x502B
13871	27014	LM555CN
13914	83186	41D2
13979-1	80031	C281CH/AIM
14006	76541	MV57124
14226	01295	TL074CN
14320-2	28821	14320
14514-1	00779	87022-1 Reeled
14634	27014	LM311N
14636	27014	DM2503N
14640	34649	P2114
14641	34649	8255A
14644	06665	DAC08EQ
14645	24355	AD56AJD
14670	27014	DM2504CN
14671	24355	AD565JN
14675	28821	Z80 CPU
14677	81073	76SB05
14881-1	01121	108B221
14881-3	01121	108B330

PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.
14977-1	34649	2716
14977-24	34649	2716
14977-25	34649	2716
15039	04713	K1148A
15076	27014	MM74C922N
15077	28821	AND124R
15079	28480	5082-7616
15080	28480	5082-7610
15081-1	28480	5082-7402
15081-2	28480	5082-7405
15083-1	28821	15083-1
15083-2	28821	15083-2
15083-3	28821	15083-3
15083-4	28821	15083-4
15083-5	28821	15083-5
15083-6	28821	15083-6
15083-7	28821	15083-7
15083-8	28821	15083-8
15083-9	28821	15083-9
15083-10	28821	15083-10
15083-11	28821	15083-11
15083-12	28821	15083-12
15083-13	28821	15083-13
15083-14	28821	15083-14
15083-15	28821	15083-15
15087	34649	8216
15088	28821	Z80 PIO
15090	81073	76C04
15091	00779	53137-1
15092	01295	TIS 93
15093	27014	LM399H
15098-1	01121	108A102
15100	02735	CA3082E
15108	27014	DM7447AN
15109	32293	ICL8052CDD
15110	32293	ICL71C03CDI
15111	02735	CA3083F
15112	16733	700214
15119	17856	DG201CJ
15120	17856	DG303CJ
15122	81073	76SB04

PART NO. CROSS REFERENCE			PART NO. CROSS REFERENCE		
PM PART NO.	MFGR. CODE	MFGR. PART NO.	PM PART NO.	MFGR. CODE	MFGR. PART NO.
15129	28821	15129			
15130	28821	15130			
15132	28821	15132			
15135	06665	OP-07CP			
15141	27014	LM339N			
15142-1	73138	66X 20KΩ			
15142-2	73138	66X 100KΩ			
15143	02735	CA3096AE			
15144-1	80031	SPR5053YD			
15156	28821	15156			
15157	28821	15157			
15164	28821	PKM11-4AO			
15165	28821	15165			
15166	28821	15166			
15175	04713	MCM6810P			
15214	24355	AD7542AD			
15232	32293	ICL8052CPD			
15233	02735	CA3240E			
15249	01295	TL064CN			
15292	28821	15292			
15293	28821	15292			
15343	01295	TL062CP			
15635-12	28821	15635-12			
15635-13	28821	15635-13			
15739	34371	HA-4741-5			
15776-1	71590	CW15C103K			
16161	27014	LF441CH			
16258-1	WIMA	mks/1.0μF/10%			

The following five-digit code numbers are listed in numerical sequence along with the manufacturer's name and address to which the code has been assigned.

The Federal Supply Code has been taken from Cataloging Handbook H 4-2, Code to Name.

00303 Shelly Associates Inc.
El Segundo, California

00656 Aerovox Corp.
New Bedford, Massachusetts

00779 Amp Inc.
Harrisburg, Pennsylvania

01002 General Electric Co.
Capacitor Dept.
Hudson Falls, New York

01121 Allen-Bradley Co.
Milwaukee, Wisonsin

01295 Texas Instruments, Inc.
Semiconductor Components Div.
Dallas, Texas

01961 Pulse Engineering Inc.
Santa Clara, California

02114 Ferroxcube Corp. of America
Saugerties, New York

02660 Amphenol-Borg Elect. Corp.
Broadview, Illinois

02735 Radio Corp. of America
Semiconductor and Materials Div.
Somerville, New Jersey

03888 Pyrofilm Resistor Co. Inc.
Whippany, New Jersey

04713 Motorola, Inc.
Semiconductor Products Div.
Phoenix, Arizona

05035 Ayer Manufacturing Co.
Chicago Heights, Illinois

07126 Digitran Co.
Pasadena, California

07263 Fairchild Camera and Inst. Corp.
Semiconductor Div.
Mountain View, California

07910 Continental Device Corp.
Hawthorne, California

09214 General Electric Co.
Semiconductor Products Dept.
Auburn, New York

09353 C and K Components Inc.
Newton, Massachusetts

11323 General Microwave Corp.
Farmingdale, New York

11711 General Instruments Inc.
Semiconductor Div.
Newark, New Jersey

12954 Dickson Electronics Corp.
Scottsdale, Arizona

14099 Semtech Corp.
Newbury Part, California

14298 American Components, Inc.
Conshohocken, Pennsylvania

14655 Cornell Dubilier Corp.
New York, New York

16733 Cablewave Systems
North Haven, Connecticut

17540 Alpha Industries
Woburn, Massachusetts

17856 Siliconix Inc.
Santa Clara, California

18235 KRL Electronics, Inc.
Manchester, New Hampshire

18324 Signetics Corp.
Sunnyvale, California

19447 Electro-Technique Inc.
Oceanside, California

21847 Aertech Industries
Sunnyvale, California

24546 Corning Glass Works Electronic
Components Div.
Raleigh, North Carolina

24931 Speciality Connector Co. Inc.
Indianapolis, Indiana

25088 Siemens America Corp.
Iselin, New Jersey

27014 National Semiconductor Corp.
Santa Clara, California

27556 IMB Electronic Products
Santa Fe Springs, California

28480 Hewlett-Packard Co.
Palo Alto, California

28821 Pacific Measurements Inc.
Sunnyvale, California

32284 Rotron Manufacturing Co. Inc.
Woodstock, New York

32293 Intersil Inc.
Cupertino, California

34078 Midwest Microwave Inc.
Ann Arbor, Michigan

34649 Intel Corp.
Santa Clara, California

50088 Mostek Corp.
Carrollton, Texas

56289 Sprague Electric Co.
North Adams, Massachusetts

70903 Belden Mfg. Co.
Chicago, Illinois

71034 Bliley Electric Co.
Erie, Pennsylvania

71400 Bussman Mfg.
Div. of McGraw-Edison Co.
St. Louis, Missouri

71450 CTS Corp.
Elkhart, Indiana

71590 Centralab Electronics
Milwaukee, Wisconsin

72982 Erie Tech. Products Inc.
Erie, Pennsylvania

73138 Beckman Instruments Inc.
Helipot Division
Fullerton, California

74970 E.F. Johnson Co.
Waseca, Minnesota

75042 TRW Electronic Components IRC.
Philadelphia, Pennsylvania

75915 Littlefuse Inc.
Des Plaines, Illinois

76493 J.W. Miller Co.
Compton, California

76541 Monsanto Commerical Products Co.
Cupertino, California

76854 Oak Mfg. Co.
Crystal Lake, Illinois

79727 Continental-Wirt Electronics Corp.
Philadelphia, Pennsylvania

80031 Mepco/Electra Inc.
A North American Phillips Co.
Morristown, New Jersey

80294 Bourns Inc.
Trimpot Div.
Riverside, California

81073 Grayhill Inc.
La Grange, Illinois

81483 International Rectifier Corp.
El Segundo, California

82389 Switchcraft Inc.
Chicago, Illinois

83330 H.H. Smith Inc.
Brooklyn, New York

83701 Electronic Devices Inc.
Yonkers, New York

84171 Arco Electronics Inc.
Great Neck, New York

91418 Radio Materials Co.
Chicago, Illinois

91637 Dale Electronics Inc.
Columbus, Nebraska

91929 Honeywell Inc.
Microswitch Div.
Freeport, Illinois

94144 Raytheon Co.
Components Div.
Quincy, Massachusetts

95146 Alco Electronics
Lawrence, Massachusetts

99800 Delavan Electronics Corp.
East Aurora, New York

06665 Precision Monolithics Inc.
1500 Space Park Drive
Santa Clara, California

24355 Analog Devices
P.O. Box 280
Norwood, MA 02062

83186 Victory Engineering Corp.
128 Springfield Avenue
Springfield, NJ 07081

34371 Harris Corp.
P.O. Box 883
Melbourne, Florida

SECTION 10

MANUAL CORRECTIONS

This section lists the corrections that must be incorporated in this manual to make it correspond to a particular instrument. The serial number of each instrument is prefixed by a code number. This code number is used to identify the applicable manual corrections for a particular instrument. When correcting this manual start with the corrections corresponding to the Code No. on the instrument. If a particular component has been changed more than one time, make only the first change encountered.

CODE NO.	CORRECTIONS	PM PART NO.	SECTION OF MANUAL AFFECTED
18	None		