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PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7D02
LOGIC ANALYZER
SERVICE MANUAL

INSTRUCTION MANUAL

Tektronix, Inc.
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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols In This Manual

This symbol indictes where applicable cautionary or other information is to be found.

Symbols As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only the power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

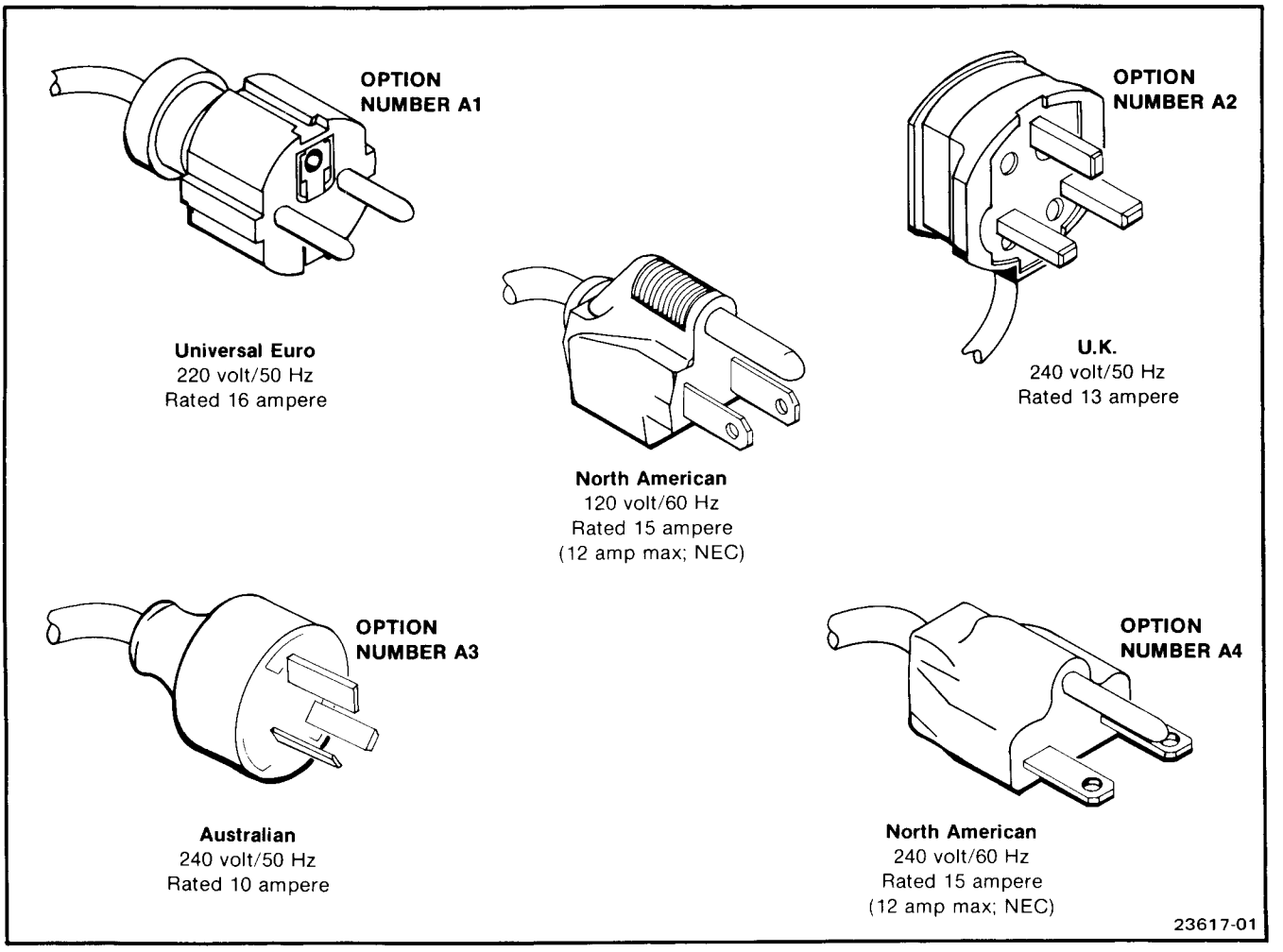
Use Care When Servicing With Power On

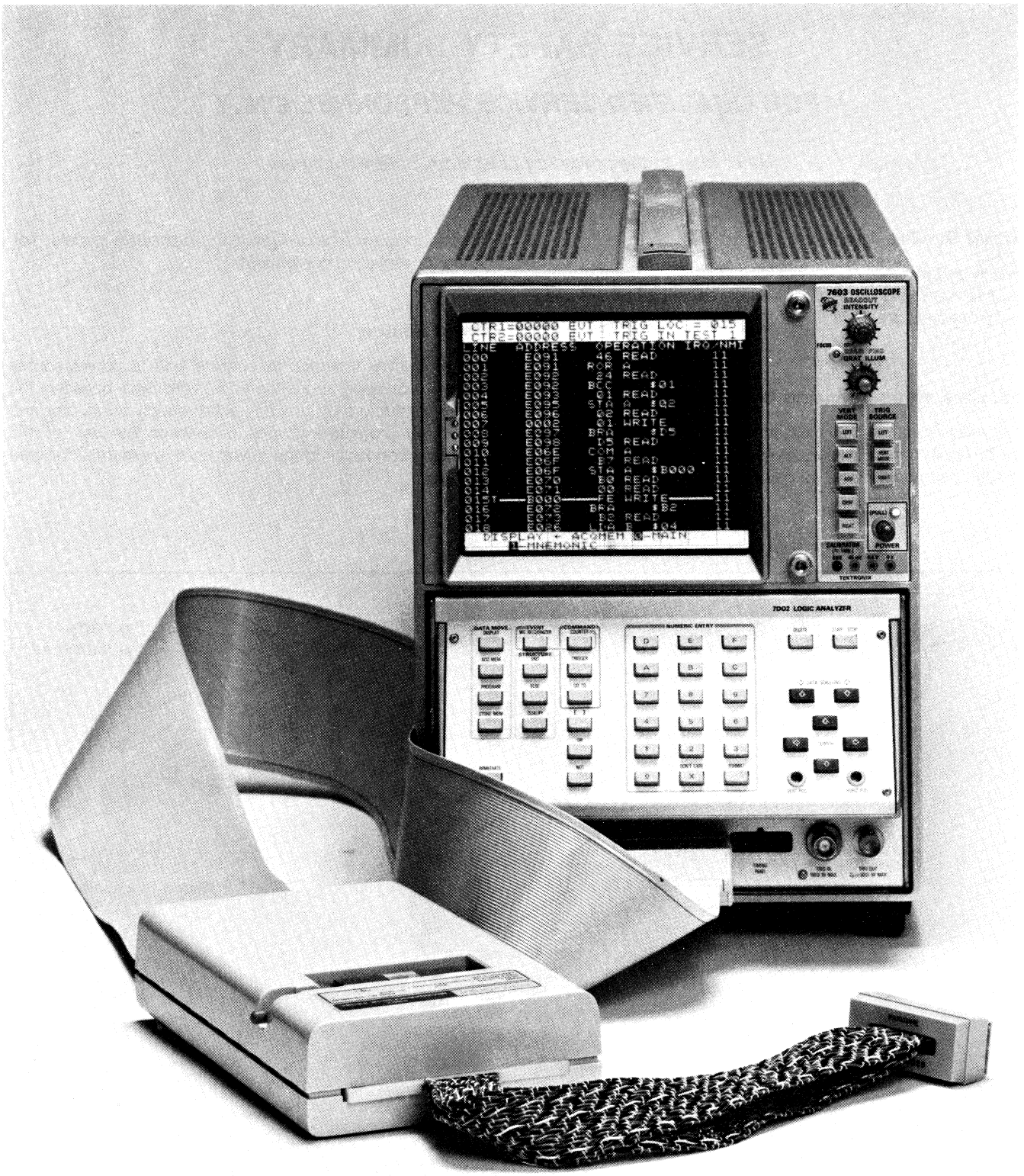
Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.





The 7D02 Logic Analyzer.

SECTION 1

GENERAL INFORMATION

Introduction

The 7D02 Logic Analyzer is a design, debugging, and troubleshooting aid for use in the development of digital systems, especially microprocessor-based systems. It is capable of supporting both 8-bit and 16-bit microprocessors. The 7D02 has been designed as a plug-in for any three-wide (or larger) Tektronix 7 Series oscilloscope mainframe.

7D02 COMPONENTS

The basic 7D02 offers a wide (28-channel) Acquisition Memory, four word recognizers, two general-purpose counters, a user-configurable clock, data qualification circuitry, a state machine architecture, three memories, and a simple facility for customizing the 7D02 for a wide variety of microprocessors.

The basic 7D02 acquires data from the system under test (SUT) on 28 channels, usually orgainized as:

16 address bus lines
8 data bus lines
4 control lines

The word recognizers perform recognition on these 28 channels plus an additional three channels (an external trigger line and two additional control lines from the SUT). Any of the four word recognizers can be used to recognize user-defined patterns on all 31 channels or on any subset thereof. The word recognizers can also be complemented, i.e., they can recognize the absence of a pattern.

The counters can count up to 65,534 events, microseconds, or milliseconds. Execution of commands (such as qualifying data or triggering) can be conditioned upon a counter reaching a user-specified value.

The state machine architecture provides tremendous flexibility in triggering. Occurrences of events (counters reaching user-specified values, word recognitions) are input to the state machine. The state machine can

examine all of its inputs simultaneously and generate a set of simultaneous commands to the counters, trigger(s), and data qualification circuitry. The commands can include a transition into a new state. Different states can associate different commands with the same inputs. The state machine executes in **real time** with the SUT and can enter any of its states in any order, any number of times. This makes the 7D02 ideal for following the complicated, convoluted sequences of bus transactions often associated with software/firmware-based systems. A simple yet powerful user language makes detailed understanding of the state machine unnecessary.

The standard 7D02 contains three memories:

1. **Program Memory** contains the current user-entered program.

2. **Acquisition Memory** (or Main Acquisition Memory) contains the data acquired the last time a 7D02 program was run.

3. **Storage Memory** can be used to save either a program or the contents of the Acquisition Memory.

The PM 100 series of Personality Modules makes it possible to reconfigure the 7D02 for a wide range of microprocessors by simply plugging the appropriate module into the front panel of the 7D02. A General Purpose Personality Module (PM 101) is available for non-microprocessor systems or for systems based on microprocessors for which a specific Personality Module is not available.

Expansion Option

Option 3 increases the width of Acquisition Memory and word recognizition by 16 channels. The 44 channels of memory are generally assigned as:

24 address bus lines
16 data bus lines
4 control lines

As in the basic 7D02, two additional control lines and the external trigger line are also available for word recognition.

Timing Option

Option 1 turns the 7D02 into two logic analyzers in one package. The Timing Option has its own trigger, acquisition memory (Timing Option Acquisition Memory), and word recognizer.

Used synchronously, the Timing Option acts as an 8-channel extension of the Main Acquisition hardware.

Used asynchronously (with its own internally-generated time base), it is a timing logic analyzer that recognizes (and stores) both data and glitch information on 8 channels.

The Timing Option can be used to trigger the main 7D02 and vice versa.

Data in the Timing Option Acquisition Memory are displayed separately from other acquired data. These data may be displayed either in timing diagram or in state table form at the user's option. These eight lines of data are the only lines of data monitored by the 7D02 that can be displayed in timing diagram form.

FUNCTIONAL OVERVIEW

This overview introduces some important terms and concepts. Understanding them may make programming the 7D02 easier.

Using the 7D02 keyboard, the user enters a program describing an event or sequence of events in the system under test. The program usually directs the 7D02 to trigger (acquire data and stop running) when the event or sequence is detected. It may also describe the type of data the user wishes to acquire.

When the program is run, information is extracted from the program to set up the various acquisition hardware components (counters, word recognizers, state machine, clock and data qualifiers, trigger delay counter, etc.).

The acquisition hardware is then activated and data sampling begins. Data is always sampled on an edge of the system under test (s.u.t.) master clock, but not necessarily on every s.u.t. clock edge. The **clock qualification** circuitry (which is set up with information from the user's program and/or

Personality Module-defined defaults) selects the edges of the s.u.t. master clock on which data is considered to be valid. This qualified s.u.t. clock becomes the **7D02 State Clock**, which defines a single **cycle** of the 7D02. Data is sampled only on the State Clock.

On each cycle of the 7D02 (at the State Clock), s.u.t. data is sampled, program-defined conditions are tested, and commands associated with conditions that have occurred are executed. For example, the occurrence of a particular word recognition can cause a counter to be incremented. The state machine checks all of its inputs simultaneously and causes the relevant programmed commands to be executed simultaneously in real time with the system under test.

Although data is sampled on every State Clock, it is not necessarily stored into the Acquisition Memory. The **data qualification** circuitry uses program-defined (or default) criteria to determine whether or not each particular word of sampled data is to be stored. A **word** of data consists of the values on all channels being sampled on the system under test at a State Clock.

Words of data that meet the data qualification criteria are stored in consecutive locations in the Acquisition Memory. Data is stored continuously from the moment the 7D02 begins running the program. Data continues to be stored even after the Acquisition Memory is filled, with the oldest word of data being lost every time a new one is stored.

Execution of a trigger command has the effect of activating a **delay counter** associated with the Acquisition Memory. Once activated, the delay counter increments every time a word of data is stored into the Acquisition Memory. When the value in the delay counter reaches the user-specified value, acquisition is considered to be complete and the 7D02 stops executing the program.

NOTE

The Timing Option has its own trigger and delay counter. If the Timing Option is installed and data is acquired with both the Main and Timing Option sections of the 7D02, then both sections must trigger and both delay counters must reach their programmed values before the program stops executing.

Once the program has stopped executing, acquired data is formatted and displayed. The user is then free to move acquired data to Storage Memory, to move programs to or from Storage Memory, to examine acquired data in different formats, to enter a new program, to rerun the program, etc.

MODES OF OPERATION

Powering-up the 7D02 causes diagnostic routines to be run automatically. Assuming there is no failure, the routines require five to ten seconds to complete. If the 7000-series mainframe is "cold," the diagnostics are usually completed before the CRT warms up. Otherwise, diagnostic displays and test patterns may be seen on the CRT.

After the completion of diagnostic testing, the 7D02 is always in one of five modes of operation. Briefly, in the order they are likely to be encountered, they are:

1. **Programming Mode.** The mode into which the 7D02 powers-up. The user enters the program describing the data to be sought and stored.

2. **Run Mode.** Data is acquired under the direction of the program in Program Memory.

3. **Display Mode.** The acquired data is formatted and displayed on the CRT display.

4. **Immediate Mode.** The user enters commands to be executed **immediately**, rather than when the program is run. These include moving information to or from Storage Memory, changing displays, and changing operating modes.

5. **Format Mode.** Characteristics of program and data displays, such as the radices in which word recognizer fields and acquired data are displayed, can be changed by the user.

OPERATING CONTROLS

The following paragraphs briefly describe the function of each of the front panel pushbutton switches (referred to as "keys"). Refer to Fig. 1-1. Note that the descriptive paragraphs are keyed numerically to the illustration to positively identify the keys. The keys are described in basically a top-to-bottom, left-to-right sequence.

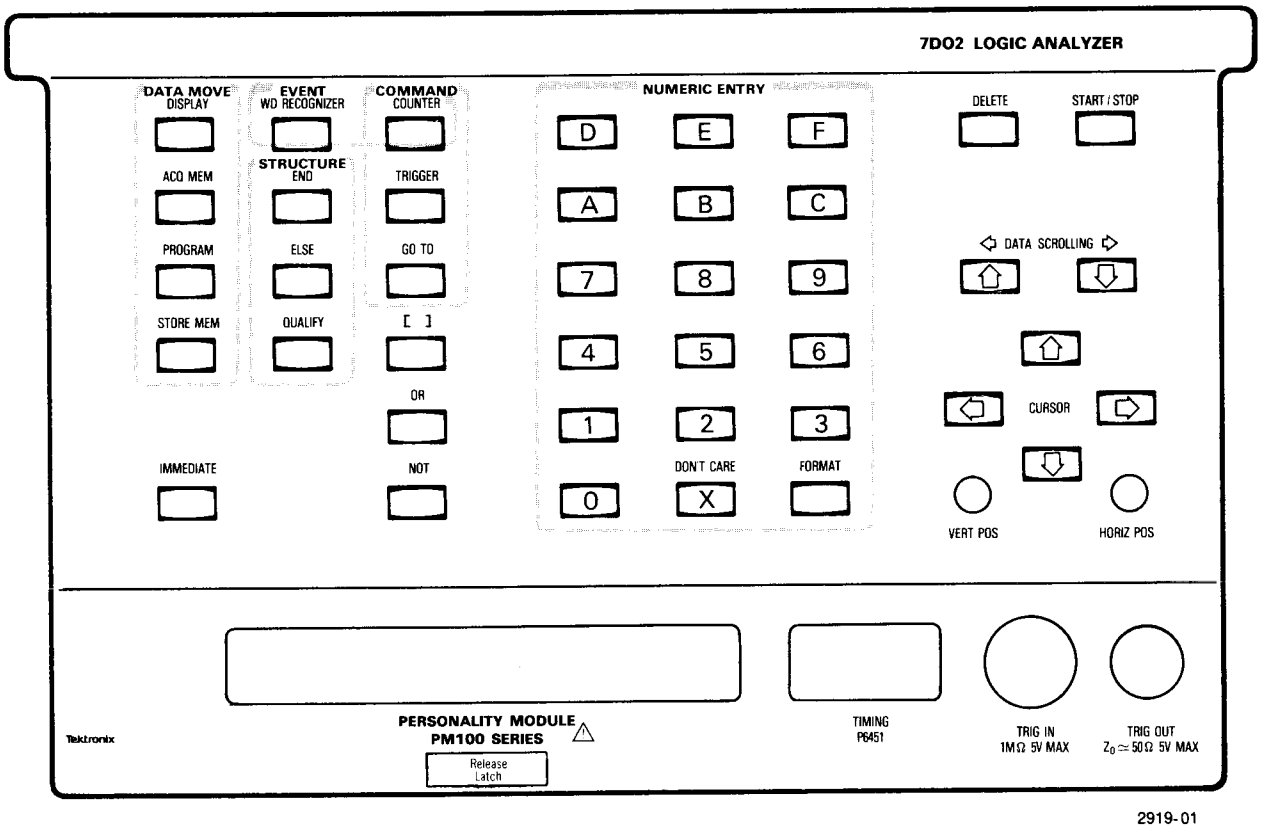


Fig. 1-1. 7D02 Front Panel.

Most keys are grouped by function within colored borders. Briefly, the functions of the key groups are as follows:

- The Data Movement keys are used to move information among the 7D02 memories and to/from the display.

- The Event, Command, and Structure keys, together with the [], OR, and NOT keys, are used to enter the user's program.

- The IMMEDIATE key is used to enter Immediate mode commands.

- The Numeric Entry keys are used to enter command and display parameters.

- The DELETE key removes unwanted items from a program.

- The START/STOP key runs or aborts execution of the current program.

- The DATA SCROLLING keys move a display "window" through acquired data or a stored program.

- The CURSOR keys move the blinking cursor around the screen, allowing programs to be entered/deleted and parameters to be changed.

1. DISPLAY

The **DISPLAY** key is used to specify the CRT as the destination of a data movement command in Immediate mode. It indicates that the contents of the memory selected as the source of the move are to be displayed in the central display area of the screen. The **DISPLAY** key is only valid in the following keystroke sequences:

IMMEDIATE DISPLAY ACQ MEM
IMMEDIATE DISPLAY PROGRAM
IMMEDIATE DISPLAY STORE MEM

The last keystroke in each sequence is the source for the move. As soon as the source key is pressed, the source memory is displayed on the screen and a mode change takes place. The 7D02 enters Programming mode if the source is **PROGRAM** and enters Display mode if the source is **ACQ MEM** or **STORE MEM**.

2. ACQ MEM

The **ACQ MEM** key is used to specify the Acquisition Memory as the source of a data movement command in Immediate mode. If the Timing Option is installed, a menu allows the user to distinguish the Main Acquisition Memory from the Timing Option Acquisition Memory. The **ACQ MEM** key is only valid in the following keystroke sequences:

IMMEDIATE DISPLAY ACQ MEM
IMMEDIATE STORE MEM ACQ MEM

The **IMMEDIATE** key puts the 7D02 into Immediate mode. The second keystroke in each sequence indicates the destination to which the contents of the Acquisition Memory are to be moved.

3. PROGRAM

The **PROGRAM** key is used to specify Program Memory as either the source or destination of a data movement command in Immediate mode. It is valid only in the following keystroke sequences:

IMMEDIATE DISPLAY PROGRAM
IMMEDIATE STORE MEM PROGRAM
IMMEDIATE PROGRAM STORE MEM

The **IMMEDIATE** key puts the 7D02 into Immediate mode. The second key in each sequence is the destination of the data movement. The third key in each sequence is the source.

4. STORE MEM

The **STORE MEM** key is used to specify the Storage Memory as the source or destination of a data movement command in Immediate mode. The **STORE MEM** key is only valid in the following keystroke sequences:

IMMEDIATE DISPLAY STORE MEM
IMMEDIATE STORE MEM ACQ MEM
IMMEDIATE STORE MEM PROGRAM
IMMEDIATE PROGRAM STORE MEM

The **IMMEDIATE** key puts the 7D02 into Immediate mode. The second

keystroke in each sequence indicates the destination of the data movement. The third keystroke indicates the source.

5. IMMEDIATE

Pressing the **IMMEDIATE** key puts the 7D02 into Immediate mode, i.e., makes it ready to execute a command immediately as opposed to entering one into a program.

Each time the **IMMEDIATE** key is pressed, the command currently in the Immediate area (at the bottom of the screen) is deleted. The blinking cursor then appears at the beginning of the area, indicating readiness to accept a new command.

Valid Immediate mode commands fall into two categories: Data Movement and the GOTO command. Data movement is further subdivided into non-destructive (Display) and destructive data movements. Legal keystroke sequences in the immediate area are:

IMMEDIATE DISPLAY ACQ MEM
IMMEDIATE DISPLAY PROGRAM
IMMEDIATE DISPLAY PROGRAM
IMMEDIATE DISPLAY STORE MEM

IMMEDIATE PROGRAM STORE MEM
IMMEDIATE STORE MEM PROGRAM
IMMEDIATE STORE MEM ACQ MEM

IMMEDIATE GOTO (optional test #)

Except for the GOTO command, each keystroke pair indicates a destination followed by a source for a data movement command. The first three sequences above are executed as soon as the last keystroke is entered and cause transition into a new mode of operation (Programming or Display). The rest are executed only when the cursor is moved onto the "EXECUTE" that appears at the end of the command. Until then, **CURSOR** and digit keys can be used to change parameters associated with the Data Movement and **GOTO** keystrokes. For more information, see Chapter 3 in the Operator's manual and the entries in this section describing the indivudal keys involved.

6. WD RECOGNIZER

The **WD RECOGNIZER** key permits the user to define a word recognition event in a 7D02 program. The event is TRUE when the incoming data matches a pattern entered by the user.

The 7D02 provides four distinct Word Recognizers. Each may be programmed with a different pattern. Each may appear any number of times in a test or program. Only the Word Recognizer(s) in the current Test and the Qualify block (if any) are evaluated when the program is running.

The numeric keypad is used to enter the pattern to be recognized into a multi-line "form" that appears on the screen when the **WD RECOGNIZER** key is pressed. Any Personality Module channel for which "X" ("DON'T CARE") is entered will be considered to match the incoming data on that channel regardless of the actual value of the data. The event is TRUE when the incoming data on **all** the channels match the corresponding entries programmed into the Word Recognizer; i.e., the value of the Word Recognizer is the AND of the matches on the individual channels.

Each Word Recognizer in the standard 7D02 can recognize up to 31 bits, usually grouped as 8 data bus bits, 16 address bus bits, 6 control bits, and a single bit for the External Trigger In line. The Expansion Option increases Word Recognizer size to 46 bits (usually 16 data, 24 address, and 6 control). Installation of the Timing Option adds a single Timing Option link bit to the 7D02 Word Recognizers.

7. END

The **END** key is used to terminate a Test or Qualify block in a program.

Subsequent legal keystrokes are automatically entered into the next unused Test, or into the Qualify block if the **QUALIFY** key is pressed after the **END** key.

8. ELSE

The **ELSE** key replaces an event in a program and indicates that the following command or compound command is to be executed whenever **none** of the events in the Test are TRUE. It may be entered as the first keystroke in a Test, or whenever an "IF" or "OR IF" prompt appears in a program.

The ELSE clause may be used once in each Test. It must be the **last** clause in the Test, i.e., no events may follow the ELSE clause in that Test.

9. QUALIFY

The 7D02 samples data from the system under test on every cycle (as determined by the State Clock--see Section 2). The default operation is to store every word of sampled data into the Acquisition Memory. The **QUALIFY** key allows the user to set up criteria that must be met for the sampled data to be stored into Acquisition Memory on any given cycle.

When used as a Structure key, **QUALIFY** creates a Qualify block. The Qualify block is always active when the program is running, regardless of which of the Tests in the program is currently active. The block is defined by pressing the **QUALIFY** key, followed by an event key (or compound event), followed by the **END** key. A compound event may include complemented events (i.e., the **NOT** key may be used). Data is stored into Acquisition Memory only on those cycles on which the event in the Qualify block is TRUE.

When used as a Command key, **QUALIFY** means "store." On every cycle on which the command is executed, the sampled data will be stored into Acquisition Memory (regardless of the status of the event in the Qualify block, if any).

10. COUNTER

The 7D02 has two general-purpose counters. A 7D02 counter can count discrete events or can measure and/or accumulate time intervals. The numeric keypad is used to select the counter mode (i.e., events or time).

A counter command is actually executed only during normal program flow. Through it, the user can direct an event counter to increment or reset to zero, or can direct a time counter to begin accumulating time, to stop accumulating time, or to reset to zero and begin accumulating time.

A counter event is defined in terms of a user-specified terminating value. Once the counter reaches the terminating value, the event becomes TRUE. The numeric keypad is used to program this value into the counter.

Both counters are initialized to a value of zero each time a program is run.

11. TRIGGER

The Trigger command allows the user to indicate the point of interest in the data being sampled by the 7D02. It defines the window within which data gathered from the system under test is to be stored in the Acquisition Memory.

By specifying the location of the trigger point within the acquired data, the user indicates a value for the delay counter associated with the Acquisition Memory. Execution of the Trigger command activates the delay counter. The delay counter then increments once with each word of data stored into the Acquisition Memory. Acquisition is considered to be complete when the counter reaches its programmed value. The program is then stopped and the 7D02 switches to Display mode.

The trigger, in conjunction with the delay counter value, defines the data window. If the delay is D, the number of words of data acquired after the trigger is D, and the number of words acquired up to and including the trigger is [256-D] (or less, if fewer than [256-D] qualified storage cycles preceded the trigger).

Data acquisition and program execution stop when each memory (Main, Timing, or both) for which a Trigger command appears in the program has triggered and has had its delay counter reach its programmed value. Therefore, triggering indirectly leads to the transition from Run mode to Display mode.

If the Timing Option is not installed, every execution of a Trigger command also causes the External Trigger Out line to go TRUE (high). If the Timing Option is installed, raising this line is a little more complicated; for full details on programming External Trigger Out, see Chapter 7 in the Operator's manual.

12. GOTO

When executed, the **GOTO** command causes the 7D02 to transfer control to one of the tests in the current program. The specified test becomes active and all other tests in the program are deactivated.

When used in a program, GOTO is executed when it is reached in normal program flow.

When GOTO is used as an Immediate mode command, the user enters the keystroke sequence **IMMEDIATE GOTO** and an optional test number. The command is not executed until the blinking cursor is moved (with the . or . key) onto the EXECUTE field that appears in the Immediate area. This allows the user to change the test number appearing with the GOTO. The effect of executing the command is to put the 7D02 into Run mode and start execution of the program currently in Program Memory at the specified test.

13. []

The **[]** key is used to combine events to form compound events or to combine commands to form compound commands.

When pressed after an "IF", "OR IF", or "STORE ON" prompt, the **[]** key generates an "open bracket" indicating the start of a compound event. The next use of the key closes the bracket, terminating the compound event. Between brackets, event keys and the **OR** key can be pressed in an "event OR event OR ... OR event" sequence. The event keys can also be preceded by the **NOT** key to negate component events. The compound event is TRUE when any one (or more) of the component events comes TRUE.

When pressed after a "THEN DO" or "ELSE DO" prompt, the **[]** key generates an "open bracket" on the screen, indicating the start of a compound command. The next use of the key closes the bracket, terminating the compound command. Any number of command keys may be entered between the brackets. The commands are connected with an implied logical AND operator, i.e., execution of the compound command during normal program flow implies simultaneous execution of **all** the component commands within the brackets.

14. OR

The **OR** key is used within brackets to form compound events within a 7D02 program. Each event within a compound event must be followed by either an **OR** and another event, or by a **[]** keystroke to terminate the compound event.

The implication of the OR is that the compound event is TRUE when one or more of the component events is TRUE. The component events within a compound event are evaluated simultaneously.

15. NOT

The **NOT** key allows the user to complement an event, i.e., to define an event as a counter **not** having reached its terminating value or as a Word Recognizer **not** matching a word of data.

A **NOT** key can only appear within the brackets of a compound event, either immediately following the opening bracket, or after an **OR**. It must be immediately followed in the program by an event (**WD RECOGNIZER** or **COUNTER**). It affects only the single event immediately following it. It cannot be used to negate a compound event as a whole.

16. Digit Keys (0-9, A-F)

The digit keys (**0 - 9** and **A - F**) provide a hexadecimal keypad that is used to make menu selections and enter numeric parameters.

Menu and numeric values may be changed by moving the blinking cursor to the menu or numeric field to be modified and pressing the appropriate digit key(s). As each digit is entered, it replaces the previous value, and (except on Format mode menus) the blinking cursor moves to the next digit position.

17. DON'T CARE

The **DON'T CARE** key can be used for certain numeric fields related to the Personality Module and Timing Option channels to indicate that the user is not concerned with the values on the corresponding channels.

The **DON'T CARE** key displays as an "X".

18. FORMAT

The **FORMAT** key switches the 7D02 to or from Format mode. It has no effect when a program is running (Run mode), however. Format mode produces a special display on the screen, temporarily replacing whatever was displayed before. The display includes menus and numeric fields that allow a user to change the form of data to be entered or displayed on the 7D02 screen. For example, the user can:

- change the radices of Word Recognizer fields, acquired data displays, etc.

- enable or disable the highlighting of differences between Storage Memory and Acquisition Memory in Display mode.

- enable and disable the display of acquired glitch information in the Timing Option data displays (if the Timing Option is installed).

- invert the Timing Option data channels (if the Timing Option is installed) and/or the system under test buses (if the PM101 General Purpose Personality Module is attached). Inversion of a channel means that word recognizer values entered for the channel are complemented before being used, and data gathered on the channel is complemented before being displayed.

The Format mode display varies depending on the Personality Module attached and the presence or absence of the Timing Option. Pressing the **FORMAT** key a second time restores the original display and operating mode of the 7D02.

19. DELETE

The **DELETE** key removes unwanted items from the end of the program currently in Program Memory. Generally, a program item consists of all of the lines in a program that are associated with a single programming keystroke. (The programming keys include the Event keys, Command keys, Structure keys, [], **OR**, and **NOT**).

The **DELETE** key only works when the blinking cursor is at the end of the program or on one of the lines associated with the last item in the program.

20. START/STOP

Pressing the **START/STOP** key while in Programming, Display. or Immediate mode causes the 7D02 to attempt to execute the program currently in Program memory. If the program contains no errors, the 7D02 enters Run mode at Test 1 of the program.

Pressing the **START/STOP** key while the 7D02 is in Run mode causes it to stop acquiring data and terminate executing of the program. The 7D02 then enters display mode.

21. DATA SCROLLING

During Display mode, the two **DATA SCROLLING** keys are used to scroll through the displayed memory (Storage Memory or one of the Acquisition Memories). The **CURSOR** keys cannot be used for this purpose because they are associated with the blinking cursor which remains in the Immediate area during Display mode (the blinking cursor can be used to modify parameters of the display command there).

Each **DATA SCROLLING** key is associated with two arrows. The ◀ and ▶ arrows on the front panel are for the Timing Diagram, which scrolls horizontally. The ▲ and ▼ arrows on the keys are for the other displays (Timing State, all Main Acquisition Memory displays, and stored Programs) which scroll vertically.

The ▲ / ◀ key scrolls toward the beginning of data; the ▼/ ▶ key scrolls toward the end of data. The arrows indicate the direction in which

the data window moves. The data actually appears to move in the opposite direction. This, however, is consistent with the manner in which the **CURSOR** ↑ and **CURSOR** ↓ keys work. The data window is defined in terms of a data cursor, which indicates the viewer's current position in the viewed memory. The Timing displays contain explicit data cursors; the data cursor for Main Acquisition Memory displays and stored-program displays is implied, and always at the top line of the display.

22. CURSOR

The four CURSOR keys (↑,↓,←,→) move the blinking cursor in the direction indicated by the arrow on the key

The only valid positions for the blinking cursor are digits of numeric fields, menus, the EXECUTE field that appears after certain Immediate mode commands, and the end of a program or Immediate mode command.

The ↑ key moves the cursor up to the next line containing a valid cursor position. It places the cursor on the leftmost position on that line. If there are no legal positions above the cursor, the cursor moves to (or remains on) the leftmost position on the current line.

The ↓ key moves the cursor down to the next line containing a valid cursor position. It places the cursor on the leftmost position on that line. If there are no legal positions below the cursor, the cursor moves to (or remains on) the rightmost position on the current line.

The ← key moves the cursor to the next legal position to the left. If there are no more legal positions on the same line, it works like the ↑ key, except that it places the cursor on the rightmost position of a line.

The → key moves the cursor to the next legal position to the right. If there are no more legal positions on the same line, it works like the ↓ key.

Position Controls and Connectors

Display Positioning Potentiometers

The VERT POS and HORIZ POS potentiometers allow the user to position the display vertically and horizontally. Due to differences in 7000 series mainframes, it may be necessary to adjust the display position for a particular mainframe. Once adjusted, there should be little need to readjust.

TRIG IN and TRIG OUT

The "TRIG IN" BNC allows devices such as a coded scope probe or the A6701 18-bit word recognizer to trigger the 7D02. This input is TTL compatible. This line is labeled "EXT TRIG IN" in 7D02 program displays.

The "TRIG OUT" BNC allows the 7D02 to trigger other instruments. The TRIG OUT signal is generated when a trigger command is executed. See Section 7 for details.

P6451 Probe Slot

The P6451 probe plugs into the P6451 Probe slot. The P6451 is used to acquire data with the Timing Option.

Personality Module Slot

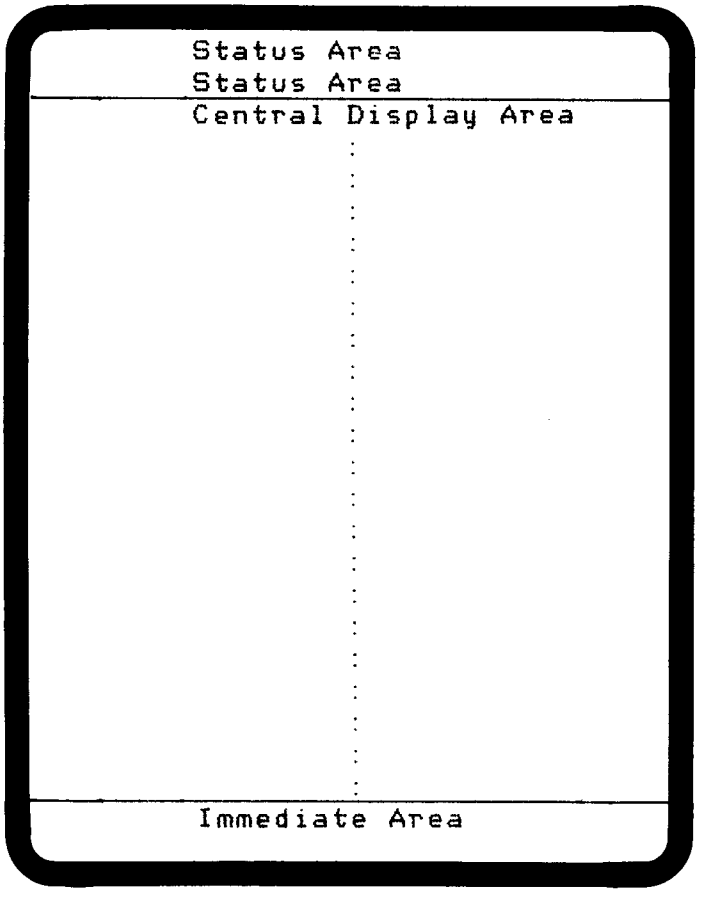
The PM-100 Series Personality Module plugs into the Personality Module slot. The Personality Module configures the 7D02 for a particular microprocessor. It acquires data from the s.u.t. and determines data display formats, disassembly of data, word recognizer formats, etc.

The 7D02 should not be operated without a Personality Module connected. The Module should not be plugged in while the 7D02 is powered up. To do so could cause permanent damage to the 7D02 or to the Personality Module.

Display Screen Characteristics

Screen Layout

Once diagnostics have been completed, the 7D02 display is generally divided into three regions (see Fig. 1-2).



2919-02

Fig. 1-2. Display Regions

They are:

1. **Status Area.** Two lines of inverse video at the top of the screen are reserved for error and informational messages. Monitoring information appears there during Run mode. Vital statistics (such as final counter values) appear during Display mode.

2. Central Display Area. The bulk of the display (a varying number of lines, depending on the size of the Immediate area) is used to display the contents of one of the memories (Program, Acquisition, or Storage) or the Format mode display.

3. Immediate Area. An inverse-video area at the bottom of the screen is used for the entry of Immediate mode commands. When the user is not in Immediate mode, the area contains the last display command entered in Immediate mode (i.e., the one responsible for the current contents of the Central Display area). During Display mode, parameters associated with the display command can be manipulated. During Format mode, this area disappears completely.

Parameters

Program and other parameters are entered with the Numeric Entry keys. User-changeable parameters always appear on the display as digits in the opposite video mode as their background (i.e., inverse video in the Central Display area, normal video in the Immediate area). There are two types of parameters that appear in 7D02 displays (see Fig. 1-3).

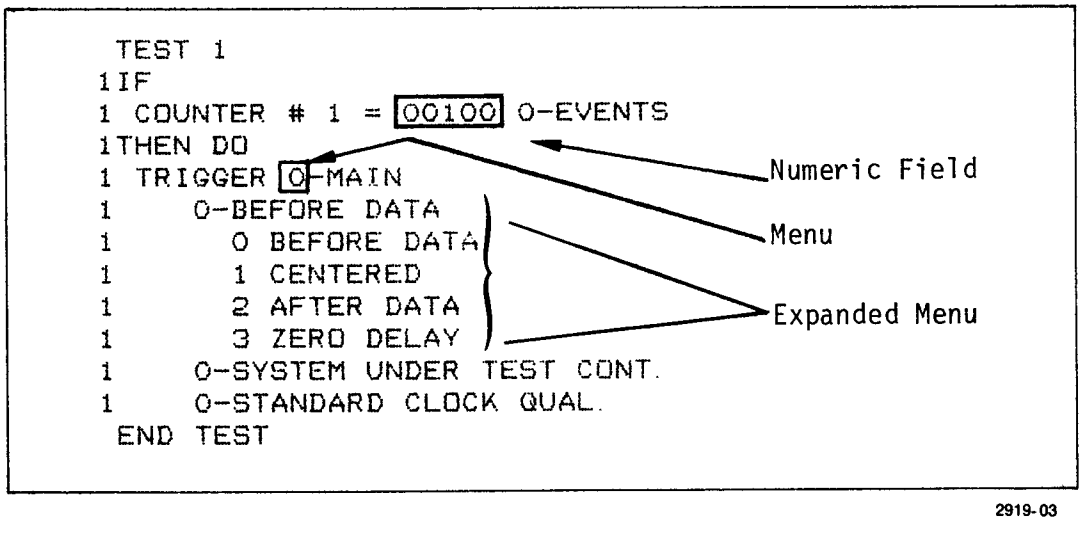


Fig. 1-3. 7D02 Display Parameters.

1. A **menu** gives the user a number of choices, each labeled with an arbitrary digit. The user selects a choice by moving the blinking cursor to the menu and pressing the digit key associated with the desired choice. Only the current selection for the menu is displayed, unless the user positions the cursor onto the digit associated with the selection; at that time, the menu is "expanded" to display all possible choices. Since there is only one cursor, only one menu can be expanded at any time.

2. A **numeric field** is a parameter for which the digits entered have meaning of themselves, i.e., they are not used for selection of a choice but actually are the parameter values.

SECTION 2

THEORY OF OPERATION

BLOCK DIAGRAM DESCRIPTION

Introduction

The 7D02 is a programmable logic analyzer used in design and development of microprocessor and microcomputer systems. It is based upon a state machine architecture and consists essentially of two functional analyzers that can be used separately or in conjunction. The Main section is a synchronous 28 stored channel logic analyzer (44 stored channels with the Expansion Option). The Timing Option section is an eight stored channel logic analyzer capable of both synchronous and asynchronous operation.

The Main section architecture (see Fig. 2-1.) is that of a general-purpose synchronous logic (state) analyzer with replaceable interface (personality) modules to adapt to different systems under test. In operation, the instrument senses data applied to the personality module and uses those data to develop qualifications and triggers under program control to store information surrounding an operational point of interest in the system under test. The Main section includes 30 bus lines (16 address, 8 data, and 4 control lines, all of which are applied to both Word Recognizer and Acquisition Memory circuit blocks; and two control lines that are applied only to the Word Recognizer block), seven lines that are applied to the Front End circuits (six control lines plus the raw clock), one external trigger line, and one Timing Option link bit line. The Expansion Option, which allows the 7D02 to operate with 16-bit microprocessors and other systems, extends the address lines to 24 and the data lines to 16.

Through the Personality Module, the 7D02 is "personalized" to fit the system under test. The Personality Module plugs into the system under test in place of its microprocessor or otherwise connects into the system bus, providing the 7D02 access to the address, data, and clock lines of that system. Dedicated Personality Modules are available for a wide range of microprocessor systems. A General Purpose Personality Module (PM101) is available for custom interconnection to other types of systems.

The Timing Option adds the capability for fast asynchronous sampling of data for development of hardware timing circuits. This option can be

used as either an independent eight-channel asynchronous logic analyzer that can use the main section to define its trigger, or as an extension of the main section, providing monitoring for eight additional lines in synchronism with the main section clock. The option includes a separate memory, called the Timing Option Acquisition Memory, used to store the eight lines of data. These data are acquired through a separate Timing Option probe, the P6451.

Data in the Timing Option Acquisition Memory are displayed separately from other acquired data. These data may be displayed either in timing diagram or in state table form at the user's option. These eight lines of data are the only lines monitored by the 7D02 that can be displayed in timing diagram form.

As shown in Fig. 2-1, the 7D02 may be conveniently divided into two parts, the Main section, and the Timing Option section. The Main section consists of all blocks in Fig. 2-1 except the P6451, IC Acquisition, and the Trigger and Time Base blocks. The Timing Option section consists of the three above listed blocks.

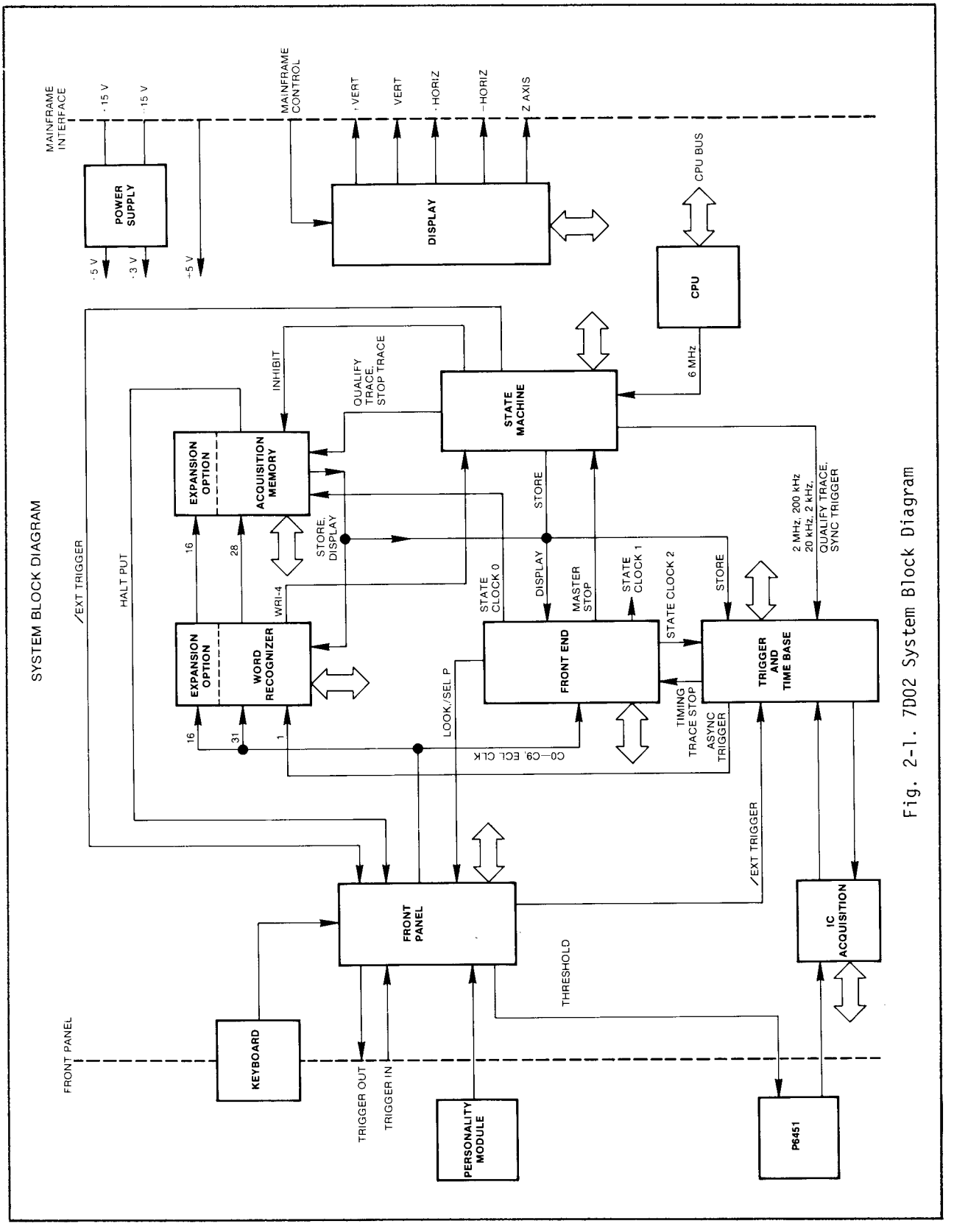


Fig. 2-1. 7D02 System Block Diagram

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Main Section

Housekeeping functions of the Main section are performed by the Keyboard, CPU, and Display circuit groups. The keyboard allows the operator to communicate commands and other program information to the logic circuits. The CPU processes information from the keyboard and other sources and provides overall control functions, while the Display circuits provide result indications and program prompts. In operation, the Display circuits present both program prompts and options; that is, the operator is notified not only of those actions that are necessary and permissible, but also of those actions that are not permissible. The Display circuits are character-oriented, translating and formatting data from the CPU for display on the mainframe screen.

Internal communication among these circuit blocks is accomplished over the CPU parallel data bus (16 address and 8 data bits). The keyboard communicates through the Front Panel circuits. Through the bus, the CPU exercises operational control over the processing and decision circuits in the 7D02, performing such tasks as setting up the word recognizer and time base values, and reading out data for display.

Interface between the 7D02 and the system under test is provided by a set of Personality Modules containing specialized circuits that transform signals in that system to the standard format of signals required by the 7D02. These circuits include very fast clock circuits to transfer the system clock signal to the 7D02 with as little propagation delay as possible. Signals from the Personality Module are applied to the Front Panel circuit block for distribution.

The Front End circuits receive the clock and control lines (C4 through C9) from the Personality Module (through the Front Panel circuits) to generate the qualified clock signals for timing 7D02 operations. Control signals from the Acquisition Memory and Timing Option circuits are processed in the Front End circuits to start and stop real time operations. Principal signals from the Front End circuits include STATE CLOCK 0, which is the raw data clock from the Personality Module used to time START/STOP operations; STATE CLOCK 1, a pulse-shaped clock that runs only during acquisiton and is used in all Main section circuit blocks; STATE CLOCK 2, a pulse-shaped clock that runs continuously and is used in the Timing Option section during synchronous operations; and the MASTER STOP signal, which is effectively the end of acquisition mode and the start of display mode.

The Word Recognizer circuit block contains four separate word recognizers that may be used relatively independently under program control. Address and data signals from the Personality module (applied through the Front Panel circuits) are loaded into input latches in both the Word Recognizer. Each word recognizer compares input data with a value entered by the operator at the keyboard. Upon recognition of a data match, the word recognizer signals the State Machine circuits, which take the appropriate action determined by the executing program. (It is also possible to enter "don't care" values, X's, into a word recognizer.) If a match occurs, the State Machine outputs change to any of the following: changing to another test, starting or reloading a counter, stopping acquisition, or qualifying data. Note that the width of the word recognizers is extended from 32 bits (including the timing option link bit and the external trigger input line) to 48 bits by the addition of the Expansion Option. All circuit operations are basically the same.

The Acquisition Memory circuit block contains a 256-bit, 28-channel RAM; the address, store, and read control circuits to operate the RAM; and the latches that temporarily store input data from the first latch. Input data are loaded into the input latches at STATE CLOCK 1 time and then loaded in the RAM. If the address counter is not enabled by the QUALIFY TRACE signal from the State Machine circuits, the address is not incremented and the next data set is written over the previous set in the same RAM location. From the RAM, data are read by the CPU over the CPU bus during display mode for application to the Display circuits. Note that the acquisition memory RAM space is increased by 16 channels, to a total of 44, by the addition of the Expansion Option. All circuit operations are basically the same.

The State Machine circuit block contains the state machine and two 16-bit counters plus input/output and associated control circuits. The state machine is implemented using RAM circuits and is thus much more versatile through programmability. Event and/or time counting functions are accommodated by the two counters. Primary inputs to the state machine are the CPU bus, four word recognizer signals, and the STORE signal (from the acquisition memory). Outputs include the QUALIFY TRACE and STOP TRACE TRIG signals, which control storage in the acquisition memory and SYNC TRIGGER, which controls Timing Option section operations.

Timing Option Section

The Timing Option section is operable either alone or in conjunction with the Main section, including being triggered by the Main section. The section consists of the P6451 probe, IC Acquisition, and Trigger and Time Base circuits. Input data on eight channels are applied through the P6451 probe to the IC Acquisition circuit block. This block includes the Timing Option Acquisition Memory and the Timing Option Word Recognizer plus associated input/output and control circuits. These circuits operate in the same manner as the similar circuits in the Main section. In synchronous operation, the circuits function as an extension of the Main section, adding eight data channels and a word recognizer. In asynchronous operations, control signals are provided by the Trigger and Time Base circuit block.

The Trigger and Time Base circuit block contains the circuits that allow the Timing Option section to operate asynchronously. These include the time base, trigger, asynchronous filter, sequencer, delay counter, and processor address decoder circuits. The time base is generated as required from either an internal 100-MHz oscillator or various lower-frequency inputs from the State Machine circuit block. If the Timing Option section is operated synchronously, triggering is caused by the SYNC TRIGGER signal from the State Machine. If the section is operated asynchronously, the Timing Option section is armed by the SYNC TRIGGER signal from the State Machine and is then triggered by a match from its own word recognizer.

Operation Sequence

For purposes of explanation, assume that this simple program has been loaded at the keyboard: If Word Recognizer #1 equals 0000 on the data bus, the Main section and Timing Option section will both trigger in synchronous operation. Both sections have been delayed to "after data" position, the system under test is not being halted, and no data qualification is being done. The general purpose Personality Module (PM101) is being used.

The CPU loads the RAMs and latches in all blocks as appropriate for the program, sets up the Word Recognizers, the State Machine, the Front End circuits, the timing trigger, and the IC Acquisition circuits. When the START/STOP key is pressed to run the program, the STORE signal from the Acquisition Memory block starts the acquisition process. Storage takes place at a 10-MHz rate.

Data are applied to both the Word Recognizers and Acquisition Memory. Control lines and clock are applied to the Front End circuits. However, since no clock qualification is called for in the program, the control line inputs are not used. The word recogniton search process is performed each time data are loaded until a match (0000) is found in Word Recognizer #1.

Until the word recognition occurs, data are continually loaded into the Acquisition Memory RAMs. After 256 load cycles, the memory load starts again at the beginning of memory. When the word recognition match occurs, Word Recognizer #1 signals the State Machine, which sends a STOP TRACE TRIG signal to the Acquisition Memory. This signal initializes a delay counter which then counts 16 qualified clocks and halts the main section acquisition. For the Timing Option section, the stop process is initiated by the State Machine issuing a SYNC TRIGGER signal. This signal initializes a delay counter which then counts 16 qualified clocks and halts the Timing Option section. (Remember that, for this program, the Timing Option section is being operated synchronously as an extension of the Main section.)

At the point of stopping acquisition, conditions are that the trigger has occurred, there are 239 locations of good data before the trigger, and there are 16 locations of good data after the trigger. (This is established by selecting the "after data" position.)

The CPU then sets up the circuits to read and display the acquired data as required in the program. Since the Timing Option section is being used, those data may be displayed, at the operator's option, in timing diagram form. All other data must be displayed in state table form. This completes one operational cycle of the program.

The preceding description is one of many possible (2304) different 7D02 operational cycles. Refer to the Operators Manual for more information.

SIGNAL TITLE DEFINITIONS

Introduction

This is an alphanumeric listing of the mnemonic titles that identify signals within the 7D02 and its internally-installed options. The listing includes the signals that are unique to a single assembly and those that are common to two or more assemblies. Following the signal title is the point of origin by diagram number, and circuit designator. An example follows this paragraph. Following the point of origin is the definition, a brief statement of the purpose of the signal, and where appropriate, the timing relationship it bears to some known point. The signal may also be a derivative of some other signal. In such cases, the "parent" signals are mentioned. Also, a signal may be controlled by several devices, as in a wire-OR configuration. All sources are mentioned in these cases.

Example:

Name **Signal Source** **Description**

STORE: Diagram 7: U6040B -- The STORE signal controls the Store operation of the Acquisition Memory circuits. It is high during the Store cycle, and low during the Display cycle.

Mnemonic Listing

A: Diagram 8A: U5050 -- The A signal is applied to the Counter Control Multiplexer to select either the 1 MHz or 1 kHz clock for application to Counter 1.

/ACQ MEM SEL: Diagram 9A: U4080-11 -- The /ACQ MEM SEL signal is one of the hardware addresses from the CPU. The signal corresponds to address page 3:Exxx. When low the signal enables reading the Acquisition Memory.

ADØ-AD7: Diagram 9A: U3050-12 through 19 -- These eight lines are part of the internal data bus on the CPU board. The lines are not buffered, and carry both address and data words at different times in the Microprocessor cycle.

AIØ-AI15: Diagram 5B: -- These signals are from the Personality Module. They carry the address word to be applied to the Word Recognizer and Memory.

AIØ-AI11: Diagram 4A: U1010 and U2010 -- These 12 lines carry buffered addresses from the CPU to the Personality Module.

AILØ-AIL15: Diagram 5B: U1040 and U2040 (CPU), or U2020 and U3020 (probe) -- These interfaced, latched address lines carry the address words from either the Personality Module or the CPU to the Word Recognizer and Memory.

AI16-AI23: Diagram 1B: -- These lines come from the Personality Module carrying the eight-bit word used in the Expansion Option section.

AIL16-AIL23: Diagram 6: U1010 -- These eight lines are the expansion of the AILØ-AIL15 lines defined above, and are used only with the Expansion Option section.

AL16-AL23: Diagram 6: U2020 -- These eight lines are the output from the Pipeline Latch Register on the Expansion Option board.

ALE: Diagram 9A: U3050 -- The ALE signal comes from the Microprocessor as the address latch enable signal. It occurs during the first clock state of a machine cycle.

ASYNC TRIG: Diagram 3A: Q7041 -- The ASYNC TRIG signal is the filtered or unfiltered trigger signal from the Timing Option section. It is applied to the Word Recognizer circuits as one of the inputs for pattern recognition.

/AØØØ-BFFF: Diagram 9A: U4040 -- This line is one of the eight major address lines to the CPU memory. When low, it enables U4030 (9B), one of the ROMs.

AØ-A15: Diagram 9A: U3065, U4070, U3050 -- These are the unbuffered address lines from the CPU. Note that the A12-A15 lines are only used on the CPU.

B: Diagram 8A: U5050 -- The B signal is applied to the Counter Control Multiplexer to select either the 1 MHz or 1 kHz clock for application to Counter 2.

BDØ-BD7: Diagram 1A: U2055, U3055 -- Buffered data lines that carry the column data from the keyboard to the CPU and, in the opposite direction, carry the offset data to the DAC, U4045.

BSØ-BS1: Diagram 2C: Q3043, Q3045 -- These two signals are derived from the /RØ and /R1 signals. /BSØ enables reading the Acquisition RAMs when low. /BS1 enables reading the Glitch/Pipeline RAM.

BSC: Diagram 8A: U1010A -- This is the buffered version of the ST CLK 1 signal; it is used to time the State Machine circuits.

/BSC: Diagram 8B: U5020A -- The complement of BSC, /BSC drives part of the Counter circuits in the State Machine.

/BSC2: Diagram 8B: U5010D -- Another complement of the /BSC signal, /BSC2 also drives part of the State Machine Counter circuits.

CHANNEL SW SIG: Diagram 10B: -- This signal is from the oscilloscope mainframe; it shuts off the Z OUT signal during the time that the mainframe circuit is switching channels.

/CHAR: Diagram 10A: U2010 -- This signal moves low for a period of about 293 ns; the low pulse occurs every 2.3 us. /CHAR is used to clock U3010, which produces the RESET HOZ and /INC VERT signals.

CHØ-CH5: Diagram 10A: U2030A,U3030B -- Used to time the Cursor Position Detector. These signals correspond to the characters written on the display.

CIØ-CI9: Diagram 1B: -- The interfaced control signals that come from the Personality Module.

CIIØ-CII5: Diagram 4B: U4010 -- These six interfaced signals are buffered versions of the CIØ-CI5 signals from the Personality Module.

CILØ-CIL7: Diagram 5B: U5030, U4040 -- The latched CIIØ-CII5, S.E. TRIG, and ASYNC TRIG signals, from the Personality Module, Front Panel, and Timing Option circuits, respectively.

CLK, /CLK: Diagram 1B: -- Complementary clock signals from the Personality Module. The frequency of the signal varies with the type of module.

CLOCK 1: Diagram 8C: U2040 -- Drives the State Machine Counter 1 circuits. Depending on the code sent to the input of U2040, the CLOCK 1 signal is ground, a modified form of the ST CLK 1 signal, the 1 MHz or 1 kHz clock from U6040, or the /MWR2 signal from the Write Decoder.

CLOCK 2: Diagram 8C: U3040 -- Virtually identical to the CLOCK 1 signal, except that the /MWR3 signal is used instead of the /MWR2 signal, and the CLOCK 2 signal drives the Counter 2 circuits.

/CNTR 1: Diagram 8C: U3010 -- Indicates termination of count by the Counter 1 circuits.

/CNTR 2: Diagram 8C: U4010 -- Indicates termination of count by the Counter 2 circuits.

CNT WR EN: Diagram 8A: U5050 -- The CNT WR EN signal is one of two signals that control output selection by Multiplexer U2040.

/CNT WR EN: Diagram 8A: U4030D -- Sent to the R/W Decoders in Counter 1 and Counter 2 of the State Machine to control the Instruction Enable input to each counter.

/CNT 1: Diagram 8C: U2030B -- Goes low when Counter 1 overflows.

/CNT 2: Diagram 8C: U3030A -- Same as above, except that it applies to Counter 2.

COUNTER RESET READ: Diagram 8C: U2040 -- Indicates the reset status of either Counter 1 or Counter 2, depending on the state of U2040. In one case, the output passes the 95 counter control code.

/CUR CLR: Diagram 10A: U2010 -- This signal moves low for a period of about 293 ns. The low pulse occurs every 2.3 us. The signal is used to initialize the Arbitration circuit.

/CUR EN: Diagram 10A: U2010 -- This signal is simply a different phase from the /CUR CLR signal. It is used to gate the Cursor in the Display circuits.

/CUR POS: Diagram 10A: U1020 -- As above, this signal is like the /CUR CLR signal, but occurs at a different phase.

CIIØ-CII5: Diagram 4B: U1040 -- Buffered versions of CIØ-CI5 from the Personality Module.

/CII7: Diagram 4B: U5010 -- The inverted and buffered form of the CI7 signal from the Personality Module. Used by the CPU to sense the state of the C7 line at the Personality Module input.

CØ-C7: Diagram 1A: U2055 -- Column input data from the keyboard matrix.

DILØ-DIL7: Diagram 5B: U3040, U4020 -- The interfaced and latched data lines from the Personality Module and from the CPU. The lines are fed to the Word Recognizer stages and to the Acquisition Memory stages. The CPU uses this data path for setting a mask in the Word Recognizer.

DISPLAY: Diagram 7A: U6040B -- The DISPLAY signal is one of the more prominent signals in the 7D02. The signal is high when the 7D02 acquisition unit is in the Display mode.

/DISPLAY COMM: Diagram 7A: U2010 -- The /DISPLAY COMM signal is set low by the CPU through the RAM Read Control when a display operation is requested. The /DISPLAY COMM signal is used to reset the Reset Flipflop in the Trigger and Timebase circuits.

/DIV EN: Diagram 4B: U4050 -- This signal comes from the CPU Control circuits. When U4050 receives a "4" code, the /DIV EN signal goes low, then high, to clock 14-bit latch U1020 (on Diagram 4A). This latch conveys the code from the CPU to set up the Programmable Clock Synthesizer circuit.

DIØ-DI7: Diagram 4A: -- These eight lines convey the data from the Personality Module to the CPU via buffer U3010.

DØ-D7: Diagram 9A: U2080 -- These eight data lines are the principal means of transporting data around the 7D02. The bus is shared with other sources: U1020 on Diagram 2, plus U2040 and U6050 on Diagrm 6.

DØ1-D71: Diagram 4B: U1040 -- The eight interfaced lines from U1040 that drive the majority of the gates in the Six-bit Comparator.

/DLY TC: Diagram 3B: U7020D, U7020A, U1030 -- The terminal count output of U1030 is held low to prevent the occurrence of a trigger until the "wait for trigger" state, which occurs when both SEQ Q1 and SEQ Q2 are both high.

DOT CLK: Diagram 10A: U2020F -- The DOT CLK signal is a 3.4133-MHz signal that is used to time Display Section operations.

E/T1: Diagram 8A: U5030F -- This signal, along with the /E/T1, E/T2, and /E/T2 signals, controls the mode of Counter 1 and 2. When E/T1 is high, Counter 1 is in the Events count mode; when the signal is low, the counter is in the Time measurement mode.

/E/T1: Diagram 8A: U5050 -- Complement of E/T1.

E/T2: Diagram 8A: U5030E -- Controls the operating mode of Counter 2 in the State Machine. When E/T2 is high, the counter is in the Events count mode; when the signal is low, the counter is in the Time measurement mode.

/E/T2: Diagram 8A: U5050 -- The complement of E/T2.

EXP Ø-3, EXP 6, 13-15: Diagram 6: U4040, U5040 -- These lines carry the results of the word recognizer comparison from the Expansion Option circuits to the Main Word Recognizer circuits.

/EXT BUS EN: Diagram 9A: U4040 -- This signal is used for two purposes: When low, it enables the passage of data through U4075 on the CPU Board; this is the link from the internal CPU data bus to the Main Data Bus for the 7D02. The signal is also connected to the Display circuits, where it enables (when low) the passage of data from the main bus to the Character ROM.

/ESYNC: Diagram 4B: U2050 -- The product of the ESYNC Comparator, U2050. Inputs to the comparator are data bits from the CPU and control bits from the Personality Module, via the Ten-bit Buffer. The /ESYNC signal is applied to the Programmable Clock Synthesizer for use as one of the control signals.

/EXT TRIG: Diagram 8A: U5010F -- Moves low under one of two conditions: 1) the /SYNC TRIG signal from the State Machine RAM moves high; or 2) the MASTER STOP signal from U4030C on the Front End Board moves high.

/EØ-/E5, /E7, /E9-/E11, /E15: Diagram 3B: U3060 -- These signals are used to trigger and time various operations in the Timing Option circuits. /EØ clocks the data from the Main Data Bus into U8050, the latch that controls the selection of the time base output frequency. The /E1, /E3, /E4, and /E5 signals clock data from the write bus through the latches that control the Input Acquisition stages; the latches are U4010, U5010, U6010, and U7010 on the IC Acquisition Board. The /E2 signal clocks data on the WBØ, WB1, and WB5 lines through U3020 to control the inputs to the Trigger stages. The /E7 signal is applied to U4045 on the Front Panel Board to

clock data into the latch of the DAC. The /E9 signal controls the Load input of U1050 and U2050, part of the timing Option Delay Counter, and /E10 controls the Load input of U2040 and U1030 (through U1040). Thus, the two signals control the loading of the Delay Counter. The /E11 signal clocks the data on the write bus into latch U8030, which controls the amount of delay that is programmed into the Async Filter circuits. The /E15 signal is used to furnish a diagnostic signal from the Time Base circuits.

G: Diagram 8B: U4020A -- The G signal is the product of the /STOP TRACE LATCHED signal, BSC, Ø1, and Y4. The G signal moves low to enable latch U3050, which reads back the qualify and reset signals onto the Buffered Data Bus. The G signal moves low following each applied ST CLK 1 signal (assuming that all other conditions are correct), and is terminated by /STOP TRACE LATCHED.

GLRCG: Diagram 2A, 2B: U4030, U5030, U6030, U7030, U4050, U5050, U6050, and U7050 -- This is the glitch recognition signal output from all eight of the Input Acquisition stages in the Timing Option circuit. The signal moves high when any one of the eight listed stages pulls high on the line. The signal is applied to the Trigger section of the Timing Option.

/HALT ENABLE: Diagram 7A: U2020 -- The /HALT ENABLE signal moves low whenever the CPU calls for a high-speed stop. The signal enables the Halt SUT Generator circuit to stop the SUT (System Under Test) when the DISPLAY signal moves high at the end of the next storage cycle.

/HALT SUT: Diagram 7A: U7010A -- The /HALT SUT signal controls the Syatem Under Test; when low, the line stops the SUT. Conditions that produce the low state are a low on the /HALT ENABLE line, and a high state on the DISPLAY line.

HOLDOFF: Diagram 10C: Q5043 -- The HOLDOFF signal is a buffered version of the RESET VERT signal from U3010B. The signal moves high once each 16.7 milliseconds, and stays high for a few microseconds before returning low. It is used by the oscilloscope circuits to determine hold-off timing.

HORIZ SIG +: Diagram 10C: Q5031 -- A positive-going ramp that is approximately 0.25 volts in amplitude, occurring at a 12.9-kHz repetition rate. The signal drives one side of the oscilloscope horizontal deflection circuits.

HORIZ SIG -: Diagram 10C: Q5032 -- A negative-going ramp that is otherwise identical to the HORIZ SIG + signal.

HORIZ POS: Diagram 16: R3076 -- The DC voltage from this potentiometer is injected into the Ramp Amplifier circuit to position the display on the CRT as required.

/INC VERT: Diagram 10A: U3010A -- This signal moves low momentarily each 77 microseconds. It signifies the end of each 32-character group and causes the Staircase Generator to add a current increment, thus moving the CRT display downward by one vertical increment.

INHIBIT DISABLE: Diagram 8A: U5050 -- Pulled high to disable the Inhibit circuit when diagnostics routines are programmed into the 7D02.

INHIBIT 2: Diagram 8B: U1010B -- The INHIBIT 2 signal moves high at the beginning of a Store cycle, and remains high until just after the second state clock signal has occurred.

/INHIBIT 2: Diagram 8B: U5010B, U5010E -- The complement of INHIBIT 2 just described. The signal is applied to Counter 1 and Counter 2 circuits, and to the Acquisition Memory circuits, in both cases to inhibit circuit activity until the input stages of the 7D02 are cleared.

IO/M: Diagram 9A: U3050 -- This signal from the Microprocessor is low during memory operations of the Microprocessor, and high during I/O operations. It is used as part of the Page Select circuit inputs, to enable U4080 and U4040, and for ancillary functions outside the 7D02 proper.

/LAST ADDR + 1: Diagram 7A: U2010 -- When instructed by the CPU, the RAM Read Control pulls this line low to enable the passage of the memory address from the MAC to the Main Data Bus.

/LATCHES SEL: Diagram 9A: U4080 -- The LATCHES SEL signal is a common enabling signal throughout the 7D02 It moves low to latch data into various buffers and latches.

/LOAD: Diagram 10A: U2010 -- The /LOAD signal is one of the five outputs from the Timing Generator, U2010. The signal moves low for a period of about 293 nanoseconds, at a repetition rate of about 2.34 microseconds. It clocks the Character Counter output into U3010A, controls the shift/load input of the Character Line shift Register, and clocks the Cursor Detector and Inverse Video Control flip-flops.

LOOK: Diagram 4A: U6010G -- Applied to the Personality Module. It goes high after the high level of the PROBE signal is clocked into U6030 by the ALE pulse.

LØ-L3: Diagram 10A: U3030B -- Outputs of the +9 Line Counter circuit. The period of the L3 signal is about 696 microseconds. These signals drive the Character ROM, U1040.

MAØ-MA7: Diagram 6: U3050, U4050 -- These eight lines carry the output of the Expansion Option MAC (Memory Address Counter) to the Expansion Option RAM.

/MAC EN: Diagram 3B: U5030A -- The MAC EN signal is applied to enable the Timing Option MAC (Memory Address Counter). The signal also controls the generation of the /MACTC signal. If the QUALIFY or STATE CLOCK CONTROL signals are low, the /MAC EN signal is held high, which prevents incrementing the MAC.

/MAC TNCK: Diagram 7A: U1025A -- Applied to the Expansion Option circuits to synchronize the reading of Expansion Option memory and the transition from Store to Display modes. This signal moves low whenever STORE moves high, or when the /RD signal is permitted to pass through U5040A and U1010A to control U1025A.

MASTER STOP: Diagram 4A: U4030B -- MASTER STOP moves high when the TIMING TRACE STOP signal from the Timing Option circuits moves high and DISPLAY moves high. If the Timing Option is not installed, the MASTER STOP signal is a copy of the DISPLAY signal.

/MEM EN: Diagram 7A: U2020 -- Moves low to enable the Load input on the MAC, for both the Acquisition Memory and the Expansion option circuits. When this signal is low, the CPU can place an address in the MAC to read the Acquisition Memory.

MAINFRAME MODE INFO: Diagram 10B: P210 -- This signal comes from the Mainframe to control the blanking of the Z-axis signal to the Mainframe. When MAINFRAME MODE INFO and CHANNEL SW SIG are the same state the Z OUT signal is held low, and the display is off.

/MWR1-6: Diagram 8A: U6050 -- These six signals are the output of the Write buffer. /MWR1 is applied to the write enable input of RAM U1060. /MWR2 and /MWR3 combine with other signals at U7040 to create the SELECT

1 and SELECT 2 signals that control R/W Multiplexers U1040 and U4040. /MWR4 is applied to the clock input of U5050; the positive transition of the signal latches the buffered data. /MWR2, /MWR3, and /MWR5 are applied to the Counter 1 and Counter 2 circuits, where the first two increment the counters and /MWR5 is used to set the Reset counters. /MWR6 sets the two flip-flops that generate the INHIBIT 2 signal.

OØ-O7: Diagram 8A: U2060, U5060 -- These eight outputs from the State Machine RAM provide instructions to the State Machine Counters. The instructions include Time Measurement, Event Count, and other forms of mode control.

/PAGE SEL Ø: Diagram 9A: U4065A -- One of two signals, PAGE SELECT Ø and PAGE SELECT 1, that subdivide the RAM address structure and provide four separate address pages that a given address may refer to.

/PAGE SEL 1: Diagram 9A: U4065B -- See /PAGE SELECT Ø.

/PATCH: Diagram 9A: J1001 -- Reserved for future use.

/PE: Diagram 2A: U4010 -- Enables the parallel loading of the MAC, and enables the /BSØ and /BS1 signals to the Acquisition RAM.

PROBE: Diagram 9A: U4055B -- When either /PROBE Ø or /PROBE 1 are low, the line moves high. The signal is applied to U6030 on the Front End Board, where it controls the state of LOOK.

/PROBE Ø: Diagram 9A: U4080 -- One of the two address subdivisions for probe selection. The line goes low to address one half the probe addresses, and high to address the other half.

/PROBE 1: Diagram 9A: U4080 -- Used to create the PROBE SEL signal.

/QC: Diagram 10A: U2020E -- The inverted ÷8 output of U2030, with a period of about 2.34 microseconds. The signal is applied to the enabling inputs of U1040 to reduce its duty cycle.

QUAL TRACE: Diagram 8A: U1060 -- This signal is used to qualify bits in all segments of the 7D02. It is routed to the Acquisition Memory, Expansion Option, Trigger and Timebase, and the IC Acquisition Memory circuits.

QUAL Ø: Diagram 4B: U2030, U2040, and U3020 -- One of two signals that come from the Six-bit Comparator. Control bits from the Personality Module are matched with data bits from the CPU to form a comparison that "qualifies" the output of a pulse from the State Clock 1 Pulse Shaper. The QUAL Ø line is also controlled by U4040B, U6020C, and U6020D.

QUAL 1: Diagram 4B: U3030, U3040, and U4020 -- The same in principle to the QUAL Ø signal, except that it applies to the control of ST CLK 2. This line is also controlled by U4040C and U6020E.

/RAM SELECT: Diagram 9A: U4040 -- The /RAM SELECT signal moves low to enable U1080, the Ram Select Decoder.

/RAW CLK: Diagram 4A: Q6041 -- This signal is the output of the ECL/TTL Translator circuit. It is applied to the ST CLK Ø Buffer, to the Programmable Clock Synthesizer, and to the two Pulse Shaper circuits.

/RBE: Diagram 3B: U3040C -- The low state of /TIM OPT SEL and /RD at the inputs of U3040 pull the /RBE signal low. This enables the Read Buffer, U1020, on the IC Acquisition Memory Board.

RBØ-RB7: Diagram 2C: U2020; Diagram 2A: U5020 and U6020; Diagram 2B: U3020 and U7020 -- These eight lines are the read bus outputs of the Data Acquisition RAM for the Timing Option. The lines are applied in common with the output of U2020 to the output translator stages.

RC-1: Diagram 7B: U4040 -- The overflow output from the MAC; when high it enables U6040 to inform the CPU that the MAC has counted past its capacity.

/RD: Diagram 9A: U4070 -- The /RD signal comes from the CPU through buffer U4070. The signal triggers reading of the Main Interface Bus throughout the 7D02. The /RD signal moves low just following the ALE pulse, assuming that a read operation is selected.

/RD EN Ø-/RD EN 3: Diagram 7A: U2010 -- Upon CPU command, this signal moves low to enable the CPU to read the status of several circuits on both the State Machine and the Acquisition Memory circuits.

/RDPL: Diagram 7A: U2020 -- This signal is used primarily in Diagnostic mode to provide CPU access to the Acquisition Memory.

/READY: Diagram 10B: U3020B -- The /READY signal is used to initiate wait states in the Microprocessor to compensate for the difference in clock rates between the CPU and Display Circuits. The signal is also applied to U3080 in the CPU circuits, which initiates a two-clock delay in the enabling process.

RESET: Diagram 3B: U4040A, U4020B -- The RESET signal is applied to the Sequencer, TC Flag, and Trigger Amplifier circuits. It is high when the /DISPLAY COMMAND signal is high, and returns low at the first ST CLK 2 signal that occurs after STORE moves low.

RESET HOZ: Diagram 10A: U3010A -- The RESET HOZ signal is applied to the Ramp Generator circuit, where it resets the ramp. It is the complement of the /INC VERT signal.

/RESET OUT: Diagram 9A: U4055A -- This signal indicates that the 7D02 Microprocessor is resetting. It is used in the CPU circuits to reset the Page Select flip-flops.

RESET VERT: Diagram 10A: U3010B -- The RESET VERT signal moves high for a short period each 16.7 milliseconds to cause the display to return to the top of the screen. The pulse is applied to the Staircase Generator and turns the reset gate on for a moment to discharge the staircase capacitor.

RESET 1: Diagram 8C: U2030A -- Informs the CPU of the reset status of Counter 1.

RESET 2: Diagram 8C: U3030B -- Same as RESET 1, except that it applies to Counter 2.

RST 6.5: Diagram 9A: -- An interrupt line to the CPU.

RUN/STOP CNTR 1: Diagram 8C: U1020B -- This signal drives U6030A. When high the signal permits the passage of the clock signal from the Divider circuits to Counter 1.

RUN/STOP CNTR 2: Diagram 8C: U2020A -- This signal drives U6030B. When high, the signal permits passage of the clock signal from the Divider circuits to Counter 2.

ROW Ø-ROW 4: Diagram 10A: U4042 -- The outputs of the Row Counter. The lines are applied to the RAM control Multiplexer as one of two sets of data that are time-shared by the multiplexer and applied to the Display RAM.

/RØ-/R4: Diagram 3B: U3050 -- These five signals from decoder U3050 are applied to the IC Acquisition Circuits, where the /RØ and /R1 signals are used to generate the bank select signals to the Data Acquisition RAM. The /R2, /R3, and /R4 signals enable U2010 and U2020.

RØ-R5: Diagram 1A: U2025 -- These six lines carry the coordinates for one axis of the keyboard.

SELECT 1: Diagram 8A: U7040C -- Controls the choice of signals that pass through the R/W Multiplexer, U1040.

SELECT 2: Diagram 8A: U7040B -- Controls the choice of signals that pass through Multiplexer U4040 in Counter 2.

/SEL P: Diagram 4A: U5020A -- Enables reading the PROMs in the Personality Module. The /SEL P line moves low if the PROBE line is high and the /RD line is low.

S.E. TRIG: Diagram 1A: U5025A -- The TRIG IN signal which is applied to the Main Word Recognizer circuits.

SEQ Q1: Diagram 3B: U4030A -- The SEQ Q1 signal is applied to multiplexer U2010 on the IC Acquisition Memory Board, then sent through the Level Translator to U1020 for transmission on the Main Data Bus.

SEQ Q2: Diagram 3B: U4030B -- See SEQ Q1.

ST CLK CONTROL: Diagram 2A: U4010 -- Used in the selection of the ST CLK 2 signal or the Timebase output as the T.O. CLK. When ST CLK CONTROL is high, the passage of the ST CLK 2 signal is blocked; when the signal is low, the ST CLK 2 signal can pass and be used as the T.O. CLK.

ST CLK Ø: Diagram 4A: U6020F -- The ST CLK Ø signal is the complement of the /RAW CLK signal.

ST CLK 1: Diagram 4A: U5050A -- The ST CLK 1 signal is the synthesized and shaped output of Pulse Shaper U5050A. The signal is applied to the Word Recognizer, Expansion Option, Acquisition Memory, and State Machine circuits as the master timing signal.

ST CLK 2: Diagram 4A: U5050B -- The ST CLK 2 signal is identical to the ST CLK 1 signal, except that ST CLK 2 runs continuously and is applied to the Timing Option and Front Panel circuits.

/ST MACH SEL: Diagram 9A: U4080 -- Enables the address latch in the State Machine circuits.

/STOP TRACE LATCHED: Diagram 8B: U6020B -- Applied to the CPU Acitivity Monitor in the Acquisition Memory circuits, where it is sent on to the CPU as a status signal indicating a main trigger has occurred.

STOP TRACE TRIGGER: Diagram 8A: U5060 -- Terminates a Store operation. It is applied to the Display/Store Mode Control to change the mode.

STORE: Diagram 7A: U6040B -- The STORE signal is high when the Main Acquisition unit is in Store mode. It is used extensively throughout the 7D02 as a control signal.

/STORE COMM: Diagram 7A: U2010 -- The /STORE COMM signal moves low in preparation for a Store operation. The signal is used by the Timing Option circuits, principally to hold the Reset flip-flop locked in the set state until the operation begins.

/SYNC TRIG: Diagram 8A: U6060 . · This signal comes from the State Machine RAM; it is combined with MASTER STOP through U7015. Either signal causes the /EXT TRIG output. Its primary function is to arm or trigger the Timing option.

S1: Diagram 9A: U3050 -- S1 is one of the timing signals from the 7D02 Microprocessor. It is used to enable decoder U4080 on the CPU board, to reset U4045, as the CPU RAM write enabling signal, and to enable the CPU Buffer in the Display circuits.

TC: Diagram 2C: U3040C -- TC indicates that terminal count has occurred in the Timing Option MAC. The signal is applied to the TC Flag flip-flop in the Trigger Amplifier.

TC FLAG: Diagram 3A: U3030A -- The TC Flag signal is set high and remains high following the terminal count (TC) signal from the MAC. At a later time, the RESET signal clears U3030A, which pulls the TC FLAG signal low. The signal is applied through the IC Acquisition Memory circuits to U1020, where it is used by the CPU as a status signal.

TIME BASE: Diagram 3A: U7060 -- The output of the Timebase circuits in the Timing Option. The output varies from 5 ms to 20 ns in 1-2-5 intervals. The output is applied to the IC Acquisition Memory circuits, where it or the ST CLK 2 signal is used as the T.O. CLK signal.

/TIM OPT SEL: Diagram 9A: U4080 -- Used by the CPU to enable addressing of the Timing Option circuits.

TIMING TRACE STOP: Diagram 3B: Q6064 -- The TIMING TRACE STOP signal is generated by several sources: The LOCKOUT signal, a high state at the WB4 line (latched by /E11), a high from the /Q output of Sequencer flip-flop U4030B, or the RESET signal. The TIMING TRACE STOP signal is used with the DISPLAY signal to generate the MASTER STOP signal. Its major purpose is to indicate that the Timing Option has stopped storing data.

T.O.AØ - T.O.A7: Diagram 2C: U2040-U3030. These are the eight output lines from the Timing Option Memory Address Counter. The lines control the RAM address, and are passed through the Read Buffer to inform the CPU of the RAM address.

T.O.CLK: Diagram 2C: U4040A -- Derived from either the TIMEBASE or the ST CLK 2 signal. It is applied to the Acquisition stages, and to the Sequencer and Delay Counter circuits on the Trigger and Timebase Board.

/TRIG: Diagram 3A: U3030B, U2020D, U5020C, U7020C -- The synchronous or asynchronous trigger signal. It is applied to the Sequencer circuits, assuming that U7020C and U5020C permit the line to move negative.

TRIG IN: Diagram 1A: -- This signal enters the 7D02 through the external trigger connector. It is applied to the Trigger Threshold circuit.

TRIG MODE: Diagram 3A: U3020B -- The TRIG MODE signal is used to hold the Async path closed while the Trigger Amplifier is operating in the Sync trigger mode. The signal is also used in conjunction with the /STORE COMMAND signal to reset the RESET flip-flop at the beginning of an Acquisition cycle.

TRIG OUT: Diagram 1A: U5035 -- The /SYNC TRIG signal from the State Machine is applied through buffer U5035B, inverted, and routed out to the front-panel BNC signal as the TRIG OUT connector.

TTL SWEEP GATE: Diagram 10A: U3010B -- The complement of the RESET VERT signal. SWEEP GATE is applied to the Mainframe by way of the Sweep Gate Buffer for unblanking the display.

/VERT CLR: Diagram 10A: U2010 -- Identical to the /CHAR, /LOAD, /CUR CLR, etc. signals that come from U2010, except that it is displaced in phase from the others. The /VERT CLR signal is applied to U3010B, where it is used to immediately reset the flip-flop after it is set by the output of the Row Counter.

VERT SIG +: Diagram 10C: Q6033 -- One of the two ramp signals that are fed to the Mainframe vertical amplifier.

VERT SIG -: Diagram 10C: Q6032 -- This signal is the same, but of opposite polarity to the VERT OUT + signal.

VERT POS: Diagram 16: R3096 -- DC current through this potentiometer is injected into the Vertical Amplifier stage to position the display.

/WAIT: Diagram 4B: U3050 -- The output of the Two-bit Wait Comparator results from comparison of the control signals from the Personality Module and data from the CPU through the 14-bit Latch. The low /WAIT signal holds the Pulse Shapers from changing state and places the Programmable Clock Synthesizer in a hold condition.

WBØ-WB7: Diagram 3B: U1060 -- These eight lines carry data from the CPU to the Timing Option circuits.

/WORD REC: Diagram 2A: U3040D -- The outputs of the Input Acquisition stages are coupled together in a wire-or configuration. The two pairs of four stages join at the inputs of U3040D to generate the /WORD REC signal. This line is low if word recognition has occurred.

/WDRA: Diagram 2B: U4050, U5050, U6050, U7050 -- Each of the outputs of these Acquisition stages join in a wire-or configuration. The line is low if word recognition has occurred.

/WR: Diagram 9A: U4070 -- The /WR signal from the Microprocessor is used to enable the application of the instructions from the CPU to the 7D02 circuits. For example, /WR is almost always asserted following the assertion of one of the select lines from U4080.

/W.R. SEL: Diagram 9A: U4080 -- The /WR SEL signal is pulled low to enable the CPU to write to the Word Recognizer RAM.

/W.R. 1: Diagram 5A: U5020 -- This signal is low when a bit pattern that is addressing the word recognizer 1 RAM is the same as that loaded into the RAM by the CPU at the outset of the Acquisition cycle. In other words, when a pattern match occurs.

/W.R. 2: Diagram 5A: U4030 -- Same as W.R. 1, except that it applies to W.R. 2.

/W.R. 3: Diagram 5A: U7040A -- Same as W.R. 1, except that it applies to W.R. 3.

/W.R. 4: Diagram 5A: U7040B -- Same as W.R. 1, except that it applies to W.R. 4.

X10 IN: Diagram 1A: -- The attenuation factor signal from the external probe. It causes the threshold to switch from 1.4 to 0.14 volts when a coded 10X probe is connected to the EXT TRIG IN connector.

/YØ-/Y7: Diagram 8A: U7050 -- Eight signals from decoder U7050. Each serves a different function: /YØ enables U6060; /Y1 enables U3050; /Y2 and /Y3 form a part of the SELECT 1 and SELECT 2 lines, and control the two 16-bit counters in Counter 1 and Counter 2; /Y4 enables the generation of the G signal; /Y5 sets the Overflow flip-flop in Counter 1; /Y6 is not used at present; and /Y7 resets the Inhibit 2.5 flip-flop.

/Z ENABLE: Diagram 10A: U1010A -- The /Z ENABLE signal is set low with each character to enable display of that character on the screen. It is a product of the Character Counter output, which furnishes the signal for the D input to U1010, and the /LOAD signal, which clocks the C5 signal into the latch.

/Ø-1FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU.

/2ØØØ-3FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU.

2-kHz CLK: Diagram 8B: U5030A -- Applied to Multiplexer U6040, where it is used as a clock signal for the State Machine counters. It is also sent to the Timing Option circuits, where it is used in forming the TIMEBASE signal.

2 MHz CLK: Diagram 8B: U7020A -- Same as above, except for the frequency.

20 kHz CLK: Diagram 8B: U5030B -- This signal is applied to the Timing Option circuits for use in generating the TIMEBASE signal.

200 kHz CLK: Diagram 8B: U7020B -- Same as 20 kHz CLK, except for the frequency.

/3ØØØ-3FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU.

3 MHz CLK: Diagram 9A: U3050 -- The 3-MHz CLK signal is generated by the Microprocessor from the incoming 6-MHz CLK signal. It is applied to the Display Circuits and used for CPU synchronization.

/4ØØØ-5FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU circuits.

/6ØØØ-7FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU circuits.

/8ØØØ-9FFF: Diagram 9A: U4040 -- One of the RAM address lines in the CPU circuits.

6 MHz CLK: Diagram 9A: U4070B -- The 6 MHz CLK signal is fed to the Microprocessor where it is used as the timing signal for the CPU circuits and for the generation of the 3 MHz CLK signal. The signal is applied to the State Machine circuits, where it is divided to produce the 2 MHz, 200 kHz, 20 kHz, and 2 kHz signals.

DETAILED CIRCUIT DESCRIPTIONS

FRONT PANEL BOARD

Introduction

Refer to Fig. 2-2, which is a block diagram of the Front Panel circuits. These circuits perform five functions:

1. The five lowest address bits are applied through the Keyboard buffer, then to the keyboard.

2. The /SYNC TRIG signal is buffered, then sent out as the TRIG OUT signal at the front-panel BNC connector.

3. Threshold data from the P6451 is applied via the BDØ-BD7 lines from the Read Buffer to the DAC (Digital to Analog Converter). The DAC output passes through several amplifier stages before it is applied to the P6451 probe.

4. The /LATCHES SEL (A9-A11) and /RD lines are applied to the Decoder, which generates a /KEYBOARD STROBE pulse that enables the Column Buffer and the Decoder. The Decoder enables the Read Buffer for CPU read access to data on the Buffered Data Bus. The Write Buffer, which is controlled by the /WR signal, enables the CPU to write on the Buffered Data Bus. The Column Buffer transmits the keyboard column data to the Buffered Data Bus for CPU use.

5. The TRIG IN signal from the 7D02 Front Panel connector is applied to the Threshold Gate circuit, where it is compared to the threshold voltage that is applied to another input of the gate. The circuit is used to adapt the trigger threshold to the probe attenuation factor. S.E. TRIG is an inverted and buffered version of /EXT TRIG.

Keyboard Circuits

Refer to Diagram 1A, which depicts part of the Front Panel Board circuits. Buffer U2025 is a hex inverter that has open-collector outputs. The AØ through A5 bits from the CPU, which in this case are used to specify the row of the keyboard, are applied through the buffer to the keyboard via connector P1012.

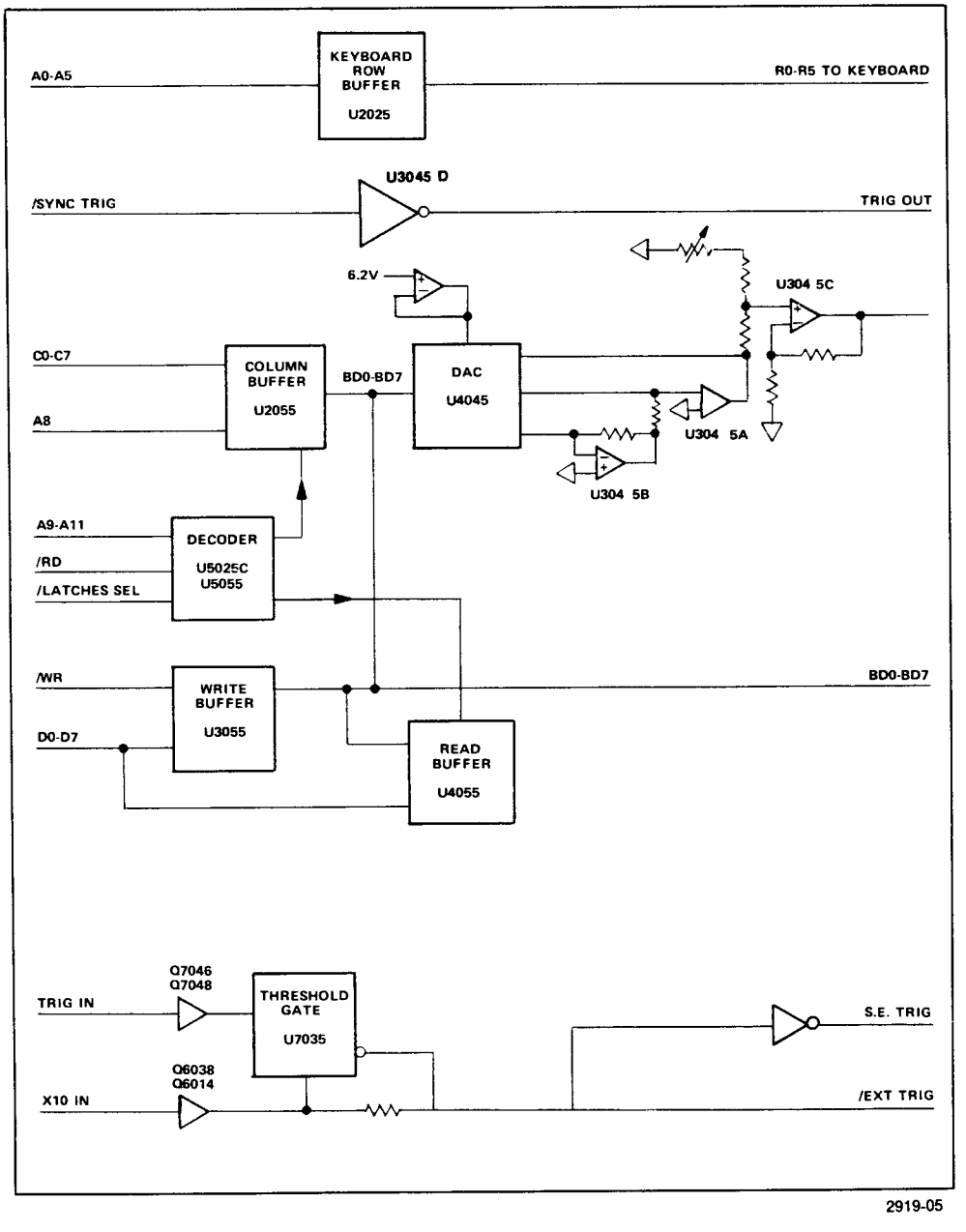


Fig. 2-2. Front Panel Circuits Block Diagram

The keyboard is accessed through the lower six address lines, AØ through A5, whenever address 0:F6XX is read. The rows of the keyboard are scanned by the address lines and the columns are read as the data byte. That is, the first row is read by reading 0:F601, the second by reading 0:F602, then 0:F604, 0:F608, 0:F610, and 0:F620. The column location of a pressed key is given by the position of a zero bit in data read at the row address. For instance, pressing the digit key "7" produces a data byte of F7 (hex) at row address 0:F604. F7 (hex) is 1111Ø111 (binary), and the zero bit is in bit position three (beginning with the LSB in position Ø at the right in the usual way). Table 2-1 lists the column and row assignments of the keyboard. Note that the "7" key is in column three in the table, corresponding to its bit position (also three) in the data word.

TABLE 2-1
Keyboard Bit Assignments

Column:	0	1	2	3	4	5	6	7
Row: 0	Display	Word Rec	Counter	D	E	F	DELETE	START/ STOP
1	ACQ MEM	END	TRIGGER	A	B	C	---	---
2	PROGRAM	ELSE	GO TO	7	8	9	S	S
3	STORE MEM	QUAL	()	4	5	6	C	---
4			OR	1	2	3	C	C
5	IMMEDIATE		NOT	0	X	FORMAT	---	C

Data from the other axis of information for the keyboard (column) enters the board through connector P1038 in parallel eight-bit format. These lines, CØ through C7, are applied to buffer U2055, which is enabled by the A8 line from the CPU address bus and the /KEYBOARD STROBE signal. When both lines are low, the buffer transfers the column data to the Buffered Data Bus for further use by the CPU.

Trigger Buffer

The /EXT TRIG OUT signal from the State Machine circuits is applied to buffer U5035, which drives the TRIG OUT signal to the Front Panel connector. Diodes CR5043 and CR5042 protect the buffer.

Threshold Voltage Generator

The Threshold Voltage Generator furnishes the threshold voltage levels for the P6451. Both the Threshold Voltage Generator and the P6451 are parts of the Timing Option.

The P6451 threshold is set by writing an eight-bit value into the DAC on the Front Panel Board at address 0:F8EØ. Each LSB of the value corresponds to a 50-mV threshold step. Table 2-2 lists the value that must be applied to the DAC to arrive at a specific threshold value. Note that an 8ØH offset is required to arrive at the expected output.

TABLE 2-2
P6451 Threshold Values

Threshold	Calculation	Value
+6.35Ø	8ØH + 7FH	FFH
+1.4ØØ	8ØH + 1ØH	9CH
+Ø.Ø5Ø	8ØH + Ø1H	81H
Ø.ØØØ	8ØH + ØØH	8ØH
-3.ØØØ	8ØH - 3ØH	44H
-6.35Ø	8ØH - 7FH	Ø1H

When a threshold voltage level is required for the P6451, the CPU addresses the DAC by way of the /E7 line from the Timing Option, and loads the BDØ-BD7 lines with the appropriate data through the Writer Buffer. Upon the low state of the /E7 line, the data is latched into U4045, which responds by producing an output that corresponds to the data just loaded. The DAC and surrounding circuits operate as follows:

DAC U4045 is a unipolar eight-bit device which, in its configuration with U3045A, B, C, and D, operates in a bipolar mode. The DAC is also equipped, as implied earlier, with an integral latch.

Operational Amplifier U3045D is configured to operate as a voltage follower amplifier, using VR1034 as the voltage reference. The purpose of the amplifier stage is to provide a fixed reference voltage at pin 15 of the DAC for the internal divider string.

Current from the internal divider string leaves U4045 by way of pin 1 and pin 2, called Iout and /Iout, respectively. The current from pin 2 is applied to the input of U3045B, which has a gain of minus one. The output current of the amplifier is applied through R5048, summed with the current from pin 1, and applied to the input of U3045A. Depending upon the value programmed into the DAC, and due to the summing of positive and negative current components from pins 1 and 2, current applied can swing either positive or negative. Figure 2-3 shows a graph of the two outputs and the composite outputs. The output of U3045A is applied to divider network R2046 and R2045, which in conjunction with GAIN adjustment R1046, divides the applied voltage by ten. Thus, one tenth of the applied voltage is sent to the input of operational amplifier U3045C. The gain of this stage, approximately 5/2, is set by resistors R2041 and R2042. ($V_{threshold}$ x 1/10 x 5/2 = 1/4 V_{th}. Thus, the gain of 4 on the P6451 threshold amplifier yields V_{th} for the circuit.)

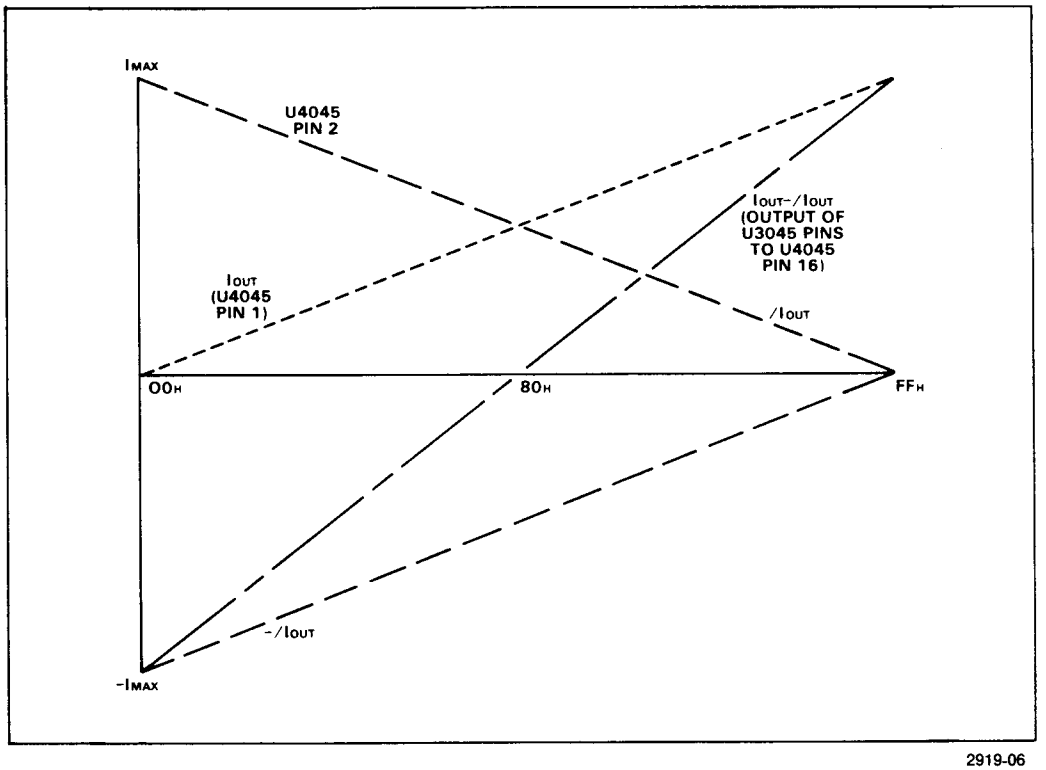


Fig. 2-3. IOUT, /IOUT, and Composite Output.

Adjustment of the stage is done by connecting the CAL-NORMAL jumper, P1034, in the CAL position, and performing the following adjustments: The maximum input value (6.350 V) is programmed into the DAC, then the voltage at TP1053 is set by GAIN adjustment R1046 for a value of 1.5833 volts. The OFFSET potentiometer (R1042) is set with zero programmed; the voltage at TP1053 is measured to be zero. (The CAL-NORM jumper is used to sum the offset of the analog ground reference--internal to the P6451 Probe--with the probe threshold.)

Buffers and Decoders

U5055A and U5055B are the Keyboard Strobe Gate and Write Decoder, respectively. The A9 and A10 address lines are held high on the input of U5025B, which enables pin 14 of U5055B. Addresses for the Keyboard Strobe are 0:F6XX or F7XX. Address line A11 to pin 13 is also held low. Then, when the /LATCHS SEL signal from the CPU moves high, the output of U5055B (/KEYBOARD STROBE) moves low to enable U5055A. The signal is also sent to U2055 to enable the Column Buffer, as required.

If the /RD line from the CPU is low, /KEYBOARD STROBE causes output pin 4 of U5055A to move low and enable U4055. This passes the BDØ-BD7 data through U4055 to the Main Data Bus.

Write Buffer U3055 sends data by way of the Buffered Data Bus to the DAC from the CPU. Any write cycle gates the data onto the BDØ-7 Data Bus. When the CPU has the appropriate data at the inputs of U3055, it pulls the /WR line low, which transfers the data to the Buffered Data Bus for loading into the DAC latch.

Trigger Threshold Circuit

This circuit provides a two-level switching threshold for the incoming EXT TRIG signal. It consists of Input Amplifier Q7046-Q7048, Probe Attenuator switch Q6038-Q6014, and Switching Comparator U7035.

The X10 In signal from the probe ring enters at P7050, pin 3. this signal is either open (X1) or closed to ground (X10). Darlington transistor Q6038 sense the switch closure and turns off, which allows Q6014 to turn off as well. The voltage across R6032 is thus reduced to about 140 mV. When the switch is open (X1) Q6038 conducts, which turns on Q6014 and sets the voltage on R6032 to approximately 1.4 volts.

The TRIG IN pulse from the front panel BNC connector is fed through pin 4 of P7050 to the gate of FET Q7046. This transistor is connected in totem-pole configuration with Q7048. From the drain of Q7048, the signal is applied to the input of U7035, a differential comparator with complementary outputs.

As the incoming trigger signal from Q7046 crosses the threshold level at pin 4 of U7035, the comparator switches and its outputs move in opposite directions (pin 11 moves high and pin 9 moves low). When the trigger ends, the comparator once again switches and the outputs move in the opposite direction.

TIMING OPTION

Introduction

The Timing Option (Option 1) consists of the IC Acquisition Board, which is depicted on diagrams 2A, 2B, and 2C; and the Trigger and Timebase Board, which is depicted on diagrams 3A and 3B. Since both of these boards share the same general function, they are discussed as a unit in this description. The description is divided as follows: Block Description, Trigger Paths, and Detailed Description.

Block Description

Refer to Fig. 2-4, which is a block diagram of the Timing Option section. The Time Base and State Clock section receives the ST CLK 2 signal and the 2 MHz- 2 kHz signals, and generates a 100-MHz signal on the board. From these signals, the circuit generates the CLOCK signal, which comes from two sources: During synchronous operation, the State Clock signal is the source, so the CLOCK signal has the same timing characteristics as the State Clock. During asynchronous operations, the Time Base-generated signals provide the CLOCK signal, which varies from 5 ms to 20 ns in 1-2-5 sequence. The CLOCK signal is applied to the Sequencer and Delay Counter, the Trigger circuit, and to the Data Acquisition stages.

The Memory Address Counter advances the RAM address whenever the /MAC EN signal is low. The Counter is loaded by the CPU address bus. It can be read by the CPU by way of the DØ-D7 lines. The /MAC EN signal, which enables

The Memory Address Counter advances the RAM address whenever the /MAC EN signal is low. The Counter is loaded by the CPU address bus. It can be read by the CPU by way of the DØ-D7 lines. The /MAC EN signal, which enables the counter, is produced by the Sequencer and Delay Counter circuits.

The Trigger and Async Filter circuits, using the external trigger signal and the output of the Word Recognizers of the Timing Option, produce the /ASYNC TRIG signal for use by the Main Word Recognizer circuits. The circuits also produce the /TRIG signal that is used by the Sequencer circuits. To reduce the effects of glitches and races in asynchronous trigger sources, the Async Filter section of this circuit delays the /TRIG signal in 20 ns steps from Ø to 300 ns. (A glitch is defined here as a repetitive, aperiodic event of unknown origin.)

The Sequencer and Delay counter circuits generate the TIMING TRACE STOP and /MAC EN signals. The first is used by the Front End board, where the signal is combined with the DISPLAY signal to form the MASTER STOP signal. The Delay Counter is a 16-bit counter that runs off the clock signal from the Timebase and State Clock circuit. The Sequencer delays the stop that follows the trigger by a programmed number of clock pulses (0 to 65534).

The Decoder consists of a pair of address range decoders that, by decoding the addresses on the AØ through All lines, determine the address on the address bus lines for the purpose of writing control signals to the Timing Option circuits and reading data from the Timing Option circuits.

The Acquisition stages consist of eight integrated circuits that recognize bit patterns from the P6451 Probe, as controlled by the CPU through the WBØ-WB7 lines.

The Acquisition RAM stages consist of four 4 by 256 RAM integrated circuits. These are used to accept the bits from the data and glitch outputs of the Input Acquisiton stages.

Note that although the CPU is involved in nearly every circuit function, it is not active (beyond setup) in the Timing Option. The CPU sets up the circuits, they become triggered, then proceed without further action from the CPU.

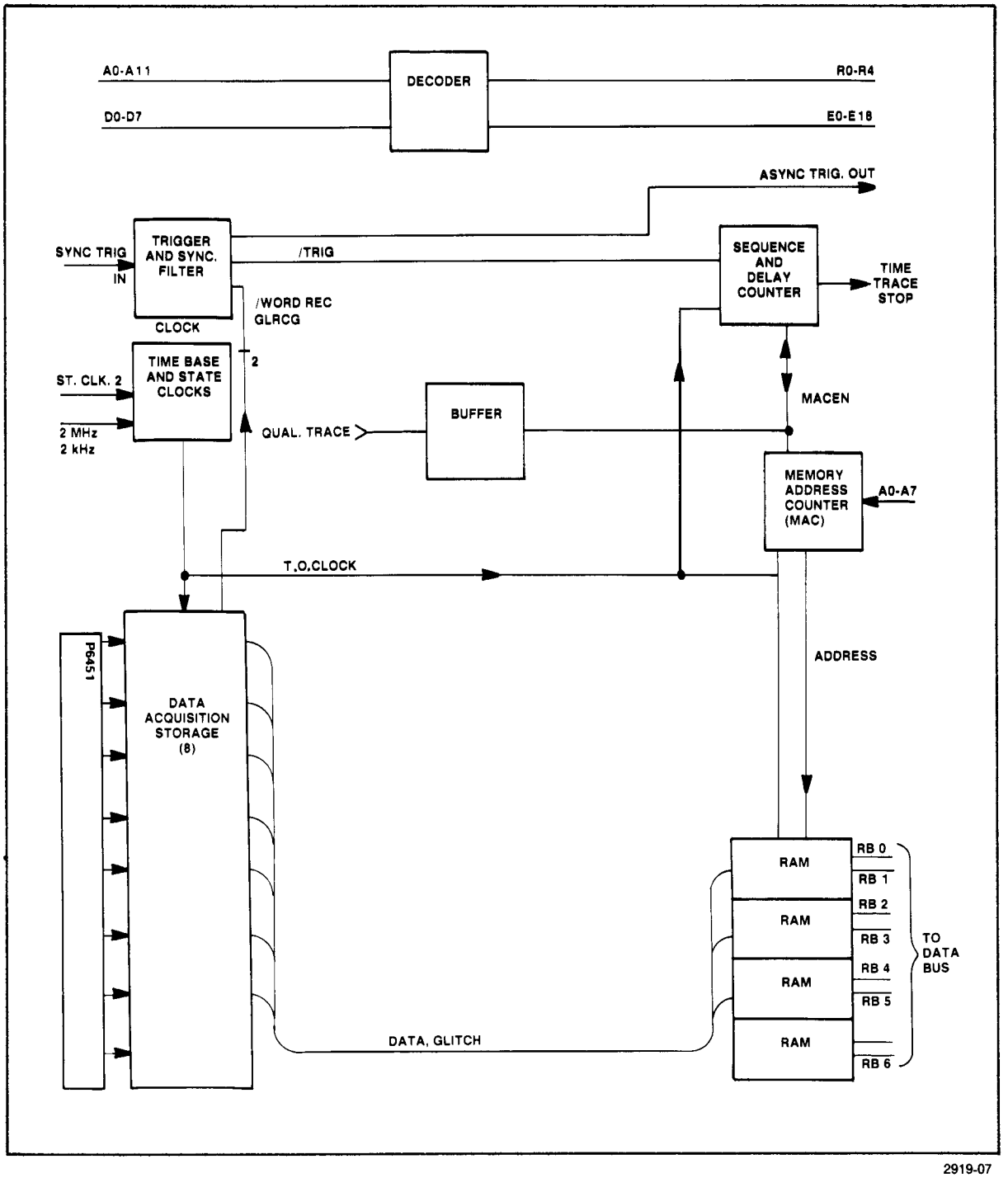


Fig. 2-4. Timing Option Block Diagram

Trigger Paths

Figure 2-5 illustrates how the Timing Option relates to the main part of the 7D02 in Sync Mode operation. The /WORD REC signal comes from the AND combination of eight P6451 inputs and the normal or inverted external trigger signal. From there the signal is applied to U5020, through a buffer, and out as the ASYNC TRIG OUT signal, to be sent to the Main Word Recognizer circuits.

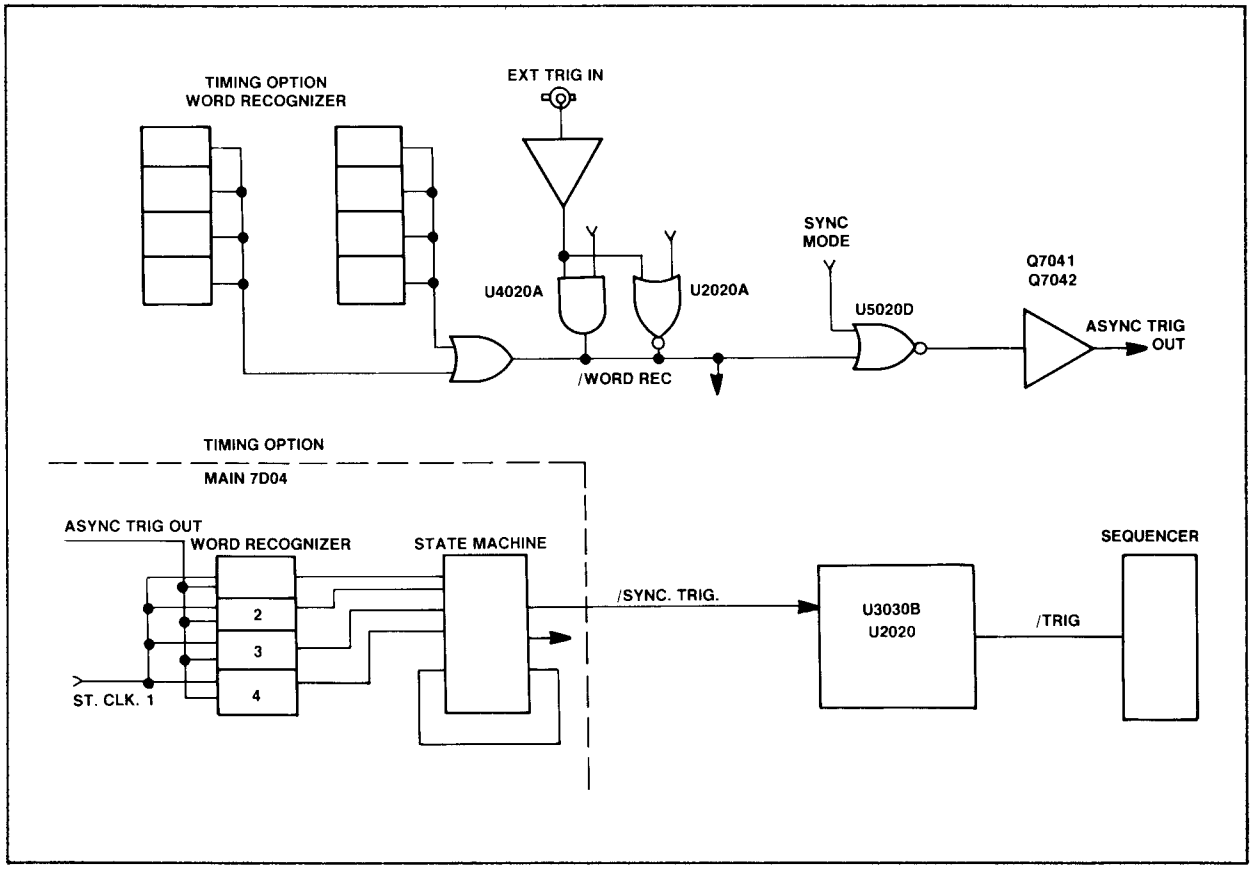


Fig. 2-5. Timing Option in SYNC Mode.

Figure 2-6 illustrates the Async Mode trigger path. Basically, the path involves the same major circuits as the Sync path, except that other circuitry is used in addition. The GR signal is fed to the GLRCG gate, which enables that signal to pass through if glitch recognition is selected. The /WORD REC signal from the Timing Option Acquisition Stage is also

passed to the Filter gating section, where it shares a common bus with the normal or inverted external trigger. This signal is applied to the Async Filter or through the Zero delay gate (U4020C), whichever is selected. From there, the signal (delayed or undelayed) is sent through the congrol gate to the Pulse Stretcher and the Edge Select gate. Through the former, the stretched pulse is applied through a buffer, then out to the Word Recognizer Board. Depending on the polarity of the other input to the Edge Select Gate, either a positive or negative edge will trigger the trigger gate. This gate is armed at an earlier time by the SYNC TRIG signal from the State Machine circuit, which, as mentioned earlier in this description, is driven by the Main Word Recognizer.

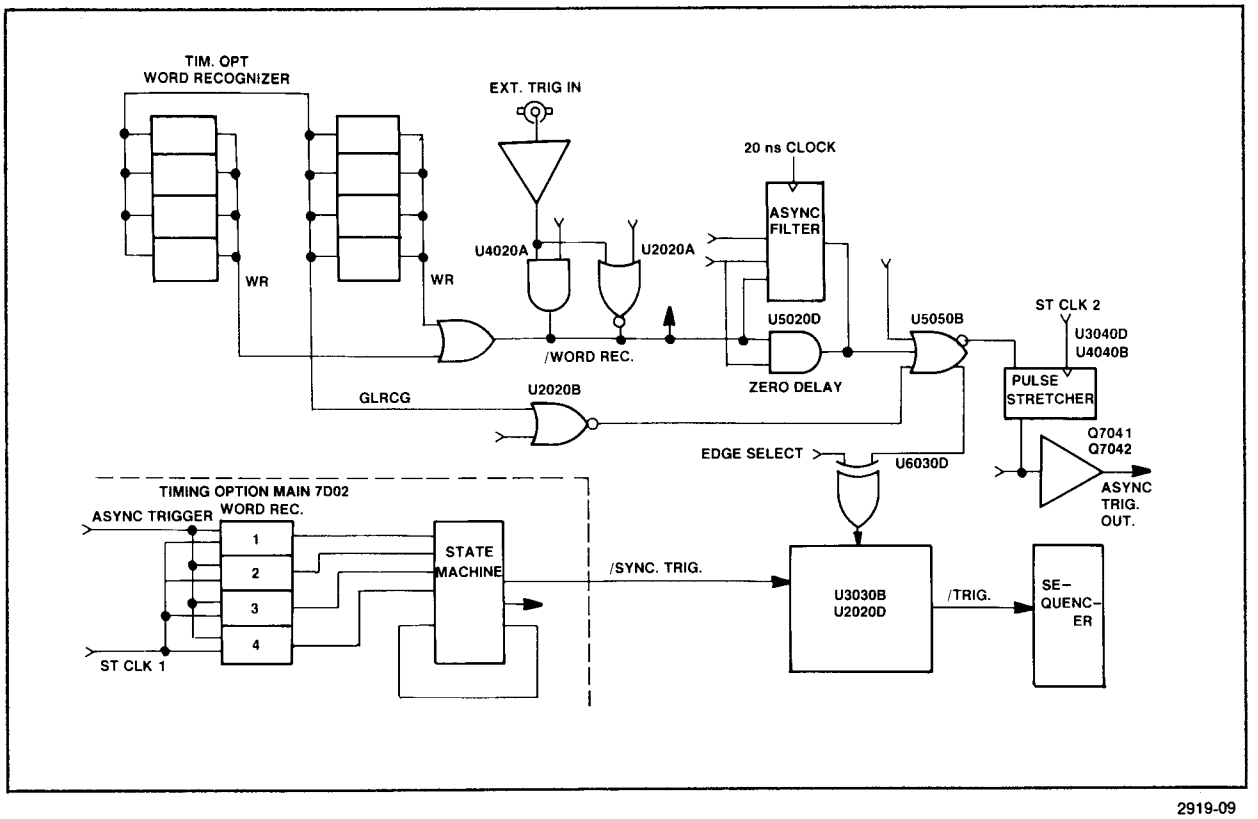


Fig. 2-6. ASYNC Mode Trigger Path.

Detailed Description

Data Acquisition. Refer to Diagrams 2A and 2B. The Acquisition stages consist of eight discrete units that perform word and glitch recognition, each with its own channel. Thus, eight channels of word recognition data come from the external probe. Each of the Acquisition stages feeds data to an acquisition RAM, where it can be read by the CPU. All of the Input Acquisition stage word recognizer outputs combine to form a wire-OR connection, so only a single output is applied to the Trigger circuits. The same applies to the glitch recognition lines, in that all eight combine to be applied to the Trigger circuits. Since the eight word recognizer channels are essentially the same, only one will be described here.

Latches U4010, U6010B, U7010B and U5010B receive the WBØ-WB4 signals, which control the instructions that are fed to the Input Acquisition stages. These include the Data Hi/Lo control, the Sync/Async control, the Off/On control, the Pipeline/Glitch control, and the Glitch Recognizer Off/On control.

Refer to Diagram 2A. U7030 receives data from Channel 3. It in turn feeds data to U6020, the RAM that stores data from U6030, the Channel 2 Input Acquisition Stage. Refer to Fig. 2-7, which is a block diagram of U7030, and also applies to the other seven units. Differential data at ECL levels from the external probe is sent to U7030 by way of pins 7 and 8 of J7048 and then to pins 9 and 10 of U7030. Once in the device, the data is applied to the differential inputs of U2. From the output of U2, the data is sent through delay line U6040 to permit the timing Option to meet its Hold Time specification. The delayed data is sent through amplifier U3, then is applied to latch U4 and Glitch Detector U5. Upon the rising edge of each clock (entering U7030 at pin 1, then through U1 to U4 and U9), the data at the input of U4 is clocked to the Q output, then sent off the device as the Data Out, at pin 3.

The Glitch Detector output moves high if at least two threshold transitions occur between the rising edges of the clock. When this occurs, the high is transferred through multiplexer U7 (assuming that the Pipeline/Glitch control line at pin 16 is low), then clocked through latch U9. If the Glitch Recognition Off/On line is low, gate U10 is enabled, and the Glitch Recognizer Out line, pin 14, will indicate the presence of one or more glitches. The Glitch Recognizer outputs of all eight word recognizers are wired together, so whenever any channel detects a glitch, that output moves high.

Glitch detection and recognition are done in the Timing Option Async Mode only. In Sync mode, the Glitch output flip-flop (U9) looks instead at the data output, becoming a second, or pipeline delay stage, which matches the main section pipeline delay. (The term "pipeline" refers to the chain of circuits through which acquired data passes before being stored in the Acquisition Memory.)

The word recognizer in the device (U6030) is always set to its internal Async mode, regardless of the Timing Option mode. This is accomplished by the Sync/Async control, which is always set low. When the Timing Option is in the Sync Mode, the Word Recognizer data is synchronized in the Main Section of the 7D02 word recognizers.

Data Acquisition RAMs. The RAMs (U6020, for example) accept data from the Data and Glitch/Pipeline outputs (pins 3 and 2, respectively) of the Word Recognizer stages. When the bank select (BS) inputs are high, the RAM is disabled, write operations cannot occur, and the outputs go to the ECL low level. During the acquisition period, the BS inputs are low and the clock to U7030 also drives the /WE (write enable) input to U6020. Following each qualified clock, the address advances to the next cell. To read the RAM, the clock input is high, and one or the other of the BS inputs is pullsed low by the CPU read pulse (/RØ or R1 on Diagram 2C). (A "qualified" clock is one that is used to store a valid signal. Invalid signals are overwritten by the next clock and data.)

Memory Address Counter. During the acquisition period, the MAC (Memory Address Counter) advances the RAM address whenever the /MAC EN signal is low (/MAC EN is controlled by QUALIFY; if this signal is low, /MAC EN is forced high). The counter consists of two four-bit binary counters, U2040 and U3030; the terminal count of U2040 is connected to the Count Enable line of U3030, which permits the latter to increment on each 16th cycle. The terminal count outputs of both counters are joined together at U3040C, which produces a terminal count signal with the occurrence of an FF count. Following the acquisition cycle, the low /R2 signal enables U2020 and U2010 to pass the stop address to the TTL translators, and eventually to the CPU.

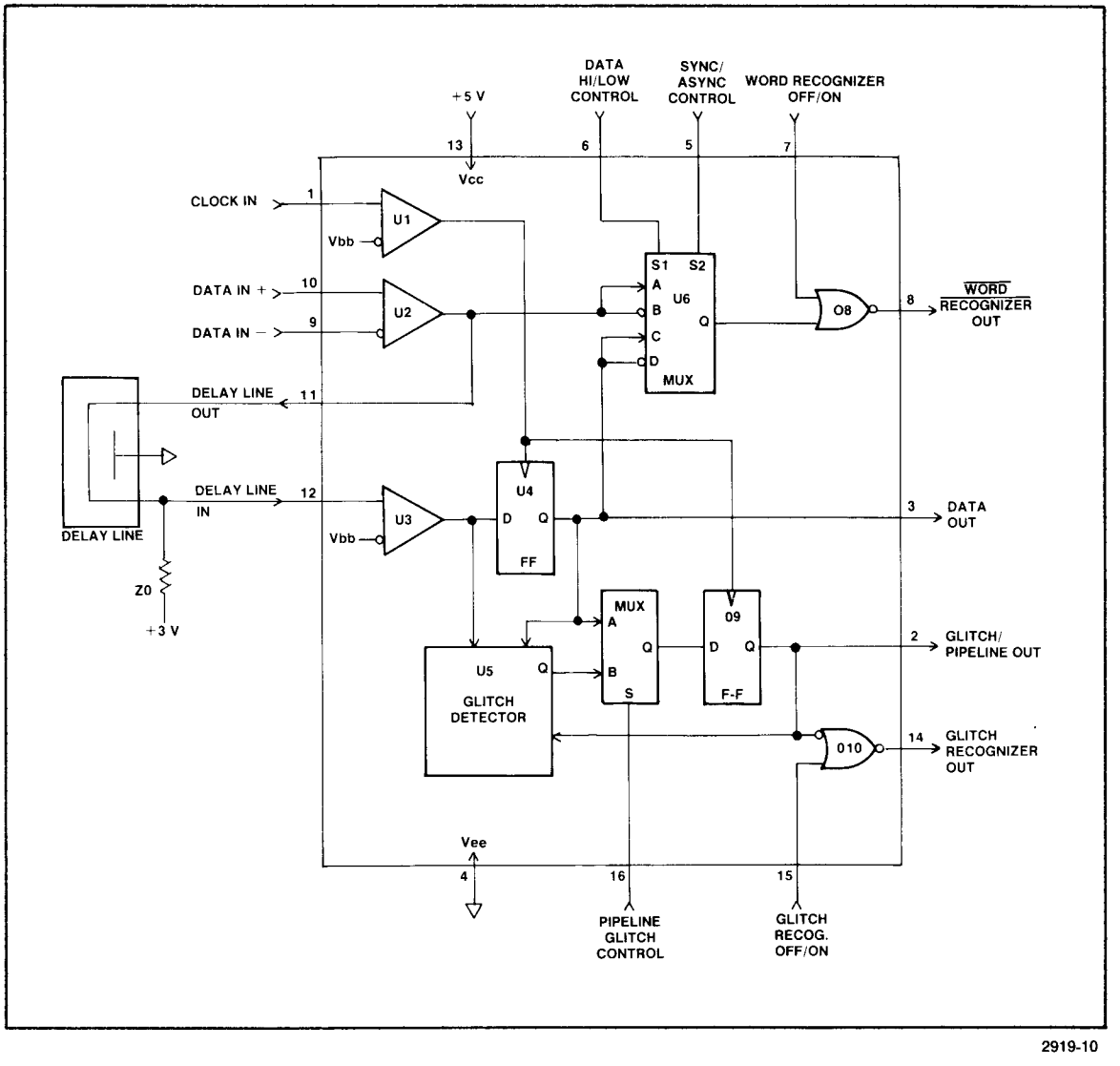


Fig. 2-7. Block Diagram of Input Acquisition Stage.

Address data for the read cycle of the MAC comes through buffers U2050 and U3010A and B, which translate the incoming TTL levels to ECL. The memory is read by writing an address through the buffers to the MAC parallel inputs. First, the /PE line from U4010 pin 5 (Diagram 2A) is held low, and the address data is placed on the address bus. Then, the CPU sends a read clock by way of either the /RØ or the /R1 line, through pin 1C or 1D of P102, which passes through several stages and eventually reaches U4040, pin 14, as the clock to load the address data. (The CLOCK signal at pin

11 of U4040 has previously been set high to enable U4040.) Note that the MAC acts more like a register than a counter when used in the read mode. After the address is clocked into the MAC, the acquired data in the RAM is sent through U2020 and U2010, through ECL to TTL translator stages, to U1020, which places the address data on the Data Bus. The /RBE signal from the Trigger Board (derived from the CPU /RD and /SEL D signals) enables the buffer when required.

The address signals from the MAC also go to each RAM, where the data selects one location in the RAM to be read by the CPU by way of the RBØ through RB7 lines.

It should be noted that the MAC is always loaded to Ø before an acquisition cycle, by reading acquisition memory location Ø. Also, after the MAC is loaded, the Parallel Enable inputs are set high. However, to prevent a false clock, the CLOCK signal is first set low. Finally, when the Parallel Enable inputs are switched high, the BS lines are switched low to begin acquisition through U3050, Q3043, and Q3045.

Clock, Qualifier and Control Circuits. Refer to Diagram 2C. The STATE CLOCK CONTROL signal from U4010 on Diagram 2A passes through buffer U4040B, where it is wire-Or connected with the pin 15 output of U4040D, and applied to the base of Q1046 and Q1042. These two transistors control the passage of the QUAL TRACE signal, which enters the board at pin 17A of P202, and the ST CLK 2 signal from P202, pin 3A. If STATE CLOCK CONTROL is high, Q1042 condusts, holding the base of Q1037 at approximately +3 volts. Thus, the QUAL TRACE signal cannot pass through to Q1037. Likewise, if the same input condition exists, Q1046 conducts to hold the base of Q1047 at about +3 volts, and the ST CLK 2 signal cannot pass through to Q1047.

At pin 2 of U4040A, the TIMEBASE and ST CLK 2 buffers are tied together. During a Sync-mode acquisition cycle, the TIMEBASE signal is set low so the state clock buffer, Q1047, can drive the line. When this occurs, the STATE CLK CONTROL line is low, enabling the state clock buffer.

The qualify buffer consists of Q1043, Q1036, and Q1035. Assuming again that the STATE CLK CONTROL line is low, the signal can pass through Q1037, which shares input pins 5 and 6 of U3040A and B with the incoming /MAC EN signal. If QUAL TRACE is high, the emitter of Q1037 can go low, permitting the /MAC EN signal to enable the MAC to count on each state clock. If, however, the QUAL TRACE signal goes low, then the MAC cannot count. (At that point, data written to the RAM is simply over-written until a qualified clock occurs, changing the RAM address by incrementing the MAC.)

When Async operation is chosen, the STATE CLK CONTROL is pulled high, which blocks the QUAL TRACE and ST CLK 2 signals.

Data Readout Circuits. As mentioned earlier, the CLOCK signal is set high by the Time Base to read the Acquisition RAM, and the /PE signal must be low. When the /RØ signal goes low to read the memory, U3050 is non-inverting, so the /BSØ line also goes low, activating the RAM to produce the memory contents on the RBØ through RB7 lines. The falling edge of /RØ or /R1 also clocks the address bits into the MAC. The RBØ-RB7 lines are inverted and translated in level by eight parallel transistors, then sent through U1020 to the Data Bus. The same CPU pulse that pulled /RØ low also pulls the /RBE line low, which enables the tri-state output of U1020. Similarly, the /R1 signal enables reading the Glitch/Pipeline RAM. In order to enable these read operations, the /PE signal must remain low, which keeps the RAM outputs low.

The /R2 line from P102 pin 2C is applied through Q2022, inverted, and enables U2020 to pass the AI2 through AI7 bits (MAC address) to the Read Bus. Also, the output of U3010 (pin 8) enables U2010 to pass AIØ and AI1. (This occurs when /R2 is low, and /R3 and /R4 are high.) When the /R2, /R3, and /R4 lines are all high, U3010 enables the A and B inputs of U2010 to pass the RBØ and RB1 signals through the multiplexer, out pins 2 and 15, and onto the bases of Q1014 and Q1017, respectively.

If /R3 is low and the other two lines are high, the SEQ Q1 and SEQ Q2 signals pass through the multiplexer. If /R4 is low and the other two lines are high, the TC FLAG signal is passed.

Time Base Section. (Refer to Diagram 3A.) The Time Base section is composed of oscillator U5050, divider U7050, latch U8050, Multiplexer U8040, and Multiplexer U7060. The oscillator operates as follows: Resistor R6067 sets the DC level; Y6060 produces feedback around U5050A to sustain oscillations. The output of the oscillator is fed to U7050, where it is divided by two at pin 15, furnishing the 20-nS signal that is applied to pin 5 of U7060 and then to the Async Filter circuits, and divided by five into a 50-nS signal, which is applied to pin 4 of U7060. The 50-nS signal is also fed to Q8069, which feeds the signal to U8060. The 20-nS signal is also applied to the Async Filter circuit multiplexer-divider.

The WBØ-WB7 data from the CPU enters the board by way of Buffer U8050. The Q1, Q7, and Q8 lines are connected to U8060, to control the selection of either the 20 MHz, 2 MHz, 200 kHz, 20 kHz, or 2 kHz signals. The Q2, Q3 and Q4 lines are applied to U7060, a one-of-eight multiplexer.

The selected signal from U8060 (2 kHz through 20 MHz in decades) is applied to the clock input of U8040, which is a synchronous four-bit counter. This counter is controlled by the Q5 and Q6 bits from U8050, which cause the stage to divide by 2, 4, or 10. Thus, for instance, the 2-kHz signal applied through U8060 will come out of U8040 as 200 Hz, 500 Hz, or 1 kHz, depending on the control inputs. Operation of the counter is as follows:

Assume that the counter has just completed a count sequence. The CARRY output at TP 85 is high just at the end of the sequence, so the U5040 output is low, which enables the load input to U8040. At this point, the D1 or D3 inputs preload the counter to determine the divide factor. (Since D2 is always high, the counter is always preloaded with at least four. If D1 is held high during the load period, the counter preloads 6, then counts the remaining 9 cycles to 15. This is the divide-by-ten mode. If the divide-by-four mode is chosen, D3 is held high, and the counter is preloaded to 12, then counts the remaining three pulses to 15. Refer to Fig. 2-8, which illustrates the divide-by-four function as an example. If D1 and D3 are both high, the counter preloads 14 and counts the remaining 1 pulse to 15, providing the divide-by-two mode.

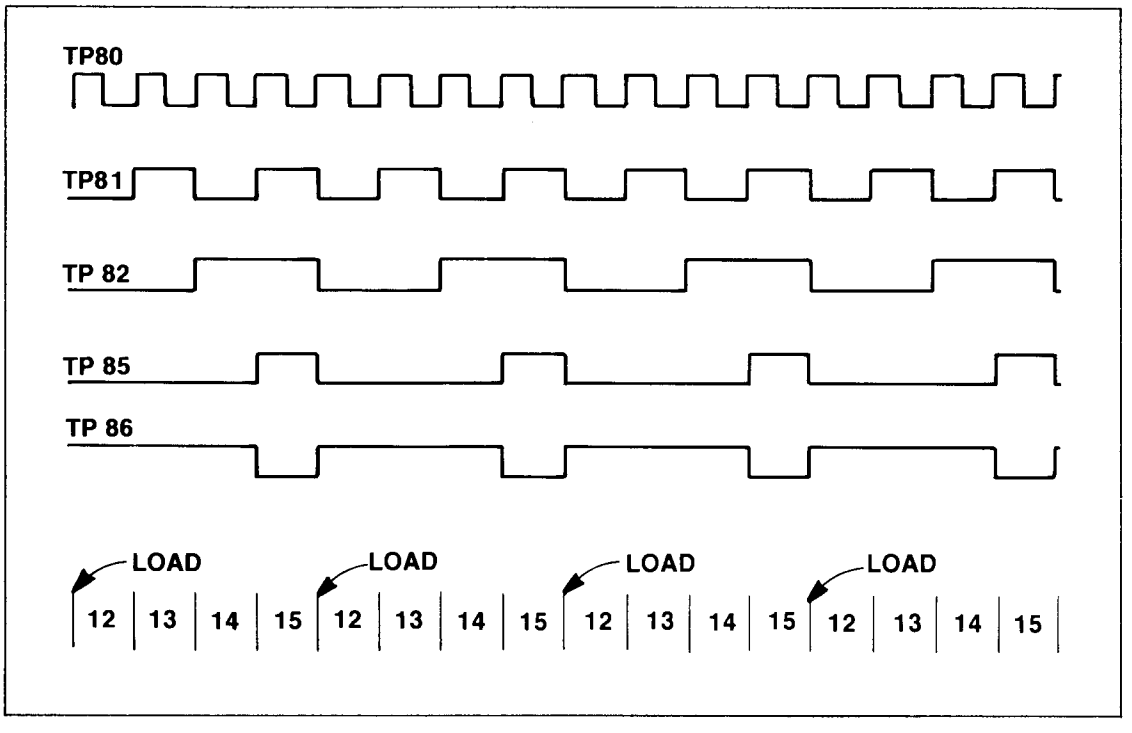


Fig. 2-8. Time Base Divide-by-four Operation.

As mentioned earlier, U7060 is a one-of-eight multiplexer. Lines WBØ-WB3 are applied through U8050 to the A, B, and C inputs of U7060 to control the selection of one of the six time-base input sources:

1. X1 at pin 5 -- the 20-nS timing signal from U7050.

2. X2 at pin 4 -- the 50-nS timing signal from U7050.

3. X4 at pin 11 -- the output of U8060 (which is the 2 kHz through 2 MHz signal in decade steps).

4. X5 at pin 12 -- the buffered output of U8040.

5. X7 at pin 14 -- the /E15 signal from U3060 (which is a four-line to sixteen-line decoder that produces a test signal from software purposes).

6. U7060 output -- the TIMEBASE signal (which is the timing signal that is passed through P203, pin 25A, to the IC ACQ MEM board).

External Trigger Amplifer

The /EXT TRIG signal from the Front Panel circuits is applied to an ECL Translator that consists of Q2010, Q2017, and Q2013. Fixed bias for the stage is provided by the resistor string that connects to the bases of Q2013 and Q2017. Constant current for the stage comes from Q2013. The /EXT TRIG signal is then applied through emitter follower Q2015, the emitter of which drives one input of U2020A and U4020A.

The WBØ and WB1 signals from U1060 on Diagram 3B are applied to triple latch U3020. This stage drives the other inputs to U2020 and U4020, as discussed earlier. The /WORD REC signal, which is the output of these two stages, is sent to U4020D, U5020D, and U6020, the Async Filter circuit. The /WORD REC signal also comes from the IC Acquisition board by way of P102, pin 11C, to P103, pin 11C.

The purpose of U2020A and U4020A is to provide an external trigger that is of either polarity. This is controlled by the WBØ and WB1 signals through U3020. Output pin 12 is high if no glitch recognition is required.

Sync Trigger Amplifier

The /SYNC TRIG signal from the State Machine circuits is applied from P203, pin 18B, to the ECL Translator that consists of Q1026, Q1022, and Q1025. This circuit operates in the same way as the External Trigger Translator described earlier. The trigger signal is taken from the collector of Q1025 and applied to the base of amplifier Q1027, which amplifies and inverts the signal, then applies it to flip-flop U2020.

Async Filter

The Async Filter section is used to delay the trigger transition to the low level by a specified amount of time, in order to avoid triggering on glitches and races caused by unmatched delays. There are four signal paths associated with the Async Filter. These are as follows:

The zero-delay path around the Async Filter in Async mode is U4020C. In this case, U8020 is loaded with an F, which causes the terminal count output at pin 4 to be low. Since pin 16 of U8030 is high, the output of U5020B holds the input, pin 12, of U4020C low. Thus, when the /WORD REC signal goes low at the pin 11 input to U4020D, the input to U5050B, pin 12, will be permitted to move low.

The second path through the Async Filter, which is the 20-nS path, is by way of U6020B. The 20-nS signal from U7050 is applied to the clock input, pin 9 of U6020. The flip-flop is held set, however, until the /WORD REC goes low. At that time, the 20-nS signal clocks the flip-flop, and the flip-flop output goes low. The hex code in U8030 is now a 1, so U8020 pin 3 is high. This forces the output of U5020A, pin 2, low. Because of the code stored in U8030, pin 6 of U7020B is also low. Thus, when the output of U5020B goes low, as just described, U4020C, pin 15 goes low, which pulls the input pin 12 of U5050B to go low. (The /WORD REC signal had already gone low, which enabled the output of U4020D to go low.)

The third path, which is the 40-nS path, is through both cells of U6020. Both remain set until the /WORD REC signal goes low. Then, the next positive transition clocks U6020B. But U6020A cannot switch until the following transition, since it must wait for U6020B to switch. The hexadecimal code on U8020 is Ø, so the 20-nS path is still open through U7020B, enabling U5020A to control the pin 13 input to U4020C. The code in U8020 holds the pin 5 input of U7020A low, so the gate output does not move low until U6020A switches high. This enables the pin 15 output of U4020C to move low. As in the 20-nS path discussion, the /WORD REC signal is already low, so the pin 12 input of U5050B can move low.

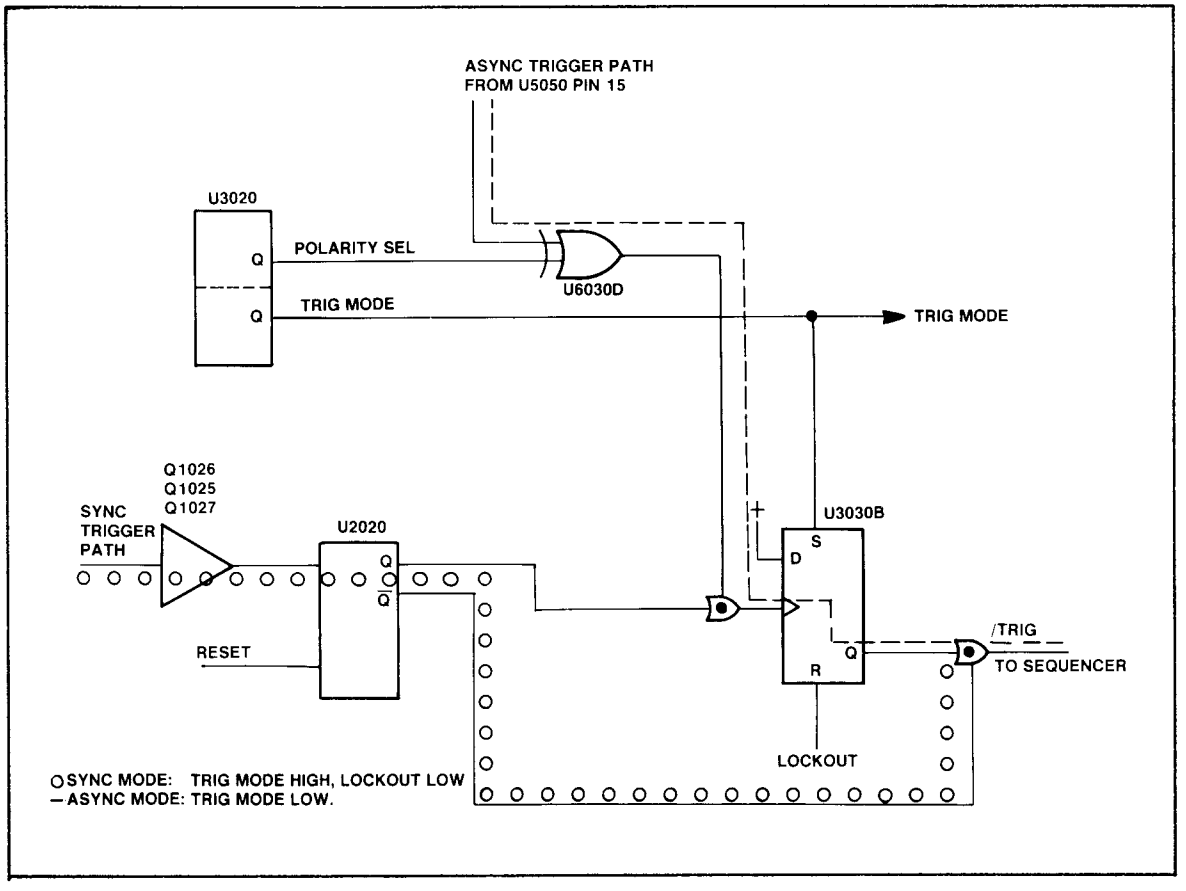
The fourth path is for 60-nS and longer delays, and is through counter U8020. The hexadecimal code for these delays is from 2 to E, where 2 is the longest delay. In this case, the code is always such that pin 6 of U7020 is always high, which blocks the path through U4020, pin 13. Following the 40-nS sequence just described, pin 5 of U8020 moves high, which permits the device to begin counting the 20-nS signal applied at pin 13. (Heretofore, U8020 was inhibited from counting by the low at pin 5, and was stopped by pin 9 of U4020C when the TC output went low following each delay period. While pin 5 of U8020 was low, the hexadecimal code from U8030 was loaded into the U8020 inputs each 20 nS.) Depending on the number preloaded into the counter (2 through F), a specified time later, the counter reaches F, the overflow point. Then, pin 4 goes low, and U4020C, pin 15 pulls U5050B low. As before, the /WORD REC signal has enabled U4020D, pin 14 to go low. At the same time, the pin 9 output of U4020C locks the count of U8020 at F.

Trigger Section. The controlling gates for both the Async Trigger paths are U5020D and U5050B. The control lines for these two gates come from U8030; pin 15 of the latch controls pin 10 of U5050B, and pin 19 of the latch controls pin 10 of U5020. The two control lines are always complementary. Refer to Fig. 2-9.

Assume that the Sync mode is selected. Thus, U5020 pin 10 is low, and U5050B pin 10 is high. When the /SYNC TRIG signal goes low, pins 9 and 14 of flip-flop U2020 go low. At this time, both the RESET signal from U4040 on Diagram 3B and the LOCKOUT signal from U4030 are low. The TRIG MODE signal from U3020 is high, which holds U3030B set. This blocks the Async trigger path through U3030B, so the Sync trigger signal from U2020, pin 9 passes by the latch to serve as the /TRIG signal. (U3030B and U2020 are connected in a wired-OR configuration.)

Assume that the Async mode is selected. Pin 10 of U5020 is high, and pin 10 of U5050B is low. When pin 10 of U5050B is low, indicating the Async mode, pin 11 is low (which occurs when glitch recognition happens or if glitch recognition is not selected), and pin 12 is low (which occurs following the Async Filter delay, if any), the TRIG signal at U5050B pin 14 goes high. This sets the pulse-stretcher flip-flop, U4040. Its output goes high, which is inverted twice through output buffer Q7042-Q7041 to become the ASYNC TRIG OUT signal at pin 19A of P203. The flip-flop stays in the set condition until the TRIG signal returns low and, following that event, the next positive edge of ST CLK 2 occurs. Thus, the ASYNC TRIG OUT signal is high from the time that the TRIG signal moves high to the positive transition that follows the TRIG signal negative edge.

While the Async mode is selected, the /SYNC TRIG signal arms the Sync Trigger path by setting U2020 pins 14 and 9 low, just as it does in the Sync mode. The LOCKOUT signal holds U3030B pin 13 high for one clock cycle following acquisition start, causing it to ignore the clock applied to pin 11. After U6030C pin 11 moves low and LOCKOUT moves low, the signal from U6030 pin 15 clocks U3030B, and its output goes low.



2-9. Sync and Async Trigger Paths for Timing Option.

U6030D is used to select the polarity of the Async trigger. The WB3 bit, which is controlled by the CPU, selects the trigger edge by placing a high or low level on pin 13 of exclusive-OR gate U6030. This causes the signal to pass through inverted, or not, depending on the output state of U3020. The signal is used to clock U3030B.

TC Flag flip-flop U3030A produces the TC FLAG signal. When the MAC Terminal count occurs, U3030A, pin 7 moves high. At the next ST CLK 2 signal, U3030A clocks the high to its Q output, and U6030A holds the D input high. The TC FLAG signal, which is used by the CPU to indicate that the Acquisition RAM is full, remains high until the RESET signal once again moves high and resets U3030A.

Sequencer and Reset Circuit. This circuit comprises the upper third of the Trigger and Timebase Diagram, sheet 3B. The Reset Circuit consists of flip-flop U4040A, plus U5040A, U5040D, U3040A, U5040F, and U3020. The RESET signal is used to reset the Sequencer flip-flops, and three more in the Trigger circuits. When RESET goes low, the Acquisition cycle begins. In the Async mode, the TRIG MODE signal is low, so the /STORE COMMAND is passed through U3040A and inverted by U5040F to set U4040. This causes the RESET signal to move low. After the completion of the Acquisition cycle, the /DISPLAY COMMAND moves low, which resets U4040 and causes the RESET line to return high.

In the Sync Mode, the TRIG MODE signal is high, which inhibits the /STORE COMMAND path. However, the STORE signal goes high on the first STATE CLK 2 signal that follows the rising edge of /STORE COMMAND. THe high state of the STORE signal pulls the J input to U4040 low. On the following ST CLK 2 pulse, the ES CLK signal clocks U4040 back to the set condition, commencing the Acquisition cycle.

The RESET signal is also applied to U5030B, pin 14, to control the TIMING TRACE STOP signal. When RESET is high, U5030 cuts off Q6063, which cuts off Q6064, and the TIMING TRACE STOP signal moves high.

The Sequencer consists of flip-flops U4030A and U4030B. Refer to Table 2-3, which lists the input conditions for the various states.

TABLE 2-3
Sequencer States

State Name	SEQ Q1	SEQ Q2	Input Conditions Causing State
1. Reset	low	high	RESET signal high.
2. Wait for Trigger	high	high	Enters on next Timing Option clock following low RESET.
3. Delaying, or zero-delay stop	high	low	Enters on next Timing Option clock after /TRIG goes low.
4. Regular stop	low	low	Enters on next Timing Option clock following low /DLYTC.

The /DLY TC signal is the terminal count signal from the Delay Counter. This signal and the /TRIG signal from the Trigger Circuits are wired-OR connected with signals from the Sequencer that permit the TRIG signal to go low only during the "wait for trigger" state, and the /DLYTC signal to go low only during the delaying state. The Sequencer then waits until the inputs (/TRIG and /DLYTC) actually occur before it changes state. The main feedback elements for this operation are U7020C, U7020D, and U5020D. Refer to Fig. 2-10.

When the RESET signal is low and before a stop state occurs, U5030 permits the /MACEN and TIMING TRACE STOP signals go low. Note from the MAC description that the /MAC EN signal has qualifier data, but the TIMING TRACE STOP signal does not. Thus, two parallel paths exist for the generation of these signals. The WB4 line, which is applied to U8030B, controls the selection of the "regular" stop versus the "zero-delay" stop. Thus, if U8030 pin 12 is high, U5030 ignores the state of SEQ Q1, and causes TIMING TRACE STOP AND /MACEN to go high on the next Timing Option CLOCK after the trigger, and no delay occurs.

Note in Fig. 2-10 that SEQ Q1 can move low only after RESET has gone low one clock previously. The same relationship exists between SEQ Q2 and /TRIG. The pulses depicted in dashed lines indicate when the QUALIFY signal is low, which forces the /MACEN signal high. This inhibits the MAC from incrementing.

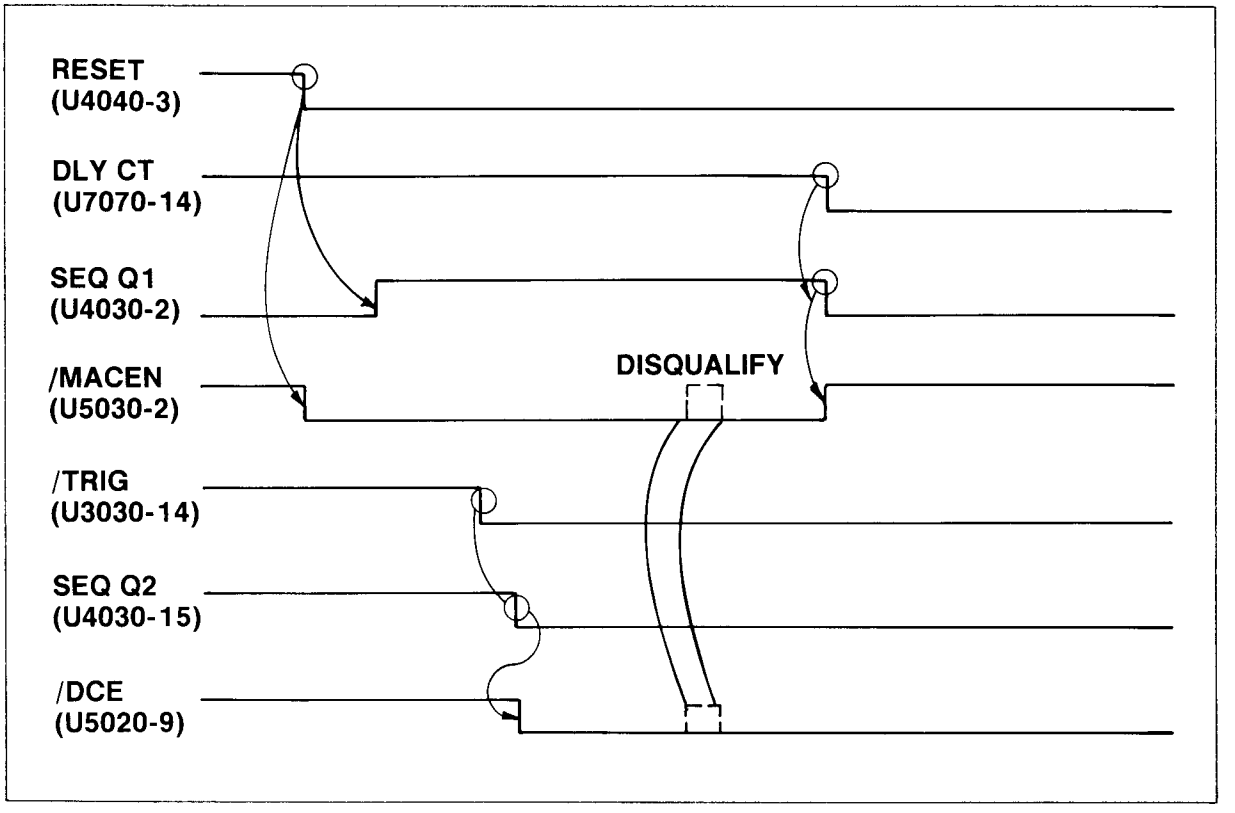


Fig. 2-10. Sequencer and Reset Circuit Waveforms.

Delay Counter. The Delay Counter, depicted on Diagram 3B, consists of U1050, U2050, U2040, and U1030, all of which are four-bit counters; buffer U1040, transistor Q2035, and inverter U5040E; and U4050B, which is configured as a 3-input OR gate. The circuit is a 16-bit binary counter that increments at the Timing Option CLOCK signal rate. The circuit is enabled to count by a low state of the /DCE signal from U5020C, which is driven by the Sequencer circuit. This signal is wired-OR connected to /MACEN, which conducts qualifier information to the Delay Counter during Sync Mode periods. Thus, when /MACEN is high, the Delay Counter does not increment.

To conserve power, the Delay Counter consists of an ECL, one TTL, and two CMOS four-bit counters. The Q3 output of ECL counter U1030 is level-shifted by Q2035 to TTL, and clocks the TTL stage, U2040. The QD output of U2040 clocks U1050 through an inverter, and the carry output of U1050

clocks U2050 directly. When U2040, U1050, and U2050 all reach terminal count, the output of U4050 (which acts like an OR gate) moves low. Then, when U1030 also reaches terminal count and the /MACEN is low, the /DLYTC can go low, signalling the Sequencer to go to the regular stop state. Note that the Delay Counter can count or end only on qualified clocks, since the /MACEN signal is wired-OR connected with both the /DCE and /DLYTC signals.

All of the Delay Counter stages are parallel-load units. thus, the counter is loaded by the CPU through the WBØ through WB7 lines, with the load command appearing on the /E9 and /E10 lines. Note that U1030 also requires a clock pulse, whereas the others load asynchronously. Consequently, the Timebase circuit is set to produce a 100-nS clock pulse on the Timing Option CLOCK line whenever U1030 is to be loaded.

CPU Address Decoder. This circuit consists of several different address buffers and decoders. The first, U1060, is the Write Bus Buffer. It buffers the signals from the Main Data Bus for distribution through the Timing Option circuits. It is gated by U4050, which is discussed next.

The Address lines from the CPU Address Bus are applied to several decoders; the A9 through A11 lines go to U3040B and U4050A. This is a range decoder that produces a low level to enable U3060 and U1060 whenever the following address ranges appear: 0:F8XX or 0:F9XX. Note that the /LATCHES SEL line from the CPU must also be low to enable U4050.

As just mentioned, U4050 enables the pin 18 input to U3060. The other enabling input, pin 19, is enabled by the /WR signal from the CPU when the Address and Data Bus lines are stable. The A5 through A8 address lines are applied to U3060, which decodes the address data into one of 11 enable lines. These drive the clock inputs of the CMOS latches in the Timing Option circuits. Note that this decoder and the previous one are both concerned with write operations only.

The Read Bus is controlled by decoder U3050. When the CPU /RD line and /SEL D line are both low, the /RBE signal is low to enable buffer U1020 (depicted on diagram 2C; it passes the CPU Data Bus contents). At the same time, the first two signals enable U3050 to decode the A9 through A11 address data. This decoder will produce one out of five outputs low; these signals are RØ through R4.

FRONT-END BOARD CIRCUIT DESCRIPTION

Introduction

The circuits on the Front End Board provide the following:

1. Pulse shaping of the non-symmetrical raw clock pulses for the low-power components used in other areas of the 7D02.

2. A preliminary clock qualification for generation of a state clock, thus defining the state time of the remainder of the Acquisition Unit.

3. High-speed control of the state clock.

4. Access to the PROM in the Personality Module (also called probe).

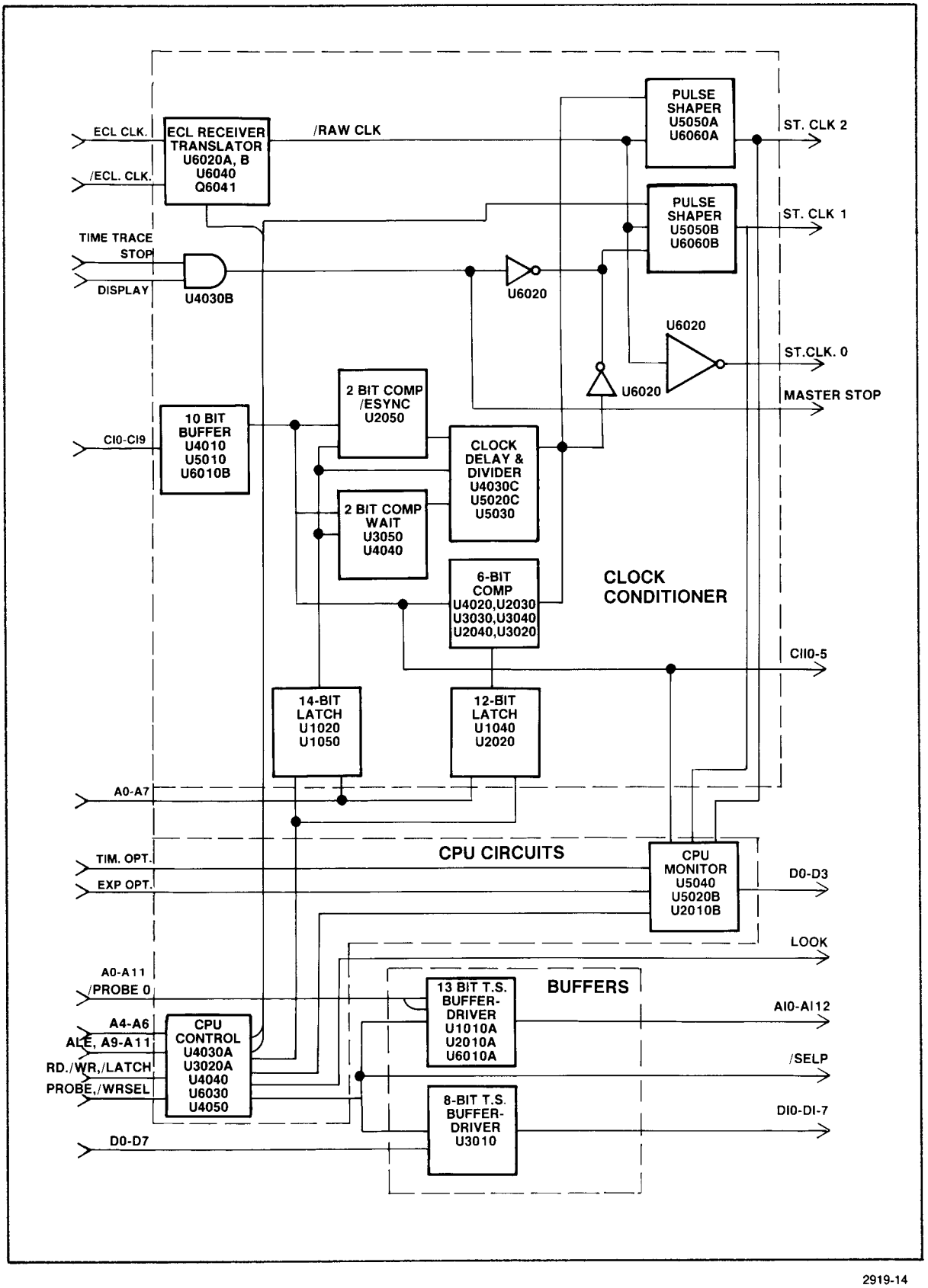
Block Diagram Description

Refer to the detailed block diagram of the Front End circuits Fig. 2-11A for 670-5989-00 boards, Fig. 2-11B for 670-5989-00 boards These circuits relate to the display menu in the following ways:

1. In the upper section of the screen, the SLOW CLOCK indicator blinks whenever the master clock frequency is less than 500 Hz.

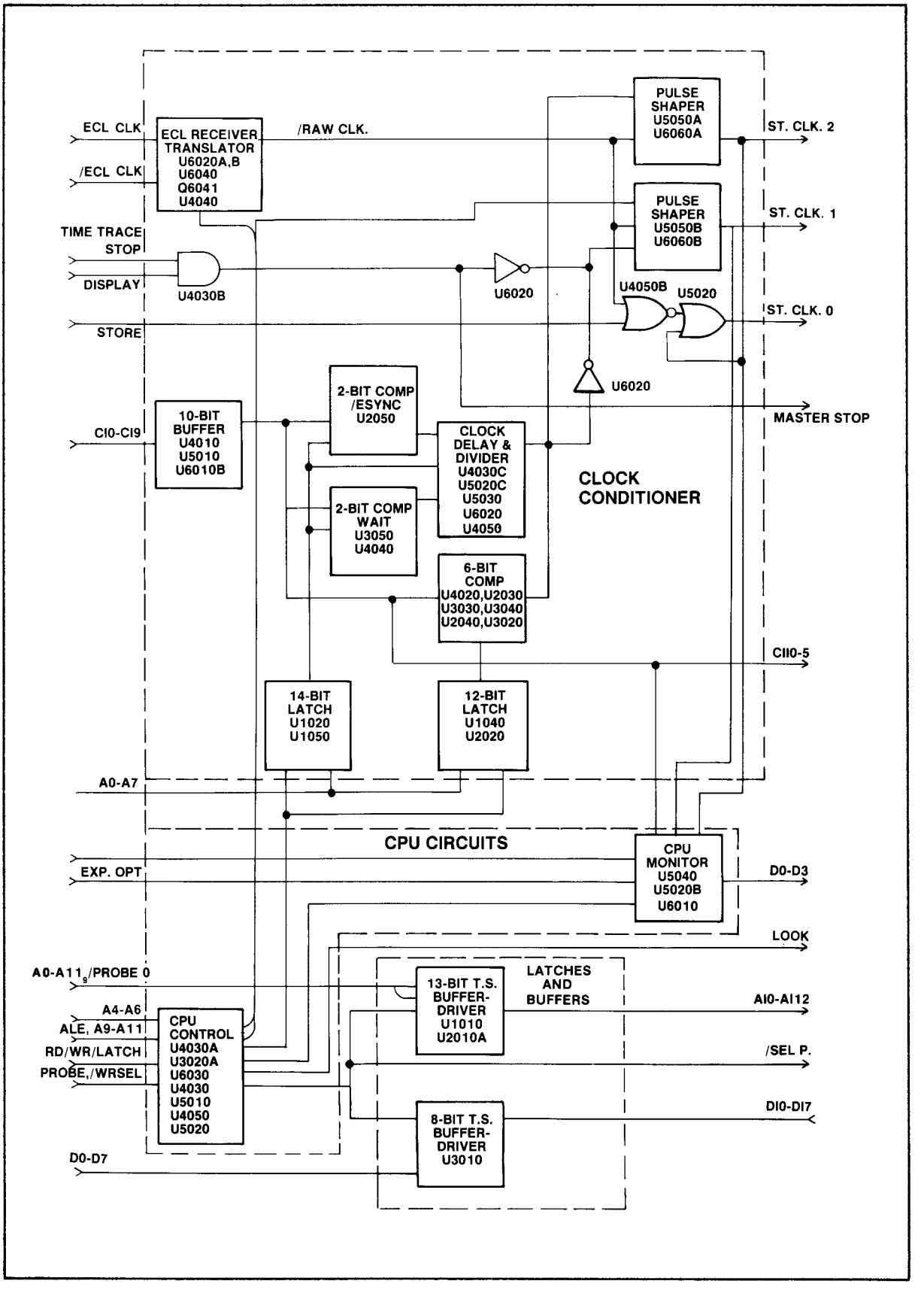
2. Also in the upper screen is a probe-specific message. The PM101 General Purpose Probe uses this portion of the display to report the status of the C7 input The PM102/103 reports CPU HALTED (if the microprocessor under test is halted) in this screen location. Other probes generate specific messages of interest for processors they test.

3. The display section entitled TRIGGER MAIN, STANDARD CLOCK QUAL, applies to these circuits. This menu segment expands to include user clock qualification definitions, positive or negative-edge clock selection, and user clock syntheses definitions.



2919-14

Fig. 2-11A. Block Diagram of Front End Circuits (670-5989-00 Boards Only)



2919-15

Fig. 2-11B. Block Diagram of Front End Circuits

(670-5989-01 Boards Only)

Clock Conditioner Circuits (670-5989-00 boards only)

Beginning at the top of Fig. 2-11A, the ECL clock signal from the probe is translated into TTL levels in the ECL Receiver-Translator, where clock polarity selection also occurs. The RAW CLOCK signal is then fed into the two Pulse Shaper circuits and the ST CLK Ø Buffer, each of which produces a different version of the RAW CLOCK signal: ST CLK Ø is simply a buffered version of the RAW CLOCK signal. The Pulse Shapers produce a 40-nS clock pulse, regardless of the pulse width of the input signal. The CIØ-CI9 lines from the probe are fed to the 10-Bit Buffer for further transmission to the Clock Qualifying circuits, which consist of the two-bit Esync and Wait Comparators, the Clock Delay-Divider, and the Six-bit Comparator.

The Clock Qual Comparator is basically a six-bit word recognizer. It is programmed to select the appropriate clock pulses from the /RAW CLK signal, to form the state clock signals. The output of the Six-bit Comparator joins with the output of the Programmable Delay-divide circuit in controlling the operation of the two Pulse Shaper circuits.

The Clock Delay-Divide circuit receives the /RAW CLK, WAIT, and ESYNC signals, plus the programming bits from the 14-bit Latch. The circuit shifts a continuous ESYNC pulse as much as four raw clock pulses to produce a state clock signal that is delayed as much as four clock pulses from /ESYNC. The circuit can also divide the raw clock by 2, 3, or 4 to produce the state clock signal. It can use the /WAIT signal to add extra raw clock pulses in either of the previous two operations.

Clock Conditioner Circuits (670-5989-01 boards only)

Beginning at the top of Fig. 2-11B, the ECL clock signal from the probe is translated into TTL levels in the ECL Receiver-Translator, where clock polarity selection also occurs. The RAW CLOCK signal is then fed into the two Pulse Shaper circuits and the ST CLK Ø Circuit, each of which produces a different version of the RAW CLOCK signal: ST CLK Ø is either ST CLK 2 or an inverted form of RAW CLK, depending on the status of STORE. With STORE high, ST CLK Ø is ST CLK 2; with STORE low, ST CLK Ø is RAW CLK inverted. This allows the STORE/DISPLAY master flip-flop to be clocked the first time by ST CLK Ø even when ST CLK 2 is very heavily qualified. The Pulse Shapers produce a 40-nS clock pulse, regardless of the pulse width of the input signal. The CIØ-CI9 lines from the probe are fed to the 10-Bit

Buffer for further transmission to the Clock Qualifying circuits, which consist of the two-bit Esync and Wait Comparators, the Clock Delay-Divider, and the Six-bit Comparator.

The Six-Bit Comparator performs clock qualification by acting as a word recognizer. It is programmed to select the appropriate clock pulses from the /RAW CLK signal, to form the state clock signals. The output of the Six-bit Comparator joins with the output of the Programmable Delay-divide circuit in controlling the operation of the two Pulse Shaper circuits.

The Clock Delay-Divide circuit receives the /RAW CLK, WAIT, and ESYNC signals, plus the programming bits from the 14-bit Latch. The circuit shifts a continuous ESYNC pulse as much as four raw clock pulses to produce a state clock signal that is delayed as much as four clock pulses from /ESYNC. The circuit can also divide the raw clock by 2, 3, or 4 to produce the state clock signal. It can use the /WAIT signal to add extra raw clock pulses in either of the previous two operations.

Buffer Circuits (670-5989-00 boards only)

The Buffer circuits consist of a 13-bit Buffer-driver, which provides buffering for the AØ-A11 bits from the CPU and for the /PROBE Ø signal from the CPU. The Buffer-driver passes address signals from the CPU to the personality module (probe) to control the PROM in the module.

The other circuit in this group is the 8-bit Buffer, which passes the data from the personality module to the CPU. Control lines from the CPU Control circuits, discussed next, enable or disable both of the Buffers as required by the CPU.

Latch and Buffer Circuits (670-5989-01 boards only)

The Latch circuits consist of a 13-bit Latch (U1010 & U2010), which provides latching for the AØ-A11 bits and /PROBE Ø from the CPU. The latches pass address signals from the CPU to the personality module (probe) to control the PROM in the module.

The other circuit in this group is the 8-bit Buffer, which passes the data from the personality module to the CPU. Control lines from the CPU Control circuits, discussed next, enable or disable both of the Buffers as required by the CPU.

CPU Circuits (670-5989-00 boards only)

CPU Monitor. The CPU Monitor keeps track of several functions on the board and notifies the display, CPU, or other circuits of the state of those functions. The functions monitored are:

1. If the DØ line is low, a slow clock indication appears on the screen.

2. If the D1 line is low, the Expansion Option is installed in the 7D02.

3. If the D2 line is low, the Timing Option is installed in the 7D02.

4. If the D3 line is low, the CPU is asynchronously checking the C7 line at the probe tip like a logic probe.

The CPU Control Circuits, using the /RD, /WR, and /LATCHES SEL signals (plus the A4-A6 and A9-A11 bits from the CPU) control the selection of the state clock division and delay functions, plus the selection of bit C4 through C9 as clock qualifying signals. The /WR SEL signal causes the generation of state clocks during diagnostics. The PROBE, ALE, and /RD signals produce the LOOK and /SEL P signals that are applied to the probe circuits.

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State Clock Generation (670-5989-00 boards only)

The Front End Board develops three state clock signals: The first, ST CLK Ø, is simply the inverted from of the /RAW CLK signal. The ST CLK 1 signal is a controlled pulse-width, qualified clock that is turned off during display and turned on during storage. The ST CLK 2 signal is identical to ST CLK 1, except that it runs continuously. For purposes of discussion, assume that no clock qualification and no clock synthesis is selected, and that the menu selection is for a positive edge. Refer to Diagram 4A, which depicts the circuits that perform the clock conditioning function.

Raw Clock Generation. The ECL differential CLK and /CLK signals from the Probe enter the board via pins 26D and 26C, respectively, of P104. The two signals are terminated and shifted in level by R6040, R6041, R6033, R6045, R6032, and two 6.2-volt Zener diodes, VR6040 and VR6041. This network changes the ECL signals at the input to levels suitable for the inputs of U6040 (-7 volts on U6040, pin 2, and -7.8 volts on U6040, pin 10).

In order to select a postive edge of the clock, it is necessary to set pin 12 of latch U1020 low. This low is applied to U6020A and U5010, p;in 8. This in turn places a negative voltage at pin 1 and 11 of U6040 (about -3.2 volts) and a less negative voltage at pins 4 and 8 (about -2 volts). The two center transistors are on, and the two outer transistors are off, making the conduction path to pin 6 of U6040, which passes the CLK signal to the base of Q6041.

If a negative edge is required for a clock, the CPU loads a high at output pin 12 of U1020. This, by way of U5010 and U6020, reverses the condition of the switching transistors. The potentials applied to the bases of the switching transistors in U6040 cause the outer pair to conduct and

the inner pair to cut off. Thus, the /CLK signal is passed to the next stage.

Q6041, VR6049, and related components form the Raw Clock Buffer. The clock signal from U6040 is clamped by CR6045, then applied to the base of Q6041, an emitter follower. The circuit is designed to produce a very fast signal that swings from about 2.5 volts to 0.3 volts. The signal from the emitter is called /RAW CLK, and is applied to the input of U6020F, the ST CLK Ø Buffer; to the clock input of U5030, the Programmable Delay-divide circuit; and to U5050A and U5050B, the two state clock Pulse Shaper stages.

Transistor Q6043 is used to shut off the state clock signals when diagnostic routines require a quiet clock line. This is done by setting the D7 bit high, which turns on Q6043 and locks the /RAW CLOCK line at near ground potential.

Pulse Shaper Circuits. The QUAL 1 signal from the Six-bit Comparator on Diagram 4B is applied to the J input, pin 11, of U5050B. It is assumed that no clock qualification has been selected by the operator, so pin 11 of U5050B is high. (Note that several sources control pin 11 of U5050B, so all must permit the line to go high.) At the negative edge of the raw clock applied at pin 13, U5050B pin 9 goes high and pin 7 goes low. The negative transition from pin 7 is applied through delay line U6050B to the clear input of U5050B, pin 14. About 40 nS after the clock, U5050B clears itself. (30 nS is from the delay line; the other 10 nS is from the pulse rise time and the delay through the flip-flop.) The output from U5050B is a positive pulse of approximately 40 nS duration that occurs with each negative edge applied.

The other Pulse shaper consists of U5050A and related components. Like the previously described circuits, no clock qualifier has been chosen, so the wire-anded Six-bit Qual Comparator is not pulling low on the J input of U5050A. Unlike the first Pulse Shaper, however, this J input (pin 3) is also controlled by the Master Stop Gate, which consists of U4030B and U6020C. The output of U4030B is called MASTER STOP, which, if high, signifies that the timing option and the main acquisition memory have completed data storage. The signals at the inputs of U4030B are the TIMING TRACE STOP and DISPLAY signals, both of which are presently high. Thus, the J input to U5050A is held low, so the flip-flop does not produce any clock pulses.

Now assume that the 7D02 switches into the store mode. First, the ST CLK Ø signal from buffer U6020 is sent out to the Acquisition Memory

circuits via P204, pin 21A. This signal clocks the Store-display flip-flop, so the DISPLAY signal at pin 20A of P204 moves low. This causes the MASTER STOP signal to move low, and U6020C permits the other circuits to hve control of the J input of U5050A. At the next clock pulse, ST CLK 1 begins. This signal is applied to the Word Recognizer, Expansion Option, Acquisition Memory, and State Machine boards; the ST CLK 2 signal is applied to the Trigger, IC ACQ Mem, and Front Panel Boards.

Slow-clock Detector. The ST CLK 1 and ST CLK 2 signals are also applied to the clock inputs of U5040A and U5040B. These are one-shots that detect if a slow clock is occurring. When the 7D02 is operating in the store mode, both the ST CLK 1 and ST CLK 2 signals are running, and both one-shots are triggered. The RC combination of each of the one-shots sets the operating period at approximately 1 mS. Thus, for each clock applied to the one-shots, a 1 mS pulse is applied to U5020, which combines the outputs of the one-shots. (In earlier models of the 7D02, only U5040A is connected to U5020B, and U5020B pin 5 is grounded. Thus, only state clock 2 is monitored.) Since both one-shots are re-triggerable, so long as neither of the state clocks slow to more than a 1 mS period, the output of U5020B will remain low and the DØ line from U2010 will also remain low.

CPU Monitor. Periodically, the CPU interrogates U2010 by reading at location page Ø at FF60. When this occurs, pin 19 of U2010 moves low, which enables the CPU to read the outputs of U2010. The low at pin 19 of U2010 comes from U4050.

CPU Control Circuits. Refer to Diagram 4B. One of the CPU Control Circuits consists of U4030A, U4050, and U4040D. The /WR and /RD signals connect to the inputs of U4040D; if either of these signals are low, indicating that a read or write operation is in process, pin 5 of U4050 is also low. (Recall that the address set for this operation is 0:FF6X.) The /LATCH SEL signal from P204 pin 4A is the first two digits of the address page 0 and F, so pin 4 of U4050 is also enabled. The third digit of the address, an "F", is applied to U4030A, so the pin 6 input of the decoder is enabled. The 6 of the address is applied to pins 1, 2, and 3 of U4050, which are the A4, A5, and A6 lines, respectively. Under the conditions just set, pin 9 of U4050 goes low, which indicates that the CPU is reading buffer U2010B (enabled at pin 19 by the low from U4050). This buffer has three inputs other than the slow-clock indication input at pin 11. These include the pin 13 input from P204, pin 17B, indicating if the Expansion Option is installed; the pin 15 input from P204, pin 17A, indicating if the Timing Option is installed; and pin 17, which is controlled

by U5010, pin 7. This line, labelled /C7, is a signal direct from the probe. It is an asynchronous sampling of C7 by the CPU, the result of which is displayed in the upper section of the 7D02 screen. Anytime the C7 signal is a high at the probe tip, a message is posted on the 7D02 display; if the signal is low, the opposite message is posted. This message is contained in the individual ROMs in the Personality Module. The messages are specific to the particular personality module connected.

ROM Read Control. The CPU reads the Probe ROM only when the system is in the Display mode. It does so by selecting Page 3 at address E000 to FFFF. This permits the CPU to address as much as 8K of ROM in any probe that is connected to the 7D02. For example, consider using the lower 4K: calling Page 3 with address EXXX stimulates the CPU to pull the PROBE signal high. It moves high well before the ALE signal goes low at the input of buffer U6010F, which removes spurious noise from the ALE signal before applying it to U6030B. When the ALE signal clocks U6030B, pin 11 (the Q output) of the flip-flop goes high, which is passed through buffer U6010G to J104, pin 27D, the LOOK signal. When high, this signal shuts off the high-speed buffers in the probe circuits.

Later, the /RD signal from the CPU, via P204, pin 14B, moves low; since the pin 1 input of U5020A is already low, the output moves low. This is the /SEL P line, which enables buffers U6010A, U2010A, U1010, and U3010, the buffers that transfer data to and from the probe. U3010, a tri-state buffer, drives the data bus to the CPU directly. U1010, U2010B, and U6010 address the probe circuit. The /SEL P signal from U5020 is also sent out J104, pin 25C, to access the P-ROM in the personality module.

State Clock Generation (670-5989-01 boards only)

The Front End Board develops three state clock signals: ST CLK Ø is either ST CLK 2 or an inverted form of RAW CLK, depending on the status of STORE. With STORE high, ST CLK Ø is ST CLK 2; with STORE low, ST CLK Ø is RAW CLK inverted. The ST CLK 1 signal is a controlled pulse-width, qualified clock that is turned off during display and turned on during storage. The ST CLK 2 signal is identical to ST CLK 1, except that it runs continuously. For purposes of discussion, assume that no clock qualification and no clock synthesis is selected, and that the menu selection is for a positive edge. Refer to Diagram 4A, which depicts the circuits that perform the clock conditioning function.

Raw Clock Generation. The ECL differential CLK and /CLK signals from the Probe enter the board via pins 26D and 26C, respectively, of P104. The two signals are terminated and shifted in level by R6040, R6041, R6033, R6045, R6032, and two 6.2-volt Zener diodes, VR6040 and VR6041. This network changes the ECL signals at the input to levels suitable for the inputs of U6040 (-7 volts on U6040, pin 2, and -7.8 volts on U6040, pin 10).

In order to select a postive edge of the clock, it is necessary to set pin 12 of latch U1020 low. This low is applied to U4040 and U6020A, pin 8. This in turn places a negative voltage on pins 1 and 11 of U6040 (about -3.2 volts) and a less negative voltage at pins 4 and 8 (about -2 volts). The two center transistors are on, and the two outer transistors are off, making the conduction path to pin 6 of U6040, which passes the CLK signal to the base of Q6041.

If a negative edge is required for a clock, the CPU loads a high at output pin 12 of U1020. This, by way of U4040 and U6020, reverses the condition of the switching transistors. The potentials applied to the bases of the switching transistors in U6040 cause the outer pair to conduct and the inner pair to cut off. Thus, the /CLK signal is passed to the next stage.

Q6041, VR6049, and related components form the Raw Clock Buffer. The clock signal from U6040 is clamped by CR6045, then applied to the base of Q6041, an emitter follower. The circuit is designed to produce a very fast signal that swings from about 2.5 volts to 0.3 volts. The signal from the emitter is called /RAW CLK, and is applied to the input of U4050B, the first gate of the ST CLK Ø Circuit; to the clock input of U5030, the Programmable Delay-divide circuit; and to U5050A and U5050B, the two state clock Pulse Shaper stages.

Transistor Q6043 is used to shut off the state clock signals when diagnostic routines require a quiet clock line. This is done by setting the D7 bit high, which turns on Q6043 and locks the /RAW CLOCK line at near ground potential.

Pulse Shaper Circuits. The QUAL 1 signal from the Six-bit Comparator on Diagram 4B is applied to the J input, pin 11, of U5050B. It is assumed that no clock qualification has been selected by the operator, so pin 11 of U5050B is high. (Note that several sources control pin 11 of U5050B, so all must permit the line to go high.) At the negative edge of the raw clock applied at pin 13, U5050B pin 9 goes high and pin 7 goes low. The negative transition from pin 7 is applied through delay line U6050B to the clear input of U5050B, pin 14. About 40 nS after the clock, U5050B clears itself. (30 nS is from the delay line; the other 10 nS is from the pulse rise time and the delay through the flip-flop.) The output from U5050B is

a positive pulse of approximately 40 nS duration that occurs with each negative edge applied.

The other Pulse shaper consists of U5050A and related components. Like the previously described circuits, no clock qualifier has been chosen, so the wire-anded Six-bit Qual Comparator is not pulling low on the J input of U5050A. Unlike the first Pulse Shaper, however, this J input (pin 3) is also controlled by the Master Stop Gate, which consists of U4030C and U6020C. The output of U4030C is called MASTER STOP, which, if high, signifies that the timing option and the main acquisition memory have completed data storage. The signals at the inputs of U4030C are the TIMING TRACE STOP and DISPLAY signals, both of which are presently high. Thus, the J input to U5050A is held low, so the flip-flop does not produce any clock pulses.

Now assume that the 7D02 switches into the store mode. First, the ST CLK Ø signal from U5020C is sent out to the Acquisition Memory circuits via P204, pin 21A. This signal clocks the Store-display flip-flop, so the DISPLAY signal at pin 20A of P204 moves low. This causes the MASTER STOP signal to move low, and U6020C permits the other circuits to have control of the J input of U5050A. At the next clock pulse, ST CLK 1 begins. This signal is applied to the Word Recognizer, Expansion Option, Acquisition Memory, and State Machine boards; the ST CLK 2 signal is applied to the Trigger, IC ACQ Mem, and Front Panel Boards.

Slow-clock Detector. The ST CLK 1 and ST CLK 2 signals are also applied to the clock inputs of U5040A and U5040B. These are one-shots that detect if a slow clock is occurring. When the 7D02 is operating in the store mode, both the ST CLK 1 and ST CLK 2 signals are running, and both one-shots are triggered. The RC combination of each of the one-shots sets the operating period at approximately 1 mS. Thus, for each clock applied to the one-shots, a 1 mS pulse is applied to U5020, which combines the outputs of the one-shots. (In earlier models of the 7D02, only U5040A is connected to U5020B, and U5020B pin 5 is grounded. Thus, only state clock 2 is monitored.) Since both one-shots are re-triggerable, so long as neither of the state clocks slow to more than a 1 mS period, the output of U5020B will remain low and the DØ line from U2010 will also remain low.

CPU Monitor. Periodically, the CPU interrogates U6010 by reading at location page Ø at FF60. When this occurs, pin 1 of U6010 moves low, which enables the CPU to read the outputs of U6010. The low at pin 1 of U6010 comes from U2055-9.

CPU Control Circuits. Refer to Diagram 4A. One of the CPU Control Circuits consists of U4030A and B, and U2055, The /WR and /RD signals connect to the inputs of U4030B; if either of these signals are low, indicating that a read or write operation is in process, pin 5 of U2055 is also low. (Recall that the address set for this operation is 0:FF6X.) The /LATCH SEL signal from P204 pin 4A is the first two digits of the address page 0 and F, so pin 4 of U2055 is also enabled. The third digit of the address, an "F", is applied to U4030A, so the pin 6 input of the decoder is enabled. The 6 of the address is applied to pins 1, 2, and 3 of U2055, which are the A4, A5, and A6 lines, respectively. Under the conditions just set, pin 9 of U2055 goes low, which indicates that the CPU is reading buffer U6010B (enabled at pin 1 by the low from U2055). This buffer has three inputs other than the slow-clock indication input at pin 2. These include the pin 4 input from P204, pin 17B, indicating if the Expansion Option is installed; the pin 6 input from P204, pin 17A, indicating if the Timing Option is installed; and pin 8, which is controlled by U5010, pin 7. This line, labelled /CII7, is a signal direct from the probe. It is an asynchronous sampling of C7 by the CPU, the result of which is displayed in the upper section of the 7D02 screen. Anytime the C7 signal is a high at the probe tip, a message is posted on the 7D02 display; if the signal is low, the opposite message is posted. This message is contained in the individual ROMs in the Personality Module. The messages are specific to the particular personality module connected.

ROM Read Control. The CPU reads the Probe ROM only when the system is in the Display mode. It does so by selecting Page 3 at address E000 to FFFF. This permits the CPU to address as much as 8K of ROM in any probe that is connected to the 7D02. For example, consider using the lower 4K: calling Page 3 with address EXXX stimulates the CPU to pull the PROBE signal high. It moves high well before the ALE signal goes low at the input of buffer U6010F, which removes spurious noise from the ALE signal before applying it to U6030B. When the ALE signal clocks U6030B, pin 10 (the /Q output) of the flip-flop goes high, which is passed through buffer U5010D to J104, pin 27D, the LOOK signal. When high, this signal shuts off the high-speed buffers in the probe circuits.

Later, the /RD signal from the CPU, via P204, pin 14B, moves low; since the pin 2 input of U5020A is already low, the output moves low. This is the /SEL P line, which enables latches U1010 and U2010, and buffer U3010, the latches and buffers that transfer data to and from the probe. U3010, a tri-state buffer, drives the data bus to the CPU directly. Latches U1010, and U2010 address the probe circuit. The /SEL P signal from U5020

is also sent out J104, pin 25C, to access the P-ROM in the personality module.

Clock Qualifier Circuits (670-5989-00 boards only)

This discussion includes a description of the Six-bit Comparators, the Two-bit Wait Comparator, the Two-bit Esync Comparator, and the Clock Delay-divider circuit. Refer to Table 2-4A, which lists the raw clock selection codes.

TABLE 2-4A
Raw Clock Selection Codes

	Data Bus Lines								
	D7	D6	D5	D4	D3	D2	D1	DØ	
Address									Upper Control Lines
0:FFØX			-	+					C4
0:FFØX	-	+							C5
0:FFØX					-	+			C6
0:FFØX							-	+	C7
0:FF1X							-	+	C8
0:FF1X					-	+			C9

Placing a 1 at any of the locations selects a clock at the indicated polarity of the signals. For example, a clock at the positive level of C7 at the the probe tip is required. Address 0:FFØX is called, and line DØ is pulled high (Ø1 hex on the data bus). These conditions are set before the store cycle begins. The expression for this function is:

C4*C5*C6*C7*C8*C9 = CLK.

Likewise, the function for removing clocks is:

/C4+/C5+/C6+/C7+/C8+/C9 = no CLK.

Six-bit Comparator. Refer to Diagram 4B. There are two comparators in parallel, one of which generates the QUAL Ø signal, the other of which generates QUAL 1. The first consists of U2030, U2040, and U3020. The second comparator consists of U3030, U3040, and U4020. Each comparator is a set of AND-OR INVERT gates connected in a wire-OR configuration. Control of the Comparators is from the ten-bit buffer, consisting of U4010, U5010, and U6010; data to the Comparators is from the twelve-bit latch (U1040 and U2020).

Assume that the clock is desired only when the C9 bit is high Referring to Table 2-4, note that the C9 bit is listed across from address page Ø at FF1X. The CPU stimulates U4050 to send a clock pulse to pin 9 of U2020. At this time, the D3, D2, D1, and DØ inputs to U2020 are a 4 hex; thus D2 is high, which in turn makes the D22 output from U2020 high. This applies a high level to pin 12 of both U3020 and U4020. The remaining pins of U3020 and U4020 are low.

The CI9 bit from the probe enters the board at P104-24D and is applied to pin 4 of U5010 and pin 15 of U6010, both part of the 10-bit Buffer. Through the buffers, the bit is applied to pin 11 of U3020 and pin 11 of U4020 from U5010, and to pin 4 of U3020 and pin 4 of U4020 from U6010. The 4 hex set previously causes U3020 pins 9, 2, and 5 to be low, and a high level at U3020-12 and U4020-12. Thus, the high at pin 12 of the two gates enables the CI9 signal to pass through U3020 and U4020, which makes QUAL 1 and QUAL 0 both high. These two signals are applied to the J inputs of U5050 (pins 3 and 11), the two Pulse Shaper circuits on Diagram 4A. The high at each J input causes the flip-flop to produce a clock output at the next raw clock occurrence. If, for example, the CI9 line is high with every other clock cycle, the two Pulse Shapers will produce a state clock 1 and 2 with every other raw clock cycle.

In conclusion, the Six-bit Comparators are used to qualify the ST CLK 1 and ST CLK 2 signals, so that clocks may be skipped, deleted, or otherwise altered by comparison with the CI4-CI9 bits from the probe.

Clock Delay and Divider. Refer to Table 2-5A, which lists the WAIT and ESYNC generation codes. This discussion is based on an example of a delay-by-two clock generation. Thus, an ESYNC function must be generated each time a delay by two is required. In this example, then, an ESYNC function is to be produced when C6 moves high. In Table 2-5A, the address for C6 is address page Ø at FF3X for a positive ESYNC on C6. As a result, latch U1050 must have a hex 80 stored; the CPU applies the required data to U4050, which produces a clocking signal from pin 12, to be applied to pin 11 of U1050, clocking the hex 80 into U1050. This makes pin 6 of U1050 high; the remainder of the output are low. The high at pin 6 is applied to pin 11 of U2050, the Esync Comparator. The CI6 line at pin 23C of P104 is now high; it connects to U5010, pin 17, and through U4010 pin 2 t 18, the line connects to pin 10 of U2030 and U3030, and to pin 12 of U2050. As a result of the high at pin 12 of U2050, the /ESYNC signal at pin 8 goes low, which makes the output of U4030B on Diagram 4A go low.

TABLE 2-5A
/WAIT and /ESYNC Generation Codes

	D7	D6	D5	D4	D3	D2	D1	DØ	
0:FF3X	S+	S-							C6
0:FF3X					W+	W-			C7
0:FF3X			S+	S-					C8
0:FF3X							W+	W-	C9

(This table represents: C6+C8 = /ESYNC, and C7+C9 = /WAIT.)

Now that the ESYNC condition is developed, the WAIT condition must be developed. In the example, a high level on the C9 line produces a WAIT state. Referring once again to Table 2-5A, for a WAIT condition on a C9 high state, an 02 hex is required. However, to avoid destroying what is already loaded into U1050, an 82 hex is loaded into U1050. The CPU clocks U1050 by the usual means (U4050), and the result at the output of U1050 is a high state at pin 15 of U1050, which makes pin 11 of U3050 high. In order to pass this level through the Wait Comparator, pin 12 must also be high. The CI9 signal from P104 pin 24D is fed to pin 4 of U5010 and pin 15 of U6010, through the buffers and to pin 11 of U3020 and pin 2 of U3050 in inverted form, and to pin 4 of U3020 and pin 12 of U3050 uninverted. The high at pins 11 and 12 of U3050 permits the /WAIT signal at output pin 8 to go low; the /WAIT signal is applied to pin 3 of U4030B and pin 9 of U5030 (see Diagram 4A). The low at pin 9 of U5030 holds U5030 from acting at present. (See Table 2-6A, which lists the states of U5030.)

TABLE 2-6A
U5030 Truth Table

Pin 9	Pin 11	Function
0	0	Hold
0	1	Not permitted
1	0	Load
1	1	Shift Right

The /WAIT signal is also applied to pins 4 and 10 of U4040. This circuitry performs a special case of the WAIT function, where wait states are to be produced at the same time as clock outputs, as when a delay by 1 or divide by 2 is selected. In such cases, only ESYNC and WAIT states are available. Referring to Table 2-7A, note that a WAIT state overrides ESYNC. Thus, if both are selected to occur simultaneously, the ESYNC will not function. Thus, when the /WAIT signal goes low, the two sections of U4040 pull the QUAL Ø and QUAL 1 lines low, disabling any clock output until the /WAIT signal returns high, at the end of the wait state.

TABLE 2-7A
Clock Delay and Divider Truth Table

Function	/ESYNC	/WAIT	CLOCK Output
Delay by n	low	high	t_0 + n
	high	low	waiting (adding clock time if output pending)
	low	low	waiting (adding clock time if output pending)
	high	high	no effect (no output if previous delay completed)
Divide by n	high	high	divde by n
	low	high	t_0 + (n-1) synchronized
	high	low	waiting (adding clock time)
	low	low	waiting (adding clock time)

NOTES: 1. /ESYNC does not override a pending output. Thus, when in a divide mode, changing the phase of division can cause false outputs.
2. The ESYNC and WAIT circuits are level-sensitive.
3. The ESYNC and WAIT functions should not be selected if a divide by 1 or delay by Ø is selected.

Example of Delay-by-two Operation. Returning to the Clock Delay and Divide circuit, the next example is a delay-by-two operation. Refer to Table 2-8A, which lists the CPU Control Codes for clock synthesis In this example, for a delay-by-two and a negative-going clock, a code 5D hex is required. This code is applied to U1020 by way of the data bus inputs. The CPU generates a strobe signal by way of U4050, which is supplied to clock pin 11 of U1020. Beginning at bit Ø, output pin 12 is high, which causes the negative edge to be selected by U6040, as discussed earlier in the description. Bit 1 is not used in this circuit. Bit 2 from pin 16 (the Delay bit) is high, and is applied to U5030, pin 3. Bit 3 from pin 19 is

also high; it is applied to pin 2 of U5030. (Pins 2, 1 13, and 12 of U5030 are the A, B, C, and D parallel inputs to the shift register.)

TABLE 2-8A
CPU Control Codes for Clock Synthesis

at ADDR CF4Ø	D6	D5	D4	D3	D2	D1	DØ	Operation	CLK Polarity
	Ø	1	1	1	1	Ø	Ø	Delay by 1	plus
	Ø	1	1	1	1	Ø	1	Delay by 1	minus
	1	Ø	1	1	1	Ø	Ø	Delay by 2	plus
	1	Ø	1	1	1	Ø	1	Delay by 2	minus
	1	1	Ø	1	1	Ø	Ø	Delay by 3	plus
	1	1	Ø	1	1	Ø	1	Delay by 3	minus
	1	1	1	Ø	1	Ø	Ø	Delay by 4	plus
	1	1	1	Ø	1	Ø	1	Delay by 4	minus
	Ø	Ø	Ø	Ø	Ø	Ø	1	Don't care	
	Ø	1	Ø	Ø	Ø	Ø	Ø	Divide by 2	plus
	Ø	1	Ø	Ø	Ø	Ø	1	Divide by 2	minus
	1	Ø	1	Ø	Ø	Ø	Ø	Divide by 3	plus
	1	Ø	1	Ø	Ø	Ø	1	Divide by 3	minus
	1	1	Ø	1	Ø	Ø	Ø	Divide by 4	plus
	1	1	Ø	1	Ø	Ø	1	Divide by 4	minus

DØ is the clock polarity bit; D2 is the delay bit.
(Example: to set up a delay-by-four, plus polarity, 1110100 (74 hex) is written at address CF4Ø.)

The following discussion describes how U5030 is loaded. Note that the /ESYNC pulse was generated in previous discussions. When /ESYNC goes low, this causes pin 11 of U5030 to go low. Since there is not wait signal at this time, pin 9 of the register is high, and the data from U1020 is loaded into the register. Thus, QD pin 10 is now low, QC pin 8 is high, and QB pin 6 is low. The high on pin 10 is inverted through U6020D and E, and applied to the J inputs of U5050 (the two pulse shapers), holding both from producing clock pulses for now. As soon as the /ESYNC pulse returns high, so does U5030 pin 11. A high at pin 11 and pin 9 of the register makes it shift to the right. At the next raw clock following the end of the ESYNC pulse, the low at QC is shifted over to the QD output, making pin 10 go low. The resulting high at the J inputs to U5050 permits the pulse shapers to produce state clock signals at the following raw clock edge. Then, the register shifts again, which causes a high to occur at the QD output. As a result, a data strobe output at ST CLK 1 and ST CLK 2 are

produced from the ESYNC pulse. Now, another ESYNC pulse is sent to U5030, and it repeats the operation just described. The result of this is that the two ESYNC pulses cause a delay-by-two operation to occur in producing the data strobe signal (called the State Clock).

Divide-by-three Operation. The next example is of dividing by three, using the positive edge of the raw clock signal (see Fig. 2-12A). Referring to Table 2-8A, to divide by three on a positive transition requires that a 5Ø hex be loaded into U1020 from the CPU. When the code is loaded, pin 3 of U5030 is low, and the A, B, C, and D inputs are low, high, low, and high, respectively. This particular code causes U5030 to load, then shift twice; load, then shift twice, etc., in a continuous series of operations. This occurs because U5020C is first disabled, which, along with the high states at pins 4 and 3 of U4030, cause pins 9 and 11 of U5030 to remain high. Now, on the first shift of U5030, the high at QB shifts to QC, so U5020 is still disabled, and conditions have not changed at the output of U4030A. On the next shift, both Qb and Qc are low, so the output of U4030 goes low. This reinstates the load operation, and the cycle begins once again.

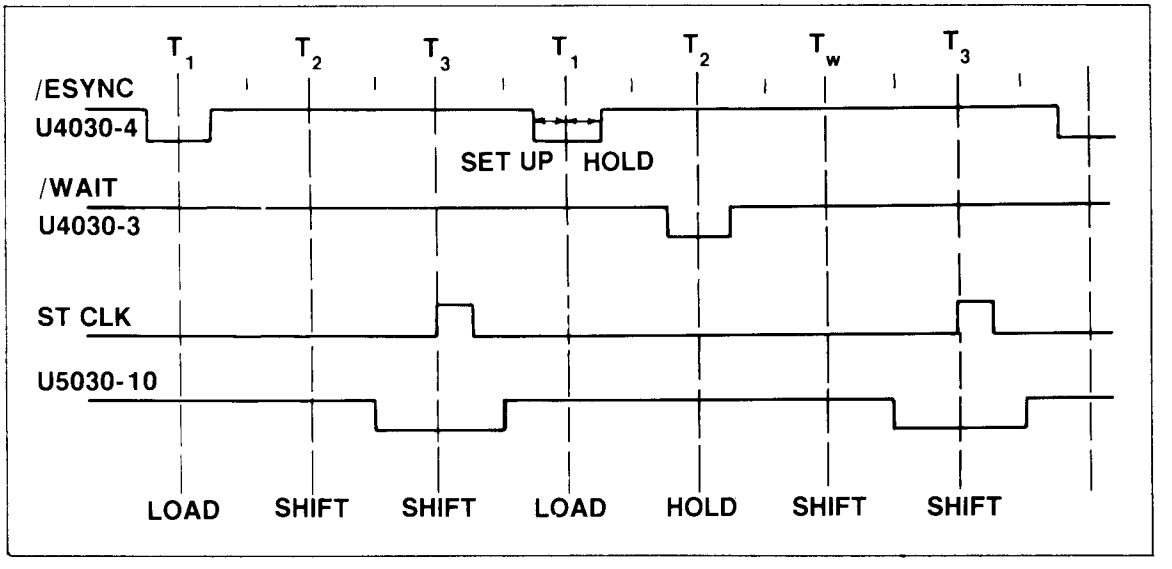


Fig. 2-12A-a. U5030 Delay-by-Two Operation with One Wait State.
(670-5989-00 Boards Only)

In the foregoing operation the circuit will divide in any one of three clock phases; thus, an ESYNC pulse is required to ensure that the proper phase is selected. Referring to Fig. 2-12A. note that an ESYNC pulse occurs just following the first self-loading operation. Thus, two load cycles will occur in a row, then the operation will begin as described above

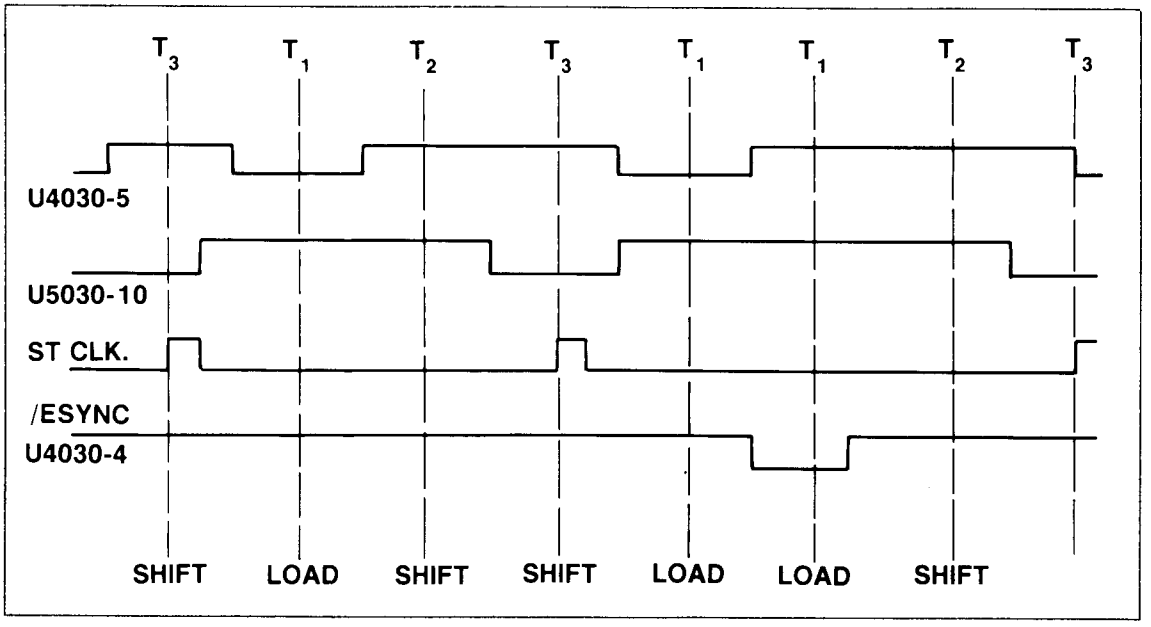


Fig. 2-12A-b. U5030 Divide-by-Three Operation Without Wait State.
(670-5989-00 Boards Only)

The Wait function operates in the same way as just described in the Delay-by-two Operation. Note that the Wait function should not be used during ESYNC time

Clock Qualifier Circuits (670-5989-01 boards only)

This discussion includes a description of the Six-bit Comparators, the Two-bit Wait Comparator, the Two-bit Esync Comparator, and the Clock Delay divider circuit. Refer to Table 2-4B, which lists the raw clock selection codes.

TABLE 2-4B

Raw Clock Selection Codes

	Data Bus Lines								
	D7	D6	D5	D4	D3	D2	D1	DØ	
Address									Upper Control Lines
0:FFØX			-	+					C4
0:FFØX	-	+							C5
0:FFØX					-	+			C6
0:FFØX							-	+	C7
0:FF1X							-	+	C8
0:FF1X					-	+			C9

Placing a 1 at any of the locations selects a clock at the indicated polarity of the signals. For example, a clock at the positive level of C7 at the the probe tip is required. Address 0:FFØX is called, and line DØ is pulled high (Ø1 hex on the data bus). These conditions are set before the store cycle begins. The expression for this function is:

C4*C5*C6*C7*C8*C9 = CLK.

Likewise, the function for removing clocks is:

/C4+/C5+/C6+/C7+/C8+/C9 = no CLK.

Six-bit Comparator. Refer to Diagram 4B. There are two comparators in parallel, one of which generates the QUAL Ø signal, the other of which generates QUAL 1. The first consists of U2030, U2040, and U3020. The second comparator consists of U3030, U3040, and U4020. Each comparator is a set of AND-OR INVERT gates connected in a wire-OR configuration. Control of the Comparators is from the ten-bit buffer, consisting of U4010, U5010, and U6010; data to the Comparators is from the twelve-bit latch (U1040 and U2020).

Assume that the clock is desired only when the C9 bit is high. Referring to Table 2-4B, note that the C9 bit is listed across from address page Ø at FF1X. The CPU stimulates U4050 to send a clock pulse to pin 9 of U2020. At this time, the D3, D2, D1, and DØ inputs to U2020 are a 4 hex; thus D2 is high, which in turn makes the D22 output from U2020 high. This applies a high level to pin 12 of both U3020 and U4020. The remaining pins of U3020 and U4020 are low.

The CI9 bit from the probe enters the board at P104-24D and is applied to pin 4 of U5010 and pin 15 of U6010, both part of the 10-bit Buffer. Through the buffers, the bit is applied to pin 11 of U3020 and pin 11 of U4020 from U5010, and to pin 4 of U3020 and pin 4 of U4020 from U6010. The 4 hex set previously causes U3020 pins 9, 2, and 5 to be low, and a high level at U3020-12 and U4020-12. Thus, the high at pin 12 of the two gates enables the CI9 signal to pass through U3020 and U4020, which makes QUAL 1 and QUAL 0 both high. These two signals are applied to the J inputs of U5050 (pins 3 and 11), the two Pulse Shaper circuits on Diagram 4A. The high at each J input causes the flip-flop to produce a clock output at the next raw clock occurrence. If, for example, the CI9 line is high with every other clock cycle, the two Pulse Shapers will produce a state clock 1 and 2 with every other raw clock cycle.

In conclusion, the Six-bit Comparators are used to qualify the ST CLK 1 and ST CLK 2 signals, so that clocks may be skipped, deleted, or otherwise altered by comparison with the CI4-CI9 bits from the probe.

Clock Delay and Divider. Refer to Table 2-5B, which lists the WAIT and ESYNC generation codes. This discussion is based on an example of a delay-by-two clock generation. Thus, an ESYNC function must be generated each time a delay by two is required. In this example, then, an ESYNC function is to be produced when C6 moves high. In Table 2-5B, the address for C6 is address page Ø at FF3X for a positive ESYNC on C6. As a result latch U1050 must have a hex 80 stored; the CPU applies the required data to U2055, which produces a clocking signal from pin 12, to be applied to pin 11 of U1050, clocking the hex 80 into U1050. This makes pin 6 of U1050 high; the remainder of the output are low. The high at pin 6 is applied to pin 11 of U2050, the Esync Comparator. The CI6 line at pin 23C of P104 is now high; it connects to U5010, pin 17, and through U4010 pin 2 to 18; that line connects to pin 10 of U2030 and U3030, and to pin 12 of U2050. As a result of the high at pin 12 of U2050, the /ESYNC signal at pin 8 goes low, which makes the output of U6020B on Diagram 4A go high.

TABLE 2-5B
/WAIT and /ESYNC Generation Codes

	D7	D6	D5	D4	D3	D2	D1	DØ	
0:FF3X	S+	S-							C6
0:FF3X					W+	W-			C7
0:FF3X			S+	S-					C8
0:FF3X							W+	W-	C9

(This table represents: C6+C8 = /ESYNC, and C7+C9 = /WAIT.)

Now that the ESYNC condition is developed, the WAIT condition must be developed. In the example, a high level on the C9 line produces a WAIT state. Referring once again to Table 2-5B, for a WAIT condition on a C9 high state, an 02 hex is required. However, to avoid destroying what is already loaded into U1050, an 82 hex is loaded into U1050. The CPU clocks U1050 by the usual means (U2055), and the result at the output of U1050 is a high state at pin 15 of U1050, which makes pin 11 of U3050 high. In order to pass this level through the Wait Comparator, pin 12 must also be high. The CI9 signal from P104 pin 24D is fed to pin 4 of U5010 and pin 15 of U6010, through the buffers and to pin 11 of U3020 and pin 2 of U3050 in inverted form, and to pin 4 of U3020 and pin 12 of U3050 uninverted. The high at pins 11 and 12 of U3050 permits the /WAIT signal at output pin 8 to go low; the /WAIT signal is applied to pin 12 of U4040D and pin 9 of U5030 (see Diagram 4A). The low at pin 9 of U5030 holds U5030 from acting at present. (See Table 2-6B, which lists the states of U5030.)

TABLE 2-6B
U5030 Truth Table

SØ Pin 9	S1 Pin 10	Function
0	0	Hold
0	1	Shift Left
1	0	Shift Right
1	1	Load

The /WAIT signal is also applied to pins 4 and 10 of U4040. This circuitry performs a special case of the WAIT function, where wait states are to be produced at the same time as clock outputs, as when a delay by 1 or divide by 2 is selected. In such cases, only ESYNC and WAIT states are available. Referring to Table 2-7B, note that a WAIT state overrides ESYNC. Thus, if both are selected to occur simultaneously, the ESYNC will not function. Thus, when the /WAIT signal goes low, the two sections of U4040 pull the QUAL Ø and QUAL 1 lines low, disabling any clock output until the /WAIT signal returns high, at the end of the wait state.

TABLE 2-7B
Clock Delay and Divider Truth Table

Function	/ESYNC	/WAIT	CLOCK Output
Delay by n	low	high	t_0 + n
	high	low	waiting (adding clock time if output pending)
	low	low	waiting (adding clock time if output pending)
	high	high	no effect (no output if previous delay completed)
Divide by n	high	high	divde by n
	low	high	t_0 + (n-1) synchronized
	high	low	waiting (adding clock time)
	low	low	waiting (adding clock time)

NOTES: 1. /ESYNC does not override a pending output. Thus, when in a divide mode, changing the phase of division can cause false outputs.
2. The ESYNC and WAIT circuits are level-sensitive.
3. The ESYNC and WAIT functions should not be selected if a divide by 1 or delay by Ø is selected.

Example of Delay-by-two Operation. Returning to the Clock Delay and Divide circuit, the next example is a delay-by-two operation. Refer to Table 2-8B, which lists the CPU Control Codes for clock synthesis. In this example, for a delay-by-two and a negative-going clock, a code 5D hex is required. This code is applied to U1020 by way of the data bus inputs. The CPU generates a strobe signal by way of U2055, which is supplied to clock pin 11 of U1020. Beginning at bit Ø, output pin 12 is high, which causes the negative edge to be selected by U6040, as discussed earlier in the description. Bit 1 is not used in this circuit. Bit 2 from pin 16 (the Delay bit) is high, and is applied to U5030, pin 2. Bit 3 from pin 19 is also high; it is applied to pin 3 of U5030. (Pins 3, 4, 5, and 6 of U5030 are the A, B, C, and D parallel inputs to the shift register.)

TABLE 2-8B
CPU Control Codes for Clock Synthesis

at ADDR CF4Ø	D6	D5	D4	D3	D2	D1	DØ	Operation	CLK Polarity
	Ø	1	1	1	1	Ø	Ø	Delay by 1	plus
	Ø	1	1	1	1	Ø	1	Delay by 1	minus
	1	Ø	1	1	1	Ø	Ø	Delay by 2	plus
	1	Ø	1	1	1	Ø	1	Delay by 2	minus
	1	1	Ø	1	1	Ø	Ø	Delay by 3	plus
	1	1	Ø	1	1	Ø	1	Delay by 3	minus
	1	1	1	Ø	1	Ø	Ø	Delay by 4	plus
	1	1	1	Ø	1	Ø	1	Delay by 4	minus
	Ø	Ø	Ø	Ø	Ø	Ø	1	Don't care	
	Ø	1	Ø	Ø	Ø	Ø	Ø	Divide by 2	plus
	Ø	1	Ø	Ø	Ø	Ø	1	Divide by 2	minus
	1	Ø	1	Ø	Ø	Ø	Ø	Divide by 3	plus
	1	Ø	1	Ø	Ø	Ø	1	Divide by 3	minus
	1	1	Ø	1	Ø	Ø	Ø	Divide by 4	plus
	1	1	Ø	1	Ø	Ø	1	Divide by 4	minus

DØ is the clock polarity bit; D2 is the delay bit
(Example: To set up a delay-by-four, plus polarity, 1110100 (74 hex) is written at address CF4Ø.)

The following discussion describes how U5030 is loaded. Note that the /ESYNC pulse was generated in previous discussions. When /ESYNC goes low this causes pin 10 of U5030 to go high Since there is no wait signal at this time, pin 9 of the register is high, and the data from U1020 is loaded into the register Thus, QD pin 12 is now low, QC pin 13 is high, and QB pin 14 is low. The high on pin 12 is inverted through U6020D and E, and applied to the J inputs of U5050 (the two pulse shapers). holding both from producing clock pulses for now. As soon as the /ESYNC pulse returns high U5030 pin 10 goes low. A low on pin 10 and a high on pin 9 of the register makes it shift to the right. At the next raw clock following the end of the ESYNC pulse, the low at QC is shifted over to the QD output making pin 12 go low. The resulting high at the J inputs to U5050 permits the pulse shapers to produce state clock signals at the following raw clock edge. Then, the register shifts again, which causes a high to occur at the QD output. As a result a data strobe output at ST CLK 1 and ST CLK 2 are produced from the ESYNC pulse

Now, another ESYNC pulse is sent to U5030, and it repeats the operation just described. The result of this is that the two ESYNC pulses cause a delay-by-two operation to occur in producing the data strobe signal (called the State Clock).

Divide-by-three Operation. The next example is of dividing by three, using the positive edge of the raw clock signal (see Fig. 2-12B). Referring to Table 2-8B, to divide by three on a positive transition requires that a 5Ø hex be loaded into U1020 from the CPU. When the code is loaded, pin 2 of U5030 is low, and the A, B, C, and D inputs are low, high, low, and high, respectively. This particular code causes U5030 to load, then shift twice; load, then shift twice, etc., in a continuous series of operations. This occurs because a high signal on either input to U4050C causes its output to be low, enabling the other input to U6020B. A shift right is then caused by /ESYNC's going low, which appears as a high on pin 10 of U5030 (since /WAIT was high on pin 9). Now, on the first shift of U5030, the high at QB shifts to QC, so that the output of U5020 is still low, and conditions have not changed at the output of U6020F. On the next shift, both Qb and Qc are low, so the output of U4050C goes high. This reinstates the load operation, and the cycle begins once again.

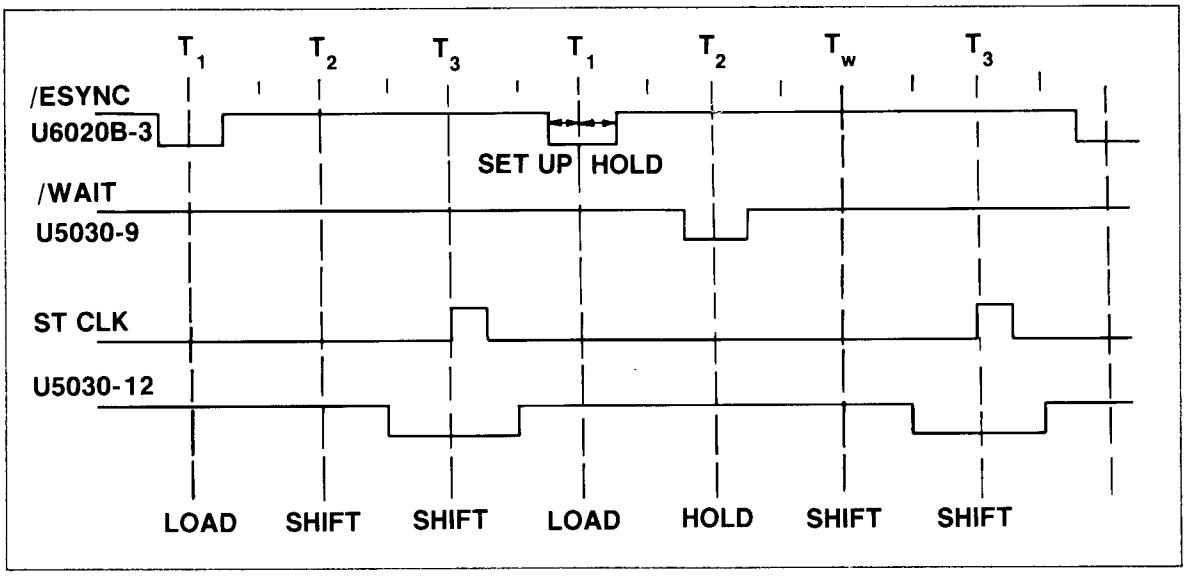


Fig. 2-12B-a. U5030 Delay-by-Two Operation with One Wait State.
(670-5989-01 Boards Only)

In the foregoing operation, the circuit will divide in any one of three clock phases; thus, an ESYNC pulse is required to ensure that the proper phase is selected. Referring to Fig. 2-12B, note that an ESYNC pulse occurs just following the first self-loading operation. Thus, two load cycles will occur in a row, then the operation will begin as described above.

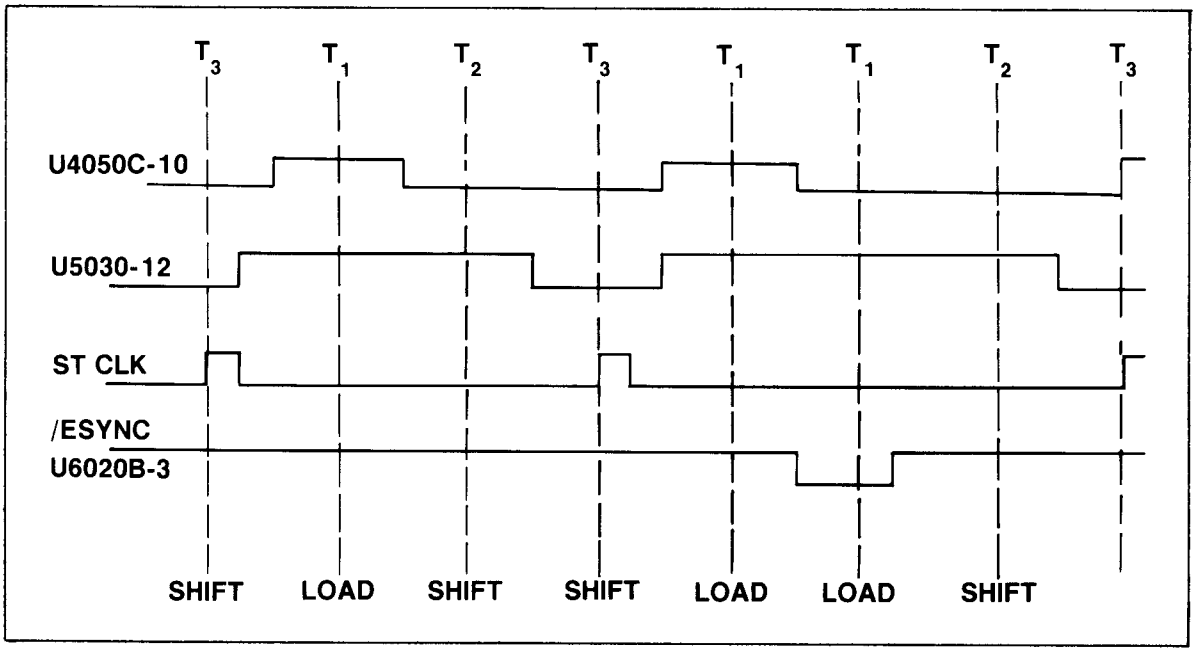


Fig. 2-12B-b. U5030 Divide-by-Three Operation Without Wait State.
(670-5989-01 Boards Only)

The Wait function operates in the same way as just described in the Delay-by-two Operation. Note that the Wait function should not be used during ESYNC time.

Diagnostics (670-5989-00 boards only)

When diagnostics are operating, the CPU is required to produce a ST CLK 1 signal to strobe data through the pipeline system, and to perform a walking code check of the memories in the 7D02 Acquisition Section. It does so by stimulating the preset input on U5050A, pin 4. This is done by first pulling the /WR SEL line at P204, pin 16A, low. Following this, the /RD line is pulled low, which permits the output, pin 11 of U5020D, to move low. This in turn causes the output of U4040A to pull the J and CLR inputs of U6030B low. The output, pin 15, of U6030 goes low, which forces U5050A to set, and the ST CLK 1 line moves high. Owing to the internal

characteristics of the flip-flop (and the delay line coupling the /Q output to the CLR input), U5050A begins to oscillate at an approximate 70-nS period.

Following the completion of the diagnostic routine that requires the State Clock, the hold on U6030B is released, and the next negative edge from pin 15 of U6050 to U6030B pin 14, will clock U6030 back to the set condition, which synchronously allows U5050 to resume normal operation.

Diagnostics (670-5989-01 boards only)

When diagnostics are operating, the CPU is required to produce a ST CLK 1 signal to strobe data through the pipeline system, and to perform a walking code check of the memories in the 7D02 Acquisition Section. It does so by stimulating the preset input on U5050A, pin 4. This is done by first pulling the /WR SEL line at P204, pin 16A, low. Following this, the /RD line is pulled low, which permits the output, pin 11 of U5020D, to move low. This in turn pulls the J and CLR inputs of U6030A low. The output, pin 15, of U6030A goes low, which forces U5050A to set, and the ST CLK 1 line moves high. Owing to the internal characteristics of the flip-flop (and the delay line coupling the /Q output to the CLR input), U5050A begins to oscillate at an approximate 70-nS period.

Following the completion of the diagnostic routine that requires the State Clock, the hold on U6030B is released, and the next negative edge from pin 15 of U6050 to U6030B pin 14, will clock U6030 back to the set condition, which synchronously allows U5050 to resume normal operation.

WORD RECOGNIZER CIRCUITS

Introduction

The Word Recognizer consists of four 32-channel word recognizers; each has 16 address channels, 8 data channels, and 8 control channels. If the Expansion Option is installed in the 7D02, the total address channels are 24 and the total data channels are 16. The 7D02 offers four word recognizer functions in that four different words may be set up at once. These are selected by calling a word recognizer and filling the appropriate fields, which offers the operator the following options: Address equals, Data equals, control Ø through 5 equals, external trigger equals, and timing word recognizer link bit. This is the generalized format for use with the General Purpose Personality Module.

Block Diagram Description

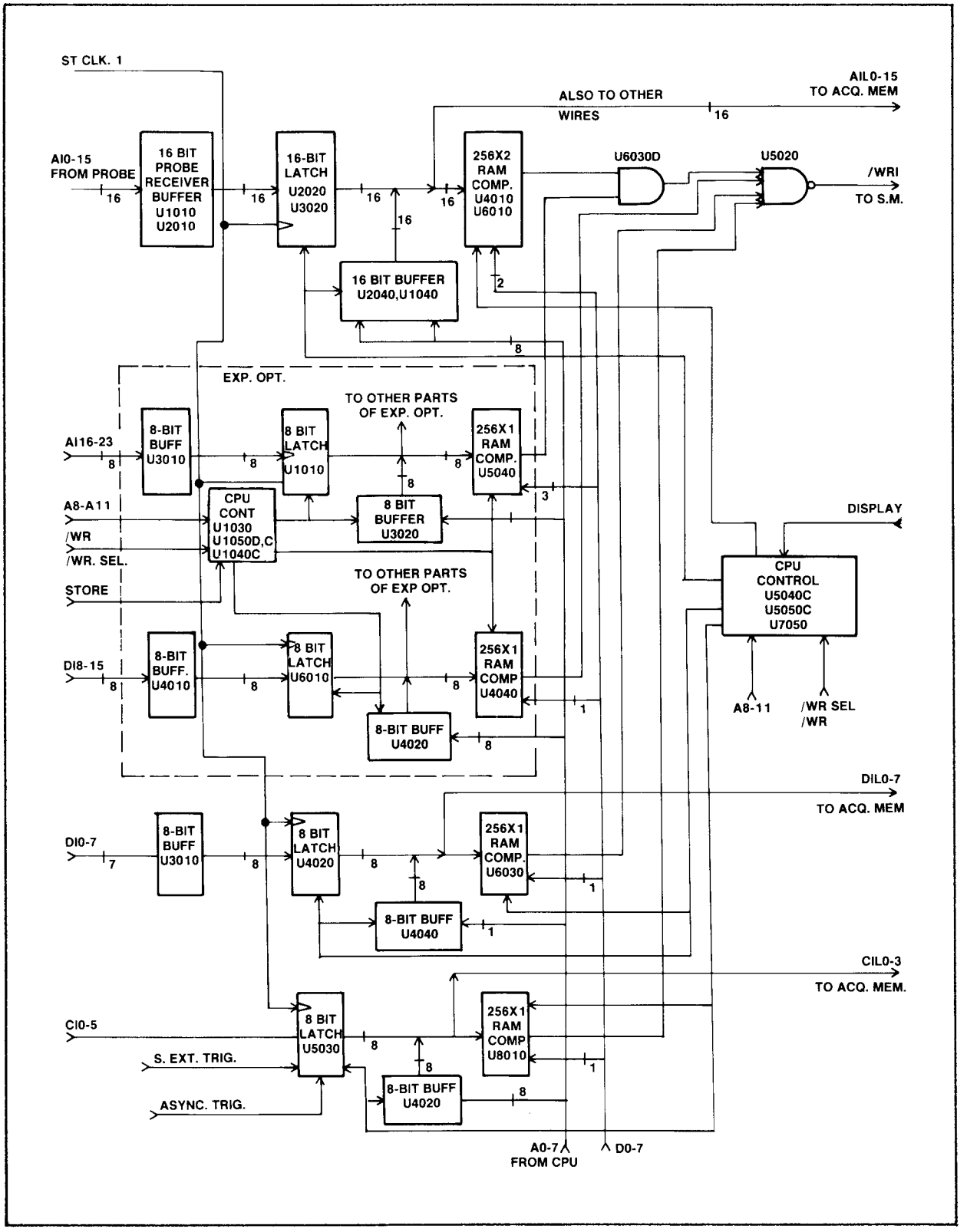
Refer to Fig. 2-13, which is a block diagram of one of the word recognizers. In the following description, only one of the word recognizers is discussed, since all four are essentially alike. Each word recognizer consists of the following major elements:

The Probe Receiver Buffer, which isolates the input to the word recognizer from the raw data probe circuits. This consists of Schmitt Trigger Buffers U1010, U2010, and U3010.

The CPU Buffer, which receives the addresses from the CPU to select a particular location to write data to during the Display mode. These are tri-state buffers U1040, U2040, U3040, and U4040.

The latches, which store the incoming address, data, and control bits for the duration of one STATE CLK 1 cycle. The latches establish the setup and hold time for the main acquisition system.

The RAM Comparator, which compares the data from the CPU, as loaded, with the incoming data from the Personality Module. The RAM consists of U6030, which receives the data byte; U8010, which receives the control signal byte; U6020, which receives the lower address byte; and U4010, which receives the upper address byte. Enabling of the RAMs is controlled by two lines from decoder U5050.



2919-20

Fig. 2-13. Word Recognizer Block Diagram

The Output Gates, which decodes the CPU instructions and loads the masking data into the RAM from the CPU. U5050 is a three-line to eight-line decoder. Only the /Y0 and /Y3 lines are used here. U5050 is addressed by calling page 1:FBXX or page 1·F8XX.

The Expansion Gates, which receive the Word Recognizer outputs from the Expansion Option circuits. These consist of U6050A, B, C, and D.

The Expansion Option circuits, which add sixteen channels to the 7D02 capacity. These circuits consist of Probe Receiver Buffers U3010 and U4010, Latches U1010 and U6010, Tri-state Buffers U3020 and U4020, and RAMs U4040 and U5040. Also, one-half of U1030 performs the CPU controller function.

Detailed Description

In this description, Diagrams 5A and 5B, which depict the Word Recognizer circuits, and Diagram 6, which depicts the Expansion Option portion of the Word Recognizer will be discussed. Note that part of the Expansion Option applies to the Acquisition Memory circuits, and is not discussed here. Refer to Diagram 5A.

Loading the Word Recognizers. In the following discussion, a 0000 hex is to be looked for on the SUT (System Under Test) data bus by word recognizer 1, and word recognizer 3 is to look for the value AAAA hex on the SUT data bus. Thus, both the main word recognizer and the Expansion Option section are used in this example.

Loading the RAM requires that all don't care bits must be loaded with ones. Thus, the address RAMs (U6020, and U4010) must be loaded with ones. To address these RAMs, the CPU calls address page 1·FBXX. This is done by first pulling the /WR SEL line low at the pin 5 input of U5050 (the line corresponds to address page 1:FXXX). This line also connects to U5040, pin 4, on Diagram 5A. The use of this gate is discussed later. The B part of address FBXX is applied to U5050, pins 1, 2, 3, and 6, which are the A8, A9, A10, and A11 signals. Now, the /WR signal must move low for U5050 to load the RAMs. However, the address bits must first be enabled to pass to the RAM inputs, as follows:

The /WR SEL signal at pin 4 of U5040B is low, thus, pins 2 and 13 of U7050 are high. At this time, the DISPLAY signal is high, so the resulting high from U7050A, pin 12, disables latches U2020, U3020, U4020, and U5030.

Also, U5040 pin 8 is low. This pulls low on one enable input of U1040, U2040, U3040, and U4040. Shortly thereafter, the ALE signal from the CPU goes low, so the bits from the CPU pass through U1040. U2040, U3040, and U4040, and are presented to the inputs of the word recognizers. The /WR signal is pulled low, which enables the outputs of U5050. The B part of address FBXX is a binary 1011, so the Y3 output, pin 12, of U5050 is low, and U6020 and U4010 are enabled to load the value on the CPU Data Bus at the selected address. As a result, U6020 and U4010 are loaded with FF (all ones) in all locations.

The upper address-equals system is not to be used in this example, so U5040 (on Diagram 6) also must be loaded with ones. This stage is located at address page 1: F7XX, which is applied to decoder U1030. As before, page 1, F, corresponds to the /WR SEL signal, which is applied to U1050D, pin 11 (Diagram 6). The other input, pin 12, is the A11 signal, now low from the 7H part of the address, so the pin 13 input to U1030 is now high, as a result of the low /WR SEL signal. Also, the A8 line, applied to the pin 14 input of U1030, is high because of the 7H part of the address. Thus, when the /WR signal goes low at pin 15 of U1030, pin 9 goes low to enable U5040. The ones to be loaded into U5040 are applied to the RAM as follows:

The low /WR SEL signal is applied to U1050C. Since the 7D02 is operating in a display mode at this time, the STORE signal is low. Thus, output pin 10 is high, and input latches U1010 and U6010 are disabled. The /WR SEL signal is also applied to pin 10 of U1040; when the ALE signal at pin 9 goes low, U1040 pin 8 goes low to enable U3020 and U4020, the CPU address buffers. Since the STORE signal is low, as previously discussed, the address buffers pass the CPU address to U5040 and U4040. However, only U5040 will load the data, since U4040 is not enabled by U1030. In this way, U5040 is loaded with ones in every cell of the RAM.

Recalling the example, word recognizer 1 is to be loaded with 0000 hex and word recognizer 3 is to be loaded with AAAA hex. Thus, the mask to be loaded into the RAMs will be as follows: location 00 and AA in U6030 will store a one and four hex, respectively; all other locations will store a zero in the lower nibble. The upper nibble of data will store an F hex in U8010.

The address for enabling U6030 and U8010 is page 1:F8XX, so the /WR SEL line is pulled low by the CPU. This disables latches U2020, U3020. U4020, and U5030, and enables the address buffers from the CPU (U1040, U2040, U3040, and U4040). This applies the addresses to the word recognizer

RAMs through U3040 and U4040. Now, the /WR signal goes low to enable U5050 (Diagram 5B), which pulls low on pin 20 of the write enable line of U6030 and U8010. At the first write, which is usually at address 00, an F1 hex is loaded. At all other addresses, except for AA (which is to be loaded with F4), a F0 is to be loaded. 256 load cycles later, the RAMs are loaded.

Returning to the circuits on Diagram 6, part of this example was to load U4040 with a 1 at location 00, and a 4 at location AA. To address the RAM, page 1:F6XX is called; the data comes into U4040 on the D4 through D7 lines, and the write enable line, pin 20, is selected by pin 10 of U1030. Following the load cycle, location 00 will contain a 1 hex and AA will contain a 4 hex; all other locations will contain 0 hex. This completes the loading of the word recognizer for this example. In summary, if the word applied to the data field in word recognizer 1 equals 0000 and at another time the word applied to the data field in word recognizer 3 equals AAAA hex, then a word recognition output should pass to the State Machine circuits from the two word recognizers just loaded.

Word Recognition. Some time after the mask is stored in the two RAMs of the Word Recognizer, the 7D02 transitions into the Store mode of operation. This means that high-speed data is coming through from the probe to the Word Recognizer via P105 (see the left edge of Diagram 5A). The incoming data is applied through data buffers U1010, U2010, and U3010, which provide hysteresis buffering to the input latches, U2020, U3020, U4020, and U5030. (Note that the lines connecting to U5030 are not buffered on this board; buffering occurs on the Front End board.)

At the proper time for each applied word, the ST CLK 1 signal clocks the words into the input latches. The word that is present on the latches outputs is sent through P105 to the Acquisition Memory circuits. The same data is also applied to the Word Recognizers on Diagram 5B. Likewise (see Diagram 6), the ST CLK 1 signal clocks the applied words into the Expansion Option input latches, U1010 and U6010. The words are then applied to the Pipeline latches, then to the Expansion Option Memory RAMs.

Recall that Word Recognizers 2 and 4 are not in use for this example. As a result of the mask that is in U6030, Pin 10 and 14 of this RAM are held low. The low from pin 10 is applied to pin 2 of U6050A; this holds its output pin 3 low, which holds the output of U7040B, /WR4, high. Likewise, the low at pin 14 of U6030 causes pin 6 of U6050 to hold the output of U4030 high (/WR2).

For any other input than 00 or AA hex, pin 16 and 12 of U6030 are low. When a 00 hex is read from U6030, output pin 16 will go high. However, the output of U6050D will not go high unless word recognition has occurred in the Expansion Option word recognizer as well. Referring to Diagram 6 again, U4040 was masked for a 00 hex on the upper data byte. When a 00 is read from U4040, pin 16 goes high, which enables the other side, pin 12 of U6050 (Diagram 5B). The output of U6050D is connected to pin 12 of U5020. The other inputs of U5020 have been set high by the mask, so when pin 12 goes high, the /WR1 signal at pin 8 goes low, and the State Machine is informed that a match has occurred in Word Recognizer 1.

In the same way, when the data applied to U6030 is AA hex, pin 12 goes high. Referring to Diagram 6, when the data at the input of U4040 is AA, pin 12 goes high also. These two events cause the output of U6050C (pin 8) to go high, enabling the output of U7040A, /WR3, to go low. (As in the case of Word Recognizer 1, the other inputs to U7040A were already high, due to the mask loaded in the RAMs.)

ACQUISITION MEMORY

Introduction

The Acquisition Memory circuits perform the following functions:

1. Storage of 44 channels of data for display on the Mainframe CRT.

2. Production of the delay that is required for generating complex triggers and qualifiers.

3. Generation of a halt command to the system under test (SUT).

4. Generation of the signal that controls the system transfer from store to display mode.

5. Positioning of the trigger word relative to the stored data.

Refer to Fig. 2-14, a detailed block diagram of the Acquisition Memory Circuits. Note that the Expansion Option is depicted, and is discussed as an integral part of the circuitry.

The 44 data inputs from the Word Recognizer Circuits are connected to the 28-bit and 16-bit Pipeline Latch Circuits. Words are consecutively clocked into the latches by the ST CLK 1 signal. The same clock edge increments the Address Counter. Following this edge, a word is written into the RAM from the Pipeline Latch. The word is store only if the Address Counter increments, as controlled by the QUAL TRACE signal from the State Machine circuits. Otherwise, the addressed RAM cell is overwritten, and the word is effectively not stored.

The Address Counter and Control Logic section receives the ST CLK 1, QUAL TRACE, and AØ-A9 signals, plus control signals from the CPU Mode Control circuit. The Address Counter and Control Logic circuits address the RAM, control the read and write operations to and from the RAM, and send out the address signals to the Last Address Buffer. The CPU Mode Control receives data from the CPU to direct the activities on the Acquisition Memory Board. This circuit directs the Address Counter and Control Logic circuits in both the main and expanded sections of the 7D02. It also controls the operating mode of the 256-bit Delay Counter.

The RAM is 256 by 44 bits in capacity. It and the input latch constitute the pipeline referred to earlier, in that a word is temporarily stored in the RAM to permit other circuits in the 7D02 time to produce complex signals such as triggers and qualifiers.

The RAM Read Control decodes the address and control lines from the CPU in order to read various buffers and the RAM. The outputs of the circuit include the /DISPLAY COMMAND and /STORE COMMAND signals, the /LAST ADDR +1 signal, the READ ENABLE signal to the RAM circuits and the READ ENABLE signal to the CPU Activity Monitor.

The Display/Store Mode Control circuit, using the signals from the RAM Read Control circuit, the 256-bit Delay Counter, and the ST CLK 1 and STOP TRACE signals, produces the DISPLAY and STORE signals that are used by the 7D02 as the timing indices for high-speed start-stop operations.

The CPU Activitiy Monitor receives status signals from the Halt SUT Generator circuit, the Display/Store Mode Control, the State Machine, the Main Section Trigger, the Main Memory, and the Main Section Start-up circuits. The monitor buffers these signals and informs the CPU of signal status.

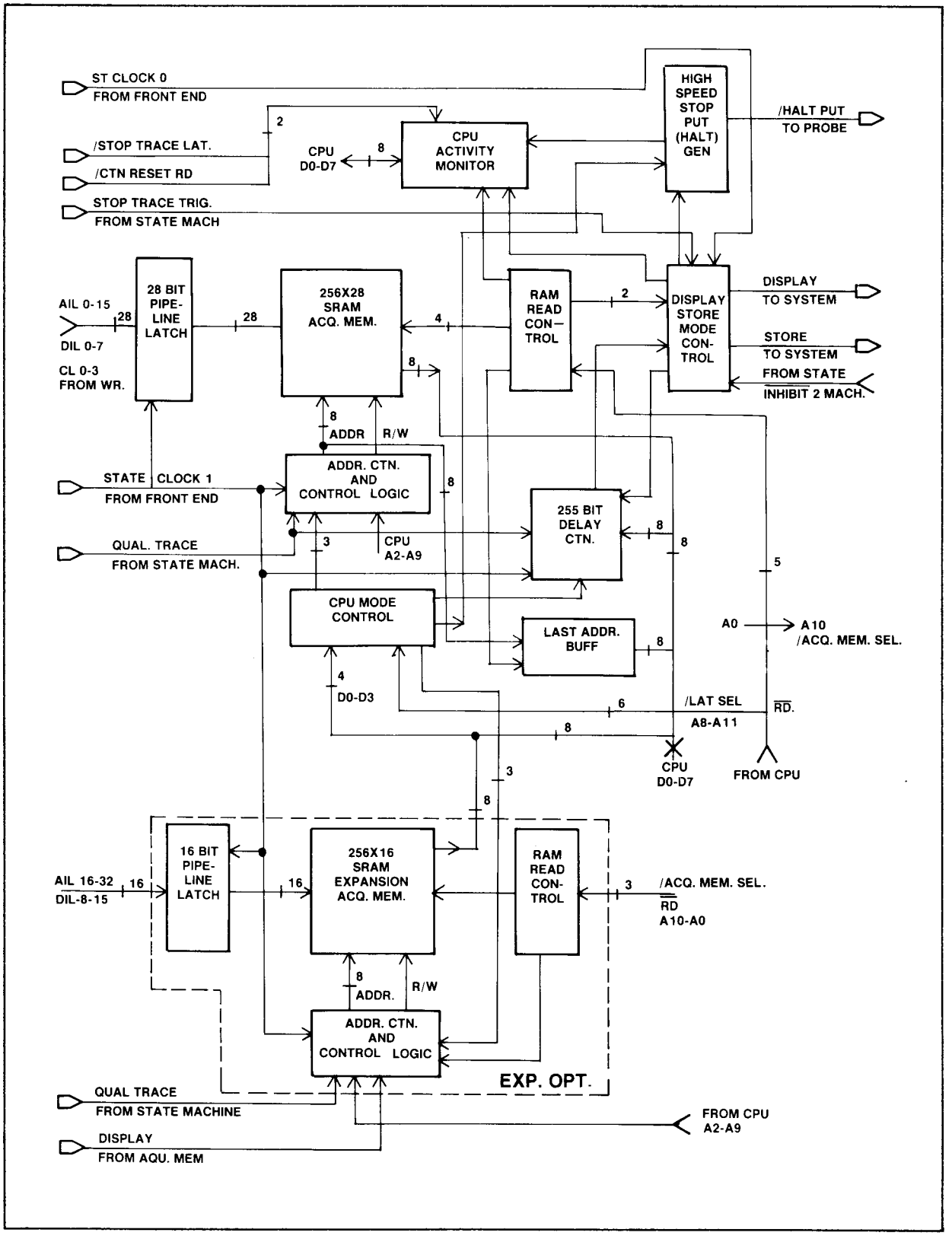


Fig. 2-14. Acquisition Memory Block Diagram

The 256-bit Delay Counter permits the operator to position the display in relation to the trigger point. The counter is controlled by the CPU Mode Control, which controls the loading of the amount of delay. The QUAL TRACE signal enables the counter operation.

The Last Address Buffer, when interrogated by the CPU, places the current address from the Memory Address Counter (MAC) onto the Data Bus lines.

Detailed Description

Refer to Diagrams 7A and 7B, which depict the circuits located on the Acquisition Memory Board. Also, refer to Diagram 6, which depicts the Expansion Option.

The following description is split into two parts. The first part discussed major circuit areas in detail; the second provides examples of operation in various modes.

CPU Mode Control

This circuit consists of U5040C and D, U1030B, U1025B and D, U1010B and Mode Control Latch U2020. It is driven by address lines A8 through A11, the /WR line, the /LATCHES SEL line, and the DØ through D3 data bus lines. The CPU addresses the Mode Control to set the operating modes of the Acquisition Memory circuits. Refer to Table 2-9, which is the truth table for the DØ through D3 inputs. These inputs set the mode of operation. The latch is enabled by holding the A8 address line high at pin 12B of P207. The clock to U2020 is permitted to pass if A10 is high, A9 is low, A11 is low, and /LATCHES SEL is low. The positive edge necessary to clock the data into the latch is furnished by the /WR signal. The address set by the CPU to enable and clock U2020 is page 0:F5XX, which includes the lines just discussed.

TABLE 2-9
Mode Control Latch Truth Table

Data Bits D3	D2	D1	DØ	Display Mode	Store Mode
0	0	0	0	No action	Storing data; no halt; delay
0	0	0	1	Reading data	not permitted
0	0	1	0	Reading pipeline	not permitted
0	0	1	1	not permitted	not permitted
0	1	0	0	Halted SUT	Storing data; halt on stop; storing; delay
0	1	0	1	Read data; Halted SUT	not permitted
0	1	1	0	Read pipeline data; Halted SUT	not permitted
0	1	1	1	not permitted	not permitted
1	0	0	0	Loading delay counter	Ø delay; storing data; no halt
1	0	0	1	Loading delay counter or reading data	not permitted
1	0	1	0	not permitted	not permitted
1	0	1	1	not permitted	not permitted
1	1	0	0	Loading delay counter and Halted SUT	Ø delay; halt on store stop; storing data
1	1	0	1	Reading data or loading delay counter; halted SUT	not permitted
1	1	1	0	not permitted	not permitted
1	1	1	1	not permitted	not permitted

The CPU Mode Control also controls loading of the Delay Counter (U1040 and U2040). This is accomplished by setting a high on the D3 line. addressing page 0:F5XX to clock the high into U2020, then addressing page 0:F4XX. This permits the /WR signal, which moves low soon thereafter, to pass through U5040C, U1030A, U1025B, U1010B, and U1020C to clock the Delay Counter. (The transition passes through U1020C because ST CLK 1 is low during the loading period.)

To summarize, the CPU Mode Control performs the following (as listed by the output pin number of U2020):

Pin 2 controls U5040B, part of the flip-flop that enables reading of the memory in Display mode.

Pin 3 generates the /MEM EN signal, which enables loading the MAC (Memory Address Counter) on the Acquisition Memory and Expansion Option boards. Addresses are loaded from the CPU Address Bus during Display Mode.

Pin 7 generates the RDPL (read pipeline) signal that controls one side of U1010D, which in turn controls the ST CLK 1 signal to be applied to the RAM read/write inputs during diagnostics.

Pin 6 is the /RDPL signal to the Expansion Option board; it serves a similar purpose to the RDPL signal.

Pin 11 is the /HALT ENABLE signal that initiates the Halt SUT (System Under Test) action; the signal also connects to the CPU Activity Monitor (U2030) to inform the CPU of circuit status.

Pin 15 enables U1030C, the Stop Trace Trigger input gate. The line is high when no delay is selected.

Pin 14 is the delay stop line. When the line is high, the Delay Counter is enabled (through U1030A) to end the Store cycle after the correct delay. Also, a high level on the line enable passage of ST CLK 1 pulses to the Delay Counter through U1020C. When low, the line enables loading of the Delay Counter. The delay value is loaded from the CPU Data Bus during Display Mode. The delay value is the complement of the absolute delay, plus one.

RAM Read Control

This circuit consists of three-line to eight-line decoder U2010, U5040A, U1010A and U5040B (connected as a flip-flop), U1010C, and U1025A. Central to the circuit is decoder U2010. CPU signals addressing the decoder are the AØ, A1, A1Ø, and A11 lines. The decoder is enabled through pin 6, which is driven by U5040A. The decoder outputs, YØ through Y7, are listed below:

YØ drives the tri-state enable input to RAM U3020 and U4030. When low, the signal causes the data in the RAM at the address specified by the MAC to be sent out on the data bus lines.

Y1 drives the second pair of RAMs, U5020 and U5030. As above, the action is the same as for YØ.

Y2 drives the third pair of RAMs, U6020 and U6030, as above.

Y3 drives the last RAM, U7020. As described above, when pin 18 of U7020 (tri-state input) is pulled low, the word at the addressed location is applied to the DØ through D3 Data Bus lines.

Y4 is the /DISPLAY COMMAND signal, which is the trigger from the CPU (through U2010) to shift the Acquisition Memory circuits to the Display mode. The signal is used to set the Display/Store flip-flop and is sent off the board to be used in the Timing Option circuits.

Y5 is the /STORE COMMAND signal, which is the trigger from the CPU (through U2010) which shifts the Acquisition Memory circuits to the Store Mode. The signal sets CPU Activity Monitor flip-flop U6040A when the Store operation begins, clocks Display/Store Mode Control flip-flop U7040B at the start of a Store operation, and is also sent to the Timing Option circuits.

Y6 is the LAST ADDR +1 line; it is used by the CPU to enable U3030, the Last Address +1 Buffer, to determine the address in the MAC at the transition to Display Mode.

Y7 is the enable line for U2030, which forms part of the CPU Activity Monitor. U2030 is the Status Monitor, which when enabled furnishes status information from the Acquisition Memory circuits to the CPU.

The /RD and /ACQ MEM SEL (address 2:EXXX) signals are applied to U5040A, another part of the RAM Read Control. When the two signals are low, U2010 is enabled and, in Display mode, flip-flop U1010A-U5040B is reset. U1010C and U1025A form the gating circuit that controls the MAC during the Display mode, on both the main Acquisition Memory and on the Expansion Option board. The ST CLK 1 signal is permitted to pass when the STORE signal is high from U6040B. This high also holds both U1010C, pin 8, and U1025A, pin 2 high. This in turn pulls pin 12 of U1020D (Diagram 7A) and pin 1 of U1040A (Expansion Option, diagram 6) low. This passes the ST CLK 1 signal to the MAC after the Display to Store transition.

During a Read operation, U2020 sets pin 6 of U5040B high. This forces pin 2 of U1010A low, which permits U5040A to control U1010A. The CPU has set address page 2:EXXX (/ACQ MEM SEL), so U5040A pin 2 is low. thus, when /RD goes low at pin 3 of U5040A, the transition is passed through U5040A and U1010A to U1010C, pin 9, and U1025A, pin 3. The STORE signal is low

to the other inputs of these gates (since the 7D02 is in Display mode), so the transition can pass through to clock the MAC. Pin 13 of U1020D is enabled by the low ST CLK 1 signal.

CPU Activity Monitor

This circuit consists of U7010D, flip-flop U6040A, and buffer U2030. Periodically, the CPU addresses page 2:E803, which causes decoder U2010 to enable placing the data at the buffer inputs on the Data Bus, lines DØ through D7. This buffered information is described in the following paragraphs. Note that part of the buffer provides the CPU with access to the State Machine status lines. The descriptions are organized by U2030 input pin number.

Pin 12 is the COUNTER RESET READ signal from the State Machine.

Pin 14 is the /HALT ENABLE signal from the pin 11 output of U2020. See the CPU Mode Control description for more information.

Pin 16 is the DISPLAY signal from U6040B. This signal is high when a Display operation is occurring.

Pin 18 is the output of U7010C, which is the pending stop acquisition signal.

Pin 2 is the /STOP TRACE LATCHED signal from the State Machine.

Pin 4 is from U6040A and indicates that the MAC has cycled at least once. (U6040A is discussed later.)

Pin 6 is the /INHIBIT 2 signal from the State Machine.

Pin 8 is the STORE signal from U6040B. It is high when a Store operation is occurring.

Some of the above-noted lines come from the State Machine. Refer to the State Machine description for more information.

Another part of the CPU Activity Monitor consists of U7010D and U6040A. At the start of a Store operation, the /STORE COMMAND signal is pulled low momentarily by U2010, which sets U6040A. The /Q output of the flip-flop connects to U2030, and indicates the status of the MAC. The Q output of the flip-flop is coupled back to its own J input, pin 2, so U6040A can

change state only once more, then it locks up. At the start of the Store operation, the /INHIBIT 2 signal is low. Thus, the output of U7010D is high and U6040A cannot switch back to the reset state. Following the positive excursion of /INHIBIT 2, the pin 12 input of U7010D is controlled by the overflow output of U4040, one stage of the MAC. This line stays low, disabling U6040A, until the MAC counts up to FF. Then the line goes high, allowing flip-flop U6040A to switch, and be reset by the next ST CLK 1 signal. As a result, U6040A pin 6 pulls its own pin 2 input low, so subsequent clock pulses have no effect. Thus, U6040A indicates to the CPU when the MAC has counted to FF, by locking up after that event occurs; i.e., when the memory is filled to capacity.

Display/Store Mode Control

This circuit consists of U1030A, U1030C, U7010C, U6040B, and U7040B, and sets the operating mode for the Acquisition Memory circuit. At the start of a Display operation, the high DISPLAY signal from U6040B, pin 10, is sent to pin 1 of U7010A to set the /HALT SUT line low, to U2030 to indicate status to the CPU, and to U7040B (to release control of the flip-flop). Sometime later, when the CPU calls for a Store operation, the /STORE COMMAND signal will go low, then high, and clock U7040B to the set state. The low from pin 9 of U7040B enables flip-flop U6040B to reset on the next excursion of the ST CLK Ø signal. When this occurs, the STORE signal moves high. At the same time, the low DISPLAY signal resets U7040B. From then on, U6040B will not change state again until a high state is provided by U7010C. This occurs when the STOP TRACE TRIGGER signal from the State Machine goes high (zero-delay path), or when the Delay Counter overflows. When either of these conditions produces the high state to pin 14 of U6040B, the next ST CLK Ø excursion sets U6040B, and the DISPLAY signal once again moves high. Flip-flop U7040B remains in the reset condition until the /STORE COMMAND signal once again clocks it to the set state.

As mentioned earlier, U1030C is one path for ending a store operation, and is used when no delay is programmed. Pin 10 of U1030C is held high by U2020 to enable this path. The /INHIBIT 2 signal is low for he first two ST CLK 1 pulses to keep the gate from terminating the operation too soon; the signal moves high after the second pulse, and the gate is then under control of the STOP TRACE TRIGGER signal from the State Machine. Later, this signal moves high, causing the J input of U6040B to move high and terminate the Store operation.

The other stop path is through U1030A. At the start of the Store operation, U7040A is reset by the /INHIBIT 2 signal. The low state from

U7040A prevents U1040 and U2040 from incrementing until the STOP TRACE TRIGGER signal at pin 2 moves high. Following the positive edge of the ST CLK 1 signal applied to pin 4 of U7040A, the flip-flop changes state, and the pin 10 input to U1040 is enabled. The pin 13 input of U1030A has already been enabled by the CPU. As each valid stored word occurs, the QUAL TRACE signal is also high. Thus, the Delay Counter increments until the overflow bit (pin 2 of U1030A) goes high. The resulting high at pin 14 of U6040B causes the Display/Store flip-flop to set at the next ST CLK Ø positive excursion.

Halt SUT Generator

This circuit consists of U1025C, U1020A, and the flip-flop that consists of U7010A and U7010B. The circuit is used to stop the system under test (SUT) when the 7D02 Main Section stops (when it changes from Store mode to Display mode).

Assume that no Halt SUT is selected and that the DISPLAY signal is low, indicating that the 7D02 is in the Store mode. The low at U7010 pin 1 ensures that the /HALT SUT line is high for the time that the DISPLAY line is low. The /HALT ENABLE line from U2020 pin 11 is high also, since Halt SUT is not selected, so that high holds pin 4 of U7010 high, which in turn holds pin 2 of U7010 low. Thus, when DISPLAY moves high at the end of the Display period, pin 2 holds the /HALT SUT signal high.

If Halt SUT is selected, the /HALT ENABLE line is pulled low, which permits U1025C to control U1020A. When STORE goes high and DISPLAY low, U7010 pin 4 goes low, and U7010 pin 2 goes high. The high on pin 2 enables the DISPLAY signal to control the state of /HALT SUT; that is, when DISPLAY is high, /HALT SUT is low, and vice versa.

Should Halt SUT be terminated, the /HALT ENABLE line returns high, which blocks the STORE signal from having further control through U1025D. The next time that /HALT SUT is moved high by the low-going DISPLAY signal, pins 4 and 5 of U7010 will both be high, forcing pin 6 low, and locking the /HALT SUT line high.

Memory Address Counter

The Memory Address Counter (MAC) consists of eight-bit binary counter U3040 and U4040 (on the Acquisiton Memory board) and U3050 and U4050 (on the Expansion Option board). Each of these counters can be preset to any number from Ø to 255, and operates in two ways: In Store operations, the counters sequentially address the RAM on each active edge of ST CLK 1. In Display operations, the counters are loaded from the CPU Address bus with a RAM address containing data needed by the CPU.

At the start of the storage operation, the CPU does a false read at address 2:E3EC, which sets the initial address for the MAC to F (hex). This loading is enabled by the /MEM EN signal from U2020. After the STORE command is sent, U1020D is enabled to pass ST CLK 1 pulses to the clock input of U3040 and U4040. Likewise, MAC U3050 and U4050 on Diagram 6 are loaded, enabled, and clocked in the same fashion as that on Diagram 7. As clock pulses are applied to the MAC, the QUAL TRACE signal is asserted with each valid word that is presented to the memory. Thus, the counter advances only when the QUAL TRACE signal is high, indicating qualified data. Otherwise, as each succeeding word enters the memory, it writes over the previously stored word until a qualified word appears and the countr is incremented.

RAM control is exercised by the MAØ through MA7 lines from the MAC. When the CPU reads the data out of the RAMs, it first interrogates the Last Address Buffer. This buffer places the last address that was sent from the MAC to the RAMs on the Data Bus. When the CPU selects a particular address to be read, it first sends that address to the MAC. Then, when the /RD signal from the CPU goes low, the address is clocked into the MAC and the contents of the address are applied to the Data Bus.

Delay Counter

This circuit consists of eight-bit binary counters U1040, U2040, and U7040A on Diagram 7A, and is used to change the position of data on the CRT. As discussed earlier, two paths exist for the STOP TRACE TRIGGER to stop the system. After the /INHIBIT 2 signal resets U7040A, the Delay Counter remains disabled until the STOP TRACE TRIGGER signal goes high. The high causes pin 6 of U7040A to go high at the next ST CLK 1. The high from U7040A enables the Delay Counter to begin counting.

The CPU loads the Delay Counter with a preset number via the DØ-D7 Data Bus lines before the storage cycle begins. It is loaded by the same line from U2020 that enables U1030A pin 13. When the counter reaches overflow, U2040 pin 15 moves high, and U1030A pin 12 moves low, which causes the 7D02 to shift back to the Display mode. Thus, the STOP TRACE TRIGGER signal is delayed in stopping acquisition by the delay set in the counter by the CPU.

Last Address Buffer

This circuit consists of only U3030, and is used to inform the CPU of the point at which the MAC stopped, and thus the location that was last stored. When the CPU requires this information, it sets the LAST ADDR +1 line from U2010 low (by doing a read at 2:E8Ø2), which enables the buffer to place the data from the MAC on the Data Bus.

Pipeline Register

This circuit consists of latches U3010, U4010, U5010, and U6010 on Diagram 7B, and U2020 and U5020 on Diagram 6. The address, data, and control bits from the Word Recognizer are applied to the inputs of the Pipeline Register, which temporarily stores these bits for later storage by the RAM. Register clocking is provided by the ST CLK 1 signal, gated by U1020D. Each ST CLK 1 pulse advances the next word from the Word Recognizer to the Register, where it is held for one ST CLK 1 cycle before being loaded into the RAM.

The Expansion Option section of the Pipeline Register (U2020 and U5020) operates in the same way as described above. the MACTNCK signal from the Acquisition Memory circuit, which controls U1040A (Diagram 6), enables the ST CLK 1 signal to latch the register. (MACTNCK clocks the register in the Display mode, since ST CLK 1 is low then.) Total capacity of the Pipeline Register, including the Expansion Option, is 44 bits.

RAM

The Random Access Memory (RAM) is the principal storage medium for the Acquisition Memory. It consists of seven integrated circuits: U3020, U4030, U5020, U5030, U6020, U6030, and U7020. Lines to each of the RAMs are the four input lines (pins 9, 11, 13, and 15), the four output lines (pins 10, 12, 14, and 16), the eight address lines (MAØ through MA7), the tri-state enable line (pin 18), and the read/write enable (pin 20).

As a word is applied to the RAM from the Pipeline Register, the MAC advances the RAM address each time a valid word is loaded. If the word just loaded is not qualified, the address is not incremented and it is written over by the next word that occurs. When a valid word occurs, the MAC advances the RAM one address, and that word is stored in the next address, rather than being over-written in the last address at the next clock pulse.

Expansion Option

As mentioned previously, the Expansion Option is an extension of the Acquisition Memory Board, although a significant portion of the board is an extension of the Word Recognizer circuits. The circuits that apply to the Acquisition Memory that have not yet been described are the RAM and the RAM Read Control. Refer to Diagram 6. The RAMs are U3030, U3040, U2030, and U2040. As in the previous description, the RAMs are controlled in pairs by the RAM Read Control, which is the upper half of U1030 and U1040 A, B, D.

The /RDPL signal enters the board through U1050D, is inverted, and then applied to pin 5 of U1050 to lock the pin 5 input of U1040 low. This permits the ST CLK 1 signal to cycle the RAM for diagnostic purposes, as in the main board.

Store Mode

The Acquisition Memory has two modes of operation, Display and Store. In the Store Mode, the first step is to set the Memory Address Counter (MAC) to its starting point (FD (hex)). Then the CPU generates the STORE command. A false read signal at location page 2:E8Ø1 is received from the CPU. The /ACQ MEM SEL line from the CPU is the 2:E part of the address.

This line is pulled low, which enables pin 2 of U5040A. A short time later, the CPU pulls the /RD line low, which in turn causes U5040A pin 1 to pull pin 3 of U1010A and pin 6 of U2010 high. The high at pin 6 of U2010 enables this decoder. Pin 5 (A1Ø) is low and pin 3 (A11) is high; lines A1Ø and A11 are the 8 part of the 2E:8 address. To enable the Y5 output of U2010, the AØ line is high and the A1 line is low (U2010, pins 1 and 2, respectively). These cause Y5 (/STORE COMMAND) to move low. Refer to Fig. 2-15, which illustrates the timing relationships of the signals involved in the Display-to-Store transition.

The low /STORE COMMAND signal resets U6040A, which is part of the CPU Activity Montior. The /Q output of this flip-flop is connected to buffer U2030 to inform the CPU of the MAC cycle status when interrogated. The /STORE COMMAND signal is also connected to the clock input of U7040B, so the positive edge of the /STORE COMMAND signal sets U7040B. (The positive edge occurs when the /RD signal returns high, ending the access period of the CPU.)

Before the sequence begins, the Master Store/Display flip-flop (U6040B) is in Display Mode with pin 9 of U6040B low. The low applied to pin 13 enables U6040B to change states at the next ST CLK Ø positive edge. When this occurs, the high applied from U6040B pin 9 forces U1010D pin 13 low, which in turn permits the ST CLK 1 signal to pass through U1020B. The clock pulses are applied to the read/write inputs of the RAMs (pin 20 of U3020, U4030, U5020, U5030, U6020, U6020 and U7020).

The high STORE signal from pin 9 of U6040B is also applied to U1010C, pin 8, and U1025A, pin 2. This forces U1010C pin 10 low, which allows passage of the ST CLK 1 signal via pin 13 of U1020D to pin 11, to increment the Memory Address Counter, U3040 and U4040. The ST CLK 1 signal from U1020D is also fed to U6040A, and as a latching signal to the Pipeline Latches (U3010, U4010, U5010, and U6010).

The high at U1025A pin 2 forces its output, pin 1, low. This low (MACTNCK) is applied to pin 1 of U1040A (see Expansion Option, Diagram 6) to enable passage of the ST CLK 1 signal to the Pipeline Register (U2020 and U5020), and to the clock inputs of MAC counters U3050 and U4050.

Still referring to Daigram 6, the STORE singal from P206 pin 20B is applied to U1050B, pin 6. The high on pin 6 forces U1040B pin 5 low, permitting the ST CLK 1 signal to pass through to the read/write inputs of RAMs U3030, U3040, U2030, and U2040.

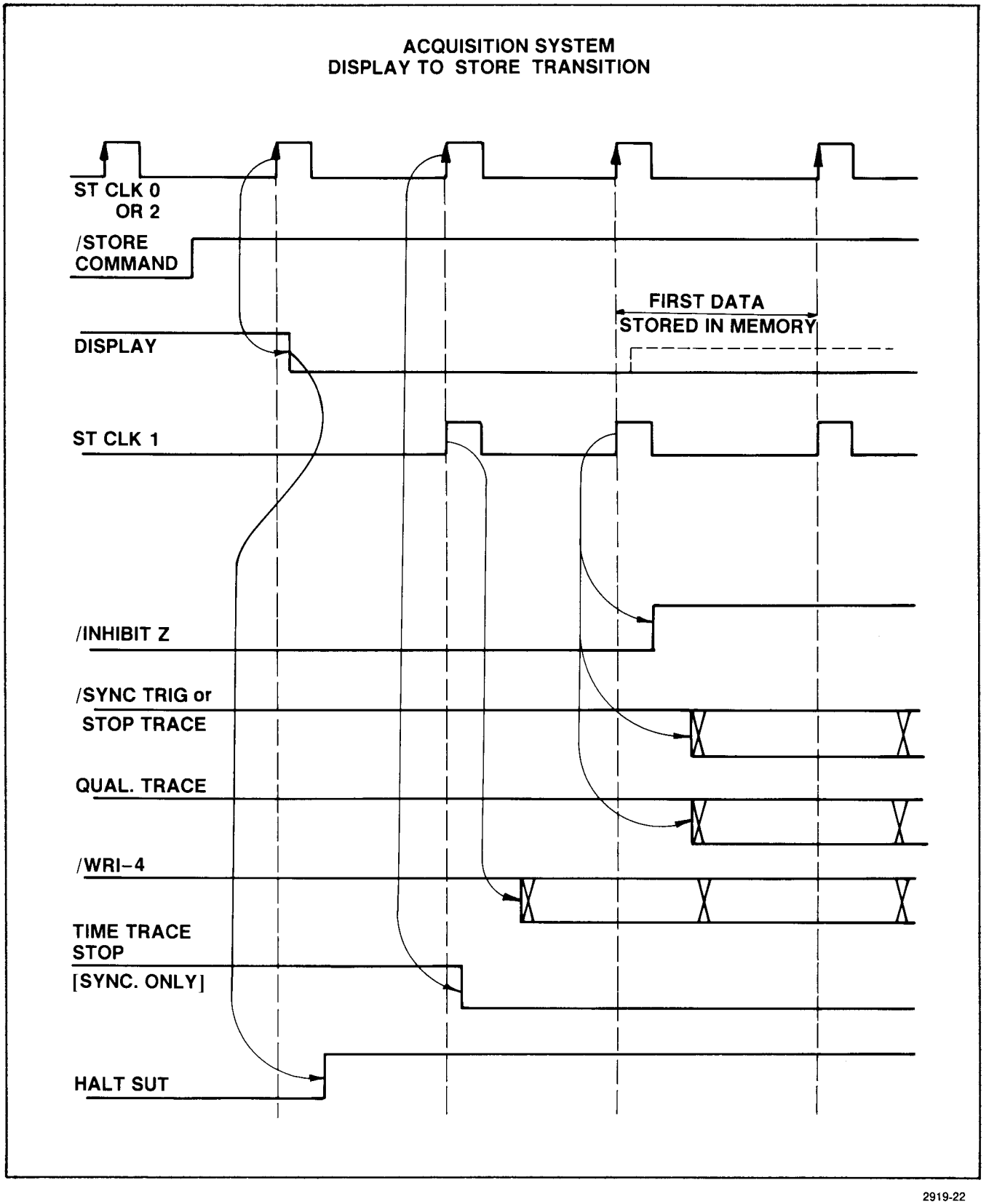


Fig. 2-15. Display to Store Transitions

At this point, the system is in the Store mode. As an example, assume that a program is to be run that includes zero delay, and that the system under test continues to run. This means that the Delay Counter is not used in this example. To begin the sequence of events, the high state from U5040A pin 1 resets the flip-flop that consists of U1010A and U5040B. The resulting low from pin 1 of U1010A is applied to pin 9 of U1010C and pin 3 of U1025A. Since the ST CLK 1 signal is low at this time, the positive edge from U1010A is passed through U1020D to increment U3040 and U4040 (the MAC). (Pin 8 of U1010C is already low; see earlier discussion.)

The same clocking signal is also applied to the Pipeline Register, consisting of U3010, U4010, U5010, and U6010, and to the Pipeline Register on the Expansion Option board (Diagram 6, U2020 and U5020). The clock also increments the MAC (U3040 and U4040 on Diagram 7B, U3050 and U4050 on Diagram 6).

After the first ST CLK 1 signal the word in the Pipeline Register is invalid, since the Register contains the previous output of the Word Recognizer latches. However, the word in the Word Recognizer latches is now valid, having been strobed by the first ST CLK 1 signal of this sequence. The following ST CLK 1 pulse (the second pulse after STORE went high) then stores a valid word in the Pipeline Register; this word is then applied to the RAMs. (The word is applied to pins 9, 11, 13, and 15 of each RAM.)

During the first two clocks applied to the Acquisition Memory circuits, the /INHIBIT 2 signal from the State Machine is low. This resets U7040A and disables U1030C until /INHIBIT 2 moves high. Then, the STOP TRACE TRIGGER signal can set U7040A, and be passed through U1030C.

Recall that on the second ST CLK 1 signal, the MAC was incremented to ØØ. Following the positive edge of ST CLK 1, a valid word is presented to the memory. The address for the RAMs is stable and applied to the MAØ-MA7 inputs. The ST CLK 1 signal is still high, lasting for about 40 nS, and is applied to U1020B pin 4. The resulting high at pin 6 of U1020B holds the pin 20 input of each RAM high. When the ST CLK 1 signal falls, the low at pin 20 causes each RAM to write, or store the applied bits. (The write cycle lasts for the low period of ST CLK 1, which is about 60 nS when running at 10 MHz.) When the ST CLK 1 signal returns high, loading stops, the MAC is incremented, and a new word is loaded into the Pipeline Register. This continues in sequence, storing a set of data into each RAM cell with each successive state clock pulse, as qualified by later discussion.

As each word enters the pipeline, it is qualified or rejected by the QUAL TRACE signal from the State Machine. This signal is high to indicate that the word in question is "qualified" or valid for storage.

The QUAL TRACE signal comes in at P207-17A, and is applied to pin 7 of U3040, U4040, U2040, and U1040, and to pin 1 of U1030A. A qualified word causes the QUAL TRACE signal to be high, so the MAC is incremented with each ST CLK 1 pulse. If the word is not qualified, the QUAL TRACE line goes low. With no qualified word, the conditions are as follows: The MAC has been incremented to Ø1 on the last cycle, and a new word is in the Pipeline Register. Since QUAL TRACE is low, the MAC does not increment on the next ST CLK 1 signal. As a result, the new word is written over the word already stored in the last cycle. This occurs any time that the QUAL TRACE signal is low and a Store cycle occurs.

The storage cycles just described are repeated as long as the ST CLK 1 signals continue and trigger conditions are not satisfied. If enough clocks occur, the MAC overflows, having counted past FF. The overflow signal from pin 15 of U4040 goes high, which also causes pin 12 of U7010D to go high. The /INHIBIT 2 signal has since gone high, following the second state clock. The output of U7010D is connected to pin 3 of U6040A, so the low applied to this pin permits the flip-flop to be reset by the next positive edge of the ST CLK 1 signal. Once U6040A is reset, it will not change state until it is again set by a low /STORE COMMAND signal, which occurs at the beginning of the next store sequence. The pin 7 output of U6040A is fed to pin 4 of U2030, which is interrogated by the CPU to determine the state of that line. (U2030 is read by addressing 2:E8Ø3.)

Some time later, the State Machine sends a STOP TRACE TRIGGER signal to the Acquisition Memory circuits. The signal is sent to pin 2 of U7040A and pin 9 of U1030C. Although U7040A changes states, it does not affect the Delay Counter. This is because the counter is held in the load mode by the low level from U2020, pin 14. The high at U1030C pin 9 (enabled by the high levels at pins 10 and 11 of U1030C) pulls output pin 8 low. This enables U6040B to set on the next ST CLK, causing the DISPLAY signal to go high and the STORE line to go low. Note that when U6040B went to the Store mode, the low DISPLAY signal placed U7040B in the reset state. This in turn placed a high level at pin 13 of U6040B, which, with the high now applied to U6040B pin 14, permitted U6040B to be clocked to the Display Mode.

When the STORE signal goes low, U1010C pin 8 and U1025A pin 2 go low. The low levels applied to U1010C pin 8 and 9 causes U1020D to block ST CLK 1 pulses from passing to the MAC. Under control of U1025A pin 1, U1040A (Diagram 6) blocks ST CLK 1 pulses from passing to the MAC and Pipeline Register on the Expansion Option board. The low STORE signal also holds U1010D pin 11 (Diagram 7A) low. U1010D pin 12 is also low, so the resulting high at pin 5 of U1020B blocks any clock signal from entering the read/write inputs to the RAMs.

Display Mode

As mentioned earlier, U2030 is interrogated, as required, to update the CPU on whether a store or display operation is occurring. It does so by interrogating the D7 bit from U2030. When a low is detected at the D7 bit, the acquisition unit has completed storing, and the CPU can read the data from the RAM. See Fig. 2-16, which illustrates the signals involved in the Store-to-Display transition.

Next, the CPU reads the Full Status Monitor to determine if the MAC has filled. Then, the CPU reads the Last Address +1 Buffer, U3030. If the memory address has passed FF during store mode, then U3030 indicates the oldest data in memory.

The CPU then sets the Mode Control Latch pin 2 to a 1, writing a 1 at DØ in address page 0:F5XX. The low /LATCHES SEL signal from the CPU (which corresponds to the 0:F portion of the address) is applied to U5040C, pin 9. Later, the /WR signal goes low at U5040C pin 8, and causes pin 10 to go high. (By addressing A1Ø high and A9 and A11 low, the CPU has already pulled pins 3 and 5 of U1030B high low.) Thus, when /WR goes low U1030B pin 6 also goes low. The high A8 bit at the input of U1025D enables U2020. Then, the positive edge of the /WR signal strobes the data into U2020, which causes pin 2 to go high and pin 3 to go low and permits the CPU to set an address into the MAC. (This also applies to the Expansion Option; the /MEM EN signal goes there to perform the same task.) At the same time, the high at pin 2 of U2020 permits U1010A to pass the enabling signal from U5040A, pin 1. When the CPU addresses page 2:EXXX, the /ACQ MEM SEL signal goes low, and the /RD signal later does also. This resulting positive edge at pin 1 of U5040A passes through U1010A, U1010C and U1020D to increment the MAC.

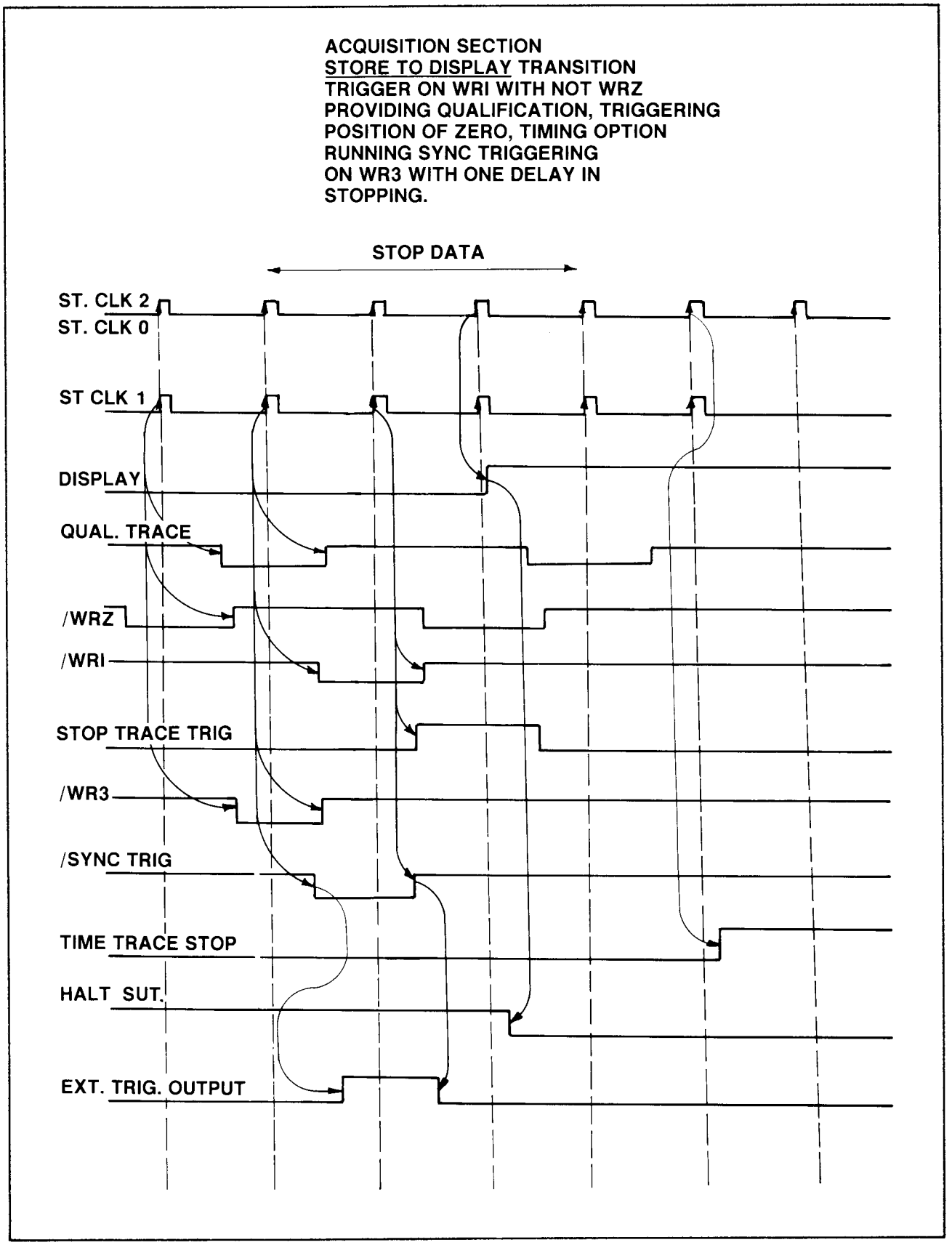


Fig. 2-16. Store-to-Display Transition Signal Timing Relations

Since the ST CLK 1 is low during the display mode, the transition from U1010A is passed to the MAC as a strobe signal. This clocks the CPU address into the MAC, permitting the CPU to select the location to be read.

Read Memory Description

Reading the Memory is accomplished as follows: First, since the CPU can read the D7 line from the Status Monitor (U2030), it can determine when the Memory is in the Display mode. When the D7 line from U2030 is low, the CPU checks the Full Status Monitor (D5 line) to determine whether the MAC has passed hexadecimal FF while storing data. Then, the CPU pulls the Y6 line of U2010 low to read the Last Address +1 Buffer, U3030. The information read there tells the CPU the address of the last word stored, plus one, which gives it a reference from which to start. The CPU then performs the following sequence of operations:

1. Address page 0:F5XX is called, and a 1 is set into the DØ line to pin 4 of U2020. (As discussed earlier, the page 0:F part of the address applies to the /LATCHES SEL signal at pin 9 of U5040C, and the 5 part of the address applies to the A11, A1Ø, A9, and A8 lines.)

2. The /WR line is pulled low, which clocks the 1 into U2020, pin 4. Pin 6 of U5040B goes high, which permits U5040A to control U1010A. Also, the pin 3 output of U2020 goes low, enabling the MAC, which now awaits a clock.

3. The CPU addresses page 2:EXXX, which is the /ACQ MEM SEL signal. This enables the /RD signal to control U5040A. In addition, the A1Ø, AØ, A11 and A1 lines are set at this time to address the desired RAMs. For example, an XX1Ø on the lower byte sets U2010, pin 13 low after the decoder is enabled. This low signal enables RAM U6020 and U6030.

4. The CPU sets a MAC address on lines A2 through A9.

5. The /RD signal goes low; this is passed through U5040A, U1010A, U1010C, and U1020D to clock the MAC, enabling the MAC output. The /RD signal also clocks U3050 and U4050 on the Expansion Option board, as the MACTNCK signal. Note that the ST CLK 1 signal is low during Display modes, so U1020D permits the MAC clocking signal to pass through the gate. The /RD signal also enables (through U5040A) pin 6 of U2010, which pulls pin 13 of U2010 low in this example, and data from U6020 and U6030 are placed on the Data Bus, lines DØ through D7.

Diagnostics

During the use of diagnostic procedures, U1010D is used for overriding the Display/Store Mode Control. Mode Control Latch U2020 sets the RDPL signal to a high state. This locks the output of U1010D low, which allows the ST CLK 1 signal to cycle the RAM during diagnostics.

STATE MACHINE

Introduction

Refer to Fig. 2-17, which is a simplified block diagram that illustrates the the most significant relationships among the State Machine circuits. The State Machine is the core of the 7D02; every other circuit is, in essence, peripheral to these circuits. A state machine is fundamentally a device that has inputs, outputs, logic, and a memory. Feedback for most state machines is provided through control logic, as just noted. However, in the 7D02, a RAM is used to make the State Machine programmable, and thus much more versatile than an ordinary state machine.

Fundamentally, the State Machine circuits consist of the State Machine (RAM, Multiplexer, Feedback, etc.) and two 16-bit Counters. The heart of the State Machine is the RAM, which is loaded by the CPU as directed by the opertor's program. The Counters provide the events or time count functions.

Figure 2-18 is a detailed block diagram of the State Machine. The Start-Up Control produces the inhibit signal, which disables the Counters and state machine during the first two clocks of a cycle, since this is a period in which invalid data occur.

The four word recognizer signals are applied to the State Machine Latch, which stores the signals at the occurrence of the state clock signal. The Latch also stores the state feedback bits from the RAM by way of the Multiplexer, and the counter feedback bits from the two 16-bit Counters. The information stored in the latch is used to address a location in the RAM. That location contains the data that are appropriate for the next operation.

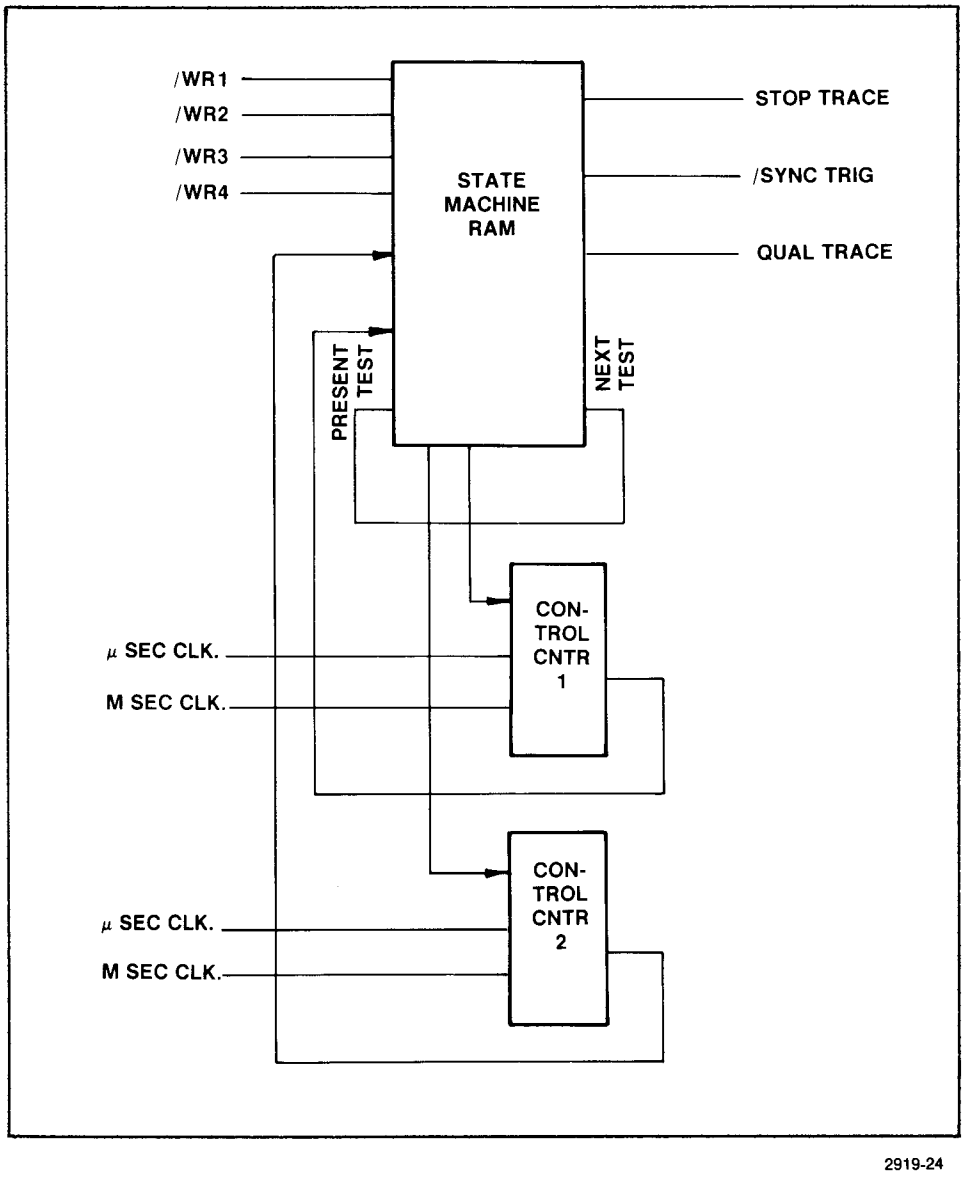


Fig. 2-17. State Machine Simplified Block Diagram.

Two 16-bit counters form a large part of the State Machine circuits. The Counters operate in two major modes: Time and Events. For example, the Counters will count events such as a re-occurring state clock, or measure the time, or define events such as: ten counts past the occurrence of WR1, or 50 uS past the occurrence of WR1. The commands that control the counters are Reset and Run, Run, and Stop, all in the Time mode; and Reset and Increment, both in the Event Mode.

The Divider circuit receives the 6-MHz signal from the CPU circuit, divides the 6 MHz signal into the 2 MHz, 200 kHz, 20 kHz, and 2 kHz output signals that are used in the State Machine, and also in the Timing Option circuits, if installed.

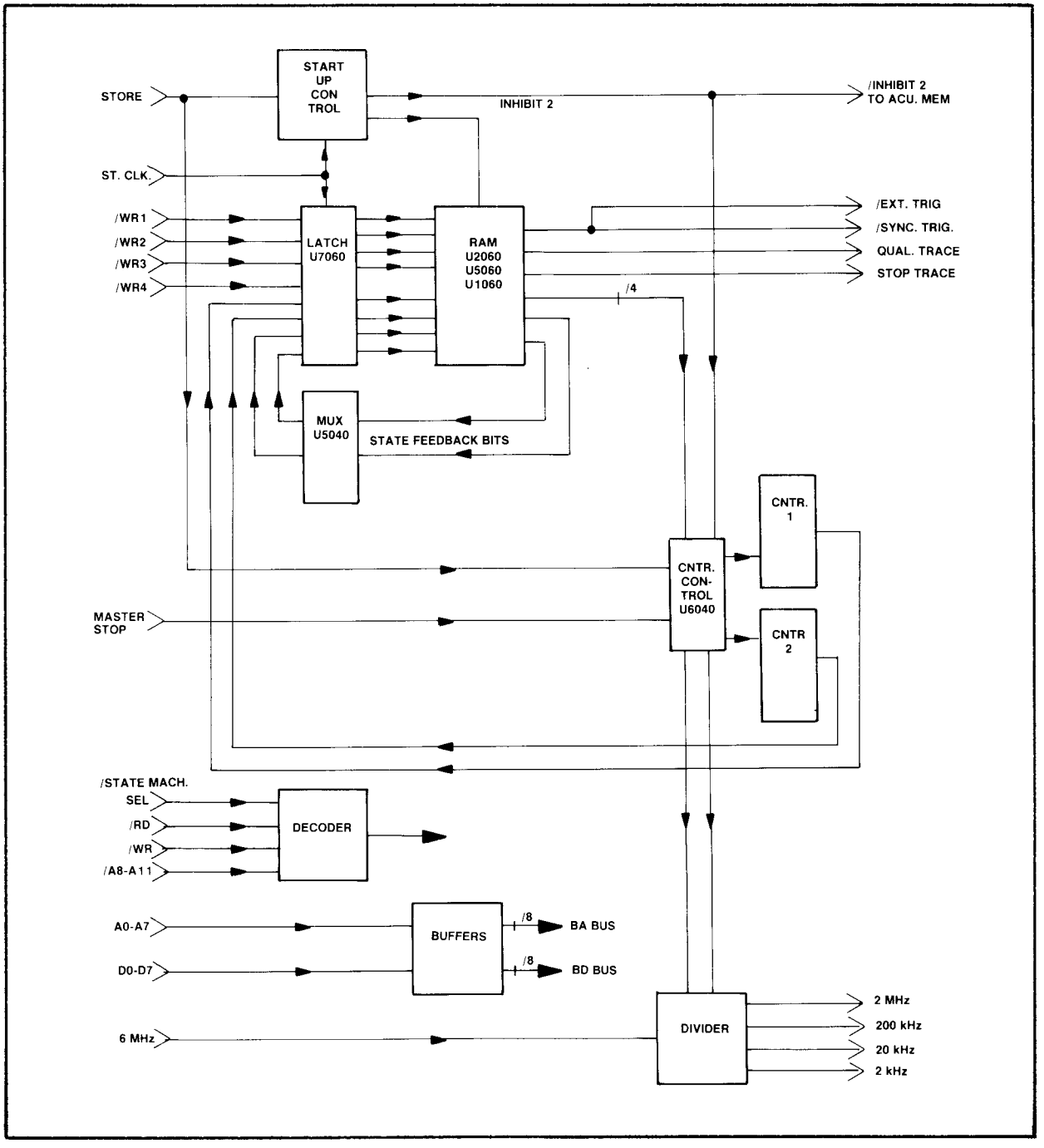


Fig. 2-18. State Machine Detailed Block Diagram.

The Decoder receives the read, write, and specific address signals, decodes those signals, and selects the appropriate devices to be read from or written into. The Decoder also furnishes timing pulses for some of the circuits in the State Machine.

The Address and Data lines are applied to the various buffer circuits on the board. These are translated into the Buffered Address (BA) Bus lines and the Buffered Data (BD) Bus lines, which are distributed throughout the State Machine for exchange of data and transmission of addresses.

While reading the following detailed description, refer to Diagrams 8A, 8B, and 8C. These depict the State Machine circuits.

Detailed Description

Buffered Address Bus (Diagram 8A)

The Word Recognizer bits, the two State Machine feedback lines, and the /CNTR 1 and /CNTR 2 signals are all fed to U7060, which is an edge-triggered octal latch. Triggering for the latch is from the BSC (Buffered State Clock) signal. The output of U7060 is applied to the three RAM integrated circuits, U2060, U5060, and U1060.

The other two devices that share the Address Bus function are U4060 and U3050. The first, U4060, is a tri-state octal buffer. It receives the AØ through A8 address bits from the CPU, and when enabled, applies the bits to the Buffered Address Bus. Pins 1 and 19 of the device enable the transfer of data; these are the CNT WR ENABLE signal from U5050, and an enable signal from latch U6020.

The second of the two is U3050, which is used to read back the Qualify RAM signals, QUALIFY TRACE, and the RESET 1 or RESET 2 signals into the buffered data bus. The latch also reads back the State Machine state during acquisition, the State Machine trigger state, the State Machine last state, and reading the Word Recognizers for self-test. Two CPU-controlled signals are applied to U3050: A read signal of 1:E4ØØ loads and latches the input information into U3050; a read signal of 1:E1ØØ puts the information present inside the latch on the BD Bus. The G signal from U4020A enables the latch. Generation of this signal is discussed later in this description.

Buffered Data Bus (Diagram 8A)

The Buffered Data Bus is used to read back the State Machine RAMs for verification, to read the Counter outputs, and to read the contents of U3050 for miscellaneous operating system information. The Buffered Data Bus consists of U2050 and U6060. Buffer U2050 is an octal tranceiver, which isolates the State Machine Data Bus from the 7D02 Main Interface Bus. The device is enabled by the /RD signal from the CPU, and the /ST MACH SEL D signal from U6020. The second device, U6060, is used to read the RAM. The RAM outputs are placed on the BD Bus whenever U2060 and U5060 are read.

State Machine Mode Register (Diagram 8A)

TABLE 2-10
State Machine Mode Register Bits

Output	State	Title	Output Mode
Q1	Ø	/E/T1	Counter 1 Events Mode
	1		Time Mode
Q2	Ø	/E/T2	Counter 2 Events Mode
	1		Time Mode
Q3	Ø	B	Counter 2: 1 kHz
	1		1 MHz
Q4	Ø	A	Counter 1: 1 kHz
	1		1 MHz
Q5	Ø	INHIBIT DISABLE	Disables the INHIBIT 1 and INHIBIT 2 signals.
	1		Normal start, discarding first two data cycles.
Q6	Ø	CNT WR EN	Read or write the RAM; write to counter.
	1		Acquisition cycle in process.
Q7			SFØ starting state.
Q8			SF1 starting state.

Octal latch U5050 serves as the State Machine Mode Register. It generates the CPU-programmable states that are used in the State Machine. Inputs to the latch come from the BD Data Bus, and are latched by the MWR4 signal from the Write Decoder, U6050. Refer to Table 2-10, which lists the outputs of U5050. Note that the output states of U5050 do not change until a bit change is applied to the device, and U5050 is once again addressed.

Inhibit Circuit (Diagram 8B)

As implied by the title, the Inhibit Circuit prevents part of the State Machine from operating during certain periods. During the first two state clock periods of the acquisition cycle, the INHIBIT 2 signal is kept high to prevent invalid data from appearing at the RAM output. Since the state clock signal is running while the RAM is inhibited, other state clock-triggered devices are also held off until the inhibit period ends. The signal is also used to preset several devices to a known state before the State Machine begins to operate, and hold those devices in that state until the second clock cycle is complete. Refer to Fig. 2-19, which illustrates the timing relationships in the Inhibit circuit.

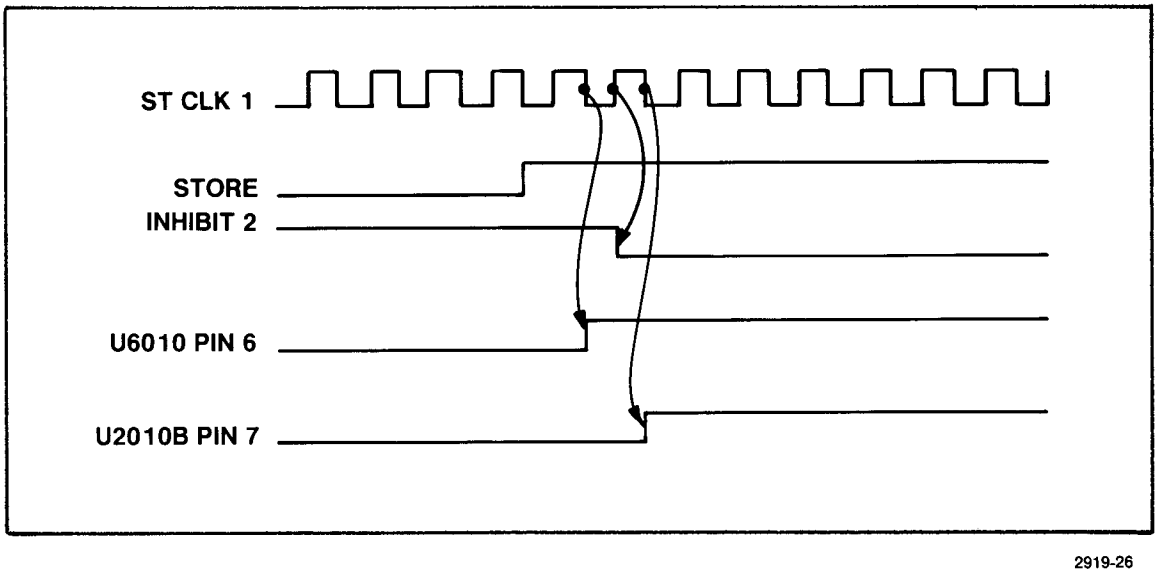


Fig. 2-19. Inhibit Circuit Timing Relationships.

The inputs to the Inhibit circuit are the /BSC 2 signal from U5010D, which is applied to the clock input of U6010A and U6010B (pins 1 and 13); the delayed store signal from multiplexer U5040; and the /MWR6 signal from the Write Decoder, U6050. The MWR6 signal, which is controlled by the CPU through the Write Decoder, is pulled low to set U6010A and B, and other flip-flops, before the acquisition cycle begins. At the point of setting U6010, the output of U1010B goes high, is inverted through U5010E as /INHIBIT 2A, and is applied to the select input of U5040 (see Diagram 8A) to enable the "A" side of the Multiplexer inputs.

Before proceeding further, it is necessary to explain the purpose of delaying the STORE signal to the K input, pin 2, of U6010A. When the 7D02 is equipped with the Timing Option, the starting time of the Main Section acquisition and that of the Timing Option Section differ slightly, in that the Timing Option will often start first. Thus, the STORE signal from the Main part of the 7D02 is used to reset U6010A. However, because of the difference in loading on the STATE CLK 1 and STATE CLK 2 lines, the STORE signal may go high before the first BSC signal has passed. To eliminate the race problem that might occur, the STORE signal is passed through U5040, which is configured to operate as a buffer for the section 4 inputs and output. In addition, R6028 and C6018 further delay the signal before it reaches U6010. Thus, an erroneous startup of the system is averted by delaying the STORE signal.

The Startup circuit operates as follows: When the first positive transition of /BSC2 occurs (as just discussed), STORE is still low, so U6010A remains set. When the second positive edge of /BSC2 occurs, the STORE signal has already gone high, so the flip-flop resets. Circuit U6010B cannot change state yet, since its K input was still low at the clock edge. On the following (third) /BSC2 edge, U6010B changes state, pulling the pin 5 input of U1010B low, and ending the positive excursion of the INHIBIT 2A signal. The /INHIBIT 2 signal moves high at this time, which switches the output of multiplexer U5040 to the "B" side of the inputs.

The INHIBIT DISABLE signal from U5050 is applied to the pin 4 input of U1010B to disable the inhibit signal at the option of the CPU. However, the disable function is used only during the Diagnostic mode of operation.

At the same time that the Inhibit circuit is set by the /MWR6 signal from U6050, that same signal sets U2010B, and its pin 7 output is low. As a result, the STATE CLK 1 signal is unable to pass through U1010A to the clock input of U1030A and U1030B in the Counter 1 and Counter 2 circuits until the first negative edge that occurs following the second STATE CLK 1 excursion. This prevents the Counters from counting an extra clock during start-up.

RAM Circuits (Diagram 8A)

The RAM circuits include the RAM, the Stop Trace Latch Circuit, and the Sync Trigger circuit. The 256 x 9 State Machine RAM consists of three integrated circuits: U2060 and U5060 are 256 x 4 devices, whereas U1060 is a 256 x 1 inverting RAM. The lines to address each RAM come from the Buffered Address circuits (BAØ-BA7), the D1 through D4 inputs are fed by the Buffered Data Bus (BDØ-BD7), and the Q1 through Q4 outputs are sent to the ØØ to Ø7 lines. Circuit U1060 is separately addressed to provide qualify information as the ninth bit of the memory.

The Stop Trace Latch circuit consists of U6020B, U7040A, U4020A, and U3050 (Diagram 8B). The circuit gates the buffered state clock (/BSC) signal to the enable input of U3050. At the outset of the Acquisition cycle, the /INHIBIT 2 signal sets the pin 9 output of U6020B high. This enables U7040A, pin 13, for the gate to pass the BSC signal if the other conditions are right. The G input to U3050 is enabled following every state clock signal. This condition persists until the STOP TRACE signal from U2060, pin 12, goes high. This resets U6020B after the next BSC pulse; U7040A is disabled, and U3050 is also disabled. Circuit U7040A is disabled by U5010A when STOP TRACE is high. This latches the trigger state, and also the state of the qualify line at that time.

The principal area of interest by the CPU in U3050 is in the BA6 and BA7 bits from that device. These lines permit the CPU to tell the operator the state of the State Machine at a given time. It should be noted that the output of U7040A is also dependent on enabling from the Y4 signal from Read Decoder U7050. Circuit U3050 also allows reading of the Qualify RAM, the RESET 1 and 2 signals, and Word Recognizer values.

The Sync Trigger circuit consists of U7015 and related components. The /SYNC TRIGGER signal comes from the State Machine RAM, and is sent to the Timing Option circuits. The signal also goes to the Front Panel of the 7D02. The signal comes from pin 10 of U2060 to an RC circuit consisting of R7060 and C7060 for filtering out the noise that occurs when a large number of address lines change at once. From the filter, the signal is applied to U7015. When writing into the RAM, a series of pulses will occur. The MASTER STOP signal is applied to the other input of U7015, which filters out the undesired signal transitions during writing time. The output signal, /EXT TRIG, is sent from P208, pin 23A to the Front Panel circuits.

State Feedback Bits Multiplexer (Diagram 8A)

This stage consists of U5040, a quad two-to-one multiplexer. The select input, pin 1, is controlled by the /INHIBIT 2 signal from U5010E, as discussed earlier. During the first part of an acquisition cycle, the select input is low. This allows the "A" side of the nputs to pass through to the outputs. Signals 1A and 2B are the starting states for the State Machine from U5050; signals 1B and 2A are the state feedback bits from the RAM. When the /INHIBIT signal goes high, the state feedback bits are selected. The 3A and 3B bits are the RESET 1 and RESET 2 signals to U3050. The RESET 2 signal is read first, after which the CPU resets U6010; then, the RESET 2 signal is read. The 4A and 4B inputs are tied together, so the STORE signal passes through despite the multiplexer state. The STORE signal is delayed by the multiplexer and the output RC circuit, as discussed earlier, to avoid producing the /INHIBIT signal too soon.

Decoder

JK flip-flop U6020 is configured as a latch and receives the /ST MACH SEL signal from the CPU board, along with the ALE signal. Whenever the CPU calls for an address in the range of 1:EØØØ-1:EFFF, the /ST MACH SEL signal goes low, and is clocked into U6020 on the negative edge of the ALE signal. (ALE is used to ensure that the enable lines to U6050 and U7050 are stable.) The output signals from U6020 are used to gate U6050, U7050, U4060, and U2050.

Decoder U6050 is called the Write Decoder. It is a 3- to 8-line decoder, and is driven by the pin 6 output of U6020, the /WR signal, and the A11 address line. Whenever the first signal is high and the last two are low, the device is enabled to pull low the output selected by address lines A8, A9, and A1Ø. For instance, whenever the address 1:E1ØØ is written, the MWR (Memory Write 1) line goes low.

Decoder U7050 is called the Read Decoder; it is similar to U6050, except that it is controlled by the /RD line from the CPU, instead of the /WR line. The outputs of the decoder, YØ through Y7, are fed to various circuits in the State Machine for read operations. Refer to Table 2-11, which is a memory map of the State Machine.

TABLE 2-11
State Machine Memory Map

1:EØØØ-1:EØFF		Main State Machine RAM	(Read or Write)
1:E1ØØ-1:E1FF		9th Bit RAM	(Write only)
1:E2XØ	Counter 1	Control Register	(Read or Write)
1:E2X1		Read Control Register	
1:E2X2		Read Upper 8 Bits	
1:E2X3		Read Lower 8 Bits	
1:E2X4		Write Re-initialize to Value in Holding Register	
1:E2X5		Write Load Lower 8 Bits	
1:E2X6		Write Load Upper 8 Bits	
1:E2X7		Counter 1 Enable	
1:E3XØ	Counter 2:	Control Register	(Read or Write)
1:E3X1		Read Control Register	
1:E3X2		Read Upper 8 Bits	
1:E3X3		Read Lower 8 Bits	
1:E3X4		Write Re-initialize to Value in Holding Register	
1:E3X5		Write Load Lower 8 Bits	
1:E3X6		Write Load Upper 8 Bits	
1:E3X7		Counter 2 Enable	
1:E4ØØ	Read:	Allows 9th-bit RAM to be read out	
1:E4ØØ	Write:	State Machine Mode Register	
1:E5ØØ	Read:	FF preset (must be done prior to loading counters)	
1:E5ØØ	Write:	counter Output Reset (must be done prior to acquisition)	
1:E6ØØ	Write:	Initializes State Machine	

Divider Circuit (Diagram 8B)

The 6-MHz clock signal from the CPU circuits enters the State Machine Board at P208, pin 26B and is applied to inverter U5030C. The inverted clock is then applied to U7020A. The inverter is a buffer to reduce noise on the received signal. AND gate U1010D provides the feedback to convert the three-cell counter into the divide-by-three counter that is required to produce the 2-MHz output. The 2-MHz signal from U7020 pin 6 is fed to U7020B, to U6040, and from P208, pin 26A to the Timing Option Circuits.

The 2-MHz signal clocks U7020B, which is configured to operate as a divde-by-ten counter. The output of the counter, 200 kHz, is fed out pin 25B to the Timing Option circuits, and to U7030A, which is a CMOS decade counter. This stage divides the signal to 20 kHz, and applies the signal to U7030B and through buffer U5030 to the Timing Option circuits. Decade Counter U7030B divides the applied 20 kHz into 2 kHz, and applies it through U5030A to the input of U6040, which is a dual four-line to one-line multiplexer. The 2-kHz signal is also sent out to the Timing Option.

Timing Counter Control Circuit (Diagram 8B)

The Timing Counter Control circuit consists of Multiplexer U6040 and JK flip-flops U6030A and U6030B. The multiplexer selects the counter signal source, as listed in Table 2-12. The two sources are the 2-kHz and 1-MHz signals from the divider circuit. The multiplexer is gated on by the MASTER STOP signal, so that, when the MASTER STOP line goes high at the end of the acquisition period, both outputs of the multiplexer turn off.

TABLE 2-12
U6040 Truth Table

A	B	1Y Output and Resolution	2Y Output and Resolution
low	low	2 kHz, 1 mS	2 kHz, 1 mS
low	high	2 kHz, 1 mS	2 MHz, 1 uS
high	low	2 MHz, 1 uS	2 kHz, 1 mS
high	high	2 MHz, 1 uS	2 MHz, 1 uS

The two outputs of the multiplexer are each fed to a gated JK flip-flop, which divides the incoming clock by two. These flip-flops operate similarly, so only U6030A is discussed here. When the count is to begin, the J and K inputs to U6030A are pulled high, by the Start/Stop Circuit (U1020), which enables U6030A to toggle on the applied clock (2 kHz or 2 MHz). The divided clock is applied to Multiplexer U2040 for application to the Counter 1 stages, as required.

Counters (Diagram 8C)

Refer to Diagram 8C; the lower half of the diagram depicts the two counters. Counter 1 is the upper circuit chain, and Counter 2 is the lower circuit. Both counters are essentially identical, so only the Counter 1 circuits will be described herein, except where important differences might affect the description. In the following discussion, the summary of counter

performance is followed by a description of the major parts of the counter. Last is a description of each major mode. Table 2-13 is a listing of the major counter performance factors.

The Counters operate in three modes of operation: time, event count, and event control. In the following discussion, the function of each major segment of the Counter is explained. Refer to Fig. 2-20, which is a detailed block diagram of the Counter 1 circuits. Refer also to Table 2-14, which lists the counter commands from the State Machine RAM.

TABLE 2-13
Counter Performance Summary

Counting Mode	Minimum Count	Maximum Count	Error
Time*	0	65534	+/- 1 count or +/- 0.01
Events	0	54434	0
Control Mode			
Time*			
Pulse Width Generation	2	65534	-0, +1 count -0, +0.2 uS, +/- 0.1%
Measurement, Counter stopped before terminal count	0	User value -1	-0, +2 counts +/- 0.01%
Events			
Event Count Window	2	65535	0
Measurement, Counter stopped before terminal count	0	User value -1	0

*When using the time mode of the counters, there is another additive error: The times noted above are given for one start/stop cycle of the counters. In the case of more than one cycle, the error bounds increase, to the absolute error bound of +/- N counts, where N is the number of start and stop cycles.

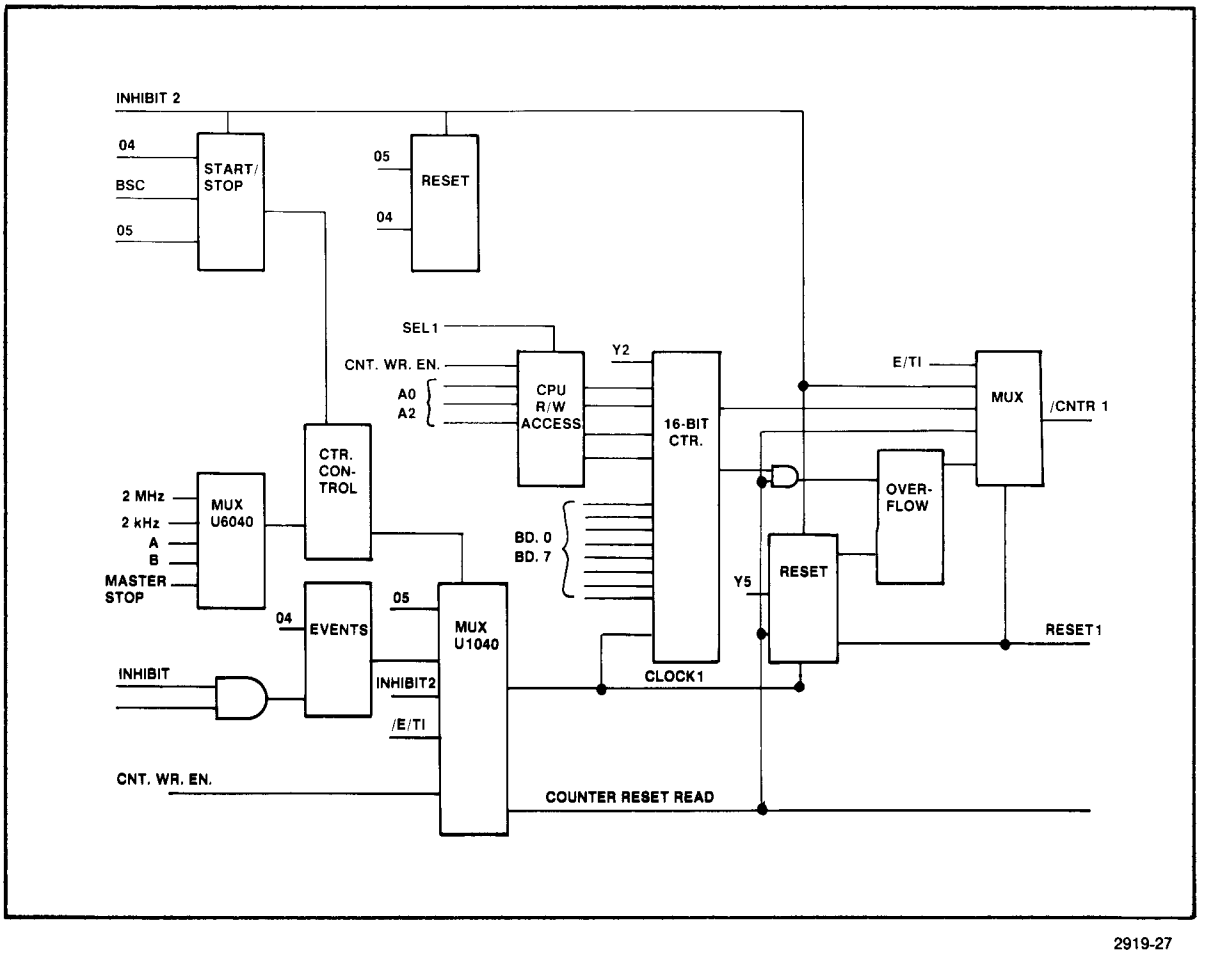


Fig. 2-20. Counter 1 Block Diagram.

TABLE 2-14
State Machine Counter Commands

05, 04 or 03, 02	Command	
	Time	Events
low low	RUN	NOP
low high	Reset and Run	Increment Once
high high	Stop	Reset
high low	NOP	(Not Used)

Start-Stop Circuit. This circuit consists of U3020B, U5010C, and U1020B. The 04 and 05 lines from the RAM control the enabling of the clock to be applied when the Time mode is selected.

Operation is as follows: The /INHIBIT 2 signal from U5010E is low for the first two state clocks of the measurement cycle. Thus, U1020 is set at this time, which causes a low to be placed on the J and K inputs of U6030A. This prevents any clock pulses from being applied to the counter for now. After an event occurs and a counter command is issued (see Table 2-14), the 04 and 05 lines are set to enable the clock signals. For now, assume that the Run command is selected for Counter 1, which means that the 05 line is low. The state of 04 is not significant to this circuit when 05 is low. When the /INHIBIT 2 line returns low, U1020B is free to change state, and the low at pin 11 and high at pin 12 arm it to do so. When the negative edge of the first /BSC1 pulse occurs, U1020B is cleared, and the high from its pin 8 permits U6030A to begin passing the divider output (1 MHz or 1 kHz) to the Counter. When the cycle is completed, the 05 line is set high by the RAM. This causes the K input to U1020B to move low, and the flip-flop will remain in the reset condition until a command is issued to change. The command that sets U1020B is the STOP command. To set U1020B, lines 04 and 05 must both be high. This presents a high at pin 11, U1020B, and a low at pin 12 of U1020B. This will set the flip-flop (U1020B) at the next negative edge of the /BSC1 signal.

Reset-Load Circuit. This circuit consists of U3020C, U5020E, and U1020A. Control inputs for the circuit are the 04 and 05 lines from the RAM, the /BSC1 signal, /INHIBIT 2, and the /LOAD 1 signal from the other Reset stage, U2030A. At setup, the CPU sets U2030A, thus clearing U1020A. At the beginning of the cycle, the /INHIBIT 2 signal moves low, forcing the K input of U1020A low for the first two clock pulses to prevent the flip-flop from switching before the cycle begins. When the /INHIBIT 2 signal returns high, the counter control codes again have control of the circuit. Depending on other requirements of the program from the State Machine RAM, the counter control codes will vary in state. When the command to reset and run Counter 1 occurs, the RAM produces a high at the 04 signal and a low at the 05 signal. This enables U1020A to reset at the next negative edge of the /BSC signal. The high level from the pin 6 output of U1020A is coupled to the pin 12 input of multiplexer U2040. If the mode of operation is Time, the high is coupled out of U2040 as the COUNTER RESET READ signal, which is sent to the J and K inputs of U2030A. This high permits U2030A to change state to the set condition, which pulls the /LOAD 1 signal low. As a result, U1020A is set by the low at pin 4, and U1040

receives a low at the pin 2 and pin 3 inputs, to be used as part of an instruction to reinitialize the counter. Flip-flop U1020A cannot change state for the remainder of the cycle, because of the low at pin 4.

The output from U3020C and U5020E is also fed forward to U3010 pin 13, as a look-ahead function. When high, and the counter completes counting /CNTR 1 goes low. However, if RESET 1 is high (meaning the counter is being reset), U5020B locks /CNTR 1 high until the counter resets. In time mode, the high state of U3020C, U5020E indicates that a Reset command was issued. This locks /CNTR 1 high.

Events Clock Generation. This circuit consists of U1030A and U4020. When the proper control code (04 high; the state of 05 is irrelevant to this circuit) is applied to pin 2 of U1030A, the flip-flop is permitted to change state when clocked. The purpose of the circuit is to produce the clock to be applied to the Counter circuit.

At the outset of the counter cycle, the state clock signal is not permitted to pass through U1010A by the high state of U2010B pin 7. Following the second state clock signal, pin 1 of U1010 moves high, so the third state clock signal will be passed to pin 4 of U1030A, which changes state to the set condition. This results in a high level, beginning the first event, to be applied to pin 3 of multiplexer U2040, and to pin 9 of U4020C. Since the gated state clock 1 and /BSC2 signals are time-coincident, pin 9 of U4020C moves high just after pin 10 moved low. At the end of the /BSC pulse, both inputs to U4020C are high, so the low at pin 1 of U1030 resets the flip-flop, ending the event pulse. With the next state clock pulse, the circuit repeats the cycle just described. Figure 2-20 illustrates the timing relationship of the signals involved in the circuit.

Multiplexer. This stage is a dual four-line to one-line multiplexer that controls the passage of clock signals and status signals to the CPU. This selects the Time or Events mode of operation. The stage is controlled by the INHIBIT 2 signal, which disables the multiplexer during the first part of the counter operating cycle, and the E/T1 and CNT WR EN signals, which carry the encoded data to control the multiplexer selection. Table 2-15 lists the outputs that occur with different input combinations.

TABLE 2-15
Truth Table for Multiplexer U2040

A	B	Output 1Y	Output 2Y
low	low	Ground; no clock to U1050	Counter 2 Reset status from U2020B
low	high	MWR2 signal from U6050	Ground
high	low	Clock signal from U6030	Counter 1 Reset status from U1020A
high	high	Events pulses from U1030A	05 Control Code from RAM

CPU Read-Write Access Gate. This is a quadruple two-line to one-line multiplexer. Its purpose is to control the operating modes of the 16-bit Counter, U1050. Selection of the channel to be enabled is controlled by the SELECT 1 line to pin 1 of the multiplexer. When the pin is low, the A channels are selected, and when pin 1 is high, the B channels are selected. Note that the pin 11 input to U1040 is connected to +5 V, and the pin 14 input is connected to the /CNT WR EN signal. Since the 4A and 4B inputs are channeled to the IE input of the counter, only the three least significant bits are used to provide instructions to the counter. Further, the 1A and 2A lines are tied together, so only a value of 4 or 7 can pass through the A side of the multiplexer. The counter receives the value 4 as an instruction to reinitialize, and the value 7 as an instruction to enable the count.

The B side of the multiplexer receives data via the AØ through A2 lines, which are then sent (when pin 1 is high) to the IØ through I2 instruction inputs to the counter.

16-bit Counter. The Counter consists of U1050, which is a programmable, presettable, 16-bit binary counter. In this configuration, three instruction lines permit the selection of eight different modes of operation. An eight-bit I/O bus permits preloading of the counter and reading of the counter output lines.

Refer to Table 2-16, which is a list of the counter states. Note that, as noted above, only the 4 and 7 values are used in normal counter operation. However, through multiplexer U1040, the CPU can select any one of the eight combinations, software permitting.

TABLE 2-16
U1050 Operating Modes

Inputs I_0 I_1 I_1 (hexadecimal)	Modes
L L L (0)	Write Control Register
L L H (1)	Read Control Register
L H L (2)	Read Word Counter
L H H (3)	Read Address Counter
H L L (4)	Reinitialize Counters
H L H (5)	Load Address
H H L (6)	Load Word Count
H H H (7)	Enable Counters

Data fed into the I/O are latched into the internal bus of the Counter on the positive edge of a clock signal applied to pin 10. The Y2 signal from the Read control Buffer (U7050) enables the pin 9 input to place the Counter outputs on the buffered data (BDØ-BD7) lines. The ACI line is used to enable incrementing or decrementing the Counter by applying a clock pulse to the clock input, pin 10. The IE input, pin 8, enables the instruction inputs listed at the top of Table 2-16.

Reset Flip-flop. As discussed earlier, the Reset Flip-flop (U2030A) operates in conjunction with U1020A through multiplexer U2040 in Time mode. The high from pin 9 of U2040 enables U2030A to change state. The /INHIBIT 2 signal has already placed U2030A in the reset state at the beginning of the count cycle, so, when the first clock pulse is applied to U2030A after the COUNTER RESET READ line goes high (from U2040, pin 9), the flip-flop sets. The pin 6 output goes high, and the pin 7 output goes low. The output from pin 6 (RESET 1) is inverted through U5020B and applied to pin 2 of U7010B, to pin 13 of multiplexer U3010, and to pin 11 of U7015. This prevents the Counter from indicating that the count is complete while the Counter is being reset. These are discussed later in this description. The RESET 1 signal is also sent to U5040 (Diagram 8A), to be multiplexed with other signals for CPU access. Output pin 7 of U2030A, now low, resets U2030B, and is fed back to set U1020A and to apply the reset value to U1040. The set input to U2030A, pin 5, is used by the CPU to set the Counter.

Overflow Flip-flop. This flip-flop, U2030B, stops the Counter when overflow occurs. Early in the sequence of count events, the Reset Flip-flop just discussed resets U2030B. The J input (pin 14) of U2030B is held low by U4030 until counter overflow occurs, so U2030B cannot set until the line moves high. When overflow occurs, COUNTER RESET READ will already have gone low, so the high at the J input of U2030B permits it to change state at the next clock signal. The pin 10 output, /CNT 1 goes high and stops the Counter from further operation. This signal is also fed to multiplexer U3010. The opposite signal from U2030B pin 9 goes to pin 10 of U7015B, which is used in the timer mode of operation.

Counter Output Multiplexer. This circuit consists of U3010 and is an AND-OR-invert gate that produces the /CNTR 1 signal from four different sources. Refer to Fig. 2-21, which illustrates the quivalent logic diagram of the device. As shown on the diagram, a low state at the /CNTR 1 output occurs with three sets of conditions. Note that the INCREMENT and RESET COMMAND lines are from the same source. These are expressed differently in the Time and Events modes to better illustrate the purpose of the line.

Counter Mode Description. In the following paragraphs, the operation of Counter 1 is described in each of the major modes of operation.

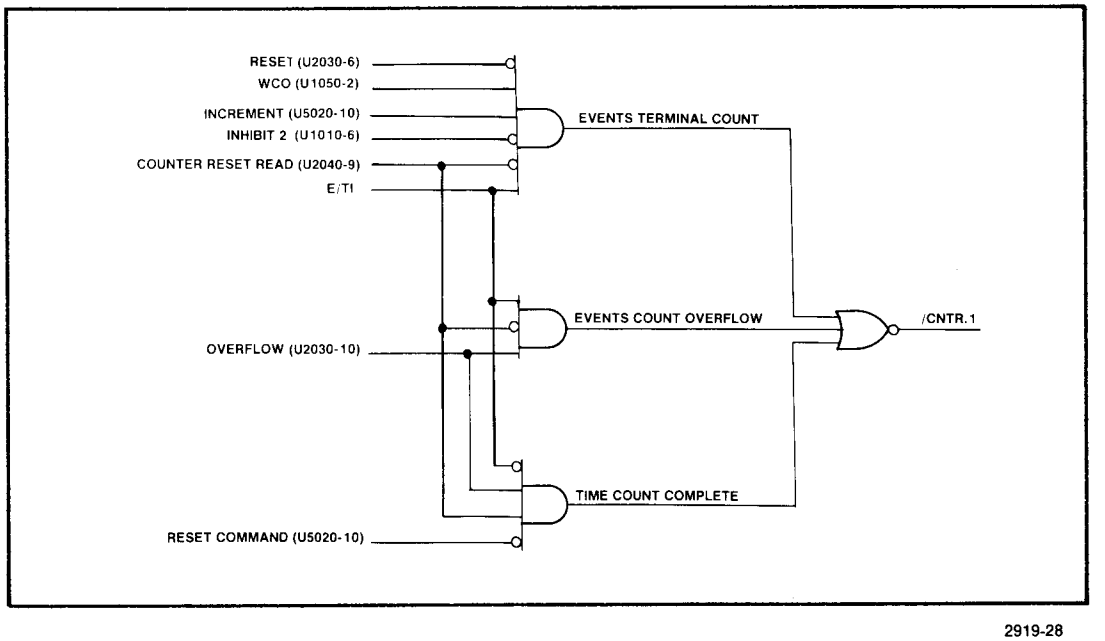


Fig. 2-21. Equivalent Logic Diagram of U3010 and Connecting Circuits.

1. **Time Mode.** In the Time mode, the following sequence and algorithm applies:

a. The CPU loads the counter with the value 3.

b. The CPU sets the counter to the decrement mode.

c. The CPU commands the counter to count twice.

d. The CPU sets the counter to the increment mode.

At this point, the counter is ready to run. Following the acquisition cycle, the counter is read by using the following algorithm.

IF (Reset and Start flip-flop (U1020A or U2020B) is set) THEN (result of count) = 0.
ELSE IF (Reset flip-flop (U2030A or U3030B) is set) THEN (result of count) = 0.
ELSE IF (value read from counter) = 1 THEN (result of count) = 0.
ELSE IF (value read from counter) = 2 THEN (result of count) = 1
ELSE IF (value read from counter) = 0000 THEN (result of count) = overflow
ELSE (result of count) = ((value read from counter) = 1).

2. **Time Control Mode.** In the Time Control mode, the following sequence and algorithm applies:

a. the CPU loads the counter with the user value -2.

b. The CPU sets the counter to the increment mode.

c. The CPU commands the counter to count twice.

d. The CPU sets the counter to the decrement mode.

At this point, the counter is ready to run. Following the acquisition cycle, the counter is read by using the following algorithm:

IF (Reset and Start flip-flop (U1020A or U2020B)) THEN result = 0.
ELSE IF (Reset flip-flop (U2030A or U3030B)) THEN result = 1.
ELSE IF (user value) equals counter value THEN result = 0.
ELSE IF (user value -1) equals counter value THEN result = 1.
ELSE IF (counter value) = FFFF THEN result = user value.
ELSE result = user value - counter value -1.

Refer to Fig. 2-22, which illustrates the circuits used in this mode. The /INHIBIT signal presets Start-Stop flip-flop U1020B and Reset-Look Ahead flip-flop U1020A at the beginning of the operation. This causes both

flip-flops to have a low output. The low from U1020B pulls the J and K inputs of U6030A low, which prevents that flip-flop from passing the applied clock signal from U6040. The low from U1020A is fed to pin 12 of multiplexer U2040. This line is used to inform the CPU (by means of the COUNTER RESET READ line) of the counter's status.

When the /INHIBIT 2 signal goes high following the second STATE CLOCK signal, U1020B is free to change state. The 05 line from the State Machine RAM is now low, so the K input of U1020B is high, and the J input is low, because of the low state of the 04 line at the input of U3020. (The low 05 and low 04 correspond to the counter commands, RUN.) When the /BSC signal next occurs, both U1020A and U1020B change states to the reset condition, and the outputs, pin 6 and 8 go high. The first, from pin 6, causes the COUNTER RESET READ line to go high when the multiplexer (U2040) selects the U1020A output; this informs the CPU that the Counter is in operation. The second, from U1020B, permits U6030 to pass the divided clock to U2040 as the timer clock. This signal is either 1 MHz or 1 kHz, depending on the instructions from the State Machine RAM.

Multiplexer U2040 is a dual four-line to one-line multiplexer. In this case, the CNT WR EN signal is high and the E/T1 signal is low, which connects the clock signal from U6030A to output pin 7 for application to the Counter, and input pin 12 (status from U1020A) to output pin 9, the COUNTER RESET READ signal. The multiplexer is initially held off by the INHIBIT 2 signal, but is enabled following the second state clock pulse. The clock signal from pin 7 of the multiplexer is applied to pin 10, the clock input, of 16-bit Counter U1050.

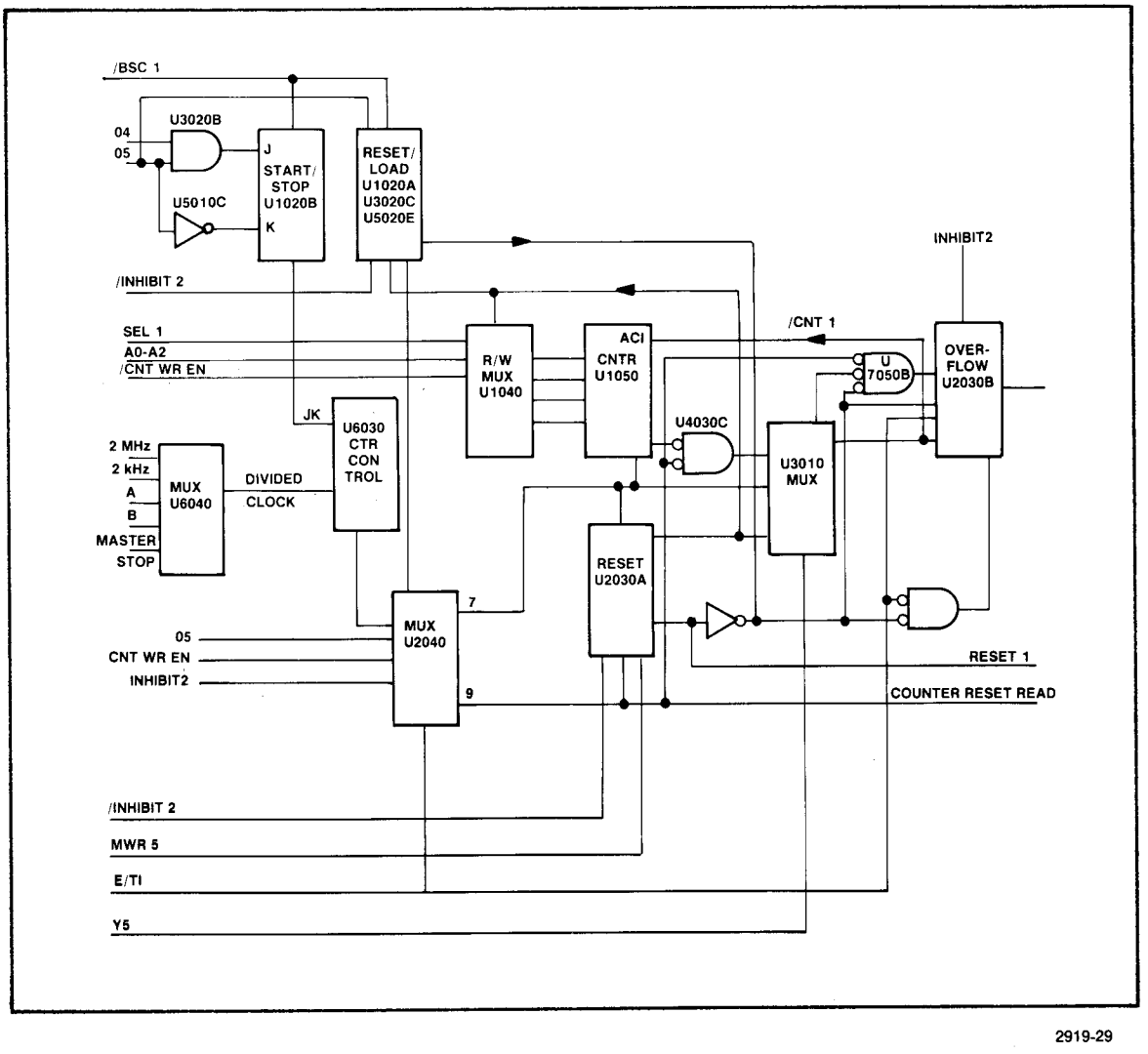


Fig. 2-22. Block Diagram of Counter #1 for Time Mode.

The CPU R/W Access Gate (U1040) is a quadruple two-line to one-line multiplexer. The SELECT 1 line from the Decoder circuits controls the multiplexer by way of the S input line, pin 1. Essentially, the multiplexer chooses between allowing the CPU to load a predetermined number into the Counter by way of the BDØ-BD7 lines, or to run the Counter. In this mode, the multiplexer passes the enable or reinitialize command from Reset flip-flop U2030A.

Central to the Counter 1 circuit is U1050. It accepts eight parallel preloading lines from the data bus, and is mode-controllable by way of the

IE, IØ, I1, and I2 lines from the CPU R/W access gate. In the timer mode, the Counter is set to Ø, then permitted to run as long as the gating signal allows clock pulses to enter. If the Counter reaches an accumulation of 66535, pin 2 of U1050 goes low. This causes U4030C, pin 10, to go high (COUNTER RESET READ is already low), which enables the J input, pin 14, of U2030B, and the flip-flop changes state at the next applied clock. (It was previously preset by the Y5 signal.) The high state from U2030B, pin 10 (IGNT1) is applied back to the ACI input of U1050, stopping the Counter. It is also applied to pin 9 of the Output Multiplexer, U3010. The pin 10 input of U3010 is already high, so U3010, pin 8 (/CNTR 1), goes low to indicate the termination of the count.

3. **Event Count Mode.** In the Event Count Mode, the following sequence and algorithm applies:

a. The CPU loads the counter with the value 2.

b. The CPU sets the counter to the decrement mode.

c. The CPU commands the counter to count once.

d. The CPU sets the counter to the increment mode.

At this point, the counter is ready to run. Following the acquisition cycle, the counters are read, using the following algorithm:

IF (value of Reset flip-flop (U2030A or U3030B)) is set OR (value of counter) = 1
THEN (result of count).
ELSE IF (value read from counter) = 0000
THEN (result of count) = (overflow).
ELSE (result of count) = ((value read from counter) -1).

Refer to Fig. 2-23, which is the detailed block diagram of the circuits used in the Events Count mode. When this mode is selected, the counter control code is such that the Events flip-flop (U1030A) begins to produce event pulses, which are derived from the STATE CLOCK pulses. These are applied to Multiplexer U2040, which passes the events pulses through to U1050, the 16-bit counter, and to clock the Reset and Overflow flip-flops (U2030A and B), as required.

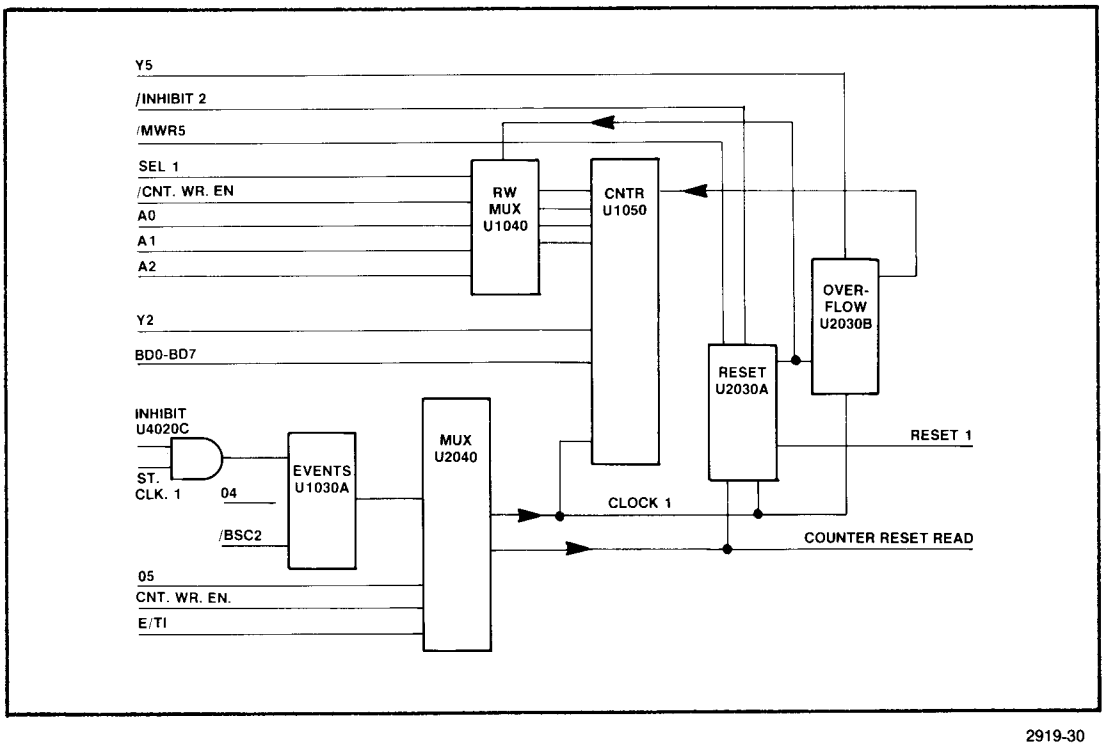


Fig. 2-23. Block Diagram of Counter #1 for Events Count Mode.

Read/Write Access Multiplexer U1040 operates the same in this mode as in the Timer mode, in that the Counter is either directed to reinitialize or to increment. See the detailed discussion on the Counter circuit earlier in this description.

The Counter increments once for each event applied to the clock input until the events to be counted have occurred, or the counter overflows. When the counter overflows, the Overflow flip-flop will stop the counter and pull low on the /CNTR 1 line at the output of Multiplexer U3010.

4. **Control Mode.** The Control Mode applies to both events and time operations. The following sequence and algorithm applies:

a. The CPU loads the counter with a value equal to the user value minus 2.

b. The CPU sets the counter to the increment mode.

c. The CPU commands the counter to count once.

d. The CPU sets the counter to the decrement mode.

At this point, the counter is ready to run. Following the acquisition cycle, the counter can be read by the CPU with the following algorithm:

IF (value of Reset flip-flop (U2030A or U3030B) is set)
THEN (result of count) = 0.

ELSE IF (value read from counters) = (FFFF)
THEN (result of count) = user value.

ELSE IF (user value -1) is less than (value read from counter)
THEN (result of count) = 0.

ELSE (result of count) = ((user value) - (value read from counter) -1).

Refer to Fig. 2-24, which is the detailed block diagram showing the circuit elements used for the Counter Control mode. The purpose of the mode is to permit the CPU to load, read, and increment or decrement the counter as required. Thus, the counter can be loaded with a number, then incremented until overflow occurs. At this time, the counter will indicate that the count is complete.

The Events circuit is used, as appropriate, to generate an event pulse for clocking the counter. Multiplexer U2040 passes the clock pulse through to the counter as the CLOCK 1 signal. The COUNTER RESET READ line is used to provide status information to the CPU.

If the CPU is to load a number into the input of the counter, the R/W Multiplexer is directed, by means of the AØ-A2 lines, to enable loading. At the same time, the CPU places the number to be loaded at the BDØ-BD7 inputs, then clocks the counter once to latch the number into the counter register.

If the CPU is to read the contents of the counter, a code is sent to the R/W Multiplexer which enables the counter to place the contents from the output register on the data bus, lines BDØ-BD7.

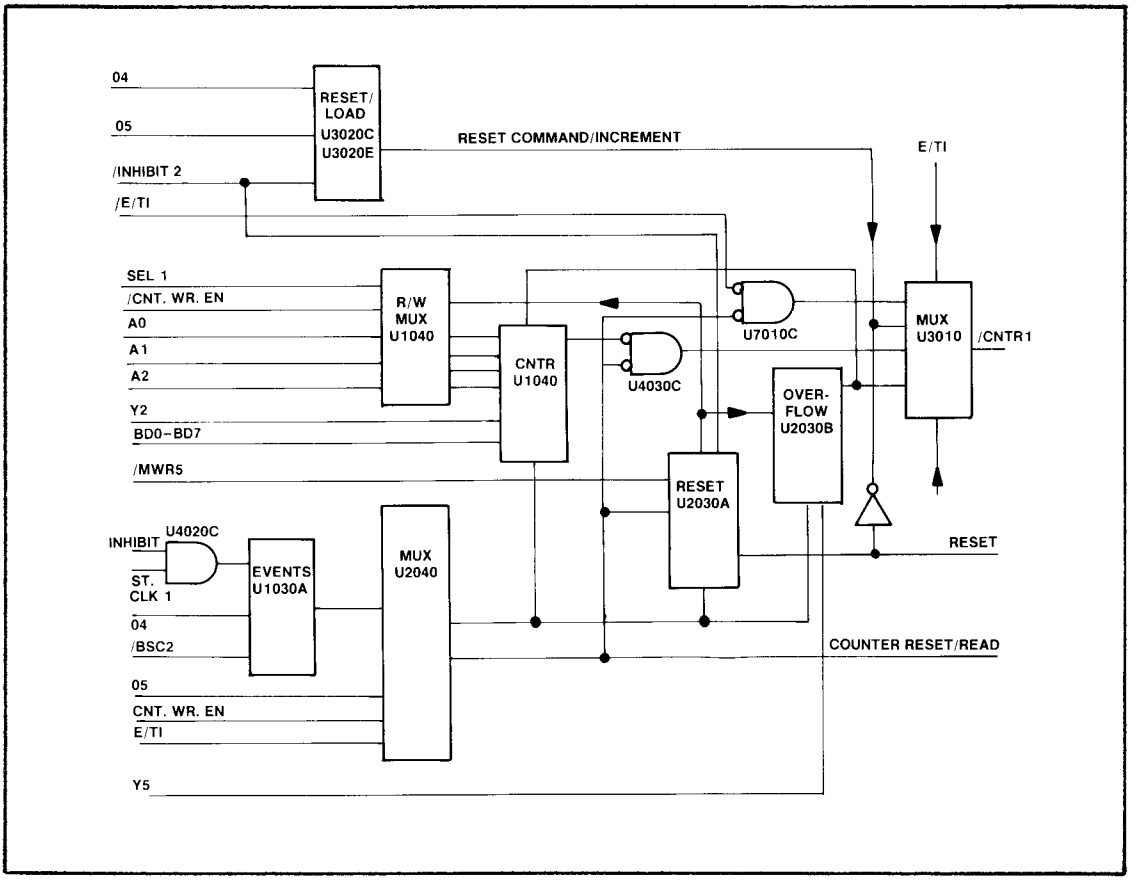


Fig. 2-24. Block Diagram of Counter #1 for Events Control Mode.

The Reset flip-flop is used in this mode to reset the counter during or after the count process. The Overflow flip-flop detects overflow, then prevents the counter from incrementing further until another count operation is commanded.

CPU CIRCUITS

Introduction

Refer to Fig. 2-25, which is a detailed block diagram of the CPU circuits. The CPU consists of the following major circuits:

1. The CPU and Buffer, which is the controller for the 7D02. The CPU is an 8085 Microprocessor that controls the entire 7D02, except for the power supply circuits. The Microprocessor communicates by way of an eight-bit data bus (DØ-D7) and a sixteen-bit address bus (AØ-A15).

2. The CPU Timing Circuits, which consist of the Clock, Interrupt Timer, Power-up Reset Gate, and Wait State Generator. The Clock circuit generates the 6-MHz timing signal for use by the Microprocessor and by the State Machine circuits. The Interrupt Timer generates a 30-Hz timing signal that prompts the Microprocessor to scan the keyboard and blink the display cursor, as required. The Power-up Reset Gate is used to reset the Microprocessor for diagnostic purposes. The Wait-State Generator creates the delay necessary to compensate for propagation delay from the Personality Module and to synchronize Microprocessor operations with those of the Display circuits.

3. The Selection Logic Circuits, which separate the memory into smaller address partitions. These circuits consist of the I/O Select Circuits, the I/O Page Select Circuit, and the Memory Partition Circuit, and combine to decode the CPU address lines into one of eight address segments.

4. The Buffers, which consist of the Address Latch and Data I/O Buffers. The Address Latch provides buffering and interim storage of the lower eight address bits from the CPU. The Data I/O Buffers receive and transmit data between the main interface and the data bus internal to the CPU board.

5. The RAM and ROM circuits, which store hardware and software instructions and routines, plus data acquired from the Timing Option circuits, or from the Personality Module.

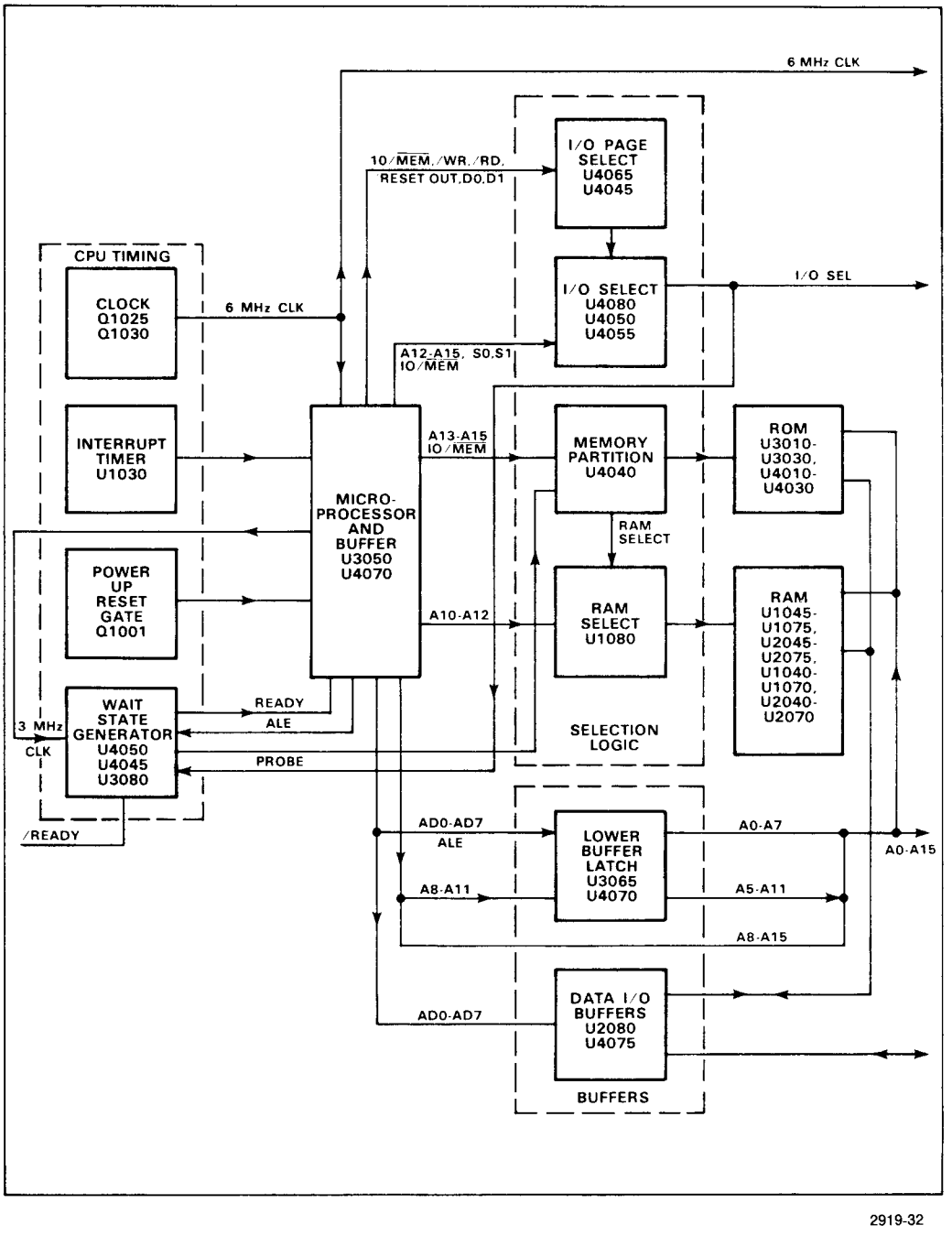


Fig. 2-25. CPU Circuits Detailed Block Diagram

CPU Timing Circuits

The CPU Timing circuits consist of the Clock circuit, the Power-up Reset Gate, the Wait-state Generator, and the Interrupt Timer. Refer to Diagrams 9A and 9B while reading these descriptions.

Clock Circuit. The clock signal is generated by the oscillator that consists of transistors Q1025, Q1030, buffer U4070B, and related components. Transistor Q1025 and nearby components form a Colpitts oscillator. The output is taken from the collector of Q1025, then applied to a temperature-compensated amplifier that is formed by diode CR1021 and transistor Q1030. The 6-MHz output signal is then applied through buffer U4070B to U3050 (the Microprocessor) and off the board to the State Machine circuits. The Microprocessor divides the applied 6-MHz clock by two for the 3-MHz clock that is used extensively throughout the 7D02.

Power-up Reset Gate. This circuit consists of Q1001 and related components. The circuit is used to reset the Microprocessor for service and diagnostic purposes, and to ensure proper turn-on. There are two modes of activation: Power-up and Reset.

When the 7D02 is turned on, nearly one-half second transpires before the supply reaches full voltage. During this time, the 7D02 will be held in the reset condition. Diodes VR1007 and CR1002 prevent Q1001 from turning on until the supply voltage rises to approximately +4.2 V. When the supply reaches this value, Q1001 begins to supply current from C1001. The Microprocessor remains in the reset condition until the charge on C1001 reaches about +2.4 V.

If the power supply fails momentarily, CR1001 discharges C1001, the Microprocessor is reset, and the system is restarted. This ensures that the Microprocessor will not execute erroneous programs that occur because of power failure.

When the RESET pushbutton is pressed, C1001 is discharged through R1001. Upon release of the pushbutton, C1001 begins to charge again, through Q1001. From the moment of pushbutton release to turn-on of the Microprocessor, the elapsed time is usually about 0.3 second.

Wait-State Generator. To begin this description, it is important to define the meaning of the term "wait-state". For the purposes of this description, the term refers to a period in which Microprocessor activity

is deferred; that is, the Microprocessor is simply held dormant. The customary length of wait-state periods is one or two 3-MHz-clock cycles, depending on the source of the wait-state prompt.

The Wait-state Generator consists of U4050A, U4050C, U4045A, U4055C, U3080, and U4055B. The purpose of the circuit is to extend the Microprocessor operating cycle to accomodate the delayed response of the Personality Module and to wait for read or write access to the Display RAM. When reading from the Personality Module ROM, the following occurs: U4050, pin 12, is low during a probe access period and when ALE is high. This low is clocked through U4045 with the rising edge of the 3-MHz clock. The low from U4045 holds pin 35 of U3050 low, which causes the Microprocessor to add a wait state to the cycle. Then, the /READY line goes high, another wait state is added, and the regular cycle is completed. The /READY line goes high in this instance after one cycle, because U4050 pin 12 goes high when ALE goes low, and the 3-MHz clock signal clocks the line low.

When read or write access to the Display RAM is required, the /READY line is low. This input initiates a processor wait cycle until the Display Access period is complete. When the Microprocessor is adding wait states, the EXT BUS EN line must be enabled for the added wait periods. This is done by the /READY signal at pin 9 of U3080 (SØ), the Two-clock Delay Register. U3080 is a four-bit shift register. The parallel inputs, pins 3, 4, 5, and 6, are wired to +5 V and ground such that each time the register is loaded, it loads a binary 1100 into the four cells. The S1 input to U3080, which is the other mode control input, is connected to the ALE signal from pin 14 of buffer U4070A.

Refer to Fig. 2-26, which is a timing diagram of signals in the CPU circuits. To begin, both /READY and ALE must be high in order for the shift register to parallel-load. When this occurs, 1100 is loaded into U3080, and the output, pin 12, moves low. This enables the Address Select Gate, U4040. The ALE signal, which is only one-half clock period in width, goes low immediately. At the next positive edge of the 3-MHz CLK signal, either of the following can occur: **1)** If the /READY signal is low because of a display cycle, the register will be in a hold state, and no shifting will occur; **2)** If the /READY signal is high, the high state stored in the shift register will be clocked out of the register following two clock excursions, and U4040 will be disabled after the two clock cycles. Note that, except during I/O operations, the IO/M signal is low, which enables the other input to gate U4040. Thus, the access period from the Data Bus that is external to the CPU is two clock cycles plus the number of wait states (one if probe access is required, and one or two during Display access). Refer to Table 2-17, which lists the states of the Wait-State Generator.

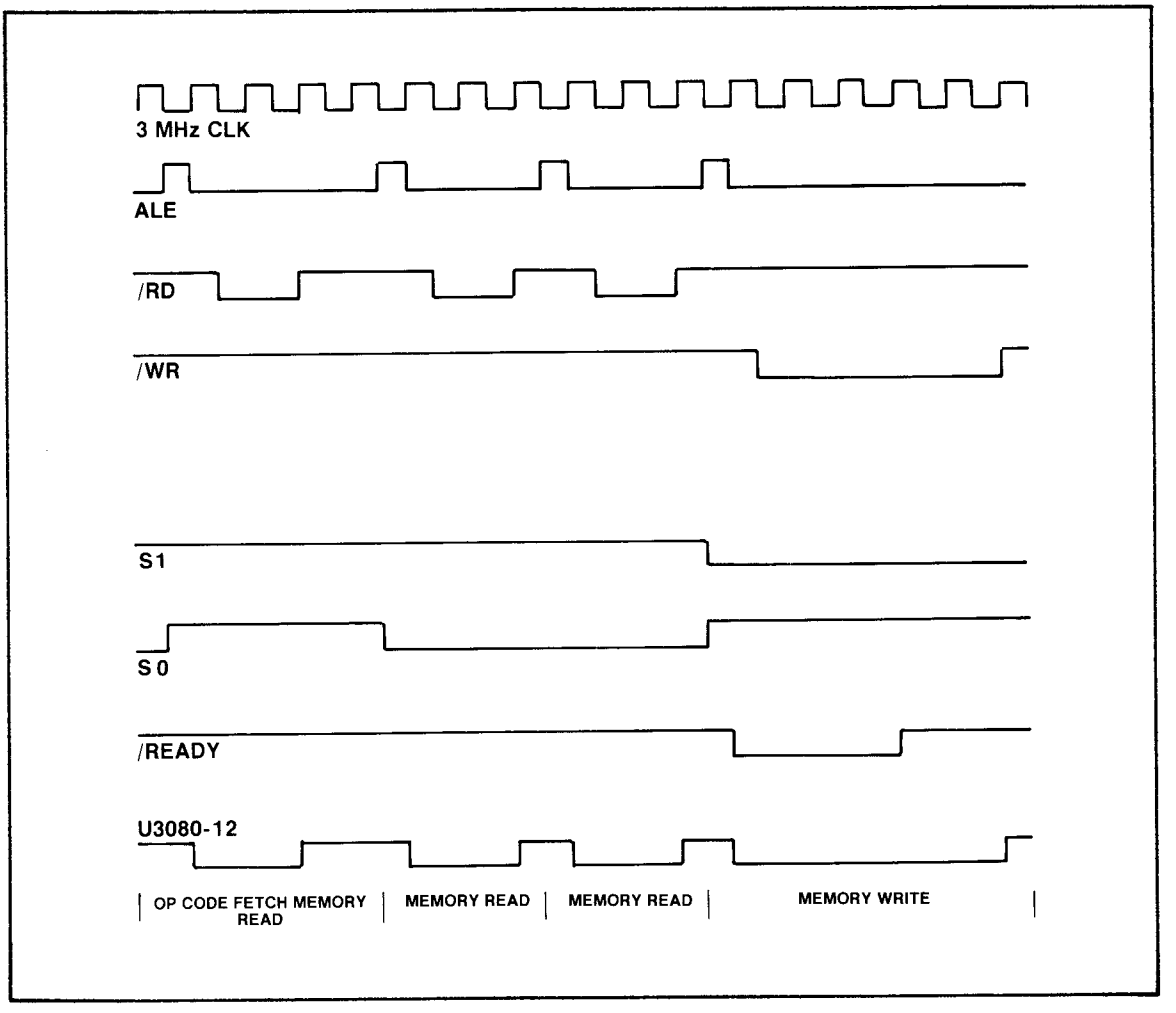


Fig. 2-26. CPU Circuit Signals Timing Diagram.

TABLE 2-17
Wait-State Generator Truth Table

S1(ALE)	SØ(READY)	FUNCTION
low	low	Hold
low	high	Shift Right
high	low	Shift Left (not permitted)
high	high	Load

Interrupt Timer. This circuit consists of timer U1030 and transistor Q1037. The circuit generates a 30-uS pulse that interrupts the Microprocessor at a rate of approximately 30 Hz. The Microprocessor, with each interrupt, scans the keyboard and updates the cursor. The jumper in the collector circuit of Q1037 permits the interrupt timer to be disabled for troubleshooting purposes.

Selection Logic Circuits

The 7D02 memory is divided into eight segments, each of which can hold 8K bytes of data. The division is done by decoder U4040, which decodes the A13, A14, and A15 bits from the Microprocessor into eight select lines. See Table 2-18, which depicts the memory map. The YØ through Y5 select lines are used to select one of the six ROM stages depicted on Diagram 9B (U3010, U3020, U3030, U4010, U4020, and U4030), which contain the firmware for the 7D02. The Y6 line of U4040 enables U1080 (Diagram 9B also), which decodes the RAM select addresses. The Y7 line enables external bus operation. (External bus, in this context, means exterior to the CPU Board.)

TABLE 2-18
CPU Memory Map

Page Address Range	Capacity	Use
ØØØØ-BFFF	48K	Program ROM
CØØØ-DFFF	8K	RAM
Ø:EØØØ-Ø:EFFF	4K	Display
Ø:FØØØ-Ø:FFFF	4K	Latches
1:EØØØ-1:EFFF	4K	State Machine
1:FØØØ-1:FFFF	4K	Word Recognizer
2:EØØØ-2:EFFF	4K	Acq Memory
2:FØØØ-2:FFFF	4K	Timing Option
3:EØØØ-3:FFFF	8K	Probe ROM

Flip-flops U4045B, U4065A, U4065B, plus U4050B and U4055D form the Page Select circuit, which drives decoder U4080. The page selection principle increases the effective address space used for addressing the hardware. The three high-order address bits (A15, A14, and A13) are applied through U4050B to enable U4080. Bit A12 and the two page-select lines are decoded to overlay the hardware enable lines, YØ through Y7, from U4080. Page select occurs as follows: The selection code is applied from the CPU, via

the DØ and D1 lines, through address buffer U2080. (R3073 is used for test purposes, as is discussed later; it is a set of zero-ohm resistors in a chip.) When the Microprocessor is ready to set the address, an output occurs, which clocks U4045B with a positive transition on the /WR line. The resulting positive edge from the output of U4045B clocks both segments of U4065, applying the select data to U4080. SØ or S1 is then set low by the Microprocessor, so by way of U4055D, the decoder is gated on and the outputs of U4080 are enabled.

On power-up, the Page Select Register is set to zero. Any I/O output latches the two lowest data bits (DØ and D1) into U4065, and sets the I/O page into U4080. This page number is stable until another output changes the page, or until the CPU is reset. Following the page selection, any memory reference to EØØØ-FFFF will select only the devices related to that page.

Memory Circuits

Refer to Diagram 9B. The 7D02 ROM consists of six 8K by 8 ROM units. These are U3010, U3020, U3030, U4010, U4020, and U4030. The 7D02 RAM section consists of sixteen 1K by 4 RAM units. These are U1040 through U1075 and U2040 through U2075.

Refer to Diagram 9A. Since the low-order address and the data from U3050 are multiplexed from the same lines (ADØ-AD7), U3065 is used to hold the low-order address bits stable for the full duration of the memory access cycle. The bits are latched into U3065 on the falling edge of the ALE signal. The lower four high-order address bits and three control signals are sent through U4070A for buffering before being applied to the Main Interface Bus (which is internal to the 7D02).

Data sent out from U3050 are sent through U2080 for application to the Main Interface Bus (U2080 is enabled by S1.) Data read from the Main Interface Bus are applied through buffer U4075, from which it is presented to the Internal Interface Bus (which directly accesses the Microprocessor). Circuit U4075 is gated by the /RD and /EXT BUS ENABLE to permit the passage of data from the Main Interface Bus to the Internal Data Bus.

When installed in the 7D02, zero-ohm resistor pack R3073 connects the Microprocessor to the External Bus. To break this connection, R3073 is removed from its socket, and another, 4.7 kOhm single-in-line package, is installed instead. This unit forces the Microprocessor to execute a fixed and continuous cycle of instructions that cycles the address bus and data bus for signature analysis purposes.

DISPLAY CIRCUITS

Introduction

Refer to Fig. 2-27, which is a simplified block diagram of the Display circuits. The Display circuits can be considered as simply a RAM and an address counter, with a processor-to-RAM interface, a data interface, and an address-to-mainframe interface.

The RAM contains a coded copy of what is to be put on the display. The information is stored in the form of a modified 7-bit ASCII character set, such that the standard ASCII control and lower-case characters are altered in this case to be graphic characters. The most significant bit (MSB) of the 8-bit RAM location indicates whether the character is to be

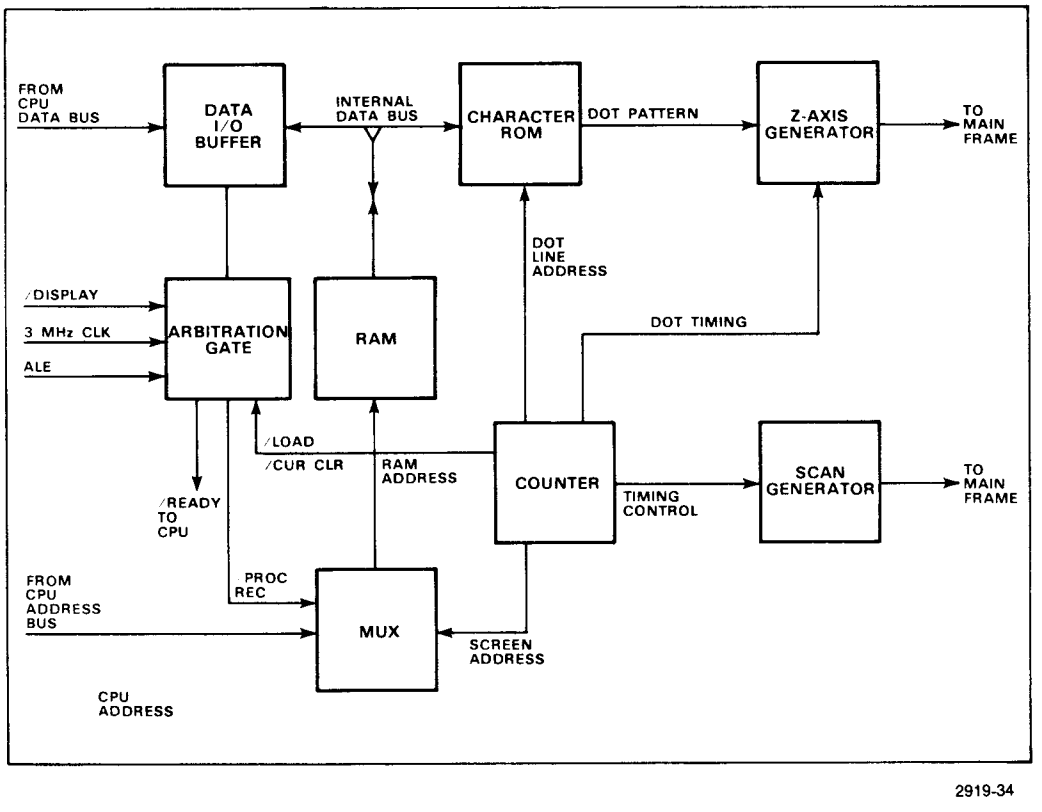


Fig. 2-27. Display Circuits Simplified Block Diagram.

The display codes are sent through the Data I/O Buffer from the Processor to the RAM. The code is then read back out of the RAM by the Counter. The code is interpreted by the Character ROM, and the appropriate dot representation is sent to the Z-axis Generation circuits, which convert the data into serial-by-bit format, then send the data on to the Mainframe Z-axis circuits. Normally, the Counter constantly counts through the RAM to refresh the display at approximately 60 times per second.

During CPU access time, the Multiplexer switches control of the RAM address from the Counter to the CPU, and the I/O Bus Buffer is activated for a read or write operation of the Display RAM. The Arbitration Gate, using CPU and counter-derived signals, blocks CPU access during display access time.

The Scan Generator circuit produces a ramp for the vertical and horizontal sweeps. The display screen is scanned by a full raster that begins on the top-left corner of the screen and moves to the right and towards the bottom. The Display Counter circuits trigger the start and stop of both the horizontal and vertical scan signals. The Scan Generator produces a ramp signal for the horizontal scan, and a staircase signal for the vertical scan.

The scan consists of an array of dot positions, made up of 256 dots per line and 216 lines of dots. Characters consist of dot arrays that are 9 lines high and 8 dots wide. Thus, there are 24 character rows on the display, each of which can contain 32 characters. Refer to Fig. 2-28, which illustrates the dot arrays that form the characters.

Refer to Fig. 2-29, which is a block diagram that represents Diagram 10A, the display counter and logic circuits. The 3.4133-MHz oscillator produces the master dot clock signal for the Display circuits, having a 293-nS period. The oscillator signal is fed to the Divide-by-eight Dot Counter to be divided to an approximate 2.3-uS period, to the Timing Generator to synchronize its outputs, and to the Character Line Shift Register and Z-axis Output circuit, to be discussed later in the Display Z-axis Logic Circuit description.

The output of the Divide-by-eight Dot Counter is fed to the Timing Generator and the Divide-by-thirty-three Character Counter. The Timing Generator produces five pulse trains, each of different phase, for timing the various display control circuits. Some of these signals are also applied to the Arbitration Gate in the Display Z-axis Control circuits to control

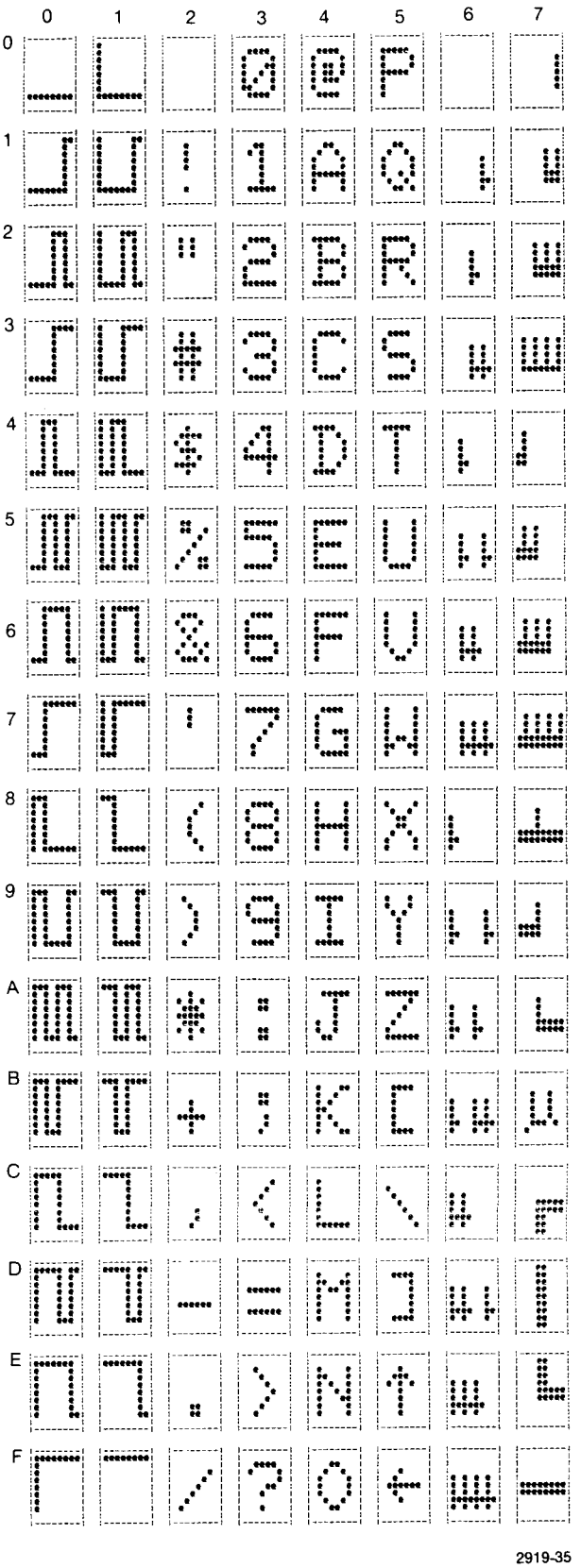


Fig. 2-28. Character Dot Arrays

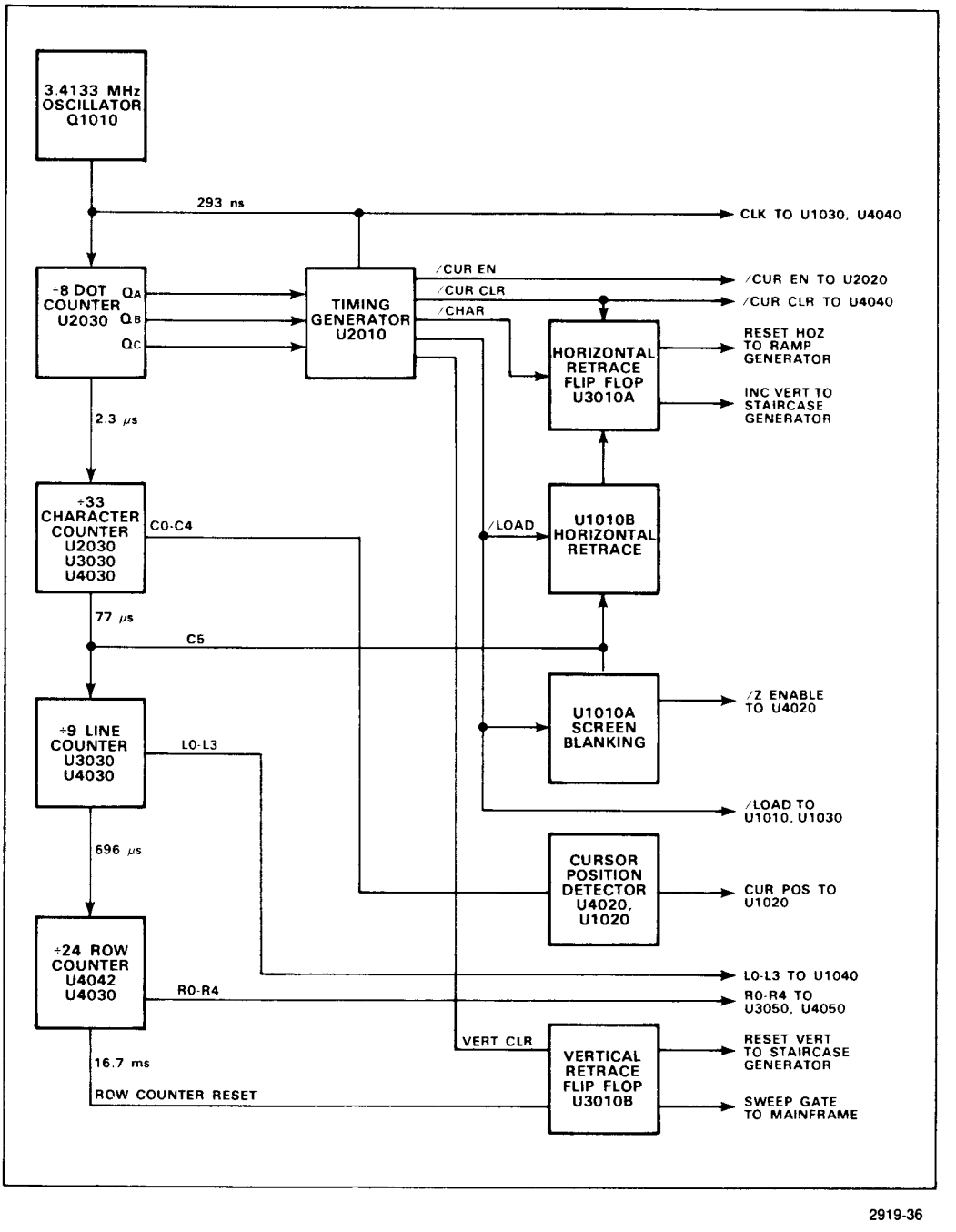


Fig. 2-29. Display and Control Logic Circuits Block Diagram

the CPU access to the Display RAM. The Divide-by-thirty-three Character Counter produces the CHØ through CH4 signals, which are used by the Cursor Position Detector to locate the cursor to address the current display character, and the CH5 signal, which resets the Horizontal Retrace and Screen Blanking Circuits.

The CH5 signal is also applied to the Divide-by-nine Line Counter. This stage produces the LØ through L3 signals, which address the dot line (in the Character ROM) of the character to be displayed. The L3 output of this stage (approximately 696-uS period) is applied to the Divide-by-twenty-four Rows Counter. The ROWØ through ROW4 lines from this stage are applied to the Display RAM to specify the row that is to be displayed. The Row Counter Reset, at a period of about 16.7 mS, is applied to the Vertical Retrace Flip-flop, which is used to reset to Staircase Generator at the end of each display frame.

The Horizontal Retrace circuit, which is driven by the Timing Generator and the CH5 signal, resets the Ramp Generator, and increments the Staircase Generator. The Screen Blanking circuit applies the /Z ENABLE signal to the Z-axis circuits to blank the display during horizontal retrace time. The Cursor Position Detector decodes the CHØ through CH4 signals, determines the position of the cursor, and sends a pulse to the Z-axis control Logic circuits, depicted in Fig. 2-30. The Vertical Retrace Flip-flop, using the VERT CLR and ROW COUNTER RESET signals, supplied the SWEEP GATE signal to the Mainframe, and the RESET VERT signal to the Staircase Generator, to reset the staircase signal at the end of each display.

Refer to Fig. 2-30, which is a block diagram of the Display Z-axis Control Logic circuits, depicted on Diagram 10B. The Arbitration Gate produces the /READY signal, and under direction of the CPU circuits, controls the RAM Control Multiplexer circuit. The Arbitration Gate decides when the CPU will have control and access to the Display RAM. The RAM Control Multiplexer switches the data and control signals (ROWØ-ROW4, CHØ-CH4, AØ-A9, etc.) to drive the Display RAM. Through the Processor I/O Buffer, the CPU reads data from or writes data into the RAM. Data from the RAM is applied to the Character ROM, which looks up the row dot patterns for each character. These dot patterns are fed to the Character Line Shift Register, which changes the serial-by-character data to serial-by-bit data.

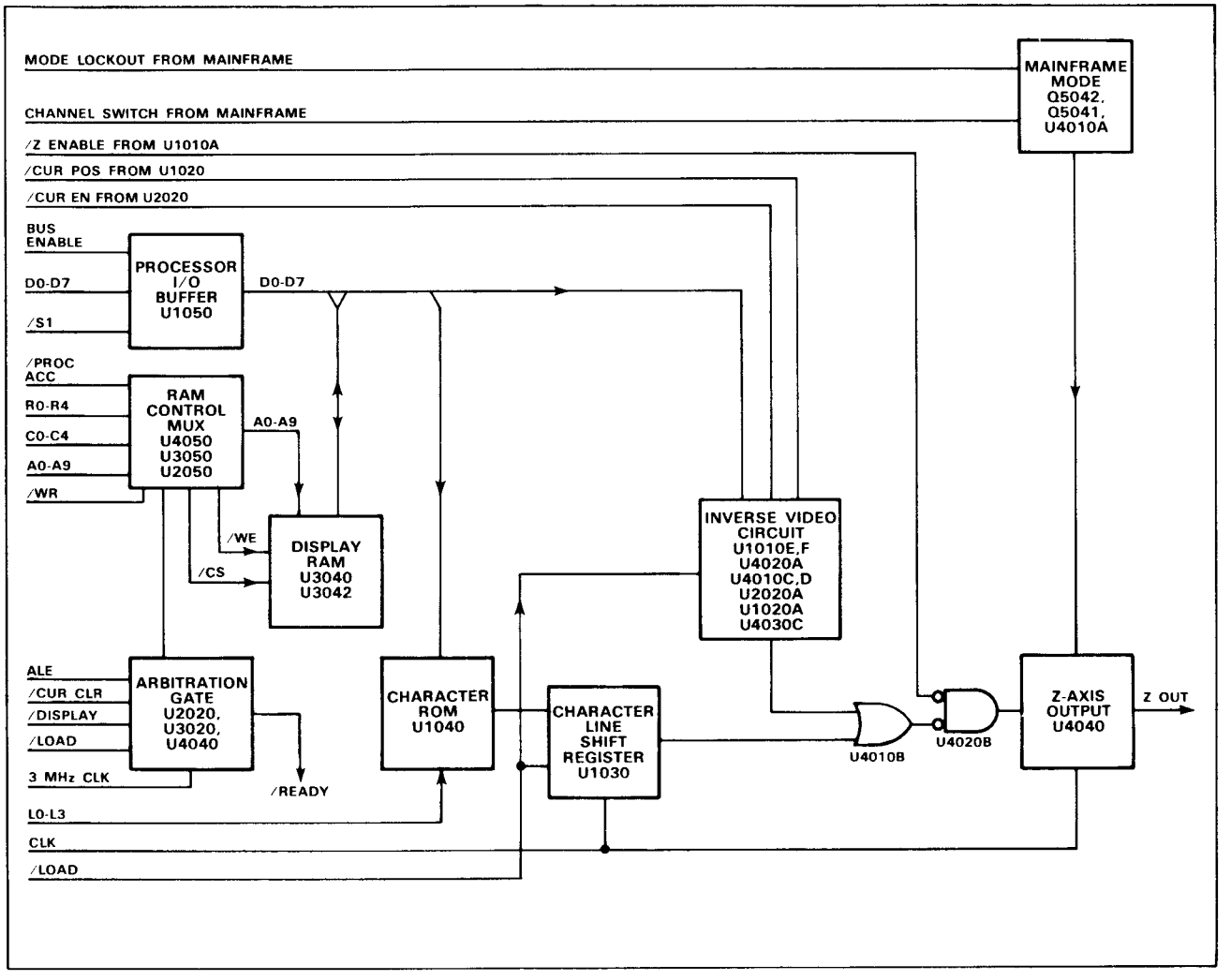


Fig. 2-30. Display Z-axis Control Logic Circuits Block Diagram.

From the Character Line Shift Register, the data are then fed into an exclusive-OR gate, which is controlled by the Inverse Video circuits. These determine if inverse video is required for a character, cursor character, or line. The output of this gate is fed through the enabling gate that is controlled by the /Z ENABLE signal. This blanks the display for one character following each set of 32 characters. The final output is through the Z-axis Output circuit, which shapes the output pulse, and allows the Mainframe Mode circuits to control the signal passage, if required. This output signal is fed to the Display Z-axis Drive circuits, to be discussed in the following paragraph.

Refer to Fig. 2-31, which is a block diagram representation of the Display Axis Drive Circuits, depicted in detail on Diagram 10C. The TTL SWEEP GATE signal from the Vertical Retrace Flip-flop is amplified by the Sweep Gate Buffer and applied to the Mainframe to unblank the display when required. The Z OUT signal from the Z-axis Output circuit is applied to the Z-axis Driver circuits, to be amplified and applied to the Mainframe Z-axis circuits to modulate the display. The RESET VERT signal is applied to the Holdoff Buffer circuit, from which the signal is applied to the Mainframe Horizontal Drive circuits.

The RESET VERT signal is also applied to the Staircase Generator, where it is used to reset the generator at the end of a complete display cycle. The /INC VERT signal is also applied to the circuit, and is used to increment the staircase signal at the end of each line of characters. The VERT POS signal is injected at the amplifier to offset the display, as necessary, and the signal is amplified and converted into differential drive signals, VERT SIG + and VERT SIG -, which are then applied to the Mainframe Vertical circuits.

The Ramp Generator, which consists of the Discharge Gate, the Current source, Amplifier, and Output Amplifier, generates the ramp that drives the mainframe horizontal circuits. The RESET HOZ signal from the Horizontal Reset circuit is used to reset the generator at the end of each display sweep. The HORIZ POS signal is injected at the Amplifier stage to offset the display horizontally, as necessary. The Output Amplifier divides the signal into differential drive signals, HORIZ SIG + and HORIZ SIG -, which are then applied to the Mainframe Horizontal Deflection circuits.

Detailed Description

Refer to Diagram 10A, which is the schematic diagram for the Display Counter and Logic circuits. These circuits form the master timing section for the Display board.

3.4133-MHz Oscillator. This stage controls the rate at which the Z-axis is modulated. Each dot is visible on the screen for a period of 293 nS, which is the oscillator signal period. The principal components of the oscillator are Q1010 and Y1015. These and related components form a transistor Colpitts oscillator. The oscillator output is fed through buffer U2020F and distributed to U2020C, U2010, U1030 and U4040B.

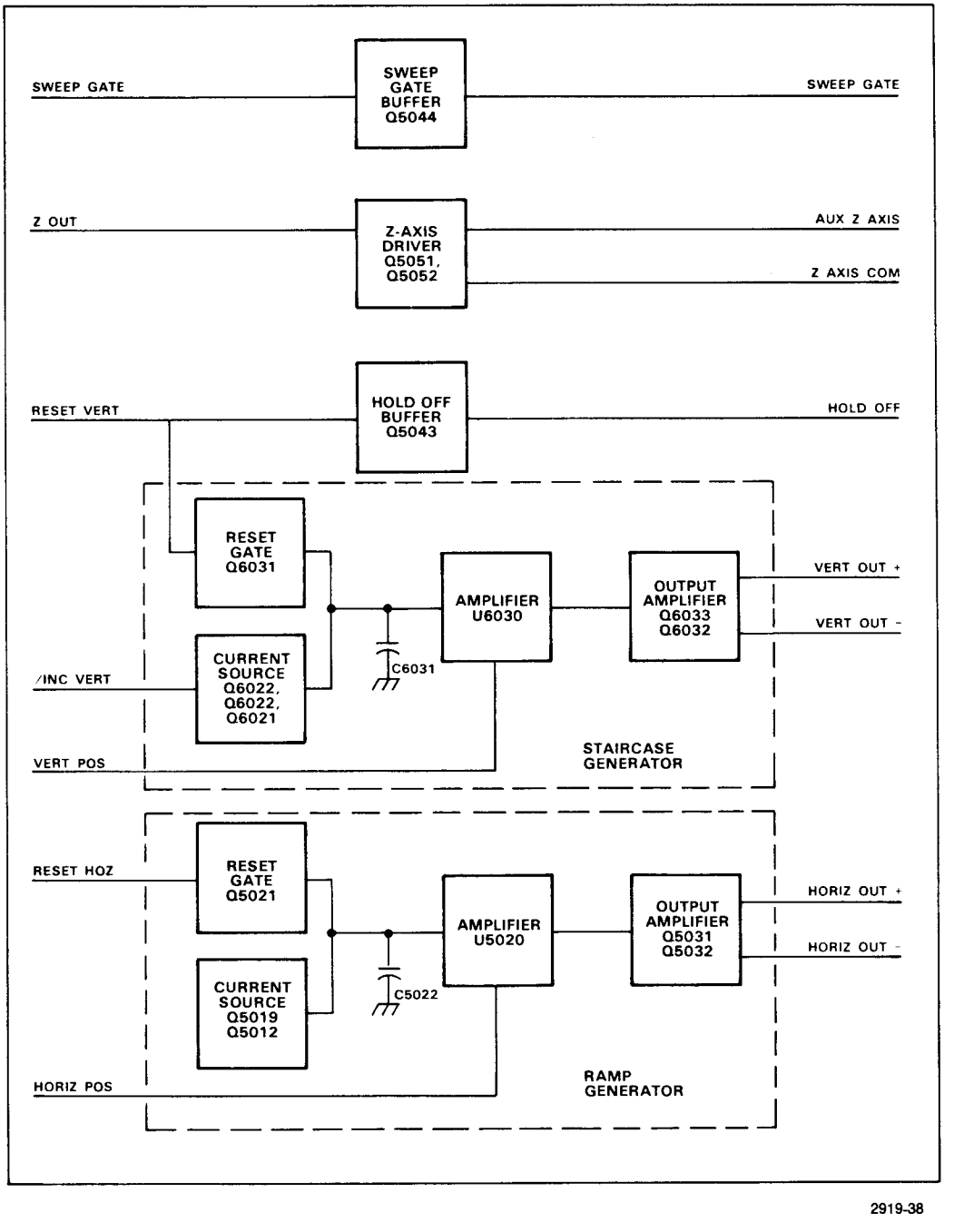


Fig. 2-31. Display Axis Drive Circuits Block Diagram

Divide-by-eight Dot Counter. This stage consists of a three-cell binary counter U2030B. The /CLK signal from U2020C is fed to this stage, where the signal is divided by two, four, and eight. The three outputs are sent to U2010, the Timing Generator, to be discussed later. The Q_C output from pin 9 is sent to the clock input of U2030A, part of the Divide-by-thirty-three Character Counter.

Divide-by-thirty-three Counter. This circuit consists of four-cell counter U2030A, two-cell counter U3030B, and U4030B. The circuit counts up to 32, at which point pin 10 of U3030B goes high. When pin 3 of U2030A goes high at the 34th count, U4030 resets the circuit, and it begins the count from Ø once again. Figure 2-32 illustrates the idealized waveforms at the output of the counter. Note that when the CHØ signal moves positive, AND-gate U4030B immediately resets all counter cells to zero, which causes a very short pulse to appear on the CHØ line at the beginning of each count cycle. The ChØ-CH4 outputs of the counter are applied to RAM Control Multiplexer U2050 and U3050 on Diagram 10B, where the signals are used to address character codes that are stored in the RAM by the CPU. Lines CHØ-CH4 are also applied to the Cursor Position Decoder, which consists of U4020D and U1020. Line CH5 is fed to U1010A and U1010B, which are discussed in subsequent paragraphs, and to the Divide-by-nine Line Counter.

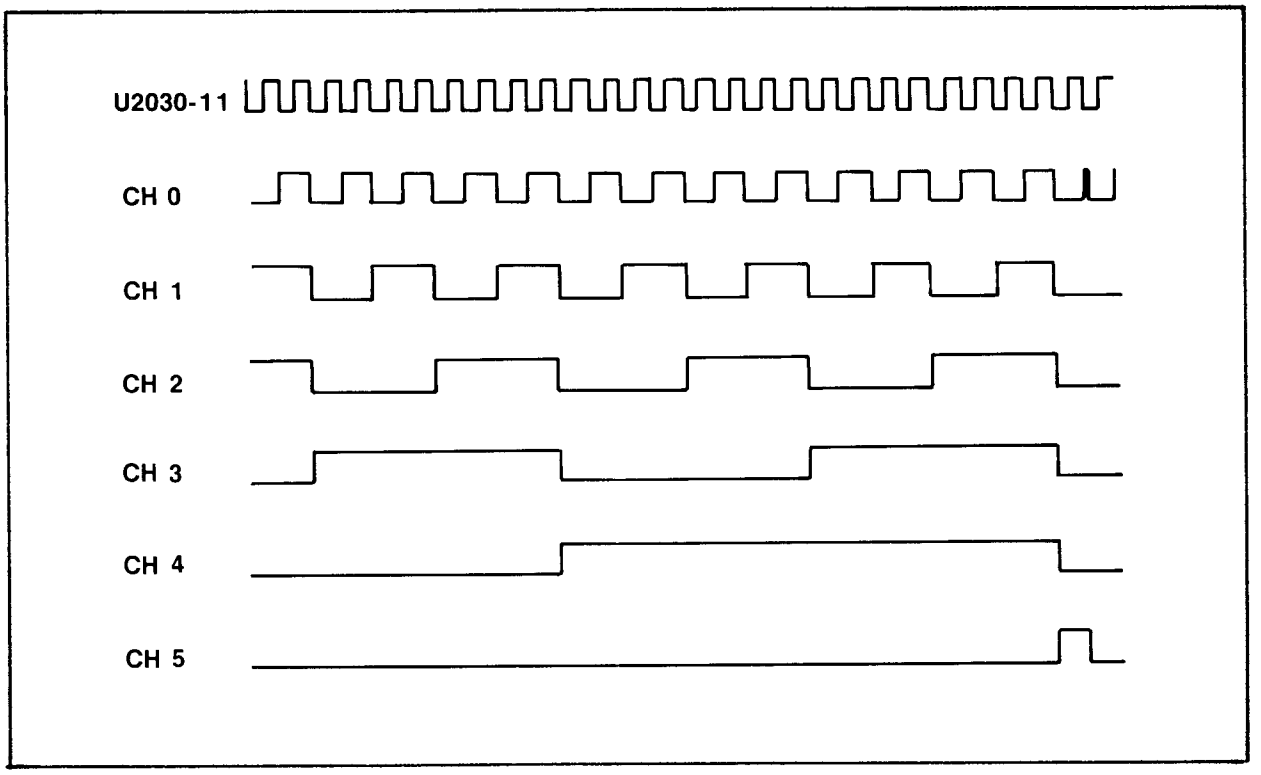


Fig. 2-32. Divide-by-Thirty-Three Character Counter.

Divide-by-nine Line Counter. This stage consists of four-cell binary counter U3030A and U4030D. As illustrated in Fig. 2-33, the stage counts up in a binary sequence until output lines LØ and L3 move high. At this point, the counter resets itself and resumes the ordinary binary count. Lines LØ-L3 are applied to the Character ROM, where the lines are used to specify the dot line of an addressed character to be displayed. The L3 line also connects to the clock input of the Divide-by-twenty-four Row Counter.

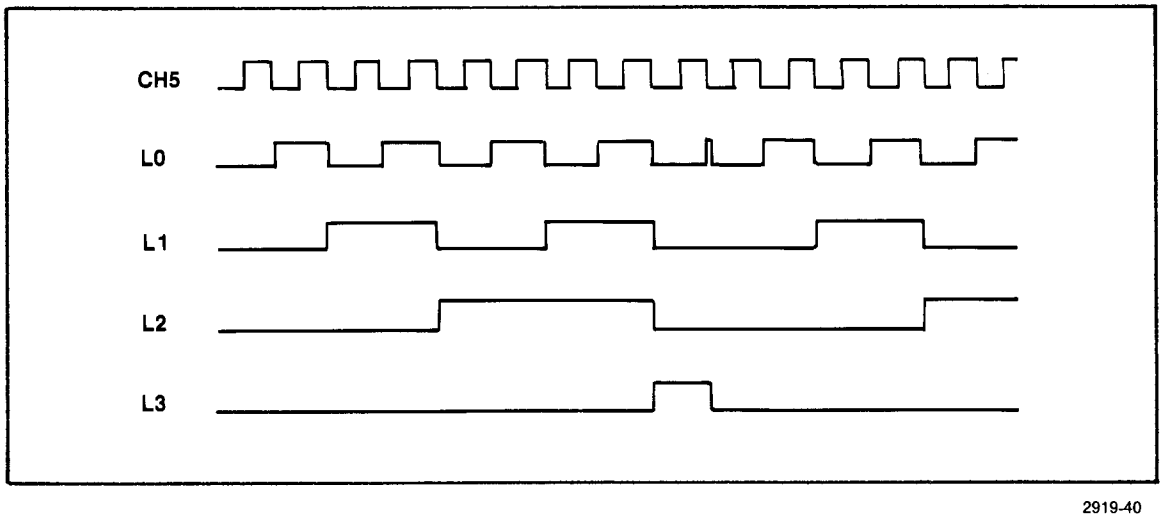


Fig. 2-33. Divide-by-Nine Line Counter Waveforms.

Divide-by-twenty-four Row Counter. This circuit consists of four-cell binary counter U4042B, AND-gate U4030A, and single-cell counter U4042A. The two counters form a simple divide-by-thirty-two counter until the ROW3 and ROW4 lines move high. At this point, AND-gate U4030A resets the circuit, and the circuit begins to count up from zero once again. The result is a divide-by-twenty-four counter, as illustrated by the idealized waveforms in Fig. 2-34. The ROWØ-ROW4 lines are sent to the Display RAM (U3050 and U4050), and used to address the character codes stored in the RAM. The output of U4030A is connected to the clock input of Vertical Retrace Flip-flop U3010B, where it is used to clock U3010B at the end of the last sweep in the display.

Timing Generator. This stage consists of U2010, a three-line to eight-line decoder. The decoder is fed the three outputs of U2030B, the Divide-by-eight Dot Counter, and produces eight output pulses that are different in phase from one another. (The second, third, and seventh of these pulses are not used.) Figure 2-35 illustrates the timing relationships

of the input and output signals. The /CHAR signal from the YØ output is used to clock the Horizontal Retrace Flip-flop, U3010A, at the end of each 32 characters.

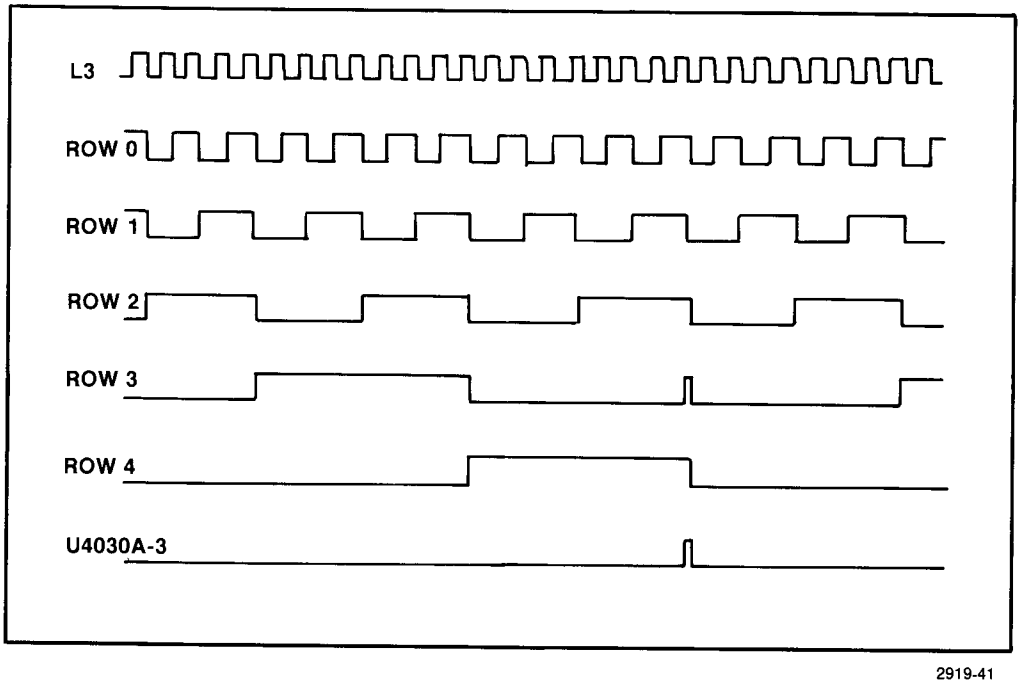


Fig. 2-34. Divide-by-Twenty-Four Row Counter Waveforms.

Screen Blanking. Flip-flop U1010A is clocked by the /LOAD signal from the Timing Generator, which recurs at approximately every 2.3 uS. The flip-flop remains reset until the CH5 signal moves high, which only does so at 77-mS intervals, or at the end of every 32 characters. Thus, during the 33rd character space, /Z ENABLE is high to blank the display during horizontal retrace time.

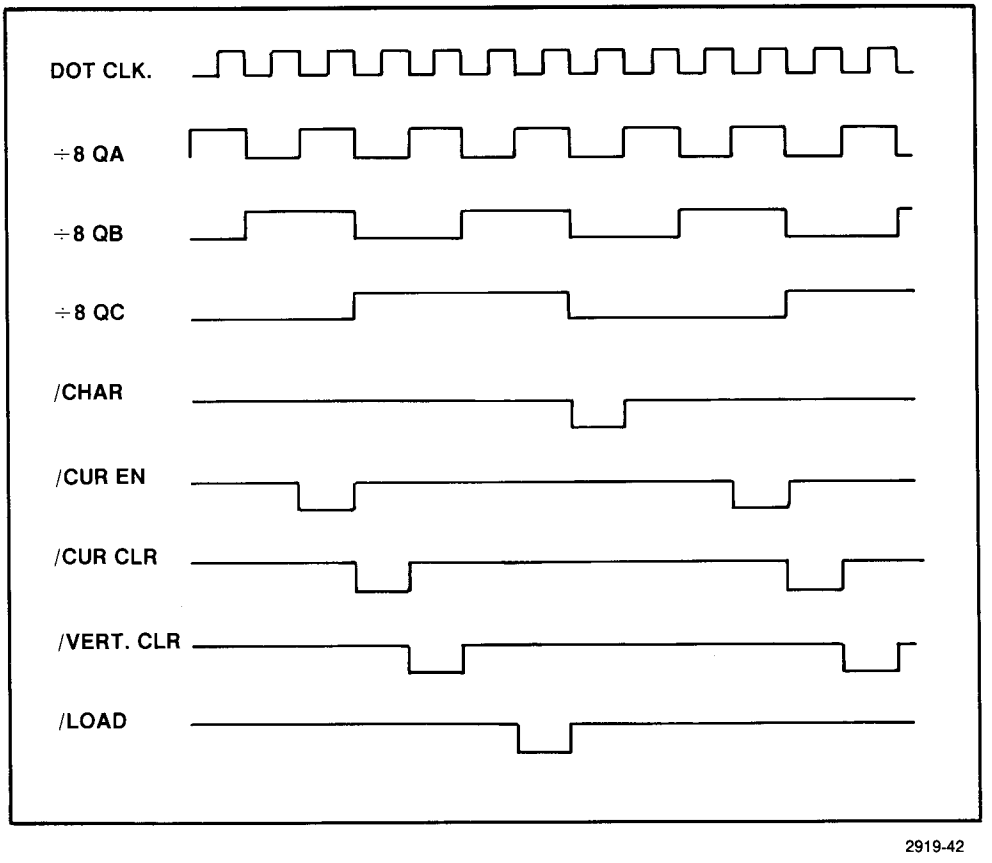


Fig. 2-35. Timing Generator Input and Output Signal Timing

Horizontal Retrace Circuits. Flip-flops U1010B and U3010A form this circuit, which produces the signals to reset the Ramp Generator and increment the Staircase Generator for the next horizontal sweep. Flip-flop U1010B stays in the reset condition until the end of a character count, when line CH5 goes high for a short time. The /LOAD signal from U2010 occurs at a rate that is 33 times faster than CH5, and clocks U1010B during the high state of CH5, passing the high to U3010A. Approximately 5 uS later, the /CHAR signal clocks the high state into U3010A, RESET HOZ goes high and /INC VERT goes low. This causes the Ramp Generator to reset and prepare for the next sweep, and the Staircase Generator to increment to the next lower level on the display. Approximately 5 uS later, the /CUR CLR signal from U2010 resets U3010A, preparing it for the next cycle. In the meantime, the CH5 line has gone low and /LOAD has reset U1010B.

Vertical Retrace. This circuit, which consists of latch U3010B, operates as does the one just previously described, except at a slower rate. Initially, U3010B is reset. At the termination of a complete display

cycle, that is, after the display is scanned, the Divide-by-twenty-four Counter output from U4030A clocks a high at the output RESET VERT line, which resets the Staircase Generator. The SWEEP GATE signal at the other output moves low to blank the display during the reset period. A few microseconds later, the /VERT CLR signal once again resets U3010B.

Cursor Position Decoder. This circuit consists of U1020 The CHØ through CH4 signals are applied to this circuit, which produces a low level at its output whenever the character address is equal to binary 10001. This low signal is used by the logic circuits, to be discussed later.

Display Z-axis Control Logic Circuits

Refer to Diagram 10B, which is the detailed schematic diagram for the Control Logic and Memory sections of the Display Board.

Arbitration Gate. This circuit consists of Inverter U2020B, plus latches U3020A, U3020B, and U4040A. The purpose of the Arbitration Gate is to compensate for the timing disparity between the 3-MHz CLK signal and the 3.4133-MHz DOT CLOCK signal in the Display circuits, and thus to resolve when the CPU circuit can access the Display RAM. The signals that are based on the DOT CLOCK signal are /LOAD and /CUR CLR; the signals that are based on the 3-MHz CLK signal are /DISPLAY and ALE. Refer to Fig. 2-36, which depicts an idealized version of the waveforms that pertain to the circuit.

As noted in the introduction, the operating cycle is divided into the Display period (which is when the /DISPLAY SEL signal is high). At some time following the negative transition of /DISPLAY SEL the /LOAD signal moves low, then high, to clock a low state at U3020A pin 5, the /PROC ACC signal. (U3020A was previously set high by the /CUR CLR signal) The low /PROC ACC signal is applied to the RAM Control Multiplexer (U4050, U3050, and U2050), to switch the Multiplexer to the CPU access mode. (Placing the /PROC ACC signal low connects the A input group to the output; high connects the B input group to the output.)

Following the next positive excursion of the 3 MHz CLK signal, the output of U4040A moves low. This sets U3020B, and the /READY signal moves high, which ends the CPU wait cycle. Shortly thereafter, the /CUR CLR signal once again sets U3020A and U4040A. When the next ALE pulse occurs, concurrently with a low /DISPLAY SEL state, U3020B pulls the /READY signal low, starting another CPU wait state. The output of U4040A is also applied to U4020C, where it is used along with /EXT BUS EN to control U1050, the I/O buffer.

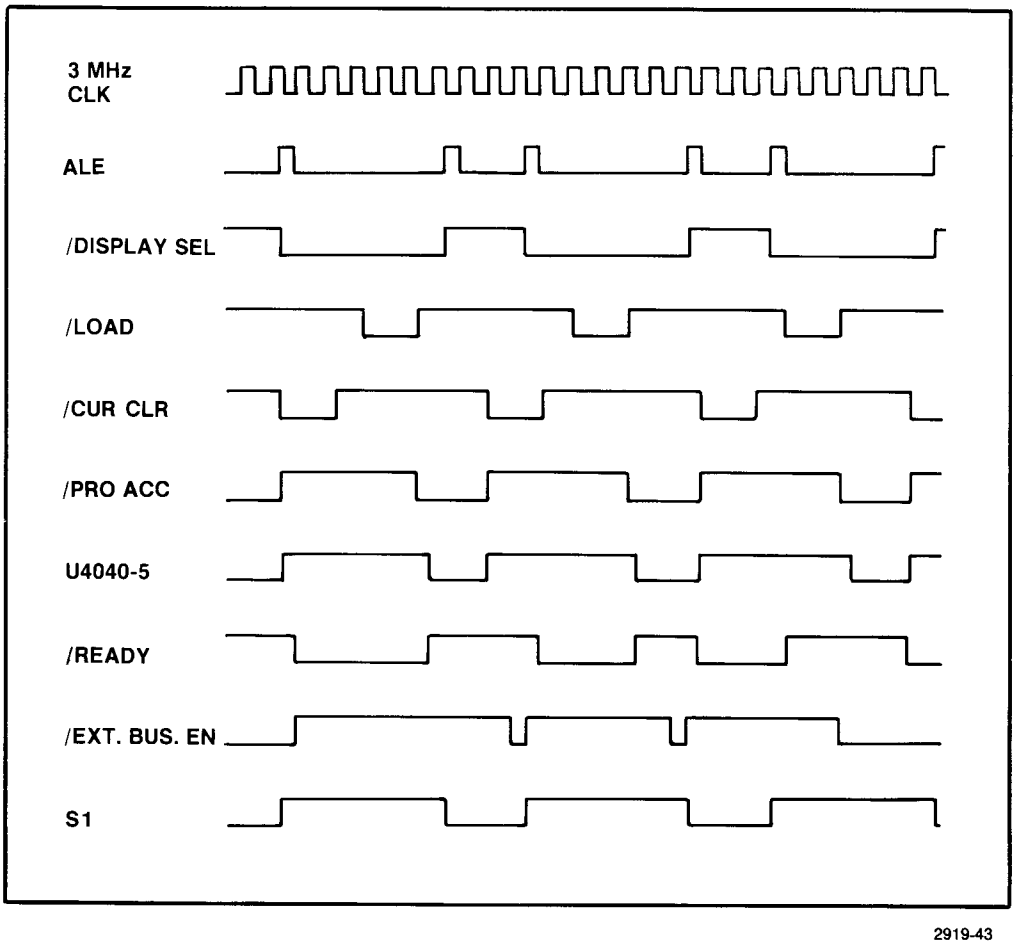


Fig. 2-36. Arbitration Gate Waveforms.

RAM Control Multiplexer. The Multiplexer consists of three distinct devices, U4050, U3050, and U2050. These devices switch the Display RAM address between the Character and Row (CHØ-CH4; ROWØ-ROW4) data from the Display Counter circuits and the Address Bus lines (AØ-A9) from the CPU.

As mentioned earlier when the CPU requires access to the Display RAM, it triggers the Arbitration Gate, which in turn produces the low /PROC ACC signal that switches the Multiplexer to give access to the CPU. The /WR signal from the CPU is used here to control /WE (Write Enable) input to the RAM. Control of this line permits selecting either a read or write function between the CPU and the Display RAM.

Processor I/O Buffer. This circuit consists of buffer U1050, inverter U2020D, and U4020C. When access to the Display RAM is required, the CPU gains this access by means of the Arbitration Gate, which enables U1050.

The Buffer is bidirectional, and is controlled by the S1 line through U2020A. When S1 is high, data are read from the Display to the CPU; when S1 is low, data come from the CPU to the Display devices.

Character ROM. The Character ROM (U1040) stores the dot patterns for all the character codes that are stored in the Display RAM. Character codes in modified ASCII format are applied to the Character ROM by the Display RAM. The appropriate dot line is chosen by the Dot Line Counter via the LØ through L3 lines. ROM data are loaded into the Character Line Shift Register once for each character on a scan line with the /LOAD signal from the master Timing Generator.

Character Line Shift Register. The Character Line Shift Register, U1030, shifts dot line data from the Character ROM in serial-by-bit format to the Z-axis circuit. The 3.4133-MHz DOT CLK signal sets the period that each bit is asserted while shifted out. After /LOAD moves high, the DOT CLK signal shifts the character data serially out of U1030, to pin 5 of U4010B, which is part of the Inverse Video circuit.

Inverse Video Circuit. This circuit consists of U4030C, U4010C and D, U4020A and D, U1010C and D, U1020 and U4020D. The four most significant bits from the Display RAM are applied to this circuit. In essence, these circuits form a decoder that determines when video inversion is to take place. The DD6, DD5, and DD4 bits are applied to U4010C, U4030C, U4020A and U1010D. This part of the decoder detects the bits that form the timing characters depicted in the first two columns and the seventh column of Fig. 2-28.

Since the 7D02 has a character-oriented display, inverse video information is often encoded in the character information. There are two cases in which an inverted video display occurs: a timing diagram, which is position-dependent; and alphanumeric data, which is not. The principal reason for the Inverse Video Circuit is to conserve the ROM space that would otherwise have been required to store all of the inverse possibilities. The circuit that is used here decodes the DD7 and timing characters to gate inverse video from the Character ROM output.

Timing character inverse video information includes the gating of a cursor that has fixed position in the display. When the cursor position (Character 17, /CUR POS) has been decoded and the fourth dot in the cursor position character (/CURS EN) is asserted, the Z-axis signal for the timing characters is inverted on pin 12 of U4010D. The alphanumeric characters

are inverted when data bit 7 (DD7) is high. If DD7 is high for timing characters (normally low) the display circuit will put out inverse-video timing diagrams. In this case, when the cursor position is decoded, the cursor will be inverted inverse video; that is, normal video.

The cursor position is decoded by U1020. Inverse video switching occurs in U4010B, and the timing diagram decoding occurs in U4010C, U4030C, U4020A. and U1010D. Inverse video alphanumeric selection occurs in U1010C; timing character selection occurs in U4010D and U4020D.

Z-axis Output Circuits. The video signal from U4010B is applied to U4020B, which is controlled at pin 5 by the /Z ENABLE signal from the Display Counter circuits. This signal is high at the 33rd character on each line, and low for the other 32. This blanks out the display during retrace of both the vertical and horizontal scans.

The signal from the output of U4020B is fed to latch U4040B, which synchronizes the Z OUT signal with the DOT CLK signal. Through Q5041, Q5042, and U4010A, the Mainframe Mode circuit, the Z OUT signal can be blanked by the Mainframe, if necessary. Refer to Diagram 10C, which is a schematic diagram of the Display Axis Drive circuits. These circuits consist of the Sweep Gate Buffer, the Z-axis Driver, the Holdoff Buffer, the Vertical Staircase Generator, and the Horizontal Ramp Generator.

Sweep Gate Buffer. The TTL SWEEP GATE signal from U3010B is applied to emitter follower Q5044, from which it is applied to the Mainframe circuits to control screen unblanking.

Z-axis Driver. The Z-axis Driver consists of transistors Q5051 and Q5052, plus related components. The transistors are connected in a single-ended current switch configuration, and provide isolation for the output Z-axis signals to the Mainframe.

Holdoff Buffer. This stage consists of transistor Q5043 and related components. The transistor is connected as an emitter follower, to isolate the Vertical Retrace Flip-flop from the Mainframe.

Vertical Staircase Generator. This circuit produces the vertical staircase that positions each scan line of the display. It consists of Discharge Gate transistor Q6031, Operational Amplifier U6030, Current Source Q6011, Q6022, and Q6021, and Output Amplifier Q6033-Q6032, plus associated components.

When /INC VERT from the Horizontal Retrace Flip-flop is high, Q6011 is conducting, which keeps Q6022 biased off. Because of the connection of Q6021, it acts as a diode placing the base of Q6022 at about +4.3 V. Then, when the INC VERT signal moves low (approximately three clock periods), Q6022 is biased on, and conducts through C6031. The conduction period of the transistor is very short, so the capacitor only takes on a small charge with each INC VERT pulse. This voltage is amplified by U6030, which also receives the offset from the VERT POS line. The output of the amplifer is applied to differential amplifier Q6033-Q6032. This stage furnishes the differential VERT SIG + and VERT SIG - signals to the Mainframe vertical circuits. At this point, each step is approximately 1.6 mV.

When the last line on the display is completed, the RESET VERT signal moves high for a moment, causing Q6031 to conduct, and discharging C6031. This brings the staircase voltage back to the beginning point. VERTICAL AMPLITUDE ADJUST R6011 sets the magnitude of each current increment, and thus the display size.

Horizontal Ramp Generator. The Ramp Generator produces the horizontal drive signal for the Mainframe horizontal circuits, in the form of a ramp that occurs at a 12,929-Hz repetition rate. The circuit consists of Discharge Gate Q5021, Current Source Q5019-Q5017, Amplifier U5020, and Output Amplifier Q5031-Q5032.

The RESET HOZ signal is normally low so Q5021 is biased off. Transistor Q5017 sets the bias on Q5019 at about +4.3 V, and R5013 sets the current through Q5019, which furnishes the current to charge C5022. The voltage at the pin 3 input of U5020 increases linearly until the RESET HOZ signal moves high. Then, Q5021 conducts, discharges C5022, and holds it discharged until RESET HOZ once again moves low. The ramp is amplified by U5020 and applied to the Output Amplifier.

Output Amplifier. Transistors Q5032 and Q5031 are connected as a differential amplifier. The output signals, HORIZ SIG + and HORIZ SIG -, are applied to the Mainframe interface to drive the Mainframe horizontal circuits. The DC level from the front-panel position control, on the HORIZ POS line, is applied to the summing point of U5020 to horizontally position the display, as necessary. The output signal is approximately 3 V p-p, measured across the outputs.

POWER SUPPLY

Introduction

The Power Supply circuits convert the +15-volt and -15-volt supplies from the Mainframe into the +5-volt and +3-volt regulated supplies (The actual voltages of the two supplies are +4.85 and +2.85. However, in this circuit description, the nominal voltages used are +5 and +3, respectively.) Overall efficiency of this circuit is approximately 83 percent. The converter consists of the +5-volt Driver, the +5-volt Power Output Stage, the +3-volt Driver, and the +3-volt Output Stage. Refer to Fig. 2-37, which is a block diagram of the Power Supply circuits.

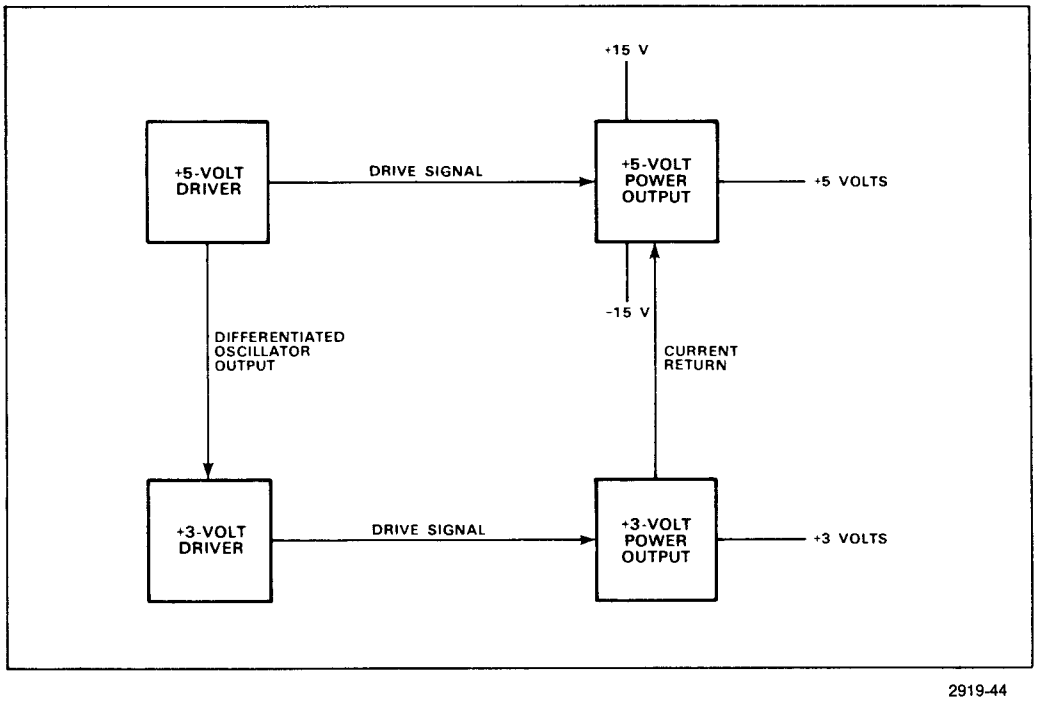


Fig. 2-37. Power Supply Circuits Block Diagram.

+5-volt Driver

The +5-volt Driver consists of Oscillator U3055C, Comparator U3055D, Ring Counter U2055, and the Base Driver, which consists of transformer T3037 and transistors Q1043, Q1049, Q1042, and Q1048

Integrated circuit U3055C and related components form the oscillator, which operates at a frequency of about 47 kHz. The oscillator output is applied to differentiator C3066-R4054, which shapes the signal into a triangular wave for application to U3055D and U3055B, to pin 13 of U2055B, and through CR3064 to pin 3 of U2055A. (CR3064 comes into operation only when the +5-volt supply has gone into current limit, to keep the Ring Counter operating.)

The Comparator stage consists of U3055D and related components. The +5-volt sense signal is applied through J211 pin 17B, through R3005, to one input of the Comparator. The combination of the differentiated oscillator output and the reference voltage from the +5-volt adjustment, R5065, is applied to pin 11. As the oscillator voltage and reference voltage combination crosses over the potential of the +5-volt sense line, the comparator output switches states. Refer to Fig. 2-38, which illustrates the comparator operation. Note that, as the dashed line (corresponding to the +5-volt sense line voltage) of the second waveform moves positive, the pulse duration of the third waveform changes. (Note that the waveforms in Fig. 2-38 are stylized and exaggerated for better illustration effect.)

The Comparator and Ring Counter form a pulse-duration modulated regulator. That is, by changing the duration of the positive and negative excursions of the drive signal to the output stage, the output voltage will also change. As mentioned earlier, the output of Comparator U3055D is a series of pulses that vary in duration, depending on the relationship of the two voltages at the inputs of U3055D. The upper half of the Ring Counter is clocked directly by the Oscillator output, so its output is in phase with that of the Oscillator. However, because of the changing pulse duration of the U3055D output signal, the output of U2055A, pin 1 is slewed in phase from that of U2055B pin 14. This is illustrated by the fourth and fifth lines in Fig. 2-38. The phase difference between the two Ring Counter outputs produces a current waveform composite that is similar to the idealized version at line six of Fig. 2-38.

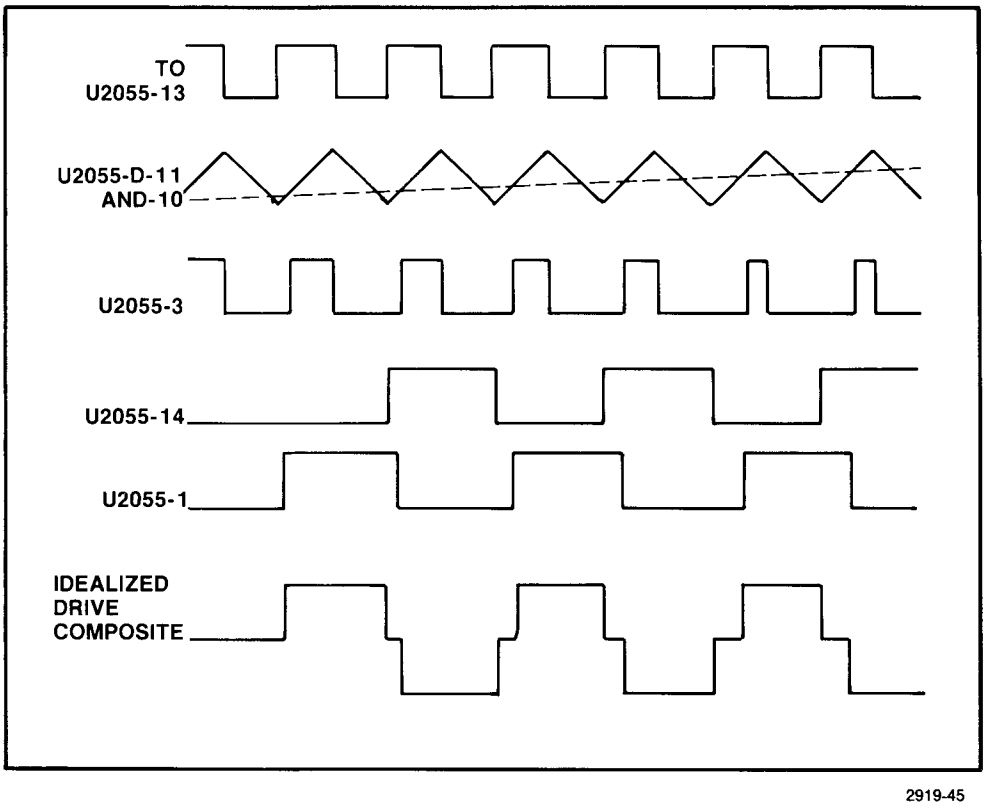


Fig. 2-38. +5 Volt Regulator during Normal Operation.

The Ring Counter section of the regulator is formed by the cross-coupling of JK flip-flops U2055A and U2055B. Figure 2-39 is an equivalent circuit of this stage, which can be considered as a pair of latches that are connected in cascade, then coupled back. Assume that, at the outset of operation, U1 is set and U2 is reset. Clocks Ø1 and Ø2 are slewed from one another, so U1 and U2 are never clocked simultaneously. As illustrated by the cross-connection, the two latches cannot make state transitions simultaneously.

In the actual circuit, the Ring Counter cells are preset in opposite states at turn-on by R3061-C2066. Because of the cross-coupling of the two flip-flops (similar in principle to the equivalent circuit in Fig. 2-39), the two stages alternate in output state with each clock pulse. The output signals are applied to the Driver Stage.

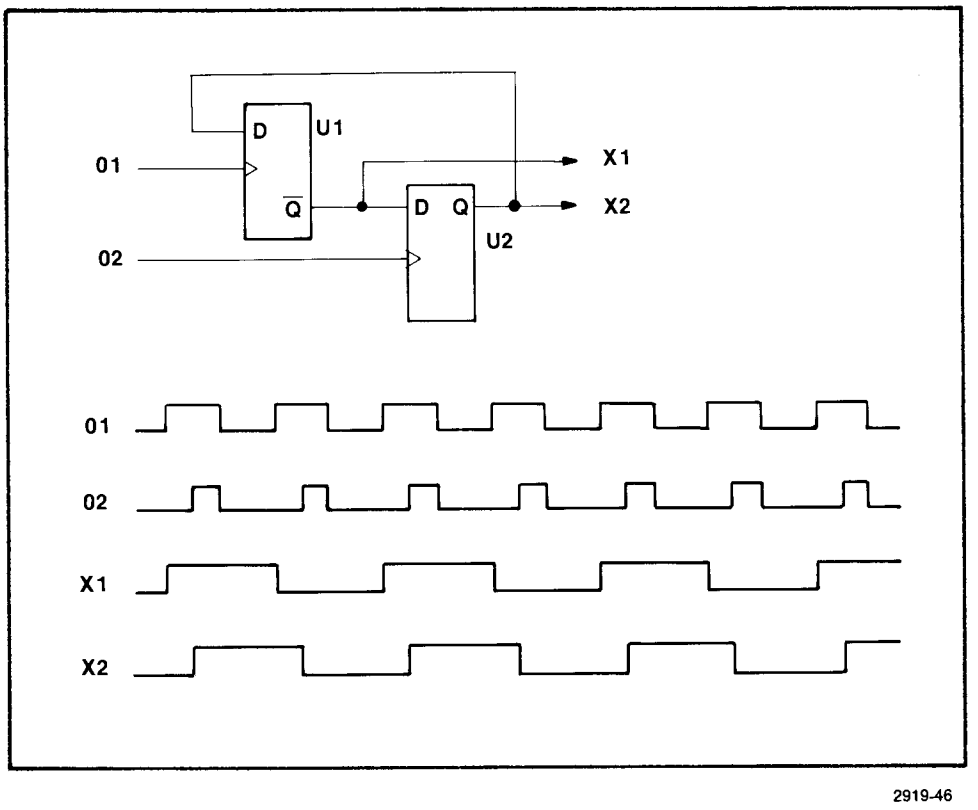


Fig. 2-39. Ring Counter Equivalent Circuit and Waveforms.

Returning to the Comparator section of the regulator, if over-current or over-voltage occurs, the potential at pin 10 of U3055D may rise to the point at which it remains more positive than the maximum excursion of pin 11, and the comparator will stop switching. Output pin 13 will be held low, and the Ring Counter will stop switching, since no clock will pass to the pin 3 clock input (See Fig. 2-40, which illustrates this action.) The stage will remain locked up until pin 10 of U3055D once again falls below the maximum positive excursion of pin 11, when the stage will resume normal operation. Note, however, that the above condition normally occurs during over-current conditions, but otherwise occurs only if a severe over-voltage condition exists.

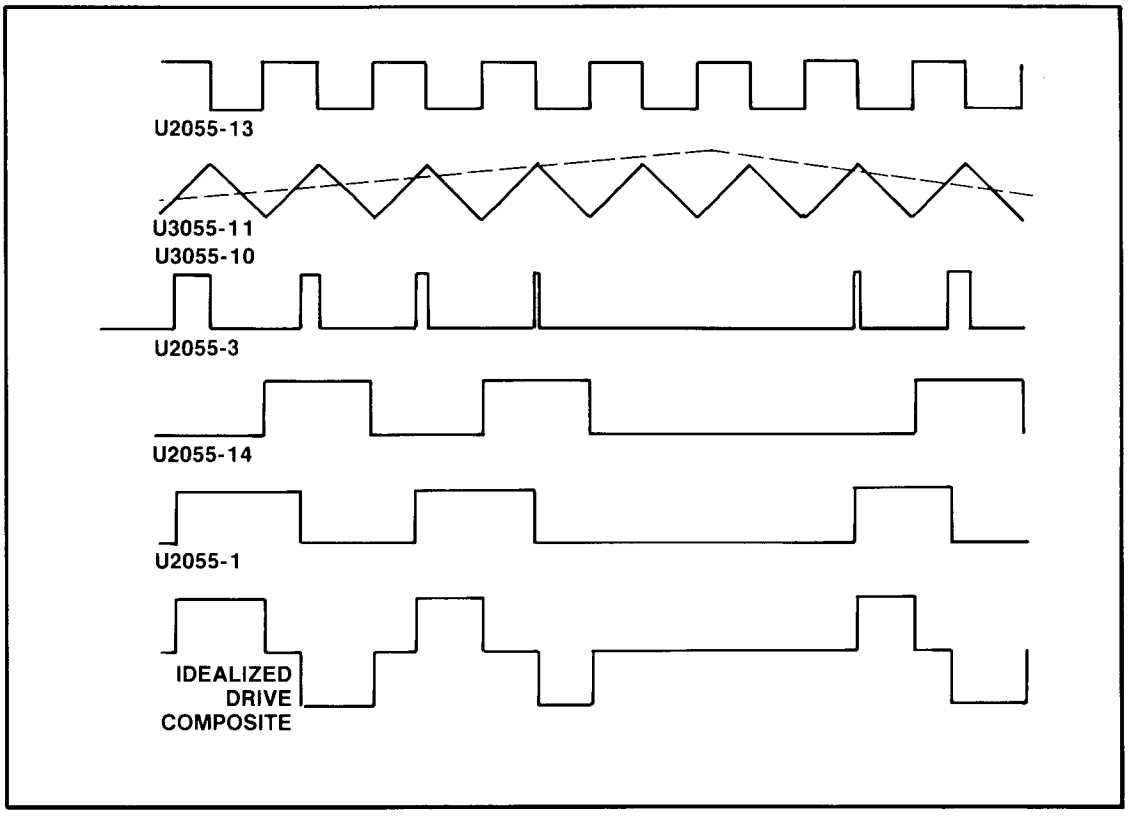


Fig. 2-40. +5 Volt Regulator during Overvoltage or Overcurrent.

If the output voltage falls to the point that U3055D is forced out of its operating range, the output of U3055D will rise positive. However, since the Comparator is an open-collector device, diode CR3064 couples the Oscillator negative transitions to the clock input of U2055A so that the Ring Counter will continue to operate at a fixed duty cycle Capacitor C3063 and resistor R3062 act to delay the clock impulse, allowing the ring counter to continue running. The result, shown in Fig. 2-41, is a maximum-duration modulated drive signal.

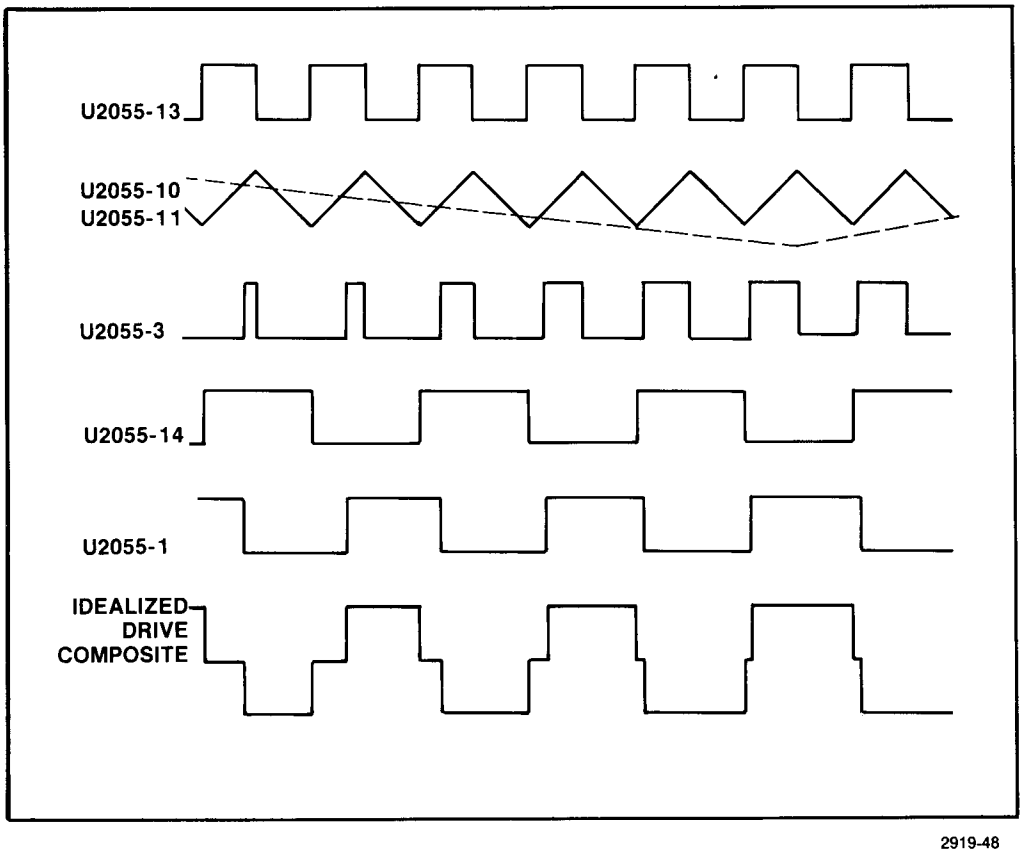


Fig. 2-41. +5 Volt Regulator during Undervoltage or Undercurrent.

The Base Driver circuit consists of complementary transistor pair Q1043-Q1049 and related components, which are driven by the /Q output of U2055B; and complementary transistor pair Q1042-Q1048 and related components, which are driven by the Q output of U2055A. The transistor pairs operate in push-pull to drive transformer T3037.

The diodes in the emitter circuits protect the emitters from voltage transients that would otherwise occur during the switching cycle. Resistor R2042 limits the baseline current through the transformer. Resistor R2041 and capacitor C2043 provide the extra current required to switch the output stages.

+5-volt Power Output Stage

This circuit consists of power transistors Q1015 and Q1035, transformers T4035 and T3024, plus current-limiting transistor Q4048. The drive signal is coupled through T3037, which steps up the current by a factor of ten. The drive signal is fed to the output drivers, which are connected as a complementary pair. Because of the "dead" areas of the drive signal applied, and because the stage is ordinarily biased at zero, both output transistors are off for some of the operating cycle. Thus, when drive is removed, the output circuit pulls the storage current out of the transistors, so that the two turn off faster. Capacitors C3018 and C3035 furnish the return current path for the transformer.

The drive current is coupled across current sense transformer T4035 to Q4048, to be discussed later, and across output transformer T3024 to the rectifier stage, which consists of CR2035 and CR2018. These are Schottky diodes, which have a very low forward voltage drop, and thus improve supply efficiency. From there, the current passes through inductive filtering to the load. Most of the capacitive load for the supply is on the circuit boards, distributed throughout the 7D02.

The current that is coupled across T4035 is used to drive Q4048. At any time that the voltage across the secondary of T4035 exceeds 0.7 volts, Q4048 begins to conduct, which pulls positive on the input network to pin 10 of U3055D. The cathode of CR4065 is normally at about +5 volts, and its anode is near ground. When Q4048 pulls positive on the network, C4067 couples this positive change to CR4065, causing it to go through U3055D into over-range, as discussed earlier. Capacitor C4049 and resistor R4057 serve as a delay circuit to hold U3055D in over-range for a short time, which slows the circuit during turn-on and slows current-limit recovery time. Diode CR4056 is connected in parallel with R4057 to reduce the discharge time of C4049.

Meanwhile, the reduced drive to the Output stage cuts down on the signal to Q4048, so it stops conducting. This permits the RC circuit to bleed down, U3055D to come out of over-range, and the supply to attempt to resume full-scale operation again. If the current demand is still too high, enough voltage is coupled across T4035 to cause Q4048 to conduct again, and the current-limit cycle repeats.

+3-volt Driver

The +3-volt Driver circuit consists of comparators U3055A, U3055B, and associated components. The differentiated wave at the input of U3055D is also applied to pin 7 of U3055B, where it is used for comparison with the +3-volt sense line. The other input to U3055B is driven by U3055A, which drives U3055B into over-range whenever current demand on the supply is too high.

It should be noted that the +3-volt supply is simply a demand current sink. That is, if the demand on the supply reduces to zero, the output voltage also goes to zero, and the current consumed by the regulator and output stages also goes to zero. The +3-volt supply need not be operating for the +5-volt supply to operate properly.

Because of the potential at pin 5 of U3055A, CR3048 is normally reverse-biased. Thus, the voltage at pin 6 of U3055B is set by R4043, R4044, and R4045 at about +5 volts. Each time the integrated oscillator signal at pin 7 of U3055B crosses +5 volts, the comparator switches. (This is virtually identical to the operation of U3055D; see the +5-volt Supply description.) The resulting output is illustrated in Fig. 2-42, which shows idealized waveforms of the circuit. Note that in actual operation the reference voltage at pin 6 of U3055B will never continue to increase as shown here for effect. Rather, the regulator circuit, being a closed loop, will quickly correct the shift in reference voltage. Thus, depending on the level of the +3-volt SENSE line, U3055B produces a drive signal that varies in pulse width and energy content to regulate the +3-volt level.

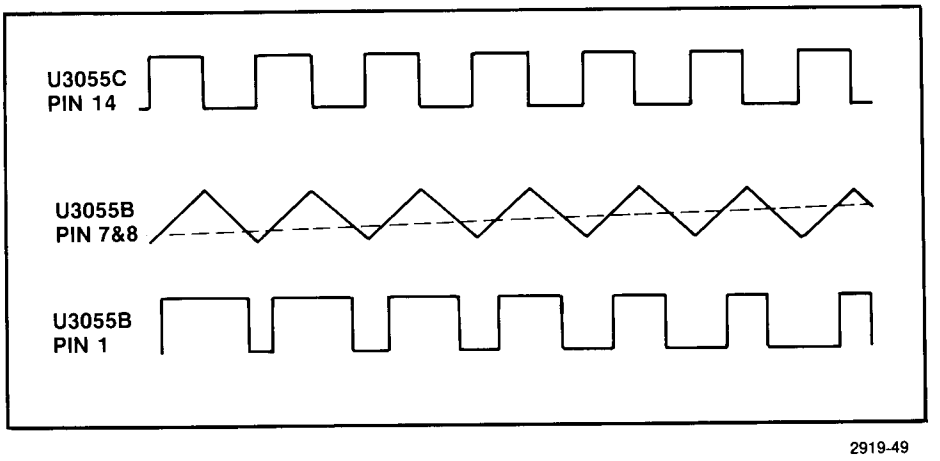


Fig. 2-42. +3 Volt Regulator Operation.

Current Limiter

Comparator U3055A and related components form the Current Limiter for the +3-volt supply. Normally, the current through R5010 is such that the potential at U3055A, pin 5, remains slightly positive relative to that at pin 4. Thus, the output of the comparator (pin 2) is +15 volts, holding CR3048 back-biased. As the demand on the supply increases to the limit point (approximately 1.3 A), the voltage at pin 5 of U3055A drops below that on pin 4. The comparator switches, and its output swings negative. Diode CR3048 is turned on, which pulls U3055B pin 6 well below the triangular wave on the other input, and the comparator output moves positive and stays there. Transistor Q2040 is biased into saturation, and Q5038 is turned off, which turns off the normal current for the +3-volt supply.

Should the current demand decrease, the voltage at pin 5 of U3055A will rise to the point at which the comparator will switch. Resistor R3044 and capacitor C3042 continue to hold CR3048 in conduction a little longer. When C3042 discharges sufficiently, CR3048 permits U3055B to switch and resume the regulation cycle.

+3-volt Output

This circuit consists of transistors Q2040 and Q5038, plus related components. Transistor Q2040 serves as a buffer stage, driving Q5038, which controls the current for the +3-volt supply. Transistor Q5038 is turned on and off at a varying duty cycle which thereby controls the current drawn through L5034. When Q5038 is off, the current that continues to flow through L5034 is returned to the +5-volt supply by diode CR5017, thereby increasing the efficiency of both supplies.

SECTION 3

PERFORMANCE CHECK AND ADJUSTMENT

Preliminary Information

Adjustment Interval

To maintain the specified accuracy of the 7D02, check the performance after each 2000 hours of operation, or after 12 months if the instrument is used infrequently. Before performing adjustment procedures thoroughly clean and inspect the instrument as described under Preventive Maintenance in Section 5, Maintenance.

Tektronix Field Service

Selected Tektronix Field Service Centers and the Factory Service Center provide complete repair and adjustment services. Contact the nearest Tektronix Field Office or representative for further information.

Using This Procedure

The procedures in this section are divided into four general areas:

Self Test Diagnostics -- exercise the 7D02 circuits under conditions approaching maximum performance. Successful completion of these tests indicates to a high confidence level that the 7D02 is operating properly.

Functional Check -- assures that the Timing Option section (if included), trigger in, trigger out, counters, state machine, and halt circuits operate normally.

Adjustment Procedure -- provides detailed instructions for adjusting internal parameters. Since very few adjustable components are used in the 7D02, the procedure is relatively short.

Performance Check Procedure -- checks each parameter in a step-by-step procedure against its specification. The procedure is necessarily long and detailed, and should be used selectively to isolate problems or to verify any suspected parameter.

All performance check procedures are done with the 7D02 plugged into the Mainframe. The adjustment procedures require that extenders be installed and that the 7D02 side panels be removed.

Refer to Table 3-1, Specifications, for a complete list of the 7D02 performance data.

TABLE 3-1

SPECIFICATIONS

Definition of Column Headings

Characteristics -- A distinguishing electrical, environmental, or physical feature or property of the product.

Performance Requirement -- Statements which describe the characteristics of the product in terms of verifiable limits. Information in this column defines the primary characteristics of the product and are considered to be a commitment between TEKTRONIX and the Customer. This performance is considered essential for minimum product performance and as such should be verified as part of the Performance Check procedure.

Description -- Statements which describe characteristics of the product which cannot be stated in terms of verifiable limits or which do not need verification (such as length or weight).

Supplemental Information -- Statements of capabilities which support or are secondary to the Performance Requirements. These statements may or may not be checked in the Performance Check procedure.

CHARACTERISTICS	DESCRIPTION
State Table Display	
Type:	Raster Scan - 24 lines x 32 characters per line
Number of channels displayed	(Basic 7D02) 28 Data 8 Address 16 Control 4

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Max number acquisition memory locations displayed	19
Typically	17
Radices Available	
Data:	Mnemonic disassembly for each supported microprocessor. ASCII HEX BINARY OCTAL
Address:	HEX BINARY OCTAL ASCII
Control:	MNEMONIC DISASSEMBLY BINARY
Signal Inputs	Signal inputs for the 7D02 are obtained through optional Personality Modules. These Personality Modules, along with Option 03, determine the number of channels that will be input to the 7D02.
Basic 7D02:	Data 8 Address 16 Control 10 Ext. Trigger 1
Input impedance:	Determined by the Personality Module (PM) used.
Setup/Hold time:	Depends on PM used.

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Synchronous Clock	
Setup/Hold time:	Determined by PM used.
Clock qualifiers:	Max number = 6 7D02 is capable of shifting or dividing qualified clocks by up to four positions or times respectively.
Memory Size	
Acquisition memory:	(Basic 7D02) = 28 x 256
Storage memory:	(Basic 7D02) = 28 x 256
Counters	
2 universal counters:	
Time mode -	
Resolution	1 ms or 1 us
Maximum count	65,534
Event mode -	
Maximum count	65,534
Control mode:	
Time mode -	
Resolution	1 ms or 1 us
Minimum interval generated	2
Maximum interval generated	65,534
Event mode -	
Minimum interval generated	2
Maximum interval generated	65,534

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Word Recognizers	
Number of word recognizers:	4
Number of channels:	(Basic 7D02) 32 Data 8 Address 16 Control 6 Ext. Trigger 1 Timing Option Link 1 (if Timing Option installed)
Triggering	The 7D02 can be triggered from any of the Word Recognizers or from either of the Counters, in the Control mode. This gives the 7D02 the ability to track and trigger on very complex program flows.
Trigger position:	Number of qualified clocks displayed after the trigger point: Trigger Before Data 240 Trigger Centered 128 Trigger After Data 16 Zero Delay 0
Data Qualification	Complex data qualification is provided through the use of the Word Recognizers and Counters.
Option 01 - Timing Option	The Timing Option provides the 7D02 user with 8 additional channels of asynchronous data acquisition at sample rates of up to 50 MHz.
Singal Inputs	
Number of channels:	8 (using a P6451 Data Probe)

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Clock	
Asynchronous:	
Sample rates	20 ns to 5 ms in a 1,2,5 sequence
Synchronous sample:	
Maximum frequency	10 MHz obtained from system under test via the Personalty Module
Memory Size	
Acquisition memory:	8 x 255
Glitch memory:	8 x 255
Word Recognizers	
One data word recognizer:	8 channels (ANDed together)
One glitch word recognizer:	8 chennels (ORed together but ANDed with the Data Word Recognizer)
External trigger in:	Front panel BNC TTL compatible
Asynchronous filter:	Programmable to 300 ns in 20 ns increments
Triggering	
The Timing Option can be triggered from any or all of the following sources:	1. Timing Option Data Word Recognizer 2. Timing Option Glitch Word Recognizer 3. Main Section (7D02) Word Recognizers 4. External Trigger In

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Digital Delay	
Maximum delay:	65,534 sample clocks
Timing Diagram Display	
Number of channels:	8
Window size:	124 words in x 1 mode or 31 words in x 4 mode. Data channels can be relocated by the user.
Numeric formats:	HEX OCTAL BINARY ASCII
Glitch display:	Glitches are displayed by an . above the line where the glitch occurred.
State Table Display	
Max number of words displayed:	19 Numeric formats: HEX OCTAL BINARY ASCII Glitch displayed as a * in the table beside DATA
Number of words scrolled:	255
Miscellaneous	The Timing Option comes standard with a P6451 Data Acquisition Probe.

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	DESCRIPTION
Option 03 - Expansion	The Expansion Option provides the 7D02 with the ability to support 16-bit microprocessors.
Signal Inputs Adds an additional 16 bits to the 7D02:	 Data 8 Address 8
Word Recognition Maximum number of channels	 48 Data 16 Address 24 Control 6 Ext. Trigger 1 Timing Option Link 1 (if Timing Option installed)
Display Max number of channels:	 44 Data 16 Address 24 Control 4
Memory Size Acquisition memory: Storage memory:	 44 x 256 44 x 256

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Timing Option		
Asynchronous Timing Mode	Sample period crystal controlled ±0.01%	
Glitch position:	+0 -1 Bit	
Trigger position accuracy:	±1 Bit	Asynchronous only
System Specs with P6451		
Max data skew:		0 ±5 ns
Glitch latch:	Type 1 glitch	Type 2 glitch
Minimum pulse width:	5 ns	6 ns
PIC NUM. 1		
System Specs with P6451 and PM101		
Data setup time:	20 ns maximum	
Data hold time:	2 ns maximum	
Timing word recognizer:		
Setup	40 ns maximum	
Hold	2 ns maximum	

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
P6451 Probe		See P6451 literature for more information.
Input R and C:		Approx. 1 M-ohm Approx. 5 pF without leads Approx. 12 pF with leads
Minimum logic swing:		500 mV +2% threshold voltage centered on threshold voltage
Maximum logic swing:		-15 V to threshold voltage plus 10 V
Maximum non-destruct input voltage:		-40 to +40 V
Threshold voltage accuracy:	±60 mV	System spec
Input current:		Approx. 8 uA measured at 6.4 V into probe tip
External Trigger In		
System spec using PM101 input impedance:	1.0 M ±2%	Compatible with 10X coded probe. nominal capacitance 20 pF. P6105 10X 2 meter probe recommended.
Threshold voltage:		1.4 V nominal
Hysteresis:		60 mV nominal at BNC 600 mV nominal with P6105

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Input voltage:		
High state		2.0 V min (with 1X probe only)
Low state		0.8 V max (with 1X probe only)
Main Word Recognizer		
Setup time:	10 ns @ BNC max	P6105 adds 9 ns to setup time, subtracts
Hold time	18 ns @ BNC max	9 ns from hold time
Timing Word Recognizer		
Asynchronous mode min. pulse width:	25 ns	
Trigger output:		TTL level signal that is 1 qualified state clock pulse approx. 86 ns after the timing trigger event is clocked into the 7D02. If timing option is not installed, the main trigger command initiates the trigger out. See Fig. 1, 50-ohm series terminated driver.

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Low state voltage:		0.5 V into R_L = 2K
High state voltage:		2.4 V into R_L = 2K Output can drive one STTL load.
System Specifications with PM101		Measured per manual performance check procedure
Clock qualifier data channels C4-C9:	Setup time = 55 ns max Hold time = 0.0 ns max	Typical setup time = 35 ns
Data/Address/CØ-C5:	Setup time = 45 ns max Hold time = 0.0 ns max	Typical setup time = 25 ns
When C6-C9 are used to generate /ESYNC and /WAIT:	Setup time = 55 ns max Hold time = 0.0 ns max	Typical setup time = 35 ns
Clock period minimum:	100 ns	
Clock pulse width, minimum:	25 ns high, 25 ns low	
Minimum interval between qualified clocks:	100 ns	

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Halt delay at PM101:		Schottky TTL level signal that is approx. 58 ns after the 7D02 stops acquisition. In zero delay trigger mode, the 7D02 stops acquisition 2 qualified state clocks after the main trigger event is clocked into the 7D02. Refer to Fig. 3-0.
Counters		
Counting mode time mS or uS clock accuracy:	0.01%	Error Bound (±0.01% ±1 count) X (number of Start/Stop cycles)
Control mode time mS or uS clock accuracy:	0.01%	Error bound (-0/+1 count ±.01% of value -0/+.2 uS) X number of start/stop cycles. Note: If 7D02 is stopped prior to terminal count, add one count to error bound.
Environmental Specifications		
Non-operating temp:		-55 to 75 (deg. C)
Operating temp:		0 to 50 (deg. C)
Relative humidity:		90 to 95 (%)
Non-operating altitude:		15 (kM)(50,000 feet)
Operating altitude		4.5 (kM)(15,000 feet)

TABLE 3-1

SPECIFICATIONS (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Vibration:		10-55 Hz (SW), 75 min. tot. Tek Std. 062-2858-00, Cl-3
Shock:		50 (g's) Half-sine, 11 mS, 18 reps Tek Std. 062-2858-00, Cl-3
Bench handling:		45 deg. or 4" All significant faces Tek Std. 062-2858-00, Cl-3
Package trans. vib.: (Non-op)		25.4 (mm)(1 inch) Approx. 270 rpm Tek Std. 062-2858-00, Cl-3
Package drop (Non-op):		0.914 (M)(3 feet) 10 drops Tek Str. 062-2858-00
Mechanical Specifications		
Weight:		Approx. 8 lbs (3.6 kg)
Outside dimensions:		21x13x37 cm (8.25" wide x 5" high x 14.6" deep)
Mainframe compatibility:		Compatible with all 3 and 4 wide 7000 Series Oscilloscopes Temperature-derated in rack-mounted oscilloscopes to 35 deg. C. Display degraded in storage oscilloscopes.

Test Equipment Required

General

The test equipment listed in Table 3-2 is required for a complete performance check and adjustment of the 7D02. Detailed operating instructions for use of the test equipment are not included in the Performance Check and Adjustment Procedures. Refer to the appropriate test equipment manuals for more information. Refer to the paragraph that follows table 3-2 for information on assembling the small test fixtures required.

TABLE 3-2

TEST EQUIPMENT REQUIRED

Item	Familiar Name	Purpose
Oscilloscope Main-Frame (7603, 7704A, or other appropriate mainframe)	Mainframe	To provide the facilities necessary to operate the 7D02.
Oscilloscope, 200-MHz bandwidth, dual-trace, calibrated 1 nS/div resolution	Test Oscilloscope	To provide for examination of 7D02 signals.
Probes (2)	P6105	Test oscilloscope input probes and EXT TRIG in check.
Time Mark Generator (TG501)	TG501	To provide a precision frequency reference to the 7D02.
Pulse Generator (PG508)	PG508	To provide stimulus pulses to 7D02.
Pulse Generator (PG502)	PG502	To provide stimulus pulses to 7D02.
Digital Counter (DC503)	DC503	To provide for measuring clock frequencies.

TABLE 3-2

TEST EQUIPMENT REQUIRED (cont.)

Item	Familiar Name	Purpose
Personality Module	PM101	To provide data acquisition for 7D02.
Digital Multimeter (DM501A)	DM501A	To provide for measuring test signals.
Power Supply (PG503A)	PS503A	To provide test voltsges.
Test Equipment Mainframe (TM504)	TM504	To provide facilities necessary to operate above six items.
Logic Analyzer (7D01)	7D01	To provide for examination of 7D02 conditions.
Miniature Retractable Hook Tip (206-0222-00)	Hook Tips	To provide for signal line connectors (9 required).
BNC Male to Dual Binding Post Adapter (103-0035-00)	BNC to Binding Post Adapter	To provide for signal line connection (4 required).
50-Ohm Feed Through Terminator (011-0049-01)	50-Ohm Termination	To provide for signal termination (2 required).
Flexible Plug-In Extender (067-0616-00)	Extender	To allow 7D02 operation outside Mainframe (2 required).
Coaxial Cable, 50-Ohm, 18-inch (012-0076-00)	Coaxial Cable	To provide for signal connection (2 required).
Test Lead, Black (012-0426-01)	Black Test Lead	To provide for signal measurement with DM501A.
Test Lead, Red (012-0426-00)	Red Test Lead	To provide for signal measurement with DM501A.

TABLE 3-2

TEST EQUIPMENT REQUIRED (cont.)

Item	Familiar Name	Purpose
BNC Elbow, Male to Female (103-0031-00)	BNC Elbow	To provide for signal connection.
BNC Female to EZ Ball Adapter (013-0076-01)	BNC to Ball Adapter	To provide for signal connection.
BNC T (103-0030-00)	BNC T	To provide for signal connection (2 required).
Probe Tip to BNC Adapter (013-0084-01)	Probe Tip to BNC Adpater	To provide for signal connection (2 required).
BNC Male to BNC Male Adapter (103-0029-00)	BNC Male to Male Adapter	To provide for signal connection.
Small Screwdriver	Screwdriver	To provide for potentiometer adjustment.
Wire, 22-gauge		To provide for test lead connections to signal source (6 1.5-inch pieces required).
Resistor, 2-kOhm		To provide for output signal loading.

Test Fixtures

Two types of test fixtures are required. For ease of reference in the procedures that follow, these are designated as Test Fixtures, 1 and 2. Test Fixture 1 is assembled by loosening the binding post screws on a BNC to Binding Post Adapter, inserting a separate piece of 22-gauge wire through each, tightening the screws, and bending the wire in opposite directions. (For most effective use, insert the wire so that all of the excess length is to one side.) Two examples of Test Fixture 1 are required. Test Fixture 2 is assembled by loosening the binding post screws on a third BNC to Binding Post Adapter, bending the wires on the 2-kOhm resistor appropriately

to fit the binding posts holes, inserting one resistor lead in each post, and tightening the screws.

Self-Test Diagnostics

PM101 Personality Module Self Test Connection Procedure

a. Turn off power to the Logic Analyzer at the oscilloscope mainframe.

b. Remove the plastic cover on the back of the Personality Module using a small screwdriver or allen wrench.

c. Move the strapping connector from the power-off position to the power-on position.

d. Connect the Data, Address, Control and Clock leads on the PM101 to the Self-Test Stimulus pins as indicated in Table 3-3 and shown in Fig. 3-1.

Note

The PM101 leads are color-coded with the standard resistor code. The color of the lead itself signifies the least significant digit, while the color of the end of the lead signifies the more significant digit. Connection to a particular pin of the up to four for each T# is arbitrary.

Table 3-3
SELF TEST STIMULUS CONNECTION

	PM101 Individual Test Leads					
Connector	Data	Address	Address	Qualifiers	Timing	Other
T2	DØ	AØ			Black	
T3	D1	A1			Brown	
T4	D2	A2			Red	
T5	D3	A3			Orange	
T6	D4	A4			Yellow	
T7	D5	A5			Green	
T8	D6	A6			Blue	
T9	D7	A7			Violet	
T10	D8	A8	A16	QØ		
T11	D9	A9	A17	Q1		
T12	D1Ø	A1Ø	A18	Q2		
T13	D11	A11	A19	Q3		
T14	D12	A12	A20	Q4		
T15	D13	A13	A21	Q5		
T16	D14	A14	A22			
T17	D15	A15	A23			
T18				Q6		
T19				Q7		
T20				Q8		
T21				Q9		
CLK						Grey
T HALT						Red
GND					White	Black

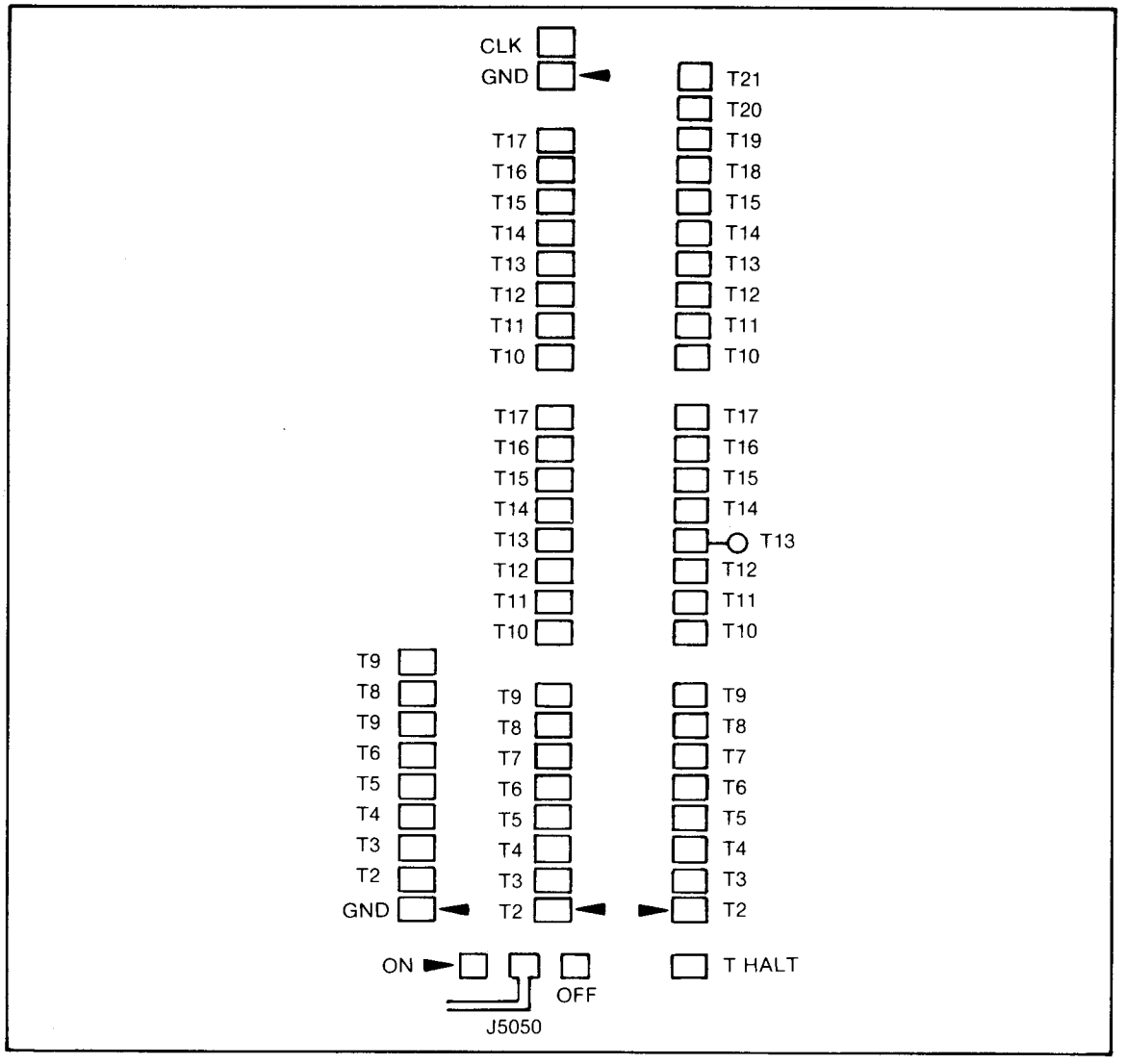


Fig. 3-1. Test Socket Layout. 2919-50

Extender Installation Procedure

For those adjustment procedures in which the 7D02 must be operated outside the Mainframe, install and connect the Extenders as follows:

1. Turn off Mainframe power.

2. If connected, disconnect PM101 and P6451 from front panel connectors.

3. Remove 7D02 from Mainframe.

4. Remove 7D02 side panel by gently prying (with fingers) at back end and pulling out directly, taking care not to bend panels.

5. Install two Extenders in appropriate Mainframe compartments.

6. Connect Extender connectors to appropriate connectors in 7D02 rear panel.

Initial Setup Procedure

Set up the 7D02 for performance check and adjustment as follows:

NOTE

In the following procedures:

1. All reference to pressing a "key" refers to pressing a pushbutton switch on the 7D02 front panel unless otherwise specified at the reference.

2. All references to "display" pertain to the Mainframe screen unless otherwise specified at the reference.

1. Perform PM101 Personality Module Self Test Connection Procedure.

2. Install 7D02 in appropriate 7000-Series Mainframe.

3. Connect PM101 General Purpose Personality Module to data input connector at lower left front of 7D02.

4. Connect P6451 Timing Probe to timing input connector at lower right front of 7D02.

5. Turn on Mainframe power. Power-up diagnostics will run automatically.

- If diagnostics run successfully, the message "POWER UP DIAGNOSTICS COMPLETE" will be displayed on screen.

- If diagnostic ROM test fails, following message will be displayed on screen:
  "POWER UP VERIFICATION"
  "XXXXXXX FAIL"
  "WARNING"
  "UNABLE TO COMPLETE VERIFICATION"

- If other diagnostic tests fail, appropriate error message will be displayed.

If error message is displayed, refer to Section 5, Maintenance.

6. Press START/STOP key. Instrument should acquire data and display ascending sequence of numbers in data and address fields. The control count increments. The control field is the binary representation of the second most significant hex digit in the data and address fields.

- If instrument does not display proper data, recheck loop connections on Personality Module.

- If no connection errors, refer to Section 5, Maintenance.

7. Allow 7D02 to warm up for 20 minutes before proceeding.

8. Turn Mainframe power off for five or more seconds, then turn power on again.

9. Within several seconds, press and hold any key. Resultant keyboard failure should cause 7D02 to remain in extended diagnostic mode, which will be indicated on screen by list of diagnostic tests, all of which pass except KEYBOARD.

10. Release held key.

11. Press X key. Diagnostic module test menu should be displayed.

12. Press 0 key to select "TEST ALL".

13. Press START/STOP key. Extended diagnostic tests should run and status should be displayed.

- If any test fails, recheck loop connections on Personality Module.

- If no connection errors caused failure, refer to Section 5, Maintenance.

14. Repeat parts 8 through 11 to set up instrument for performance test and adjustment. Display should appear as in Fig. 3-2.

15. Press "X" to exit diagnostic monitor.

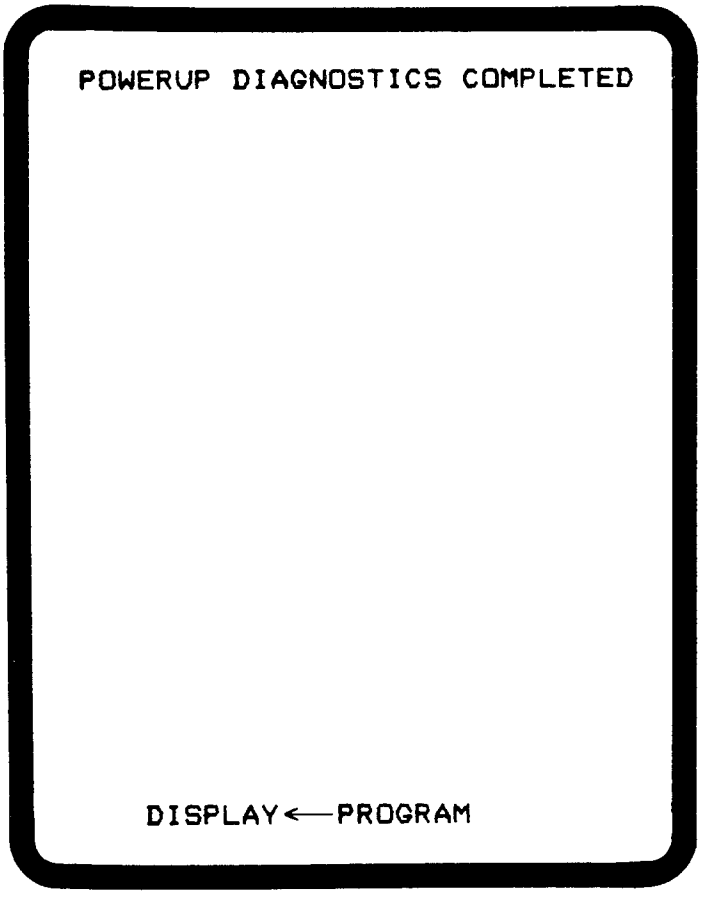


Fig. 3-2. Power Up Verification Display.

Functional Check

1. Check Timing Option Operation

a. Press ELSE, TRIGGER, and 1 (Timing) keys.

b. Move cursor to sample period field and enter 20 nS.

c. Move cursor to Word Recognizer field and enter all 0's.

d. Move cursor to filter field and enter 40 nS.

e. Press END key.

f. Press START/STOP key to run program.

g. CHECK - that display is binary pattern.

2. Check External Trigger In

Equipment required:

P6105 10X Probe (from Test Oscilloscope)

NOTE

Make certain that P6105 Test Oscilloscope probe used in following parts is properly compensated at 20 pF before performing this procedure. This probe must be a 10 X coded probe.

a. Remove P6105 probe from Test Oscilloscope and connect to EXT TRIG IN connector on 7D02.

b. Disconnect control line C9 from PM101 test socket terminal T21.

c. Connect P6105 probe ground to test socket ground.

d. Connect P6105 probe tip to terminal T21.

e. Turn mainframe off for five seconds to reset default parameters. Turn on the mainframe power again.

f. Press FORMAT key and change "Word Recognizer Data Field" and "Data Field Display" radices to binary.

g. Press FORMAT key again to exit format mode.

h. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

i. Press WD RECOGNIZER key.

j. Move cursor to Word Recognizer data field and enterXXXXXXXXXXXXXX0X. as shown for check #1 in the following table.

CHECK #	DATA VALUE	EXT TRIG IN VALUE	RESULT
1	XXXXXXXXXXXXXX0X	0	Trigger on Data Bit #1=0
2	XXXXXXXXXXXXXX0X	1	No Trigger
3	XXXXXXXXXXXXXX1X	0	No Trigger
4	XXXXXXXXXXXXXX1X	1	Trigger on Data Bit #1=1 (Bit Ø is the least significant bit)

k. Move cursor to External Trigger In field and enter 0.

l. Press TRIGGER and END keys.

m. Press START/STOP key.

n. CHECK - that result is as shown in table above.

o. Repeat step h and perform checks 2 through 4 and verify results. After tests 2 and 3, press the START/STOP button to stop acquisition.

p. Disconnect P6105 probe and reconnect control line C9.

3. Check Counter, Trigger, and State Machine

Equipment required:

DC503
Coaxial Cable
50-ohm Termination

a. Using Coaxial Cable, connect TRIG OUT connector to 50-ohm Termination. Connect terminator to DC503 CHANNEL B input connector.

b. Set DC503 FUNCTION control to PERIOD. Set clock rate to 1 uS. Set all buttons to out position.

c. Power down mainframe for five seconds to reset default parameters.

d. Press COUNTER key and enter 10,000 uS.

e. Press [] (brackets) key.

f. Press COUNTER key.

g. Enter 2 for Counter #, and enter 1 to select uS.

h. Enter 2 to select reset and run mode.

i. Press GO TO, [] (brackets), ELSE, COUNTER, and END keys.

j. Press counter, enter 2 for counter #, enter 10000 and 1 for uS.

k. Press [] (brackets) keys, then press COUNTER key again.

l. Move cursor to Counter Mode field and enter 2 to select reset and run mode.

m. Press GO TO key and enter 1.

n. Press [] (brackets) key.

o. Press ELSE, TRIGGER, 1 (Timing), and END keys.

p. Press ELSE, TRIGGER, and END keys.

q. Press START/STOP key.

r. Adjust B level control for a stable display.

s. CHECK - that DC503 indicates 20 mS.

t. Press the STOP key.

4. Check HALT Circuit

a. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

b. Move cursor to end of existing program.

c. Press and hold DELETE key until entire program is deleted.

d. Press WD RECOGNIZER key.

e. Press TRIGGER key.

f. Move cursor to Trigger Delay field and enter 3 to select zero delay.

g. Enter 1 to select system under test halt mode.

h. Press END key.

i. Press WD RECOGNIZER key and enter 0000 into the Word Recognizer Data Field. All other values should be "X".

j. Press TRIGGER and END keys.

k. Press IMMEDIATE GO TO, 2, and right-hand cursor (execute) keys.

l. CHECK - that trigger occurs on data 0000.

m. Press START/STOP key.

n. CHECK - that trigger occurs on data 0003.

o. Continue pressing START/STOP key and checking that data increments by 3 each time key is pressed.

Adjustment Procedure

1. Adjust +5-Volt Power Supply

Equipment required:

DM501A
Screwdriver
Extender (P/O Service Maintenance Kit, 067-0939-00)

a. Perform Extender Inatallation Procedure and Initial Setup Procedure.

b. Set DM501A to measure DC volts in 20-volt range.

c. Connect DM501A VOLTS test lead to Power Supply Board J211, pin 27B.

d. Connect DM501A LOW test lead to Power Supply Board J211, pin 20B.

e. Record voltage indicated on DM501A.

f. Calculate difference between recorded voltage and +15V, divide result by three. If recorded voltage is below +15 V, subtract quotient from +4.85 V; if recorded value is above +15 V, add quotient to +4.85 V. Resultant value is adjustment voltage.

g. Connect DM501A VOLTS test lead to Main Interface Board J201, pin 3B (+5-volt sense line).

h. Connect DM501A LOW test lead to Main Interface Board J201, pin 1A.

i. CHECK - that indicated voltage is as calculated in part f.

j. INTERACTION

- If voltage is not as calculated, adjust potentiometer R5065 at left edge of Power Supply Board.

- If voltage cannot be adjusted to calculated value, refer to Section 5, Maintenance.

2. Check +3-Volt Power Supply

NOTE

This check is required only if the 7DO2 is equipped with the Timing Option. This supply may be checked, however, even if no Timing Option is available, by using the Power Supply Test Fixture which is part of the Service Maintenance Kit (Tek. P/N 067-0939-00) and an alternative procedure described below. Instructions for installation of the Fixture come with the Service Maintenance Kit.

Equipment required:

DM501A
(Optional) Power Supply Test Fixture

a. Connect DM501A VOLTS test lead to Main Interface board J202, pin 27B.

b. Connect DM501A LOW test lead to Main Interface board J202, pin 1B.

c. CHECK - that indicated voltage is between 2.71 and 2.99 V.

d. INTERACTION - If voltage indication is not correct, refer to Section 5, Maintenance.

2.1 Alternative +3 Volt Power Supply Check

If the Timing Option is to be installed for the first time, or if no Timing Option is available, the +3 Volt Power Supply can be tested anyway using the Power Supply Test Fixture in slot AØ3 instead of the Timing Option Board. AØ2, the IC Acquisition board, also must be removed.

Install the Power Supply Test Fixture in slot AØ3 in accordance with the instructions in the Service Maintenance Kit and perform the same procedure as above.

3. Check and Adjust Display Vertical and Horizontal Gain and Position

Equipment required:

Screwdriver

a. Perform Extender Installation Procedure and Initial Setup Procedure steps 1 and 3 through 11. (If 7D02 has been warmed up for 20 minutes, perform only Steps 1 and 3 through 5, plus 8 through 11.)

b. Press 2 key to select Display Module.

c. Press START/STOP key twice.

d. CHECK - that full screen inverse-video display appears.

e. Adjust front panel VERT POS control to set top of display at top graticule line.

f. Adjust front panel HORIZ POS control to set left-hand side of display at left-hand graticule line.

g. CHECK - that screen inverse video display is: 1) not larger than 1 minor division wider or higher than graticule, and 2) not smaller than 2 minor divisions narrower or lower than graticule.

h. INTERACTION - If display is not correct, perform parts **i** through **r**. If display is correct, perform parts **k** through **r**.

i. Adjust Display Board VERT gain control potentiometer R6011 (at left-hand edge of board) to set bottom of display at bottom graticule line.

j. Adjust Display Board HORIZ gain control potentiometer R5013 (at left-hand edge of board) to set right-hand side of display at right-hand graticule line.

k. Turn front panel VERT POS control to clockwise extreme, then counterclockwise extreme.

NOTE

It is possible that, if the Mainframe calibration is not proper, there might be two major divisions of total displacement, but the displacement might not be plus and minus one division.

l. CHECK - that top and bottom edges of display move at least 1 major division above and below corresponding graticule lines.

m. Reset VERT POS control for centered display.

n. Turn front panel HORIZ POS control to clockwise extreme, then counterclockwise extreme.

NOTE

It is possible that, if the Mainframe calibration is not proper, there might be two major divisions of total displacement, but the displacement might not be plus and minus one division.

o. CHECK - that right-hand and left-hand edges of diplay move at least 1 major division to right and to left of corresponding graticule lines.

p. Reset VERT POS control for centered display.

q. Press START/STOP key three times.

r. Press X key to display diagnostic module test menu.

4. Check and Adjust Timing Option Threshold Voltage

NOTE

This check is applicable only if subject 7D02 is equipped with Timing Option.

Equipment required:

PS503A
DM501A
Hook Tip (8)
Wire, 22 gauge
Test Oscilloscope

a. Perform Extender Installation Procedure and Initial Setup Procedure through step 6.

b. Turn off Mainframe and PS503A power.

c. Disconnect P6451 probe leads from PM101, and move PM101 jumper from ON position (test) to OFF position (operate).

d. Insert short piece of 22-gauge wire in PS503A positive 0-20V 1A output binding post. Tighten post knob.

e. Install Hook Tips on P6451 probe leads.

f. Connect P6451 probe lead Hook Tips to wire installed in part d.

g. Use short piece of 22-gauge wire to connect PS503A COMMON and ground binding posts.

h. Connect P6451 ground (black) lead to above wire.

i. Connect DM501A to measure output voltage of PS503A.

j. Turn on Mainframe power.

k. After message "DIAGNOSTICS COMPLETED" is displayed, press ELSE, TRIGGER, and 1 (Timing) keys.

l. Press 1 key to select data centered.

m. Enter PLUS 0.00 in Threshold Voltage field.

n. Move cursor to Word Recognizer field and enter all 1's.

o. Move cursor to Filter field and enter 300 ns.

p. Press END key.

q. CHECK - that program is as shown in Fig. 3-3.

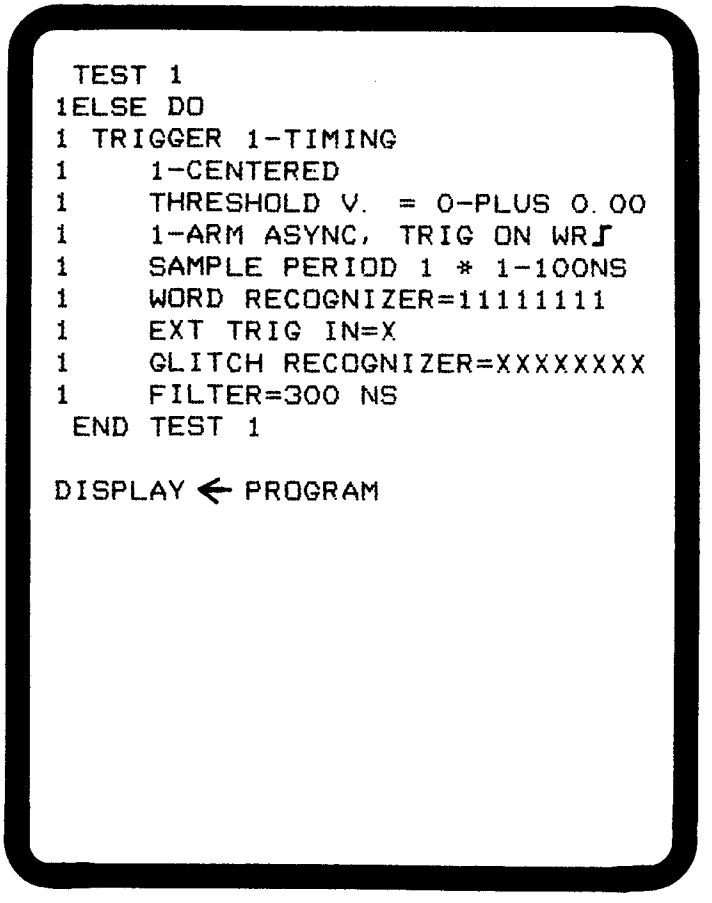


Fig. 3-3. Threshold Voltage Program.

r. Turn PS503A output voltage to 0.

s. Turn on PS503A power.

t. Press START/STOP key.

u. CHECK - that display indicates that program is running.

v. Slowly increase PS501A output voltage (very slowly as it approaches 60 mV).

w. CHECK - that Timing Option triggers at voltage less than 60 mV.

x. INTERACTION

- If Timing Option triggers properly, proceed to part **y**.

- If Timing Option does not trigger properly, perform parts **an** through **bi**.

y. Press IMMEDIATE, DISPLAY, PROGRAM keys.

z. Move cursor to Threshold Voltage field and enter PLUS 6.35.

aa. Press START/STOP key.

ab. CHECK - that display indicates that program is running.

ac. Slowly increase PS503A output voltage (very slowly as it approaches 6.4 V).

ad. CHECK - that Timing Option triggers at less voltage than 6.41 V.

ae. INTERACTION

- If Timing Option triggers properly, proceed to part **af**.

- If Timing Option does not trigger properly, perform parts **bl** through **cg**.

af. Increase PS503A output voltage to 6.5 V.

ag. Press IMMEDIATE, DISPLAY, PROGRAM keys.

ah. Move cursor to Word Recognizer field and enter all 0's.

ai. Press START/STOP key.

aj. CHECK - that display indicates that program is running.

ak. Very slowly, decrease PS503A output voltage.

al. CHECK - that Timing Option triggers at voltage greater than 6.29 V.

am. INTERACTION

- If Timing Option triggers properly, perform parts **an** through **bk**.

- If Timing Option does not trigger properly, perform parts **bl** through **cg**.

an. Move piece of 22-gauge wire from PS503A positive output to negative output.

ao. Turn PS503A output voltage to 0.

ap. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

aq. Move cursor to Threshold Voltage field and enter 0.00.

ar. Press START/STOP key.

as. CHECK - that display indicates that program is running.

at. Increase PS503 output voltage (in negative direction) until trigger occurs.

au. CHECK - that Timing Option triggers at voltage less than -60 mV.

av. INTERACTION

- If Timing Option triggers properly, proceed to part **aw**.

- If Timing Option does not trigger properly, perform parts **bl** through **cg**.

aw. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ax. Move cursor to Threshold Voltage field and enter MINUS 6.35.

ay. Press START/STOP key.

az. CHECK - that display indicates that program is running.

ba. Increase PS503A output voltage, slowly as it approaches -6.4 V.

bb. CHECK - that Timing Option triggers at voltage more positive than -6.41 Vo.

bc. INTERACTION

- If Timing Option triggers properly, proceed to part **bd**.

- If Timing Option does not trigger properly, perform parts **bl** through **cv**.

bd. Increase PS603A output voltage to -6.5 V.

be. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bf. Move cursor to Word Recognizer field and enter all 0's.

bg. Press START/STOP key.

bh. CHECK - that display indicates that program is running.

bi. Slowly decrease PS03A output voltage.

bj. CHECK - that Timing Option triggers at voltage more negative than -6.29 V.

bk. INTERACTION

- If Timing Option triggers properly, adjustment verification is complete.

- If Timing Option does not trigger properly, perform parts **bl** through **cv**.

bl. Turn off Mainframe power for five or more seconds, then turn power on again.

bm. Within several seconds, press and hold any key to cause Keyboard Module failure and cause 7D02 to remain in extended diagnostic mode.

bn. CHECK - that display shows list of diagnostic tests, all of which pass except KEYBOARD.

bo. Press X key to display module test menu.

bp. Press 2 key to select Display module.

bq. Press START/STOP key twice.

br. CHECK - that full-screen inverse-video diplay appears.

bs. Move Front Panel Board jumper P1034 (at upper right-hand edge of board) from pins 2 and 3 (NORMAL) to pins 1 and 2 (CAL).

bt. Disconnect P6451 from front panel connector.

bu. Connect DM501A LOW test lead to Front Panel Board P1034, pin 1 (at upper right-hand edge of board).

bv. Connect DM501A VOLTS test lead to Front Panel Board Test Point 1053 (at upper right-hand edge of board).

bw. CHECK - that DM501A indicates 0 $\pm$0.012 V.

bx. INTERACTION

- If voltage is not correct, perform part **by.**

- If voltage is correct, proceed to part **bz.**

by. Adjust OFFSET potentiometer R1042 (left-hand potentiometer of two at upper right-hand edge of board) for DM501A indication of 0 $\pm$0.012 V.

bz. Press START/STOP key.

ca. CHECK - that display consists of 24 horizontal lines and 1 vertical line at center.

- that DM501A indicates +1.588 $\pm$0.012 V.

cb. INTERACTION

- If voltage indication is not correct, perform part **cc**.

- If voltage indication is correct, proceed to part **cd**.

cc. Adjust GAIN potentiometer R1046 (right-hand potentiometer of two at upper right-hand edge of board) for DM501A indication of +1.588 ±0.012 V.

cd. Press START/STOP key.

ce. CHECK - that DM501A indicates -1.588 ±0.012 V.

cf. INTERACTION

- If voltage indication is not correct, perform part **cg**.

- If voltage indication is correct, proceed to part **ch**.

cg. Press START/STOP key three times; repeat part **by**, moving offset slightly; then repeat parts **bz** through **cf**.

NOTE

If, after three or more iterations of adjusting offset and gain potentiometers, voltage still cannot be set to specifications, refer to Section 5, Maintenance.

ch. Connect Test Oscilloscope probe to Front Panel Board Test Point 1053 (at upper right-hand edge of board).

ci. Set Test Oscilloscope controls for 0.5 V/div, 0.2 ms/div, rising edge auto triggering, and AC coupling.

cj. Turn off Mainframe power for five or more seconds, then turn power on again.

ck. Within several seconds, press and hold any key to cause keyboard Module failure and cause 7D02 to remain in extended diagnostic mode.

cl. Press X key to display module test menu.

cm. Press 2 key to select Display module.

cn. Press E key to enable looping.

co. Press START/STOP key to run diagnostic program.

cp. CHECK - that display indicates that program is running and is looping on test 1 (test 1 passes but program does not enter test 2).

cq. Adjust Test Oscilloscope controls for display of single decreasing ramp.

cr. CHECK - that ramp decreases at linear rate.

cs. INTERACTION - If ramp shape is not correct, it may be necessary to perform more detailed procedure than outlined in this procedure from part **a** through part **am** (particularly parts **v** through **am**). This would entail making threshold check at every 60-mV step as voltage is increased, and would consist of 256 checks. If ramp shape is correct, proceed to part **ct**.

ct. Disconnect Test Oscilloscope probe.

cu. Move Front Panel Board jumper P1034 (at upper right-hand edge of board) from pins 1 and 2 (CAL) to pins 2 and 3 (NORMAL).

cv. Turn Mainframe power off and remove Extenders in essentially reverse order of installation.

Performance Check Procedure

1. Perform Self-Test Diagnostic Procedure

2. Perform Functional Check Procedure

3. Check Display Vertical and Horizontal Gain and Position

Equipment required:

Screwdriver

a. Perform Initial Setup Procedure, Steps 1 and 3 through 11. (If 7D02 has been warmed up for 20 minutes, perform only Steps 2 and 3 through 5, plus 8 through 11.)

b. Press 2 key to select Display Module.

c. Press START/STOP key twice.

d. CHECK - that full screen inverse-video display appears.

e. Adjust front panel VERT POS control to set top of display at top graticule line.

f. Adjust front panel HORIZ POS control to set left-hand side of display at left-hand graticule line.

g. CHECK - that screen inverse video display is: 1) not larger than 1 minor division wider or higher than graticule, and 2) not smaller than 2 minor divisions narrower or lower than graticule.

h. Turn front panel VERT POS control to clockwise extreme, then counterclockwise extreme.

NOTE

It is possible that, if the Mainframe calibration is not proper, there might be two major divisions of total displacement, but the displacement might not be plus and minus one division.

i. CHECK - that top and bottom edges of display move at least 1 major division above and below corresponding graticule lines.

j. Reset VERT POS control for centered display.

k. Turn front panel HORIZ POS control to clockwise extreme, then counterclockwise extreme.

NOTE

It is possible that, if the Mainframe calibration is not proper, there might be two major divisions of total displacement, but the displacement might not be plus and minus one division.

l. CHECK - that right-hand and left-hand edges of diplay move at least 1 major division to right and to left of corresponding graticule lines.

m. Reset VERT POS control for centered display.

n. Press START/STOP key three times.

o. Press X key to display diagnostic module test menu.

4. Check Timing Option Threshold Voltage

NOTE

This check is applicable only if subject 7D02 is equipped with Timing Option.

Equipment required:

PS503A
DM501A
Hook Tip (8)
Wire, 22 gauge
Test Oscilloscope

a. Perform Initial Setup Procedure through step 6.

b. Turn off Mainframe and PS503A power.

c. Disconnect P6451 probe leads from PM101, and move PM101 jumper (J5050) from ON position (test) to OFF position (operate).

d. Insert short piece of 22-gauge wire in PS503A positive 0-20V 1A output binding post. Tighten post knob.

e. Install Hook Tips on P6451 probe leads.

f. Connect P6451 probe lead Hook Tips to wire installed in part d.

g. Use short piece of 22-gauge wire to connect PS503A COMMON and ground binding posts.

h. Connect P6451 ground (white) lead to above wire.

i. Connect DM501A to measure output voltage of PS503A.

j. Turn on Mainframe power.

k. After message "DIAGNOSTICS COMPLETED" is displayed, press ELSE, TRIGGER, and 1 (Timing) keys.

l. Press 1 key to select data centered.

m. Enter PLUS 0.00 in Threshold Voltage field.

n. Move cursor to Word Recognizer field and enter all 1's.

o. Move cursor to Filter field and enter 300 ns.

p. Press END key.

q. CHECK - that program is as shown in Fig. 3-4.

r. Turn PS503A output voltage to 0.

s. Turn on PS503A power.

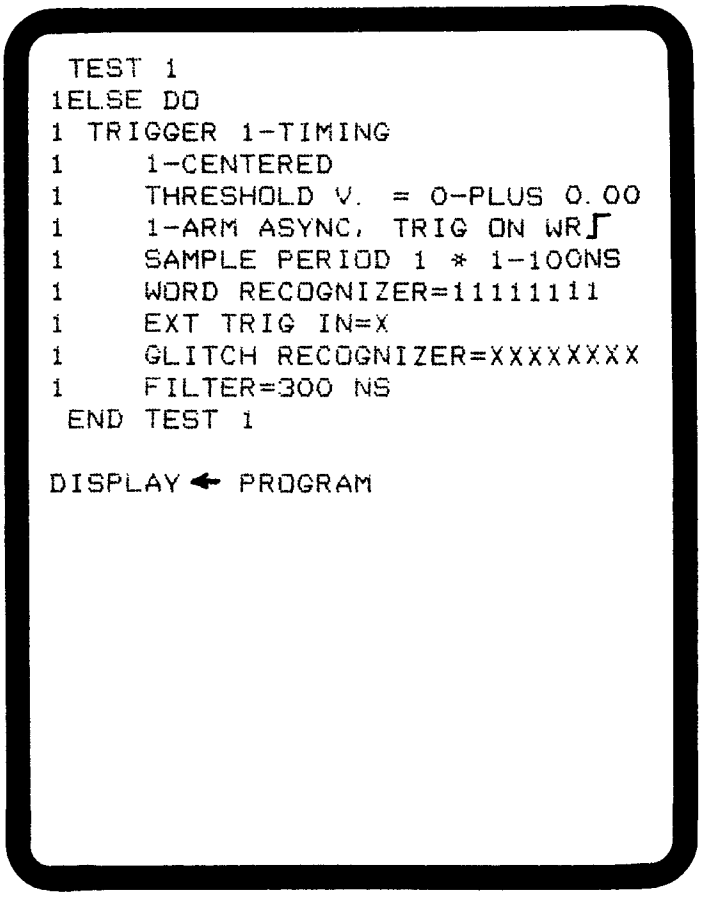


Fig. 3-4. Timing Option Threshold Voltage Program.

t. Press START/STOP key.

u. CHECK - that display indicates that program is running.

v. Slowly increase PS501A output voltage (very slowly as it approaches 60 mV).

w. CHECK - that Timing Option triggers at voltage less than 60 mV.

x. Press IMMEDIATE, DISPLAY, PROGRAM keys.

y. Move cursor to Threshold Voltage field and enter PLUS 6.35.

z. Press START/STOP key.

aa. CHECK - that display indicates that program is running.

ab. Slowly increase PS503A output voltage (very slowly as it approaches 6.4 V).

ac. CHECK - that Timing Option triggers at less voltage than 6.41 V.

ad. Increase PS503A output voltage to 6.5 V.

ae. Press IMMEDIATE, DISPLAY, PROGRAM keys.

af. Move cursor to Word Recognizer field and enter all 0's.

ag. Press START/STOP key.

ah. CHECK - that display indicates that program is running.

ai. Very slowly, decrease PS503A output voltage.

aj. CHECK - that Timing Option triggers at voltage greater than 6.29 V.

ak. Move piece of 22-gauge wire from PS503A positive output to negative output.

al. Turn PS503A output voltage to 0.

am. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

an. Move cursor to Threshold Voltage field and enter 0.00.

ao. Press START/STOP key.

ap. CHECK - that display indicates that program is running.

aq. Increase PS503 output voltage (in negative direction) until trigger occurs.

ar. CHECK - that Timing Option triggers at voltage less than -60 mV.

as. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

at. Move cursor to Threshold Voltage field and enter MINUS 6.35.

au. Press START/STOP key.

av. CHECK - that display indicates that program is running.

aw. Increase PS503A output voltage, slowly as it approaches -6.4 V.

ax. CHECK - that Timing Option triggers at voltage greater than -6.41 Vo.

ay. Increase PS603A output voltage to 06.5 V.

az. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ba. Move cursor to Word Recognizer field and enter all 0's.

bb. Press START/STOP key.

bc. CHECK - that display indicates that program is running.

bd. Slowly decrease PS03A output voltage.

be. CHECK - that Timing Option triggers at voltage greater than -6.29 V.

5. Check Setup and Hold, Main Section Data, Address, and Control Bits

Equipment required:

PG508
Hook Tips
Test Fixture 1
50-Ohm Termination
Test Oscilloscope

a. Connect 50-Ohm Termination to PG508 OUTPUT connector.

b. Connect Test Fixture 1 to 50-Ohm Termination.

c. Connect PM101 grounds (2) and Test Oscilloscope probe grounds to Test Fixture 1 black terminal.

d. Disconnect data lines 15 through 0 from PM101 test socket sections B and C (see Fig. 3-1) and connect four channels to Test Fixture 1 red terminal.

e. Disconnect PM101 clock line from test socket pin (See Fig 3-1), and connect clock line and Test Oscilloscope probe to Test Fixture 1 red terminal.

f. Using Test Oscilloscope to measure signal voltage, set PG508 output pulse for high level of +2.4 V and low level of +0.5 V.

g. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, which is desired threshold.

h. Set PG508 TRANSITION TIME control fully counterclockwise (lowest transition time).

i. Set PG508 PERIOD outer control to .2 uS and PERIOD center control fully counterclockwise.

j. Set PG508 NORM/COMPLEMENT switch to out position to select non-inverted output.

k. Set PG508 MODE switches for undelayed mode.

l. Set PG508 DURATION outer control to 10 nS and adjust DURATION center control for 45 nS pulse as displayed on Test Oscilloscope.

m. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

n. Move curson to end of existing program.

o. Press and hold DELETE key until entire program is deleted.

p. Press [] (brackets), NOT, and WD RECOGNIZER keys.

q. Press FORMAT key, select Word Recognizer Address and Data fields binary mode, and press FORMAT key again.

r. Move cursor to Word Recognizer Data field and enter 1's in bit positions corresponding to those connected to PG508 output. (All other bit positions should contain X's.)

s. Press [] (brackets) key.

t. Press TRIGGER key.

u. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

v. Enter 1 to select falling edge of clock. Press END.

w. CHECK - that display is of program as shown in Fig. 3-5.

x. Press START/STOP key to run program.

y. CHECK - that program continues to run.

z. Wait approximately 15 seconds and press START/STOP key to stop program.

aa. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ab. Move cursor to Clock Edge Selection field and enter 0 to select rising edge of clock.

ac. Set PG508 NORM/COMPLEMENT switch to in position to invert output

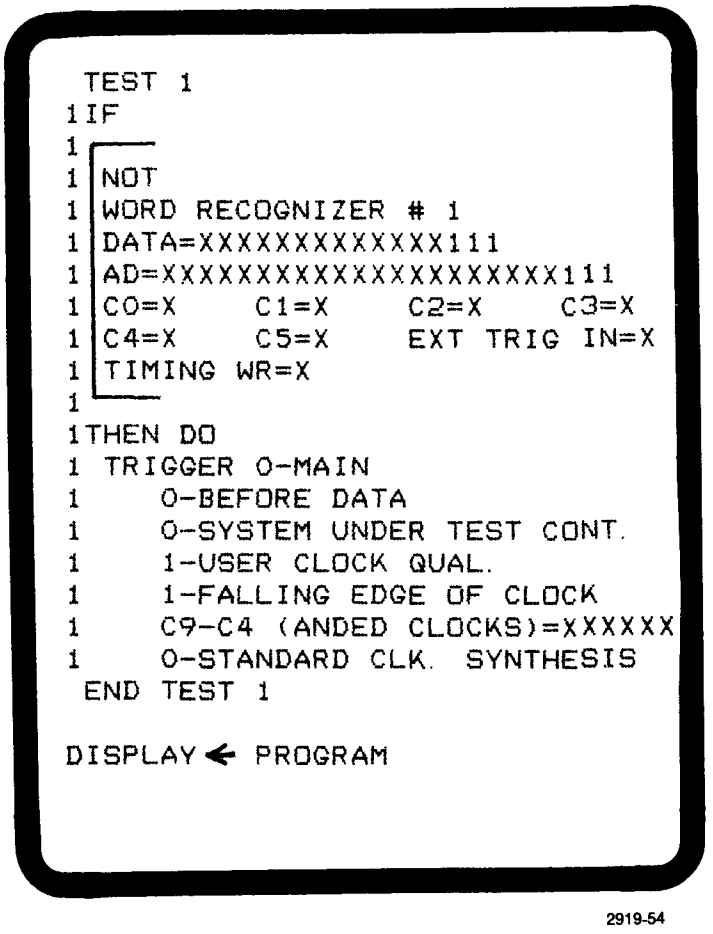


Fig. 3-5. Setup and Hold Data Program.

ad. CHECK - that pulse on Test Oscilloscope display is negative-going and of 45-nS duration.

ae. INTERACTION - If pulse duration is not 45 nS, adjust PG508 DURATION control.

af. Move cursor to Word Recognizer Data field and enter 0's in bit positions in which 0's were entered in part **r**.

ag. Press START/STOP key to run program.

ah. CHECK - that program continues to run.

ai. Wait approximately 15 seconds. then press START/STOP key to stop program.

aj. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ak. Repeat parts **r** through **aj** for groups of approximately four-channels for rest of data channels, all of address channels, and six control bit channels (CØ-C5).

6. Check Setup and Hold, Main Section ANDed Clocks

Equipment required:

PG508
Hook Tips
Test Fixture 1
50-Ohm Termination
Test Oscilloscope

a. Perform parts **a** through **o** of step 5 **except** parts **d**, **i** and **l**. Instead, disconnect control lines C9 through C0 from PM101 test socket section A (see Fig. 3-1) and connect lines C6, C5, and C4 to Test Fixture 1 red terminal; set PG508 PERIOD outer control to 20 uS and turn PERIOD center control fully counterclockwise. Set pulse width to 55 nS.

b. Press ELSE and [] (brackets) keys.

c. Press COUNTER key.

d. Enter 1 to select uS.

e. Press GO TO key.

f. Press [] (brackets) key.

g. Press ELSE key.

h. Press GO TO key.

i. Press [] (brackets) key.

j. Press NOT and COUNTER keys.

k. Enter 00050 (uS).

l. Press [] (brackets) key twice.

m. Press COUNTER key.

n. Move cursor to Counter Command field and enter 2 to select reset and run mode.

o. Press GO TO key and enter 2.

p. Press [] (brackets) key, then ELSE key, then [] key again.

q. Press TRIGGER key.

r. Move cursor to Trigger Delay field and enter 3 to select zero delay.

s. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

t. Enter 1 to select falling edge of clock.

u. Move cursor to C9-C4 ANDed Clocks field and enter 1's in bit positions C6, C5, and C4 (C9, C8, and C7 must be X's).

v. Press GO TO key.

w. Press [] (brackets) key.

x. Press END key to end Test 3, then again to end Test 4.

y. CHECK - that program is as shown in Fig. 3-6A.

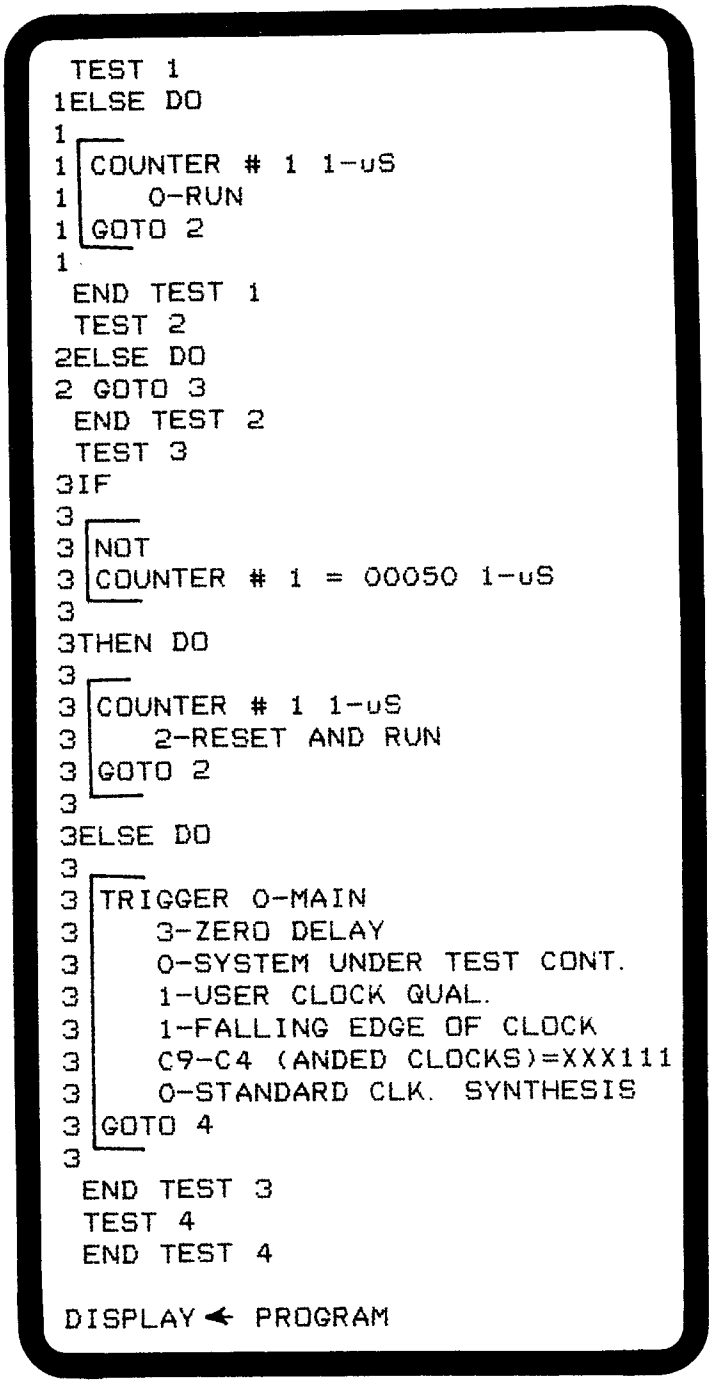


Fig. 3-6A. Setup and Hold ANDed Clocks Program.

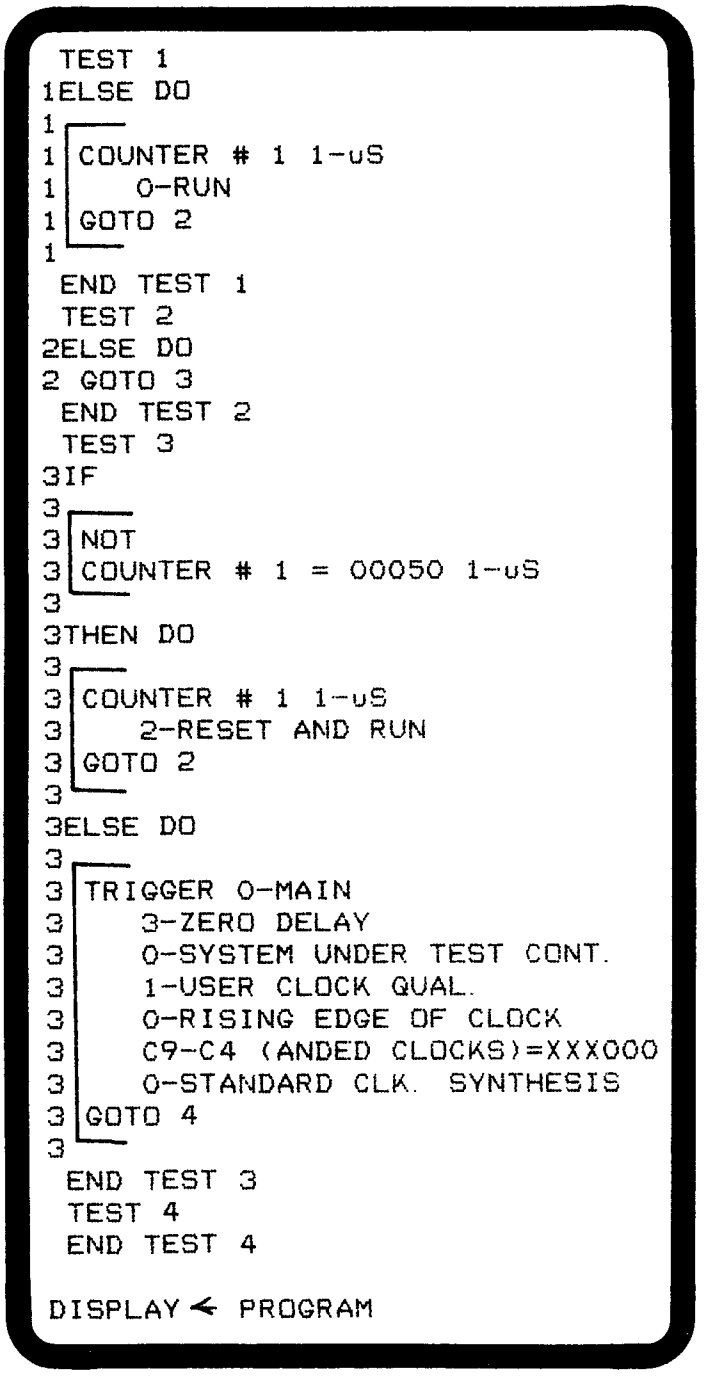


Fig. 3-6B. Setup and Hold ANDed Clocks Program.

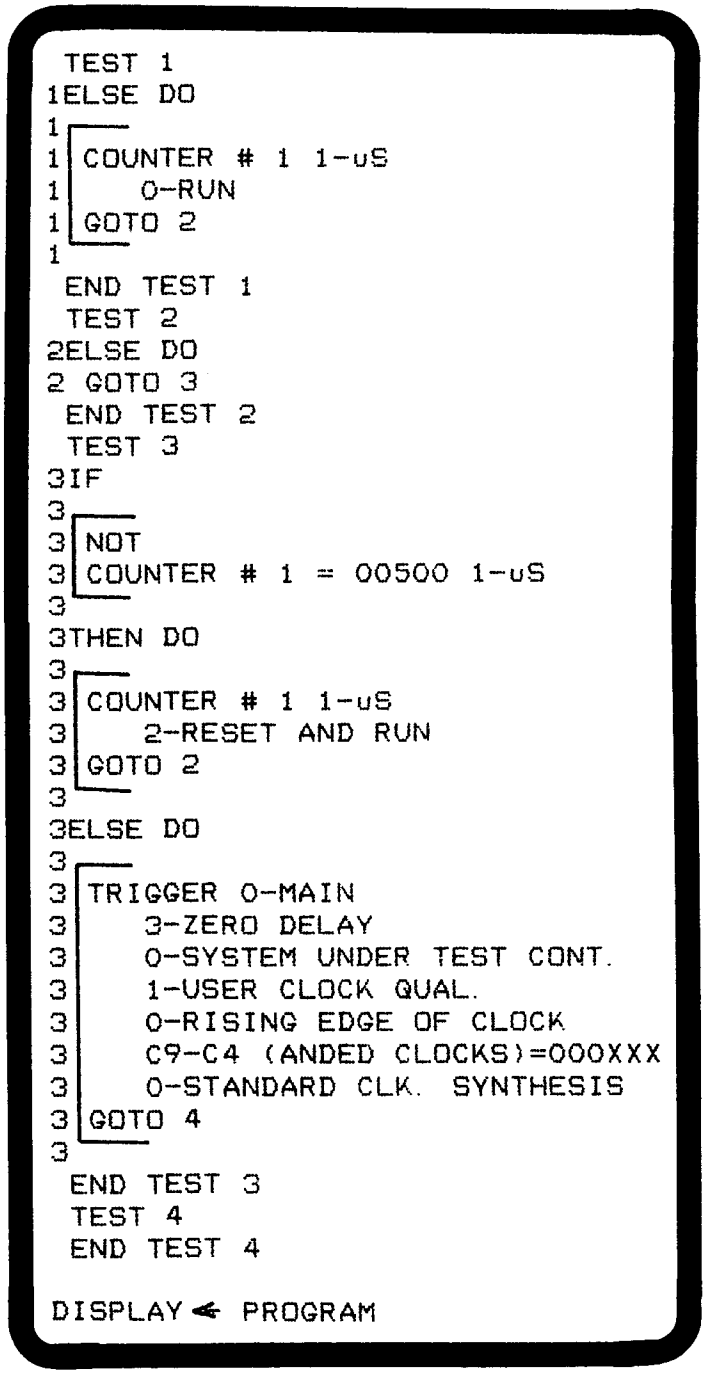


Fig. 3-6C. Setup and Hold ANDed Clocks Program.

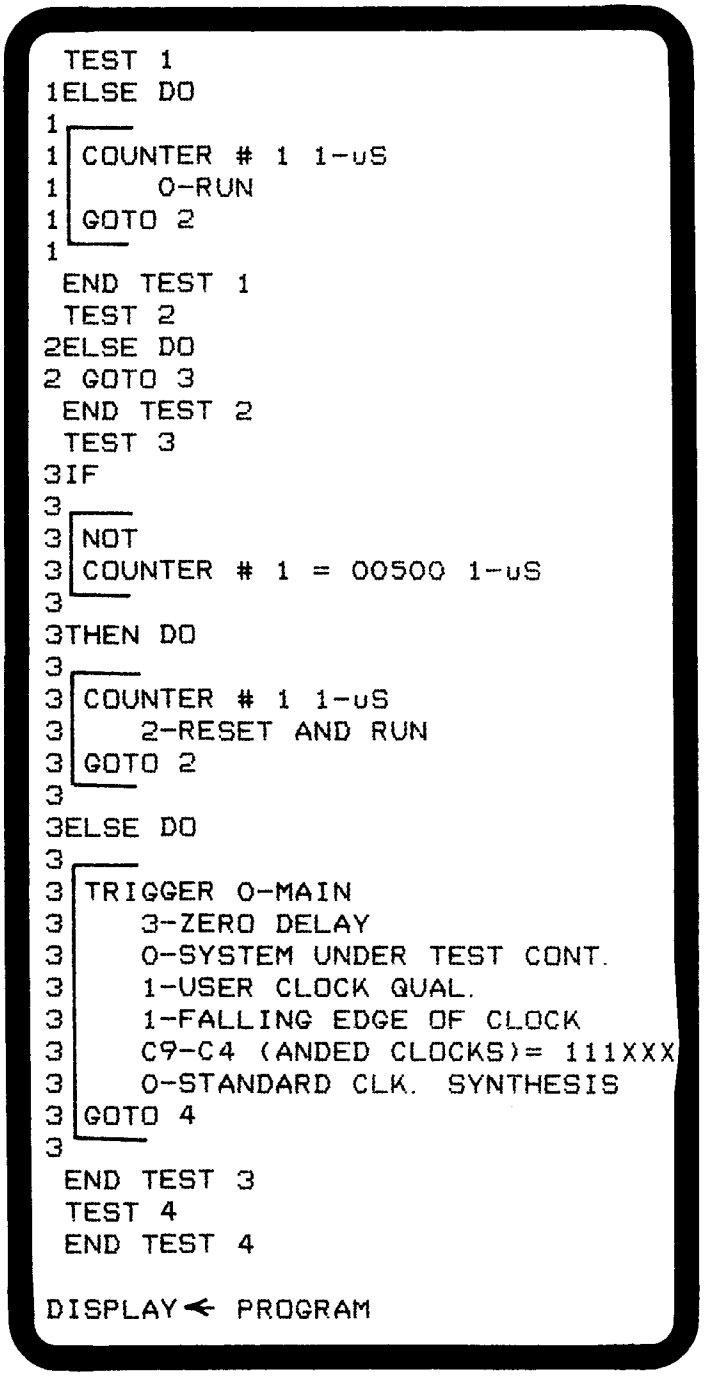


Fig. 3-6D. Setup and Hold ANDed Clocks Program.

z. Press START/STOP key to run program.

aa. CHECK - that program continues to run, with no trigger and no slow clock indication.

ab. Wait approximately 15 seconds and press START/STOP key to stop program.

ac. CHECK - that 255 data words were stored in memory by scrolling data to the last word of memory. The last location should be labeled 254.

ad. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ae. Move cursor to Clock Edge Selection field and enter 0 to select rising edge of clock.

af. Move cursor to C9-C4 ANDed Clocks field and enter 0's in bit positions C6, C5 and C4.

ag. CHECK - that program is as shown in Fig. 3-6B.

ah. Set PG508 NORM/COMPLEMENT switch to in position to invert output.

ai. CHECK - that pulse on Test Oscilloscope display is negative going and of 55-nS duration.

aj. INTERACTION - If pulse duration is not 55 nS, adjust PG608 DURATION control.

ak. Press START/STOP key to run program.

al. CHECK - that program continues to run, with no trigger and no slow clock indication.

am. Wait approximately 15 seconds and press START/STOP key to stop program.

an. CHECK - that 255 data words were stored in memory.

ao. Press IMMEDIATE, DISPLAY and PROGRAM keys.

ap. Move cursor to C9-C4 ANDed Clocks field and enter 0's in bit positions C9, C8, and C7; enter X's in bit positions C6, C5 and C4.

aq. CHECK - that program is as shown in Fig. 3-6C.

ar. Disconnect PM101 control lines C6, C5, and C4 from Test Fixture 1 red terminal and connect PM101 control lines C9, C8, and C7 instead.

as. Press START/STOP key to start program.

at. CHECK - that program continues to run, with no trigger and no slow clock indication.

au. Wait approximately 15 seconds and press START/STOP key to stop program.

av. CHECK - that 255 data words were stored in memory.

aw. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ax. Move cursor to Clock Edge Selection field and enter 1 to select falling edge of clock.

ay. Enter 1's in C9-C4 ANDed Clocks field bit positions C9, C8, and C7.

az. CHECK - that program is as shown in Fig. 3-6D.

ba. Set PG508 NORM/COMPLEMENT switch to out position to invert output.

bb. CHECK - that pulse on Test Oscilloscope display is positive-going and of 55-nS duration.

bc. INTERACTION - If pulse duration is not 55 nS, adjust PG508 DURATION control.

bd. Press START/STOP key to start program.

be. CHECK - that program continues to run, with no trigger and no slow clock indication.

bf. Wait approximately 15 seconds and press START/STOP key to stop program.

bg. CHECK - that 255 data words were stored in memory.

7. Check Setup and Hold, Main Section ESYNC and WAIT

Equipment required:

PG508
Hook Tips
Test Fixture 1
50-Ohm Termination
Test Oscilloscope

ESYNC Section

a. Perform parts **a** through **o** of step 5 **except** parts **i** and **l**. Instead, disconnect control lines C9 through C0 from PM101 test socket section A (see Fig. 3-1) and connect control lines C6 and C8 (ESYNC) to Test Fixture 1 red terminal; set PG508 PERIOD outer control to 20 uS and turn PERIOD center control fully counterclockwise. Set PG508 duration to 55 nS.

b. Press COUNTER key and enter 2 for counter #.

c. Enter 10 events.

d. Press [] (brackets) key.

e. Press TRIGGER key.

f. Move cursor to Trigger Delay Field and enter 3 to select zero delay.

g. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

h. Enter 1 to select falling edge of clock. Enter "X" in C4-C9.

i. Move cursor to clock synthesis field and enter 1 to select user clock synthesis.

j. Enter 1 to select divide clock; and enter 2 to divide clock by 2.

k. Enter 1 in ESYNC bit 6 position.

l. Press COUNTER key and enter 1 for Counter #.

m. Enter 1 to select uS.

n. Enter 1 to select stop command.

o. Press GO TO key.

p. Press [] (brackets) key, ELSE key, and [] (brackets) key again.

q. Press COUNTER key.

r. Press COUNTER key again and enter 2 for Counter #.

s. Press [] (brackets) key.

t. Press END key twice to end Tests 1 and 2.

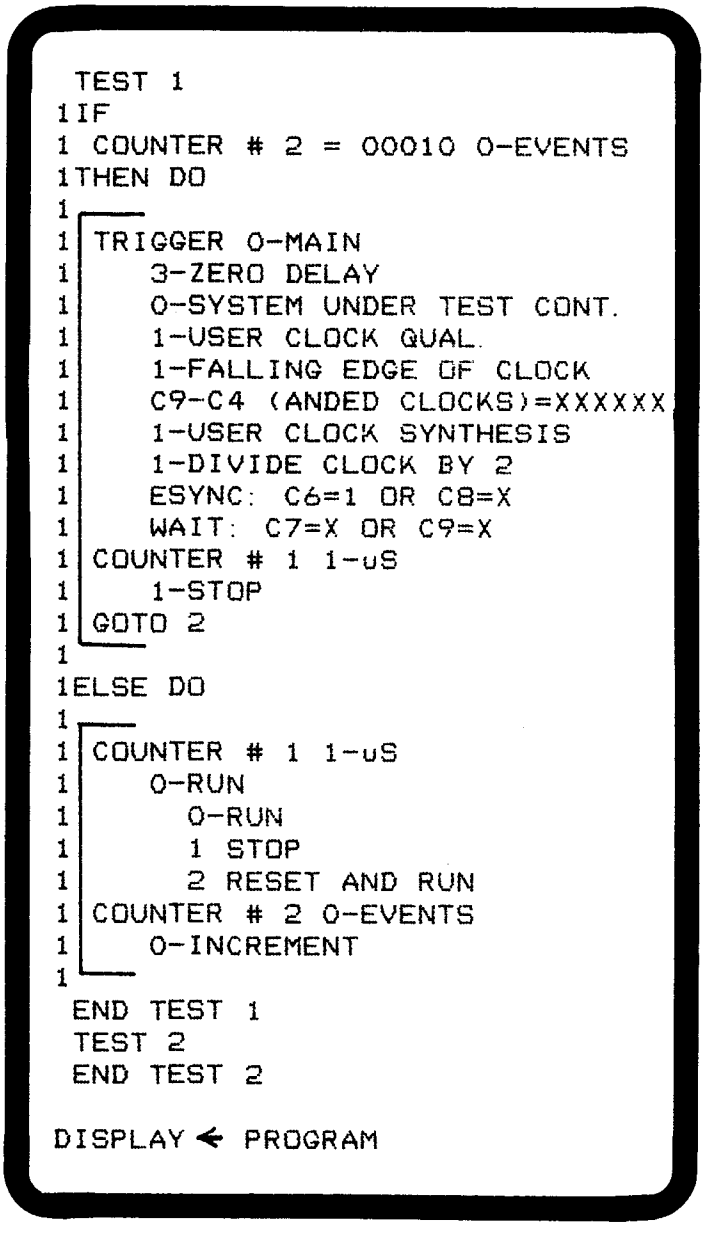
u. CHECK - that program is as shown in Fig. 3-7.

v. Press START/STOP key to run program.

w. CHECK - that count stored in Counter #1 is approximately 200 uS (ten times PG508 period).

x. Repeat parts **v** and **w** several more times.

y. Press IMMEDIATE, DISPLAY, and PROGRAM keys.



2919-59

Fig. 3-7. Setup and Hold, ESYNC Program.

z. Move cursor to Divide Clock field and enter 3 to select divide by 3.

aa. Press START/STOP key.

ab. CHECK - that program runs continuously, with slow clock indications.

ac. Wait approximately 15 seconds and press START/STOP key to stop program.

ad. CHECK - that no data were stored in memory.

ae. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

af. Move cursor to Clock Edge Selection field and enter 0 to select rising edge of clock.

ag. Move cursor to ESYNC C6 bit position and enter 0.

ah. Set PG508 NORM/COMPLEMENT switch to in position to invert output.

ai. CHECK - that pulse on Test Oscilloscope display is negative-going and of 55-nS duration.

aj. INTERACTION - If pulse duration is not 55 nS, adjust PG508 DURATION control.

ak. Press START/STOP key to run program.

al. CHECK - that program runs continuously, with slow clock indication.

am. Wait approximately 15 seconds and press START/STOP key to stop program.

an. CHECK - that no data were stored in memory.

ao. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ap. Move cursor to Divide Clock field and enter 2 to select divide by 2.

aq. Press START/STOP key to run program.

ar. CHECK - that count stored in Counter #1 is approximately 200 uS.

as. Repeat parts **aq** and **ar** several times.

at. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

au. Move cursor to ESYNC C6 bit position and enter X.

av. Enter 0 in C8 bit position.

aw. Press START/STOP key to run program.

ax. CHECK - that count stored in Counter #1 is approximately 200 uS.

ay. Repeat parts **aw** and **ax** several times.

az. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ba. Move cursor to Divide Clock field and enter 3 to select divide by 3.

bb. Press START/STOP key to run program.

bc. CHECK - that program runs continuously, with slow clock indication.

bd. Wait approximately 15 seconds and press START/STOP key to stop program.

be. CHECK - that no data were stored in memory.

bf. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bg. Move cursor to Clock Edge Selection field and enter 1 to select falling edge of clock.

bh. Move cursor to ESYNC C8 bit position and enter 1.

bi. Set PG508 NORM/COMPLEMENT switch to out position (NORM).

bj. CHECK - that pulse on Test Oscilloscope display is positive-going and of 55-nS duration.

bk. INTERACTION - If pulse duration is not 55-nS, adjust PG608 DURATION control.

bl. Press START/STOP key to run program.

bm. CHECK - that program runs continuously, with slow clock indication.

bn. Wait approximately 15 seconds and press START/STOP key to stop program.

bo. CHECK - that no data were stored in memory.

bp. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bq. Move cursor to Divide Clock field and enter 2 to select divide by 2.

br. Press START/STOP key to run program.

bs. CHECK - that count stored in Counter #1 is appxomately 200 uS. 210 uS.

bt. Repeat parts **br** and **bs** several times.

WAIT Section

bu. Disconnect PM101 control lines C6 and C8 (ESYNC) from Test Fixture 1 red terminal; connect instead PM101 control lines C7 and C9 (WAIT) to red terminal.

bv. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bw. Move cursor to ESYNC C8 bit position and enter X.

bx. Move cursor to WAIT C7 bit position and enter 1.

by. CHECK - that program is as shown in Fig. 3-8.

@

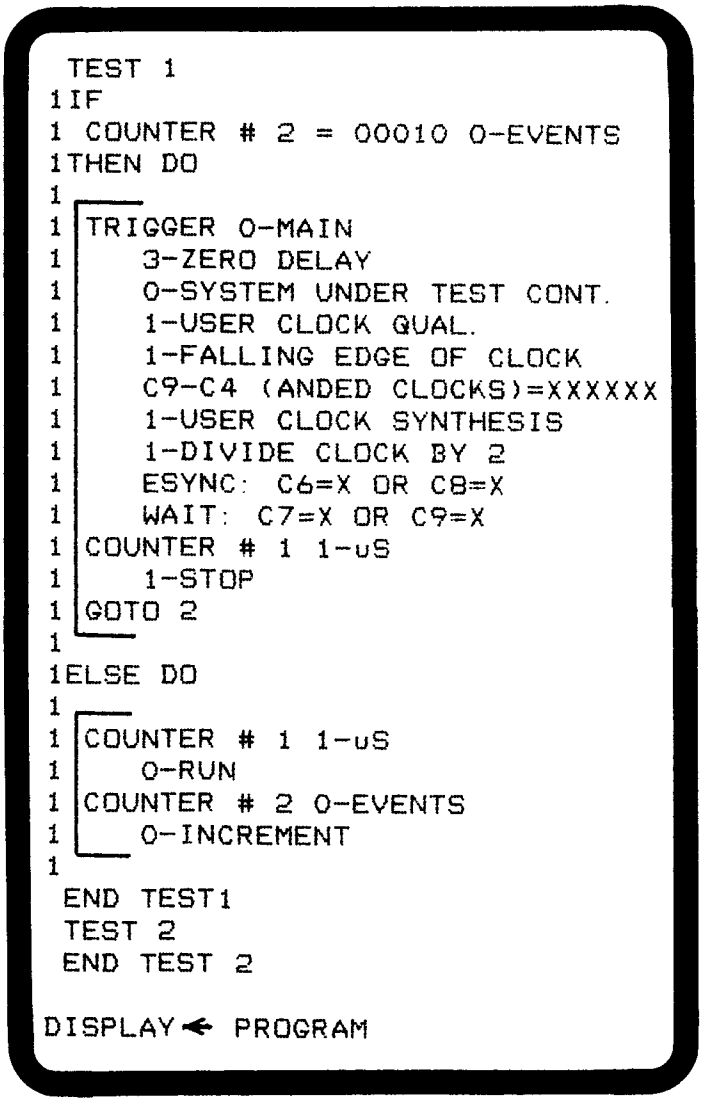


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Fig. 3-8. Setup and Hold, WAIT Program.

bz. CHECK - that pulse in Test Oscilloscope display is positive-going and of 55-nS duration.

ca. INTERACTION - If pulse duration is not 55 nS, adjust PG608 DURATION control.

cb. Press START/STOP key to run program.

cc. CHECK - that program runs continuously, with slow clock indication.

cd. Wait approximately 15 seconds and press START/STOP key to stop program.

ce. CHECK - that no data were stored in memory as shown in Fig. 3-9.

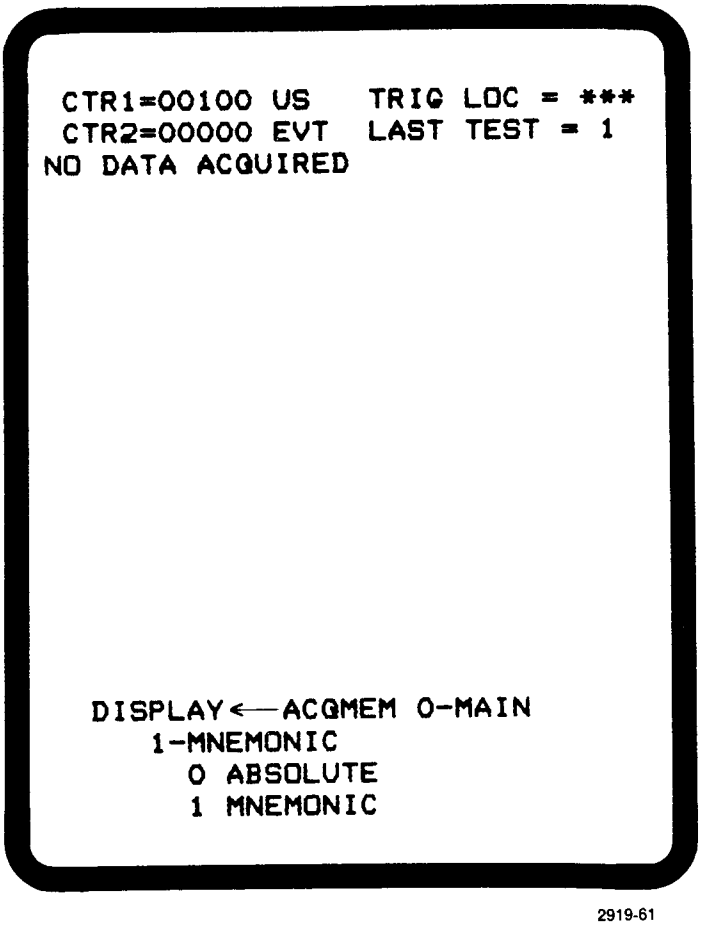

Fig. 3-9. WAIT Program Result (No Data Stored).

cf. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

cg. Move cursor to ESYNC C7 bit position and enter X.

ch. Move cursor to WAIT C9 bit position and enter 1.

ci. Press START/STOP key to run program.

cj. CHECK - that program runs continuously, with slow clock indication.

ck. Wait approximately 15 seconds and press START/STOP switch to stop program.

cl. CHECK - that no data were stored in memory.

cm. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

cn. Move cursor to Clock Edge Selection field and enter 0 to select rising edge of clock.

co. Move cursor to WAIT C9 bit position and enter 0.

cp. Set PG508 NORM/COMPLEMENT switch to in position to invert output.

cq. CHECK - that pulse on Test Oscilloscope display is negative-going and of 55-nS duration.

cr. INTERACTION - If pulse duration is not 55 nS, adjust PG508 DURATION control.

cs. Press START/STOP key to run program.

ct. CHECK - that program runs continuously, with slow clock indication.

cu. Wait approximately 15 seconds and press START/STOP key to stop program.

cv. CHECK - that no data were stored in memory.

cw. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

cx. Move cursor to WAIT C7 bit position and enter 0.

cy. Enter X in C9 bit position.

cz. Press START/STOP key to run program.

da. CHECK - that program runs continuously, with slow clock indication.

db. Wait approximately 15 seconds and press START/STOP key to stop program.

dc. CHECK - that no data were stored in memory.

8. Check Minimum Clock Pulse Width (25 nS), Minimum Clock Period (100 nS), Minimum Data Acquisition Period (100 nS), and Minimum Interval Between Qualified Clocks

Equipment required:

Test Oscilloscope
PG502
PG508
Coaxial Cable
Test Fixture 1 (2)
50-Ohm Termination
Hook Tips

a. Using coaxial cable, connect PG502 + TRIG OUT connector to PG508 TRIG/GATE IN connector.

b. Connect Test Fixture 1 to PG502 output connector.

c. Connect PM101 ground (2) and Test Oscilloscope channel 1 probe ground to PG502 Test Fixture 1 black terminal.

d. Connect PM101 clock and Test Oscilloscope channel 1 probe to PG502 Test Fixture 1 red terminal.

e. Pull PG502 BACK TERM switch to out position.

f. Set PG502 PERIOD control to .1 uS and turn PERIOD VARIABLE control fully counterclockwise (X1 position).

g. Using Test Oscilloscope to measure signal voltage, adjust PG502 output controls for high level of +2.4 V and low level of +0.5 V.

h. Set PG502 COMPLEMENT NORM switch to in position to invert output.

i. Set PG502 PULSE DURATION control to 5 nS and adjust PULSE DURATION VARIABLE control for 25-nS negative-going pulse on Test Oscilloscope. Set period control for 100 nS.

j. Connect 50-Ohm Termination to PG508 OUTPUT connector.

k. Connect second Test Fixture 1 to 50-Ohm Termination.

l. Connect Test Oscilloscope channel 2 probe ground to second Test Fixture 1 black terminal.

m. Connect PM101 data lines 0 through 3 and Test Oscilloscope channel 2 probe to second Test Fixture 1 red terminal.

n. Turn PG508 PERIOD control fully clockwise (to EXT TRIG position).

o. Set PG508 TRIGGERING switches to out positions.

p. Adjust PG508 TRIG/GATE LEVEL control so that TRIG'd/GATED LED indicator above control blinks (which indicates that PG508 is triggering on input signal from PG502).

q. Using Test Oscilloscope channel 2 to measure signal voltage, set PG508 output pulse for high level of +2.4 V and low level of +0.5 V.

r. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, which is threshold level.

s. Set PG508 NORM/COMPLEMENT switch to its normal, out position.

t. Set PG508 TRANSITION TIME controls fully counterclockwise (lowest transition time).

u. CHECK - that PG508 output pulse on Test Oscilloscope display (channel B) is positive-going and of 45-nS duration at center graticule line.

v. INTERACTION - If pulse duration is not 45 nS, adjust PG508 DURATION control.

w. Set PG508 DELAY switches for delay mode (lower switch to in position).

x. Adjust PG508 DELAY controls so that the falling edge of the PG508 pulse is coincident with the rising edge of the PG502 pulse at the center graticule line.

y. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

z. Move cursor to end of existing program.

aa. Press and hold DELETE key until entire program is deleted.

ab. Press COUNTER key and enter 10000 events.

ac. Press [] (brackets) key.

ad. Press COUNTER key and enter 2 for Counter #.

ae. Enter 1 to select uS.

af. Enter 1 to select stop command.

ag. Press GO TO key.

ah. Press [] (brackets) key twice.

ai. Press NOT key, then WD RECOGNIZER key.

aj. Press FORMAT key, binary for Word Recognizer Address and Data fields, and press FORMAT key again.

ak. Enter 1's in Word Recognizer Data bit positions 3, 2, 1, and 0. Enter X in C4 and C5.

al. Press [] (brackets) key twice.

am. Press TRIGGER key.

an. Move cursor to Trigger Delay field and enter 3 to select zero delay.

ao. Move cursor to Clock Qualification field and enter 0 to select standard clock qualification.

ap. Press GO TO key and enter 3.

aq. Press [] (brackets) key, ELSE key, then [] (brackets) key again.

ar. Press COUNTER key, enter 0 for events.

as. Press COUNTER key and enter 2 for Counter #.

at. Press [] (brackets) key twice.

au. Press COUNTER key and enter 2 for Counter #.

av. Enter 1050 uS.

aw. Press OR key, then NOT key.

ax. Press WD RECOGNIZER key and enter 1 for Word Recognizer #.

ay. Press [] (brackets) key twice.

az. Press TRIGGER key.

ba. Press GO TO key, the [] (brackets) key.

bb. Press ELSE key.

bc. Press [] (brackets) key.

bd. Press COUNTER key.

be. Enter 1 to select reset command.

bf. Press COUNTER key and enter 2 for Counter #.

bg. Enter 1 to select uS.

bh. Enter 2 to select reset and run command.

bi. Press GO TO key and enter 1.

bj. Press [] (brackets) key.

bk. Press END key to end Test 2 and again to END Test 3.

bl. CHECK that program is as shown in Fig. 3-10.

bm. Press START/STOP key to run program.

bn. CHECK - that program runs continuously, with no trigger.

bo. Wait approximately 15 seconds and press START/STOP key to stop program.

bp. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bq. Move cursor to Clock Qualification field in Test 2 and enter 1 to select user clock qualification.

br. Enter 1 to select falling edge of clock.

bs. Set PG502 NORM/COMPLEMENT switch to out position for normal output.

bt. CHECK that PG502 output pulse on Test Oscilloscope display is positive-going and of 25-nS duration.

bu. INTERACTION - If pulse duration is not 25 nS, adjust PG502 PULSE DURATION VARIABLE control.

bv. Press START/STOP key to run program.

bw. CHECK - that program runs continuously.

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Fig. 3-10. Clock Check Program.

bx. Press START/STOP key to stop program.

by. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

bz. Move cursor to Word Recognizer Data field and enter 0's in data bit positions 3, 2, 1, and 0.

ca. Set PG508 NORM/COMPLEMENT switch to in position to invert output.

cb. CHECK - that PG508 output pulse on Test Oscilloscope display is negative-going and of 45-nS duration.

cc. INTERACTION - If pulse duration is not 45 nS, adjust PG508 DURATION control.

cd. Press START/STOP key to run program.

ce. CHECK that program runs continuously while triggering on falling edge of clock with 0's on data lines.

cf. Press START/STOP key to stop program.

cg. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ch. Move cursor to Clock Edge field and enter 0 to select rising edge of clock.

ci. Set PG502 NORM/COMPLEMENT switch to in position to invert output.

cj. CHECK - that PG502 output pulse on Test Oscilloscope display is negative-going and of 25-nS duration.

ck. INTERACTION - If pulse duration is not 25 nS, adjust PG502 PULSE DURATION VARIABLE control.

cl. Press START/STOP key to run program.

cm. CHECK - that program runs continuously while triggering on rising edge of clock with 0's on data lines.

9. Check Counter Accuracy

Equipment required:

TG501
PG508
50-Ohm Termination
Test Fixture 1
Coaxial Cable
Hook Tips
Test Oscilloscope

a. Connect 50-Ohm Termination to PG508 OUTPUT connector.

b. Connect Test Fixture 1 to 50-Ohm Termination.

c. Connect PM101 and Test Oscilloscope probe grounds to Test Fixture 1 black terminal.

d. Connect PM101 clock lead and Test Oscilloscope probe to Test Fixture 1 red terminal.

e. Using coaxial cable, connect TG501 MARKER OUT connector to PG508 TRIG/GATE IN connetor.

f. Set TG501 MARKER control to 50 mS and press button in control center to select calibrated operation.

g. Set PG508 PERIOD control to EXT TRIG.

h. Press PG508 MODE UNDLY switch.

i. Set PG508 DURATION output control to 10 nS and adjust the DURATION VARIABLE control for a 25 nS pulse width at the center graticule line.

j. Using Test Oscilloscope to measure signal voltage, set PG508 output pulse for high level of +2.4 V and low level of +0.4 V.

k. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, which is desired threshold.

l. Adjust PG508 TRIG/GATE LEVEL control so that TRIG'D/GATED LED indicator above control blinks (which indicates that PG508 is triggering on input from TG501).

m. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

n. Move cursor to end of existing program.

o. Press and hold DELETE key until entire program is deleted.

p. Press ELSE key.

q. Press [] (brackets) key.

r. Press COUNTER key and enter 2 for Counter #.

s. Enter 1 to select uS.

t. Press GO TO key, then press [] (brackets) key.

u. Press ELSE key, then [] (brackets) key.

v. Press COUNTER key and enter 2 for Counter #.

w. Enter 1 to select stop command.

x. Press TRIGGER key.

y. Move cursor to Trigger Delay field and enter 3 to select zero delay.

z. Move cursor to Clock Qualification field and enter 0 to select standard clock qualification.

aa. Press [] (brackets) key.

ab. Press COUNTER key.

ac. Enter 399 events.

ad. Press GO TO key and enter 2, press ELSE, then press [] (brackets) key.

ae. Press COUNTER key.

af. Press COUNTER key and enter 2 for Counter #.

ag. Press [] (brackets) and end keys.

ah. CHECK - that program is as shown in Fig. 3-11.

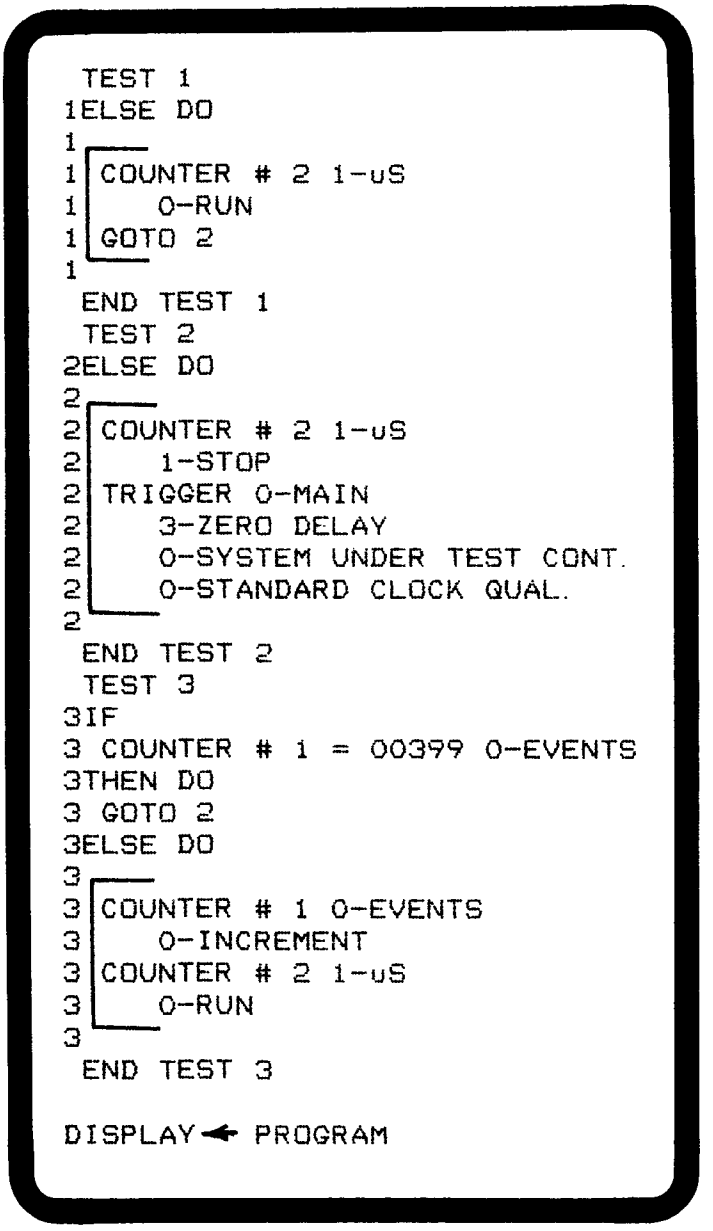


Fig. 3-11. Counter Accuracy Program 1.

ai. Press START/STOP key to run program.

aj. CHECK - that Counter #1 contains 0 and Counter #2 contains 50000 ±6 uS.

ak. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

al. Move cursor to Counter Mode field and enter 2 to select mS.

am. CHECK - that program is as shown in Fig. 3-12.

an. Press IMMEDIATE, GO TO, 3, and right-hand cursor movement keys.

ao. CHECK - that program runs continuously, with slow clock indication.

ap. Wait approximately 20 seconds for trigger to occur.

aq. CHECK - that Counter #1 contains 399 and Counter #2 contains 20000 ±3 mS.

ar. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

as. Move cursor to Test 1 counter number and change 2 to 1.

at. Enter 1 to select uS.

au. Move cursor to Test 2 counter number and change 2 to 1.

av. Move cursor to Test 3 first counter number and change 1 to 2.

aw. Enter 399 and enter 0 to select events mode.

ax. Press START/STOP key to run program.

ay. CHECK - that Counter #1 contains 50000 ±6 uS and Counter #2 contains 0.

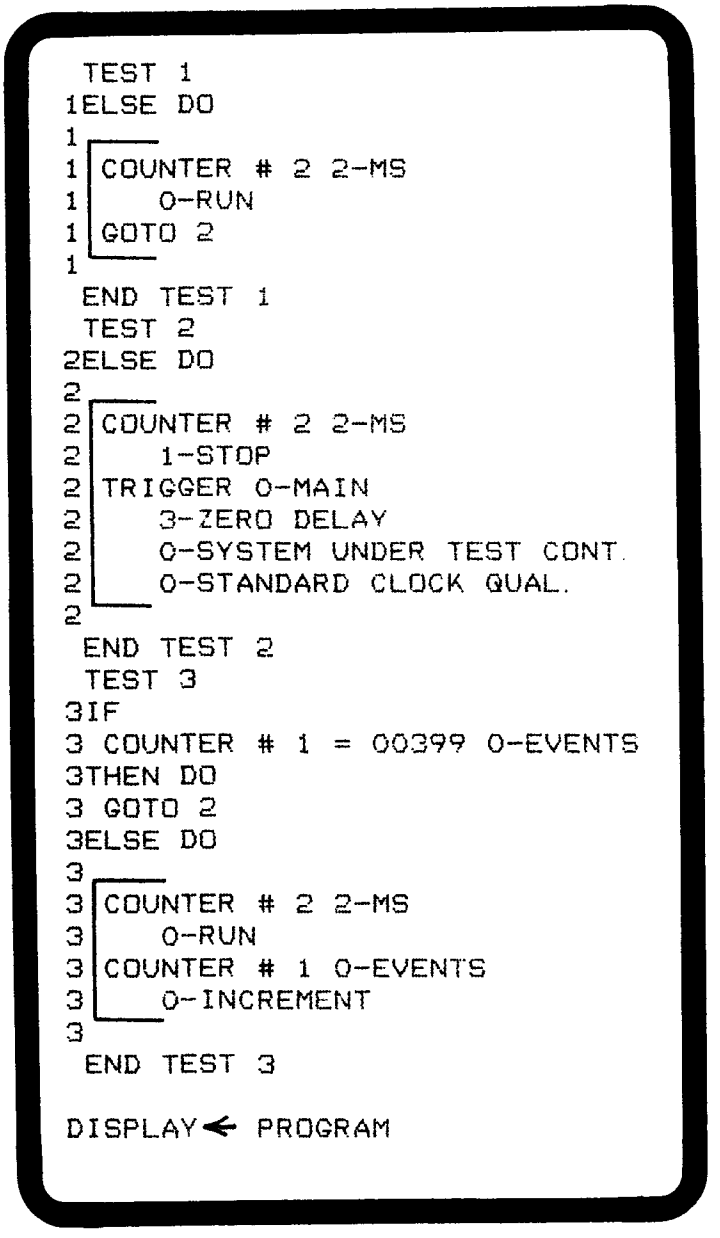


Fig. 3-12. Counter Accuracy Program 2.

az. Press IMMEDIATE, DISPLAY and PROGRAM keys.

ba. Move cursor to Test 1 Counter Period field and enter 2 to select mS

bb. Press IMMEDIATE, GO TO, 3, and right-hand cursor movement keys.

bc. CHECK - that program runs, with slow clock indication.

bd. Wait approximately 20 seconds.

be. CHECK - that Counter #1 contains 20000 ±3 mS and Counter #2 contains 399.

10. Check External Trigger In Input Resistance

Equipment required:

DM501A
BNC to Dual Binding Post Adapter

a. Connect BNC to Dual Binding Post Adapter to TRIG IN connector.

b. Connect DM501A test leads to binding posts with positive meter lead to red binding post.

c. Set DM501A to 2M ohm scale.

d. CHECK - that resistance is between 980 kohms and 1.02 Mohms.

11. Check External Trigger Setup and Hold

Equipment required:

PG508
PG502
BNC Elbow
BNC T
Probe Tip to BNC Adapter
Test Oscilloscope
Coaxial Cable (2)
50-Ohm Termination
BNC to Dual Binding Post Adapter

a. Connect BNC Elbow to 7D02 TRIG IN connector.

b. Connect BNC T to BNC Elbow.

c. Using coaxial cable, connect PG502 OUTPUT connector to BNC T.

d. Pull PG502 BACK TERM switch to out position.

e. Connect Probe Tip to BNC Adapter to remaining section of BNC T.

f. Remove retractable hook tip from Test Oscilloscope channel 1 probe and connect probe to Probe Tip to BNC Adapter.

g. Using coaxial cable, connect PG502 + TRIG OUT connector to PG508 TRIG/GATE IN connector.

h. Set PG502 PERIOD control to .1 uS and adjust PERIOD VARIABLE control for 200 nS period as measured on Test Oscilloscope.

i. Set PG502 NORM/COMPLEMENT switch to in position (COMP).

j. Set PG502 PULSE DURATION control to 10 nS and adjust PULSE DURATION VARIABLE control for pulse with of 28 nS as measured on Test Oscilloscope.

k. Connect 50-Ohm Termination to PG508 OUTPUT connector.

l. Connect BNC to Dual Binding Post Adapter to 50-ohm Termination.

m. Connect PM101 and Test Oscilloscope channel 2 grounds to BNC to Dual Binding Post Adapter black terminal.

n. Connect PM101 clock line and Test Oscilloscope channel 1 probe to BNC to Dual Binding Post Adapter red terminal.

o. Set PG508 PERIOD control to EXT TRIG.

p. Press PG508 MODE DELAY switch in.

q. Set PG508 COMPLEMENT switch to out position (NORM).

r. Set PG508 DURATION outer control to 10 nS and adjust DURATION center control for pulse duration of 100 nS.

s. Adjust PG508 TRIG/GATE LEVEL control so that TRIG'D/GATED LED indicator blinks.

t. Set PG508 TRANSITION TIME, LEADING, and TRAILING controls fully counterclockwise.

u. Using Test Oscilloscope to measure signal voltage, adjust PG508 output pulse for high level of +2.4 V and low level of +0.4 V.

v. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, which is desired threshold level.

w. Set PG508 DELAY outer control to 10 nS and adjust DELAY center control so that rising edge of output is 10 nS after PG502 output pulse rising edge.

x. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

y. Move cursor to end of existing program.

z. Press and hold DELETE key until entire program is deleted.

aa. Press WD RECOGNIZER key.

ab. Move cursor to External Trigger In field and enter 0. (All other fields should contain X's.)

ac. Press [] (brackets) key, then TRIGGER key. Move cursor to Delay field and enter 0 for before data.

ad. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

ae. Enter 0 to select rising edge of clock.

af. Press TRIGGER key and enter 1 to select Timing Option Section. Enter 0 into Delay field for before data.

ag. Press [] (brackets) key.

ah. Press END key to end Test 1.

ai. CHECK - that program is as shown in Fig. 3-13.

aj. Press START/STOP key to run program.

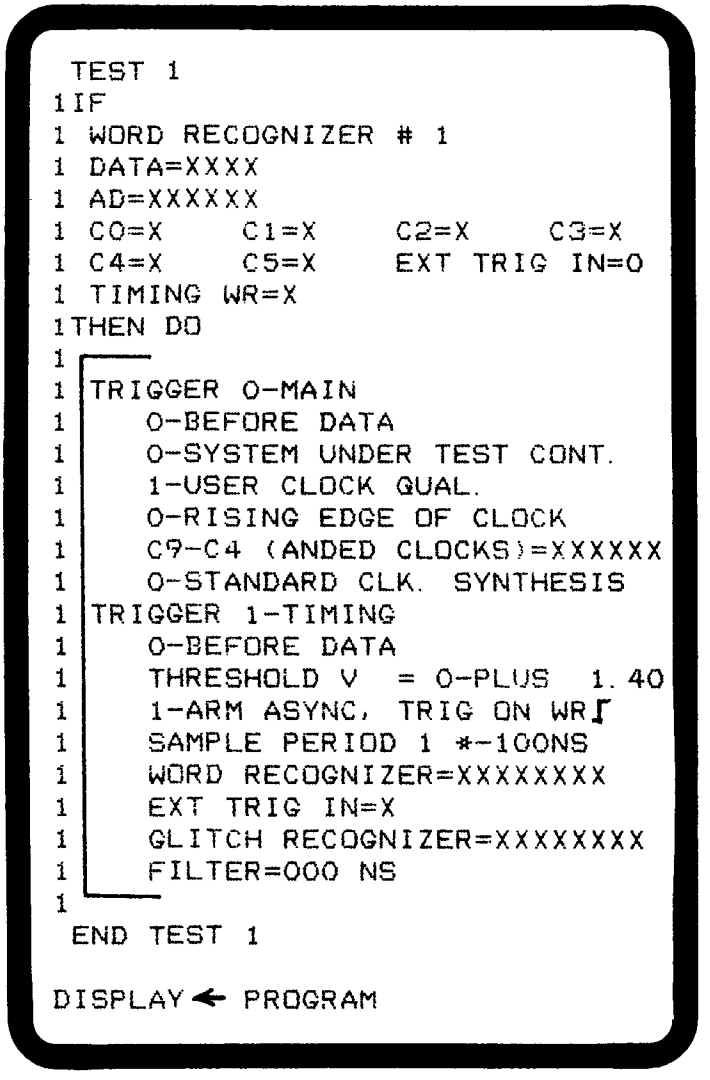


Fig. 3-13. External Trigger Setup and Hold Program.

ak. CHECK - that program runs continuously with no trigger.

al. Wait approximately 15 seconds and press START/STOP key to stop program.

am. Set PG502 NORM/COMPLEMENT switch to in position to invert output.

an. CHECK - that PG502 output pulse on Test Oscilloscope display is negative-going and of 28-nS duration.

ao. INTERACTION - If pulse duration is not 28 nS, adjust PG502 PULSE DURATION VARIABLE control.

ap. CHECK - that rising edge of PG508 output pulse occurs 10 nS after PG502 output pulse falling edge.

aq. INGERACTION - If PG508 output pulse is not positioned properly, adjust PG508 DELAY control.

ar. Press START/STOP key.

as. Press IMMEDIATE, DISPLAY and PROGRAM keys.

at. Move cursor to Word Recognizer External Trigger In field and change 0 to 1.

au. Press START/STOP key.

av. CHECK - that program runs, with no trigger.

12. Check Asynchronous Mode Pulse Width In

Equipment required:

PG502
BNC T
BNC Elbow
Probe Tip to BNC Adapter
Coaxial Cable
Test Oscilloscope

a. Make certain that PM101 self-test jumper J5050 (see Fig. 3-1) is in on position.

b. Connect BNC Elbow to 7D02 front panel TRIG IN connector.

c. Connect BNC T to BNC Elbow above.

d. Connect Probe Tip to BNC Adapter to BNC T above

e. Using Coaxial Cable, connect BNC T above to PG502 output connector.

f. Pull PG502 BACK TERM switch to out position.

g. Remove retractable hook tip from Test Oscilloscope probe and connect probe to Probe Tip to BNC Adapter.

h. Using Test Oscilloscope to measure signal voltage, set PG502 output pulse for high level of +2.4 V and low level of +0.4 V.

i. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V.

j. Set PG502 PULSE DURATION control to 5 nS and adjust PULSE DURATION VARIABLE control for 25-nS pulse at center graticule line on Test Oscilloscope display.

k. Recheck signal levels as in part **h**.

l. Set PG502 PERIOD control to EXT TRIG (to employ manual triggering).

m. Make certain that PG502 NORM/COMPLEMENT switch is set to NORM position.

n. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

o. Move cursor to end of existing program.

p. Press and hold DELETE key until entire program is deleted.

q. Press ELSE key.

r. Press TRIGGER key and enter 1 to select Timing Option Section.

s. Move cursor to Timing Mode field and enter 1 to arm async trigger on Word Recognizer true.

t. Select sample period of 20 nS.

u. Enter filter value of 000 nS.

v. Move cursor to External Trigger In field and enter 1.

w. Press START/STOP key to run program.

x. CHECK - that program runs continuously.

y. Press PG502 MAN TRIG switch once.

z. CHECK - that display indicates that trigger occurred.

aa. Repeat parts **w** through **z** approximately 20 times to ensure that each single pulse is recognized.

ab. Set PG502 NORM/COMPLEMENT switch to in position to complement output.

ac. Set PG502 PERIOD control to 1 uS.

ad. CHECK - that PG502 output pulse on Test Oscilloscope Display is negative-gain and of 25-nS duration at center graticule line.

ae. INTERACTION - If pulse is not 25 nS, adjust PG502 PULSE DURATION VARIABLE control.

af. Set PG502 PERIOD control to EXT TRIG again.

ag. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ah. Move cursor to External Trigger In field and enter 0.

ai. Press START/STOP key to run program.

aj. CHECK - that program runs continuously.

ak. Press PG502 MAN TRIG switch once.

al. CHECK - that display indicates that trigger occurred.

am. Repeat parts **ai** through **al** approximately 20 times to ensure that each single pulse is recognized.

13. Check Setup and Hold, Timing Option Section Data

Equipment required:

Test Oscilloscope
PG508
PG502
50-Ohm Termination (2)
Test Fixture 1 (2)
Hook Tips
Coaxial Cable

a. Connect 50-ohm Termination to PG502 OUTPUT connector.

b. Connect Test Fixture 1 to 50-Ohm Termination.

c. Connect Test Oscilloscope channel 1 probe ground to Test Fixture 1 black terminal.

d. Connect Test Oscilloscope channel 1 probe to Test Fixture 1 red terminal.

e. Using Hook Tips, connect eight channels of P6451 to Test Fixture 1 red terminal.

f. Using Hook Tip, connect P6451 ground to Test Fixture 1 black terminal.

g. Connect second 50-Ohm Termination to PG508 OUTPUT connector.

h. Connect second Test Fixture 1 to 50-Ohm Termination above.

i. Connect Test Oscilloscope channel 2 probe ground to second Test Fixture 1 black terminal.

j. Connect Test Oscilloscope channel 2 probe to second Test Fixture 1 red terminal.

k. Connect PM101 clock lead to second Test Fixture 1 red terminal.

l. Connect PM101 grounds to second Test Fixture 1 black terminal.

m. Set PG502 PERIOD control to .1 uS.

n. Turn PG502 PERIOD VARIABLE control fully counterclockwise (to X1 position).

o. Make certain that PG502 NORM/COMPLEMENT switch is set to out (NORM) position.

p. Set PG502 PULSE DURATION control to 5 nS and adjust PULSE DURATION VARIABLE control for 22-nS pulse on Test Oscilloscope channel 1.

q. Pull PG502 BACK TERM switch to out position.

r. Using Test Oscilloscope to measure signal voltage adjust PG502 OUTPUT (VOLTS) controls for output high level of +2.4 V and low level of +0.4 V on channel 1.

s. Using Coaxial Cable, connect PG502 + TRIG OUT connector to PG508 TRIG/GATE IN connector.

t. Adjust PG508 TRIG/GATE LEVEL control so that TRIG'D/GATED LED indicator above control blinks (which indicates that PG508 is triggering on PG502 output).

u. Set PG508 PERIOD control to EXT TRIG.

v. Using Test Oscilloscope to measure signal voltage, adjust PG508 output (VOLTS) control for output high level of +2.4 V and low level of +0.4 V on channel 2.

w. Press PG508 MODE DELAY switch.

x. Make certain that PG508 NORM/COMPLEMENT switch is set to out (NORM) position.

y. Set PG508 DURATION outer control to 10 nS and adjust DURATION center control for 50 percent duty cycle waveform on Test Oscilloscope channel 2.

z. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V for both channels.

aa. Adjust PG508 DELAY control so that the falling edge of PG502 positive pulse crosses center graticule line 2 nS following point at which the rising edge of PG508 positive-going pulse crosses center graticule line.

ab. Power down mainframe for five seconds to reset 7D02 default parameters.

ac. Power up mainframe.

ad. Press ELSE key.

ae. Press TRIGGER key.

af. Enter 1 to select Timing Option Section.

ag. Move cursor to Trigger Arm field and enter 0 to select synchronous mode.

ah. Press END key.

ai. Press START/STOP key to run program.

aj. CHECK - that data displayed are all 1's

ak. Repeat parts **ai** and **aj** ten times to ensure that data 1's are always displayed.

al. Set PG502 NORM/COMPLEMENT switch to in position to complement output.

am. CHECK - that rising edge of PG502 negative-going pulse crosses center graticule line 2 nS following point at which rising edge of PG508 positive-going pulse crosses center graticule line.

an. INTERACTION - If pulse timing is not correct, adjust PG508 DELAY control.

ao. Press START/STOP key to run program.

ap. CHECK - that data displayed are all 0's.

aq. Repeat parts **ao** and **ap** 10 times to ensure that data 0's are always displayed.

ar. Set PG508 NORM/COMPLEMENT switch to in position to complement output.

as. CHECK - that rising edge of PG502 negative-going pulse crosses center graticule line 2 nS after falling edge of PG508 negative-going pulse crosses center graticule line.

at. INTERACTION - If pulse timing is not correct, adjust PG508 DELAY control.

au. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

av. Move cursor to position after end of Test 1.

aw. Press ELSE key.

ax. Press TRIGGER key.

ay. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

az. Enter 1 to select falling edge of clock.

ba. Press and quickly release DELETE key three times to delete Test 2.

bb. Press START/STOP key to run program.

bc. CHECK - that data displayed are all 0's.

bd. Repeat parts **bb** and **bc** ten times to ensure that data 0's are always displayed.

be. Set PG502 NORM/COMPLEMENT switch to out position (NORM).

bf. CHECK - that falling edge of PG502 positive-going pulse crosses center graticule line 2 nS following point at which falling edge of PG508 negative-going pulse crosses center graticule line.

bg. INTERACTION - If pulse timing is not correct, adjust PG508 DELAY control.

bh. Press START/STOP key to run program.

bi. CHECK - that data displayed are all 1's.

bj. Repeat parts **bh** and **bi** ten times to ensure that data 1's are always displayed.

14. Check Setup and Hold, Timing Option Section Word Recognizer

Equipment required:

Test Oscilloscope
PG508
PG502
50-Ohm Termination (2)
Test Fixture 1 (2)
Hook Tips
Coaxial Cable

a. Perform parts **a** through **aa** of step 13 except, in part **p**, set PG502 output pulse duration to 42 nS.

b. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

c. Move cursor to end of existing program.

d. Press and hold DELETE key until entire program is deleted.

e. Press WD RECOGNIZER key.

f. Move cursor to Timing WR bit field and enter 0 to select Timing Word Recognizer.

g. Move cursor to Acquisition Mode field and enter 0 to select synchronous mode.

h. Enter all 1's in Word Recognizer field.

i. Press [] (brackets) key.

j. Press TRIGGER key.

k. Move cursor to Clock Qualification field and enter 1 to select user clock qualification.

l. Move cursor to Clock Edge field and enter 0 to select rising edge of clock. Press TRIGGER key and enter 1 to select Timing Option Trigger.

m. Press [] (brackets) and END keys.

n. CHECK - that program is as shown in Fig. 3-14.

o. Press START/STOP key to run program.

p. CHECK - that program runs continuously, with no trigger.

q. Press START/STOP, IMMEDIATE, DISPLAY, and PROGRAM keys.

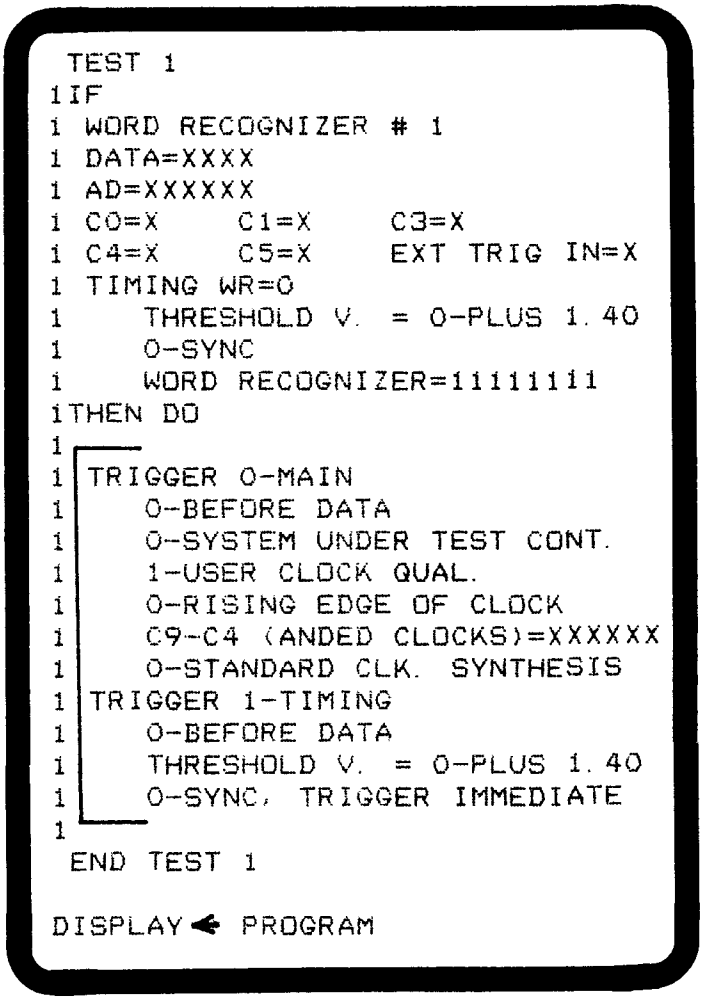
r. Move cursor to Timing Option Word Recognizer field and change all 1's to all 0's.

s. Set PG502 NORM/COMPLEMENT switch to in position to complement output.

t. CHECK - that rising edge of PG502 negative-going pulse crosses center graticule line 2 nS after rising edge of PG508 positive-going pulse crosses center graticule line.

u. INTERACTION - If pulse timing is not correct, adjust PG508 DELAY control.

v. Press START/STOP key to run program.



2919-66

Fig. 3-14. Setup and Hold, Timing Option Word Recognizer Program.

w. CHECK - that program runs continuously, with no trigger.

x. Set PG508 NORM/COMPLEMENT switch to in position to complement output.

y. CHECK - that rising edge of PG502 negative-going pulse crosses center graticule line 2 nS after falling edge of PG508 negative-going pulse crosses center graticule line.

z. INTERACTION - If pulse timing is not correct, adjustPG508 DELAY control.

aa. Press START/STOP IMMEDIATE, DISPLAY, and PROGRAM keys.

ab. Move cursor to Clock Edge field and enter 1 to select falling edge of clock.

ac. Press START/STOP key to run program.

ad. CHECK - that program runs continuously, with no trigger.

ae. Press START/STOP key to stop program.

af. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ag. Move cursor to Timing Option Word Recognizer field and change all 0's to all 1's.

ah. Set PG502 NORM/COMPLEMENT switch to out position (NORM).

ai. CHECK - that falling edge of PG502 positive-going pulse crosses center graticule line 2 nS after falling edge of PG508 negative-going pulse crosses center graticule line.

aj. INTERACTION - If pulse timing is not correct, adjust PG508 DELAY control.

ak. Press START/STOP key to run program.

al. CHECK - that program runs continuously, with no trigger.

15. Check Internal Clock Accuracy

Equipment required:

DC503
Test Oscilloscope Probe

a. Turn off Mainframe power.

b. Remove 7D02 from Mainframe.

c. Remove 7D02 right-hand side panel.

d. If Mainframe is three-compartment type, remove right-hand side panel.

e. Reinstall 7D02 in Mainframe (in left-hand three compartments if Mainframe is four-compartment type).

f. Disconnect probe from Test Oscilloscope.

g. Connect probe BNC connector to DC503 channel A input connector.

h. Connect probe tip to Main Interface Board J202, pin 25A.

i. Connect probe ground to Main Interface board J201, pin 1A.

j. Set DC503 function control to .1 S.

k. Set DC503 channel A DC/AC COUPL switch to out position.

l. Turn on Mainframe power while holding any 7D02 key pressed (to hold operating system in diagnostic mode).

m. Press X key to display module test menu.

n. Press 3 key to call keyboard diangostic module.

o. Press START/STOP key twice to call keyoard layout display for key test.

p. Press ACQ MEM key.

NOTE

The diagnostic routines are designed so that certain keys at the left-hand side of the keyboard call certain clock frequencies.

q. Adjust DC503 channel A LEVEL control for Stable DC503 display.

r. CHECK - that count indicated on DC503 display is between 19.998 and 20.002 MHz.

s. Press PROGRAM key.

t. CHECK - that count indicated on DC503 display is between 9.999 and 10.001 MHz.

NOTE

DC503 display should be quite stable. Indication should not vary by more than two counts. If variance occurs, adjust DC503 LEVEL control to stabilize.

u. Press IMMEDIATE key.

v. CHECK - that count indicated on DC503 display is between 1.9998 and 2.0002 MHz.

w. Press WD RECOGNIZER key.

x. Adjust DC503 channel A LEVEL control for stable DC503 display.

y. CHECK - that count indicated on DC503 display is between 0.19998 and 0.20002 MHz.

z. Press QUALIFY key.

aa. Adjust DC503 channel A LEVEL control for maximum indication of approximately 19 or 20.

ab. Set DC503 channel A function control to 10 S.

ac. CHECK - that count indicated on DC503 display is between 199.9 and 200.0.

ad. Turn off Mainframe power.

ae. Perform reverse order of parts **a** through **i**.

af. Turn on Mainframe power.

16. Check Trigger Position Accuracy

Equipment required:

Test Oscilloscope
50-Ohm Termination (2)
Hook Tips
PG502
Coaxial Cable
Test Fixture 1 (2)

a. Perform parts **a** through **aa** of step 13 except part **p**; set output pulse duration to 42 nS. .

b. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

c. Move cursor to end of existing program.

d. Press and hold DELETE key until entire program is deleted.

e. Press ELSE key.

f. Press TRIGGER key and enter 1 to select Timing Option section.

g. Move cursor to Timing Acquisition Mode field and enter 1 to select asynchronous with triggering on rising edge.

h. Enter 2 and 0 to select 20 nS sample period.

i. Move cursor down to Word Recognizer field and enter all 0's.

j. If necessary, move cursor to Filter field and enter 000 nS.

k. Press START/STOP key to run program.

l. Move cursor to Horizontal Expansion field and enter 1 for X4 expansion.

m. CHECK - that trigger occurs within one sample period of time that last channel changed from 1 to 0. For three permissible displays, see Fig.

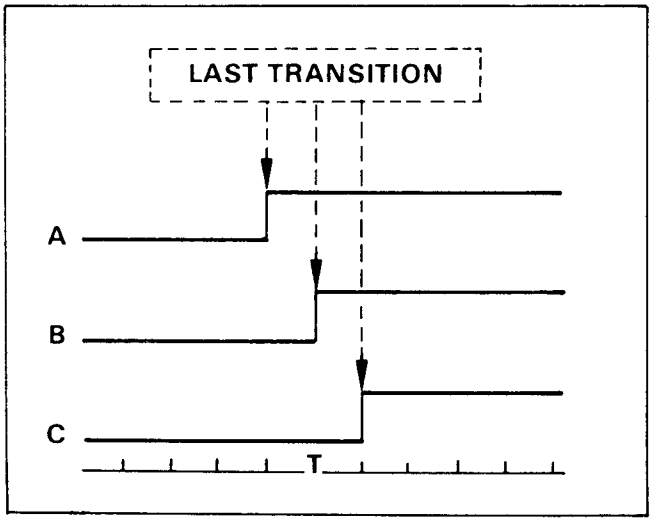


Fig. 3-15. The 3 Permissible Trigger Point Transitions

n. Repeat parts k and l ten times to ensure that triggering occurs within one sample period.

17. Check Glitch Latch and Glitch Trigger

Equipment required:

Test Oscilloscope
Test Fixture 1
Hook Tips
PG502
50-Ohm Termination

a. Connect 50-Ohm Termination to PG502 OUTPUT connector.

b. Connect Test Fixture 1 to 50-Ohm Termination.

c. Using Hook Tips, connect eight channels of P6451 to Test Fixture 1 red terminal. Connect oscilloscope channel 1 to red terminal; ground to black terminal.

d. Using Hook Tip, connect P6451 ground to Test Fixture 1 black terminal.

e. Pull PG502 BACK TERM switch to out position.

f. Set PG502 PERIOD control to 1 uS and turn PERIOD VARIABLE control fully counterclockwise (to X1 position).

g. Set PG502 PULSE DURATION control to <2 nS.

h. Make certain that PG502 NORM/COMPLEMENT switch is set to out (NORM) position.

i. Using Test Oscilloscope to measure voltage, set PG502 OUTPUT (VOLTS) controls for high level of +2.4 V and low level of +0.4 V.

j. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, which is desired threshold.

k. Adjust PG502 PULSE DURATION VARIABLE control for 5 nS pulse width at center graticule line.

NOTE

As the PULSE DURATION VARIABLE control is adjusted, it may not be possible to reach both +0.4 and +2.4 V. In that event, it is important to adjust the voltage levels so that the threshold is at the 50-percent point of the rising and falling edges.

l. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

m. Move cursor to end of existing program.

n. Press and hold DELETE key until entire program is deleted.

o. Press ELSE key.

p. Press TRIGGER key and enter 1 to select Timing Option section.

q. Move cursor to Timing Acquisition Mode field and enter 1 to select asynchronous with triggering on rising edge

r. Move cursor to Sample Period field and enter 1 twice to select 100 nS.

s. Enter X's in all positions of Word Recognizer field.

t. Move cursor to Glitch Recognizer field and enter 1 in bit position 7 (most significant bit).

u. CHECK - that program is as shown in Fig. 3-16.

v. Press START/STOP key to run program.

w. CHECK - that each channel contains series of glitch marks 10 $\pm$ 1 sample periods apart.

NOTE

It may be possible that a pulse or a pulse and glitch may appear instead of only a glitch. However, a glitch, or a pulse, or a pulse and glitch must appear in each position. See Fig. 3-17.

x. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

y. Move cursor to Glitch Recognizer field and enter X in bit position 7 and 1 in bit position 6.

z. Press START/STOP key to run program.

@

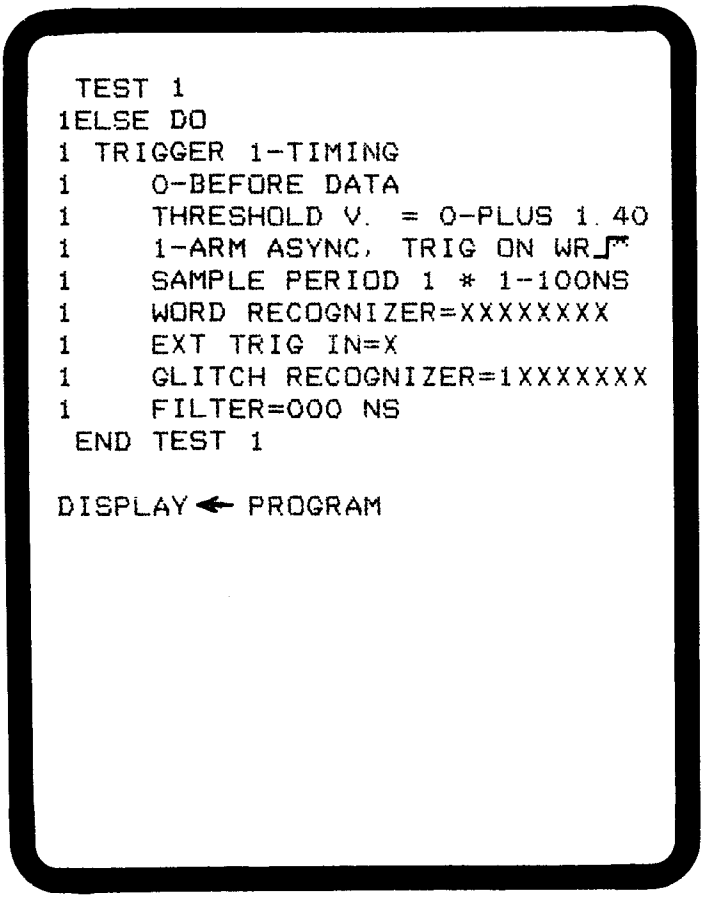


Fig. 3-16. Glitch Latch and Trigger Program.

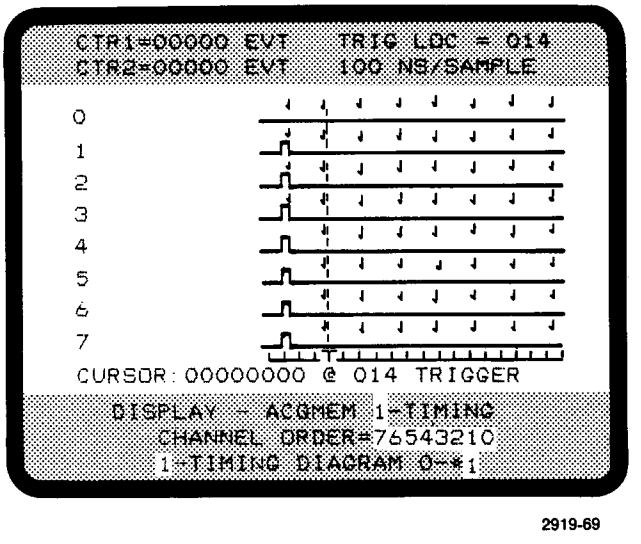


Fig. 3-17. Glitch Latch and Trigger Data.

aa. CHECK - that each channel contains series of glitch marks 10 ± 1 sample periods apart. See note above

ab. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

ac. Move cursor to Glitch Recognizer field and enter X in bit position 6 and 1 in bit position 5.

ad. Press START/STOP key to run program.

ae. CHECK - that each channel contains series of glitch marks 10 ± 1 sample periods apart. See note above

af. Continue procedure of inserting 1 in individual Glitch Recognizer bit position and check for recognition in all eight bit positions.

18. Check Glitch Position

Equipment required:

Test Oscilloscope
PG502
PG508
Hook Tips
Test Fixture 1(2)
50-Ohm Termination (2)
Coaxial Cable

a. Connect 50-ohm Termination to PG502 OUTPUT.

b. Connect Test Fixture 1 to 50-Ohm Termination.

c. Connect 50-ohm termination to PG508 output.

d. Connect Test Fixture 1 to 50-ohm Termination.

e. Connect 50-ohm Coaxial Cable from PG502 Trigger Output to TRIG/GATE IN of PG508.

f. Using Hook Tips, connect P6451 channel 0 to PG508 Test Fixture red terminal.

g. Connect Test Oscilloscope Channel 1 Probe to PG508 Test Fixture red terminal.

h. Connect Test Oscilloscope Channel 1 Probe ground to PG508 Test Fixture black terminal.

i. Using Hook Tips connect P6451 Channel 1 to red terminal of PG502 Test Fixture.

j. Connect P6451 ground to black terminal of PG502 Test Fixture.

k. Connect Test Oscilloscope Channel 2 probe to red terminal of PG502 Test Fixture.

l. Connect Test Oscilloscope Channel 2 ground to black terminal of PG502 Test Fixture.

m. PG502 Setup:

Period to 1 uS; Variable Control fully counterclockwise.
Duration to $\leq$ 2 nS.
Pull back termination to OUT position.
Set NORM/COMPLEMENT switch to OUT (NORM) position.

n. Set PG502 output level volts to low level = +0.4 V, high level = +2.4 V as measured on Test Oscilloscope Channel 2.

o. Set Test Oscilloscope position controls so that center graticule line represents +1.4 V, the desired threshold.

p. Adjust PG502 pulse duration variable control for 5 nS pulse width at center graticule line.

NOTE

As the PULSE DURATION VARIABLE control is adjusted, it may not be possible to reach both +0.4 and +2.4 V. In that event it is important to adjust the voltage levels so that the threshold is at the 50-percent point of the rising and falling edges.

q. PG508 setup:

Period Control to EXT TRIG.
Set TRIG/GATE level to make TRIG'D GATED light blink.
Set mode to DELAYED.
Set DELAY range to 0.1 uS.
Set DURATION range to 0.1 uS.
Set DURATION VARIABLE fully counterclockwise.
Set TRANSITION TIME controls fully counterclockwise.
Set NORMAL/COMPLEMENT switch to OUT.

r. Set PG508 output level controls to low level = +0.4 V, high level = +2.4 V as measured on Test Oscilloscope Channel 1.

s. Set Test Oscilloscope POSITION control such that the center graticule line represents +1.4 V.

t. Adjust PG508 DELAY VARIABLE such that the rising edges of both channels coincide at the center graticule lines

u. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

v. Move cursor to end of existing program.

w. Press and hold DELETE key until entire program is deleted.

x. Press ELSE key.

y. Press TRIGGER key and enter 1 to select Timing Option section.

z. Move cursor to Sample Period field and enter 2 and 0 to select 20 nS. Enter XXXXXXX1 into Word Recognizer. Enter XXXXXXXX into Glitch Recognizer.

aa. CHECK - that program is as shown in Fig. 3-18.

ab. Press START/STOP key to run program.

ac. Move cursor on data display to Timing Diagram field at bottom of display and enter 1 before asterisk to select X4 magnification.

ad. CHECK - that data display is as shown in Fig. 3-19.

ae. Check that glitch on Channel 1 either coincides with or is one sample after the rising edge of Channel 0. If Channel 1 is sampled as data. the glitch may or may not be present Repeat steps **i** and **ab** through **ae** for P6451 Channel 2 through Channel 7.

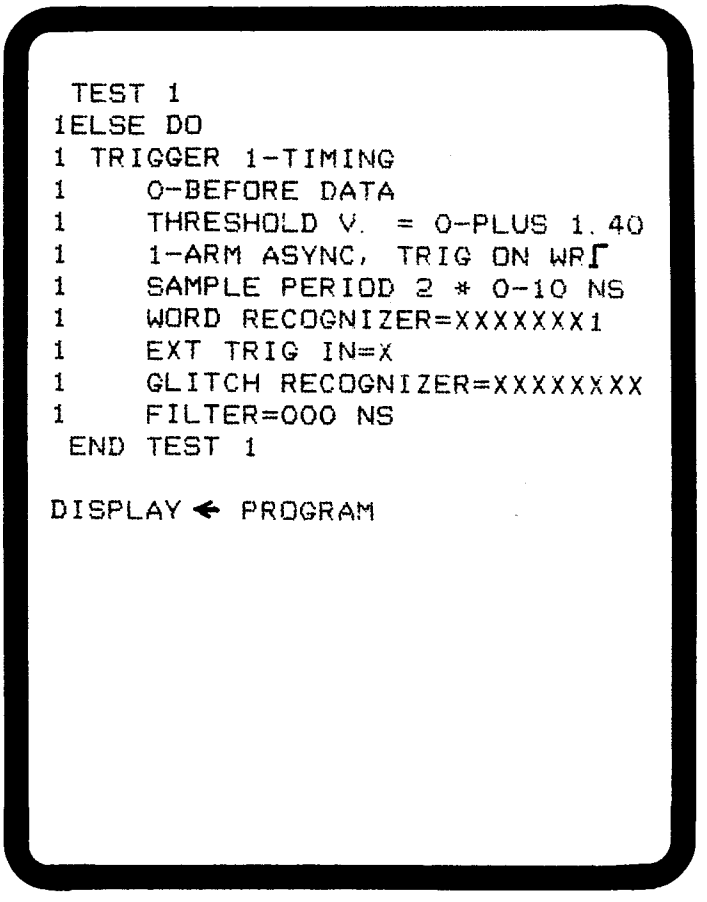


Fig. 3-18. Glitch Position Program.

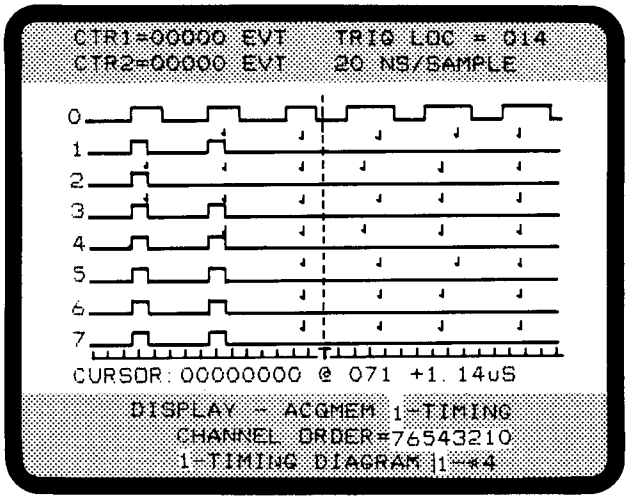


Fig. 3-19. Glitch Data.

SECTION 4

PREPARATION FOR USE AND RESHIPMENT

Introduction

The 7D02 Logic Analyzer is calibrated and ready to use upon receipt. It is electrically compatible with all 7000-Series mainframes except that used in the Digital Processing Oscilloscope (DPO). (The DPO mainframe will not digitize the 7D02 outputs.) However, for best overall performance, two mainframe models are preferred: the 7603 and the 7704A. If used in a rack mounted mainframe, the 7D02 operating temperature specification must be derated to 35 degrees Celsius to accommodate different air flow patterns. If the 7D02 is used in a storage mainframe, it is recommended that the mainframe be operated in non-store mode.

Installation

The 7D02 is designed to occupy three plug-in compartments in a mainframe. It thus fills a three-compartment mainframe, such as the 7603. In a four-compartment mainframe, such as the 7704A, the 7D02 may be installed in either the right-hand three or left-hand three compartments. Mainframe interface switching accommodates this.

Note that some rack mounted mainframes include vertical rods in front of the plug-in compartments. These rods interfere with 7D02 installation and must be removed. To do so, remove the screws at the ends and remove the rods.

Install the 7D02 in the mainframe as follows:

1. Turn off mainframe power.

2. Align 7D02 bottom tracks with rails in appropriate plug-in compartments.

3. Carefully slide 7D02 into mainframe and apply firm pressure to seat connectors so that front panel vertical face is flush with mainframe front.

4. Connect PM101 and P6451 to front panel connectors as appropriate.

To remove the 7D02 from the mainframe, turn off mainframe power disconnect PM101 and P6451, grasp the release latch at the lower edge of the front panel and pull the unit out of the mainframe.

Packaging for Shipment

If the 7D02 is to be shipped for a long distance by commercial carrier, it is strongly recommended that the instrument be packaged in the original manner for appropriate protection. The carton and packing material in which the instrument was shipped from the factory should be saved and used for this purpose.

If the original package is unavailable or is unfit for use, pack the instrument as follows:

1. Obtain corrugated cardboard carton with test strength of at least 200 pounds and inside dimensions of not less than six inches more than instrument dimensions in all places (this will allow for inclusion of cushioning materials).

2. Wrap instrument in polyethylene sheeting to protect finish.

3. Place three inches of cushioning material such as urethane foam in bottom of carton, place wrapped instrument on cushioning, and add at least three inches of cushioning at ends and sides and on top of instrument so that it is held firmly in place.

4. Seal carton securely with shipping tape or industrial stapler or a combination of both methods.

Further, if the instrument is to be shipped to a Tektronix Service Center or to the Factory Service Center for repair or service, attach to the instrument a tag containing the following information:

1. Name and address of the owner.

2. Name of the individual to be contacted if necessary.

3. Instrument type and serial number.

4. Description of the required service.

Also, include the Tektronix Service Center address and the owner's address on the carton in one or more prominent locations.

SECTION 5

MAINTENANCE

Preventive Maintenance

Preventive maintenance consists of periodic inspection and cleaning of the instrument. Preventive maintenance procedures performed on a regular basis may prevent instrument breakdown and will improve reliability. The severity of the conditions under which the instrument is operated will determine the frequency of preventive maintenance procedures. A usually convenient and appropriate time to perform these procedures is immediately prior to instrument adjustment.

Visual Inspection

The instrument should be inspected carefully for such defects as broken connections, damaged circuit boards, improperly seated semiconductors, and heat-damaged parts. It is normally not necessary to disassemble the instrument for this purpose. However, removal of covers is appropriate.

Corrective procedures for most visible defects are obvious. However, particular care must be taken if heat-damaged components are found. It may not be sufficient to merely replace such components. Overheating usually indicates other problems in the instrument. Therefore, it is most important that the cause of overheating be identified and corrected to prevent recurrence of the damage.

Cleaning

Accumulation of dust and dirt on components acts as an insulating blanket and prevents efficient heat dissipation. This can cause overheating and component breakdown. Dust on components is troublesome also because of its electrical conductivity under high humidity operating conditions.

CAUTION

Avoid the use of checmical cleaning agents that might damage plastic parts used in the instrument. In particular, avoid chemical compounds that contain benzene, toluene, xylene, acetone, or similar solvents.

Exterior

Loose dirt and dust accumulation on exterior surfaces can be removed with a soft cloth or brush. Built up accumulation of hardened materials can be removed with a soft cloth dampened in a solution of mild detergent and water. Abrasive cleaners should not be used.

Extra care should be taken in cleaning the front panel pushbutton area. Cleaning solution must not be allowed to enter around the buttons. If a dry cloth or brush does not suffice in cleaning the front panel, use a very slightly dampened cloth to remove soil.

Interior

Loose dust can best be removed from interior surfaces by blowing with low-pressure, dry air. Any remaining dirt can be removed either with a bruch and air pressure or with a cloth dampened in a solution of mild detergent and water. A cotton-tipped swab is useful for cleaning in small spaces.

Note that cleaning normally required with most keyboards is not required for the 7D02 keyboard. Disassembly and reassembly requires special tools and fixtures and should not be attempted in the field.

CORRECTIVE MAINTENANCE

Corrective maintenance consists usually of component replacement to effect repairs. Techniques required to replace components in the 7D02 are described in this section.

Static-Sensitive Components

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 5-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capabile of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic suction type or wick type desoldering tools.

TABLE 5-1

RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels*
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

*Voltage equivalent for levels:

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V
(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms.)

Obtaining Replacement Parts

All electrical and mechanical replacement parts can be obtained through any Tektronix Field Office or representative. However, many standard electronic components may be obtained locally in less time than would be required to order from Tektronix, Inc. Before ordering or purchasing replacement parts, check the appropriate parts list for value, tolerance, rating and description.

NOTE

When selecting replacement parts, it is important to remember that the physical size and shape of a component may affect its performance in the instrument, particularly at high frequencies. All parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance.

Some parts used in the 7D02 are manufactured or selected by Tektronix to satisfy particular requirements, or are manufactured for Tektronix to internally generated specifications. Most of the mechanical parts used in the instrument were manufactured by Tektronix. To determine the manufacturer of parts, refer to the parts list, Cross Index Mfg. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.

2. Instrument serial number.

3. Description of the part (if electrical, include circuit designator).

4. Tektronix part number.

Soldering Techniques

WARNING

To avoid electrical shock, disconnect the instrument from the power source before attempting soldering.

CAUTION

The circuit boards used in the 7D02 are multilayer type boards with conductive paths laminated between the board layers. All soldering on these boards should be done with extreme care to avoid breaking the connections. Only experienced maintenance personnel should attempt repair of the boards.

The reliability and accuracy of the 7D02 can be maintained only if proper soldering techniques are used when repairing or replacing parts. General soldering techniques that apply to maintenance of any precision electronic equipment should be used when repairing the instrument. Use only 60/40 resin-core, electronic-grade solder. The choice of soldering iron is determined by the repair to be made. When soldering on circuit boards, use an 8- to 15-watt pencil-type soldering iorn with a very small wedge-shaped or pointed tip. Keep the tip properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the wiring from the board base material. Apply only enough heat to remove the component or to make a good solder joint. Also, apply only enough solder to make a firm joint.

For metal terminals such as coaxial cable ground lugs, a higher wattage soldering iron may be required. It is thus necessary to match the soldering iron to the task. For example if the component is connected to the chassis or other such large heat-radiating surface, a soldering may require a larger tip and higher wattage iron (about 40 watts).

The following technique should be used to replace a soldered component on a circuit board:

1. Grip one lead of the component to be removed with long-nose pliers and touch the soldering iron tip to the lead at the solder connection. Do not place the tip directly on the board as this may cause damage to the board.

2. Gently pull the lead out as the solder melts. If the lead cannot be removed without increased force, try to remove the other lead of the component.

NOTES

Some component leads are difficult to remove because of a bend placed in each lead during the board manufacturing process. The purpose of the bends is to hold the component in place during a flow soldering process that solders all components at one time.

If a component lead is extremely difficult to remove, it may be helpful to straighten the lead on the back side of the board with pliers or a small screwdriver while heating the connection.

Unsolder the component from the circuit board by applying heat to the component lead so that the solder will remain on the board. If it is necessary to remove excess solder from a circuit board hole for easier installation of a new component, a solder-removal tool should be used.

3. Bend the leads on the new component to fit the circuit board holes. (If the component is to be installed while the board is still installed in the instrument, trim the leads to just protrude through the board.)

4. Insert the component leads in the holes and seat the component in the same position as was the removed component. If the component will not seat properly because of solder remaining in the holes, heat the solder until the component will seat properly.

5. Hold the lead between the component body and the solder connection with long-nose pliers (or another heat sink to protect the heat-sensitive component), touch the soldering iron tip to the lead connection, and apply a small amount of solder to make a firm connection.

6. Trim any lead excess that protrudes through board (if not already done in step 3).

7. Clean the area around the connection with a flux-remover solvent, taking care not to remove information printed on the board.

Component Removal and Replacement

WARNING

To avoid electrical shock, disconnect the instrument from the power source before removing components.

Mechanical and Small Components

The exploded view drawing associated with the Replaceable Mechanical Parts list may be helpful in the removal or disassembly of individual components subassemblies. Component locations are shown in the Diagrams and Circuit Board Illustrations Section. For specific instructions pertaining to soldered parts such as resistors, capacitors, and diodes, refer to the Soldering Techniques paragraph.

Circuit Boards

The following paragraphs contain detailed procedures for removal of circuit boards for repair or replacement. If a circuit board is damaged beyond the practical limit of field repair, replace the entire board and return the board through a Field Office or the Factory Service Center. Part numbers of completely wired boards are given in the Replaceable Electrical Parts List.

NOTE

In the following procedures: the term "right side up" means that the instrument is in normal operating position, the term "left-hand side up" means that the instrument is resting on the surface thatis to the right when one faces the front panel, and the term "right-hand side up" means the opposite.

In each instance, replacement is accomplished in essentially the reverse order of removal.

CAUTION

Avoid touching the gold connectors on circuit boards. Oils and moisture can seriously degrade contact quality.

Keyboard -- Remove the Keyboard as follows:

1. Place instrument right side up while facing front panel.

2. Remove four screws on upper front panel; remove panel.

3. Remove two larger screws that fasten subpanel to front casting; lift subpanel and keyboard out from casting.

4. Remove three harmonica connectors from back of keyboard and remove keyboard/subpanel assembly.

5. Remove eight small screws to separate keyboard from subpanel.

Probe Interface Board -- Remove the Probe Interface Board as follows:

NOTE

This board must be removed before the Front Panel, IC Acquisition, Trigger, Front End, Word Recognizer, Expansion Option, and Acquisition Memory Boards can be removed.

1. Place instrument left-hand side up while facing instrument bottom.

2. Remove three screws that secure board to nutblocks.

3. Using finger pressure, carefully pry board loose from connector and remove board.

NOTE

To remove any of the other boards, the long aluminum strip screwed to the top center rail must be removed.

Front Panel Board -- Remove the Front Panel Board as follows:

1. Place instrument left-hand side up.

2. Remove screws from two nutblocks on board at top center and bottom center rails. The bottom screw is located under the latch bar. (Leave nutblocks on board.)

3. Disconnect five-wire harmonica connector that leads to front panel BNC connectors.

4. Disconnect two-wire harmonica connector that leads to P6451 Board.

5. If Keyboard has not been removed, disconnect three harmonica connectors that lead to Keyboard.

6. Using finger pressure, carefully loosen board from connector; remove board from instrument, taking care not to damage components on board.

IC Acquisition Board -- Remove the IC Acquisition Board as follows:

1. Place instrument left-hand side up while facing instrument bottom.

2. Remove connector leading to P6451 Board. Do not pull on the cable.

3. Using finger pressure, carefully loosen board from connector; remove board from instrument, taking care not to damage components.

Trigger Board, Front End Board, Word Recognizer Board, Expansion Option Board, and Acquisition Memory Board -- Remove each of these boards as follows:

1. Place instrument right side up while facing instrument left-hand side.

2. Using finger pressure, carefully loosen board from connector; remove board from instrument, taking care not to damage components on board.

NOTE: The Probe Interface board need not be removed in order to remove the following board.

State Machine Board, CPU Board and Display Board -- Remove each of these boards as follows:

1. Place instrument right side up while facing instrument left-hand side.

2. Remove screw that secures nutblock at corner of board to upper left-hand rail. (Leave nutblock on board.)

3. Using finger pressure, carefully loosen board from connector; remove board from instrument, taking care not to damage components on board.

Power Supply Board -- Remove the Power Supply Board as follows:

1. Remove Display and CPU boards as outlined above.

2. Place instrument right side up while facing rear panel.

3. Remove two large screws that secure heat sink to rear panel.

4. Remove screw that secures nutblock at corner of board to upper left-hand rail. (Leave nutblock on board.)

5. Turn instrument upside down.

6. Remove screw that secures nutblock at corner of board to lower left-hand rail.

7. Place instrument right side up.

8. Remove screw that secures nutblock at center of board to top center rail.

9. Using finger pressure, carefully loosen board from connector.

10. Taking care not to damage components on board or other components, move board toward Display Board position and remove from instrument.

Vertical and Horizontal Interface Boards -- Remove each board as follows:

1. Place instrument right side up while facing instrument rear panel.

2. Remove Power Supply Board as outlined above.

3. Remove four screws that secure plastic circuit card guide to rear panel.

4. Disconnect two harmonica connectors that lead to Main Interface board.

5. Remove plastic circuit card guide and board from rear panel.

6. Spring plastic guide fingers open to separate board from guide.

P6451 Board -- Remove the P6451 Board as follows:

1. Place instrument left-hand side up while facing front panel.

2. Remove four screws that secure lower front panel to front casting; remove panel while at the same time disconnecting five-wire harmonica connector from Front Panel Board.

3. Disconnect two-wire harmonica connector that leads to Front Panel Board.

4. Remove four screws that secure P6451 Board bracket to front casting.

5. Disconnect multi-pin connector from IC Acquisition Board.

6. Remove board from bottom of instrument.

Main Interface Board -- Remove the Main Interface Board as follows:

1. Remove all other boards as outlined above.

2. Place instrument right side up while facing right-hand side.

3. Remove seven screws that secure board to nutblocks on upper and lower right-hand rails.

4. Disconnect four harmonica connectors that lead to Vertical and Horizontal Interface Boards.

5. Remove board from instrument.

Semiconductors

Semiconductors should not be removed unless defective. If removed from its socket during maintenance, a semiconductor should be returned to the same socket. When a semiconductor is replaced, a thorough check of the affected instrument section should be performed.

CAUTION

To avoid component damage, remove power from the instrument before removing or replacing semiconductors.

Replacement devices should be either of the original type or direct replacements. The lead configuration of semiconductor devices used in the 7D02 are shown in the Diagrams and Circuit Board Illustrations section. When replacing, check the manufacturer's basing diagram. Semiconductors that have heat radiators use silicone grease to increase heat transfer. Replace the grease when replacing the semiconductors.

WARNING

Handle silicone grease with care. Avoid getting grease in eyes. Wash hands thoroughly after use.

An extracting tool should be used to remove the socketed multi-pin integrated circuit to prevent pin damage. The tool is available from

Tektronix as Part Number 003-0619-00. If an extracting tool is not available, exert pressure evenly on both ends of the device. Avoid disengaging pins on one end before the other as this may damage the device.

Interconnecting Pins

The pin connectors used to connect wires to interconnection pins are clamped to the ends of the wires. These are replaced by removing the old connector and clamping a new one in its place.

These pins can be grouped together and mounted in a plastic holder, thus forming a harmonic connector that is installed and removed as a multi-pin connector. The first end-lead pin (number 1) is soldered to a square pad to provide correct orientation of the multi-pin connector. Make certain that the arrow on the multi-pin connector is aligned with this square pad when replacing the connector. If individual end-lead connectors are removed from the plastic holder, note the wire colors for replacement.

Circuit-Board Pins

A circuit board pin replacement kit, including the necessary tools, instructions, and replacement pins, is available from Tektronix as Part Number 040-0542-00.

CAUTION

Only experienced service personnel should attempt to replace pins on multi-layer boards.

Replace a pin as follows:

1. Disconnect connector from pin.

2. Using soldering techniques outlined earlier in this section, unsolder pin and remove it from board, leaving ferrule in hole if possible. (If ferrule is removed with pin, clean hole with solder removal tool and scribe.)

3. Carefully press new pin into hole in board. (If ferrule remained in hole in step 2 above, remove new ferrule from new pin before insertion into hole. If ferrule was removed, press new pin with ferrule into hole.)

4. Position replacement pin squarely as was removed pin.

5. Solder pin to board as was removed pin.

6. If removed pin was bent to move with connector, carefully bend replacement pin to same angle.

7. Replace connector.

Performance Check After Repair

After any electrical component has been replaced, the performance of the affected circuits should be checked. If there are adjustments affected, those adjustments should be checked. Refer to Section 3, Performance Check and Adjustment.

INTERNAL DIAGNOSTICS

Introduction

The 7D02 contains three types of diagnostics to make the task of troubleshooting easier and more efficient. These are: 1) the Power-Up Verification routine, which runs automatically each time the unit is powered up; 2) the Diagnostic Monitor--Module Test, which can be run by the user if an error has been detected during the Power-Up Verification or to exercise the instrument; and 3) the Signature Exerciser Mode, which generates test patterns that can be verified with a signature analyzer such as the Sony Tektronix 308.

Diagnostics Overview

Power-up verification is the self-test process that the 7D02 goes through each time power is turned on or the reset switch is pressed. The idea behind power-up verification is to provide the user with a high confidence level that the 7D02 is operating correctly. The only tests that are not performed at power-up are those that require stimulus from the personality module or require some response from the operator such as pressing keys or examining displays. If the power-up tests find no failures, the 7D02 goes directly into normal operation. If a failure is detected, the test results remain on the screen and the operator is given the option

of either ignoring the error and going into normal operation, or of entering the diagnostics monitor and attempting to isolate the cause of the failure.

In choosing to enter the diagnostics monitor, the operator should refer to the troubleshooting trees at the back of this section. If the power-up verification does not detect any errors but the user wishes to run the additional tests not run at power-up, a failure may be induced at power-up. Hold a key down for about five seconds immediately after turning on the power, which causes the KEYBOARD test to fail. Then select the diagnostic monitor option from the instructions on the screen.

Power-up Test vs Diagnostic Monitor "Test All"

In most respects, power-up verification is the same as the diagnostic "test all" function. The exceptions to this rule are explained below.

1. **Diagnostics ROM.** The power-up sequence is the only time that the diagnostics ROM is treated differently than any other ROM. Since an error in this ROM could cause the diagnostics to fail, it is essential to verify its operation as quickly as possible. The tests performed are precisly the same ones used later to check the firmware ROMs. If the diagnostic ROM should happen to fail power-up verification, the user is so informed and is prompted to press a key to begin normal operation, since power-up verification cannot continue. See the explanation of test strap P1006 for an exception to this rule.

2. **Program RAM.** During power-up verification, no RAM is used until it can be proven good. The only area of RAM that is critical for diagnostics is that between address C000 and C0FF, where stack and variables are stored. After the Power-up Program RAM check is complete, the diagnostics writes the test results on the screen, then checks to see if any failure that may have occurred was in the critical area. If no errors were found in that first 256 words of RAM, then power-up continues with the rest of the tests. If a failure did occur somewhere between addresses C000 and C0FF, the user is warned that power-up verification cannot continue and is prompted to press a key to begin normal operation. (See the explanation of test strap P1006 for an exception to this rule.) The fail address is written on the screen during power-up because, if it is in the critical area, the user will not be able to get this information by running the individual RAM test.

Since no RAM is used prior to the power-up RAM test, there is no information in the RAM to be preserved at the time of the test. However, this is not the case after power-up is complete. The RAM addresses between 0:E300 and 0:E3FF are part of the display RAM but are not displayed on the screen. The area is used as temporary storage for information that must be preserved during the program RAM test run under diagnostic Monitor control. Before this is done, the diagnostics must make certain that the temporary buffer operates properly. At all times except power-up, whenever the program RAM is tested, four tests are run. The first two check the temporary buffer to make certain that it operates properly, the last two actually check the program RAM. If either of the first two tests fail, the last two will not run. See the program RAM test description for a more complete explanation.

3. **Display.** Power-up verification tests only the display RAM, since that's all that can be done without operator assistance. The full test in the diagnostics monitor displays patterns on the screen to allow the operator to subjectively check the operation of the rest of the display system.

4. **Keyboard.** If a key were stuck during power-up, the operator would not be able to enter the diagnostics monitor to do additional testing, so the fail address and data bit indicating precisely which key is stuck is printed on the screen. See the keyboard test description for details on how to interpret the fail information. The full keyboard test in the diagnostics monitor includes a subjective test that is not run at power-up since it requires operator assistance.

5. **Per. Mod. System.** The power-up verification tests on the Personality Module system include two (of several) routines that do not require stimulus from the module itself. Per. Mod. tests run from the diagnostic monitor require stimulus and are more complete.

6. **Timing Option.** Power-up verification tests those facets of the Timing Option that do not require operator intervention. As with several other tests, more complete analysis results from routines run from the diagnostic monitor.

CPU Test Jumpers

The CPU Board (A09) contains three test jumpers that can be used to assist in troubleshooting. The purpose of each of the jumpers is explained below.

P1031. In the normal position, it allows the 555 timer to generate interrupts to the processor. These interrupts are used to service the keyboard, and are disabled internally by the processor during tests that should not be interrupted. The TEST position is for use by service personnel who want to disable interrupts at other times. The keyboard will not functiion while interrupts are disabled.

P1006. The main purpose of this test jumper is to cause the 7D02 to automatically begin looping on "TEST ALL" after completing Power-Up Verification. In addition to the automatic looping function, this jumper affects what happens if either the Diagnostics ROM or the Program RAM tests fail during Power-Up Verification. If the jumper is in the TEST position and the Diagnostics ROM test fails, the user is prompted to press the START/STOP key to re-test the ROM. The diagnostics program then continuously reads the last ROM address (1FFF). If a program RAM failure is detected in the address range of C000 to C0FF, the user is prompted to press the START/STOP key to re-test the RAM. The diagnostics then continuously reads and writes the location where the error was detected. The two test loops described above enable the service technician to observe the processor bus and address decoder activity with an oscilloscope. While in the loops, the START/STOP key is checked directly because interrupts are not enabled.

SIP Resistor Pack. This single-in-line resistor pack (a pullup resistor network), allows the CPU Board and the 7D02 address and data bus to be tested with signature analysis even if the diagnostics will not run. The technique used is to isolate the processor from the rest of the instrument by breaking the data bus at the processor and tying the inputs all high through resistors, causing the processor to read FF whenever it does an Instruction Fetch. The instruction FF is "RST 7", which causes the processor to do two writes to the stack, then fetch another instruction from address 0038. Each time the processor writes to the stack, it decrements the address and eventually addresses every possible memory location then wraps around and repeats. Even though these are write operations, the firmware ROM's are being addressed and are driving the data bus that was disconnected from the processor. The result of all of this activity is that the address and data bus are being driven with a constantly repeating pattern, which is exactly what is needed for signature analysis.

The 0-ohm resistor pack normally installed (R3070) should be removed to break the data bus. The SIP resistor pack provided in the service kit should be installed instead in pins one through nine of the same socket with the marked end in pin one. (Refer to the service kit for more information.) The SIP resistor pack pulls the data inputs to the processor high. The signature analyzer should have the clock input connected to pin 31, and the start and stop inputs tied to pin 28 of U3050 on the CPU board. For more information on setting up the signature exerciser for this test, see the "Kernel Signature Analysis Tree." Note that when the 0-ohm pack is reinstalled, it must be **centered** in the 20-pin socket, leaving two pins open on each end as shown in Fig. 5-1.

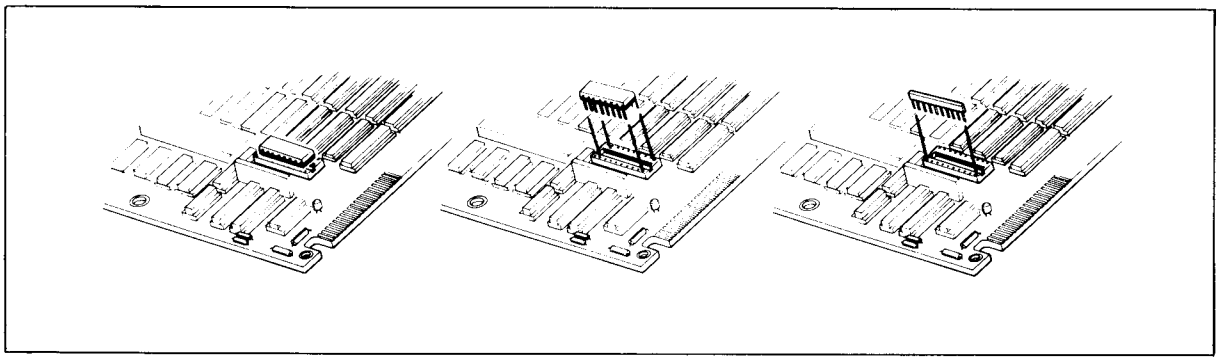


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Fig. 5-1. SIP Resistor Pack Installation Location.

Troubleshooting Trees

The back of this section contains a set of flow charts that can be used as a guide when troubleshooting. The flow charts begin with the power-up verification and lead the service technician to, or as near as possible to the component causing the failure. While using the troubleshooting trees, the technician has several aids available:

Inspection. Many points in the troubleshooting trees recommend a component or group of components to inspect. The part numbers referenced are those most likely to have generated the particular failure code that led the technician to that point in the tree. Further in the tree, there may be additional components listed that could have caused the same failure but are not quite as likely candidates. When the troubleshooting trees recommend inspecting a component, the intention is to make a cursory check for obvious problems such as damaged parts, overheated components and the like. If the part in question is socketed, it might be a good idea to try replacing it before going any further. If the tree leads to signature analysis, the components that were recommended for inspection are also prime locations to take signatures.

Test Description. When a particular diagnostic test fails, the service technician should refer to the test description to get an understanding of just what was being tested and how. It is often possible to compare the descriptions of several tests to find common areas to check. At the end of the test descriptions for each module is a list of the possible failure codes and the components likely to cause such a failure. By comparing the lists from several tests that failed, it is sometimes possible to find components or sections that are common to all failures.

Circuit Description. The circuit descriptions for each board or module can be used in conjunction with the test descriptions to more fully understand how the circuit under test operates and what the particular failure code implies. The circuit description will give details about circuits such as expected waveforms and voltages that can be used to supplement the built-in diagnostics.

Special Test Modes

In addition to the individual module tests, the 7D02 diagnostics contain several special test modes to extend the range of diagnostic coverage. These modes are described below along with an explanation of how each is used.

Kernel Test. In the event that the power-up verification routine does not run when the instrument is first turned on, it is necessary to resort to some more primitive form of troubleshooting. If the display is inoperative, it is not easy to tell whether the diagnostics program is running at all. The first thing that happens when the processor is reset, or when power is first applied, is that the processor generates 200 pulses on the SOD pin, (TP41 and TP42 on the CPU board, A09). By connecting a TTL-level pulse counter to one of these test points, it is simple to verify that the CPU is running. The kernel troubleshooting tree will lead a technician through the above procedure. See the explanation of the SIP Resistor Pack (part of the 7D02 Service Kit) and "Signature Analysis Kernel Mode" for more information on testing the 7D02 kernel.

Test All. The test all mode provides the service technician with a quick and simple means of thoroughly exercising the 7D02. When this test is run, each of the module names is printed on the screen (as it is run) along with the test results for that module. When the test is complete, the user can see at a glance if any problems were detected, and if so, which modules contained problems. In addition to identifying defective modules, a number to the right of the word FAIL indicates which test in that particular module failed. Using this information, it is possible for the technician to proceed straight to the failing test or tests. Because of space limitations on the screen during test all mode, only the first test to fail in each module is listed; the rest of that module is not tested.

Looping. The looping mode allows any test (including "TEST ALL") to be run continuously. Looping is enabled by pressing the "E" key after selecting a module test from the menu. The primary use for looping is locating intermittent failures. When looping is enabled, the Diagnostics Monitor updates the test results on the screen after each iteration of the test. By observing the PASS/FAIL flag, the service technician can determine if a test is failing continuously, intermittently, or only occasionally. In addition, by watching the failure code, the technician can also determine if the failure is exactly the same each time or if it is changing. When a

test passes, the word PASS is printed on the screen in place of the word FAIL, but the failure code is left undisturbed as a record of any previous failures that may have occurred. The 7D02 diagnostics can easily be caused to loop on any particular test or on all tests. If even a single failure occurs while the test is looping, the failure code will remain on the screen to pinpoint the problem. If multiple failures occur, only the most recent failure code will remain.

Signature Analysis

If visual inspection of the components recommended by the troubleshooting trees does not succeed in locating the source of a failure, signature analysis provides a means of further isolating the problem. During signature analysis, the circuit under test is stimulated with a constantly repeating pattern and an external instrument is used to sample points within the circuit for correct response to the stimulus. The external instrument, a Signature Analyzer, such as the SONY/TEKTRONIX 308, samples the point under test once each time it is clocked, after it receives a start signal and continues until it receives a stop signal. The circuit or instrument under test must therefore provide four signals to the Signaure Analyzer: start, stop, clock and data, where "data" is the point being tested. In the 7D02, these four signals are generated in three different manners to suit different circuits under test. The details of how to connect the Signature Analyzer for each circuit under test are listed in a table at the start of the signature analysis troubleshooting tree for that circuit. The three different methods of stimulating the circuits are described in general below.

1. **Kernel Mode** is used when even the most basic part of the diagnostics ROM refuses to run. The SIP Resistor Pack (part of the 7D02 Service Kit) is put in place to cause the processor to "free run" which, in turn, stimulates the address and data busses. Address line A15, is used as the source of both start and stop by setting the Signature Analyzer to recognize the rising edge for one signal and the falling edge for the other. The processor write line is used as the clock, and data are sampled at the points indicated in the signature table.

2. **Programmed Mode** is used when the processor generates the signature stimulus under program control. In this mode, the start and stop signal usually comes from the serial-out data pin on the CPU via TP41 and TP42 (CPU board A09). The clock signal is generated by either a read or a write from the processor and is found on TP49. In this mode, the operator must

select a particular signature exerciser routine from the menu as specified in the signature table.

3. **Per. Mod. Stimulus Mode** is similar to "programmed mode," in that the operator must select a signature exerciser routine from the menu. In this instance, however, the stimulus for the signatures is generated by the general purpose Personality Module (PM101). The signature exerciser program configures the instrument to receive the stimulus, then stands aside and allows the Personality Module to stimulate the test points. This approach is necessary for those parts of the 7D02 that can only be driven from a personality module.

Flow charts at the end of this diagnostic section show troubleshooting trees for the Power-Up Verification routine, Diagnostic Monitor--Module Test, and the Signature Exerciser Mode. The steps shown in these trees will direct troubleshooting operations from the initial failure analysis, which is part of the Power-Up Verification, to the more complete analysis provided by the Diagnostics Monitor--Module Test and the Signature Exerciser Mode. If a failure is encountered in the Diagnostic Monitor--Module Test, the fault should be corrected before proceeding with the diagnostics. Later tests in the sequence require correct operation of the earlier test in order to function properly.

Power-Up Verification

General

The Power-Up Verification routine runs automatically each time the 7D02 is powered up. As it starts, the display screen is cleared, the verification routine runs, and a message indicating the results is displayed. If the mainframe is cold when turned on, the Power-Up Verification may be complete by the time the display warms up. The message that is displayed depends upon the results of the verification. If the verification routine is successful, the message shown in Fig. 5-2 is displayed. This indicates that the operator may proceed with normal operation with confidence that the unit is working correctly. However, it is important to note that the verification routine checks the basic operation of the unit but does not perform an exhaustive test of all facets of operation. If the operator wishes to run more exhaustive tests, further instructions are contained in the description for the Diagnostic Monitor.

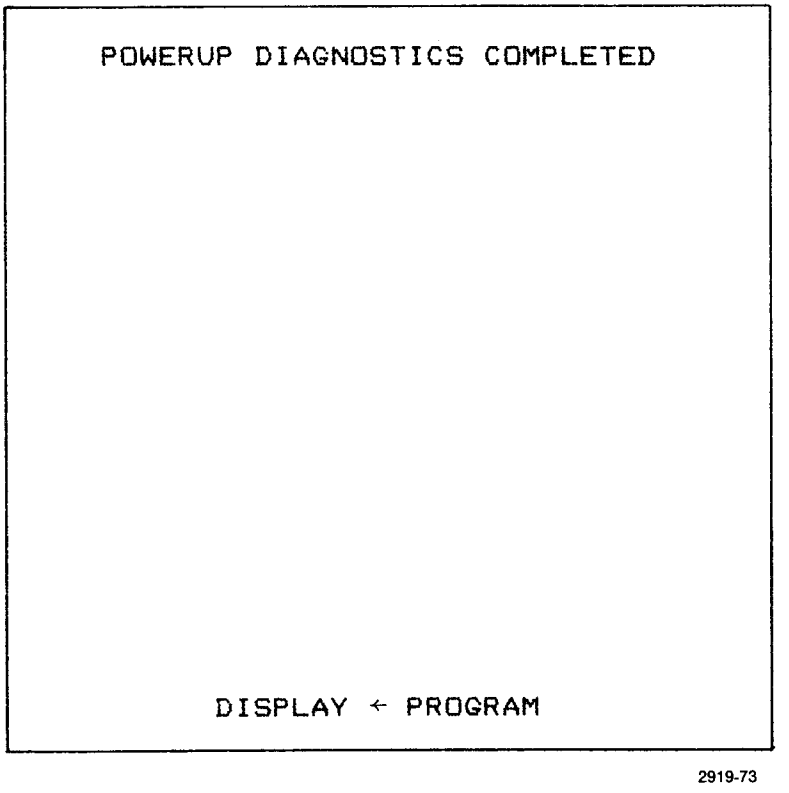


Fig. 5-2. Display resulting from successful power-up verification.

If Power-Up Verification detects a failure, the display indicates which test (or tests) failed. Figure 5-3 shows a typical display when Power-Up Verification detects a failure. At this point, the operator has two choices:

1. Press the X key to enter the Diagnostic Monitor--Module Test mode. This will display the diagnostic menu (see Diagnostic Monitor--Module Test for details).

2. Press the START/STOP key to exit the diagnostic mode and begin normal operation. This implies that the area affected by the failed test is not important for the planned operation (e.g., if the Timing Option test failed but timing data acquisition is not planned, the operator may try to use the instrument). However, if the area that has failed affects other parts of the instrument, improper operation may result.

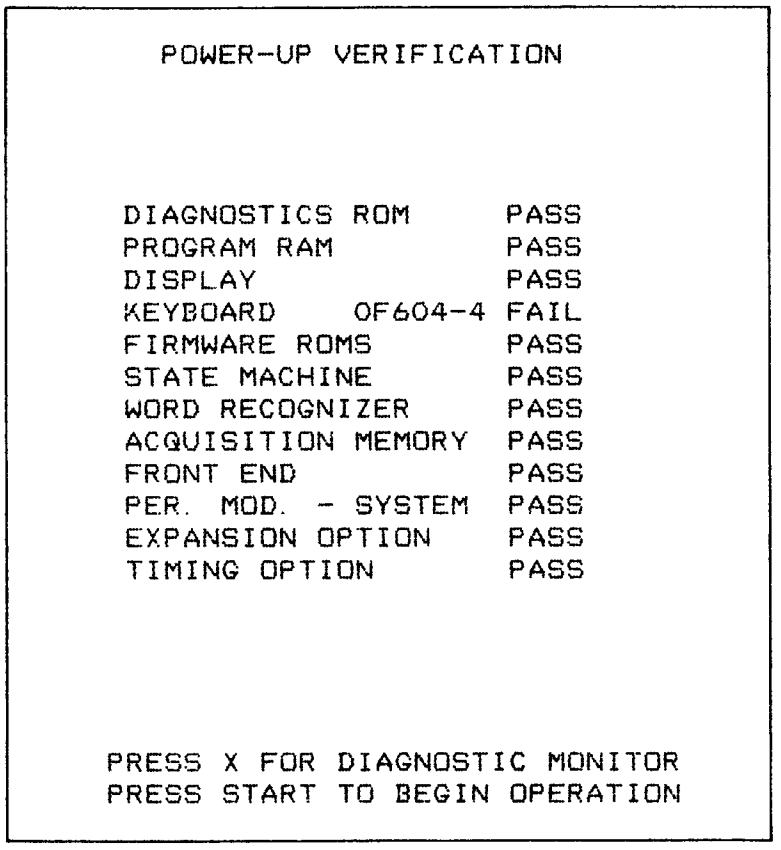


Fig. 5-3. Typical display of failure detected during power-up verification. In this example, the "3" key was stuck or held down.

Power-Up Verification Tests

The Power-Up Verification routine runs the following tests in order:

1. Diagnostic ROM checksum (16 bit).

2. Program RAM addressing and bit independence (March test).

3. Display RAM addressing and bit independence (March test).

4. Keyboard (no keys pressed).

5. Firmware ROM's checksum (16 bit).

6. State Machine verification.

7. Word Recognizer verification.

8. Acquisition Memory verification.

9. Personality Module presence and Personality Module ROM checksum.

NOTE

The following tests are run only if the associated option is installed.

10. Expansion Option presence and verification.

11. Timing Option presence and verification.

As each test is completed, the name of the test and the test results are displayed on the screen. If all tests are successful, the unit is ready to begin normal operation. If any test fails, the failure information remains on the screen for operator action as described.

Diagnostic Monitor - Module Test

Introduction

The Diagnostic Monitor Mode - Module Test provides a more detailed check of the individual modules in the 7D02. This allows a closer look into the unit to help isolate a problem.

Calling The Module Test Diagnostic Mode

If a failure occurs during Power-Up Verification, the user may enter the Diagnostic Monitor--Module Test by pressing the X key. This displays the module test diagnostic menu on the screen (see Fig. 5-4).

NOTE

The Power-Up Verification routine can be "forced" into the failure mode by holding any of the keys down while Power-Up Verification is running.

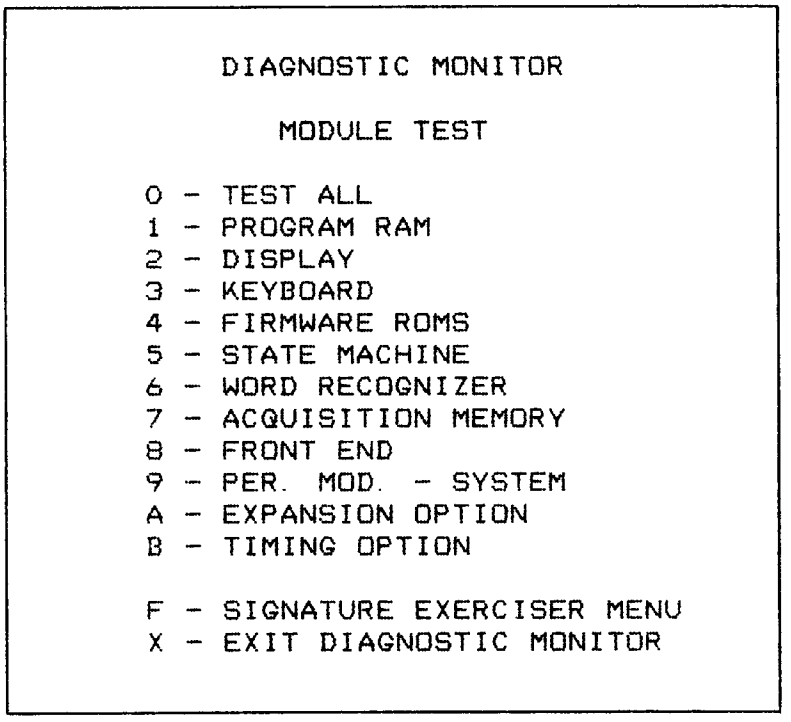


Fig. 5-4. Module test diagnostic monitor menu.

The user can select individual module tests from this menu by pressing the corresponding key; 1 through B correspond to individual test modules (A and B are displayed only if the associated options are installed); 0 selects all tests and executes those tests sequentially from 1 through B. F is not a test, but it provides a branch to the signature exerciser menu (see Signature Exerciser Mode for details). X allows exiting the diagnostic monitor.

Running a Diagnostic Module

When a test is selected, a display similar to Fig. 5-5 is displayed on the screen. The upper part of the display identifies current operation. For example, Fig. 5-5 shows the following:

The Diagnostic Mode	MODULE TEST
The Test Selected	WORD RECOGNIZER
The Test Mode	LOOPING DISABLED (default mode)

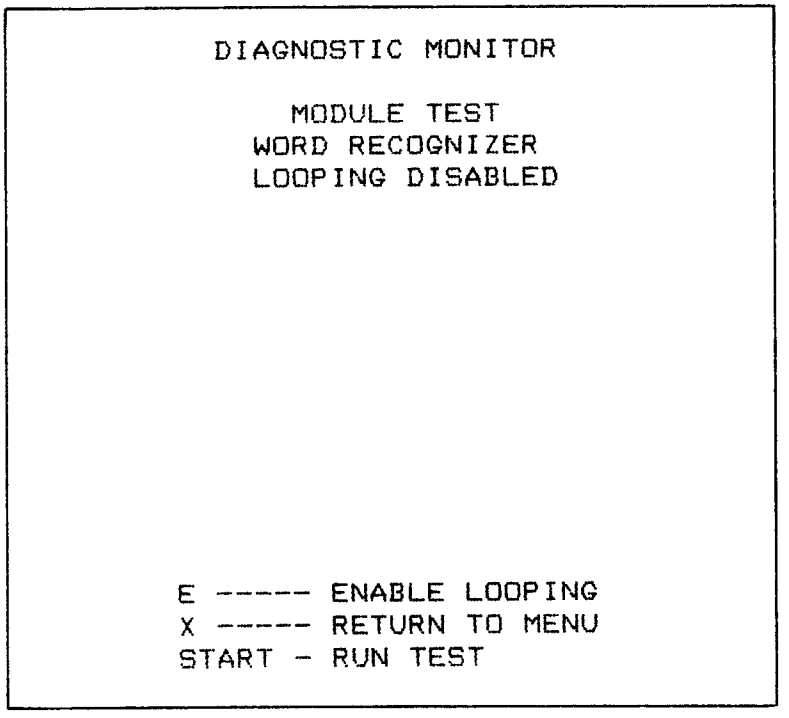


Fig. 5-5. Example of module test instructions with looping disabled.

The lower part of the display provides three operating choices:

E ----- ENABLE LOOPING
X ----- RETURN TO MENU
START - RUN SELECTED TEST

When the E key is pressed, looping is enabled. Fig. 5-6 shows the instructions that are displayed when looping is enabled. Notice that D ----- DISABLE LOOPING replaces E ----- ENABLE LOOPING in the operating choices.

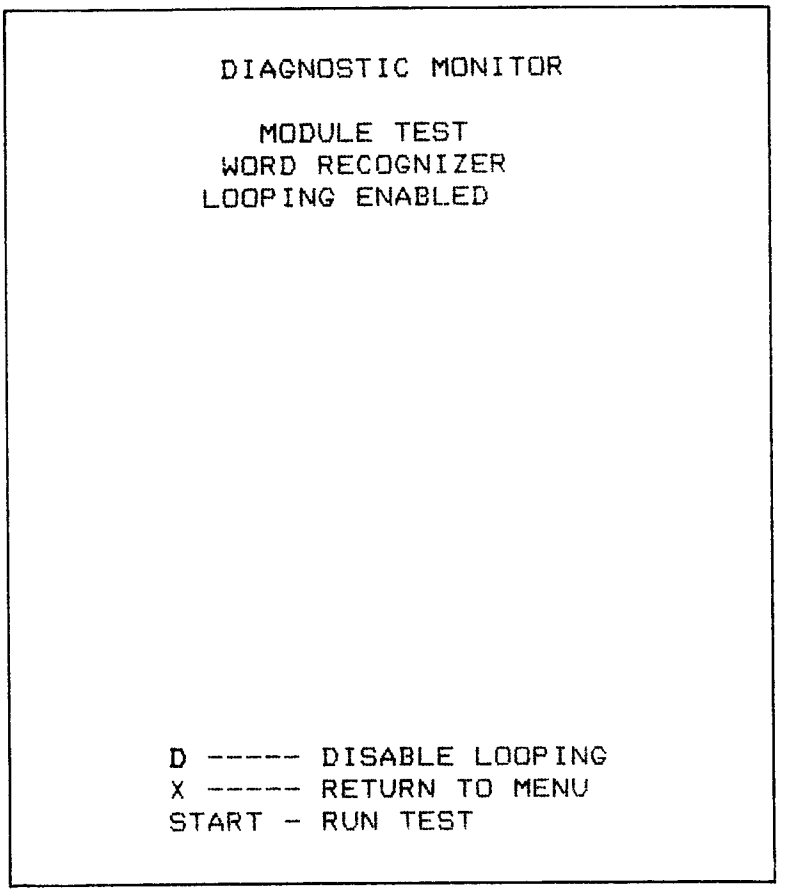


Fig. 5-6. Example of module test instructions with looping enabled.

Pressing the X key returns the menu to the screen to allow selection of another test. START begins the selected test. The lower portion of the screen is cleared in preparation for display of the test results. Figure 5-7 and 5-8 show typical module test results. The numbers represent the subtests and the accompanying statement indicates the test results.

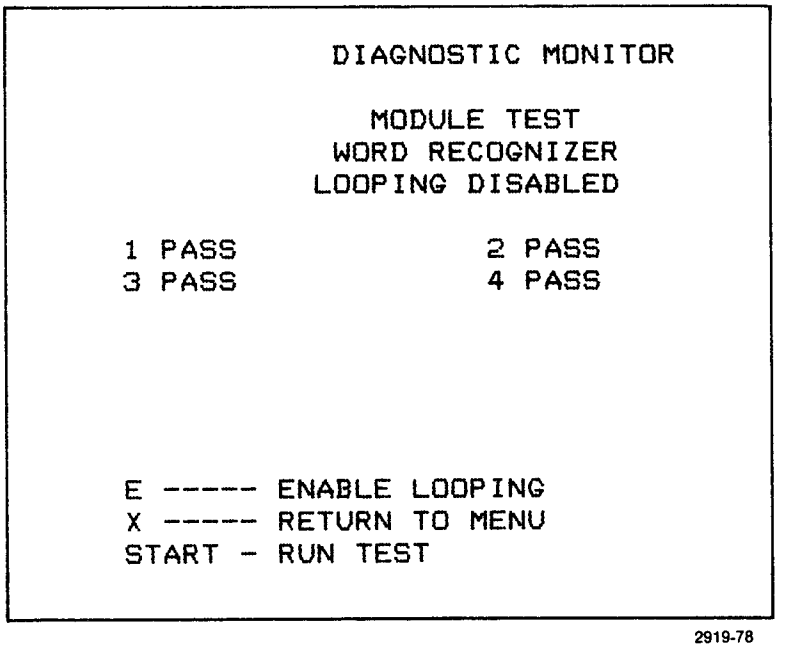


Fig. 5-7. Example of module test results with looping disabled.

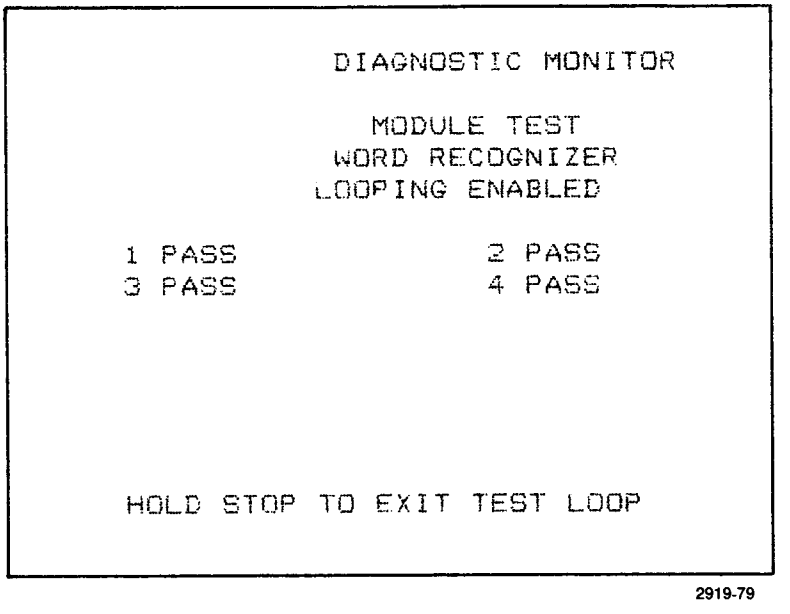


Fig. 5-8. Example of module test results with looping enabled.

Looping A Test

When looping is enabled, the program begins looping on the first subtest and continuously updates the display on the screen with the results of the last test. The program can be advanced to the next subtest by pressing the START/STOP key (in the TEST ALL mode and in some subtests, the START/STOP key must be held down in order to be recognized). All subtests must be stepped through in this manner to complete the entire module test. By doing this, the operator can select a particular subtest for looping while looking for an intermittent problem. Although the pass/fail indication gives only the results of the last test pass, the failure information printed to the right of the word FAIL remains, showing that a failure occurred and where it occurred. Once looping is enabled, it remains enabled until disabled by pressing the D key.

Details of Module Tests

The following information provides details of the individual tests in the Module Test diagnostic mode. Numbers used as headings in the following descriptions refer to the subtests displayed during the tests. The following descriptions provide a general overview of the tests performed in the Diagnostics Monitor--Module Test. This information should be used along with the troubleshooting trees found in the back of this section. Components listed in the tables at the end of each test are provided as an indication of which IC's should be checked using the Signature Exerciser Mode to isolate the failure.

Diagnostics ROM Test

General

The first test performed as part of diagnostics is a check of the Diagnostics ROM itself. This test is made without using any RAM since it is not yet known whether the RAM is functioning correctly. The approach used in the 7D02 is to assume that the first part of the Diagnostics ROM will work. The entire Power-Up Verification and Diagnostics routine, including the messages displayed on the screen, is located in the lower part of this ROM. Therefore, if at least this portion of the ROM is operational, the diagnostics process can continue. This module runs separately only during power-up verification.

Subtest Details

Subtest 1. Checks the Diagnostics ROM to see if it is capable of driving the bus both high and low by reading two complementary bytes stored in the ROM. The complementary data are stored at XXFC and XXFD. If the bytes are not complementary, the test fails.

Subtest 2. Calculates the checksum on the Diagnostics ROM. If the calculated value does not match the expected value, the test fails.

If the display indicates that the Diagnostics ROM test passes, it is reasonably certain that this ROM is working correctly. Failures occur for a variety of reasons. A single defective bit in the ROM will cause the checksum to fail, but will probably allow the instrument firmware to run.

A defective output buffer will probably prevent the test from running at all, as would a shorted or open data bus. A defective address line or address decoder may or may not allow the test to run depending on the location and type of fault.

Program RAM Test

General

The first two subtests check the Display RAM (0:E300-0:E3FF), which is not used in normal operation. If tests 1 and 2 pass, this RAM is used to store the stack and other temporary values during tests 3 and 4. If the first two subtests do not pass, subtests 3 and 4 are not run since doing so would probably result in a program failure.

Subtest Details

Subtest 1. Checks Display RAM for bit independence. This test checks that data bits are not shorted together so that the next test can test the bits in parallel. The test performed is to write a value in address 0:E300 in the RAM. It is then read back and checked to see that it is the correct value.

Subtest 2. Tests the top 256 bytes of the Display RAM using the march test described in detail in subtest 4.

Subtest 3. Assuming that subtests 1 and 2 above pass, this test checks the Program RAM for bit independence in the same manner as subtest 1.

Subtest 4. Interrupts are disabled during this test since a stack is not available. All temporary values used by the diagnostics monitor (including the stack) are temporarily copied into the Display RAM while Program RAM is tested. The results of the subtest are also written in this temporary location so as to be in the proper place when the temporary storage is moved back to the Program RAM.

The test used is a march test. First, the entire RAM is filled with a background of 0's. Then a 1 is walked up through memory, one bit at a time. Before any bit is altered from a 0 to a 1, the bit is checked to see that it was not altered by any previous writes. When the top of RAM is reached, the RAM should contain all 1's. The march is then repeated, only

this time it progresses from the top down and a 0 is marched across a field of 1's. When the bottom of the RAM is reached, the entire process repeats, beginning with a background of 1's. A 0 is marched up, then a 1 is marched down. To interrupt this test, the START/STOP key must be held down until recognized.

At the conclusion of the test, the data in temporary storage is copied back to its original location in the Program RAM and interrupts are again enabled.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
Power-Up	Ø:CØXX	Ø-3	A09U1040*	A09U1080, A09U3065
		4-7	A09U2040*	A09U3080, A09U4070
	Ø:C1XX-DBFF	X	See subtest 4 below	A09U2080, A07U3065 A09U3080, A09U4045, A09U4065, A09U4075, A09U4080
1, 2	Ø:E3XX	Ø-3	A10U3042	A10U1050, A10U2050, A10U3020
		4-7	A10U3040	A10U3050, A10U4040, A10U4050
3, 4	Ø:CØØØ-C3FF	Ø-3	A09U1040	A09U1080, A09U3080,
		4-7	A09U2040	A09U4040, A09U4070,
	Ø:C4ØØ-C7FF	Ø-3	A09U1045	A09U3065
		4-7	A09U2045	Same to end
	Ø:C8ØØ-C8FF	Ø-3	A09U1050	
		4-7	A09U2050	
	Ø:CCØØ-CFFF	Ø-3	A09U1055	
		4-7	A09U2055	
	Ø:DØØØ-D3FF	Ø-3	A09U1060	
		4-7	A09U2060	
	Ø:D4ØØ-D7FF	Ø-3	A09U1065	
		4-7	A09U2065	
	Ø:D8ØØ-DBFF	Ø-3	A09U1070	
		4-7	A09U2070	

* Fatal error; diagnostics will not run.

A09 = CPU board.
A10 = Display board.

Display Test

General

Tests the Display RAM and produces test displays for calibration. Subtest 3 is not run during Power-Up Verification and TEST ALL mode since it requires interaction by the operator.

Subtest Details

Subtest 1. Tests Display RAM for bit independence. This test checks that data bits are not shorted together so that the next test can test the RAM in parallel. The test performed is to write a value in the first location in the RAM, then read it back and check to see that it is the correct value.

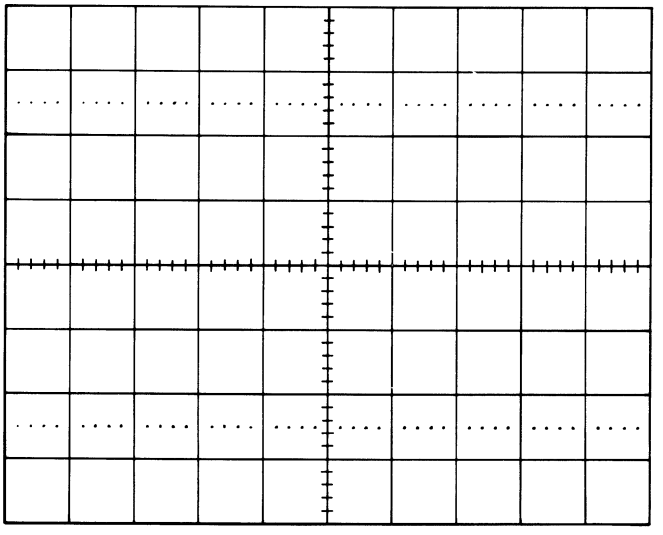
Subtest 2. Tests the Display RAM using the march test described for the Program RAM, subtest 4. The data presently on the screen is preserved by moving it to temporary storage and then moving it back at the conclusion of the test. During the test itself, the display will flash as the RAM is tested.

Subtest 3. This is a calibration routine that is not run during power-up or in TEST ALL mode since it requires operator interaction. First, the entire screen is filled with rubout characters that appear as a full raster see Fig. 5-9A). This is useful for adjusting height, width, and position of the display.

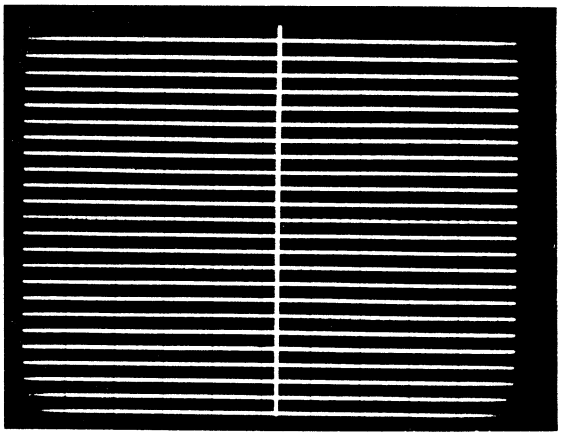
The second pattern fills the entire screen with lines to check focus and linearity (see Fig. 5-9B).

The third pattern is the output of the Character Generator, which allows the operator to check that the Character Generator is being addressed correctly and all characters are correct (see Fig. 5-9C).

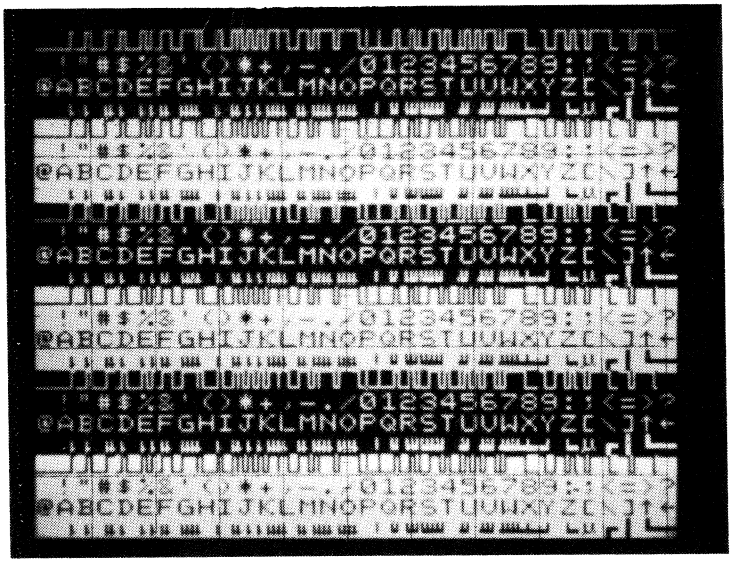
For each of the above patterns, a predetermined value is written in the Probe Threshhold DAC for calibration purposes. The values written and the corresponding patterns are listed below. This allows the DAC and the display to be checked with a single setup. Jumper P1034 on the Front-Panel board must be set to the CALIBRATE position. Voltages shown are measured at TP1053 on the same board, referenced to ground.



9A



9B



9C

2919-80

Fig. 5-9. Calibration test patterns produced in Display Test routine.

Pattern	DAC Value	DAC Output Voltage
Rubout	8ØH	0 volts dc
Lines	Ø1H	+1.588 volts dc
Character Generator	FFH	-1.588 volts dc

During subtest 1, the DAC is ramped once. Thus, by looping this test, it is possible to generate a ramp output from the DAC (at test point TP1053) for display on the oscilloscope. As in all other tests, the SOD pin on the CPU is pulsed once at the start of each loop for oscilloscope triggering purposes.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1, 2	Ø:EØØØ-E2FF	Ø-3	A10U3042	A10U1050, A10U2050, A10U3020
		4-7	A10U3040	A10U3050, A10U4050, A10U4040
3*			A10U1030, A10U1040, A10U2010, A10U2030, A10U3030, A10U3040, A10U3042, A10U4040, A10U4042	A10U1010, A10U1020, A10U1050, A10U2020, A10U2050, A10U3010, A10U3050, A10U4010, A10U4020, A10U4030, A10U4050, A10U5020, A10U6030
DAC TEST			A01U3045 A01U4045 A01U3055	A03V3060 A03U4050

* This is a subjective test requiring the operator to decide pass or fail.

A10 = Display board.

Keyboard Test

General

Tests the Keyboard for stuck keys and for correct key action. Subtest 2 is not run during Power-Up Verification and TEST ALL mode since it requires operator interaction.

Subtest Details

Subtest 1. Scans the keyboard and checks that no keys are pressed. If any key is pressed, it reports the address of the row and the data bit corresponding to the key that was pressed.

If a key is stuck at power-up, the Power-Up Verification routine will indicate a failure and the instrument will not operate correctly. However, the address and data bit corresponding to the stuck key is printed so the problem can be identified. Holding a key down during power-up is an easy way to force the instrument into the Module Test Diagnostic Mode if desired.

Subtest 2. This test is not run during Power-Up Verification or in TEST ALL mode since it requires operator interaction. The keyboard is scanned and each key not pressed is graphically represented by a square on the screen corresponding to its approximate location on the keyboard (see Fig. 5-10). Thus, if no keys are pressed, the screen represents the entire keyboard. Whenever a key is held pressed, a new map is drawn. In this manner, it is easy to see that the key is read correctly and that it does not interfere with any other key. Notice that the map is redrawn only when the key is first pressed. Pressing a second key while holding the first one pressed is ignored.

This test is also used to assist in calibration. As each of the nine keys in the two rows on the left side of the keyboard is pressed, the Timing Option Time Base is programmed to a predetermined value (shown in the table below). This allows the operation of the Time Base and Keyboard to be verified with a single setup. (See Section 3, Performance Check and Adjustment, for details.)

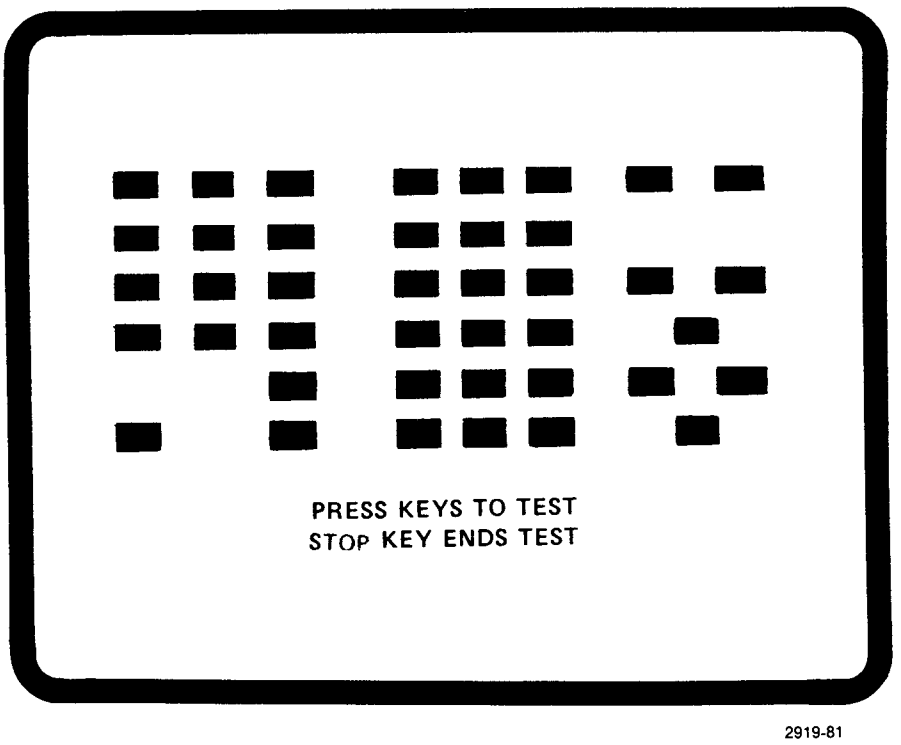


Fig. 5-10. Keyboard test location display.

Key Name	Time Base Value
DISPLAY	20 nanoseconds
ACQUISITION MEMORY	50 nanoseconds
PROGRAM	100 nanoseconds
STORE MEMORY	200 nanoseconds
IMMEDIATE	500 nanoseconds
WORD RECOGNIZER	5 microseconds
END	50 microseconds
ELSE	500 microseconds
QUALIFY	5 milliseconds

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1	X:F6ØX	X	A01U2025, A01U2055,	A01U5025, A01U5055
	X:F61Ø	X	A01U4055	
	X:F62Ø	X		

X indicates the fail address and data to locate keys on the Keyboard location map shown in Fig. 5-11.

2 This test is subjective and requires operator interaction. IC's involved are the same as in subtest 1.

Time Base Test	A03U7060	A03U5050
	A03U8040	A03U1060
	A03U8060	A03U3060
	A03U8050	A03U4050
		A08U7020
	A08U7030	

A01 = Front Panel board.

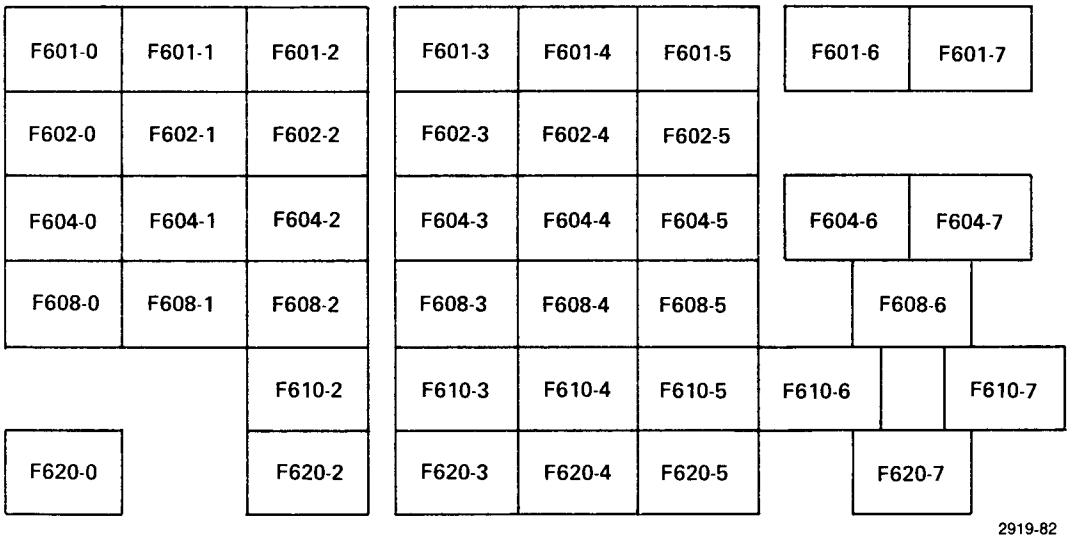


Fig. 5-11. Keyboard location by fail address and data.

Firmware ROM's Test

General

This test checks each ROM for correct operation and for correct location. In the last seven memory locations of each ROM in the system (except the Character Generator) are seven bytes that contain checksum information. This information is accessed in the following tests.

Subtest Details

Subtest 1. Checks Diagnostics ROM to see if it is capable of driving the bus both high and low. The ROM part number, which is stored in the ROM itself, is printed on the screen during the test; if the test fails, the fail address and data are printed. If the ROM is operative but is in the wrong location, the test fails and the part number of the ROM is printed.

Subtest 2. Calculates the checksum on the Diagnostics ROM. If the calculated value does not match the expected value, the calculated value is reported as an error.

Subtest 3. This test is the same as subtest 1 except the ROM under test is Firmware ROM at address 2ØØØ-3FFF.

Subtest 4. This test is the same as subtest 2 except that the ROM under test is the Firmware ROM at address 2ØØØ-3FFF.

Subtest 5. This test is the same as subtest 1 except that the ROM under test is the Firmware ROM at address 4ØØØ-5FFF.

Subtest 6. This test is the same as subtest 2 except that the ROM under test is the Firmware ROM at address 4ØØØ-5FFF.

Subtest 7. This test is the same as subtest 1 except that the ROM under test is the Firmware ROM at address 6ØØØ-7FFF.

Subtest 8. This test is the same as subtest 2 except that the ROM under test is the Firmware ROM at address 6ØØØ-7FFF.

Subtest 9. This test is the same as subtest 1 except that the ROM under test is the Firmware ROM at address 8ØØØ-9FFF.

Subtest 10. This test is the same as subtest 2 except that the ROM under test is the Firmware ROM at address 8ØØØ-9FFF.

Subtest 11. This test is the same as subtest 1 except that the ROM under test is the Firmware ROM at address AØØØ-BFFF.

Subtest 12. This test is the same as subtest 2 except that the ROM under test is the Firmware ROM at address AØØØ-BFFF.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1	Ø:1FFD XXXX-XX	X	A09U3010 (part number should be 0361-XX)	A09U1080, A09U3080, A09U4040, A09U4070,
2	XXXX		A09U3010	Same to end
3	Ø:3FFD XXXX-XX	X	A09U3020 (part number should be 0359-XX)	
4	XXXX		A09U3020	
5	Ø:5FFD XXXX-XX	X	A09U3030 (part number should be 0358-XX)	
6	XXXX		A09U3030	
7	Ø:7FFD XXXX-XX	X	A09U4010 (part number should be 0360-XX)	
8	XXXX		A09U4010	
9	Ø:9FFD XXXX-XX	X	A09U4020 (part number should be 0818-XX)	
10	XXXX		A09U4020	
11	Ø:BFFD XXXX-XX	X	A09U4030 (part number should be 0819-XX)	
12	XXXX		A09U4030	

A09 = CPU board.

State Machine Test

General

Subtests 1 through 6 check subsections of the State Machine Board to isolate problem areas. Subtest 7 paces the State Machine through a simulated acquisition using all previously checked parts of the circuit and some new components as well.

Subtest Details

Subtest 1. Checks State Machine Control RAM's A08U2060 and A08U5060 for bit independence. This test checks that data bits in one RAM are not shorted to the other RAM so that the next test can test the two RAM's in parallel. The test performed is to write FØ in address 2:E000 in the two RAMs. It is then read back and checked to see that it is the correct value.

Subtest 2. Tests State Machine Control RAMs A08U2060 and A08U5060 using the march test described for the Program RAM, subtest 4.

Subtest 3. Tests State Machine Qualify RAM A08U1060 by filling it with a background of 1's and then marching a 0 through while reading 1's. A second pass is made, this time marching 1's while reading 0's. A final pass is made, identical to the first, to check that the RAM once again contains 1's. The RAM is read after each write operation by reading 1:E4XX to latch the Qual. RAM output into A08U3050 and then reading the latch bit 0 at address 1:E100HEX. The RAM inverts the data at the output so the output is 1's when 0's were applied, and vice versa.

Subtest 4. Checks Second Latch A08U3050 on the State Machine board by marching a 1 across the inputs, one at a time, and examining the outputs (bit 5 saved for the last). This is accomplished on bits 1, 2, 3, 4, 6, 7 by doing false reads at 1:E4XX, where XX represents the data applied to the inputs of A08U3050. Then the data is read of 1:E100 which reads all eight bits of latch A08U3050. Bit 5 of A08U3050 is tested by manipulating multiplexer A08U5040. Each time the output data is read, all bits are examined so that bit independence is checked.

Subtest 5. Tests B inputs of Multiplexer A08U5040 by manipulating the inputs and examining the outputs for the expected value. A 1 is walked across the inputs and the outputs are examined after each step for the expected value. The B inputs to multiplexer A08U5040 are changed by loading A08U5060 with the correct values and changing RESET 1 and RESET 2. Then a write at address 1:E500 causes loading.

Subtest 6. Tests the A inputs of Multiplexer A08U5040 by walking a 1 across the inputs as described above.

NOTE

Section 4 of this multiplexer is not checked at this time.

Subtest 7. The State Machine Control and Qualify RAM's are programmed with the following test program which is run at CPU speed.

```
1IF WR1
1THEN
1 CTR1-INC
1 CTR2-IN
1OR IF WR2
1THEN
1 GOTO 2
1OR IF WR4
1THEN
1 GOTO 3
1 END

2IF WR1
2THEN
2 CTR1-DCR
2 CTR2-DCR
2OR IF WR3
2THEN
2 GOTO 3
2OR IF WR4
2THEN
2 GOTO 1
2 END
```

```
3IF WR2
3THEN
3 CTR1-RESET
3 CTR2-RESET
3OR IF WR1
3THEN
3 GOTO 4
3OR IF WR4
3THEN
3 GOTO 1
3 END

4IF WR4
4THEN
4 GOTO 1
```

When the previous sequential test runs the following failure codes are reported:

0001 - Counter 1 did not reset to zero initially.

0002 - Same for Counter 2.

0003 - After WR1 is valid for 300 CPU State Clocks Counter 1 is checked for the value 299.

0004 - Same for Counter 2.

*0005 - State Machine is checked for proper state (Test 1).

0006 - After asserting WR2 once and settling the counters to decrement and having WR1 valid for 100 CPU State Clocks, Counter 1 is checked for a value of 202.

0007 - Same for Counter 2.

0008 - State Machine is checked for proper state (Test 2).

0009 - After asserting WR3 once and WR2 three times, compare Counter 1 with the value zero.

000A - Same as Counter 1.

@

000B - State Machine is checked for proper state (Test 3).

*000C - After asserting WR1 once the State Machine is checked for proper state (Test 4).

* On the first and last CPU State Clock WR4 is asserted true and a transfer from Test 4 to Test 1 is accomplished if this is not the first time through the sequence.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1, 2	1:EØXX	Ø-3	A08U2050, A08U2060, A08U6060	A08U6020, A08U6050, A08U4060
		4-7	A08U2050, A08U5060, A08U6060	A08U7050, A08U4060
3	1:E1XX	Ø	A08U1060, A08U2050, A08U3050	A08U4020, A08U6020, A08U7040, A08U7050, U6050
4	1:E1ØØ	Ø	A08U1060, A08U2050, A08U3050	Same to end
		1-4, 6-7	A08U2050, A08U3050, A08U4060	
		5	A08U2030, A08U3050, A08U5040	
5	1:E1ØØ	5	A08U2030, A08U3050, A08U5040	
		6-7	A08U5040, A08U5050 A08U5060, A08U7060	
6	1:E1ØØ	5	A08U3030, A08U3050, A08U5040	
		6-7	A08U5040, A08U5050, A08U7060	
7	ØØØ1		A08U1050	
	ØØØ2		A08U4050	
	ØØØ3		A08U1040, A08U1050, A08U2040	

ØØØ4	A08U3040, A08U4040, A08U4050
ØØØ5	A08U3050, A08U5040, A08U5060, A08U7060
ØØØ6	A08U1040, A08U1050, A08U2040
ØØØ7	A08U3040, A08U4040, A08U4050
ØØØ8	A08U3050, A08U5040, A08U5060, A08U7060
ØØØ9	A08U1040, A08U1050, A08U2040
ØØØA	A08U3040, A08U4040, A08U4050
ØØØB	A08U3050, A08U5040, A08U5060, A08U7060
ØØØC	A08U3050, A08U5040, A08U5060, A08U7060

A08 = State Machine board.

Word Recognizer Test

General

In order to test any of the Word Recognizer RAM's, it is first necessary to fill all RAM's (including the one under test) with 1's. In this way, any change in the RAM under test results in a change in one of the four Word Recognizer outputs. After the RAM's are all filled with the background of 1's, a 0 is marched through the particular RAM under test, one bit at a time, and the outputs are examined after each bit is altered. When the entire RAM is filled with 0's, the test begins again at the bottom; this time, 1's are marched across a field of 0's. When the end of the RAM is reached a second time, a quick check is made to see that the RAM is indeed filled with 1's again. Be aware that a bit stuck low in any RAM can cause all RAM's to appear to be defective in that Word Recognizer since correct reading of a RAM can only occur if all other RAM's also output a 1 at the address under test.

Subtest Details

Subtest 1. Checks Word Recognizer RAM A05U6030, which is responsible for data inputs Ø-7. The output data is examined by latching the Word Recognizer outputs into A08U7060 where it can be examined with a read by way of A08U3050. Latching into A08U7060 is accomplished by doing false reads of the Word Recognizer RAM (1:FXXXADDR).

Subtest 2. Tests Word Recognizer RAM A05U8010, which is responsible for control inputs Ø-7. The test performed is the same as subtest 1.

Subtest 3. Tests Word Recognizer RAM A05U6020, which is responsible for address inputs Ø-7. The test performed is the same as subtest 1.

Subtest 4. Tests Word Recognizer RAM A05U4010, which is responsible for address input 8-15. The test performed is the same as subtest 1.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1	1:F8XX	1	A05U5020, A05U6030, A05U6050	A05U3040, A05U5050, A08U7060, A05U4020
		2	A05U4030, A05U6030, A05U6050	
		3-4	A05U6030, A05U6050, A05U7040	
2	1:F8XX	1	A05U5020, A05U8010	A05U4040,
		2	A05U4030, A05U8010	A05U5030
		3-4	A05U7040, A05U8010	
3	1:FBXX	1	A05U5020, A05U6020	A05U1040, A05U5050
		2	A05U4030, A05U6020	A05U2020
		3-4	A05U6020, A05U7040, A05U7050	
4	1:FBXX	1	A05U4010, A05U5020	A05U2040
		2	A05U4010, A05U4030	A05U3020
		3-4	A05U4010, A05U7040, A05U7050	

A05 = Word Recognizer board.
A08 = State Machine board.

Acquisition Memory Test

General

Tests components on the Acquisition Memory board for correct operation.

Subtest Details

Subtest 1. Tests Acquisition Memory Address Counter by initializing the MAC to FFH then incrementing it by generating false State Clock 1 pulses as in the Word Recognizer test. The counter is incremented through a full count and then examined for the correct value of 01H.

Subtest 2. Fills Acquisition Memory RAM at addresses 2:E000 to Z:E3FF with a checkerboard pattern. It is then examined for the correct pattern, scanning from bottom to top. The address of the first location found to be in error (if any) is reported along with the first incorrect data bit, scanning from bit Ø through 7.

Subtest 3. Same as the preceeding test except that the pattern begins at a different point so that bits that were previously 1's will now be 0's.

Subtest 4. Similar to subtest 2 except that the RAM is filled with an incrementing pattern to check for address independence (the previous two tests checked for bit independence).

Subtest 5. Tests Delay Counter at address 0:F4XX on the Acquistion Memory board. The counter is first loaded with 0. It is then clocked ØFEH times with false State Clock 1's while the Ripple Carry Out (RCO) is observed to make sure it stays LOW. It is then incremented once more to see that RCO goes high.

Subtest 6. Tests the Activity Monitor at address 2:E803 on the Acquisition Memory Board and several of the circuits that provide its inputs. The HALT output from the Mode Control Latch at address 0:F5XX is set to both the HIGH and LOW states and examined at each. The Acquisition Memory Full flip-flop is preset, then clocked and examined for correct output. RCO is set HIGH on the Delay Counter, then read at the point where it enters the Display/Store flip-flop to see that it propagates through

the Stop Trace Gating. The Display/Store flip-flop outputs are examined to verify the DISPLAY mode state.

Subtest 7. Checks Display/Store flip-flop by first presetting it with a DISPLAY command and then checking to see that the Q and /Q inputs are both in the correct state. It then sets J and K inputs LOW and generates multiple State Clock 0 pulses to force the flip-flop to Store mode. The Q and Q outputs are checked again for correct state.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1	2:E8Ø2	3	A07U3030, A07U3040, A07U4040	A07U1010, A07U1020, A07U2020, A07U5040, A04U5050
2, 3, 4	2:EXXØ			
2, 3, 4	2:EXX4			A07U2020
2, 3, 4	2:EXX8			A05U1040, A07U1020
2, 3, 4	2:EXXC	Ø-3	A07U3010, A07U3020, A05U1040	A07U2010, A07U3040, A07U4040, A07U5040, A05U1040, A07U1020
		4-7	A07U3010, A07U4030, A05U1040	A07U2010, A07U3040, A07U4040, A05U2040
2, 3, 4	2:EXX1			
2, 3, 4	2:EXX5			
2, 3, 4	2:EXX9			
2, 3, 4	2:EXXD	Ø-3	A07U4010, A07U5020, A05U2040	A07U2010, A07U3040, A07U4040, A07U5040, A04U5050, A05U5040
		4-7	A07U4010, A07U5030, A05U2040	A07U2010, A07U3040, A07U4040, A07U5040, A04U5050, A05U5040
2, 3, 4	2:EXX2			
2, 3, 4	2:EXX6			
2, 3, 4	2:EXXA			A05U3040

2, 3, 4	2:EXXE	Ø-3	A07U5010, A07U6020,	A07U2010, A07U3040, A07U4040
		4-7	A07U5010, A07U6030,	A05U3040 A07U2010, A07U3040, A07U4040
2, 3, 4	2:EXX3			
2, 3, 4	2:EXX7			
2, 3, 4	2:EXXB			A05U4040
2, 3, 4	2:EXXF	Ø-3	A07U6010, A07U7020,	A07U2010, A07U3040, A07U4040
5	2-E8Ø3	3	A07U1040, A07U2040	A07U1020, A07U1030, A07U2030, A07U7010, A07U2020
6, 7	2:E8Ø3	1	A07U2020, A07U2030	A07U2010
		2	A07U2030, A07U6040	Same to end
		3	A07U1030, A07U1040, A07U2030, A07U2040, A07U7010	
		5	A07U2030, A07U3040, A07U4040, A07U6040	
		6	A08U1010, A08U4010, A08U6010	
		7	A07U2030, A07U6040	

A04 = Front End board.
A05 = Word Recognizer board.
A07 = Acquisition Memory board.
A08 = State Machine board.

Front End Test

General

Most of the circuitry on the Front End Board can be simulated only via the Personality Module. Therefore, this test checks only a small part of the board. To test the board more completely, the user should run the Personality Module - System test with a Personality Module capable of generating self-test stimulus.

Subtest Details

Subtest 1. Checks the Slow Clock Detect circuitry on the Front End Board. Before doing anything, the test waits two milliseconds for the results of any previous test to time out. Then it checks Slow Clock Indicator A04U2010 for a slow clock indication. After reading the Slow Clock bit, the test generates a false State Clock 1 and 2. Then it checks to see that the slow clock bit went LOW as expected. A half millisecond later, the slow clock bit is checked to see that it is still LOW. Two milliseconds after that, it is checked to see that it has gone HIGH again.

Components Checked

Subtest	Address	Data	Specific ICs Tested	Other ICs Tested
1	Ø:FF6X	Ø	A04U2010 on -00 bds, A04U6010 on -01 bds, A04U5040, A04U5050	A04U6030, A04U6040, A04U6050, A04U4040

A04 = Front End board.

Personality Module - System

General

This test is designed to accomodate the variety of Personality Modules that can be used with the 7D02. As a result, some subtests may not be run with the particular Personality Module in use. Also, subtests 3 through 8 require connection of self-test stimulus. Therefore, these subtests are not run during Power-Up Verification (since it requires operator interaction). These subtests are also not run if the Personality Module in use is not capable of self-test stimulus. See the Personality Module Manual for details of the data supplied to the diagnostics monitor by the Personality Module ROM. Also, this test is designed to look at the total 7D02 system not the particular boards as the other tests. Therefore error codes indicate large sections of the 7D02 that could be the cause of the problem. This test is primarily used to check the system at full operating speed.

Subtest Details

Subtest 1. Reads a byte at 3:E010 in the Personality Module ROM to determine the ROM length. Using these data, it locates the ROM trailer and reads the value at 3:YYF0 (where YY is the value read from 3:E010). The value at 3:YYFC is compared with the value at 3:YYFC, which should be its complement. If the two bytes are not complementary, an error message is printed as follows:

```
1       FAIL      3E7FD-X    ; 2K ROM
1       FAIL      3EFFD-X    ; 4K ROM
1       FAIL      3FFFD-X    ; 8K ROM
1       FAIL      3YYFD-X    ; INCORRECT VALUE @ 3:EØ1Ø
```

Where: X signifies the first non-complementary data bit when the two bytes are compared on a bit-by-bit basis.

If this part of the test passes, it is assumed that the ROM can be read correctly so the ROM socket location is checked. If the location byte is correct, PASS is printed followed by the ROM part number. If incorrect, FAIL is printed, followed by the part number as follows (part number 0361-00 used for example):

```
1       PASS      Ø361-ØØ
        or
1       FAIL      Ø361-ØØ
```

Note that this is the only time that any data follow the word PASS. It verifies that the correct ROM is present. The part number prefix is 160-; the full part number in the above example would be 160-0361-00.

Subtest 2. Calculates a 16-bit checksum on the Personality Module ROM. If the calculated value does not match the expected value, the calculated value is reported as an error as follows:

```
2       FAIL      XXXX
```

Where: XXXX is the calculated checksum.

If the first part of subtest 1 failed, it is very likely that this test will also fail. However, if the first part of subtest 1 passed but the second part failed, it is still possible for this test to pass since the checksum is location independent.

Subtest 3. The Personality Module must be connected for self-test stimulus for the remaining subtests; see the Personality Module manual for details on connecting self-test stimulus. Prior to running this test, the four Word Recognizers are programmed according to data stored in the Personality Module ROM. If the Expansion Option is not present or if the Personality Module ROM specifies that this Personality Module does not stimulate the Expansion Option lines, address lines A16 - A23 and data lines D8 - D16 are set to X (don't care). The External Trigger and ASYNC Trigger are always set to X (don't care). The Word Recognizers remain programmed to these values throughout the remaining Personality Module - System tests.

The State Machine is programmed to execute a test sequence:

```
1       IF WR1 THEN TRIGGER MAIN AND TIMING
1       IF WR2 OR WR3 OR WR4, THEN DON'T TRIGGER
1       GOTO 1
```

Then, the Acquisition Memory board is set for zero delay. The Front End Qualifiers and the Clock Shifter/Divider are programmed to default values according to data stored in the Personality Module ROM. After all setups

are complete, a DISPLAY command is sent and the Slow Clock Detector is checked. A slow clock indication will result in the following error:

```
3       FAIL      ØFF6Ø-1    ; SLOW OR NO CLOCK
```

If the clock appears to be running, the Personality Module ROM is read to determine how long to wait for a trigger to occur. Then, a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If the Main Section is still in STORE mode, the following error is generated:

```
3       FAIL      2E8Ø3-7    ; MAIN SECTION FAILED TO TRIGGER
```

Failure to trigger can be caused by failure of the Personality Module to generate the WR1 value; failure of the Word Recognizer, State Machine, or the Acquisition Memory to respond; or lack of State Clocks on the Acq. Mem. Board. Numerous other problems could also cause this failure, such as a defective Activity Monitor.

If the Main Section triggers, a DISPLAY command is sent before proceeding further. This makes certain that the Timing Option will not remain in STORE mode and interfere with reading the Personality Module ROM. The next step is to read the Last Address +1 Buffer (A07U3030) and calculate the trigger location. The trigger location in the Acquisition Memory is examined and the data stored there are compared with the data in the Personality Module ROM that was used to program WR1. Any values that were set to X (don't care) in WR1 are not compared. If the acquired data do not match the expected data, the following error is reported:

```
3       FAIL      2YYZZ-W    ; TRIGGER VALUE INCORRECT
```

Where: YYZZ is the Acquisition Memory address that holds the data that did not match.
W is the first bit that did not match when comparing LSB through MSB.

The data are compared one byte at a time in the following order:

```
AØ - A7
A8 - A15
DØ - D7
CØ - C5    ; EXT TRIG & ASYNC TRIG ARE DON'T CARE
D8 - D15   ;   ONLY IF EXPANSION OPTION IS PRESENT
A16 - A23  ;   AND STIMULATED BY THE PER. MOD.
```

The fail data are interpreted as follows:

YY=	ZZ=	W= 7	6	5	4	3	2	1	Ø
EØ,E1,E2,E3	XØ,X4,X8,XC	A7	A6	A5	A4	A3	A2	A1	AØ
EØ,E1,E2,E3	X1,X5,X9,XD	A15	A14	A13	A12	A11	A1Ø	A9	A8
EØ,E1,E2,E3	X2,X6,XA,XE	D7	D6	D5	D4	D3	D2	D1	DØ
EØ,E1,E2,E3	X3,X7,XB,XF	-	-	C5	C4	C3	C2	C1	CØ
E4,E5,E6,E7	XØ,X4,X8,XC	D15	D14	D13	D12	D22	D1Ø	D9	D8
E4,E5,E6,E7	X1,X5,X9,XD	A23	A22	A21	A2Ø	A19	A18	A17	A16

This type of failure can be caused by a defective RAM in the Acquisition Memory, a defective Memory Address Counter, or a faulty Last Address +1 Buffer. If the Word Recognizer triggered on the wrong word or if the State Machine sent STOP TRACE prematurely, this could also result. One other possibility is that the Main Section failed to acquire the correct data from the probe system at all.

Subtest 4. This test involves all four Word Recognizers, the two Counters, the State Machine, and the Acquisition Memory. The Word Recognizers are programmed the same as for subtest 3. The State Machine is also programmed with a special test program.

The State Machine begins in state 1 and advances to the next state as each of the four Word Recognizers occurs in order. While in state 1, the two Counters are reset. While in state 2, Counter 1 is incremented, and while in state 3, Counter 2 is incremented. While all of this is going on, the Acquisition Memory is acquiring data. When Word Recognizer 4 occurs, that single data sample is not stored and the Main Section and the Timing Option are both triggered. At that point, the Acquisition Memory Delay Counter begins counting down 240 State Clocks, then ceases to acquire data. The Acquisition Memory contains the last 16 words generated before Word Recognizer 4 and the 240 words generated immediately after Word Recognizer 4. If the Qualify RAM works correctly, the Word Recognizer 4 value was not stored. Counter 1 contains the number of clocks that occurred between Word Recognizer 1 and Word Recognizer 2, and Counter 2 contains the number of clocks that occured between Word Recognizer 1 and Word Recognizer 3.

The Acquisition Memory board is set for a delay of 240 clocks and the Memory Address Counter is preset to ØFDH. The Front End Qualifiers and Clock Shifter/Divider are programmed with default values according to data

stored in the Personality Module ROM. After all steps are complete, a DISPLAY command is sent and the Slow Clock Detector is checked. A Slow Clock indication results in the following error:

```
4       FAIL      ØFF6Ø-1    ; SLOW, OR NO CLOCK
```

If the clock appears to be running, the Personality Module ROM is read to determine how long to wait for a trigger. Then, a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory Board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If still in the STORE mode, the following error is generated:

```
4       FAIL      2E8Ø3-7    ; MAIN SECTION FAILED TO TRIGGER
```

Failure to trigger can be caused by failure of the Personality Module to generate any one of the four Word Recognizer values; failure of the Word Recognizer, the State Machine, or the Acquisition Memory to respond; or lack of State Clocks on the Acq. Mem. Board. Numerous other problems such as a defective Activity Monitor could also cause this failure.

If the Main Section triggers, a DISPLAY command is sent before proceeding further. This makes certain that the Timing Option will not remain in STORE mode and interfere with reading the Personality Module ROM.

The Memory Full bit of the Activity Monitor is examined next. If the Memory Full bit indicates that the Acquisition Memory is not full, the following error results:

```
4       FAIL      2EXXX-5    ; MEM FULL BIT NOT SET
```

Where XXX is less than 400 hexadecimal. Divided by four, this number is the Memory Address Counter value (in hexadecimal) of the last word recognizer data stored. This indication can be caused by a malfunctioning Word Rec., a bad State Machine, a faulty Acq. Mem. Board, or a faulty self test stimulus.

The next part of the test is a check of the Counters. First, the MSB of Counter 1 is read and compared with the expected value stored in the the Personality Module ROM. If it matches, the LSB is compared. Then, Counter 2 is checked. If any byte fails to match exactly, the appropriate error is printed:

```
4       FAIL      1E2Ø2-X   ; CTR 1 MSB BIT X IS WRONG
4       FAIL      1E2Ø3-X   ; CTR 1 LSB BIT X IS WRONG
4       FAIL      1E3Ø2-X   ; CTR 2 MSB BIT X IS WRONG
4       FAIL      1E3Ø3-X   ; CTR 2 LSB BIT X IS WRONG
```

This can be caused by a malfunctioning Word. Rec. or a faulty State Machine expecially on of the counters.

If the Counters are working correctly, the next step is to checksum the Acquisition Memory. All bytes between 2:EØØØ and 2:E3FF are summed and the result stored. The Expansion Option Acquisition Memory is then checksummed by summing all bytes between 2:E4ØØ and 2:E7FF. The result of the first checksum is compared with the expected data stored in the Personality Module ROM. If the Expansion Option is present and stimulated by this Personality Module, the second checksum is also compared with its expected value. Failure of either comparison results in one of the following error messages:

```
4       FAIL      3EØ35-X   ; MAIN ACQ. MEM. FAILS CHECKSUM
4       FAIL      3EØ36-X   ; EXP. OPT. ACQ. MEM. FAILS CHECKSUM
```

Since this RAM is checked separately in the Acquisition Memory and Expansion Option tests, this check primarily tests the ability of the RAM to acquire data at high speed. This one checksum could indicate an error in any one of several areas; the Memory Address Counter, the Qualify RAM, the Personality Module Data Buffers on the Word Recognizer and Expansion Option boards, the Personality Module itself, the Front End Qualifiers, and the Acquisition RAM.

Subtest 5. Checks the ability of the State Machine Time Base to generate millisecond clocks and the the ability of Counter 1 to count these clocks while operating in CONTROL mode. The State Machine is programmed with a special test sequence. The Counters are both loaded with 48 (desired count - 2) and placed in the CONTROL mode (decrement). The Counter 1 Time Base is set to milliseconds and a DISPLAY command is sent. The Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the Personality Module. If none is present, the following error is displayed:

```
5       FAIL      ØFF6Ø-1   ; SLOW OR NO CLOCK FROM PER. MOD.
```

If a clock is present, a STORE command is sent and the Processor enters a delay loop for 46 milliseconds. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see if the State Machine has timed out and returned to the DISPLAY mode. If it has, the following error is reported:

```
5       FAIL      2E8Ø3-2    ; CTR 1 TIMED OUT PREMATURELY
```

If the Main Section was still in STORE mode, the Processor delays another 8 milliseconds. Then, it checks the Activity Monitor again. If the Main Section has not returned to DISPLAY mode, the following error is displayed:

```
5       FAIL      2E8Ø3-7    ; CTR 1 DIDN'T TIME OUT IN 50 MS
```

Since the Processor and Time Base are both derived from the same 6-megahertz crystal, this is not intended to be a check of absolute time base accuracy.

This type of error can be caused by failure of the Time Base Divider on the State Machine Board, failure of the Counter to count the clock pulses correctly, or failure of the State Machine to respond to the Counter reaching zero or by the 7D02 CPU to incorrectly time the test.

Subtest 6. Checks the ability of the State Machine Time Base to generate microsecond clocks and the ability of Counter 2 to count those clocks while operating in the CONTROL mode. The State Machine is programmed with a special test sequence. The Counters are both loaded with 49998 (desired count - 2) and placed in CONTROL mode (decrement). Counter 2 Time Base is set to microseconds and a DISPLAY command is sent. The Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the Personality Module. If none is present, the following error is displayed:

```
6       FAIL      ØFF6Ø-1    ; SLOW OR NO CLOCK FROM PER. MOD.
```

If a clock is present, a STORE command is sent and the Processor enters a delay loop for 46 milliseconds. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see if the State Machine has timed out and returned to DISPLAY mode. If it has, the following error is reported:

```
6       FAIL      2E8Ø3-2    ; CTR 2 TIMED OUT PREMATURELY
```

If the Main Section was still in STORE mode, the Processor delays another 8 milliseconds and then checks the Activity Monitor again. If the Main Section has not returned to DISPLAY mode, the following error is displayed:

```
6       FAIL      2E8Ø3-7    ; CTR 2 DIDN'T TIME OUT IN 50,000 uS
```

Since the Processor and Counter Time Base are both derived from the same 6-megahertz crystal, this is not intended to be a check of absolute time base accuracy.

This type of error can be caused by failure of the Time Base Divider on the State Machine board, failure of the Counter to count the clock pulses correctly, or failure of the State Machine to respond to the Counter reaching zero or by the 7D02 CPU to incorrectly time the test.

Subtest 7. Checks the control (qualifier) lines C4 - C9 on the Front-End Board. The State Machine is programmed with a special test sequence:

```
1       IF WR1    THEN TRIGGER MAIN
1       GO TO 1
```

Word Recognizer 1 was programmed in an earlier subtest to a value specified by the Personality Module ROM. This test uses each of the control lines in turn to qualify out the value to which Word Recognizer 1 has been programmed. If the control line works correctly, the State Clock that occurs with Word Recognizer 1 will be inhibited and the State Machine will not see the Word Recognizer output. A PASS condition, then, is indicated by the failure of the Main Section to trigger. A byte in the Personality Module ROM specifies how long the Processor should wait for the trigger to occur.

The Clock Shifter/Divider ESYNC and WAIT are set up as specified by the Personality Module ROM. Six additional bytes in the Personality Module ROM specify what value to send to the Front End to inhibit State Clocks when Word Recognizer 1 occurs for each of the six control lines. The following sequence is repeated six times, once for each control line or until a failure occurs:

```
Read value from Personality Module ROM
Write value to Front End Latch
Send STORE command
Wait specified length of time
Check Activity Monitor on Acquisition Memory board
If in DISPLAY mode, print FAIL and STOP
```

A note of caution about this test. Because of the way it operates, anything that prevents the Store/Display flip flop on the Acquisition Memory board from returing to DISPLAY mode will cause the test to pass; for example, lack of a clock from the Personality Module. If subtest 3 and 4 pass, it is safe to assume that this test is working correctly.

The test results are interpreted as follows:

```
7       FAIL      3EØ39     ; C4 DIDN'T INHIBIT TRIGGER
7       FAIL      3EØ3A     ; C5 DIDN'T INHIBIT TRIGGER
7       FAIL      3EØ3B     ; C6 DIDN'T INHIBIT TRIGGER
7       FAIL      3EØ3C     ; C7 DIDN'T INHIBIT TRIGGER
7       FAIL      3EØ3D     ; C8 DIDN'T INHIBIT TRIGGER
7       FAIL      3EØ3E     ; C9 DIDN'T INHIBIT TRIGGER
```

Subtest 8. Checks the Programmable Shifter/Divider on the Front End Board in the delay-by-one and divide-by-two modes. Since not all Personality Modules will generate meaningful data under these conditions, there is a byte in the Personality Module ROM that specifies whether or not this test should be run.

When this test is run, the State Machine is programmed with the following program:

```
1IF WR1
1THEN
1GOTO 4

4IF WR1
4THEN
4TRIG MAIN
```

The Front End is set up as specified by the Personality Module ROM except that it is set to divide-by-two using the low state of C6 to generate ESYNC. A DISPLAY command is sent and the Acquisition Memory Delay Counter

is set for a delay of 16 clocks. The Acquisition Memory Address Counter is pre-loaded with a value of ØFDH. Before proceeding, the Slow Clock Detector is checked and, if no clock is present, the following error is reported:

```
8    FAIL ØFF6Ø-1    ; SLOW OR NO CLOCK
```

If the Clock appears to be running, a STORE command is sent and the Processor waits a period specified by the Personality Module ROM. At the end of the delay, the Acquisition Memory Activity Monitor is checked, and if the Main Section hasn't returned to DISPLAY mode (triggered), the following error is displayed:

```
8    FAIL 2E8Ø3-7    ; MAIN SECTION FAILED TO TRIGGER
```

If the Main Section triggered, the Acquisition Memory should now be full. All of the bytes between 2:EØØØ and 2:E3FF are checksummed and the result is compared to the expected value stored in the Personality Module ROM. If the values do not match, the following error is reported:

```
8    FAIL 3EØ37-X    ; DIVIDE BY 2 CHECKSUM FAILED
```

If the divide-by-two test passes, the entire test is repeated with the Front End set to delay-by-one instead of divide-by-two (C6 generates ESYNC as before). If the test fails under these conditions, the following error is reported:

```
8    FAIL 3EØ38-X    ; DELAY BY 1 CHECKSUM FAILED
```

Expansion Option Test

General

This test is run only if the Expansion Option is installed and is responsible for checking the additional bits of acquisition and word recognizer provided by the Expansion Option.

Subtest Details

Subtest 1. Checks for bit independence by filling the Expansion Option Acquisition Memory with a checkerboard pattern beginning with the value 55H. The RAM is then examined for the correct pattern, scanning from bottom to top. The address of the first location found to be in error is reported, along with the first incorrect data bit scanning from data bit Ø through 7. This test also indirectly checks the memory address counters A06U3050 and A06U4050.

Subtest 2. This test is the same as subtest 1 except that the pattern begins with the value AAH so that all bits that were previously 1 will now be 0.

Subtest 3. Similar to subtest 1 except that the RAM is filled with an incrementing pattern to check for address independence.

Subtest 4. Tests the Word Recognizer Expansion Option RAM which is responsible for data inputs 8 - 15. The test performed is the same as Word Recognizer subtest 2 except that a different RAM is tested.

Subtest 5. Tests the Word Recognizer Expansion Option RAM which is responsible for ADDR inputs 16 - 24. The test performed is the same as Word Recognizer subtest 2 except that a different RAM is tested.

Components Checked

Test	Address	Data	Specific ICs Tested	Other ICs Tested
1,2,3	2:EXXØ 2:EXX2 2:EXX4 2:EXX6 2:EXX8 2:EXXA	Ø-3	A06U3030, A06U4020, A06U5020	A06U1030, A06U3050, A06U4050, A06U1040, Same to end

	2:EXXC			
	2:EXXE			
	2:EXXØ	4-7	A06U3040, A06U4020,	
	2:EXX2		A06U5020	
	2:EXX4			
	2:EXX6			
	2:EXX8			
	2:EXXA			
	2:EXXC			
	2:EXXE			
	2:EXX1	Ø-3	A06U2020, A06U2030,	
	2:EXX3			
	2:EXX5			
	2:EXX7			
	2:EXX9			
	2:EXXB			
	2:EXXD			
	2:EXXF			
	2:EXX1	4-7	A06U2020, A06U2030,	
	2:EXX3			
	2:EXX5			
	2:EXX7			
	2:EXX9			
	2:EXXB			
	2:EXXD			
	2:EXXF			
4	1:FØXX	1	A06U4040, A05U5020,	A05U3040, A08U3050, A08U7060, A06U6010
		2	A06U4040, A05U4030,	A06U1030, A06U1050, A06U4020
		3-4	A06U4040, A05U6050, A05U7040, A05U5020	Same to end
5	1:F1XX	1	A06U5040, A05U5020	
		2	A06U5040, A05U4030	
		3-4	A06U5040, A05U7040, A05U7050	

A05 = Word Recognizer board.
A06 = Expansion Option board.
A08 = State Machine board.

Timing Option Test

General

This test is run only if the Timing Option is installed. It requires self-test stimulus from the Personality Module for subtest 3. This subtest is not run during Power-Up Verification since operator interaction is required.

Subtest Details

Subtest 1. Checks the Timing Option read and write bus, and to a limited extent, the Timing Option Memory Adress Counter. A 1 is written in each bit of the Counter individually and read back to check the Counter Latch and the two buses. If the read data are not the exact complement of the write data, the following error is reported:

1 FAIL 2F4ØØ-X

Where: X is the first non-complementary bit when scanned from LSB to MSB.

Subtest 2. This test is a simulated asynchronous acquisition without stimulus from the Personality Module to check the Timing Option Sequencer. The Time Base is set to 100 nanoseconds and the trigger is set for zero delay, SYNC mode. After sending a DISPLAY command, the Sequencer is checked for a reset condition. A STORE command is sent and false state clock 2 is generated by asserting sync trigger from the State Machine and toggling bit 3 at Ø:F84Ø from 1 to 0 and back to 1. The Sequencer is checked for an indication of delaying by count. If the Sequencer is not the correct value, the following error is displayed:

2 FAIL 2F6ØØ-X

Where: X is the Sequencer bit in error.

If the Sequencer value is correct, a STORE command is sent and Sync Trigger is asserted. A trigger is simulated and the Sequencer is checked again. If the Sequencer is not in the correct state, the same error as above is reported.

NOTE

For specific and general ICs tested, refer to the Timing Option troubleshooting tree.

Subtest 3. This test requires stimulus from the Personality Module and is not run during Power-Up Verification since the operator is required to connect the Personality Module for self-test stimulus. See the Personality Module manual for details on connecting self-test stimulus. Also, this test is not run if the Personality Module ROM indicates that the Module does not generate self-test stimulus. The Personality Module provides the stimulus via the Timing Option P6451. The Personality Module ROM contains details of the stimulus provided by that Personality Module to the Timing Option. The Timing Option Word Recognizer is set to trigger on the occurrence of a value specified by the Personality Module ROM. The State Machine is programmed with the following program.

```
1IF TIM OPT WR=YY (WR1=TIM.OPT.WR)
 AND WR2,3,4=DON'T CARE
1THEN
1GO TO 4
1 END
4IF TIM OPT WR=YY (TIM.OPT.WR=WR1)
 AND WR2,3,4=DON'T CARE
4THEN
4TRIG MAIN AND TIMING
4 END
```

The Timing Option Memory Address Counter is set to 0. All Word Recognizers except the Timing Option are set to X (don't care).

A DISPLAY command is sent and the State Machine Counters are set to count events. The Main Section Address Counter is set to ØFDH. Then the Slow Clock Indicator is checked for the presence of the same clock as was checked in the Per. Mod. Sys. tests. If none is detected, the following error is printed:

```
3    FAIL ØFF6Ø-1    ; SLOW OR NO CLOCK DETECTED
```

If the clock appears to be running, a byte is read from the Personality Module ROM that specifies how long to wait for a trigger. Then a STORE

command is sent. After waiting the specified length of time, the Acquisition Memory Activity Monitor is examined to see if only the Main Section has triggered. If it hasn't, the following error is reported:

```
3    FAIL 2E8Ø3-7    ; MAIN SECTION FAILED TO TRIGGER
```

If the Main Section triggered, the Timing Option Memory Address Counter (A02U2040 and A02U3030) is examined to determine the last data location and the trigger location is calculated. The value saved in the trigger location is then compared with the value in the Personality Module ROM that was used to program the Timing Option Word Recognizer. If the two are not complementary (data are inverted), the following error is reported:

```
3    FAIL 3EØ3F-X    ; TRIGGER VALUE INCORRECT
```

If the trigger test passes, the Timing Option Acquisition Memory at address 2:FØØØ - 2:FØFF is checksummed (with the exception of one data byte, which is X's) and the result compared with the expected value stored in the Personality Module ROM. If the values are not the same, the following error is reported:

```
3    FAIL 3EØ4Ø-X    ; CHECKSUM ERROR 2:FØØØ - 2:FØFF
```

Where: X indicates the bit that didn't match.

If the first checksum passes, a checksum is calculated for the Memory at 2:F2ØØ - 2:F2FF. The result is compared to an expected value stored in the Personality Module ROM. If the two do not match, the following error is displayed:

```
3    FAIL 3:EØ41-X   ; CHECKSUM ERROR 2:F2ØØ - 2:F2FF
```

In Synchronous mode, both sections of the Timing Option RAM store data, although only one is displayed. Therefore, both of the above checksum calculations depend upon the data that were acquired.

Signature Exerciser Mode

Introduction

The Signature Exerciser Mode generates a data stream that can be verified with a signature analyzer such as the SONY/TEKTRONIX 308. This technique facilitates detection of faults by comparing the measured signature with the correct signature at a particular point in the cirucit (as shown by the Signature Tables).

Flow charts at the end of this section show troubleshooting trees for the Signature Exerciser Mode. Following the procedures shown will provide a logical signature analysis sequence once a failure has been detected by the Diagnostic Monitor - Module Test routine.

Calling Signature Exerciser Mode

The Signature Exerciser Mode can be entered from the module test menu by pressing the F key. This displays the signature exerciser menu on the screen (see Fig. 5-12). Item 7 - PER. MOD.-SYSTEM will not be displayed if a Personality Module is not connected to the 7D02. Applicable signatures were taken using Self Test Stimulus from a PM101 Personality Module. Refer to that manual or section 3 of this manual for connection information.

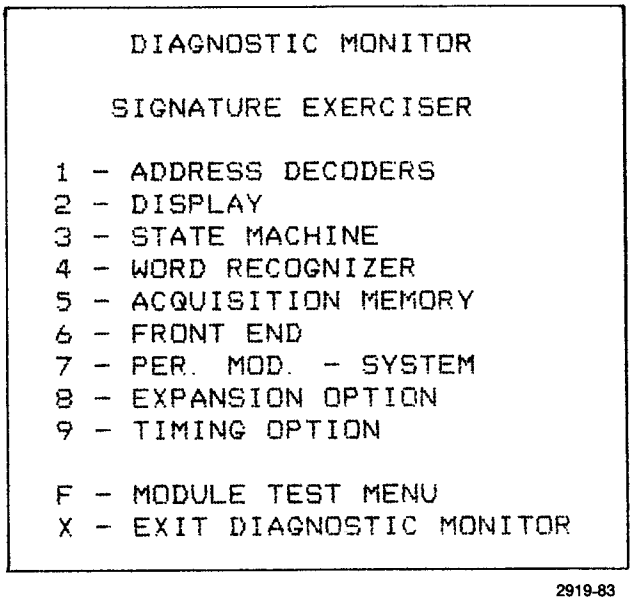


Fig. 5-12. Signature exerciser menu.

The user can select individual Signature Exerciser tests from the menu; 1 through 9 select corresponding Signature Exercisers, which run continuously until the START/STOP key is pressed; F provides a branch to return to the module test menu; X allows exiting the diagnostic monitor.

Figure 5-13 shows a typical display when using the Signature Exerciser mode.

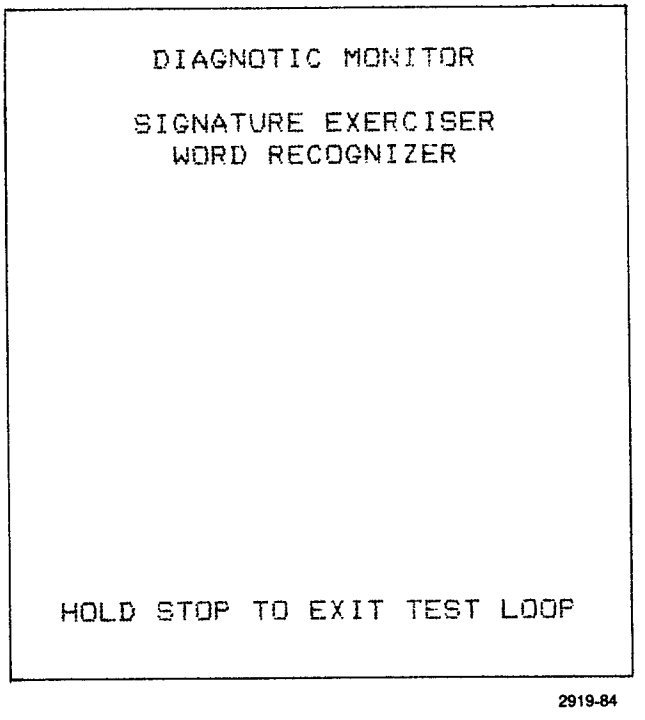


Fig. 5-13. Typical display in signature exerciser mode.

Preparing the Unit for Signature Analysis

1. Install the 7D02 on the plug-in extenders.

2. Remove the board to be tested and install it in the test position using the 067-0939-00 service test kit (see the service test kit manual 070-3639-00 for details). Figure 5-14 identifies the board locations in the 7D02.

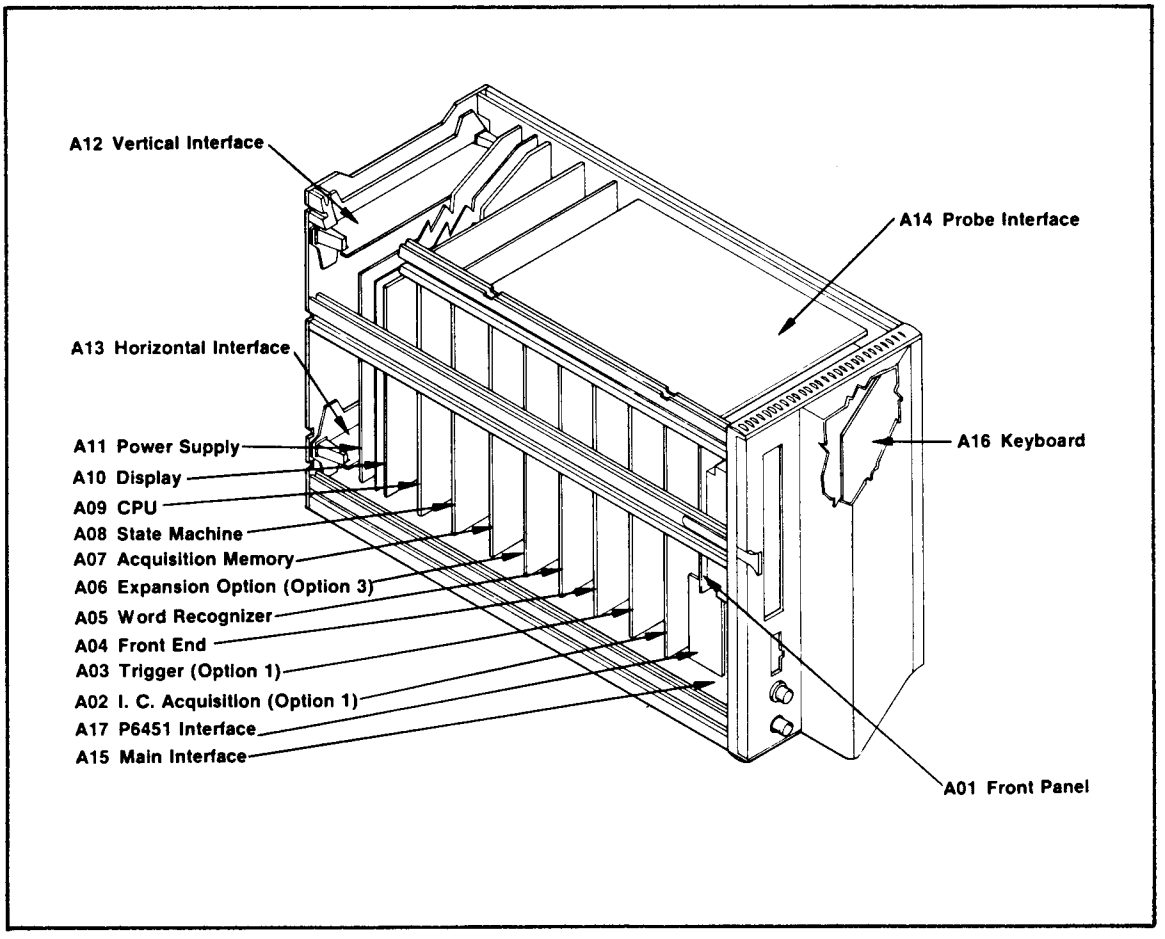


Fig. 5-14. Location of boards in the 7D02.

3. Connect the Signature Analyzer CLOCK, START, and STOP inputs to the points shown in the applicable signature table and set the controls as shown under Analyzer Setup. For details on operation of the Signature Analyzer, refer to the SONY/TEKTRONIX 308 Instruction Manual.

4. Turn on the power to the 7D02. If power-up verification does not detect a failure in the unit, press and hold a front-panel key during power-up to force the unit into the diagnostics mode.

5. After Power-Up Verification is completed, press the X key to enter Diagnostic Mode - Module Test; then press the F key to enter Signature Exerciser Mode.

6. Refer to the signature table for the board under test and verify the signatures shown. The Signature Analyzer setup can be easily verified by taking a signature on +5 volts and comparing it to the reference signature shown on the signature table.

Signature Tables

All signatures in the following tables were taken with a SONY/TEKTRONIX 308 Data Analyzer. The indicated tests require PM101 Personality Module stimulation.

SIGNATURE ANALYSIS TABLES

In the following signature tables special notice should be taken of the configuration. Invalid signatures may be taken if the set-up is not exactly like the configuration shown.

On any tristate lines, a special tip for the P6107 probe may be needed for valid signatures. The special probe tip consists of a 2.2 k-ohm resistor with a wire to any +5 V supply (Tektronix part number 206-0252-01). This ensures that tristate lines will not float, causing unstable or invalid signatures. Signatures requiring the probe tip are marked with an asterisk (*).

It is very important that the board number on the signature tables match the board numbers you are trying to analyze or different signatures may occur.

Assembly: I.C. ACQ.

Assembly #A02
Board # Y-6483-01
670-5985-00

Configuration: CPU provides stimulus from Timing Option Signature Exerciser Routine.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	1826
Stop	AØ9 TP42	DOWN	1826
GND	AØ9 TP43		

Power	SIG
+5	1826
Gnd	0000

U2040	SIG
5	1826
7	587C
9	P723
10	7918
11	82C0
13	1826

U2050	SIG
5	587C
7	90U5
9	82C0
10	82C0
11	7918
13	0000

U3010	SIG
1	U19P
2	U19P

(U3010 cont.)	
3	U19P
4	F423
5	F423
6	F423

U3030	SIG
5	1826
7	90U5
9	882A
10	F423
11	U19P
13	1826

U3050	SIG
1	4AAP
2	1826
3	5288
4	4AAP

(U3050 cont.)	
5	0000
6	4AAP
8	PPFH
9	4AAP
10	A463
11	4AAP
12	0000
13	4AAP

U4010	SIG
2	92C3
3	10A6
4	9A58
5	4AAP
6	7537
7	5712
9	508U
10	HA4A
11	A0F5
12	HA4A
13	A0F5
14	10A6
15	92C3

U4030	SIG
5	92C3
6	HH9P
7	1FCC
15	U9FA
16	HA4A

U4050	SIG
5	92C3
6	86U4
7	AH15
15	PP67
16	HA4A

U5010	SIG
2	P934
3	52H4
4	P536

(U5010 cont.)	
5	9383
6	C45F
7	FPFH
8	A0F5
9	PP67
11	6395
12	U9FA
13	7537
14	0AFU
15	9402
16	H9C5
17	9A58
18	10A6
19	6083

U5030	SIG
5	92C3
6	A773
7	7472
15	9402
16	HA4A

U5050	SIG
5	92C3
6	761P
7	8PC4
15	C45F
16	HA4A

U6010	SIG
2	C8A5
3	52H4
4	P536
5	5A53
6	761P
7	FPFH
8	A0F5
9	86U4
11	PC76
12	HH9P
13	7537
14	0AFU

(U6010 cont.)	
15	A773
16	93P0
17	9A58
18	10A6
19	P24A

U6030	SIG
5	92C3
6	93P0
7	5HH1
15	H9C5
16	HA4A

U6050	SIG
5	92C3
6	C8A5
7	1A3A
15	P934
16	HA4A

U7010	SIG
2	1A3A
3	52H4
4	P536
5	5H34
6	8PC4

(U7010 cont.)	
7	FPFH
8	A0F5
9	AH15
11	6UPU
12	1FCC
13	7537
14	0AFU
15	7472
16	5HH1
17	9A58
18	10A6
19	4577

U7030	SIG
5	92C3
6	P24A
7	4577
15	6083
16	HA4A

U7050	SIG
5	92C3
6	5A53
7	5H34
15	9383
16	HA4A

Assembly: Trigger

Assembly #A03
Board # Y-6535-01
670-6038-00

Configuration: CPU provides stimulus from Timing Option Signature Exerciser Routine.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	1826
Stop	AØ9 TP42	DOWN	1826
GND	AØ9 TP43		

Power	SIG
+5	1826
Gnd	0000

U2020	SIG
2	1826
3	1826
4	91U4
5	1826
6	2652
7	1826

U3020	SIG
2	91U4
3	7537
4	0AFU
5	9031
6	9A58
7	HUFP
9	9CFA
10	128H
11	10A6
12	2652
13	FPFH
14	A0F5

(U3020 cont.)	
15	U714

U4020	SIG
2	1826
4	9031
5	1826
10	6P39
11	1826
14	1826

U5020	SIG
10	5746
11	1826
14	1826

U8020	SIG
2	1826
3	1826
5	1826

(U8020 cont.)	
6	1826
7	5310
9	P94F
10	93A5
11	8A4P
13	1826

U1030	SIG
4	1826
5	0A90
6	1826
7	7537
9	0AFU
10	9A58
11	10A6
13	1826
14	1826

U3030	SIG
12	HUFP

U5030	SIG
9	0F96

U6030	SIG
13	128H

U8030	SIG
2	5310
3	7537
4	0AFU
5	P94F
6	93A5
7	9A58
8	10A6
9	8A4P
11	82FC
14	FPFH
15	1FF7
16	6P39

(U8030 cont.)	
17	52H4
18	P536
19	5746

U1040	SIG
2	7537
3	7537
4	0A90
5	0A90
6	04F7
7	04F7
9	0AFU
10	0AFU
11	9A58
12	9A58
13	0000
14	10A6
15	10A6

U2040	SIG
1	FPFH
7	5F04
9	P536
10	52H4
11	0A90
12	1826
15	A0F5

U3040	SIG
1	HUFP
2	7HU2
3	1826
4	3FA0
5	8667
6	2AFP
8	A463
9	8A1C
10	A463

U5040	SIG
1	A260
2	CA46
8	3C07
9	2321
10	4422
11	5F04

U8040	SIG
1	1826
4	H43A
5	1826
6	P590

U1050	SIG
1	0AFU
5	4422
9	10A6
10	9A58
11	1140
12	1826
14	0000
15	7537

U2050	SIG
1	FPFH
9	P536
10	52H4
11	1140
12	1826
15	A0F5

U4050	SIG
1	1P49
2	08HA
3	2AFP

(U4050 cont.)	
4	1826
5	1AF6
12	1826
13	1826
14	1826
15	1826

U5050	SIG
10	1FF7

U8050	SIG
2	H43A
3	A0F5
4	FPFH
5	P590
6	F023
7	52H4
8	P536
9	C895
11	6PU4
12	CP90
13	10A6
14	9A58
15	HF69
16	9H12
17	0AFU
18	7537
19	CCC3

U3050	SIG
1	8667
2	3FA0
3	08HA
4	A463
5	8A1C
15	A463

U1060	SIG
1	1AF6
3	P536
5	52H4
7	A0F5
9	FPFH
11	7537
13	0AFU
15	9A58
17	10A6

U3060	SIG
1	6PU4
2	508U
3	9CFA
4	6395
5	6UPU
6	PC76
8	3243
10	1140
11	0A90
13	82FC
17	04F7
18	1AF6
19	923H

U7060	SIG
4	1826
5	1826
7	CP90
9	HF69
10	9H12
11	1826
12	1826
14	04F7
15	1826

U8060	SIG
9	CCC3
10	F023
11	C895

TEST POINT	SIG
15	A463
16	8A1C
17	1AF6
19	923H

@

Assembly: Front End

Assembly #A04
Board # Y-6487-01
670-5989-00

Configuration: CPU provides stimulus from Front End Signature Exerciser Routine. Probe must be disconnected from 7D02.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP42	UP	F271
Stop	AØ9 TP41	DOWN	F271
GND	AØ9 TP43		

Power	SIG
+5	F271
Gnd	0000

TEST POINT	SIG
1	4689
2	031H
3	484F
4	9780
5	FUF2
6	96HP
7	6233
8	1HP0
9	2HF8
10	5075
11	2F6P
12	2UCF
13	P57U
14	45AH
15	F9U2
16	0686
17	U69A
18	A887
19	9C65

(TEST POINT cont.)	
33	987F
34	FF0H
35	PF49
36	1A68

U1010	SIG
1	FA65
19	FA65

U1020	SIG
2	PA2A
5	3F37
6	FF8P
9	U21A
11	9U1H
12	UHH7
16	F8FP
19	5322

U1040	SIG
2	031H
5	484F
6	96HP
9	6233
11	U69A
12	1HP0
15	FUF2
16	9780
19	4689

U1050	SIG
2	5075
5	2F6P
6	45AH
9	F9U2
11	9C65
12	0686
15	P57U
16	2UCF

U2010	SIG
1	FA65

U2020	SIG
2	987F
7	PF49
9	A887
10	1A68
15	FF0H

U2030	SIG
2	4689
5	FUF2
9	1HP0
12	9780

U2040	SIG
2	031H
5	6233
9	96HP
12	484F

U2050	SIG
3	5075
4	F9U2
10	2F6P
11	4FAH

U3010	SIG
1	FA65
19	FA65

U3020	SIG
2	987F
5	PF49
9	1A68
12	FF0H

U3030	SIG
2	4689
5	FUF2
9	1HP0
12	9780

U3040	SIG
2	031H
5	6233
9	96HP
12	484F

U3050	SIG
3	0686
4	2UCF
10	2HF8
11	P57U

U4020	SIG
2	987F
5	PF49
9	1A68
12	FF0H

U4040	SIG
1	F271
2	5U05
3	5U05
11	0000
12	9270
13	5001

U4050	SIG
4	27UP
5	0000
7	5U05
9	FF02
10	A2H7
11	9U1H
12	9C65
13	8P3A
14	A887
15	U69A

U5010	SIG
8	UHH7
6	0814
12	3UA6
14	FA65

U5020	SIG
1	FA65
2	5001
3	FA65
11	F271
12	5001
13	5271

U5030	SIG
1	PA2A
2	5322
3	F8FP
12	U21A
13	3F37

U5050	SIG
4	5U05

U6010	SIG
1	FA65
2	FA65
3	0814
7	0000
13	0000
17	0814
18	0000

U6020	SIG
1	UHH7
2	3UA6
3	3UA6
4	UHH7

U6030	SIG
2	F271
3	5U05
4	5U05
6	0000
7	F271
8	F271
9	0814
10	FA65
11	0814
12	FA65
13	0000
14	9H74
15	5U05

Assembly: Front End

Assembly #A04
Board # Y-6487-02
670-5989-01

Configuration: CPU provides stimulus from Front End Signature Exerciser Routine. Probe must be disconnected from 7D02. An "$" indicates all options required.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP42	UP	F271
Stop	AØ9 TP41	DOWN	F271
GND	AØ9 TP43		

Power	SIG
+5	F271
Gnd	0000

TEST POINT	SIG
1	4689
2	031H
3	484F
4	9780
5	FUF2
6	96HP
7	6233
8	1HP0
9	2HF8
10	5075
11	2F6P
12	2UCF
13	P57U
14	45AH
15	F9U2
16	0686
17	U69A
18	A887
19	9C65

(TEST POINT cont.)	
33	987F
34	FF0H
35	PF49
36	1A68

U1010	SIG
1	FA65
11	0000

U1020	SIG
2	PA2A
5	3F37
6	FF8P
9	U21A
11	9U1H
12	UHH7
16	F8FP
19	5322

U1040	SIG
2	031H
5	484F
6	96HP
9	6233
11	U69A
12	1HP0
15	FUF2
16	9780
19	4689

U1050	SIG
2	5075
5	2F6P
6	45AH
9	F9U2
11	9C65
12	0686
15	P57U
16	2UCF

U2010	SIG
1	FA65
11	0000

U2020	SIG
2	987F
7	PF49
9	A887
10	1A68
15	FF0H

U2030	SIG
2	4689
5	FUF2
9	1HP0
12	9780

U2040	SIG
2	031H
5	6233
9	96HP
12	484F

U2050	SIG
3	5075
4	F9U2
10	2F6P
11	4FAH

U2055	SIG
4	27UP
5	0000
7	5U05
9	FF02
10	A2H7
11	9U1H
12	9C65
13	8P3A
14	A887
15	U69A

U3010	SIG
1	FA65
19	FA65

U3020	SIG
2	987F
5	PF49
9	1A68
12	FF0H

U3030	SIG
2	4689
5	FUF2
9	1HP0
12	9780

U3040	SIG
2	031H
5	6233
9	96HP
12	484F

U3050	SIG
3	0686
4	2UCF
10	2HF8
11	P57U

U4020	SIG
2	987F
5	PF49
9	1A68
12	FF0H

U4040	SIG
1	UHH7
2	UHH7
3	UHH7

U5010	SIG
6	0814
8	FA65
12	0814
14	FA65

U5020	SIG
1	FA65
2	5001
3	FA65
11	F271
12	5001
13	5271

U5030	SIG
2	F8FP
3	5322
4	PA2A
5	3F37
6	U21A

U5050	SIG
4	5U05

U6010	SIG
1	FF02
$ 4	0000
$ 6	0000
7	0000
13	0000

U6020	SIG
1	UHH7
2	3UA6

U6030	SIG
2	F271
3	5U05
4	5U05
6	0000
7	F271
8	F271
9	0814
10	FA65
11	0814
12	FA65
13	0000
14	9H74
15	5U05

Assembly: Word Recognizer

Assembly #A05
Board # Y-6486-01
670-5988-00

Configuration: CPU provides stimulus from Word Recognizer Signature Exerciser. Probe must be connected to 7D02. Self stimulus OFF. Signatures marked with an "*" require a 5 Volt pull-up.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	PU2H
Stop	AØ9 TP42	DOWN	PU2H
GND	AØ9 TP43		

Power	SIG
+5	PU2H
Gnd	0000

TEST POINT	SIG
* 9	7661
* 10	65C6
* 11	7661
* 12	65C6
* 13	7661
* 14	74A5
* 15	7661
* 16	74A5
* 25	7661
* 26	74A5
* 27	7661
* 28	74A5
29	13H7
31	02F4

U4010	SIG
1	3AA4
2	H224
3	3FCA
4	994F
5	372F
6	8364
7	1C90
* 10	7661
* 12	65C6
* 14	7661
16	65C6
20	13H7
21	67P2

U8010	SIG
1	3AA4
2	H224
3	3FCA
4	994F
5	372F

(U8010 cont.)	
6	791C
7	P1PU
* 10	7661
* 12	74A5
* 14	7661
* 16	74A5
20	02F4
21	67P2

U2020	SIG
1	1552
2	8364
5	H224
6	67P2
9	994F
11	P675
12	1C90
15	372F
16	3AA4
19	3FCA

U3020	SIG
1	1552
2	8364
5	994F
6	67P2
9	H224
11	P675
12	372F
15	1C90
16	3AA4
19	3FCA

U4020	SIG
1	1552
2	8364
5	994F
6	67P2
9	H224
11	P675
12	372F
15	1C90

(U4020 cont.)	
16	3AA4
19	3FCA

P205	SIG
29A	7661
29B	994F
30A	7661
30B	994F

U5020	SIG
1	994F
* 2	65C6
* 3	65C6
4	PU2H
5	PU2H
* 6	74A5
8	7661
11	PU2H
12	994F

U6020	SIG
1	3AA4
2	H224
3	3FCA
4	994F
5	372F
6	8364
7	1C90
* 10	7661
* 12	65C6
* 14	7661
* 16	65C6
20	13H7
21	67P2

U4030	SIG
1	PU2H
2	7661

(U4030 cont.)	
* 3	7661
* 4	7661
5	7661
* 6	7661
8	994F
11	PU2H
12	PU2H

U5030	SIG
1	1552
2	3FCA
5	3AA4
6	994F
9	H224
11	P675
12	P1PU
15	791C
16	67P2
19	372F

U6030	SIG
1	3AA4
2	H224
3	3FCA
4	994F
5	372F
6	8364
7	1C90
* 10	7661
* 12	74A5
* 14	7661
* 16	74A5
20	02F4
21	67P2

U1040	SIG
1	UA7U
* 3	994F
* 5	67P2
* 7	H224

(U1040 cont.)	
* 9	8364
* 11	3FCA
* 13	3AA4
* 15	372F
* 17	1C90
19	0000

U2040	SIG
1	UA7U
* 3	H224
* 5	67P2
* 7	994F
* 9	8364
* 11	3FCA
* 13	3AA4
* 15	1C90
* 17	372F
19	0000

U3040	SIG
1	UA7U
* 3	H224
* 5	67P2
* 7	994F
* 9	8364
* 11	3FCA
* 13	3AA4
* 15	1C90
* 17	372F
19	0000

U4040	SIG
1	UA7U
* 3	3FCA
* 5	H224
* 7	3AA4
* 9	67P2
* 11	P1PU
* 13	791C
* 15	372F
* 17	994F
19	0000

U5040	SIG
4	UA7U
5	PU2H
6	1552
8	UA7U
9	1552
10	PU2H

U7040	SIG
* 2	74A5
4	994F
5	PU2H
8	994F
9	7661
* 10	7661
12	7661
13	PU2H

U5050	SIG
* 1	09H4
* 2	3AF7
* 3	8FA6
4	37F5
5	UA7U
* 6	273F
12	13H7
15	02F4

U6050	SIG
1	7661
* 2	7661
3	7661
4	7661
* 5	7661
6	7661
8	994F
9	994F
* 10	74A5
11	994F
12	994F
* 13	74A5

U7050	SIG
1	PU2H
2	1552
* 3	7661
* 4	7661
5	7661
6	7661
* 9	65C6
* 10	65C6
11	994F
12	1552
13	1552

Assembly: Expansion Option

Assembly #A06
Board # Y-6485-01
670-5987-00

Configuration: CPU provides stimulus from Expansion Option Signature Exerciser Routine, probe must be disconnected.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	UUC2
Stop	AØ9 TP42	DOWN	UUC2
GND	AØ9 TP43		

Power	SIG
+5	UUC2
Gnd	0000

TEST POINT	SIG
1	3A34
2	8129
3	3F71
4	P179
5	C455
6	7161
7	0P06
8	7A58
9	402A
10	8841
11	UUC2
12	UUC2
13	PACC
14	UUC2
15	3A34
16	8129
17	3F71
18	P179
19	C455

(TEST POINT cont.)	
20	7161
21	0P06
22	7A58
23	U15C
24	812H
25	7782
26	166U
27	P69A
28	F0F8
29	79P2
30	9694
31	U15C
32	812H
33	7782
34	166U
35	P69A
36	F0F8
37	79P2
38	9694

(TEST POINT cont.)	
39	91PP
40	4PAP
41	H48A
42	6369
43	15FA
44	4F55
45	0873
46	5155

U1010	SIG
1	687A
2	U15C
5	812H
6	7782
9	166U
11	687A
12	P69A
15	F0F8
16	79P2
19	9694

U2020	SIG
1	0000
2	3A34
3	U15C
4	812H
5	8129
6	3F71
7	7782
8	166U
9	P179
11	PACC
12	C455
13	P69A
14	F0F8
15	7161
16	0P06
17	79P2
18	9694
19	7A58

U3020	SIG
1	97F8
3	U15C
5	812H
7	7782
9	166U
11	P69A
13	F0F8
15	79P2
17	9694
19	0000

U4020	SIG
Same as U3020	

U5020	SIG
Same as U2020	

U1030	SIG
1	5U0F
6	402A
7	8841
9	UUC2
10	UUC2
13	10U4
15	90C8

U2030	SIG
1	6369
2	H48A
3	4PAP
4	91PP
5	4F55
6	0873
7	5155
9	3A34
11	8129
13	3F71
15	P179
17	UUC2
18	8841

(U2030 cont.)

20	UUC2
21	15FA

U3030	SIG
Same as U2030	
except for:	
18	402A

U1040	SIG
1	82F1
2	687A
3	PACC
4	687A
5	UUC2
6	UUC2
8	97F8
9	0000
10	97F8
11	5U0F
12	5U0F
13	6U0A

U2040	SIG
Same as U2030	
except for:	
9	C455
11	7161
13	0P06
15	7A58

U3040	SIG
Same as U3030	
except for:	
9	C455
11	7161
13	0P06
15	7A58
18	402A

U4040	SIG
1	166U
2	7782
3	812H
4	U15C
5	F0F8
6	79P2
7	9694
10	0PP9
12	U15C
14	0PP9
16	U15C
17	UUC2
20	UUC2
21	P69A

U5040	SIG
Same as U4040	

U1050	SIG
4	UUC2
5	0000
6	0000
8	0000
9	97F8
10	687A
11	97F8
12	49PC
13	10U4

U3050	SIG
2	PACC
7	UUC2
9	3U04
10	UUC2
11	6369
12	H48A
13	4PAP
14	91PP
15	FH4C

U4050	SIG
2	PACC
7	UUC2
9	3U04
10	FH4C
11	5155
12	0873
13	4F55
14	15FA
15	C15P

U5050	SIG
1	U15C
2	U15C
3	0PP9
4	687A
5	UUC2
6	97F8
8	U15C
9	0PP9
10	0PP9
11	0000
12	UUC2
13	UUC2

U6010	SIG
Same as U1010	

Assembly: Acquisition Memory

Assembly #A07
Board # Y-6493-01
670-5995-00

Configuration: CPU provides stimulus from Acquisition Memory Signature Exerciser. Probe must be disconnected from 7D02.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	13P1
Stop	AØ9 TP42	DOWN	13P1
GND	AØ9 TP43		

Power	SIG
+5	13P1
Gnd	0000

TEST POINT	SIG
1	P767
2	61P4
3	7HUP
4	1FA2
5	61F2
6	FCFF
7	P8U7
8	8895
9	UA1F
10	8PHP
11	4046
12	9995
13	2U03
14	8C12
15	3766
16	652H
17	A3F3
18	0000
19	A06P

(TEST POINT cont.)	
20	H092
21	3A94
22	0489
23	2A39
24	0703
25	34P5
26	C636
27	8A43
28	8C6F
29	10PA
30	2A66
31	8895
32	P8U7
33	FCFF
34	61F2
35	1FA2
36	7HUP
37	61P4
38	P767

(TEST POINT cont.)	
39	8895
40	P8U7
41	FCFF
42	61F2
43	1FA2
44	7HUP
45	61P4
46	P767
47	8895
48	P8U7
49	FCFF
50	61F2
51	C374
52	76FF
53	60C0
54	1C64

P207	SIG
20A	13P1
20B	0000
21A	2U03
21B	8C12

U1010	SIG
1	0HU4
2	1P15
3	9AUP
4	CAU2
5	F9A3
6	60C0
8	0000
9	0HU4
10	1P15
11	0000
12	76FF
13	652H

U1020	SIG
1	13P1
2	1C64
3	13P1
4	1A9F
5	652H
6	652H
8	A06P
9	1A9F
10	CAU2
11	0489
12	1P15
13	1A9F

U1025	SIG
1	1P15
2	0000
3	0HU4
4	F9A3
5	0PPU
8	0000
9	0000
10	13P1

U1030	SIG
1	13P1
2	H092
3	3C66
4	1H0P
5	HUUC
6	0PPU
8	60C0
9	13P1
10	7351
11	F174
12	F373
13	60C0

@

U1040	SIG
2	A06P
7	13P1
9	60C0
10	3A94
15	420H

U2010	SIG
3	A5AH
4	0000
5	3C66
6	9AUP
7	A498
9	3766
10	8C12
11	2U03
12	9995
13	4046
14	8PHP
15	UA1F

U2020	SIG
2	A095
3	C374
6	652H
7	76FF
9	0PPU
10	0885
11	1C64
14	60C0
15	7351

U2030	SIG
1	A498
2	2975
4	A4A0
6	F174
8	0000
14	1C64
16	13P1
18	A3F3
19	A498

U2040	SIG
2	A06P
7	13P1
9	60C0
10	420H
15	H092

U3010	SIG
1	0000
2	1FA2
3	8AA4
4	6790
5	7HUP
6	61P4
7	HC56
8	U587
9	P767
11	0489
12	61F2
13	A440
14	U5AH
15	FCFF
16	P8U7
17	96P6
18	A5UP
19	8895

U3020	SIG
1	C636
2	34P5
3	0703
4	2A39
5	8C6F
6	10PA
7	2A66
9	8895
11	P8U7

(U3020 cont.)	
13	FCFF
15	61F2
18	UA1F
20	652H
21	8A43

U3030	SIG
1	3766
2	8A43
4	8C6F
6	10PA
8	2A66
12	2A39
14	0703
16	34P5
18	C636
19	3766

U3040	SIG
1	13P1
2	0489
7	13P1
9	C374
10	13P1
11	C636
12	34P5
13	0703
14	2A39
15	4F46

U4010	SIG
Same as U3010	

U4030	SIG
Same as U3020	
except for.	
9	1FA2
11	7HUP
13	61P4
15	P767

U4040	SIG
1	13P1
2	0489
7	13P1
9	C374
10	4F46
11	2A66
12	10PA
13	8C6F
14	8A43
15	U1P3

U5010	SIG
Same as U3010	

U5020	SIG
Same as U3020	
except for:	
18	8PHP

U5030	SIG
Same as U3020	
except for:	
9	1FA2
11	7HUP
13	61P4
15	P767
18	8PHP

U5040	SIG
1	9AUP
2	891U
3	5U68
4	1P15
5	0HU4
6	A095
8	4F89
9	AAP9
10	1H0P
11	A5AH
12	69C2
13	HUUC

U6010	SIG
4	A5UP
5	96P6
6	U5AH
7	A440
10	0489
12	61F2
13	FCFF
14	P8U7
15	8895

U6020	SIG
Same as U3020 except for:	
18	4046

U6030	SIG
Same as U3020 except for:	
9	1FA2
11	7HUP
13	61P4
15	P767
18	4046

U6040	SIG
1	13P1
2	C741
3	P202
4	0489
5	8C12
6	C741
7	A4A0
9	0000
10	13P1
11	2U03
12	13P1
13	0000
14	A3F3
15	13P1

U7010	SIG
1	13P1
2	0000
3	13P1
4	13P1
5	13P1
6	0000
8	A3F3
9	60C0
10	F373
11	P202
12	U1P3
13	F174

U7020	SIG
Same as U3020 except for:	
18	9995

U7040	SIG
1	F174
2	13P1
3	13P1
4	A06P
5	13P1
6	3A94
7	2975
9	0000
10	13P1
11	13P1
12	8C12
13	13P1
14	13P1
15	13P1

Assembly: State Machine

Assembly #A08
Board # Y-6484-02
670-5986-00

Configuration: CPU provides stimulus from State Machine Signature Exerciser. Probe must be disconnected from 7D02. *Requires +5 V pullup.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	2U19
Stop	AØ9 TP42	DOWN	2U19
GND	AØ9 TP43		

Power	SIG
+5	2U19
Gnd	0000

TEST POINT	SIG
1	UP2F
* 3	9217
* 4	747P
* 5	78U9
* 6	H5H9
* 7	77PF
* 8	7P07
* 9	CFH5
*10	140C
12	F75F
13	2U2C

U1010	SIG
1	5FFF
2	2U2C
3	HUU6
4	067P
5	2U19
6	067P
8	2U2C
9	2U2C
10	2U19

(U1010 cont.)

U1020	SIG
1	0032
2	9020
4	P4H5
6	54A4
8	044F
10	2967
11	0795
12	288F
13	0032

U1030	SIG
1	2U19
2	97C5
3	2U19
4	HUU6
5	2U19
6	78PU
10	78PU
11	2U19
12	HUU6
13	2U19
14	91FC
15	2U19

U1040	SIG
1	75C7
2	P4H5
* 3	118A
4	PU60
5	P4H5
* 6	5092
7	58PF
9	77H5
* 10	U48P
12	5A4A
14	C50A

U1050	SIG
2	F588
3	740H
*4	0HAP
*5	U5CC
*6	29H7
*7	0A61
8	5A4A
9	1CP2
10	UP2F
12	PU60
13	58PF

(U1050 cont.)	
14	77H5
*16	1227
*17	9HHF
*18	121F
*19	1FF6

U1060	SIG
*1	9217
*2	747P
3	067P
6	01CA
*7	77PF
*9	7P07
*10	CFH5
*11	140C
12	84F9
*13	0HAP
*14	78U9
*15	H5H9

U2010	SIG
7	5FFF
10	C94A
12	0000
13	2U2C
14	6H27

U2020	SIG
1	0032
2	2PU2
3	01PC
4	2967
6	044F
8	54A4
10	F91F
11	0000
12	9020
13	0032

U2030	SIG
1	2967
2	F7PU
3	F7PU
4	UP2F
5	6FC1
6	FCFF
7	P4H5
9	5C14
10	740H
11	9014
12	UP2F
13	9014
14	P77C
15	P4H5

U2040	SIG
1	067P
2	9A13
3	78PU
4	0000
5	6P55
6	0000
7	UP2F
9	F7PU
10	54A4
11	0000
12	54A4
13	0795
14	F115
15	067P

U2050	SIG
1	48C6
*11	1FF6
*12	121F
*13	9HHF
*14	1227
*15	0A61

(U2050 cont.)	
*16	29H7
*17	U5CC
*18	0HAP
19	H115

U2060	SIG
*1	H5H9
*2	78U9
*3	747P
*4	9217
*5	7P07
*6	CFH5
*7	140C
*9	0HAP
*10	C031
*11	U5CC
*12	7F3A
*13	29H7
*14	91FC
*15	0A61
*16	01PC
18	067P
20	H515
*21	77PF

U3010	SIG
1	F115
2	PP0F
3	2104
4	2104
5	2967
6	PP0F
8	5C14
9	740H
10	06UA
11	P77C
12	2967
13	9020

U3020	SIG
1	01PC
2	91FC
3	01PC
4	0795
5	97C5
6	0795
8	9020
9	2967
10	97C5
11	9020
12	2967
13	91FC

U3030	SIG
1	F91F
2	U462
3	54P9
4	F75F
5	54P9
6	PC1F
7	F405
9	F91F
10	P605
11	6FC1
12	F75F
13	F7PU
14	F7PU
15	2U19

U3040	SIG
1	067P
2	9A13
3	78PU
4	0000
5	6144
7	F75F
9	F7PU

(U3040 cont.)	
12	54A4
14	F8A1
15	067P

U3050	SIG
1	546U
*2	0A61
*3	78U9
4	01CA
*5	0HAP
*6	9HHF
7	12A4
*8	CFH5
*9	121F
11	4CAU
*12	1FF6
*13	140C
*14	747P
*15	29H7
*16	U5CC
*17	9217
*18	H5H9
*19	1227

U4010	SIG
1	F8A1
2	P7C8
3	CP15
4	CP15
5	P7C8
6	2967
8	F405
9	PC1F
10	0U4P
11	U462
12	2967
13	9020

U4020	SIG
1	F2F3
2	896F
3	4CAU
4	0000
5	067P
6	2U19
8	2U19
9	78PU
10	0032
11	2U19
12	0032
13	78PU

U4030	SIG
1	2U2C
2	0000
3	0032
4	U462
5	F7PU
6	H691
8	F7PU
9	F588
10	P77C
11	0000
12	9A13
13	C50A

U4040	SIG
1	UH12
2	F91F
* 3	118A
4	2607
5	F91F
* 6	5092
7	3CCC
9	A618
* 10	U48P
12	21C7
14	C50A

U4050	SIG
2	H691

(U4050 cont.)	
3	PC1F
*4	0HAP
*5	U5CC
*6	29H7
*7	0A61
8	21C7
9	9F56
10	F75F
12	2607
13	3CCC
14	A618
15	0000
*16	1227
*17	9HHF
*18	121F
*19	1FF6

U4060	SIG
1	H115
*3	H5H9
*5	747P
*7	9217
*9	140C
*11	CFH5
*13	7P07
*15	77PF
*17	78U9
19	9A13

U5010	SIG
1	7F3A
2	5323
3	067P
4	2967
5	0795
6	288F
8	0032
9	2U2C
10	2967
11	067P
12	2U19
13	0000

U5020	SIG
1	2U2C
2	0032
3	FCFF
4	9020
5	P605
6	9020
8	2PU2
10	9020
12	9020

U5030	SIG
6	0000
8	UP0F
9	H115
10	F8A1
11	P7C8
12	F115
13	PP0F

U5040	SIG
1	2967
2	PC12
*3	9P4A
4	9P4A
5	FA8P
*6	7237
7	7237
9	12A4
10	FCFF
11	P605
12	0000
13	0000
14	0000

U5050	SIG
1	2U19
*2	FA8P
*3	1FF6
*4	121F
*5	PC12
*6	9A13
*7	9HHF

(U5050 cont.)	
*8	1227
*9	067P
11	8247
*12	PP0F
*13	0HAP
*14	0A61
*15	HAAP
*16	AC9P
*17	29H7
*18	U5CC
*19	P7C8

U5060	SIG
* 1	H5H9
* 2	78U9
* 3	747P
* 4	9217
* 5	7P07
* 6	CFH5
* 7	140C
* 9	1227
*10	97C5
*11	9HHF
*12	0795
*13	121F
*14	9P4A
*15	1FF6
*16	7237
20	H515
*21	77PF

U6010	SIG
1	0032
2	0000
4	C94A
5	2U19
6	0000
9	2U19
10	C94A
12	0000
13	0032

U6020	SIG
1	0000
2	UP0F
3	H115
4	2U19
5	H115
6	UP0F
8	6ACH
9	45A4
10	2967
11	0000
12	7F3A
13	0032

U6030	SIG
1	2U19
2	044F
3	044F
4	2967
6	0000
8	0000
10	2967
11	044F
12	044F
13	2U19

U6040	SIG
1	2U19
2	AC9P
7	2U19
9	2U19
14	HAAP
15	2U19

U6050	SIG
* 1	691F
* 2	236C
* 3	F482
* 4	2U3A
5	67AU
6	UP0F

(U6050 cont.)	
9	C94A
10	6FC1
11	8247
12	6144
13	6P55
14	84F9
15	H515

U6060	SIG
1	60A6
*2	91FC
*3	29H7
*4	01PC
*5	0A61
*6	7F3A
*7	U5CC
*8	C031
*9	0HAP
*11	1FF6
*12	7237
*13	121F
*14	9P4A
*15	9HHF
*16	0795
*17	1227
*18	97C5

U7010	SIG
1	PP0F
2	9020
3	F115
4	0U4P
5	P7C8
6	F7PU
8	F7PU
9	PP0F
10	06UA
11	9020
12	F8A1
13	P7C8

U7015	SIG
* 1	C031
2	2U19
3	9020
4	F7PU
5	F405
6	CP15
8	2104
9	F7PU
10	5C14
11	9020
12	0000
13	0000

U7040	SIG
1	2U2C
2	5323
3	2U19
4	6144
5	9F56
6	UH12
8	75C7
9	1CP2
10	6P55
11	2U19
12	896F
13	45A4

U7050	SIG
* 1	691F
* 2	236C
* 3	F482

(U7050 cont.)	
* 4	2U3A
5	48C6
6	UP0F
7	6H27
9	54P9
10	9014
11	F2F3
12	9F56
13	1CP2
14	546U
15	60A6

U7060	SIG
1	C50A
*2	H5H9
3	H6C3
4	5C14
*5	77PF
*6	747P
7	9A90
8	9P4A
*9	CFH5
11	2U2C
*12	140C
13	7237
14	F405
*15	7P07
*16	9217
17	F8A1
18	A085
*19	78U9

Assembly: State Machine (Time Base Divider)

Assembly #A08
Board # Y-6484-02
670-5986-00

Configuration: CPU provides stimulus from a free running 6 MHz Clock. No special setup required. 7D02 must be ON (no Signature Exerciser Routine). These signatures can be run with or without the PM101 Self Test Stimulus.

Software: N/A

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ8 U7020-4	DOWN	N/A
Start	AØ8 U6040-6	UP	773U
Stop	AØ8 U6040-6	DOWN	773U
GND	AØ8 TP11		

Power	SIG
+5	773U
Gnd	0000

P208	SIG
24B	773U
25A	9HC6
25B	937H
26A	FA64

U5030	SIG
1	0000
2	773U
3	PA89
4	9HC6

U6040	SIG
1	0000
3	FA64
4	773U
5	FA64
6	773U
11	773U
10	773U
12	FA64

(U6040 cont.)	
13	FA64
15	0000

U7020	SIG
2	0000
5	94F9
6	FA64
9	937H
12	FPP3
13	FPP3
15	FA64

U7030	SIG
1	937H
2	773U
6	PA89
9	PA89
10	773U
14	0000

Assembly: CPU (Address Decoder)

Assembly #A09
Board # Y-6482-02
670-5984-00

Configuration: CPU provides stimulus from Address Decoder Signature Exerciser.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	AØ9 TP49	UP	N/A
Start	AØ9 TP41	UP	1CAU
Stop	AØ9 TP42	DOWN	1CAU
GND	AØ9 TP43		

Power	SIG
+5	1CAU
Gnd	0000

U4045	SIG
11	1PHF
12	FP01
13	0573

U4050	SIG
1	1CAU
2	0000
3	A51A
4	HA16
5	1417
6	CPC5
8	0000
9	1CAU
10	1CAU
11	1CAU
12	1CAU
13	2846

U4055	SIG
4	13CC
5	3CUH
6	2846
8	1CAU
9	0000
10	0000
11	AHFU
12	1PHF
13	C313

U4065	SIG
5	CA00
6	A1AU
8	420C
9	59A4

U4070	SIG
6	0000
7	1PHF
8	0573
12	0573
13	1PHF
14	0000

U4080	SIG
1	7869
2	CA00
3	59A4
4	FP01
5	CPC5
6	AHFU
7	13CC
9	3CUH
10	P755
11	P845
12	8AU2
13	5PH9
14	A0P4
15	U683

Assembly: Display Board

Assembly #A10
Board # Y-6481-02
670-5983-00

Configuration: Stimulus from Display Signature Exerciser Routine.

Software: 160-0361-00 Diagnostic ROM

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	A1Ø U2020-6	DOWN	N/A
Start	A1Ø U4042-3	UP	01U0
Stop	A1Ø U4042-3	UP	01U0
GND	P208 1B		

Power	SIG
+5	AF28
Gnd	0000

U1010	SIG
2	5FF1
4	4570
5	4570
7	5FF1
9	6C1C
11	C490
12	3FCF
13	5846
14	43U4
15	PUHF

U1020	SIG
1	24FH
2	7652
3	841F
4	HU1F
5	CP22
6	9189
7	U9HH

(U1020 cont.)	
9	5932
10	C635
11	C1A6
12	2236
13	C274
14	U045
15	F15P

U1030	SIG
2	AF2A
3	3PC5
4	C89C
5	5HU7
10	U45U
11	403H
12	76UP
13	2CPC
14	6844
15	6C1C

U1040	SIG
1	P4P7
2	7728
3	31HU
4	7HP6
5	C2UU
6	P799
7	F374
8	8U71
9	AF2A
10	3PC5
11	C89C
13	5HU7
14	U45U
15	403H
16	76UP
17	6844
18	F02A
19	7AFA
20	F02A
21	AF28
22	UU17
23	511P

U1050	SIG
11	3FCF
12	7AFA
13	UU17
14	511P
15	P4P7
16	7728
17	31HU
18	7HP6
19	AF28

U2010	SIG
1	6418
2	HF08
3	6F02
4	0000

(U2010 cont.)	
5	0000
7	6C1C
10	C0P5
11	95C2
12	HU1F
15	358H

U2020	SIG
1	AF28
2	0000
7	0000
8	AF28
9	0000
10	F02A
11	6F02
12	0000

U2030	SIG
1	6F02
2	0000
3	24FH
4	7652
5	841F
6	CP22
9	6F02
10	HF08
11	6418
13	AF28

U2050	SIG
1	AF28
3	CP22
4	CP22
6	841F
7	841F
9	7652
10	7652
12	24FH
13	24FH

U3010	SIG
1	95C2
2	5FF1
3	358H
5	09A5
6	A58H
8	049P
9	A8C6
11	0000
13	C0P5

U3020	SIG
2	AF28
3	6C1C
4	95C2
5	AF28
9	AF28
10	AF28
12	AF28

U3030	SIG
1	4570
2	0000
3	8U71
4	F374
5	P799
6	C2UU
10	4570
11	9189
12	0000
13	CP22

U3040	SIG
1	H4A4
2	P952
3	9189
4	CP22
5	24FH
6	7652
7	841F

(U3040 cont.)	
8	0000
10	AF28
11	3FCF
12	7AFA
13	UU17
14	511P
15	01U0
16	2HF2
17	7328

U3042	SIG
1	H4A4
2	P952
3	9189
4	CP22
5	24FH
6	7652
7	841F
8	0000
10	AF28
11	P4P7
12	7728
13	31HU
14	7HP6
15	01U0
16	2HF2
17	7328

U3050	SIG
1	AF28
3	7328
4	7328
6	H4A4
7	H4A4
9	P952
10	P952
12	9189
13	9189

U4010	SIG
1	AF28
2	0000
3	AF28
4	1743
5	2CPC
6	3FA8
8	85HH
9	UU17
10	7AFA
11	1743
12	A3H3
13	C490

U4020	SIG
1	5846
2	A7H5
3	85HH
4	0HF3
5	5FF1
6	3FA8
9	AF28
10	0000
11	43U4
12	U045
13	A3H3

U4030	SIG
1	2HF2
2	01U0
3	0000
4	4570
5	24FH
6	0000
8	A7H5
9	UU17

(U4030 cont.)	
10	511P
11	0000
12	C2UU
13	8U71

U4040	SIG
1	AF28
2	AF28
4	95C2
5	AF28
8	50U5
10	AF28
12	0HF3

U4042	SIG
1	2HF2
2	0000
3	01U0
8	2HF2
9	7328
10	H4A4
11	P952
12	0000
13	C2UU

U4050	SIG
1	AF28
4	AF28
6	0000
7	0000
9	01U0
10	01U0
12	2HF2
13	2HF2

Assembly: Front End (GP Probe)

Assembly #A04
Board # Y-6487-01
670-5989-00

Configuration: PM101 Self Test Stimulus and Per. Mod. System signature Exerciser Routine. Modify Self Test Stimulus by disconnecting Q6, Q7, and Q8 from T17, T18, and T19 and connect to T2, T3, and T4. This setup produces a Per. Mod. diagnostic failure.

Software: 160-0361-00 Diagnostic ROM -- 160-0853-00 GP Probe ROM.

Analyzer: Sony Tek 308.

	Location	S/W	SIG
Clock	AØ4U5050-1	DOWN	0000
Start	J106-11D	UP	0000
Stop	J106-11D	UP	0000

Power	SIG
+5	0001
Gnd	0000

TEST POINT	SIG
20	0000
21	UUUP
22	CCCC
23	HAP6
24	CCCC
25	5555
26	5554
27	5554
28	3C97
29	UUUU
30	HAP7
31	5555
32	3C96
37	HAP6
38	HAP6
39	0001
41	0000
42	0000

U1010	SIG
3	52F8
5	UPFH
7	0AFA
9	5H21
11	7F7F
13	CCCC
15	5555
17	UUUU

U2010	SIG
12	1293
14	HPP0
16	2H70
18	HC89

U3010	SIG
2	UPFH
4	5H21
6	CCCC
8	UUUU
11	5555
13	7F7F
15	52F8
17	0AFA

U4010	SIG
2	UUUU
3	HC89
4	HAP7
5	HPP0
6	5555
7	2H70
8	3C96
9	1293
11	1293
12	3C96
13	2H70
14	5555
15	HPP0
16	HAP7
17	HC89
18	UUUU

U5010	SIG
2	CCCC
3	UUUP
4	5555
5	HAP6
7	5554
9	3C97
11	3C96
15	HA97
16	5554
17	AUUU
18	CCCA

U6010	SIG
2	0001
5	5555
9	CCCC
11	CCCC
15	5555

U2030	SIG
3	5554
4	UUUP
8	HAP6
10	UUUU
11	5555

U2040	SIG
3	3C97
4	HAP6
8	HAP6
10	HAP7
11	3C96

U2050	SIG
2	CCCC
5	UUUP
8	0000
9	CCCC

U3020	SIG
3	CCCC
4	5555
8	HAP6
10	CCCA
11	5554

U3030	SIG
3	5554
4	UUUP
8	1180
10	UUUU
11	5555

U3040	SIG
3	3C97
4	HAP6
8	HAP6
10	HAP7
11	3C96

U3050	SIG
2	5554
5	5554
8	0001
9	5555
12	5555

U4020	SIG
3	CCCC
4	5555
8	HAP6
10	CCCA
11	5554

U4030	SIG
3	0001
4	CCCA
5	0000
6	0000
8	0000
9	0000
10	0001
11	0001

U4040	SIG
4	0001
5	0001
6	HAP6
8	HAP6
9	0001
10	0001

U5020	SIG
4	0000
5	0000
6	0000

U5030	SIG
5	0001
6	0000
8	0000
9	0001
10	0000
11	0000

U5040	SIG
4	0000
7	0000
9	0000
12	0000

U5050	SIG
1	0001
2	0000
3	HAP6
5	0000
6	0001
7	0001
9	0000
10	0001
11	HAP6
12	0000
13	0001
14	0001
15	0001

U6020	SIG
5	0000
6	HAP6
8	HAP6
9	0000
10	HAP6
11	0000
12	0000
13	0001

U6050	SIG
6	0001
7	0001
14	0001
15	0001

Assembly: Front End (GP Probe)

Assembly #A04
Board # Y-6487-02
670-5989-01

Configuration: PM101 Self Test Stimulus and Per. Mod. System signature Exerciser Routine. Modify Self Test Stimulus by disconnecting Q6, Q7, and Q8 from T17, T18, and T19 and connect to T2, T3, and T4. This setup produces a Per. Mod. diagnostic failure.

Software: 160-0361-00 Diagnostic ROM -- 160-0853-00 GP Probe ROM.

Analyzer: Sony Tek 308.

	Location	S/W	SIG
Clock	AØ4U5050-1	DOWN	0001
Start	J106-11D	UP	755P
Stop	J106-11D	UP	755P

Power	SIG
+5	0001
Gnd	0000

TEST POINT	SIG
20	0000
21	UUUP
22	CCCC
23	HAP6
24	CCCC
25	5555
26	5554
27	5554
28	3C97
29	UUUU
31	5555
37	HAP6
38	HAP6
39	0001
42	0000

U1010	SIG
2	52F8
5	UAFH
6	0AFA
9	5H21
12	7F7F
15	CCCC
16	UUUU
19	5555

U2010	SIG
9	HAP7
12	1293
15	HPP0
16	2H70
19	HC89

U3010	SIG
2	UPFH
4	5H21
6	CCCC
8	UUUU
11	5555
13	7F7F
15	52F8
17	0AFA

U4010	SIG
2	UUUU
3	HC89
4	HAP7
5	HPP0
6	5555
7	2H70
8	3C96
9	1293
11	1293
12	3C96
13	2H70
14	5555
15	HPP0
16	HAP7
17	HC89
18	UUUU

U5010	SIG
2	CCCC
3	UUUP
4	5555
5	HAP6
7	5554
9	3C97
11	3C96
15	HA97
16	5554
17	AUUU
18	CCCA

U6010	SIG
5	5555
9	CCCC

(U6010 Cont.)	
11	CCCC
15	5555

U2030	SIG
3	5554
4	UUUP
8	HAP6
10	UUUU
11	5555

U2040	SIG
3	3C97
4	HAP6
8	HAP6
10	HAP7
11	3C96

U2050	SIG
2	CCCC
5	UUUP
8	0000
9	CCCC

U3020	SIG
3	CCCC
4	5555
8	HAP6
10	CCCA
11	5554

U3030	SIG
3	5554
4	UUUP
8	1180
10	UUUU
11	5555

U3040	SIG
3	3C97
4	HAP6
8	HAP6
10	HAP7
11	3C96

U3050	SIG
2	5554
5	5554
8	0001
9	5555
12	5555

U4020	SIG
3	CCCC
4	5555
8	HAP6
10	CCCA
11	5554

U4030	SIG
8	0000
9	0000
10	0001
11	0001

U4040	SIG
4	0001
5	0001
6	HAP6
8	HAP6
9	0001
10	0001
11	0001
12	0001
13	0001

U4050	SIG
1	0000
2	0000
3	0001
4	0000
5	0001
6	0001

(U4050 Cont.)	
8	0000
9	0000
10	0001

U5020	SIG
8	0000
9	0000
10	0000

U5030	SIG
9	0001
10	0001
11	0000
12	0000
13	0000
14	0000

U5040	SIG
4	0000
7	0000
9	0000
12	0000

U5050	SIG
1	0001
2	0000
3	HAP6
5	0000
6	0001
7	0001
9	0000
10	0001
11	HAP6
12	0000
13	0001
14	0001
15	0001

U6020	SIG
3	0000
4	0001
5	0000
6	HAP6
8	HAP6
9	0000
10	HAP6
11	0000
12	0000
13	0001

U6050	SIG
6	0001
7	0001
14	0001
15	0001

Assembly: Word Recognizer (GP Probe)

Assembly #A05
Board # Y-6486-01
670-5988-00

Configuration: PM 101 Self Test Stimulus connected.

Software: 160-0361-00 Diagnostic ROM -- 160-0853-00 PM 101 ROM.

Analyzer: Sony Tek 308

	Location	S/W	SIG
Clock	J204-23A	UP	N/A
Start	J106-11D	DOWN	0000
Stop	J106-11D	UP	0000
GND	J204-1A		

Power	SIG
+5	1180
GND	0000

U1010	SIG	U2010	SIG
1	0000	1	0000
2	A7A2	2	P254
3	4PCC	3	H6AA
4	5342	4	0000
5	108P	5	0000
6	0108	6	0P0P
7	1100	7	0F62
8	0U7U	8	FF4F
9	052A	9	5HC4
11	052A	11	5HC4
12	0U7U	12	FF4F
13	1100	13	0F62
14	0108	14	0P0P
15	108P	15	0000
16	5342	16	0000
17	4PCC	17	H6AA
18	A7A2	18	P254
19	0000	19	0000

U2020	SIG
3	A7A2
4	0108
7	5342
8	0U7U
13	4PCC
14	108P
17	1100
18	052A

U3010	SIG
1	0000
2	A7A2
3	108P
4	5342
5	4PCC
6	0108
7	1100
8	0U7U
9	052A
11	052A
12	0U7U
13	1100
14	0108
15	4PCC
16	5342
17	108P
18	A7A2
19	0000

U3020	SIG
3	P254
4	FF4F
7	0000
8	0P0P
13	H6AA
14	0000
17	0F62
18	5HC4

U4020	SIG
3	A7A2
4	0U7U
7	5342
8	0108
13	108P
14	4PCC
17	1100
18	052A

U5030	SIG
3	5HC4
4	0F62
7	FF4F
8	0P0P
13	71F6
14	0000
17	0000
18	H6AA

Assembly: Expansion Option (GP Probe)

Assembly #A06
Board # Y-6485-01
670-5987-00

Configuration: PM 101 provides stimulus from Per. Mod. System Signature.

Software: 160-0361-00 Diagnostic ROM -- 160-0853-00 GP Probe ROM.

Analyzer: Sony Tek 308.

	Location	S/W	SIG
Clock	P204-23A	UP	0000
Start	J106-11D	DOWN	0000
Stop	J106-11D	UP	0000
GND	P204-1A		

Power	SIG
+5	1180
GND	0000

U1010	SIG
3	FF4F
4	5HC4
7	0P0P
8	0F62
13	0000
14	H6AA
17	P254
18	0000

U3010	SIG
2	FF4F
3	0000
4	5HC4
5	P254
6	0P0P
7	H6AA
8	0F62
9	0000
11	0000
12	0F62

(U3010 cont.)	
13	H6AA
14	0P0P
15	P254
16	5HC4
17	0000
18	FF4F

U4010	SIG
2	FF4F
3	0000
4	5HC4
5	P254
6	0P0P
7	H6AA
8	0F62
9	0000
11	0000
12	0F62
13	H6AA
14	0P0P

(U4010 cont.)

15	P254
16	5HC4
17	0000
18	FF4F

U6010	SIG
3	FF4F
4	5HC4
7	0P0P
8	0F62
13	0000
14	H6AA
17	P254
18	0000

Assembly: CPU (Kernel)

Assembly #AØ9
Board # YA-6482-02
670-5984-00

Configuration: CPU in test mode, SIP Resistor Pack installed. An "*" indicates that +5 Volt Pull-up is required.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
160-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer: Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	AØ9 U3050-31	UP	N/A,	+5	0001
Start	AØ9 U3050-28	UP	755P,	Gnd	0000
Stop	AØ9 U3050-28	UP	755P		
GND	AØ9 TP43				

U1040	SIG	U2040	SIG
1	UPFF	1	UPFF
2	0AFC	2	0AFC
3	5H20	3	5H20
4	7F7H	4	7F7H
5	UUUP	5	UUUP
6	5554	6	5554
7	CCCA	7	CCCA
8	5F6A	8	5F6A
10	0000	10	0000
* 11	1A6U	* 11	54FU
* 12	F2U8	* 12	40HP
* 13	83F6	* 13	841P
* 14	HPPC	* 14	3406
15	2H71	15	2H71
16	HC88	16	HC88
17	52F9	17	52F9

U1045	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	UAP0
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2045	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	UAP0
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1050	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	3FC7
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2050	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	3FC7
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1055	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	9PF1
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2055	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	9PF1
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1060	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	P5H8
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2060	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	P5H8
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1065	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	7H99
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2065	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	7H99
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1070	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	85H3
10	0000
* 11	1A6U
* 12	F2U8
* 13	83F6
* 14	HPPC
15	2H71
16	HC88
17	52F9

U2070	SIG
1	UPFF
2	0AFC
3	5H20
4	7F7H
5	UUUP
6	5554
7	CCCA
8	85H3
10	0000
* 11	54FU
* 12	40HP
* 13	841P
* 14	3406
15	2H71
16	HC88
17	52F9

U1080	SIG
1	HPP1
2	1292
3	HAP6
4	12U3
5	12U3
7	0C9F
9	85H3
10	7H99
11	P5H8
12	9PF1
13	3FC7
14	UAP0
15	5F6A

U3010	FIG
1	52F9
2	UPFF
3	0AFC
4	5H20
5	7F7H
6	CCCA
7	5554
8	UUUP
* 9	HPPC
* 10	83F6
* 11	F2U8
* 13	1A6U
* 14	3406
* 15	841P
* 16	40HP
* 17	54FU
18	1292
19	HPP1
20	P255
21	HAP6
22	2H71
23	HC88

U3020	SIG
Same as U3010	
except for:	
20	U3H5

U3030	SIG
Same as U3010	
except for:	
20	0996

U4010	SIG
Same as U3010	
except for:	
20	6H49

U4020	SIG
Same as U3010	
except for:	
20	F2A6

U4030	SIG
Same as U3010	
except for:	
20	PC01

U4040	SIG
1	3C97
2	3826
3	755P
4	0000
5	0000
6	0001
7	4P0A
9	12U3
10	PC01
11	F2A6
12	6H49
13	0996
14	U3H5
15	P255

U3065	SIG
2	UUUP
5	5554
6	CCCA
9	7F7H
11	0000
12	5H20
15	0AFC
16	UPFF
19	52F9

U4045	SIG
2	0001
5	0001
9	0000
11	0000
12	0000
13	0001

U4050	SIG
2	0000
3	3C97
4	3826
5	755P
6	4P0A
8	0000
9	0001
10	0001
11	0001
12	0001
13	0000

U4070	SIG
2	HC88
3	2H71
4	HPP1
5	1292
6	0000
7	0000
8	0001
12	0001
13	0000
14	0000
15	1292
16	HPP1
17	2H71
18	HC88

U4075	SIG
1	0001
19	4P0A

U4080	SIG
1	HAP6
2	0000
3	0000
4	0000
5	4P0A
6	0001
7	0001
9	0001
10	0001
11	0001
12	0001
13	0001
14	383A
15	7631

Assembly:
CPU (Kernel) - Continued with the following setup:

	Location		S/W	SIG	Power	SIG
Clock	AØ9	U3050-31	UP	N/A	+5	755U
Start	AØ9	U3050-28	DOWN	0000	Gnd	0000
Stop	AØ9	U3050-28	UP	0000		
GND	AØ9	TP43				

U2080	SIG
1	0000
* 2	7H21
* 3	1U0H
* 4	82HP
* 5	95P8
* 6	P9FC
* 7	331H
* 8	5316
* 9	F7H4
* 11	F7H4
* 12	5316
* 13	331H
* 14	P9FC
* 15	95P8
* 16	82HP
* 17	1U0H
* 18	7H21
19	0000

U4065	SIG
* 2	1U0H
* 12	7H21

U4075	SIG
* 2	F7H4
3	F7H4
4	1U0H
5	1U0H
6	82HP
7	82HP
8	P9FC
9	P9FC
11	5316
12	5316
13	7H21
14	7H21
15	95P8
16	95P8
17	331H
18	331H

Assembly: Front Panel, Keyboard (Kernel)

Assembly #A01, A16
Board # YA-6488-01
670-6039-00

Configuration: CPU in Test Mode. SIP resistor pack installed. The correct button on keyboard must be pressed for valid signatures. Buttons on the keyboard are designated by **Row** and **Column** as depicted below. Note that each x corresponds to a key on the 7D02 keyboard. The up and down cursor keys actually fall between columns 7 and 8, however. For convenience, the cursor up key is assumed to be in column 7 and the cursor down key in column 8.

	COLUMN							
	1	2	3	4	5	6	7	8
ROW 1	x	x	x	x	x	x	x	x
ROW 2	x	x	x	x	x	x		
ROW 3	x	x	x	x	x	x	x	x
ROW 4	x	x	x	x	x		x	
ROW 5			x	x	x	x	x	x
ROW 6	x		x	x	x	x		x

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
160-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer: Sony Tek 308.

	Location	**S/W**	**SIG**
Clock	AØ9U3050-31	UP	N/A
Start	AØ9U3050-28	UP	755P
Stop	AØ9U3050-28	UP	755P
GND	AØ9 TP43		

Power	**SIG**
+5	0001
Gnd	0000

AØ1U2055 Pin		ROW 1	ROW 2	ROW 3	ROW 4	ROW 5	ROW 6
2	COLUMN 1	UUUU	5555	CCCC	7F7F	0001	0AFA
4	" 2	UUUU	5555	CCCC	7F7F	0001	0001
6	" 3	UUUU	5555	CCCC	7F7F	5H21	0AFA
8	" 4	UUUU	5555	CCCC	7F7F	5H21	0AFA
12	" 5	UUUU	5555	CCCC	7F7F	5H21	0AFA
14	" 6	UUUU	5555	CCCC	7F7F	5H21	0AFA
16	" 7	UUUU	0001	CCCC	7F7F	5H21	0001
18	" 8	UUUU	0001	CCCC	0001	5H21	0AFA

		COLUMN							
AØ1U2025 Pin		1	2	3	4	5	6	7	8
2	ROW 1	UUUU	UUUU	UUUU	UUUU	UUUU	UUUU	UUUU	UUUU
4	ROW 2	5555	5555	5555	5555	5555	5555	0000	0000
6	ROW 3	CCCC	CCCC	CCCC	CCCC	CCCC	CCCC	CCCC	CCCC
8	ROW 4	7F7F	7F7F	7F7F	7F7F	7F7F	7F7F	7F7F	0000
10	ROW 5	0000	0000	5H21	5H21	5H21	5H21	5H21	5H21
12	ROW 6	0AFA	0000	0AFA	0AFA	0AFA	0AFA	0000	0AFA

Assembly: Front Panel (Kernel)

Assembly #A01
Board # YB-6488-01
670-5990-00

Configuration: CPU in Test Mode, SIP resistor pack installed. An "*" indicates that a +5V pull-up resistor is required.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
160-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer: Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	AØ9U3050-31	UP	N/A	+5V	0001
Start	AØ9U3050-28	UP	755P	GND	0000
Stop	AØ9U3050-28	UP	755P		
GND	AØ9 TP43				

U2055	SIG
19	2H54

U2025	SIG
1	UUUP
3	5554
5	CCCA
9	7F7H
11	5H20
13	0AFC

U4045	SIG
13	9464

U5025	SIG
8	8670
10	HPP1
11	2H71
12	1A6U

U5055	SIG
2	2H54
3	0001
4	0001
12	2H54
13	1292
14	8670
15	383A

	Location	S/W	SIG	Power	SIG
Clock	AØ9U3050-31	UP	N/A	+5V	755U
Start	AØ9U3050-28	DOWN	0000	GND	0000
Stop	AØ9U3050-28	UP	0000		
GND	AØ9 TP43				

U2055	SIG
1	0258
* 3	1UOH
* 5	7H21
* 7	95P8
* 9	82HP
* 11	331H
* 13	P9FC
* 15	F7H4
* 17	5316

U3055	SIG
* 2	1UOH
* 3	1UOH
* 4	7H21
* 5	7H21
* 6	95P8
* 7	95P8
* 8	82HP
* 9	82HP
* 11	331H
* 12	331H
* 13	P9FC
* 14	P9FC
* 15	F7H4
* 16	F7H4
* 17	5316
* 18	5316

U4055	SIG
1	755U
* 2	1UOH
* 3	5316
* 4	7H21
* 5	F7H4
* 6	95P8
* 7	P9FC
* 8	82HP
* 9	331H
* 11	331H
* 12	82HP
* 13	P9FC
* 14	95P8
* 15	F7H4
* 16	7H21
* 17	5316
* 18	1UOH
19	755U

U4045	SIG
* 4	5316
* 5	F7H4
* 6	P9FC
* 7	331H
* 8	82HP
* 9	95P8
* 10	7H21
* 11	1UOH

@

Assembly: IC ACQ (Kernel)

Assembly #A02
Board # Y-6483-01
670-5985-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	UP	755P
Stop	AØ9J1001-2	UP	755P
GND	AØ9 TP43		

Power	SIG
+5	0001
GND	0000

U2050	SIG
2	0AFC
* 3	0AFC
4	UUUP
* 5	UUUP
6	5H20
* 7	5H20
* 9	7F7H
10	7F7H
* 11	CCCA
12	CCCA

(U2050 Cont.)	
* 14	5554
15	5554

U3010	SIG
* 1	52F9
* 2	52F9
3	52F9
* 4	UPFF
* 5	UPFF
6	UPFF

Assembly: IC ACQ (Kernel) Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1020	SIG
* 3	1U0H
* 5	95P8
* 7	33IH
* 9	F7H4
* 11	5316
* 13	P9FC
* 15	82HP
* 17	7H21

Assembly: Trigger + Timebase (Kernel)

Assembly #A03
Board # Y-6535-01
670-6038-00

Configuration: CPU in Test Mode. SIP resistor pack in TEST. Signatures with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
160-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	UP	755P
Stop	AØ9J1001-2	UP	755P
GND	AØ9 TP43		

Power	SIG
+5	0001
GND	0000

U3040	SIG
* 4	HPP1
* 5	2H71
6	75P1

U3050	SIG
* 1	2H71
* 2	HPP1
* 3	1292

U3060	SIG
* 20	HC88
* 21	52F9
* 22	UPFF
* 23	OAFC

U4050	SIG
* 1	383A
* 2	1292
3	75P1

Assembly: Trigger + Timebase (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1060	SIG
* 2	5316
* 4	F7H4
* 6	331H
* 8	P9FC
* 12	1U0H
* 14	7H21
* 16	95P8
* 18	82HP

Assembly: Front End (Kernel)

Assembly #A04
Board # Y-6487-01
670-5989-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	UP	755P
Stop	AØ9J1001-2	UP	755P
GND	AØ9 TP43		

Power	SIG
+5	0001
GND	0000

U1010	SIG
* 2	52F9
* 4	UPFF
* 6	0AFC
* 8	5H20
* 12	7F7H
* 14	CCCA
* 16	UUUP
* 18	5554

U4030	SIG
* 1	2H71
* 2	HPP1
12	F0C8

U4050	SIG
* 1	5H20
* 2	0AFC
* 3	UPFF
6	F0C8

Assembly: Front End (Kernel) - Continued

Assembly #A04
Board # Y-6487-01
670-5989-00

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1020	SIG
* 3	331H
* 4	P9FC
* 7	5316
* 8	F7H4
* 13	1UOH
* 14	7H21
* 17	95P8
* 18	82HP

U1040	SIG
* 3	F7H4
* 4	5316
* 7	P9FC
* 8	331H
* 13	82HP
* 14	95P9
* 17	7H21
* 18	1UOH

U1050	SIG
* 3	331H
* 4	P9FC
* 7	5316
* 8	F7H4
* 13	1UOH
* 14	7H21
* 17	95P8

(U1050 Cont.)	
* 18	82HP

U2010	SIG
* 2	0258
* 3	82HP
* 4	2225
* 5	95P8
* 6	A8H9
* 7	7H21
* 8	UF9P
* 9	1UOH

U2020	SIG
* 4	7H21
* 5	82HP
* 12	1UOH
* 13	95P8

U3010	SIG
* 3	P9FC
* 5	531C
* 7	82HP
* 9	7H21
* 12	1UOH
* 14	95P8
* 16	331H
* 18	F7H4

Assembly: Front End (Kernel)

Assembly #A04
Board # Y-6487-02
670-5989-01

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	J209-15A	UP	N/A	+5	0001
Start	AØ9J1001-2	UP	755P	GND	0000
Stop	AØ9J1001-2	UP	755P		
GND	AØ9 TP43				

U1010	SIG
* 3	52F9
* 4	UPFF
* 7	0AFC
* 8	5H20
* 13	7F7H
* 14	CCCA
* 17	5554
* 18	UUUP

U2010	SIG
* 8	0001
* 13	1292
* 14	HPP1
* 17	2H71
* 18	HC88

U2055	SIG
* 1	5H20
* 2	0AFC
* 3	UPFF
6	F0C8

U4030	SIG
* 1	2H71
* 2	HPP1
3	0000
4	0001
6	0000
12	F0C8

Assembly: Front End (Kernel) - Continued

Assembly #A04
Board # Y-6487-02
670-5989-01

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1020	SIG
* 3	331H
* 4	P9FC
* 7	5316
* 8	F7H4
* 13	1U0H
* 14	7H21
* 17	95P8
* 18	82HP

U1040	SIG
* 3	F7H4
* 4	5316
* 7	P9FC
* 8	331H
* 13	82HP
* 14	95P9
* 17	7H21
* 18	1U0H

U1050	SIG
* 3	331H
* 4	P9FC
* 7	5316
* 8	F7H4
* 13	1U0H

(U1050 Cont.)	
* 14	7H21
* 17	95P8
* 18	82HP

U2020	SIG
* 4	7H21
* 5	82HP
* 12	1U0H
* 13	95P8

U3010	SIG
* 3	P9FC
* 5	531C
* 7	82HP
* 9	7H21
* 12	1U0H
* 14	95P8
* 16	331H
* 18	F7H4

U6010	SIG
* 3	82HP
* 5	95P8
* 7	7H21
* 9	1U0H

Assembly: Word Recognizer (Kernel)

Assembly #A05
Board # Y-6486-01
670-5988-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	J209-15A	UP	N/A	+5	0001
Start	AØ9J1001-2	UP	755P	GND	0000
Stop	AØ9J1001-2	UP	755P		
GND	AØ9 TP43				

U1040	SIG
* 2	UUUP
* 4	5H20
* 6	CCCA
* 8	UPFF
* 12	5554
* 14	7F7H
* 16	0AFC
* 18	52F9

U2040	SIG
* 2	CCCA
* 4	5H20
* 6	UUUP
* 8	UPFF

(U2040 Cont.)	
* 12	5554
* 14	7F7H
* 16	52F9
* 18	0AFC

U3040	SIG
* 2	CCCA
* 4	5H20
* 6	UUUP
* 8	UPFF
* 12	5554
* 14	7F7H
* 16	52F9
* 18	0AFC

U4040	SIG
* 2	5554
* 4	CCCA
* 6	7F7H
* 8	5H20
* 12	52F9
* 14	UPFF
* 16	0AFC
* 18	UUUP

Assembly: Word Recognizer (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U4010	SIG
* 9	5316
* 11	F7H4
* 13	P9FC
* 15	331H

U6030	SIG
* 9	82HP
* 11	95P8
* 13	7H21
* 15	1U0H

U6020	SIG
* 9	82HP
* 11	95P8
* 13	7H21
* 15	1U0H

U8010	SIG
* 9	5316
* 11	F7H4
* 13	P9FC
* 15	331H

Assembly: Expansion Option (Kernel)

Assembly #A06
Board # Y-6485-01
670-5987-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	J209-15A	UP	N/A	+5	0001
Start	AØ9J1001-2	UP	755P	GND	0000
Stop	AØ9J1001-2	UP	755P		
GND	AØ9 TP43				

U1030	SIG
* 2	UUUP
* 3	HPP1
* 14	HC88

U1050	SIG
* 12	1292

U3020	SIG
* 2	UUUP
* 4	5554
* 6	CCCA

(U3020 Cont.)	
* 8	7F7H
* 12	5H20
* 14	0AFC
* 16	UPFF
* 18	52F9

U3050	SIG
* 3	CCCA
* 4	7F7H
* 5	5H20
* 6	0AFC

U4020	SIG
* 2	UUUP
* 4	5554
* 6	CCCA
* 8	7F7H
* 12	5H20
* 14	0AFC
* 16	UPFF
* 18	52F9

U4050	SIG
* 3	UPFF
* 4	52F9
* 5	HC88
* 6	2H71

Assembly: Expansion Option (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U2030	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

U2040	SIG
* 10	331H
* 12	P9FC
* 14	F7H4
* 16	5316

U2040	SIG
* 10	331H
* 12	P9FC
* 14	F7H4
* 16	5316

U4040	SIG
* 9	5316
* 11	F7H4
* 13	P9FC
* 15	331H

U3030	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

U5040	SIG
* 9	5316
* 11	F7H4
* 13	P9FC
* 15	331H

Assembly: ACQ Memory (Kernel)

Assembly #A07
Board # Y-6493-01
670-5995-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	UP	755P
Stop	AØ9J1001-2	UP	755P
GND	AØ9 TP43		

Power	SIG
+5	0001
GND	0000

U2010	SIG
* 1	UUUP
* 2	5554
* 3	1292
* 5	HPP1

U3040	SIG
* 3	CCCA
* 4	7F7H
* 5	5H20
* 6	0AFC

U1025	SIG
* 6	HC88
* 11	HC88
13	HC89

U4040	SIG
* 3	UPFF
* 4	52F9
* 5	HC88
* 6	2H71

Assembly: ACQ Memory (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1040	SIG
* 3	1U0H
* 4	7H21
* 5	95P8
* 6	82HP

U2040	SIG
* 3	331H
* 4	P9FC
* 5	F7H4
* 6	5316

U2020	SIG
* 4	1U0H
* 5	7H21
* 12	95P8
* 13	82HP

U3020	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

U2030	SIG
* 3	331H
* 5	P9FC
* 7	F7H4
* 9	5316
* 11	1U0H
* 13	7H21
* 15	95P8
* 17	82HP

U3030	SIG
* 3	331H
* 5	P9FC
* 7	F7H4
* 9	5316
* 11	1U0H
* 13	7H21
* 15	95P8
* 17	82HP

U4030	SIG
* 10	331H
* 12	P9FC
* 14	F7H4
* 16	5316

U5020	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

U5030	SIG
* 10	331H
* 12	P9FC
* 14	F7H4
* 16	5316

U6020	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

U6030	SIG
* 10	331H
* 12	P9FC
* 14	F7H4
* 16	5316

U7020	SIG
* 10	1U0H
* 12	7H21
* 14	95P8
* 16	82HP

Assembly: State Machine (Kernel)

Assembly #A08
Board # Y-6484-02
670-5986-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG	Power	SIG
Clock	J209-15A	UP	N/A	+5	0001
Start	AØ9J1001-2	UP	755P	GND	0000
Stop	AØ9J1001-2	UP	755P		
GND	AØ9 TP43				

U1040	SIG
* 3	UUUP
* 6	5554
* 10	CCCA

U4040	SIG
* 3	UUUP
* 6	5554
* 10	CCCA

U4060	SIG
* 2	7F7H
* 4	5554
* 6	UUUP
* 8	52F9
* 12	UPFF

(U4060 Cont.)	
* 14	0AFC
* 16	5H20
* 18	CCCA

U6050	SIG
* 1	HC88
* 2	2H71
* 3	HPP1
* 4	1292

U7050	SIG
* 1	HC88
* 2	2H71
* 3	HPP1
* 4	1292

Assembly: State Machine (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U2050	SIG
* 2	1U0H
* 3	7H21
* 4	95P8
* 5	82HP
* 6	331H
* 7	P9FC
* 8	F7H4
* 9	5316

Assembly: Display (Kernel)

Assembly #A10
Board # Y-6481-02
670-5983-00

Configuration: CPU in Test Mode. SIP resistor pack installed. Signatures marked with an "*" require a +5V pull-up.

Software:

160-0361-00 Diagnostic ROM
160-0358-00 Firmware ROM
160-0359-00 Firmware ROM
160-0360-00 Firmware ROM
106-0818-00 Firmware ROM
160-0819-00 Firmware ROM

Analyzer:
Sony Tek 308.

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	UP	755P
Stop	AØ9J1001-2	UP	755P
GND	AØ9 TP43		

Power	SIG
+5	0001
GND	0000

U2050	SIG
* 2	7F7H
* 5	CCCA
* 11	5554
* 14	UUUP

U3050	SIG
* 2	52F9
* 5	UPFF
* 11	0AFC
* 14	5H20

U4050	SIG
* 11	2H71
* 14	HC88

Assembly: Display (Kernel) - Continued

	Location	S/W	SIG
Clock	J209-15A	UP	N/A
Start	AØ9J1001-2	DOWN	0000
Stop	AØ9J1001-2	UP	0000
GND	AØ9 TP43		

Power	SIG
+5	755U
GND	0000

U1050	SIG
* 2	1UOH
* 3	7H21
* 4	95P8
* 5	82HP
* 6	331H
* 7	P9FC
* 8	F7H4
* 9	5316

TROUBLESHOOTING AND SIGNATURE TREES LIST

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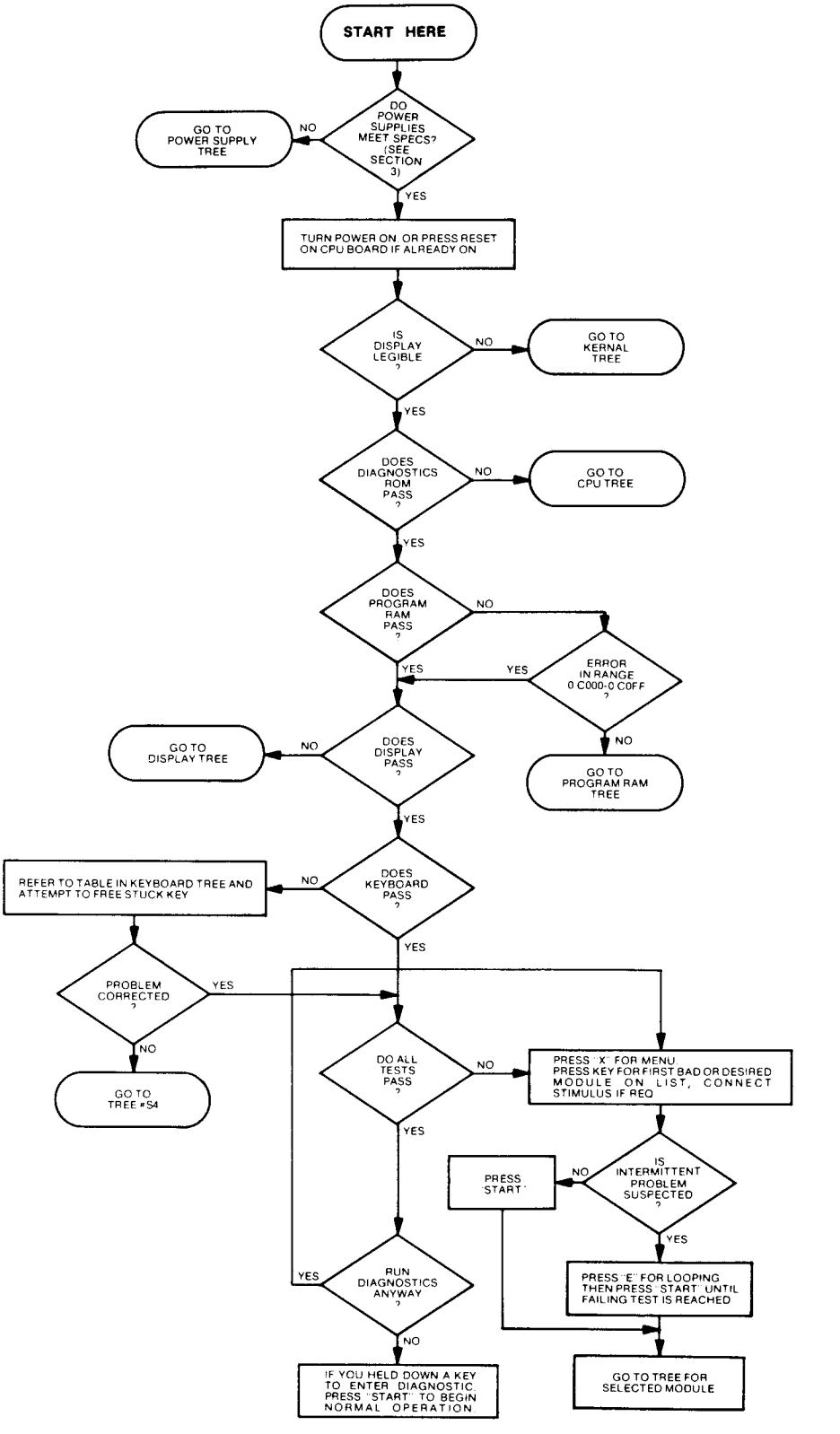
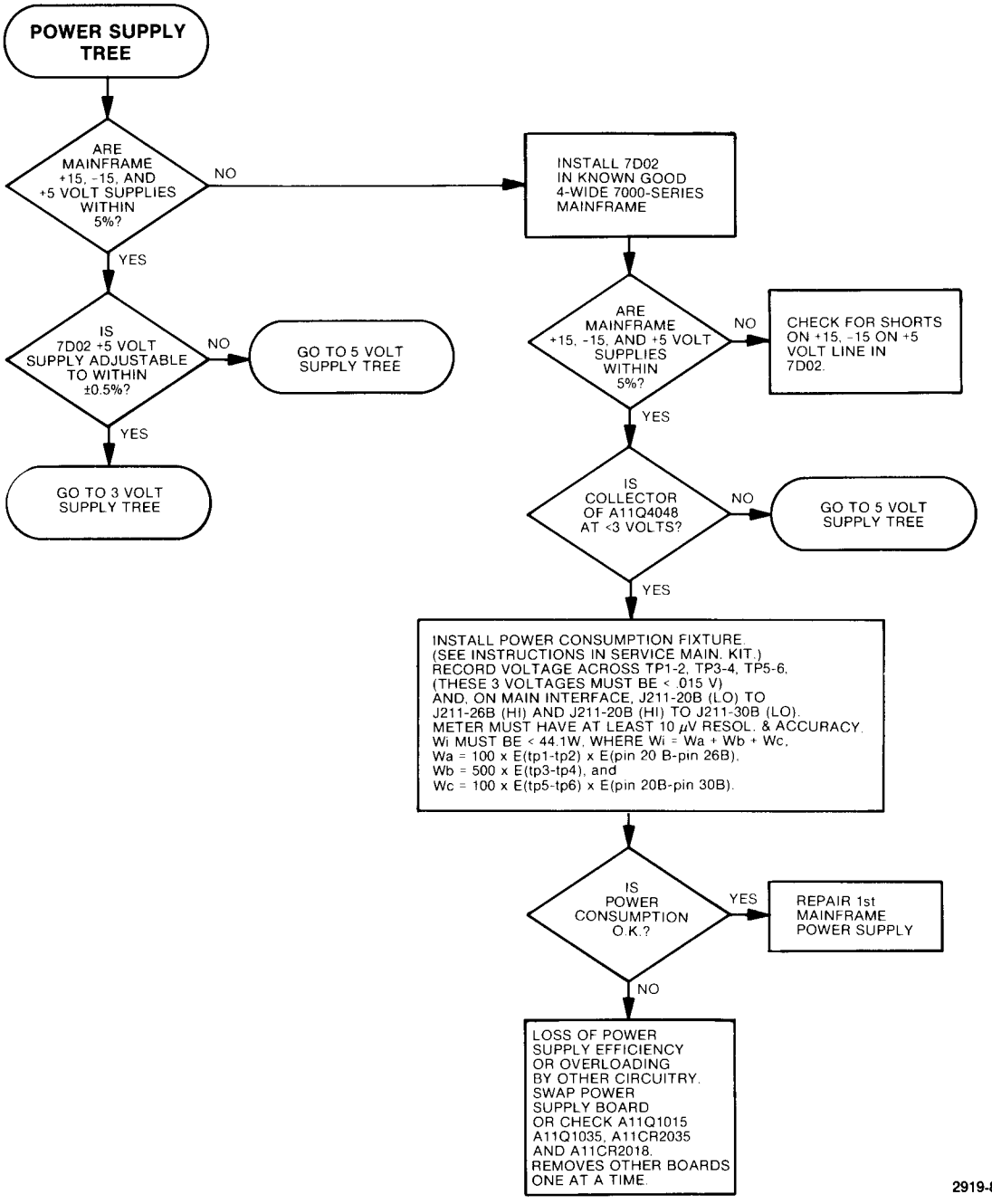
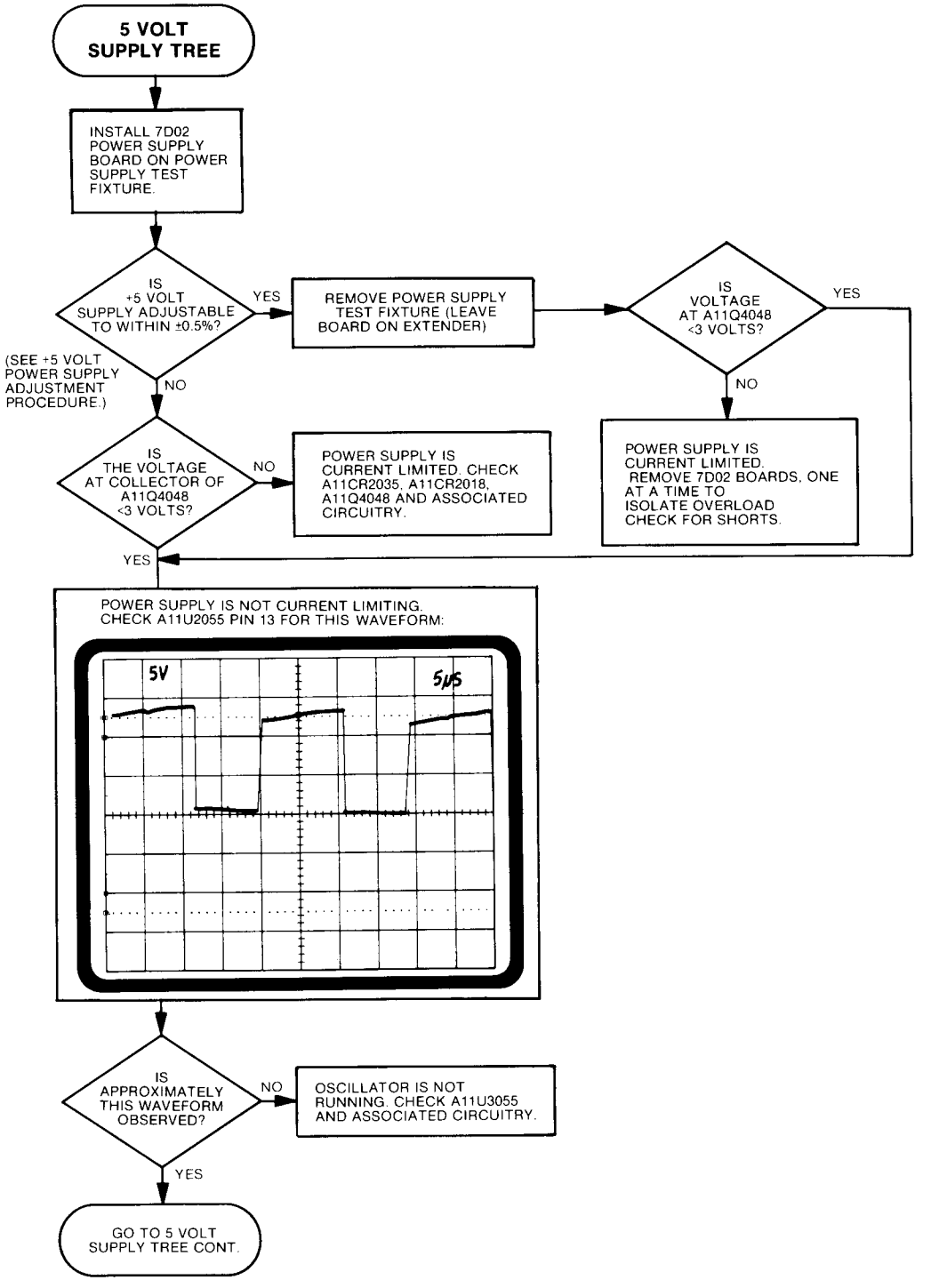
TROUBLESHOOTING TREES

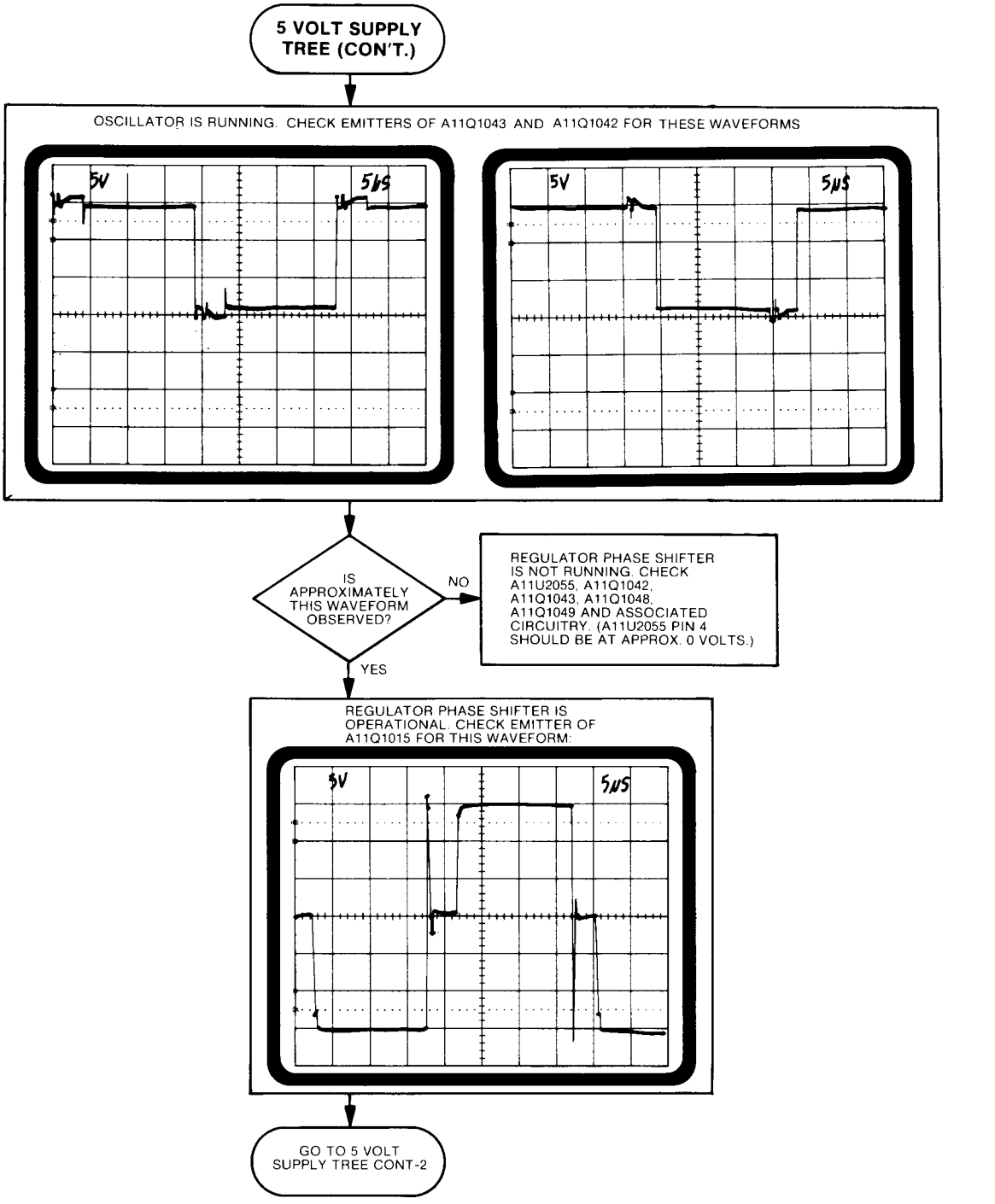


2919-86

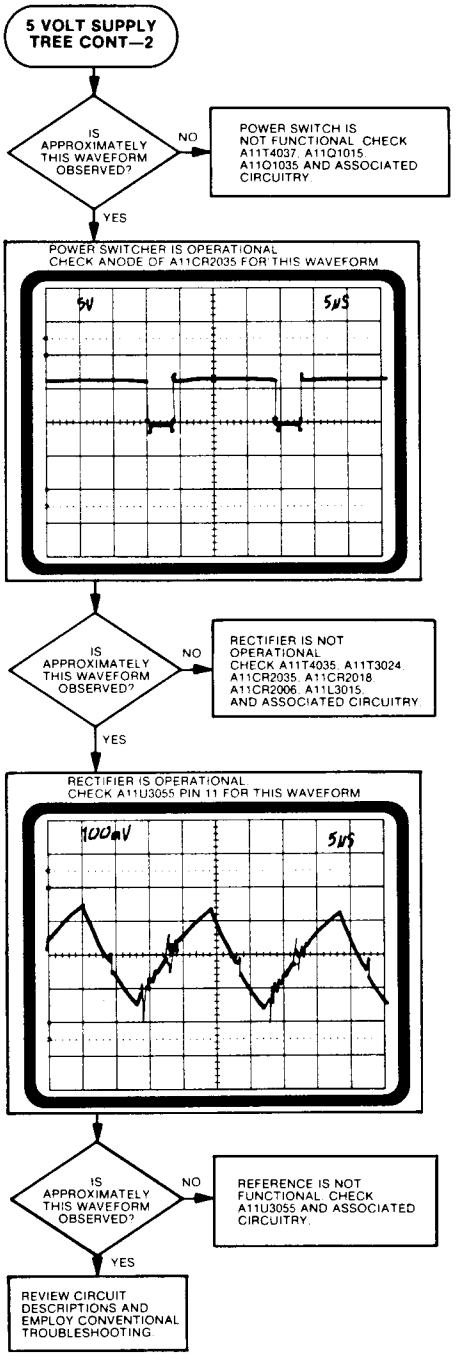

POWER SUPPLY TREE
ARE MAINFRAME +15, -15, AND +5 VOLT SUPPLIES WITHIN 5%?
NO
YES
INSTALL 7D02 IN KNOWN GOOD 4-WIDE 7000-SERIES MAINFRAME
IS 7D02 +5 VOLT SUPPLY ADJUSTABLE TO WITHIN ±0.5%?
NO
GO TO 5 VOLT SUPPLY TREE
YES
GO TO 3 VOLT SUPPLY TREE
ARE MAINFRAME +15, -15, AND +5 VOLT SUPPLIES WITHIN 5%?
NO
CHECK FOR SHORTS ON +15, -15 ON +5 VOLT LINE IN 7D02.
YES
IS COLLECTOR OF A11Q4048 AT <3 VOLTS?
NO
GO TO 5 VOLT SUPPLY TREE
YES
INSTALL POWER CONSUMPTION FIXTURE. (SEE INSTRUCTIONS IN SERVICE MAIN. KIT.) RECORD VOLTAGE ACROSS TP1-2, TP3-4, TP5-6, (THESE 3 VOLTAGES MUST BE < .015 V) AND, ON MAIN INTERFACE, J211-20B (LO) TO J211-26B (HI) AND J211-20B (HI) TO J211-30B (LO). METER MUST HAVE AT LEAST 10 μV RESOL. & ACCURACY. Wi MUST BE < 44.1W, WHERE Wi = Wa + Wb + Wc, Wa = 100 x E(tp1-tp2) x E(pin 20 B-pin 26B), Wb = 500 x E(tp3-tp4), and Wc = 100 x E(tp5-tp6) x E(pin 20B-pin 30B).
IS POWER CONSUMPTION O.K.?
YES
REPAIR 1st MAINFRAME POWER SUPPLY
NO
LOSS OF POWER SUPPLY EFFICIENCY OR OVERLOADING BY OTHER CIRCUITRY. SWAP POWER SUPPLY BOARD OR CHECK A11Q1015 A11Q1035, A11CR2035 AND A11CR2018. REMOVES OTHER BOARDS ONE AT A TIME.
2919-87


5 VOLT SUPPLY TREE
INSTALL 7D02 POWER SUPPLY BOARD ON POWER SUPPLY TEST FIXTURE.
IS +5 VOLT SUPPLY ADJUSTABLE TO WITHIN ±0.5%?
YES
REMOVE POWER SUPPLY TEST FIXTURE (LEAVE BOARD ON EXTENDER)
IS VOLTAGE AT A11Q4048 <3 VOLTS?
YES
(SEE +5 VOLT POWER SUPPLY ADJUSTMENT PROCEDURE.)
NO
NO
IS THE VOLTAGE AT COLLECTOR OF A11Q4048 <3 VOLTS?
NO
POWER SUPPLY IS CURRENT LIMITED. CHECK A11CR2035, A11CR2018, A11Q4048 AND ASSOCIATED CIRCUITRY.
POWER SUPPLY IS CURRENT LIMITED. REMOVE 7D02 BOARDS, ONE AT A TIME TO ISOLATE OVERLOAD CHECK FOR SHORTS.
YES
POWER SUPPLY IS NOT CURRENT LIMITING. CHECK A11U2055 PIN 13 FOR THIS WAVEFORM:
5V
5µS
IS APPROXIMATELY THIS WAVEFORM OBSERVED?
NO
OSCILLATOR IS NOT RUNNING. CHECK A11U3055 AND ASSOCIATED CIRCUITRY.
YES
GO TO 5 VOLT SUPPLY TREE CONT.

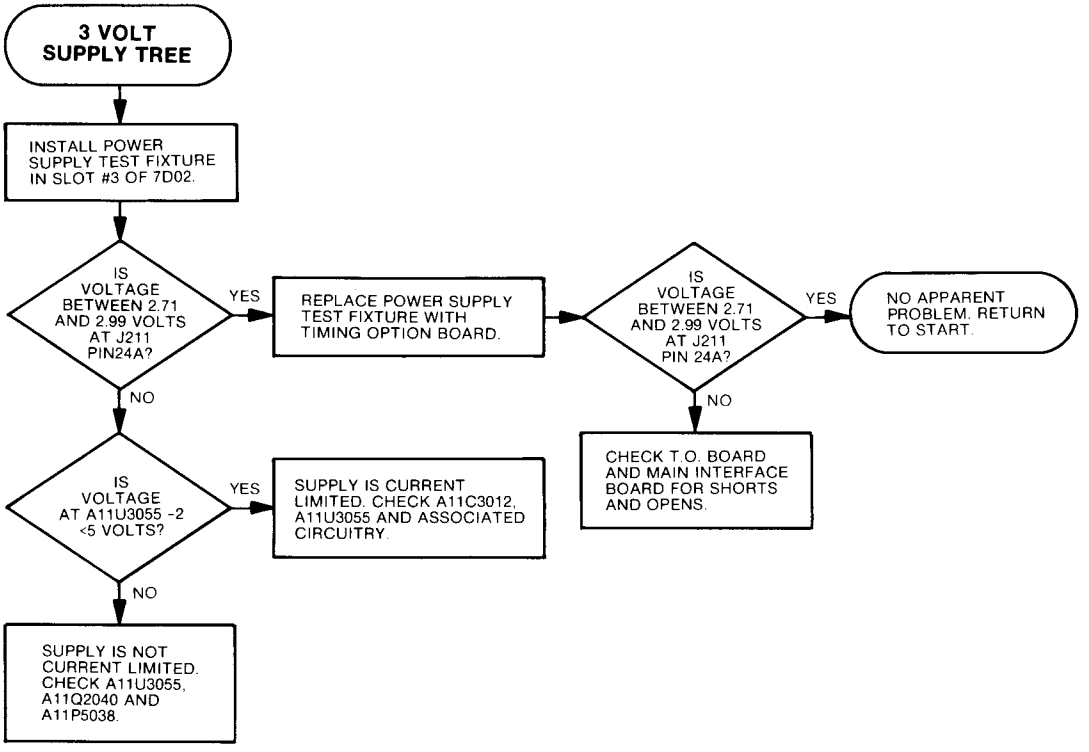
2919-88


5 VOLT SUPPLY TREE (CON'T.)
OSCILLATOR IS RUNNING. CHECK EMITTERS OF A11Q1043 AND A11Q1042 FOR THESE WAVEFORMS
5V
5µS
5V
5µS
IS APPROXIMATELY THIS WAVEFORM OBSERVED?
NO
REGULATOR PHASE SHIFTER IS NOT RUNNING. CHECK A11U2055, A11Q1042, A11Q1043, A11Q1048, A11Q1049 AND ASSOCIATED CIRCUITRY. (A11U2055 PIN 4 SHOULD BE AT APPROX. 0 VOLTS.)
YES
REGULATOR PHASE SHIFTER IS OPERATIONAL. CHECK EMITTER OF A11Q1015 FOR THIS WAVEFORM:
5V
5µS
GO TO 5 VOLT SUPPLY TREE CONT-2

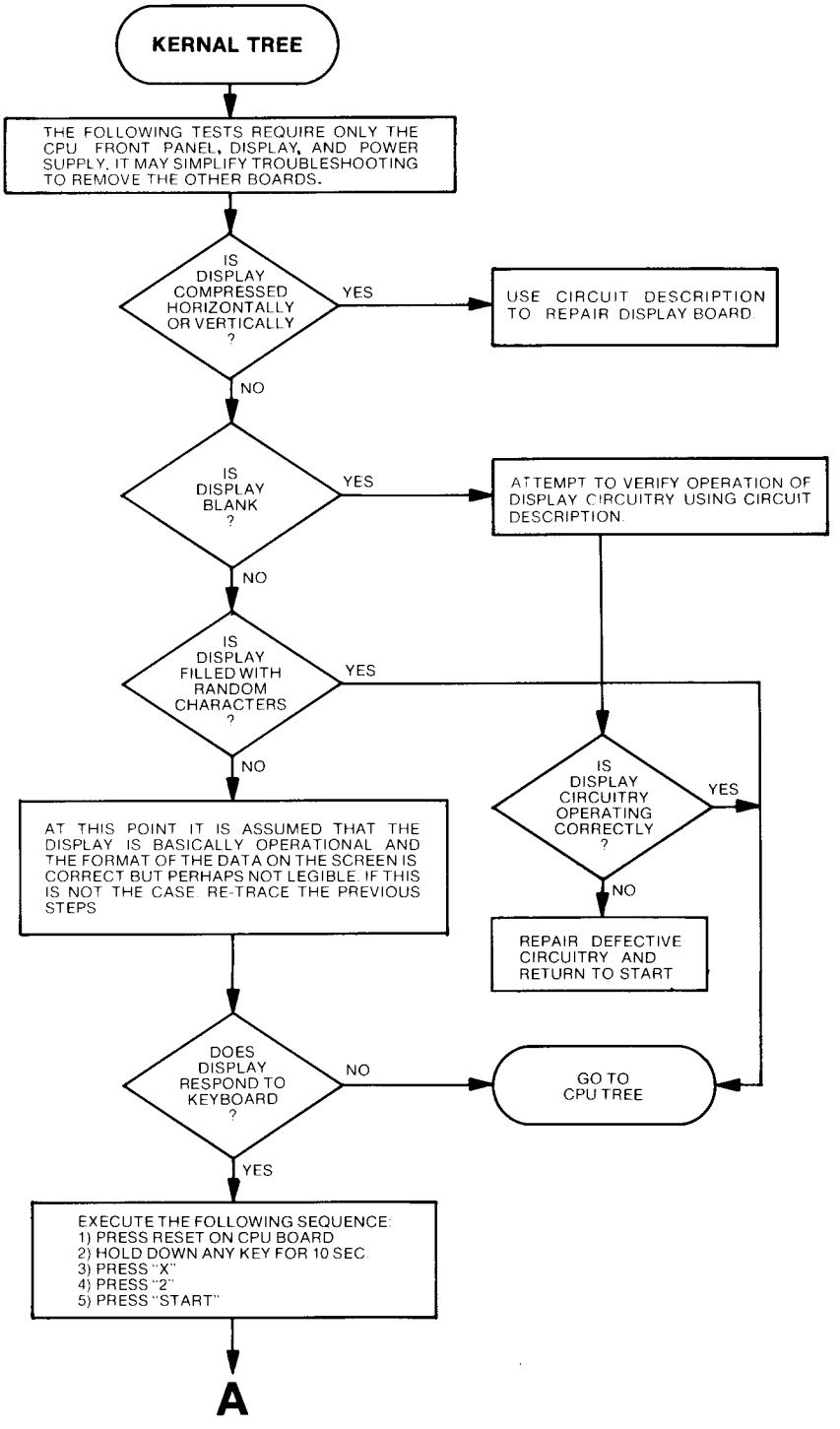
2919-89


5 VOLT SUPPLY TREE CONT—2
IS APPROXIMATELY THIS WAVEFORM OBSERVED?
NO
POWER SWITCH IS NOT FUNCTIONAL. CHECK A11T4037, A11Q1015, A11Q1035, AND ASSOCIATED CIRCUITRY.
YES
POWER SWITCHER IS OPERATIONAL. CHECK ANODE OF A11CR2035 FOR THIS WAVEFORM
5V
5µS
IS APPROXIMATELY THIS WAVEFORM OBSERVED?
NO
RECTIFIER IS NOT OPERATIONAL. CHECK A11T4035, A11T3024, A11CR2035, A11CR2018, A11CR2006, A11L3015, AND ASSOCIATED CIRCUITRY.
YES
RECTIFIER IS OPERATIONAL. CHECK A11U3055 PIN 11 FOR THIS WAVEFORM
100mV
5µS
IS APPROXIMATELY THIS WAVEFORM OBSERVED?
NO
REFERENCE IS NOT FUNCTIONAL. CHECK A11U3055 AND ASSOCIATED CIRCUITRY.
YES
REVIEW CIRCUIT DESCRIPTIONS AND EMPLOY CONVENTIONAL TROUBLESHOOTING.

2919-90

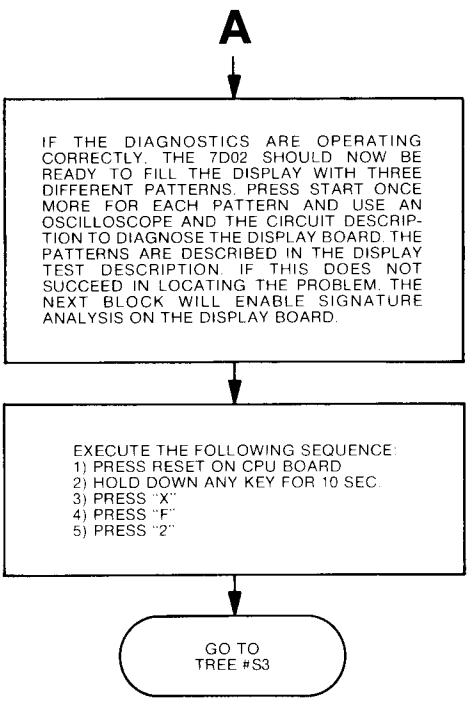

3 VOLT SUPPLY TREE
INSTALL POWER SUPPLY TEST FIXTURE IN SLOT #3 OF 7D02.
IS VOLTAGE BETWEEN 2.71 AND 2.99 VOLTS AT J211 PIN24A?
YES
REPLACE POWER SUPPLY TEST FIXTURE WITH TIMING OPTION BOARD.
IS VOLTAGE BETWEEN 2.71 AND 2.99 VOLTS AT J211 PIN 24A?
YES
NO APPARENT PROBLEM. RETURN TO START.
NO
CHECK T.O. BOARD AND MAIN INTERFACE BOARD FOR SHORTS AND OPENS.
IS VOLTAGE AT A11U3055 -2 <5 VOLTS?
YES
SUPPLY IS CURRENT LIMITED. CHECK A11C3012, A11U3055 AND ASSOCIATED CIRCUITRY.
NO
SUPPLY IS NOT CURRENT LIMITED. CHECK A11U3055, A11Q2040 AND A11P5038.

2919-91


KERNAL TREE
THE FOLLOWING TESTS REQUIRE ONLY THE CPU FRONT PANEL, DISPLAY, AND POWER SUPPLY. IT MAY SIMPLIFY TROUBLESHOOTING TO REMOVE THE OTHER BOARDS.
IS DISPLAY COMPRESSED HORIZONTALLY OR VERTICALLY ?
YES
USE CIRCUIT DESCRIPTION TO REPAIR DISPLAY BOARD.
NO
IS DISPLAY BLANK ?
YES
ATTEMPT TO VERIFY OPERATION OF DISPLAY CIRCUITRY USING CIRCUIT DESCRIPTION.
NO
IS DISPLAY FILLED WITH RANDOM CHARACTERS ?
YES
NO
IS DISPLAY CIRCUITRY OPERATING CORRECTLY ?
YES
NO
REPAIR DEFECTIVE CIRCUITRY AND RETURN TO START
AT THIS POINT IT IS ASSUMED THAT THE DISPLAY IS BASICALLY OPERATIONAL AND THE FORMAT OF THE DATA ON THE SCREEN IS CORRECT BUT PERHAPS NOT LEGIBLE. IF THIS IS NOT THE CASE, RE-TRACE THE PREVIOUS STEPS
DOES DISPLAY RESPOND TO KEYBOARD ?
NO
GO TO CPU TREE
YES
EXECUTE THE FOLLOWING SEQUENCE:
1) PRESS RESET ON CPU BOARD
2) HOLD DOWN ANY KEY FOR 10 SEC.
3) PRESS "X"
4) PRESS "2"
5) PRESS "START"
A

2919-92

KERNAL TREE (CON'T.)

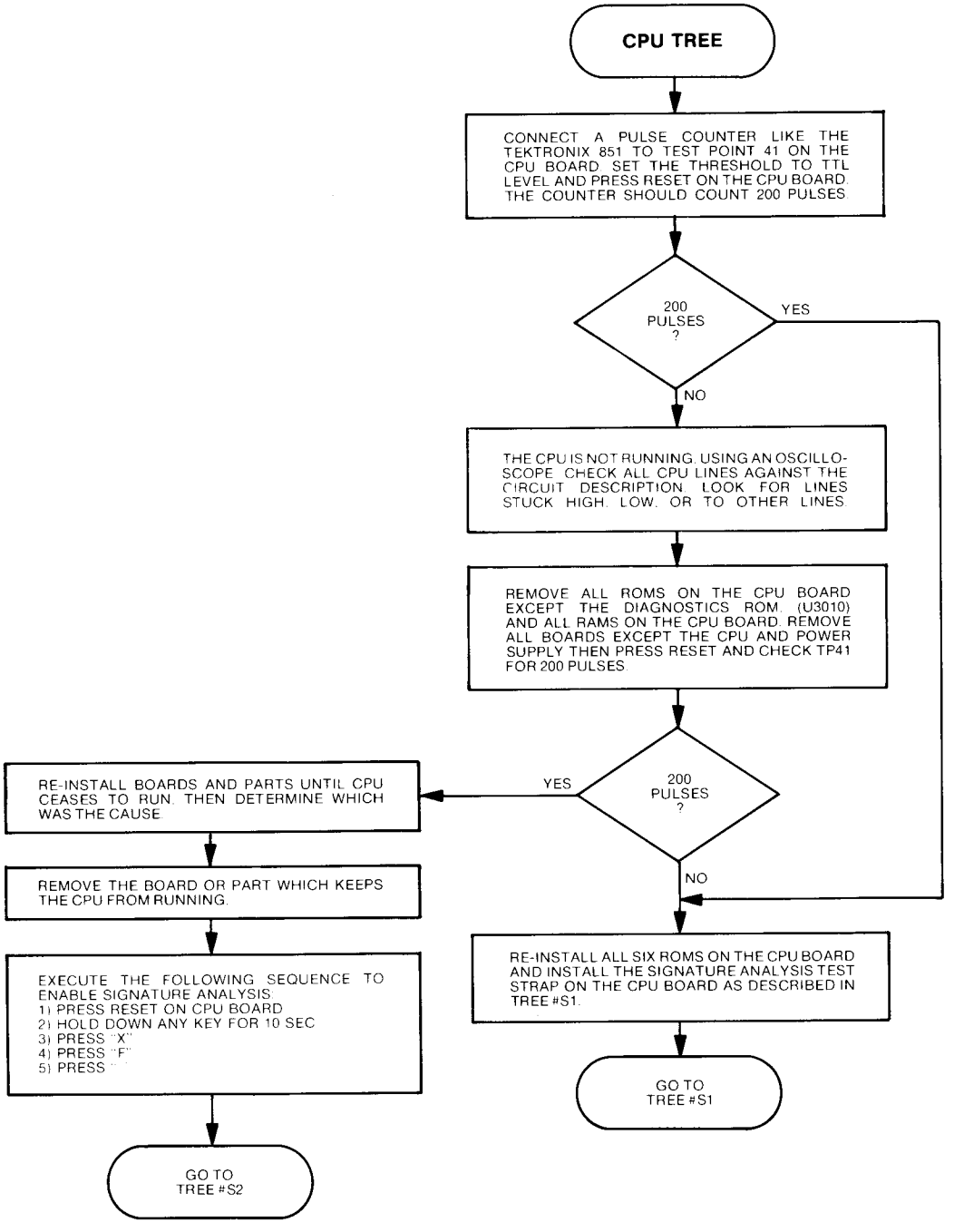


NOTE:

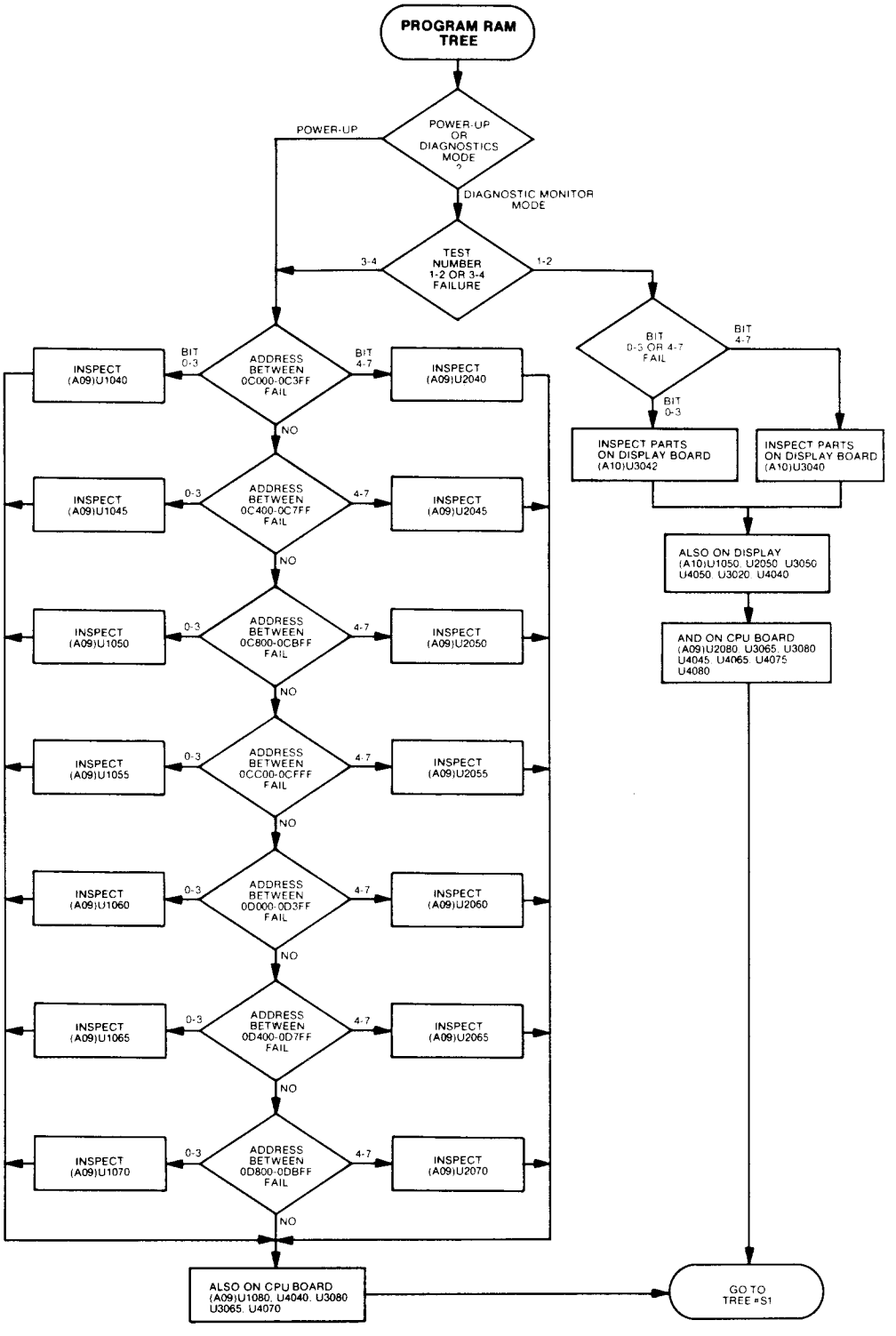
IF THE SCREEN WAS LEGIBLE ENOUGH TO INDICATE A FAILURE OF EITHER OF THE FIRST TWO DISPLAY TESTS, USE THE BOTTOM HALF OF THE DISPLAY TREE AS A TROUBLESHOOTING GUIDE.

2919-93

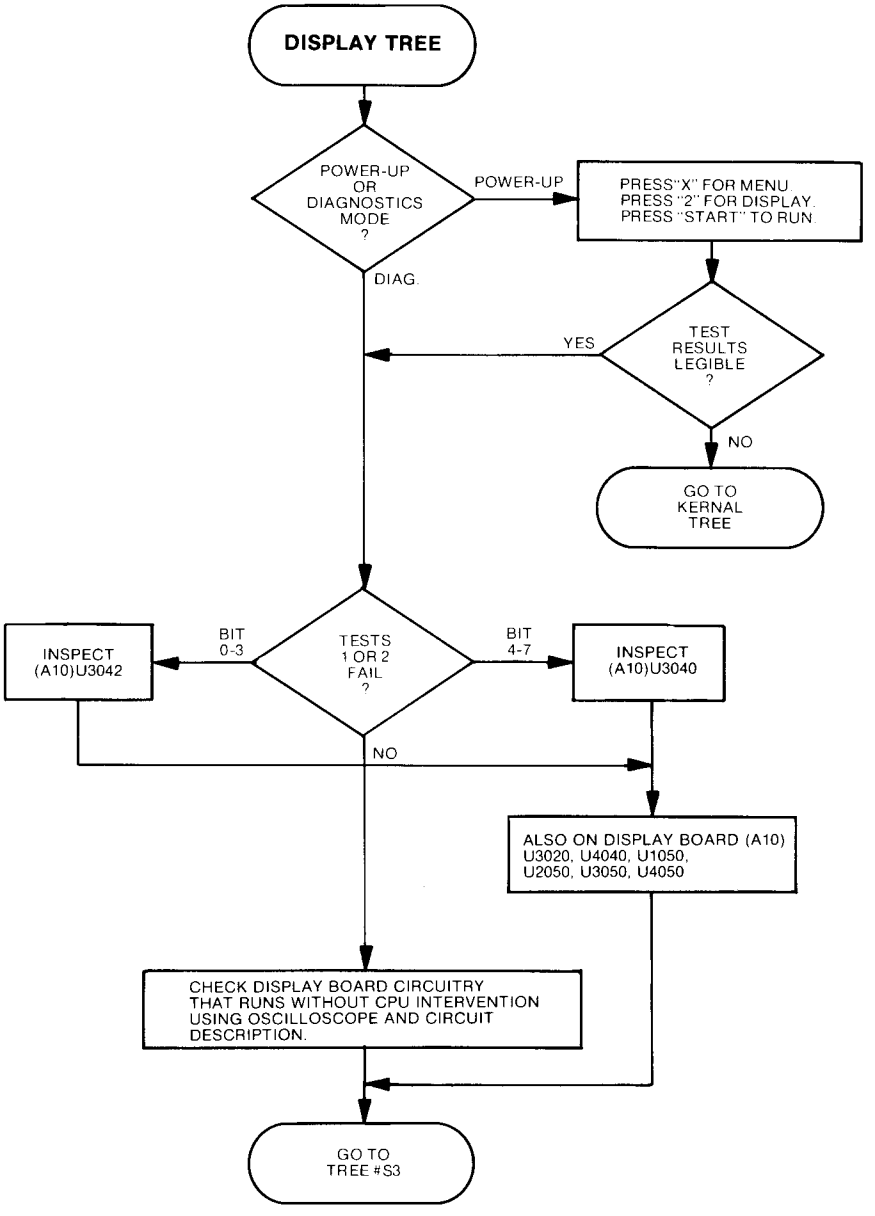
@


CPU TREE
CONNECT A PULSE COUNTER LIKE THE TEKTRONIX 851 TO TEST POINT 41 ON THE CPU BOARD. SET THE THRESHOLD TO TTL LEVEL AND PRESS RESET ON THE CPU BOARD. THE COUNTER SHOULD COUNT 200 PULSES.
200 PULSES ?
YES
NO
THE CPU IS NOT RUNNING. USING AN OSCILLOSCOPE CHECK ALL CPU LINES AGAINST THE CIRCUIT DESCRIPTION. LOOK FOR LINES STUCK HIGH, LOW, OR TO OTHER LINES.
REMOVE ALL ROMS ON THE CPU BOARD EXCEPT THE DIAGNOSTICS ROM. (U3010) AND ALL RAMS ON THE CPU BOARD. REMOVE ALL BOARDS EXCEPT THE CPU AND POWER SUPPLY THEN PRESS RESET AND CHECK TP41 FOR 200 PULSES.
200 PULSES ?
YES
NO
RE-INSTALL BOARDS AND PARTS UNTIL CPU CEASES TO RUN. THEN DETERMINE WHICH WAS THE CAUSE.
REMOVE THE BOARD OR PART WHICH KEEPS THE CPU FROM RUNNING.
EXECUTE THE FOLLOWING SEQUENCE TO ENABLE SIGNATURE ANALYSIS:
1) PRESS RESET ON CPU BOARD
2) HOLD DOWN ANY KEY FOR 10 SEC
3) PRESS "X"
4) PRESS "F"
5) PRESS "
GO TO TREE #S2
RE-INSTALL ALL SIX ROMS ON THE CPU BOARD AND INSTALL THE SIGNATURE ANALYSIS TEST STRAP ON THE CPU BOARD AS DESCRIBED IN TREE #S1.
GO TO TREE #S1

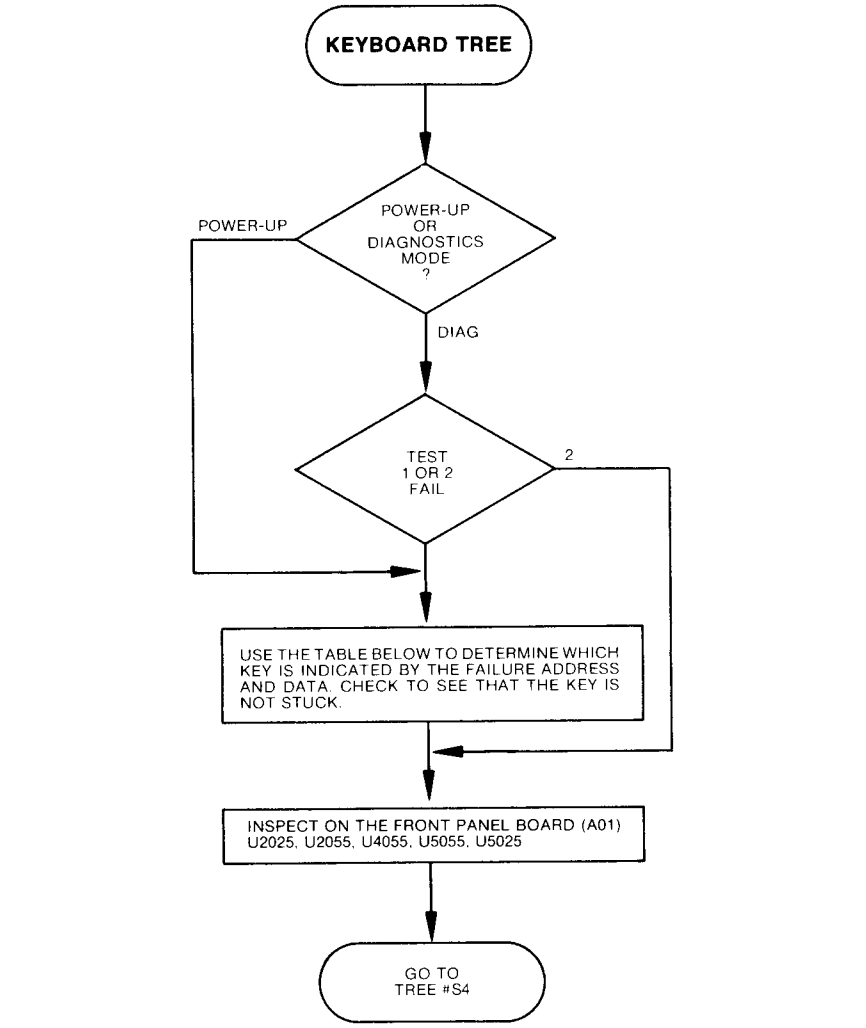
2919-94


PROGRAM RAM TREE
POWER-UP OR DIAGNOSTICS MODE ?
POWER-UP
DIAGNOSTIC MONITOR MODE
TEST NUMBER 1-2 OR 3-4 FAILURE
3-4
1-2
BIT 0-3 OR 4-7 FAIL
BIT 4-7
BIT 0-3
INSPECT PARTS ON DISPLAY BOARD (A10)U3042
INSPECT PARTS ON DISPLAY BOARD (A10)U3040
ALSO ON DISPLAY (A10)U1050, U2050, U3050, U4050, U3020, U4040
AND ON CPU BOARD (A09)U2080, U3065, U3080, U4045, U4065, U4075, U4080
ADDRESS BETWEEN 0C000-0C3FF FAIL
INSPECT (A09)U1040
INSPECT (A09)U2040
ADDRESS BETWEEN 0C400-0C7FF FAIL
INSPECT (A09)U1045
INSPECT (A09)U2045
ADDRESS BETWEEN 0C800-0CBFF FAIL
INSPECT (A09)U1050
INSPECT (A09)U2050
ADDRESS BETWEEN 0CC00-0CFFF FAIL
INSPECT (A09)U1055
INSPECT (A09)U2055
ADDRESS BETWEEN 0D000-0D3FF FAIL
INSPECT (A09)U1060
INSPECT (A09)U2060
ADDRESS BETWEEN 0D400-0D7FF FAIL
INSPECT (A09)U1065
INSPECT (A09)U2065
ADDRESS BETWEEN 0D800-0DBFF FAIL
INSPECT (A09)U1070
INSPECT (A09)U2070
BIT 0-3
BIT 4-7
NO
ALSO ON CPU BOARD (A09)U1080, U4040, U3080, U3065, U4070
GO TO TREE #S1

2919-95


DISPLAY TREE
POWER-UP OR DIAGNOSTICS MODE ?
POWER-UP
PRESS "X" FOR MENU.
PRESS "2" FOR DISPLAY.
PRESS "START" TO RUN.
DIAG.
YES
TEST RESULTS LEGIBLE ?
NO
GO TO KERNAL TREE
BIT 0-3
TESTS 1 OR 2 FAIL ?
BIT 4-7
INSPECT (A10)U3042
INSPECT (A10)U3040
NO
ALSO ON DISPLAY BOARD (A10) U3020, U4040, U1050, U2050, U3050, U4050
CHECK DISPLAY BOARD CIRCUITRY THAT RUNS WITHOUT CPU INTERVENTION USING OSCILLOSCOPE AND CIRCUIT DESCRIPTION.
GO TO TREE #S3

2919-96



F601-0	F601-1	F602-2	F601-3	F601-4	F601-5	F601-6	F601-7
F602-0	F602-1	F602-2	F602-3	F602-4	F602-5		
F604-0	F604-1	F604-2	F604-3	F604-4	F604-5	F604-6	F604-7
F608-0	F608-1	F608-2	F608-3	F608-4	F608-5	F608-6	
		F610-2	F610-3	F610-4	F610-5	F610-6	F610-7
F620-0		F620-2	F620-3	F620-4	F620-5	F620-7	

THE ABOVE MAP SHOWS WHICH KEY IS INDICATED BY THE FAIL ADDRESS AND DATA.

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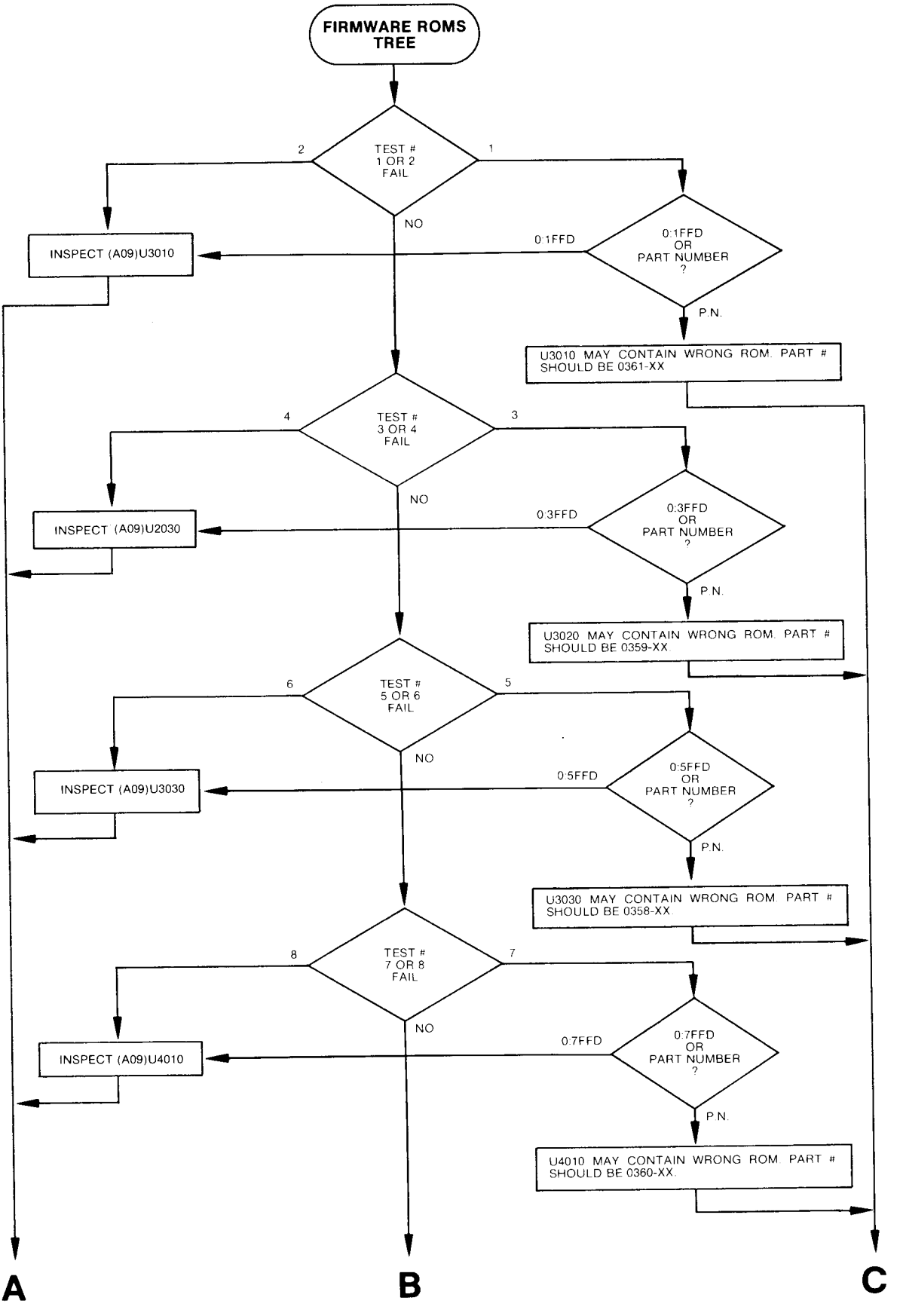
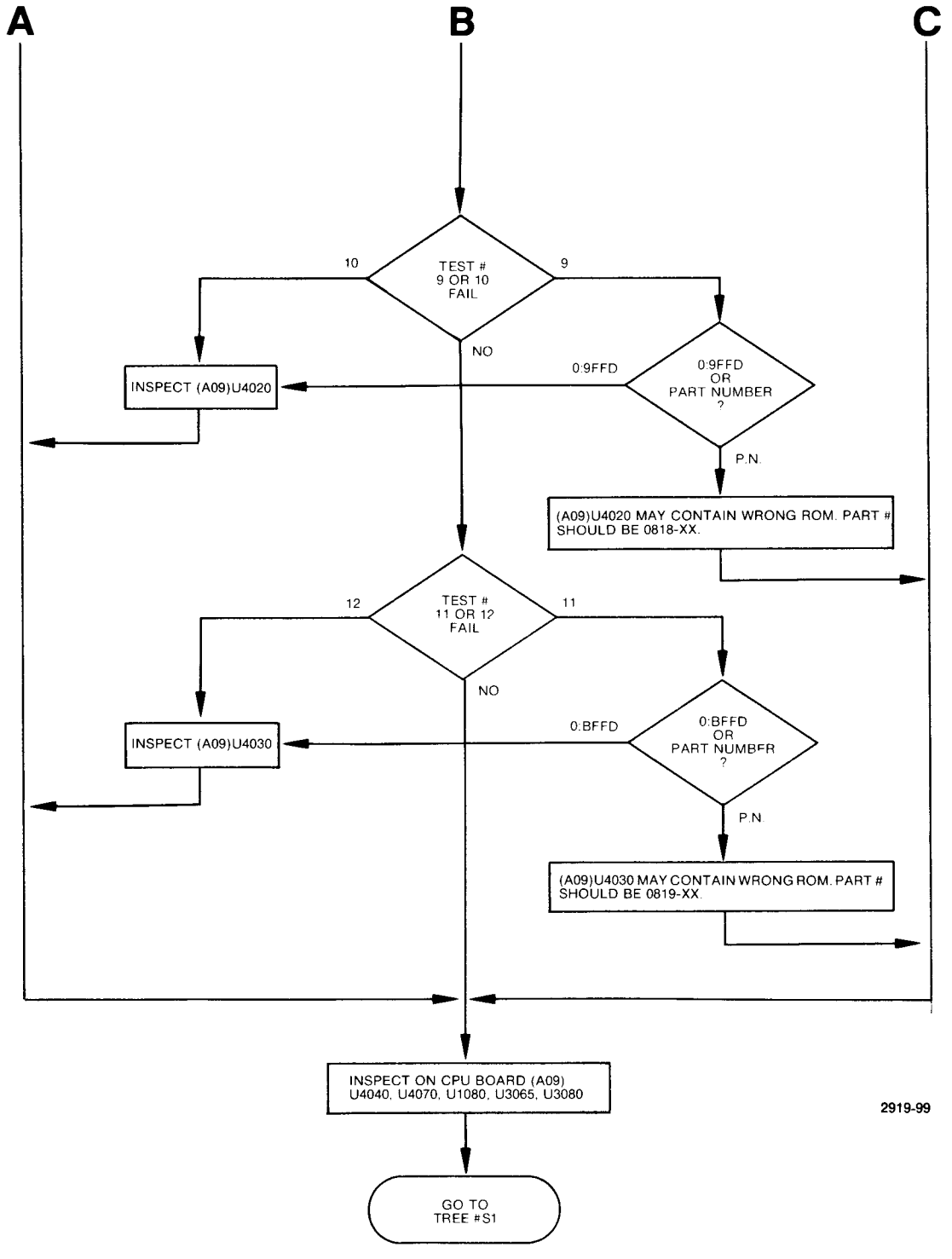
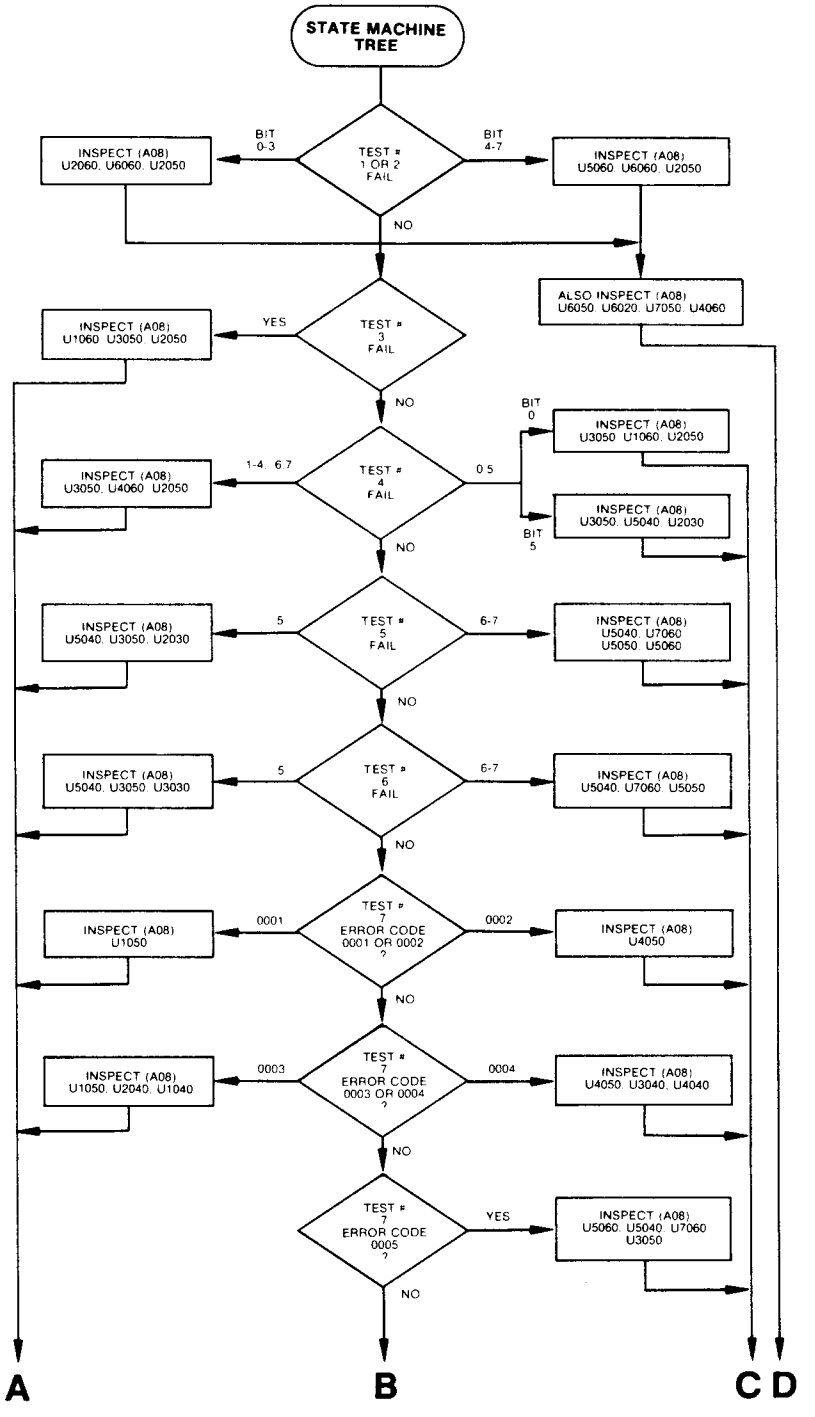

FIRMWARE ROMS TREE
TEST # 1 OR 2 FAIL
2
1
NO
INSPECT (A09)U3010
0:1FFD
0:1FFD OR PART NUMBER ?
P.N.
U3010 MAY CONTAIN WRONG ROM. PART # SHOULD BE 0361-XX
TEST # 3 OR 4 FAIL
4
3
NO
INSPECT (A09)U2030
0:3FFD
0:3FFD OR PART NUMBER ?
P.N.
U3020 MAY CONTAIN WRONG ROM. PART # SHOULD BE 0359-XX
TEST # 5 OR 6 FAIL
6
5
NO
INSPECT (A09)U3030
0:5FFD
0:5FFD OR PART NUMBER ?
P.N.
U3030 MAY CONTAIN WRONG ROM. PART # SHOULD BE 0358-XX
TEST # 7 OR 8 FAIL
8
7
NO
INSPECT (A09)U4010
0:7FFD
0:7FFD OR PART NUMBER ?
P.N.
U4010 MAY CONTAIN WRONG ROM. PART # SHOULD BE 0360-XX.
A
B
C

2919-98

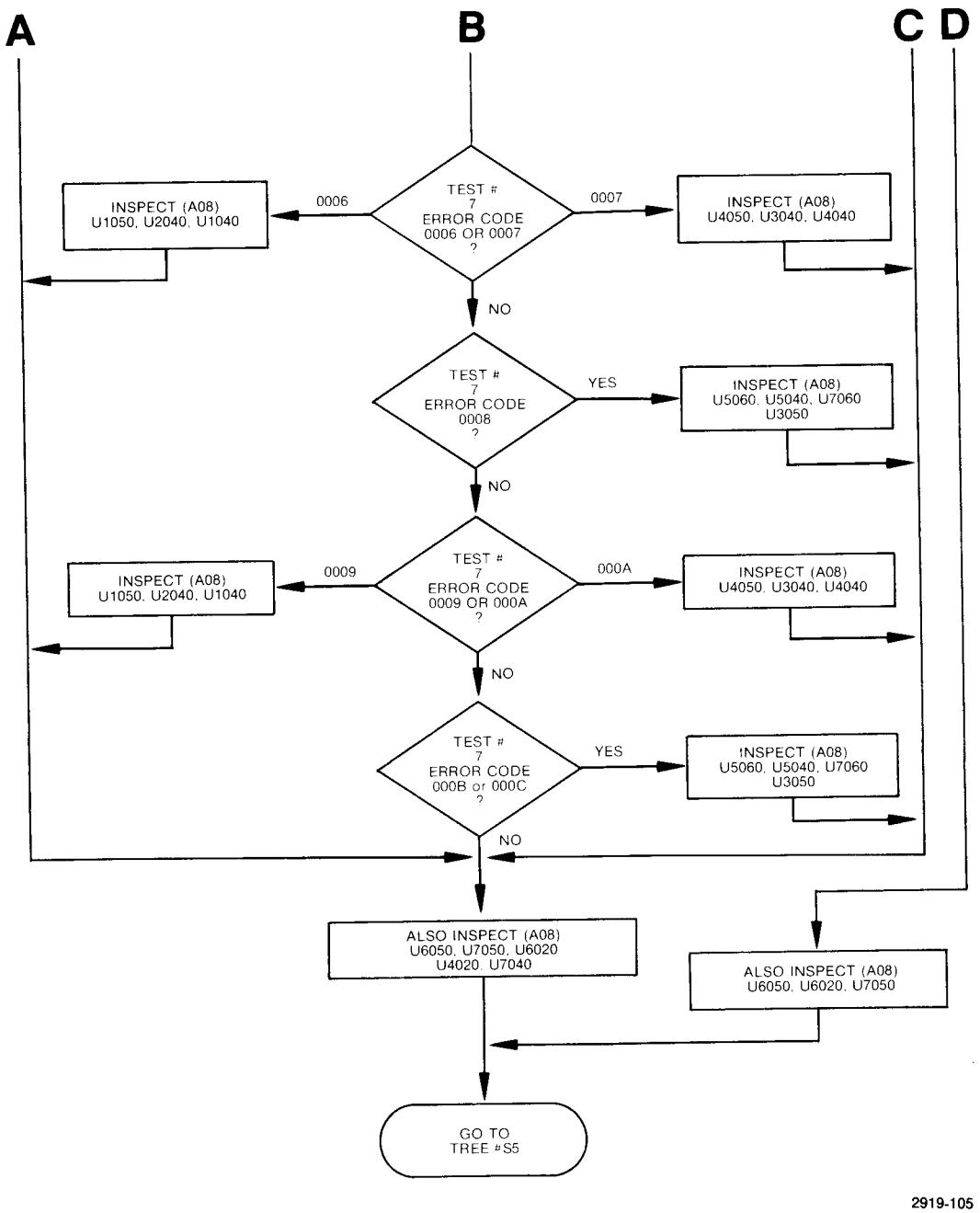
FIRMWARE ROMS TREE (CON'T.)




STATE MACHINE TREE
TEST # 1 OR 2 FAIL
BIT 0-3
INSPECT (A08) U2060, U6060, U2050
BIT 4-7
INSPECT (A08) U5060, U6060, U2050
NO
ALSO INSPECT (A08) U6050, U6020, U7050, U4060
TEST # 3 FAIL
YES
INSPECT (A08) U1060, U3050, U2050
NO
TEST # 4 FAIL
1-4, 6,7
INSPECT (A08) U3050, U4060, U2050
0,5
BIT 0
INSPECT (A08) U3050, U1060, U2050
BIT 5
INSPECT (A08) U3050, U5040, U2030
NO
TEST # 5 FAIL
5
INSPECT (A08) U5040, U3050, U2030
6-7
INSPECT (A08) U5040, U7060 U5050, U5060
NO
TEST # 6 FAIL
5
INSPECT (A08) U5040, U3050, U3030
6-7
INSPECT (A08) U5040, U7060, U5050
NO
TEST # 7 ERROR CODE 0001 OR 0002 ?
0001
INSPECT (A08) U1050
0002
INSPECT (A08) U4050
NO
TEST # 7 ERROR CODE 0003 OR 0004 ?
0003
INSPECT (A08) U1050, U2040, U1040
0004
INSPECT (A08) U4050, U3040, U4040
NO
TEST # 7 ERROR CODE 0005 ?
YES
INSPECT (A08) U5060, U5040, U7060 U3050
NO
A
B
C D

2919-100

STATE MACHINE TREE (CON'T.)



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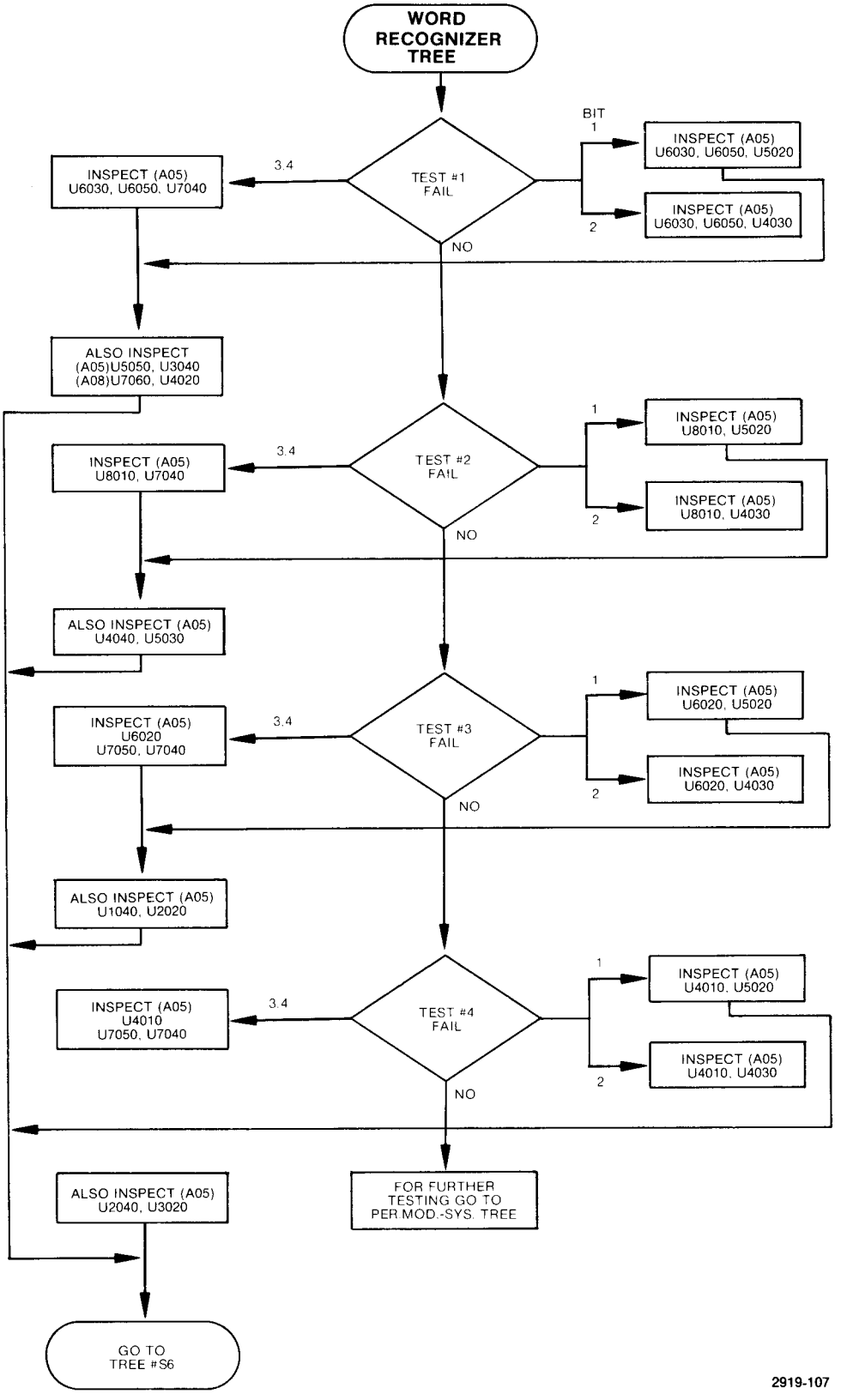
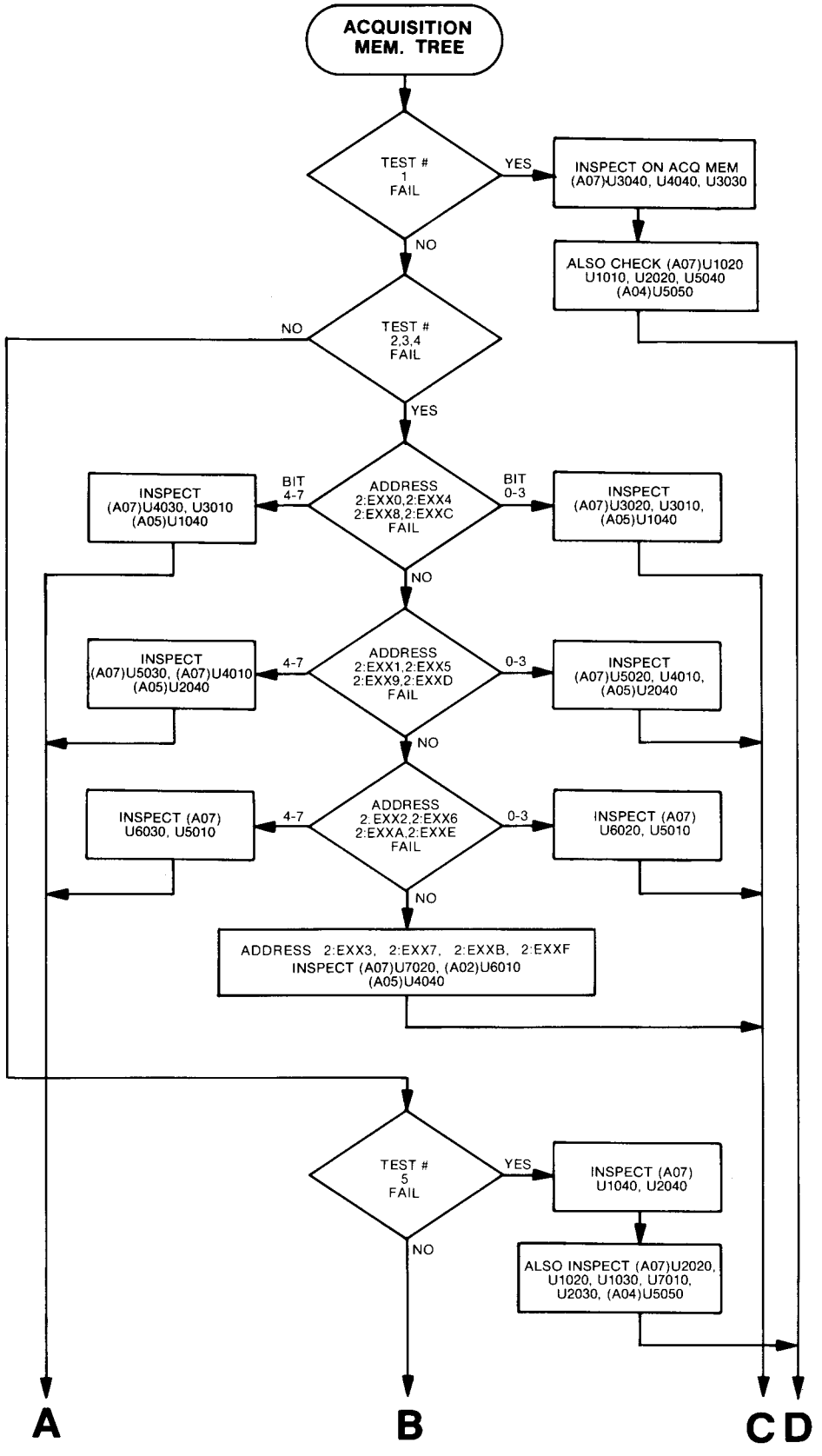
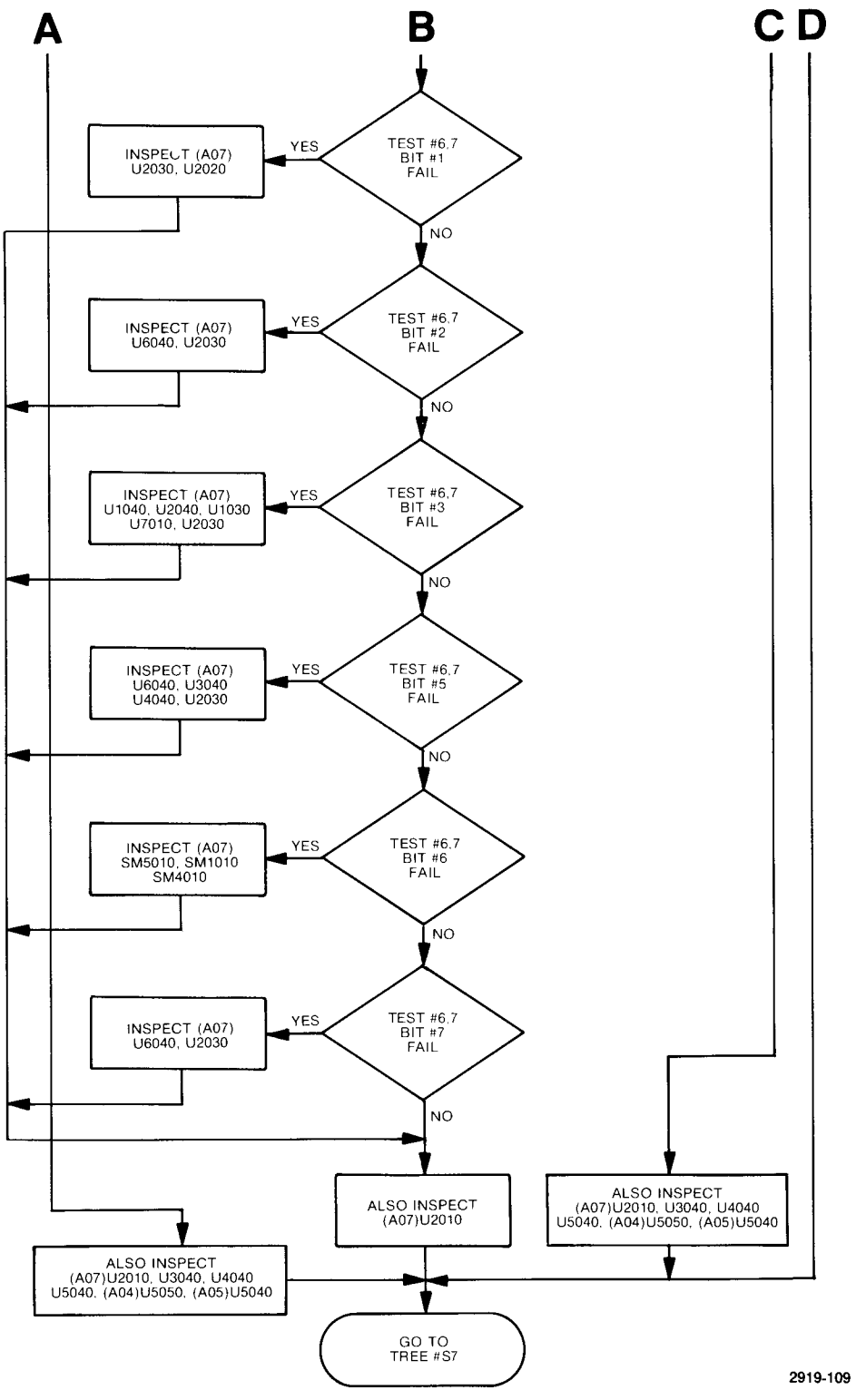
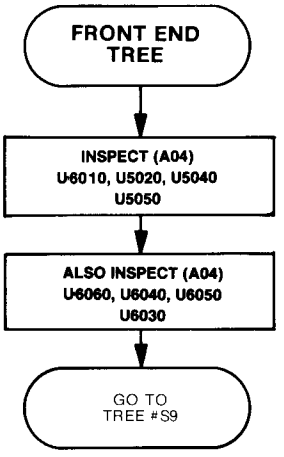

WORD RECOGNIZER TREE
TEST #1 FAIL
BIT
1
2
3.4
INSPECT (A05) U6030, U6050, U5020
INSPECT (A05) U6030, U6050, U4030
INSPECT (A05) U6030, U6050, U7040
NO
ALSO INSPECT (A05)U5050, U3040 (A08)U7060, U4020
TEST #2 FAIL
INSPECT (A05) U8010, U5020
INSPECT (A05) U8010, U4030
INSPECT (A05) U8010, U7040
ALSO INSPECT (A05) U4040, U5030
TEST #3 FAIL
INSPECT (A05) U6020, U5020
INSPECT (A05) U6020, U4030
INSPECT (A05) U6020 U7050, U7040
ALSO INSPECT (A05) U1040, U2020
TEST #4 FAIL
INSPECT (A05) U4010, U5020
INSPECT (A05) U4010, U4030
INSPECT (A05) U4010 U7050, U7040
FOR FURTHER TESTING GO TO PER MOD.-SYS. TREE
ALSO INSPECT (A05) U2040, U3020
GO TO TREE #S6
2919-107


ACQUISITION MEM. TREE
TEST # 1 FAIL
YES
INSPECT ON ACQ MEM (A07)U3040, U4040, U3030
ALSO CHECK (A07)U1020 U1010, U2020, U5040 (A04)U5050
NO
TEST # 2,3,4 FAIL
NO
YES
ADDRESS 2:EXX0,2:EXX4 2:EXX8,2:EXXC FAIL
BIT 4-7
INSPECT (A07)U4030, U3010 (A05)U1040
BIT 0-3
INSPECT (A07)U3020, U3010, (A05)U1040
NO
ADDRESS 2:EXX1,2:EXX5 2:EXX9,2:EXXD FAIL
4-7
INSPECT (A07)U5030, (A07)U4010 (A05)U2040
0-3
INSPECT (A07)U5020, U4010, (A05)U2040
NO
ADDRESS 2:EXX2,2:EXX6 2:EXXA,2:EXXE FAIL
4-7
INSPECT (A07) U6030, U5010
0-3
INSPECT (A07) U6020, U5010
NO
ADDRESS 2:EXX3, 2:EXX7, 2:EXXB, 2:EXXF INSPECT (A07)U7020, (A02)U6010 (A05)U4040
TEST # 5 FAIL
YES
INSPECT (A07) U1040, U2040
NO
ALSO INSPECT (A07)U2020, U1020, U1030, U7010, U2030, (A04)U5050
A
B
C D
2919-108

ACQUISITION MEMORY TREE (CON'T)





NOTE:
FOR FURTHER CHECKS OF THE FRONT END AT THIS LEVEL, GO TO PER MOD-SYS. TREE.

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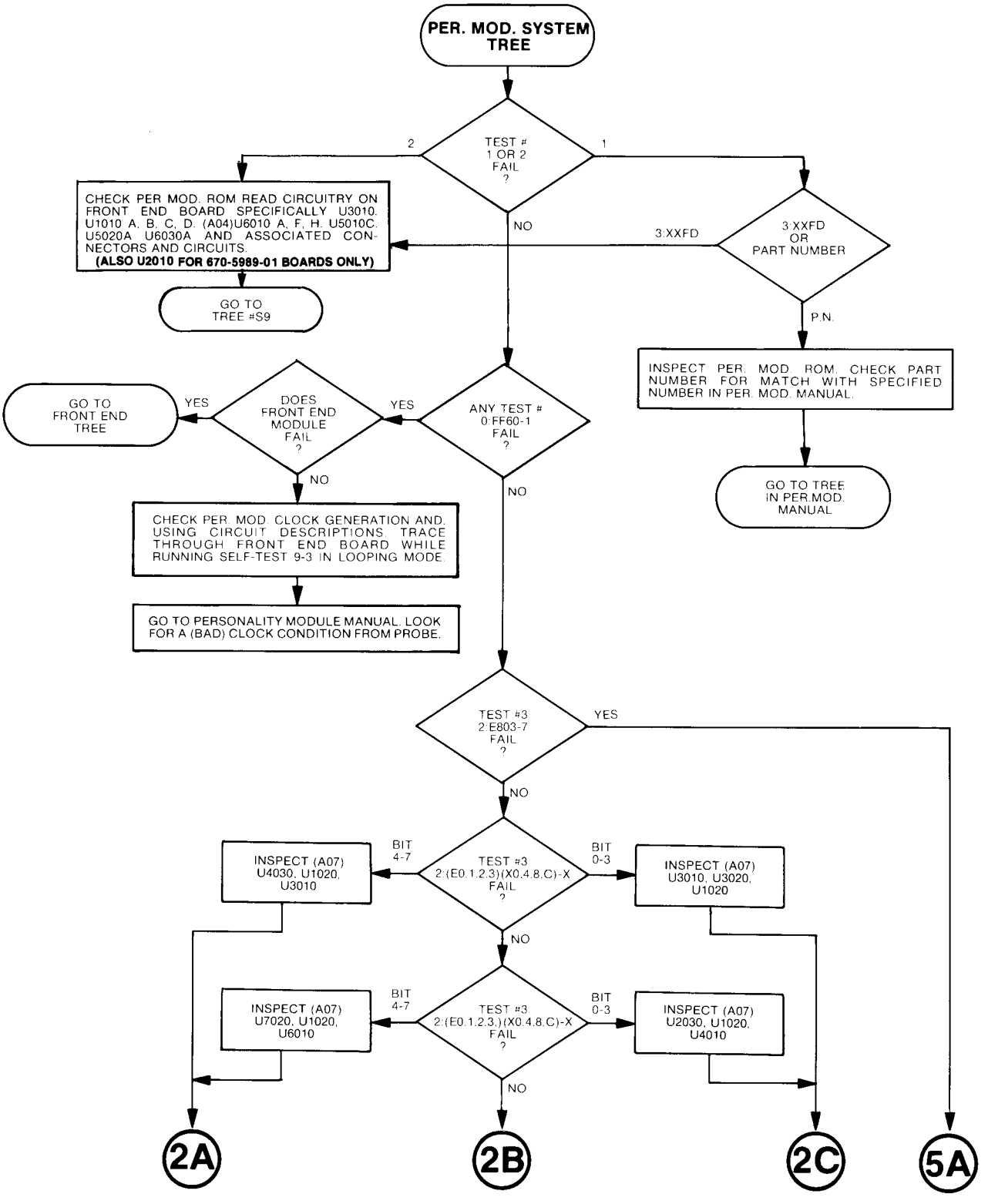
ASSUME PROBE IS OPERATIONAL



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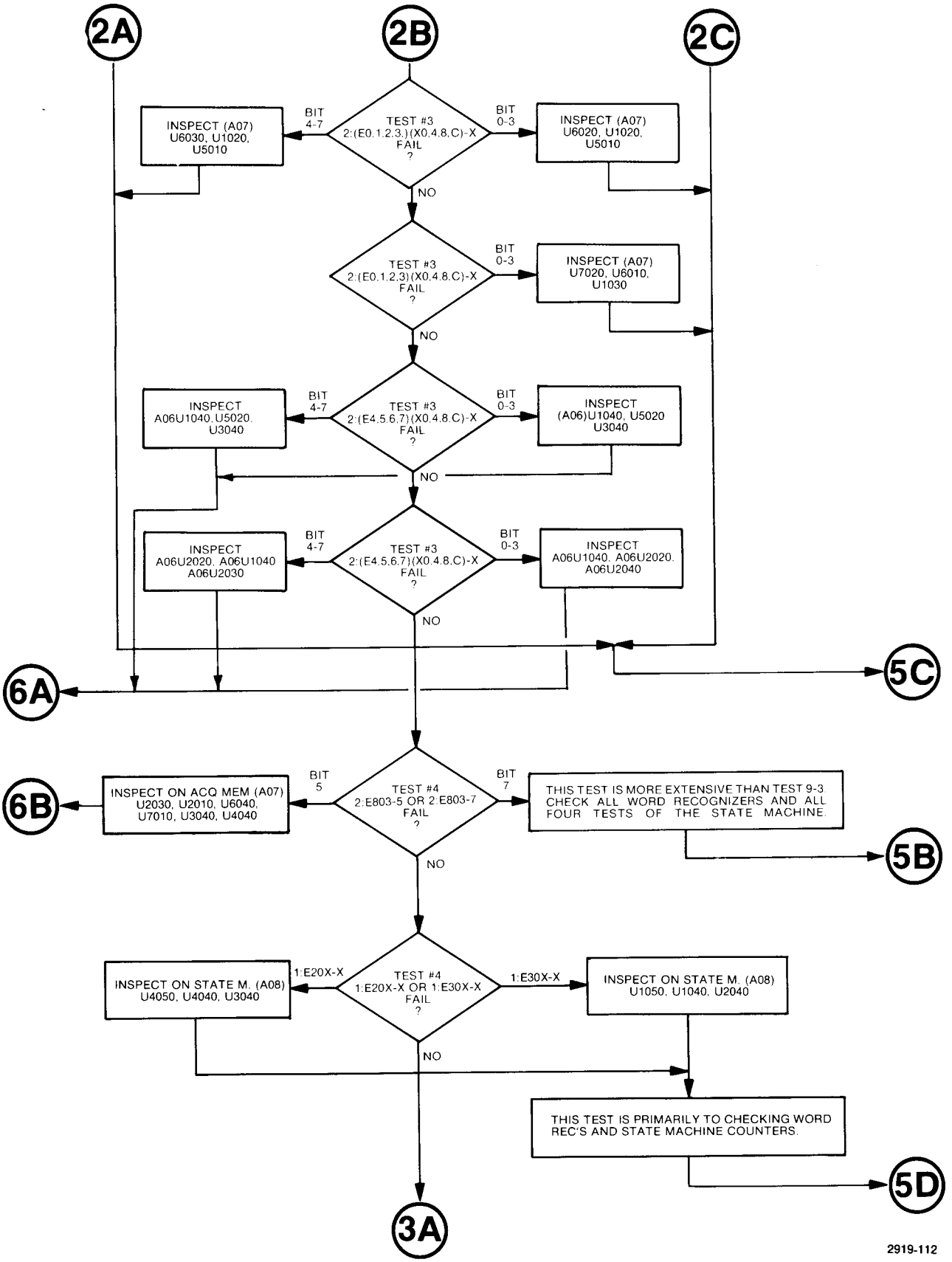
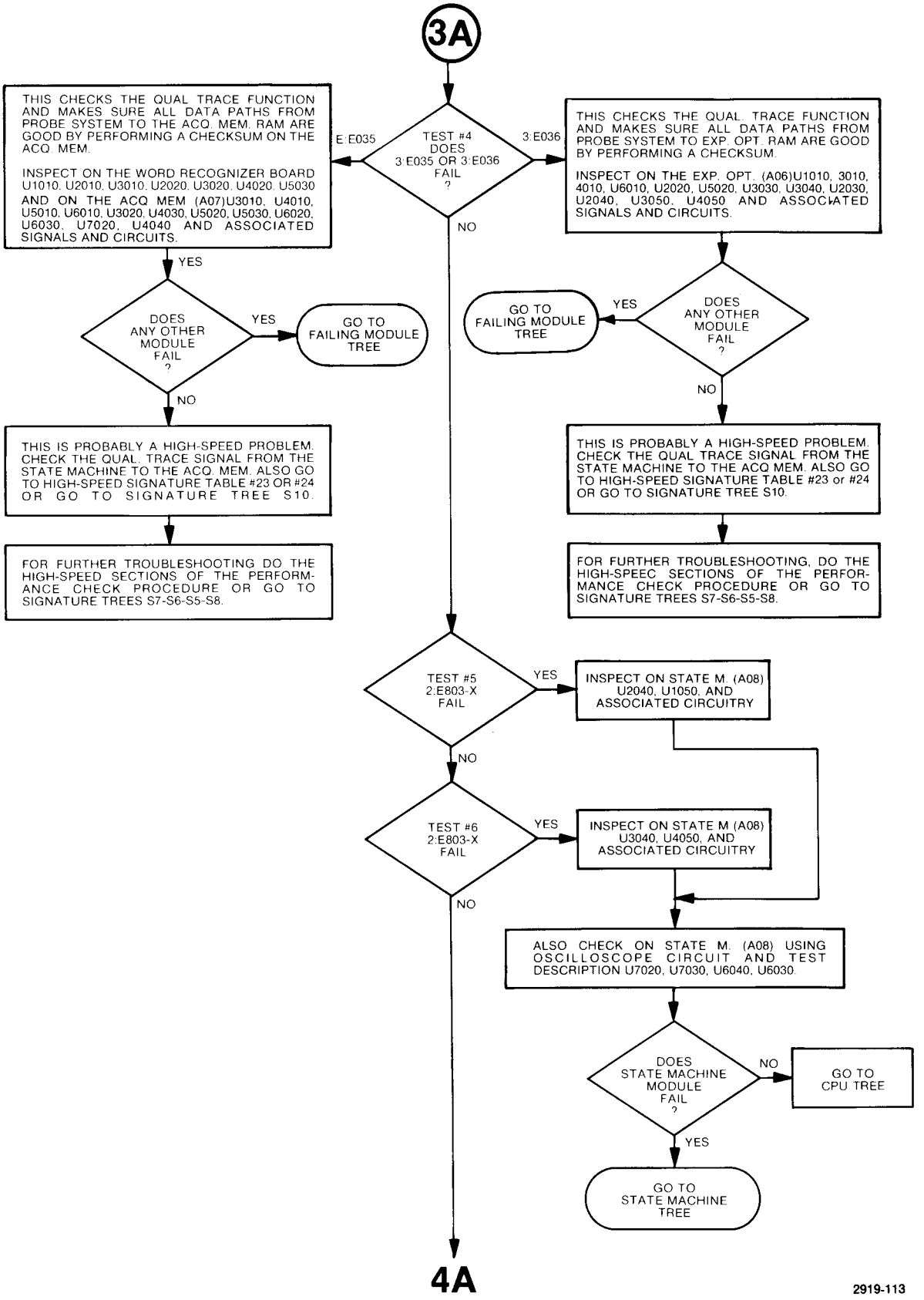
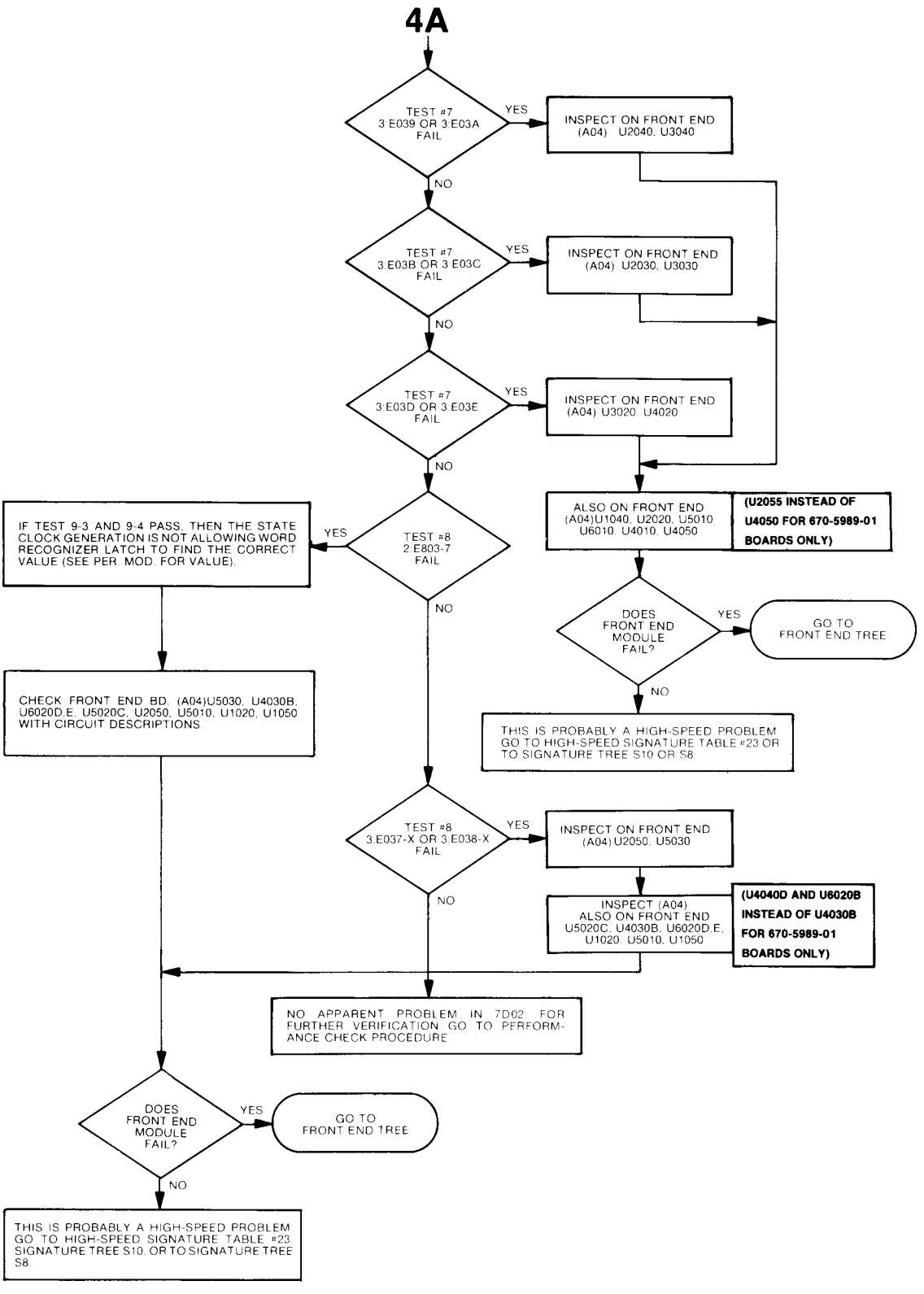
PERSONALITY MODULE SYSTEM TREE (CON'T.)



PERSONALITY MODULE SYSTEM TREE (CON'T.)



PERSONALITY MODULE SYSTEM TREE (CON'T.)



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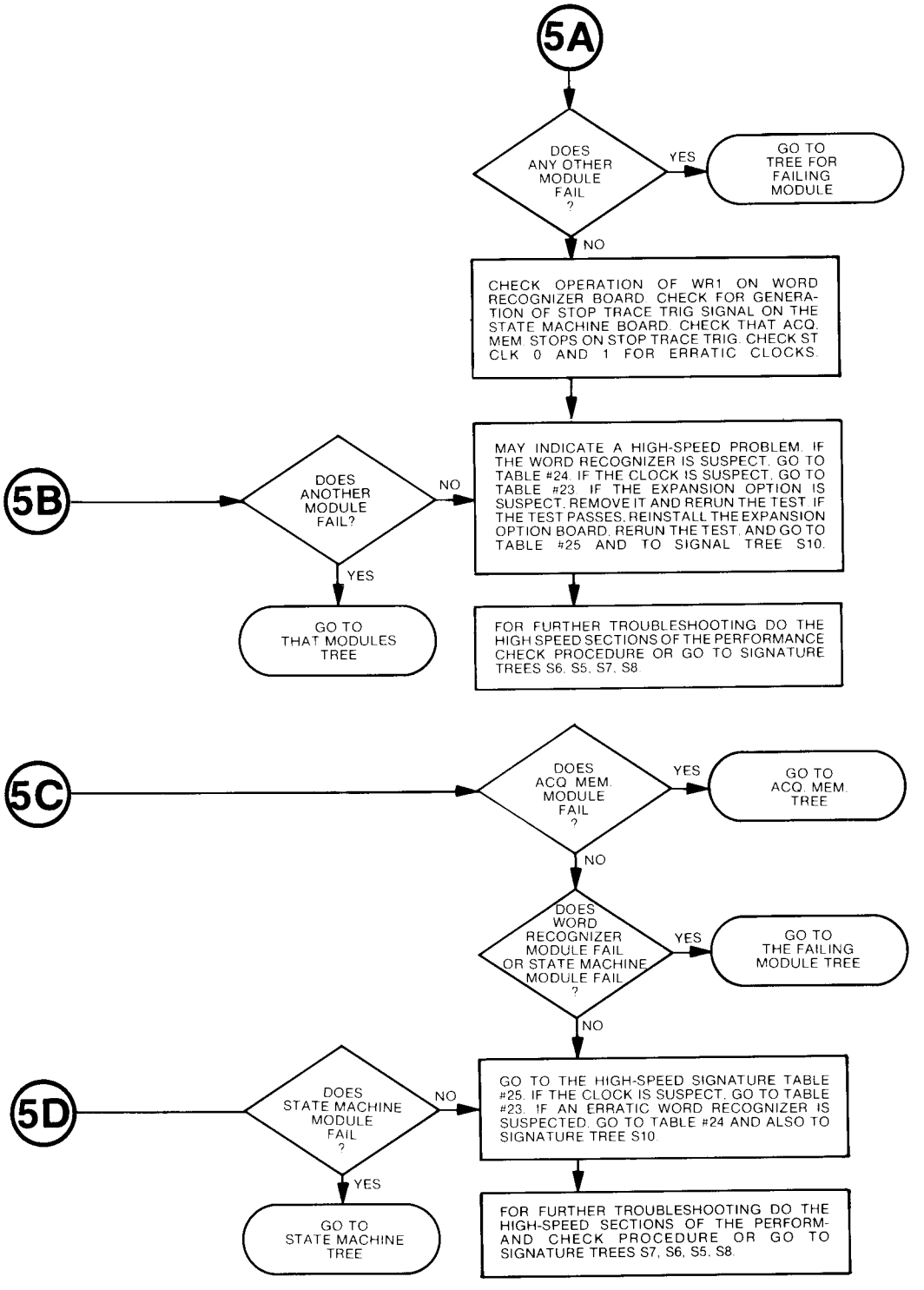
PERSONALITY MODULE SYSTEM TREE (CON'T.)



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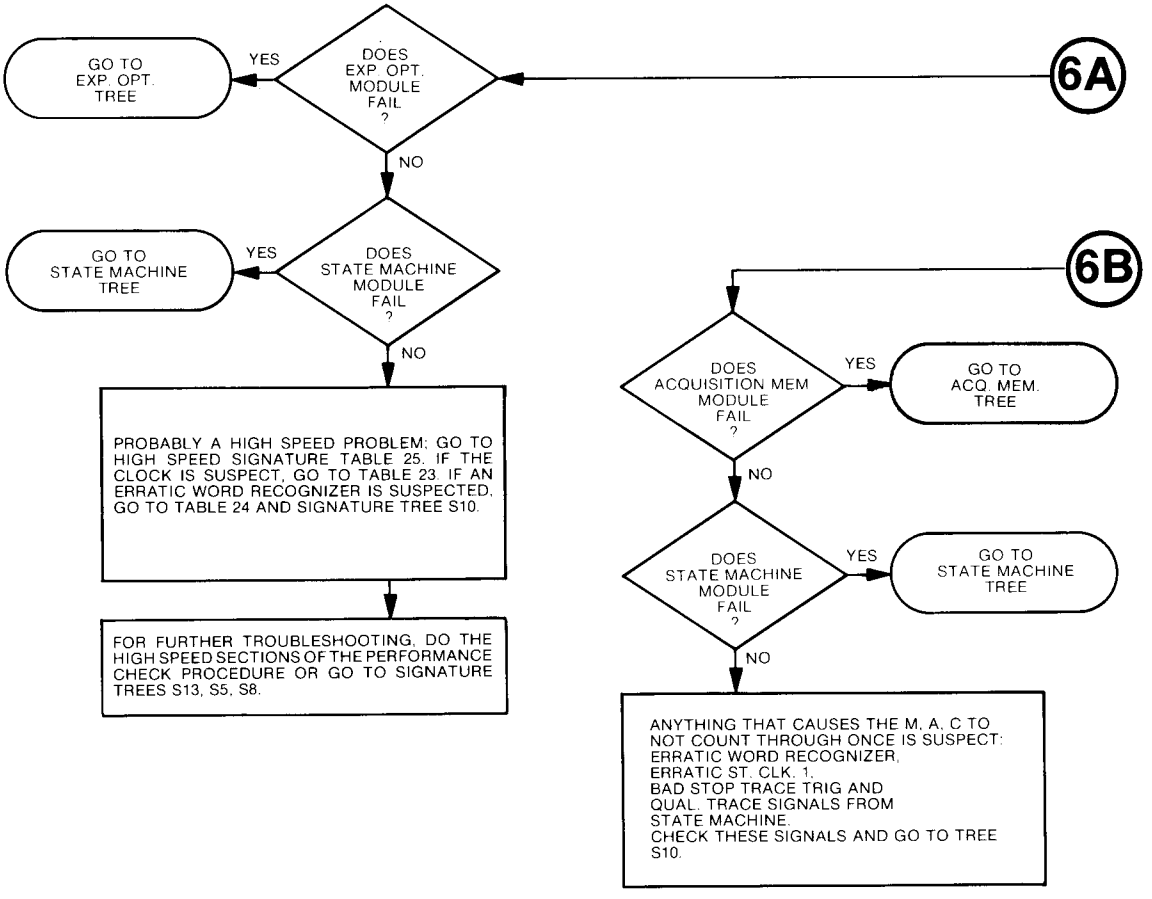
PERSONALITY MODULE SYSTEM TREE (CON'T.)



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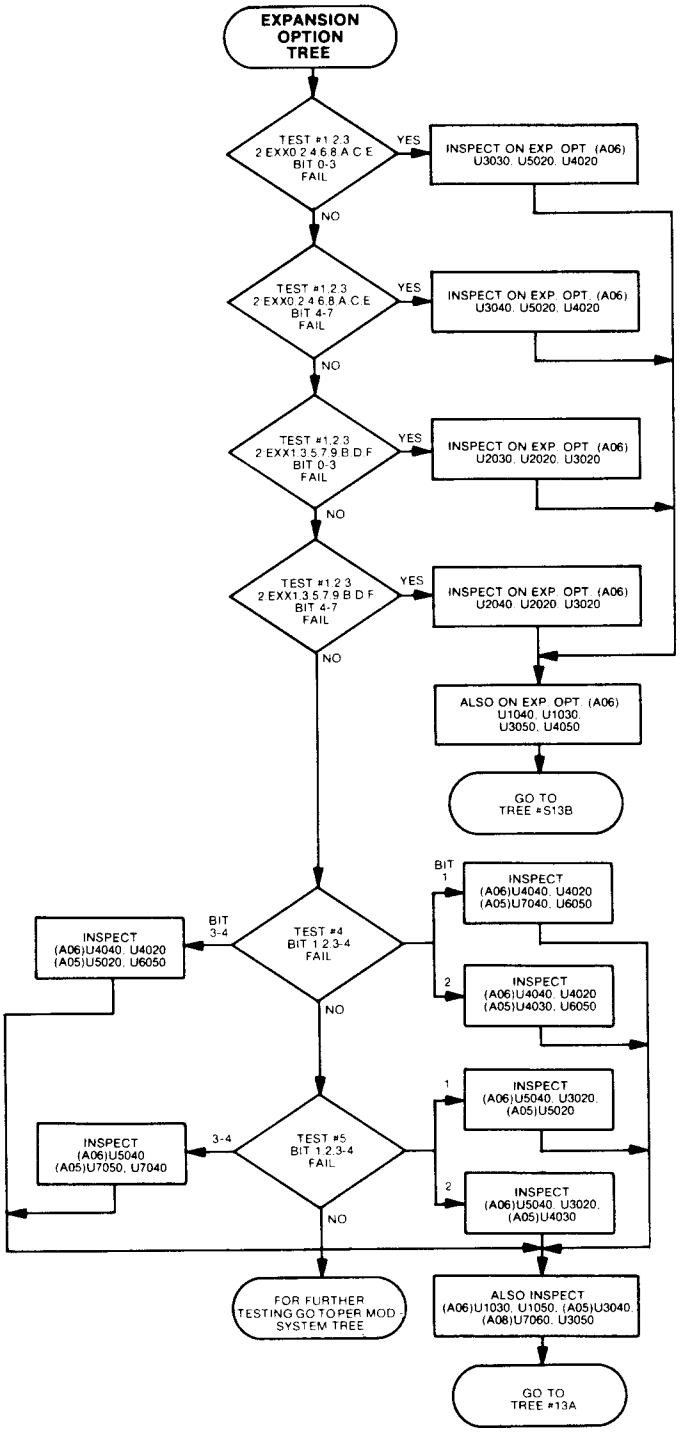
EXPANSION OPTION TREE
TEST #1,2,3 2 EXX0,2,4,6,8,A,C,E BIT 0-3 FAIL
YES
INSPECT ON EXP. OPT. (A06) U3030, U5020, U4020
NO
TEST #1,2,3 2 EXX0,2,4,6,8,A,C,E BIT 4-7 FAIL
YES
INSPECT ON EXP. OPT. (A06) U3040, U5020, U4020
NO
TEST #1,2,3 2 EXX1,3,5,7,9,B,D,F BIT 0-3 FAIL
YES
INSPECT ON EXP. OPT. (A06) U2030, U2020, U3020
NO
TEST #1,2,3 2 EXX1,3,5,7,9,B,D,F BIT 4-7 FAIL
YES
INSPECT ON EXP. OPT. (A06) U2040, U2020, U3020
NO
ALSO ON EXP. OPT. (A06) U1040, U1030, U3050, U4050
GO TO TREE #S13B
TEST #4 BIT 1,2,3-4 FAIL
BIT 3-4
INSPECT (A06)U4040, U4020 (A05)U5020, U6050
BIT 1
INSPECT (A06)U4040, U4020 (A05)U7040, U6050
2
INSPECT (A06)U4040, U4020 (A05)U4030, U6050
NO
TEST #5 BIT 1,2,3-4 FAIL
3-4
INSPECT (A06)U5040 (A05)U7050, U7040
1
INSPECT (A06)U5040, U3020, (A05)U5020
2
INSPECT (A06)U5040, U3020, (A05)U4030
NO
FOR FURTHER TESTING GO TO PER MOD - SYSTEM TREE
ALSO INSPECT (A06)U1030, U1050, (A05)U3040, (A08)U7060, U3050
GO TO TREE #13A

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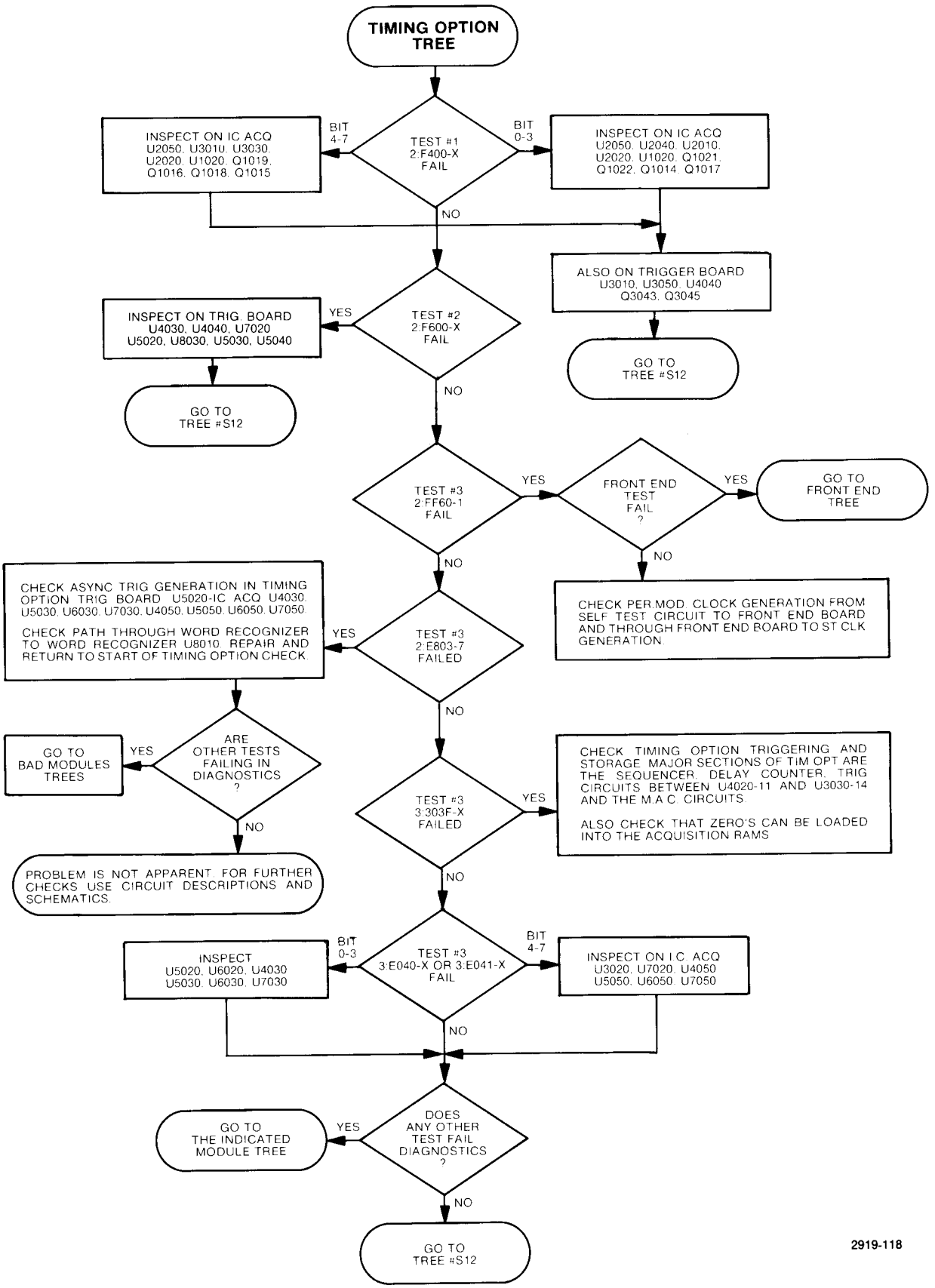
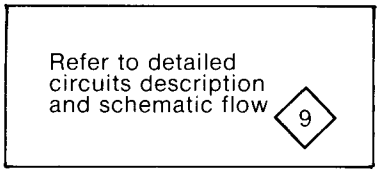

TIMING OPTION TREE
TEST #1 2:F400-X FAIL
BIT 4-7
INSPECT ON IC ACQ U2050, U3010, U3030, U2020, U1020, Q1019, Q1016, Q1018, Q1015
BIT 0-3
INSPECT ON IC ACQ U2050, U2040, U2010, U2020, U1020, Q1021, Q1022, Q1014, Q1017
NO
ALSO ON TRIGGER BOARD U3010, U3050, U4040 Q3043, Q3045
GO TO TREE #S12
TEST #2 2:F600-X FAIL
YES
INSPECT ON TRIG. BOARD U4030, U4040, U7020 U5020, U8030, U5030, U5040
GO TO TREE #S12
NO
TEST #3 2:FF60-1 FAIL
YES
FRONT END TEST FAIL ?
YES
GO TO FRONT END TREE
NO
CHECK PER.MOD. CLOCK GENERATION FROM SELF. TEST CIRCUIT TO FRONT END BOARD AND THROUGH FRONT END BOARD TO ST.CLK GENERATION.
NO
TEST #3 2:E803-7 FAILED
YES
CHECK ASYNC TRIG GENERATION IN TIMING OPTION TRIG BOARD U5020-IC ACQ U4030, U5030, U6030, U7030, U4050, U5050, U6050, U7050.
CHECK PATH THROUGH WORD RECOGNIZER TO WORD RECOGNIZER U8010. REPAIR AND RETURN TO START OF TIMING OPTION CHECK.
NO
TEST #3 3:303F-X FAILED
YES
CHECK TIMING OPTION TRIGGERING AND STORAGE MAJOR SECTIONS OF TIM OPT ARE THE SEQUENCER, DELAY COUNTER, TRIG CIRCUITS BETWEEN U4020-11 AND U3030-14 AND THE M.A.C. CIRCUITS.
ALSO CHECK THAT ZERO'S CAN BE LOADED INTO THE ACQUISITION RAMS
NO
ARE OTHER TESTS FAILING IN DIAGNOSTICS ?
YES
GO TO BAD MODULES TREES
NO
PROBLEM IS NOT APPARENT. FOR FURTHER CHECKS USE CIRCUIT DESCRIPTIONS AND SCHEMATICS.
TEST #3 3:E040-X OR 3:E041-X FAIL
BIT 0-3
INSPECT U5020, U6020, U4030 U5030, U6030, U7030
BIT 4-7
INSPECT ON I.C. ACQ U3020, U7020, U4050 U5050, U6050, U7050
NO
DOES ANY OTHER TEST FAIL DIAGNOSTICS ?
YES
GO TO THE INDICATED MODULE TREE
NO
GO TO TREE #S12

2919-118

SIGNATURE TREES

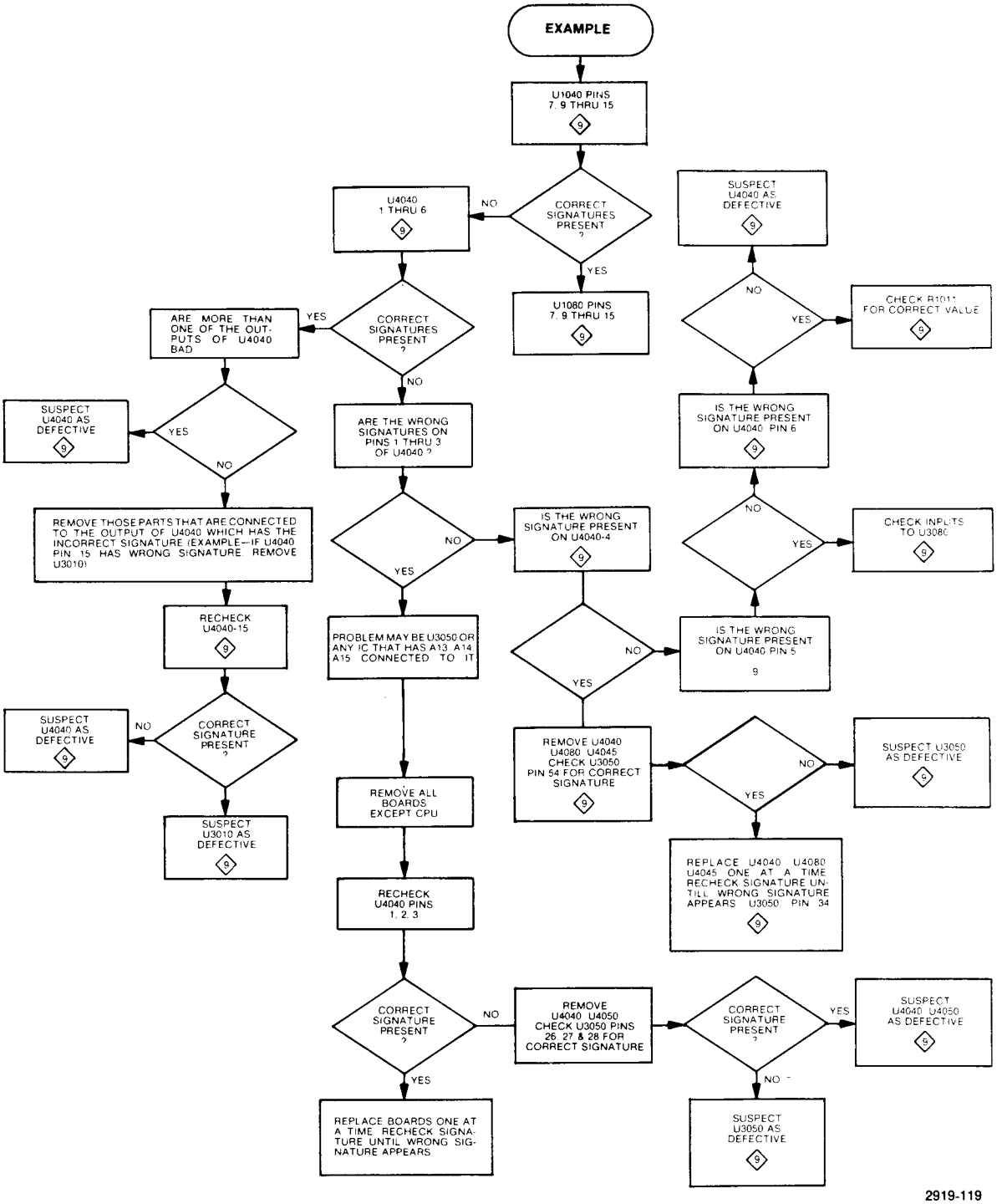
The signature trees which follow are only for preliminary localization of the problem. An Example Tree on the next page shows a process that a service person might use to get to specific faults from the process blocks which appear at the end of each branch of the signature trees. These process blocks look like this:



The number in the diamond is the schematic diagram (in the Diagrams section).

In the Example Tree which follows, a wrong output from one unit is traced backward through the circuitry to its various possible sources. The technician should employ a similar method in the circuits indicated by a particular signature tree outcome.

If the indications of a particular problem lead to specific possiblities, the technician may wish to bypass these trees and go directly to the signature tables for the suspect area.


EXAMPLE
U1040 PINS 7, 9 THRU 15
CORRECT SIGNATURES PRESENT ?
NO
YES
U4040 1 THRU 6
U1080 PINS 7, 9 THRU 15
SUSPECT U4040 AS DEFECTIVE
NO
YES
CHECK R1011 FOR CORRECT VALUE
CORRECT SIGNATURES PRESENT ?
YES
NO
ARE MORE THAN ONE OF THE OUTPUTS OF U4040 BAD
IS THE WRONG SIGNATURE PRESENT ON U4040 PIN 6
SUSPECT U4040 AS DEFECTIVE
YES
NO
ARE THE WRONG SIGNATURES ON PINS 1 THRU 3 OF U4040 ?
NO
YES
CHECK INPUTS TO U3080
IS THE WRONG SIGNATURE PRESENT ON U4040-4
REMOVE THOSE PARTS THAT ARE CONNECTED TO THE OUTPUT OF U4040 WHICH HAS THE INCORRECT SIGNATURE (EXAMPLE—IF U4040 PIN 15 HAS WRONG SIGNATURE, REMOVE U3010)
NO
YES
IS THE WRONG SIGNATURE PRESENT ON U4040 PIN 5
RECHECK U4040-15
PROBLEM MAY BE U3050 OR ANY IC THAT HAS A13, A14, A15 CONNECTED TO IT
NO
YES
SUSPECT U4040 AS DEFECTIVE
NO
CORRECT SIGNATURE PRESENT ?
REMOVE U4040 U4080 U4045 CHECK U3050 PIN 54 FOR CORRECT SIGNATURE
NO
YES
SUSPECT U3050 AS DEFECTIVE
SUSPECT U3010 AS DEFECTIVE
REMOVE ALL BOARDS EXCEPT CPU
REPLACE U4040, U4080, U4045, ONE AT A TIME, RECHECK SIGNATURE UNTIL WRONG SIGNATURE APPEARS, U3050, PIN 34
RECHECK U4040 PINS 1, 2, 3
CORRECT SIGNATURE PRESENT ?
NO
YES
REMOVE U4040, U4050, CHECK U3050 PINS 26, 27, & 28 FOR CORRECT SIGNATURE
CORRECT SIGNATURE PRESENT ?
YES
NO
SUSPECT U4040, U4050 AS DEFECTIVE
REPLACE BOARDS ONE AT A TIME, RECHECK SIGNATURE UNTIL WRONG SIGNATURE APPEARS
SUSPECT U3050 AS DEFECTIVE

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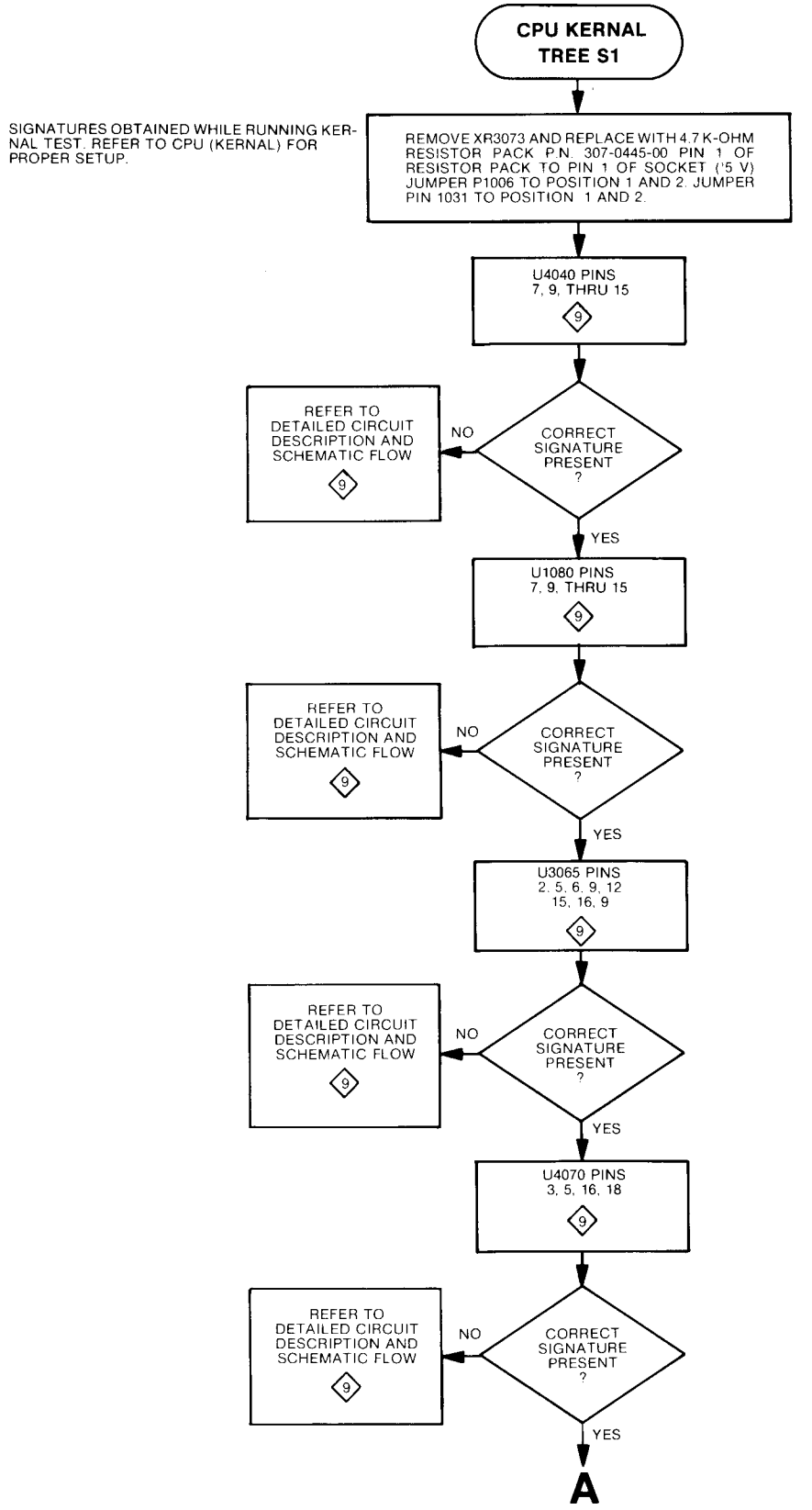
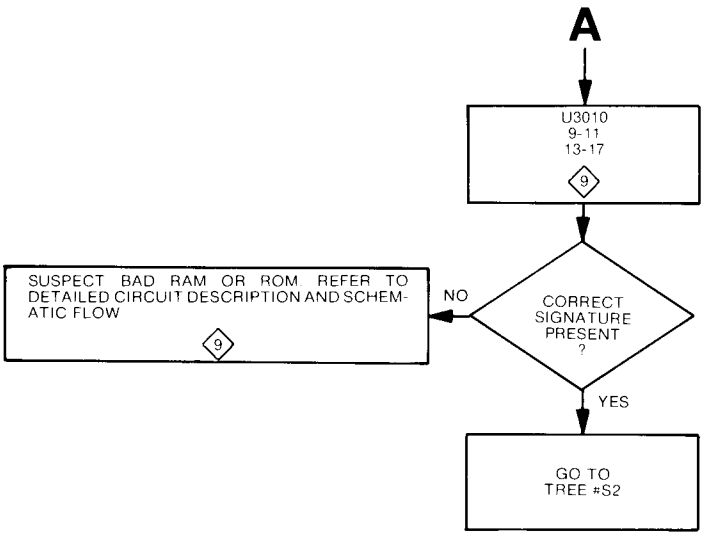

CPU KERNAL TREE S1
SIGNATURES OBTAINED WHILE RUNNING KERNAL TEST. REFER TO CPU (KERNAL) FOR PROPER SETUP.
REMOVE XR3073 AND REPLACE WITH 4.7 K-OHM RESISTOR PACK P.N. 307-0445-00 PIN 1 OF RESISTOR PACK TO PIN 1 OF SOCKET ('5 V) JUMPER P1006 TO POSITION 1 AND 2. JUMPER PIN 1031 TO POSITION 1 AND 2.
U4040 PINS 7, 9, THRU 15
9
CORRECT SIGNATURE PRESENT ?
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
9
YES
U1080 PINS 7, 9, THRU 15
9
CORRECT SIGNATURE PRESENT ?
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
9
YES
U3065 PINS 2, 5, 6, 9, 12 15, 16, 9
9
CORRECT SIGNATURE PRESENT ?
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
9
YES
U4070 PINS 3, 5, 16, 18
9
CORRECT SIGNATURE PRESENT ?
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
9
YES
A

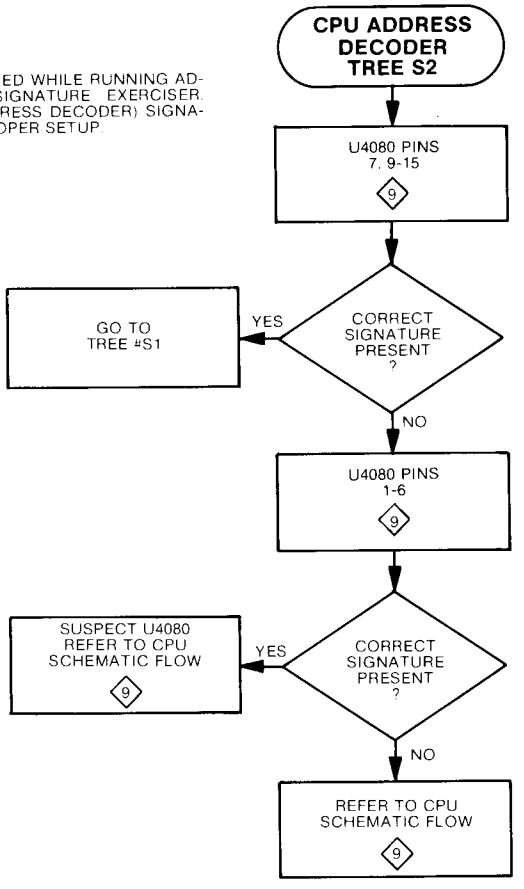
2919-120

CPU KERNAL TREE S1 (CON'T.)

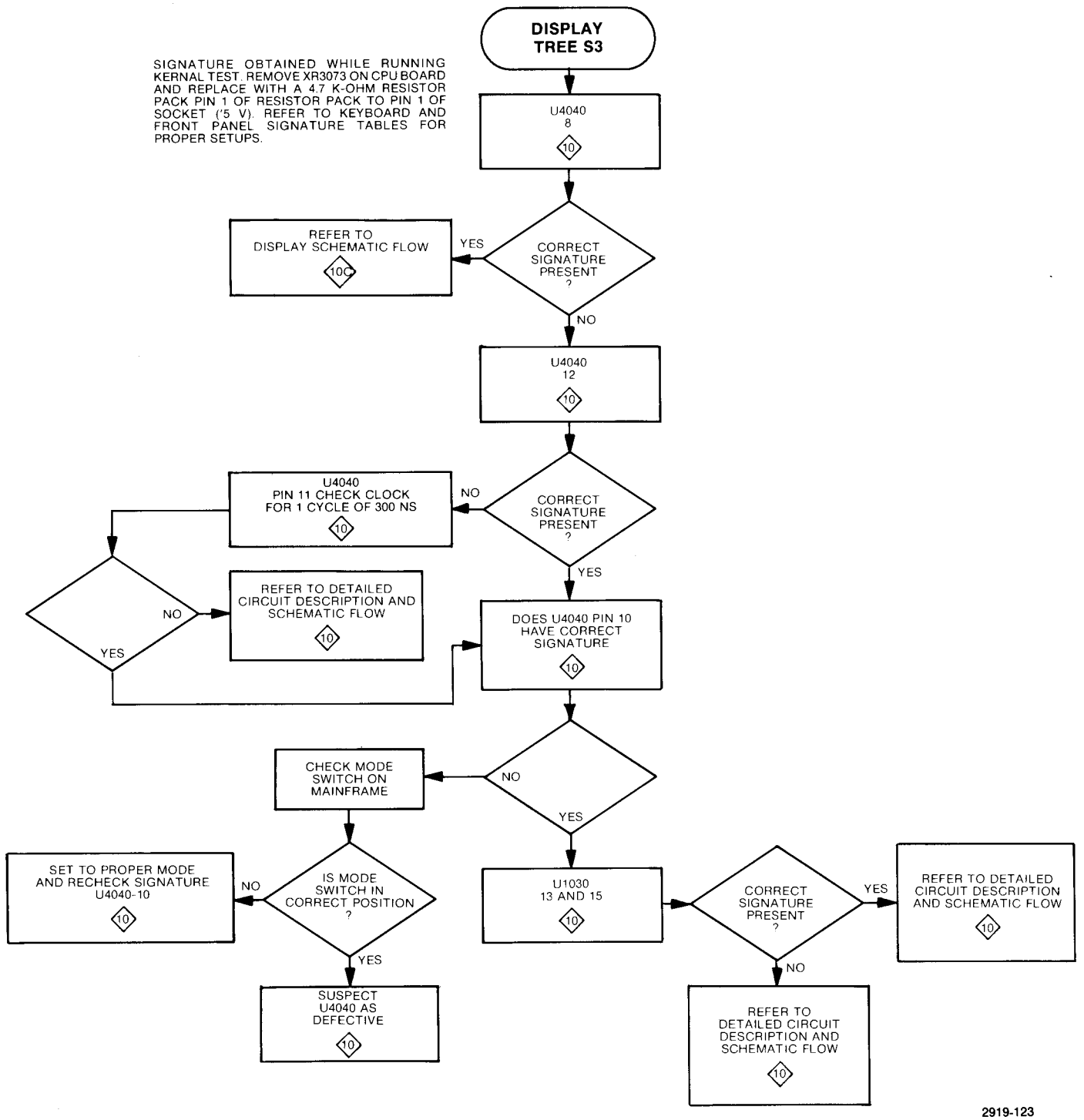


2919-121

SIGNATURES OBTAINED WHILE RUNNING ADDRESS DECODER SIGNATURE EXERCISER. REFER TO CPU (ADDRESS DECODER) SIGNATURE TABLE FOR PROPER SETUP.



2919-122


DISPLAY TREE S3
SIGNATURE OBTAINED WHILE RUNNING KERNAL TEST. REMOVE XR3073 ON CPU BOARD AND REPLACE WITH A 4.7 K-OHM RESISTOR PACK PIN 1 OF RESISTOR PACK TO PIN 1 OF SOCKET ('5 V). REFER TO KEYBOARD AND FRONT PANEL SIGNATURE TABLES FOR PROPER SETUPS.
U4040 8 10
CORRECT SIGNATURE PRESENT ?
YES
REFER TO DISPLAY SCHEMATIC FLOW 10C
NO
U4040 12 10
CORRECT SIGNATURE PRESENT ?
NO
U4040 PIN 11 CHECK CLOCK FOR 1 CYCLE OF 300 NS 10
YES
DOES U4040 PIN 10 HAVE CORRECT SIGNATURE 10
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW 10
YES
NO
CHECK MODE SWITCH ON MAINFRAME
YES
U1030 13 AND 15 10
CORRECT SIGNATURE PRESENT ?
YES
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW 10
NO
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW 10
IS MODE SWITCH IN CORRECT POSITION ?
NO
SET TO PROPER MODE AND RECHECK SIGNATURE U4040-10
YES
SUSPECT U4040 AS DEFECTIVE 10

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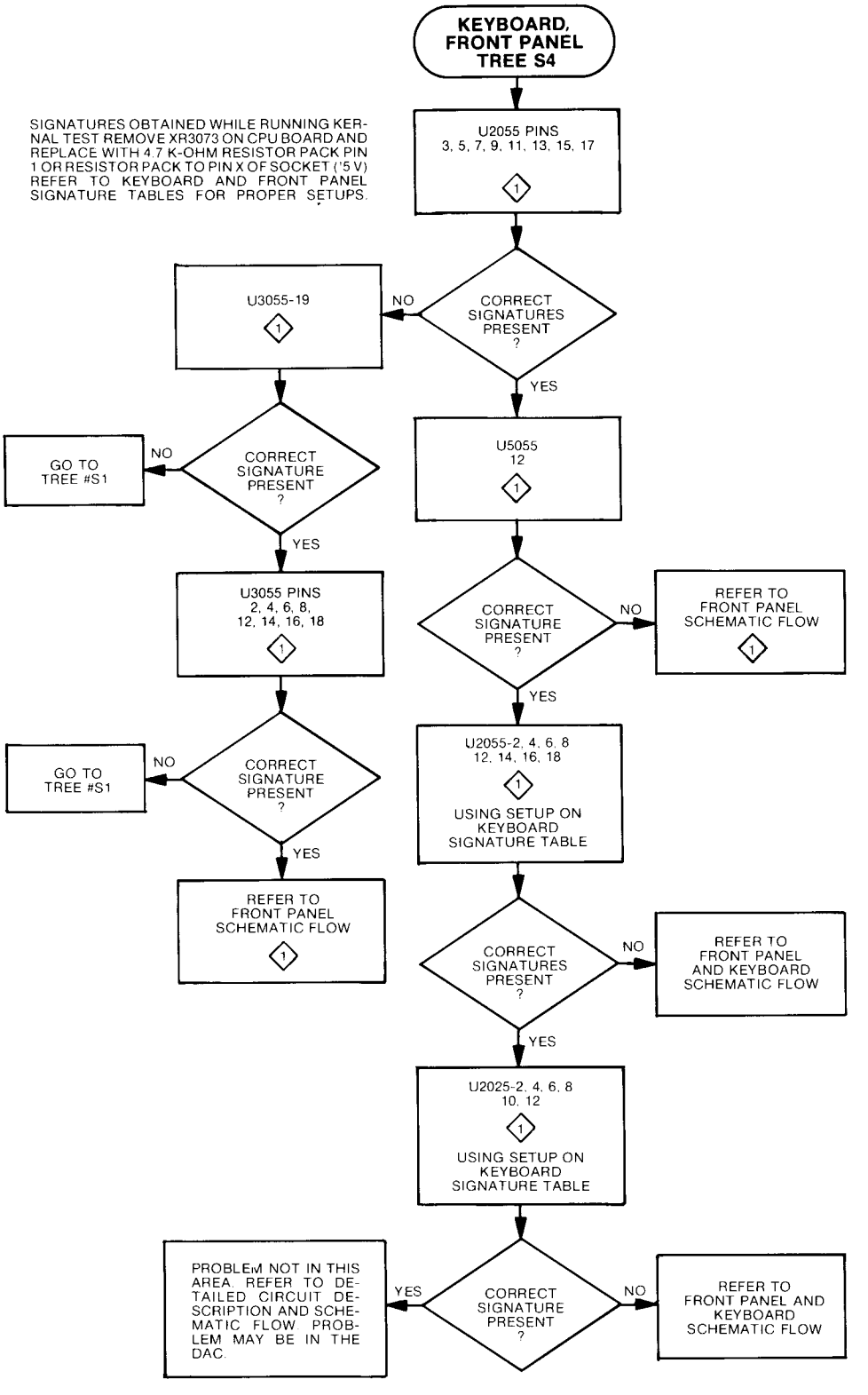
KEYBOARD, FRONT PANEL TREE S4
SIGNATURES OBTAINED WHILE RUNNING KERNAL TEST REMOVE XR3073 ON CPU BOARD AND REPLACE WITH 4.7 K-OHM RESISTOR PACK PIN 1 OR RESISTOR PACK TO PIN X OF SOCKET ('5 V) REFER TO KEYBOARD AND FRONT PANEL SIGNATURE TABLES FOR PROPER SETUPS.
U2055 PINS 3, 5, 7, 9, 11, 13, 15, 17
1
CORRECT SIGNATURES PRESENT ?
NO
U3055-19
1
YES
U5055 12
1
CORRECT SIGNATURE PRESENT ?
NO
REFER TO FRONT PANEL SCHEMATIC FLOW
1
YES
U2055-2, 4, 6, 8 12, 14, 16, 18
1
USING SETUP ON KEYBOARD SIGNATURE TABLE
CORRECT SIGNATURES PRESENT ?
NO
REFER TO FRONT PANEL AND KEYBOARD SCHEMATIC FLOW
YES
U2025-2, 4, 6, 8 10, 12
1
USING SETUP ON KEYBOARD SIGNATURE TABLE
CORRECT SIGNATURE PRESENT ?
NO
REFER TO FRONT PANEL AND KEYBOARD SCHEMATIC FLOW
YES
PROBLEM NOT IN THIS AREA. REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW. PROBLEM MAY BE IN THE DAC.
CORRECT SIGNATURE PRESENT ?
NO
GO TO TREE #S1
YES
U3055 PINS 2, 4, 6, 8, 12, 14, 16, 18
1
CORRECT SIGNATURE PRESENT ?
NO
GO TO TREE #S1
YES
REFER TO FRONT PANEL SCHEMATIC FLOW
1

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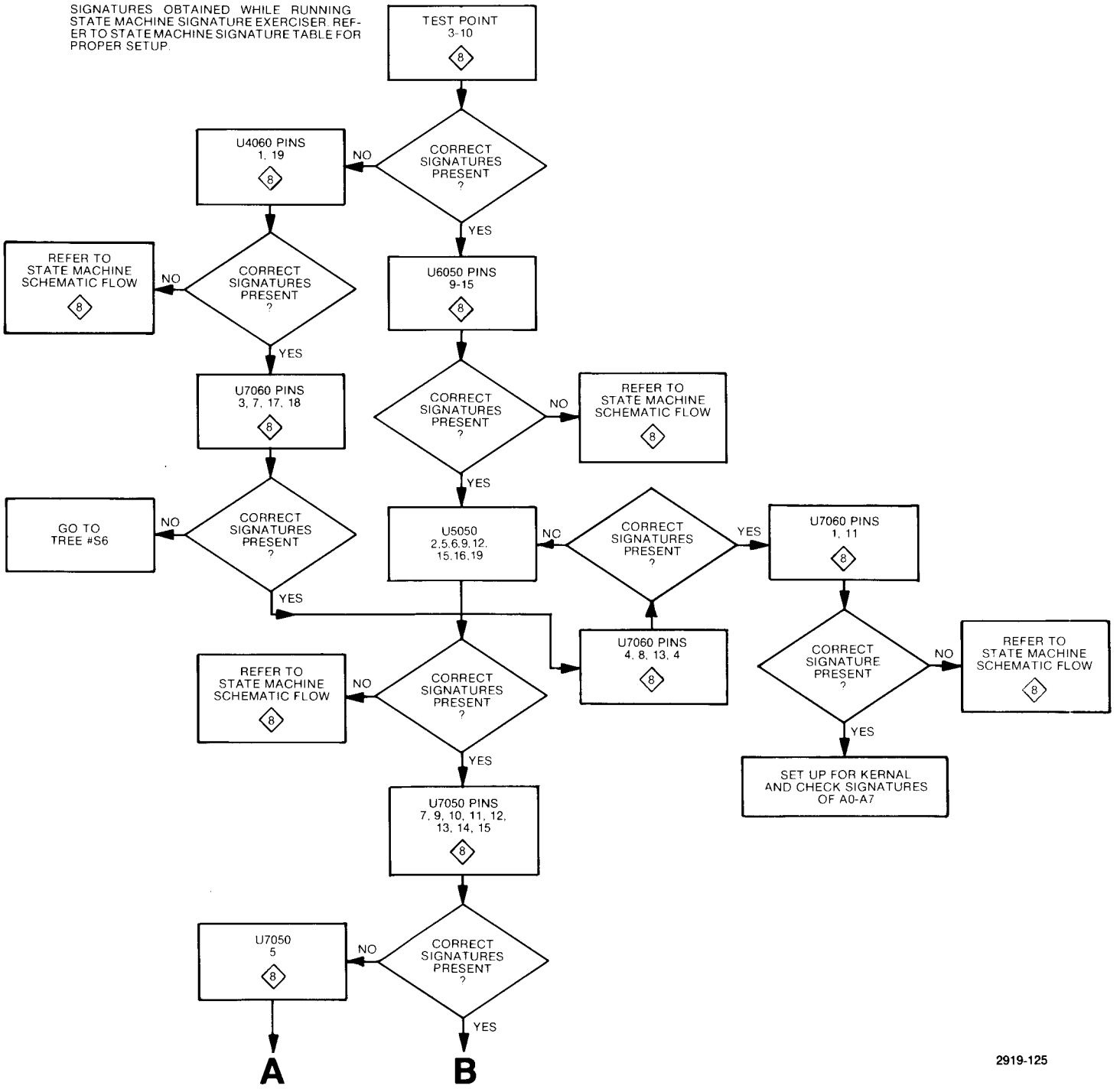
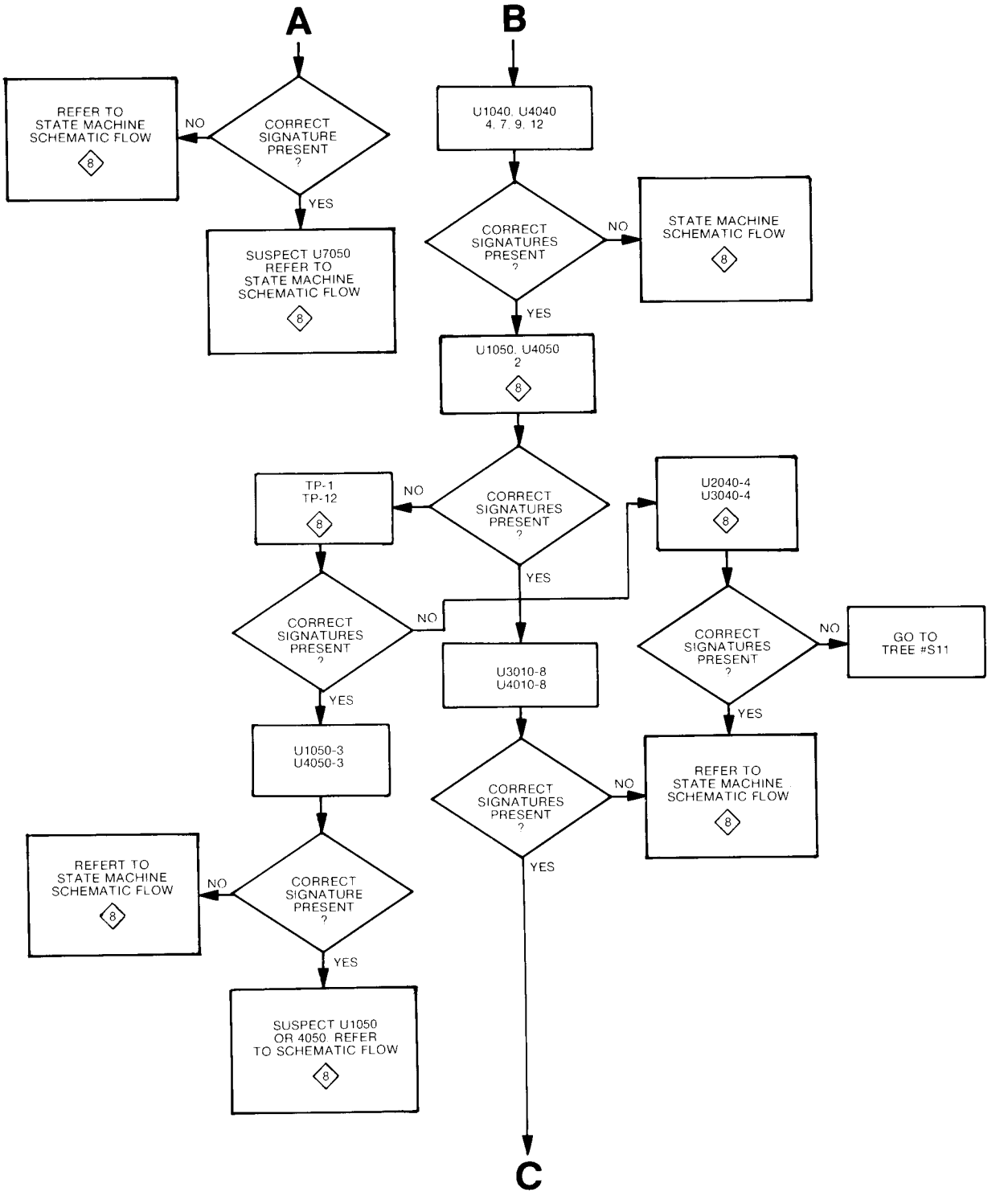
STATE MACHINE TREE S5



STATE MACHINE TREE S5 (CON'T.)



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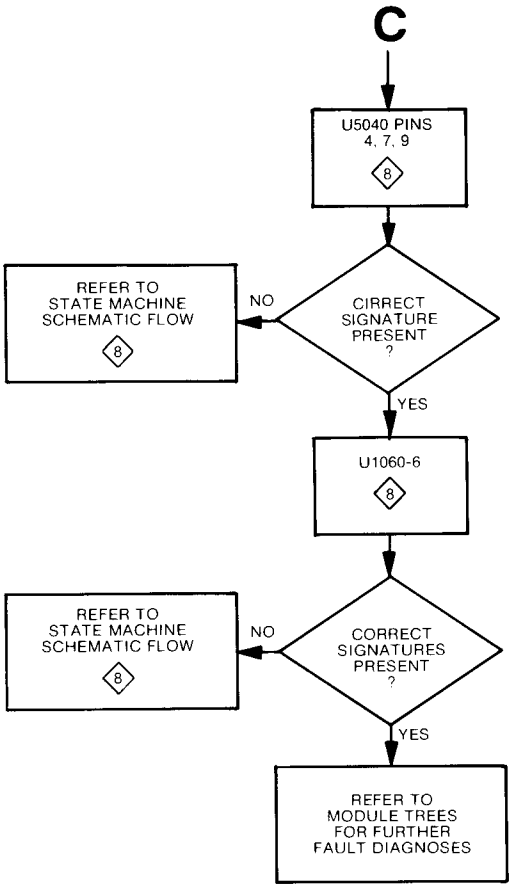
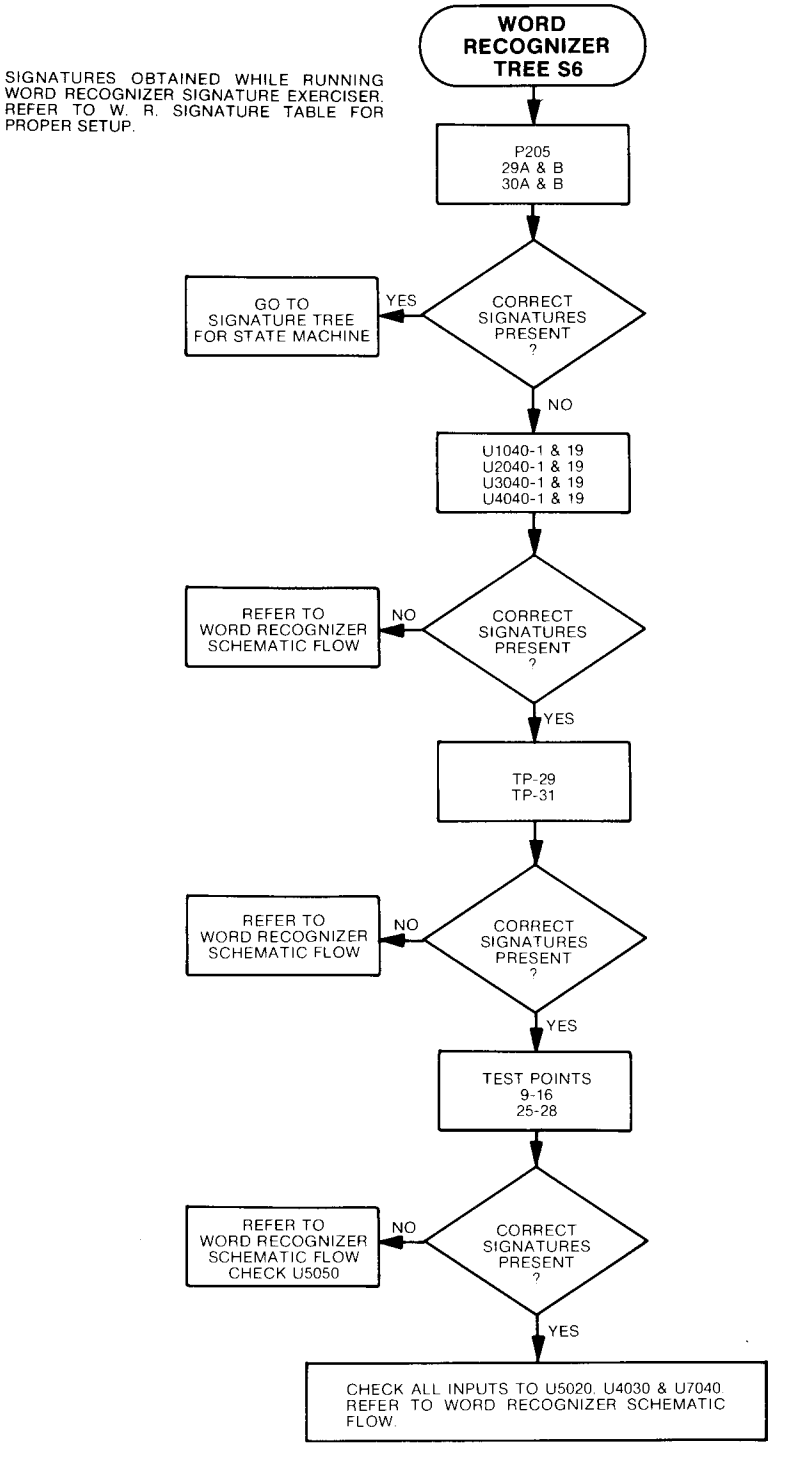
STATE MACHINE TREE (CON'T.)



2919-127


SIGNATURES OBTAINED WHILE RUNNING WORD RECOGNIZER SIGNATURE EXERCISER. REFER TO W. R. SIGNATURE TABLE FOR PROPER SETUP.
WORD RECOGNIZER TREE S6
P205 29A & B 30A & B
CORRECT SIGNATURES PRESENT ?
YES
GO TO SIGNATURE TREE FOR STATE MACHINE
NO
U1040-1 & 19 U2040-1 & 19 U3040-1 & 19 U4040-1 & 19
CORRECT SIGNATURES PRESENT ?
NO
REFER TO WORD RECOGNIZER SCHEMATIC FLOW
YES
TP-29 TP-31
CORRECT SIGNATURES PRESENT ?
NO
REFER TO WORD RECOGNIZER SCHEMATIC FLOW
YES
TEST POINTS 9-16 25-28
CORRECT SIGNATURES PRESENT ?
NO
REFER TO WORD RECOGNIZER SCHEMATIC FLOW CHECK U5050
YES
CHECK ALL INPUTS TO U5020, U4030 & U7040. REFER TO WORD RECOGNIZER SCHEMATIC FLOW.

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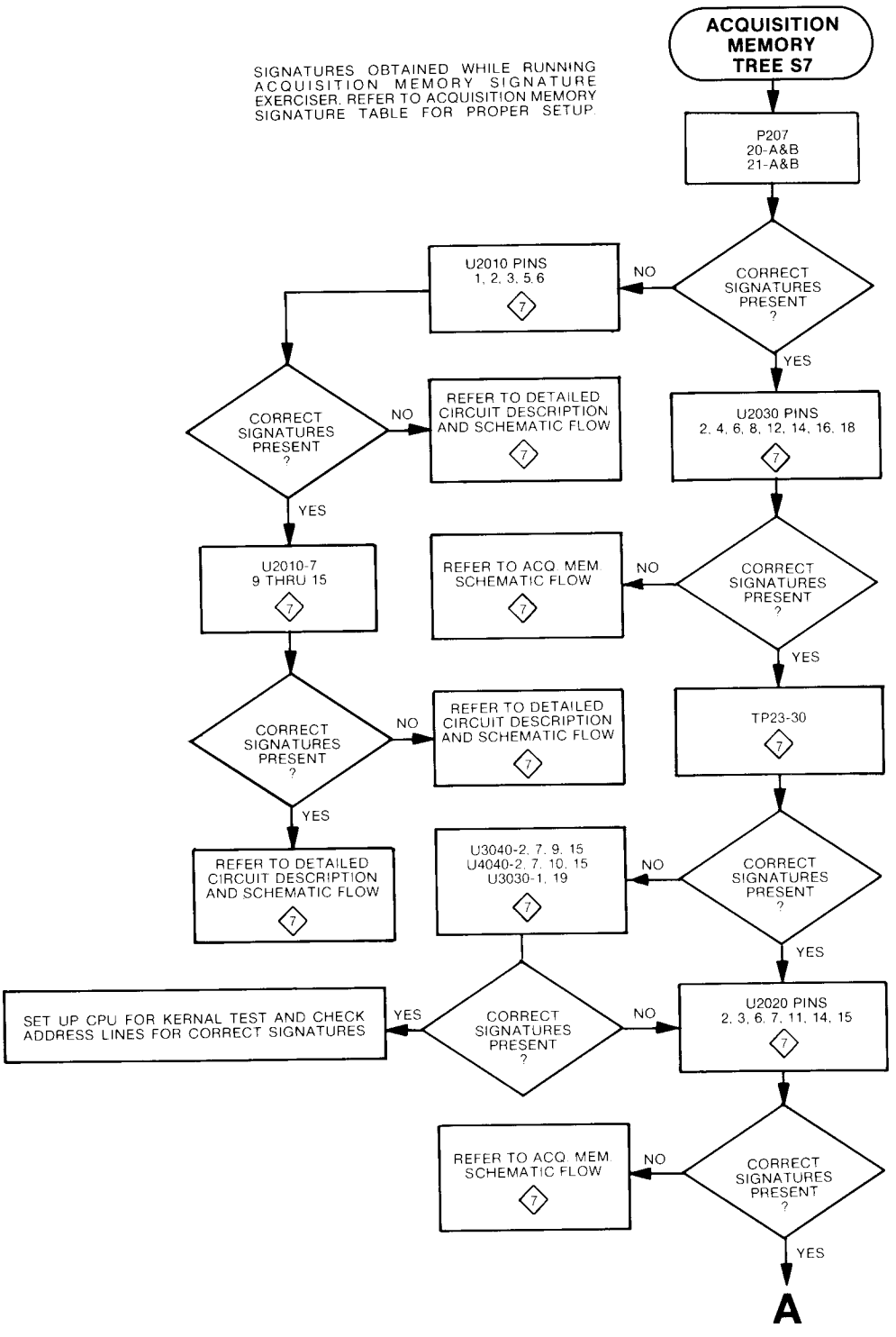
ACQUISITION MEMORY TREE S7
SIGNATURES OBTAINED WHILE RUNNING ACQUISITION MEMORY SIGNATURE EXERCISER. REFER TO ACQUISITION MEMORY SIGNATURE TABLE FOR PROPER SETUP.
P207 20-A&B 21-A&B
CORRECT SIGNATURES PRESENT ?
NO
YES
U2010 PINS 1, 2, 3, 5, 6
U2030 PINS 2, 4, 6, 8, 12, 14, 16, 18
CORRECT SIGNATURES PRESENT ?
NO
YES
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
U2010-7 9 THRU 15
CORRECT SIGNATURES PRESENT ?
NO
YES
REFER TO ACQ. MEM. SCHEMATIC FLOW
TP23-30
CORRECT SIGNATURES PRESENT ?
NO
YES
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
U3040-2, 7, 9, 15 U4040-2, 7, 10, 15 U3030-1, 19
CORRECT SIGNATURES PRESENT ?
NO
YES
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
U2020 PINS 2, 3, 6, 7, 11, 14, 15
CORRECT SIGNATURES PRESENT ?
NO
YES
SET UP CPU FOR KERNAL TEST AND CHECK ADDRESS LINES FOR CORRECT SIGNATURES
REFER TO ACQ. MEM. SCHEMATIC FLOW
CORRECT SIGNATURES PRESENT ?
NO
YES
A
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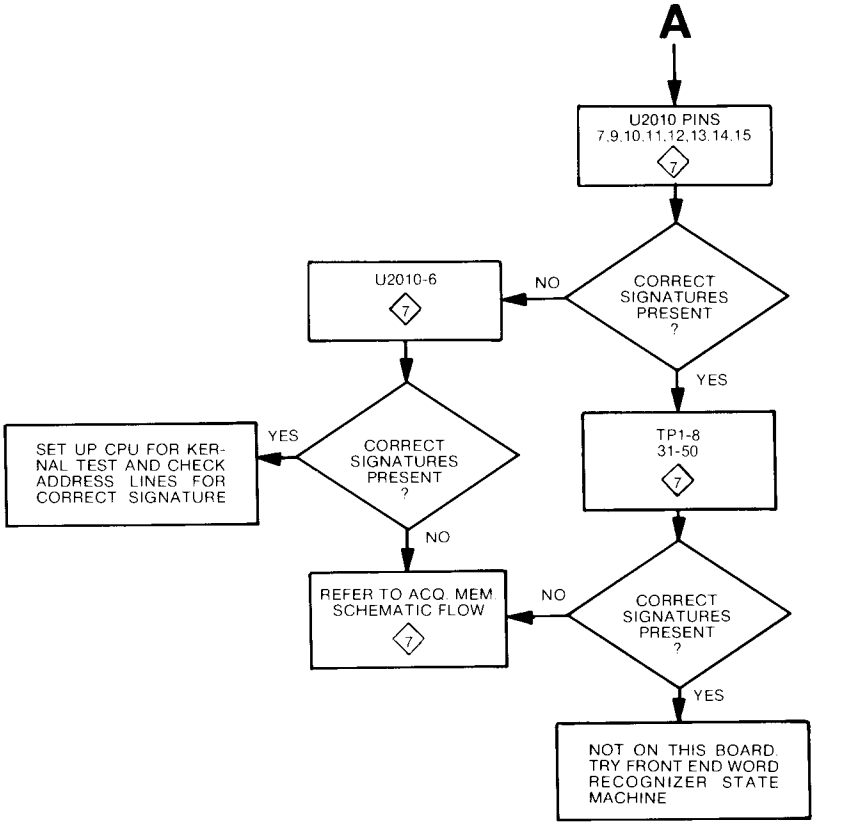
ACQUISITION MEMORY TREE S7 (CON'T.)



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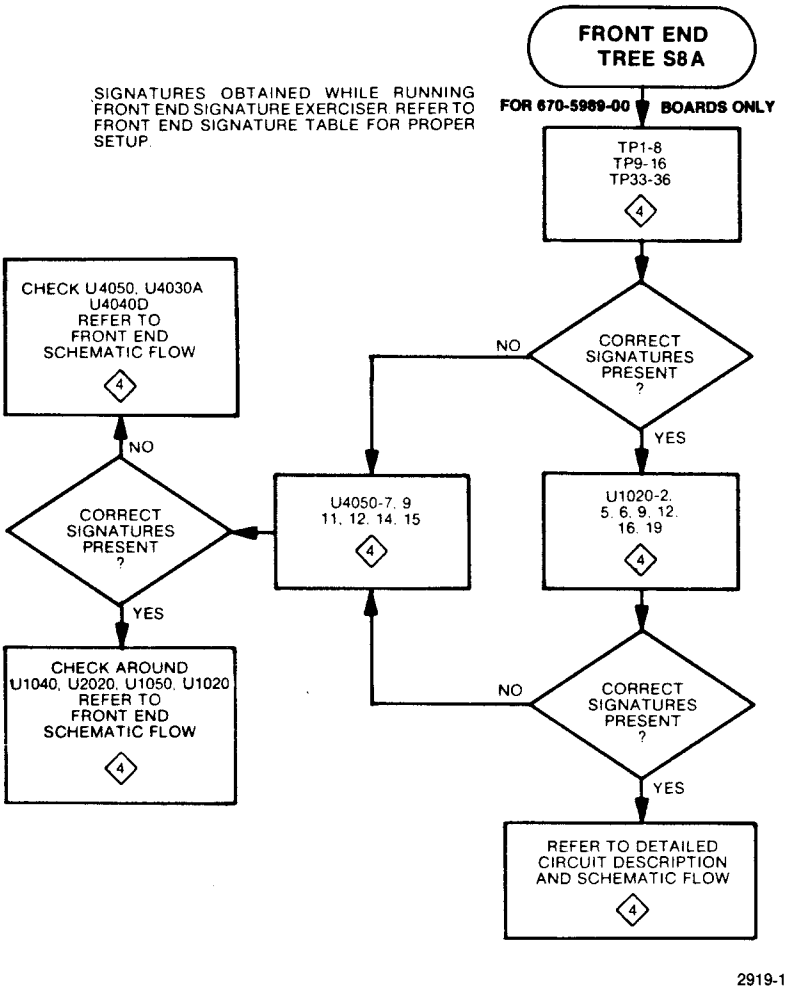
FRONT END
TREE S8A
SIGNATURES OBTAINED WHILE RUNNING FRONT END SIGNATURE EXERCISER REFER TO FRONT END SIGNATURE TABLE FOR PROPER SETUP.
FOR 670-5989-00 BOARDS ONLY
TP1-8
TP9-16
TP33-36
4
CORRECT SIGNATURES PRESENT ?
NO
YES
CHECK U4050, U4030A U4040D REFER TO FRONT END SCHEMATIC FLOW
4
U4050-7, 9 11, 12, 14, 15
4
U1020-2, 5, 6, 9, 12, 16, 19
4
CORRECT SIGNATURES PRESENT ?
NO
YES
CORRECT SIGNATURES PRESENT ?
NO
YES
CHECK AROUND U1040, U2020, U1050, U1020 REFER TO FRONT END SCHEMATIC FLOW
4
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
4

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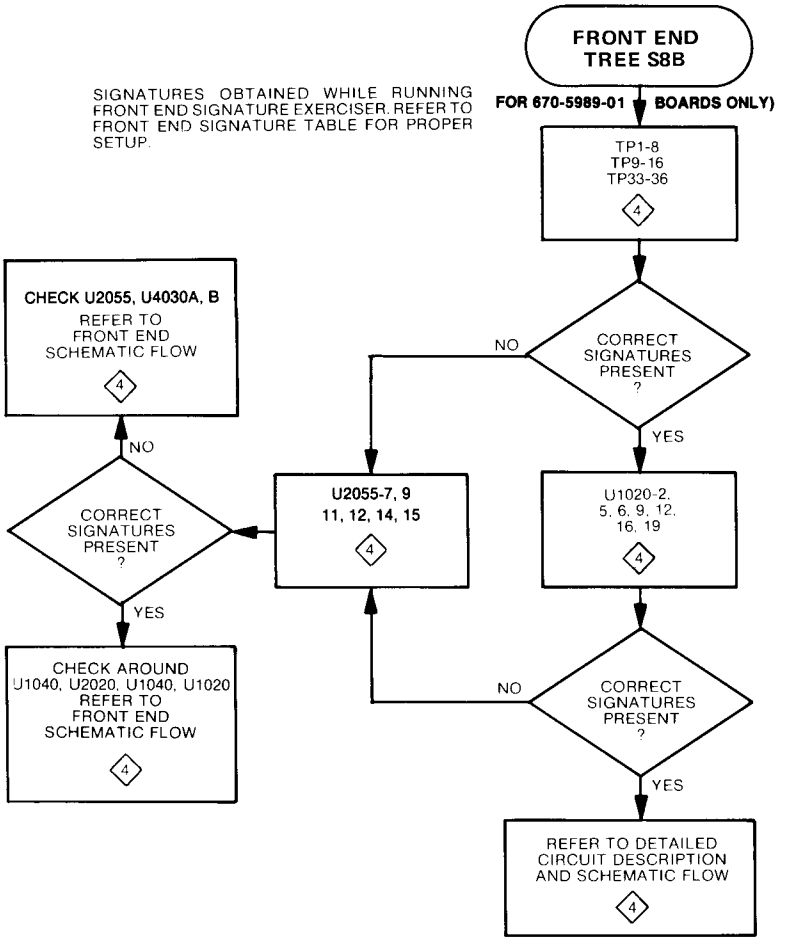
FRONT END
TREE S8B
FOR 670-5989-01 BOARDS ONLY)
SIGNATURES OBTAINED WHILE RUNNING FRONT END SIGNATURE EXERCISER. REFER TO FRONT END SIGNATURE TABLE FOR PROPER SETUP.
TP1-8
TP9-16
TP33-36
4
CORRECT SIGNATURES PRESENT ?
NO
YES
U1020-2, 5, 6, 9, 12, 16, 19
4
CORRECT SIGNATURES PRESENT ?
NO
YES
U2055-7, 9 11, 12, 14, 15
4
CORRECT SIGNATURES PRESENT ?
NO
YES
CHECK U2055, U4030A, B
REFER TO FRONT END SCHEMATIC FLOW
4
CHECK AROUND U1040, U2020, U1040, U1020
REFER TO FRONT END SCHEMATIC FLOW
4
REFER TO DETAILED CIRCUIT DESCRIPTION AND SCHEMATIC FLOW
4

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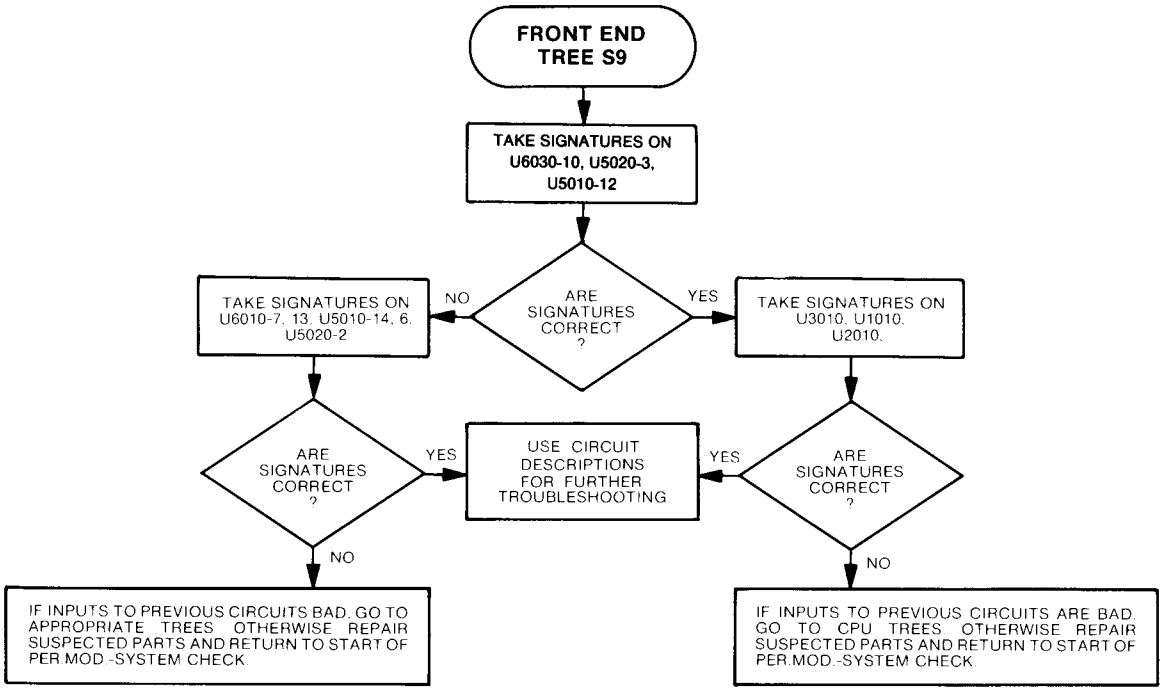
FRONT END TREE S9
TAKE SIGNATURES ON U6030-10, U5020-3, U5010-12
ARE SIGNATURES CORRECT ?
NO
YES
TAKE SIGNATURES ON U6010-7, 13, U5010-14, 6, U5020-2
TAKE SIGNATURES ON U3010, U1010, U2010,
ARE SIGNATURES CORRECT ?
YES
USE CIRCUIT DESCRIPTIONS FOR FURTHER TROUBLESHOOTING.
ARE SIGNATURES CORRECT ?
YES
NO
NO
IF INPUTS TO PREVIOUS CIRCUITS BAD, GO TO APPROPRIATE TREES. OTHERWISE REPAIR SUSPECTED PARTS AND RETURN TO START OF PER.MOD.-SYSTEM CHECK.
IF INPUTS TO PREVIOUS CIRCUITS ARE BAD, GO TO CPU TREES. OTHERWISE REPAIR SUSPECTED PARTS AND RETURN TO START OF PER.MOD.-SYSTEM CHECK.

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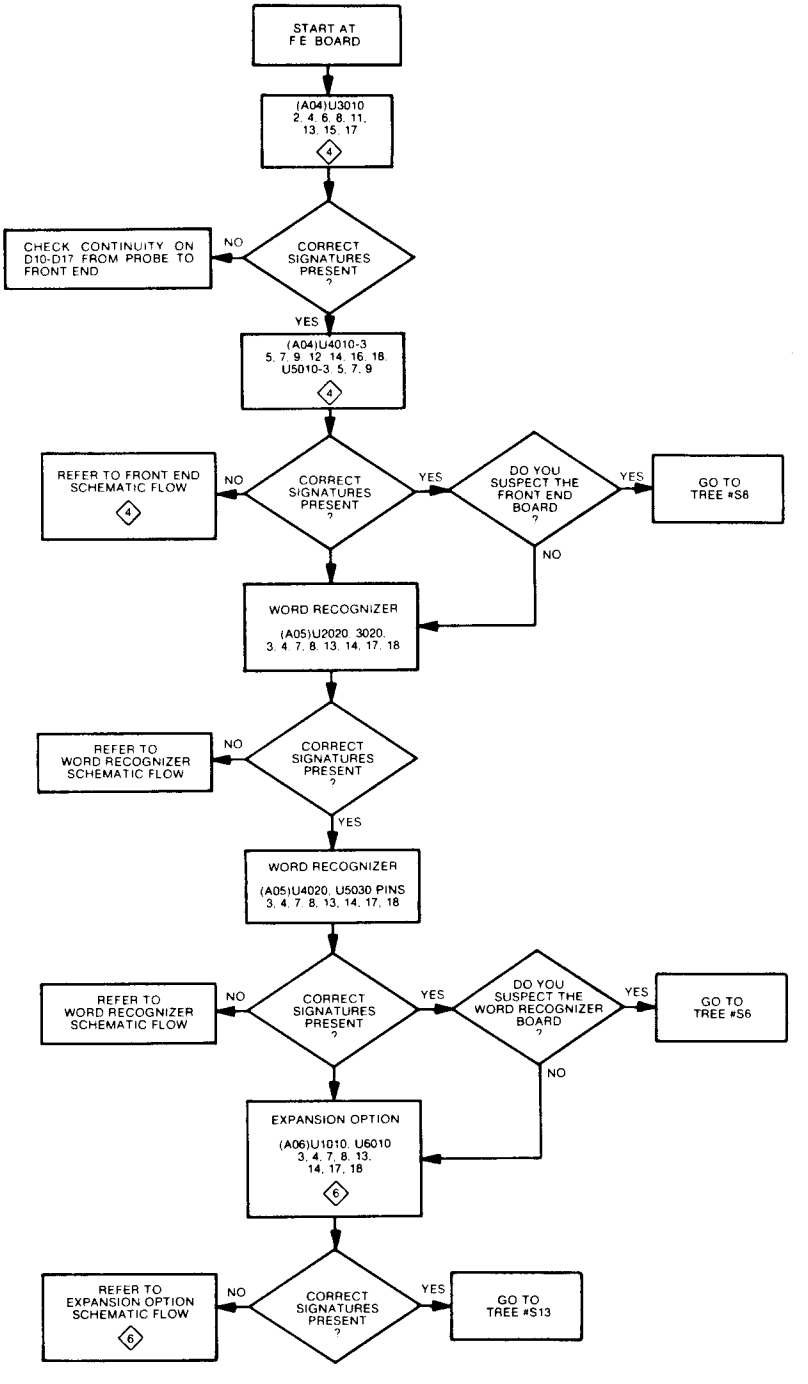
FRONT END, WORD RECOGNIZER, EXPANTION OPTION TREE S10



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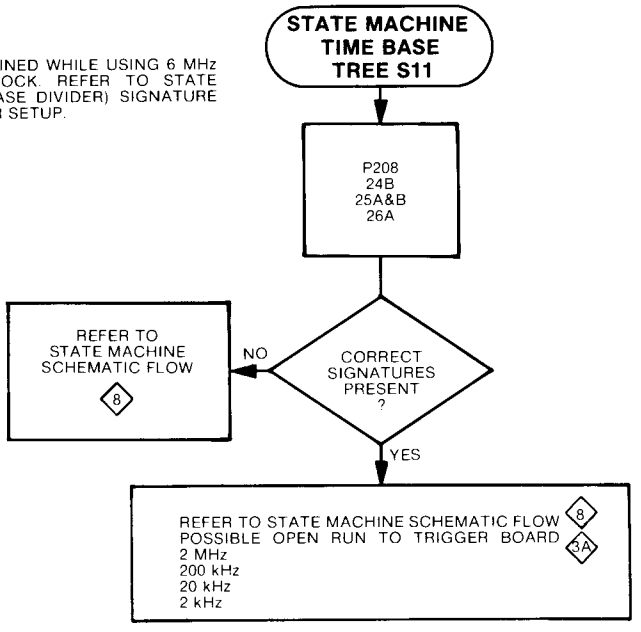
SIGNATURES OBTAINED WHILE USING 6 MHz FREE-RUNNING CLOCK. REFER TO STATE MACHINE (TIME BASE DIVIDER) SIGNATURE TABLE FOR PROPER SETUP.



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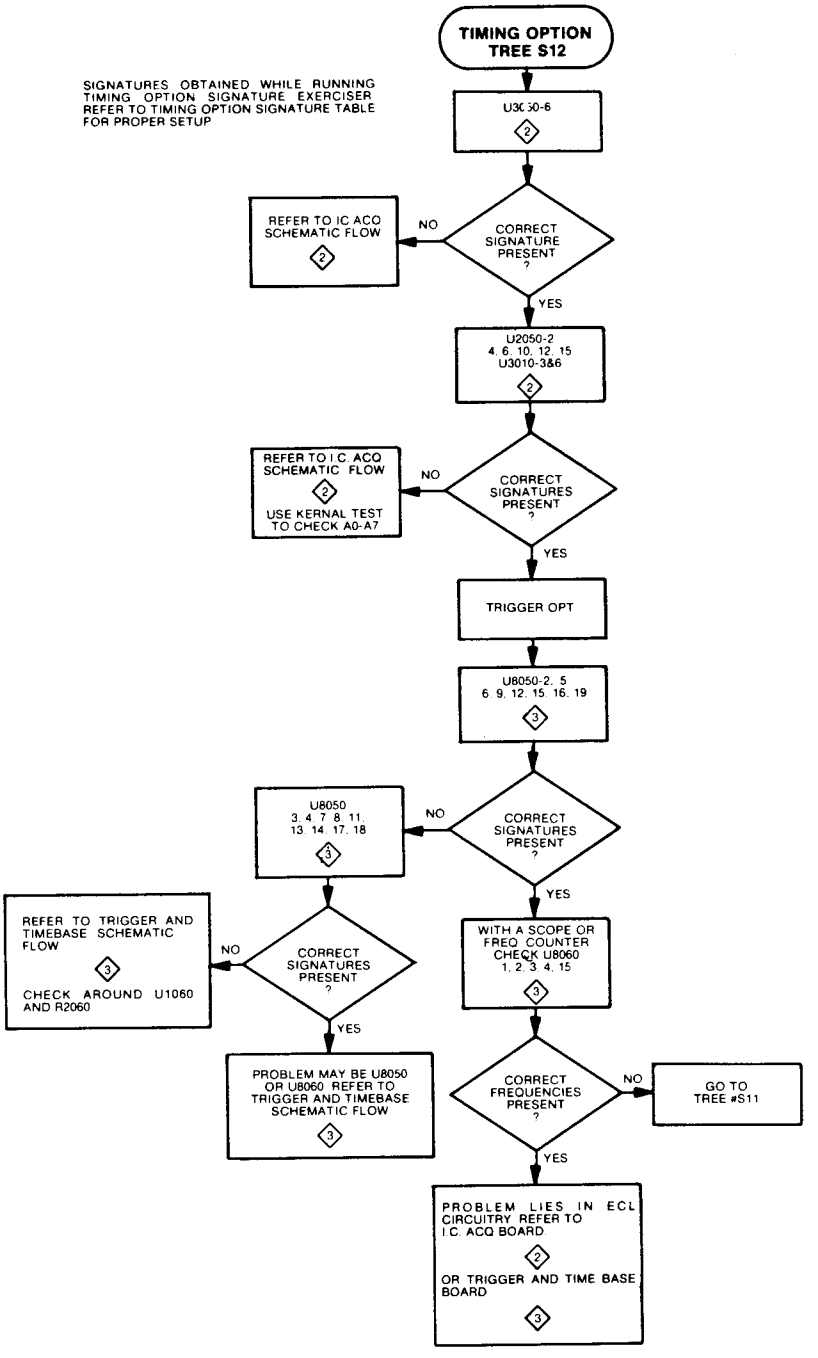
TIMING OPTION TREE S12
SIGNATURES OBTAINED WHILE RUNNING TIMING OPTION SIGNATURE EXERCISER REFER TO TIMING OPTION SIGNATURE TABLE FOR PROPER SETUP
U3050-6
2
CORRECT SIGNATURE PRESENT ?
NO
REFER TO IC ACQ SCHEMATIC FLOW
2
YES
U2050-2 4, 6, 10, 12, 15 U3010-3&6
2
CORRECT SIGNATURES PRESENT ?
NO
REFER TO I.C. ACQ SCHEMATIC FLOW
2
USE KERNAL TEST TO CHECK A0-A7
YES
TRIGGER OPT
U8050-2, 5 6, 9, 12, 15, 16, 19
3
CORRECT SIGNATURES PRESENT ?
NO
U8050 3, 4, 7, 8, 11, 13, 14, 17, 18
3
YES
WITH A SCOPE OR FREQ COUNTER CHECK U8060 1, 2, 3, 4, 15
3
CORRECT SIGNATURES PRESENT ?
NO
REFER TO TRIGGER AND TIMEBASE SCHEMATIC FLOW
3
CHECK AROUND U1060 AND R2060
YES
PROBLEM MAY BE U8050 OR U8060 REFER TO TRIGGER AND TIMEBASE SCHEMATIC FLOW
3
CORRECT FREQUENCIES PRESENT ?
NO
GO TO TREE #S11
YES
PROBLEM LIES IN ECL CIRCUITRY REFER TO I.C. ACQ BOARD
2
OR TRIGGER AND TIME BASE BOARD
3

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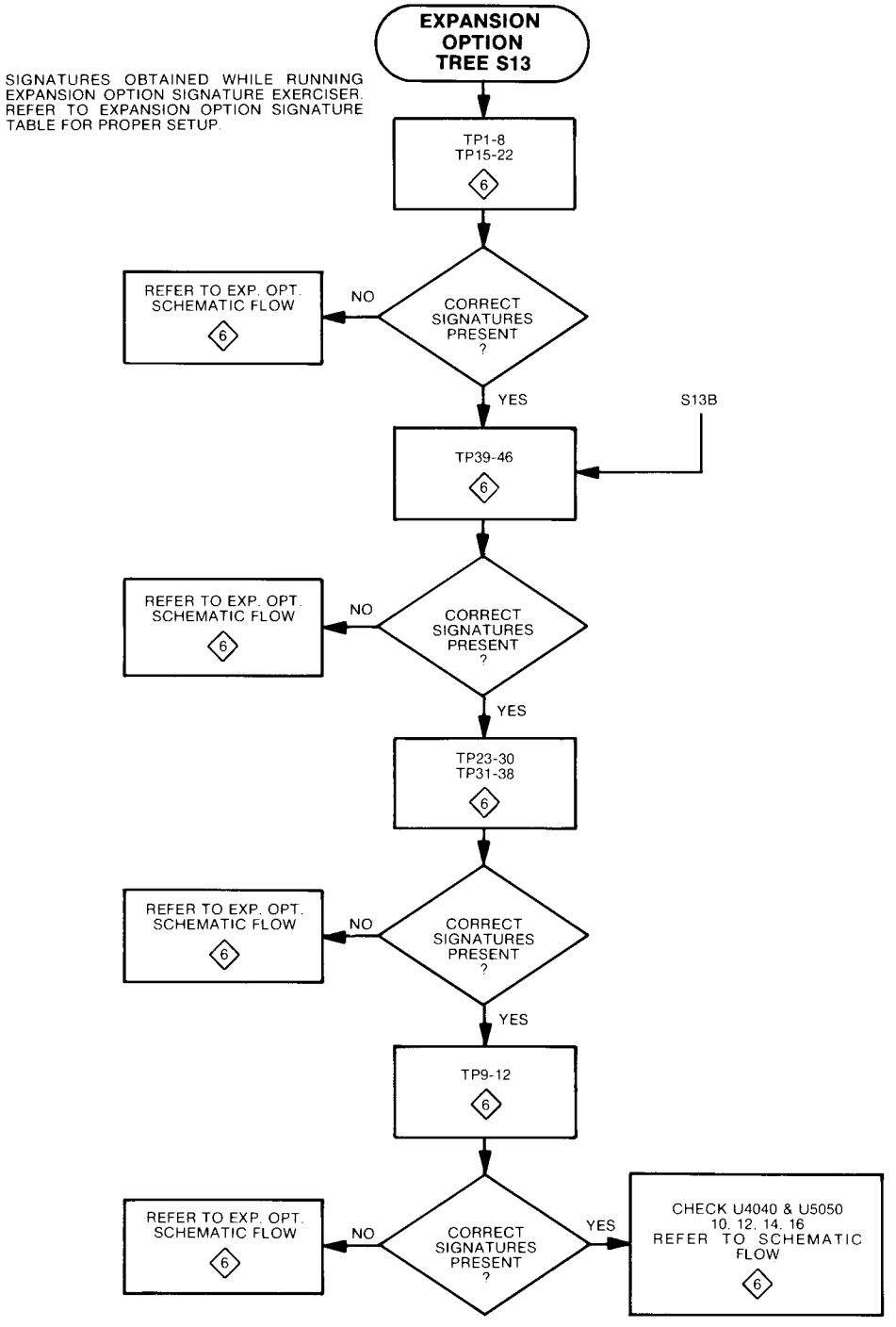
EXPANSION OPTION TREE S13
SIGNATURES OBTAINED WHILE RUNNING EXPANSION OPTION SIGNATURE EXERCISER. REFER TO EXPANSION OPTION SIGNATURE TABLE FOR PROPER SETUP.
TP1-8
TP15-22
6
CORRECT SIGNATURES PRESENT ?
NO
REFER TO EXP. OPT. SCHEMATIC FLOW
6
YES
S13B
TP39-46
6
CORRECT SIGNATURES PRESENT ?
NO
REFER TO EXP. OPT. SCHEMATIC FLOW
6
YES
TP23-30
TP31-38
6
CORRECT SIGNATURES PRESENT ?
NO
REFER TO EXP. OPT. SCHEMATIC FLOW
6
YES
TP9-12
6
CORRECT SIGNATURES PRESENT ?
NO
REFER TO EXP. OPT. SCHEMATIC FLOW
6
YES
CHECK U4040 & U5050 10, 12, 14, 16 REFER TO SCHEMATIC FLOW
6

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REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

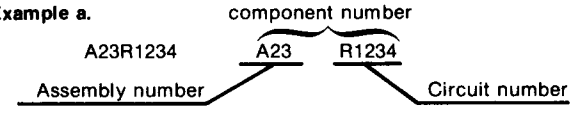
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

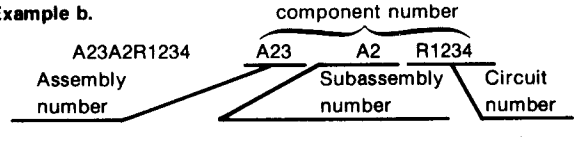
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01961	PULSE ENGINEERING, INC.	7250 CONVOY COURT	SAN DIEGO, CA 92111
02111	SPECTROL ELECTRONICS CORPORATION	17070 EAST GALE AVENUE	CITY OF INDUSTRY, CA 91745
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
03888	KDI PYROFILM CORPORATION	60 S JEFFERSON ROAD	WHIPPANY, NJ 07981
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867, 19TH AVE. SOUTH	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
13571	ELECTRONIC RESEARCH CO.	P O BOX 913	SHAWNEE MISSION, KS 66201
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
16546	GLOBE UNION INC. USCC/CENTRALAB ELECTRONICS DIV.	4561 COLORADO	LOS ANGELES, CA 90039
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
19396	ILLINOIS TOOL WORKS, INC. PAKTRON DIV.	900 FOLLIN LANE, SE	VIENNA, VA 22180
19701	ELECTRA-MIDLAND CORP., MEPCO ELECTRA INC.	P O BOX 760	MINERAL WELLS, TX 76067
24355	ANALOG DEVICES INC.	RT 1 INDUSTRIAL PK,P O BOX 280	NORWOOD, MA 02062
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
50558	ELECTRONIC CONCEPTS, INC.	526 INDUSTRIAL WAY WEST	EATONTOWN, NJ 07724
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
91929	HONEYWELL, INC., MICRO SWITCH DIV.	CHICAGO & SPRING STS.	FREEPORT, IL 61032

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01	670-5990-00			CKT BOARD ASSY:FRONT PANEL (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5990-00
A02	670-5985-00	B010100	B021084	CKT BOARD ASSY:I.C. AQUISITION (OPT 01,REFER TO MAINT SECT WHEN REPLACING)	80009	670-5985-00
A02	670-5985-01	B021085		CKT BOARD ASSY:I.C. AQUISITION (OPT 01,REFER TO MAINT SECT WHEN REPLACING)	80009	670-5985-01
A03	670-6038-00			CKT BOARD ASSY:TRIGGER (OPT 01,REFER TO MAINT SECT WHEN REPLACING)	80009	670-6038-00
A04	670-5989-00	B010100	B020599	CKT BOARD ASSY:FRONT END (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5989-00
A04	670-5989-01	B020600		CKT BOARD ASSY:FRONT END (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5989-01
A05	670-5988-00			CKT BOARD ASSY:WORD RECOGNIZER (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5988-00
A06	670-5987-00			CKT BOARD ASSY:EXPANSION OPTION (OPT 03,REFER TO MAINT SECT WHEN REPLACING)	80009	670-5987-00
A07	670-5995-00	B010100	B020884	CKT BOARD ASSY:AQUISITION MEMORY (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5995-00
A07	670-5995-01	B020885		CKT BOARD ASSY:AQUISITION MEMORY (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5995-01
A08	670-5986-00			CKT BOARD ASSY:STATE MACHINE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5986-00
A09	670-5984-00	B010100	B021564	CKT BOARD ASSY:CPU (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5984-00
A09	670-5984-01	B021565		CKT BOARD ASSY:CPU (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5984-01
A10	670-5983-00			CKT BOARD ASSY:DISPLAY (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5983-00
A11	670-5982-00	B010100	B021239	CKT BOARD ASSY:POWER SUPPLY (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5982-00
A11	670-5982-01	B021240		CKT BOARD ASSY:POWER SUPPLY (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5982-01
A12	670-5993-00			CKT BOARD ASSY:VERTICAL INTERFACE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5993-00
A13	670-5994-00			CKT BOARD ASSY:HORIZONTAL INTERFACE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5994-00
A14	670-5991-00	B010100	B021859	CKT BOARD ASSY:PROBE INTERFACE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5991-00
A14	670-5991-01	B021860		CKT BOARD ASSY:PROBE INTERFACE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5991-01
A15	670-5992-00			CKT BOARD ASSY:INTERFACE (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-5992-00
A16	670-6039-00			CKT BOARD ASSY:KEYBOARD (REFER TO MAINTENANCE SECT WHEN REPLACING)	80009	670-6039-00
A17	670-6148-00			CKT BOARD ASSY:P6451 INTERFACE (REFER TO MAINT SECT WHEN REPLACING)	80009	670-6148-00
A01	----- -----			CKT BOARD ASSY:FRONT PANEL		
A01C1013	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1026	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C1052	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A01C1057	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A01C1058	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A01C2047	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C3048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C5032	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A01C5033	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A01C5046	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A01C5047	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A01C6044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A01C6056	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A01C6058	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A01C7052	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A01C7054	281-0757-00			CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-C0G-100G
A01CR3010	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A01CR5042	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A01CR5043	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A01CR5044	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A01CR5045	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A01CR7052	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A01L1034	108-0520-00			COIL,RF:2.2UH (WOUND ON A 10 OHM RES)	80009	108-0520-00
A01L2032	108-0520-00			COIL,RF:2.2UH (WOUND ON A 10 OHM RES)	80009	108-0520-00
A01L3047	108-0520-00			COIL,RF:2.2UH (WOUND ON A 10 OHM RES)	80009	108-0520-00
A01L7057	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A01L7058	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A01Q6014	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A01Q6038	151-0254-00			TRANSISTOR:SILICON,NPN	03508	X38L3118
A01Q7046	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	01295	SKA5390
A01Q7048						
A01R1032	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A01R1042	311-1241-00			RES.,VAR,NONWIR:100K OHM,10%,0.5W	32997	3386X-T07-104
A01R1046	311-1917-00			RES.,VAR,NONWIR:TRMR,5K OHM,10%,0.5W	73138	72-198-0
A01R2033	321-0276-00			RES.,FXD,FILM:7.32K OHM,1%,0.125W	91637	MFF1816G73200F
A01R2041	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A01R2042	321-0603-07			RES.,FXD,FILM:15K OHM,0.1%,0.125W	91637	MFF1816C15001B
A01R2043	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A01R2045	321-0272-07			RES.,FXD,FILM:6.65K OHM,0.1%,0.125W	91637	MFF1816C66500B
A01R2046	321-0680-03			RES.,FXD,FILM:35.3K OHM,0.25%,0.125W	91637	MFF1816D35301C
A01R2049	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A01R3007	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R3008	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R3012	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A01R3013	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A01R5048	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A01R5052	321-0289-07			RES.,FXD,FILM:10K OHM,0.1%,0.125W	91637	MFF1816C10001B
A01R6026	321-0200-00			RES.,FXD,FILM:1.18K OHM,1%,0.125W	91637	MFF1816G11800F
A01R6027	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A01R6032	321-0102-00			RES.,FXD,FILM:113 OHM,1%,0.125W	91637	MFF1816G113R0F
A01R6033	321-0269-00			RES.,FXD,FILM:6.19K OHM,1%,0.125W	91637	MFF1816G61900F
A01R6034	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R6035	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A01R6046	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A01R7042	308-0720-00			RES.,FXD,WW:50 OHM,1%,3W	12697	RS2B-B50R00F
A01R7044	321-0030-00			RES.,FXD,FILM:20 OHM,1%,0.125W	91637	MFF1816G20R00F
A01R7045	321-0030-00			RES.,FXD,FILM:20 OHM,1%,0.125W	91637	MFF1816G20R00F
A01R7053	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A01R7054	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A01R7056	322-0481-00			RES.,FXD,FILM:1M OHM,1%,0.25W	75042	CEBT0-1004F
A01TP1053	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A01U2025	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05

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A01U2055	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A01U3045	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A01U3055	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A01U4045	156-1367-00			MICROCIRCUIT,LI:8 BIT BUFF,MULT D/A CONV	24355	AD11/297
A01U4055	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A01U5025	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10
A01U5035	156-0419-02			MICROCIRCUIT,DI:DUAL 4 INP NAND LINE DRVR	07263	74S140
A01U5055	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A01U7035	156-1324-00			MICROCIRCUIT,LI:COMPARATOR	27014	LM361N/A+
A01VR1034	152-0456-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	1N827
A01VR7043	152-0359-00			SEMICOND DEVICE:ZENER,0.25W,5%,9V	80009	152-0359-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A02	----- -----			CKT BOARD ASSY:I.C. ACQUISITION		
A02C1023	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C1034	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	272C13
A02C1057	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	272C13
A02C1058	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A02C2011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2021	281-0562-00			CAP.,FXD,CER DI:39PF,10%,500V	59660	301-000U2J0390K
A02C2031	281-0785-00	XB021200		CAP.,FXD,CER DI:68PF,10%,100V	72982	8035D2AADC0G680K
A02C2028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2033	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2034	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C2048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C3021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C3033	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C4048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C5021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C5058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C6021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C6031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C7011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C7021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C7041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A02C7045	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A02CR1030	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A02CR1042	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A02CR1043	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A02CR1052	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A02Q1014	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1015	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1016	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1017	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1018	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1019	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1021	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1022	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q1035	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1036	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1037	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1042	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1043	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1046	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A02Q1047	151-0472-00			TRANSISTOR:SILICON,NPN	80009	151-0472-00
A02Q1054	151-0472-00			TRANSISTOR:SILICON,NPN	80009	151-0472-00
A02Q1055	151-0402-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	80009	151-0402-00
A02Q1056	151-0402-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	80009	151-0402-00
A02Q2022	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A02Q3043	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A02Q3045	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A02R1011	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A02R1012	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A02R1013	307-0674-00			RES,NTWK,FXD FI:9,430 OHM,2%,1.25W	01121	210A431
A02R1031	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A02R1032	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A02R1033	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A02R1038	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A02R1041	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715

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A02R1044	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A02R1045	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A02R1048	321-0122-00			RES.,FXD,FILM:182 OHM,1%,0.125W	91637	MFF1816G182R0F
A02R1049	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	91637	MFF1816G24300F
A02R1050	321-0120-00			RES.,FXD,FILM:174 OHM,1%,0.125W	91637	MFF1816G174R0F
A02R1051	321-0152-00			RES.,FXD,FILM:374 OHM,1%,0.125W	91637	MFF1816G374R0F
A02R1053	321-0080-00			RES.,FXD,FILM:66.5 OHM,1%,0.125W	91637	MFF1816G66R50F
A02R2012	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A02R2013	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A02R2014	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A02R2024	307-0675-00			RES NTWK,FXD FI:9,1K OHM,2%,1.25W	01121	210A102
A02R2031	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A02R2032	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A02R2048	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A02R3022	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A02R3024	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A02R3045	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A02R3047	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A02R3334	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A02R3335	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
A02R5022	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A02R5041	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A02R6022	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A02R6041	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A02R7022	307-0486-00			RES,NTWK,THK FI:100 OHM,20%,1.125W	91637	MSP10A01-101J
A02R7031	307-0640-00			RES NTWK,FXD FI:9,50 OHM,5%,0.125W	32997	4308R101-151J
A02R7044	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	80009	307-0108-00
A02R7051	307-0640-00			RES NTWK,FXD FI:9,50 OHM,5%,0.125W	32997	4308R101-151J
A02U1020	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A02U2010	156-0637-01			MICROCIRCUIT,DI:DUAL 4 TO 1 MUX	80009	156-0637-01
A02U2020	156-1021-01			MICROCIRCUIT,DI:HEX & GATE,SCRN	80009	156-1021-01
A02U2040	156-1038-01			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A02U2050	156-0330-02			MICROCIRCUIT,DI:HEX BUFFER	04713	MC14050BCLD
A02U3010	156-0577-02			MICROCIRCUIT,DI:QUAD 2-INP AND GATE,SEL	27014	DM74C08
A02U3020	156-1297-00			MICROCIRCUIT,DI:256 X 4 STATIC RAM	0001G	MB7072EC
A02U3030	156-1038-01			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A02U3040	156-0759-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	SC22689P103
A02U3050	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A02U4010	156-0682-02			MICROCIRCUIT,DI:HEX D FLIP-FLOP,SEL	27014	MM74C174
A02U4030	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U4040	156-0458-01			MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	SC22689P104
A02U4050	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U5010	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A02U5020	156-1297-00			MICROCIRCUIT,DI:256 X 4 STATIC RAM	0001G	MB7072EC
A02U5030	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U5050	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U6010	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A02U6020	156-1297-00			MICROCIRCUIT,DI:256 X 4 STATIC RAM	0001G	MB7072EC
A02U6030	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U6040	119-0775-01			DELAY LINE,ELEC:12.5NS,100 OHM,24 PIN DBL	01961	PE 22297
A02U6050	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U7010	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A02U7020	156-1297-00			MICROCIRCUIT,DI:256 X 4 STATIC RAM	0001G	MB7072EC
A02U7030	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00
A02U7050	155-0215-00			MICROCIRCUIT,DI:LOGIC ANALYZER INPUT,16 DIP	80009	155-0215-00

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A03	----- -----			CKT BOARD ASSY:TRIGGER		
A03C1021	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	272C13
A03C1045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C1067	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A03C2025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2043	281-0816-00	XB010385	B020833	CAP.,FXD,CER DI:82PF,5%,100V	20932	201-E0-100AT820J
A03C2043	281-0792-00	B020834		CAP.,FXD,CER DI:82PF,10%,100V	72982	8035D2AADC0G820K
A03C2046	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C2067	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C3020	281-0508-00			CAP.,FXD,CER DI:12PF,+/-0.6PF,500V	59660	301-000C0G0120J
A03C3043	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C3050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C3055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C4017	283-0108-00			CAP.,FXD,CER DI:220PF,10%,200V	56289	272C13
A03C4025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C5017	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C5055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C6063	281-0634-00	B010100	B010584	CAP.,FXD,CER DI:10PF,+/-0.25PF,500V	59660	374 011 C0G0100C
A03C6063	281-0578-00	B010585		CAP.,FXD,CER DI:18PF,5%,500V	59660	301-050C0G0180J
A03C6067	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	91418	SP103Z151-4R9
A03C7015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C7043	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	273C20
A03C7065	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A03C8017	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8036	281-0634-00			CAP.,FXD,CER DI:10PF,+/-0.25PF,500V	59660	374 011 C0G0100C
A03C8041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8042	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8043	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8054	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8056	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03C8061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A03CR1010	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A03CR2028	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A03CR3019	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A03CR5060	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A03CR7042	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A03CR7044	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A03L6061	108-0182-00			COIL,RF:0.3UH	80009	108-0182-00
A03Q1022	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q1025	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q1026	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q1027	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A03Q2010	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q2013	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q2015	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q2017	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q2035	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A03Q6063	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A03Q6064	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A03Q7041	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A03Q7042	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K

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A03Q7046	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A03Q8069	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A03R1011	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A03R1012	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A03R1013	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A03R1014	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
A03R1017	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A03R1030	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A03R1033	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A03R1035	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A03R1037	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R2027	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A03R2029	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R2033	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R2037	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A03R2060	307-0422-00			RES.,FXD,FILM:15 RES. NETWORK	73138	898-1-R2.4K
A03R3011	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A03R3013	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A03R3015	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A03R3017	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A03R3033	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R3035	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R3037	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R3040	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A03R3047	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R4033	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R4035	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R4043	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R4045	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R5020	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A03R5031	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A03R5033	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R5035	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R5043	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R5045	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A03R5047	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R5060	307-0422-00			RES.,FXD,FILM:15 RES. NETWORK	73138	898-1-R2.4K
A03R6020	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	80009	307-0108-00
A03R6035	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A03R6037	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R6061	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A03R6065	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A03R6067	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A03R6068	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R7036	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A03R7040	307-0488-00			RES,NTWK,FXD,FI:100 OHM,20%,0.75W	01121	206A101
A03R7041	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R7046	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A03R7047	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A03R7050	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A03R8010	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R8020	307-0489-00			RES,NTWK,FXD,FI:100 OHM,20%,1W	32997	4308R-101-101
A03R8031	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A03R8039	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A03R8063	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A03R8065	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A03U1030	156-1038-01			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01

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A03U1040	156-0330-02			MICROCIRCUIT,DI:HEX BUFFER	04713	MC14050BCLD
A03U1050	156-0627-02			MICROCIRCUIT,DI:SYN 4-B UP/DN BIN,CNTR,SEL	80009	156-0627-02
A03U1060	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A03U2020	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	SC22689L102
A03U2040	156-0412-02			MICROCIRCUIT,DI:SYN 4 BIT UP/DOWN CNTR	01295	SN74LS193N3
A03U2050	156-0627-02			MICROCIRCUIT,DI:SYN 4-B UP/DN BIN,CNTR,SEL	80009	156-0627-02
A03U3020	156-0682-02			MICROCIRCUIT,DI:HEX D FLIP-FLOP,SEL	27014	MM74C174
A03U3030	156-0230-02			MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	80009	156-0230-02
A03U3040	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A03U3050	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A03U3060	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02
A03U4020	156-0458-01			MICROCIRCUIT,DI:QUAD AND GATE 2 INP,SCRN	04713	SC22689P104
A03U4030	156-0688-01			MICROCIRCUIT,DI:DUAL J-K MASTER SLAVE FF	04713	SC22689L135
A03U4040	156-0688-01			MICROCIRCUIT,DI:DUAL J-K MASTER SLAVE FF	04713	SC22689L135
A03U4050	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A03U5020	156-0205-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	04713	SC22689L102
A03U5030	156-1214-01			MICROCIRCUIT,DI:DUAL 2 WIDE,3 INPUT OR GATE	04713	SC22689P118
A03U5040	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A03U5050	156-0282-02			MICROCIRCUIT,DI:DUAL 4-INPUT GATE	52648	SP1660BDG
A03U6020	156-0230-02			MICROCIRCUIT,DI:DUAL D-TYPE M/S,FF,SCRN	80009	156-0230-02
A03U6030	156-0687-01			MICROCIRCUIT,DI:QUAD EXCL OR CMPTR	04713	MC10113PI
A03U7020	156-0759-01	B010100	B010529	MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE,CHK	80009	156-0759-01
A03U7020	156-0759-02	B010530		MICROCIRCUIT,DI:QUAD 2-INP OR GATE,SCRN	04713	SC22689P103
A03U7050	156-0642-01			MICROCIRCUIT,DI:BI QUINARY CNTR,SCRN	80009	156-0642-01
A03U7060	156-0640-02			MICROCIRCUIT,DI:8 LINE MULTIPLEXER	80009	156-0640-02
A03U8020	156-1038-01			MICROCIRCUIT,DI:4 BIT BINARY COUNTER	80009	156-1038-01
A03U8030	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A03U8040	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A03U8050	156-1327-00			MICROCIRCUIT,DI:3 STATE OCTAL D FF,SCRN	27014	MM74C374
A03U8060	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A03Y6060	158-0106-00			XTAL UNIT,QTZ:100MHZ,+/-0.0025%,SERIES	13571	TEK158-0106-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A04	----- -----			CKT BOARD ASSY:FRONT END		
A04C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C1055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C1056	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A04C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C2057	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C3010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C3051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C4010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C4054	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C5040	283-0347-00	B010100	B020599	CAP.,FXD,CER DI:68PF,5%,100V	72982	8121A108P3K680J
A04C5040	281-0549-00	B020600		CAP.,FXD,CER DI:68PF,10%,500V	59660	301-000U2J0680K
A04C5056	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A04C5057	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	GC70-1C103K
A04C6010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C6011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C6032	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A04C6049	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A04C6050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A04C6054	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A04C6056	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A04CR6045	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A04L6055	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A04L6057	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A04Q6041	151-0438-00			TRANSISTOR:SILICON,PNP,SEL FROM SPS6927	80009	151-0438-00
A04Q6043	151-0225-00			TRANSISTOR:SILICON,NPN	07263	S39291
A04R1010	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A04R1040	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A04R3010	307-0721-00	XB020600		RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A04R3011	315-0680-00	XB020600		RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A04R3052	315-0102-00	B010100	B020599	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A04R3052	315-0301-00	B020600		RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A04R3054	315-0102-00	B010100	B020599	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A04R3054	315-0301-00	B020600		RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A04R4010	307-0721-00	XB020600		RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A04R4040	317-0101-00	XB020600		RES.,FXD,CMPSN:100 OHM,5%,0.125W	01121	BB1015
A04R4052	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A04R4053	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A04R4055	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A04R4056	315-0304-00			RES.,FXD,CMPSN:300K OHM,5%,0.25W	01121	CB3045
A04R4057	315-0304-00			RES.,FXD,CMPSN:300K OHM,5%,0.25W	01121	CB3045
A04R5042	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A04R5052	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A04R5053	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A04R5054	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A04R5055	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	01121	CB1135
A04R6010	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A04R6020	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A04R6030	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	01121	CB1135
A04R6031	321-0183-00			RES.,FXD,FILM:787 OHM,1%,0.125W	91637	MFF1816G787R0F
A04R6032	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A04R6033	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A04R6040	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A04R6041	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A04R6042	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A04R6043	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A04R6044	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A04R6045	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A04R6049	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A04R6050	321-0128-00			RES.,FXD,FILM:210 OHM,1%,0.125W	91637	MFF1816G210R0F
A04R6051	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A04R6052	321-0128-00			RES.,FXD,FILM:210 OHM,1%,0.125W	91637	MFF1816G210R0F
A04R6053	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A04U1010	156-0916-02	B010100	B020599	MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A04U1010	156-1065-01	B020600		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A04U1020	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A04U1040	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A04U1050	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A04U2010	156-0956-02	B010100	B020599	MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A04U2010	156-1065-01	B020600		MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A04U2020	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A04U2030	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U2040	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U2050	156-0703-02	B010100	B020599	MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A04U2050	156-1285-00	B020600		MICROCIRCUIT,DI:4-2-3-2 INPUT & OR GATE	01295	SN74S65
A04U2055	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A04U3010	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A04U3020	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U3030	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U3040	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U3050	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U4010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A04U4020	156-1285-00			MICROCIRCUIT,DI:4-2-3-2 INP & OR INV GATE	01295	SN74S65N3
A04U4030	156-0320-03			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S11NP3
A04U4040	156-1286-00			MICROCIRCUIT,DI:QUAD 2-INP & GATES W/OC	01295	SN74S09
A04U4050	156-0690-03	XB020600		MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,BURN IN	01295	SN74S02
A04U5010	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	18324	CD2064N
A04U5020	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A04U5030	156-1328-00	B010100	B020599	MICROIRCUIT,DI:4 BIT SHIFT REGISTER	18324	82S70(NB OR FB)
A04U5030	156-0744-01	B020600		MICROCIRCUIT,DI:4 BIT BIDIR UNIV SR,CHK	80009	156-0744-01
A04U5040	156-1335-00			MICROCIRCUIT,DI:DUAL RETRIG RESET MONO MV	07263	96LS02
A04U5050	156-0118-02			MICROCIRCUIT,DI:DUAL J-K FLIP-FLOP	80009	156-0118-02
A04U6010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A04U6020	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A04U6030	156-0731-02			MICROCIRCUIT,DI:DUAL J-K FF W/PRESET & CLR	01295	SN74LS76N3
A04U6040	156-0534-01			MICROCIRCUIT,LI:DUAL DIFF AMPL	80009	156-0534-01
A04U6050	119-1169-00			DELAY LINE:DUAL.30NS,120 OHM,16 DIP	01961	PE22376
A04VR6040	153-0071-00			SEMICOND DEVICE:ZENER,MATCHED PAIR	80009	153-0071-00
A04VR6041						
A04VR6049	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A05	----- -----			CKT BOARD ASSY:WORD RECOGNIZER		
A05C1015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C1032	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C1041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C1050	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A05C3021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C3041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C4008	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C4031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C5055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C6021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C7051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C8011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05C8015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A05R5041	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9) RES	91637	MSP10A01-472M
A05R5051	307-0651-00			RES NTWK,FXD FI:5,3.3K OHM,5%,0.15W	01121	206A332
A05R8020	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A05U1010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A05U1040	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A05U2010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A05U2020	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A05U2040	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A05U3010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A05U3020	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A05U3040	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A05U4010	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A05U4020	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A05U4030	156-0418-01			MICROCIRCUIT,DI:8 INPUT NAND GATE,SCRN	01295	SN74S30
A05U4040	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A05U5020	156-0418-01			MICROCIRCUIT,DI:8 INPUT NAND GATE,SCRN	01295	SN74S30
A05U5030	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A05U5040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A05U5050	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A05U6020	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A05U6030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A04U6050	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A05U7040	156-0304-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74S20
A05U7050	156-0320-03			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S11NP3
A05U8010	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A06	----- -----			CKT BOARD ASSY:EXPANSION OPTION		
A06C1011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C1041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C1051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C1059	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A06C2021	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C3041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C4011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C4019	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C4039	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C4041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C6011	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06C6051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A06U1010	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02
A06U1030	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A06U1040	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A06U1050	156-0043-03			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	01295	SN7402
A06U2020	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A06U2030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U2040	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U3010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A06U3020	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A06U3030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U3040	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U3050	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A06U4010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244
A06U4020	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A06U4040	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U4050	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A06U5020	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A06U5040	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A06U5050	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A06U6010	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A07	----- -----			CKT BOARD ASSY:ACQUISITION MEMORY		
A07C1049	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A07C1012	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C2015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C2032	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C3015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C3035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C4035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C5015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C5035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C6015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C6035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C7015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07C7035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A07R1016	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A07R6036	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A07R6048	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A07R7031	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A07U1010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A07U1020	156-0739-02			MICROCIRCUIT,DI:QUAD 2 INP OR GATE,SCRN	01295	SN74S32
A07U1025	156-0043-03			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE,SCRN	01295	SN7402
A07U1030	156-0321-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S10
A07U1040	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A07U2010	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A07U2020	156-1326-00			MICROCIRCUIT,DI:QUAD D TYPE FF,SCRN	80009	156-1326-00
A07U2030	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A07U2040	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A07U3010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A07U3020	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U3030	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A07U3040	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A07U4010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A07U4030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U4040	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A07U5010	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A07U5020	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U5030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U5040	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A07U6010	156-0376-01			MICROCIRCUIT,DI:4 BIT PRL I/OSR,BURN-IN	01295	SN74LS195A
A07U6020	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U6030	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U6040	156-1061-02			MICROCIRCUIT,DI:DUAL JK FF,SCREENED	07263	SL81712
A07U7010	156-0180-04			MICROCIRCUIT,DI:QUAD 2 INP NAND GATE	01295	SN74S00NP3
A07U7020	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A07U7040	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A08	----- -----			CKT BOARD ASSY:STATE MACHINE		
A08C1018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C1048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C1068	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A08C2038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C3048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C3058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C4008	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C4018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C4028	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C4038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C5068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C6018	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	51642	150-050-NP0-101J
A08C6038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C7018	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C7038	283-0256-00			CAP.,FXD,CER DI:130PF,5%,100V	51642	200-100N1500131J
A08C7045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C7058	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A08C7060	283-0182-00			CAP.,FXD,CER DI:51PF,5%,400V	72982	8121N400A510J
A08R1028	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R1058	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A08R2018	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A08R2028	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R3008	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R3028	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R3068	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A08R5008	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R5028	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R6028	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A08R6048	317-0680-00	XB010410		RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A08R6068	317-0680-00	XB010410		RES.,FXD,CMPSN:68 OHM,5%,0.125W	01121	BB6805
A08R7008	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A08R7020	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A08R7028	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A08R7060	315-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.25W	01121	CB3305
A08R7068	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A08TP11	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A08U1010	156-0459-02			MICROCIRCUIT,DI:QUAD 2 INPUT & GATE,BURN	01295	SN74S08
A08U1020	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A08U1030	156-1061-02			MICROCIRCUIT,DI:DUAL JK FF,SCREENED	07263	SL81712
A08U1040	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A08U1050	156-1385-00			MICROCIRCUIT,DI:PROGRAMMABLE TIMER/COUNTER	34335	AM2942DCB2
A08U1060	156-1357-00			MICROCIRCUIT,DI:256 X 1 STATIC RAM 3 STATE	80009	156-1357-00
A08U2010	156-1258-00			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A08U2020	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A08U2030	156-1061-02			MICROCIRCUIT,DI:DUAL JK FF,SCREENED	07263	SL81712
A08U2040	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153
A08U2050	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A08U2060	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A08U3010	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A08U3020	156-1286-00			MICROCIRCUIT,DI:QUAD 2-INP & GATES W/OC	01295	SN74S09
A08U3030	156-1061-02			MICROCIRCUIT,DI:DUAL JK FF,SCREENED	07263	SL81712
A08U3040	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153
A08U3050	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A08U4010	156-0703-02			MICROCIRCUIT,DI:4-2-3-2 INPUT& OR GATE	07263	74S64
A08U4020	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A08U4030	156-0690-01			MICROCIRCUIT,DI:2-INP NOR GATE,CHK	80009	156-0690-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A08U4040	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A08U4050	156-1385-00			MICROCIRCUIT,DI:PROGRAMMABLE TIMER/COUNTER	34335	AM2942DCB2
A08U4060	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A08U5010	156-0323-02			MICROCIRCUIT,DI:HEX INVERTER,BURN-IN	01295	SN74S04
A08U5020	156-0403-02			MICROCIRCUIT,DI:HEX INVERTER,SCRN	01295	SN74S05
A08U5030	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A08U5040	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A08U5050	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A08U5060	156-1293-01			MICROCIRCUIT,DI:256 X 4 STATIC RAM	80009	156-1293-01
A08U6010	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A08U6020	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A08U6030	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG	01295	SN74LS113NP3
A08U6040	156-1521-00			MICROCIRCUIT,DI:4 TO 1 DATA SEL/MULTIPLEXER	07263	74LS352
A08U6050	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A08U6060	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A08U7010	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A08U7015	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	80009	156-0718-03
A08U7020	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A08U7030	156-0752-01			MICROCIRCUIT,DI:DUAL BCD UP COUNTER,SCRN	04713	MC14518BCLD
A08U7040	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10
A08U7050	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A08U7060	156-1046-02			MICROCIRCUIT,DI:OCTAL D TYPE EDGE TRIG FF	80009	156-1046-02

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A09	----- -----			CKT BOARD ASSY:CPU		
A09C1001	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A09C1014	283-0636-00			CAP.,FXD,MICA D:36PF,1.4%,100V	00853	D155E360G0
A09C1016	283-0197-00			CAP.,FXD,CER DI:470PF,5%,100V	72982	8121N075C0G0471J
A09C1018	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	72982	855-535U2J101J
A09C1030	285-1134-00			CAP.,FXD,PLSTC:0.1UF,0.5%,100V	50558	MH12D104J
A09C1044	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C1054	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C1064	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C1068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C1081	283-0194-00			CAP.,FXD,CER DI:4.7UF,20%,50V	56289	275C4
A09C2039	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4008	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4050	281-0814-00	XB021565		CAP.,FXD,CER DI:100PF,10%,100V	04222	GC70-1-A101K
A09C4051	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4055	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4068	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09C4082	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A09CR1001	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A09CR1002	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A09CR1021	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A09Q1001	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A09Q1025	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A09Q1030	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A09Q1037	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A09Q3073	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A09R1001	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A09R1002	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A09R1005	321-0773-03			RES.,FXD,FILM:400 OHM,0.25%,0.125W	91637	MFF1816D400R0C
A09R1009	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A09R1011	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A09R1012	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A09R1014	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A09R1016	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A09R1020	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A09R1023	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A09R1024	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A09R1025	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A09R1034	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A09R1035	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A09R1037	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A09R3070	307-1137-00			RES NTWK,FXD,FI:8.5M OHM,50%,0.125W	03888	A3UT17
A09R3073	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A09R3076	315-0472-00	XB010410		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A09R4050	315-0680-00	XB021565		RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A09R4054	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A09R4059	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A09R4061	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A09R4073	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A09R4082	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A09S1001	260-0612-00			SWITCH,SENS:SPDT,7A,230VAC OR 115 VAC	91929	1SX1-T
A09TP41	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A09TP42	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A09TP43	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A09TP49	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A09U1030	156-0402-00			MICROCIRCUIT,LI:TIMER	27014	LM555CN

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A09U1040	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1045	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1050	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1055	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1060	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1065	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1070	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U1080	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A09U2040	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2045	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2050	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2055	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2060	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2065	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2070	156-1359-01			MICROCIRCUIT,DI:1024 X 4 RAM W/3 STATE	80009	156-1359-01
A09U2080	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A09U3010	160-0358-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASK ROM	80009	160-0358-00
A09U3020	160-0359-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASK ROM	80009	160-0359-00
A09U3030	160-0360-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASK ROM	80009	160-0360-00
A09U3050	156-1088-00			MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	80009	156-1088-00
A09U3065	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A09U3080	156-0768-00			MICROCIRCUIT,DI:BIDIRECT UNIVSR	01295	SN74LS194AN
A09U4010	160-0361-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASK ROM	80009	160-0361-00
A09U4020	160-0818-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASKED ROM	80009	160-0818-00
A09U4030	160-0819-00			MICROCIRCUIT,DI:8192 X 8 CUSTOM MASKED ROM	80009	160-0819-00
A09U4040	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A09U4045	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A09U4050	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10
A09U4055	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A09U4065	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A09U4070	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A09U4075	156-1277-00			MICROCIRCUIT,DI:3 STATE OCTAL BFR	27014	DM81LS95
A09U4080	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A09VR1007	152-0278-00			SEMICOND DEVICE:ZENER,0.4W,3V,5%	04713	SZG35009K20
A09Y1030	158-0185-00			XTAL UNIT,QTZ:6MHZ,0.015%,PAR	75378	MP060

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	----- -----			CKT BOARD ASSY:DISPLAY		
A10C1016	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	8035D2AADX5P151K
A10C1020	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	8035D9AADC0G270M
A10C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C1040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C1050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C1065	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	56289	502D223
A10C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C2050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C3010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C3039	290-0523-00	XB010410		CAP.,FXD,ELCTLT:2.2UF,20%,20V	56289	196D225X0020HA1
A10C3040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C3050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C4010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C4020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C4030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C4040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C4050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A10C5011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5012	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5013	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5022	285-1142-00			CAP.,FXD,PLSTC:0.01UF,1%,200VDC	19396	103F02PP580
A10C5031	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A10C5032	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5033	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A10C5034	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5040	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C5048	281-0809-00			CAP.,FXD,CER DI:200PF,5%,100V	72982	8013T2ADDC1G201J
A10C5051	283-0204-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N061Z5U0103M
A10C5052	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A10C6021	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6022	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6023	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6024	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6031	285-1142-00			CAP.,FXD,PLSTC:0.01UF,1%,200VDC	19396	103F02PP580
A10C6050	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6052	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A10C6053	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6054	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A10C6055	290-0770-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	502D230
A10C6056	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A10CR6021	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10L5051	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A10L5052	108-0458-00			COIL,RF:FIXED,76UH	80009	108-0458-00
A10L6056	108-0458-00			COIL,RF:FIXED,76UH	80009	108-0458-00
A10Q1010	151-0190-06			TRANSISTOR:SILICON,NPN	80009	151-0190-06
A10Q5017	151-0453-00			TRANSISTOR:SILICON,PNP	80009	151-0453-00
A10Q5019	151-0453-00			TRANSISTOR:SILICON,PNP	80009	151-0453-00
A10Q5021	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A10Q5031	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10Q5032	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10Q5041	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A10Q5042	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A10Q5043	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A10Q5044	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10Q5051	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10Q5052	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10Q6011	151-0424-00			TRANSISTOR:SILICON,NPN	04713	SPS8246
A10Q6021	151-0453-00			TRANSISTOR:SILICON,PNP	80009	151-0453-00
A10Q6022	151-0453-00			TRANSISTOR:SILICON,PNP	80009	151-0453-00
A10Q6031	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS6521	04713	SPS8801
A10Q6032	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10Q6033	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A10R1010	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R1012	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R1017	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A10R2020	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A10R3052	315-0182-00	XB010410		RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A10R4040	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A10R5011	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A10R5012	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A10R5013	311-1916-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-197-0
A10R5014	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A10R5015	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A10R5016	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R5021	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A10R5022	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R5023	321-0389-00			RES.,FXD,FILM:110K OHM,1%,0.125W	91637	MFF1816G11002F
A10R5024	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A10R5025	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A10R5026	315-0623-00			RES.,FXD,CMPSN:62K OHM,5%,0.25W	01121	CB6235
A10R5031	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R5032	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R5033	321-0661-00			RES.,FXD,FILM:600 OHM,1%,0.125W	91637	MFF1816G600R0F
A10R5034	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A10R5035	321-0247-00			RES.,FXD,FILM:3.65K OHM,1%,0.125W	91637	MFF1816G36500F
A10R5036	321-0661-00			RES.,FXD,FILM:600 OHM,1%,0.125W	91637	MFF1816G600R0F
A10R5037	321-0254-00			RES.,FXD,FILM:4.32K OHM,1%,0.125W	91637	MFF1816G43200F
A10R5038	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A10R5039	321-0254-00			RES.,FXD,FILM:4.32K OHM,1%,0.125W	91637	MFF1816G43200F
A10R5042	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R5043	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R5044	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R5045	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R5046	321-0247-00			RES.,FXD,FILM:3.65K OHM,1%,0.125W	91637	MFF1816G36500F
A10R5047	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A10R5048	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A10R5051	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A10R5052	321-0273-00			RES.,FXD,FILM:6.81K OHM,1%,0.125W	91637	MFF1816G68100F
A10R5053	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R5054	321-0181-00			RES.,FXD,FILM:750 OHM,1%,0.125W	91637	MFF1816G750R0F
A10R6011	311-1240-00			RES.,VAR,NONWIR:25K OHM,10%,0.50W	73138	72-30-0
A10R6012	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R6013	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R6021	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A10R6022	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R6023	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A10R6025	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R6031	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
A10R6032	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R6034	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A10R6035	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10R6036	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R6037	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R6038	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A10R6041	321-0217-00			RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	MFF1816G17800F
A10R6042	321-0180-00			RES.,FXD,FILM:732 OHM,1%,0.125W	91637	MFF1816G732R0F
A10R6043	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A10R6044	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A10R6045	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A10R6046	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A10R6047	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A10R6048	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A10R6049	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A10R6051	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A10R6052	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A10R6053	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R6055	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A10U1010	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A10U1020	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A10U1030	156-1313-00			MICROCIRCUIT,DI:8 BIT SHIFT REGISTER,SCRN	01295	SN741S166
A10U1040	160-0362-00			MICROCIRCUIT,DI:2048 X 8 CUSTOM MASK	80009	160-0362-00
A10U1050	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A10U2010	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A10U2020	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A10U2030	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	01295	SN74LS393
A10U2050	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A10U3010	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A10U3020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A10U3030	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	01295	SN74LS393
A10U3040	156-1429-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1429-01
A10U3042	156-1429-01			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1429-01
A10U3050	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A10U4010	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A10U4020	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A10U4030	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A10U4040	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A10U4042	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR,BURN IN	01295	SN74LS393
A10U4050	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A10U5020	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	LF351N/A+
A10U6030	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	LF351N/A+
A10Y1015	158-0088-00			XTAL UNIT,QTZ:3.4133MHZ,0.01%,PARALLEL	33096	PB-1309

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11	----- -----			CKT BOARD ASSY:POWER SUPPLY		
A11C1002	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C1024	283-0180-00			CAP.,FXD,CER DI:5600PF,20%,200V	72982	8121N204 E 562M
A11C2006	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C2043	281-0769-00			CAP.,FXD,CER DI:840PF,10%,100V	56289	192C067841
A11C2066	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	35ULA4R7V-T
A11C3004	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C3012	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C3018	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C3022	285-1200-00			CAP.,FXD,PLSTC:0.022UF,5%,200V	14752	950D1C223J
A11C3031	283-0001-00			CAP.,FXD,CER DI:0.005UF,+100-0%,500V	72982	831-559E502P
A11C3035	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C3042	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C3063	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	8035D9AADC1G470K
A11C3066	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A11C4018	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C4033	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C4038	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C4046	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C4049	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	25ULA10V-T
A11C4063	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	72982	8035D9AADX7R102K
A11C4067	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	72982	805-509B152J
A11C5005	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C5006	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C5007	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C5016	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A11C5026	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A11C5044	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	410P10291
A11C5046	285-0862-00			CAP.,FXD,PLSTC:0.001,10%,100V	56289	410P10291
A11CR1005	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A11CR1006	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A11CR1037	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A11CR1044	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR1045	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR1046	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR1047	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR2068	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR3008	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	03508	1N5624
A11CR3048	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR3064	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR4049	152-0456-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	1N827
A11CR4056	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR4065	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A11CR5017	152-0581-00			SEMICOND DEVICE:SILICON,20V,1A	80009	152-0581-00
A11L3010	108-0337-00			COIL,RF:25UH	80009	108-0337-00
A11L3015	108-1026-00			COIL,RF:29UH	80009	108-1026-00
A11L4005	108-0337-00			COIL,RF:25UH	80009	108-0337-00
A11L5024	108-0554-00			COIL,RF:5UH	80009	108-0554-00
A11L5034	108-0993-00			COIL,RF:FIXED,400UH	80009	108-0993-00
A11Q1042	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A11Q1043	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A11Q1048	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A11Q1049	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A11Q2040	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A11Q4048	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A11Q5038	151-0426-00			TRANSISTOR:SILICON,NPN	03508	X44H242
A11R1025	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11R1053	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R1058	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R2028	301-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.50W	01121	EB1505
A11R2041	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A11R2042	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
A11R2044	301-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.50W	01121	EB6805
A11R2067	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R3003	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A11R3005	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R3032	301-0330-00			RES.,FXD,CMPSN:33 OHM,5%,0.50W	01121	EB3305
A11R3041	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A11R3043	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A11R3044	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R3045	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R3046	315-0184-00			RES.,FXD,CMPSN:180K OHM,5%,0.25W	01121	CB1845
A11R3047	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R3061	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A11R3062	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A11R3065	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A11R3067	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A11R3068	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A11R4036	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R4037	307-0589-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	19701	145P6R8T
A11R4043	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A11R4044	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A11R4045	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A11R4049	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A11R4053	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R4054	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045
A11R4057	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A11R4061	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A11R4062	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A11R4064	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R4066	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A11R5010	308-0695-00			RES.,FXD,WW:0.05 OHM,10%,5W	91637	RLS-5 .050HM,10%
A11R5014	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A11R5042	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A11R5054	321-0363-00			RES.,FXD,FILM:59K OHM,1%,0.125W	91637	MFF1816G59001F
A11R5056	321-0422-00			RES.,FXD,FILM:243K OHM,1%,0.125W	91637	MFF1816G24302F
A11R5058	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A11R5065	311-1246-00			RES.,VAR,NONWIR:50K OHM,10%,0.50W	02111	63X-503-T602
A11T3024	120-1264-00			XFMR,PWR,STPDN:HIGH FREQUENCY	80009	120-1264-00
A11T3037	120-1262-00			TRANSFORMER,RF:BASE DRIVE,POT CORE	80009	120-1262-00
A11T4035	120-1263-00			TRANSFORMER,RF:CURRENT	80009	120-1263-00
A11U2055	156-0525-03			MICROCIRCUIT,DI:DUAL J-K MASTER SLAVE FF	80009	156-0525-03
A11U3055	156-0411-02			MICROCIRCUIT,LI:QUAD COMPARATOR,SEL	04713	LM339JDS

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12	----- -----			CKT BOARD ASSY:VERTICAL INTERFACE		
A12C1011	283-0156-00			CAP.,FXD,CER DI:1000PF,+100-0%,200V	72982	8111A208Z5U0102Z
A12TP1	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP2	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP3	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP4	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A14	----- -----			CKT BOARD ASSY:PROBE INTERFACE		
A14J101	131-2614-00			CONN,RCPT,ELEC:CKT BD,32/64 FEM CONT	05574	3VH32/1JNK12
A15	----- -----			CKT BOARD ASSY:INTERFACE		
A15C203	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	72982	8141N064Z5U205M
A15C204	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	72982	8141N064Z5U205M
A15C209	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	72982	8141N064Z5U205M
A15C210	283-0212-00			CAP.,FXD,CER DI:2UF,20%,50V	72982	8141N064Z5U205M
A16	----- -----			CKT BOARD ASSY:KEYBOARD		
A16R1012	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1013	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1021	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1031	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1041	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1051	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1081	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R1082	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A16R3076	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A16R3096	311-1235-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	32997	3386F-T04-104
A16S1011	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1012	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1021	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1022	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1031	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1032	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1041	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1042	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1051	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1052	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1061	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1062	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1071	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S1091	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2013	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2014	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2023	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2024	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2033	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2034	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2043	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2044	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2053	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2054	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2063	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2064	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2073	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A16S2075	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2084	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S2093	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3016	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3035	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3036	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3045	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3046	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3055	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3056	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3065	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3066	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3086	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09
A16S3095	263-0019-09			SWITCH PB ASSY:MOMENTARY	80009	263-0019-09

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
C1000	283-0180-00			CAP.,FXD,CER DI:5600PF,20%,200V	72982	8121N204 E 562M
CR2018	152-0540-00			SEMICOND DEVICE:RECTIFIER,20V,25A	04713	SBR5366
CR2035	152-0540-00			SEMICOND DEVICE:RECTIFIER,20V,25A	04713	SBR5366
Q1015	151-0621-01			TRANSISTOR:SILICON,NPN	80009	151-0621-01
Q1035	151-0625-00			TRANSISTOR:SILICON,PNP	03508	D45H11

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

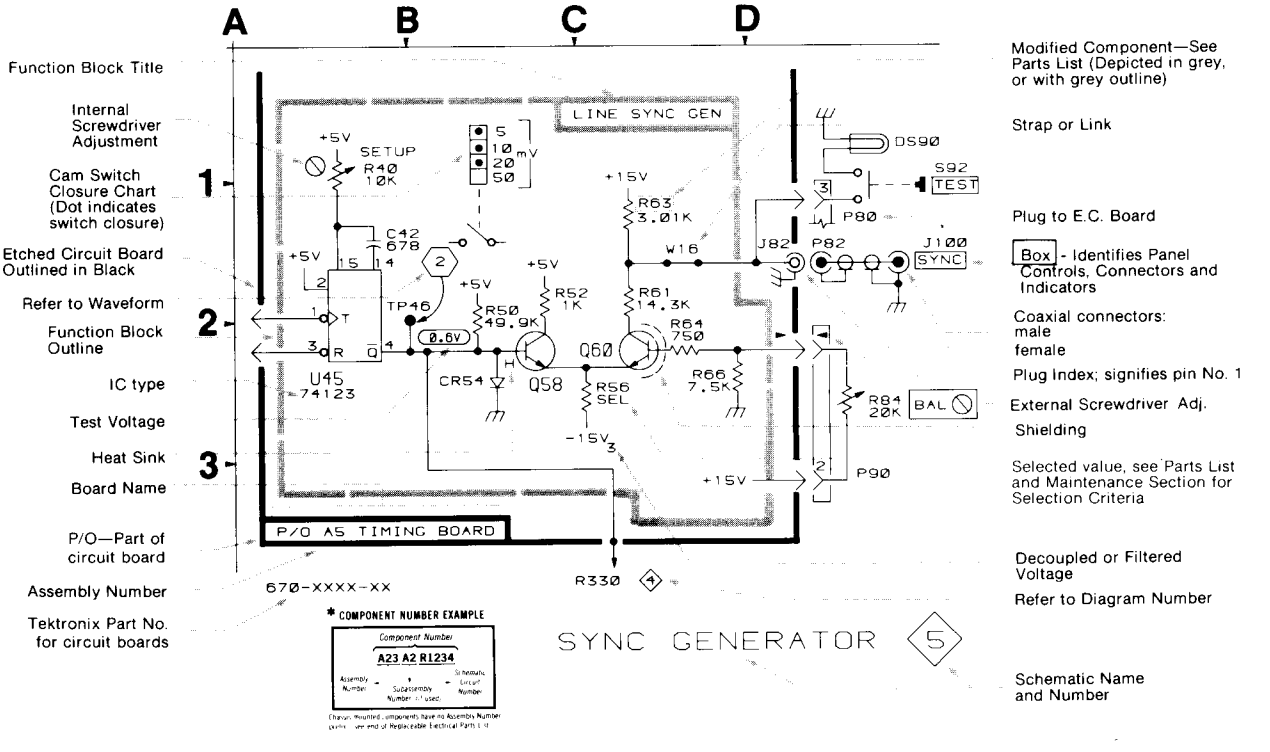
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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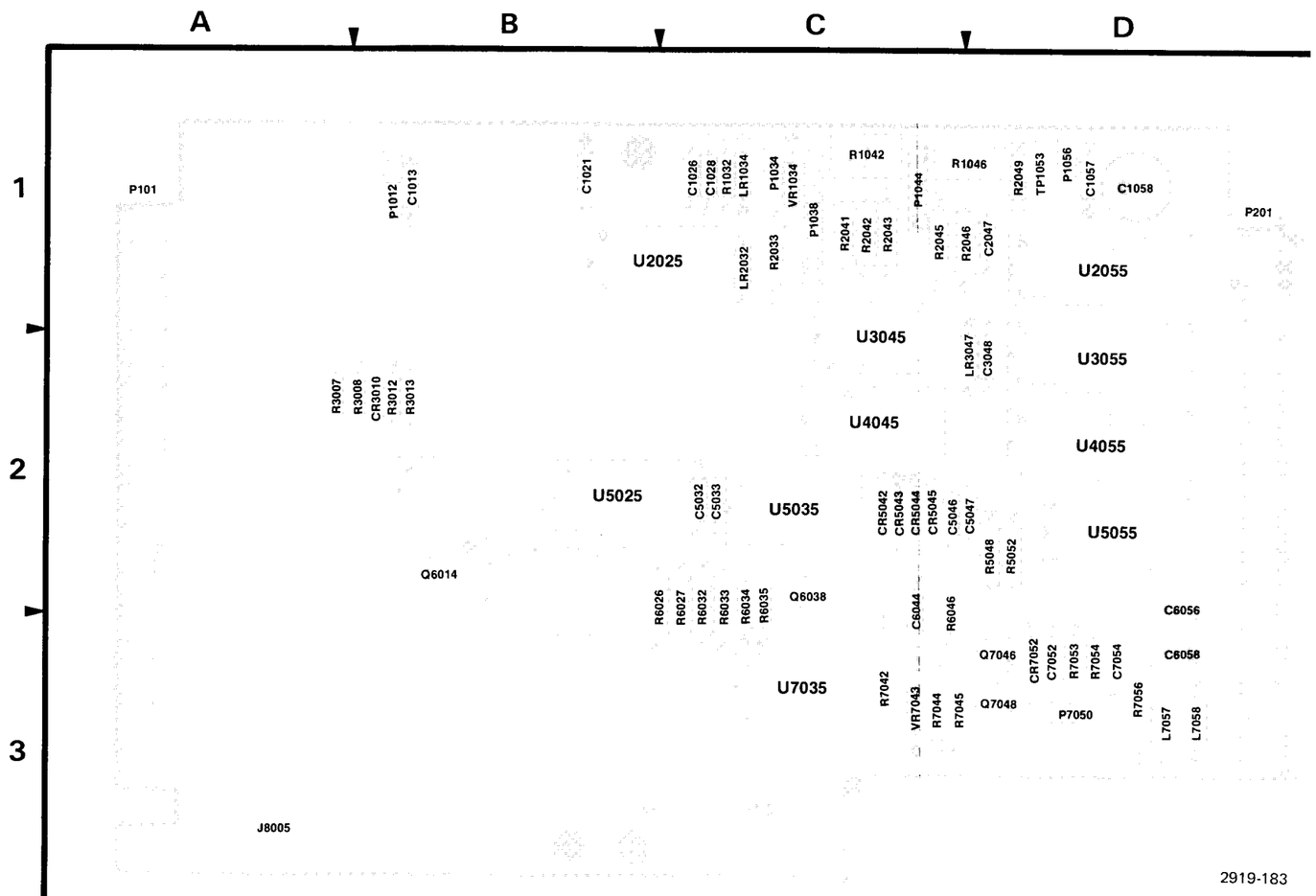

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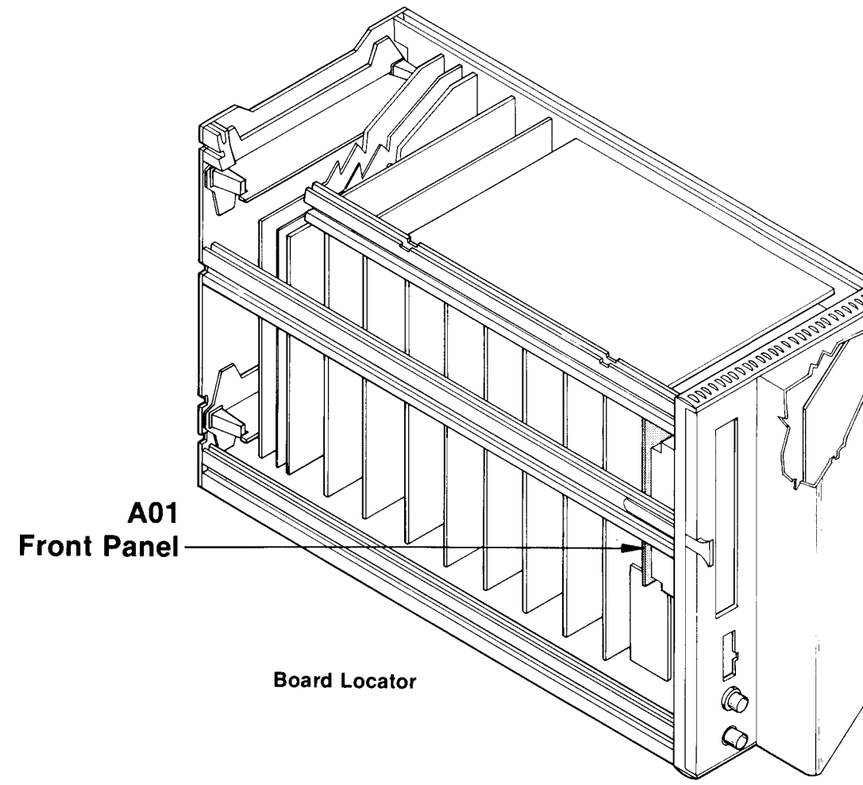
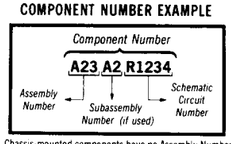


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-1A. A01 Front Panel board component locations.

P/O A1 FRONT PANEL DIAGRAM 1A

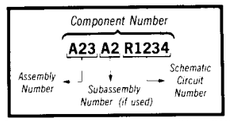
ASSEMBLY A1					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1013	E1	B1	R1046	C2	D1
C1021	E1	B1	R2033	C2	C1
C1026	A1	C1	R2041	C2	C1
C1028	B1	C1	R2042	C2	C1
C1057	F1	D1	R2043	B2	C1
C1058	F1	D1	R2045	C2	C1
C2047	D3	D1	R2046	C2	D1
C3048	B2	D2	R3007	C4	A2
C5032	F1	C2	R3008	C5	B2
C5033	E1	C2	R3012	A5	B2
C5046	C2	C2	R3013	C5	B2
C5047	B3	D2	R5048	C2	D2
C6044	C4	C3	R5052	B3	D2
C6056	E1	D3	R6026	C5	C2
C6058	E2	D3	R6027	C4	C2
C7052	C3	D3	R6032	C5	C2
C7054	C3	D3	R6033	D5	C2
			R6034	D4	C2
CR3010	C5	B2	R6035	D5	C2
CR5042	E2	C2	R6046	D4	D3
CR5043	E1	C2	R7042	E2	C3
CR5044	C2	C2	R7044	D4	C3
CR5045	B3	C2	R7045	D4	D3
CR7052	C3	D3	R7053	C3	D3
			R7054	A5	D3
L7057	E1	D3	R7056	C3	D3
L7058	E1	D3			
			TP1053	C2	D1
LR1034	B1	C1			
LR2032	A1	C1	U2025	D2	B1
LR3047	B1	D2	U2055	A2	D1
			U3045A	C2	C1
P1012	F2	B1	U3045B	B3	C1
P1034	C1	C1	U3045C	C2	C1
P1038	A2	C1	U3045D	B1	C1
P1044	F1	C1	U3055	A3	D2
P1056	F3	D1	U4045	B2	C2
P7050	A5	D3	U4055	B3	D2
P7050	F2	D3	U5025A	F4	B2
			U5025C	A4	B2
Q6014	C4	B2	U5035	D1	C2
Q6038	C5	C2	U5055A	B4	D2
Q7046	C3	D3	U5055B	B5	D2
Q7048	C4	D3	U7035	D4	C3
R1032	A1	C1	VR1034	A1	C1
R1042	B2	C1	VR7043	D4	C3

Partial A1 also shown on diagram 1B.

A01 FRONT PANEL 1A

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

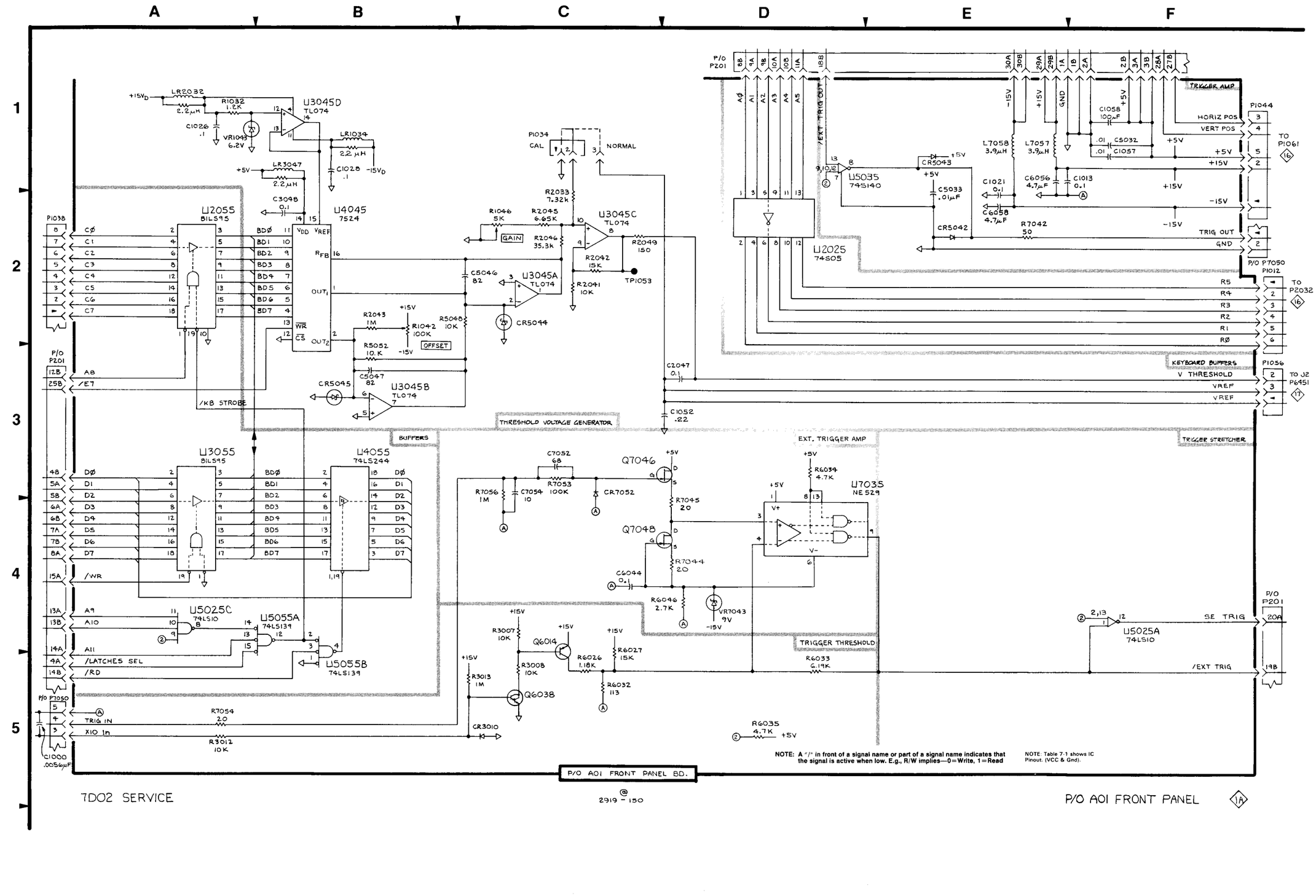


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Table 7-1

IC Pin Information

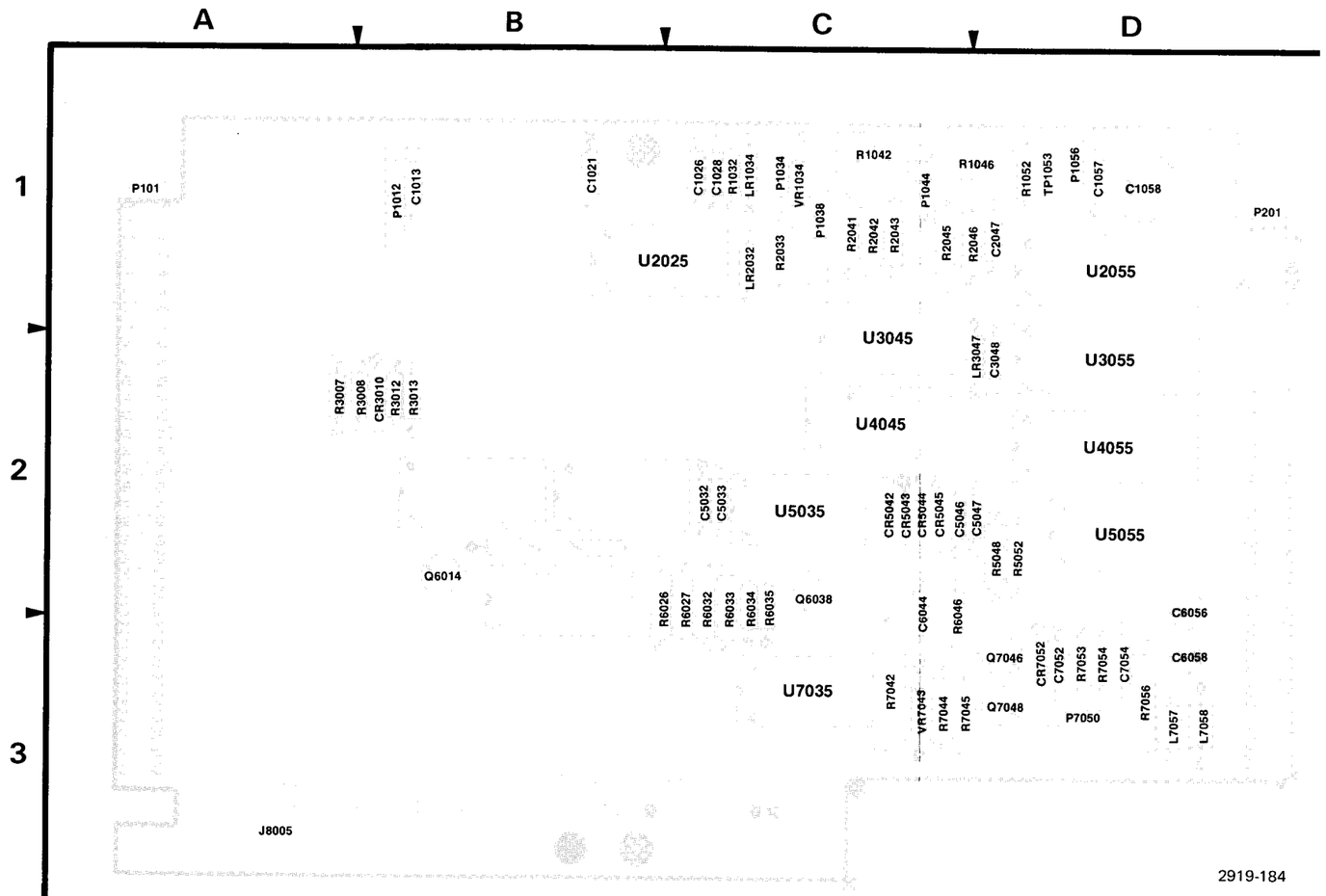
Device Type	VDD or VCC	GND
1660	1,16	8
10016	1,16	8
10102	1,16	8
10103	1,16	8
10104	1,16	8
10113	1,16	8
10118	1,16	8
10131	1,16	8
10135	1,16	8
10138	1,16	8
10164	1,16	8
10174	1,16	8
10197	1,16	8
14518B	16	8
2716	24	12
4027	16	8
6514	18	9
7072	20,21	11
74C08	14	7
74C139	16	8
74C174	16	8
74C193	16	8
74C374	20	10
74LS00	14	7
74LS02	14	7
74S04	14	7
74S05	14	7
74S08	14	7
74S09	14	7
74LS10	14	7
74S11	14	7
74S20	14	7
74LS21	14	7
74LS27	14	7
74S30	14	7
74LS32	14	7
74S64	14	7
74S65	14	7
74S74	14	7
74S76	5	13
74LS86	14	7
74LS109	16	8
74LS112	16	8
74LS113	14	7
74LS138	16	8
74LS139	16	8
74S140	14	7
74LS151	16	8
74LS153	16	8
74LS154	24	12
74LS157	16	8
74LS161	16	8
74LS163	16	8
74LS166	16	8
74LS175	16	8
74LS193	16	8
74LS195	16	8
74LS240	20	10
74LS244	20	10
74LS245	20	10
74LS273	20	10
74LS373	20	10
74LS374	20	10
74LS379	16	8
74LS390	16	8
74LS393	14	7
8085A	40	20
81LS95	20	10
81LS97	20	10
82S70	14	7
93L422	22	8
96LS02	16	8
AD7524	14	3
AM2942	22	11
AM2972	16	8
LF351	7	4
LM339	3	12
M218	13	4
MK36000	24	12
NE529	14	10
NE555	8	1
S6831	24	12
TL074	4	11
UDP444	18	9



NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read

NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).

P/O A01 FRONT PANEL BD.



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A01 FRONT PANEL BOARD

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-1B. A01 Front Panel board component locations.

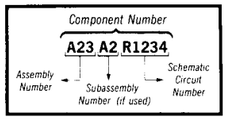
P/O A2 IC ACQUISITION DIAGRAM 2A

ASSEMBLY A2		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J7048	A2	D3
P102	A1	A2
P102	F5	A2
P202	B1	D3
P202	D1	D3
R2032D	B5	C1
R2032E	B5	C1
R2032F	A5	C1
R3024A	D3	B2
R3024B	D3	B2
R3024C	D3	B2
R3024D	D2	B2
R5022A	D5	B3
R5022B	D4	B3
R5022C	D5	B3
R5041F	D3	C2
R5041I	D2	C2
R6022D	D4	B3
R6041F	C4	C3
R6041I	C5	C3
R7031A	A2	C3
R7031B	A2	C3
R7031C	A4	C3
R7031D	A5	C3
R7031E	A5	C3
R7031F	A4	C3
R7031G	A3	C3
R7031H	A3	C3
TP74-1	A5	C3
U3040D	B5	C2
U4010	B1	A2
U4030	B2	C2
U5010B	E1	A2
U5020	E3	B2
U5030	B3	C2
U6010B	D1	A3
U6020	E4	B3
U6030	B4	C3
U6040A	C5	C3
U6040B	C2	C3
U6040C	C3	C3
U6040D	C4	C3
U7010B	D1	A3
U7030	B5	C3

Partial A2 also shown on diagrams 2B and 2C.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

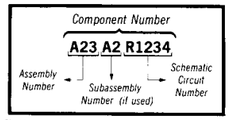
P/O A1 FRONT PANEL DIAGRAM 1B

ASSEMBLY A1		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J8005	C1	A3
J8005	F1	A3
P101	A1	A1
P101	D1	A1

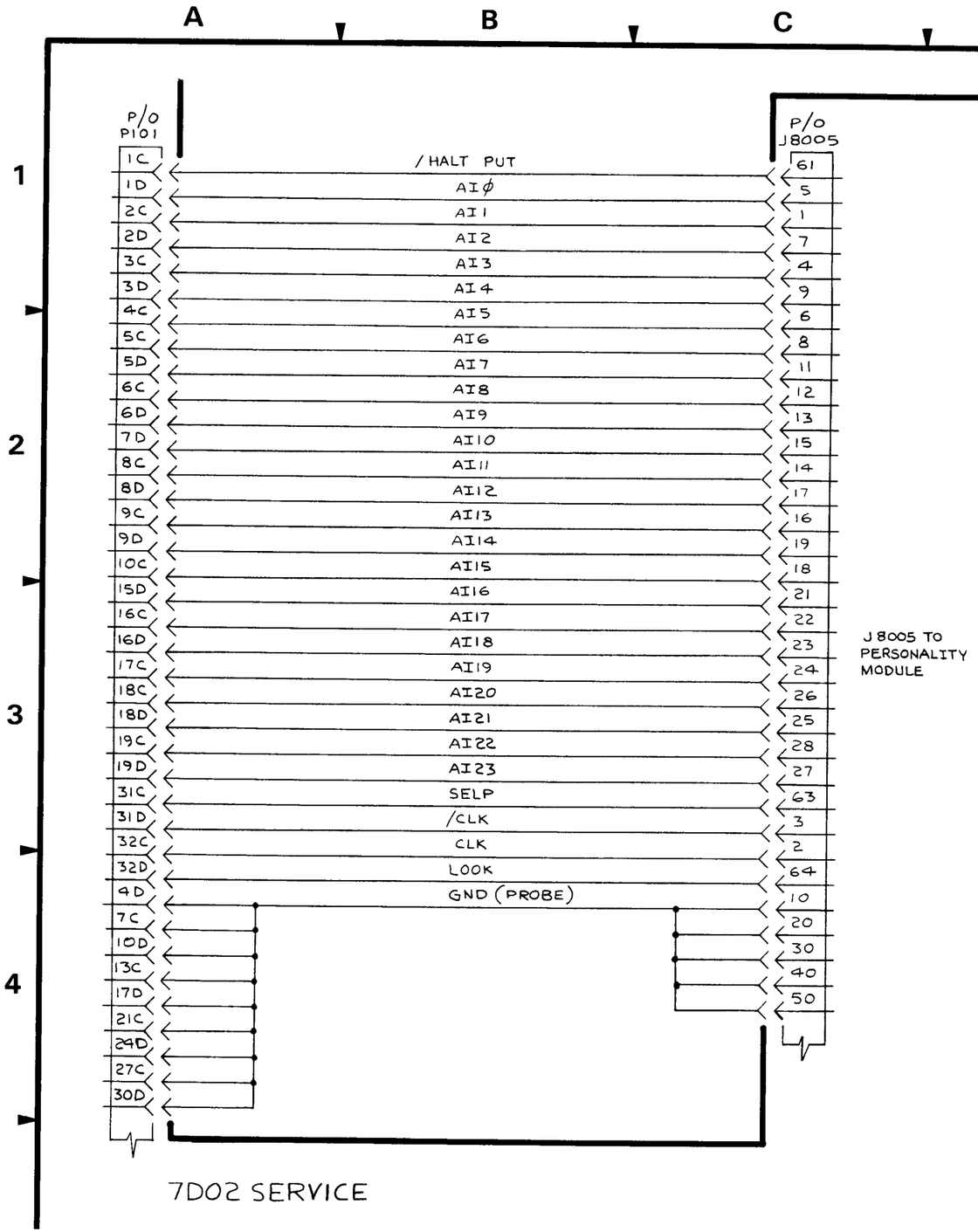
Partial A1 also shown on diagram 1A.

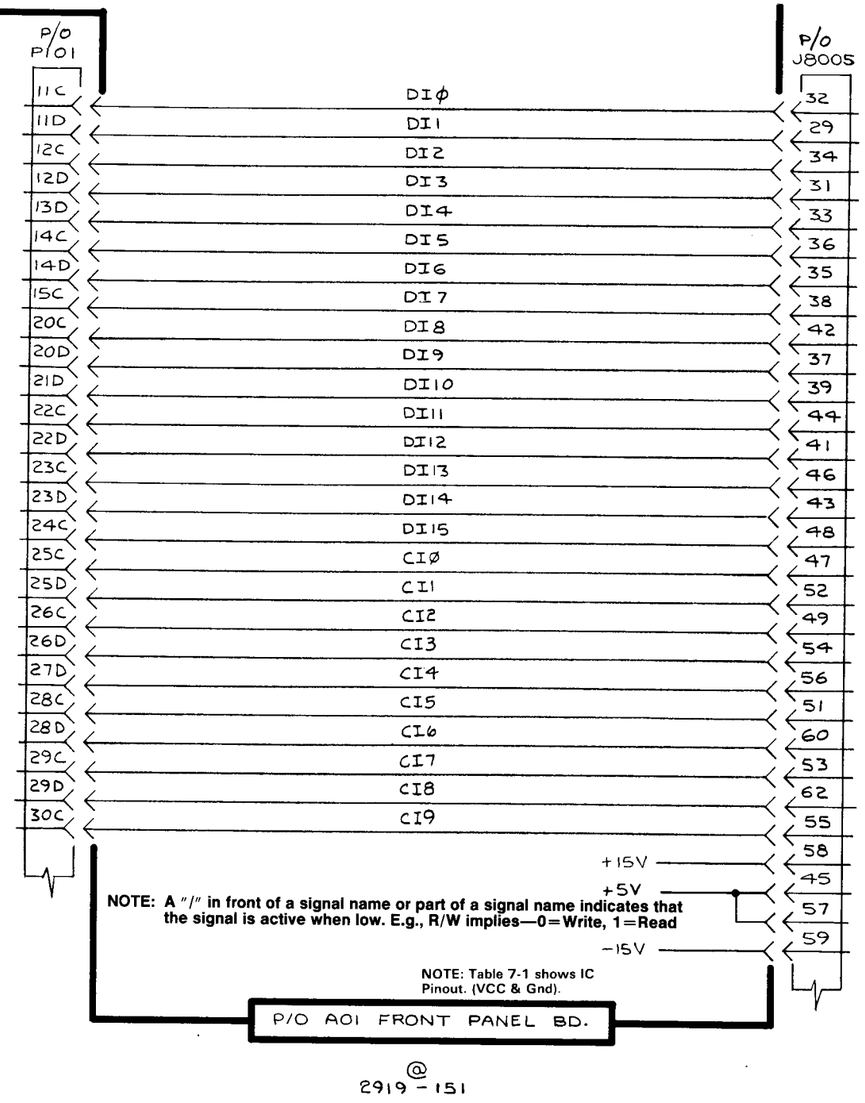
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
P/O P101
1C /HALT PUT
1D AIØ
2C AI1
2D AI2
3C AI3
3D AI4
4C AI5
5C AI6
5D AI7
6C AI8
6D AI9
7D AI10
8C AI11
8D AI12
9C AI13
9D AI14
10C AI15
15D AI16
16C AI17
16D AI18
17C AI19
18C AI20
18D AI21
19C AI22
19D AI23
31C SELP
31D /CLK
32C CLK
32D LOOK
4D GND (PROBE)
7C
10D
13C
17D
21C
24D
27C
30D
P/O J8005
61
5
1
7
4
9
6
8
11
12
13
15
14
17
16
19
18
21
22
23
24
26
25
28
27
63
3
2
64
10
20
30
40
50
J 8005 TO PERSONALITY MODULE
7D02 SERVICE


P/O P101
11C DIØ
11D DI1
12C DI2
12D DI3
13D DI4
14C DI5
14D DI6
15C DI7
20C DI8
20D DI9
21D DI10
22C DI11
22D DI12
23C DI13
23D DI14
24C DI15
25C CIØ
25D CI1
26C CI2
26D CI3
27D CI4
28C CI5
28D CI6
29C CI7
29D CI8
30C CI9
P/O J8005
32
29
34
31
33
36
35
38
42
37
39
44
41
46
43
48
47
52
49
54
56
51
60
53
62
55
58
45
57
59
+15V
+5V
-15V
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O AOI FRONT PANEL BD.
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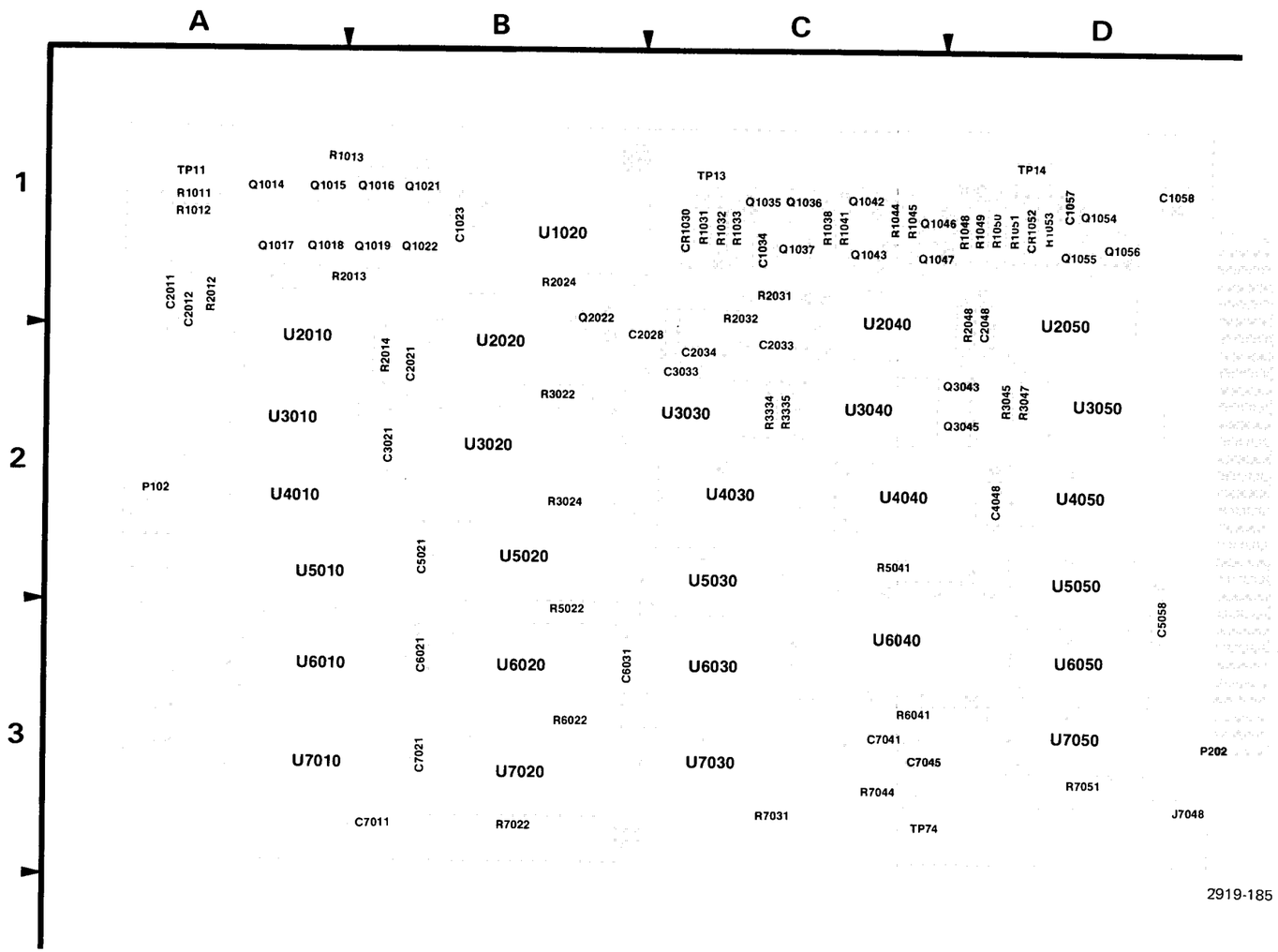
P/O AOI FRONT PANEL 1B



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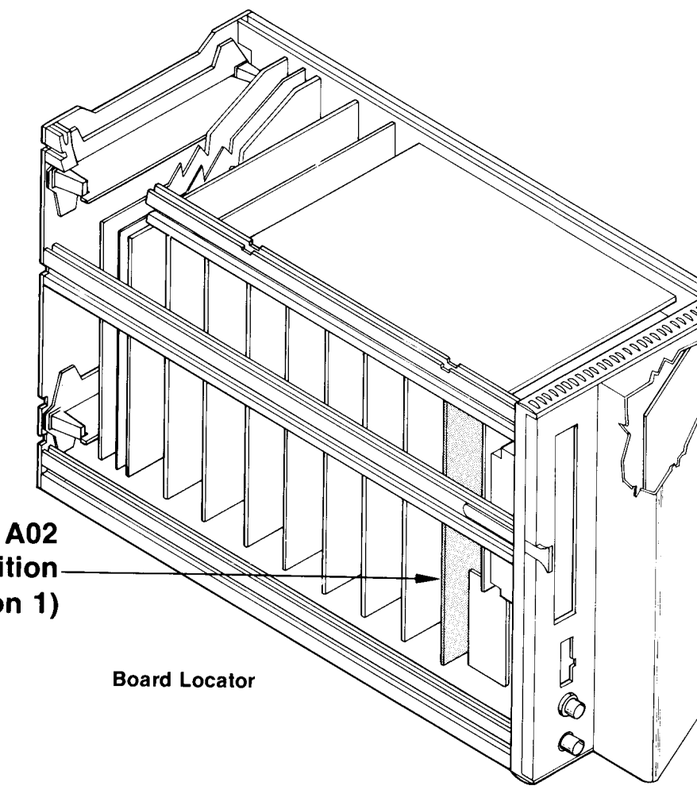
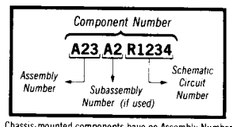


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

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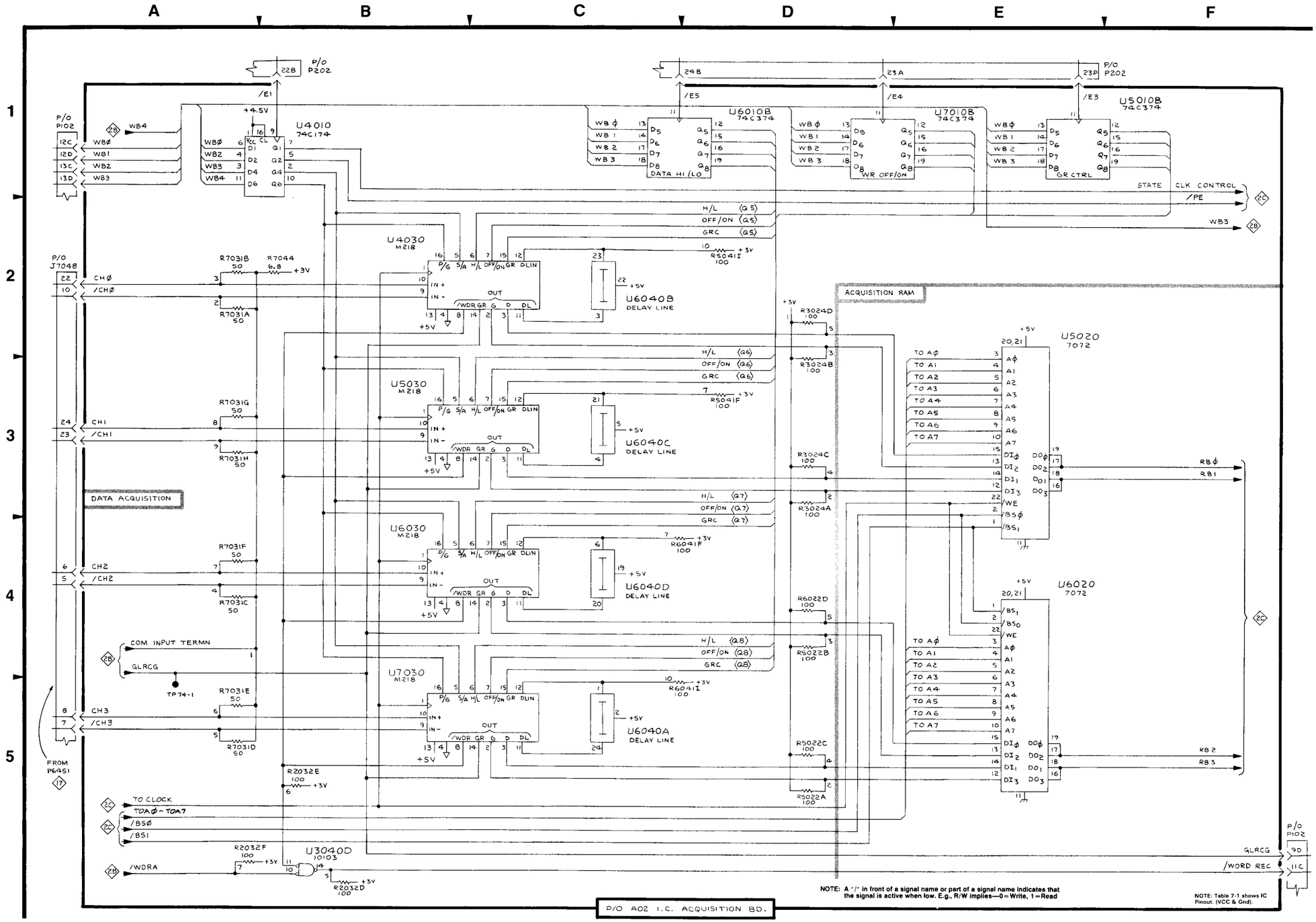
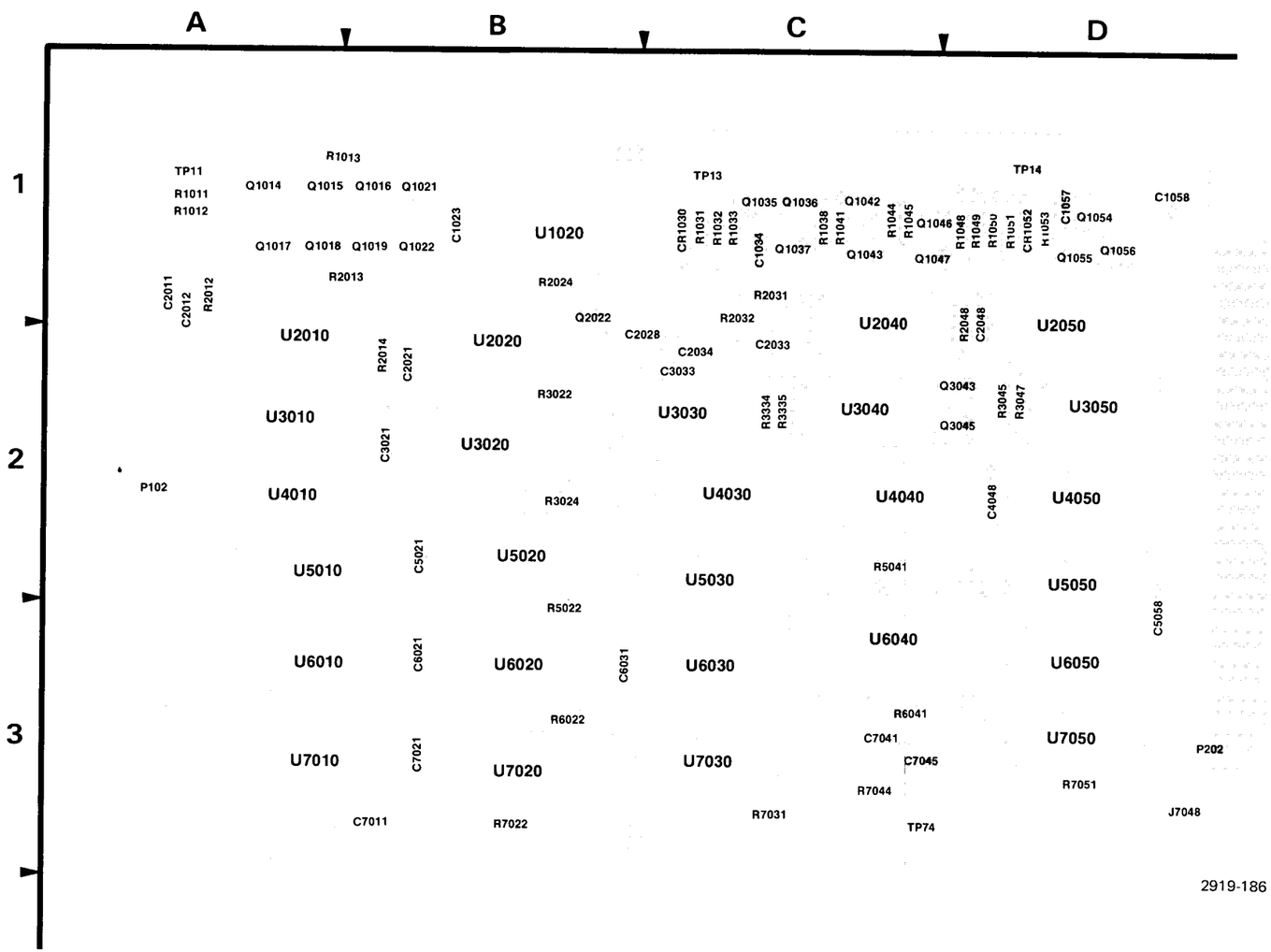
Figure 7-2A. A02 Option 1 IC Acquisition board component locations.


A
B
C
D
E
F
1
2
3
4
5
P/O P202
22B
/E1
+4.5V
U4010
74C174
P/O P102
WB4
WBØ
WB1
WB2
WB3
23B
/E5
23A
/E4
23P
/E3
U6010B
74C374
U7010B
74C374
U5010B
74C374
DATA HI/LO
WR OFF/ON
GR CTRL
STATE CLK CONTROL
/PE
WB3
H/L (Q5)
OFF/ON (Q5)
GRC (Q5)
R5041I 100
U4030
M218
P/S S/A H/L OFF/ON GR DLIN
IN+
IN-
OUT
/WDR GR G D DL
U6040B
DELAY LINE
P/O J7048
CHØ
/CHØ
R7031B 50
R7044 6.8
+3V
R7031A 50
H/L (Q6)
OFF/ON (Q6)
GRC (Q6)
R5041F 100
U5030
M218
U6040C
DELAY LINE
CH1
/CH1
R7031G 50
R7031H 50
ACQUISITION RAM
R3024D 100
R3024B 100
R3024C 100
R3024A 100
U5020
7072
TO AØ
TO A1
TO A2
TO A3
TO A4
TO A5
TO A6
TO A7
DIØ
DI1
DI2
DI3
/WE
/BSØ
/BS1
DOØ
DO1
DO2
DO3
RBØ
RB1
DATA ACQUISITION
H/L (Q7)
OFF/ON (Q7)
GRC (Q7)
R6041F 100
U6030
M218
U6040D
DELAY LINE
CH2
/CH2
R7031F 50
R7031C 50
R6022D 100
R6022B 100
R5022C 100
R5022A 100
U6020
7072
RB2
RB3
COM INPUT TERMN
GLRCG
TP74-1
H/L (Q8)
OFF/ON (Q8)
GRC (Q8)
R6041I 100
U7030
M218
U6040A
DELAY LINE
CH3
/CH3
R7031E 50
R7031D 50
FROM P6451
R2032E 100
TO CLOCK
TDAØ-TDA7
/BSØ
/BS1
/WDRA
R2032F 100
U3040D
10103
R2032D 100
P/O P102
9D
11C
GLRCG
/WORD REC
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A02 I.C. ACQUISITION BD.



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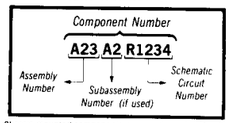
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

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Figure 7-2B. A02 Option 1 IC Acquisition board component locations.

P/O A2 IC ACQUISITION DIAGRAM 2C

ASSEMBLY A2

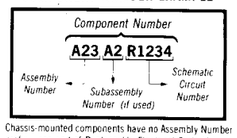
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1023	F1	B1	Q1043	B2	C1	R2024I	F4	B1
C1034	C2	C1	Q1046	B1	C1	R2031	B4	C1
C1057	D1	D1	Q1047	D1	C1	R2032A	B3	C1
C1058	F2	D1	Q1055	D1	D1	R2032B	E3	C1
C2011	F1	A1	Q1056	D1	D1	R2032C	C5	C1
C2012	F1	A1	Q2022	B5	B1	R2032G	B2	C1
C2021	A5	B2	Q3043	C3	D2	R2048	B4	D1
C2028	F1	B2	Q3045	C3	D2	R5041B	C5	C2
C2033	F1	C2				R5041D	D3	C2
C2034	F1	C2	R1011	E3	A1	R5041E	B2	C2
C2048	F1	D1	R1012	E3	A1	R5041G	B4	C2
C3021	F1	B2	R1013A	E4	B1	R5041H	B5	C2
C3033	F1	C2	R1013B	E4	B1	R6041	D2	C3
C4048	F1	D2	R1013D	E5	B1	R6041E	D2	C3
C5021	F1	B2	R1013E	E5	B1	R7022B	C4	B3
C5058	F1	D3	R1013F	F5	B1	R7022C	C4	B3
C6021	F1	B3	R1013G	F5	B1	R7022D	C4	B3
C6031	F1	B3	R1013H	F4	B1	R7022E	C4	B3
C7011	F1	B3	R1013I	F4	B1	R7022F	C5	B3
C7021	F1	B3	R1031	C2	C1	R7022G	C5	B3
C7041	F1	C3	R1032	C2	C1	R7022H	C5	B3
C7045	F1	C3	R1033	C2	C1	R7022I	C5	B3
			R1038	B2	C1			
CR1030	C2	C1	R1041	C1	C1	TP11	E3	A1
CR1042	B2	D1	R1044	B1	C1	TP13	E3	C1
CR1052	D2	D1	R1045	B1	C1	TP14-1	C1	D1
CR1059	C1	D1	R1048	D1	D1	TP14-2	E2	D1
CR1059	C2	D1	R1049	D1	D1	TP14-3	F2	D1
			R1050	D1	D1	TP74-4	F2	C3
P102	A3	A2	R1051	D2	D1	TP74-4	C2	C3
P102	A5	A2	R1053	D2	D1			
P102	F1	A2	R2012A	C4	A1	U1020	F4	B1
P102	F2	A2	R2012B	C4	A1	U2010	D4	A2
P102	F5	A2	R2012C	D5	A1	U2010	D5	A2
P202	A2	D3	R2012D	C4	A1	U2020	D5	B2
P202	A4	D3	R2013A	F3	B1	U2040	C4	C1
P202	A5	D3	R2013B	F3	B1	U2050A	A5	D1
P202	F1	D3	R2013C	D5	B1	U2050C	A5	D1
P202	F2	D3	R2013D	D5	B1	U2050	B4	D1
P202	F4	D3	R2013E	D5	B1	U3010A	A5	A2
			R2013F	D5	B1	U3010B	A5	A2
Q1014	F4	A1	R2013G	D5	B1	U3010C	B5	A2
Q1015	F5	A1	R2013H	D5	B1	U3010D	B4	A2
Q1016	E5	B1	R2013I	D5	B1	U3030	C5	C2
Q1017	F4	A1	R2014	A5	B2	U3040A	B5	C2
Q1018	F5	A1	R2024A	F5	B1	U3040B	B5	C2
Q1019	E5	B1	R2024B	F5	B1	U3040C	C5	C2
Q1021	E4	B1	R2024C	E5	B1	U3050A	B3	D2
Q1022	E4	B1	R2024D	E5	B1	U3050B	A4	D2
Q1035	C2	C1	R2024E	E4	B1	U3050C	B3	D2
Q1036	B2	C1	R2024F	E4	B1	U3050D	A4	D2
Q1037	C1	C1	R2024G	D5	B1	U4040A	D2	C2
Q1042	B1	C1	R2024H	F4	B1	U4040B	B1	C2
						U4040D	D3	C2

Partial A2 also shown on diagram 2A and 2B

A02 OPTION 1 IC ACQUISITION 2C

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A2 IC ACQUISITION DIAGRAM 2B

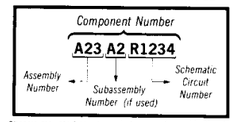
ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J7048	A2	D3
P102	A1	A2
R3022A	D3	B2
R3022B	D2	B2
R3022C	D3	B2
R3022D	D2	B2
R5041A	D2	C2
R5041C	D3	C2
R6022A	D5	B3
R6022B	D4	B3
R6022C	D5	B3
R6022E	D4	B3
R6041B	C4	C3
R6041C	C3	C3
R7051A	A4	D3
R7051B	A4	D3
R7051D	A5	D3
R7051E	A5	D3
R7051F	A2	D3
R7051G	A2	D3
R7051H	A3	D3
R7051I	A3	D3
U3020	E3	B2
U4010	B1	A2
U4050	B2	D2
U5010A	E1	A2
U5050	B3	D2
U6010A	D1	A3
U6040E	C3	C3
U6040F	C4	C3
U6040G	C5	C3
U6040H	C2	C3
U6050	B4	D3
U7010A	D1	A3
U7020	E4	B3
U7050	B5	D3

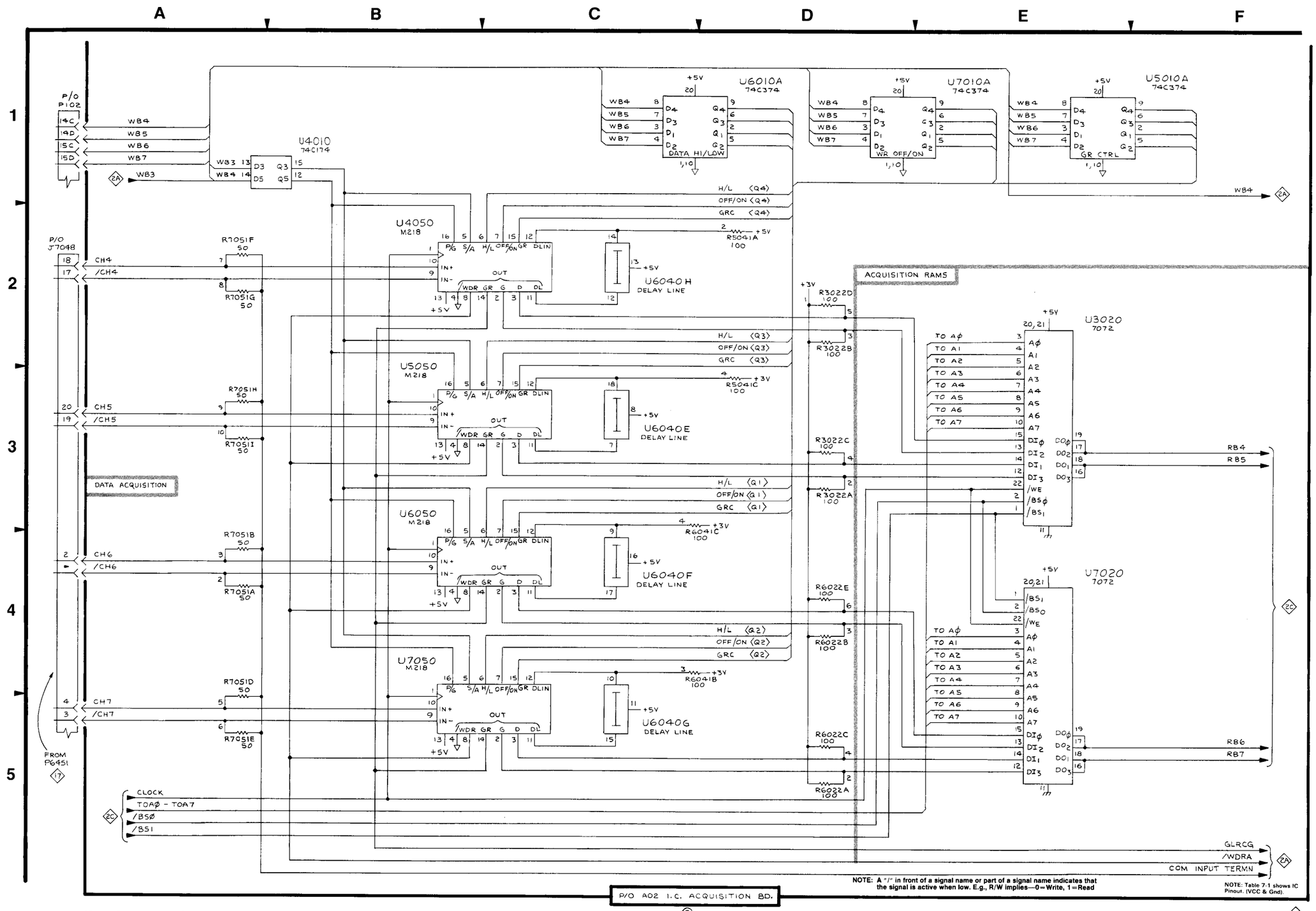
Partial A2 also shown on diagrams 2A and 2C.

Static Sensitive Devices
See Maintenance Section

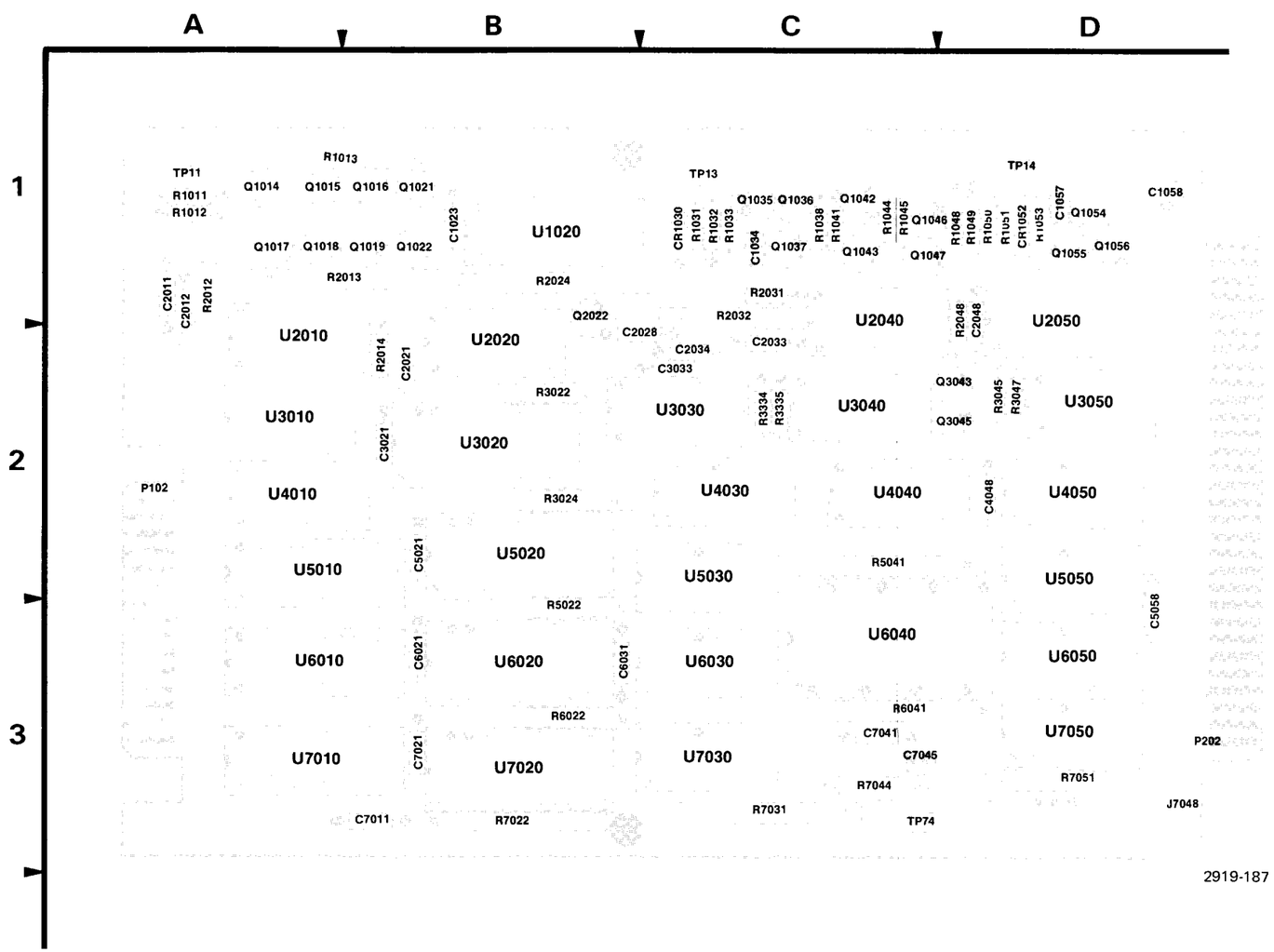
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
5
P/O P102
14C
19D
15C
15D
WB4
WB5
WB6
WB7
2A
WB3
U4010
74C174
WB3 13
WB4 14
D3 Q3 15
D5 Q5 12
U6010A
74C374
U7010A
74C374
U5010A
74C374
+5V
20
DATA HI/LOW
WR OFF/ON
GR CTRL
1,10
H/L (Q4)
OFF/ON (Q4)
GRC (Q4)
R5041A 100
U4050
M218
U6040H
DELAY LINE
P/O J7048
18 CH4
17 /CH4
R7051F 50
R7051G 50
U5050
M218
U6040E
DELAY LINE
20 CH5
19 /CH5
R7051H 50
R7051I 50
H/L (Q3)
OFF/ON (Q3)
GRC (Q3)
R5041C 100
DATA ACQUISITION
U6050
M218
U6040F
DELAY LINE
2 CH6
/CH6
R7051B 50
R7051A 50
H/L (Q1)
OFF/ON (Q1)
GRC (Q1)
R6041C 100
U7050
M218
U6040G
DELAY LINE
4 CH7
3 /CH7
R7051D 50
R7051E 50
H/L (Q2)
OFF/ON (Q2)
GRC (Q2)
R6041B 100
FROM P6451
17
ACQUISITION RAMS
+3V
R3022D 100
R3022B 100
R3022C 100
R3022A 100
R6022E 100
R6022B 100
R6022C 100
R6022A 100
U3020
7072
U7020
7072
20,21
TO A0
TO A1
TO A2
TO A3
TO A4
TO A5
TO A6
TO A7
A0
A1
A2
A3
A4
A5
A6
A7
DI0
DI1
DI2
DI3
/WE
/BS0
/BS1
DO0
DO1
DO2
DO3
RB4
RB5
RB6
RB7
2C
CLOCK
TOA0 - TOA7
/BS0
/BS1
GLRCG
/WDRA
COM INPUT TERMN
2A
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A02 I.C. ACQUISITION BD.
@ 2919-153
7D02 SERVICE
P/O A02 I.C. ACQUISITION
2B

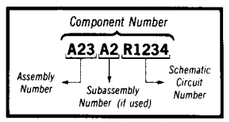
A02 OPTION 1 IC ACQUISITION BOARD



2919-187

Static Sensitive Devices
See Maintenance Section

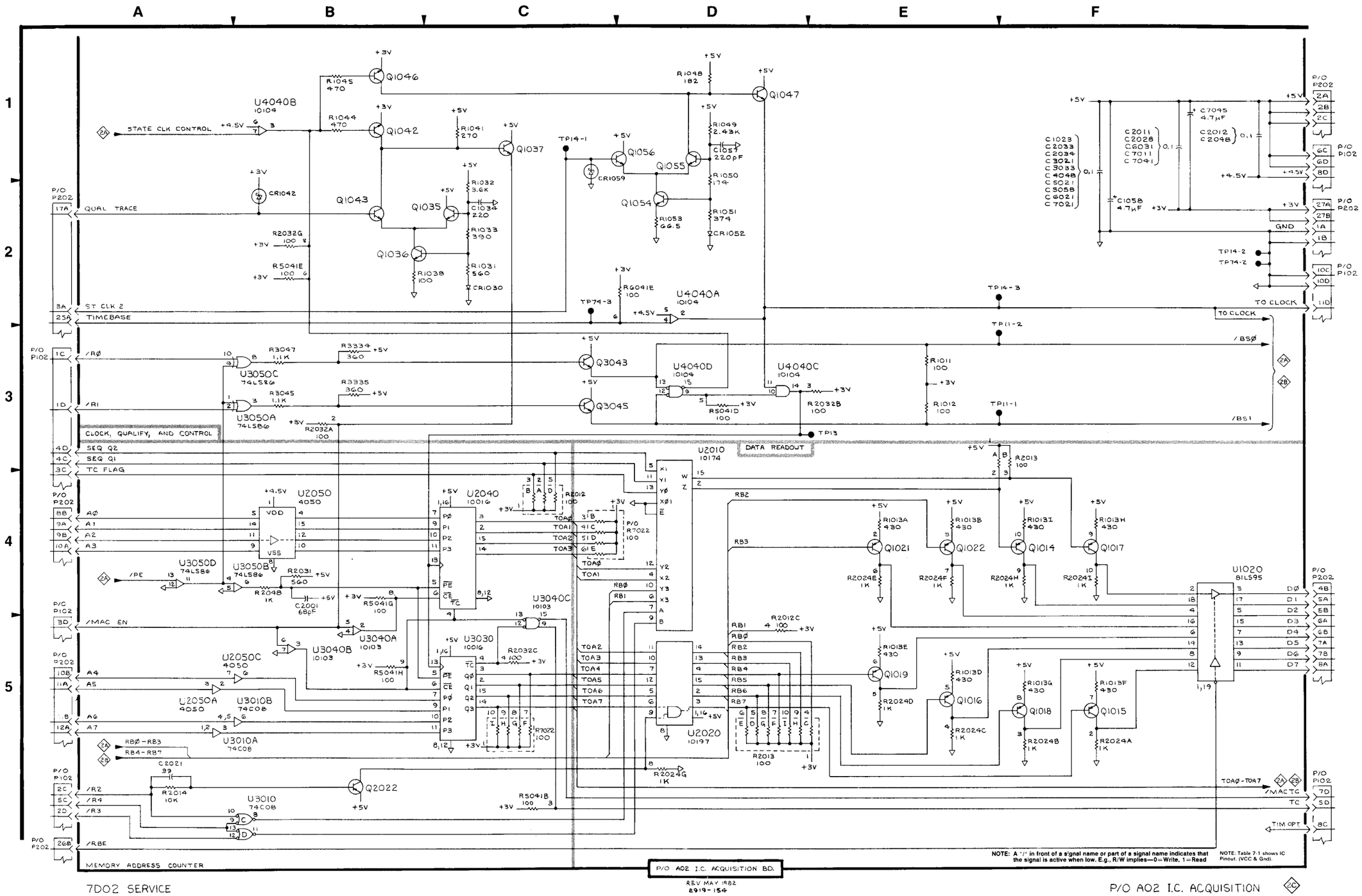
COMPONENT NUMBER EXAMPLE

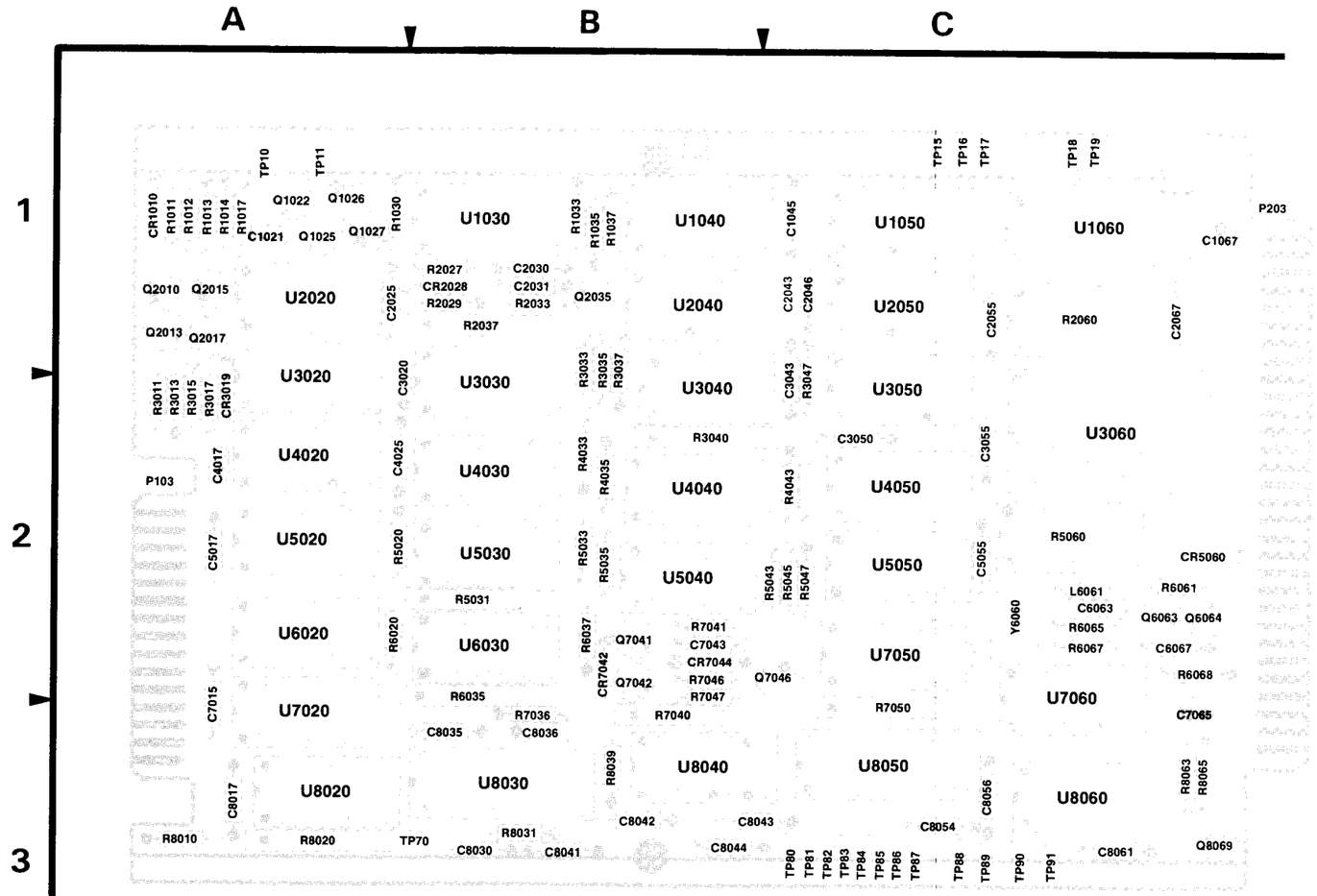


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

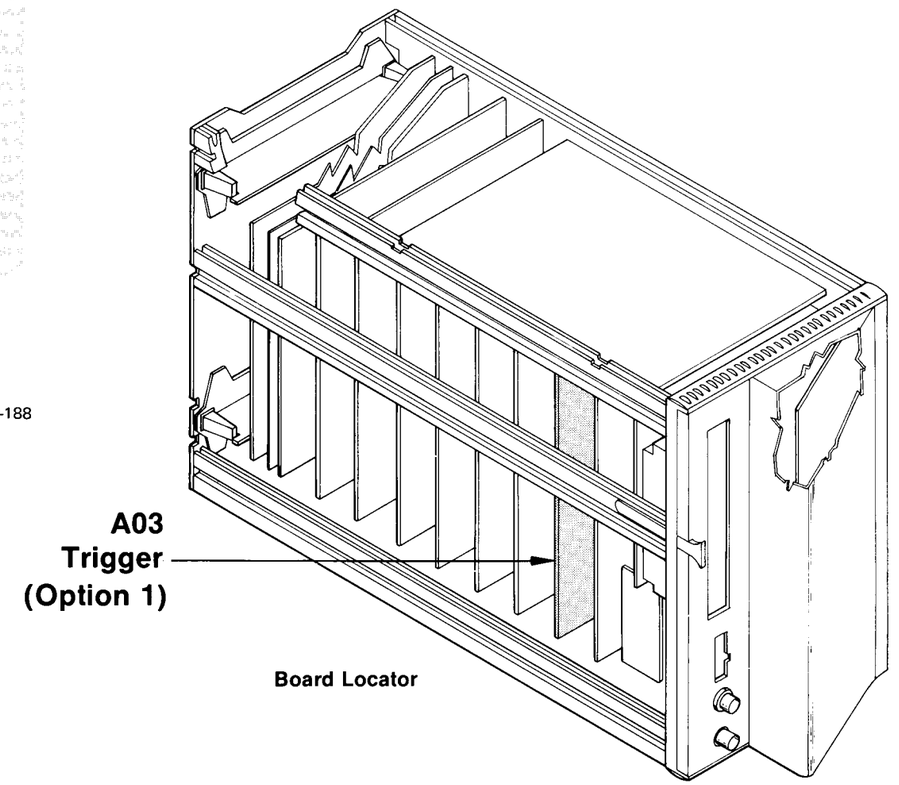
@

Figure 7-2C. A02 Option 1 IC Acquisition board component locations.


A
B
C
D
E
F
1
2
3
4
5
U4040B
10104
STATE CLK CONTROL
QUAL TRACE
ST CLK 2
TIMEBASE
/RØ
/RI
CLOCK, QUALIFY, AND CONTROL
SEQ Q2
SEQ Q1
TC FLAG
/PE
/MAC EN
RBØ-RB3
RB4-RB7
/R2
/R4
/R3
/RBE
MEMORY ADDRESS COUNTER
DATA READOUT
TO CLOCK
/BSØ
/BS1
GND
TOAØ-TOA7
/MACTC
TC
TIM OPT
U4040A
U4040C
U4040D
U3050C
U3050A
U3050D
U3050B
U3040C
U3040B
U3040A
U3030
U3010B
U3010A
U3010
U2050
U2050C
U2050A
U2040
U2010
U2020
U1020
Q1046
Q1042
Q1037
Q1047
Q1056
Q1055
Q1054
Q1043
Q1035
Q1036
Q3043
Q3045
Q2022
Q1021
Q1022
Q1014
Q1017
Q1019
Q1016
Q1018
Q1015
P/O P202
P/O P102
P/O R7022
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout (VCC & Gnd).
P/O A02 I.C. ACQUISITION BD.
REV MAY 1982
8919-154
7D02 SERVICE
P/O A02 I.C. ACQUISITION
A02 OPTION 1 IC ACQUISITION

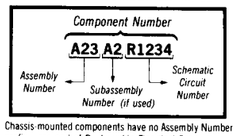


2919-188



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

Figure 7-3A. A03 Option 1 Trigger board component locations.

P/O A3 TRIGGER AND TIMEBASE DIAGRAM 3B

ASSEMBLY A3

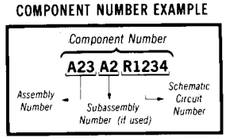
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1045	F3	C1	R3040E	B3	B2
C1067	E3	C1	R3040F	B3	B2
C2025	E3	A1	R3040G	C1	B2
C2030	F3	B1	R3047	B1	C1
C2031	F3	B1	R4035	B1	B2
C2043 *	B2	C1	R4045	B2	C2
C2046	E3	C1	R5031B	D2	B2
C2055	E3	C1	R5033	B2	B2
C2067	E3	C1	R5035	B1	B2
C3043	E3	C1	R5060A	C5	C2
C3050	F3	D2	R5060B	A3	C2
C3055	E3	C2	R5060C	C5	C2
C4025	F3	A2	R5060F	C5	C2
C5017	E3	A2	R5060G	C5	C2
C5055	E3	C2	R5060H	C5	C2
C7015	F3	A2	R5060I	C5	C2
C7043	E4	B2	R5060K	C5	C2
C7065	F3	C3	R5060L	C5	C2
C8017	F3	A3	R5060M	C5	C2
C8030	E3	B3	R5060N	C5	C2
C8035	F3	B3	R5060P	E5	C2
C8041	F3	B3	R6035A	E2	B2
C8042	E3	B3	R6035G	C1	B2
C8043	F3	B3	R6037	B2	B2
C8044	E3	B3	R6061	E1	C2
C8054	E3	C3	R6068	E1	C2
C8056	F3	C3	R7040E	E1	B3
C8061	E3	C3	R7046	E4	B2
			R7047	E4	B2
CR5060	F1	C2			
CR7044	E4	B2	TP11	B2	A1
			TP15	D6	C1
P103	A2	A2	TP16	D6	C1
P103	A4	A2	TP17	B5	C1
P103	F1	A2	TP18	F4	C1
P103	F2	A2	TP19	B5	C1
P103	F3	A2	TP91	F4	C3
P103	F3	A2			
P203	A1	C1	U1030	D3	B1
P203	A4	C1	U1040A	D3	B1
P203	F1	C1	U1040B	D4	B1
P203	F3	C1	U1050	B3	C1
P203	F5	C1	U1060	A4	C1
			U2040	C3	B1
Q2035	E4	B1	U2050	B3	D1
Q6063	E1	C2	U3020C	B2	A1
Q6064	F1	C2	U3040A	A2	B2
Q7046	E4	C2	U3040B	B6	B2
			U3040C	D6	B2
R1033	E2	B1	U3050	D5	D2
R1035	E4	B1	U3060	C5	C2
R1037	E4	B1	U4020B	B2	A2
R2033	E4	B1	U4030A	C1	B2
R2060B	E5	C1	U4030B	C1	B2
R2060C	E5	C1	U4040A	B2	B2
R2060D	E5	C1	U4050A	B5	D2
R2060E	E5	C1	U4050B	D3	D2
R2060G	C5	C5	U5020D	D1	A2
R2060H	B5	C1	U5030A	E2	B2
R2060I	B5	C1	U5030B	E1	B2
R2060J	B5	C1	U5040A	B1	B2
R2060K	B5	C1	U5040D	B2	B2
R2060L	B5	C1	U5040E	A3	B2
R2060M	B5	C1	U5040F	B2	B2
R2060N	B5	C1	U6030B	E2	C3
R2060P	B5	C1	U7020A	E3	A2
R3035	D3	B1	U7020C	C1	A2
R3037	D3	B1	U7020D	C1	A2
R3040B	C2	B2	U8030B	E2	B3

Partial A3 also shown on diagram 3A.

***See Parts List for serial number ranges.**

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A3 TRIGGER AND TIMEBASE DIAGRAM 3A

ASSEMBLY A3

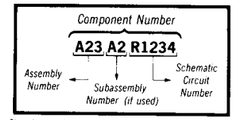
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1021	D4	A1	R7040A	G3	B3
C3020	E3	A1	R7041	G4	B2
C4017	B4	A2	R7050B	B1	C3
C6063 *	A1	C2	R7050C	B1	C3
C6067	A1	C2	R7050D	B1	C3
C8036	G4	B3	R7050E	B1	C3
			R7050F	C4	C3
CR1010	D5	A1	R7050G	D1	C3
CR2028	D4	B1	R8010	F2	A3
CR3019	B4	A2	R8020B	F1	A3
CR7042	H3	B2	R8020C	E2	A3
			R8020D	G2	A3
L6061	A1	C2	R8020E	C1	A3
			R8020F	D1	A3
P103	A5	A2	R8020G	E2	A3
P103	H2	A2	R8031	F2	B3
P103	H4	A2	R8039	G4	B3
P203	A3	C1	R8063	C2	C3
P203	A5	C1	R8065	C1	C3
P203	H1	C1			
P203	H3	C1	TP10	C4	A1
			TP70	C1	A3
Q1022	D5	A1	TP80	C3	C3
Q1025	D4	A1	TP81	C3	C3
Q1026	C4	A1	TP82	C3	C3
Q1027	D4	A1	TP83	C3	C3
Q2010	A4	A1	TP84	C3	C3
Q2013	A4	A1	TP85	C3	C3
Q2015	B4	A1	TP86	C2	C3
Q2017	B4	A1	TP87	C3	C3
Q7041	H3	B2	TP88	F4	C3
Q7042	G4	B2	TP89	B1	C3
Q8069	C2	C3	TP90	C1	C3
R1011	D5	A1	U1040C	C3	B1
R1012	D4	A1	U2020	C4	A1
R1013	B4	A1	U2020B	C5	A1
R1014	D4	A1	U2020C	E5	A1
R1017	D5	A1	U2020D	E5	A1
R1030	D4	A1	U3020A	B4	A1
R2027	D4	B1	U3020B	E4	A1
R2029	F3	B1	U3030A	F4	B2
R2037A	G4	B1	U3030B	F4	B2
R2037B	C5	B1	U3040D	F5	B2
R2037C	E5	B1	U4020A	C4	A2
R2037D	E5	B1	U4020C	G1	A2
R2037E	D4	B1	U4020D	E4	A2
R2037F	C4	B1	U4040B	G4	B2
R2037G	F5	B1	U5020A	F1	A2
R3011	B4	A2	U5020B	F1	A2
R3013	B4	A2	U5020C	F3	A2
R3015	B4	A2	U5040B	C3	B2
R3017	A4	A2	U5040C	C2	B2
R3033	G5	B1	U5050A	B1	C2
R3040C	F4	B2	U5050B	E4	C2
R3040D	F4	B2	U6020	E2	A2
R4033	G5	B2	U6030B	G4	B2
R4043	C2	C2	U6030C	F5	B2
R5031C	F2	B2	U6030D	F4	B2
R5031	D2	B2	U7020B	F2	B2
R5043	C2	C2	U7050	C1	C2
R5045	C3	C2	U7060	D2	C2
R5047	C3	C2	U8020	F1	A3
R6020	D2	A2	U8030A	E2	B3
R6035B	G4	B2	U8040	B3	B3
R6035C	F4	B2	U8050	A2	C3
R6035D	E4	B2	U8060	B3	C3
R6067	A1	C2			
R7036	H3	B3	Y6060	B1	C2

Partial A3 also shown on diagram 3B.

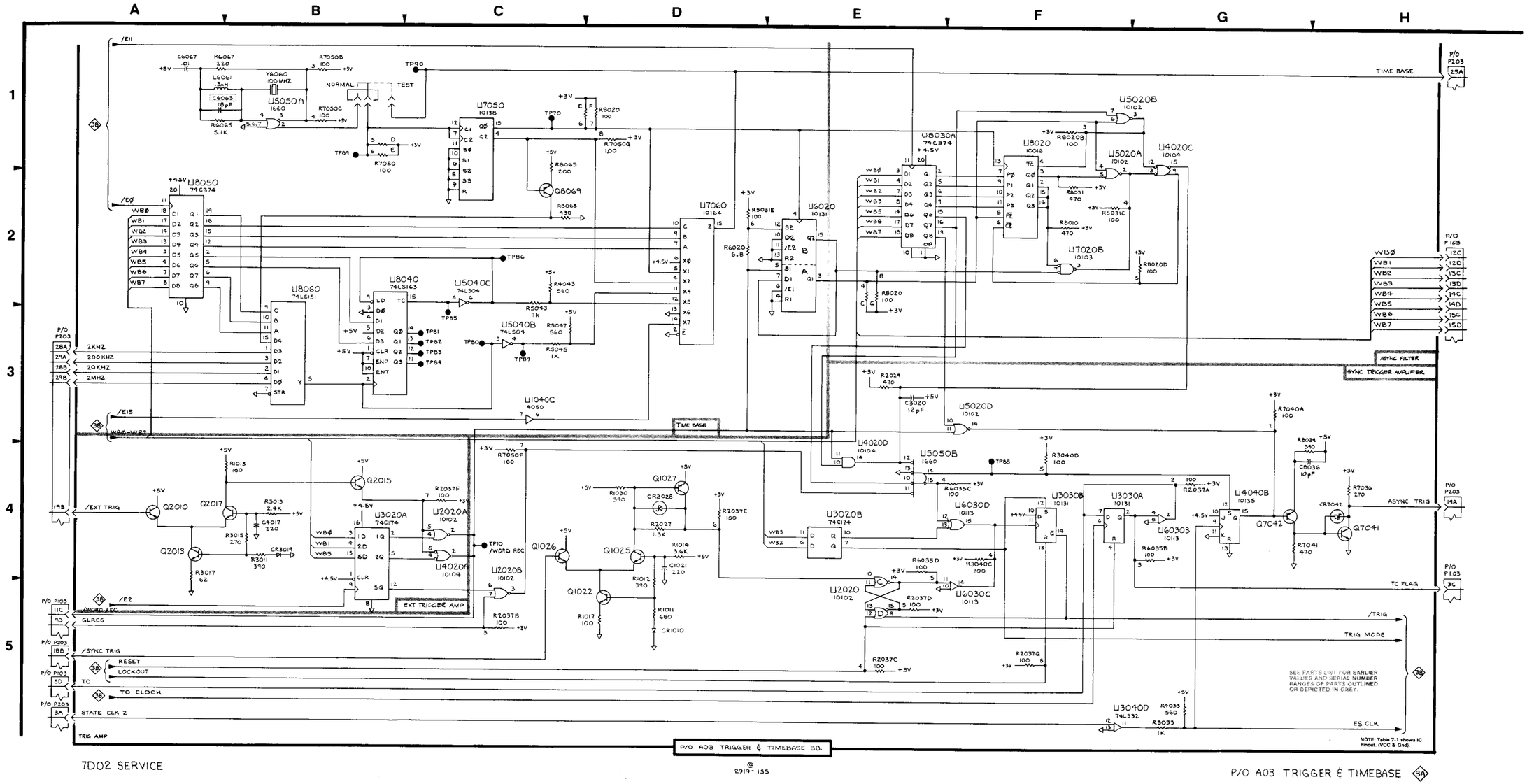
***See Parts List for serial number ranges.**

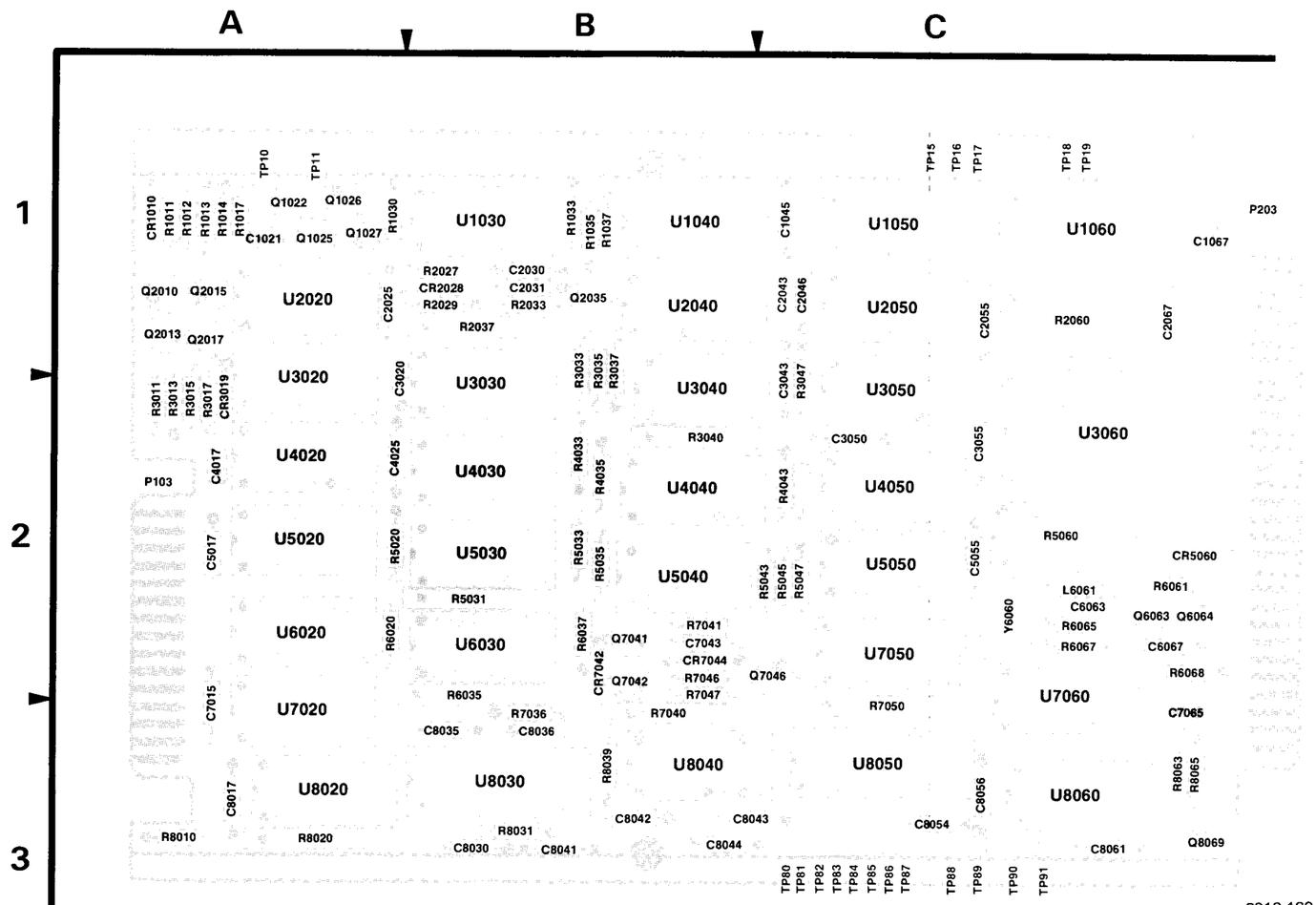
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
G
H
1
2
3
4
5
/E11
/E9
/E15
/E2
TIME BASE
TRIG AMP
P/O A03 TRIGGER & TIMEBASE BD.
SYNC TRIGGER AMPLIFIER
ASYNC FILTER
EXT TRIGGER AMP
NORMAL
TEST
2KHZ
200KHZ
20KHZ
2MHZ
/EXT TRIG
/WORD REC
GLRCG
/SYNC TRIG
RESET
LOCKOUT
TC
TO CLOCK
STATE CLK 2
TIME BASE
ASYNC TRIG
TC FLAG
/TRIG
TRIG MODE
ES CLK
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
U8050 74C374
U8060 74LS151
U8040 74LS163
U5040C 74LS04
U5040B 74LS04
U1040C 4050
U7050 10136
U7060 10164
U6020 10131
U8030A 74C374
U8020 10016
U5020B 10102
U5020A 10102
U4020C 10104
U7020B 10103
U4020D 10104
U5020D 10102
U5050B 1660
U6030D 10113
U6030B 10113
U6030C 10113
U3020B 74C174
U3020A 74C174
U3030B 10131
U3030A 10131
U4040B 10135
U3040D 74LS32
U7042
U7041
Q8069
Q2010
Q2013
Q2015
Q2017
Q1027
Q1026
Q1025
Q1022
U7020
U2020A 10102
U2020B 10102
U4020A 10104
P/O P203
P/O P103
P/O P108



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Static Sensitive Devices
See Maintenance Section

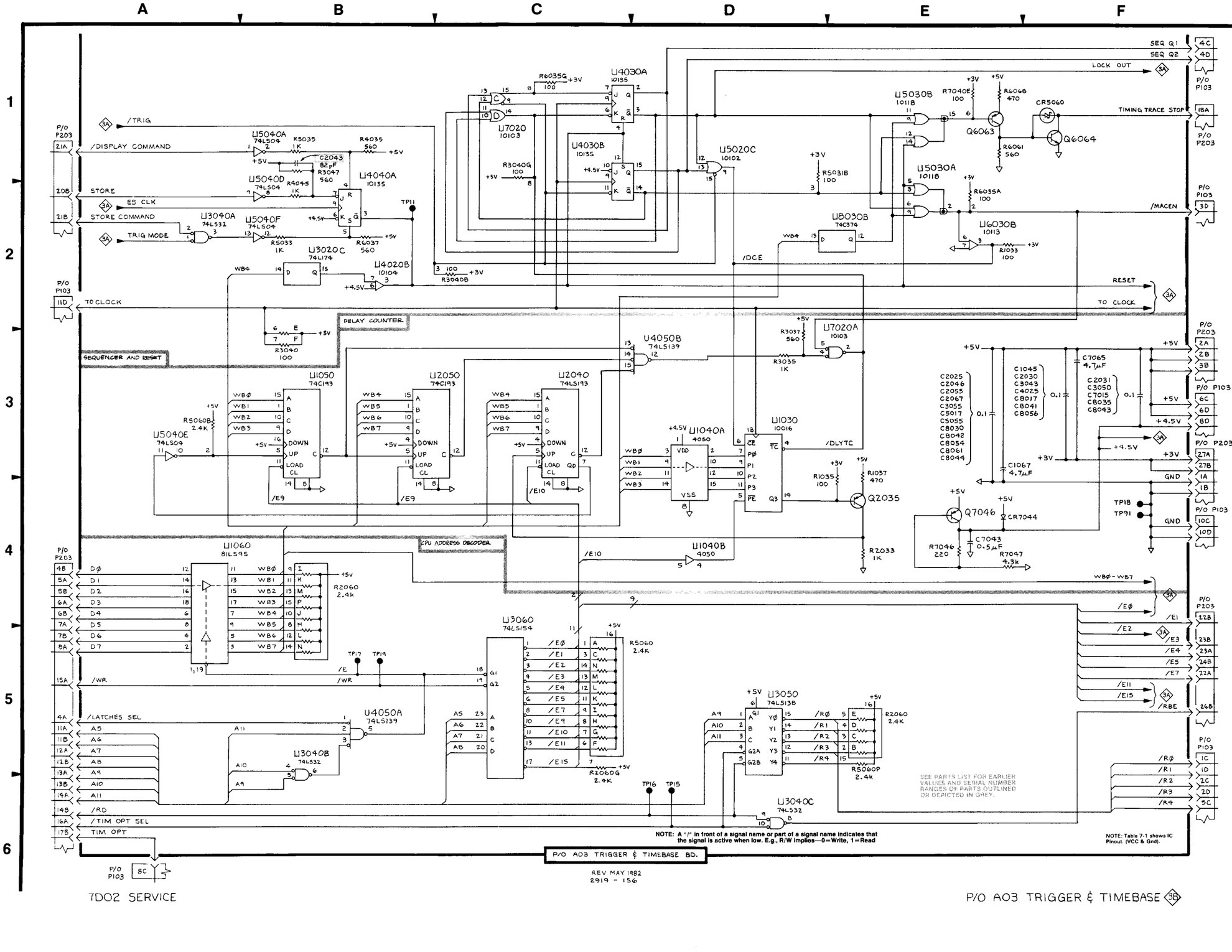
COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

@

Figure 7-3B. A03 Option 1 Trigger board component locations.


A
B
C
D
E
F
1
2
3
4
5
6
/TRIG
/DISPLAY COMMAND
STORE
ES CLK
STORE COMMAND
TRIG MODE
TO CLOCK
/DCE
/MACEN
TIMING TRACE STOP
LOCK OUT
RESET
TO CLOCK
SEQ Q1
SEQ Q2
/DLYTC
DELAY COUNTER
SEQUENCER AND RESET
CPU ADDRESS DECODER
/WR
/RD
/LATCHES SEL
/TIM OPT SEL
TIM OPT
WB0 - WB7
/E0
/E1
/E2
/E3
/E4
/E5
/E7
/E10
/E11
/E15
/RBE
/R0
/R1
/R2
/R3
/R4
U5040A
U5040D
U5040E
U5040F
U4040A
U3040A
U3040B
U3020C
U4020B
U4030A
U4030B
U5020C
U5030B
U5030A
U6030B
U8030B
U7020
U7020A
U4050B
U1050
U2050
U2040
U1030
U1040A
U1040B
U1060
U3060
U4050A
U3050
U3040C
Q6063
Q6064
Q2035
Q7046
CR5060
CR7044
TP11
TP16
TP15
TP17
TP19
TP18
TP91
P/O P203
P/O P103
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A03 TRIGGER & TIMEBASE BD.
REV MAY 1982
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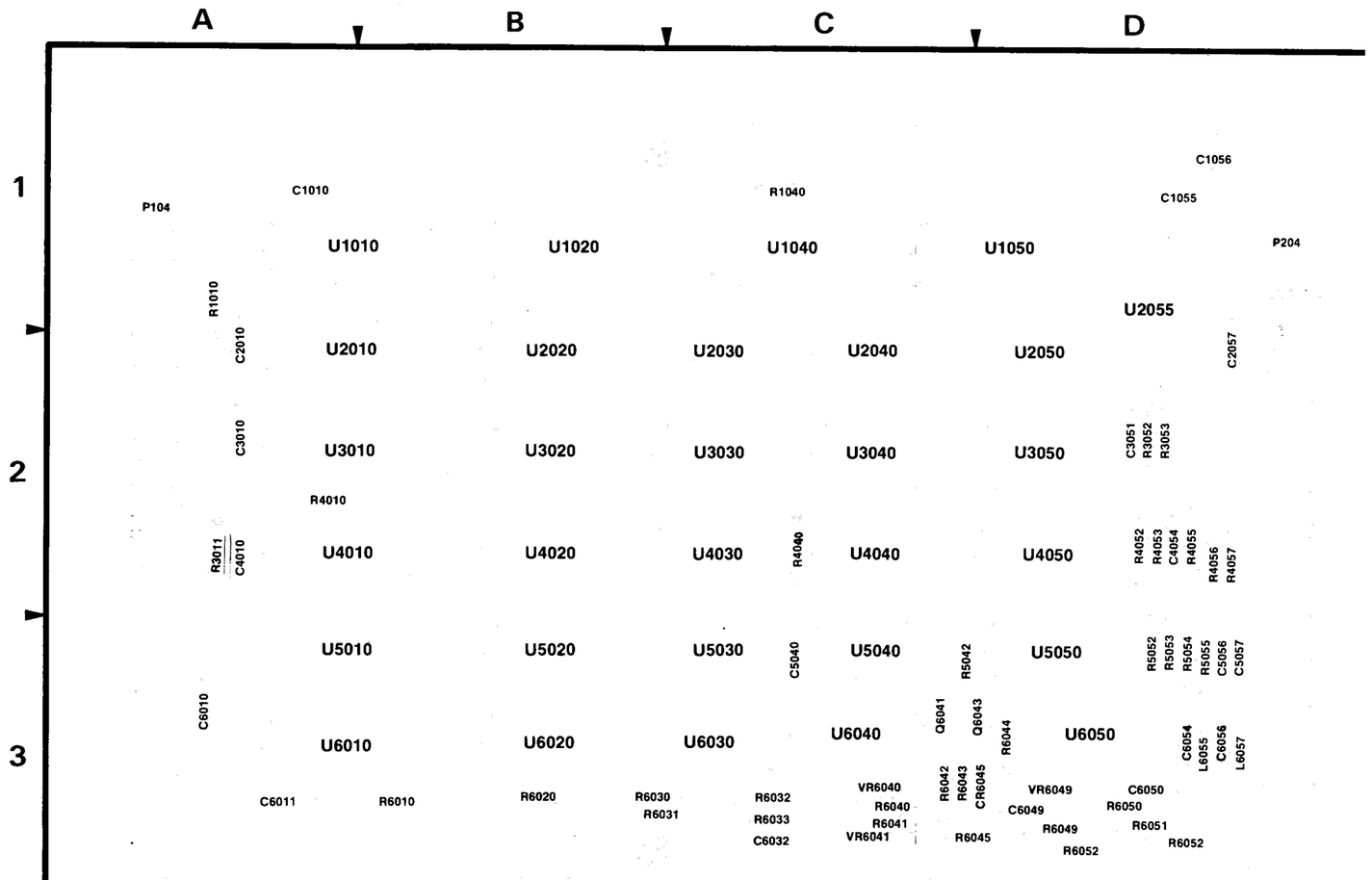

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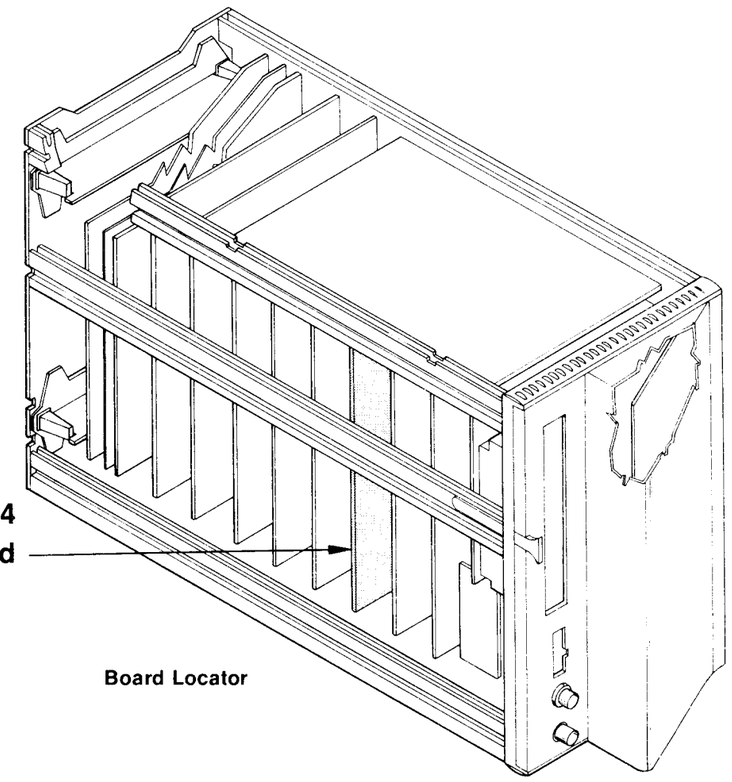
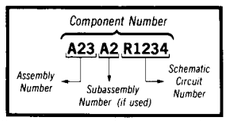


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

@

Figure 7-4A. A04 Front end board component locations 670-5989-01.

P/O A4 FRONT END DIAGRAM 4A

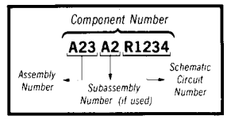
ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C5056	E3	D3	TP41	C2	A1
C5057	E2	D3	TP42	B3	A1
CR6045	D1	D3	U1010	B5	A1
			U1020	B2	B1
P104	A1	A1	U2010A	B5	A2
P104	A5	A1	U2010B	E3	A2
P104	A6	A1	U3010	C5	A2
P204	A2	D1	U4030B	B3	C2
P204	A6	D1	U4030C	A4	C2
P204	F2	D1	U4040A	D2	C2
			U4040B	B3	C2
Q6041	D1	C3	U4040C	B3	C2
Q6043	B2	D3	U5010C	D5	A3
			U5010D	B1	A3
R1010	A4	A1	U5020A	D6	B3
R1040	F5	C1	U5020B	E3	B3
R3053	D2	D2	U5020C	C3	B3
R4052	A4	D2	U5020D	D2	B3
R4053	A4	D2	U5030	C2	C3
R4055	C3	D2	U5040A	E3	C3
R4056	E3	D2	U5040B	E3	C3
R4057	E4	D2	U5050A	D2	D3
R5042	B2	C3	U5050B	D3	D3
R5052	C2	D3	U6010A	B6	A3
R5053	B1	D3	U6010F	D5	A3
R5054	B1	D3	U6010H	E5	A3
R5055	C1	D3	U6020A	B1	B3
R6010	B1	B3	U6020B	B1	B3
R6020	B1	B3	U6020C	C4	B3
R6030	C1	B3	U6020D	C2	B3
R6031	C2	B3	U6020E	C3	B3
R6032	C2	C3	U6020F	E2	B3
R6033	B2	C3	U6030A	D2	C3
R6040	B2	C3	U6030B	D5	C3
R6041	B2	C3	U6040	C1	C3
R6042	C1	C3	U6050	D2	D3
R6043	D1	C3	U6050	D3	D3
R6044	D1	D3			
R6045	C2	C3	VR6040	B2	C3
R6049	D3	D3	VR6041	B1	C3
R6050	D3	D3	VR6049	D1	D3
R6051	D3	D3			
R6052	D3	D3			
R6043	E4	D3			

Partial A4 also shown on diagram 4B.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

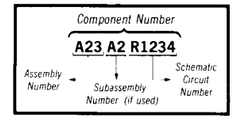
P/O A4 FRONT END DIAGRAM 4A

ASSEMBLY A4

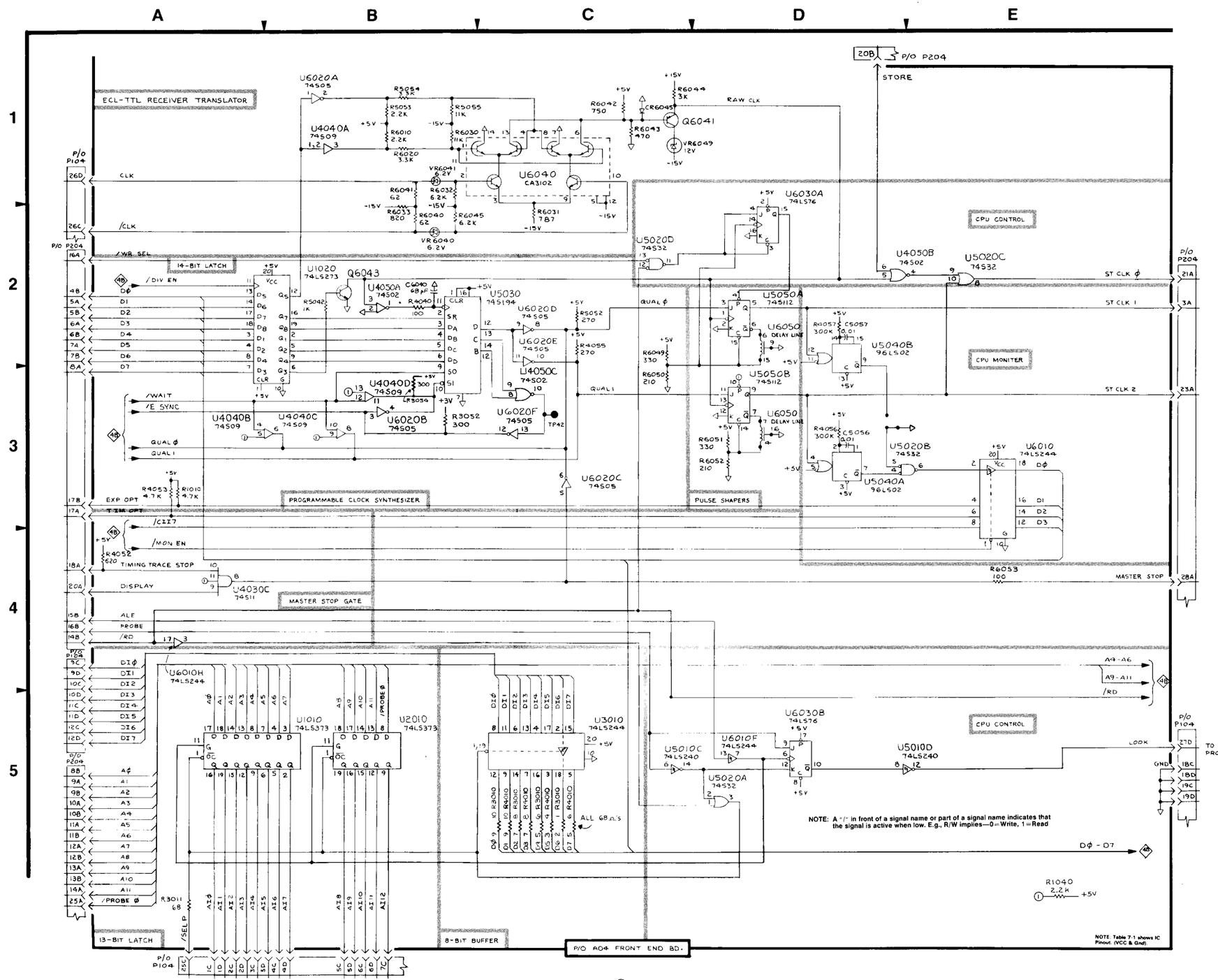
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR6045	C1	D4	R6045	B2	D4
			R6049	C2	D4
C5056	D3	E3	R6050	C3	E4
C5057	D2	E3	R6051	D3	E4
C6040	B2	C3	R6052	D3	D4
			R6053	E4	E4
P104	A1	A1			
P104	A4	A1	U1010	A5	B1
P104	A5	A1	U1020	B2	B1
P104	E5	A1	U2010	B5	B2
P204	A2	E1	U3010	C5	B2
P204	A5	E1	U4030C	A4	C3
P204	D1	E1	U4040A	B1	D3
P204	E2	E1	U4040B	A3	D3
			U4040C	B3	D3
Q6041	C1	D3	U4040D	B3	D3
Q6043	B2	D3	U4050B	D2	D3
			U4050C	C3	D3
R1010	A3	A2	U5010C	C5	B3
R1040	E5	C1	U5010D	E5	B3
R3010	C5	B2	U5020A	D5	B3
R3011	A5	A2	U5020B	D3	B3
R3052	B3	E2	U5020C	E2	B3
R3054	B3	E2	U5020D	C2	B3
R4010	C5	A2	U5030	B2	C3
R4040	B2	C3	U5040A	D3	D3
R4052	A4	E3	U5040B	D2	D3
R4053	A3	E3	U5050A	D2	D3
R4055	C2	E3	U5050B	D3	D3
R4056	D3	E3	U6010	E3	B3
R4057	D2	E3	U6010F	D5	B3
R5042	B2	D3	U6010H	A4	B3
R5052	C2	E3	U6020A	B1	B3
R5053	B1	E3	U6020B	B3	B3
R5054	B1	E3	U6020C	C3	B3
R5055	B1	E3	U6020D	C2	B3
R6010	B1	B4	U6020E	C2	B3
R6020	B1	B4	U6020F	C3	B3
R6030	B1	C4	U6030A	D2	C3
R6031	C2	C4	U6030B	D5	C3
R6032	B1	C4	U6040	C1	D3
R6033	B2	C4	U6050	D2	D3
R6040	B2	D4	U6050	D3	D3
R6041	B1	D4			
R6042	C1	D4	VR6040D	B2	D4
R6043	C1	D4	VR6041	B1	D4
R6044	C1	D3	VR6049	C1	D4

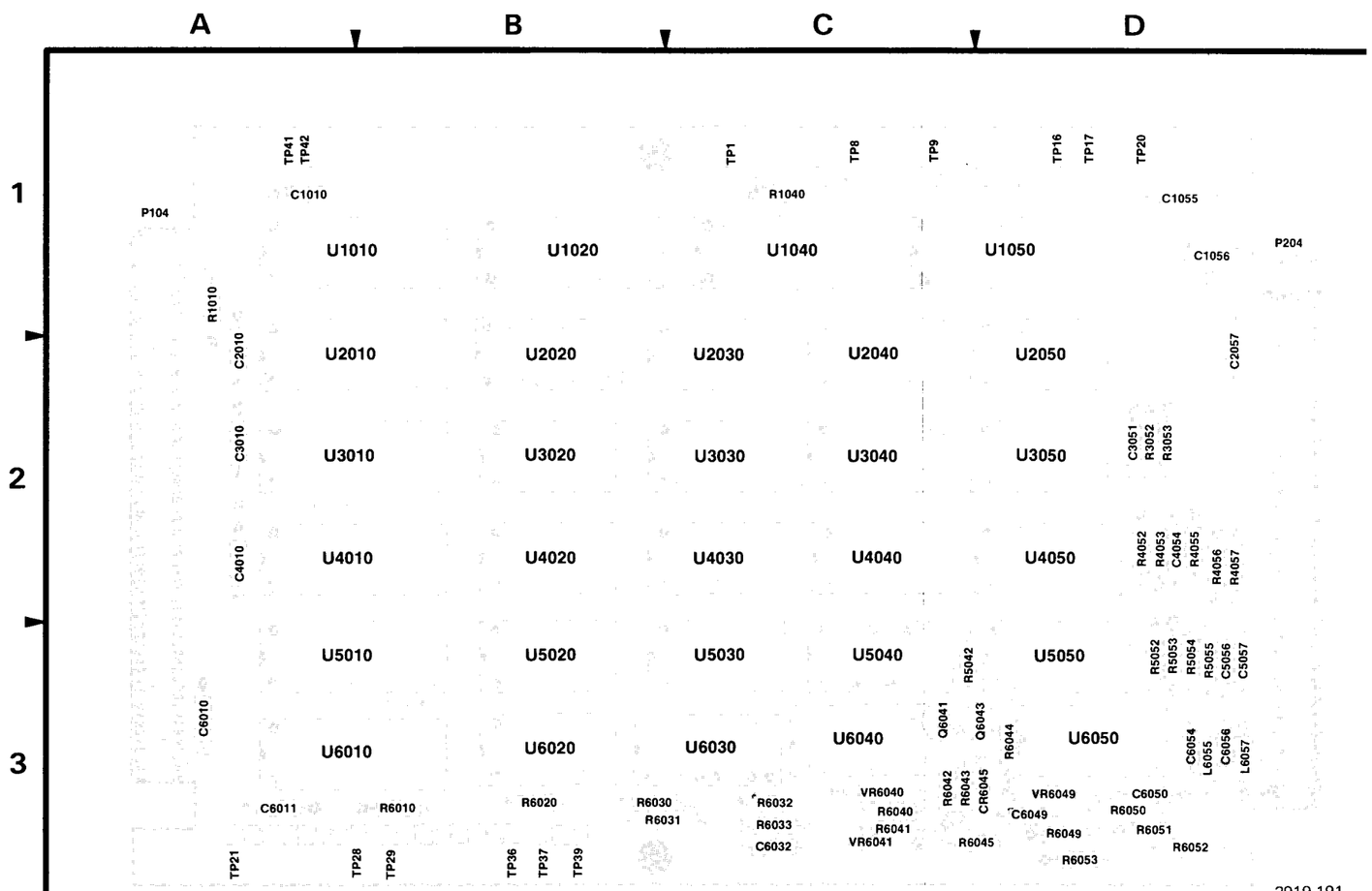
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
1
2
3
4
5
ECL-TTL RECEIVER TRANSLATOR
U6020A 74S05
U4040A 74S09
R5054 5K
R5053 2.2K
R5055 11K
R6010 2.2K
R6020 3.3K
R6030 11K
+5V
-15V
R6042 750
+15V
R6044 3K
CR6045
RAW CLK
Q6041
R6043 470
VR6049 12V
U6040 CA3102
VR6041 6.2V
R6041 62
R6032 6.2K
R6033 820
R6040 62
R6045 6.2K
R6031 787
VR6040 6.2V
P/O P104
26D
CLK
26C
/CLK
P/O P204
16A
/WR SEL
14-BIT LATCH
U1020 74LS273
Q6043
U4050A 74S02
C6040 68pF
R4040 100
R5042 1K
U5030 74S194
U6020D 74S05
U6020E 74S05
U4050C 74S02
R5052 270
R4055 270
U4040D 74S09
R3050 300
U6020B 74S05
U4040B 74S09
U4040C 74S09
R3052 300
U6020F 74S05
TP42
U6020C 74S05
/DIV EN
D0
D1
D2
D3
D4
D5
D6
D7
CLR
/WAIT
/E SYNC
QUAL φ
QUAL 1
PROGRAMMABLE CLOCK SYNTHESIZER
R4053 4.7K
R1010 4.7K
EXP OPT
TIM OPT
17B
17A
/CLK7
/MON EN
R4052 620
18A
TIMING TRACE STOP
20A
DISPLAY
U4030C 74S11
MASTER STOP GATE
15B
ALE
16B
PROBE
/RD
P/O P104
9C
DI0
9D
DI1
10C
DI2
10D
DI3
11C
DI4
11D
DI5
12C
DI6
12D
DI7
U6010H 74LS244
U1010 74LS373
U2010 74LS373
U3010 74LS244
R3010
R4010
ALL 68Ω's
P/O P204
8B
A0
9A
A1
9B
A2
10A
A3
10B
A4
11A
A5
11B
A6
12A
A7
12B
A8
13A
A9
13B
A10
14A
A11
25A
/PROBE 0
R3011 68
/SELP
13-BIT LATCH
P/O P104
25C
1C
1D
2C
2D
3C
3D
4C
4D
5C
5D
6C
6D
7C
8-BIT BUFFER
P/O A04 FRONT END BD.
20B
P/O P204
STORE
CPU CONTROL
U6030A 74LS76
U5020D 74S32
U4050B 74S02
U5020C 74S32
P/O P204
21A
ST CLK 0
3A
ST CLK 1
23A
ST CLK 2
CPU MONITER
U5050A 74S112
U6050 DELAY LINE
U5050B 74S112
U5040B 96LS02
R6049 330
R6050 210
R6051 330
R6052 210
R4057 300K
C5057 .01
R4056 300K
C5056 .01
U5020B 74S32
U5040A 96LS02
U6010 74LS244
D0
D1
D2
D3
PULSE SHAPERS
R6053 100
MASTER STOP
28A
A9-A6
A9-A11
/RD
U6030B 74LS76
U6010F 74LS244
U5010C 74LS240
U5020A 74S32
U5010D 74LS240
CPU CONTROL
LOOK
GND
P/O P104
27D
18C
18D
19C
19D
TO PROBE
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
D0 - D7
R1040 2.2K
+5V
NOTE: Table 7-1 shows IC Pinout (VCC & Gnd).



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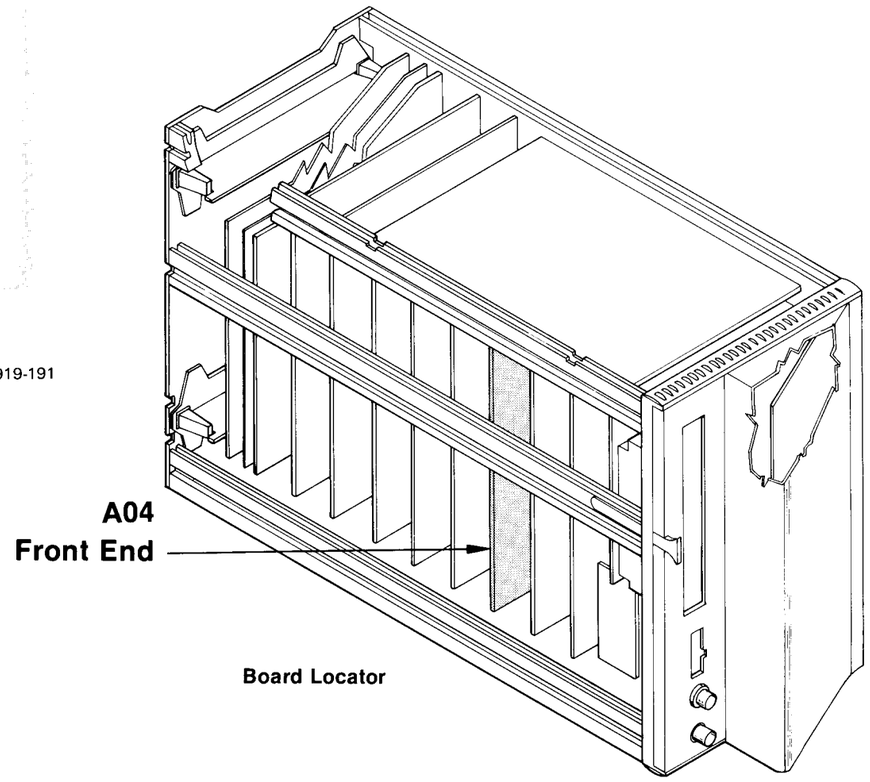
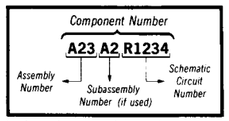


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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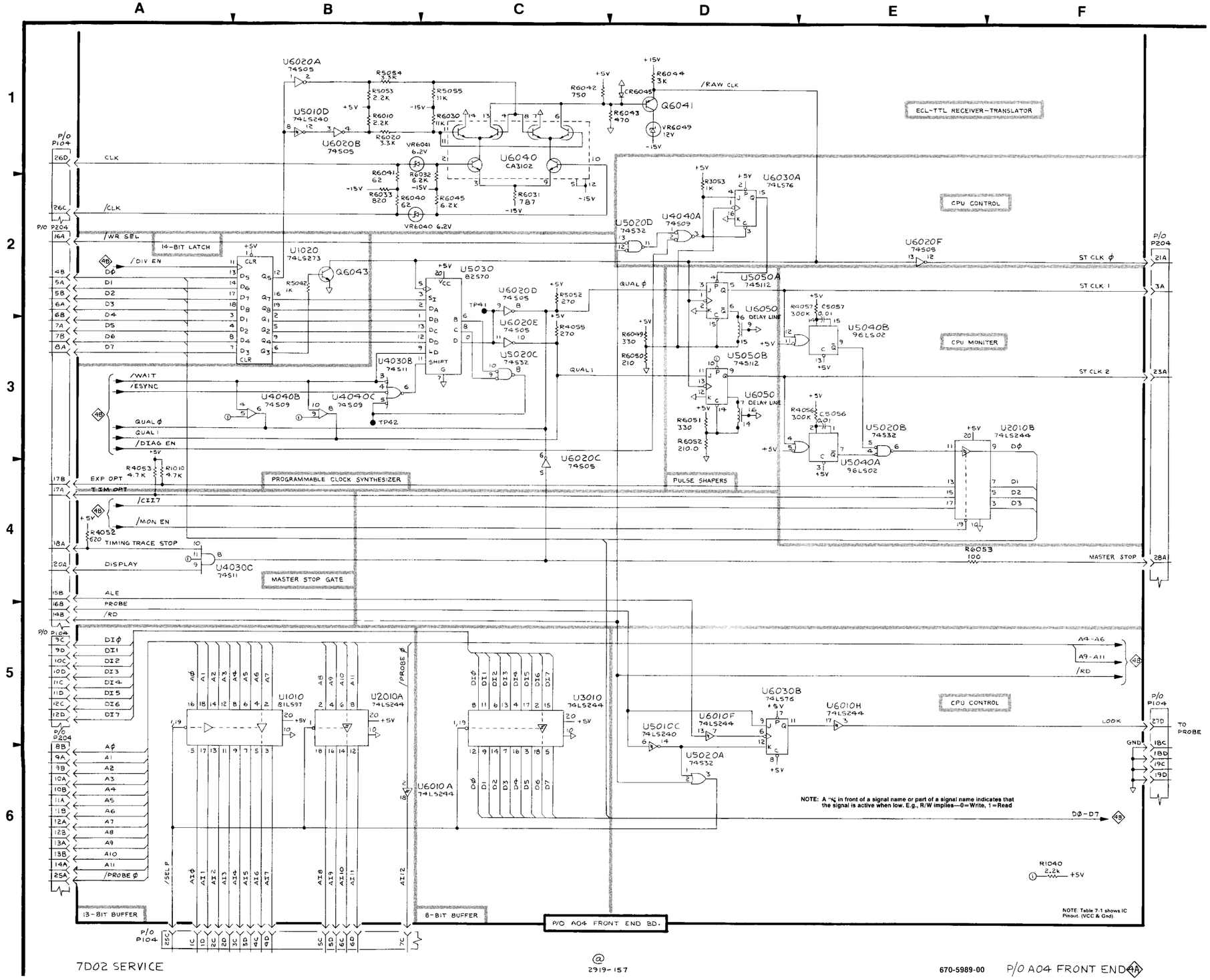
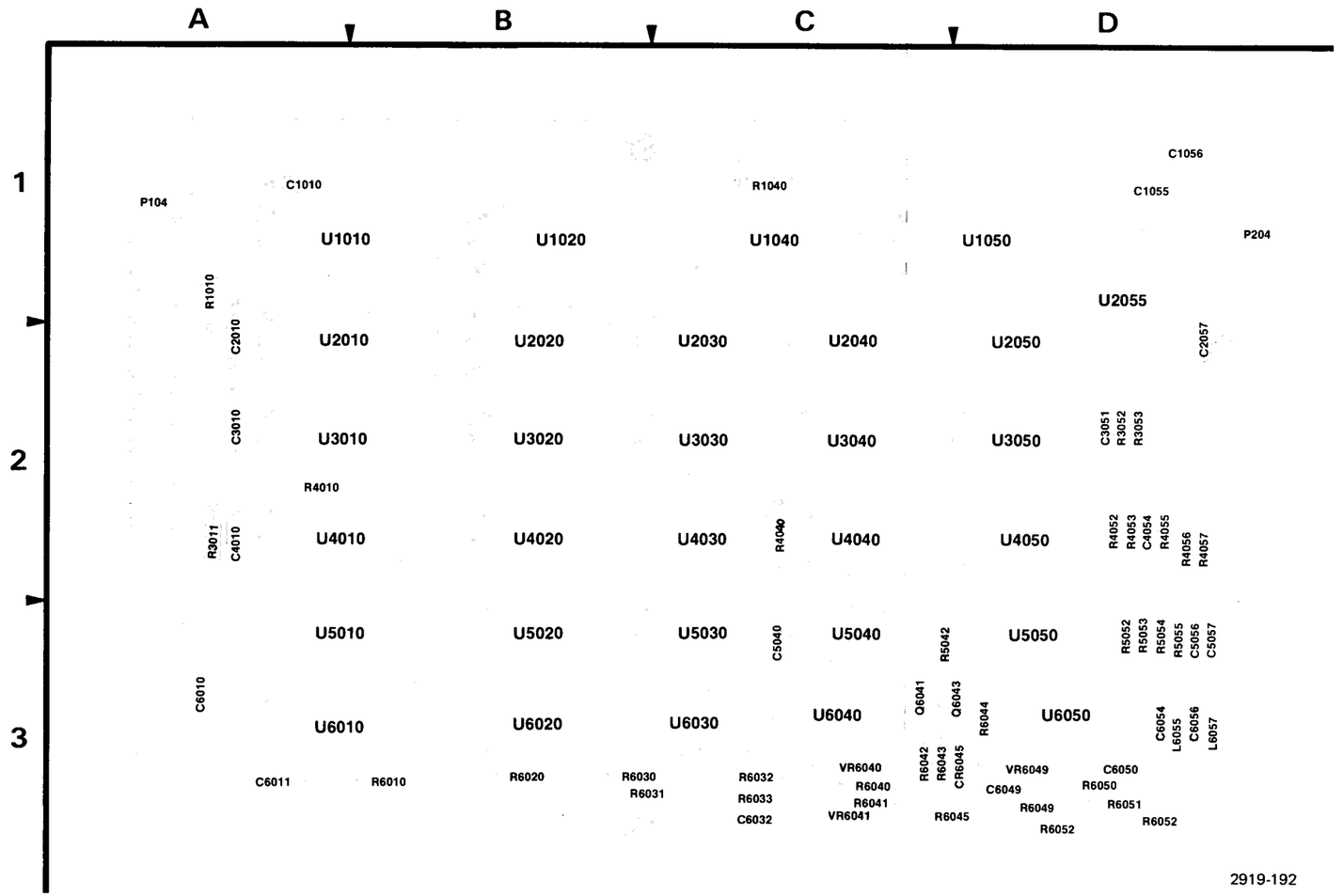
Figure 7-4A. A04 Front end board component locations 670-5989-00.


ECL-TTL RECEIVER-TRANSLATOR
CPU CONTROL
CPU MONITER
PROGRAMMABLE CLOCK SYNTHESIZER
PULSE SHAPERS
MASTER STOP GATE
14-BIT LATCH
13-BIT BUFFER
8-BIT BUFFER
P/O A04 FRONT END BD.
/RAW CLK
CLK
/CLK
/WR SEL
/DIV EN
/WAIT
/ESYNC
QUAL Φ
QUAL I
/DIAG EN
EXP OPT
TIM OPT
/CII7
/MON EN
TIMING TRACE STOP
DISPLAY
ALE
PROBE
/RD
/SEL P
/PROBE Φ
ST CLK Φ
ST CLK 1
ST CLK 2
MASTER STOP
LOOK
TO PROBE
A4-A6
A9-A11
D0-D7
NOTE: A ~ in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd)



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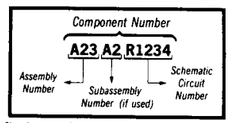
A04 FRONT END BOARD
670-5989-01

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

Figure 7-4B. A04 Front end board component locations.

P/O A5 WORD RECOGNIZER DIAGRAM 5A

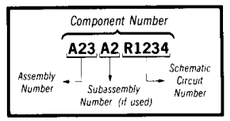
ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1015	F3	B1
C1032	F3	C1
C1041	F3	D1
C1050	F3	D1
C3021	F3	B1
C3041	F3	D1
C4008	F3	A2
C4031	F3	C2
C5055	F3	D2
C6021	F3	B2
C7051	F3	D3
C8011	F3	A3
C8015	F3	B3
P105	F5	A2
P205	A1	D2
P205	F1	D2
R5041	A1	C3
R5051	A2	D3
R8023	F1	B3
TP9	E4	C3
TP10	E4	C3
TP11	D4	C3
TP12	D4	C3
TP13	B4	D3
TP14	B4	D3
TP15	B4	D3
TP16	B4	D3
TP25	C4	C3
TP26	C4	C3
TP27	C4	C3
TP28	C4	C3
TP29	B3	D3
TP31	B3	D3
U4010	E4	A2
U4030	F2	C2
U5020	F1	B2
U5050	A3	D2
U6020	D4	B2
U6030	B4	C2
U6050	B2	D2
U7040A	F2	C3
U7040B	F3	C3
U7050B	E3	D3
U7050C	E2	D3
U8010	C4	A3

Partial A5 also shown on diagram 5B.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



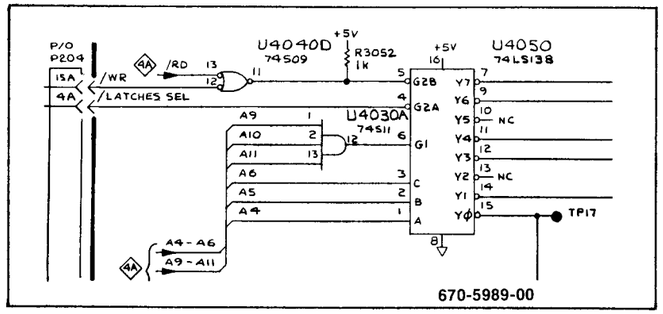
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A4 FRONT END DIAGRAM 4B

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	A2	A1	TP19	E1	D1
C1055	A2	D1	TP20	E5	D1
C1056	A2	D1	TP21	A5	D1
C2010	A2	A2	TP22	C5	D1
C2057	A2	D2	TP23	B5	D1
C3010	A2	A2	TP24	C5	D1
C3051	A2	D2	TP25	C5	D1
C4010	A2	A2	TP26	C5	D1
C4054	A2	D2	TP27	A5	D1
C6010	A2	A3	TP28	B5	B3
C6011	A2	A3	TP29	A5	B3
C6050	A2	D3	TP31	A5	B3
C6054	A2	D3	TP33	D2	B3
C6056	A2	D3	TP34	D2	B3
			TP35	D2	B3
L6055	A2	D3	TP36	D2	B3
L6057	A2	D3	TP37	B5	B3
			TP38	A5	B3
P104	A3	A1	TP39	D5	B3
P104	F3	A1			
P204	A1	D1	U1040	B2	C1
			U1050	E2	D1
R1040	E5	C1	U2020	D2	B2
R3052 *	A1	D2	U2030	A5	C2
			U2040	C5	C2
TP1	B2	C1	U2050	E5	D2
TP2	B2	C1	U2055 *	B1	D2
TP3	B2	C1	U3020	D5	B2
TP4	B2	C1	U3030	B5	C2
TP5	B2	C1	U3040	C5	C2
TP6	B2	C1	U3050	F5	D2
TP7	B2	C1	U4010	A3	A2
TP8	B2	C1	U4020	D5	B2
TP9	E2	C1	U4030A	A1	C2
TP10	E2	C1	U4030B	A1	C2
TP11	E2	C1	U4040D	A1	C2
TP12	E2	D1	U4050 *	B1	D2
TP13	E2	D1	U5010	A4	A3
TP14	E2	D1	U5010A	C3	A3
TP15	E2	D1	U5010B	C3	A3
TP16	E2	D1	U6010E	E3	A3
TP17	B1	D1	U6010G	E3	A3
TP18	D1	D1			

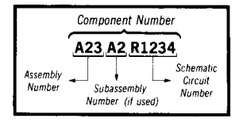
Partial A4 also shown in diagram 4A.



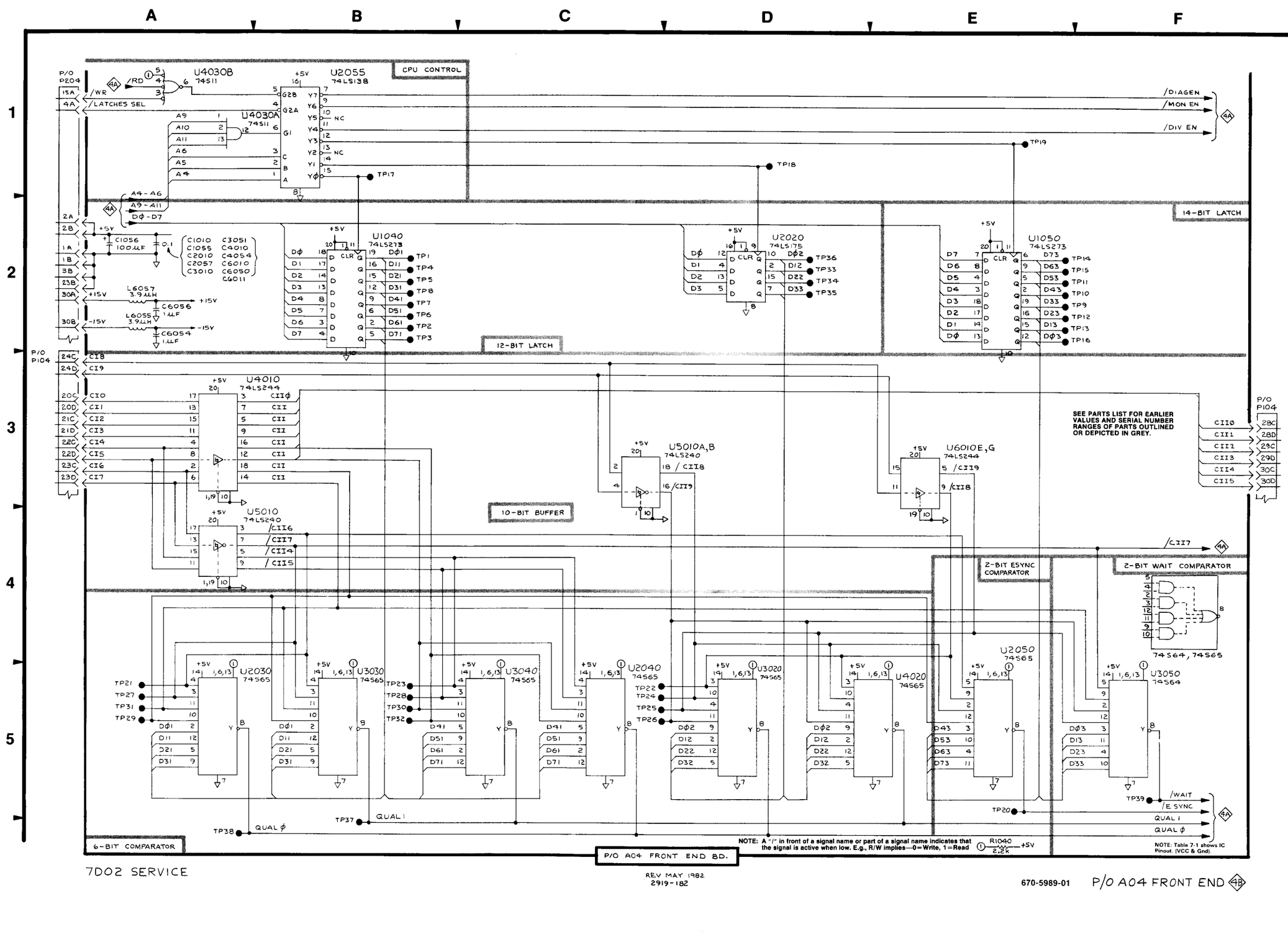
***See Parts List for serial number ranges.**

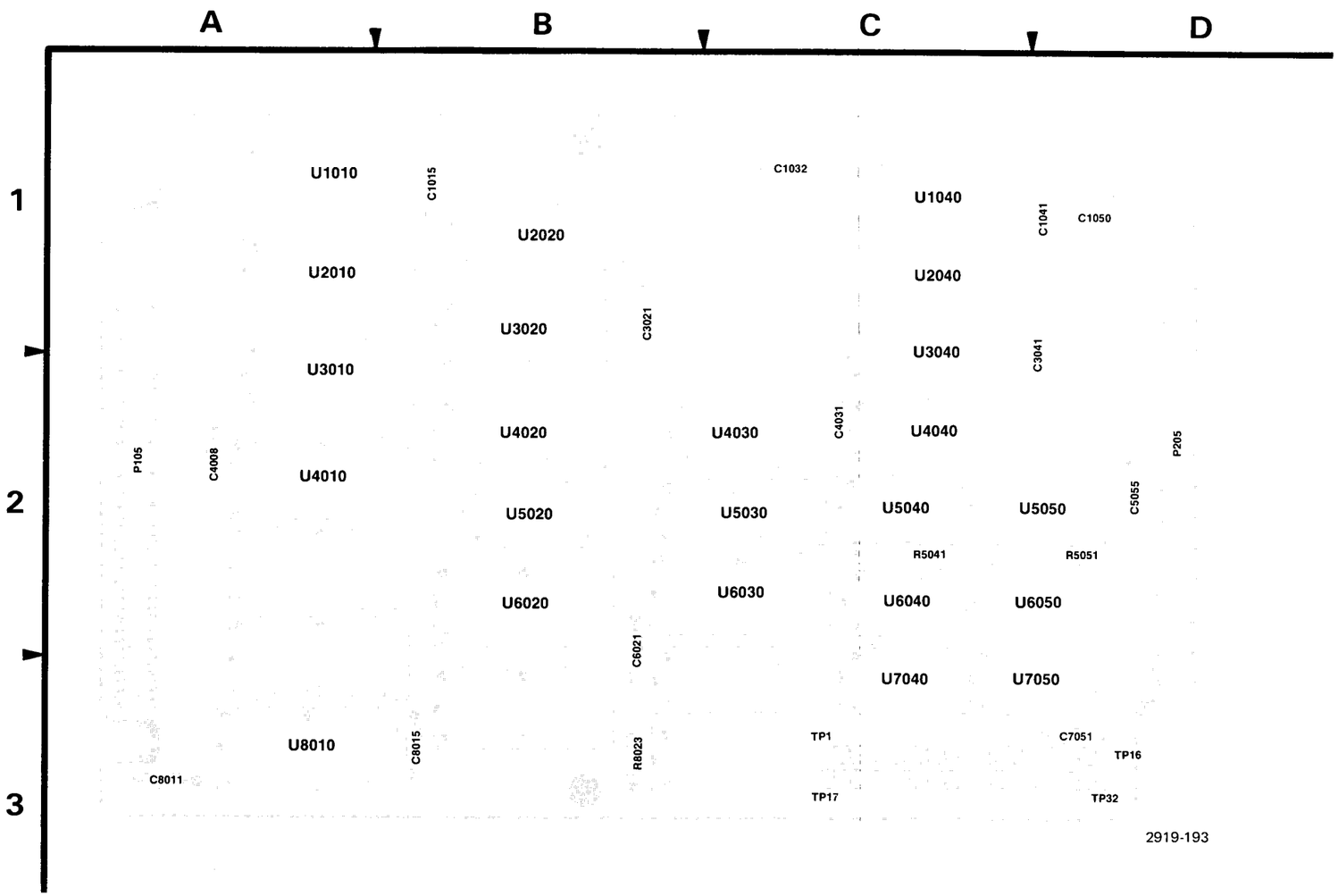
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

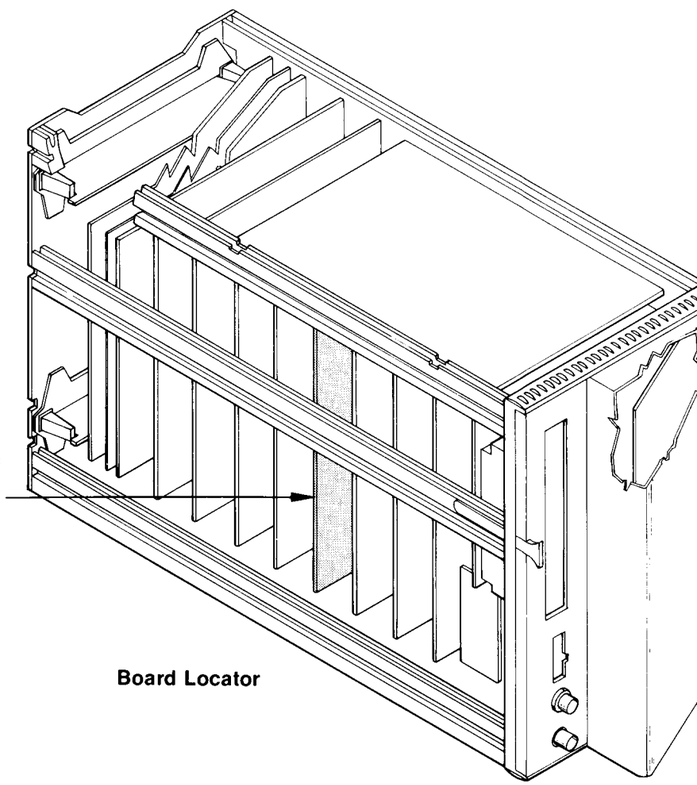


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
5
CPU CONTROL
14-BIT LATCH
12-BIT LATCH
10-BIT BUFFER
2-BIT ESYNC COMPARATOR
2-BIT WAIT COMPARATOR
6-BIT COMPARATOR
U4030B 74S11
U4030A 74S11
U2055 74LS138
U1040 74LS273
U2020 74LS175
U1050 74LS273
U4010 74LS294
U5010 74LS240
U5010A,B 74LS240
U6010E,G 74LS244
U2030 74S65
U3030 74S65
U3040 74S65
U2040 74S65
U3020 74S65
U4020 74S65
U2050 74S65
U3050 74S64
74S64, 74S65
/DIAGEN
/MON EN
/DIV EN
/WR
/LATCHES SEL
/RD
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39
QUAL I
QUAL Φ
/WAIT
/E SYNC
/CII7
P/O P204
P/O P104
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout (VCC & Gnd).
P/O A04 FRONT END BD.
REV MAY 1982
2919-182
7D02 SERVICE
670-5989-01
P/O A04 FRONT END

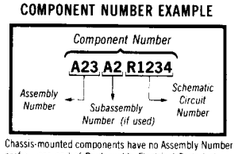


2919-193



Static Sensitive Devices
See Maintenance Section

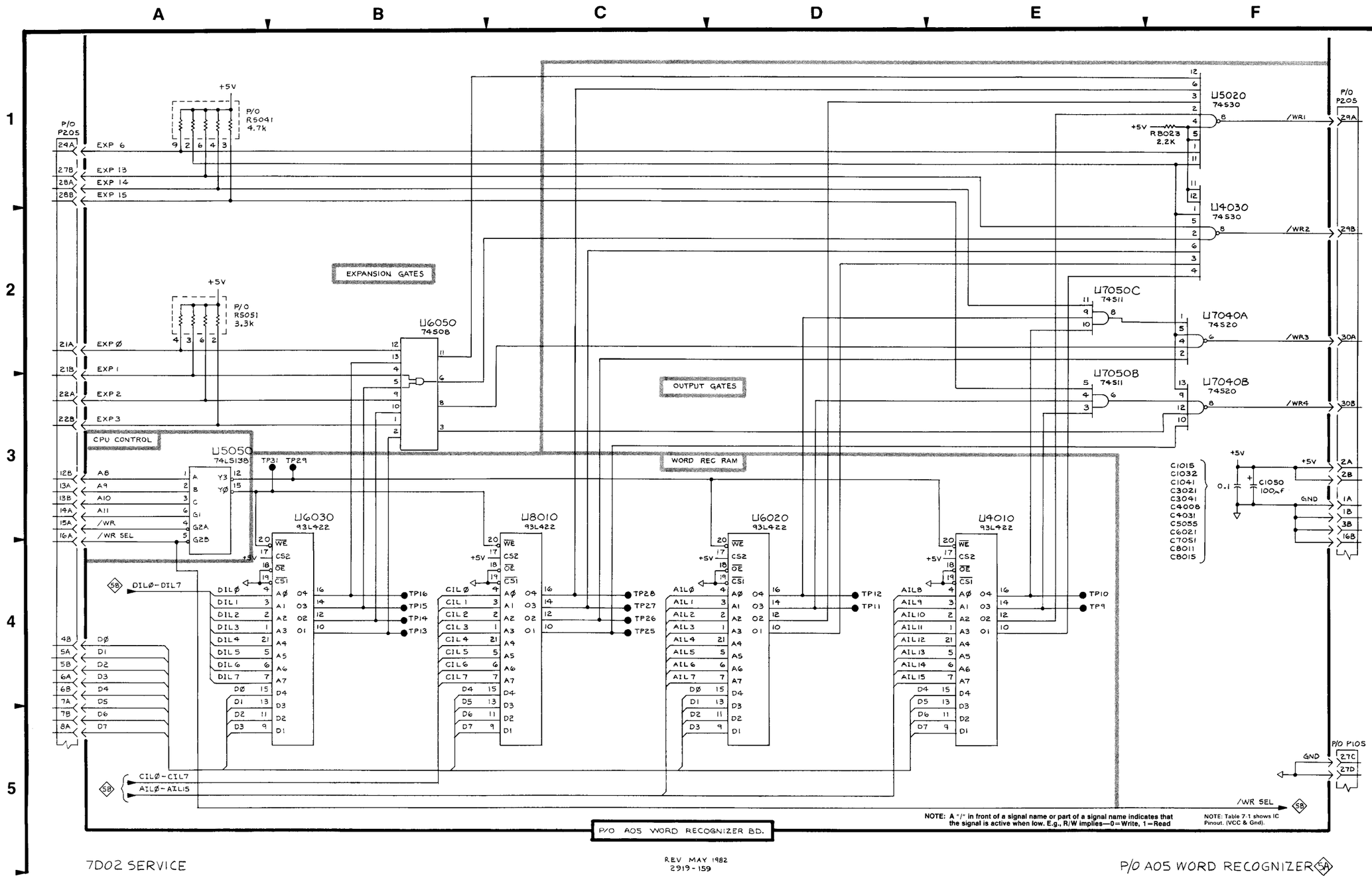
COMPONENT NUMBER EXAMPLE



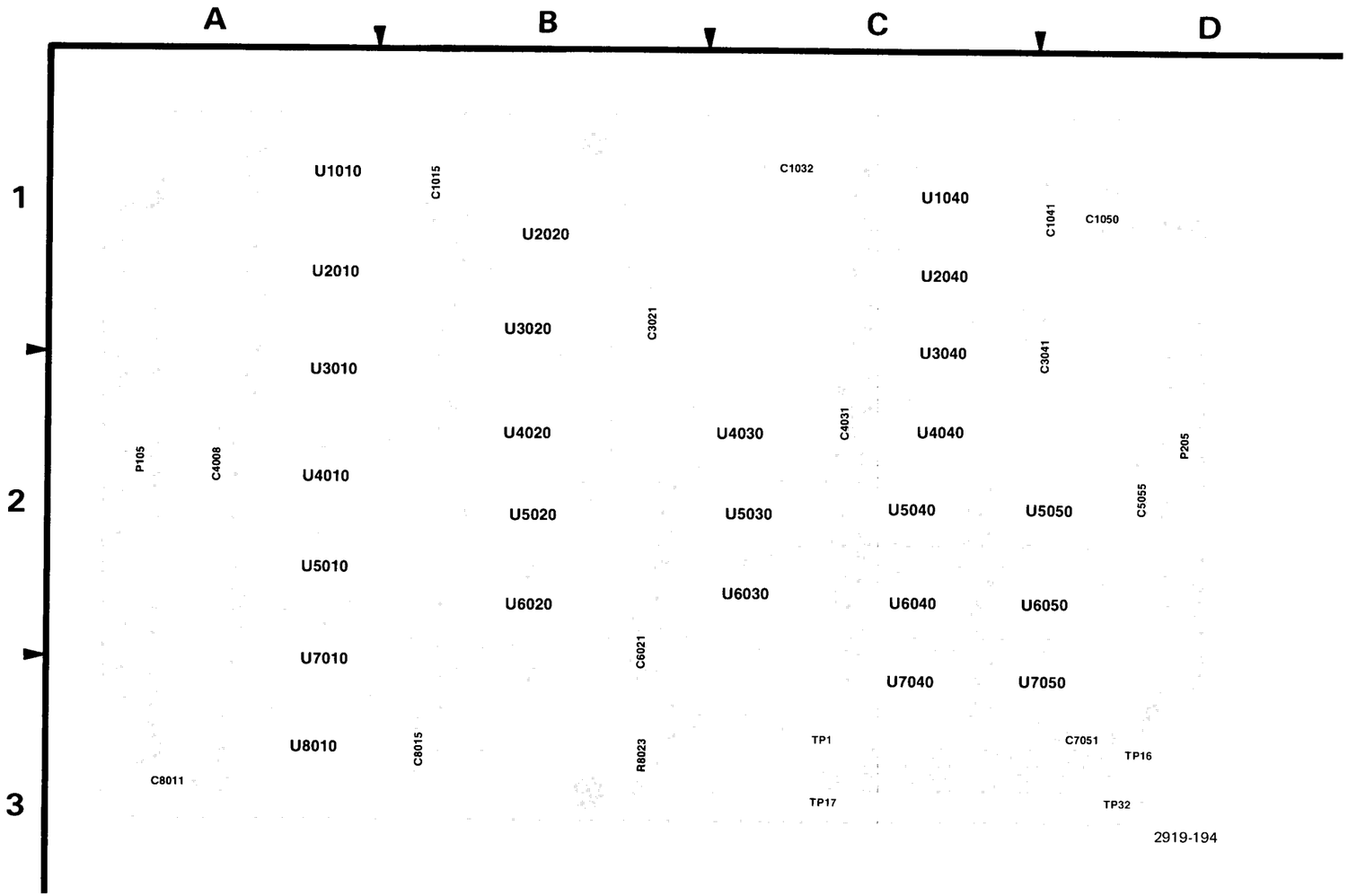
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

Figure 7-5A. A05 Word recognizer board component locations.



REV MAY 1982
2919-159



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

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Figure 7-5B. A05 Word recognizer board component locations.

A6 EXPANSION OPTION DIAGRAM 6

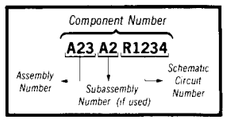
ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1011	F3	B1	TP26	E5	B3
C1041	F3	C1	TP27	E5	B3
C1051	F3	D1	TP28	E5	B3
C1059	F3	D1	TP29	E5	B3
C2021	F3	B2	TP30	E5	B3
C2031	F3	B2	TP31	E3	B3
C3041	F3	C2	TP32	E3	B3
C4011	F3	B2	TP33	E3	B3
C4013	F3	B2	TP34	E4	B3
C4039	F3	C2	TP35	E4	B3
C4041	F3	C2	TP36	E4	B3
C6011	F3	B3	TP37	E4	B3
C6051	F3	D3	TP38	E4	B3
			TP39	B2	B3
P106	A3	A2	TP40	B2	B3
P106	A5	A2	TP41	B2	B3
P106	F4	A2	TP42	B2	B3
P206	A1	D1	TP43	C2	B3
P206	A4	D1	TP44	C2	B3
P206	F2	D1	TP45	C2	B3
P206	F5	D1	TP46	C2	B3
TP1	D3	B1	U1010	B4	A1
TP2	D3	B1	U1030	C2	B1
TP3	D4	B1	U1040C	A4	C1
TP4	D4	B1	U1040D	C1	C1
TP5	D4	B1	U1040	B3	C1
TP6	D4	B1	U1050A	C1	C1
TP7	D4	B1	U1050B	B3	C1
TP8	D4	B1	U1050C	A4	C1
TP9	D2	B1	U2020	C4	B1
TP10	D2	B1	U2030	D1	B1
TP11	D2	C1	U2040	E1	C1
TP12	D2	C1	U3010	B3	A2
TP13	B3	C1	U3020	E3	B2
TP14	C3	C1	U3030	F1	B2
TP15	D5	B3	U3040	F1	C2
TP16	D5	B3	U3050	B2	D2
TP17	D5	B3	U4010	B5	A2
TP18	D5	B3	U4020	E5	B2
TP19	D5	B3	U4040	F5	C2
TP20	D5	B3	U4050	B2	D2
TP21	D5	B3	U5020	C5	B3
TP22	D5	B3	U5040	F3	C3
TP23	E5	B3	U5050D	A3	D3
TP24	E5	B3	U6010	B5	A3
TP25	E5	B3			

A06 OPTION 3 EXPANSION OPT. 6

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A5 WORD RECOGNIZER DIAGRAM 5B

ASSEMBLY A5

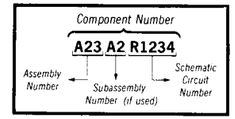
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P105	A1	A2
P105	F1	A2
P205	A5	D2
P205	C1	D2
R5041	A5	C3
U1010	B1	A1
U1040	E1	C1
U2010	B2	A1
U2020	C1	B1
U2040	E2	C1
U3010	B3	A2
U3020	C2	B1
U3040	E3	C1
U4020	C3	B2
U4040	E4	C2
U5030	C4	C2
U5040B	A5	C2
U5040C	B5	C2
U7050C	B5	D3

Partial A5 also shown on diagram 5A.

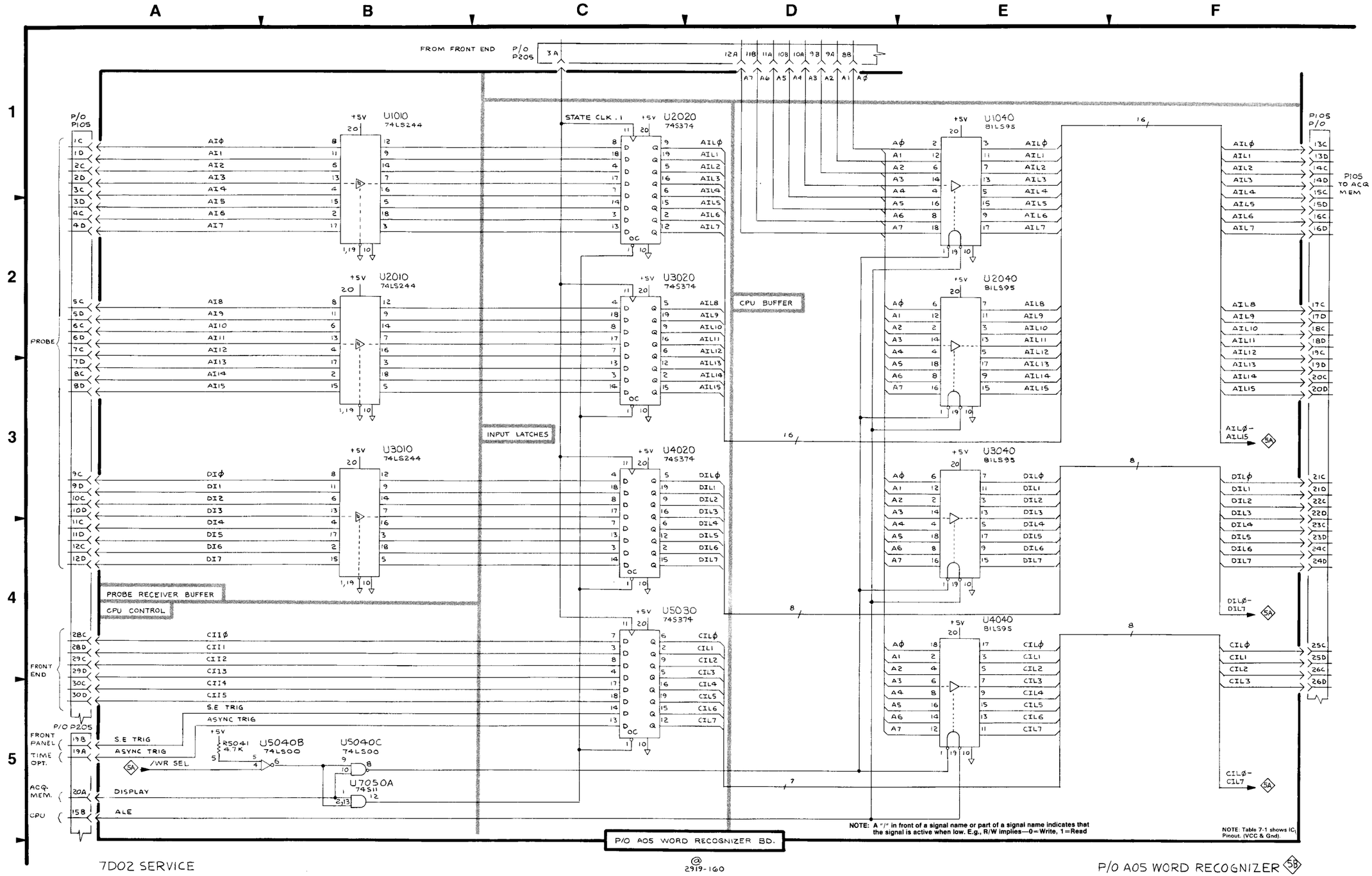
A05 WORD RECOGNIZER 5B

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



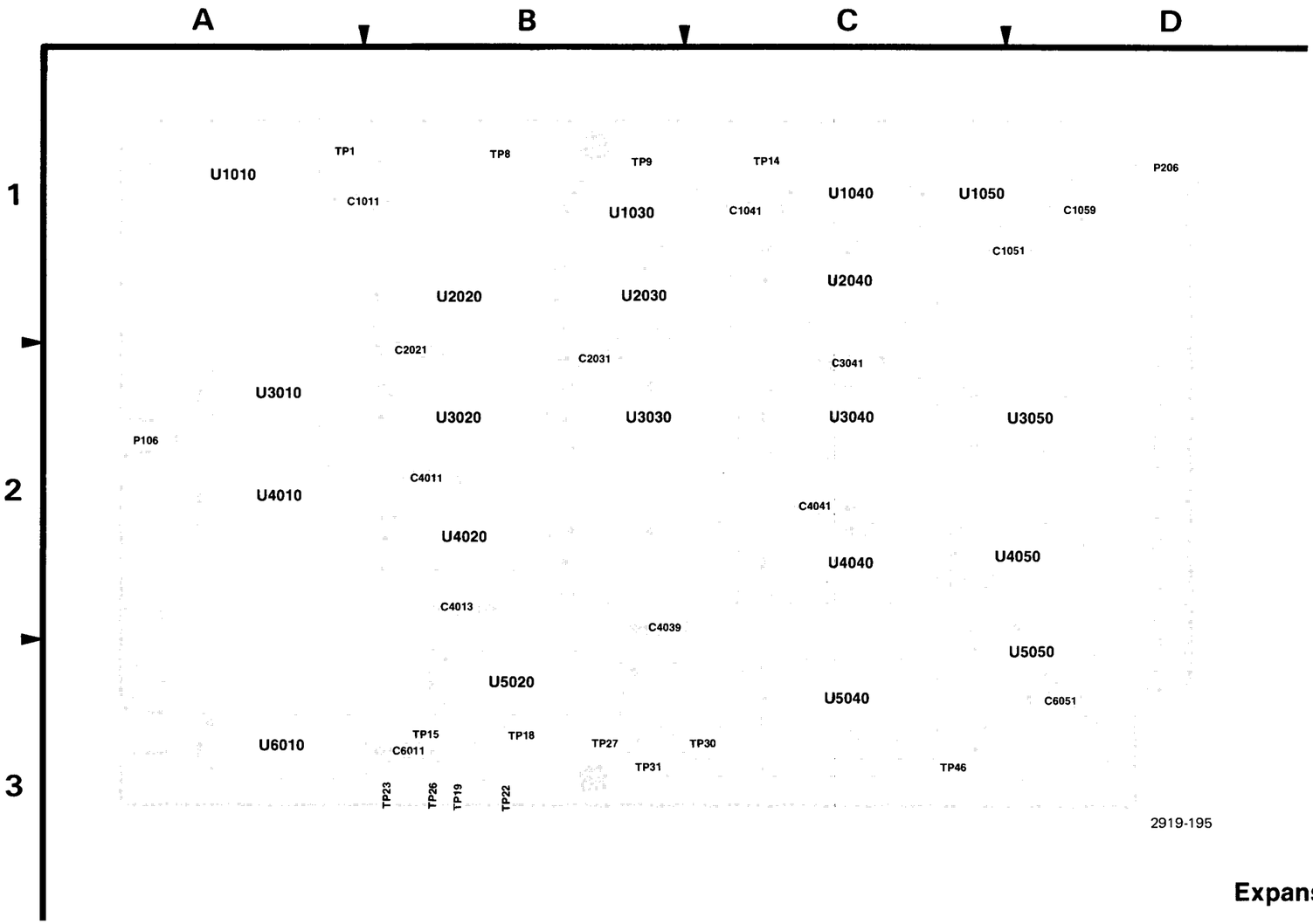
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List



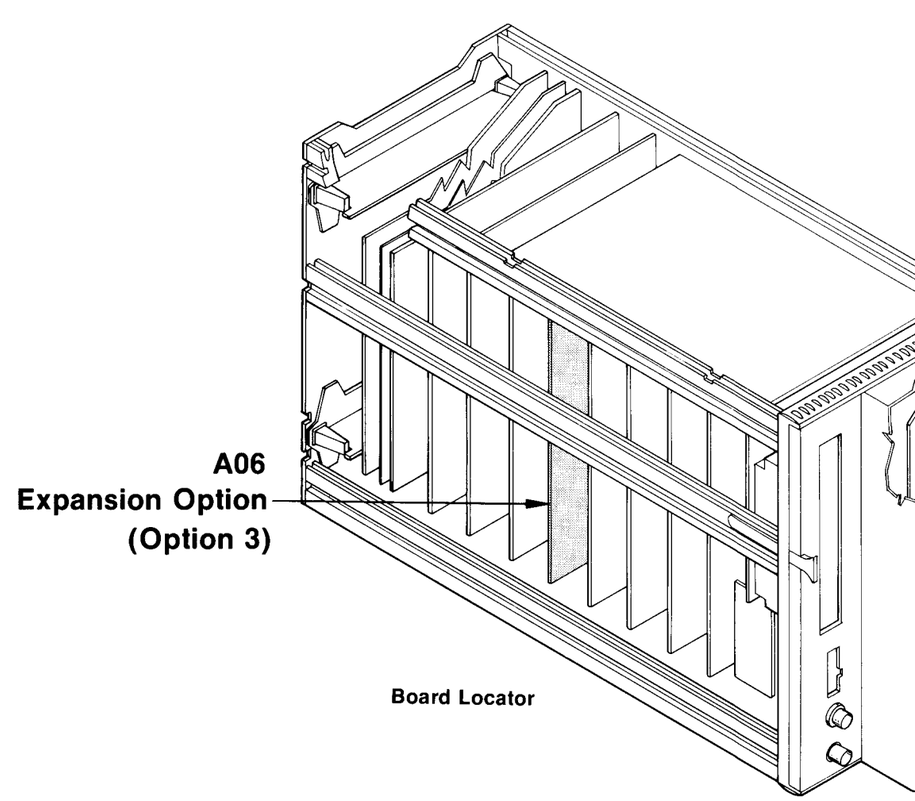
7D02 SERVICE

@ 2919-160

P/O A05 WORD RECOGNIZER 5B

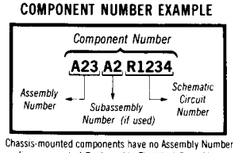


2919-195



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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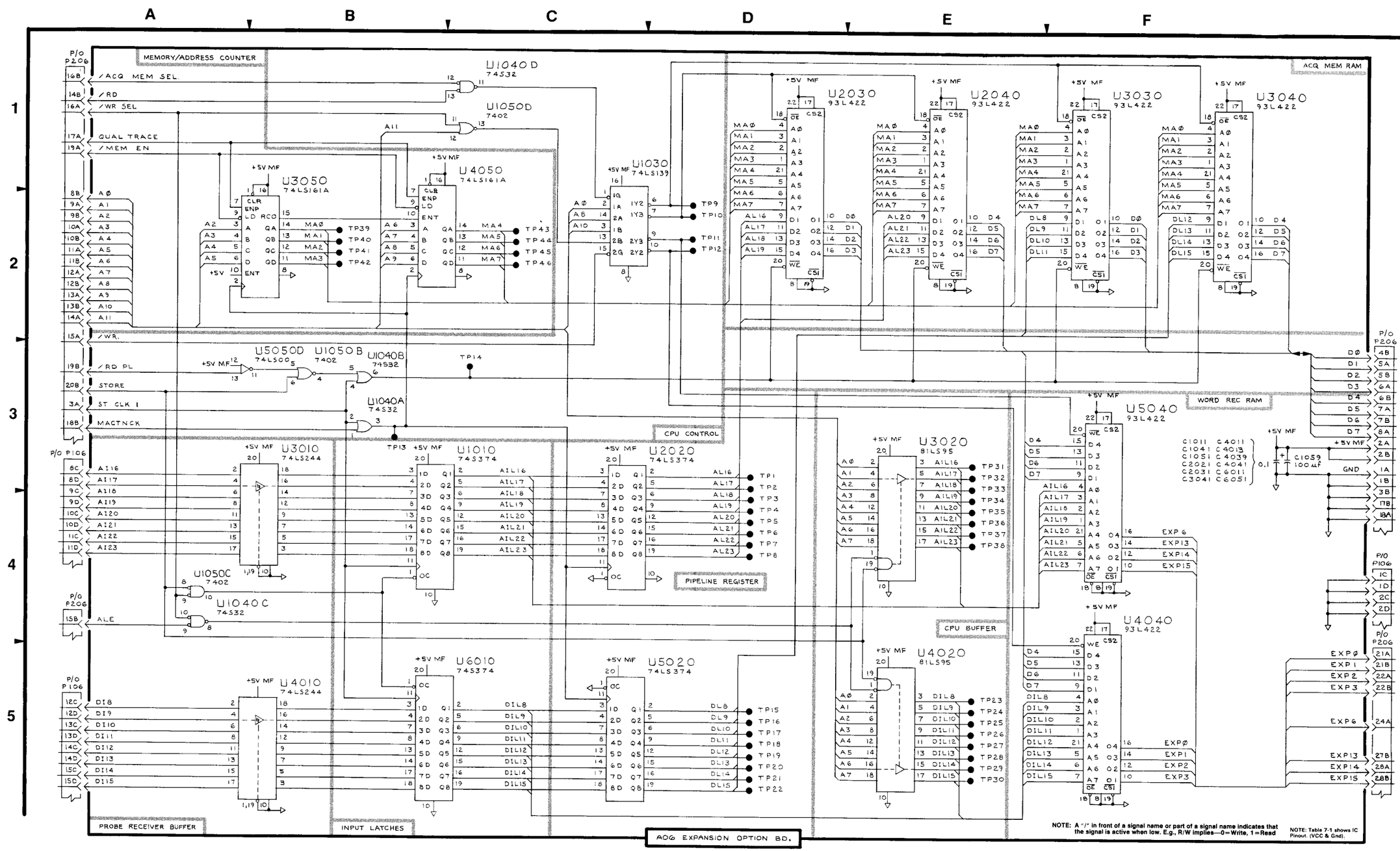
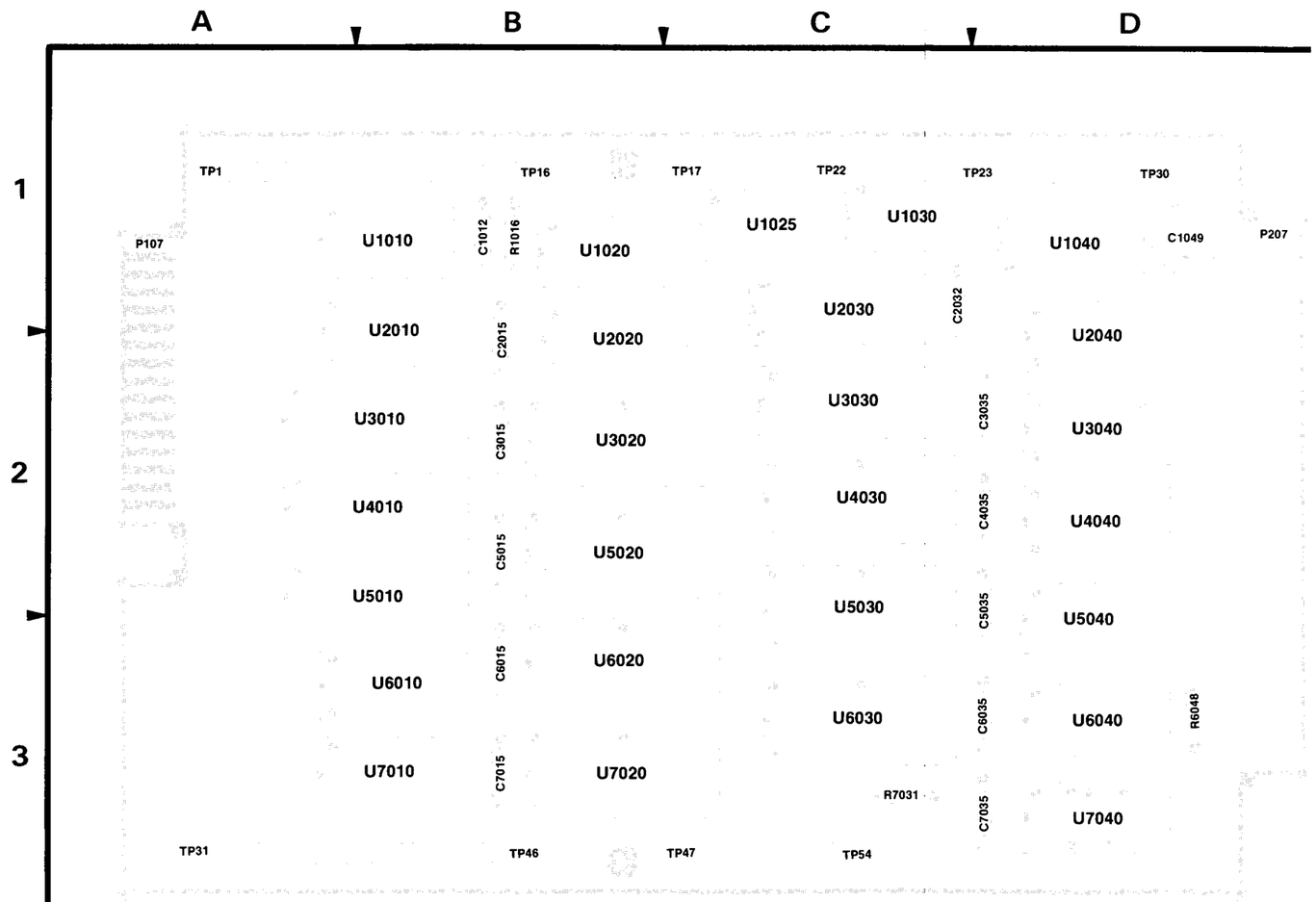
Figure 7-6. A06 Option 3 Expansion option board component locations.



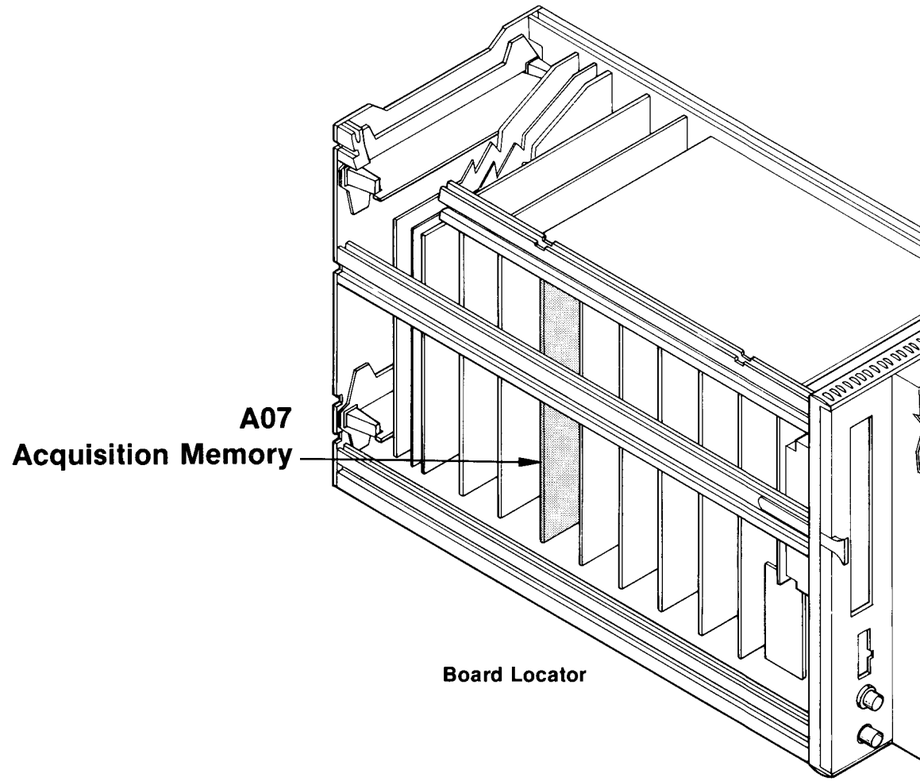
7D02 SERVICE

@ 2919-161

A06 EXPANSION OPTION 6

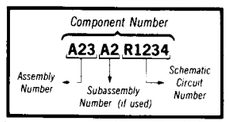


2919-196



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-7A. A07 Acquisition memory board component locations.

P/O A7 ACQUISITION MEMORY DIAGRAM 7B

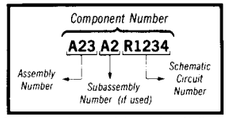
ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1012	F5	B1	TP30	C4	D1
C1049	F5	D1	TP31	C3	A3
C2015	F5	B2	TP32	C3	A3
C2032	F5	C1	TP33	C3	A3
C3015	F5	B2	TP34	C3	A3
C3035	F5	D2	TP35	C3	A3
C4035	F5	D2	TP36	C3	A3
C5015	F5	B2	TP37	C4	A3
C5035	F5	D2	TP38	C4	A3
C6015	F5	B3	TP39	D3	B3
C6035	F5	D3	TP40	D3	B3
C7015	F5	B3	TP41	D3	B3
C7035	F5	D3	TP42	D3	B3
			TP43	D3	B3
P107	A2	A1	TP44	D3	B3
P107	F1	A1	TP45	D4	B3
P107	F4	A1	TP46	D4	B3
P207	A5	D1	TP47	E3	C3
P207	F5	D1	TP48	E3	C3
			TP49	E3	C3
R1016	B3	B1	TP50	E3	C3
R7031	E5	C3	TP51	C5	C3
			TP54	C5	C3
TP1	B4	A1			
TP2	B4	A1	U1010A	B4	B1
TP3	F5	A1	U1025B	B4	C1
TP4	F5	A1	U1025D	B5	C1
TP5	F5	A1	U1030B	B5	C1
TP6	F5	A1	U2010	C1	B2
TP7	F5	A1	U2020	B5	B2
TP8	B3	B1	U3010	B3	B2
TP9	C1	B1	U3020	A1	B2
TP10	C1	B1	U3030	D5	C2
TP11	C1	B1	U3040	B4	D2
TP13	C1	B1	U4010	C3	B2
TP14	D1	B1	U4030	B1	C2
TP15	D5	B1	U4040	C4	D2
TP16	D3	B1	U5010	D3	B2
TP17	C3	C1	U5020	C1	B2
TP22	F1	C1	U5030	C1	C2
TP23	B4	D1	U5040A	B4	D2
TP24	C1	D1	U5040B	B4	D2
TP25	D3	D1	U6010	E3	B3
TP26	F1	D1	U6020	D1	B3
TP27	C4	D1	U6030	E1	C3
TP28	C4	D1	U6040A	C2	D3
TP29	C4	D1	U7020	F1	B3

Partial A7 also shown on diagram 7A.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A7 ACQUISITION MEMORY DIAGRAM 7A

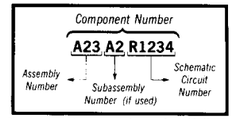
ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P107	F1	A1
P207	A1	D1
P207	F1	D1
R1016	B3	B1
R6048	F5	D3
R7031	E5	C3
TP9	C1	B1
TP10	C1	B1
TP11	B3	B1
TP12	B3	B1
TP13	C1	B1
TP14	D1	B1
TP15	D1	B1
TP16	D3	B1
TP17	C3	C1
TP18	E2	C1
TP19	E4	C1
TP20	E4	C1
TP21	E3	C1
TP22	D4	C1
TP51	C5	C3
TP52	D5	C3
TP53	C5	C3
TP54	C5	C3
U1010A	B4	B1
U1010B	C4	B1
U1010C	C4	B1
U1010D	D3	B1
U1020A	E1	B1
U1020B	D3	B1
U1020C	C4	B1
U1020D	C4	B1
U1025A	C4	C1
U1025B	B4	C1
U1025C	D1	C1
U1025D	B5	C1
U1030A	C3	C1
U1030B	B5	C1
U1030C	C3	C1
U1040	F3	D1
U2010	C1	B2
U2020	B5	B2
U2030	D2	C1
U2040	F4	D1
U5040A	B4	D2
U5040B	B4	D2
U5040C	F1	D2
U5040D	A5	D2
U6040A	C2	D3
U7010C	C3	B3
U7010D	B2	B3
U7010	E1	B3
U7040A	B3	D3
U7040B	E2	D3

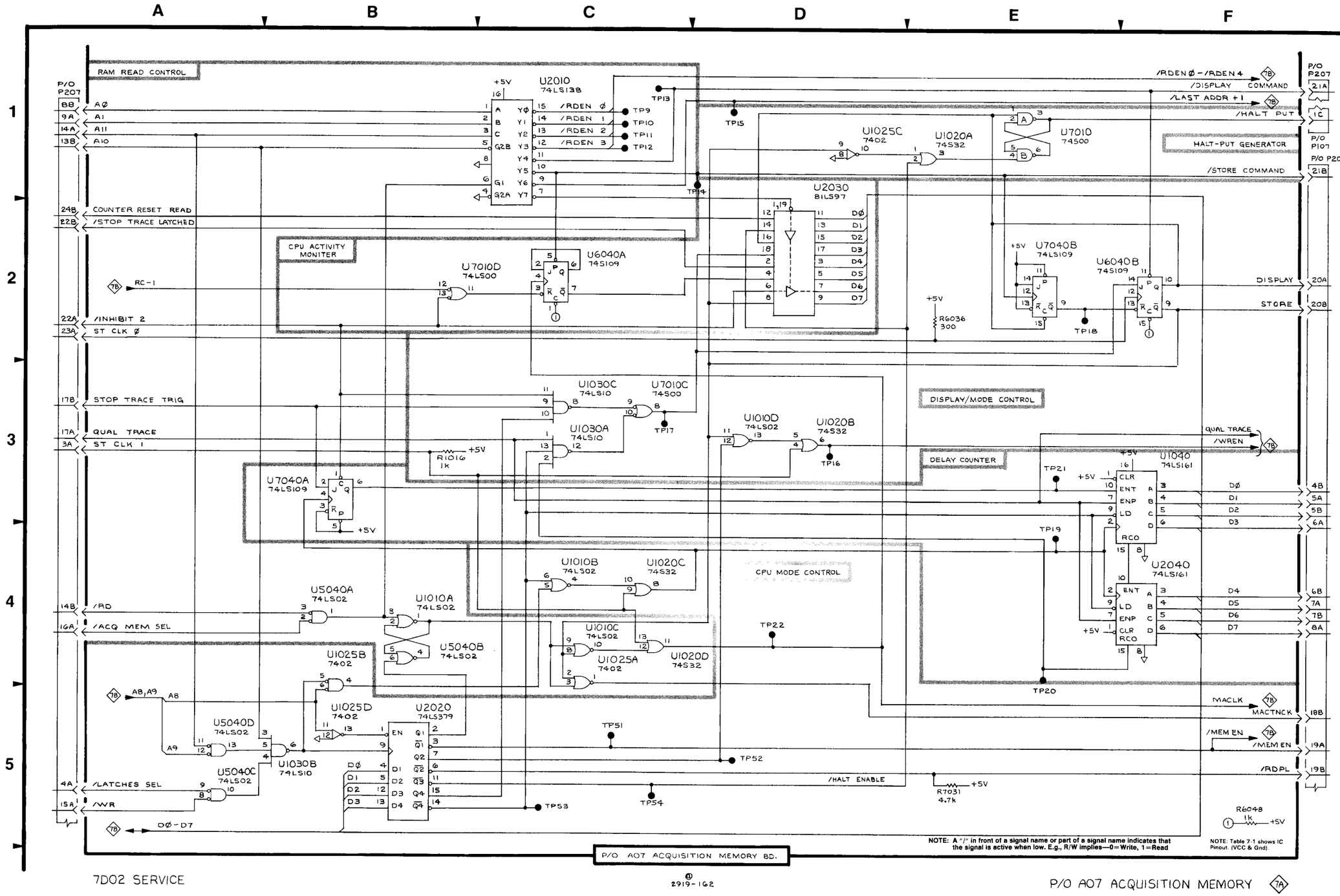
Partial A7 also shown on diagram 7B.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



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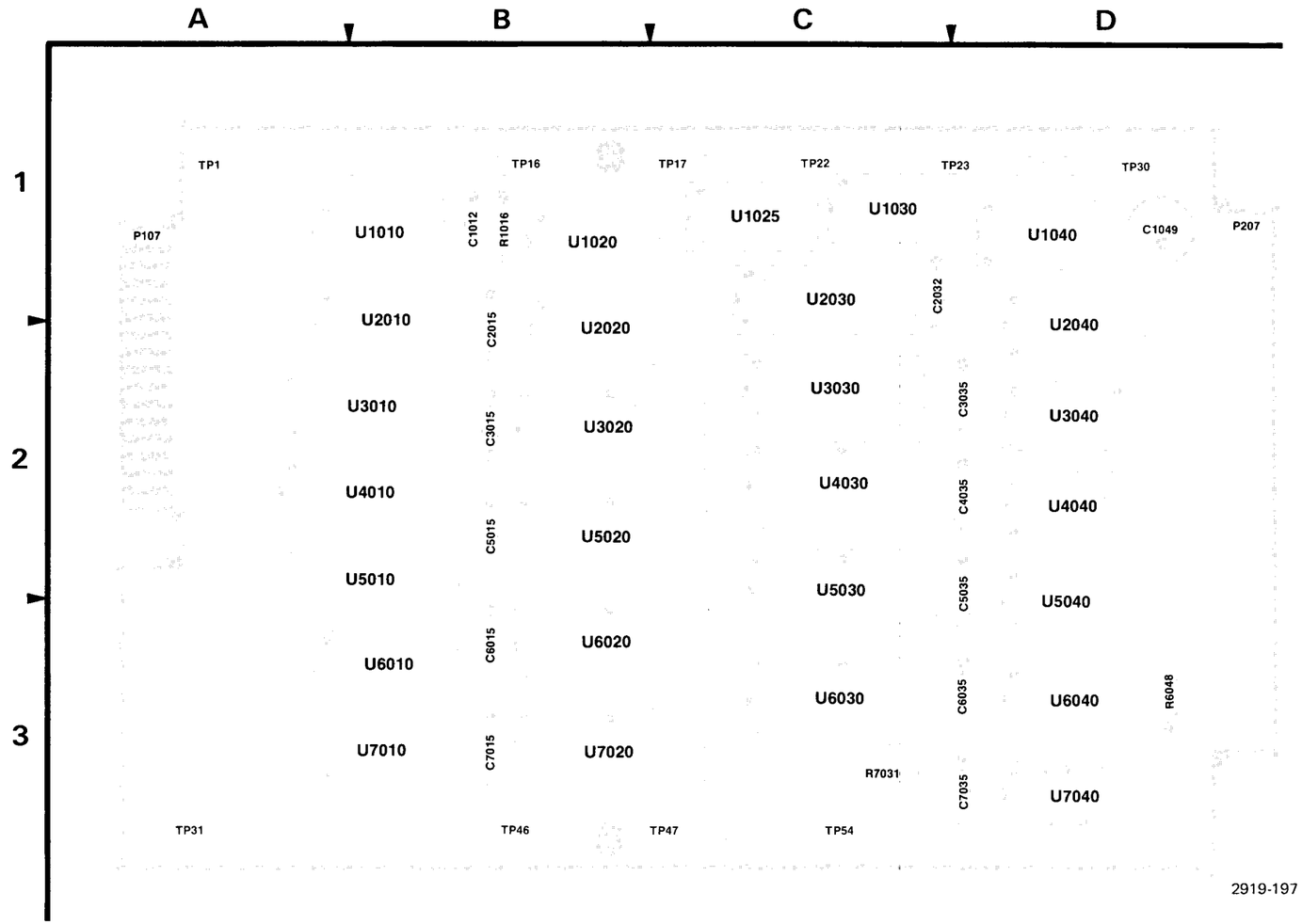
P/O A07 ACQUISITION MEMORY 7A



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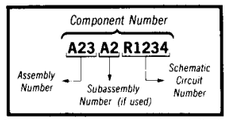
Static Sensitive Devices
See Maintenance Section

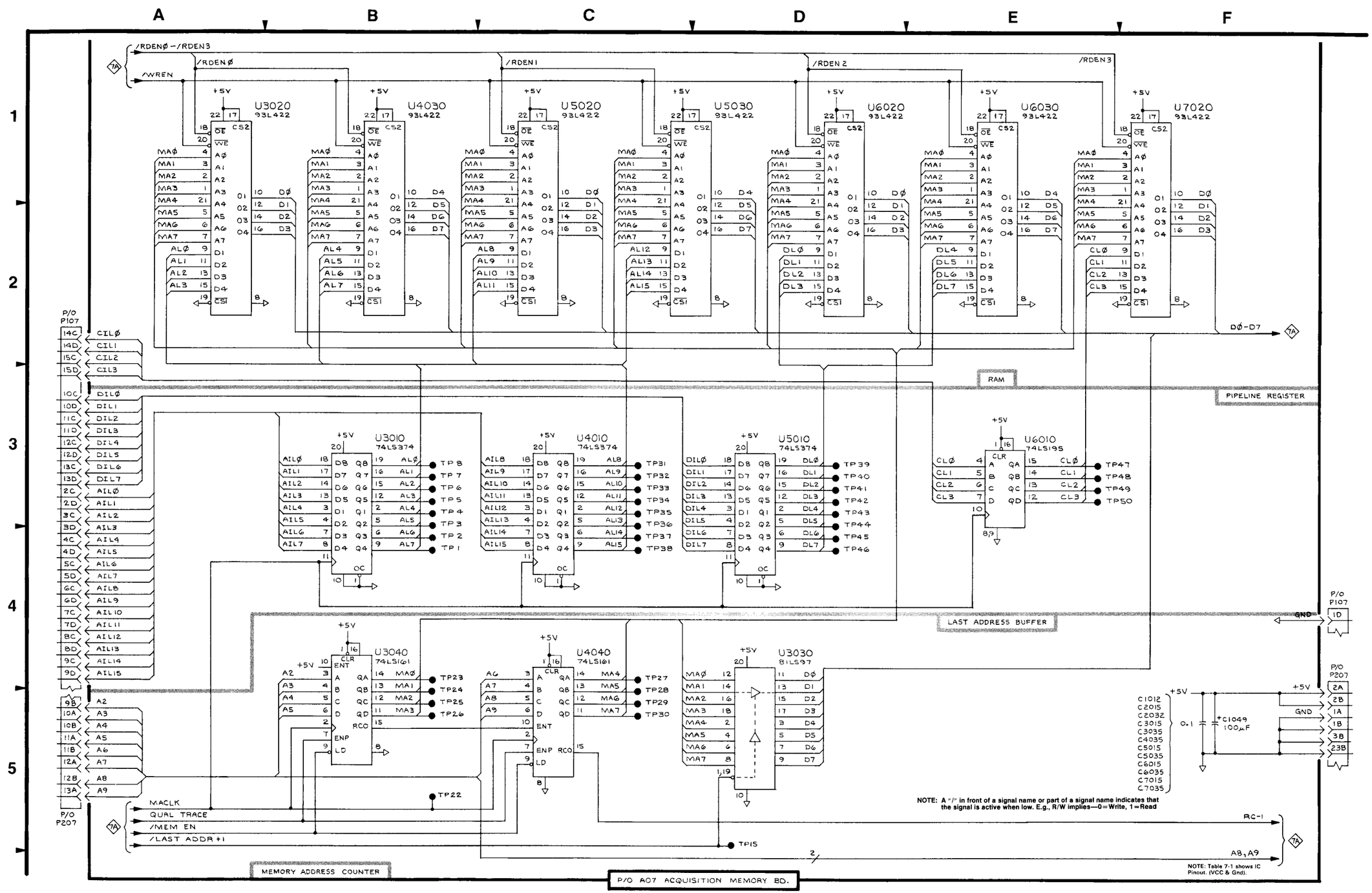
COMPONENT NUMBER EXAMPLE

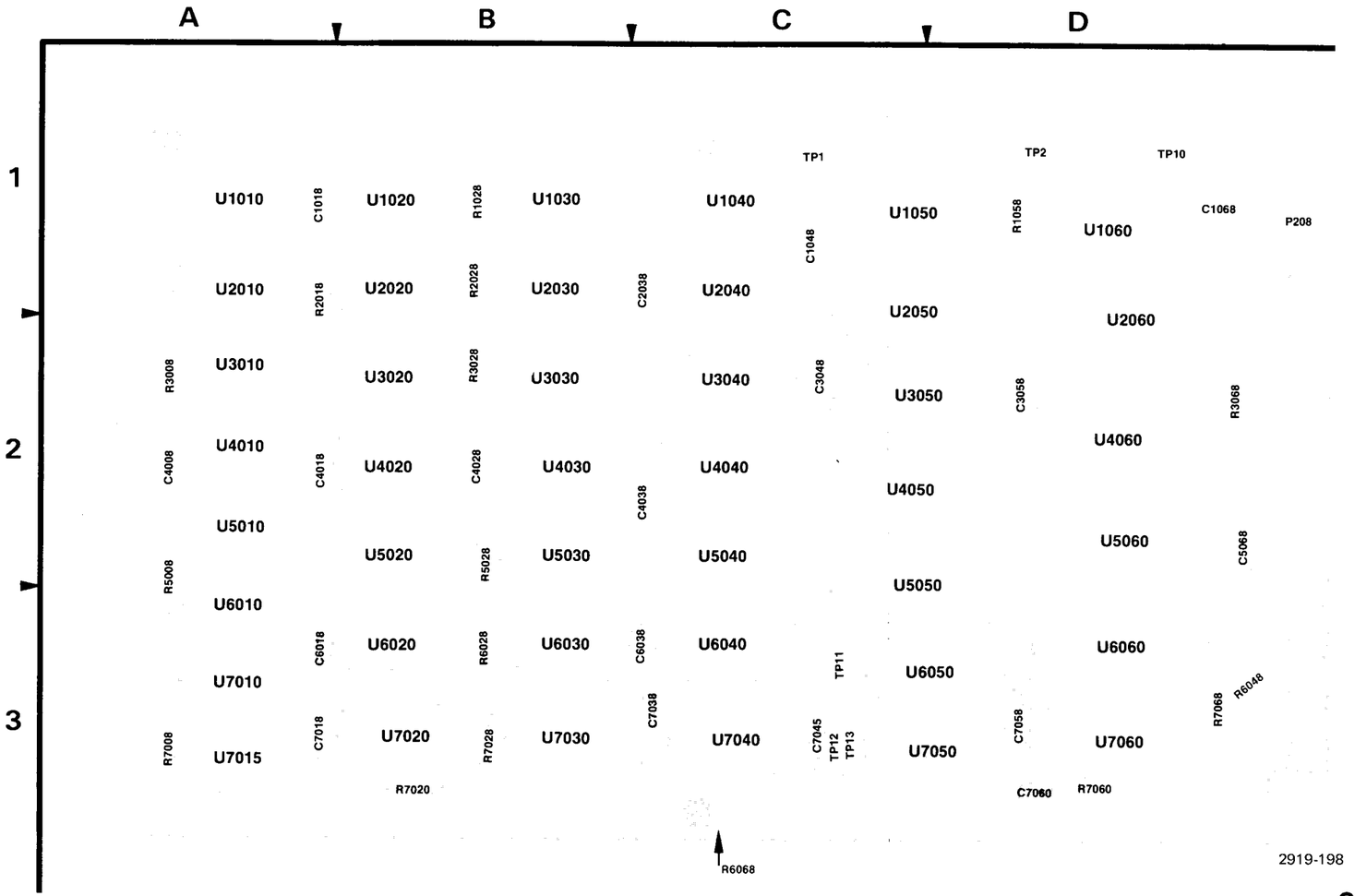


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

@

Figure 7-7B. A07 Acquisition memory board component locations.


A
B
C
D
E
F
1
2
3
4
5
/RDEN0 – /RDEN3
/WREN
/RDEN0
/RDEN1
/RDEN2
/RDEN3
U3020 93L422
U4030 93L422
U5020 93L422
U5030 93L422
U6020 93L422
U6030 93L422
U7020 93L422
D0-D7
RAM
PIPELINE REGISTER
P/O P107
U3010 74LS374
U4010 74LS374
U5010 74LS374
U6010 74LS195
U3040 74LS161
U4040 74LS161
U3030 81LS97
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39
TP40
TP41
TP42
TP43
TP44
TP45
TP46
TP47
TP48
TP49
TP50
MACLK
QUAL TRACE
/MEM EN
/LAST ADDR+1
TP15
RC-1
A8,A9
2
LAST ADDRESS BUFFER
MEMORY ADDRESS COUNTER
P/O A07 ACQUISITION MEMORY BD.
GND
C1012
C2015
C2032
C3015
C3035
C4035
C5015
C5035
C6015
C6035
C7015
C7035
0.1
C1049 100µF
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).



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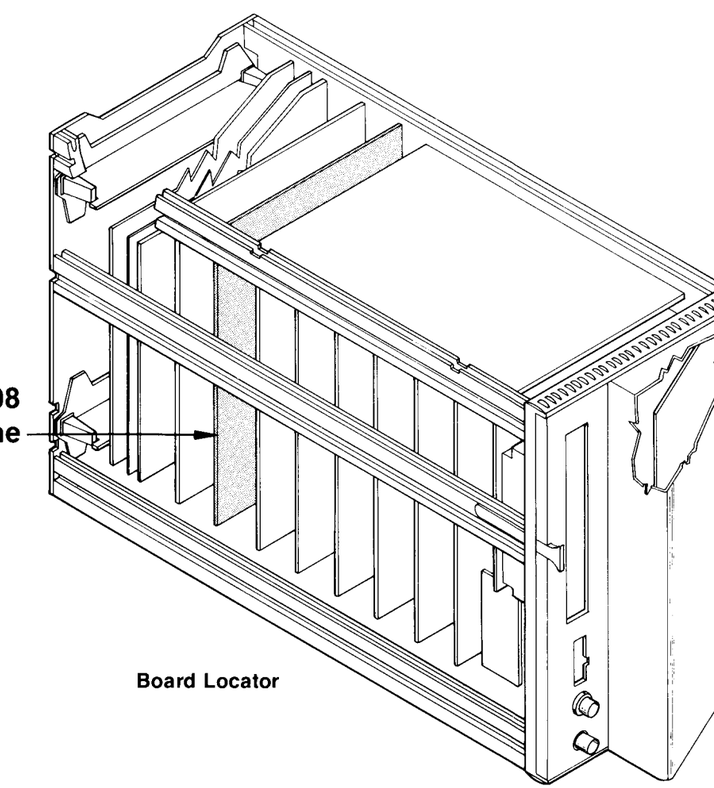
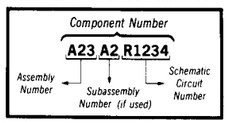


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-8A. A08 State machine board component locations.

P/O A8 STATE MACHINE DIAGRAM 8B

ASSEMBLY A8

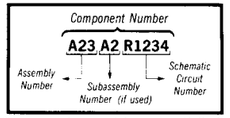
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1018	F3	A1
C1048	F3	C1
C1068	F3	D1
C2038	F3	C1
C3048	F3	C2
C3058	F3	D2
C4008	F3	A2
C4018	F3	A2
C4028	F3	B2
C4038	F3	C2
C5068	F3	D2
C6038	F3	C3
C7018	F3	A3
C7038	C3	C3
C7045	F3	C3
C7058	F3	D3
P208	A1	D1
P208	F1	D1
R2018	A3	A1
R6048 *	F1	D3
R6068 * †	F1	C3
R7020	C3	B3
R7028	D1	B3
TP2	F3	D1
TP11	F3	C3
U1010A	F3	A1
U1010B	C4	A1
U1010D	B2	A1
U2010B	D3	A1
U4010A	B3	A2
U4020A	C4	B2
U4020B	D4	B2
U4030A	C3	B2
U5010B	F3	A2
U5010E	D4	A2
U5020A	A3	B2
U5030A	D2	B2
U5030B	D1	B2
U5030C	A2	B2
U6010A	C3	A3
U6010B	C3	A3
U6020B	B3	B3
U6030A	E2	B3
U6030B	F2	B3
U6040	E2	C3
U7020A	B2	B3
U7020B	B2	B3
U7030A	C2	B3
U7030B	D2	B3
U7040A	B3	C3

Partial A8 also shown on diagram 8A and 8C.

A08 STATE MACHINE 8B

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

***See Parts List for serial number ranges.**

†-Component located on back of board

P/O A8 STATE MACHINE DIAGRAM 8A

ASSEMBLY A8

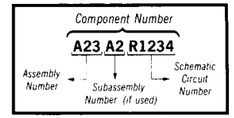
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C6018	E5	A3
C7060	F2	D3
P208	A1	D1
P208	F2	D1
R1058	E2	D1
R3068	D1	D2
R6028	F3	B3
R7008	E5	A3
R7060	F2	D3
R7068	D1	D3
TP13	E5	C3
U1010C	D5	A1
U1060	D1	D1
U2050	A1	C1
U2060	B1	D1
U3050	E3	C2
U4030D	D4	B2
U4060	C3	D2
U5010F	F2	A2
U5030D	A3	B2
U5030E	F1	B2
U5030F	F1	B2
U5040	F3	C2
U5050	E1	C2
U5060	C1	D2
U6020A	A3	B3
U6050	B3	D3
U6060	E1	D3
U7015A	F2	A3
U7040B	C4	C3
U7040C	C4	C3
U7050	C3	D3
U7060	E3	D3

Partial A8 also shown on diagram 8B and 8C.

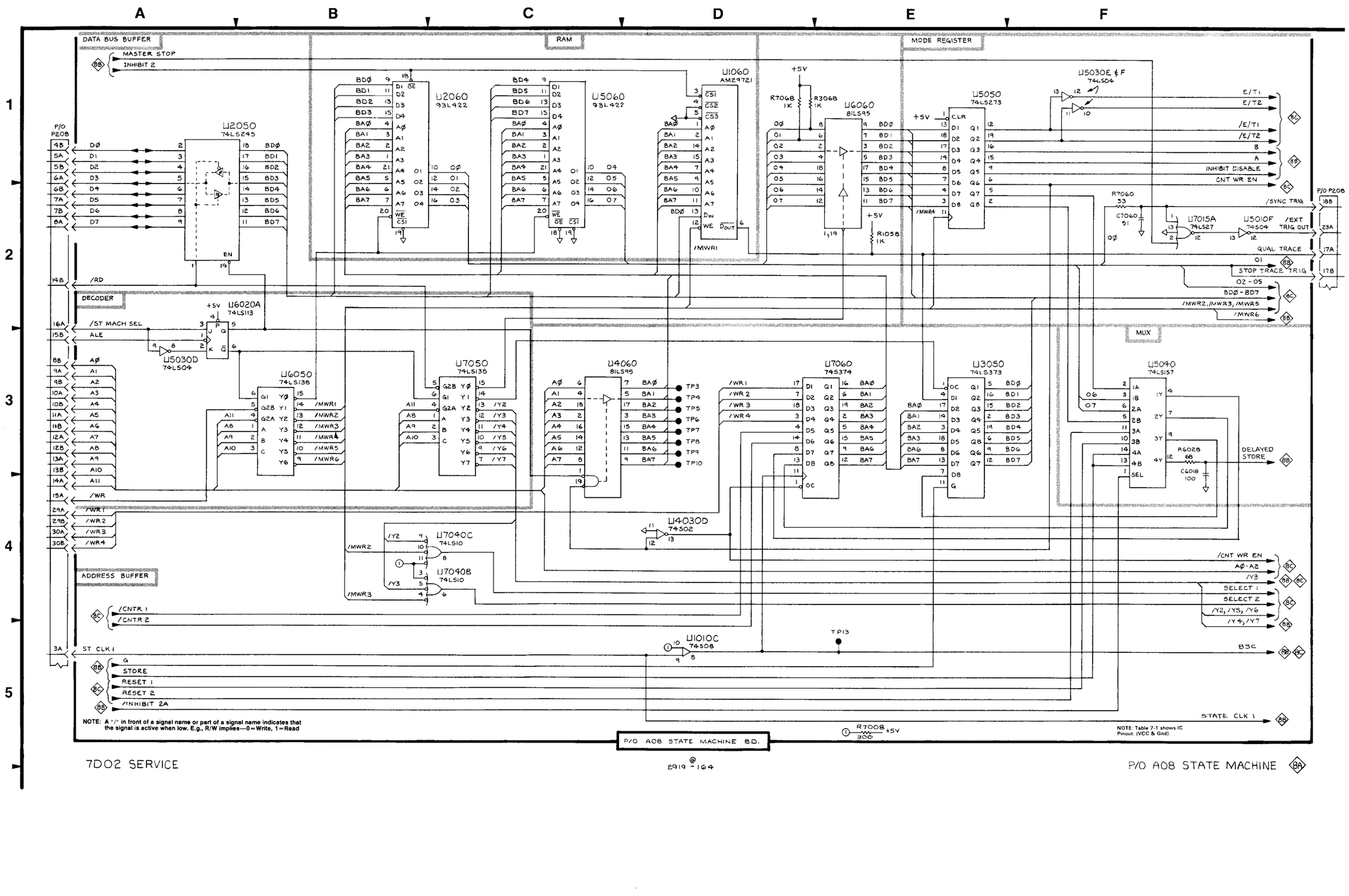
A08 STATE MACHINE 8A

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



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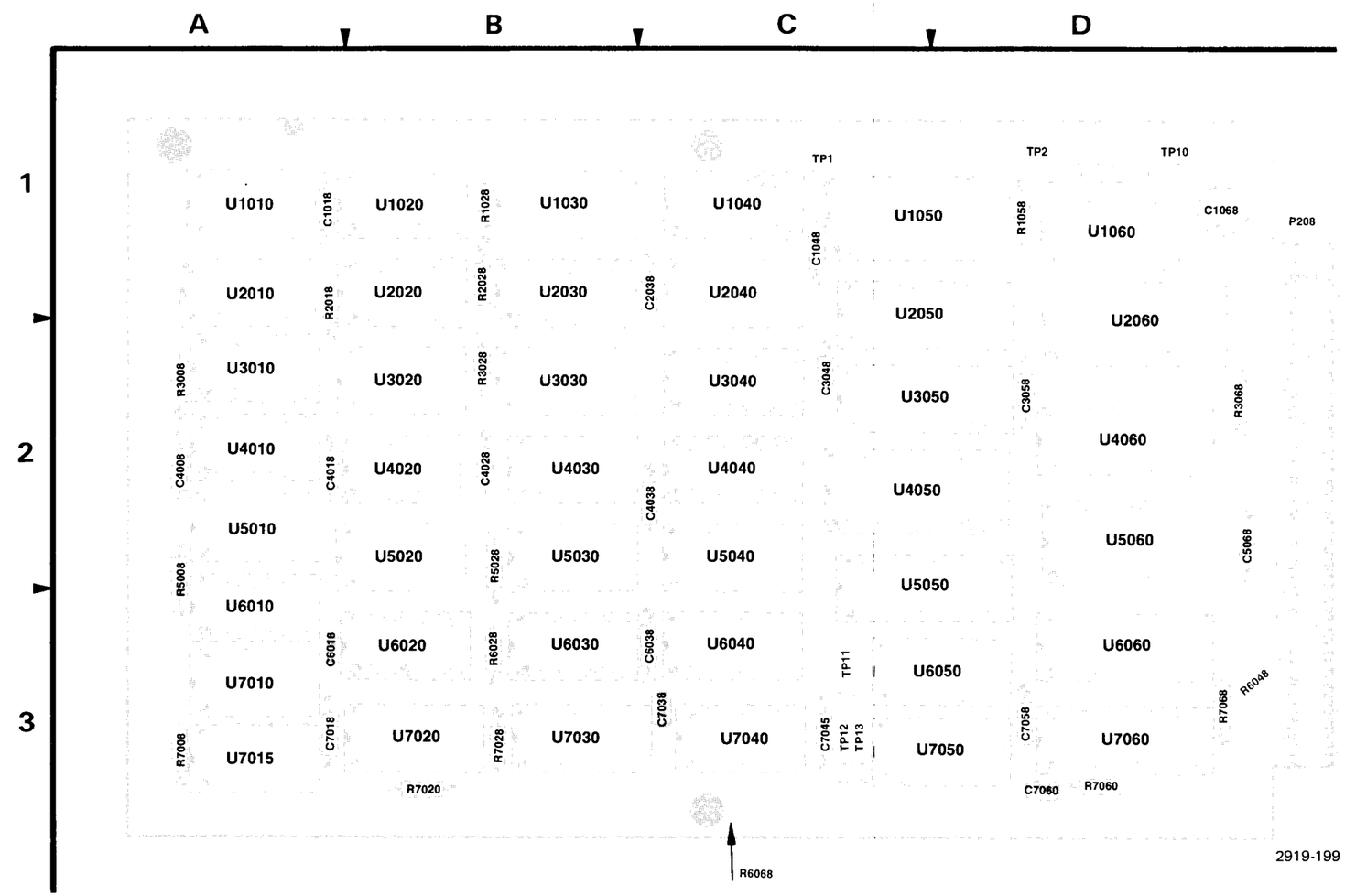
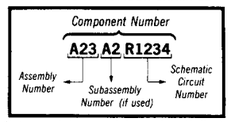
P/O A08 STATE MACHINE 8A



Static Sensitive Devices
See Maintenance Section

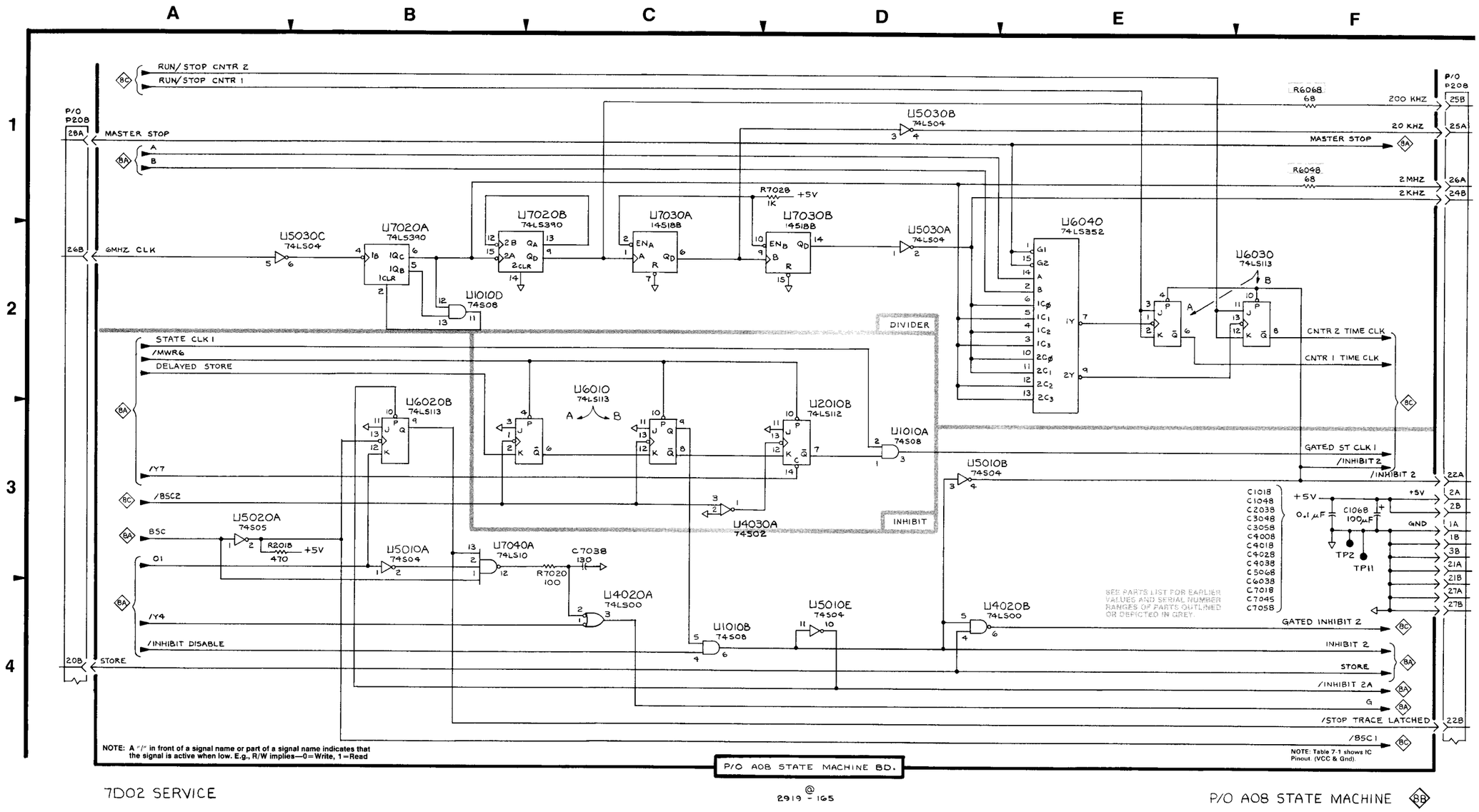
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

Figure 7-8B. A08 State machine board component locations.



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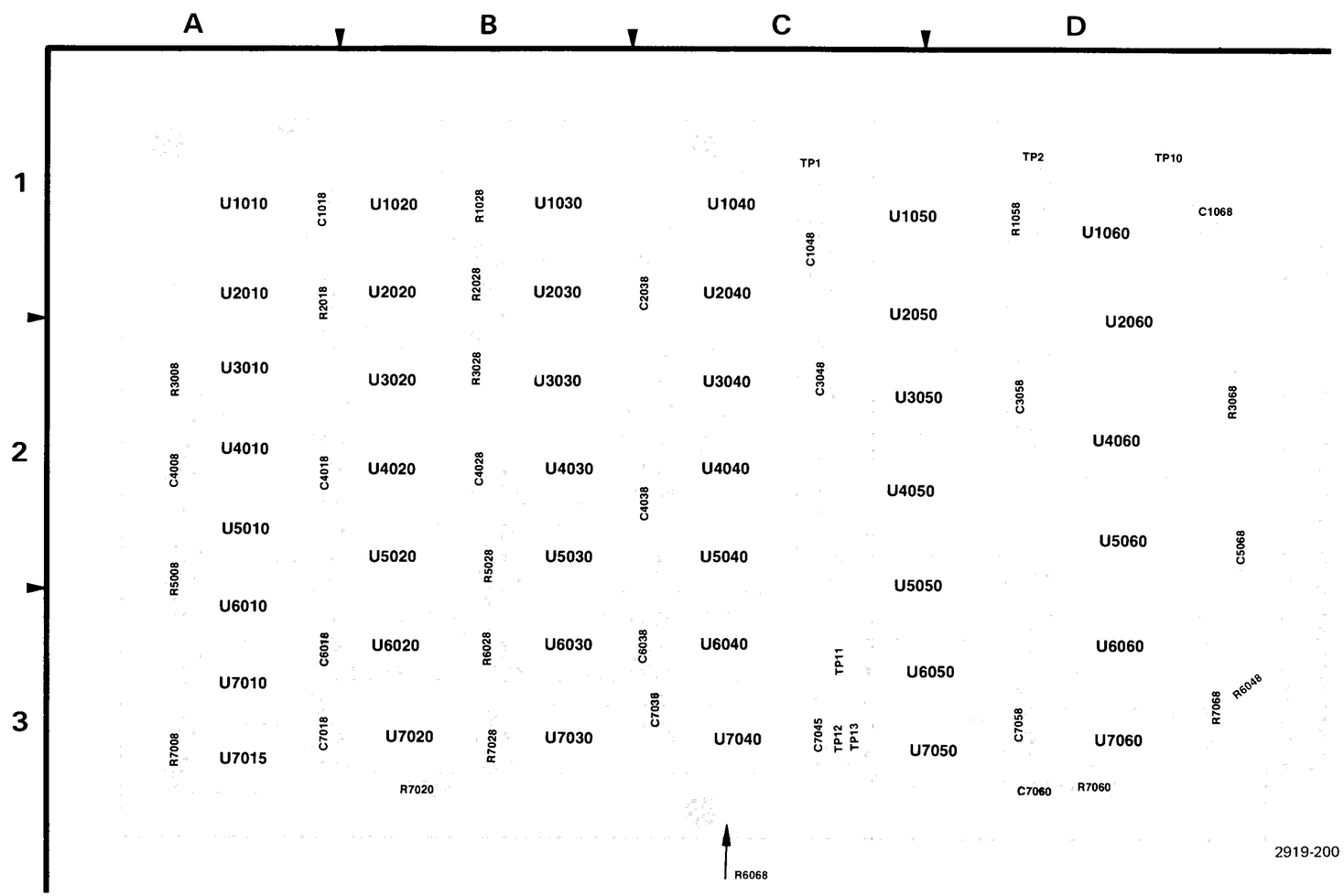
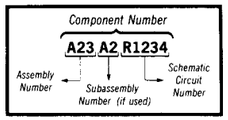
P/O A08 STATE MACHINE 8B



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

@

Figure 7-8C. A08 State machine board component locations.

P/O A9 CENTRAL PROCESSOR UNIT DIAGRAM 9A

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1001	B2	A1	R1023	B1	B1
C1014	A2	A1	R1024	B2	B1
C1016	A2	A1	R1025	B1	B1
C1018	A2	A1	R1034	B5	B1
C1030	B5	B1	R1035	B5	B1
C1044	A3	B1	R1037	B5	B1
C1054	A3	C1	R3070	D5	D2
C1064	A3	C1	R3073	F5	D2
C1068	A3	C1	R3076 * †	E2	P2
C1081	A3	D1	R4054	B4	C3
C2039	A3	B2	R4059	F5	C3
C4008	A3	A2	R4073	F3	D2
C4040	A3	B3	R4082	B1	D3
C4051	A3	C3			
C4055	A3	C3	S1001	B3	A1
C4068	A3	C3			
C4082	A3	D3	TP41	B3	A2
			TP42	B3	A2
CR1001	B2	A1	TP43	A3	A2
CR1002	A3	A1			
CR1021	B1	B1	U1030	B5	B1
			U2080	D3	D2
J1001	A1	A1	U3050	B2	C2
J1001	F1	A1	U3065	C3	C2
			U3080	D3	D2
P209	F2	D1	U4040	D2	B3
P209	F5	D1	U4045A	B3	B3
P1006	B3	A1	U4045A	B4	B3
P1031	C5	B1	U4045B	F3	B3
			U4050A	A4	C3
Q1001	B2	A1	U4050B	E2	C3
Q1025	A2	B1	U4050C	B4	C3
Q1030	B1	B1	U4055A	C4	C3
Q1037	C5	B1	U4055B	F2	C3
Q3073	F3	C2	U4055C	B4	C3
			U4055D	E2	C3
R1001	B2	A1	U4065A	F3	C3
R1002	B2	A1	U4065B	F4	C3
R1005	A2	A1	U4070B	B2	C3
R1009	B3	A1	U4070	C2	C3
R1011	D2	A1	U4075	E3	D3
R1012	A2	A1	U4080	F2	D3
R1014	A2	A1			
R1016	B2	A1	VR1007	A2	A1
R1020	B5	B1			
			Y1030	A2	B1

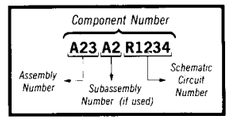
Partial A9 also shown on diagram 9B.

***See Parts List for serial number ranges.**

†-Component located on back of board

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A8 STATE MACHINE DIAGRAM 8C

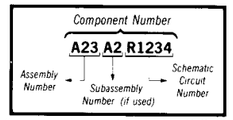
ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
R1028	C4	B1
R2028	A4	B1
R3008	B4	A2
R3028	A1	B2
R5008	B2	A2
R5028	A4	B2
TP1	D2	C1
TP12	D4	C3
U1020A	B1	B1
U1020B	B1	B1
U1030A	C1	B1
U1030A	C4	B1
U1040	D1	C1
U1050	E1	C1
U2020A	B4	B1
U2020B	B4	B1
U2030A	E2	B1
U2030B	F2	B1
U2040	D1	C1
U3010	F1	A2
U3020A	A4	B2
U3020B	A1	B2
U3020C	B2	B2
U3020D	B4	B2
U3030A	F5	B2
U3030B	E5	B2
U3040	D4	C2
U4010	F4	A2
U4020C	C2	B2
U4020D	C4	B2
U4030B	E4	B2
U4030C	E2	B2
U4040	D4	C2
U4050	E4	C2
U5010C	A2	A2
U5010D	B2	A2
U5020B	E2	B2
U5020C	E5	B2
U5020D	A4	B2
U5020E	B2	B2
U5020F	B4	B2
U7010A	F3	A3
U7010B	E4	A3
U7010C	F1	A3
U7010D	F5	A3
U7015B	F4	A3
U7015C	F2	A3

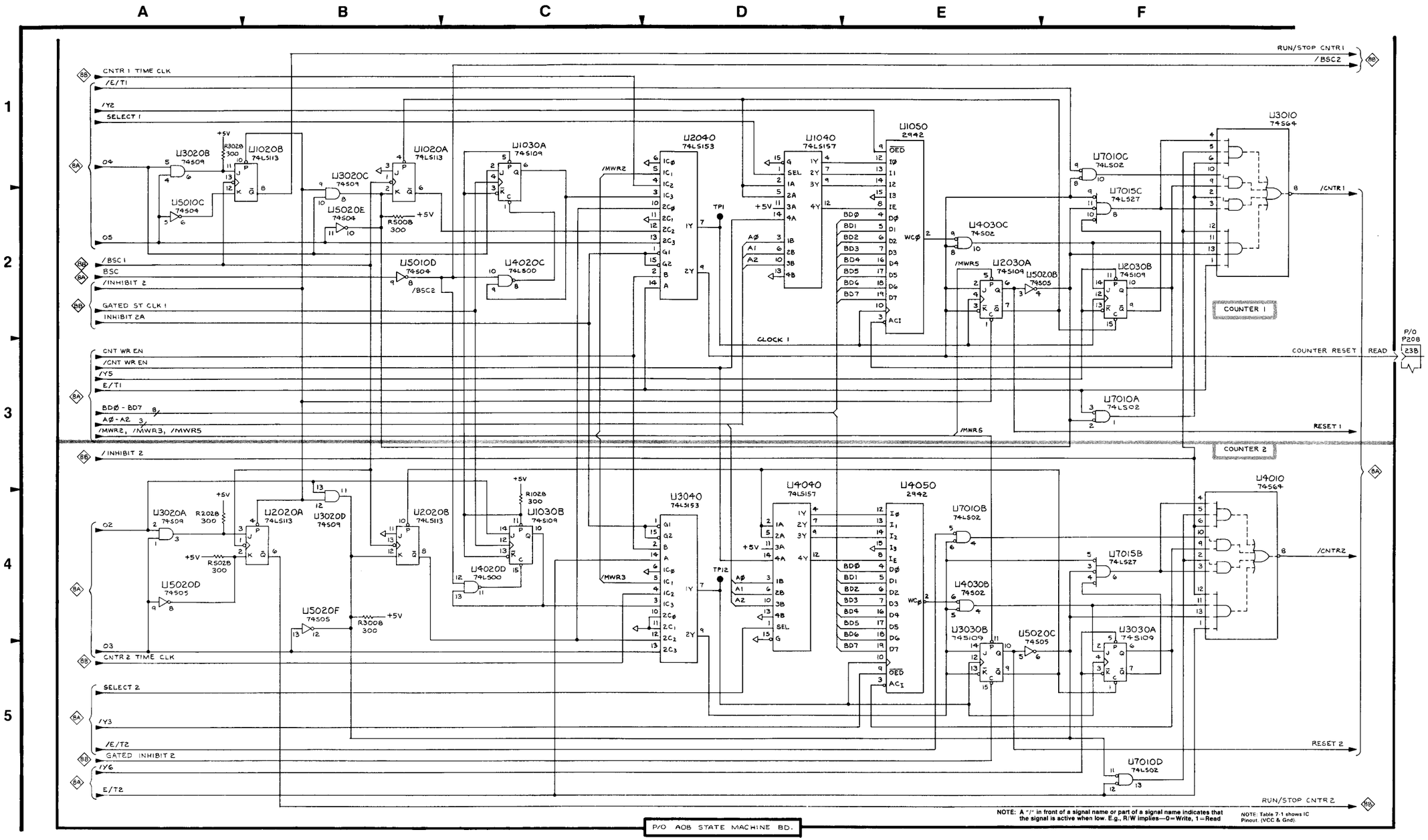
Partial A8 also shown on diagrams 8A and 8B.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



P/O A08 STATE MACHINE BD.

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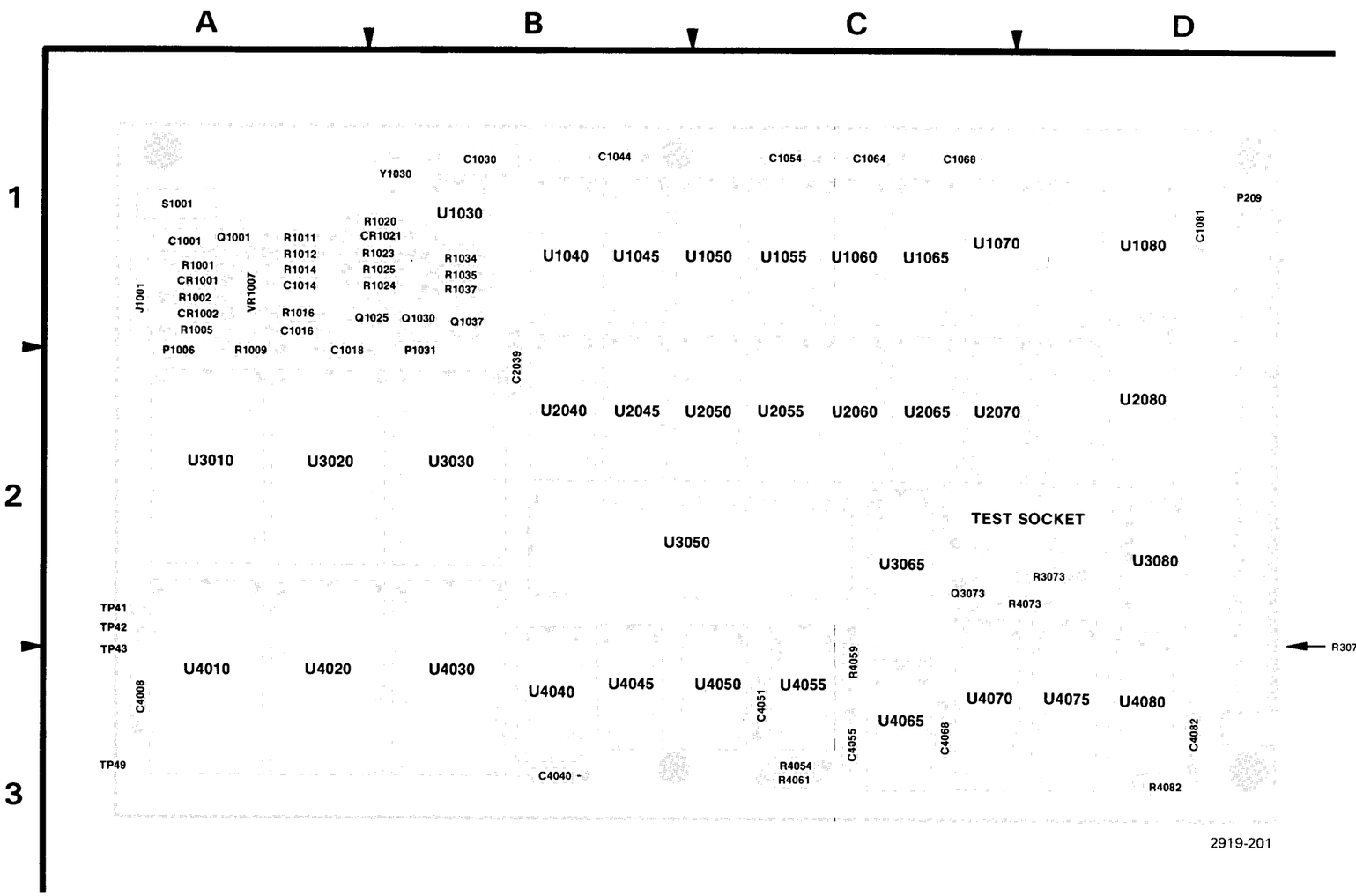
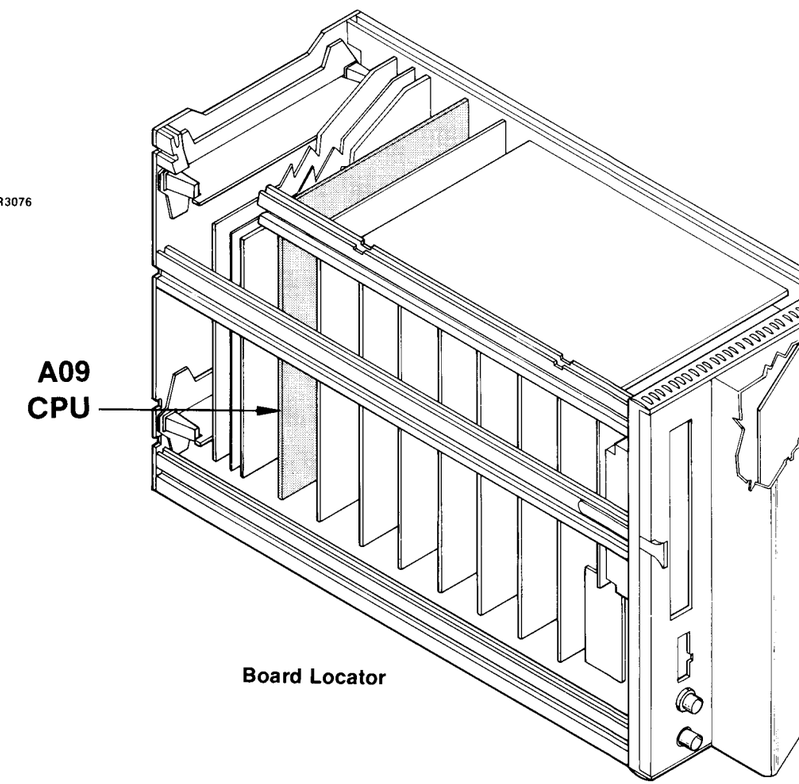
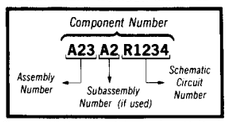




Board Locator

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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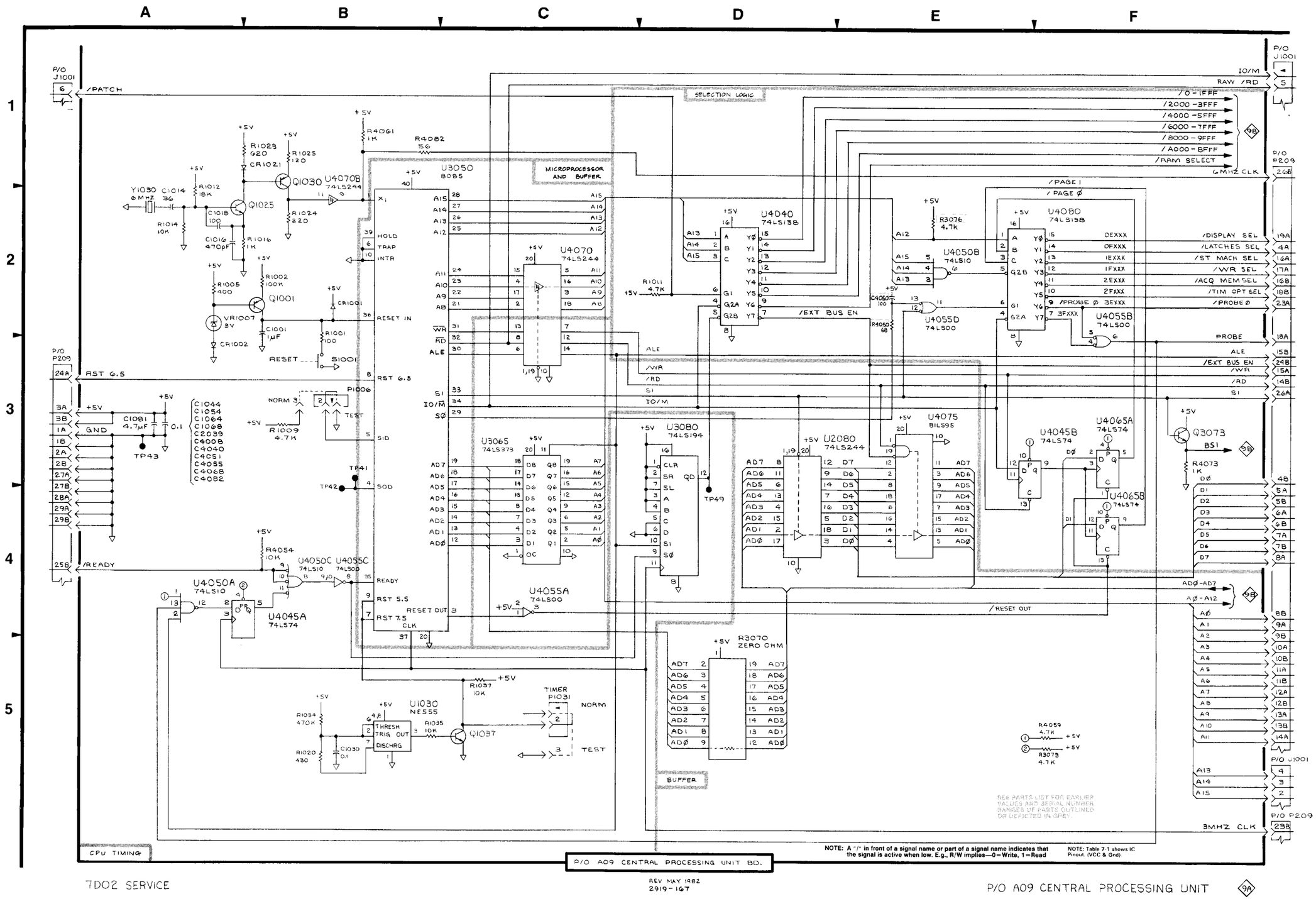
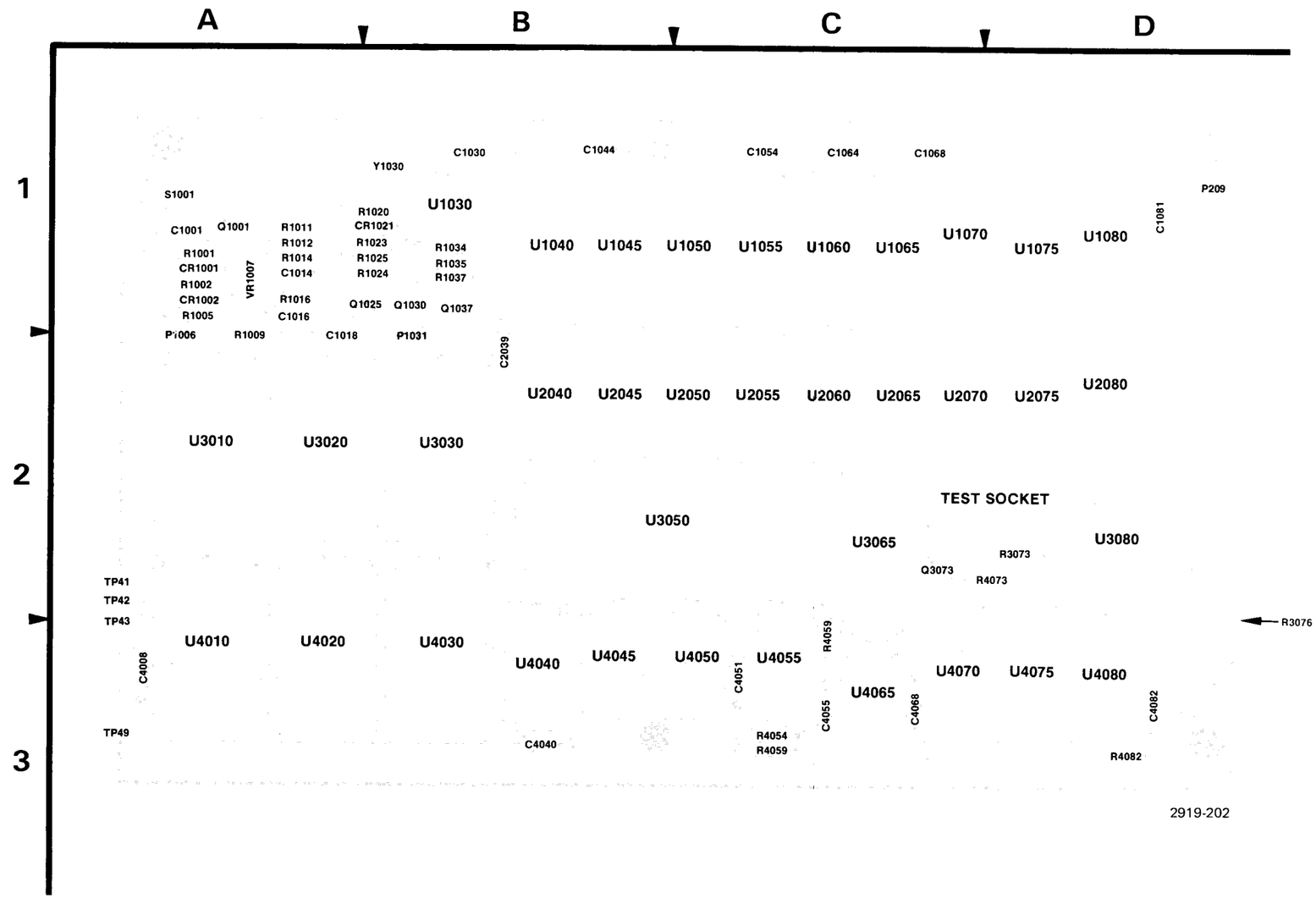
Figure 7-9A. A09 CPU board component locations.


A
B
C
D
E
F
1
2
3
4
5
P/O J1001
6
/PATCH
+5V
R1023 620
R1025 120
CR1021
Q1030
U4070B 74LS244
Y1030 6MHZ
C1014 36
R1012 18K
Q1025
C1018 100
R1014 10K
C1016 470pF
R1016 1K
R1024 220
R4061 1K
R4062 56
U3050 8085
X1
HOLD
TRAP
INTR
R1005 400
Q1001
VR1007 3V
CR1002
C1001 1μF
R1002 100K
CR1001
R1001 100
RESET
S1001
RESET IN
P/O P209
24A
RST 6.5
8
RST 6.5
P1006
NORM
TEST
R1009 4.7K
5
SID
TP41
TP42
4
SOD
3A
3B
1A
1B
2A
2B
27A
27B
28A
29A
29B
C1081 4.7μF
0.1
GND
TP43
C1044
C1054
C1064
C1068
C2039
C4008
C4040
C4051
C4055
C4068
C4082
25B
/READY
R4054 10K
U4050C 74LS10
U4055C 74LS00
READY
RST 5.5
RST 7.5
CLK
37
20
RESET OUT
3
U4050A 74LS10
U4045A 74LS74
U4055A 74LS00
U3065 74LS373
U4070 74LS244
MICROPROCESSOR AND BUFFER
A15
A14
A13
A12
A11
A10
A9
A8
WR
RD
ALE
S1
IO/M
SØ
AD7
AD6
AD5
AD4
AD3
AD2
AD1
ADØ
OC
U3080 74LS194
CLR
SR
SL
QD
TP49
R1011 4.7K
SELECTION LOGIC
U4040 74LS138
G1
G2A
G2B
/EXT BUS EN
R4060 68
C4060 100
U4050B 74LS10
U4055D 74LS00
R3076 4.7K
U4080 74LS138
/PAGE 1
/PAGE Ø
OEXXX
OFXXX
1EXXX
1FXXX
2EXXX
2FXXX
3EXXX
3FXXX
/PROBE Ø
U4055B 74LS00
U4075 BIL595
U2080 74LS244
U4045B 74LS74
U4065A 74LS74
U4065B 74LS74
Q3073
BS1
R4073 1K
R3070 ZERO OHM
BUFFER
U1030 NE555
THRESH
TRIG
OUT
DISCHRG
R1034 470K
R1035 10K
R1020 430
C1030 0.1
Q1037
R1037 10K
TIMER P1031
NORM
TEST
R4059 4.7K
R3079 4.7K
+5V
IO/M
RAW /RD
/0-1FFF
/2000-3FFF
/4000-5FFF
/6000-7FFF
/8000-9FFF
/A000-BFFF
/RAM SELECT
6MHZ CLK
98
P/O P209
2GB
/DISPLAY SEL
/LATCHES SEL
/ST MACH SEL
/WR SEL
/ACQ MEM SEL
/TIM OPT SEL
/PROBE Ø
PROBE
ALE
/EXT BUS EN
/WR
/RD
S1
19A
4A
16A
17A
16B
18B
23A
18A
15B
24B
15A
14B
26A
4B
5A
5B
6A
6B
7A
7B
8A
ADØ-AD7
AØ-A12
98
/RESET OUT
8B
9A
9B
10A
10B
11A
11B
12A
12B
13A
13B
14A
P/O J1001
4
3
2
P/O P209
23B
3MHZ CLK
CPU TIMING
P/O A09 CENTRAL PROCESSING UNIT BD.
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd)
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.



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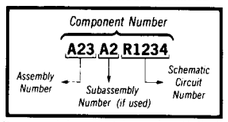
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-9B. A09 CPU board component locations.

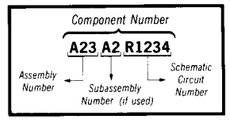
P/O A10 DISPLAY DIAGRAM 10A

ASSEMBLY A10		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1016	B3	A1
C1020	B2	A3
C1030	C1	A3
C1040	C1	C1
C1050	C1	D1
C1065	A1	D1
C2030	C1	B2
C2050	C1	D1
C3010	C1	A2
C3020	C1	A2
C3040	C1	C2
C3050	C1	D2
C4010	C1	A2
C4020	C1	A2
C4030	C1	B2
C4040	C1	C2
C4050	C1	D2
C5013	D4	A3
C5052	C2	D3
C6021	C1	A3
C6052	B2	D3
C6053	B2	D3
C6054	B1	D3
C6055	B1	D3
C6056	A2	D3
L5051	B1	D2
L5052	B1	D3
L6056	B2	D3
P210	A1	D1
Q1010	B2	A1
R1010	B2	A1
R1012	B2	A1
R1017	B3	A1
U1010A	E2	A1
U1010B	D5	A1
U1020	E5	A3
U2010	D2	A2
U2020C	C2	B1
U2020E	C3	B1
U2020F	B2	B1
U2030A	B3	B1
U2030B	C2	B1
U3010A	E3	A2
U3010B	E4	A2
U3030A	C3	B2
U3030B	C3	B2
U4020D	F5	B2
U4030A	D4	B2
U4030B	B4	B2
U4030D	C4	B2
U4042	D4	C2
Y1015	A2	A1

Partial A10 also shown on diagram 10B and 10C.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A10 DISPLAY 10A

P/O A9 CENTRAL PROCESSOR UNIT DIAGRAM 9B

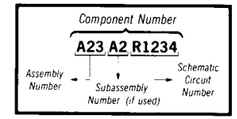
ASSEMBLY A9		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
U1040	E1	B1
U1045	C1	B1
U1050	E2	C1
U1055	C2	C1
U1060	E4	C1
U1065	C4	C1
U1070	C5	C1
U1080	B2	D1
U2040	F1	B2
U2045	D1	B2
U2050	F2	C2
U2055	D2	C2
U2060	F4	C2
U2065	D4	C2
U2070	D5	C2
U3010	A1	A2
U3020	A2	A2
U3030	B4	B2
U4010	A4	A2
U4020	B5	A3
U4030	A5	B3

Partial A9 also shown on diagram 9A.

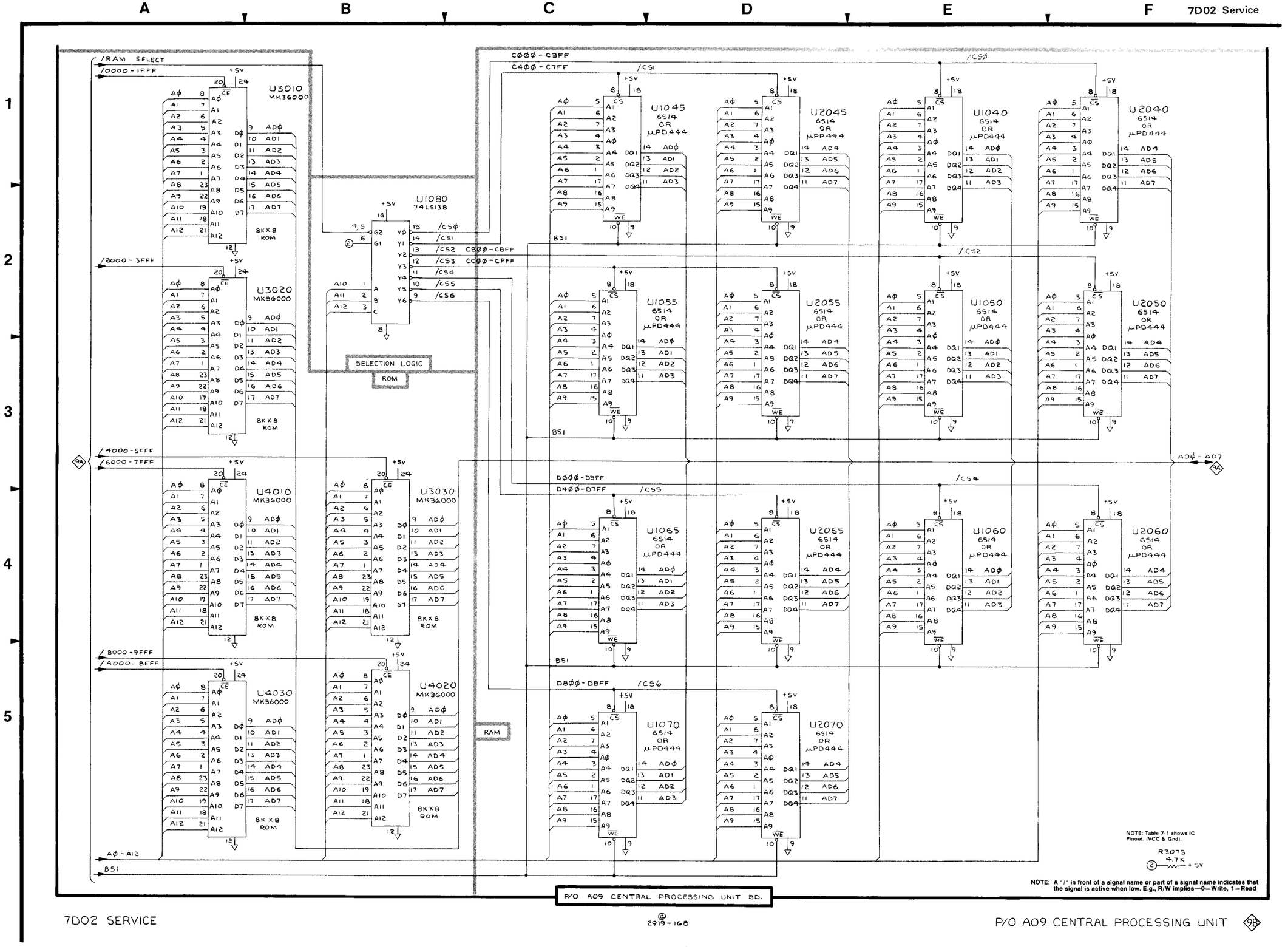
A09 CPU 9B

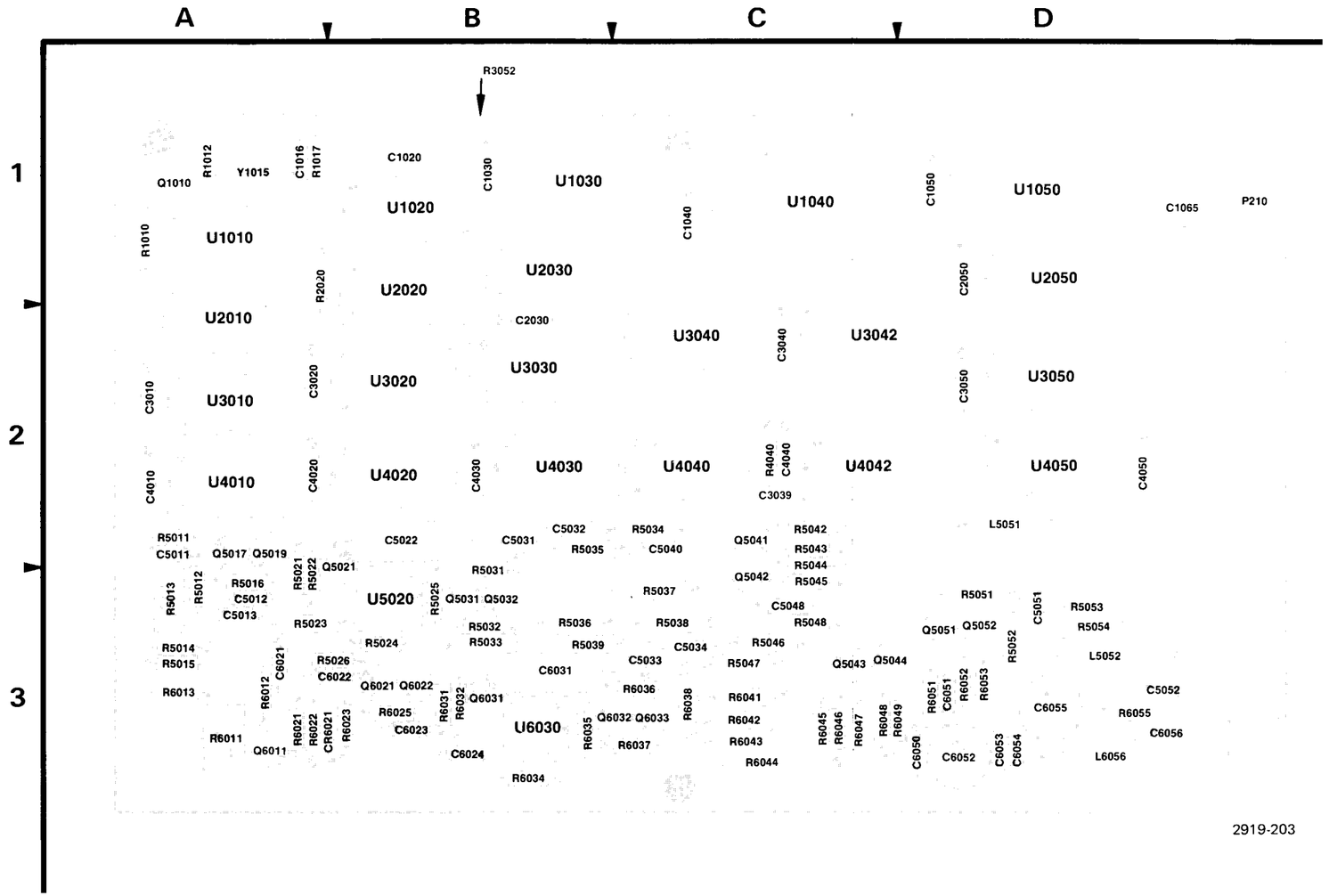
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
5
/RAM SELECT
/0000 - 1FFF
/2000 - 3FFF
/4000 - 5FFF
/6000 - 7FFF
/8000 - 9FFF
/A000 - BFFF
U3010
MK36000
U3020
MK36000
U4010
MK36000
U3030
MK36000
U4020
MK36000
U4030
MK36000
8K X 8
ROM
U1080
74LS138
SELECTION LOGIC
ROM
RAM
C000 - C3FF
C400 - C7FF
D000 - D3FF
D400 - D7FF
D800 - DBFF
DC00 - DFFF
/CS0
/CS1
/CS2
/CS3
/CS4
/CS5
/CS6
U1045
U2045
U1040
U2040
U1055
U2055
U1050
U2050
U1065
U2065
U1060
U2060
U1070
U2070
6514
OR
μPD444
BS1
A0 - A12
AD0 - AD7
R3073
4.7K
+5V
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
P/O A09 CENTRAL PROCESSING UNIT BD.



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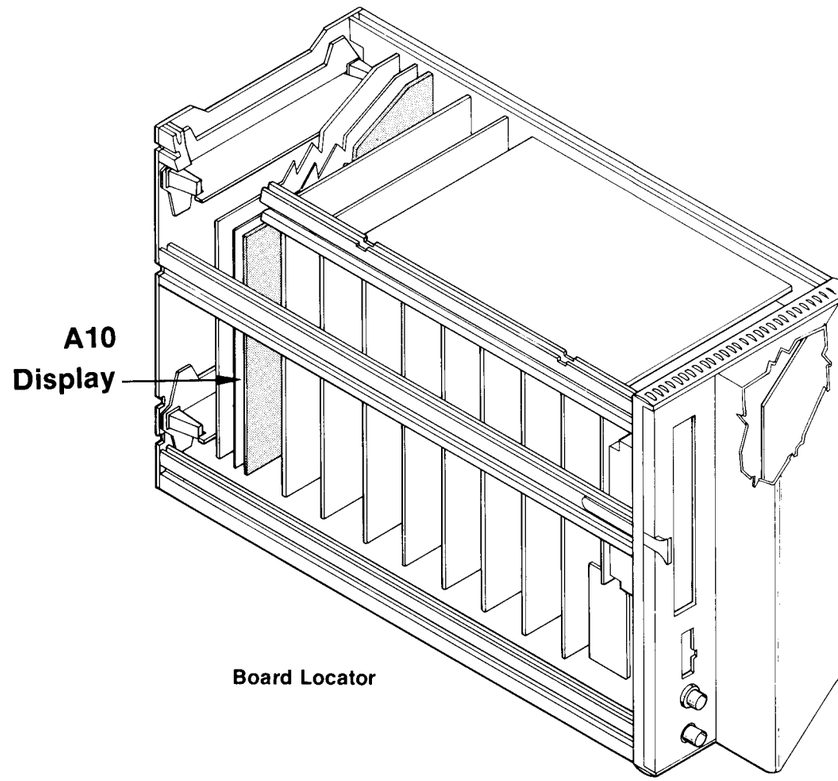
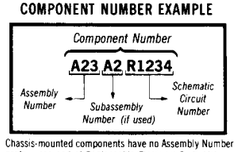


Figure 7-10A. A10 Display board component locations.

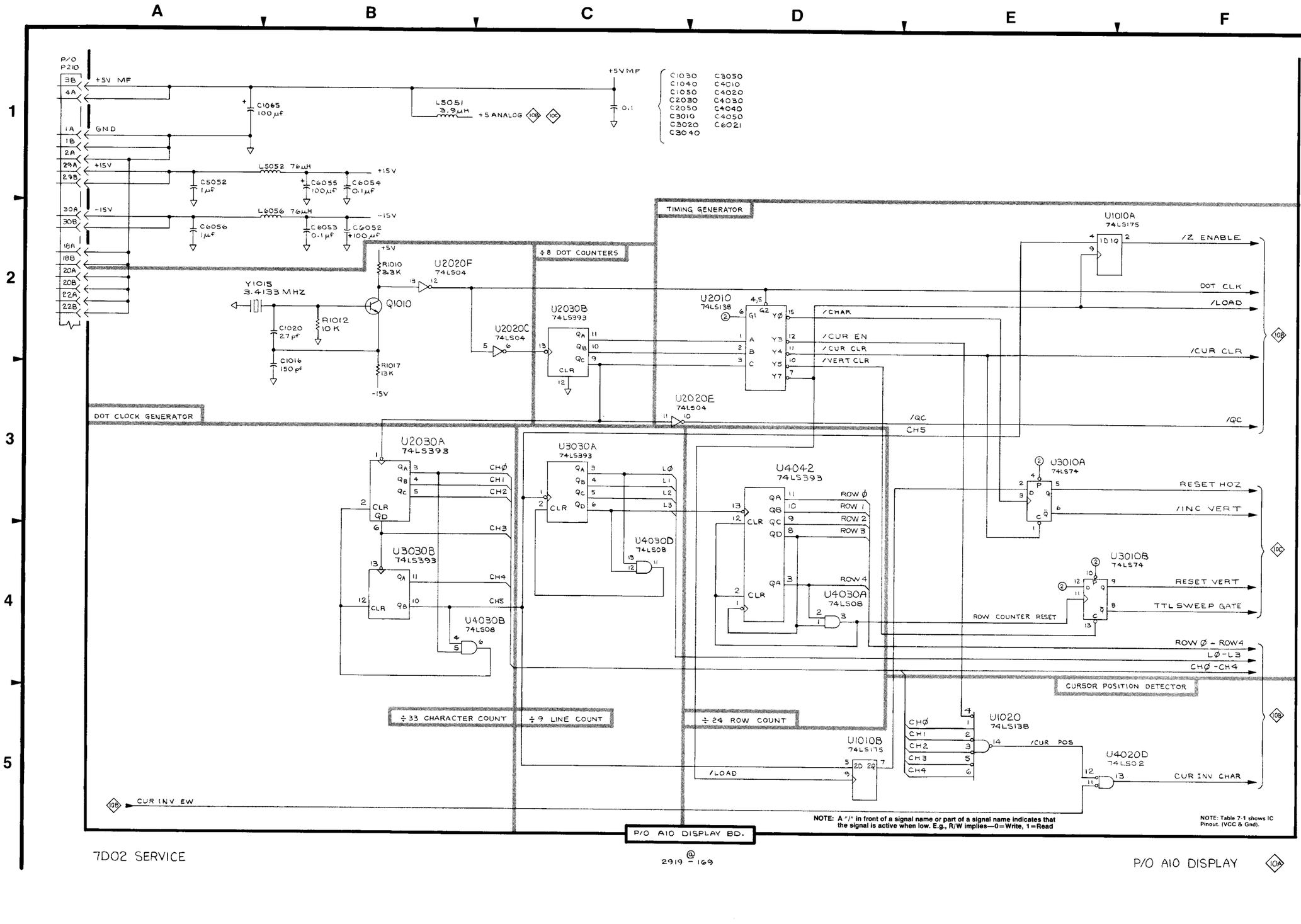
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@



NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read

NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).

P/O A10 DISPLAY BD.

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7D02 SERVICE

P/O A10 DISPLAY 10A

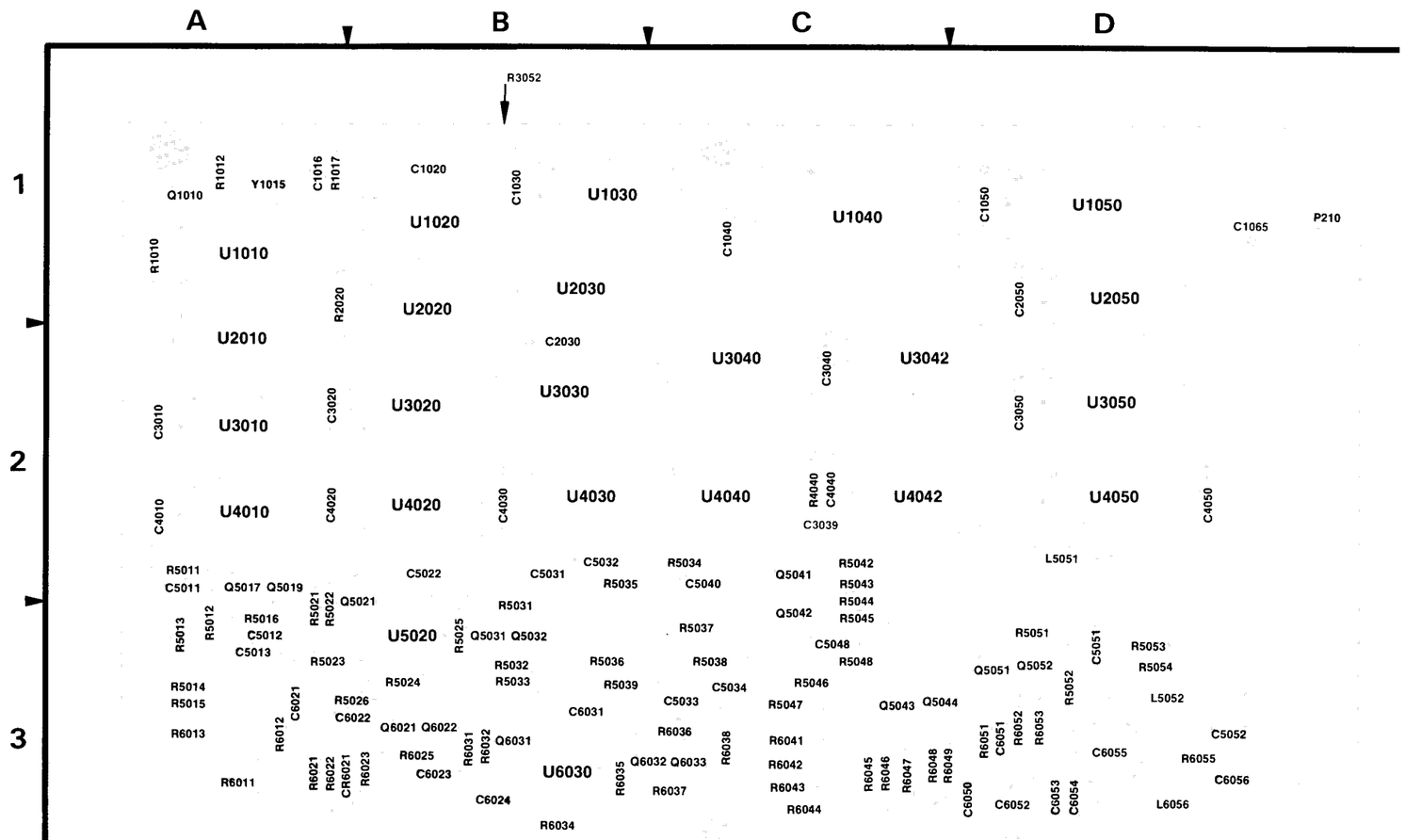

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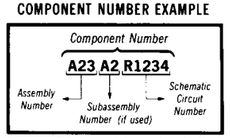
Figure 7-10B. A10 Display board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

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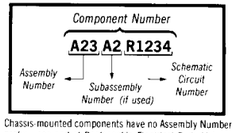
P/O A10 DISPLAY DIAGRAM 10C

ASSEMBLY A10					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C5011	C3	A2	R5024	C4	B3
C5012	D4	A3	R5025	C4	B3
C5022	B4	B2	R5026	C2	B3
C5031	E4	B2	R5031	E4	B2
C5032	C5	B2	R5032	D4	B3
C5033	E3	C3	R5033	D4	B3
C5034	B3	C3	R5034	E4	C2
C5040	E4	C2	R5035	E4	B2
C5048	E5	C3	R5036	E4	B3
C5051	C1	D3	R5037	D4	C3
C6021	C2	A3	R5038	E4	C3
C6022	C2	B3	R5039	D5	B3
C6023	D3	B3	R5046	E3	C3
C6024	D2	B3	R5047	E2	C3
C6031	C3	B3	R5048	B4	C3
C6050	D2	D3	R5051	C1	D3
C6051	D1	D3	R5052	D1	D3
			R5053	C1	D3
CR6021	C2	A3	R5054	D1	D3
			R6011	C2	A3
P210	A1	D1	R6012	B2	A3
P210	A4	D1	R6013	B2	A3
P210	F1	D1	R6021	B2	A3
			R6022	B2	A3
Q5017	C4	A2	R6023	C2	B3
Q5019	C4	A2	R6025	B3	B3
Q5021	B4	B2	R6031	B2	B3
Q5031	E4	B3	R6032	C2	B3
Q5032	D4	B3	R6034	C3	B3
Q5043	F2	C3	R6035	C3	B3
Q5044	D1	C3	R6036	E2	C3
Q5051	B1	D3	R6037	D3	C3
Q5052	C1	D3	R6038	D2	C3
Q6011	B2	B3	R6041	E2	C3
Q6021	C2	B3	R6042	E3	C3
Q6022	C2	B3	R6043	D3	C3
Q6031	B3	B3	R6044	E3	C3
Q6032	E2	B3	R6045	F2	C3
Q6033	D2	C3	R6046	F2	C3
			R6047	F3	C3
R5011	C3	A2	R6048	D1	C3
R5012	C4	A3	R6049	D1	C3
R5013	C3	A3	R6051	D1	D3
R5014	B4	A3	R6052	B2	D3
R5015	B3	A3	R6053	B1	D3
R5016	B4	A3	R6055	B3	D3
R5021	B4	A3			
R5022	C4	A3	U5020	C4	B3
R5023	C4	A3	U6030	C2	B3

Partial A10 also shown on diagram 10A and 10B.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A10 DISPLAY DIAGRAM 10B

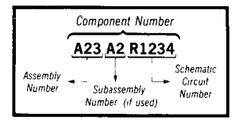
ASSEMBLY A10		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C3039 *	B3	C2
P210	A1	D1
P210	F4	D1
Q5041	E1	C2
Q5042	E2	C3
R2020	D5	A1
R3052 *	A3	B1
R4040	D5	C2
R5042	E1	C2
R5043	E1	C2
R5044	E2	C2
R5045	E2	C3
U1010C	E5	A1
U1010D	E4	A1
U1030	D2	B1
U1040	C2	C1
U1050	B2	D1
U2020A	A2	B1
U2020B	A4	B1
U2020D	B1	B1
U2050	B5	D1
U3020A	A2	B2
U3020B	A4	B2
U3040	C3	C2
U3042	C5	C2
U3050	B4	D2
U4010A	E2	A2
U4010B	D2	A2
U4010C	D4	A2
U4010D	E5	A2
U4020A	D4	B2
U4020B	E2	B2
U4020C	A1	B2
U4030C	D4	B2
U4040A	B2	C2
U4040B	F2	C2
U4050	B3	D2

Partial A10 also shown on 10A and 10C.

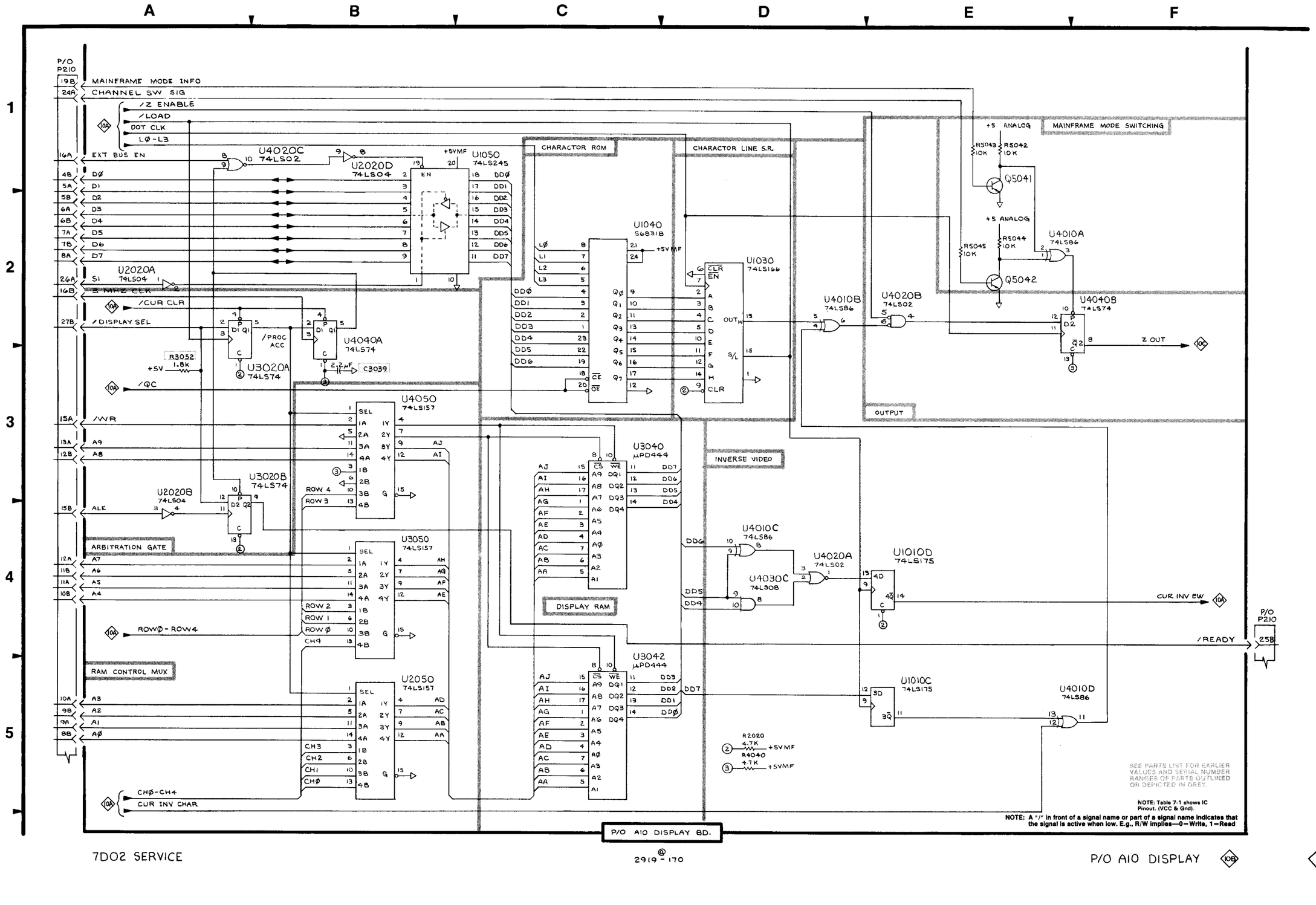
***See Parts List for serial number ranges.**

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
5
P/O P210
19B MAINFRAME MODE INFO
24A CHANNEL SW SIG
/Z ENABLE
/LOAD
DOT CLK
L0-L3
16A EXT BUS EN
4B D0
5A D1
5B D2
6A D3
6B D4
7A D5
7B D6
8A D7
26A SI
16B S MUX CLR
/CUR CLR
27B /DISPLAY SEL
/QC
15A /WR
13A A9
12B A8
15B ALE
ARBITRATION GATE
12A A7
11B A6
11A A5
10B A4
ROW0 - ROW4
RAM CONTROL MUX
10A A3
9B A2
9A A1
8B A0
CH0-CH4
CUR INV CHAR
U2020C 74LS02
U2020D 74LS04
U1050 74LS245
+5VMF
U2020A 74LS04
U4040A 74LS74
/PROC ACC
U3020A 74LS74
R3052 1.8K
+5V
C3039 .2µF
U4050 74LS157
U3020B 74LS74
U2020B 74LS04
U3050 74LS157
U2050 74LS157
CHARACTOR ROM
CHARACTOR LINE S.R.
U1040 S6831B
U1030 74LS166
DISPLAY RAM
U3040 µPD444
U3042 µPD444
INVERSE VIDEO
U4010C 74LS86
U4030C 74L308
U4020A 74LS02
U1010D 74LS175
U1010C 74LS175
U4010D 74LS86
R2020 4.7K +5VMF
R4040 4.7K +5VMF
+5 ANALOG
MAINFRAME MODE SWITCHING
R5043 10K
R5042 10K
Q5041
R5045 10K
R5044 10K
Q5042
U4010A 74LS86
U4010B 74LS86
U4020B 74LS02
U4040B 74LS74
Z OUT
OUTPUT
CUR INV EW
/READY
P/O P210 25B
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
P/O A10 DISPLAY BD.

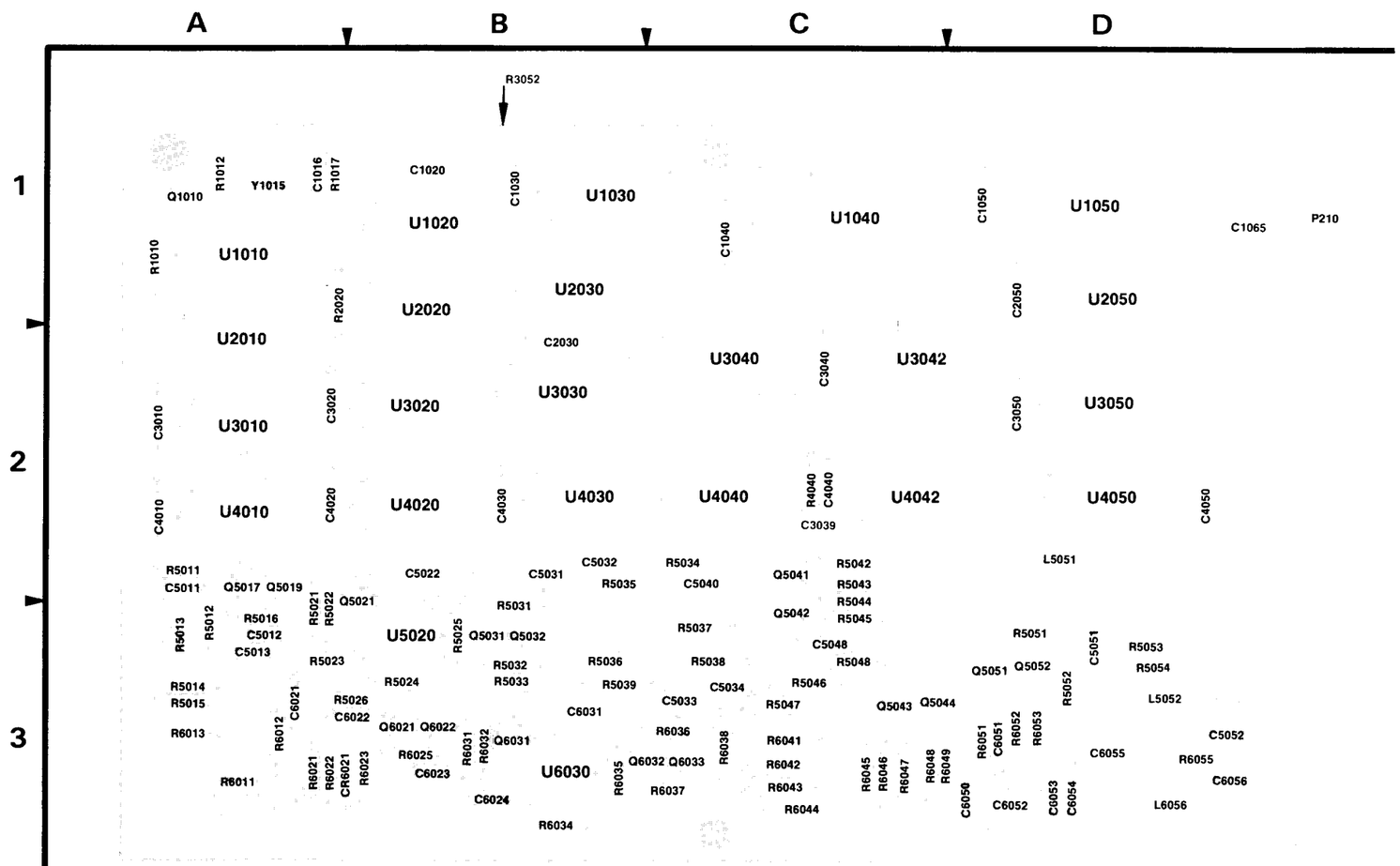


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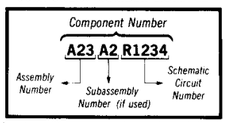
Figure 7-10C. A10 Display board component locations.

A10 DISPLAY BOARD

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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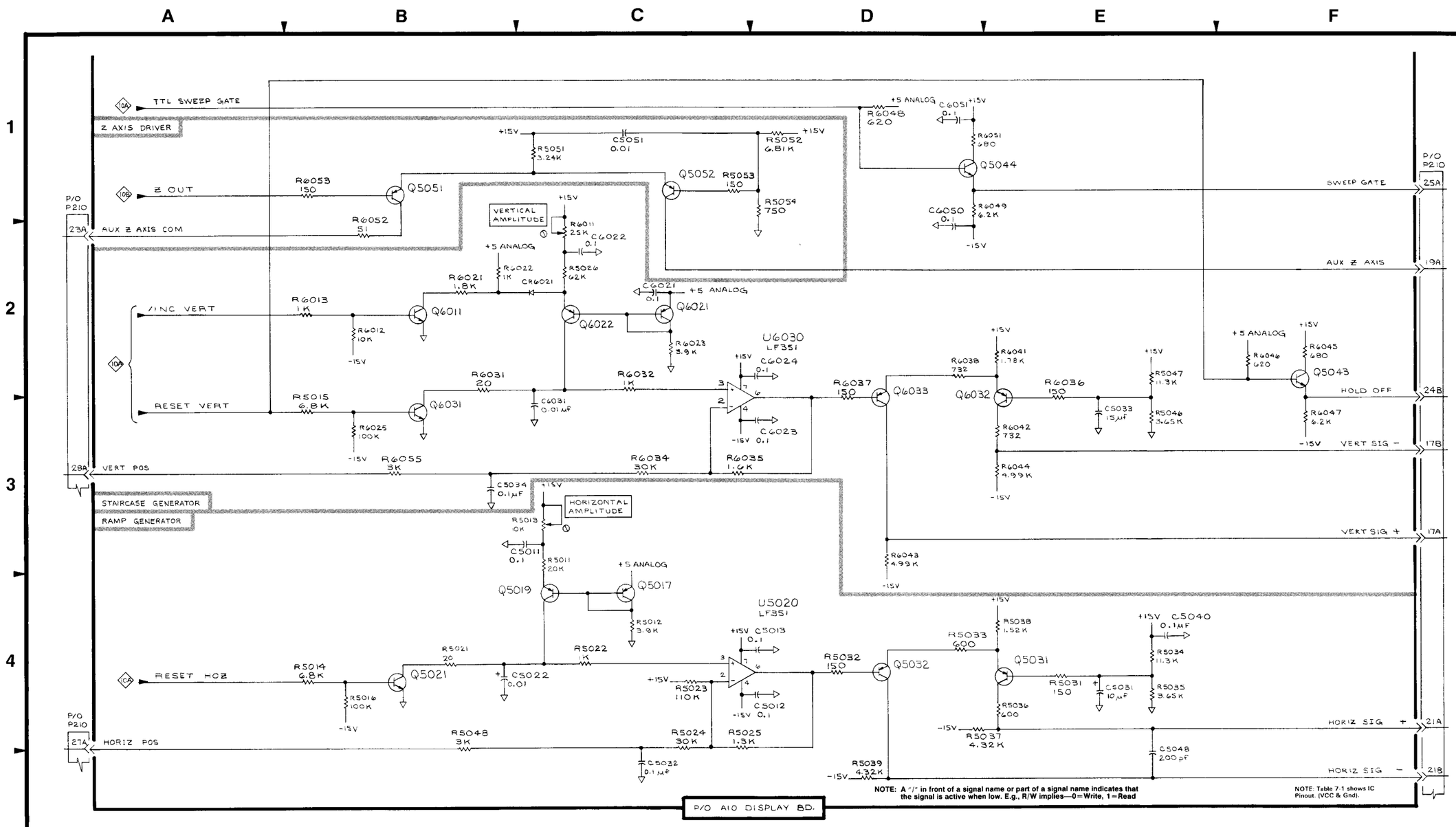
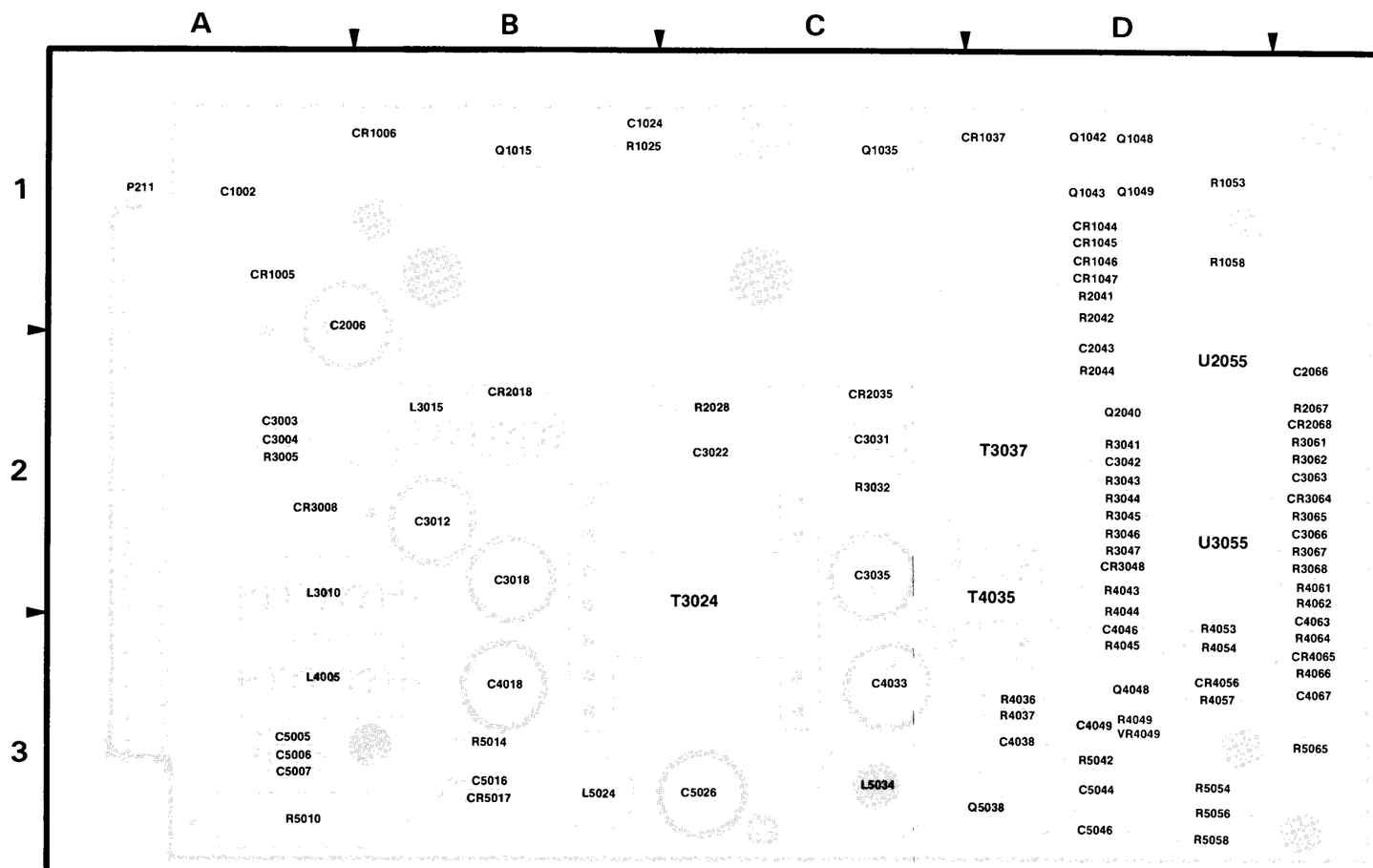


NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read

NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).



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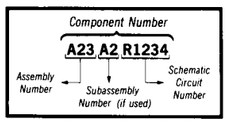
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

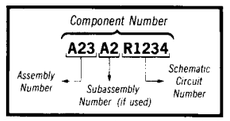
Figure 7-11. A11 Power Supply board component locations.

A12 VERTICAL INTERFACE DIAGRAM 12

ASSEMBLY A12		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P212	A1	B1
P213	C2	A1

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

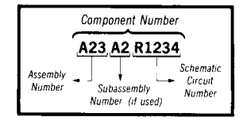
A11 POWER SUPPLY DIAGRAM 11

ASSEMBLY A11					
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1002	F2	A1	Q1049	C2	D1
C1024	D2	B1	Q2040	D4	D2
C2006	F2	A1	Q4048	E2	D3
C2043	D1	D2	Q5038	D4	D3
C2066	C2	E2			
C3003	E2	A2	R1025	D2	B1
C3004	E2	A2	R1053	C2	D1
C3012	F4	B2	R1058	C1	D1
C3018	D2	B2	R2028	D2	C2
C3022	D2	C2	R2041	D1	D1
C3031	E2	C2	R2042	D1	D1
C3035	E2	C2	R2044	D4	D2
C3042	C4	D2	R2067	C2	E2
C3063	B2	E2	R3005	F3	A2
C3066	B2	E2	R3032	E2	C2
C4018	A3	B3	R3041	D4	D2
C4033	A4	C3	R3043	C4	D2
C4038	A4	D3	R3044	C4	D2
C4046	E4	D3	R3045	B4	D2
C4049	A2	D3	R3046	B4	D2
C4063	A2	E3	R3047	B4	D2
C4067	B2	E3	R3061	C2	E2
C5005	A3	A3	R3062	B2	E2
C5006	A4	A3	R3065	B1	E2
C5007	F4	A3	R3067	A1	E2
C5016	E3	B3	R3068	A1	E2
C5026	D4	C3	R4036	E2	D3
C5044	B3	D3	R4037	E2	D3
C5046	A2	D3	R4043	C4	D2
			R4044	C4	D3
CR1006	D2	B1	R4045	E4	D3
CR1037	D2	D1	R4049 *	A2	D3
CR1044	C2	D1	R4053	A3	D3
CR1045	C2	D1	R4054	B2	D3
CR1046	C1	D1	R4057	A2	D3
CR1047	C2	D1	R4061	B1	E2
CR2018	E2	B2	R4062	B2	E3
CR2035	E2	C2	R4064	B2	E3
CR2068	C2	E2	R4066	B2	E3
CR3008	F4	A2	R5010	E4	A3
CR3048	C4	D2	R5014	D2	B3
CR3064	B2	E2	R5042	B3	D3
CR4056	A3	D3	R5054 *	A2	D3
CR4065	B2	E3	R5056	A2	D3
CR5017	D4	B3	R5058 *	A2	D3
			R5065	A2	E3
L3010	A3	A2			
L3015	E3	B2	T3024	E2	C2
L4005	A4	A3	T3037	D2	D2
L5024	E4	B3	T4035	E2	D2
L5034	D4	C3			
			U2055A	B2	D2
P211	A3	A1	U2055B	B1	D2
			U3055A	B4	D2
Q1015	D2	B1	U3055B	C4	D2
Q1035	D2	C1	U3055D	B2	D2
Q1042	C2	D1	U3055	B1	D2
Q1043	C1	D1			
Q1048	C2	D1	VR4049 *	A2	D3

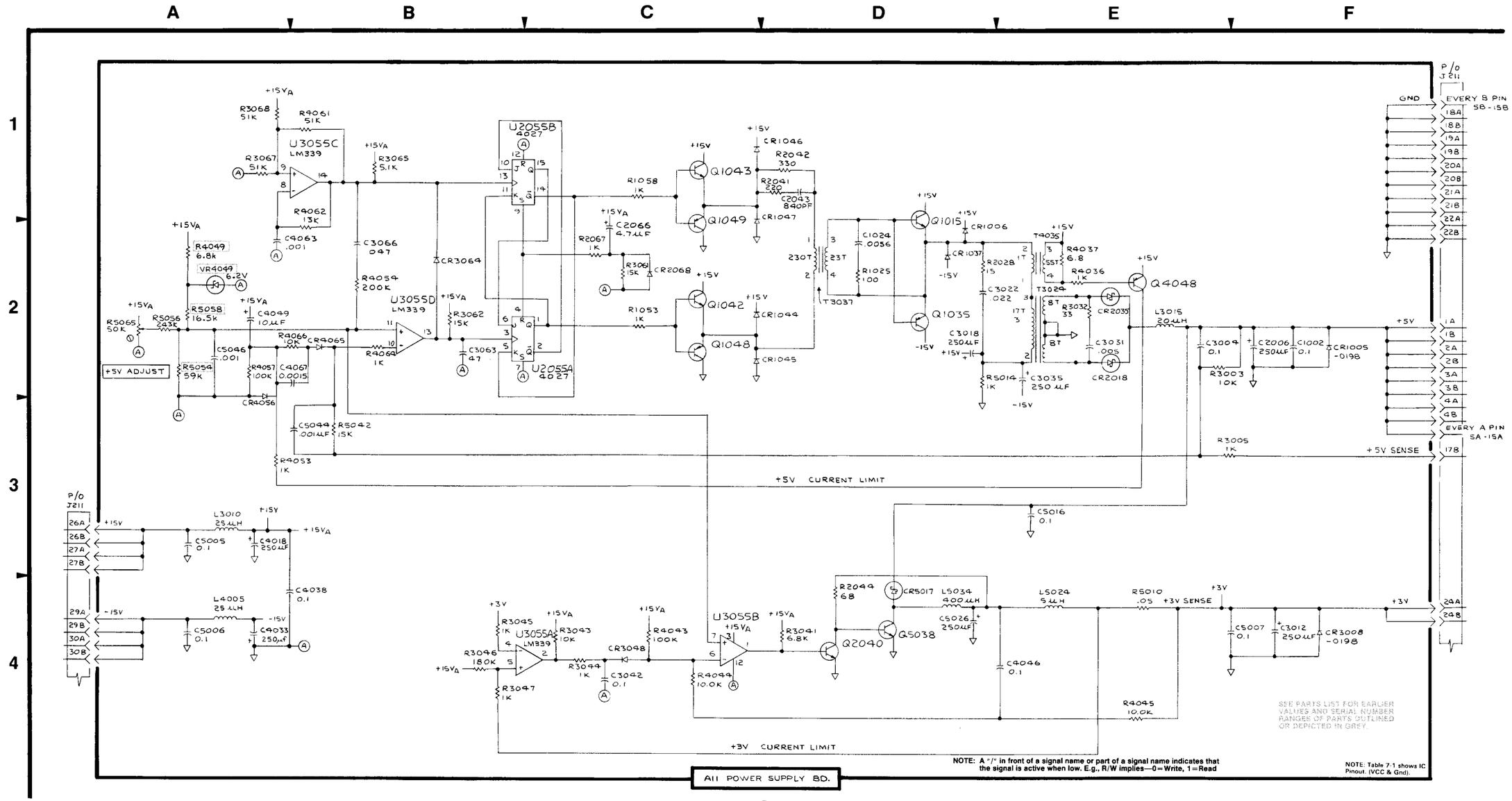
***See Parts List for serial number ranges.**

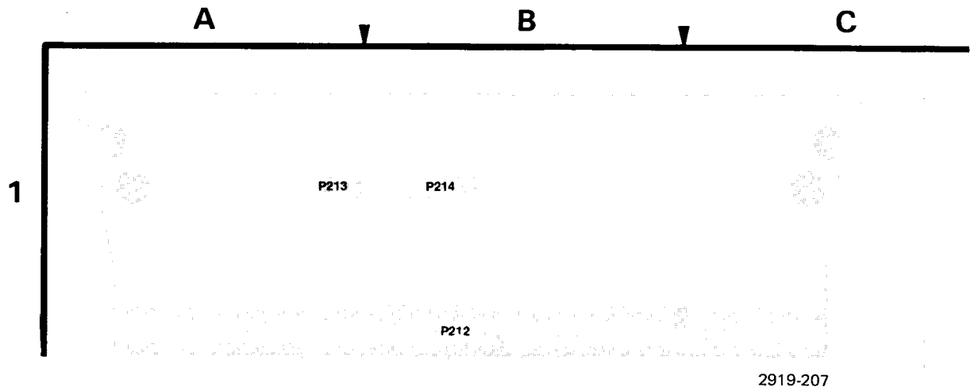
Static Sensitive Devices
See Maintenance Section

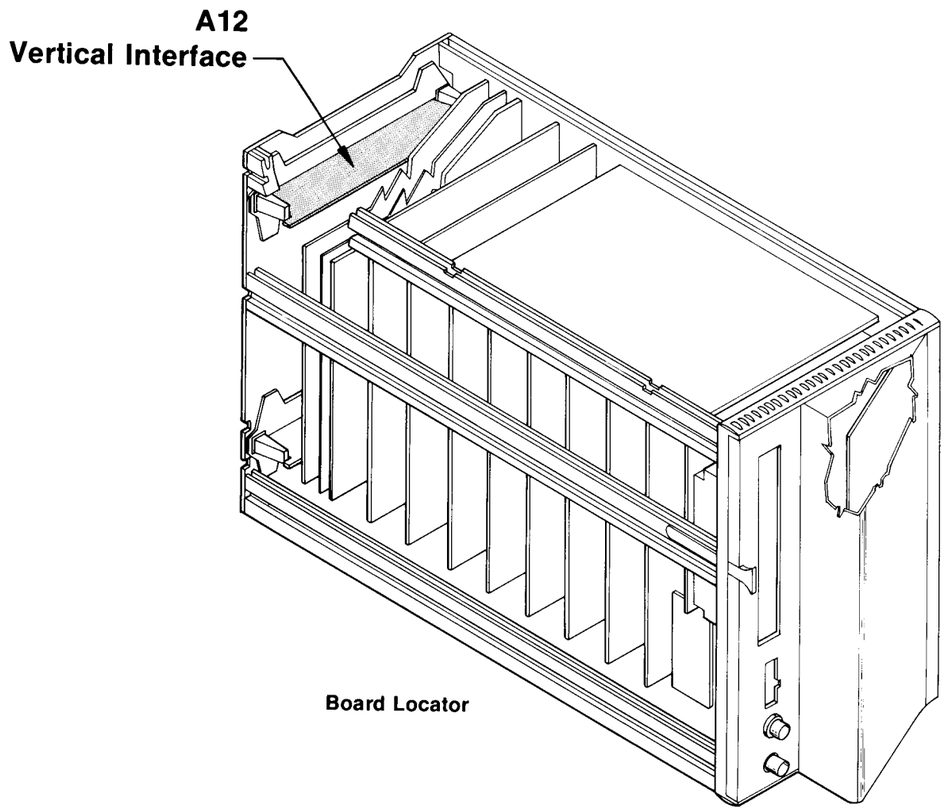
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

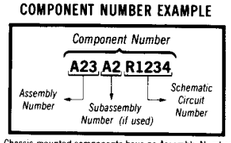

A
B
C
D
E
F
1
2
3
4
U3055C LM339
U3055D LM339
U3055A LM339
U3055B LM339
U2055B 4027
U2055A 4027
+15VA
+15V
-15V
+3V
+5V ADJUST
+5V CURRENT LIMIT
+3V CURRENT LIMIT
+5V SENSE
+3V SENSE
P/O J211
EVERY B PIN 5B-15B
EVERY A PIN 5A-15A
GND
A11 POWER SUPPLY BD.
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).





Static Sensitive Devices
See Maintenance Section

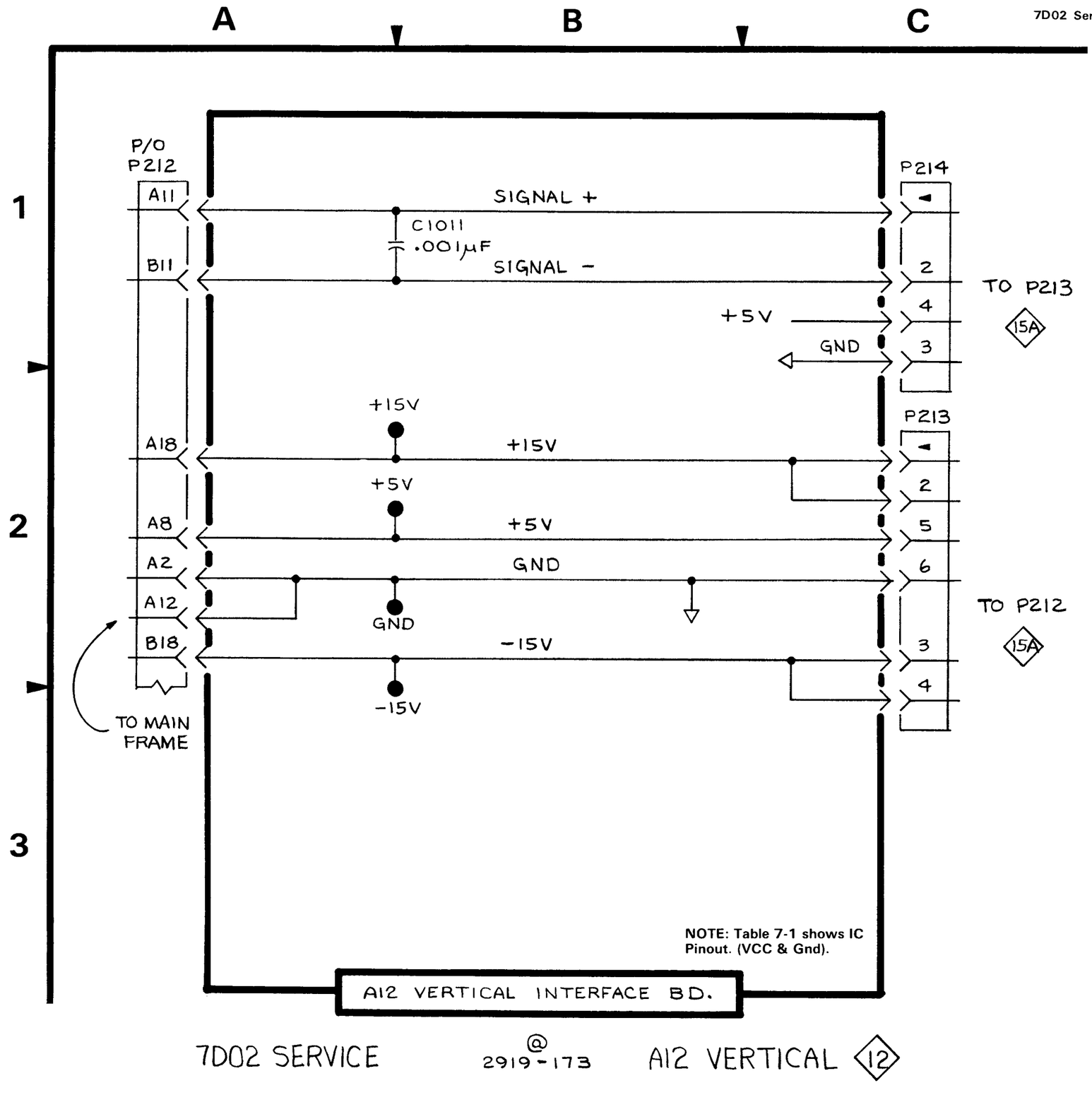
COMPONENT NUMBER EXAMPLE



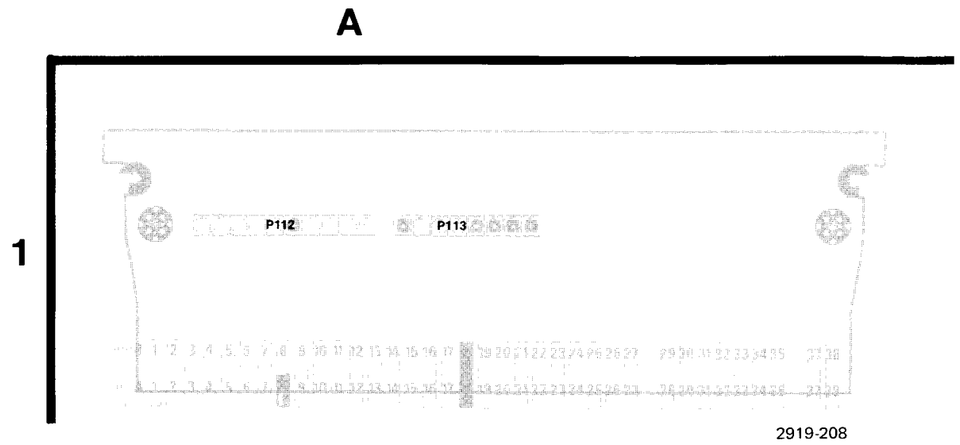
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

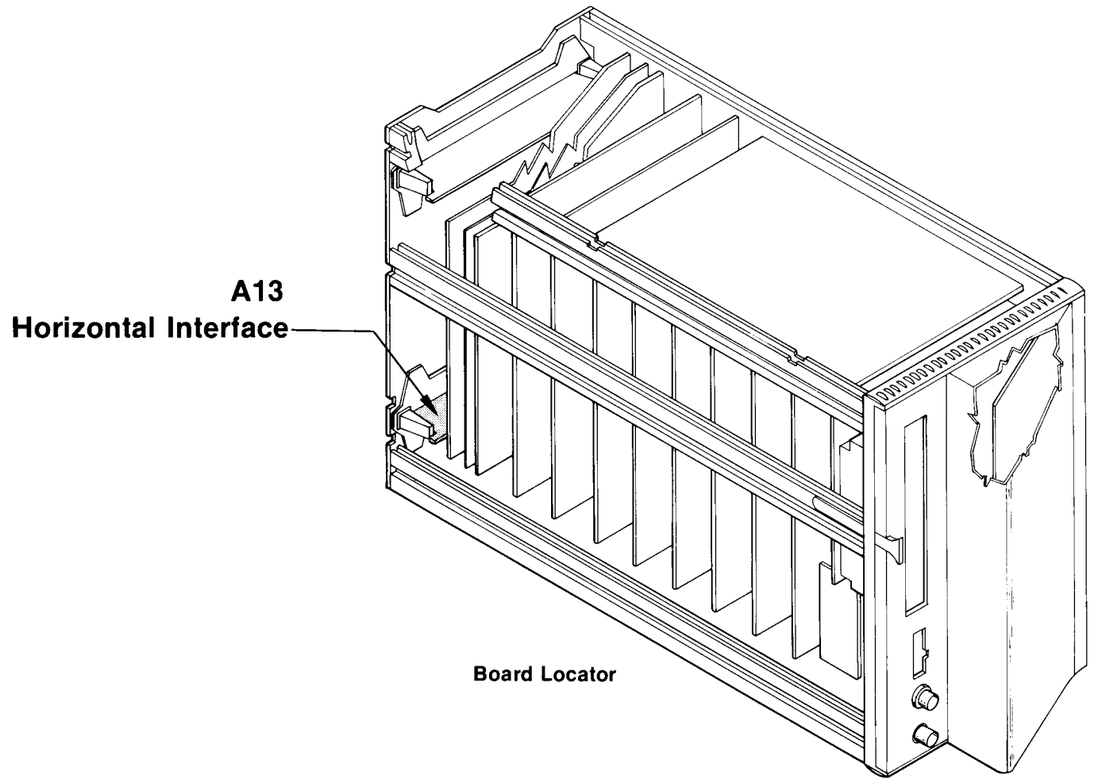
Figure 7-12. A12 Vertical interface board component locations.



7D02 SERVICE @ 2919-173 A12 VERTICAL 12

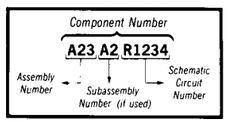


2919-208



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

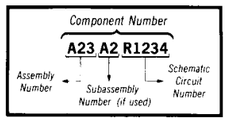
Figure 7-13. A13 Horizontal interface board component locations.

P/O A14 PROBE INTERFACE DIAGRAM 14A

Assembly A14		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J101	D1	A1
J102	D1	A2
J103	C1	B2
J104	C1	B1
J105	B1	B1
J106	A1	C2
J107	A1	C1

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



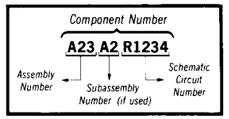
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

A13 HORIZONTAL INTERFACE DIAGRAM 13

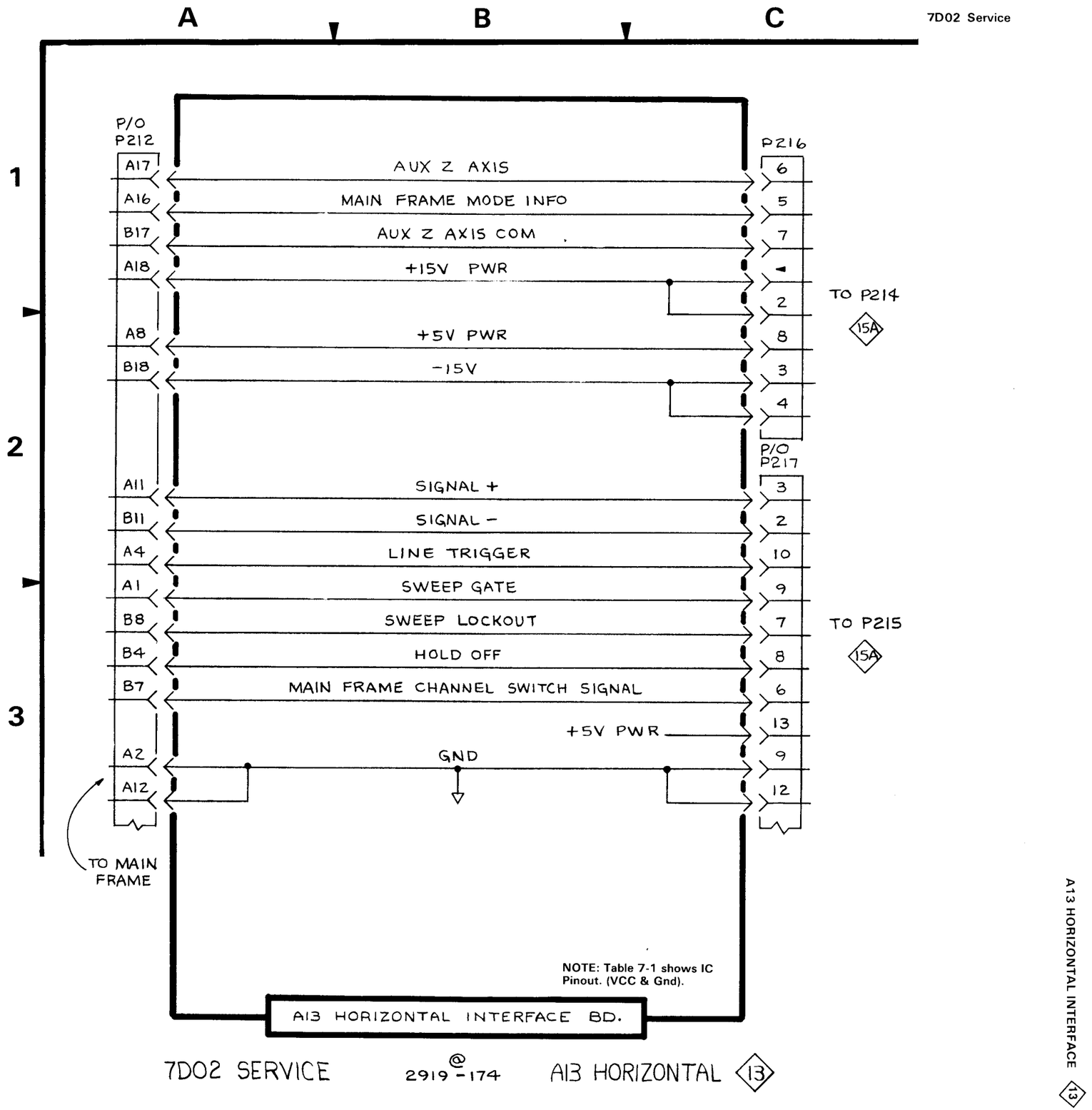
ASSEMBLY A13		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P212	A1	A1
P216	C1	A1
P217	C2	A1

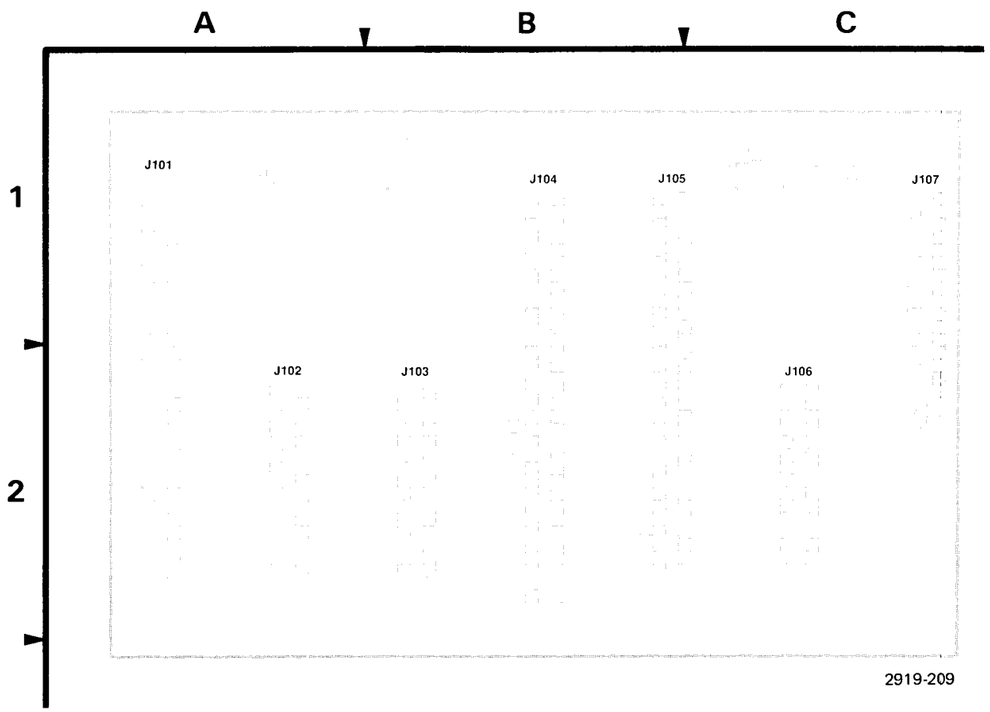
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

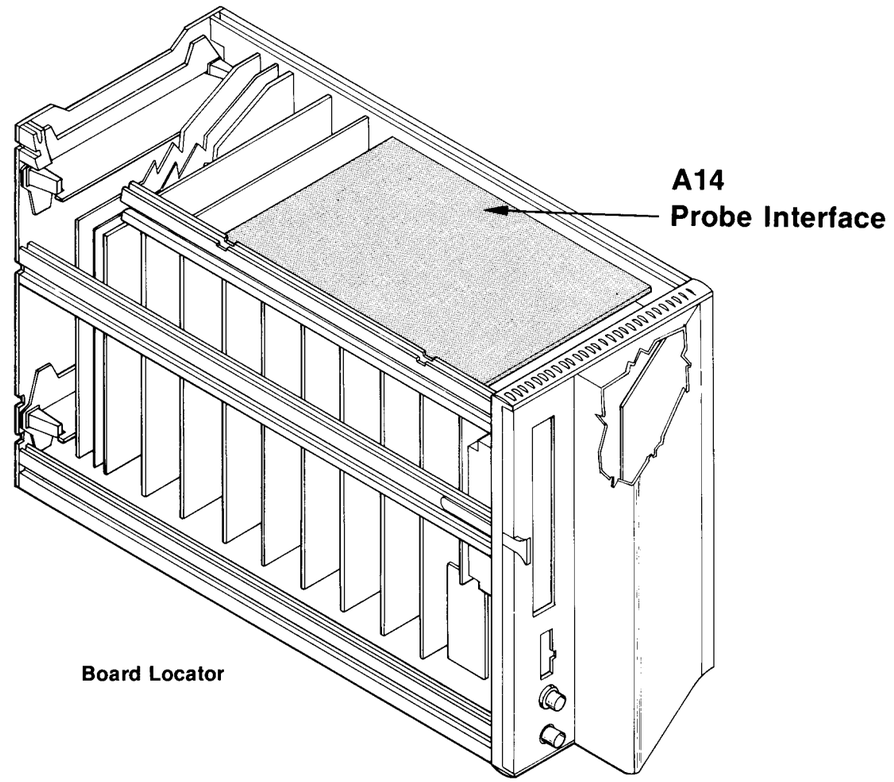


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
1
2
3
P/O P212
A17
A16
B17
A18
A8
B18
A11
B11
A4
A1
B8
B4
B7
A2
A12
P216
6
5
7
4
2
8
3
P/O P217
3
2
10
9
7
8
6
13
9
12
AUX Z AXIS
MAIN FRAME MODE INFO
AUX Z AXIS COM
+15V PWR
+5V PWR
-15V
SIGNAL +
SIGNAL -
LINE TRIGGER
SWEEP GATE
SWEEP LOCKOUT
HOLD OFF
MAIN FRAME CHANNEL SWITCH SIGNAL
+5V PWR
GND
TO P214
15A
TO P215
15A
TO MAIN FRAME
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
A13 HORIZONTAL INTERFACE BD.
7D02 SERVICE
2919-174
A13 HORIZONTAL
13

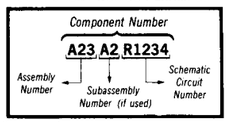


2919-209



Static Sensitive Devices
See Maintenance Section

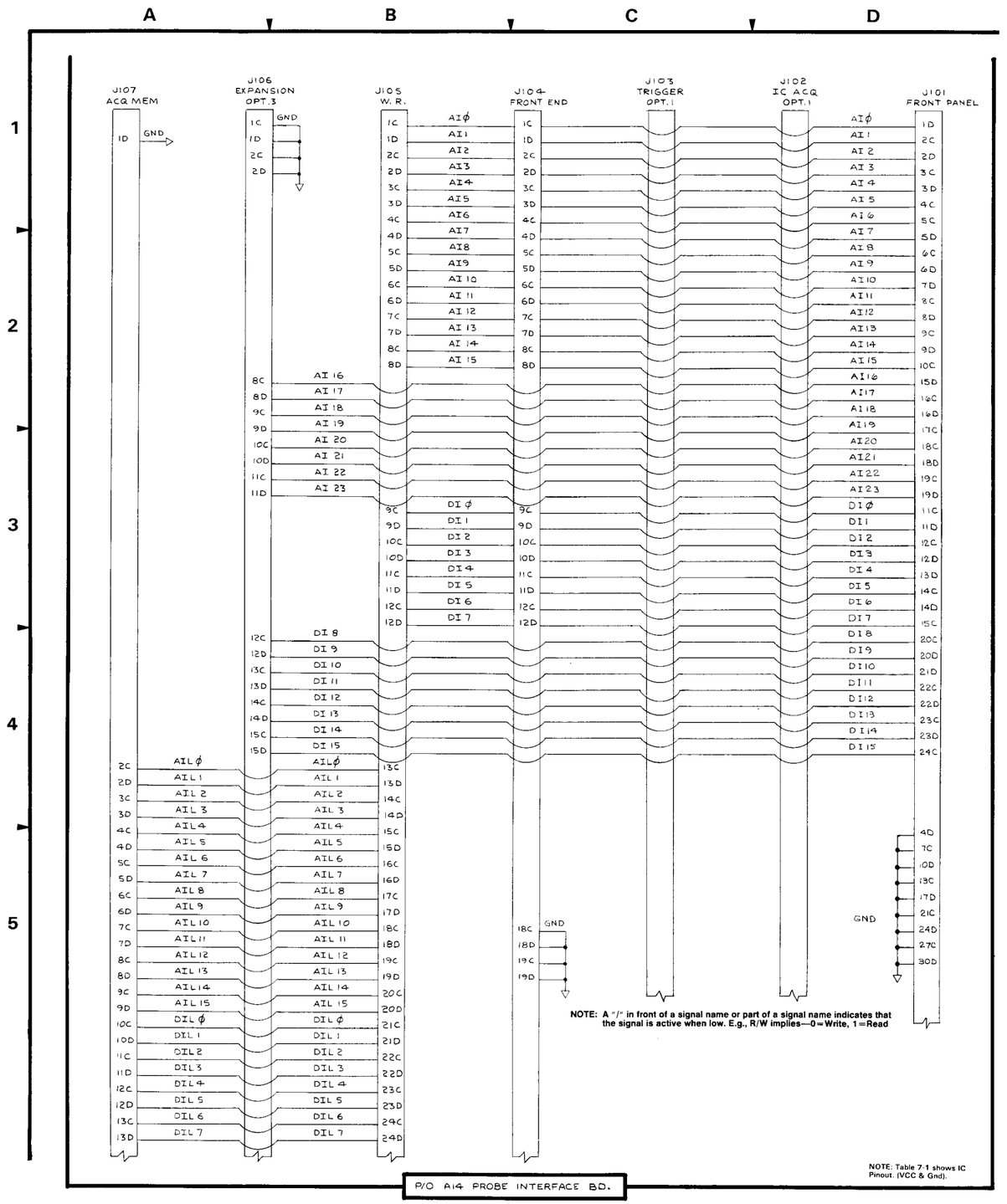
COMPONENT NUMBER EXAMPLE

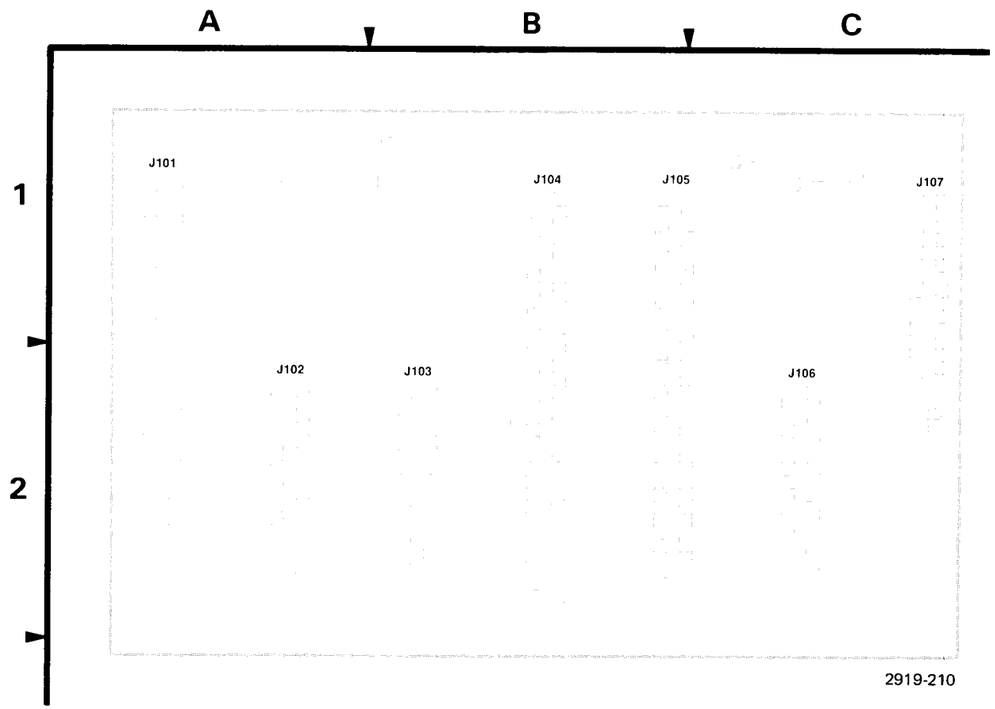


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

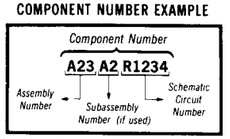
Figure 7-14A. A14 Probe interface board component locations.


A
B
C
D
1
2
3
4
5
J107 ACQ MEM
J106 EXPANSION OPT. 3
J105 W. R.
J104 FRONT END
J103 TRIGGER OPT. 1
J102 IC ACQ OPT. 1
J101 FRONT PANEL
1D GND
1C 1D 2C 2D GND
AI Ø AI 1 AI 2 AI 3 AI 4 AI 5 AI 6 AI 7 AI 8 AI 9 AI 10 AI 11 AI 12 AI 13 AI 14 AI 15
8C AI 16
8D AI 17
9C AI 18
9D AI 19
10C AI 20
10D AI 21
11C AI 22
11D AI 23
DI Ø DI 1 DI 2 DI 3 DI 4 DI 5 DI 6 DI 7
12C DI 8
12D DI 9
13C DI 10
13D DI 11
14C DI 12
14D DI 13
15C DI 14
15D DI 15
2C AIL Ø
2D AIL 1
3C AIL 2
3D AIL 3
4C AIL 4
4D AIL 5
5C AIL 6
5D AIL 7
6C AIL 8
6D AIL 9
7C AIL 10
7D AIL 11
8C AIL 12
8D AIL 13
9C AIL 14
9D AIL 15
10C DIL Ø
10D DIL 1
11C DIL 2
11D DIL 3
12C DIL 4
12D DIL 5
13C DIL 6
13D DIL 7
18C GND
18D
19C
19D
4D 7C 10D 13C 17D 21C 24D 27C 30D GND
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A14 PROBE INTERFACE BD.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

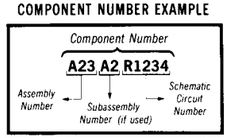
Figure 7-14B. A14 Probe interface board component locations.

P/O A15 MAIN INTERFACE DIAGRAM 15A

ASSEMBLY A15		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C203	D3	D3
C204	D3	D3
C209	B3	B3
C210	B3	B3
J201	F1	F2
J202	F1	e2
J203	E1	e2
J204	E1	D2
J205	D1	D2
J206	D1	C2
J207	C1	C2
J208	C1	B2
J209	B1	B2
J210	B1	B2
J211	B1	A2
P212	A2	A1
P212	A3	A1
P213	A2	A2
P214	A3	A2
P214	A4	A2
P215	A3	A3
P215	A4	A3
Partial A15 also shown on diagram 15B and 15C.		

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



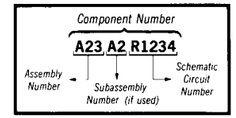
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A14 PROBE INTERFACE DIAGRAM 14B

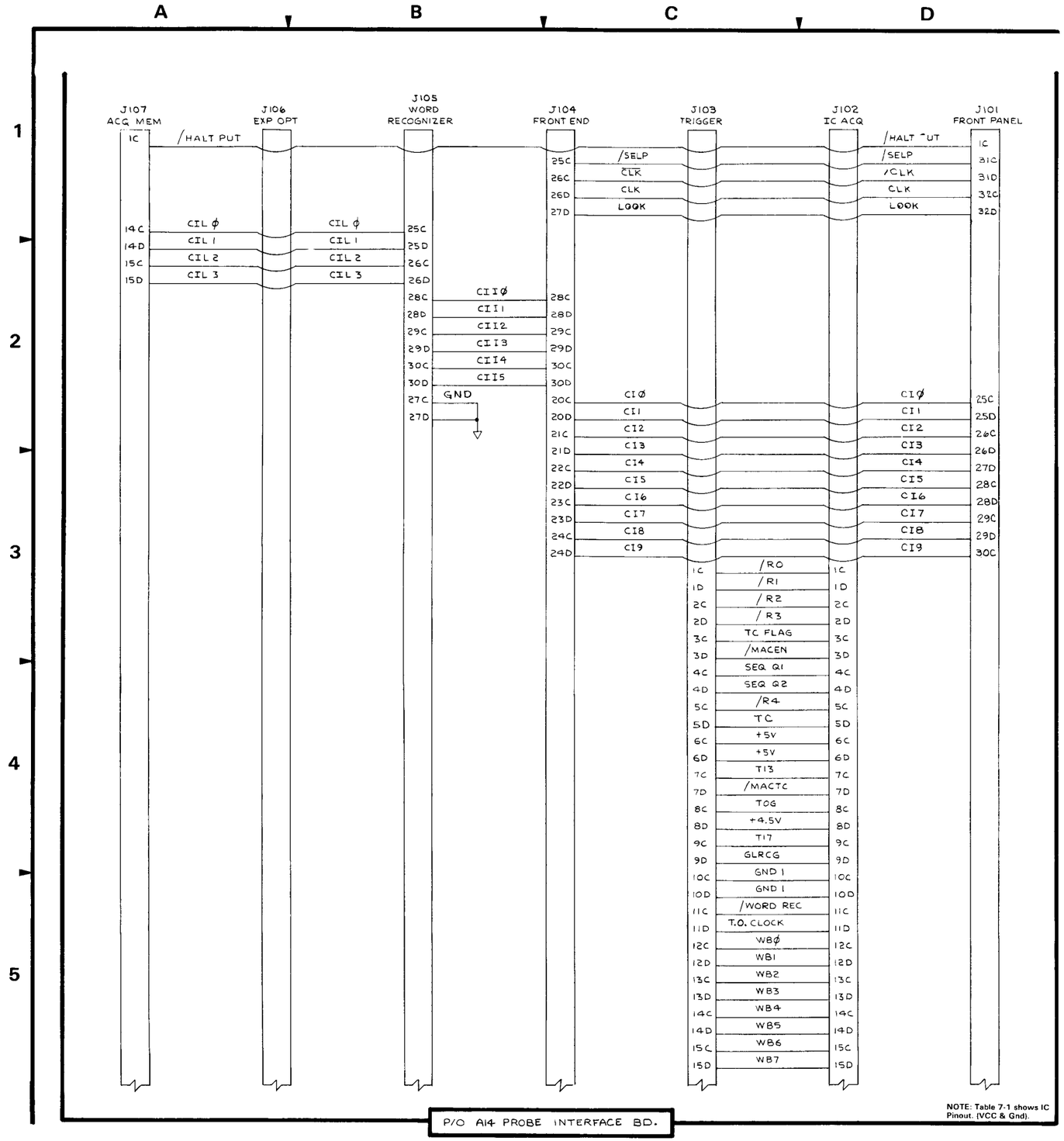
Assembly A14		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J101	D1	A1
J102	D1	A2
J103	C1	B2
J104	C1	B1
J105	B1	B1
J106	A1	C2
J107	A1	C1
Partial A14 also shown on 14A		

Static Sensitive Devices
See Maintenance Section

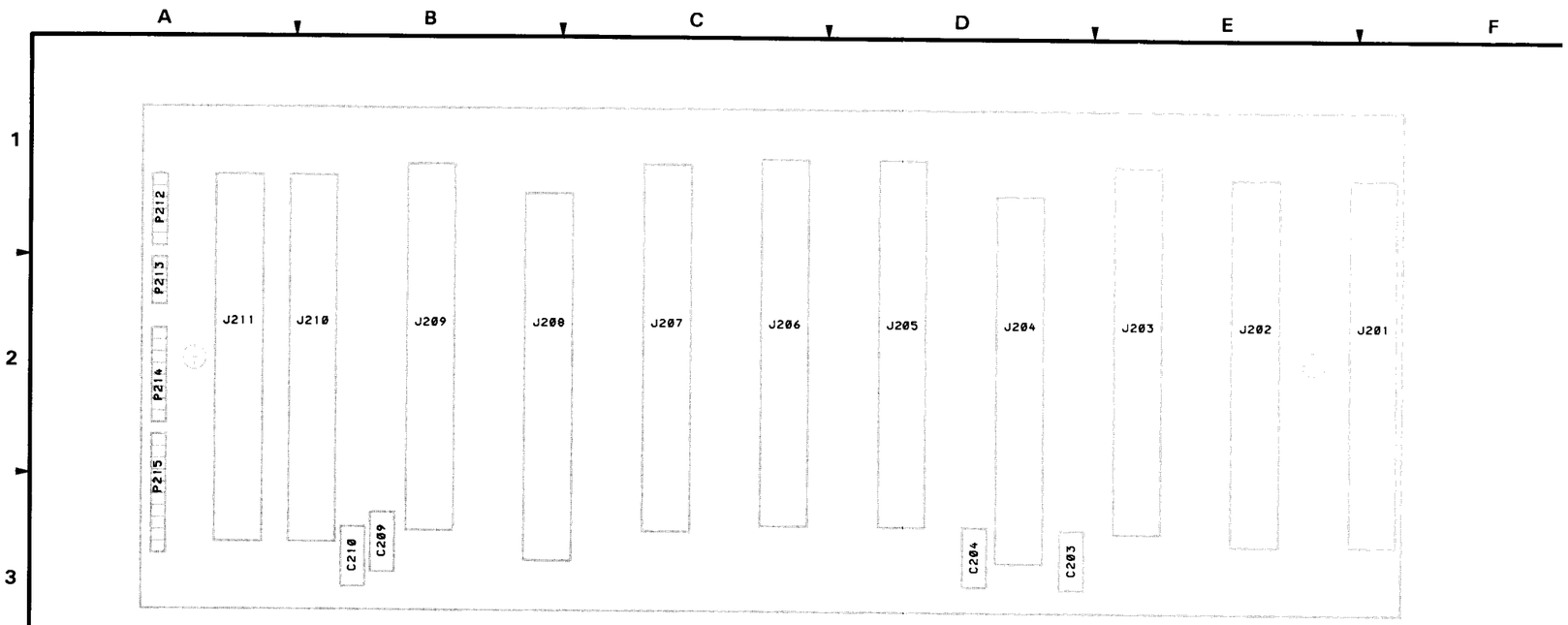
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



7D02 SERVICE @ 2919-176 P/O A14 PROBE INTERFACE 14B



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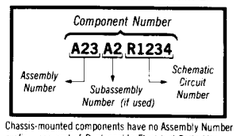
Static Sensitive Devices
See Maintenance Section

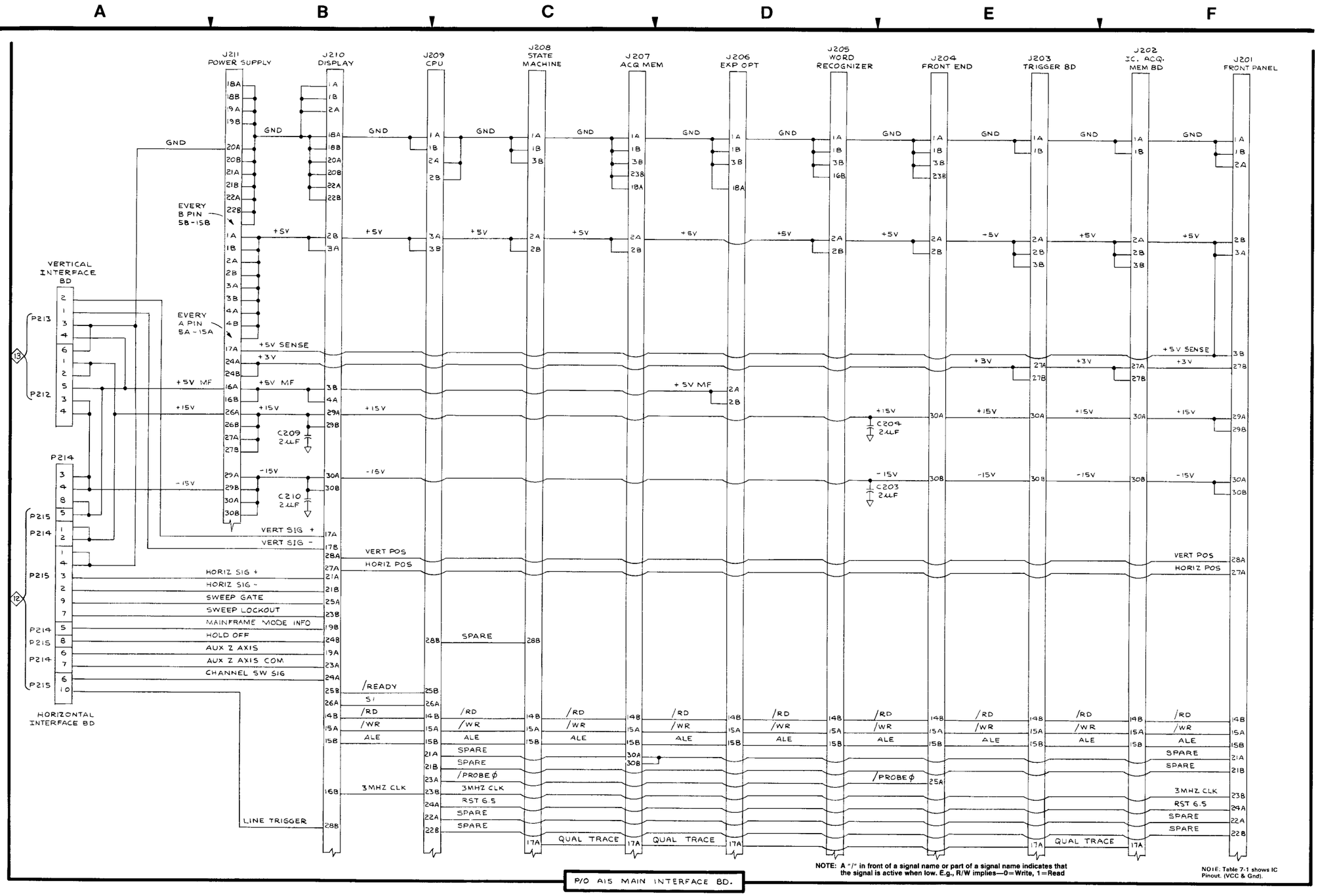
COMPONENT NUMBER EXAMPLE

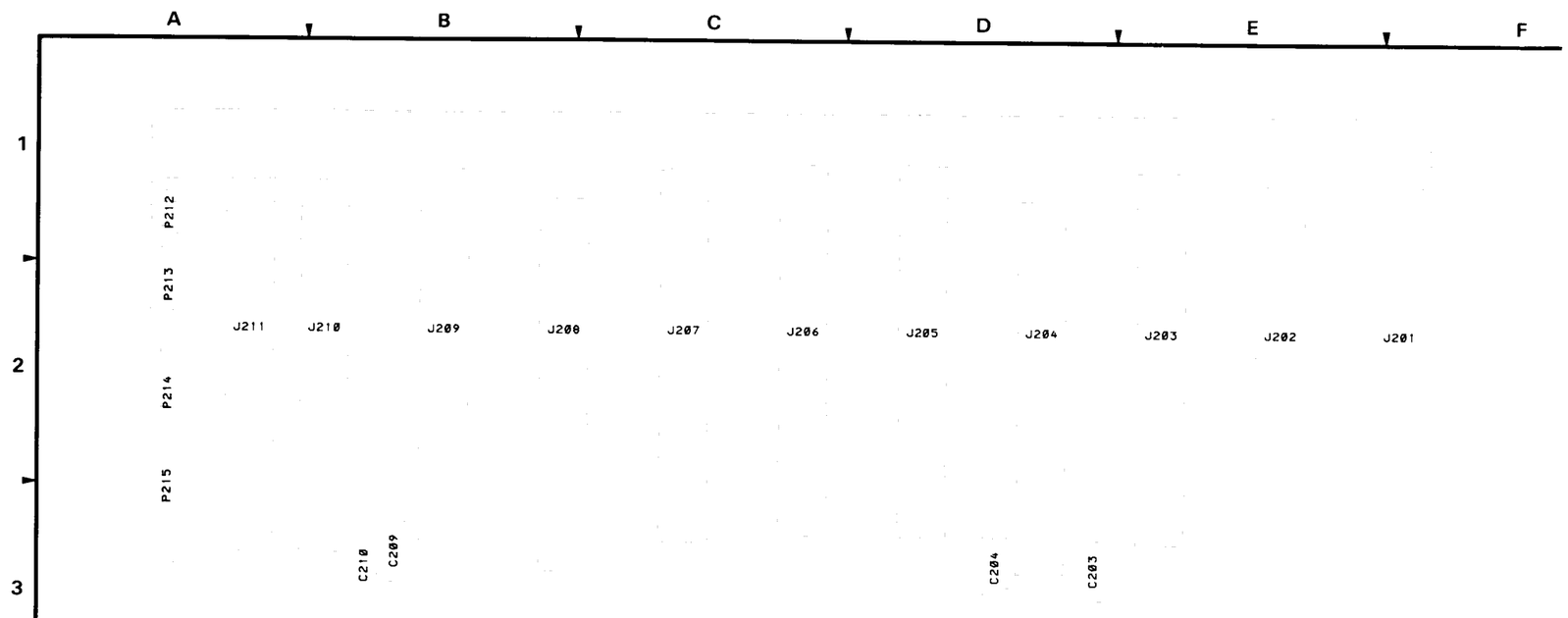


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

Figure 7-15A. A15 Main interface board component locations.


A
B
C
D
E
F
1
2
3
4
5
J211 POWER SUPPLY
J210 DISPLAY
J209 CPU
J208 STATE MACHINE
J207 ACQ MEM
J206 EXP OPT
J205 WORD RECOGNIZER
J204 FRONT END
J203 TRIGGER BD
J202 IC. ACQ. MEM BD
J201 FRONT PANEL
VERTICAL INTERFACE BD
HORIZONTAL INTERFACE BD
P213
P212
P214
P215
EVERY B PIN 5B-15B
EVERY A PIN 5A-15A
GND
+5V
+5V SENSE
+3V
+5V MF
+15V
-15V
C209 2uF
C210 2uF
C203 2uF
VERT SIG +
VERT SIG -
HORIZ SIG +
HORIZ SIG -
SWEEP GATE
SWEEP LOCKOUT
MAINFRAME MODE INFO
HOLD OFF
AUX Z AXIS
AUX Z AXIS COM
CHANNEL SW SIG
LINE TRIGGER
VERT POS
HORIZ POS
/READY
S1
/RD
/WR
ALE
3MHZ CLK
/PROBE ϕ
RST 6.5
SPARE
QUAL TRACE
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A15 MAIN INTERFACE BD.



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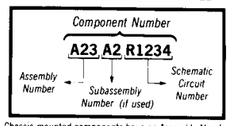
A15 MAIN NTERFACE BOARD

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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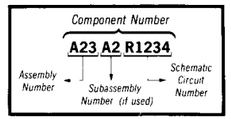
Figure 7-15B. A15 Main interface board component locations.

P/O A15 MAIN INTERFACE DIAGRAM 15C

Assembly A15		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J201	F1	F2
J202	E1	E2
J203	E1	E2
J204	D1	D2
J205	D1	D2
J206	C1	C2
J207	C1	C2
J208	B1	B2
J209	A1	B2
J210	A1	B2
Partial A15 also shown on 15A and 15B.		

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



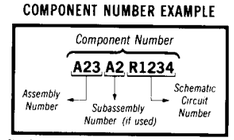
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

P/O A15 MAIN INTERFACE DIAGRAM 15B

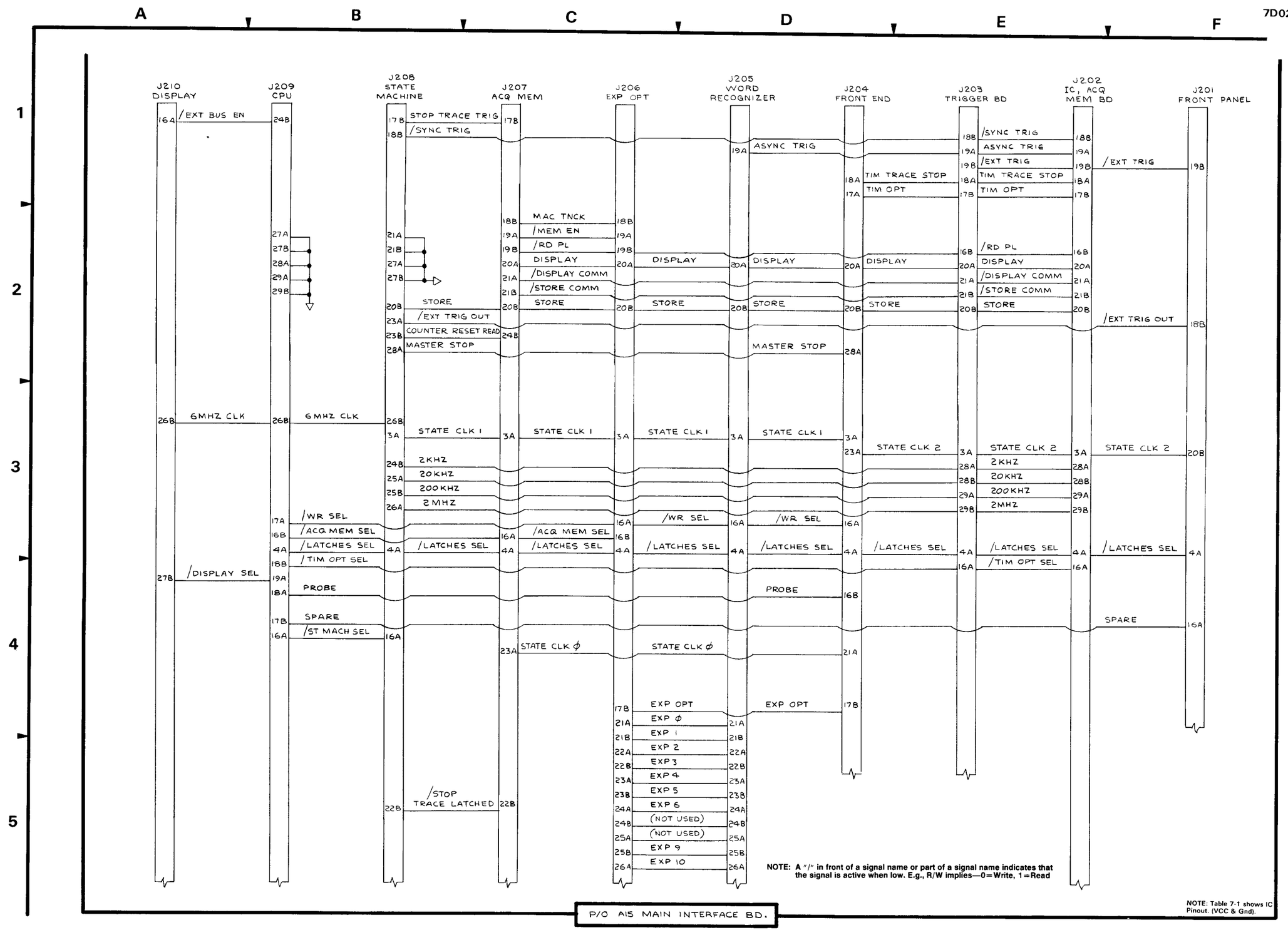
Assembly A15		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J201	F1	F2
J202	E1	E2
J203	E1	E2
J204	D1	D2
J205	D1	D2
J206	C1	C2
J207	C1	C2
J208	B1	B2
J209	A1	B2
J210	A1	B2
Partial A15 also shown on diagram 15A and 15C.		

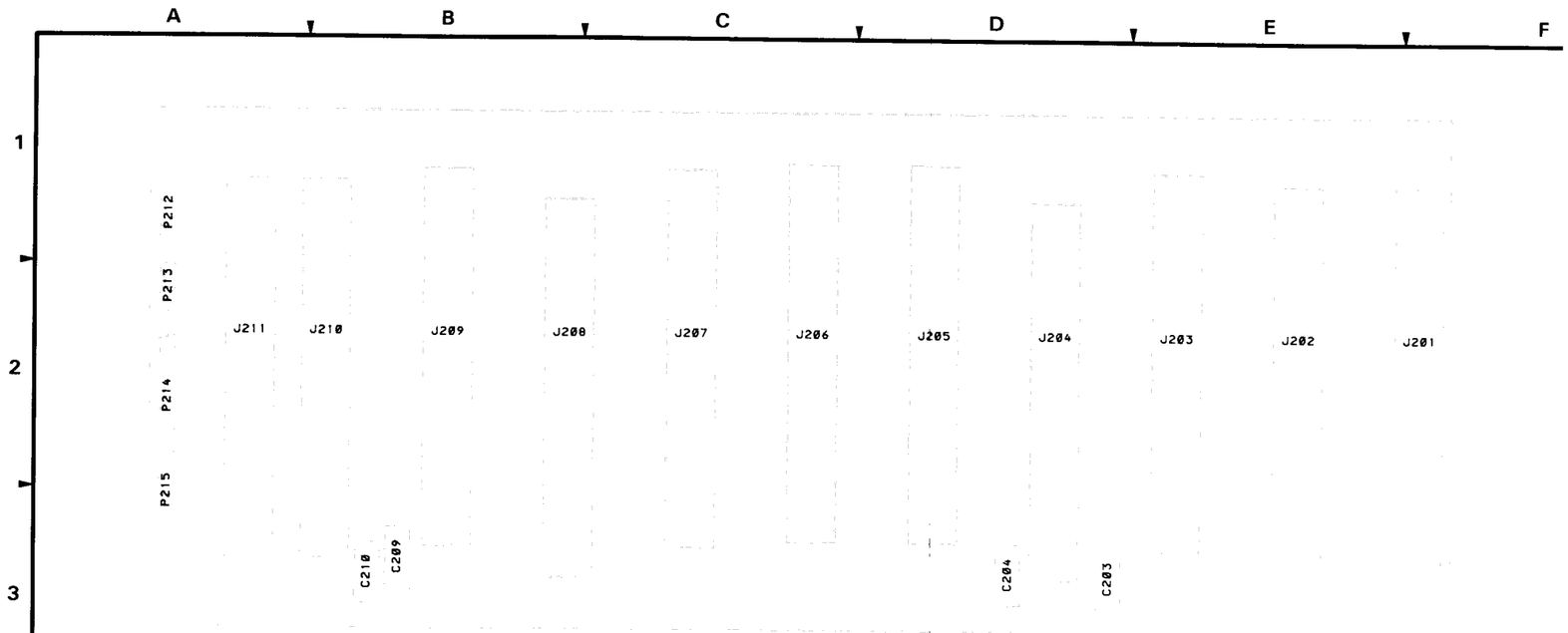
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


A
B
C
D
E
F
1
2
3
4
5
J210 DISPLAY
J209 CPU
J208 STATE MACHINE
J207 ACQ MEM
J206 EXP OPT
J205 WORD RECOGNIZER
J204 FRONT END
J203 TRIGGER BD
J202 IC, ACQ MEM BD
J201 FRONT PANEL
/EXT BUS EN
STOP TRACE TRIG
/SYNC TRIG
ASYNC TRIG
TIM TRACE STOP
TIM OPT
MAC TNCK
/MEM EN
/RD PL
DISPLAY
/DISPLAY COMM
/STORE COMM
STORE
/EXT TRIG OUT
COUNTER RESET READ
MASTER STOP
/EXT TRIG
/EXT TRIG OUT
6MHZ CLK
STATE CLK 1
STATE CLK 2
2KHZ
20KHZ
200KHZ
2MHZ
/WR SEL
/ACQ MEM SEL
/LATCHES SEL
/TIM OPT SEL
/DISPLAY SEL
PROBE
SPARE
/ST MACH SEL
STATE CLK ϕ
/STOP TRACE LATCHED
EXP OPT
EXP ϕ
EXP 1
EXP 2
EXP 3
EXP 4
EXP 5
EXP 6
(NOT USED)
(NOT USED)
EXP 9
EXP 10
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A15 MAIN INTERFACE BD.



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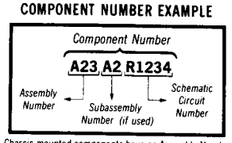
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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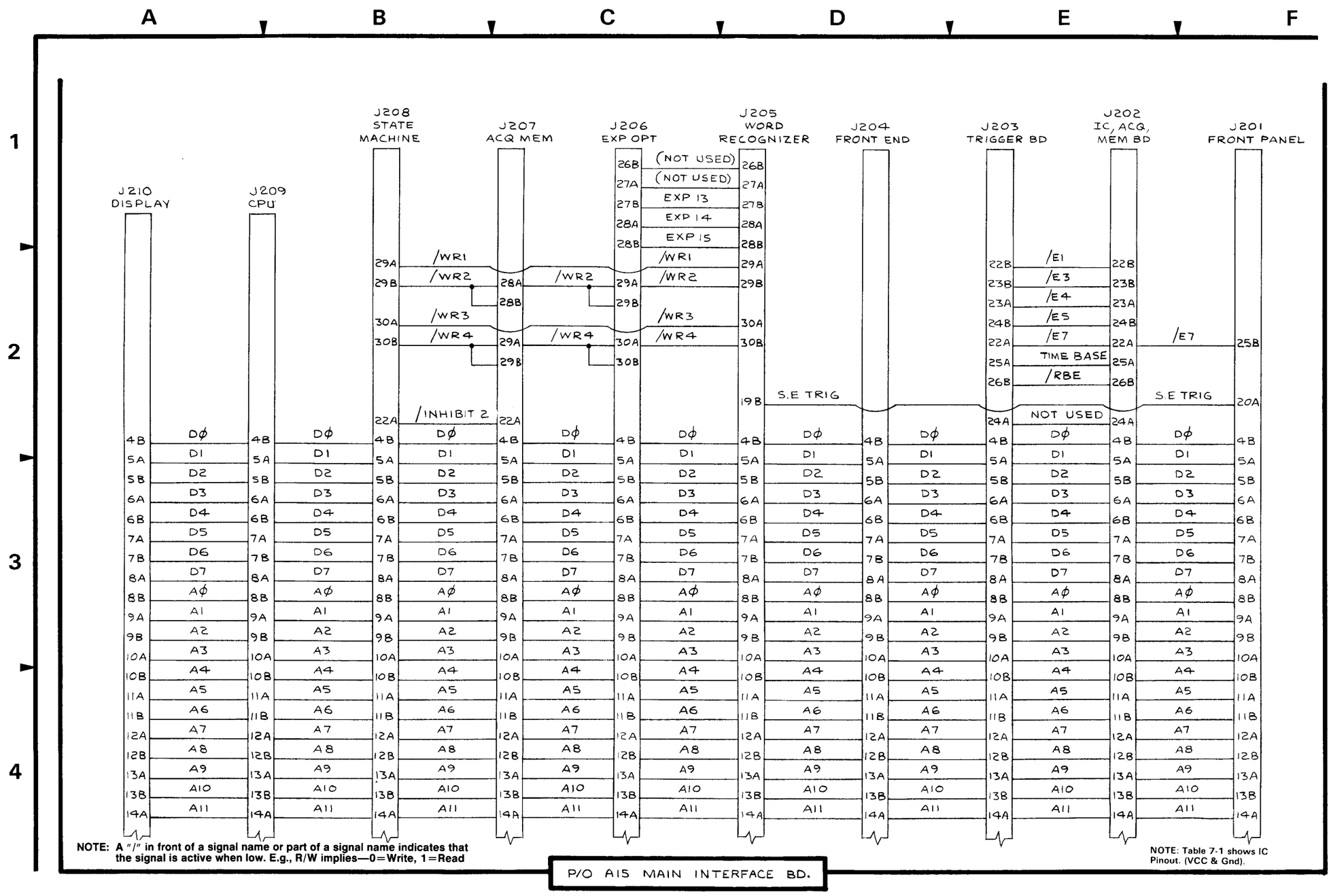
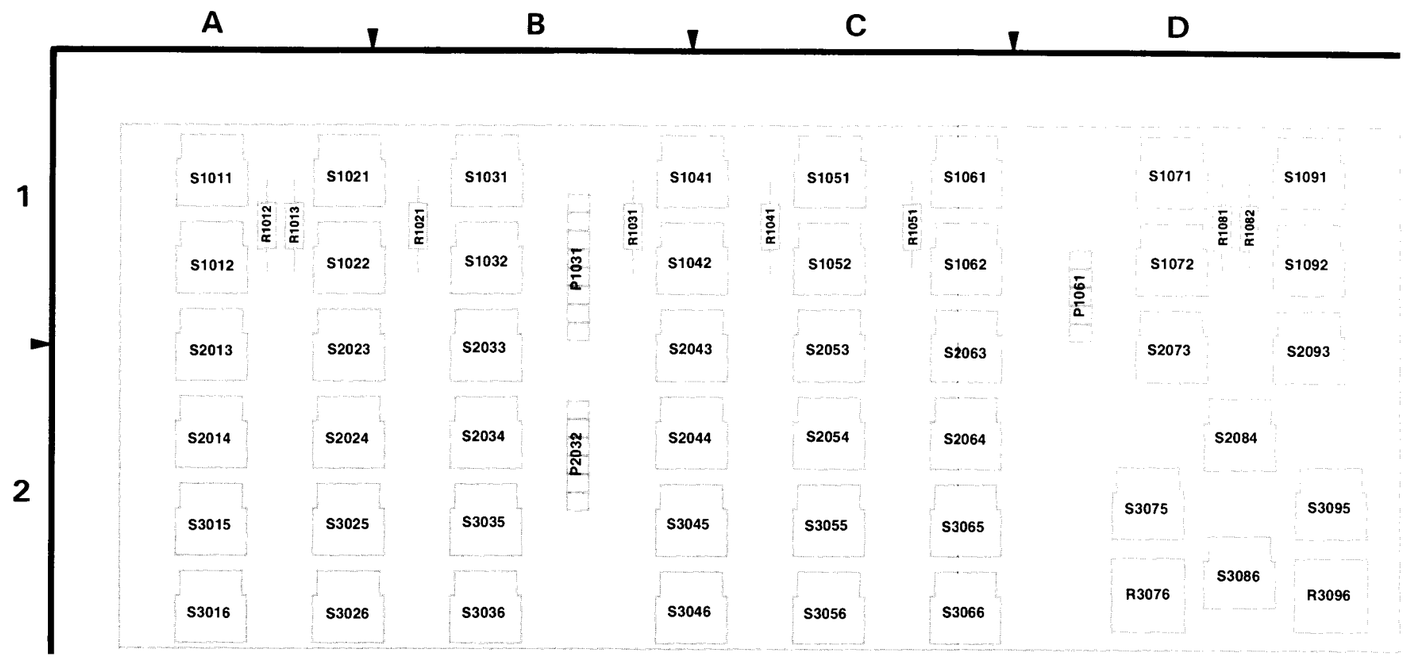
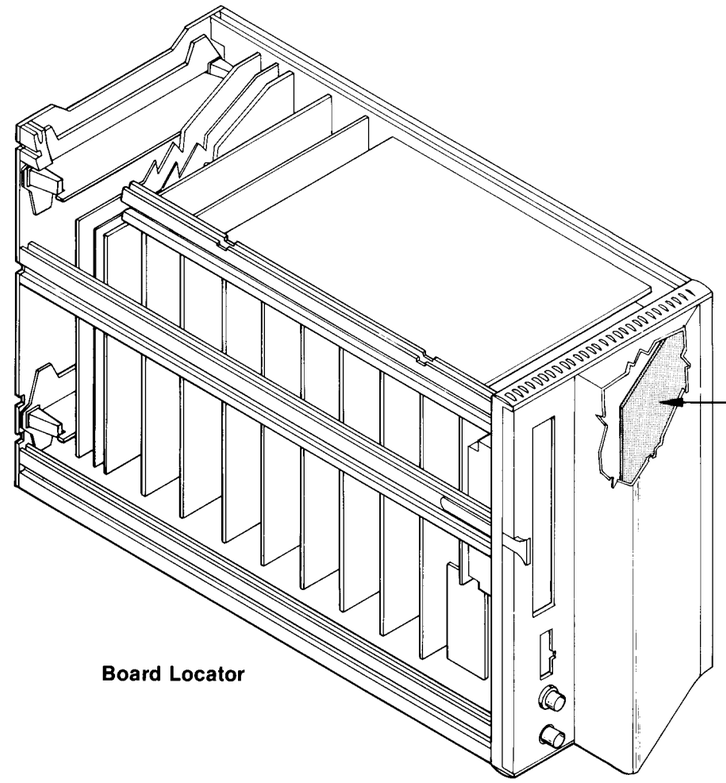
Figure 7-15C. A15 Main interface board component locations.

A15 MAIN INTERFACE BOARD


A
B
C
D
E
F
1
2
3
4
J210 DISPLAY
J209 CPU
J208 STATE MACHINE
J207 ACQ MEM
J206 EXP OPT
J205 WORD RECOGNIZER
J204 FRONT END
J203 TRIGGER BD
J202 IC, ACQ, MEM BD
J201 FRONT PANEL
(NOT USED)
EXP 13
EXP 14
EXP 15
/WR1
/WR2
/WR3
/WR4
/INHIBIT 2
S.E TRIG
/E1
/E3
/E4
/E5
/E7
TIME BASE
/RBE
NOT USED
Dϕ
D1
D2
D3
D4
D5
D6
D7
Aϕ
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read
NOTE: Table 7-1 shows IC Pinout. (VCC & Gnd).
P/O A15 MAIN INTERFACE BD.



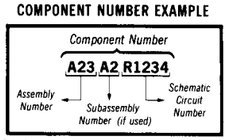
2919-214



Board Locator

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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Figure 7-16. A16 Keyboard board component locations.

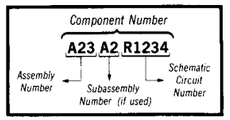
A17 P6451 DIAGRAM 17

ASSEMBLY A17		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1	B1	A1
J2	B2	A1
J3	A1	A1

A. P6451 INTERFACE 17

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

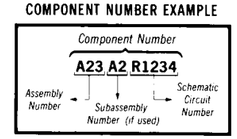
A16 KEYBOARD DIAGRAM 16

ASSEMBLY A16		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P1031	F2	B1
P1061	A1	D1
P1061	E1	D1
P1061	F1	D1
P2032	A2	B2
R1012	A1	A1
R1013	B1	A1
R1021	B1	B1
R1031	C1	B1
R1041	C1	C1
R1051	D1	C1
R1081	D1	D1
R1082	E1	D1
R3076	E1	D2
R3096	F1	D2
S1011	A2	A1
S1012	A2	A1
S1021	B2	A1
S1022	B2	A1
S1031	B2	B1
S1032	B2	B1
S1041	C2	B1
S1042	C2	B1
S1051	C2	C1
S1052	C2	C1
S1061	D2	C1
S1062	D2	C1
S1071	D2	D1
S1091	E2	D1
S2013	A3	A2
S2014	A3	A2
S2023	B3	A2
S2024	B3	A2
S2033	B3	B2
S2034	B3	B2
S2043	C3	B2
S2044	C3	B2
S2053	C3	C2
S2054	C3	C2
S2063	D3	C2
S2064	D3	C2
S2073	D3	D2
S2084	D3	D2
S2093	E2	D2
S3016	A4	A2
S3035	B3	B2
S3036	B4	B2
S3045	C3	B2
S3046	C4	B2
S3055	C3	C2
S3056	C4	C2
S3065	D3	C2
S3066	D4	C2
S3075	D3	D2
S3086	E4	D2
S3095	E3	D2

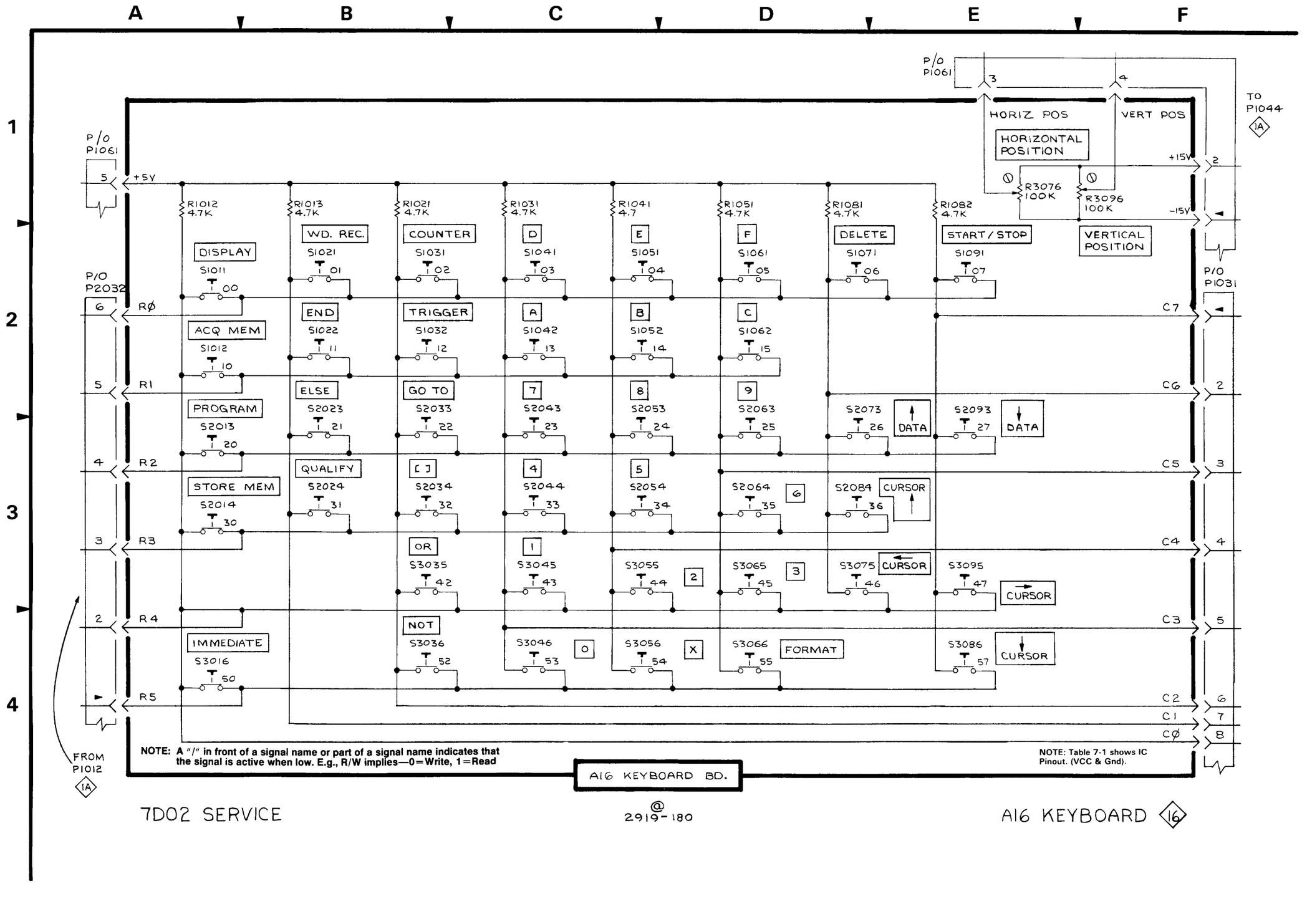
A16 KEYBOARD 16

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



7D02 SERVICE

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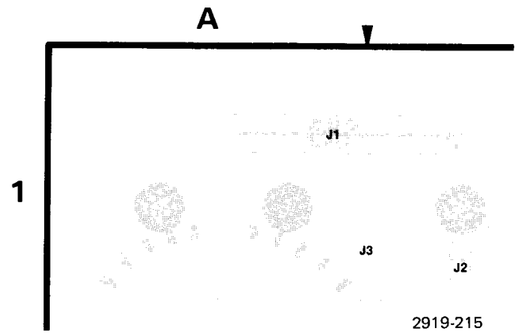
A16 KEYBOARD 16



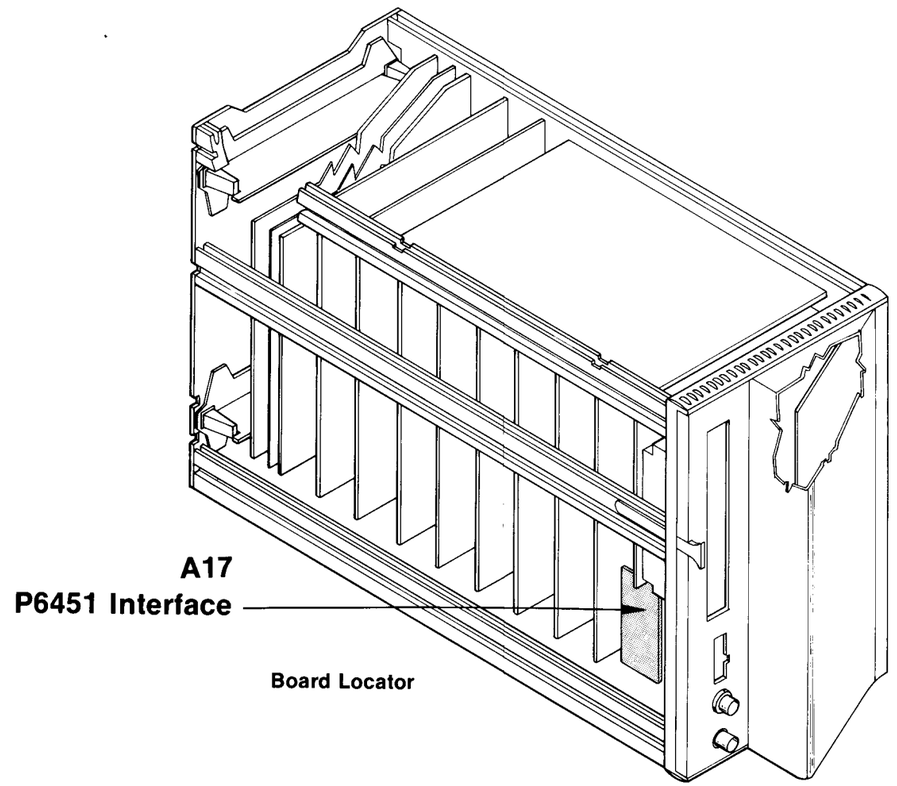
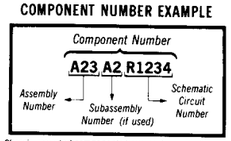


Figure 7-17. A17 P6451 Interface board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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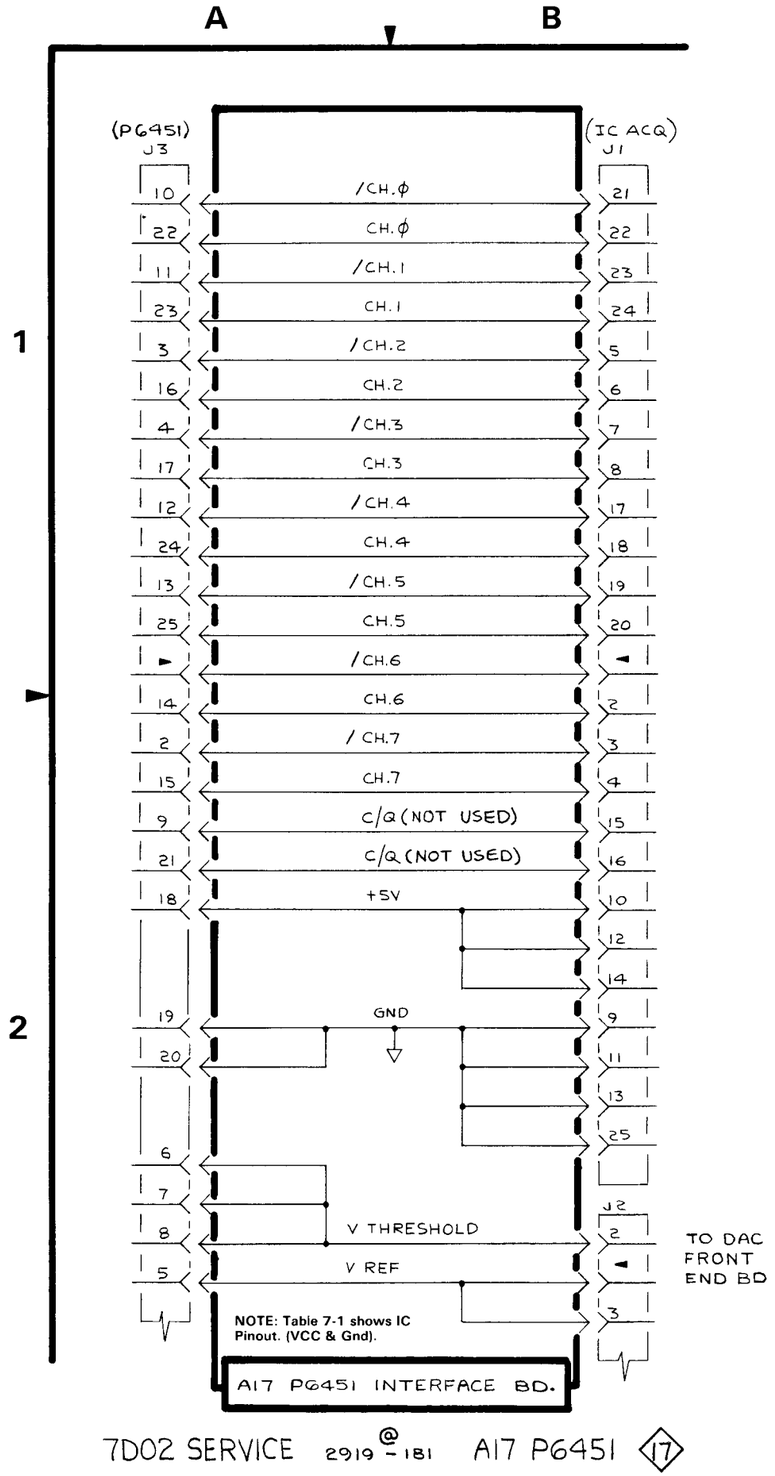


NOTE: A "/" in front of a signal name or part of a signal name indicates that the signal is active when low. E.g., R/W implies—0=Write, 1=Read

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000FU	WRIGHT ENGINEERED PLASTICS	10350 OLD REDWOOD HIGHWAY	WINDSOR, CA 95492
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
02107	SPARTA MANUFACTURING COMPANY	ROUTE NO. 2, BOX 128	DOVER, OH 44622
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
13511	AMPHENOL CARDRE DIV., BUNKER RAMO CORP.		LOS GATOS, CA 95030
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
22599	ESNA, DIV. OF AMERACE CORPORATION	16150 STAGG STREET	VAN NUYS, CA 91409
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
52905	SIMPLEX MFG. COMPANY	5224 NE 42ND AVENUE	PORTLAND, OREGON 97218
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
74921	ITEN FIBRE CO.,	4001 BENEFIT AVE., P O BOX 9	ASHTABULA, OH 44004
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83294	ARROW FASTENER CO., INC.	271 MAYHILL ST.	SADDLE BROOK, NJ 07662
83309	ELECTRICAL SPECIALITY CO., SUBSIDIARY OF BELDEN CORP.	213 E. HARRIS AVE. SOUTH	SAN FRANCISCO, CA 94080
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	333-2589-00			1		PANEL,FRONT:UPPER	80009	333-2589-00
						(ATTACHING PARTS)		
-2	211-0285-00			4		SCREW,CAP:2-56 X 0.25,BUTTON HD,SST	83294	OBD
-3	210-0001-00			4		WASHER,LOCK:INTL,0.092 ID X 0.18"OD,STL	78189	1202-00-00-0541C
						- - - * - - -		
-4	358-0628-00			2		BUSHING,SLEEVE:0.190 ID X 0.175 THK	80009	358-0628-00
-5	386-4250-00			1		SUBPANEL,FRONT:UPPER	80009	386-4250-00
						(ATTACHING PARTS)		
-6	211-0087-01			9		SCREW,MACHINE:2-56 X 0.188,FLH 82 DEG,STL	83385	OBD
-7	211-0105-00			2		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-8	361-0993-00			8		SPACER,POST:0.275,2-56 THD THRU	80009	361-0993-00
						(ATTACHING PARTS)		
-9	211-0022-00			8		SCREW,MACHINE:2-56 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-10	366-1770-00			18		PUSH BUTTON:GY,0.225 X 0.4 X 0.17	000FU	OBD
	366-1770-02			1		PUSH BUTTON:GRAY,1	000FU	OBD
	366-1770-03			1		PUSH BUTTON:GRAY,2	000FU	OBD
	366-1770-04			1		PUSH BUTTON:GRAY,3	000FU	OBD
	366-1770-05			1		PUSH BUTTON:GRAY,4	000FU	OBD
	366-1770-06			1		PUSH BUTTON:GRAY,5	000FU	OBD
	366-1770-07			1		PUSH BUTTON:GRAY,6	000FU	OBD
	366-1770-08			1		PUSH BUTTON:GRAY,7	000FU	OBD
	366-1770-09			1		PUSH BUTTON:GRAY,8	000FU	OBD
	366-1770-10			1		PUSH BUTTON:GRAY,9	000FU	OBD
	366-1770-11			1		PUSH BUTTON:GRAY,O	000FU	OBD
	366-1770-12			1		PUSH BUTTON:GRAY,A	000FU	OBD
	366-1770-13			1		PUSH BUTTON:GRAY,B	000FU	OBD
	366-1770-14			1		PUSH BUTTON:GRAY,C	000FU	OBD
	366-1770-15			1		PUSH BUTTON:GRAY,D	000FU	OBD
	366-1770-16			1		PUSH BUTTON:GRAY,E	000FU	OBD
	366-1770-17			1		PUSH BUTTON:GRAY,F	000FU	OBD
	366-1770-18			1		PUSH BUTTON:GRAY,X	000FU	OBD
	366-1784-19			4		PUSH BUTTON:TV GRAY,TRIANGLE SILVER	000FU	OBD
	366-1784-20			2		PUSH BUTTON:TV GRAY,TRIANGLE SILVER	000FU	OBD
-11	----- -----			1		CKT BOARD ASSY:KEYBOARD(SEE A16 REPL)		
-12	131-0608-00			19		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-13	----- -----			41		. SWITCH,PUSHBUTTON:(SEE A16S1011,S1012,S1021,		
	----- -----			-		. S1022,S1031,S1032,S1041,S1042,S1051,S1052		
	----- -----			-		. S1061,S1062,S1071,S1091,S2013,S2014,S2023,		
	----- -----			-		. S2024,S2033,S2034,S2043,S2044,S2053,S2054,		
	----- -----			-		. S2063,S2064,S2073,S2084,S2093,S3016,S3035,		
	----- -----			-		. S3036,S3045,S3046,S3055,S2056,S3065,S3066,		
	----- -----			-		. S3075,S3086,S3095 REPL)		
-14	333-2590-00			1		PANEL,FRONT:	80009	333-2590-00
						(ATTACHING PARTS)		
-15	211-0285-00			4		SCREW,CAP:2-56 X 0.25,BUTTON HD,SST	83294	OBD
-16	210-0001-00			4		WASHER,LOCK:INTL,0.092 ID X 0.18"OD,STL	78189	1202-00-00-0541C
						- - - * - - -		
-17	131-0679-02			1		CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
						(ATTACHING PARTS)		
-18	220-0497-00			1		NUT,PLAIN,HEX.:0.5-28 X 0.562 INCH HEX,BRS	73743	OBD
-19	210-1039-00			1		WASHER,LOCK:INT,0.521 ID X 0.625 INCH OD	24931	OBD
						- - - * - - -		
-20	131-0955-00			1		CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
-21	210-0255-00			1		TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	80009	210-0255-00
-22	386-4249-00			1		SUBPANEL,FRONT:LOWER	80009	386-4249-00
						(ATTACHING PARTS)		
-23	211-0105-00			3		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-24	----- -----			1		CKT BOARD ASSY:P6451 INTERFACE(SEE A17 REPL)		
						(ATTACHING PARTS)		
-25	211-0087-01			4		SCREW,MACHINE:2-56 X 0.188,FLH 82 DEG,STL	83385	OBD
-26	129-0546-00			4		POST,ELEC-MECH:0.475" LONG X0.125 HEX	80009	129-0546-00
-27	211-0022-00			4		SCREW,MACHINE:2-56 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	----- -----			-		CKT BOARD ASSY INCLUDES:		
1-28	131-0608-00			28		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-29	131-1897-00			1		. CONNECTOR,RCPT,:25 MALE CONTACT	71785	2805125002
						(ATTACHING PARTS)		
-30	211-0022-00			2		. SCREW,MACHINE:2-56 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-31	386-4224-00			1		. PLATE,CONN MTG:ALUMINUM	80009	386-4224-00
						(ATTACHING PARTS)		
-32	211-0007-00			2		. SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
-33	210-0259-00	B010100	B020944X	1		. TERMINAL,LUG:0.099"ID INT TOOTH,SE	80009	210-0259-00
						- - - * - - -		
-34	129-0285-00			2		. POST,ELEC-MECH:0.281 L X 0.188 HEX BRS	80009	129-0285-00
						(ATTACHING PARTS)		
-35	211-0007-00			2		. SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-36	175-2853-00			1		CA ASSY,SP,ELEC:5,26 AWG,3.0 L	80009	175-2853-00
-37	348-0235-00			2		SHLD GSKT,ELEC:4.734 INCH LONG	80009	348-0235-00
-38	386-4098-01			1		SUBPANEL,FRONT:FINISHED	80009	386-4098-01
-39	----- -----			1		CKT BOARD ASSY:MAIN INTERFACE(SEE A15 REPL)		
						(ATTACHING PARTS)		
-40	211-0661-00			7		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-41	131-0608-00			28		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-42	131-2451-00			11		. CONN,RCPT,ELEC:EDGECARD,15/30 CONT,0.1 SP	05574	000264-0064
-43	220-0547-06			7		NUT BLOCK:0.38 X 0.26 X0.282	80009	220-0547-06
						(ATTACHING PARTS)		
-44	211-0105-00			7		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-45	426-1603-00			2		FR SECT,PLUG-IN:TOP & BOTTOM RIGHT	80009	426-1603-00
						(ATTACHING PARTS)		
-46	213-0793-00			8		SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FIL	93907	OBD
						- - - * - - -		
-47	361-0326-00			1		SPACER,SLEEVE:0.18 ID X 0.25 OD X 0.10"L	80009	361-0326-00
-48	366-1058-80			1		KNOB:GRAY,7D02	80009	366-1058-80
-49	214-1095-00			1		PIN,SPG,SPLIT:0.094 OD X 0.187 INCH LONG	22599	52-022-094-0187
-50	105-0076-00			1		REL BAR,LATCH:PLUG-IN UNIT	80009	105-0076-00
-51	214-1280-00			1		SPRING,HLCPS:0.14 OD X 1.126"L,0.16"DIA W	80009	214-1280-00
-52	214-1054-00			1		SPRING,FLAT:0.825 X 0.322,SST	80009	214-1054-00
-53	105-0075-00			1		BOLT,LATCH:7A & 7B SER PL-IN	80009	105-0075-00
-54	426-1650-00	B010100	B021864	1		FR SECT,PLUG-IN:CENTER BOTTOM	80009	426-1650-00
	426-1650-01	B021865		1		FR SECT,PLUG-IN:CENTER BOTTOM	80009	426-1650-01
						(ATTACHING PARTS)		
-55	213-0793-00			4		SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FIL	93907	OBD
						- - - * - - -		
-56	214-2976-00			1		STAB,CIRCUIT BD:ALUMINUM	80009	214-2976-00
						(ATTACHING PARTS)		
-57	211-0007-00			2		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-58	214-1061-00			1		SPRING,GROUND:FLAT	80009	214-1061-00
-59	214-3121-00			1		STAB,CIRCUIT BD:ALUMINUM	80009	214-3121-00
						(ATTACHING PARTS)		
-60	211-0007-00			2		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-61	220-0547-06			5		NUT BLOCK:0.38 X 0.26 X0.282	80009	220-0547-06
						(ATTACHING PARTS)		
-62	211-0105-00			5		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-63	426-1602-00			2		FR SECT,PLUG-IN:TOP LEFT	80009	426-1602-00
						(ATTACHING PARTS)		
-64	213-0793-00			8		SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FIL	93907	OBD
						- - - * - - -		
-65	220-0547-06			2		NUT BLOCK:0.38 X 0.26 X0.282	80009	220-0547-06
						(ATTACHING PARTS)		
-66	211-0105-00			2		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-67	426-1601-00			1		FR SECT,PLUG-IN:BOTTOM LEFT	80009	426-1601-00
						(ATTACHING PARTS)		
-68	213-0793-00			4		SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FIL	93907	OBD
						- - - * - - -		
-69	----- -----			1		CKT BOARD ASSY:PROBE INTERFACE(SEE A14 REPL)		
						(ATTACHING PARTS)		
-70	211-0008-00			3		SCREW,MACHINE:4-40 X 0.250,PNH,STL,CD PL	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-71	131-2451-00			2		. CONN,RCPT,ELEC:EDGECARD,15/30 CONT,0.1 SP	05574	000264-0064
-72	131-2452-00			4		. CONN,RCPT,ELEC:EDGECARD,30/60 CONT,0.1 SP	05574	00264-0085
-73	----- -----			1		. CONN,RCPT,ELEC:(SEE A14J101 REPL)		
	337-1399-09			2		SHIELD,ELEC:PLUG-IN SIDE	80009	337-1399-09
-74	342-0470-00			2		. INSULATOR,PLATE:CONNECTOR,POLYESTER	80009	342-0470-00
-75	337-1064-11			2		. SHIELD,ELEC:PLUG-IN SIDE	80009	337-1064-11
-76	337-2721-00			1		SHIELD,ELEC:CIRCUIT BOARD	80009	337-2721-00
						(ATTACHING PARTS)		
-77	211-0661-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	83385	OBD
						- - - * - - -		
-78	----- -----			1		TRANSISTOR:(SEE Q1035 REPL)		
						(ATTACHING PARTS)		
-79	211-0097-00			1		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-80	210-1171-00			1		WSHR,SHOULDERED:0.116 ID X 0.138 INCH OD	52905	A7148516P2
						- - - * - - -		
-81	342-0322-00			1		INSULATOR,FILM:TRANSISTOR	80009	342-0322-00
-82	----- -----			1		TRANSISTOR:(SEE Q1015 REPL)		
						(ATTACHING PARTS)		
-83	211-0097-00			1		SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
-84	210-1171-00			1		WSHR,SHOULDERED:0.116 ID X 0.138 INCH OD	52905	A7148516P2
						- - - * - - -		
-85	342-0322-00			1		INSULATOR,FILM:TRANSISTOR	80009	342-0322-00
-86	----- -----			2		SEMICOND,DEVICE:(SEE CR2013,CR5013 REPL)		
						(ATTACHING PARTS)		
-87	220-0410-00			2		NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD
-88	210-0805-00			2		WASHER,FLAT:0.204 ID X 0.438 INCH OD,STL	12327	OBD
-89	210-0813-00			2		WSHR,SHOULDERED:# 10 FIBER	74921	OBD
-90	210-0910-00			2		WASHER,NONMETAL:0.188 ID X 0.313" OD,TEFLON	02107	OBD
-91	210-0909-00			2		WASHER,NONMETAL:0.196 ID X 0.625" OD,MICA	83309	OBD
-92	210-0224-00			2		TERMINAL,LUG:0.20 ID X 0.344 OD,SE,BRS	86928	A373-148-1
	210-0457-00			2		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	OBD
						- - - * - - -		
-93	214-2857-00			1		HEAT SINK,ELEC:(2)TO-220 & (2) DIODES,AL	80009	214-2857-00
						(ATTACHING PARTS)		
-94	212-0518-00			1		SCREW,MACHINE:10-32 X 0.312,PNH,STL,CD PL	83385	OBD
-95	211-0559-00			2		SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-96	385-0154-00			2		SPACER,POST:1.296 L W/6-32 THD EA END,AL	80009	385-0154-00
						(ATTACHING PARTS)		
-97	211-0658-00			2		SCR,ASSEM WSHR:6-32 X 0.312 L,PNH,STL	78189	OBD
						- - - * - - -		
-98	----- -----			1		CKT BOARD ASSY:POWER SUPPLY(SEE A11 REPL)		
-99	----- -----			1		. COIL,RF:(SEE L5034 REPL)		
						(ATTACHING PARTS)		
-100	211-0003-00			1		. SCREW,MACHINE:2-56 X 0.875 INCH,PNH,STL	83385	OBD
-101	210-0405-00			1		. NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	12157-50
-102	210-0001-00			1		. WASHER,LOCK:INTL,0.092 ID X 0.18"OD,STL	78189	1202-00-00-0541C
-103	210-0850-00			1		. WASHER,FLAT:0.093 ID X 0.281 INCH OD	12327	OBD
						- - - * - - -		
-104	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-105	136-0269-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-106	136-0760-00	B010100	B021099X	2		. SKT,PL-IN ELEK:TRANSISTOR,3 CONTACT		
-107	----- -----			1		CKT BOARD ASSY:HORIZONTAL INTFC(SEE A13 REPL)		
-108	131-0608-00			18		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-109	----- -----			1		CKT BOARD ASSY:VERTICAL INTERFACE(SEE A12 REPL)		
-110	131-0608-00			10		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-111	----- -----			4		. TERM,TEST POINT:(SEE A12TP1,TP2,TP3,TP4 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-112	351-0217-00			2		GUIDE,CKT CARD:PLASTIC	80009	351-0217-00
						(ATTACHING PARTS)		
-113	211-0507-00			8		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
-114	220-0557-00			8		NUT,SLEEVE:6-32 X 0.204 OD X 0.118 L BRS	80009	220-0557-00
						- - - * - - -		
-115	175-2638-00			1		CA ASSY,SP,ELEC:6,26 AWG,10.0L	80009	175-2638-00
-116	198-3434-00			1		WIRE SET,ELEC:	80009	198-3434-00
-117	175-2849-00			1		CA ASSY,SP,ELEC:10,26 AWG,3.0L	80009	175-2849-00
-118	198-4454-00			1		WIRE SET,ELEC:	80009	198-4454-00
-119	343-0298-00			1		CLAMP,LOOP:PLASTIC,W/ADHESIVE BACK	95987	HPC25
-120	333-2522-00			1		PANEL,REAR:	80009	333-2522-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	175-3226-00			1		CA ASSY,SP,ELEC:3,26 AWG,6.0 L	80009	175-3226-00
-2	175-2774-00			1		CA ASSY,SP,ELEC:5,26 AWG,3.0L	80009	175-2774-00
-3	175-2850-00			1		CA ASSY,SP,ELEC:8,26 AWG,3.5 L	80009	175-2850-00
	175-2851-00			1		CA ASSY,SP,ELEC:6,26 AWG,3.5 L	80009	175-2851-00
-4	----- -----			1		CKT BOARD ASSY:FRONT PANEL(SEE A01 REPL)		
						(ATTACHING PARTS)		
-5	211-0105-00			1		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH STL	83385	OBD
						- - - * - - -		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-6	351-0624-00			1		. GUIDE,PROBE:POLYCARBONATE	80009	351-0624-00
						(ATTACHING PARTS)		
-7	211-0121-00			1		. SCR,ASSEM WSHR:4-40 X 0.438 INCH,PNH BRS	83385	OBD
-8	210-1348-00			1		. WASHER,FLAT:0.115 ID.X 0.008 THK	80009	210-1348-00
-9	211-0661-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	83385	OBD
-10	220-0547-06			2		. NUT BLOCK:0.38 X 0.26 X0.282	80009	220-0547-06
						- - - * - - -		
-11	131-0608-00			30		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-12	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-13	131-2416-00			1		. CONN,RCPT,ELEC:EDGECARD,32/34 CONT	05574	000201-5422
-14	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-15	----- -----			1		. TERM,TEST POINT:(SEE A01TP1053 REPL)		
-16	----- -----			1		CKT BOARD ASSY:IC ACQUISTION(SEE A02 REPL)		
-17	131-0608-00			9		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-18	131-1857-00			1		. TERM. SET,PIN:36/0.025 SQ PIN,ON 0.1 CTRS	22526	65500136
-19	136-0260-02			8		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-20	136-0621-00			4		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
-21	----- -----			1		CKT BOARD ASSY:TRIGGER(SEE A03 REPL)		
-22	131-0608-00			25		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-23	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-24	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-25	----- -----			1		CKT BOARD ASSY:FRONT END(SEE A04 REPL)		
-26	131-0608-00	B010100	B020599	41		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	131-0608-00	B020600		38		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	136-0252-07			14		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-28	136-0269-02	B010100	B020599	2		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
	136-0269-02	B020600		1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-29	136-0634-00			6		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-30	----- -----			1		CKT BOARD ASSY:WORD RECOGNIZER(SEE A05 REPL)		
-31	131-0608-00			32		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-32	136-0269-02			2		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-33	136-0621-00			4		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
-34	136-0634-00			3		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-35	----- -----			1		CKT BOARD ASSY:EXPANSION OPT(SEE A06 REPL)		
-36	131-0608-00			46		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-37	136-0621-00			6		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
-38	136-0634-00			2		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-39	----- -----			1		CKT BOARD ASSY:ACQUISITION MEM(SEE A07 REPL)		
-40	131-0608-00			54		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-41	136-0269-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-42	136-0621-00			7		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
-43	----- -----			1		CKT BOARD ASSY:STATE MACHINE(SEE A08 REPL)		
-44	131-0608-00			12		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-45	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-46	136-0621-00	B010100	B021209	2		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
	136-0621-00	B021210		4		. SOCKET,PLUG-IN:22 CONTACT	73803	CS9002-22
	136-0634-00	XB021210		1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-47	----- -----			1		. TERM,TEST POINT:(SEE A08TP11 REPL)		
-48	----- -----			1		CKT BOARD ASSY:CPU(SEE A09 REPL)		
-49	131-0608-00			6		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-50	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-51	131-2471-00			1		. CONN,RCPT,ELEC:CKT BOARD,6 CONTACT,FEM	22526	65780-006
-52	136-0578-00			6		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-53	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-54	136-0634-00			2		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-55	136-0670-00			16		. SKT,PL-IN ELEK:MICROCKT,18 PIN,LOW PROFILE	73803	CS9002-18
-56	----- -----			4		. TERM,TEST POINT:(SEE A09TP41,TP42,TP43 AND		
	----- -----			-		. TP49 REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-57	----- -----			1		CKT BOARD ASSY:DISPLAY(SEE A10 REPL)		
-58	136-0234-00			2		. SOCKET,PIN TERM:0.088 OD X 0.247 INCH L	00779	380598-1
-59	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-60	136-0670-00			2		. SKT,PL-IN ELEK:MICROCKT,18 PIN,LOW PROFILE	73803	CS9002-18
-61	346-0032-00			1		. STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2859-75-4

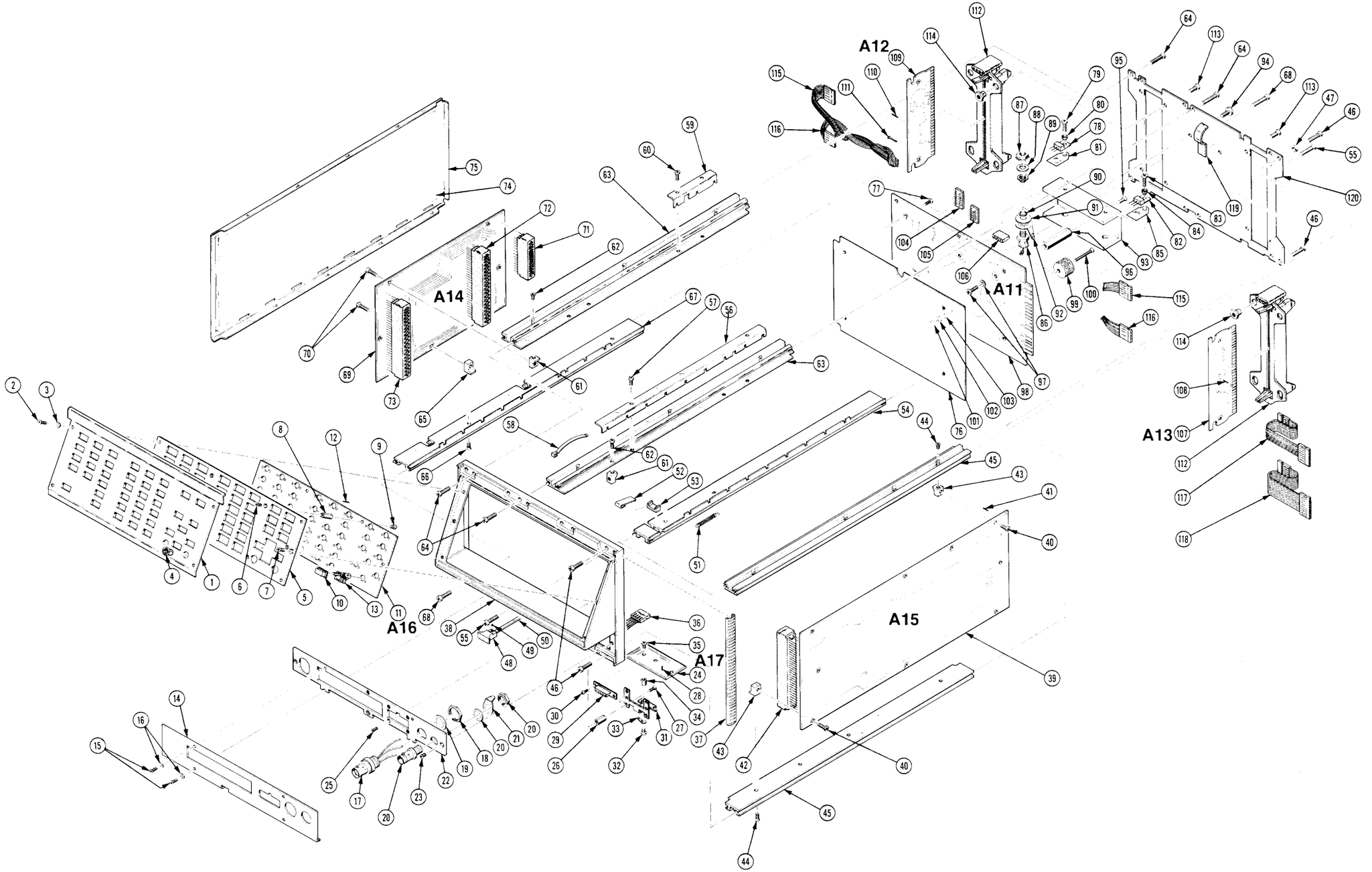
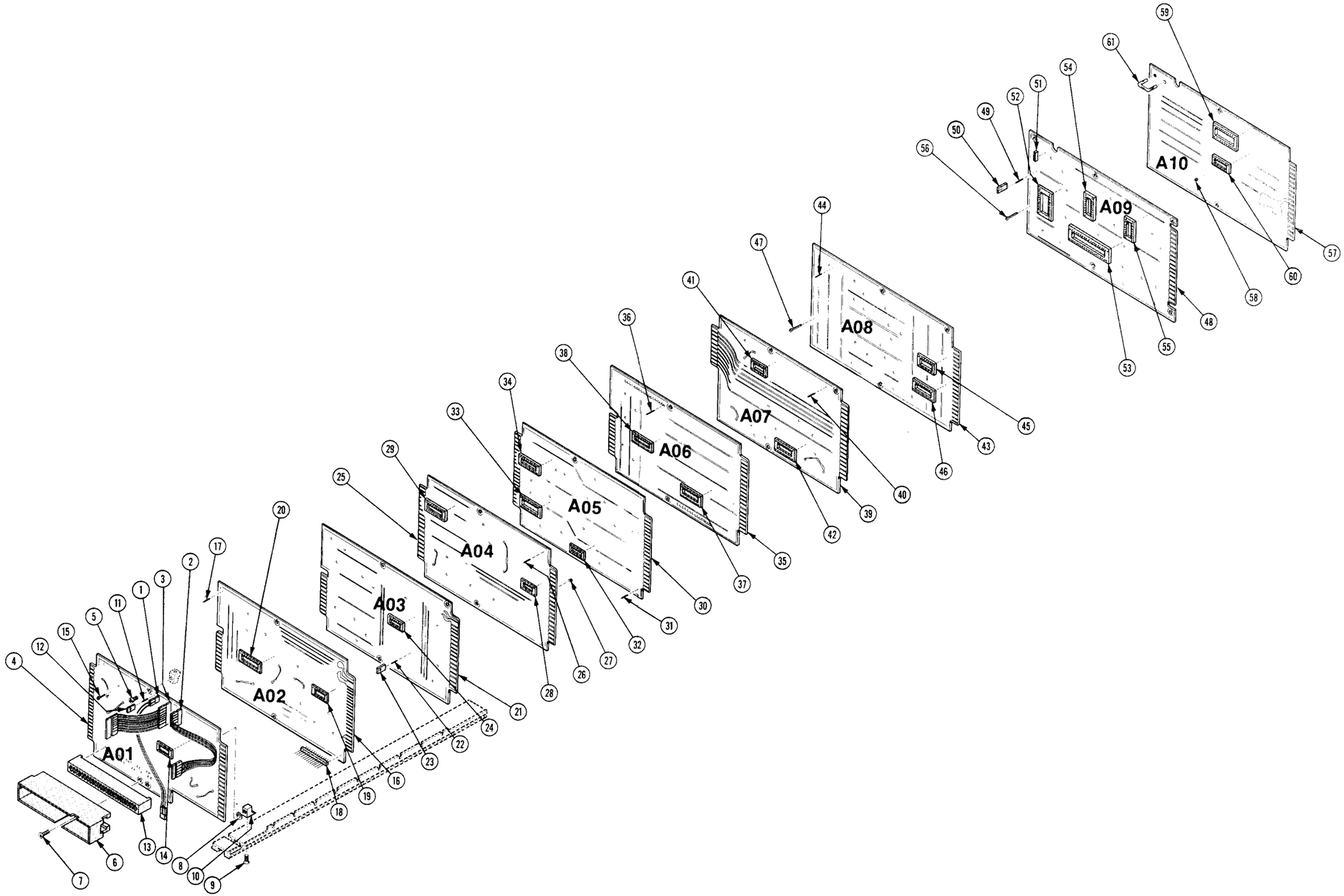

A12
A14
A11
A13
A16
A17
A15

FIG. 2 CIRCUIT BOARDS



7D02

@

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	010-6451-03			1		PROBE,DATA ACQ: MULTI LEAD,W/ACCESS	80009	010-6451-03
	070-2915-00			1		MANUAL,TECH:OPERATORS,REFERENCE	80009	070-2915-00
	070-2918-00			1		MANUAL,TECH:OPERATORS	80009	070-2918-00
	070-2919-00			1		MANUAL,TECH:SERVICE	80009	070-2919-00
	070-3622-00			1		SHEET,TECHNICAL:INSTR 7D02F01	80009	070-3622-00
	070-3623-00			1		SHEET,TECHNICAL:INSTR 7D02F03	80009	070-3623-00
	070-3420-00			1		MANUAL,TECH:OPERATORS,LEARNING GUIDE	80009	070-3420-00

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MANUAL CHANGE INFORMATION

Date: 2-22-82 Change Reference: C1/282

Product: 7D02 LOGIC ANALYZER Service Manual Manual Part No.: 070-2919-00

DESCRIPTION

TEXT CORRECTIONS

SECTION 2 THEORY OF OPERATION

page 2-136 2nd paragraph last sentence

CHANGE TO:

The most significant bit (MSB) of the 8-bit RAM location indicates whether the character is to be displayed as normal or inverse video.

page 2-152 last paragraph last sentence

CHANGE TO:

The output signal is approximately 1/2 V p-p, measured across the outputs.

SECTION 3 PERFORMANCE CHECK AND ADJUSTMENT

page 3-11 2nd row, under Performance Requirements

CHANGE TO:

18 ns @ BNC max

16 ns @BNC max

2nd row, under Supplemental Information

CHANGE TO:

DESCRIPTION

P6105 adds 12 ns to setup time,
subtracts 12 ns from hold time
page 3-15 Table 3-2 under Probes (2)

ADD:

Probe X1 P6101 Internal clock check

page 3-17 Table 3-2 last item

DELETE:
Resistor, 2-kOhm

Bottom of page

CHANGE TO:

Test Fixtures

Refer to Fig. 3-1 and assemble two test fixtures as follows; loosen the binding post screws on a BNC to binding post adapter, insert a separate piece of 22-gauge wire through each post, tighten the screws, and bend the wires in opposite directions. (For most effective use, insert the wires so that all of the excess length is to one side.)

ADD:

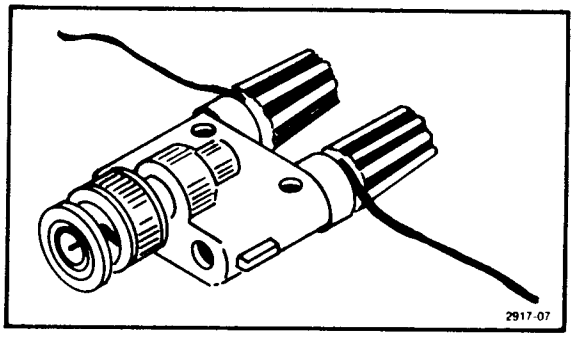

Fig. 3-1. An Assembled Text Fixture.

Increment remaining figures and figure references by 1.

DESCRIPTION

Page 3-18 top of page

DELETE:
top two lines

Item d.

CHANGE TO:
d. Connect the Data, Address, Control, Clock leads, and P6451 timing probes on the Self-Test Stimulus pins as indicated in Table 3-3 and shown in Fig.3-2.

Bottom of page

DELETE:

Note

Page 3-19 Table 3-3

CHANGE TO:

DESCRIPTION

Table 3-3

SELF TEST STIMULUS CONNECTION

PM101 Individual Test Leads					P6451
Connector	Data	Address	Address	Control	Timing
T2	D0 (blk)	A0 (blk)			Black
T3	D1 (brn)	A1 (brn)			Brown
T4	D2 (red)	A2 (red)			Red
T5	D3 (orn)	A3 (orn)			Orange
T6	D4 (yel)	A4 (yel)			Yellow
T7	D5 (grn)	A5 (grn)			Green
T8	D6 (blu)	A6 (blu)			Blue
T9	D7 (v)	A7 (v)			Violet
T10	D8 (gry)	A8 (gry)	A16 (blu)	C0 (blk)	
T11	D9 (w)	A9 (w)	A17 (v)	C1 (brn)	
T12	D10 (blk)	A10 (blk)	A18 (gry)	C2 (red)	
T13	D11 (brn)	A11 (brn)	A19 (w)	C3 (orn)	
T14	D12 (red)	A12 (red)	A20 (blk)	C4 (yel)	
T15	D13 (orn)	A13 (orn)	A21 (brn)	C5 (grn)	
T16	D14 (yel)	A14 (yel)	A22 (red)		
T17	D15 (grn)	A15 (grn)	A23 (orn)		
T18				C6 (blu)	
T19				C7 (v)	
T20				C8 (gry)	
T21				C9 (w)	

SINGLE LEADS		
CLK	Grey	
T HALT	Red	
GND	Both Blacks	White

Page 3-21 top of page items 5. and 6.

CHANGE TO:

DESCRIPTION

5. Install two Extenders, one in vertical and one in horizontal mainframe

Bottom of page items 1.,2.,3., and 4.

CHANGE TO:

1. Perform PM101 Personality Module Self Test Connention Procedure, if not already done.
2. Install 7D02 in appropriate 7000-Series Mainframes, if plug-in extenders are not being used.
3. Connect PM101 General Purpose Personality Module to data input connector at lower left front of 7D02. Insure 7D02 power is off.
4. (option 1 only) ....etc

Bottom of page

ADD:

NOTE

The following performance checks were made with OPT.3 installed. When performing checks without OPT.3, the eight most significant bits in the Address and Data fields are omitted.

page 3-22 1st sub paragraph under item 5

ADD:

See Fig. 3-3

page 3-23 item 12

CHANGE TO:

DESCRIPTION

12. Press 0 key to select "TEST ALL". "PLEASE CONNECT SELF TEST STIMULUS" will be displayed as a reminder that PM101 leads should be commected to PM101 self test before continuing with tests.

Above item 14

ADD:

NOTE

Test will repeat in a continous loop if looping is enabled.

Item 14

CHANGE TO:

14. Press "X" to return to menu.

Page 3-24 item 1.

ADD:
(OPT.1 ONLY)

item 1b.

ADD:
(2*10ns)

item 1d.

ADD:
(040ns)

DESCRIPTION

Page 3-28 item 1

ADD:
(Power Supply Board 670-5982-00)

Bottom of page

ADD:
1A. Adjust +5-Volt Power Supply (Power Supply Board 670-5982-01)

Equipment required:

DM 501A
Screwdriver
Extender (P/O Service Maintenance Kit, 067-0939-00

a. Perform Extender Installation Procedure and Initial Setup Procedure.
b. Set DM501A to measure DC Volts in 20-Volt range
c. Connect DM501A VOLTS test lead to J201, pin 3A.
d. Connect DM501A LOW test lead to J201, pin 1A.
c. Adjust potentiometer A11-R5065, atleft edge of power supply board, for 4.85 volts on DM501A.

Page 3-31 item p.

CHANGE TO:
p. Reset HORZ POS control for centered display.

Item q.

CHANGE TO:
q. Press START/STOP key three times (end of display test).

DESCRIPTION

page 3-32 item h.

CHANGE TO:

h. Connect P6451 ground (white) lead to above wire.

Page 3-46 item d.

CHANGE TO:

d. Disconnect data lines 15 through Ø from PM101 test socket section (see Fig. 3-2) and connect data line Ø-3 to Test Fixture 1 red terminal.

Page 3-47 item r.

CHANGE TO:

r. Move cursor to Word Recognizer Data field and enter 1's in bit positions corresponding to those four data lines connected to PG5Ø8 output. (All other remaining positions should contain X's.)

Page 3-48 Fig. 3-5 Word Recognizer Data and Address fields

CHANGE TO:

DATA=XXXXXXXXXXXX1111
AD=XXXXXXXXXXXXXXXXXXXXXXXX

Item af.

CHANGE TO:

af. Move cursor to Word Recognizer Data field and enter Ø's in bit positions in which 1's were entered in part r.

DESCRIPTION

Page 3-49 item ak.

CHANGE TO:

ak. Set NORM/COMPLEMENT back to NORM.

ADD:

al. Repeat parts d and r through aj except for s,t,and w for groups of approximately four-channels for rest of data channels, al of address channels, and six control bit channels (C0-C5).

Page 3-53 Fig. 3-7C TEST 3 COUNTER # 1 =

CHANGE TO:

TEST 3 COUNTER # 1 = 00050 1-uS

Page 3-54 Fig. 3-7D TEST 3 COUNTER # 1 =

CHANGE TO:

TEST 3 COUNTER # 1 = 00050 1-uS

Page 3-57 item a

CHANGE TO:

a. Perform parts a through o of step 5 except parts d, i and l. Instead, disconnect control lines C9 through C0 from PM101 test socket (see Fig. 3-2) and.....etc

DESCRIPTION

Page 3-62 item bs.

DELETE:

210 uS

Page 3-63 Fig. 3-8 WAIT: C7=X

CHANGE TO:
WAIT C7=1

Page 3-64 Fig. 3-9 LAST TEST = 1

CHANGE TO:
LAST TEST = 2

Page 3-67 item i. last sentence

CHANGE TO:
Adjust period variable control for 100 nS.

Page 3-70 item be.

CHANGE TO:
be. Move cursor to increment field and enter 1 to select reset command

Page 3-77 Fig 3-13 after the last ELSE DO

CHANGE TO:
COUNTER # 1 0-EVENTS
0-INCREMENT
COUNTER # 2 2-MS

DESCRIPTION

Ø-RUN
PAGE 3-78 check 11.

REPLACE WITH:

11. Check External Trigger Setup and Hold

Equipment required:

PG 5Ø8
BNC T
Probe Tip to BNC Adapter
Test Oscilloscope
Coaxial Cable (2)
5Ø-Ohm Termination
1X Probe
1ØX Probe (2)

a. PG 5Ø8 Setup

TRIGGERING	minus. FREERUN
PERIOD	EXT TRIG OR MAN
TRANSITION TIME	5nS
LEADING	X1
TRAILING	X1
MODE	DELAY
DELAY	1ØnS
DELAY VARIBLE	MIDRANGE
DURATION	1ØnS
DURATION VARIBLE	MIDRANGE
OUTPUT VOLTS	NORM PRESET (+.8 to +2V)
5Ø/1M-OHM SWITCH INSIDE	1M OHM

b. Connect 5Ø ohm cable from PG5Ø8 + TRIG OUT to test scope external trigger in.

c. Connect 1X probe from PG5Ø8 TRIG/GATE IN to PM1Ø1 pin T19. Connect proge ground to PM1Ø1 ground.

d. Adjust PG5Ø8 TRIG/GATE LEVEL untill triggered (light flashes).

e. Connect 5Ø ohm cable from PG5Ø8 OUTPUT to BNC T. Connect T to 5Øm ohm terminator. Connect terminator to 7DØ2 TRIG IN.

f. Connect 1ØX probe from test scope CH2 to probe tip to BNC adapter. Connect adapter to BNC T at 7DØ2 TRIG IN.

DESCRIPTION

g. Connect another 10X probe from test scope CH1 to PM101 CLK ground then connect probe ground to PM101 ground.

h. Set test scope trigger source to EXTERNAL.

i. Connect data lines D0-D7 to PM101 pins T2-T9. Connect CLK line to PM101 CLK.

j. Using test oscilloscope to measure signal voltage, adjust PG508 output pulse for high level of +2.0 V and low level of +0.8V.

k. Set test oscilloscope display mode to ALTERNATE and position controls so that center graticule line represents +1.4V on both CH1 and CH2.

l. Adjust PG508 varible DELAY until CH2's pulse rising edge is 18 nS before CH1's 2nd pulse rising edge. Measure time at the +1.4 V level. Magnify the test scope sweep to set greater accuracy.

m. Adjust PG508 varible DURATION until CH2's pulse falling edge is 16 nS after CH1's rising edge.

n. Press IMMEDIATE, DISPLAY, and PROGRAM keys

o. Move cursor to end of existing program.

p. Press and hold DELETE key until entire program is deleted.

q. Press WD RECOGNIZER key

r. Move cursor to Data field and enter XXFF(HEX).

s. Press COUNTER key and enter 0 for 0 events. Enter 0 for Increment.

t. Press WD RECOGNIZER key

u. Move cursor to Est Trig In filed and enter 1.

v. Press TRIGGER key and enter 0 for Main.

DESCRIPTION

w. Move cursor Delay field and enter 3 for Zero delay.

x. Press Ø for System Under Test Cont.

y. Press Ø for Standard Clock Qual. Press END key to end test.

z. Press START and check that the 7DØ2 always triggers on DATA word XXØØ. Check that CTR1=ØØØØ1. Repeat this test several times.

aa. Set PG5Ø8 OUTPUT to COMPLEMENT. Inverted data on test scope should have the same setup and hold. Adjust PG5Ø8 if necessary.

ab. Press IMMEDIATE, DISPLAY, and PROGRAM keys

ac. Move cursor to Ext Trig IN under Word Recognizer #2 and change the 1 to Ø. Repeat step x.

Page 3-87 item aa.

ADD:

(see Fig. 3-14)

Below item aa.

ADD:

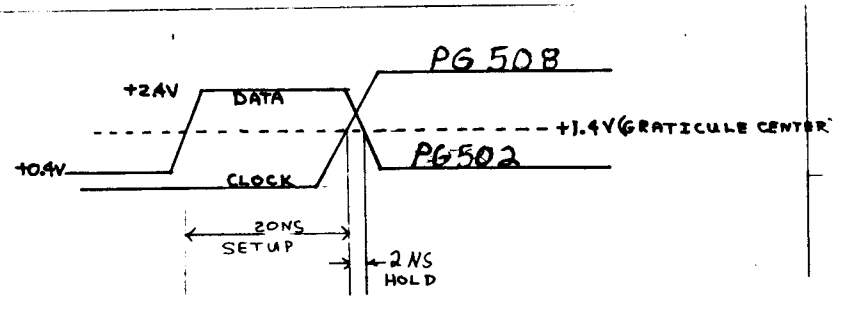

Fig. 3-14. Oscilloscope view of Setup and Hold.

Increment remaining figures and figure references by 1.

DESCRIPTION

Page 3-93 item f.

DELETE:
item f.

SECTION 5 MAINTENANCE

Page 5-55 2nd paragraph line 4

CHANGE TO:
The value at 3:YYFC is compared with the value at 3:YYFD, which should be its complement.

page 5-179 through 5-182 all references to

signature tables #23, #24 and #25

REPLACE

#23 with Front End (GP Probe) 670-5989-00
or with Front End (GP Probe) 670-5989-01

#24 with Word Recognizer (GP Probe)

#25 with Expansion Option (GP Probe)

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MANUAL CHANGE INFORMATION

Date: 4-23-82 Change Reference: C2/482

Product: 7D02 LOGIC ANALYZER Manual Part No.: 070-2919-00

DESCRIPTION

TEXT CORRECTIONS

SECTION 3 PERFORMANCE CHECK AND ADJUSTMENT

TABLE 3-1 Specifications page 3-12

Clock period minumum: 100ns

CHANGE TO:
Clock period minimum 50ns
(Delay by 1 or divide by 2)

page 3-66 above step 8

ADD:

8A. Minimum Clock Period (50ns) SNB020600 and above

Equipment required:

Test Oscilloscope
PG508
Text Fixture 1
50-Ohm Termination
Hook Tips
10X Probe (P6105) QTY 2
Extender (P/O Service Maintenance Kit, 067,0939-00)

a. Perform the Extender Installation Procedure.

b. PG508 Setup

PERIOD.....20ns (variable CW)
DURATION.....10ns (varible midrange)
MODE.....UNDLY
TRANSITION TIME.....5ns,1X,1X
OUTPUT VOLTS.....NORM

DESCRIPTION

c. Connect 50 ohm Terminator to PG508 OUTPUT.

d. Connect Test Fixture 1 to 50 ohm Terminator

e. Connect PM101 CLK lead to Test Fixture 1 red terminal and GND to black terminal.

f. Connect 10X Probe from Test scope CH1 to Test Fixture 1 red terminal and probe GND strap to black terminal.

g. Adjust PG508 OUTPUT for 0 to 5V amplitude signal.

h. Set Test Scope

DISPLAY MODE.....ALT
TRIGGERING .....CH1,AS,INT,+SLOPE
CH1 & CH2 VOLTS/DIV.....1V,DC
CH1 POSITION.....1.4 div below midscreen
TIME/DIV.....10ns

i. Adust scope trig. LEVEL for triggered display.

j. Adjust PG508 DURATION (variable) for 25ns pulse measured at midscreen (+1.4V)

k. Adjust PG508 PERIOD (VARIABLE) for 50ns period (20MHz)

l. Connect 10X probe from Test Scope CH2 to 7D02 J204-21A

m. Press IMMEDIATE, DISPLAY, and PROGRAM keys.

n. Move cursor to end of existing program.

o. Press and hold DELETE key until entire program is deleted.

p. Press WD RECOGHIZER key.

q. Enter all 0's in DATA field.

DESCRIPTION

r Move cursor to ADDRESS field and enter ALL F's in ADDRESS field

s. Press TRIGGER key then Ø for Ø-MAIN

t. Press Ø for BEFORE DATA

u. Press Ø for SYSTEM UNDER TEST CONT.

v. Press 1 for USER CLOCK QUAL.

w. Press Ø for RISING EDGE OF CLOCK

x. Enter all X's in C9-C4 (ANDED CLOCKS) field

y. Press 1 for USER CLOCK SYSNTHESIS

z. Press 1 then 2 for DIVIDE CLOCK BY 2

aa. Press END key to end test.

ab. Check that screen display matches Fig 3-1Ø

DESCRIPTION

```
 TEST 1
1 IF
1 WORD RECOGNIZER #1
1 DATA=0000
1 AD=XXFFFF
1 C0=X      C1=X      C2=X      C3=X
1 C4=X      C5=X      EXT TRIG IN=X
1 TIMING WR=X
1 THEN DO
1 TRIGGER 0-MAIN
1       0-BEFORE DATA
1       0-SYSTEM UNDER TEST CONT.
1       1-USER CLOCK QUAL.
1       0-RISING EDGE OF CLOCK
1       C9-C4 (ANDED CLOCKS)=XXXXXX
1       1-USER CLOCK SYNTHESIS
1       1-DIVIDE CLOCK BY 2
1       ESYNC: C6=X or C8=X
1       WAIT: C7=X OR C9=X
 END TEST 1
```

Fig. 3-10 Minimum Clock Period program result

ac. Press START and check the 7D02 does not trigger

ad. Set test scope trigger source to CH2 and adjust TIME/DIV to 20ns/div then check that CH2's frequency is one half that of CH1.

ae. Remove cables an probes.

Increment remaining Figures by one.

Step 8 title

CHANGE TO:

DESCRIPTION

8B. Check Minimum Clock Pulse Width (25 nS), Minimum Clock Period (100 nS SN8020599 and below), Minimum Data Acquisition Period (100 nS), and Minimum Interval Between Qualified Clocks