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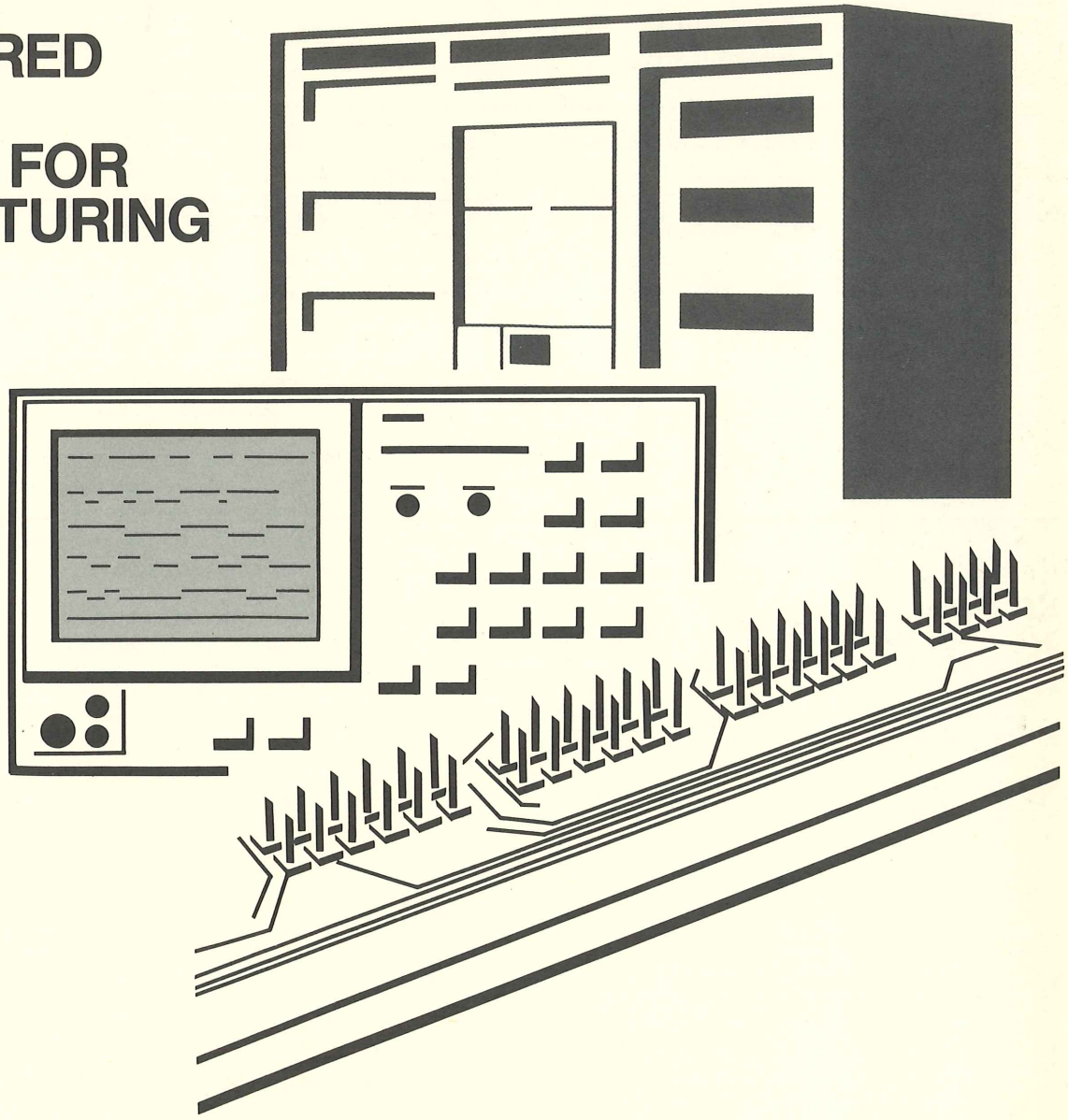
TECHNOLOGY report

COMPANY CONFIDENTIAL

STRUCTURED LOGIC ANALYSIS FOR MANUFACTURING TESTING



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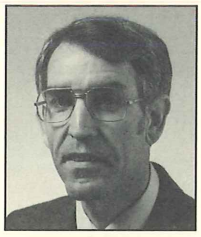
STRUCTURED LOGIC ANALYSIS FOR MANUFACTURING TESTING



Bob Broughton is an Engineer III in the Logic Analyzer business unit. Bob first joined Tektronix in 1960 in field engineering. He joined EH Research in 1966 as a product manager. Before rejoining Tek in 1979, he was the engineering vice president for a small business-computation company.

Until now, logic analyzers have not been used extensively in manufacturing test because logic analyzers have been considered as a design tool, useful only to the design engineer. However, logic analyzers have the promise of being the most powerful of the tools available to the manufacturing test organization. But first they must display additional information about the data acquired and the internal architecture of the logic analyzer, itself, must be better organized.

Fault Location in the Manufacturing Environment

Although problems can be discovered at any manufacturing step, the troubleshooting function seems to be the "hot spot" in the process. This hot spot is the point of delays and excess effort. (See figure 1 for a typical manufacturing test flow.) However once the fault is found, repair is straightforward.

Fault location is an exercise in information management. The more that is known about the fault, the less time the correct diagnosis will take. To learn more about the fault, new techniques are needed.

Some methods of fault detection, such as signature analysis, are powerful, but speed limited. ECL devices are an example of one of the logic families that can't be signature analyzed adequately. Skilling[1], Marshall[2], and Yates[3] have described limitations and problems with the signature method. Fichtenbaum[4] gave an excellent review of the fault-location limitations of in-circuit testing systems.

Although internal diagnostics are helpful in manufacturing, internal diagnostics are primarily end-user oriented, and therefore may not be thorough enough to diagnose all failures, particularly timing errors. External equipment such as logic analyzers may be required. (The methods described in this article complement internal diagnostics.)

But logic analyzers alone won't solve all problems. The testing processes, themselves, must be organized better – both within the manufacturing test organization and within the logic analyzer.

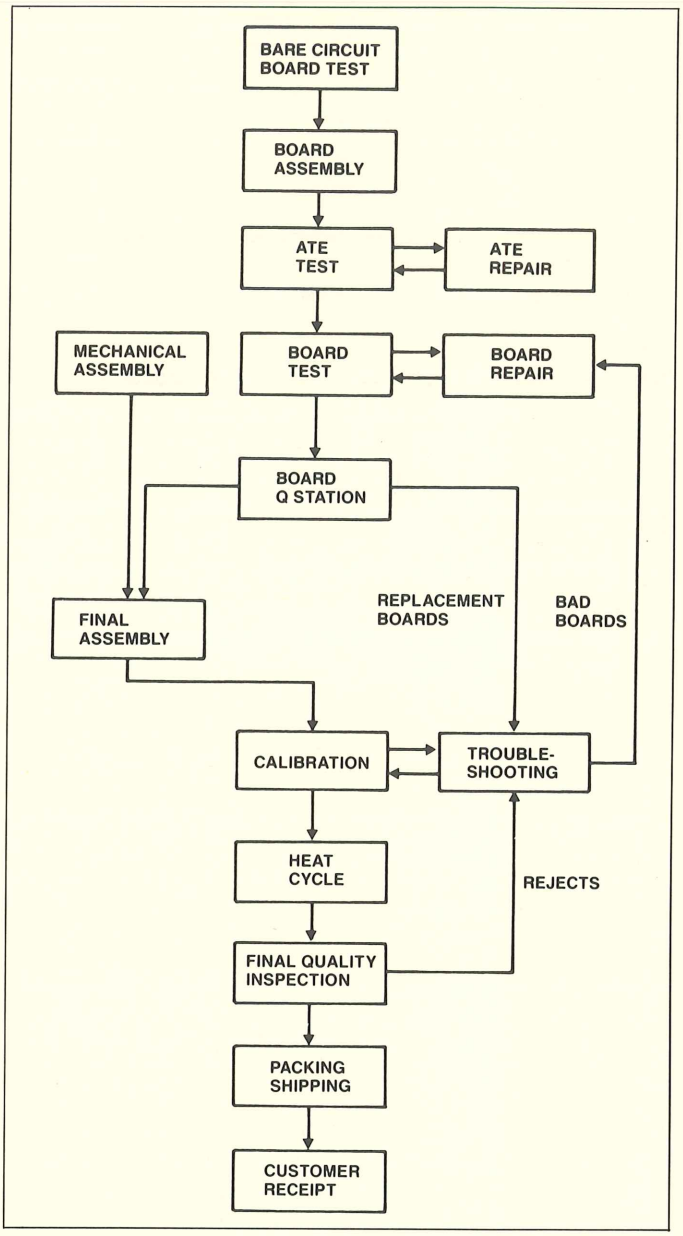


Figure 1. In a typical manufacturing test flow, the troubleshooting block is particularly labor intensive.

CHANNEL	MIN HI	MAX HI	MIN LO	MAX LO	CRC16	# OF GLITCHES	TRANSITION % HI	TRANSITION COUNT
[C 02]	3.05US	4.85US	7.25US	7.45US	4EC1	0	59	273
	(FULL) CURSORS:		+10.25US	-5.50US				
A 04	10.25US	12.80US	11.60US	15.40US	17F6	0	44	138
	(FULL) CURSORS:		+10.25US	-5.50US				
A 01	0.66US	100.66US	0.00US	2.03US	A406	737	100	3
	(FULL) CURSORS:		+10.25US	-5.50US				
C 02	2.65US	4.20US	12.55US	18.00US	103D	10	28	62
	(FULL) CURSORS:		+7.35US	-3.50US				
A 04	1.30US	1.40US	7.55US	7.60US	47AE	0	54	194
	(FULL) CURSORS:		+10.25US	-5.50US				
A 01	8.25US	9.05US	8.55US	8.85US	80C2	219	51	219
	(FULL) CURSORS:		+10.25US	-5.50US				

Figure 2. Logic-analyzer data statistics show the context of the acquisition, such as "full memory" and cursor locations.

Information Required from Logic Analyzers

Much fault-locating information can be acquired and displayed by a logic analyzer. The logic analyzer's internal computer can process data and present it in forms useful in the testing process. By displaying the context in which the failure occured, the troubleshooting task is simplified. Figure 2 shows such data presented on a logic analyzer.

In addition to the context information such as "full" memory and "cursor" location (shown in figure 2) an analyzer can also display these acquisition data:

Logic durations:
Minimum high level
Minimum low level
Maximum high level
Maximum low level
Cyclical redundancy check (CRC)
Number of glitches
Transition count
Duty cycle

These acquisition data describe the signal and its context in many meaningful ways and, by doing so, increase the opportunities to detect an incorrect value. An incorrect value often identifies the fault at hand.

All of the data values listed can be obtained over the logic analyzer's entire acquisition memory, or just between user-defined cursors. This additional data makes more analysis tools available. For example, an index or cross-reference can be used to correlate signal names as used on the schematics with the identifying group names used by the logic-analyzer, probe-pod, or channel number.

Method of acquiring "good" data for comparison

A logic analyzer captures and stores digital data in its acquisition memory. (See *What Is a Logic Analyzer,* following this article.) If a logic analyzer also has a reference memory, then data may be transfered from the acquisition to the reference memory. The reference memory enables an analyzer to hold the profile of a "good" product for comparison to the profile of a failing product stored in the acquisition memory. Such comparison is a powerful way to pinpoint a fault.

The good-product data in the reference memory can be transfered to a disk, tape, or computer for transfer back to the logic analyzer later. In this way, images of a working product can thus be stored indefinitely and used at any time.

As à product is designed and evaluated, logic analyzers with reference memories can capture data about the product's internal operation. For example, state and timing data may be acquired and saved. When the product is introduced to manufacturing, this data about prototypes may be transferred to manufacturing test.

Comparisons between data contained within logic-analyzer acquisition and reference memories may detect either *parallel* or *longitudinal* errors. When one analyzer channel has an acquired image (profile) that differs from that in the reference memory, this *longitudinal* error indicates failure in the tested product. *Parallel* errors result when a word of data formed from many acquisition channels differs from that in reference memory.

Logic analyzers that permit such comparisons provide manufacturing-testing power beyond the simple "good" or "bad." With logic analyzers, manufacturing organizations can test for quality concerns such as system set-up, hold-time sensitivity, and guard-band values.

If a logic analyzer having acquisition and reference memories can also control high-level acquisitions and comparisons in a programmed loop, the analyzer can search for intermittent faults. Such searches are done in an *auto-run* mode.

While searching for an intermittent fault, the logic analyzer's auto-run mode is used to complete these tasks:

1. Identify what section of the product contains the problem. (This, of course, is the hardest task of all.)
2. Connect the probes of the logic analyzer to that section.
3. Select the data source for the reference memory, and transfer the good-product data to the reference memory of the analyzer.
4. Select the logic-analyzer setup for the test.
5. Select the auto-run condition frame within the setup mode.
6. Set up the comparison of acquisition to reference data.
7. Select masking to mask out non-critical channels.
8. Set the analyzer to continue to cycle when comparisons are equal. (That is, when the tested product tests "good.")
9. Set the analyzer to stop looping and to display memory content when comparisons are unequal. (Product tests "bad.")
10. Start the logic analyzer.

Using the auto-run mode, the logic analyzer will loop on the test. If an error occurs (that is, a discrepancy between the data just acquired and data in the reference memory), the looping stops and the analyzer displays the just-acquired data. This process (acquire data, compare against reference, continue if ok) repeats automatically until an intermittent is located. (This method is also useful in verifying operation of prototypes in design engineering.)

As powerful as the logic analyzer is, it can't use all its muscle unless other data are available – and "structured" to help the person who is the actual troubleshooter.

Structuring is an information management tool. As I said earlier, fault location is an exercise in information management. We have discussed information organization in the logic analyzer. Next we will discuss the human component.

Structured Text Guides Test Technicians

Probably the least structured troubleshooting tool is the circuit diagram. A diagram cannot be used effectively without extensive technical knowledge.

The traditional fault tree is complex and tedious to use, but the tree is a more effective troubleshooting tool than just a circuit diagram. Unlike the circuit diagram, the tree does graphically relate operating nodes (see figure 3).

Because of the graphic emphasis of the tree format, trees present at least two difficulties: (1) Updating requires graphics editing, an expensive process. Adding or removing a node, requires redrawing to show how the nodes now interrelate. (2) Because functions often interrelate complexly, the troubleshooter often has to trace through an equally complex series of trees.

A better method is *structured text.* Compared to fault trees or circuit descriptions, structured text is easier to understand (more descriptive) and does not refer to other pages or diagrams as does the fault tree. And structured text is easy to update, with a computer, as the product changes.

To construct structured text, the designer or test engineer first decides what points within the unit under test demonstrate the characteristics of a working unit. Manufacturing or service technicians then use the text to check performance or to locate failures.

The Tektronix 834 Data Communications Analyzer[6] uses structured text to guide the test technician through manual fault diagnosis. Randle[7] and Thompson[8] have described the increase in effectiveness that the structured text methods bring. Several Tektronix instruction manuals[9,10,11] also use the technique effectively. Figure 4 shows two examples of structured text.

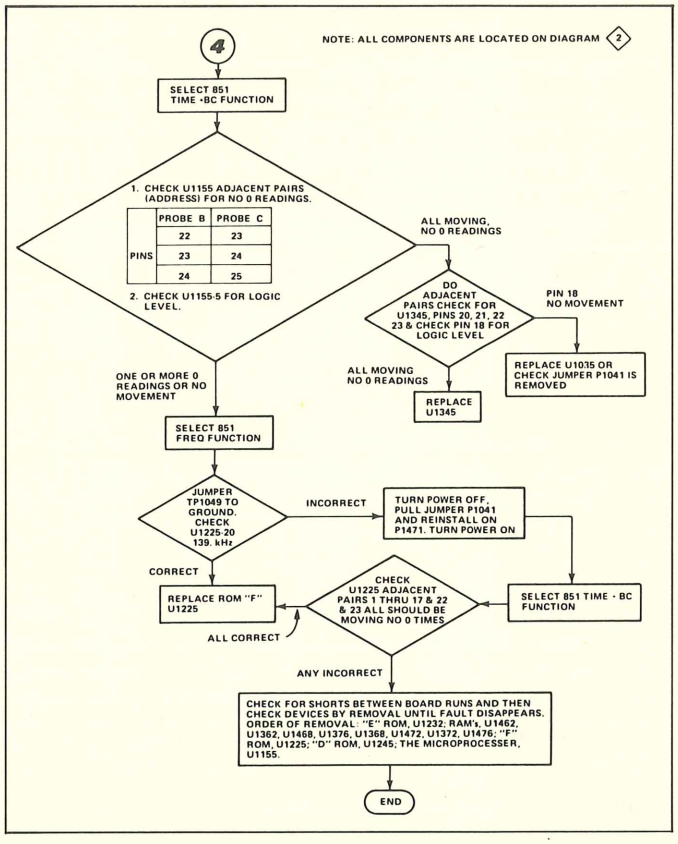


Figure 3. A fault tree guides a test technician through a troubleshooting problem but is cumbersome and difficult to update.

BI: 1 SYNC: RCVR <A or B>

EXPLANATION: The transmitter sent two sync characters (16 hex, 16 hex) to receiver A and receiver B. The receiver indicated by this error message did not receive the sync characters. The setup for this test is:

TX Free Run-off (Rec. B clock signal from TC 24 line [4]).
RX Free Run-on (Rec. A clock directly from timer BR0).
DCE SIM-on (RCT line used for transmit timing).
DATA SYNC-off (BR0 and BR1 used for receive timing).
NRZI off

POSSIBLE CAUSE:

1. The affected receiver did not receive a clock signal (not too likely since the test before this checked to see if a clock was available).

2. The affected receiver did not receive data.

3. The SIO is defective.

ACTION:

1. Restart the SVC-INT DATA test and let it stop on this error message. Check that the clock input pin (Rec. A=A1U211-13, Rec. B=A1U211-27 [3]) is being driven.

—If it is not being driven, trace the affected clock line back to the timer A1U235 [3]. See the setup for this test above to determine if the affected clock line comes directly from the timer or if it must go through the MODE SWITCH and the LINE RECEIVERS and DRIVERS via TC15.

—If it is being driven, see 2.

2. Initiate the SVC-XOR loop which causes the SIO's transmitter A1U211-25 to continuously send data over the SDT line. Check to see that the data is able to loop back to the affected receiver.

—If data is not getting back to the affected receiver (Rec. A=A1U211-12, Rec. B=A1U211-28 [3]), trace the data line back through the NRZI decodes [4], through the LINE RECEIVERS A5U221A, B [4] to the MODE SWITCH. (Because one of the receivers is working, data is getting from the transmitter at least as far as the MODE SWITCH where it splits to go to the two receivers.)

—If data is getting back to the affected receiver, the SIO A1U211 [3] is probably defective; see 3.

3. Replace the SIO A1U211 [3].

Table: Node Set 006

NODE SET 006 Board: 2952 Interface

Manual: 2952 Pattern Processor
Functional Block:
Select/control signals from 2952 I/F to remainder of 2952 via backplane

C H	Test Point	I O	Schem Loc'n	Signal Name	Signal Source
0	A08	O	04B05	SELECT 0	2952 Interface
1	A10	O	04B05	SELECT 1	2952 Interface
2	A12	O	04B05	SELECT 2	2952 Interface
3	A14	O	04B05	SELECT 3	2952 Interface
4	A16	O	04C05	SELECT 4	2952 Interface
5	A18	O	04C05	SELECT 5	2952 Interface
6	A20	O	04C05	MEM SELECT*	2952 Interface
7	A22	O	02D05	REGISTER SELECT	2952 Interface
C	829	I	02D01	COMMAND SHIFT SEQUENCE*	2952/1341 Interface

CIRCUITS VERIFIED: Select and Control signals used to address the desired register in the 2952. The data written into the command register (PPAR) is decoded following the trailing edge of COMMAND SHIFT SEQUENCE. The data written into the PPAR determines the state of SELECT 0 through SELECT 5, MEM SELECT and REGISTER SELECT, which are decoded by the other cards in the 2952 to enable the selected register. A bit is walked in bits 4 through 15 of the command register (PPAR) to verify that the command register data is decoded properly.

Figure 4. Examples of structured text.

Managing the Design for Testability

Somehow the signals necessary for manufacturing testing must be made accessible. To do this where high-speed logic is employed, circuit designers should assign critical signals to square-pin (test-port) connectors on circuit boards. Figure 5 shows some square-pin sets placed within difficult-to-test high-speed ECL areas of 1240 Logic Analyzer circuit boards. By increasing connectability, these circuits can be monitored easily by logic analyzers.

By such pin placement, the design engineer provides a means to verify the design – and "gives" manufacturing the "tools" of the design engineer: the test-port connectors.

Adding such connectors doesn't burden the design engineer; it aids the design process. Because, as the product moves from design engineering to test engineering in manufacturing, prototypes and production units can verified with identical processes and data sets. This "identicalness" presents a great opportunity to quantify quality issues.

Test engineers, in STS, found that when square-pin test ports can't be placed on the circuit boards, they can be placed on extender boards. This technique simplifies monitoring bus and backplane activity.

To construct structured text, the designers, after completing the design, must identify critical timing paths, significant state modes, and feedback loops. Then they tie the appropriate signals to square-pin sets on the circuit boards and specify the control needed to exercise the functional block. Next, they document the "test port" using the hard-copy output of the logic analyzer that verified prototype operation. Symptoms of potentially bad ICs are written into the support manual for test engineering.

This method encourages the design team to include many test-port connectors in early circuitry. The test-port connectors provide quick access to the critical lines of each functional block within the design.

Methods Assisting Manufacturing Testing

To locate faults to the component level in the S-3275, the STS business unit uses a combination of internal diagnostics and external instrumentation. This use, in the S-3275, is a good example of an integrated test strategy in a complex testing-system product.

The strategy in the S-3275 is a strategy of fault location by information management. The strategy has been successful, reducing fault diagnosis time and speeding final test verification. A logic analyzer is used for data acquisition and expanded data presentation. The product was designed for testability. Structured text was prepared to guide test and service technicians.

The logic analyzer, controlled by the S-3275 system computer, acquires data about the high-speed pattern generation in the system. The S-3275 is, itself, a testing system, containing three to four thousand ECL ICs on two dozen or so boards of several square feet each.

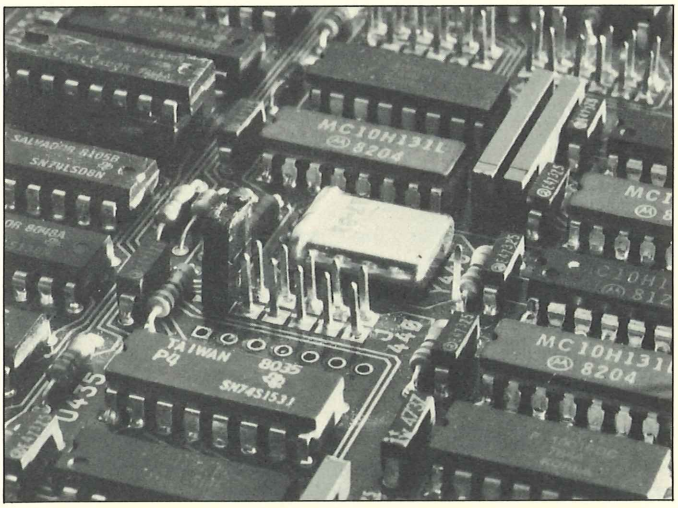


Figure 5. Square-pin sets increase connectability to high speed logic in the 1240 Logic Analyzer.

Because Field Service wanted fault isolation down to the component level, STS engineers designed an interface to allow the S-3275's system-control computer to access the data acquired by the logic analyzer. This interface is built into the S-3275. As test procedures were developed, good data was acquired from all parts of a working S-3275 and stored in disk files within the system-control computer. These files now contained a profile of the system as it should work.

An aspect of the service strategy for the S-3275 is repeated verification with on-line diagnostic software. If these diagnostic programs indicate a failure within the S-3275, the diagnostic documentation details the required tests to be performed by a service technician. The data stored for each test is recalled and compared by the system computer against data newly acquired by the logic analyzer. Any differences are documented and pinpointed and the remedy specified. The three interrelated instruction manuals for the S-3275[9,10,11], use and demonstrate this technique.

After repair, internal diagnostics verify that the failure has been cured. If anything fails, the technician reviews the internal diagnostics and selects the suspect section for examination by the logic analyzer. After the failure data is read back, the S-3275's CPU compares this data with good data from disk files. Following this routine, STS service people have reduced typical fault-location time from two hours to 5 minutes.

For More Information

For more information, call Bob Broughton, 629-1901.

Acknowledgments

Mark Dahl, of Tektronix STS manufacturing engineering, originated the concept of using logic analyzers in the manufacturing test process for the Tektronix S-3275 Test System. Larry Lewis helped write the test software for the S-3275.

Doug Boyce and the author extended the logic-analyzer-in-manufacturing test strategy to the manufacturing test process for the Tektronix 1240 Logic Analyzer. Bob Heath provided support with diagnostics software for the 1240 project. □

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WHAT'S A LOGIC ANALYZER?

Logic analyzers are instruments used to acquire and display digital signals occurring in electronic systems.

Logic analyzers always seem to be compared to oscilloscopes. In fact, the logic analyzer evolved from the oscilloscope. The timing diagram displays of logic analyzers look much like the displays of a multichannel oscilloscope.

The oscilloscope made it possible to view the change of electrical signals with time. As digital circuits became more and more common, the oscilloscope was pressed into service to view "digital" signals. As digital circuits became more complex, the oscilloscope's limitations became more apparent, principally its inability to show data and control flow. The logic analyzer was conceived to deal with the need to display data and control flow within these ever more complex digital circuits.

Where the input signal in a scope is processed through an amplifier, the input signal in a logic analyzer is routed to an analog comparator circuit which continuously monitors whether the analog signal (yes, it really is analog) at the probe tip is above or below a threshold value. The threshold levels of the comparators are usually adjustable in some way by the user.

A digital trigger circuit fed from the comparators monitors the data as acquired by the logic analyzer, continuously comparing the qualified incoming data with user-specified data values. In addition to the trigger circuitry, qualification circuitry ignores incoming data values that are unwanted, again as specified by the user.

When a combination of user-determined data values exists in the incoming signal, the trigger circuitry halts the advance of the memory address counter in accordance with user specification and 'freezes' what has been acquired up to now in the acquisition memory for later processing and/or display.

How comprehensively this trigger and qualification circuitry can distinguish between sequences of digital data determines how effectively the logic analyzer can detect the event of interest within a given stream of data.

Thus, the 'analog' signal at the probe tip is converted to a digital representation in two ways: vertically, by use of the comparators, and horizontally, by use of sampling in time. Once digitizing has occurred, it is possible to store the digital result in sequentially addressed computer memories for computer analysis, transmission to another location, storage, or display.

The display, then, is a statistical reconstruction of the original signal. What was an infinitely varying analog signal is now reduced to a granular representation of the original. It shows a likeness to the original signal, but with a graininess caused by the sampling process.

Where the oscilloscope is designed to observe the integrity of the analog signal in the analog signal path, logic analyzers observe the integrity of data in the digital data path. Although analog considerations cannot be totally divorced from digital circuitry, the logic analyzer, in the main, does not concern itself with analog issues. Of course, just because the result appears as a digital signal on the logic analyzer does not mean that precautions of handling (analog) signals do not apply.

Triggering

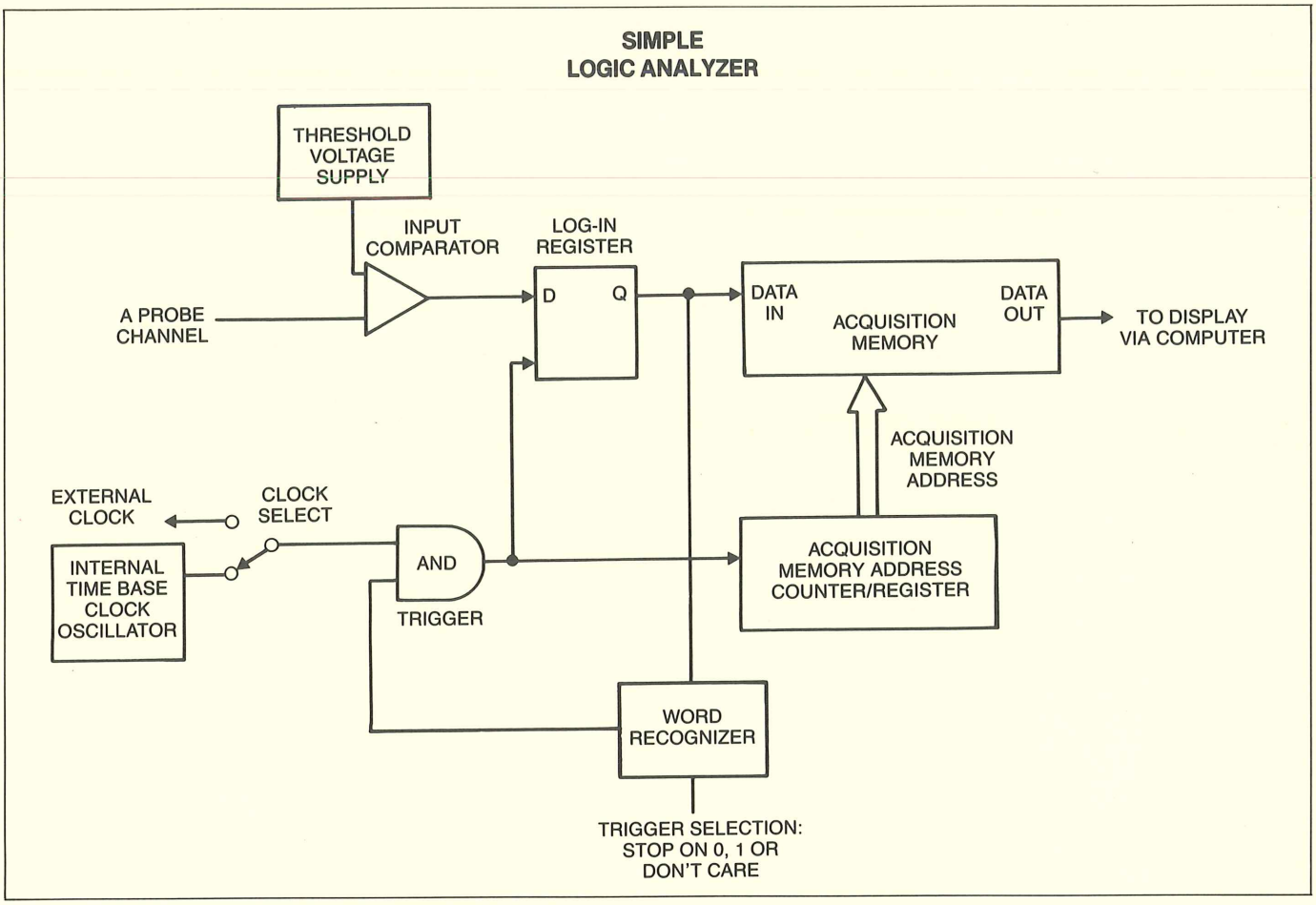
The digital memory stores the current digital value and sequentially increments its address upon receipt of each clock signal. Clock signals may be obtained externally from the equipment of interest, or internally from adjustable frequency oscillators or time bases; the first situation describes synchronous operation; the second describes asynchronous operation.

Regrettably, the logic analyzer is misnamed. It does not analyze anything, but rather it acquires and displays logic signals. Humans or computer software are the real 'analyzers' here.

Logic Analyzer Display Modes

Timing diagram displays

Timing diagram displays (or timing displays) appear as a multichannel oscilloscope display, but with nicely rectangular rise-and-fall times and flat-topped pulses. This display is designed to convey *timing* information, not amplitude information.



State table displays

A state table (or state display) shows the data the way you would expect a typewriter to display it. Binary ones and zeros or a variety of bases – octal, decimal or hexadecimal – may be presented. State table data may also be displayed coded in ASCII or EBCDIC characters, or as computer instruction-set mnemonics.

A set of input-channel data may be grouped as useful subsets. Grouping forms binary words by assigning a helter-skelter collection of data from various acquisition channels – individual data bits – to a named group defining the least-to-most significant bits on the basis of a user-defined list of channels.

Map displays

Map displays are accomplished by splitting the number of input channels in half, applying each half to a digital-to-analog converter, and then applying the resulting two analog signals to each axis of a X-Y oscilloscope display. The result is that the X-Y position of the spot on the display is determined by the value of the digital word applied to the input channels.

Connecting the logic analyzer to the memory address register of a computer and then using this map mode provides a graphic display of the usage of address space by the current software. Watching this rapidly updated display requires quite a bit of interpretation and an intuitive feel for the data being displayed.

Mapping has been displaced by more comprehensive trigger circuits and by more effective qualification methods. □

DATA DISPLAY CRT RESOLUTION MEASUREMENT TECHNIQUES

Pete Keller is an electro-optics engineer in the Technology Group. Pete joined Tektronix in 1963. Earlier, his interests in electro-optical devices and optical characteristics were exercised in his work at Stanford University and at the Kitt Peak National Observatory. He is currently chairman of an EIA subcommittee on resolution measurement.

Information density in displays is increasing rapidly with the phenomenal growth in data and graphics displays. The introduction of color to data and avionics displays has required improvement of the shadow mask CRT, which heretofore had only limited resolution demands placed on it, mostly for television use. All of this has renewed interest in display resolution and resolution measurement.

The resolution of data displays and data display cathode-ray tubes is a most difficult parameter to characterize. To be useful, resolution measurements must consider both the amount of information to be displayed and the repeatability of the measurement itself.

Large differences in resolution measurements are often observed, due to the diversity of display formats, such as raster scan, stroke writing, alphanumerics, and graphics. The diversity of measurement techniques often produces differing results. Differences in test operator perception and skills add to the problem. Resolution data should, therefore, be used with caution.

In comparing displays or CRTs, the display engineer must be sure that resolution data are comparable. A display from manufacturer A specified as having 20-mil resolution at the half-amplitude points with 200-microamp beam current may actually have better resolution than a display from manufacturer B specified as having 10-mil spot size measured with the shrinking raster technique at 100 microamps. Its the age-old "apples-and-oranges" problem again.

The resolution of a CRT display is often expressed several ways and measured in even more ways. Spot size, line width, number of lines, spatial frequency, MTF, etc., are all used as a measure of display resolution; each has differing connotations.

Spot Characteristics

The profile of the current distribution in a typical undeflected electron beam is usually nearly Gaussian, although it may differ with the angle of the sample slice. When this electron beam strikes the phosphor screen the light output distribution can differ from the current distribution in several ways (see figure 1): (1) The light output of an undeflected beam may be nonlinear due to phosphor saturation at high-current densities, thus flattening the peak. (2) Reflections within the CRT faceplate glass may cause spurious light at points well away from the central peak. (3) Phosphor graininess roughens the smooth profile. (4) Etched glare-reduction panels broaden the profile by scattering of the light from the spot. (5) Screen structure such as phosphor dots for shadow mask tubes and target patterns for storage tubes may cause gross features that limit resolution (figure 2).

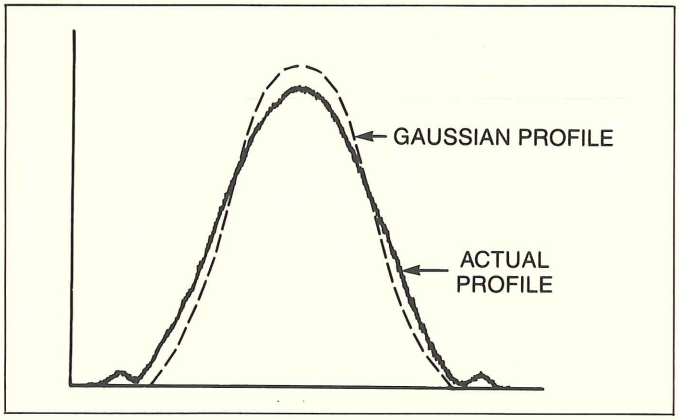


Figure 1. The theoretical beam-current profile is Gaussian but the luminance profile produced by the typical beam may differ in several respects.

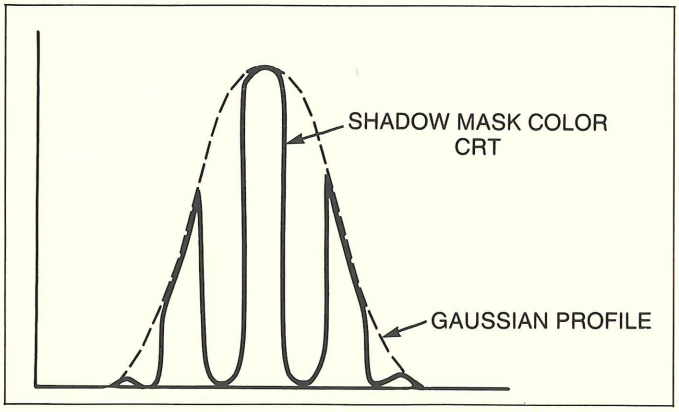


Figure 2. Profile of a shadow mask color CRT.

In addition to the above static-beam problems, deflecting the beam adds coma, astigmatism, and focus aberrations to the spot. Further, magnetic fields, power supply ripple, vibration, beam current and CRT operating voltages externally influence resolution and its measurement. All these factors are important as they determine the ultimate, useful resolution of the display. They must be eliminated to properly characterize the CRT alone, but need to be considered in determining the resolution of a complete display system such as a terminal.

Ways of Expressing Resolution

Resolution can be expressed several ways: (1) as spot size, typically spot width at the 50%-luminance points; (2) as line width, at either 50%-amplitude width or 60% if measured by the shrinking raster method; (3) as trace width, the width at approximately the 1%-luminance points, which are the trace limits as seen by the eye and measured with a microscope; (4) as the number of TV lines as judged from merging of tapered alternate black and white bars on a video test pattern; and (5) as MTF (in cycles/unit distance for a specified modulation depth), which is a measure of the spatial frequency response of a display. For a Gaussian spot these are related as follows (see figure 3):

Height	Correction Factor
60%	1.0
50%	1.18
10%	2.15
1%	3.03

The correction factor for other heights may be calculated using the equation:

$$CF = \sqrt{-2 \ln \left(\frac{h}{100}\right)}$$

where h is the height at which the trace is measured in percent.

Visual Methods

Microscope trace-width measurement – The simplest visual measurement method utilizes a microscope with calibrated reticle to measure trace width. This method is subjective and results in a width measurement at about the 1% level of the spot profile; this level varies considerably with ambient light and trace luminance. A single line, expanded raster, or circular trace may be used depending on the ultimate application.

Shrinking raster method – The shrinking raster method is widely used because it requires minimal instrumentation and is more accurate than the microscope method described above. It also produces "comfortingly" small spot-size numbers since the width is effectively measured at the 60% amplitude. With this method, a raster of usually 10 or 100 lines is first expanded until the lines are easily resolvable. Then the raster is shrunk until the individual lines are just barely discernable (figure 4). To obtain spot size, the raster's vertical size is divided by the number of lines.

Among the drawbacks of the shrinking raster technique is the subjectivity of judging when the lines merge. It is also difficult to apply it to structured screens such as in shadow mask color tubes.

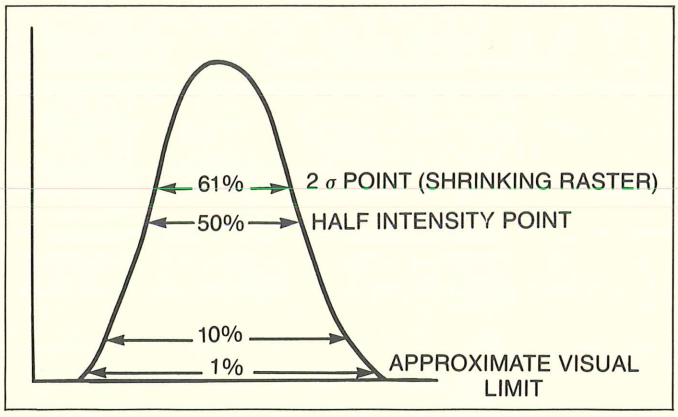


Figure 3. Common luminance amplitudes at which resolution is measured.

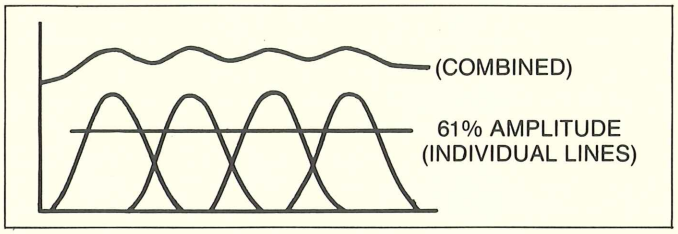


Figure 4. The luminance profile of a shrinking raster at the point at which individual traces are just resolvable.

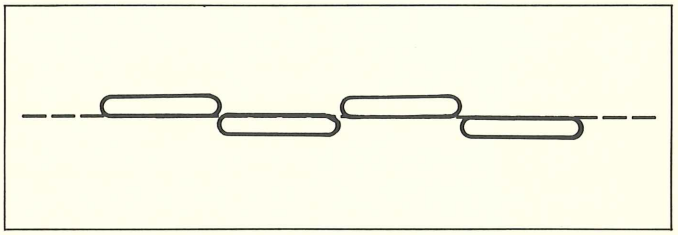


Figure 5. In the vernier line method, a trace width is determined by offsetting part of the trace by an adjustable amplitude square wave. When the trace "bottom " and "top" line up, trace width is determined from the deflection factor (sensitivity) and the square wave drive amplitude.

Vernier line method – This less known method is said to have the advantage of measuring the total width of the visable trace with greater repeatability than the microscope method. With the vernier line method, the amplitude of a small amplitude square-wave is adjusted until the top of one segment is co-plannar with the bottom of the other on the CRT (figure 5). At this point, the visual trace width is obtained by measuring the amplitude of the square wave input to the display and comparing it to deflection factor for the display. The deflection factor may be obtained by applying a known DC voltage to the input and dividing by the distance the trace shifts.

Photographic method – The photographic method is simple, provides qualitative values of astigmatism, coma, and halation and is especially useful for comparing the effects of gun design, alignment, focus voltage, beam current, etc. It is less useful for quantifying spot size due to differences in the sensitivity thresholds of film and the eye. With this technique, a series of photographs using a constant exposure are taken of the spot at various currents (pulsed to avoid phosphor damage or saturation) or focus voltages (figure 6). The film is moved slightly for each exposure so that an entire series of exposures appears on one print.

Television camera method – This method is similar to the photographic method except a television camera is used to display a magnified image of the spot or trace on a monitor. While being easier to view, it is not very useful for quantative measurements due to limited dynamic range, and because TV system gamma and threshold sensitivities differ from those of the eye. (Recently, some work using a television camera, frame storage, and a desk top computer has been reported to avoid the visual problems.)

Television test pattern method – Television resolution is usually determined by televising a test pattern having wedge-shaped alternate black and white bars with a calibrated scale (figure 7). The number of lines resolution is then visually determined by the point at which the individual lines are just discernable on the monitor or receiver under test. Both vertical and horizontal wedges are used in the center and corners to characterize the entire display. A variation of this method uses the radial resolution test chart developed by Tektronix (figure 8) which allows resolution to be evaluated at all angles rather than just vertical and horizontal.

As with other visual techniques, there is subjectivity in the test pattern method. Also, unless the associated electronics perform much better than the CRT, the results will be a measure of system performance rather than the CRT alone.

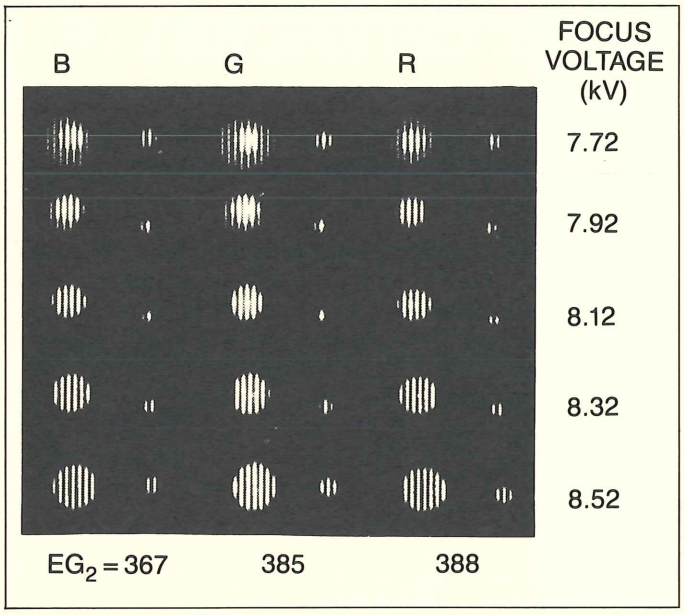


Figure 6. The photographic method (each beam at two beam currents).

Aperture/Slit Scan Methods

In aperture/slit scan methods lies the best potential for accuracy since the methods are photometric rather than visual. However, these methods are more complex and require greater operator knowledge to avoid errors. Most of these methods either electrically scan the beam past a detector having a finite area (figure 9) or move the detector across a stationary trace (figure 10). The resultant beam profile is displayed on a CRT or plotter as a curve of light intensity versus beam position.

Both slits and round apertures are commonly used. Each has advantages. A slit is best where the profile of a scanned line is necessary. The slit is oriented 90° to the direction of the scan. An aperture has the advantage of allowing a beam to be scanned past it in any axis to give a profile of the beam in that axis.

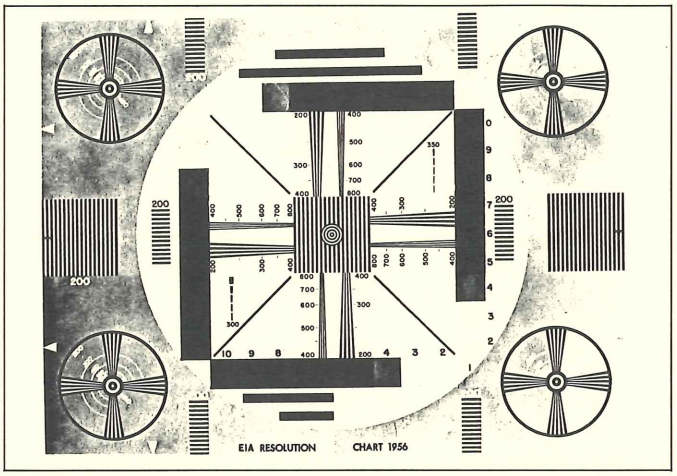


Figure 7. The EIA television resolution chart. Note the "resolution wedges" are oriented for the horizontal characteristics of a television picture system. (The blotches and loss of grey scale in this figure are due to limitations in the printing processes and don't appear in the actual chart.)

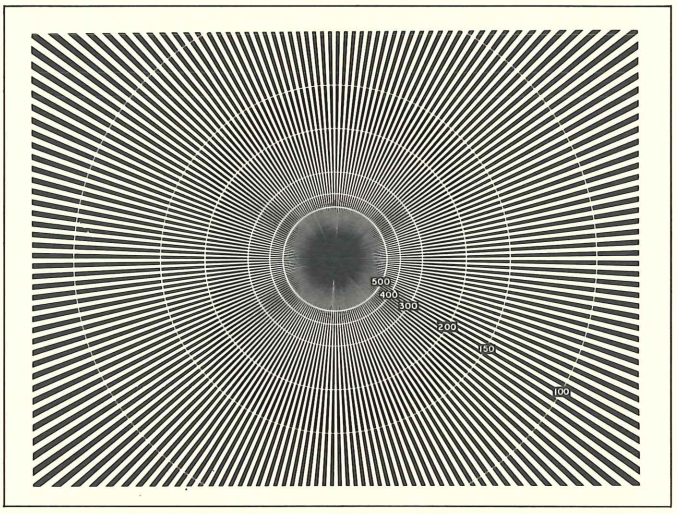


Figure 8. The radial resolution chart developed by Tektronix allows resolution to be evaluated at any scan angle.

The slit method allows more light to reach the detector since the slit samples more of a trace than would an aperture. The slit is also easier to position since the trace may cross anywhere along the length of the slit. The double-slit method (figure 11) is similar except that a second slit is spaced a known distance from the first. This distance is used to calibrate the beam position scale of the display; the display will now show a pair of profiles separated by the slit spacing.

Usually the trace is imaged at the plane of the slit or aperture using a lens. The light passing throught the slit or aperture is detected with a photomultiplier tube.

As an alternative, a fiber optic probe may be placed at the image plane of the lens and the output coupled to a photomultiplier tube (figure 12). The advantage of this is that the fiber position may be viewed through an eyepiece to aid correct positioning. The photomultiplier tube may be separate from microscope, reducing the mass and increasing the mechanical stability of the microscope.

Where small spots are to be measured, the microscope must be rigidly supported relative to the CRT and all local magnetic fields reduced to a minimum. Electrical noise on the deflection system must also be minimized. Aperture size or slit width should be about 10% of the expected trace width to minimize errors although it is reported that up to 40% may be used for truly Gaussian spots.

Several scan methods are in use presently. Mechanical scanning of the microscope assembly across a stationary spot or trace is widely used in aperture/slit scanning methods. Although this is slow due to mechanical constraints, it allows a display to be measured using its own circuits without applying external electrical scanning signals. It is also free of phosphor decay effects – an important consideration for long-decay phosphors such as type GR (previously P39). Electrical scanning of the CRT spot past a fixed microscope is the only practical way to profile shadow mask color CRTs without the screen structure affecting the profile. Such scanning also eliminates the effects of phosphor graininess on spot profile smoothness.

Where electrical scanning is used, either line scan in a single axis or a fast scan in one axis with a slower scan on the other axis (perpendicular to the slit) may be used. The two-axis scan avoids phosphor burning by reducing current density. Z-axis duty cycling may be used to hold the average beam current density to a safe level while measuring the beam profile at high peak-current densities with either scan format.

Spot Contour Plotting Methods

Two other methods of electrical scanning, developed recently, offer further significant measurement advantages but increase system complexity by requiring a desk top computer for control and data manipulation. Both methods produce a two-dimensional isophot plot of the spot. The plot shows spot intensity contours, making beam aberrations such as coma and astigmatism easily visible. These are not usually apparent in conventional X or Y plane profiles.

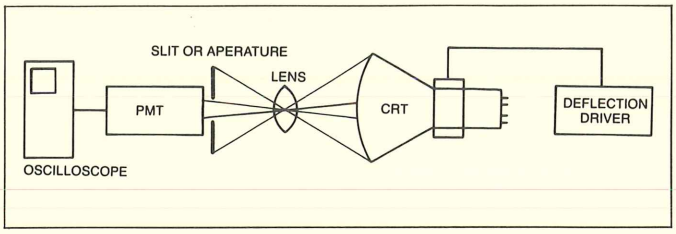


Figure 9. A single slit or aperture with CRT scanned electrically.

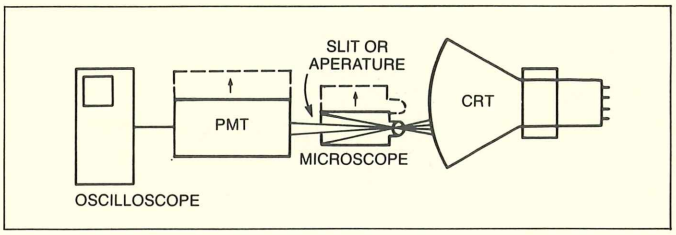


Figure 10. A single slit or aperture mechanically scanned across a stationary spot or line.

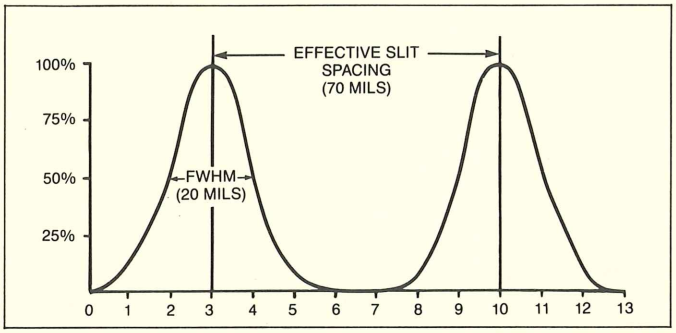


Figure 11. Typical beam profile with double slit method.

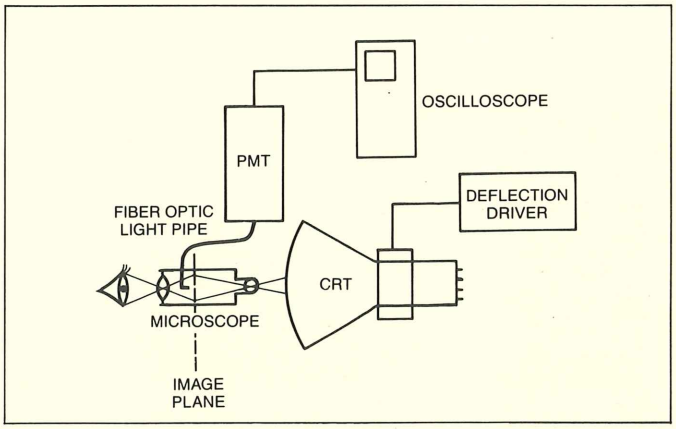


Figure 12. Fiber optic pickup of CRT beam profile.

The first method, developed by Phillips ECG, involves a series of radial scans, transfer of intensity values at various radial distances to local memory, normalization, interpolation, computation of percentages for these values, and plotting of the data at selected percentage levels.

The second method, developed by Tektronix, uses a dot-matrix scan with temporary storage of all intensity values in a matrix array; computation and plotting is accomplished as in the radial-scan method (see figure 13). The advantages of this method include uniform spacing of data points in the profile and ease of retrieving data from the array for further computations (such as MTF) or for plotting conventional beam-profile curves.

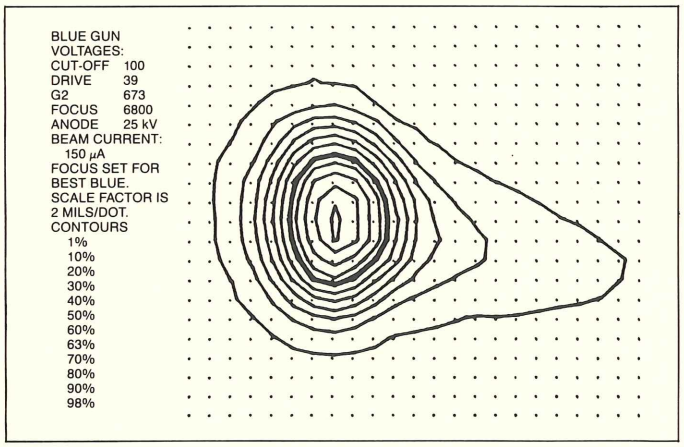


Figure 13. The Tektronix spot-contour plotting method clearly shows aberations such as coma – the lobe in this plot.

Image Dissector and CCD Methods

These two methods are distantly related to the aperature scanning technique. One images the trace with a lens on the photocathode of an image-dissector tube. The image dissector may be thought of as a photomultiplier tube having a very small effective area (aperture) on its photo-cathode. This small aperture may be electrically or magnetically scanned across the image of the CRT trace using conventional CRT scanning techniques. The output of the image dissector is then displayed on a CRT or X-Y plotter.

The other technique has just recently been introduced by Microvision as a commercial trace-width measurement product. In it, a line scan on the CRT being tested is imaged with a lens on a line-scan CCD array positioned perpendicular to the direction of CRT scan. The instrument then measures the trace width at any desired percentage of peak amplitude. The trace width, in mils, is displayed directly on an LED display. As this method requires little skill or judgement it is particularly well suited for manufacturing areas.

Since both of these methods use a stationary CRT trace while effectively moving the detector, structured screens such as color shadow mask CRTs are not easily measured with them.

Variable slit-width method – The variable slit-width method uses a calibrated, adjustable-width slit aligned parallel to a scanned line. The line is imaged on the slit by a lens with known magnification and the light passing through the wide-open slit is measured with a photomultiplier tube. The slit width is then reduced until a reading of one-half is obtained. The width of the reduced slit divided by the magnification equals the 50% width of the line. A related approach uses a spot photometer with two apertures of known size to calculate spot size.

Modulation transfer function (MTF) – MTF indicates the ability of a CRT to display sine wave modulation of various spatial frequencies (cycles per unit distance instead of cycles per second). It can also indicate the performance of a system or combination of system components by multiplying the modulation percentages of each component together for each spatial frequency. MTF is expressed as modulation percentage versus spatial frequency, usually in cycles/millimeter.

In shadow mask CRTs, MTF must be used cautiously. The MTF concept presupposes that the entire system is linear and spatially invariant. This invariance means the response to a given spatial frequency must be independent of the screen position of the sine wave excitation.

At least four methods are used to measure MTF for CRT displays. One replaces the slit with a grating in front of the photomultiplier tube (PMT). The grating is then scanned at various sweep rates and the percent of modulation measured using an oscilloscope connected to the PMT.

The second method uses a single slit at the PMT and a variable frequency sine wave applied to the CRT perpendicularly to the sweep. The sweep and sine wave are not synchronized, which allows the sine wave pattern to drift across the slit and the apparent modulation is measured with an oscilloscope. The procedure is repeated using different sweep rates or sine-wave frequencies.

The third method is similar to the second except that the sine wave modulates the Z-axis.

The fourth method uses Fourier transformation of conventional spot-profile data to produce a MTF curve. MTF data is difficult to measure but has distinct advantages when determining overall data display system resolution.

Conclusion

Because there are many ways to measure resolution, data must be carefully compared to avoid erroneous conclusions. In addition, whatever the method used, many factors influence the accuracy of resolution data including magnetic fields, vibration, duty cycle, power supply regulation and filtering, operator judgement, equipment calibration, deflection linearity, and stray light.

While the more sophisticated methods have higher inherent accuracy and repeatability, they also have subtle traps that negate their advantages if not used cautiously.

For More Information

For more information, call Pete Keller, 627-5429.

References

A list of references is available from the author, Pete Keller, 627-5429. □

NATFIN, A USER FRIENDLY HEAT ANALYSIS PROGRAM

Gordon Ellison is a physical scientist in thermal analysis. He joined Tek in 1976. Before coming to Tek, Gordon was a technical specialist at NCR, San Diego, working mostly in thermal analysis. He has also had experience with magnetic components and materials, laser generators, and infrared systems at NCR and at General Dynamics and Aerojet General. Gordon received his BA from the University of California and his MA from the University of Southern California.

NATFIN is one of a series of heat-analysis programs being developed at Tektronix, Inc. for in-house use. These programs are being used by mechanical and electrical design engineers and, occasionally, by industrial engineers.

The first in this heat-analysis series is VENTBOX[1], a program used to estimate the thermal characteristics of sealed or ventilated, but nonfan-cooled, enclosures. NATFIN, the principal subject of this article, is the second program in this series. The third and fourth programs, CATS[2] and FACFIN predict the airflow and temperature for forced-air-cooled enclosures, and extruded heat sinks, respectively.

We have designed NATFIN for the brief, but important, heat-analysis problem. It is for the user whose needs are occasional, perhaps no more than a few times each year. Because usage will be infrequent, we designed NATFIN to minimize difficulties caused by inexperience.

NATFIN computes the thermal characteristics of a vertically oriented plate having one of four heat-transfer configurations (see figure 1): Heat transfer to ambient from (1) the finned side of a sink, (2) the finned and flat sides of a sink, (3) one flat side of a plate, or (4) both flat sides of a plate. Because the flat plate is used often, it is worthwhile to consider it as a separate configuration.

In NATFIN, the opposite sides of the sink or plate are permitted to transfer heat to two ambient temperatures: TAF (front) and TAR (rear). This two-sided approach is useful when a rear panel/heat sink combination dissipates to both a room-ambient TAF and a higher TAR (internal instrument ambient).

VENTBOX, NATFIN, FACFIN, and CATS are interactive, menu-driven programs. In NATFIN, for example, a balance is achieved between user-command requirements and program prompting. Efficient use of the command philosophy is obtained by including only major options in the menu. The user can obtain the actual menu list and option definitions from most locations within the program execution sequence by using the HELP option. More obscure data-entry requirements are specifically requested by NATFIN prompts.

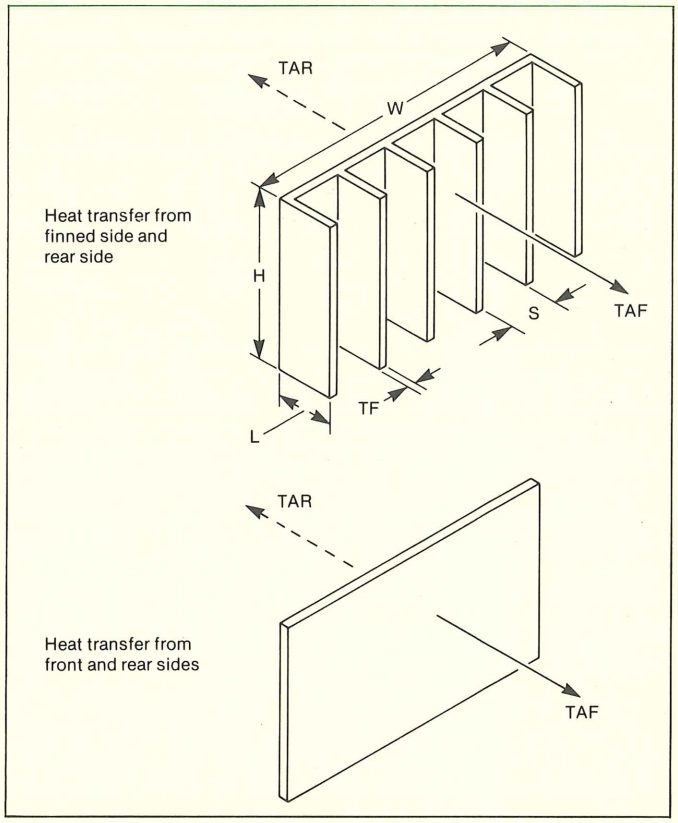


Figure 1. NATFIN heat-transfer configurations[4].

NATFIN solutions are obtained through twelve user-callable options. Any one of these is selected by typing the option name on the terminal keyboard. Program execution is stopped by typing END. Most of the options are shown in the sample problem in the next section.

NATFIN is written in FORTRAN 77 and resides on the Cyber. The PLOT 10 graphics package (designed for Tektronix 4010-series terminals) is extensively used for output display.

Sample Problem

We used a Thermalloy extruded heat sink as a sample problem (shown in figure 2). Thermalloy specifies the heat sink's thermal resistance for a 75°C mounting-surface temperature rise and a black anodized surface ($\varepsilon = 0.7$).

The first option used, but not shown in the sample-problem illustrations, is CONFIG. NATFIN responds to CONFIG with questions about the heat-transfer configuration. In the problem, the configuration of heat transfer from both the finned and flat sides were used.

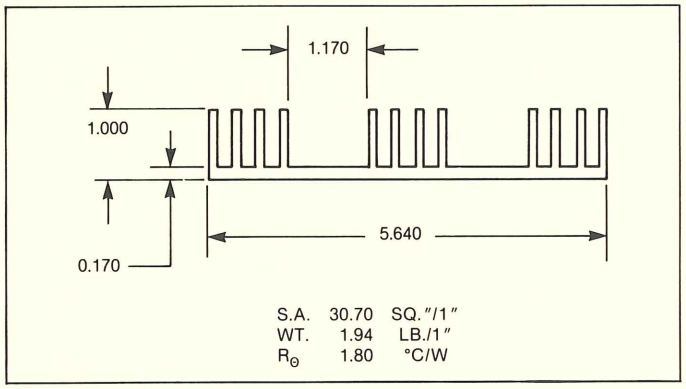


Figure 2. Cross-section of heat sink used in the sample problem. The dimension labels are from the Thermaloy catalog. H = 5.6 in., L = 0.83., T_F = 0.080 in. Reprinted with permission of Thermaloy, Inc.

All NATFIN variables (dimensions, etc.) are preset to default values. The user changes these values to correspond to the dimensions of figure 2 by using the INPUT option. The variable values, options, and definitions are listed by a NATFIN response to the HELP command (figure 3). Note that NF is the number of uniformly spaced fins and is estimated to be 16. The fin spacing S was computed by NATFIN.

An exit from INPUT and an exercise of the DRAW option produces a top and rear view of the heat sink. Width and fin-number scales help determine what fins can be deleted to make space for transistor mounting. In this example, fins 5, 6, 11, and 12 must be removed. Fins are removed by a simple exercise of the DELETE option. A subsequent use of DRAW results in the device shown in figure 4. The NATFIN model now adequately represents the Thermalloy heat sink.

Once the heat-sink geometry has been established, thermal computations are completed using the STANDARD command. Graphical results are obtained by using the PLOT command, to which NATFIN responds with questions concerning sink temperature, resistance, or heat-transfer coefficients as the dependent variable (Y-axis) and sink temperature or heat dissipation as the independent variable (X-axis).

It is important to note that NATFIN results are *averages* over the heat-sink surface. And since temperature gradients through the base thickness are not determined, thermal spreading resistances must be determined in some other way.

The heat sink is rated by Thermalloy at a 75°C rise, which is a 95°C surface temperature for the 20°C ambient used in the problem. An OUTPUT option is used to list the computed results. In this case, NATFIN predicted R = 1.65°C/W. An enhanced heat transfer coefficient computed with NATFIN was used as input to TAMS[3] to include the effect of thermal-spreading resistance for one TO-3 transistor centrally mounted and two TO-3 transistors uniformly distributed from left to right. The net results were R = 1.91 and 1.74°C/W, respectively. These results bracket Thermalloy's measured 1.8°C/W.

SINK CONFIG. - HEAT TRANSFER FROM FINNED/FLAT SIDES

OPTIONS	DESCRIPTION
DRAW	DRAW AND LABEL SINK
HELP	LIST VARIABLE NAMES, OPTIONS
LIST	LIST CURRENT DATA VALUES
INPUT	INPUT DATA
EXIT	EXIT FROM DATA INPUT OPTION
DELETE	DELETE FINS
REPLACE	REPLACE DELETED FINS
CONFIG	SELECT SINK SURFACE CONFIGURATION
STANDARD	SELECT STANDARD COMPUTATIONAL OPTION
OPTIMIZE	SELECT OPTIMIZATION OPTION
PLOT	PLOT RESULTS
OUTPUT	LIST SPECIFIC DATA VALUES
END	TERMINATE PROGRAM

INPUT VARIABLE	DEFINITION	VALUE
H	SINK HEIGHT	3.00 IN
W	SINK WIDTH	5.64 IN
L	FIN LENGTH	.83 IN
S	FIN SPACING	.291 IN
TF	FIN THICKNESS	.080 IN
NF	MAXIMUM NUMBER OF UNIFORMLY SPACED FINS	16
KAL	SINK THERMAL CONDUCTIVITY	5.0 W/DEG C IN
EF	EMISSIVITY, FIN SIDE	.70
ER	EMISSIVITY, REAR FLAT SIDE	.70
TAF	AMBIENT, FIN SIDE	20.0 DEG
TAR	AMBIENT, REAR FLAT SIDE	20.0 DEG
QSINK	MAXIMUM DISSIPATION	50.0 WATTS
UNITS	LENGTH	IN

ENTER <RETURN> TO CONTINUE

Figure 3. NATFIN response to HELP command.

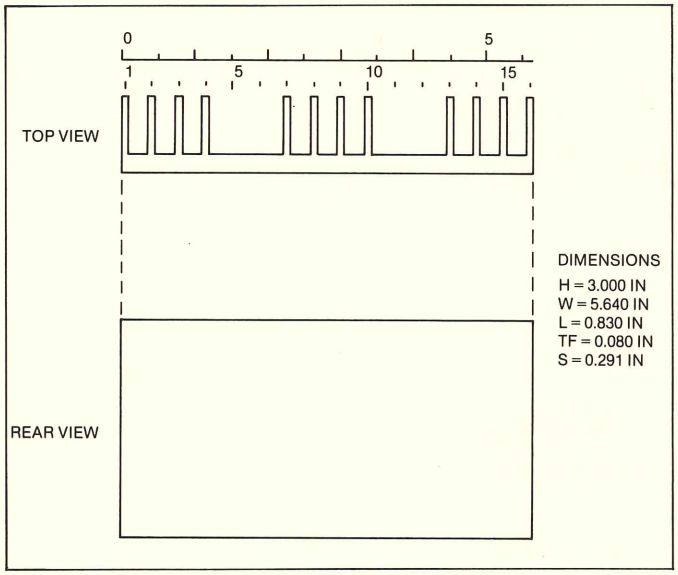


Figure 4. NATFIN response to DRAW command following use of DELETE option[4]. Fins 5, 6, 11, and 12 are removed.

An important NATFIN option, OPTIMIZE, is usually used before STANDARD in most design applications. OPTIMIZE computes the sink temperature and resistance versus the number of uniformly spaced fins over the sink width.

Figure 5, the result of an OPTIMIZE followed by PLOT, indicates that the vendor's heat sink was well designed when based on 16 uniformly distributed fins. Fewer fins are insufficient for cooling, while more fins choke the air draft.

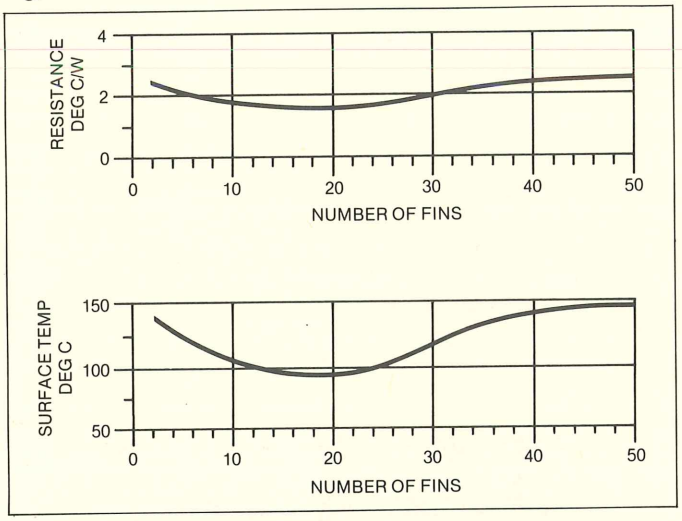


Figure 5. The NATFIN OPTIMIZE[4] option used in the sample problem.

For More Information

For more information, contact Gordon Ellison at 627-6441, d.s. 50/454. Or try NATFIN for yourself by logging onto Cyber and entering THERMAL,NATFIN<CR>.

This article is based on the paper in reference 4.

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2. Ellison, G.N., "Computer Aided Analysis of Forced Air Cooled Enclosures," presented at the Third International Electronics Packaging Conference (1983) Oct.
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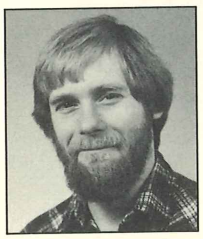
4. Ellison, G. N., "NATFIN – An Interactive Thermal Analysis Program for Natural Convection/Radiation Cooled Heat Sinks," presented at the Second Annual International Electronics Packaging Conference (1982) Nov.

DIELECTRIC CHARACTERIZATION
WHEN THE ECB ITSELF IS PART OF THE CIRCUIT



Cal Diller is a senior instrument engineer (IV) in Portable Oscilloscope Engineering. Cal joined Tektronix in 1974 after five years at Triplett. He received his BSEE from Ohio Northern University.

A new method allows easy electrical characterization of ECB raw materials and solder masks in adverse environments. Insulation resistance and capacitance versus frequency are more completely testable, opening the door to specifiying these parameters. The method employs a Tektronix developed test pattern and a specially developed measurement instrument.

In most electronic equipment, the etched circuit board is the primary means of mounting and electrically interconnecting components. In most cases, circuit designers can assume the interconnections are isolated from each other; they don't have to consider the dielectric performance of the board material (the resistive and capacitance effects). Low-voltage power supplies, for example, are insensitive to such effects. However where high-impedance circuits process signals, particularly high frequency signals, board effects should be known.

At high frequencies, the board itself is an electrical component. For example, to achieve broad frequency response, high-impedance resistive divider networks are usually compensated with capacitors. (The resistive elements in these networks, as used in scopes, range from 10 K to 1 megohms.) At low frequencies, the resistors dictate the division ratio, while at high frequencies capacitance dominates. The frequency where both effects are equal is the *crossover frequency* – typically between 1 and 200 kHz.

Since ECB stray capacitance is often sizable compared to at least one of the compensating capacitances, it can distort divider performance. At Tek, we call this effect dielectric "hook." Hook describes the distortion of the pulse response that remains when the compensating capacitances have been adjusted for a displayed waveform shape that matches the actual pulse characteristics. In the frequency domain, the effect simply amounts to dielectric constant changing with frequency.

Since ECB techniques cost less than most alternatives, the cost-conscious circuit designer is driven to build high-impedance dividers almost exclusively on ECBs – despite dielectric effects. Therefore, before the designer can rely on a material for circuit board use, it must be characterized relevant to the application. Only when a suitable characterization method exists can ECB material specs be written.

Characterization Methods

Traditional ECB characterization methods are difficult and limited in scope; they require lots of interpretation to extract useful data. What we needed was a new method to characterize ECBs for sensitive circuit design. And, since ECB insulation qualities are worst at high temperatures and humidities – conditions for which Tek instruments are spec'd – we needed a method that would work in those harsh environments.

We needed to know three characteristics: *insulation resistance* to at least 10^{12} ohms, *test pattern capacitance* to better than 1%, and *capacitance change versus frequency* (hook) to better than 0.1%.

These parameters are important referred both to the surface and through the thickness (bulk) of a sample. Most parameters are only useful when measured at high temperature, or high humidity. Surface measurements are useful both with and without solder mask.

Test Pattern

To make these measurements easily, a simple, universal test pattern must be used. A test pattern is an arrangement of conductors that is applied to a sample to simulate the physical properties of actual circuits applied to boards.

The pattern should (1) fit within the margins of a fully utilized flat without displacing actual circuitry, (2) resemble actual circuits, and (3) allow all measurements with minimum reconfiguration of equipment. Many patterns are available, but since none meet all three requirements, we chose to modify the IPC standard interdigitated comb.

The resulting dimensions are shown in figure 1. This image is placed once on each side of a sample of the material under evaluation; the front pattern overlays the rear with the board material sandwiched between.

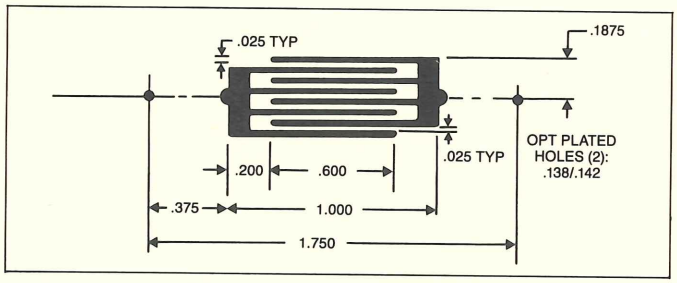


Figure 1. The test pattern. The .025 inch line, .025 inch space/finger arrangement are equivalent to two parallel runs 4.2 inches long spaced at .025 inches. Because the line widths and spacings of the pattern are the same as in many Tek circuits, pattern measurements and actual circuit performance correlate.

A solder mask is applied to the solder side. The other side is left uncovered, so that measurements of masked versus unmasked patterns can be compared. The technique allows measurement of both surface and bulk characteristics. Holes for locating pins are provided beyond the ends of the pattern. When a material sample with patterns applied is removed from its flat, the pattern is called a *coupon.*

Measurement Fixture

We developed a measurement instrument to meet the environmental demands of this application (see figure 2). A remote test head, designed for demanding environments, attaches to the sample. A pair of index holes in the test pattern orient the head of the measurement fixture, eliminating wire soldering and manual alignment. With fully guarded surfaces, the head shields the test sample from the stray charges common in breezy test chambers. For ease of changing test samples in the test chamber, the head features pogo-pin simplicity (see figure 2).

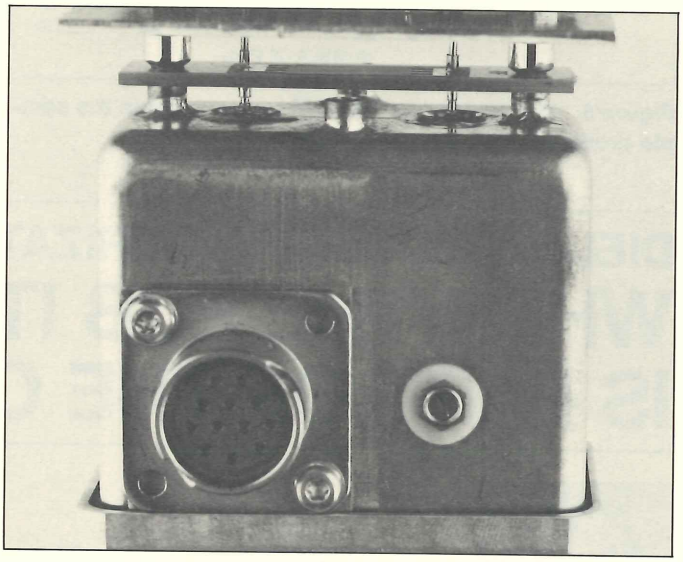


Figure 2. To make measurements in environmental chambers, the remote head is sealed and guarded with a drive voltage.

Synchronous AC detectors are used for high sensitivity, noise immunity, wide bandwidth, and stability. Together with a split-path head amplifier, the system measures capacitance within 0.2% from 20 Hz to 500 KHz. (See figure 3.)

The instrument measures and digitally displays:

- DC insulation resistance (IR) in terms of conductance (200 nanosiemens full scale, 0.1 picosiemen resolution)
- AC insulation resistance in terms of conductance up to 1 KHz max (200 nanosiemens full scale, 10 picosiemen resolution)
- Absolute sample capacitance (20 pF full scale, 0.01 pF resolution)
- Relative sample capacitance deviation from set reference (200% full scale with 0.1% resolution)

All four measurements can be made in either a surface or bulk mode at the command of a front panel switch. Test frequencies are supplied by a built-in function generator (see figure 4).

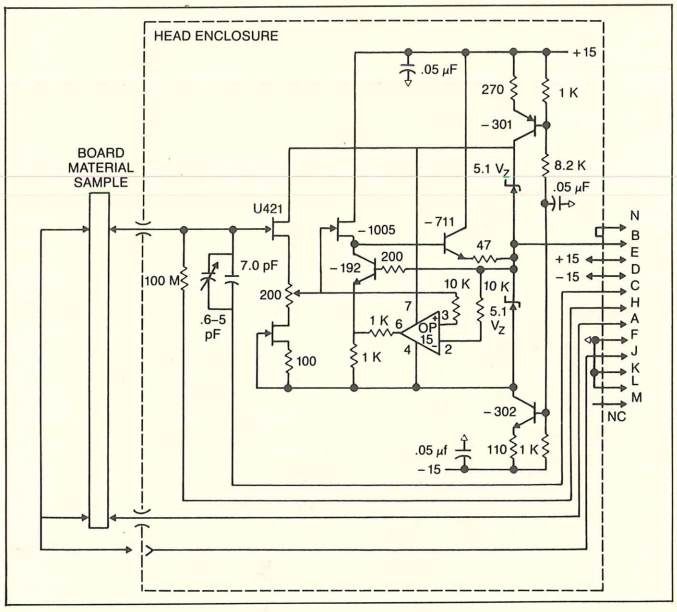


Figure 3. The split-path head circuit drives the test unit to one volt (0.1%) at 500 kHz into 200 pF while maintaining less than 1 pA input bias and 15 μV/°C offset drift.

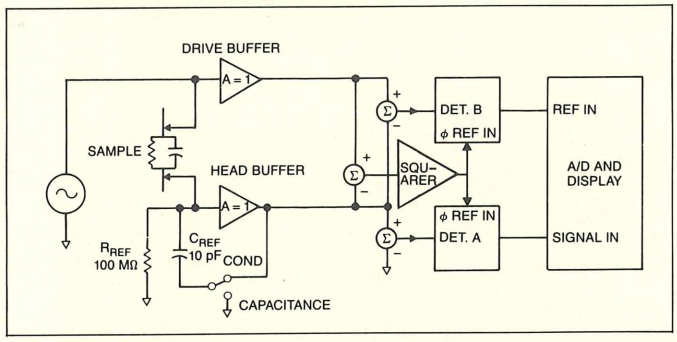


Figure 4. The instrument setup for absolute capacitance and AC conductance measurements.

For capacitance measurements the measurement fixture simulates the crossover effect (described earlier) with a switch-selectable crossover frequency, settable in four decades from 2 Hz to 2 KHz. The same switches select conductance measurement ranges so that an appropriate crossover frequency choice is automatically made once leakage has been measured.

The ease and consistency this method offers allows ECBs to be specified as "electrical" components. The following characteristics may now be measured:

- Surface insulation resistance in humidity (bare ECB)
- Surface insulation resistance in humidity (with solder mask)
- Bulk insulation resistance after humidity at high temperture
- Bulk capacitance at one test frequency (relates to dielectric constant)
- Surface capacitance change (hook) with frequency (two frequencies – with mask)

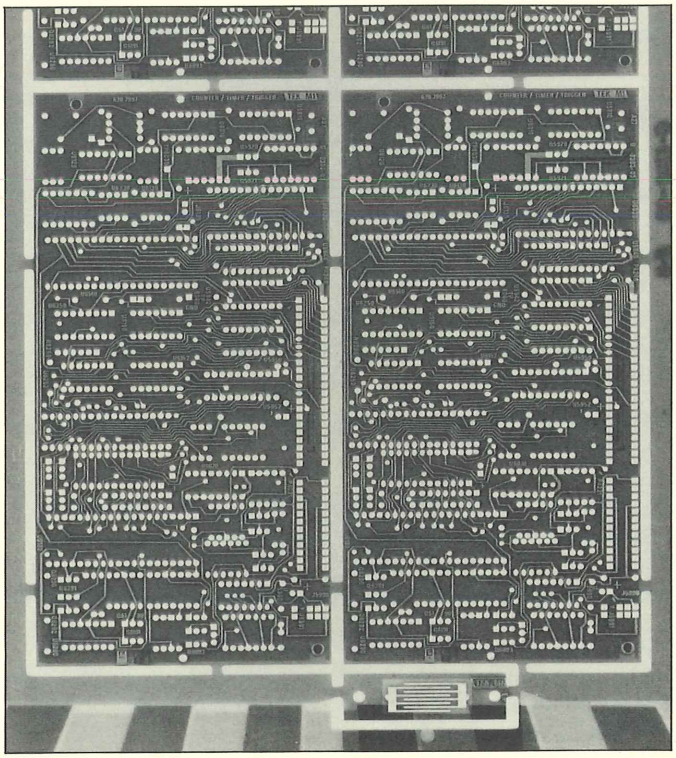


Figure 5. A fully utilized flat still has room for a *test coupon.* The coupon allows electrical tests at any manufacturing stage. It is discarded later.

- Bulk capacitance change (hook) with frequency (two frequencies)
- Surface capacitance variations with environmental conditions (at one test frequency, no mask versus masked)

Usually, even in sensistive designs, just one or two of these parameters are important. Because additional specs usually add to board costs, specifications should be used only when they are required, and when their cost impact has been researched with the vendor.

Now, with the new method, ECB quality can be tested at the vendor's site. Testing can also be done readily at incoming inspection. If the test coupon is part of the flats processed in assembly manufacturing, solder, wash, and handling processes can be monitored for cleanliness – IR measurements quickly reveal dirty processes.

Summary

Some solder mask qualification has been performed with promising results. But much remains to be learned – the dielectric characterization method is only beginning to be applied.

For More Information

Questions involving the equipment and test pattern should be directed to the author, Cal Diller, at 627-2874. For questions about solder mask and ECB measurements, call Richard Van Epps at 253-5275. Bob Forman (640-2288, ext. 4248 (F1)) can answer questions concerning performance of solder mask materials.

HOLMES, JONES, AND KESKI RECOGNIZED FOR HYBRID ACHIEVEMENTS

Do people outside Tek know that we make hybrid microelectronic components? Yes they do. That's not surprising since Tek is one of the larger captive manufacturers of microelectronics in the United States.

ISHM members know us too. Not just for size, but for technical and professional achievements.

The International Society for Hybrid Microelectronics acknowleged Tektronix contributions with the 1983 Corporate Award and individual awards to Bob Holmes, Roydn Jones, and Jim Keski. The awards were presented October 31, in Philadelphia.

Bob Holmes received the Daniel C. Hughes Award – ISHM's highest individual award – for his administrative contributions to ISHM and his technical innovations in thin-film deposition and photolithographic processes.

Roydn D. Jones received a Technical Achievement Award for design methodology for microwave integrated circuits and his recently published book, *Hybrid Circuit Design and Manufacture*.

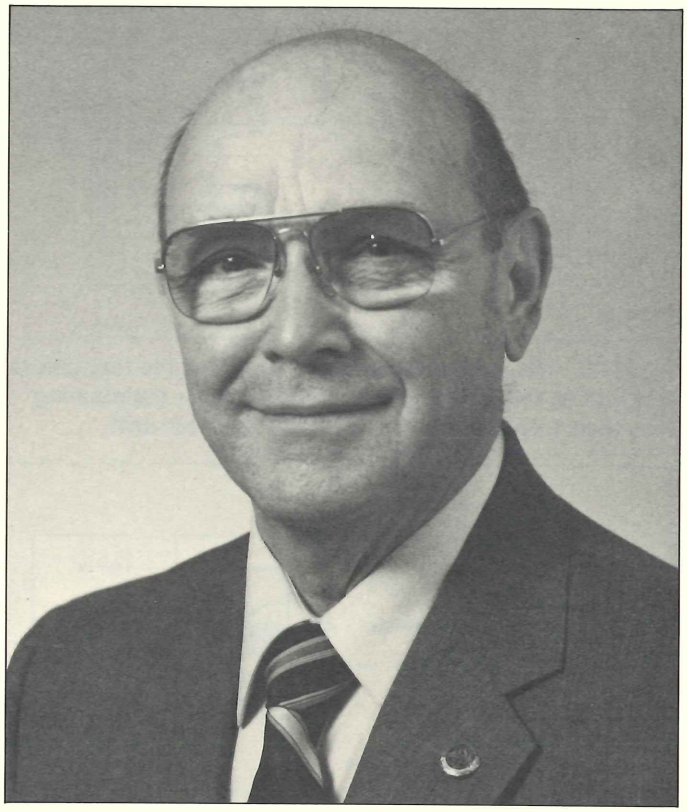
Jim Keski was made a Fellow of the Society for his continuing contributions to the hybrid microelectronics industry and his support of ISHM.

Tektronix was recognized for both its outstanding contributions to the hybrid technology and its support of ISHM at both the national and local levels.

Microelectronics include both integrated circuits and hybrids. ICs are monolithic – everything is built in. Hybrids, in contrast, may contain both components that are fabricated into the hybrid and discrete components that are built separately and attached to the hybrid.

Why two types of microcircuits? Economics and performance.

In some cases, it costs too much to develop an IC for a low volume product. In other cases, the physical and process realities do not allow an IC to achieve a necessary range of component values or performance. A hybrid can often outperform and underprice an IC.

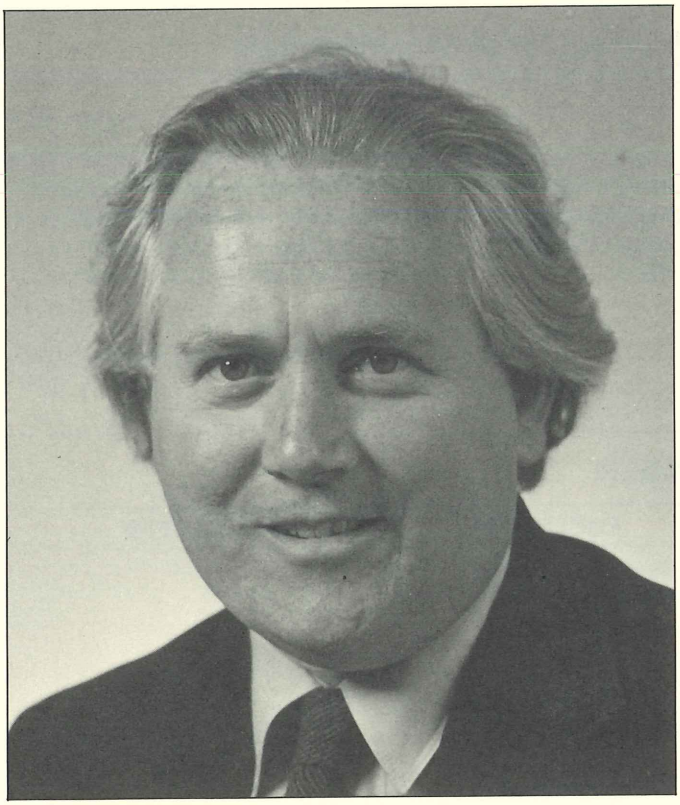


Bob Holmes

Bob Holmes is a charter member of ISHM. He was national president, 1980; president-elect, 1979; vice president, 1978; treasurer, 1976-77; and technical chairman, 1975. He was president and secretary of the Northwest Chapter, including Oregon, Washington, Idaho, and British Columbia.

Bob was instrumental in establishing the Microelectronic Process Technology program at Portland Community College; Bob is the chairman of the College Advisory Board for that program. He is also responsible for the hybrid component bank, one of ISHM's University Educational programs. He is a member of the American Chemical Society, the Vacuum Society, and was recently elected to the adminstrative committee for the Components, Hybrids, and Manufacturing Technology (CHMT) group of IEEE.

Bob is a principal engineering scientist, reporting to the director of the Solid State operation. Bob joined Tek in 1967 as a CRT engineer. He has managed the thin film development group and been a senior process engineering advisor in hybrid circuits engineering.

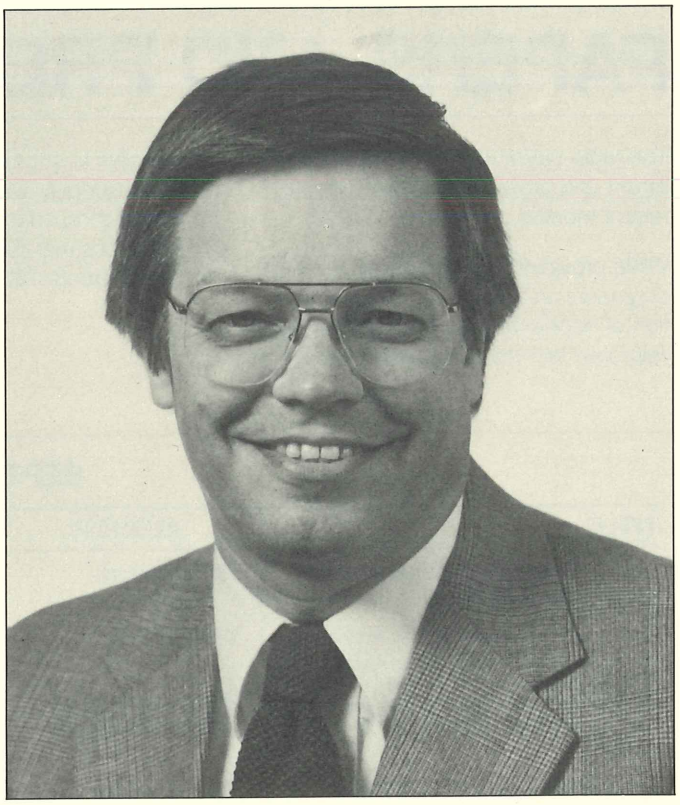


Roydn Jones

Roydn Jones is the manager of Hybrid Circuits Engineering. Roydn joined Tektronix in 1974 as a hybrid design engineer. He worked in the Instruments Divisions Advanced Development group, Applied Research, and was manager of instrumentation systems research prior to taking his current position in February of 1983.

Roydn was involved in microwave IC designs throughout the 1970s. He has also contributed to the development of charge-coupled device applications and liquid crystal displays. Prior to joining Tek, he worked five years for Hewlett-Packard in microwave hybrids. He is a member of ISHM and the Society for Information Display (SID).

Roydn's book, *Hybrid Circuit Design and Manufacture,* was sponsored by ISHM, and published in 1982 by Marcel Dekker, Inc., New York. The book relates materials science, ceramics technology, physics, chemistry, and electronic engineering to hybrid circuit design and manufacture. No other book so thoroughly details thick film and hybrid design and manufacturing.



Jim Keski

Jim Keski is a principal engineering scientist in Hybrid Circuits Engineering. He joined Tek as a project leader in ceramics in January 1970. In April 1973 was named manager, thick film engineering. He was made a ceramic engineering manager in December 1978 and in December 1980 became manager of Hybrid Process Development.

Jim has had many articles and papers published. Before Tektronix, he was a research ceramist for E.I. duPont de Nemours & Company. He is technical vice president of ISHM, and a member of the American Ceramics Society. □

PAPERS AND PRESENTATIONS

The table below is a list of papers published and presentations given during recent months.

While providing recognition for Tektronix engineers and scientists, the presentation of papers and articles contributes to Tektronix' technological leadership image.

If you plan to submit an abstract, outline, or manuscript to a conference committee or publication editor, take advantage of the services that Technology Communication Support (TCS) offers.

TCS provides editorial and graphic assistance to Tektronix engineers and scientists for papers and articles presented or published outside Tektronix and obtains patents and confidentiality reviews as required.

Call Eleanor McElwee on ext. MR-8924. □

SEPTEMBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
Video Frequency Measurements for TV Broadcasting	(Staff Report)	**Test and Measurement World**	
General-Purpose Ladder Analysis with the Hand-Held Calculator	Wes Hayward	**RF Design**	
Interactive Graphics Help Us Visualize Data, Communicate Results	Robert Anundson and David Squire	**Industrial Research and Development**	
Envelope Mode's Broad Field of View Spots 'Invisible' Problems	Clive Steward	**Electronic Design**	
Process and Device Performance of 1-μm-, Channel N-Well CMOS Using Deep-Trench Isolation Technology	Tad Yamaguchi Seiichi Morimoto Galen Kawamoto		1983 Symposium on VLSI Technology, Maui, Hawaii
Managing the Incoming Inspection Function	Theresa Cuchra		Electronic Insulation Conference, Chicago, IL

OCTOBER

TITLE	AUTHOR	PUBLISHED	PRESENTED
Measuring a Television System	William Montgomery	**Educational and Industrial TV**	
EMI Considerations in Oscilloscope Design	Pat Adamosky	**EMC Technology**	
Testing Devices for IEEE-488 Compliance	Steve Coan	**EDN**	
A Diagnostic Journey: High-Voltage Insulation Systems	Ben Schafer		Electronic Insulation Conference, Chicago, IL
A High-Resolution Color Display with Auto Convergence	Dan Denham Bill Meyer		SID Display Research Conference, Japan
A High-Resolution CRT for a Monitor with Auto-Convergence Features	David Bates Gary Nelson Ron Robinder (with A.V. Gallaro and G.N. Williams of Philips ECG)		SID Display Research Conference, Japan
A Novel High-Performance CRT with Meshless Scan Expansion	Ken Hawken Norm Franzen John Sonneborn		SID Display Research Conference, Japan

Design Considerations for the Pi-Cell	Phil Bos		SID Display Research Conference, Japan
The Display Marketplace Today and Tomorrow	Aris Silzars		SID Display Research Conference, Japan
Design Factors in a Programmable Distortion Measurement System	Richard Cabot		Audio Engineering Society Meeting, New York, NY
Design Criteria and Optical Performance of LC/CRT Color Displays	Tom Buzak		Electrochemical Society Meeting, Washington, DC
CRT Phosphor Selection for LC/CRT Displays	Ron Petersen		Electrochemical Society Meeting, Washington, DC
Reactive Ion Etching of N^+ Poly Silicon in a Sulfur Hexafluoride Plasma	Greg Eiden Eric Lane		Electrochemical Society Meeting, Washington, DC
Technology, Productivity, and Quality	John Ristow		Oregon Productivity Parade, Portland, OR
Color Graphics Hard Copy: Where Can Ink Jet Win?	Chuck Davis		IGC Ink Jet Conference, Boston, MA
An Automated Screen Line	Lee Vannice Mary Kyan Keith James Steve Boughton		Electrochemical Society Meeting, Washington, DC
Structured Logic Analysis for Manufacturing Testing	Bob Broughton		IEEE Int'l. Test Conference, Philadelphia, PA
VLSI Education at the Oregon Graduate Center	Kit Bradley		IEEE/ASEE Frontiers in Education Conference, Worcester, MA
State of the Art in Electronic Testing from Design to Final Inspection	John Ristow		Quality Expo, Los Angeles, CA
Computer-Aided Analysis of Forced-Air-Cooled Enclosures	Gordon Ellison		Int'l. Electronics Packaging Conference, Itasco, IL
Computer Tools for Thermal Analysis of Electronics	Gordon Ellison		Int'l. Electronics Packaging Conference (Panel Discussion), Itasca, IL
A GHz GaAs Digital-to-Analog Converter	George LaRue		GaAs IC Symposium, Phoenix, AZ
A Monolithic 10-GHz Vector Modulator	Eric Strid		GaAs IC Symposium, Phoenix, AZ
A High Yield GaAs Gate-Array Technology and Applications	Tim Flegal Ajit Rode George LaRue		GaAs IC Symposium Phoenix, AZ

Technology Report

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TEK ADOPTS NEW DRAFTING STANDARDS

All persons who deal with mechanical drawings need to be familiar with the new standard. In some cases, implementation will require education regarding new symbology, and/or Geometric Dimensioning and Tolerancing (GD&T). The previous version of ANSI Y14.5 included the principles of GD&T, but the potential for cost-of-quality improvements are such that it's advisable to be sure our education level is adequate.

A future *Agenda* article will list available educational resources.

Tektronix has adopted a new drafting standard, ANSI Y14.5M-1982. Use of the new standard has begun in some parts of the company, and company-wide use is expected to occur early in 1984.

A detailed description of the standard, its impact, and it's implementation is available from Technical Standards (627-1800, del. sta. 78-529).

STANDARDS REVIEW BOARD CREATED AT TEK

For many years Tek's management of standards has revolved around a large number of ad hoc groups. These groups have placed heavy emphasis on the technical and operational aspects of standards, sometimes at the expense of the managerial and business orientation needed for a good standards program.

A Standards Review Board (SRB) has been created to bridge the gap between those who create and use standards and those who are responsible for the overall business success of the company and its component parts. Board members have been named by division and business unit managers (or by their authorized representatives).

While I (Warren Collier) will chair the SRB initially, the board's authority and responsibility are tied to the appointing officers, not to myself or to CQA.

Most of the detailed work required to generate, review and implement standards will continue to be done by those who have contributed in the past. The SRB will focus on the overall process of generating, approving, revising and retiring standards; and the assurance that the process results in good business decisions and practices. It will also concern itself with the use and generation of external standards and local standards (i.e., business unit or divisional standards).

For more information on the SRB, contact Technical Standards (627-1800, del. sta. 78-529). □

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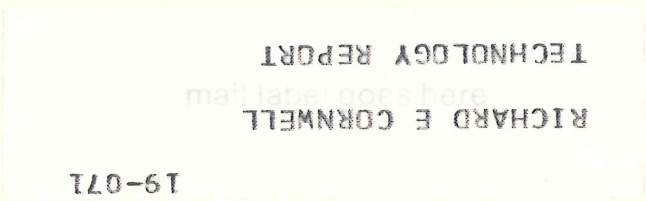

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