

**INTRODUCTION TO THE
7000 SERIES
SWITCHING AND LOGIC
CIRCUITS**

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Portions of this publication contain information which could jeopardize our competitive position if it were made available to people outside of the company. It is intended, therefore, that it be used only for "in-house" training purposes.

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Product Technical Information
January 1970

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PREFACE

An operator can choose any one of twenty possible display modes with the VERTICAL and HORIZONTAL MODE switches on the front panel of a 7000-Series mainframe. In addition, there are nine separate trigger options made available by the TRIGGER SOURCE switches. These capabilities are incorporated in the mainframe and provide the user with unparalleled flexibility of operation. The circuits which allow this can be divided into three sections:

1. Vertical and Horizontal Switches.
2. Logic which controls the switching operation.
3. Trigger Selection Circuit.

In this article, the above circuits are not discussed in detail. The intent is to provide a basic understanding of each major circuit in terms of the signals produced and their functions. The emphasis is on establishing relationships between a given CRT display and the circuits which produce it.

A circuit description is given for the Integrated Circuit switch (155-0022). This IC is a basic part of several circuits and a description is provided to give better understanding of its applications.

The section on MAINFRAME SWITCHING LOGIC is the most detailed. The reason becomes apparent when one considers all the possible operating mode configurations. Emphasis, again, is placed on describing what signals are produced, discussing their functions, and relating each to the front panel. The circuit description section of the 7504 manual gives a detailed account of the logic circuit. Each stage contained in the circuit is discussed in terms of positive logic. Truth tables are provided for all front panel operating modes.

CONTENTS

This article is divided into four major topic headings.
The topics, listed in the sequence to be covered, are:

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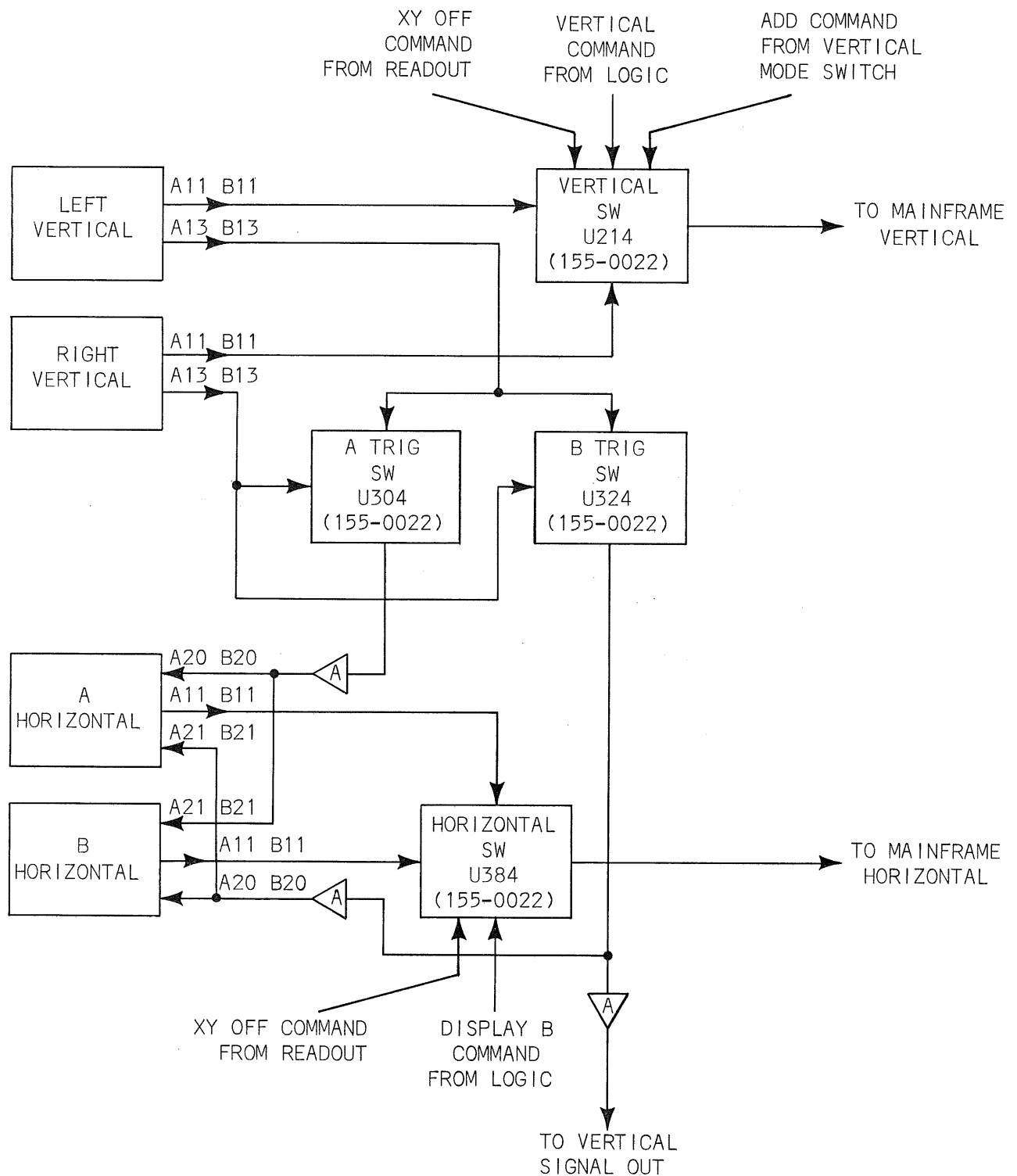


FIGURE 1. PLUG-IN AND TRIGGER SWITCHING BLOCK DIAGRAM.

BLOCK DIAGRAM DISCUSSION OF PLUG-IN and TRIGGER SWITCHING

Figure 1 is a simplified block diagram of the plug-in and trigger switches. The drawing shows only one line for a balanced pair of signals but both pin numbers on the plug-in connectors are given. The drawing is applicable to both the 7504 and the 7704, even though the 7704 differs by using discrete components for the vertical switch. The signal risetime through the IC switch is not fast enough for its use in the 7704. The 7504 uses the Tek-made IC (155-0022) for both plug-in switches and the trigger switches. In this discussion we will be referring to the 7504 configuration.

Notice that from each vertical plug-in there are separate pairs of signal leads for the trigger and vertical signal. Inputs to the VERTICAL IC SWITCH come from both the LEFT and RIGHT VERTICAL plug-ins. The output goes to the mainframe vertical amplifier. A command signal, determining which plug-in will be displayed, is derived from the logic circuit. Inputs from the readout circuit and the front panel VERTICAL MODE switch are also shown. The VERTICAL IC SWITCH and associated circuitry are located on the Vertical Interface Board.

The balanced outputs from the A HORIZ and B HORIZ plug-ins are directed through the HORIZONTAL IC SWITCH to the mainframe horizontal amplifier. The command signal that determines which plug-in is to be displayed is, again, derived from the logic circuit. The XY OFF COMMAND is an interrupt signal from the readout.

The trigger signal leads from each vertical plug-in are connected in parallel to two different integrated circuits. These IC's are only a part of the trigger select circuit and are located on the Trigger Select Board. In addition, the TRIGGER SOURCE and VERTICAL MODE switches on the front panel and two transistors located on the Main Interface Board, complete the trigger selection circuit. The Trigger selection circuit is covered later but, basically, the logic which directs the switching IC's may come from either the TRIGGER SOURCE or VERTICAL MODE switches, depending on the operating mode. The TRIGGER SOURCE switch furnishes the logic when either LEFT VERT or RIGHT VERT triggering is chosen. When VERT MODE is used, the VERTICAL MODE switch directs the operation of the trigger channel IC switches.

Referring again to Figure 1, the output from each of the trigger channel switches is fed through an amplifier stage to both the A and B HORIZ plug-ins. The A TRIGGER SWITCH directs its output to pins A20 and B20 of the A HORIZ plug-in. It also goes to pins A21 and B21 of the B HORIZ plug-in. In a like manner, the B TRIGGER SWITCH

directs its output to pins A20 and B20 of the B HORIZ plug-in and also to the A HORIZ plug-in through pins A21 and B21. This parallel arrangement is not used at present but is there to accommodate future time-base plug-ins that incorporate both a delaying and delayed sweep. For example, if a delaying/delayed time base were used in the A HORIZ plug-in, it would be possible to trigger the delaying sweep from the left plug-in and the delayed sweep from the right plug-in or vice versa.

THE INTEGRATED CIRCUIT SWITCH (155-0022) and ITS APPLICATION TO VERT and HORIZ SWITCHING

As is shown in the block diagram, this IC is used both for the plug-in switches and for the trigger switches. This Tek-made device is intended for use in circuits in which one, both, or none of two differential analog signals are to be processed. It performs this function in response to a digital input. One could think of it as a double-pole double-throw selector of one of two balanced input signals.

The three basic functions performed are:

1. Channel Selection -- Either Channel 1 or Channel 2 analog signals are transferred to the output.
2. Add -- The sum of Channel 1 and Channel 2 analog signals are transferred to the output.
3. Off -- No analog signal transferred to the output.

A schematic diagram of the IC is shown in Figure 2. It is designed for two balanced input signals of 25 mV/div per side into 50 Ω per side (.5 mA/div). The 50- Ω terminations to ground are external to the package. Pins 2 and 15 are the inputs for Channel 1 and pins 7 and 10 are for Channel 2. Each pair of inputs drives a differential common emitter amplifier. For Channel 1, pins 1 and 16 are connected to an external power supply that furnishes a DC bias of 7.5 mA per side. Pins 8 and 9 serve the same purpose for Channel 2. The signal output is taken from pins 12 and 13. The signal drive at these outputs is a current which rides at approximately a +5 volt DC level. Side-to-side diodes are included inside the IC for limiting the differential voltage swing of the output. A current gain of 1 is intended with this arrangement; the actual gain being determined by the external circuit. Total dynamic range for this IC is ± 7.5 mA which gives a ± 15 division total dynamic range. The risetime of the switch is less than 1 nanosecond.

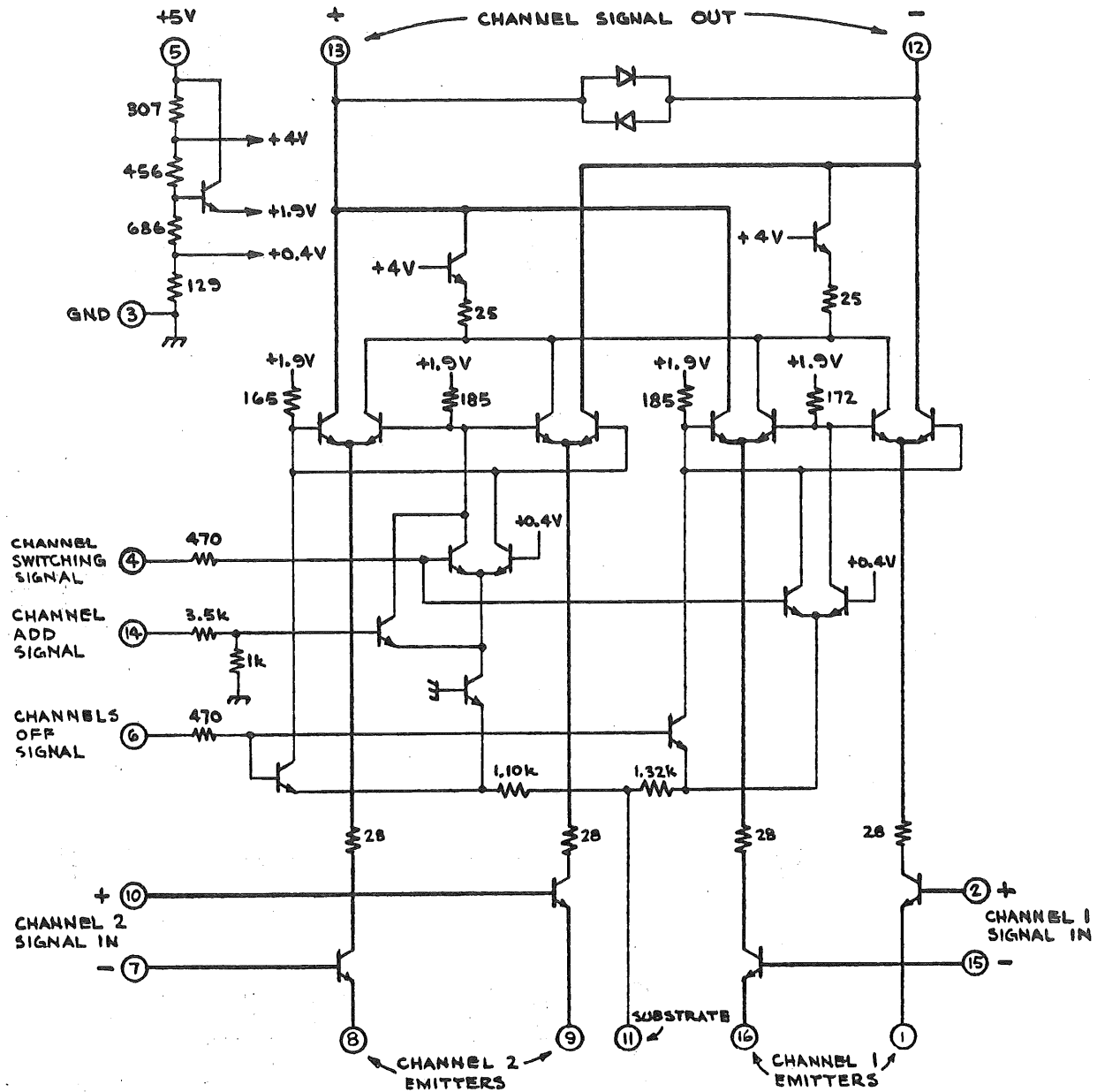


FIGURE 2. M036 CHANNEL SWITCH.

FIGURE 3.

There are three signal selection inputs -- pins 4, 6 and 14. The logic input at pin 4 provides high speed switching between the two signal input channels. It can accommodate switching frequencies of 1 MHz or greater. A LO (-.5 volts) at pin 4 selects Channel 1 and a HI (+1 volt) selects Channel 2. These binary instructions are either the VERTICAL MODE COMMAND or the DISPLAY B COMMAND, depending on whether the IC is the vertical switch or the horizontal switch. For either case, the signals are originated in the Logic Circuit.

The OFF input (pin 6) inhibits both signal inputs from reaching the output. The logic levels are the same as for pin number 4 with a HI inhibiting both signal inputs and a LO permitting the selected input to reach the output. When used as the Vertical or Horizontal switch, pin 6 receives instructions from the SCALE FACTOR logic to turn off the X and Y channels before readout information is to be displayed. The logic signals appearing at this pin supersede whatever states the other two inputs are in.

The ADD input (pin 14) requires a HI (+5 volts) to combine the two input signals at the output terminals. The LO state is 0 volts. In addition to requiring +5 volts at pin 14 to add the two signal inputs, a LO must be present at pins 6 and 4. The ADD instruction comes direct from the VERTICAL MODE switch whenever the ADD MODE is used.

Figure 3 is a partial schematic of the Vertical Interface Circuit. It shows the vertical switch and associated circuitry designed to accommodate VERTICAL TRACE SEPARATION. Briefly, the DISPLAY B COMMAND goes HI when the B plug-in displayed (with HORIZONTAL MODE in ALT or CHOP). This forward biases Q273 and furnishes a constant current to Q254 and Q256, which can then be controlled by the TRACE SEPARATION CONTROL (R1045). If the HORIZONTAL MODE is in B, then a HI is present at the base of Q283, turning it on and turning Q273 off, which disables the TRACE SEPARATION control.

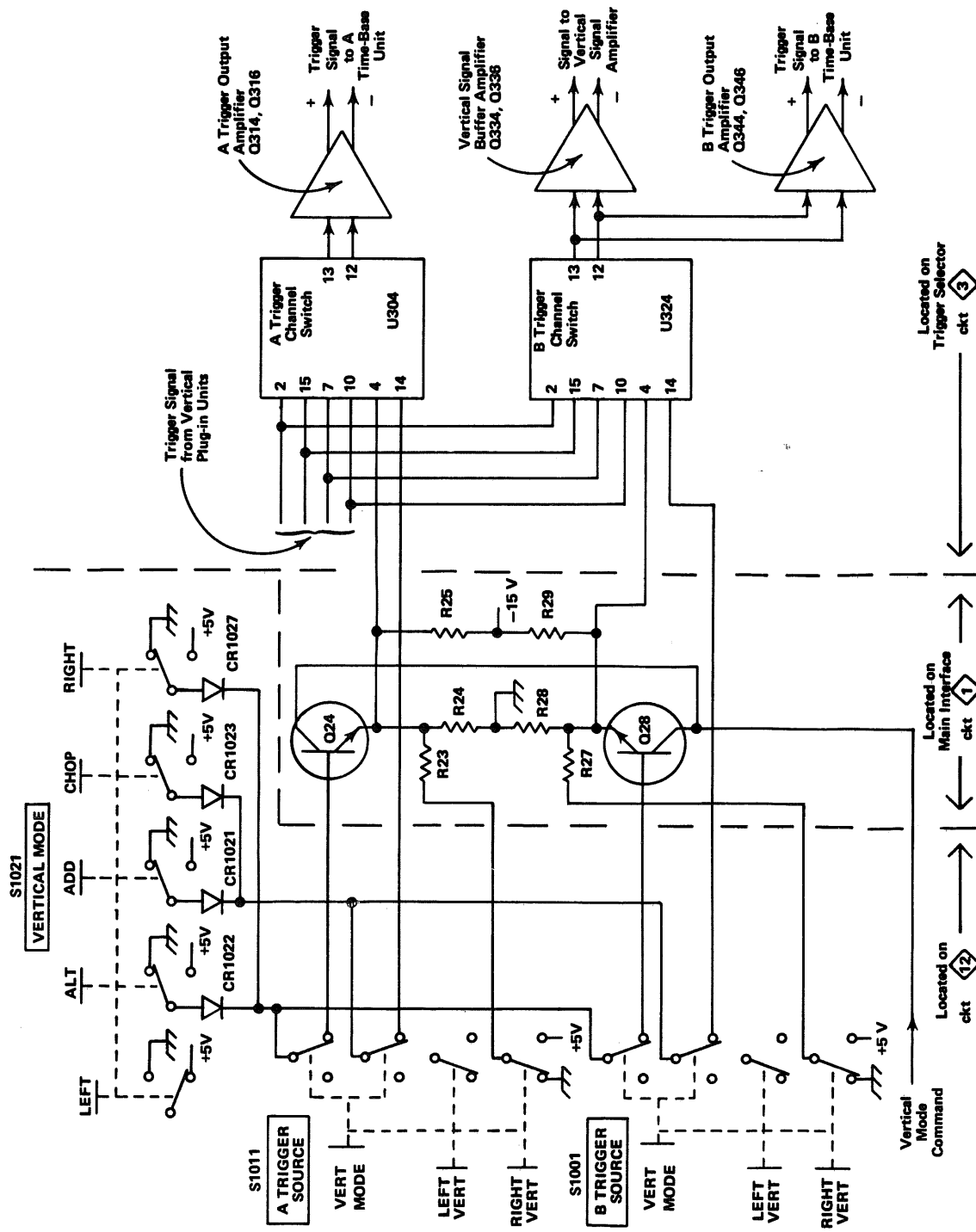


FIGURE 4.

THE TRIGGER SELECTION CIRCUIT

A simplified schematic of the trigger selection circuit is shown in Figure 4.

U304 and U324 are the same type IC as used for the Vertical and Horizontal switches. Pins 2 and 15 are the left vertical trigger inputs and pins 7 and 10 are the right vertical inputs. A LO at pin 4 passes the left vertical trigger signal and a HI passes the right vertical trigger signal to the output terminals. A HI at pin 14 on either IC will pass both the right and left vertical trigger signals added together. For the trigger switches, the OFF input, pin 6, is not used.

Notice that if the VERTICAL MODE is in either ADD or CHOP and if VERT MODE triggering is used, a HI (+5 V) is applied to pin 14 of the appropriate IC, which adds the left and right vertical trigger signals. This arrangement prevents the time-base trigger circuits from seeing either the mainframe or plug-in chop signal.

Two transistors, Q24 and Q28, located on the Main Interface Board, have their bases connected, through the A and/or B TRIGGER SOURCE switches, to the VERTICAL MODE switch when the VERTICAL MODE is in ALT or RIGHT and when the TRIGGER SOURCE is in VERT MODE. For example, the base of Q24 is connected to +5 volts when the VERTICAL MODE switch is in either ALT or RIGHT and when the A TRIGGER SOURCE switch is in VERT MODE. Likewise, the base of Q28 is connected to the same voltage whenever the B TRIGGER SOURCE switch is in VERT MODE. In this configuration, the transistors are saturated. For vertical ALT, the collectors receive the VERTICAL MODE COMMAND signal from the logic circuit in addition to the +5 V on the bases. Although the transistors are saturated, the emitter level remains dependent on the collector level. A HI at the collectors will be transferred to the emitters and to pin 4 of both IC's. This results in the right vertical signal being selected as the trigger at the same time it is displayed on the CRT. A LO at the collectors results in a LO at pin 4 of both switches which selects the left vertical signal. When two vertical amplifiers are used with a single time base, the logic level changes state at the end of each sweep when the VERTICAL MODE switch is in ALT. This instructs the trigger switch to alternately select the left and right plug-in trigger signal.

The schematic in Figure 4 shows the VERTICAL MODE switch in the LEFT position and both TRIGGER SOURCE switches in VERT MODE. In this case, the bases of Q24 and Q28 are grounded and the transistors are turned off. This presents a low at pin 4 on both IC's and instructs the switches to pass the left vertical signal to its output.

In summary of the Trigger Selection Circuit, there are several operator considerations worth noting.

1. When either TRIGGER SOURCE switch is in VERT MODE and the VERTICAL MODE switch operated in ALT, the logic for the trigger switch is the same as that for the Vertical IC switch. If, in addition, the HORIZ MODE is CHOP, the result is an incompatible arrangement of display modes and trigger modes. There is no assurance that each successive sweep will be triggered from the same vertical plug-in. For this reason, the following rule should be noted; *When in vertical ALT and horizontal CHOP, use LEFT VERT position of B TRIGGER SOURCE and RIGHT VERT for the A TRIGGER SOURCE.*
2. When either or both TRIGGER SOURCE switches are in VERT MODE and the VERTICAL MODE switch is in either ADD or CHOP, the appropriate trigger switch receives an ADD instruction. This prevents the trigger circuit from triggering on the chop waveform when the VERTICAL MODE is in CHOP.
3. The output from the B TRIGGER SOURCE switch provides the signal to the SIGNAL OUTPUT connector on the front panel. This allows the operator to select which vertical output he wants with the B TRIGGER SOURCE switch.

MAINFRAME SWITCHING LOGIC

The logic circuit, comprised of seven integrated circuits, seven transistors, and a handful of components, is contained on one circuit board. The basic functions of the logic circuitry can be identified and listed as follows:

1. Provides command signals to the Vertical Channel Switch, Horizontal Channel Switch and Trigger Selection Circuit.
2. Provides CHOP and ALTERNATE drive signals to dual trace amplifiers.
3. Provides sweep inhibit signals for either the A or B Time Base Plug-ins.
4. Provides logic for correct steering of Z-axis signals from:
 - A. Time-base plug-in blanking circuits.
 - B. A and B intensity controls.
 - C. External Z-axis inputs.
 - D. Vertical and horizontal chopped blanking circuits.
 - E. Z-axis commands from the readout circuit.

The emphasis on the following discussion will be directed toward an explanation of the signals produced, their functions and their relationships to front panel operation.

First, the outputs from the logic circuit will be discussed in terms of:

1. Functions and distribution to other circuits.
2. Characteristics.
3. Considerations for operating modes and plug-ins used.

Following the discussion on the outputs, each block within the circuit will be discussed in terms of:

1. Its specific functions.
2. Its inputs/outputs.
3. Considerations for operating modes and plug-ins used.

A schematic diagram of the 7504 logic circuit is included with this article and will be the primary reference. For the purpose of this discussion, the schematic can be considered as a detailed block diagram.

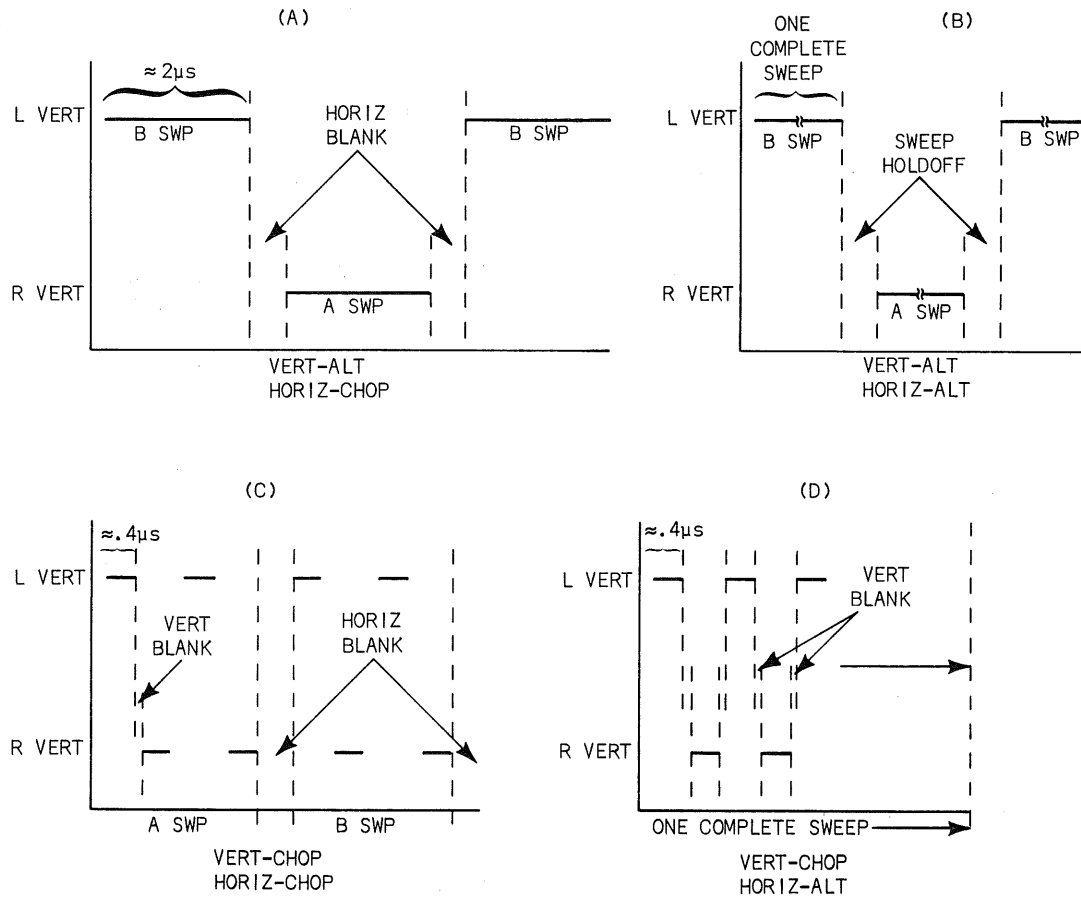


FIGURE 5. 2 SINGLE CHANNEL AMPS
2 TIME BASE UNITS (INDEPENDANT MODE)

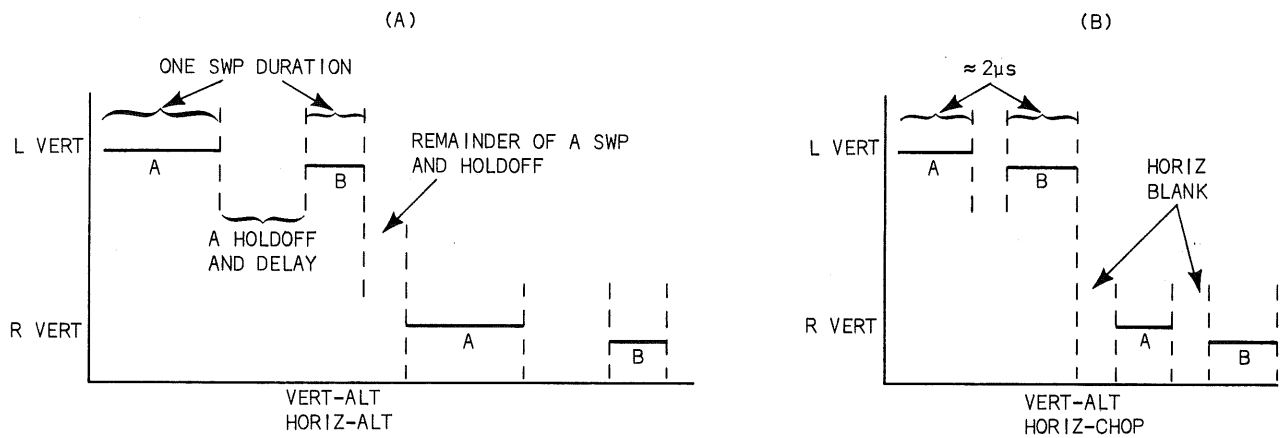


FIGURE 6. 2 SINGLE CHANNEL AMPS
2 TIME BASES (DELAYED SWEEP MODE)

LOGIC OUTPUTS

VERTICAL MODE COMMAND

Functions - This command pulse is used to switch the vertical plug-in display and to direct the trigger switching when the TRIGGER SOURCE is in VERT MODE and the VERTICAL MODE is in ALT. The signal is routed to the Vertical Switch IC and to the collectors of Q24 and Q28.

Characteristics - A binary signal with 5 volts being the HI state and 0 volts the LO state. The HI state will direct the RIGHT vertical to be displayed.

Considerations - The VERTICAL MODE switch selects one of two different binary signals to be the VERTICAL MODE COMMAND. In CHOP operation, the Vertical Chop signal (1 MHz from pin 1 of U130) is selected and routed through LR138, CR139, CR128, Q194 and Q196. When the VERTICAL MODE is in ALT, the output from pin 6 of the Vertical Binary (U180) is selected and routed through CR183, CR184, Q194 and Q196. The VERTICAL MODE COMMAND changes state at the end of each sweep (with Horiz ALT) or at the same time the DISPLAY B COMMAND switches (with Horiz CHOP).

The VERTICAL MODE COMMAND together with the DISPLAY B COMMAND produce display-switching sequences depicted in Figure 5A, B, C and D. Figure 5A and 5B are examples with the VERTICAL MODE in ALT and 5C and 5D are examples with CHOP operation. Notice, in Figure 5A and 5B, that the LEFT VERTICAL is displayed with the B HORIZONTAL and the RIGHT VERTICAL is displayed with the A HORIZONTAL. This "slaving" arrangement is significant in that it provides the equivalent of independent dual-beam operation for many measurement applications.

One additional consideration must be taken in obtaining the slaved condition -- the time base plug-ins must be operated in INDEPENDENT mode. If delayed sweep is used, the switching sequences are changed to that shown in Figure 6A and B. The reason for this arrangement is to allow each vertical plug-in to be displayed with both the A INTENSIFIED DURING B sweep and the B sweep alone.

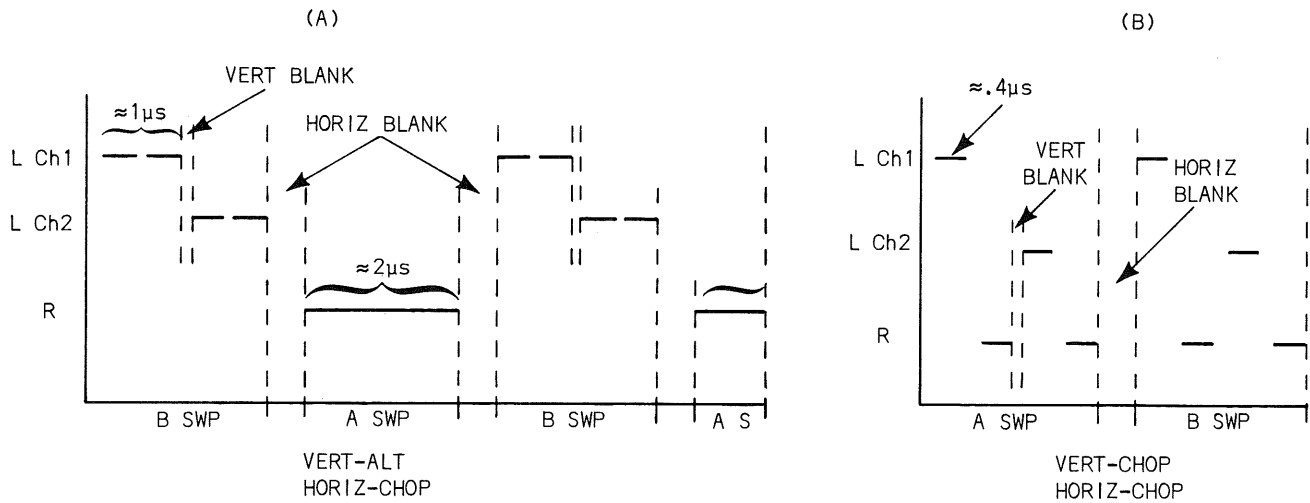


FIGURE 7. 1 7A12 (CHOP)
1 SINGLE CHANNEL AMP
2 TIME BASES

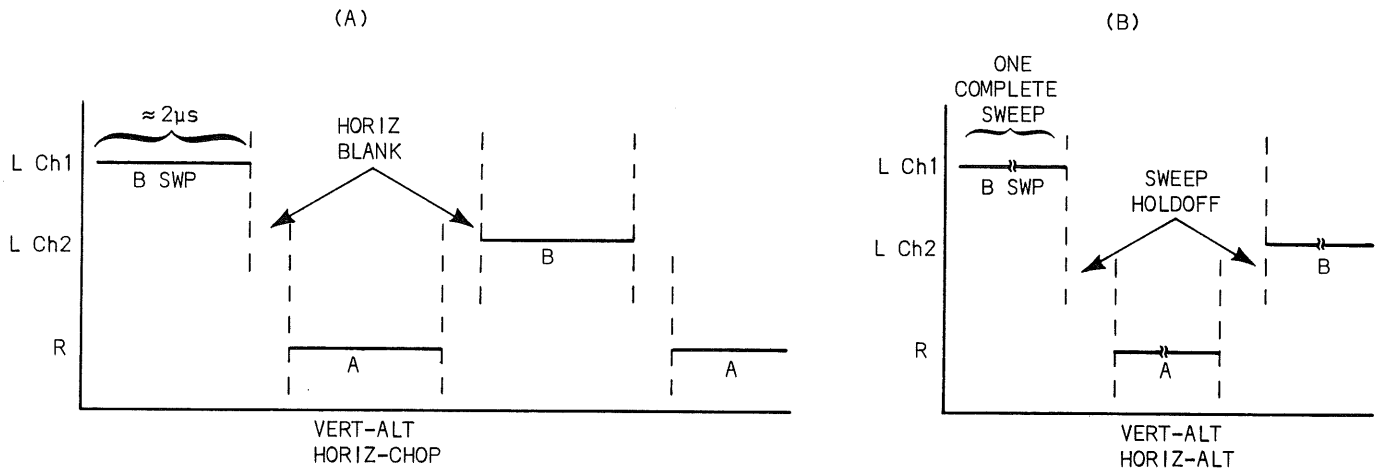


FIGURE 8. 1 7A12 (ALT)
1 SINGLE CHANNEL AMP
2 TIME BASES

PLUG-IN CHOP COMMAND

Functions - Provides the Chop driving signal to dual-trace plug-ins operated in CHOP. It is connected through the plug-in connector at both vertical plug-in compartments.

Characteristics - The signal is derived directly from pin 8 of the Chop Counter IC. It is a binary signal which switches at one-half the rate of the VERTICAL MODE CHOP signal. A HI selects channel 2 and a LO selects channel 1.

Considerations - The signal is always present regardless of mainframe operating mode or plug-in used. This insures that a dual-trace plug-in, operated in the CHOP MODE, will switch at approximately a 500-kHz rate, independent of mainframe operating modes. Figures 7A and B are examples of two arrangements using a 7A12 operated in CHOP.

This Chop drive signal is directed only to the vertical plug-in compartments; therefore, no Chop driving signal is available for dual-trace units operated in the horizontal plug-in compartments.

PLUG-IN ALTERNATE COMMAND

Functions - This signal serves as the alternate drive signal for dual-trace amplifiers when these amplifiers are operated in ALT. It is connected to all four plug-in connectors.

Characteristics - A binary signal in which a HI will display channel 2 of a dual-trace plug-in and a LO will display channel 1.

Considerations - The binary signal changes state at the end of each sweep for LEFT or RIGHT vertical operation in the mainframe. For Vertical ALT, the plug-in binary (U190) counts down by 2 and produces an alternate drive signal to a dual-trace plug-in which is one-half the rate of the mainframe alternate switching between vertical plug-ins. Figures 8A and B show switching sequences for different mainframe operating configurations. Both examples depict a 7A12 operated in ALT. Notice that in both examples, channel 1 of the 7A12 is "slaved" to the B Time Base and channel 2 is "slaved" to the A Time Base. This occurs in a dual-trace amplifier when it is ALT and the HORIZONTAL MODE is set to ALT or CHOP.

DISPLAY B COMMAND

Functions - A Logic command used to switch the horizontal plug-in display. It is also used in the trace separation circuit to provide additional vertical positioning during the time the B time base is displayed.

The signal is routed to the horizontal switching IC and to the Trace Separation circuit located on the vertical interface board.

Characteristics - A binary signal produced at pin 6 of the Horizontal Binary IC. A HI produces a display of the B Horizontal plug-in. A LO displays the A plug-in.

Considerations - When the HORIZONTAL MODE switch is in ALT, the command pulse changes state at the end of each sweep, thereby switching the horizontal plug-in display at the end of each sweep. The above statement assumes that two operating time bases are being used. If only one time base, or no time bases are operated in the horizontal compartments, the results are different. Before discussing what these differences are, it should be noted that the derivation of this command signal is the Holdoff waveforms, originating in the Time-Base plug-ins and appearing at pin 6 and 13 of U160. The Holdoff waveforms are differentiated at the inputs of U160 and used to generate an Alternate pulse at pin 8, which then drives pin 8 of the Horizontal Binary IC (U150). This IC, in turn, produces the DISPLAY B COMMAND signal at pin 6.

Consider the following plug-in arrangements with the HORIZONTAL MODE in ALT:

1. If a time base unit and an amplifier are used in the horizontal plug-in compartments, the single time base unit provides the holdoff waveform which directs the horizontal switching. The horizontal display will alternate between the time base and amplifier with the amplifier being displayed every other sweep for a duration of one sweep.
2. If only a single time base unit is used, and the other horizontal plug-in compartment left empty, no display is obtainable. This single time base is inhibited and the CRT remains blanked.
3. If two amplifier units are used in the horizontal plug-in compartments, again there is no display. There is no Time Base to generate the Holdoff waveform for this plug-in configuration.

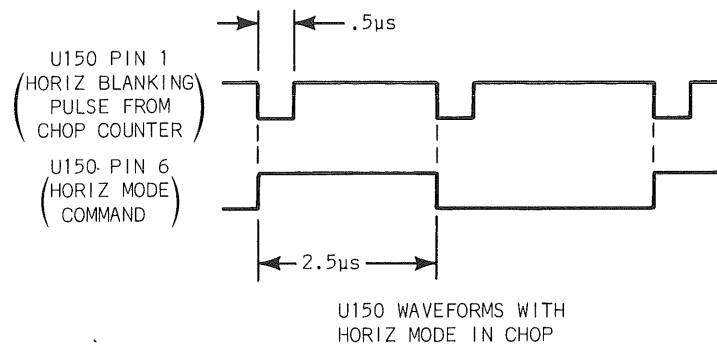


FIGURE 9.

If the HORIZONTAL MODE is operated in CHOP, a Horizontal blanking signal is developed at pin 4 of the Chop Counter (U130) and fed to pin 1 of the Horizontal Binary (U150). The signal is divided by 2 at the output of U150 (pin 6), and becomes the DISPLAY B COMMAND, switching at about a 200-kHz rate. The timing relationships are shown in Figure 9.

Horizontal CHOP provides the only means of obtaining a time-shared X/Y display between 4 amplifier plug-ins or a time-shared display between real-time and sampling plug-ins. There is no dependency, in the CHOP mode, on time-base plug-ins for generation of the switching signal. Display sequences, shown in Figures 5A and 5C, would apply for either of the above situations if the A and B SWP nomenclature were replaced by A and B AMPLIFIER.

A and B SWEEP INHIBITS

Functions - The function of both these logical signals is to develop a sweep lockout signal for the appropriate time-base unit. The A sweep lockout signal goes to the lockout circuitry in the A horizontal time-base unit and the B lockout pulse to the B horizontal plug-in unit.

Characteristics - Both of these outputs from U160 are binary signals with a HI in either case initiating sweep lockout.

Considerations - The A sweep receives a lockout instruction from U160 under the following operating conditions:

1. Horizontal Mode ALT. (Pin 1 HI.)
2. Both time bases in use and operated in INDEPENDENT. (Pins 4 and 5 HI; Pin 12 LO.)
3. During the time B sweep is displayed (Pin 16 HI.)

The B sweep receives a lockout instruction under the same conditions stated above except that it occurs during the time the A sweep is displayed (pin 16 LO.).

There is one other condition in which the A sweep may receive a holdoff instruction. When the time bases are operated in DELAYED MODE, A sweep is inhibited during the holdoff time of the B sweep if the A sweep has ended. In other words, if the A sweep (delaying sweep) has ended by the time the delayed sweep ends, then it is locked out until after the holdoff time of the delayed sweep.

Z-AXIS SIGNAL

Functions - The Z-axis output signal is an analog current which provides Z-axis drive to the Z-axis amplifier and CRT grid. Actually, the Z-Axis IC (U170) has several analog signal inputs. Separate logic inputs provide selection and steering for these analog signals. The functions of the Z-axis IC are:

1. Provides vertical and horizontal chop blanking signals to the Z-axis amplifier.
2. Provides the current drive determined by settings of the A and B intensity controls.
3. Processes the interrupt blanking signal from the readout circuit. This is a priority command signal and overrides any other existing Z-axis signal.
4. Provides intensity limit for slow sweep rates.

Considerations - When the time bases are operated in DELAYED MODE, an additional current is added to the A sweep Z-axis signal during the time B sweep runs and produces the intensified trace. This additional current level is set by R178, connected to pin 2 of the Z-axis IC. The intensity ratio between the intensified trace and the normal trace remains constant with this arrangement. For example, if the A INTENSITY control setting is changed to a higher level, the intensified level is increased proportionately.

The external Z-axis inputs on the rear panel and the auxiliary Z-axis connections from each plug-in are connected to the Z-axis IC at pin 9. The auxiliary Z-axis inputs are not used with present plug-ins.

An Intensity Limit circuit, comprised of R141-R142-R143-R144-R145-R140-R175 is automatically brought into play by either time base unit when slow sweep speeds are used. This circuit serves to prevent phosphor burning when the TIME/DIV control is suddenly changed from a fast to slow sweep rate. The effect is produced by grounding the junction of R143, R144 and R145, with the result of a reduction of available current to pins 7 and 9 of U170.

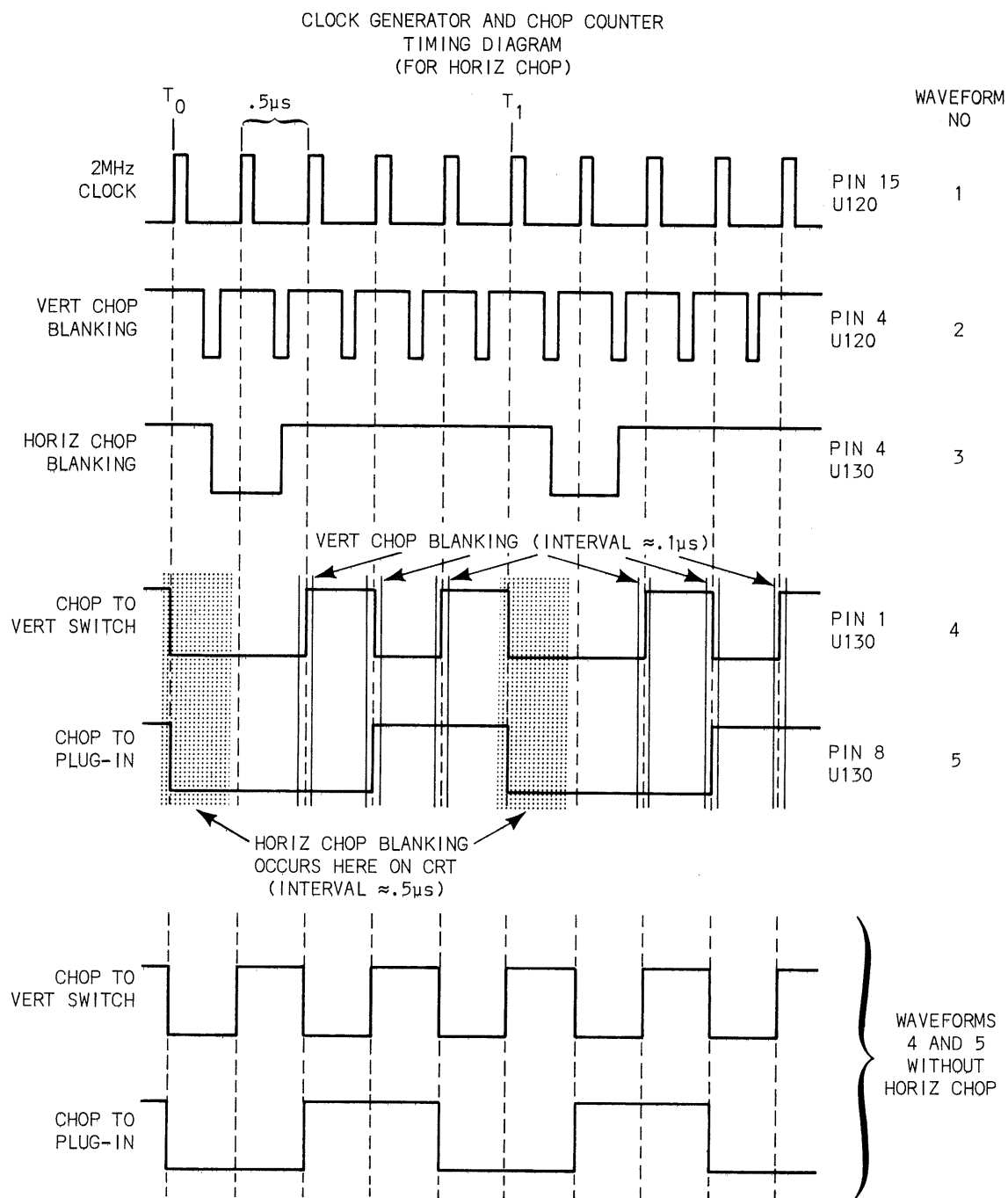


FIGURE 10.

LOGIC BLOCKS

Now, let's consider each stage contained within the logic diagram and discuss each in terms of:

1. Its basic functions.
2. Characteristics of Input/Output signals and their relationships to other circuits.

THE CLOCK GENERATOR (U120) and THE CHOP COUNTER (U130)

Functions - These two blocks together form the basic timing and correct switching sequences for mainframe and plug-in chopping. Refer to Figure 10 and to the logic schematic for the following description.

Inputs/Outputs - U120 contains two separate circuits: A free-running two-megahertz oscillator and a shaping circuit with delay network to generate the vertical blanking pulse. The two-megahertz clock signal appears continuously at pin 15 of U120.

The vertical chop blanking signal is brought out on pin 4 whenever the VERTICAL MODE is in CHOP or if a displayed Dual-Trace amplifier is operated in CHOP. It is basically the two-megahertz clock signal inverted and delayed. The signal is routed to pin 6 of the Z-axis IC (U170). The delay compensates for the delay line in the vertical signal path in the mainframe, allowing the blanking interval to occur at the correct time with respect to the CRT display.

The Chop counter (U130) receives the two-megahertz clock signal on pin 10 and produces three separate logic signals at its output:

1. Mainframe Chop signal - Pin 1
2. Plug-in Chop signal - Pin 8
3. Horizontal Chop Blanking signal - Pin 4

The mainframe vertical Chop signal is produced continuously on pin 1 but is connected to the base of the Q194 through CR139 and CR128 only when the VERTICAL MODE is in CHOP. In this mode, +5 V from the VERT MODE switch forward biases CR128 and CR139. The Plug-in Chop signal is produced on pin 8 and goes directly to both vertical plug-in connectors as the PLUG-IN CHOP COMMAND. The Horizontal Chop Blanking pulse is produced at pin 4 whenever Horizontal CHOP is used and is directed through pins 6 and 7 of the Z-axis IC and to pin 1 of U150. The signal at pin 4 of U130 acts as the source voltage for Q146 when pin 4 is HI. The emitter, in turn, goes HI and transfers the logic on to the Z-axis IC. A HI state at the inputs (pins 6 and 7 of U170) initiates unblanking.

Notice in Figure 10 that whenever the HORIZONTAL MODE switch is in any position except CHOP, both the mainframe Vertical Chop and the Plug-in Chop signals are symmetrical (bottom two waveforms). The mainframe Vertical Chop operates at a one-megahertz rate while the plug-in Chop signal is 500 kilohertz. If, however, Horizontal CHOP is used, these 2 signals are altered to that shown by waveforms 4 and 5. With Horizontal CHOP, waveform 3 is produced, resulting in the timing sequences of waveforms 4 and 5. Notice that the Horizontal Chop Blanking pulse is delayed to allow the blanking interval to occur at the correct time with respect to the CRT display.

Beginning at time T_0 , the switching of waveforms 4 and 5 is influenced by the presence of the Horizontal Chop Blanking signal in addition to the Clock signal. It now takes 5 clock pulses (from T_0 to T_1) to complete two cycles of waveform 4 and one cycle of waveform 5. Therefore, whenever horizontal CHOP is used, the vertical Chop rate is 2/5 of the master clock rate and the plug-in Chop rate is 1/5 the clock rate. The displayed segments on the CRT, however, remain approximately the same as without Horizontal CHOP because of the Horizontal CHOP blanking interval. In other words, referring to waveforms 4 and 5, each displayed segment of the vertical plug-ins remains approximately .5 μ s. Also, the displayed segments of each channel in a dual-trace amplifier remains approximately 1 μ s. It may help to relate the waveforms discussed here to the switching diagrams shown in Figures 5C, 7A and 7B.

THE HORIZONTAL BINARY (U150)

Functions - This integrated circuit, as was mentioned earlier, produces the DISPLAY B COMMAND signal at pin 6 (a HI displays B and a LO displays A). In addition to being a direct output from the logic to the horizontal channel switch, the signal at pin 6 is routed to the Horizontal Logic IC, the Z-Axis Logic IC, and to the Vertical Binary IC.

Inputs/Outputs - The rate at which the output (pin 6) switches depends upon the operating mode of the HORIZONTAL MODE switch. In CHOP operation (pin 10 HI), the horizontal chop blanking signal, generated in U130, is applied to pin 1 and determines what the output will be. The output in this case divides the input signal by two, switching at approximately a 200-kilohertz rate.

When the horizontal mode is ALT, pin 10 goes LO. This instructs U150 to select the signal appearing at pin 8. The alternate pulse, developed in U160, is then applied to this input. The alternate pulse is generated at the beginning of holdoff time from either or both time bases. For this mode of operation the output of U150 changes state each time an alternate pulse occurs at pin 8. Refer to Figure 11 for DISPLAY B COMMAND timing relationships with the HORIZONTAL MODE in ALT or CHOP.

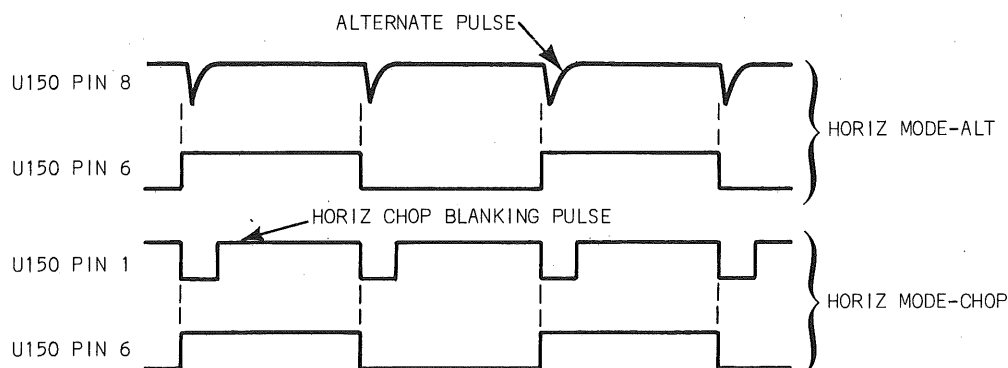


FIGURE 11.

If the horizontal mode is in A or B, a HI is applied respectively to either pin 3 or to pins 4 and 7. A HI at pin 3 produces a HI at the output and the B plug-in is displayed. A HI at pins 4 and 7 produces a LO at the output, resulting in the A plug-in being displayed.

THE VERTICAL BINARY (U180) and THE PLUG-IN BINARY (U190)

Functions - U180 generates a binary signal at pin 6 of its output and channels it to the vertical IC switch whenever the VERTICAL MODE switch is in ALT. The output of U180 also serves as the input to the Plug-in Binary IC (U190).

The output of the Plug-in Binary is the PLUG-IN ALTERNATE COMMAND to dual-trace plug-ins. Depending on the VERTICAL MODE switch, the output is either slaved directly with its input or divides the input by two.

Inputs/Outputs - U180 receives the DISPLAY B COMMAND signal on pin 8 at its input. This binary signal is also inverted by Q182 and applied to pin 7. A HI appears at pin 4 when the HORIZONTAL MODE switch is in either ALT or CHOP (nondelayed sweep operation only). When a HI does appear at pin 4, U180 is slaved to the Horizontal Binary IC. In other words, the output at pin 6 switches at the same rate as does the input at pin 8. Further, when the VERTICAL MODE switch is in ALT, a HI is applied to the junction of R183 and R192. This turns on CR183 and CR184 and allows the output from U180 to be passed through Q194 and Q196 to the output as the VERTICAL MODE COMMAND.

Thus, the necessary conditions for "plug-in slaving" (vertical ALT and horizontal ALT or CHOP) are a HI at pin 4 of U180 and a HI at the junction of CR183 and CR184. Figure 12 depicts the timing relationship between the outputs of U150 and U180 for slaved operation.

In vertical ALT, a HI also appears at the base of Q192. The HI state is inverted to a LO at its collector and at pin 4 of U190. With this condition, U190 receives the output from U180 and divides by two at its output. For any vertical mode other than ALT, pin 4 of U190 is HI. This results in the output of U190 being slaved to the output of U180. Refer to Figure 13.

If the vertical mode is in RIGHT, a HI is applied directly to the base of Q194 from the VERTICAL MODE switch. For a LEFT display, a LO exists at the base of Q194. Therefore, when the vertical mode is either LEFT or RIGHT, the VERTICAL MODE COMMAND is derived directly from the front panel VERTICAL MODE switch.

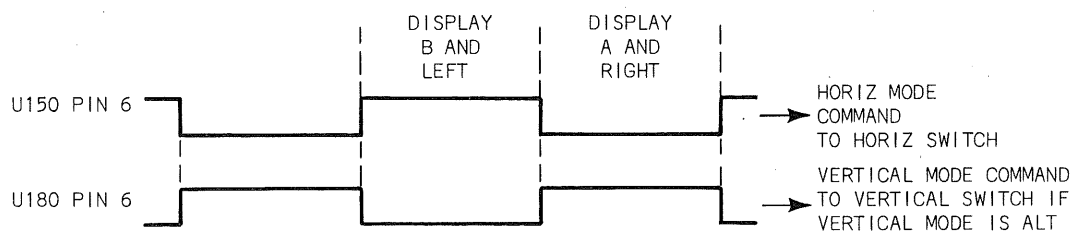


FIGURE 12. HORIZONTAL MODE (ALT OR CHOP).

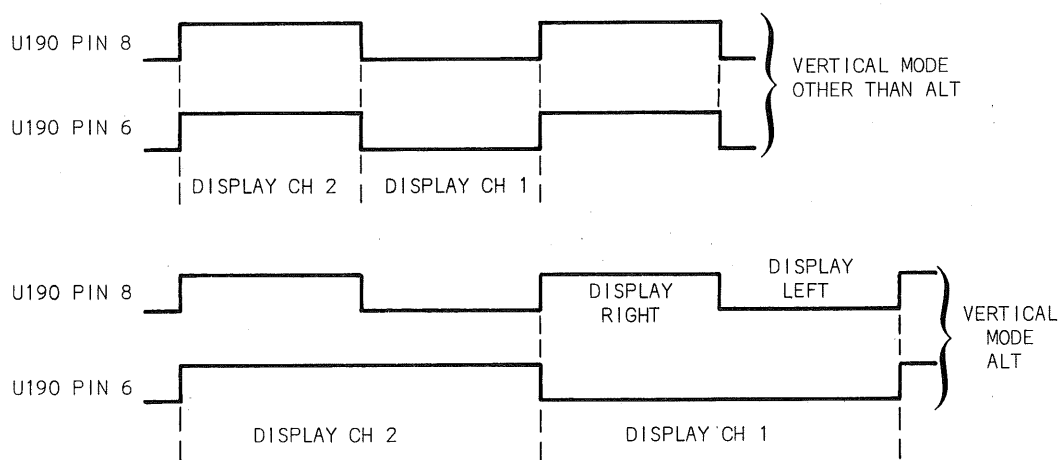


FIGURE 13. PLUG-IN ALTERNATE COMMAND WAVEFORMS.

Earlier, it was mentioned that in order to achieve slaving, the time bases must be operated in INDEPENDENT. This requirement is established by the state of the DELAYED MODE CONTROL line connected to the base of Q162. This line is HI whenever delayed sweep mode is used in the time bases. A HI turns on Q162 and produces a LO at pin 4 of U180 regardless of whether horizontal ALT or CHOP operation is used. A LO at pin 4 causes U180 to divide by two the signal at its input. Refer to Figures 6A and B for switching sequence examples of delayed sweep operation with mode switches in vertical ALT and horizontal ALT or CHOP.

THE HORIZONTAL LOGIC (U160)

Functions - The Horizontal Logic IC develops the A and B INHIBIT signals. The characteristics of these two signals were described earlier when the outputs from the Logic Circuit were discussed. In addition to the inhibit signals, this IC develops the alternate pulse at pin 8. This pulse may drive any one, any two, or all three of the following Binaries - U150, U180 and U190 (U190 is not driven directly -- it is indirectly driven through U180). This means the alternate pulse could direct mainframe vertical switching, mainframe horizontal switching, and dual-trace channel switching -- all at the same time. This would be the case if the mainframe modes were ALT/ALT and a 7A12 (or two 7A12's) operated in ALT.

The alternate pulse is a short duration pulse occurring at the leading edge of the holdoff waveform from either or both sweeps. The source of the alternate pulse is listed below for various operating configurations.

1. The A sweep and the B sweep when the horizontal mode is in ALT or CHOP.
2. The A sweep when the horizontal mode is in A.
3. The B sweep when the horizontal mode is B.
4. The A sweep only (horizontal mode ALT or CHOP) when time bases are operated in Delayed Mode.
5. The A sweep only (horizontal mode ALT or CHOP) when an amplifier is in the B compartment.
6. The B sweep only (horizontal mode ALT or CHOP) when an amplifier is in the A compartment.

The A sweep and B sweep holdoff waveforms appear at pins 6 and 13 respectively. This positive-going gate is differentiated by R165, R166, C165 and C166 at the inputs. The X COMPENSATION INHIBIT logic from the horizontal plug-ins is applied to pin 4 and pin 5 of U160. A HI exists at these inputs when time base plug-ins are used and are operated in the time-base mode. For example, if the horizontal mode is ALT with time bases being used, then both pins 4 and 5 are HI. This allows the alternate pulse to be generated at the end of each of the sweeps. If the horizontal mode is B, pin 7 of U160 becomes HI and with pin 5 being HI, the alternate pulse is generated from the B Time Base alone. Conversely, if the horizontal mode is A, then pin 10 is HI and, assuming the X COMPENSATION INHIBIT to be HI at pin 4, the alternate pulse is generated at the end of each A sweep.

Notice that the alternate pulse is also applied to pin 1 of U180. It should be noted that an alternate pulse is generated anytime there is at least one time-base unit operated in a horizontal compartment. (The one exception is when the other horizontal compartment is left empty and the horizontal mode set to ALT. See discussion on DISPLAY B COMMAND.) However, the alternate pulse serves as the input drive to U150 only when the horizontal mode is in ALT. For horizontal modes other than ALT, its function is to switch U180 and/or U190.

It was mentioned earlier that U180 furnishes the VERTICAL MODE COMMAND signal when the vertical mode is ALT. In addition, U190 drives dual-trace plug-ins when these units are operated in ALT. The alternate pulse instructs U180 to change states every time an alternate pulse occurs. Keep in mind that U190 is slaved to U180 for all vertical modes *except* ALT. If ALT is used, then U190 divides its input by two. Figures 14A and B depict two examples of switching sequences resulting from the alternate pulse driving U180. In Figure 14A, U190 is dividing by two and in 14B, U190 is slaved to U180.

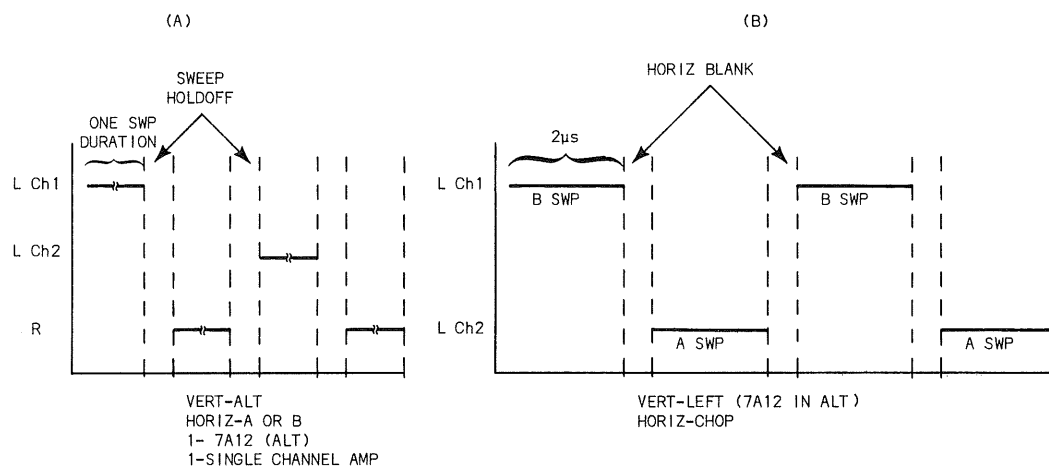


FIGURE 14.

THE Z-AXIS LOGIC (U170)

Functions - The single output of U170 (pin 8) was discussed earlier under the heading Z-AXIS SIGNAL. The signal appearing on this pin is an analog current which drives the Z-axis amplifier.

Inputs - The inputs to the Z-axis logic are as follows:

1. Pin 15 - The DISPLAY B COMMAND from pin 6 of U150.
2. Pin 6 - Both the vertical and horizontal chop blanking signals appear here. The HI state initiates unblanking and the LO state blanks.
3. Pin 4 - The B sweep gate waveform.
4. Pin 14 - The A sweep gate waveform.
5. Pin 5 - The DELAYED MODE CONTROL OUT signal from the A plug-in. A HI state indicates delayed sweep mode of operation.
6. Pin 7 - The horizontal chop blanking waveform and the intensity limit current.
7. Pin 9 - Intensity limit current and Z-axis information from rear panel inputs and plug-in auxiliary inputs.
8. Pin 16 - Current input from the A INTENSITY control.
9. Pin 2 - An additional current input selected only during the Intensified portion of the Intensified sweep.
10. Pin 1 - Current input from the B INTENSITY control.

Considerations - When the DISPLAY B COMMAND is HI at pin 15, and when the B gate waveform appears at pin 4, an input current determined by the setting of the B INTENSITY control is applied at pin 1 and steered to the output. Conversely, when pin 15 is LO and the A gate waveform appears at pin 14, then the current level determined by the A INTENSITY control at pin 16 is steered through the IC and appears at the output.

For either case above, two important additional requirements exist at pin 6. First, a HI must be present to initiate unblanking. During the vertical or horizontal blanking interval (LO state), both the A and B INTENSITY currents are gated off within the IC. Secondly, the Z-AXIS COMMAND from the readout circuit is applied to this input through Q146. The base of Q146 goes LO when the readout is ready to display a character. This turns Q146 off and presents a LO at pins 6 and 7 regardless of what states they would have been in otherwise.

At pin 9, various Z-axis current signals can be added to or subtracted from either or both the current levels supplied from the INTENSITY controls. The effect of the signals appearing at this pin is intensity modulation of whatever display is presented.

A HI is applied to pin 5 whenever the A time-base unit is operated in delayed sweep. A HI state here gates an additional parallel current path through R178 to pin 2 during the intensified portion of the delaying sweep. The combined currents at pin 16 and pin 2 are added at the output to provide correct Z-axis information to the CRT circuit.

