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A MONOLITHIC INTEGRATED CIRCUIT WIDEBAND OSCILLOSCOPE AMPLIFIER

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SUMMARY

Describes 29 dB, 600 MHz vertical output amplifier consisting of one 1.5 watt monolithic chip and two 1.5 watt discrete chip output transistors on Beryllium oxide substrate. Also includes circuit techniques, application and specifications.

INTRODUCTION

The vertical output amplifier in an oscilloscope amplifies signals from the delay line and drives the CRT. Ideally, this should be a low cost, high performance circuit. The circuit to be discussed is used in instruments with 200-250 MHz bandwidth. Older designs had the required performance characteristics, but were very expensive.

Taking the circuit performance requirements together with the available IC processes and devices, it will be shown how amplifying stages and circuit techniques were chosen to design an efficient, low cost circuit.

PRODUCT APPLICATION REQUIREMENTS

Since the initial design was done for the Tek 7704A Digital Processing Oscilloscope, and for the 475 Portable Oscilloscope, the input and output specifications were as follows:

The input signal comes from a push-pull 50 ohm delay line with a magnitude of 0.5 mA/division.

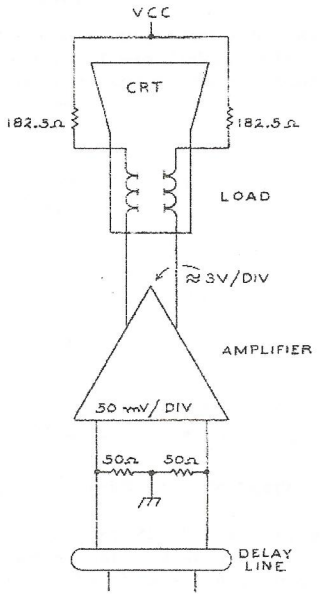

Figure 1 - Amplifier System

The output drives a CRT with a 365 ohm distributed vertical deflection system at about 3V/division with a dynamic range of ±9 divisions.

The nominal gains would then be:

Current gain 16.25
Voltage gain 59.31
Power gain 932.92 or 29.83 dB

In addition to the low frequency gain, extra gain is needed at higher frequencies (1) to compensate for high frequency losses in the 125 nsec delay line, at 3 dB/octave, a factor of two at 200 MHz, and (2) to compensate for the high frequency roll-off due to unavoidable amplifier output capacitance which shunts the 365 ohm CRT load.

The instrument bandwidth of dc to 250 MHz dictates that the output amplifier bandwidth must be about dc to 600 MHz.

Table I shows the more important instrument specs.

Table I

Instrument Specifications:

Bandwidth	-	dc - 250 MHz
Risetime - Aberrations	-	1.4 nsec, 3%
Gain Accuracy	-	2%
Gain Linearity (Low Freq)	-	0.1 division in a two division signal on-screen
Temperature Range	-	0°C to 50°C

IC PROCESS DEVICES

A monolithic process was available in-house with the following parameters:

f_T = 3.3 GHz
BV_{CBO} > 13 volts
LV_{CEO} > 6 volts

Emitters are 3.8 μm wide "washout", and will handle almost one milliamp per micron of length.

Diffused resistors (base diffusions) are:

p+ = 65 ohms/square
p- = 500 ohms/square

Thin film (nichrome) resistors are available on the chip with sheet resistance of 10 ohms/square, TCR 100 ppm/°C.

Discrete transistors with higher breakdown voltages are obviously needed to drive the high voltage swings at the CRT (almost 30 volts on each pin). Fortunately an in-house NPN transistor was available with adequate parameters:

BV_{CBO} > 50 volts
Typical f_T = 2.5 GHz at 160 ma

CIRCUIT DESIGN

One of the most stringent limitations on this

amplifier was producibility. Production was to begin at the rate of more than one hundred a day, at a time when our modest manufacturing facility was already operating near capacity. The design therefore, had to be simple and straightforward.

With the multitude of amplifier stages to choose from, what do we look for in an oscilloscope amplifier? An oscilloscope needs very flat, calibrated gain vs. frequency. In addition, the transient response should be clean and predictable with very little or no adjustment. The easiest way to satisfy these demands is to use stages that need not be squeezed to their maximum limit in gain-bandwidth product.

Space does not permit a complete discussion of all the alternatives considered. One example is given here to indicate the type of circuits examined in this project. The common emitter shunt feedback stage shown in Figure 2a was considered and rejected for the following reasons.

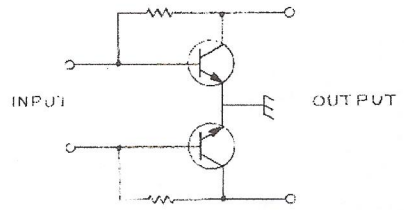

Figure 2a - Shunt Feedback Stage

The forward gain path contains several distinct time delays between the base current and the collector voltage response, i.e., extra phase shift at high frequencies. Excess phase shift is often used to trade delay for increased bandwidth. However, month to month processing variations could mean unpredictable high frequency response, requiring adjustments.

While the stage could undoubtedly be made to work adequately, it was judged inferior to the common emitter-common base cascode in this application.

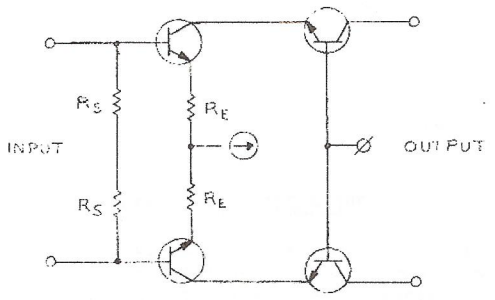

Figure 2b - CE-CB Cascode Stage

The cascode, see Figure 2b, has a very predictable high frequency response, particularly when made with thin film resistors in the chip - i.e., no bond wires. The emitter resistor produces the gain-setting feedback signal as soon as the input base current produces an emitter current. The output impedance of the common base transistors is high and only shunted by a small capacitance which is virtually constant with frequency. The input impedance is predictable even at high frequencies, resulting in a calibrated gain throughout the frequency range. The modification of the "f_T doubler" to this stage, Figure 3, made it a clear choice for our application because of its almost doubled gain bandwidth product compared to the standard cascode stage.

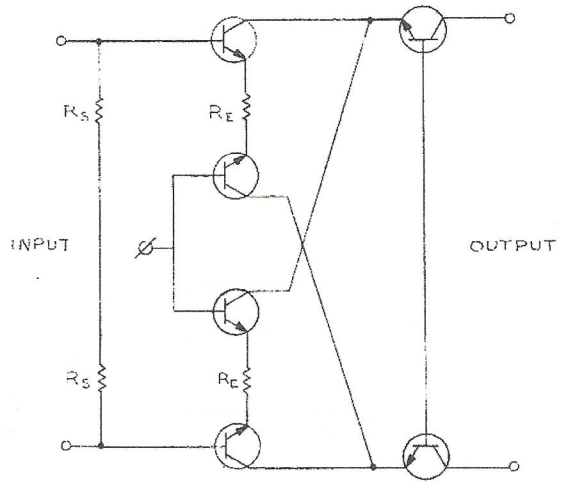

Figure 3 - f_T Doubler Cascode Stage

FUNCTIONS OF THE STAGES

Cascode stages can conveniently be considered in terms of current gain. In this case, the product of the current gains must be 16.25 at low frequencies. Additionally, high frequency gain boost is needed as outlined earlier.

The use of three stages (Figure 4) permits the last stage to have a reasonably high flat gain vs. frequency, while the two first stages have low gains at low frequencies. Then they won't run out of steam, i.e., gain-bandwidth product, as their gains are boosted at high frequencies.

The first stage must terminate the delay line in 50 ohms per side. The "f_T doubler" configuration is not used here because the large gain boost required for the high frequency loss of the delay line would require that the R-C circuits in the emitters be duplicated on both sides. Figure 4. Dynamic range is ±20 divisions.

The second stage is an "f_T doubler" because its high frequency gain boost can conveniently be achieved with inductors in series with the source resistor. The same source resistor is made variable to calibrate the overall gain of the amplifier. The inductors are also variable. Dynamic range is ±20 divisions.

The third stage has fixed gain vs. frequency except for small corrections of a few percent to compensate for thermal distortion. It has dynamic range of ± 9 to 10 divisions to allow a clean response even when fast signals are positioned to be displayed partially off-screen.

Since the total power dissipation on the chip is virtually independent of signals, all thermal distortion is fast enough to be conveniently compensated by electrical time constants, in this case, emitter RC circuits not shown. Thermal resistance between devices is very distributed, so six discrete RC time constants are needed for compensation. The total gain compensation is only a few per cent, so it is possible to

arbitrarily put three of the time constants on one side of the f_T doubler and three on the other side, rather than duplicating all six on both sides.

The common base transistors of this cascode drive the CRT, and are therefore discrete chips.

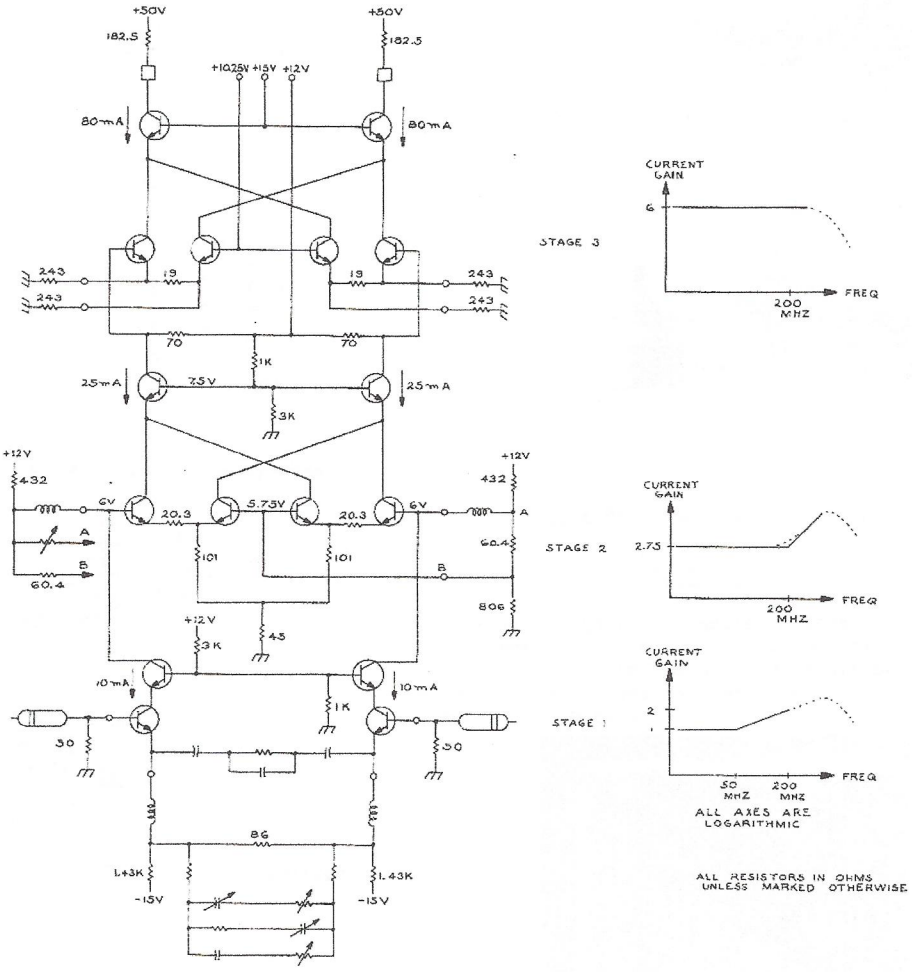

Figure 4 - The Complete Amplifier

SOME CIRCUIT TECHNIQUES

The first stage has external emitter resistors to better track the external delay-line compensation. This means bondwires (inductors) will be in series with the emitter resistors. A simple "constant resistance network" was synthesized to remove the effect of this bondwire. Figures 5 and 6.

The actual network in Figure 6 has too much junction capacitance (C_2 in Figure 5d), with high series resistance. Also, the resistance realized by the p+ diffusion (R_1 in Figure 5d), is very distributed. However, sensitivity analysis shows that as long as C_1 is correct, the other two are not very critical - within reasonable limits.

PACKAGING

The IC along with the discrete output chips is packaged on a BeO substrate in a modified TO-8 package. The modification consists of a copper stud heat sink brazed under the header, then bolted to the chassis in the instrument. This allows dissipation of 1.5 watts in the monolithic chip and 1.5 watts in each output transistor with a temperature rise of about 35°C junction to chassis.

Parkinson's law states that the number of wire bonds will grow until it consumes all the available pins. This circuit obeys Parkinson's law. The 16 standard pins of the package and the grounded stud provide the 17 leads required by the IC. See Figures 7 and 8 for a picture of the chip and header.

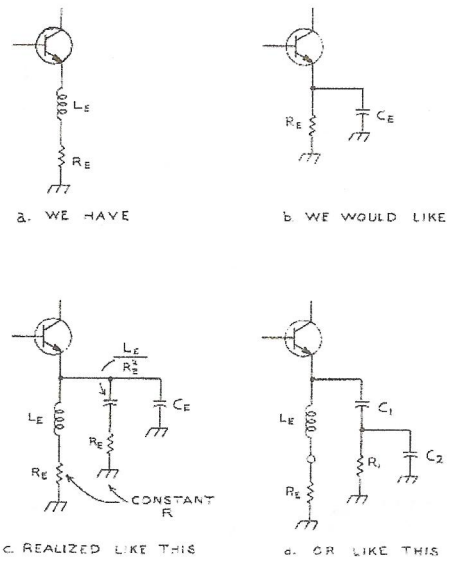

Figure 5 - Emitter Bondwire Cancellation Synthesis

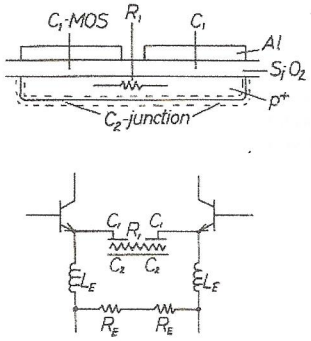

Figure 6 - Emitter Bondwire Cancellation Realized

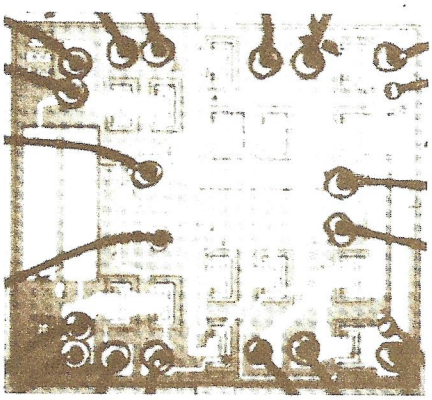

Figure 7 - The Integrated Circuit

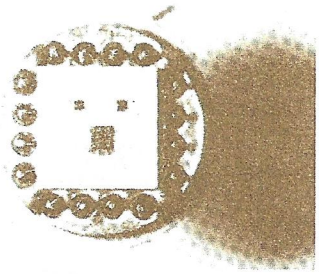

Figure 8a - Hybrid Substrate on TO-8 Header

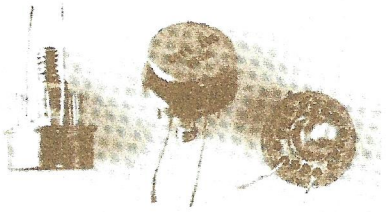

Figure 8b - Modified TO-8 Package

CONCLUSIONS

This design is currently in production. It routinely meets all specifications including its original cost goals. Figure 9 shows the result of the effort - a rather clean transient response. Figure 10 shows the frequency response.

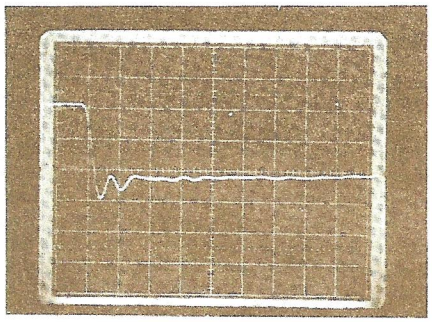

Figure 9a - Amplifier Alone (Source + CRT Risetime = 490 psec) 2ns/div

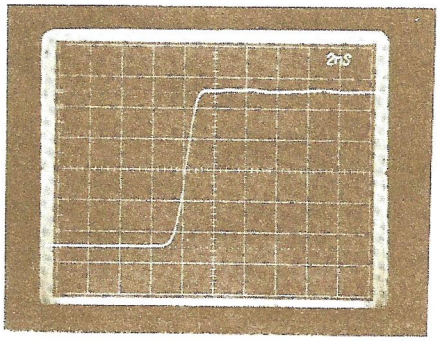

Figure 9b - The Whole Vertical Channel at 2ns/div

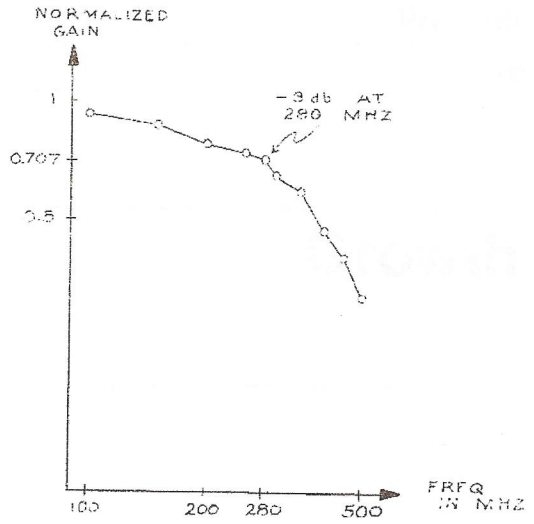

Figure 10a - Frequency Response of the 7704A Oscilloscope Serial #B101922

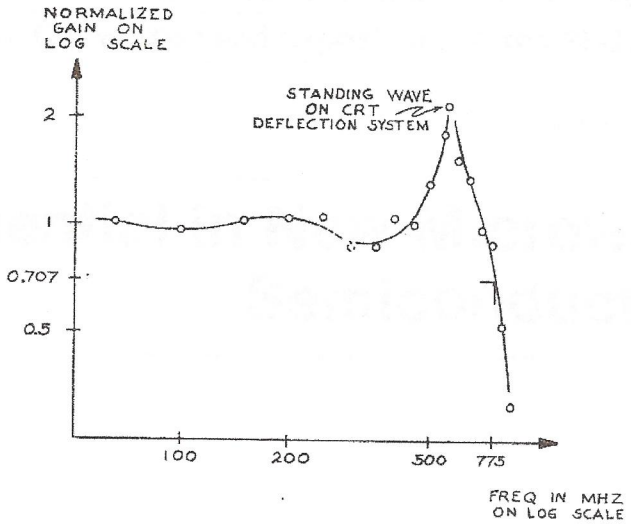

Figure 10b - Frequency response of the Amplifier and CRT Alone

ACKNOWLEDGEMENTS

The electrical design was done jointly by Jim Cavoretto and the author. The package modification was done by Conrad Chapple.