TEKTRONIX®

DF2
DISPLAY FORMATTER

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077
070-2478-00

Serial Number _____

First Printing JAN 1978

WARRANTY

All TEKTRONIX instruments are warranted against defective materials and workmanship for one year. Any questions with respect to the warranty should be taken up with your TEKTRONIX Field Engineer or representative.

All requests for repairs and replacement parts should be directed to the TEKTRONIX Field Office or representative in your area. This will assure you the fastest possible service. Please include the instrument Type Number or Part Number and Serial Number with all requests for parts or service.

Specifications and price change privileges reserved.

Copyright © 1978 by Tektronix, Inc., Beaverton, Oregon. Printed in the United States of America. All rights reserved. Contents of this publication may not be reproduced in any form without permission of Tektronix, Inc.

Portions of this document have been taken from IEEE STD 488-1975, Digital Interface for Programmable Instrumentation, with permission of the Institute of Electrical and Electronics Engineers, Inc.

U.S.A. and foreign Tektronix products covered by U.S. and foreign patents and/or patents pending.

TEKTRONIX is a registered trademark of Tektronix, Inc.

Contents

Page

LIST OF ILLUSTRATIONS ii
LIST OF TABLES iii
SAFETY INFORMATION iv

SECTION 1 GENERAL INFORMATION

Introduction 1-1
Glossary of Terms 1-1
Installation 1-2
Packaging for Shipment 1-2
Specifications 1-4
Standard Accessories 1-6

SECTION 2 OPERATING INSTRUCTIONS

Front Panel Controls 2-1
Internal 2-1
External 2-1
Basic Operating Instructions 2-4
Power-On-Mode 2-4
Display Modes 2-4
Timing Diagram Displays 2-4
Map Displays 2-4
State Table Displays 2-4
Menu Displays 2-8
Size and Position Adjustment . . . 2-8
Error Message Displays 2-8
Basic Functional Check 2-9
Setup Procedure 2-9
Timing Diagram Displays 2-9
Map Displays 2-9
State Table Displays 2-10
Front Panel Adjustments 2-11
Irregular Operating Symptoms 2-12

SECTION 3 DETAILED OPERATING INSTRUCTIONS FOR GPIB

GPIB Overview 3-1
General 3-1
Mechanical Elements 3-1
Electrical Elements 3-1
Functional Elements 3-2
GPIB Line Definitions 3-2
ATN (Attention) Messages 3-4
Interface Functions 3-4
Setup Procedure for GPIB Operation . . . 3-5
Full Display/First Trigger Selector of 7D01 Logic Analyzer 3-5
GPIB Adapter 3-5
Installation of GPIB Adapter 3-8
7D01 Front Panel 3-8
GPIB Acquisition and Display 3-8
General 3-8
Menu Display 3-8

Page

SECTION 3 DETAILED OPERATING INSTRUCTIONS FOR GPIB (cont.)

GPIB Display 3-8
GPIB Crt Display 3-10
Control Lines (Channels 4-7) . . 3-10
Data Bus Lines (Channels 8-15) 3-10
Device Dependent Messages . . . 3-13
User Definable Lines (Channels 0-3) 3-13
Secondary Functions of Display Push Buttons 3-15
GPIB Triggering 3-15
General Description and Features . . . 3-15
ATN (Attention) Message Triggering . 3-16
Triggering on Any ATN Message . . 3-16
Triggering on Any ATN Message Group 3-16
Triggering on A Specific ATN Message 3-18
NON-ATN Message Triggering 3-20
Triggering on Any NON-ATN Message 3-20
Triggering on A Specific NON-ATN Message 3-20
Control Line Triggering 3-20
GPIB Timing 3-21
Correct Handshake 3-21
Asynchronous Triggering 3-21
Time Measurements 3-23
Error Message Display 3-27
Requires 16 Channel Mode 3-27
Irregular Operating Symptoms for GPIB 3-28
GPIB Applications 3-29
Procedure 3-29
Possible Causes 3-29
GPIB Functional Check 3-30

SECTION 4 DETAILED OPERATING INSTRUCTIONS FOR ASCII

ASCII Acquisition and Display 4-1
General 4-1
Menu Display 4-1
ASCII Display 4-1
ASCII Crt Display 4-1
Secondary Functions of Display Push Buttons 4-6
ASCII Triggering 4-8
8 Channel ASCII Triggering 4-8
16 Channel ASCII Triggering 4-8
Trigger Word 4-9
Negative Logic ASCII Triggering . . . 4-10
Error Message Display 4-10
Requires 8 or 16 Channel Mode . . . 4-10
Irregular Operating Symptoms for ASCII 4-11
ASCII Functional Check 4-12

WARNING

THE REMAINING PORTION OF THIS TABLE OF CONTENTS LISTS THE SERVICING INSTRUCTIONS. THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CALLED OUT IN THE OPERATING INSTRUCTIONS UNLESS QUALIFIED TO DO SO.

Page

SECTION 5 THEORY OF OPERATION

Front Panel 5-1
Data Acquisition 5-1
MPU, Program, and Data Storage 5-2
Vert and Horiz Display Output 5-2
Character Memory and Generator 5-3
Display Control and Z-Axis 5-3
Display 5-4
ROM Extension 5-4

SECTION 6 MAINTENANCE

Preventive Maintenance 6-1
Cleaning 6-1
Visual Inspection 6-1
Semiconductor Checks 6-1
Troubleshooting 6-2
Troubleshooting Aids 6-2
Troubleshooting Equipment 6-2
Troubleshooting Techniques 6-3
Troubleshooting With the System Text Fixture 6-4
Corrective Maintenance 6-14
Obtaining Replacement Parts 6-14
Soldering Techniques 6-14
Component Removal and Replacement 6-15
Circuit Boards 6-15
Push Button Switches 6-18
Semiconductors 6-19
Interconnecting Pins 6-19
Adjustment After Repair 6-20

SECTION 7 PERFORMANCE CHECK AND ADJUSTMENT

Preliminary Information 7-1
Adjustment Interval 7-1
Tektronix Field Service 7-1
Performance Check 7-1
Adjustment Procedure 7-1
Partial Procedure 7-1
Test Equipment Required 7-2
Index to Performance Check and Adjustment 7-3
Preliminary Procedure 7-3
Performance Check Procedure 7-4
Adjustment Procedure 7-8

SECTION 8 INSTRUMENT OPTIONS

Page

SECTION 9 REPLACEABLE ELECTRICAL PARTS

SECTION 10 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

SECTION 11 REPLACEABLE MECHANICAL PARTS

CHANGE INFORMATION

List of Illustrations

Figure No.		Page
Frontis-piece	DF2 Features	v
1-1	Attaching the DF to the 7D01	1-3
1-2	DF Dimensional Drawing	1-5
2-1	Location of the Readout Source Multi-pin Jumper	2-1
2-2	Front Panel Controls, Connectors, and Indicators	2-2
2-2 (cont)	Front Panel Controls, Connectors, and Indicators	2-3
2-3	Typical DF Display Modes	2-5
2-4	Typical Map Display Usage	2-6
2-5	Typical State-Table Display Showing Offset Between 7D01 and Reference State Tables	2-7
3-1	GPIB Connector	3-2
3-2	General Purpose Interface Bus Structure	3-3
3-3	Location of 7D01 Full Display/First Trigger Selector	3-6
3-4	GPIB Adapter	3-7
3-5	GPIB Operational Mode Display	3-9
3-6	Changing Trigger Word Readout in GPIB Operation	3-10
3-7	Typical DF GPIB Display Showing Disassembled Instructions in IEEE Standard 488-1975 Message Mnemonics	3-11
3-8	Hex and Binary to Mnemonic Message Conversion Table	3-12
3-9	Hex and Binary to ASCII Conversion Table	3-14
3-10	GPIB Handshake Timing Diagram	3-22
3-11	GPIB Handshake and ATN With Associated State Diagrams	3-24
3-11 (cont)	GPIB Handshake and ATN With Associated State Diagrams	3-25
4-1	ASCII Operational Mode Display	4-2
4-2	ASCII State Table Displays of Hex, Octal, and Binary Values	4-3
4-3	Changing Display Mode in ASCII Operation	4-4
4-4	Hex and Binary to ASCII Conversion	4-5
4-5	Octal to ASCII Conversion	4-6
6-1	Test Equipment Setup for Troubleshooting the DF Display Formatter	6-5

@

Figure No.		Page
6-2	Partial View of ROM Extension Board. Shows Pin Location and Indexing for Connection to the Interface Test Fixture	6-5
6-3	Location of Readout Source Multi-pin Jumper	6-9
6-4	Circuit Board Locations	6-16
6-5	Locations of Securing Screws on the Front Sub-Panel	6-17
6-6	Locations of Securing Screws on A2 Button Lights Circuit Board	6-17
6-7	Locations of Hex Securing Spacers and Wiring to be Disconnected on A1 Formatter Keyboard Circuit Board	6-18
6-8	Locations of Securing Screws on A3 Intelligence Circuit Board and A5 ROM Extender Circuit Board	6-18
6-9	Locations of Securing Screws and Hardware Mounting Screws on A4 Acquisition Circuit Board	6-19
6-10	Exploded View of Circuit Board Pin and Ferrule	6-20
7-1	Location of 7D01 Full Display/First Trigger Jumper	7-4
7-2	Test Setup for Performance Check and Adjustment Procedure	7-5
7-3	Hexadecimal State Table Display	7-6
7-4	Reset Out Check Test Setup	7-7

The illustrations in Section 10 are located near their associated diagrams on the foldout pages.

10-1	Semiconductor lead configurations.	
10-2	Circuit board locations.	
10-3	A1—Formatter Keyboard circuit board locations as viewed from front of instrument	
10-4	A2—Button Lights circuit board component locations as viewed from the component side of the board.	
10-5	A4—Acquisition circuit board component locations.	
10-6	A3—Intelligence circuit board component locations.	
10-7	Partial A4—Acquisition circuit board. Component locations as viewed from component side of the board.	
10-8	A4—Acquisition circuit board component locations.	
10-9	A3—Intelligence circuit board component locations.	
10-11	Partial A3—Intelligence circuit board. Component locations as viewed from the component side of the board.	
10-12	Partial A4—Acquisition circuit board. Component locations as viewed with board installed.	
10-13	Partial A3—Intelligence circuit board component locations.	
10-14	A2—Button Lights circuit board component locations, as viewed from component side of the board.	

List of Tables

Table No.		Page
1-1	Electrical Characteristics	1-4
1-2	Environmental Characteristics	1-5
1-3	Physical Characteristics	1-5
2-1	Irregular Operating Symptoms	2-12
2-1 (cont)	Irregular Operating Symptoms	2-13
2-1 (cont)	Irregular Operating Symptoms	2-14
3-1	Minimum Clock Pulses Required to Display Data	3-5
3-2	Irregular Operating Symptoms for GPIB	3-28
4-1	Secondary Functions of Display Push Buttons	4-7
4-2	Irregular Operating Symptoms for ASCII	4-11
5-1	Data Acquisition Address Decoder	5-1
5-2	Extended ROM Decoder	5-4
6-1	Error Messages and Responses	6-2
6-2	Hex to Binary Conversion	6-6
6-3	ROM Hexadecimal Output Program	6-7
6-4	Keyboard Circuit Checkout Procedure	6-7
6-5	Manual Clock Pulses Required to Control Button Lights	6-8
6-6	Formatter Readout Truth Table	6-10
6-7	Mainframe Readout Truth Table	6-10
7-1	Performance Check Description	7-1
7-2	Test Equipment	7-3

SAFETY INFORMATION

GENERAL

The following general safety information applies to all operator and service personnel. Specific warnings will be found throughout the manual where they apply and should be followed in each instance.

WARNING statements identify conditions or practices which could result in personal injury or loss of life.

CAUTION statements identify conditions or practices which could result in damage to the equipment or other property.

The word DANGER on the equipment identifies areas of immediate hazard which could result in personal injury or loss of life.

NOTES identify a procedure, condition, statement, etc., which may be essential for better understanding.

The following safety symbols may appear on the equipment.

CAUTION—Refer to manual

DANGER—High voltage

Protective ground (earth) terminal

Chassis ground

GROUNDING

To avoid electric shock, plug in the power cord with its grounding (earth) conductor before connecting to the instrument input or output terminals.

Do not defeat the grounding connections.

USE THE PROPER POWER CORD

To avoid electric shock and fire hazard, use only the power cord and connector specified for your instrument. Use only a power cord in good condition.

For detailed information on power connectors, see appropriate (operators, servicing) instructions.

USE THE PROPER FUSE

To avoid electric shock and fire hazard, use only fuses specified in parts list for your instrument, and identical in the following respects:

A. Type: Slow blow, fast blow, etc.
B. Voltage rating: 250 V, etc.
C. Current rating

Fuse replacement procedures, that require qualified service personnel to perform, are described in the Service portion of the appropriate manual.

Disconnect the power input before replacing the fuse.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERE

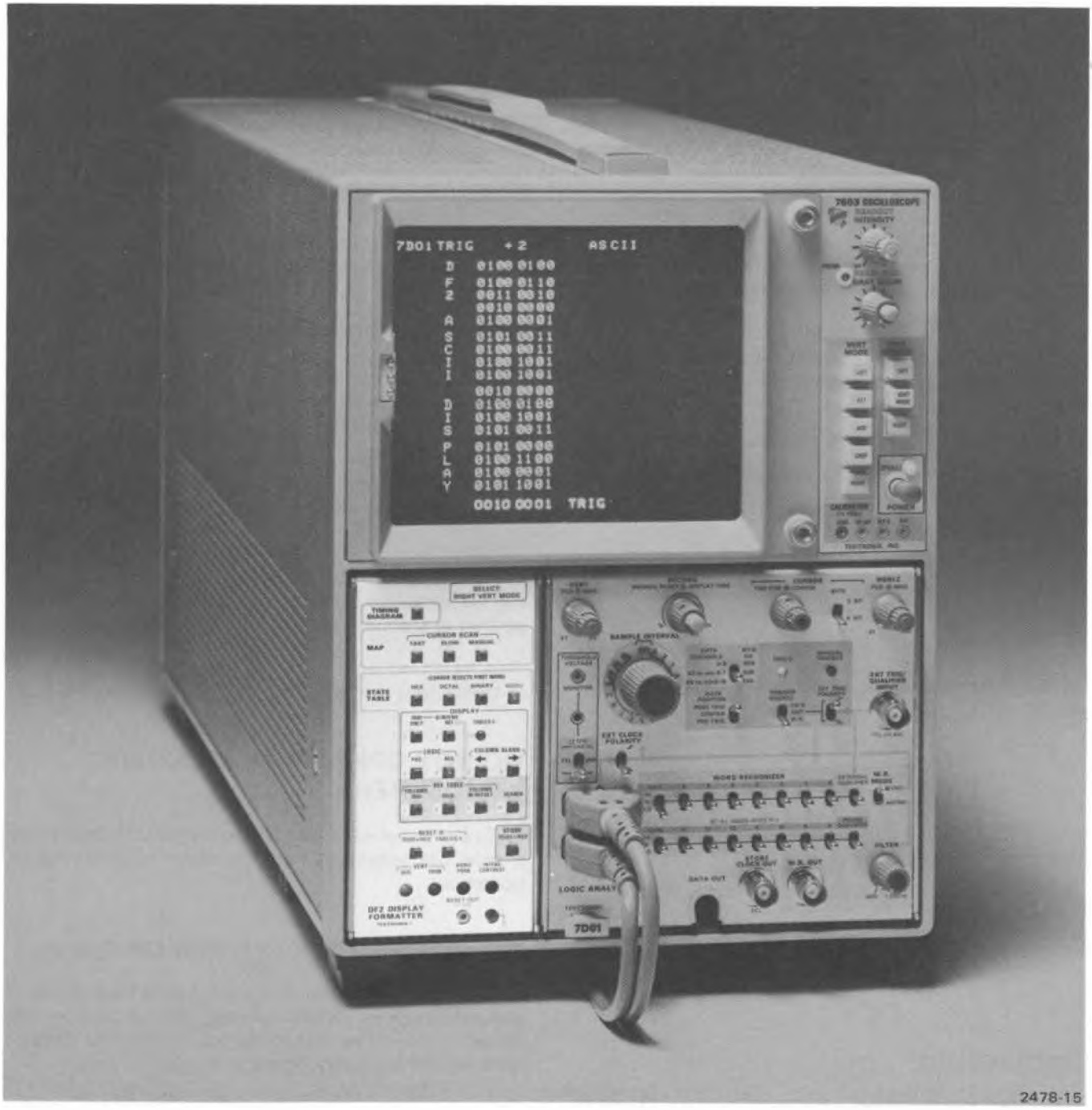
To avoid explosion, do not operate this instrument in an explosive atmosphere unless it has been certified for such operation.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not operate the instrument without covers or panels installed. Do not perform any servicing other than that contained in operating instructions unless you are qualified to do so.

DO NOT SERVICE ALONE

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.



DF2 FEATURES

The DF Display Formatter provides data-domain display modes in addition to the existing time-domain display of the 7D01 Logic Analyzer. It adds state table displays with a comparison mode, a map display and other operational modes as assigned to the Menu List. The DF attaches to the left side of the 7D01, forming a three-wide plug-in assembly. This assembly operates in a 7000-series oscilloscope mainframe to comprise a complete 16-channel logic timing-state analyzer system.

A microprocessor controlled memory system, contained in the DF, is capable of recording two 7D01 information records. Portions of both information records may be displayed concurrently in a state table presentation.

State tables are displayed in terms of either hexadecimal, octal, or binary formats. This data may be displayed in up to two tables of 17 lines of 16-bit words each. The left-hand table displays data currently stored in the 7D01 memory (7D01 display). The right-hand table displays data that has been transferred from previous 7D01 displays to the DF memory (reference display). The DF compares the 2 tables and resets the 7D01 when the 7D01 data equals the reference data.

The map function plots a dot display of the 16 data channels in X-Y coordinate points. Each dot location represents one possible combination of up to 16 inputs to the 7D01.

GENERAL INFORMATION

INTRODUCTION

The Instruction Manual contains eleven sections. Operating information is covered in the first four sections; servicing information is covered in the remaining seven sections. Schematic diagrams are located at the rear of the manual and can be unfolded for reference while reading other parts of the manual. The reference designators and symbols used on the schematic diagrams are defined on the first page of the Diagrams and Circuit Board Illustrations section. Abbreviations used in the manuals, except in the parts list and schematic diagrams, comply with the American National Standards Institute Y1.1-1972 publication. The parts list is a computer printout and uses computer-supplied abbreviations.

Throughout this manual the DF2 Display Formatter will be referred to as the "DF."

GLOSSARY OF TERMS

The following logic terms are used throughout this manual.

Asynchronous Mode—The data is acquired by the 7D01 using its internal clock at a rate selected by its sample interval control.

Bit—The smallest increment of digital information.

Blanked Columns—The columns eliminated from the memory by the COLUMN BLANK function.

Compare—A check between the 7D01 memory and the reference memory for equality (a microprocessor function.)

Data—This is information acquired by the 7D01. Up to 16 channels of data may be acquired, and each data bit is one clock period in the synchronous mode.

Data Record—All of the information stored in the 7D01 memory or the DF memory. (A Data Record has 4096 bits of information.)

Data Word—This is Good Data that may be formatted in any of three different ways:

1. A vertical slice of the Timing Diagram display.

2. A coordinate point of the Map display.

3. A horizontal line of characters in a State Table display.

NOTE

Channel 0 is the top-most channel displayed in TIMING DIAGRAM format and is always considered the least significant bit.

Don't Care Data—Invalid Data that is excluded from comparison in all comparison modes.

End Data—Data that fills out the last portion of a table when valid data ends before completion of the table. This is indicated by an "*" in the display.

Good Data—All data which is not Invalid Data.

Indeterminate Data—This is valid data but is considered invalid because its location cannot be defined. This data is indicated by an "X" in the display and occurs during sweep retrace in Timing Diagram. The number of Indeterminate Data bits for each position of the 7D01 bits/channel switch are: Two bits (254 bits/channel position), four bits (508 bits/channel position), and eight bits (1016 bits/channel position).

Invalid Data—This term describes a combination of Indeterminate Data, Old Data (if any), and End Data.

New Data—The most recent acquisition of Good Data into the 7D01.

Old Data—Data which was part of a previous Data Record in the 7D01 memory but is out of sequence. This is caused by the arrival of the trigger before the New Data has completely filled the memory. Old Data is indicated by an "X" in the display.

Reference State Table—A display of DF memory data transferred from a previous 7D01 display and displayed on the right half of the crt.

Synchronous Mode—The data is acquired by the 7D01 using an externally supplied clock signal (7D01 sample interval switch set to external, and with the external clock signal connected to the clock input of the channel 0-7 Data Acquisition Probe).

TABLE—This term refers only to the 17 lines of data displayed on the left or right sides of the crt an any one time. "TABLES-" refers to only the displayed data contained in the two tables and should not be confused with the total memory capacity.

Word—See Data Word.

INSTALLATION

The DF Display Formatter attaches to the left side of the 7D01 Logic Analyzer to make a three-wide plug-in system. The two units latch together to provide a rigid instrument that plugs into a 7000-series mainframe. Refer to Figure 1-1 to attach the DF to the 7D01.

CAUTION

To prevent instrument damage, plug-in units should not be installed or removed without first turning off the mainframe power.

To install the DF/7D01, first turn off the power to the oscilloscope mainframe. Then, gently push the 2 plug-in units into the appropriate plug-in compartments until they fit firmly. The front panels of the DF/7D01 should be flush with the front panel of the oscilloscope mainframe.

NOTE

When installed in a four-compartment mainframe, the DF/7D01 occupies the left vertical, right vertical, and A horizontal compartments only. The oscilloscope mainframe vertical mode switch must be set to right and the horizontal mode switch must be set to A.

To remove the DF/7D01, pull the release latch (located on the lower left corner of the 7D01) to disengage the DF/7D01 from the mainframe. Then, gently slide the plug-in units from the mainframe.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, it is recommended that the instrument be packaged in the original manner for maximum protection. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of an individual at your firm that can be contacted, complete instrument type and serial number, and a description of the service required.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a carton of corrugated cardboard with at least a 200-pound test strength and at least 6 inches larger than the instrument dimensions to allow for cushioning.

2. Surround the instrument with polyethylene sheeting to protect the instrument.

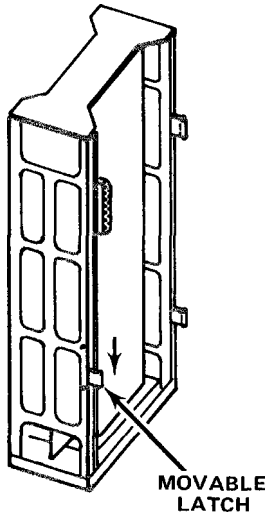
3. Allow a 3-inch cushion on all sides by tightly packing dunnage or urethane foam between the carton and the instrument.

4. Seal the carton with shipping tape or with an industrial stapler.

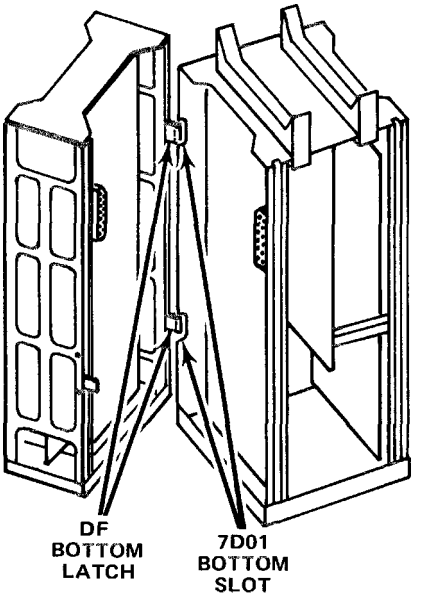
5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more locations.

DF/7D01 INSTALLATION

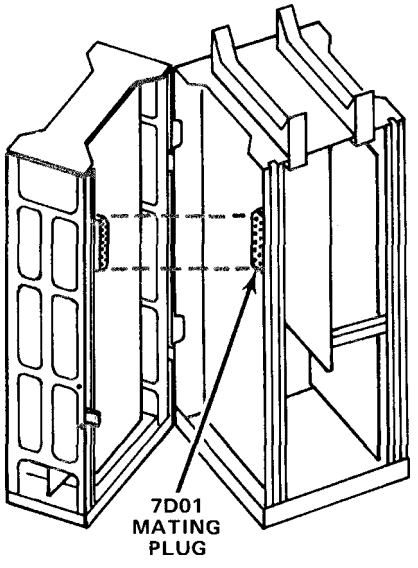
1. Slide the movable latch on the top of the DF forward until it stops.



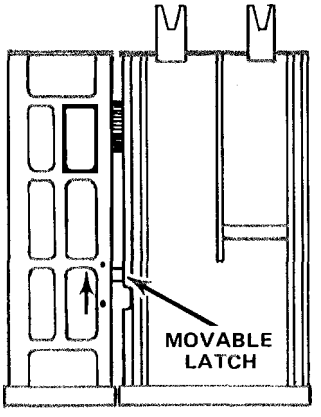
2. Tilt the DF and 7D01 slightly and place the bottom two latches on the DF into the bottom two slots on the 7D01. Gently slide the DF forward to just engage the bottom latches with the bottom track on the 7D01.



3. Continue to slide the DF forward until the jack at the top rear of the DF lines up with its mating plug on the 7D01.



4. Gently press the units together until the connector is properly mated and the movable latch is inserted into the rail slot on the 7D01.



Make sure the movable latch fits into the 7D01 rail groove and slide the movable latch toward the rear along the rail groove until it stops. The DF and 7D01 should now be latched together to form a rigid three-wide plug-in system.

(2150-10)2478-42

Figure 1-1. Attaching the DF to the 7D01.

SPECIFICATIONS

The electrical specifications listed in Table 1-1 apply for the DF/7D01 system under the following conditions: (1) the instrument must have been adjusted at an ambient temperature between +20° and +30° C (+68° to +86° F), (2) the instrument must be operating in an ambient temperature between 0° and +40° C (+32° and +104° F), and (3) the instrument must have been operating for at least 20 minutes.

TABLE 1-1

Electrical Characteristics

Characteristic	Performance Requirement
External Read Clock	
Frequency Range	100 kHz to 500 kHz.
Duty Cycle	50% within 5%.
Display	
Vertical Size	Adjustable from 6.9 div or less to at least 8.1 div from the top of the first line of DF readout to the bottom of the last line of DF readout.
Vertical Position	Adjustable to vertical center of display area in any calibrated 7000-series mainframe.
Horizontal Position	Adjustable to horizontal center of display area in any calibrated 7000-series mainframe.
Output Signals	
Reset Logic Voltage Level	LO: +0.4 V or less at 2 mA. HI: at least +2.4 V at 2 mA.
Waveshape	Positive-going rectangular pulse.
Duration	100 μs within 50 μs when used with the 7D01 internal read clock.

TABLE 1-2

Environmental Characteristics

Characteristic	Performance Requirement
Temperature	
Calibration	+20° to +30° C (+68° to +86° F).
Operating	0° to +40° C (+32° to +104° F).
Storage	–55° to +75° C (–67° to +167° F).
Altitude	
Operating	To 15,000 feet.
Storage	To 50,000 feet.
Transportation	Qualified under National Safe Transit Committee Test Procedure 1A, Category II.

TABLE 1-3

Physical Characteristics

Characteristic	Description
Net Weight	Approximately 2 lbs (0.9 kg).
Overall Dimensions	See Figure 1-2, Dimensional Drawing.

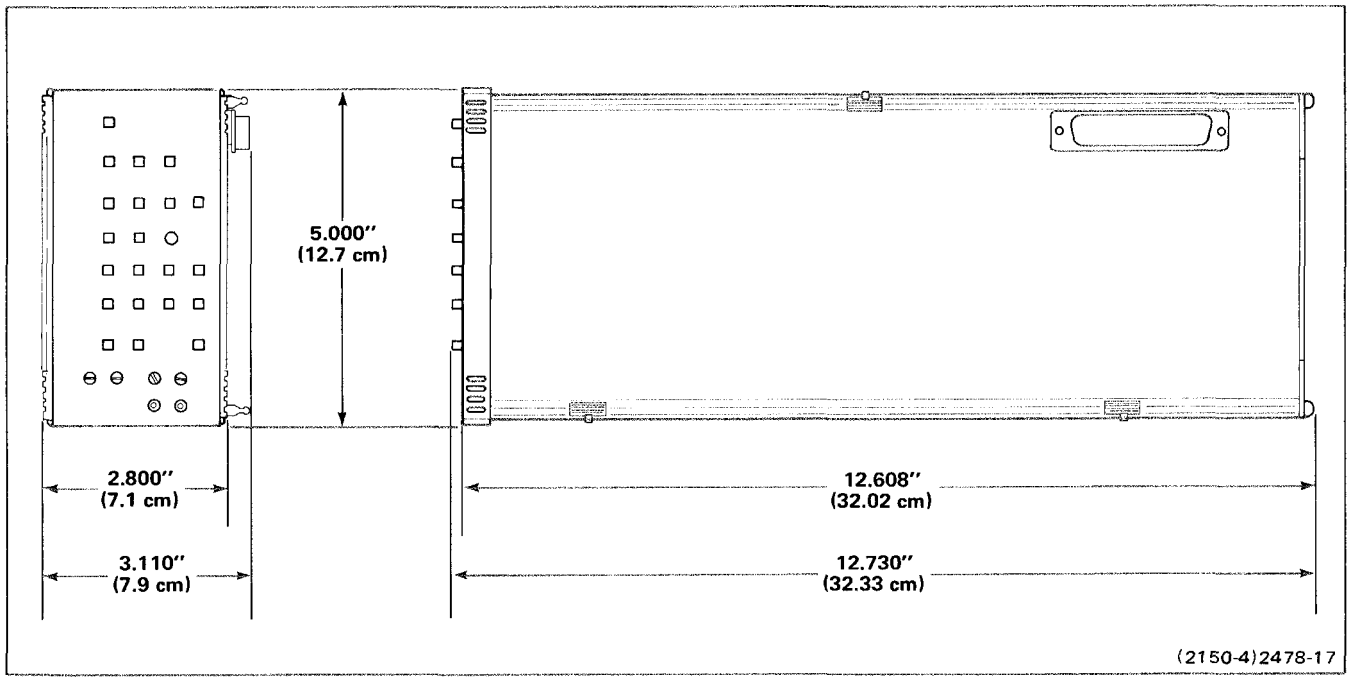


Figure 1-2. DF dimensional drawing.

STANDARD ACCESSORIES

1 ea . . . . . .GPIB Adapter

1 ea . . . . . .Instruction Manual

Refer to the tabbed Accessories page in the back of this manual for standard accessory part numbers.

OPERATING INSTRUCTIONS

To effectively use the DF Display Formatter, the capabilities of the DF and the companion 7D01 Logic Analyzer must be known. This section briefly describes the operation of the controls and connectors, provides detailed operating instructions, and a functional check procedure for the DF. The General Information section provides instructions for installation of the DF and the 7D01 into a 7000-series oscilloscope mainframe. Refer to the 7D01 Operators or Instruction Manuals for information on the 7D01 Logic Analyzer.

CONTROLS AND CONNECTORS

INTERNAL

The Readout Source jumper is located inside the DF. When using the Timing Diagram display, readout can be produced either by the DF readout system or by the readout system of the associated oscilloscope mainframe (refer to Figure 2-1). We recommend using the DF readout unless it is important to have the style of characters produced by the mainframe readout system.

EXTERNAL

The major controls required for operation of the DF are located on the front panel of the unit. Figure 2-2 provides a brief description of the front-panel functions. More information is given under Basic Operating Instructions.

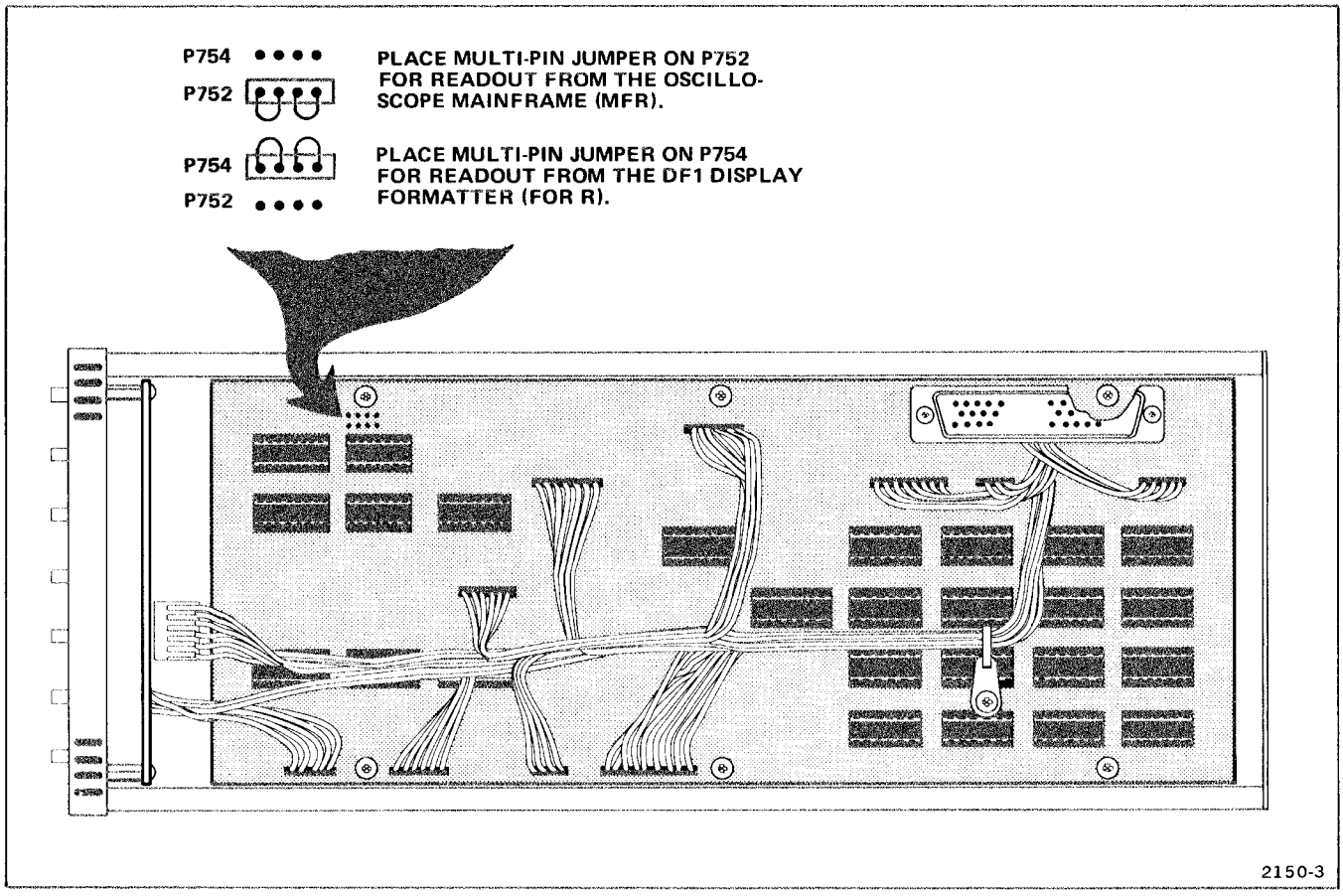
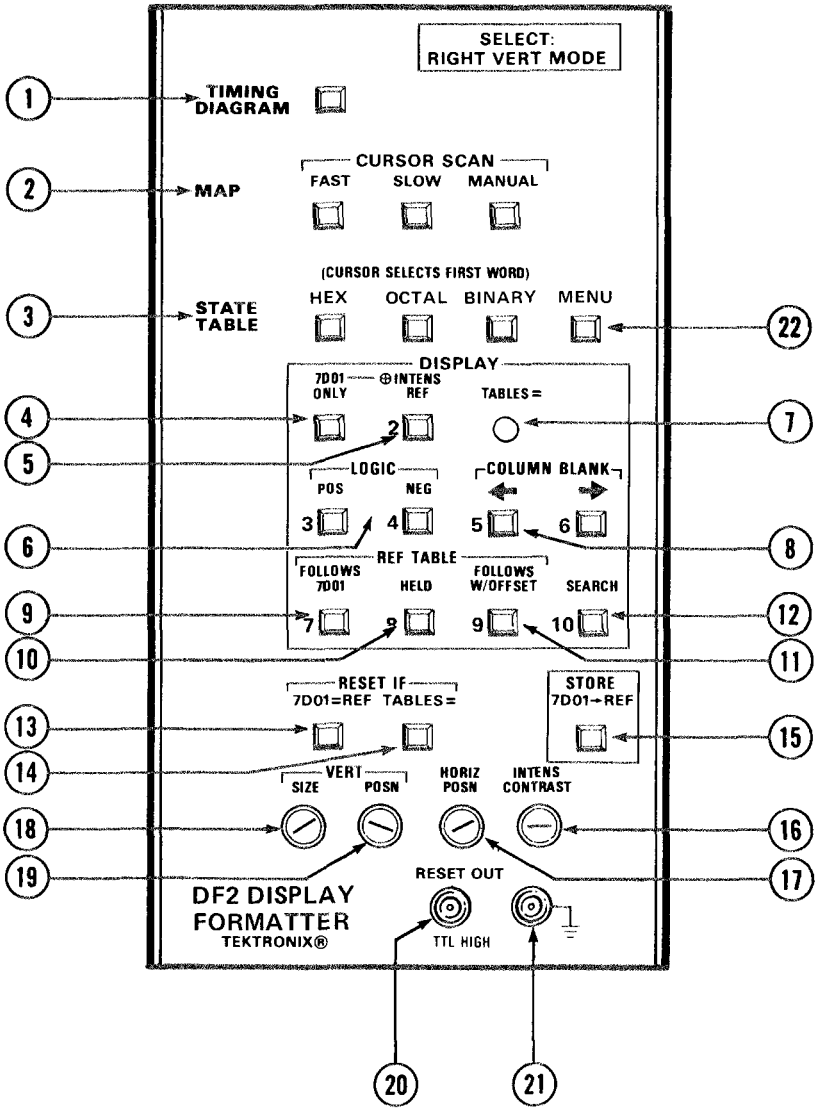


Figure 2-1. Location of the Readout Source multi-pin jumper.



(2150-1A)2478-18

Figure 2-2. Front-panel controls, connectors, and indicators.

(1) **Timing Diagram Switch**—Selects the timing diagram display from the 7D01 Logic Analyzer.

(2) **MAP (CURSOR SCAN Switches)**—Select view of the 7D01 memory data in X-Y coordinate points on the oscilloscope mainframe crt. The DF automatically sequences the data locations at a FAST or SLOW rate, or data locations are selected manually with the 7D01 Cursor control.

(3) **STATE TABLE Switches**—Select tabular display of the cursor word, the 16 words following the cursor word, and the trigger word. The tabular format can be displayed in HEX (hexadecimal), OCTAL, or BINARY base-number systems.

(4) **7D01 ONLY Switch**—Selects the state table from the 7D01 memory for display on the left-hand side of the crt.

(5) **⊕(Exclusive Or) INTENS REF Switch**—Compares state table display from the 7D01 memory (left-hand column) to a reference state table stored by the DF (right-hand colunn).

(6) **LOGIC Switches**—Determine whether the state table displays are in positive or negative logic.

(7) **TABLE = Indicator**—Lamp turns on when the 7D01 state table and the reference state table are equal.

(8) **COLUMN BLANK Switches**—Provide column blanking for state table displays. The blanked columns are excluded from the data base for all state table comparison and reset functions.

(9) **REF TABLE FOLLOWS 7D01 Switch**—The cursor location (trigger-to-cursor difference) in the reference state table (right-hand column) follows the cursor location in the 7D01 state table (left-hand column).

(10) **REF TABLE HELD Switch**—Locks the cursor location in the reference state table which allows the cursor location in the 7D01 reference state table to be moved independently.

(11) **REF TABLE FOLLOWS W/OFFSET Switch**—Maintains the cursor location offset, between the 7D01 and reference state tables, that was established in the REF TABLE HELD mode.

(12) **SEARCH Switch**—The 7D01 memory is searched for a match of the cursor word (first word) in the reference state table.

(13) **RESET IF 7D01 = REF Switch**—The 7D01 memory is reset when the 7D01 memory equals the DF reference memory.

(14) **RESET IF TABLES = Switch**—The 7D01 memory is reset when the 7D01 state table display equals the reference state table display.

(15) **STORE 7D01 → REF Switch**—Transfers the 7D01 memory into the DF reference memory.

(16) **INTENS CONTRAST Adjustment**—Controls brightness of the intensified characters of the DF display.

(17) **HORIZ POSN Adjustment**—Controls horizontal position of the DF display.

(18) **VERT SIZE Adjustment**—Varies vertical size of the DF display.

(19) **VERT POSN Adjustment**—Controls vertical position of the DF display.

(20) **RESET OUT Connector**—Pin-jack connector provides a HIGH TTL level output when the 7D01 memory is reset by the DF.

(21) **Ground Connector (⏚)**—Pin-jack connector provides a ground return for the RESET OUT gate.

(22) **MENU Switch**—Selects the Menu List display.

(2150-1B)2478-43

Figure 2-2. Front-panel controls, connectors, and indicators (continued).

BASIC OPERATING INSTRUCTIONS

POWER-ON-MODE

When power is applied to the oscilloscope mainframe (Power-On mode), the DF reference memory and the memory which acquires data from the 7D01 are checked for proper operation of the random access memory (RAM) integrated circuits (refer to Error Message Displays in this section). Then, the 7D01 is reset and the DF reference memory and the 7D01 memory are cleared. The Display Mode is automatically set to Timing Diagram, the LOGIC is set to POS, and the cursor location (trigger-to-cursor readout) is set to +0. All other DF push-button selections are cancelled.

DISPLAY MODES

The DF displays digital data in 3 Display Modes: Timing Diagram, Map, and State Table. Figure 2-3 shows the controls required to activate typical DF displays.

Timing Diagram Displays

The front-panel TIMING DIAGRAM push button selects the Timing Diagram display (4, 8, or 16 channels) from the companion 7D01 Logic Analyzer (see Fig. 2-3). The cursor function of the 7D01 provides an intensified zone on the data display and a corresponding numerical readout display shows the logic state for each displayed channel of data. The position of the cursor, relative to the trigger, is also displayed on the crt readout. Refer to the 7D01 manual for more information on the 7D01 Logic Analyzer.

The source of the display readout can be from the oscilloscope mainframe readout system (MFR) or the DF (FOR R). (Refer to Internal Controls and Connectors, in this section, for more information.) When the Timing Diagram Display Mode is selected (Readout Source jumper set to Formatter Readout) after either the HEX, OCTAL, or BINARY State Table function has been displayed, the cursor word readout is displayed in the same base-number system as displayed previously in the State Table Display Mode. Then, the cursor word readout changes between binary and the base-number system in the previously selected State Table Display Mode, with every other push of the TIMING DIAGRAM push button. However, if the Readout Source jumper is set for mainframe readout (MFR), cursor word readout is displayed only in the binary system.

Map Displays

The Map function provides a view of the 7D01 memory displayed as x-y coordinate dots on the crt. The vertical axis represents the most significant half of the data word and the horizontal axis represents the least significant half (see Figure 2-3).

The map display can be formatted from 4, 8, or 16 channels of input data. Therefore, 4- and 8-channel map displays are plotted over the entire crt display area in the same manner as a 16-channel display. A 16-channel display is capable of 64,000 coordinate points, an 8-channel display is capable of 256 coordinate points, and a 4-channel display is capable of 16 coordinate points.

A map cursor, indicated by a plus symbol (+), sequences automatically through the data locations in the order in which the data was loaded into memory. The cursor scans at a FAST or SLOW rate, as determined by the CURSOR SCAN push buttons. When either the FAST or SLOW push button is held in, the cursor scan is stopped near a desired location on the display and can be positioned to the exact location with the 7D01 cursor position controls. Also, when the MANUAL CURSOR SCAN push button is pressed, the 7D01 cursor position controls are used to manually position the cursor to the exact position desired. The readout display shows the logic state of the cursor word (bottom of crt), and the position of the cursor point, relative to the trigger point, is displayed at the top of the crt.

The map display is particularly useful for a fast overall check of digital systems. First of all, the map display pattern for a particular set of digital inputs must be known. Then, if there is a change in any one of the input signals, the map display pattern will change. A different map display pattern indicates that the circuits are not operating in the normal manner. Figure 2-4 illustrates a map display pattern from 16 signal inputs and shows that the map display pattern changes when input signals are removed.

State Table Displays

The State Table function enables the data, recorded in the 7D01, to be displayed in a tabular format. The cursor word, the sixteen words which follow, and the trigger word are

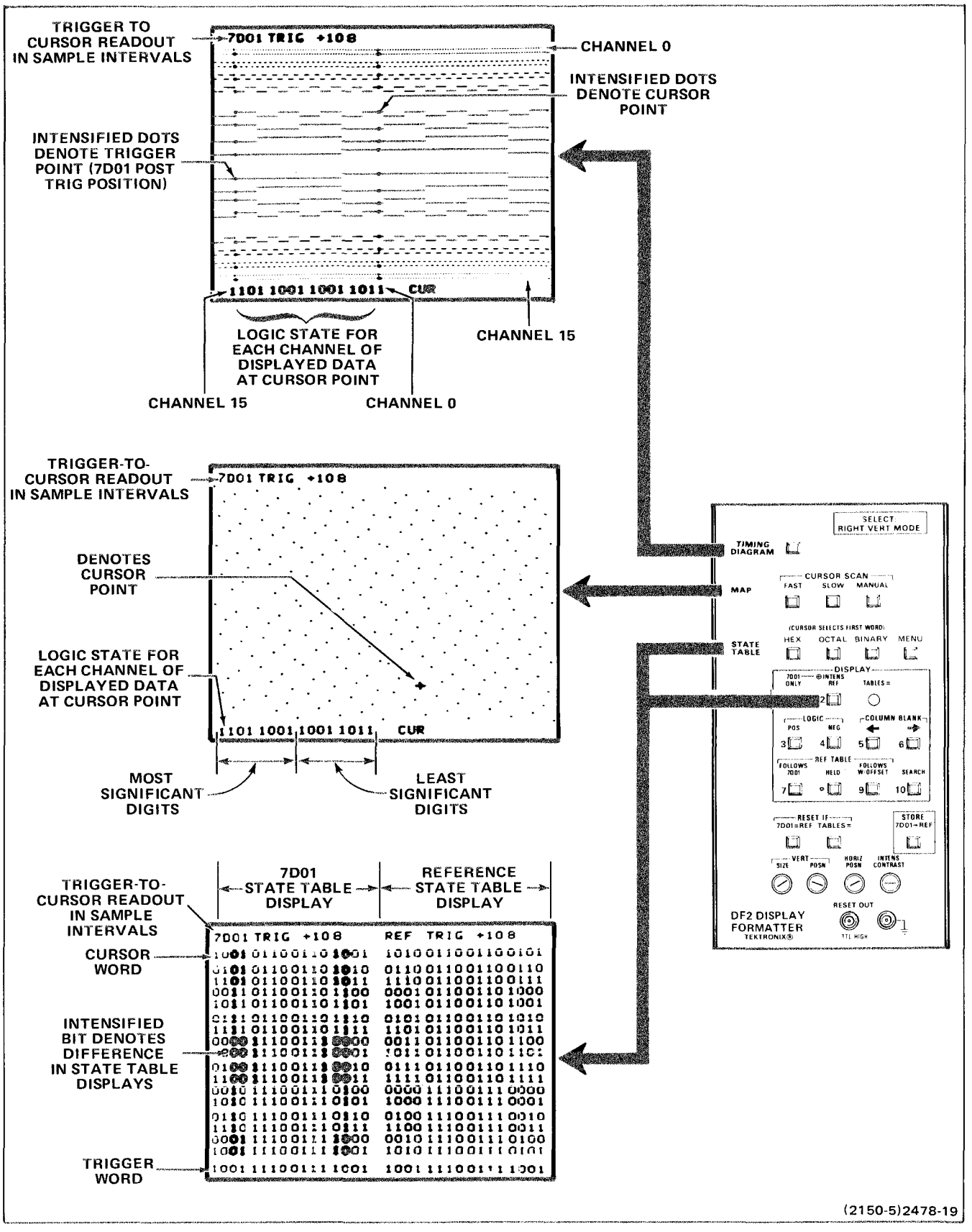


Figure 2-3. Typical DF Display Modes.

displayed. If the trigger word is displayed in the first 17 words of the state table, it is indicated by a blinking condition. The position of the cursor, relative to the trigger, is also displayed on the crt readout (see Figure 2-3).

Each time the 7D01 cursor position is changed or the 7D01 is reset, the display is updated. If the data ends before 17 words are displayed, the remainder of the display is filled with an asterisk (*) character. Any "old data" from the 7D01 memory is indicated by an "X" character.

Three push button switches select State Table displays in HEX (hexidecimal, base 16), OCTAL (base 8), or BINARY (base 2) codes. The digits are grouped in threes or fours depending upon the setting of the 7D01 cursor byte switch.

The ten Display push buttons are functional in STATE TABLE format only. When the HEX, OCTAL, or BINARY push buttons are depressed the function of all ten DISPLAY push buttons corresponds to the functional name positioned above each button. When the MENU push button is depressed the function of each push button changes to the number positioned to the left of each button. These numbers correspond to the numbers in the MENU list display.

7D01 ONLY. The State Table display from the 7D01 is displayed on the left side of the crt. The ⊕ INTENS REF displays are not functional in the 7D01 ONLY mode.

7D01 ⊕ INTENS REF. Two state tables are displayed simultaneously on the crt. The state table from the 7D01 is displayed on the left half of the crt and a reference state table is displayed on the right half of the crt (see Figure 2-3). When the 7D01 ⊕ INTENS REF is initially selected, the STORE 7D01→REF push button must be pressed to load the reference memory. Any differences between the 7D01 and reference state tables are indicated by intensified bits at the appropriate location in the 7D01 state table. Any differences in the state tables due to old data, indeterminate data, end data, or blanked columns, is interpreted as "don't care" conditions and are not intensified in the 7D01 state table (refer to the Glossary in the General Information section). If there are no differences between state tables, the TABLES= indicator is illuminated.

REF TABLE FOLLOWS 7D01. The FOLLOWS 7D01 mode is functional only when operating in the 7D01 ⊕ INTENS REF mode. The cursor location (trigger-to-cursor readout) in the reference state table is aligned with the cursor location of the 7D01 state table. As the 7D01 location is changed (by means of the 7D01 cursor position or data position controls), the cursor location of the reference state table follows.

REF TABLE HELD. The HELD mode is functional only when operating in the 7D01 ⊖ INTENS REF mode. The reference table cursor location remains at one setting, allowing the cursor location in the 7D01 state table to be moved independently (offset). Refer to Figure 2-5.

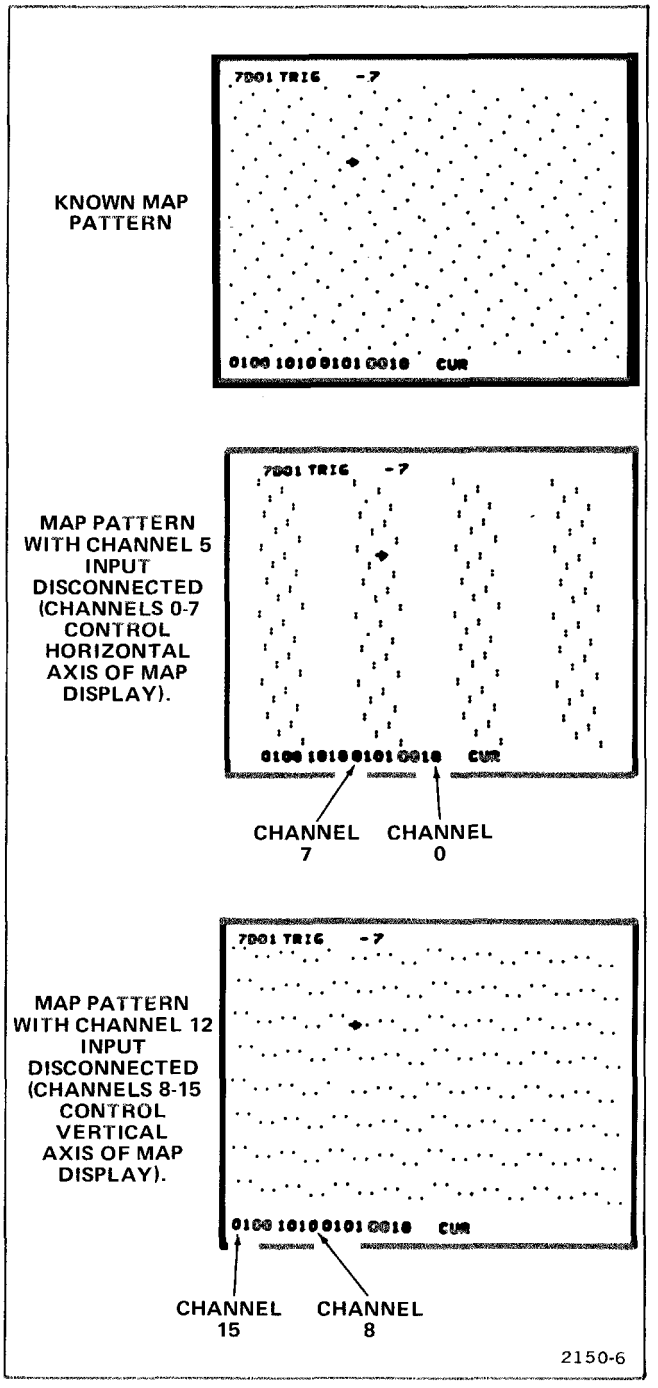


Figure 2-4. Typical map display usage.

@

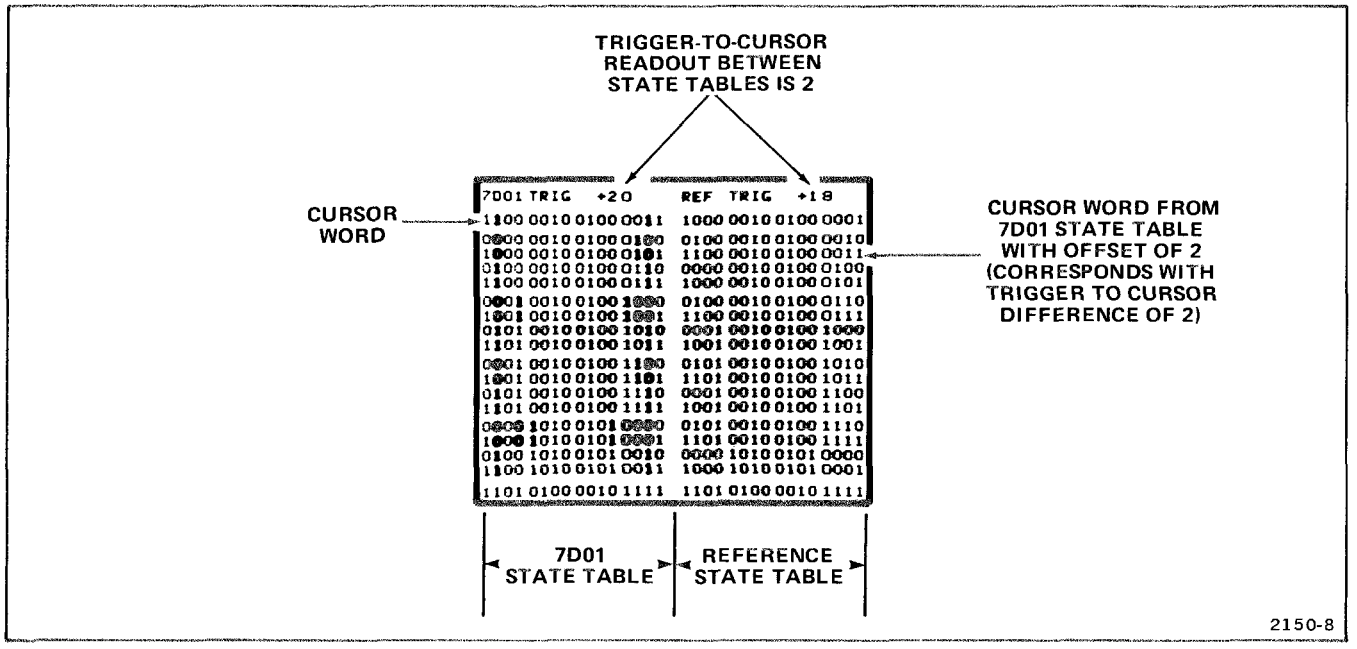


Figure 2-5. Typical state-table display showing offset between the 7D01 and reference state tables.

REF TABLE FOLLOWS WITH/OFFSET. The FOLLOWS WITH/OFFSET mode is functional only when operating in the 7D01 ⊕ INTENS REF mode. The difference in cursor location (offset) between the 7D01 state table and the reference state table, is maintained at the time the FOLLOWS W/OFFSET push button is pressed (see Figure 2-5). The offset between the 7D01 and reference state tables remains constant as the 7D01 cursor is moved. To delete the trigger-to-cursor offset, select REF TABLE FOLLOWS 7D01.

SEARCH. The SEARCH mode is functional when operating in the 7D01 ⊕ INTENS REF mode. When the SEARCH push button is pressed, the 7D01 memory is searched for a match of the reference cursor word. When a match of the reference cursor word is found, the REF TABLE mode is automatically set to HELD and the matching word is moved to the 7D01 cursor word position (first word) of the 7D01 state table.

If a match for the cursor word is not found in the 7D01 memory, the state table display remains unchanged. Also, if the first word in the reference memory is not valid, or a comparison is presently being made in the RESET IF 7D01=REF mode, a search of the 7D01 memory is not made.

RESET IF TABLES=. This mode is functional only when operating in the 7D01 ⊙ INTENS REF mode. When the RESET IF TABLES= push button is pressed, the 7D01 resets and compares the data in the 7D01 state table to the data in the reference state table. If there are no differences, the 7D01 resets, acquires new data, and repeats the comparison. The number of resets is displayed on the crt readout. If there are differences, the acquisition, compare, and reset cycle stops. The differences between state-table displays are intensified in the 7D01 state table. To cancel the RESET IF TABLES= function, a second push of the RESET IF TABLES= push button is required.

RESET IF 7D01=REF. This mode is functional when operating in all DF display modes. When the RESET IF 7D01=REF push button is pressed, the data in the 7D01 memory is compared to the data in the reference memory. If there are no differences, the 7D01 resets, acquires new data, and repeats the comparison. The number of resets is displayed on the crt readout. If there are differences, the acquisition, compare, and reset cycle stops. The cursor word is moved to the first difference and the RESET IF 7D01=REF function is canceled. The RESET IF 7D01=REF function may also be canceled with a second push of the RESET IF 7D01=REF push button.

STORE 7D01→REF. This mode is functional in all DF display modes (Timing Diagram, Map, and State Table). When the STORE 7D01→ REF push button is engaged, the 7D01 memory is transferred into the DF reference memory. When the trigger-to-cursor readout is the same in both state table displays, the 7D01 state table is transferred into the reference state table with no intensified bits. However,

if the trigger-to-cursor readout of the state table displays is offset, the 7D01 state table will be transferred to the reference state table with that offset (intensified bits may appear). The tables are equal but offset by the trigger-to-cursor readout (see Figure 2-5). To make the tables equal, either set the 7D01 cursor position controls so that the trigger-to-cursor readout is the same for both state tables or press the REF TABLE FOLLOWS 7D01 push button.

COLUMN BLANKING. Column blanking is functional when operating in any State Table mode. Undesired vertical columns of data can be blanked from the state-table displays (COLUMN BLANK→ push button). The blanked columns are interpreted as "don't care" information for state table comparisons and reset functions (refer to the Glossary in the General Information section). To restore a blanked column, press the COLUMN BLANK← push button. The column blanking function is automatically reset to display or compare all columns when the TIMING DIAGRAM, MAP, STATE TABLE (HEX, OCTAL, BINARY), 7D01 ONLY, 7D01 ⊕ INTENS REF or MENU push buttons are pressed.

LOGIC STATES. When POS LOGIC is selected, the most positive voltage level is interpreted as a logic HI and the most negative level is interpreted as a logic LO. When NEG LOGIC is selected, the most negative level is displayed as a logic HI and the most positive level is interpreted as a logic LO.

Menu Displays

The front-panel MENU push button provides a Menu List display on the crt which lists additional operational modes assigned to the DF. The numbers in the Menu List correspond to the numbers assigned to the 10 Display push buttons. The detailed operating instructions, for the various operational modes listed in the Menu List, are provided in more detail further on in this section.

To select a desired operational mode, after the MENU push button has been pushed, depress the numbered Display push button corresponding to the numer in the Menu list. Refer to the detailed operating instructions in this section for additional instruction regarding the operational mode selected.

Size and Position Adjustment

The controls used to adjust the size and position of displays depend on the Display Mode selected.

When operating in the Timing Diagram Display Mode, positioning of the timing diagram display is controlled by the 7D01 vertical and horizontal position controls. The size of the timing diagram display is determined by the 7D01 vertical and horizontal magnification controls. Vertical positioning of the display readout is controlled by the DF front-panel VERT SIZE and VERT POSN adjustments and horizontal positioning is controlled by the DF HORIZ POSN adjustment.

When operating in the Map or State Table Display Modes, vertical and horizontal positioning of the entire display (data and readout displays) is controlled by the DF front-panel VERT POSN and HORIZ POSN adjustments. Vertical height of the entire display is controlled by the DF front-panel VERT SIZE adjustment.

Error Message Displays

Error messages are provided on the crt readout to identify operator error and instrument failures.

SEE MANUAL CUR CAN'T MOVE. This error message generally occurs when the 7D01 cursor control is set between switch detents. When the error message appears on the crt, move the 7D01 cursor control into a switch detent and the error message should disappear. If the error message does not disappear, refer to the error message discussion in the Maintenance section of the Instruction Manual.

BAD RAM SEE MANUAL. This error message indicates that a random access memory (RAM) integrated circuit has failed. To test the DF for a bad RAM: Turn off power to oscilloscope mainframe, wait a short time, and turn power on (Power-On Mode). Then check the crt readout for an error message. If the error message appears on the crt read-out, refer to the error message discussion in the Maintenance section of the DF Instruction Manual.

BASIC FUNCTIONAL CHECK

The following procedure is provided for familiarization and for checking basic instrument functions of the Display Formatter. Refer to the Controls and Connectors discussion while performing this procedure. If a malfunction or possible improper adjustment is revealed while performing this procedure, first check the operation of the 7D01 and associated oscilloscope mainframe, then refer to the DF Instruction Manual for troubleshooting and adjustment procedures.

The functions are checked without removing the covers or making internal connections. Performance requirements, functions which require removal of side panels, and detailed checks of the DF memory are provided in the Performance Check and Adjustment procedures in the DF Instruction Manual.

SETUP PROCEDURE

1. Attach the Display Formatter to the 7D01 Logic Analyzer and install the three-wide plug-in assembly into the oscilloscope mainframe (refer to Installation, in the General Information section, for assembly instructions). Set the oscilloscope mainframe to display the right vertical and A horizontal compartments.

2. Connect one P6451 probe connector to the CH 0-7 input connector on the 7D01. Connect all ten P6451 probe tips together (to a common wire or connection).

3. Set the 7D01 Logic Analyzer controls as follows:

Sample Interval	1 ms
Record Display Time	∞
Data Position	Post Trig
Data Channels	0-15
Trigger Source	W.R.
Word Recognizer	CH 0 through CH 6—LO CH 7—HI CH 8 through CH 15—X External Qualifier—X Probe Qualifier—X
W.R. Mode	Sync
Threshold Voltage	TTL (+1.4 V)

4. Perform the Power-On function (turn mainframe power off, wait a short time, then turn power on).

5. Press the Manual Trigger push button.

TIMING DIAGRAM DISPLAYS

1. Perform the Setup Procedure.

2. Check crt display for a 16-channel display. It may be necessary to adjust the mainframe intensity and the 7D01 vertical and horizontal position/magnification controls.

3. Check that the trigger-to-cursor readout is zero and that the intensified cursor point is superimposed on the intensified trigger point (left-hand side of the crt display).

4. Set the 7D01 Data Position switch to Center and press the Manual Reset and Trigger push buttons. Check that the trigger point (intensified dots) is near the center of the crt display and that the trigger-to-cursor readout is approximately −112. Rotate the 7D01 Cursor Fine Position control and note that the cursor point (indicated by intensified dots on the left side of the 16-channel display) moves in 1-bit increments as shown by the trigger-to-cursor readout. Rotate the 7D01 Cursor Coarse Position control and note that the cursor point moves in 16-bit increments. Note that the logic state for each channel of displayed data (16-bit readout at bottom of crt) changes corresponding to the cursor position. Set the 7D01 Cursor Position controls for a trigger-to-cursor readout of zero. Check that the intensified cursor point is superimposed on the intensified trigger point (center of crt).

5. Set the 7D01 Data Position switch to Pre Trig and press the Manual Reset and Trigger push buttons. Check that the trigger point (intensified dots) is at the right-hand side of the display and that the trigger-to-cursor readout is approximately −112. Set the 7D01 Cursor Position controls for a trigger-to-cursor readout of zero. Check that the intensified cursor point is superimposed on the intensified trigger point (right-hand side of crt display).

MAP DISPLAYS

1. Perform the Setup Procedure.

2. Press the MANUAL MAP push button. Check display for a trigger-to-cursor readout at the top of the crt and a cursor word at the bottom.

3. Rotate the 7D01 Cursor Position controls and note that the trigger-to-cursor reading can be manually changed.

4. Press the SLOW MAP push button and check that the trigger-to-cursor readout sequences automatically at a slow rate. Press the FAST MAP push button and check that the trigger-to-cursor readout sequences at a fast rate.

STATE TABLE DISPLAYS

1. Perform the Setup Procedure.

2. Press the STATE TABLE HEX push button. Then, press the TIMING DIAGRAM push button and check for 16 channels on the crt. Note the logic-state readout of the cursor word, in hexadecimal code, at the bottom of the crt.

3. Press the STATE TABLE HEX and 7D01 ONLY push buttons. Check for a State Table display on left side of the crt in hexadecimal code (base 16). Note that the cursor word (top word in state table) is the same as the cursor word in the Timing Diagram display noted in step 2 and that the trigger-to-cursor readout is +0. Check that the cursor word is blinking and that the trigger word (bottom) is the same as the cursor word.

4. Rotate the 7D01 Cursor Fine Position control counter-clockwise, 1 bit at a time, until the trigger-to-cursor readout is −16. Check that the blinking word is the seventeenth word in the State Table display.

5. Press the STATE TABLE OCTAL push button. Check that the State Table display is given in the octal (base 8) code.

6. Press the STATE TABLE BINARY push button. Check that the State Table display is given in the binary (base 2) code. Press the NEG LOGIC push botton and check that all zeros become ones and that all ones become zeros.

7. Turn off power to the oscilloscope mainframe, wait a short time, and turn power on (Power-On mode). Press the Manual Trigger push button. Check crt for Timing Diagram display with trigger-to-cursor readout of zero.

8. Press the STATE TABLE BINARY push button and note the State Table display on the left half of the crt. Press the 7D01 ⊕ INTENS REF push botton and check for a reference state table on the right side of the crt, in addition to the 7D01 state table. Note that the reference state table is all zeros and that the ones in the 7D01 state table are intensified.

9. Press the STORE 7D01 → REF push button and check that the 7D01 display is transferred into the reference memory. Note that the trigger-to-cursor readout is +0 for both state tables displayed, and that there are no intensifed characters in the 7D01 state table.

10. Press the REF TABLE FOLLOWS 7D01 push button. Rotate the 7D01 Cursor Position controls and check that the trigger-to-cursor readout of the reference state table follows the trigger-to-cursor readout of the 7D01 state table.

11. Press the REF TABLE HELD push button. Rotate the 7D01 Cursor Position controls. Check that the trigger-to-cursor readout in the 7D01 state table changes and the trigger-to-cursor readout in the reference state table remains fixed.

12. Rotate the 7D01 Cursor Position controls to set the 7D01 trigger-to-cursor readout to +5 and press the REF TABLE FOLLOWS W/OFFSET push button. Rotate the 7D01 Cursor Position controls and check that the trigger-to-cursor offset between state tables is maintained (offset is obtained in REF TABLE HELD mode).

13. Press the COLUMN BLANK→ push button and check that columns of data are blanked from the State Table displays. The blanked columns are interpreted as "don't care" information for state table comparisons. Press the COLUMN BLANK← push button and check that the blanked columns of data are restored.

14. Press the REF TABLE FOLLOWS 7D01 push button. Check that both state tables have the same trigger-to-cursor readout and that there are no intensified characters in the 7D01 state table. Check that the TABLES= indicator is illuminated.

15. Press the RESET IF TABLES= push button. Check that the state tables are reset and the number of resets is displayed below the reference state table. Each time the Manual Trigger push button is pressed the number of resets displayed should advance by one. Repress the RESET IF TABLES= push button to turn off backlit LED. Press Manual Trigger push button to return state table display.

16. Press the RESET IF 7D01=REF push button. Check that the state tables are reset and the number of resets is displayed below the reference state table. Each time the Manual Trigger push button is pressed the number of resets displayed should advance by one. Repress the RESET IF 7D01=REF push button to turn off backlit LED. Press Manual Trigger push button to return state table display.

FRONT-PANEL ADJUSTMENTS

1. Perform the Setup Procedure.

2. Rotate the 7D01 Horizontal Position control and note that it horizontally positions the Timing Diagram display. Rotate the 7D01 Horizontal Magnification control and note that it controls the horizontal size of the Timing Diagram display.

3. Rotate the 7D01 Vertical Position control and note that it vertically positions the Timing Diagram display. Rotate the 7D01 Vertical Magnification control and note that it controls the vertical size of the Timing Diagram display.

4. Press the STATE TABLE BINARY and 7D01 ⊕ INTEN REF push buttons. Rotate the DF VERT SIZE screwdriver adjustment and note that it controls the vertical size of the entire State Table display. Rotate the DF VERT POSN screwdriver adjustment and note that it vertically positions the entire State Table display.

5. Rotate the DF HORIZ POSN screwdriver adjustment and check that it horizontally positions the entire State Table display.

6. Rotate the DF INTENS CONTRAST screwdriver. adjustment and check that it controls the brightness of the intensified characters in the 7D01 State Table display.

NOTE

The Functional Check procedure is provided for familiarization and for checking basic functions of the Display Formatter. These functions are checked without removing the covers or making internal connections. Performance requirements, functions which require removal of side panels, and detailed checks of the DF memory are provided in the Performance Check and Adjustment procedures in the DF Instruction Manual. Only qualified service personnel should perform checks given in the Instruction Manual.

IRREGULAR OPERATING SYMPTOMS

The following table lists some irregular operating symptoms with their probable causes and corrective procedures. Table 2-1 is intended to assist the operator in determining whether an irregular operating symptom is the result of an operational error, a measurement technique problem or a malfunction in the DF/7D01. The probable causes for the symptoms listed in Table 2-1 assume that the DF/7D01 and associated equipment are operating properly. The corrective procedures can be performed by the operator without additional test equipment, excluding equipment malfunction.

TABLE 2-1
Irregular Operating Symptoms

Symptom	Probable Cause	Corrective Procedure
1. No data display.	Display positioned off screen.	Check Horiz and Vert Position settings.
2. No data display with Sample Interval in EXT Position.	No external clock signal.	Check that clock signal is applied through Data Acquisition Probe P6451.
	Wrong threshold voltage.	Check Threshold Voltage selector and/or adjustment for proper setting.
3. No data display with: a. W.R. Mode in SYNC position. b. Trigger Source in W.R. position. c. TRIG'D indicator not lit.	No external clock signal for the W.R. in SYNC position.	Check that clock signal is applied through Data Acquisition Probe P6451.
	Word selected on W.R. channel switches does not exist.	Check that W.R. channel switches are set for an existing word.
4. No data display with: a. W.R. Mode in ASYNC position. b. Trigger Source in W.R. position. c. TRIG'D indicator not lit.	Word selected on channel switches does not exist.	Check that channel switches are set for an existing word.
	Asynchronous filter is rejecting valid data.	Check that Filter is not set too far clockwise.
5. When testing circuits with gated clocks. a. No data display with: (1) Sample interval in EXT Position. (2) Full display/First Trigger (P617) in **First Trigger position.** (3) TRIG'D indicator not lit.	Trigger word existed only during first clock pulse and is ignored by the 7D01.	Set the W.R. switches to a value not equal to the first word that is synchronously clocked, but equal to some other data to be captured.
	Word selected on W.R. switches does not equal any data being clocked in.	Check that the W.R. switches are set for an existing word.
	Data on the channels the W.R. switches are set to be triggered on is not changing. The W.R. requires an edge; i.e., a transition from NOT true data to true data. If the data clocked in always equals the W.R. switches, no trigger will occur. This may occur if only one W.R. switch is set to trigger while all the other switches are on X (don't care) and the data on that one channel is not changing.	Push manual trigger while the data is being clocked in. Look at the data to see if it is all the same as the settings of the W.R. switches. —OR— Set the W.R. switches to a more unique trigger word being clocked in; i.e., if only one channel is not changing, trigger on another channel that is changing.

TABLE 2-1 (CONT.)
Irregular Operating Symptoms

Symptom	Probable Cause	Corrective Procedure
5. (cont) b. No data display with: (1) Sample Interval in EXT position. (2) Full Display/First Trigger (P617) in **First Trigger position.** (3) TRIG'D indicator lit.	Insufficient number of clock pulses after trigger word to fill memory (display) from trigger markers to end of sweep.	See Table 3-1 for minimum number of clock pulses required to obtain a display in First Trigger mode. —OR— Set Sample Interval to 5 ms position until display appears. Then reset Sample Interval to EXT position. This fills up the remaining memory and switches the 7D01 from record to display mode.
c. No data display with: (1) Sample Interval in EXT position. (2) Full Display/First Trigger (P617) in **Full Display position.** (3) TRIG'D indicator not lit.	Insufficient number of clock pulses to fill 7D01 memory.	See Table 3-1 for minimum number of clock pulses required to obtain a display in Full Display mode.
	Trigger word existed only during the time when the clock pulses were clearing the 7D01 memory in Full Display mode and is ignored by the 7D01.	Change Full Display/First Trigger selector (P617) to First Trigger position to catch all trigger events.
d. No data display with: (1) Sample Interval in EXT position. (2) Full Display/First Trigger (P617) in **Full Display position.** (3) TRIG'D indicator lit.	Insufficient number of clock pulses after trigger word to first clear 7D01 memory then fill 7D01 memory (display) from trigger markers to end of sweep.	See Table 3-1 for minimum number of clock pulses required to obtain a display in full Display mode. —OR— Set Sample Interval to 5 ms position until display appears. Then reset Sample Interval to EXT position. *NOTE* *This fills up the remaining memory and switches the 7D01 from record mode to display mode. First Trigger mode may be preferred since fewer clock pulses are required to switch from record to display mode.*

TABLE 2-1 (CONT.)
Irregular Operating Symptoms

Symptom	Probable Cause	Corrective Procedure
6. Incorrect data display.	Wrong mainframe Vertical and/or Horizontal Mode.	Check that proper mainframe Vertical and/or Horizontal Mode is selected.
	Wrong threshold voltage.	Check Threshold Voltage selector and/or adjustment for proper setting.
7. Incorrect data display after changing Data Channel or Data Position setting.	Manual Reset button was not pressed after changing Data Channel or Data Position setting.	Press Manual Reset button to acquire new data in memory in the correct format.
8. Incorrect or noisy data display on channels that are not connected to a Data Acquisition Probe P6451.	Data input lines are not biased properly when a Data Acquisition Probe P6451 is not connected.	Connect a Data Acquisition Probe P6451 to unused channels. —OR— Use P6451 probe only in channel 0-7 and set Data Channels to 0-3 or 0-7 position. Set all unused W.R. channel switches (8-15) to X (don't care) position.
9. Random or incorrect triggering from W.R. with only one Data Acquisition Probe P6451 connected.	W.R. channel switches on unused channels are set to HI or LO positions which can cause some channels to oscillate.	Set W.R. channel switches on unused channels to X (don't care) position.
10. Displayed data on left side of trigger marker is blanked out.	Full Display/First Trigger (P617) is in First Trigger position. The data is blanked because no new data was stored in those locations.	Set Full Display/First Trigger (P617) to Full Display position.

DETAILED OPERATING INSTRUCTIONS FOR GPIB

GPIB OVERVIEW

GENERAL

The primary purpose of the General Purpose Interface Bus (IEE Standard 488-1975 or ANSI MC 1.1-1975) is to define an interface system to interconnect self-contained devices and other devices by external means. The GPIB is a device-independent standard interface which allows easy configuration of devices into a system, or easy addition of modules to an existing system.

Taking full account of cost, flexibility, and compatibility as major factors to be considered, the objectives of the IEEE Standard 488-1975 are to:

1. Define a general-purpose system for use in limited distance applications.

2. Specify the device-independent mechanical, electrical, and functional interface requirements.

3. Specify the terminology and definitions related to the system.

4. Enable the interconnection of independently manufactured apparatus into a single functional system.

5. Permit devices with a wide range of capability — from the simple to the complex - to be interconnected to the system simultaneously.

6. Permit direct communication between devices without requiring all messages to be routed through a control unit.

7. Define a system with a minimum of restrictions on the performance characteristics of the devices.

8. Permit asynchronous communication over a wide range of data rates.

9. Define a system that, of itself, may be relatively low cost, and permit the interconnection of low cost devices.

10. Define a system that is easy to use.

There are three elements that specify the device-independent interface requirements. These elements are:

1. Mechanical elements
2. Electrical elements.
3. Functional elements.

MECHANICAL ELEMENTS

The mechanical elements, as defined by the standard, consist of the physical connectors and cables. This ensures that the interconnecting GPIB compatible devices will never require more than a standard interfacing cable assembly. The connectors have 24 pins with trapezoidal shells for ease in interconnecting devices. (See Figure 3-1.) The pins connect to 16 active signal lines interlaced with eight ground lines. Cables are provided with a plug and a receptacle at each end to allow rigid stacking of connectors on any cable intersection or device connection. This permits either star or daisy-chain configurations.

ELECTRICAL ELEMENTS

The electrical elements, the voltage and current values required at the interface connector, are well defined by the standard. All specifications are based on the use of TTL technology. The logical states are defined as follows:

Coding Logical State	Electrical Signal Levels
0	Corresponds to $\geq$ +2.0 V but $\leq$ +5.25 V (high state)
1	Corresponds to $\geq$ 0 V but $\leq$ +0.8 V (low state)

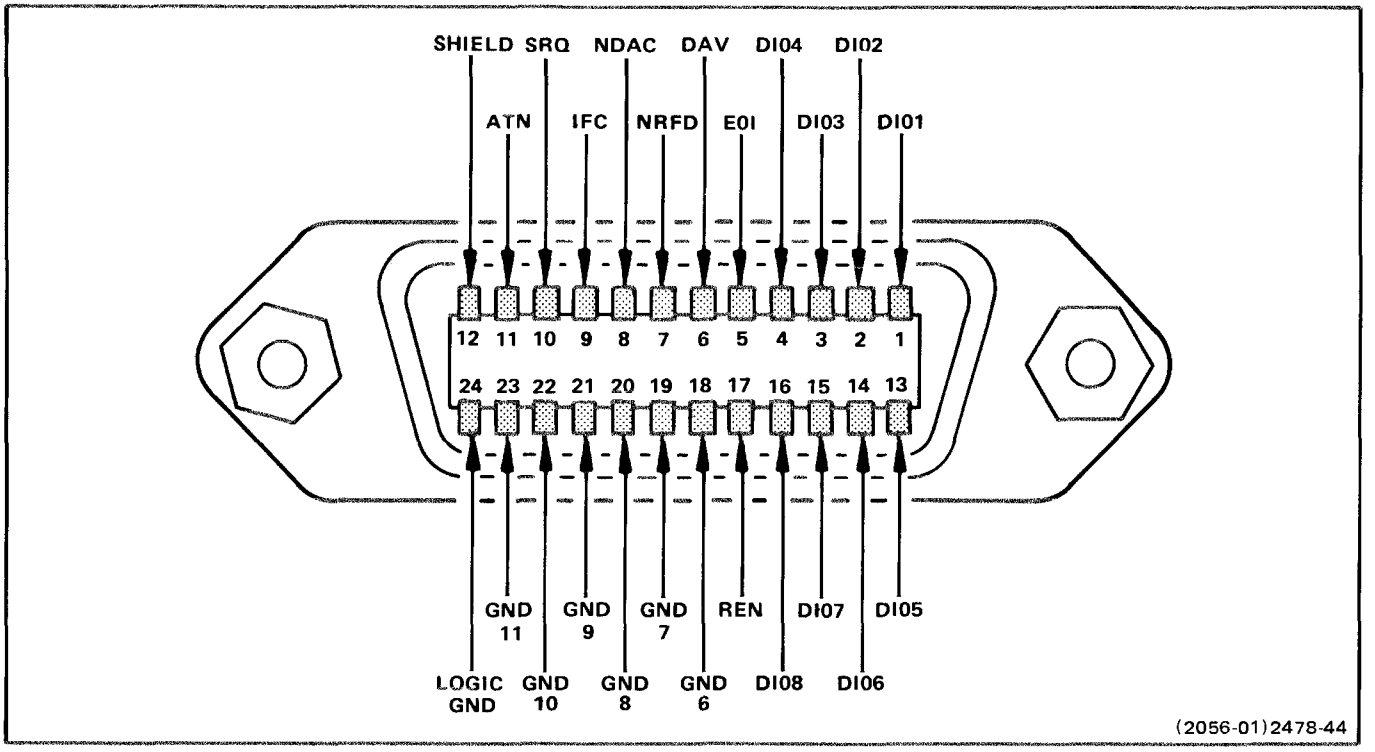


Figure 3-1. GPIB connector.

Messages can be sent as either active or passive true signals. Active true signals occur in the low state and passive true signals occur in the high state. Active transfer of a message is the technique for resolving conflicts between two devices simultaneously sending opposite remote message values, whereby, the interface is so structured that the active value overrides the passive value (using open-collector drivers into a terminated bus).

The electrical limits of the IEEE Standard 488-1975 document also specify that not more than 15 devices can be connected to the bus at any one time; and that the total transmission length is not to exceed 20 meters, or two meters times the number of devices, whichever is less. The data rate through any signal line must be less than, or equal to, 1 Megabit per second.

FUNCTIONAL ELEMENTS

GPIB LINE DEFINITIONS

The GPIB is functionally divided into three component buses: an eight-line Data Bus, a five-line Management Bus, and a three-line Transfer Bus for a total to sixteen active signal lines. This bus structure is shown in Figure 3-2.

Data Bus

The Data Bus contains eight bidirectional active low signal lines, designated DI01 thru DI08. One byte of information (eight bits) is transferred over the bus at a time. DI01 represents the least significant bit in the byte and DI08 represents the most significant bit in the byte. The Data Bus is used to transfer data in a bit-parallel, byte-serial form from talkers to listeners; it also transfers certain commands or addresses from the controller to subordinate devices. Data on the bus can be represented in ASCII (with or without parity), binary coded decimal (BCD), or a machine-dependent binary code.

Management Bus

The Management Bus is a group of five signal lines generally used by the controller to coordinate interface messages and manage the interface functions. The signal definitions for the Management Bus are as follows:

ATN (Attention). This signal line can be asserted true only by the active controller in a system (usually there is only one controller in a system). This line indicates to all devices that the eight data bus signal lines represent interface messages. These messages are for controlling and addressing peripheral devices. When ATN is unasserted (passive false), only one talker and those peripheral devices which are assigned as listeners can take part in data transfers.

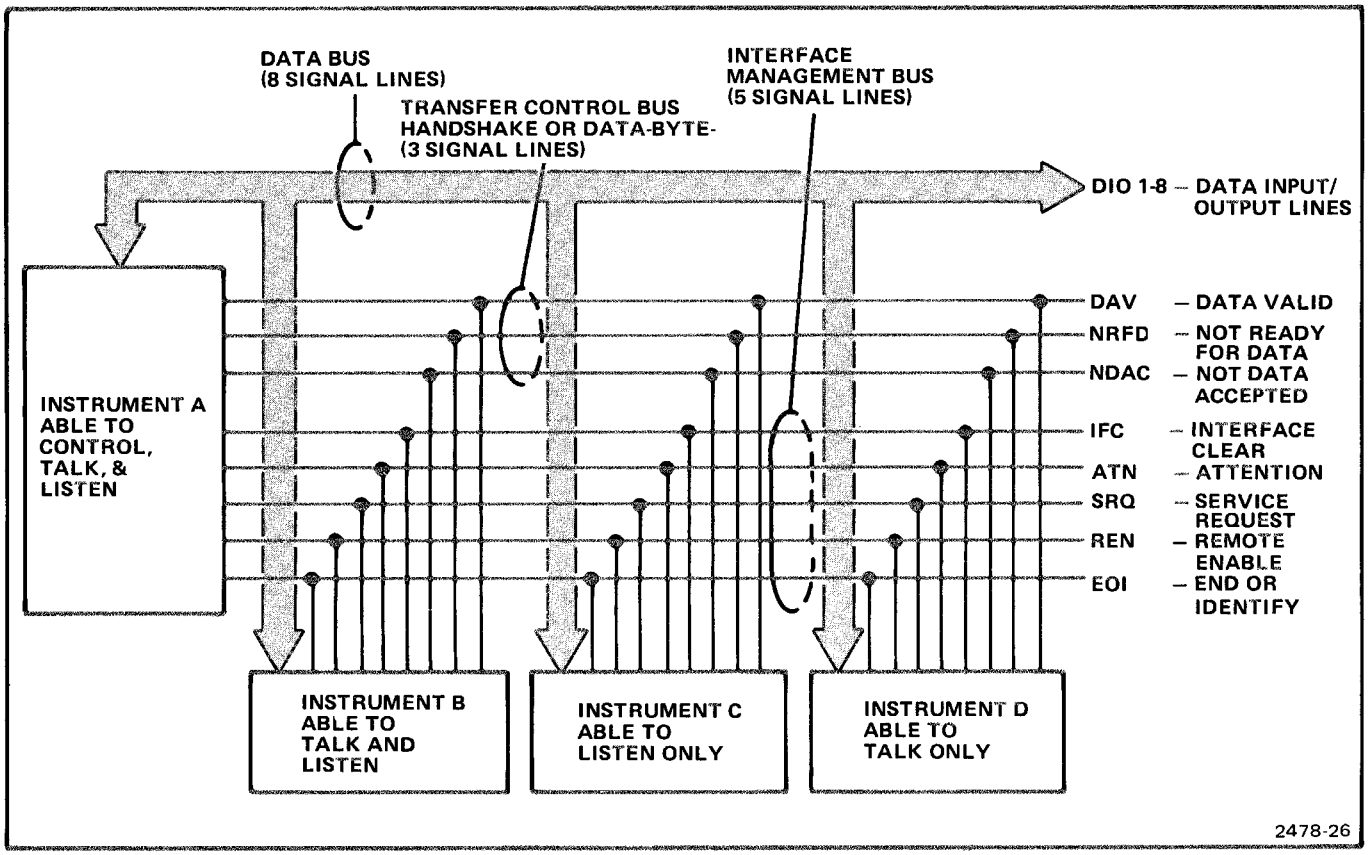


Figure 3-2. General purpose interface bus structure.

SRQ (Service Request). This signal line is used by any device to request service from the controller and thus indicate the need to interrupt the current sequence of events. Reasons for asserting SRQ range from an error generated in a device to alerting the controller that a reading is available.

REN (Remote Enable). The remote enable signal line is asserted only by the active controller, and normally when under program control. The controller has the ability to put a listened device into a state in which the device ignores its front panel controls. If the device is listen-addressed by the controller, it can still have an active front panel if it generates a return to local (rtl) message internally and the controller has not previously put it in the remote with lockout state (RWLS).

EOI (End or Identify). The EOI signal line is used by any talker to indicate the end of a data transfer sequence. The EOI line is normally asserted along with the last byte of data transmitted. When a controller sets both ATN and EOI lines true, each device capable of a parallel poll, and programmed to do so, will indicate its current status on the DIO line assigned to it.

IFC (Interface Clear). The IFC signal line is activated by the controller when it is desirable to place all the interface circuitry in a predetermined quiescent state.

Transfer Bus

When a talker sends data over the Data Bus to a listener, they coordinate their activities by a handshaking process carried out over the three-line Transfer Bus. The Transfer Bus lines are defined as follows:

NRFD (Not Ready for Data). The NRFD signal line remains asserted active low when one or more assigned listeners are not ready to receive the next data byte. When all assigned listeners for a particular data transfer have released NRFD, the line goes inactive high. This tells the talker to place the next data byte on the Data Bus. NRFD cannot go high until NDAC goes low.

DAV (Data Valid). The talker activates the DAV signal line after placing a new data byte on the Data Bus. An active low DAV signal tells each listener to capture the new data byte presently on the Data Bus. The talker is inhibited from activating DAV when a listener holds NRFD active low.

NDAC (Not Data Accepted). The NDAC signal line is held active low by each listener until the listener captures the new data byte currently being transmitted over the Data Bus. When all listeners have captured the data byte, NDAC goes inactive high. This tells the talker that the new data byte has been accepted and to start another handshake sequence by letting DAV go high. NDAC goes low again after DAV goes high.

As a result of the three-wire Transfer Bus, the rate at which data is transferred is determined only by the characteristics of the devices involved. This is what is meant by an asynchronous data and message transfer. Only those devices listened or talked are involved in the handshake when device dependent data is transmitted. Moreover, several devices can listen to the same data simultaneously. The transfer rate is then a function of the slowest peripheral device taking part in a transfer at any one time. This is an advantage when high-speed devices are configured to talk and listen at a high burst speed while slower devices are still in the system.

It needs to be noted, however, that all devices are required to handshake and respond to ATN messages; i.e., those control and address messages that are sent while the ATN (attention) line is true.

ATN (ATTENTION) MESSAGES

Attention messages can be broken down into four groups.

1. Address attention messages, i.e., talk and listen commands, program the devices to transmit or accept data.

   a. A talk address selects one device to send data and disables, or untalks, all the other devices equipped with talker functions from sending data. This allows only one talker on the bus at a time.

   b. The command to disable all devices with talker functions from talking is the UNT (untalk) message. UNT has a hexadecimal value of $5F.

   c. A listen address selects one device to receive data, but does not affect the others: they remain as they were, addressed or unaddressed. Thus, several devices may listen at the same time. Sending a talk address does not affect listeners, nor does sending a listen address affect a talker.

   d. The command to disable or stop all devices from listening is the UNL (unlisten) message. UNL has a hexadecimal value of $3F.

   e. Addresses are normally set by switches on the interior or exterior of a device. Each device must be assigned one or more addresses unique to it.

2. Universal ATN messages cause every device, so equipped, to perform the function defined in the IEEE Standard 488-1975. For example, the serial poll enable (SPE) message causes all those devices with serial poll capability to handle this command and move to the serial poll mode state (SPMS).

3. Addressed commands affect only those devices that are addressed. For example, the selective device clear (SDC) message only clears the device functions (not interface functions) of the devices that were previously listen-addressed. (Normal usage of a device clear is to put the device into its power-on state.)

4. Secondary commands are multiline messages that are always used in series with address, universal command, or addressed command messages (also referred to as primary commands) to form a longer version of each. Thus they extend the code space when necessary. Some devices, however, use the secondary commands as device dependent command messages.

INTERFACE FUNCTIONS

An interface function is the system element which provides the basic operational facility through which a device can receive, process, and send messages. There are ten interface functions which provide the system with communications and control capabilities. They consist of:

Source Handshake	SH
Acceptor Handshake	AH
Talker or Extended Talker	T or TE
Listener or Extended Listener	L or LE
Service Request	SR
Remote Local	RL
Parallel Poll	PP
Device Clear	DC
Device Trigger	DT
Controller	C

Each of these interface functions has a number of allowable subsets ranging from two for the Source and Acceptor Handshake functions, to 28 allowable subsets for the Controller function. The designer may choose the particular set of interface functions necessary to fit the particular device application. This implies, in interest of cost effectiveness, that it is not necessary to respond to all the GPIB lines, but rather only to those lines pertinent to the necessary functions of a particular device. For example, a device with listen-only mode capability requires the least number of signal lines to be implemented. These are:

1. The eight data lines, DI01 thru DI08.

2. The three transfer handshake lines, NRFD, NDAC, and DAV.

3. One management line, ATN.

SETUP PROCEDURE FOR GPIB OPERATION

FULL DISPLAY/FIRST TRIGGER SELECTOR OF 7D01 LOGIC ANALYZER

The Full Display/First Trigger Selector (P617, inside the 7D01) permits the user to select when the 7D01 will be triggered (switched from record to display mode) after the Manual Reset button has been pressed. A minimum number of clock pulses is required before the 7D01 will switch from record to display mode. The minimum number of pulses depends on the settings of the Full Display/First Trigger Selector (P617), Data Channels, and Data Position switches as shown in Table 3-1.

TABLE 3-1
Minimum clock pulses required to display data. (After the Manual Reset button is pressed.)

DATA CHANNELS	First Trigger Mode			Full Display Mode[1]		
	DATA POSITION			DATA POSITION		
	POST TRIG	CENTER	PRE TRIG	POST TRIG	CENTER	PRE TRIG
0-3	958	510	62	1982	1534	1086
0-7	497	255	31	991	767	543
GPIB→0-15	239	127	15	495	383	271

[1] **In Full Display mode, the 7D01 must have 1024 clock pulses with 0-3 data channels, 512 clock pulses with 0-7 data channels, and 256 clock pulses with 0-15 data channels before a trigger is accepted.**

The Full Display position of P617 is recommended for most repetitive signal applications. The First Trigger position of P617 is recommended for slow gated clock pulses and data, where there may not be enough clock pulses to cause the 7D01 to trigger or display data in the Full Display mode without a considerable waiting period. The First Trigger position is also recommended for a burst of clock and data where the clock and data occur at a reasonable rate, but where the quantity of clocks in the burst is less than the number necessary to change the 7D01 from record mode to display mode. See Table 3-1.

In Full Display mode, after the Manual Reset button has been pressed, the entire memory must be filled with new data before the 7D01 will accept a trigger. (This is indicated by illumination of the TRIG'D indicator light.) After the trigger is accepted, another block of data must be acquired (filling the memory a second time) before the 7D01 will switch from record mode to display mode. The size of this block of data depends on the Data Channels and Data Position switch settings on the 7D01. Refer to Table 3-1.

In First Trigger mode, it is not necessary to fill the entire 7D01 memory before a trigger is accepted. Instead, a trigger can be accepted at any time after the Manual Reset button is pressed and the first clock pulse is accepted. However, the data is not displayed until the minimum number of clock pulses are available. This may require a long wait for very slow gated systems; or display may never occur for a burst of clock pulses that stop. The additional clock pulses required to switch the 7D01 from record to display mode can be obtained by changing the Sample Interval switch from the EXT position to the 5 ms position after the data is recorded. The data recorded after the Sample Interval switch is changed to the 5 ms position is not valid, since that data was not clocked in by the external clock. (The data will represent the state of the lines sampled at a 5 ms rate.)

The position of selector P617, therefore, is a user decision, based on whether the GPIB is running in a continuous data transfer mode or in a burst mode. See Figure 3-3 for the location of P617.

GPIB ADAPTER

The GPIB Adapter is furnished as a standard accessory. It provides a quick means of connecting a standard GPIB connector to two P6451 Data Acquisition Probes. The two P6451 probes provide 16 channels of data input signals to the 7D01, plus the DAV clock input from the channels 0-7 probe and one qualifier input from the channel 8-15 probe.

The GPIB Adapter consists of a GPIB connector and interconnecting wires, terminating in two "combs." Each comb is inserted into the probe head of a P6451 probe. (Remove any probe leads from the probe head prior to inserting the comb.) Figure 3-4 depicts the GPIB adapter and provides a cross reference between the GPIB lines and the channels in the Logic Analyzer System.

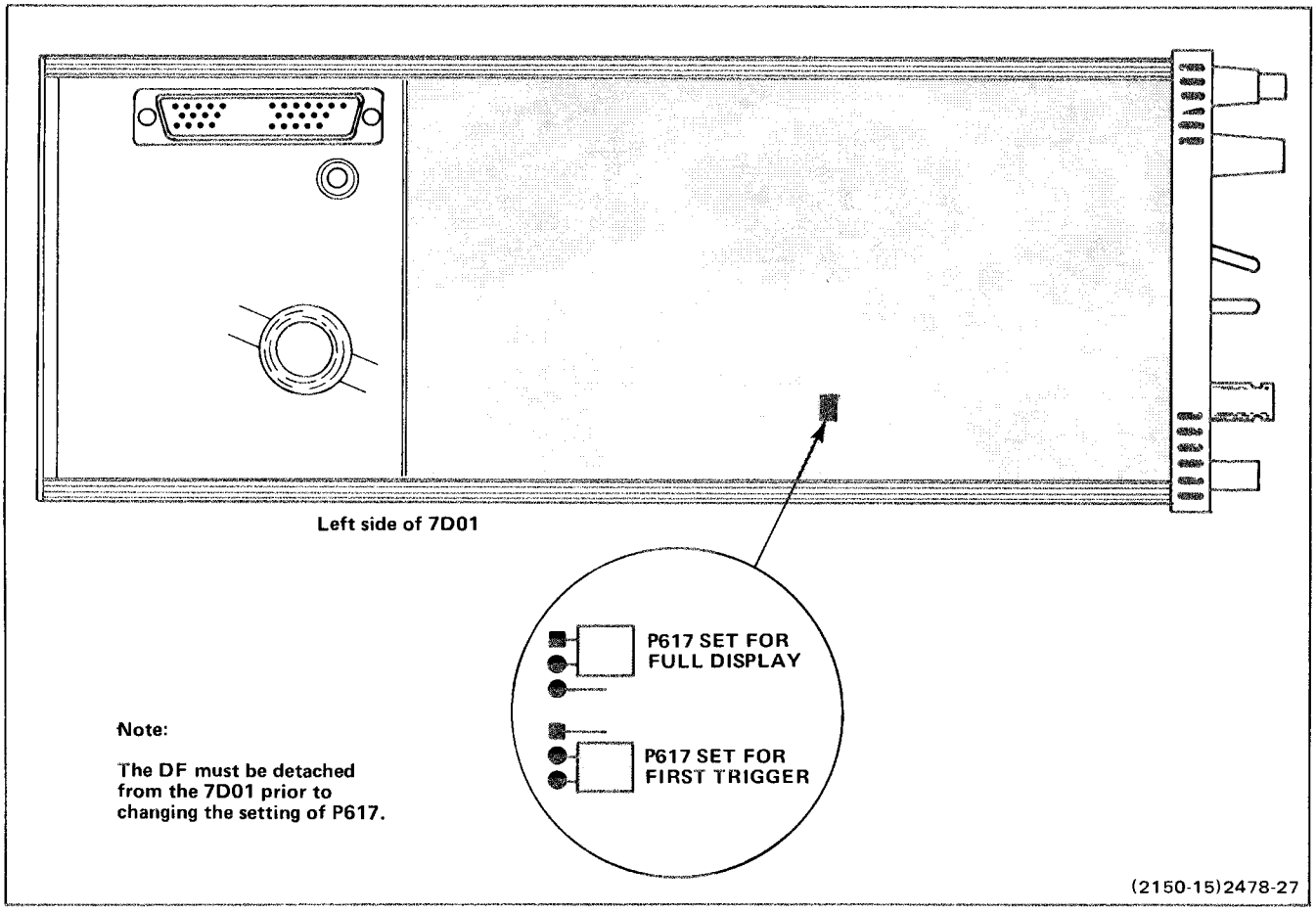


Figure 3-3. Location of 7D01 Full Display/First Trigger Selector.

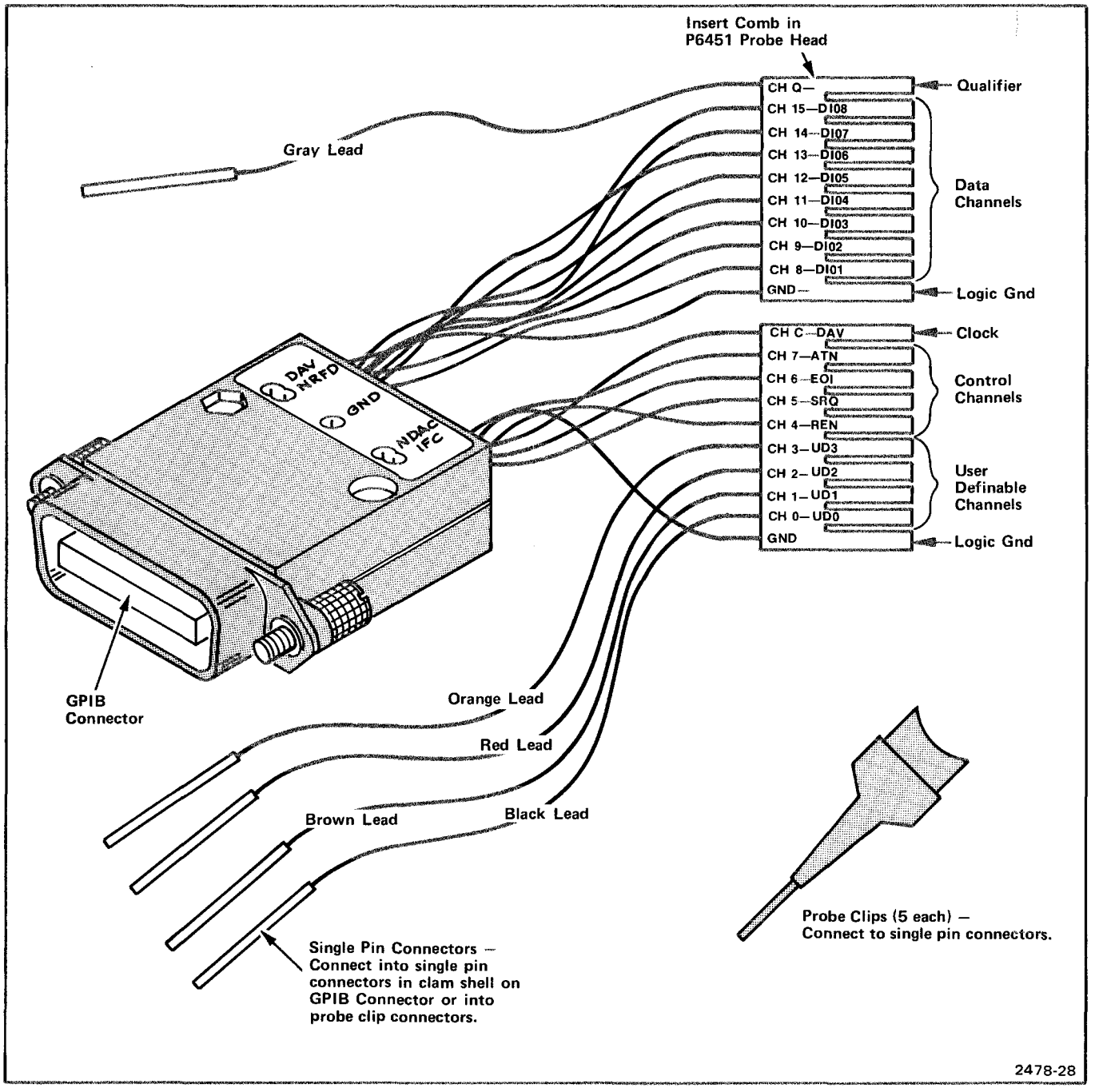


Figure 3-4. GPIB adapter.

Four holes with recessed single-pin connectors are provided in the "clam-shell" housing surrounding the GPIB connector. The recessed single-pin connectors are connected to the three handshake lines (DAV, NRFD, and NDAC) and control line (IFC) within the GPIB connector. Four user-definable leads (UDØ thru UD3) are connected to channels 0 thru 3 in the Chan 0-7 comb. The other end of these leads terminates in single-pin connectors. These user-definable leads may be connected to the recessed single-pin connectors in the GPIB connector in any desired order; however, it is recommended when observing the handshake cycle to connect DAV to UDØ, NRFD to UD1 and NDAC to UD2. If other connections are desired for the user-definable lines, probe clips are provided that connect to the single-pin connectors of UDØ thru UD3. The probe clips have a retractable hook that can be attached to a terminal, wire, or test point in the user circuitry.

INSTALLATION OF THE GPIB ADAPTER

Install the GPIB Adapter as follows:

1. Insert the two combs of the GPIB Adapter into the two P6451 probe heads. The combs are marked for channels 0-7 and channels 8-15. Follow the labeling to make sure each is inserted into the correct probe head.

2. Insert the two connectors of the P6451 probes into the input connectors on the 7D01. (Top connector — channels 0-7; bottom connector — channels 8-15.)

3. Connect the four user-definable lines as desired.

4. Connect the GPIB Adapter to the user's GPIB connector.

7D01 FRONT PANEL

Set the 7D01 Logic Analyzer controls as follows:

Sample Interval	Ext
Record Display Time	∞ (Full clockwise detent)
Data Channels	0-15
Data Position	Post Trig
Byte Switch	4 Bit
Trigger Source	W. R.
Ext Clock Polarity	⌐
W. R. Mode	Sync
Word Recognizer	CH 0-15 — set W.R. switches to trigger on particular bus transactions as described later in this section under the heading, GPIB TRIGGERING
External Qualifier	X (Don't care)
Probe Qualifier	X (Don't care)
Threshold Voltage	TTL (+1.4 V)

GPIB ACQUISITION AND DISPLAY

GENERAL

In GPIB mode of operation, the digital information on the interfacing bus lines is acquired synchronously using the negative-going edge of the GPIB DAV (Data Valid) line as a clock. Up to 254 instructions are stored in the 7D01 memory, then disassembled and displayed on the crt in IEEE Standard 488 mnemonic message format. The screen format allows 17 GPIB events to be displayed at one time as shown in Figure 3-5. As the data is "scrolled" manually, (by the 7D01 cursor control) all 254 events may be viewed.

The GPIB Adapter (furnished as a standard accessory) provides an interconnection between the GPIB and the 7D01, via the P6451 probes. This allows monitoring of up to sixteen interface bus lines at any one time.

MENU DISPLAY

When the MENU push button is depressed, the DF displays a Menu List on the crt. See Figure 3-5. Various operational modes are displayed in a numerical listing. The numbered Display push button, corresponding to the number in the Menu List, is selected to obtain the desired operational mode. If another operational mode is desired, the MENU push button must be depressed before each operational mode selection.

GPIB DISPLAY

GPIB mode of operation is assigned to position No. 1 in the Menu List (see Figure 3-5). This function enables the data, recorded in the 7D01 memory from the GPIB Adapter, to be displayed in a tabular format.

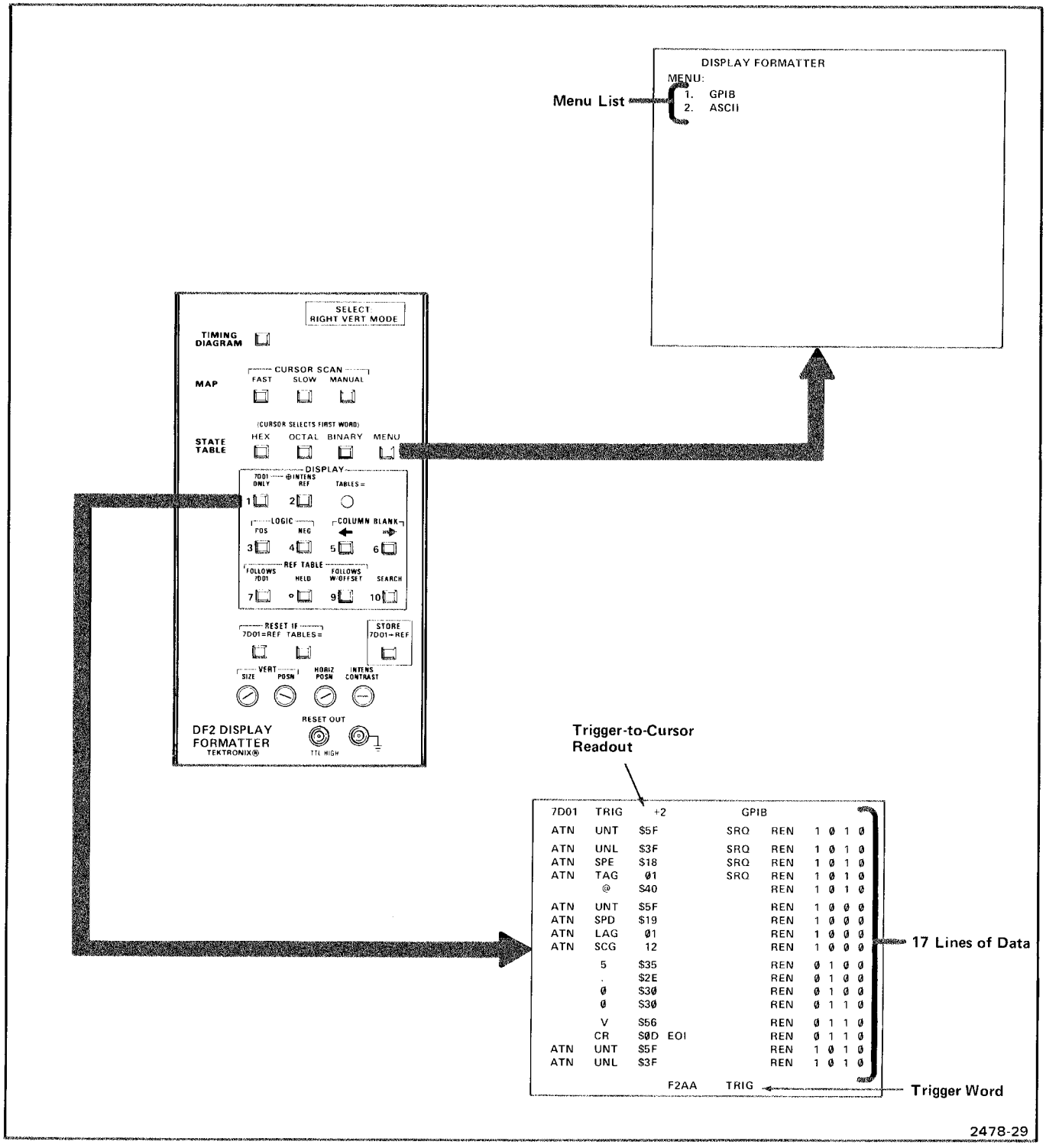


Figure 3-5. GPIB operational mode display.

GPIB CRT DISPLAY

The tabular format consists of:

1. Trigger-to-cursor readout.

   a. Located at the top (first line) of the crt.

   b. Indicates the position of the cursor, relative to the trigger. Readout is in a + or – decimal number of external clocks.

   c. The word "GPIB" is also displayed on the top line, indicating that the crt is displaying GPIB data information.

2. Trigger word readout.

   a. Located at the bottom (19th line) of the crt.

   b. Trigger word is displayed in its hex, octal, or binary equivalent numbers, depending on which state table push button (HEX, OCTAL, or BINARY) was depressed prior to selecting the MENU push button. See Figure 3-6.

3. Seventeen lines of data in IEEE Standard 488 mnemonic message format.

   a. Located between the top and bottom lines (trigger-to-cursor and trigger word readouts).

   b. The information contained in the 17 lines is a 17-event data segment of the 254 events (instructions) stored at any one time in the 7D01 memory. As the data is "scrolled" manually, (by the 7D01 cursor control) all 254 events may be viewed.

   c. Each line (bus transaction) on the crt contains data information from the interface bus. Up to 16 bus lines may be connected through the GPIB Adapter via the P6451 probes to the 16 channels in the 7D01. Figure 3-7 depicts the relationship of the 16 channels in the 7D01 to each line readout on the crt display and describes the mnemonic representation of the GPIB signal lines.

   d. The functions of the 16 bus lines are defined as follows:

   - Four control lines: ATN, EOI, SRQ, and REN. (CH 4-7)
   - Eight data bus lines. (CH 8-15)
   - Four user-definable lines, used to provide additional circuit information. (CH 0-3)

Control Lines (Channels 4-7)

The four control lines are displayed on the crt in GPIB mnemonic form as ATN, EOI, SRQ, and REN. The mnemonic for each control line is displayed on the crt when the line is asserted true (the GPIB lines are active low).

Data Bus Lines (Channels 8-15)

The information contained on the eight data lines of the interface bus represent control or address messages whenever the ATN line is set true (active low). The mnemonic message format for these ATN messages displayed on the crt is in accordance with the multiline interface message format specified in IEEE Standard 488-1975. Figure 3-8 is a conversion table showing the relationship of the mnemonic messages to their equivalent hex or binary value.

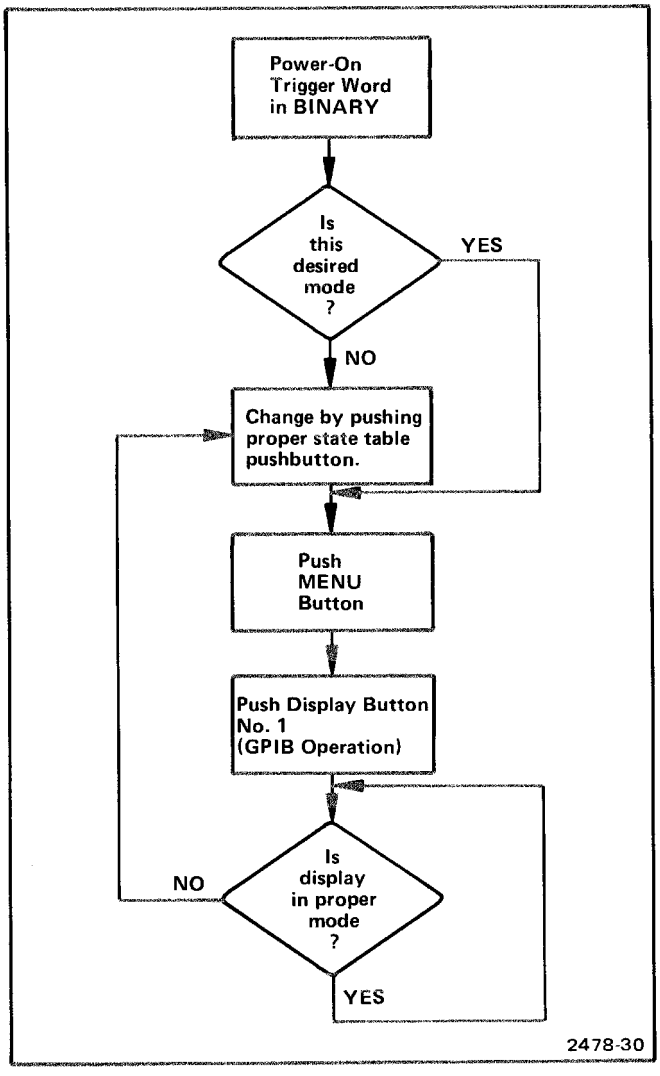


Figure 3-6. Changing trigger word readout in GPIB operation.

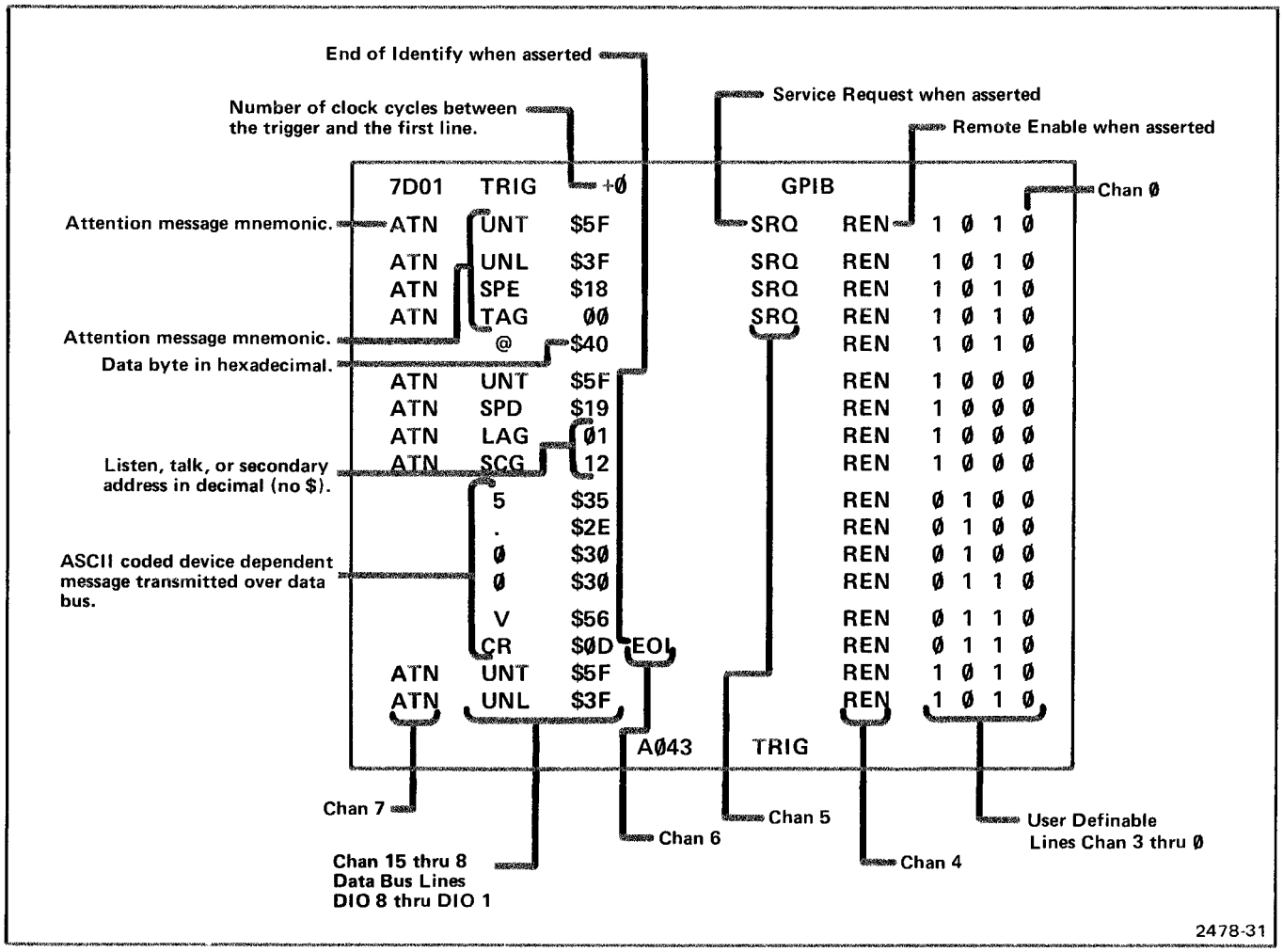


Figure 3-7. Typical DF GPIB display showing disassembled instructions in IEEE Standard 488-1975 message mnemonics.

MULTILINE INTERFACE MESSAGES SENT AND RECEIVED ON THE DATA BUS WITH ATN (ATTENTION) TRUE

LEAST SIGNIFICANT BITS (DIO 1 thru 4)					MOST SIGNIFICANT BITS (DIO 5 thru 7)							
Bits: b_7					Ø	Ø	Ø	Ø	1	1	1	1
b_6					Ø	Ø	1	1	Ø	Ø	1	1
b_5					Ø	1	Ø	1	Ø	1	Ø	1
BINARY b_4	b_3	b_2	b_1	HEX	$SØ	$1	$2	$3	$4	$5	$6	$7
Ø	Ø	Ø	Ø	Ø	- - -	- - -	ØØ	16	ØØ	16	ØØ	16
Ø	Ø	Ø	1	1	GTL	LLO	Ø1	17	Ø1	17	Ø1	17
Ø	Ø	1	Ø	2	- - -	- - -	Ø2	18	Ø2	18	Ø2	18
Ø	Ø	1	1	3	- - -	- - -	Ø3	19	Ø3	19	Ø3	19
Ø	1	Ø	Ø	4	SDC	DCL	Ø4	2Ø	Ø4	2Ø	Ø4	2Ø
Ø	1	Ø	1	5	PPC	PPU	Ø5	21	Ø5	21	Ø5	21
Ø	1	1	Ø	6	- - -	- - -	Ø6	22	Ø6	22	Ø6	22
Ø	1	1	1	7	- - -	- - -	Ø7	23	Ø7	23	Ø7	23
1	Ø	Ø	Ø	8	GET	SPE	Ø8	24	Ø8	24	Ø8	24
1	Ø	Ø	1	9	TCT	SPD	Ø9	25	Ø9	25	Ø9	25
1	Ø	1	Ø	A	- - -	- - -	1Ø	26	1Ø	26	1Ø	26
1	Ø	1	1	B	- - -	- - -	11	27	11	27	11	27
1	1	Ø	Ø	C	- - -	- - -	12	28	12	28	12	28
1	1	Ø	1	D	- - -	- - -	13	29	13	29	13	29
1	1	1	Ø	E	- - -	- - -	14	3Ø	14	3Ø	14	3Ø
1	1	1	1	F	- - -	- - -	15	UNL	15	UNT	15	31

(ACG) ADDRESSED COMMAND GROUP

(UCG) UNIVERSAL COMMAND GROUP

(LAG) LISTEN ADDRESS GROUP

(TAG) TALK ADDRESS GROUP

SECONDARY COMMAND GROUP (SCG)

PRIMARY COMMAND GROUP (PCG)

2478-32

Figure 3-8. Hex and binary to mnemonic message conversion table.

These ATN messages are categorized as follows, with their hexadecimal or decimal value(s).

Addressed Command Group	GTL	$Ø1	Data in hex ($) values. (See Notes 1 and 3)
	SDC	$Ø4	
	PPC	$Ø5	
	GET	$Ø8	
	TCT	$Ø9	
Universal Command Group	LLO	$11	Data in hex ($) values. (See Notes 1 and 3)
	DCL	$14	
	PPU	$15	
	SPE	$18	
	SPD	$19	
Listen Address Group	LAG	ØØ thru 3Ø	Address displayed in decimal. (see Note 2.)
	UNL	$3F	Value of UNL in hex ($). (See Note 1.)
Talk Address Group	TAG	ØØ thru 3Ø	Address displayed in decimal. (See Note 2.)
	UNT	$5F	Value of UNT in hex ($). (See Note 1.)
Secondary Command Group	SCG	ØØ thru 31	Address displayed in decimal. (see Note 2.)

NOTES:

1. All hex values displayed are identified by the dollar sign ($) preceding the numeric or alphanumeric hex value.

2. The numeric value of an address message is in decimal (base 10), and is not preceded by the dollar sign. Figure 3-8 may be used to convert this number to either a hex or binary number. (e.g., TAG 28 is equivalent to a hex value of $5C or a binary value of 101 1100.)

3. An ATN message that is "not defined," will be displayed with an intensified hex value. Refer to Figure 3-8 to verify that a displayed message is "not defined". (e.g, ATN **$ØD** – The "$ØD" is intensified since it is a "not defined" message.)

Device-Dependent Messages

The controller may address itself as a talker or a listener. After the controller has addressed all listeners and one talker via 7-bit coded interface messages (when ATN is true), any commonly understood binary, BCD, or alpha-numeric code may be used to transfer data between peripheral devices, once the ATN line becomes unasserted (passive high). The standard ASCII code is the most commonly used code. Figure 3-9 is a conversion table to convert ASCII characters to hex or binary values.

User-Definable Lines (Channels Ø–3)

The four user-definable lines may be connected to the three handshake lines (DAV, NRFD, and NDAC) and control line (IFC) at the GPIB Adapter connector. Or, if desired, they may be connected to other points within the user's circuitry. The binary value of each line is displayed on the right of the crt. See Figure 3-7.

LEAST SIGNIFICANT BITS →				MOST SIGNIFICANT BITS →								
Bits: b_7 →				Ø	Ø	Ø	Ø	1	1	1	1
b_6 →				Ø	Ø	1	1	Ø	Ø	1	1
b_5 →				Ø	1	Ø	1	Ø	1	Ø	1
BINARY ↓				HEX ↓							
b_4	b_3	b_2	b_1	→	$\$Ø$	$\$1$	$\$2$	$\$3$	$\$4$	$\$5$	$\$6$	$\$7$
Ø	Ø	Ø	Ø	Ø	NUL	DLE	SP	Ø	@	P	<'>	<P>
Ø	Ø	Ø	1	1	SOH	DC1	!	1	A	Q	<A>	<Q>
Ø	Ø	1	Ø	2	STX	DC2	"	2	B	R	<B>	<R>
Ø	Ø	1	1	3	ETX	DC3	#	3	C	S	<C>	<S>
Ø	1	Ø	Ø	4	EOT	DC4	$	4	D	T	<D>	<T>
Ø	1	Ø	1	5	ENQ	NAK	%	5	E	U	<E>	<U>
Ø	1	1	Ø	6	ACK	SYN	&	6	F	V	<F>	<V>
Ø	1	1	1	7	BEL	ETB	'	7	G	W	<G>	<W>
1	Ø	Ø	Ø	8	BS	CAN	(	8	H	X	<H>	<X>
1	Ø	Ø	1	9	HT	EM	)	9	I	Y	<I>	<Y>
1	Ø	1	Ø	A	LF	SUB	*	:	J	Z	<J>	<Z>
1	Ø	1	1	B	VT	ESC	+	;	K	[	<K>	<[>
1	1	Ø	Ø	C	FF	FS	,	<	L	\	<L>	<\>
1	1	Ø	1	D	CR	GS	-	=	M	]	<M>	<]>
1	1	1	Ø	E	SO	RS	.	>	N	^	<N>	<^>
1	1	1	1	F	SI	US	/	?	O	_	<O>	DEL

2478-33

Figure 3-9. Hex and binary to ASCII conversion table.

@

SECONDARY FUNCTIONS OF DISPLAY PUSH BUTTONS

During GPIB display, DISPLAY push buttons 3 through 6 (LOGIC POS, LOGIC NEG, COLUMN BLANK←, and COLUMN BLANK→) perform their normal functions, affecting the four user-definable line columns only. The remaining DISPLAY push buttons (7, 8, 9, and 10) have no effect on the GPIB display.

When entering GPIB mode from a power-on state, the LOGIC POS button is backlit. This indicates that the user-definable lines (represented by columns of ones and zeros on the right portion of the crt) are displayed in positive logic (Ø = logic low and 1 = logic high). To represent the user-definable lines in negative logic (Ø = logic high and 1 = logic low), push the LOGIC NEG button. When this state is selected the LOGIC NEG button is backlit. Depressing the COLUMN BLANK→ push button blanks the user-definable columns (channels 3, 2, 1, and 0), in that order. Depressing the COLUMN BLANK← push button restores the columns (channels 0, 1, 2, and 3), in that order. Momentarily depressing the buttons will blank or restore one column at a time. Holding either button down will cause the function to automatically blank or unblank all columns. The user may wish to column blank all the user-definable lines to exclude them from photographic documentation. Whenever any columns are blanked, both push buttons are backlit.

GPIB TRIGGERING

GENERAL DESCRIPTION AND FEATURES

The versatile word recognizer feature of the 7D01 allows considerable flexibility in triggering on any particular transaction over the GPIB. For most triggering needs, the word recognizer mode should be synchronous. (The word recognizer will trigger the 7D01 on the falling edge of the Data Valid (DAV) clock signal, when all word recognizer conditions are met; i.e., when there is a match between the W.R. switches and the input lines.) When the 7D01 is triggered, the green LED (TRIG'D) on the front panel of the 7D01 lights, to indicate the triggered condition.

NOTE

Two trigger modes exist in the 7D01:

1. First Trigger mode — The 7D01 is triggered when the first W.R. condition goes true, after at least one clock pulse has occurred to arm the W. R.

2. Full Display mode — After 256 clocks have cleared the memory, followed by the W.R. condition going true, the 7D01 is triggered.

Asynchronous triggering of the 7D01 is useful for storing data from an event that is not synchronous with the DAV clock. An example of this is triggering on Interface Clear (IFC), which can be asynchronous to the DAV clock.

While the word recognizer is used most often to trigger the 7D01 on the occurrence of a specified event, it can also be used to look for illegal states of the GPIB. If the logic analyzer is triggered with the W. R. switches in a position representing an illegal GPIB state, the data captured before and after the trigger can be useful in uncovering the cause of the error. This is especially useful in the design phase of a GPIB interface. For example, if the GPIB system configuration does not implement or use parallel poll, then the W. R. can be set to trigger the 7D01 on the simultaneous occurrence of ATN and EOI. Triggering on this event would indicate an error; the cause of the error could then be investigated by viewing the data captured.

The GPIB Adapter, an accessory of the DF, provides twelve dedicated lines from the GPIB to the Word Recognizer inputs in the 7D01. These dedicated lines and associated inputs are listed as follows:

GPIB Lines	W.R. Channels (7D01)
REN (Remote Enable)	4
SRQ (Service Request)	5
EOI (End or Identify)	6
ATN (Attention)	7
DI01	8
DI02	9
DI03	10
DI04	11
DI05	12
DI06	13
DI07	14
DI08	15

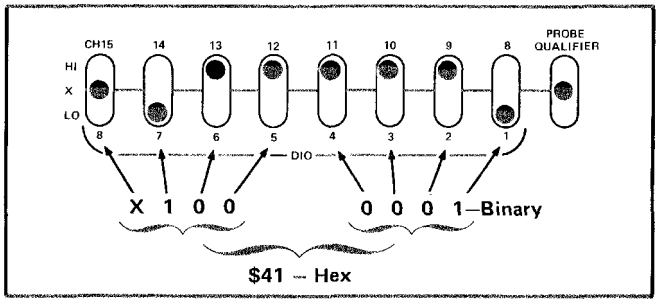
NOTE

In the synchronous W. R. mode, the clock is the negative-going edge of the DAV signal. This clock synchronously clocks data into the memory and compares this data to the settings of the W. R. switches. If the data and settings are the same, a pulse the length of the clock pulse is transferred to the W. R. output. The DAV line going true (active low) is a signal from a talking unit to each listener that a new byte is valid on the data lines.

Four user-definable (UD) lines (UDØ through UD3), connected to W. R. channels 0 through 3, can be used for additional trigger qualification. The probe qualifier input from the channel 8-15 probe and external qualifier may be used similarly. The lines can be attached, for example, to a user's internal GPIB circuitry to provide further ability to trigger the 7D01 on a specific GPIB transaction.

For triggering on a GPIB event, the most important point to remember is that the bus is defined in negative logic. This means that a true (active) signal is a LOW signal to the word recognizer. For example, when ATN is asserted it means a LOW voltage appears at the input to channel 7 in the word recognizer. This also applies to the other control lines, channels 4, 5, and 6.

The GPIB data lines are also expressed in negative logic. These lines contain information regarding a specific GPIB interface message or device-dependent message. The binary value of a specific message is set into the W. R. switches (CH 8-15). For example, the ASCII character "A" has a hex value of $41, and a binary value of X100 0001. Thus, to recognize the data byte "A", set the W. R. switches as shown below:



ATN (ATTENTION MESSAGE TRIGGERING)

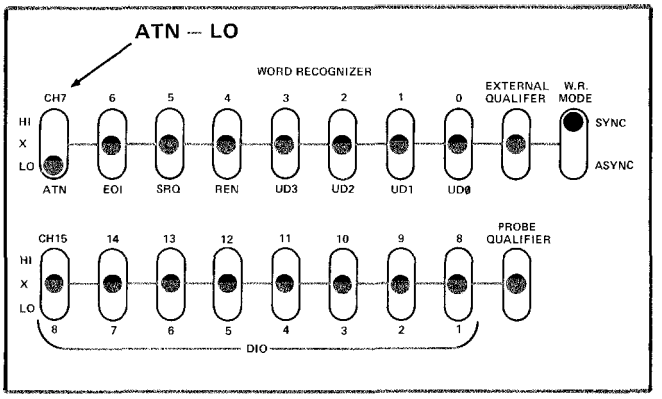
To effectively analyze the conditions on the GPIB it is important to be able to trigger the 7D01 on any one of the following ATN messages.

1. Trigger on any ATN message.
2. Trigger on any ATN message group.
3. Trigger on a specific ATN message.

TRIGGER ON ANY ATN MESSAGE

To trigger the 7D01 on the first ATN message after the Reset button is pushed, set the W. R. switches as follows:

ATN – CH 7	LO
All other W.R. switches	X (don't care)



TRIGGER ON ANY ATN MESSAGE GROUP

The 7D01 may be triggered on the first ATN message within a specified group. There are five group categories of ATN messages.

ACG (Addressed Command Group)	X000 XXXX
UCG (Universal Command Group)	X001 XXXX
LAG (Listen Address Group)	X01X XXXX
TAG (Talk Address Group)	X10X XXXX
SCG (Secondary Command Group)	X11X XXXX

When the 7D01 is triggered on an ATN message group, the W. R. switches for channels 8-15 (corresponding to the data lines, DI01 thru DI08) must be set to recognize the desired group. The higher-order bits define the groups and the lower-order bits define a specific address or message within the group. To trigger the 7D01 on an ATN message group set the W. R. switches as follows:

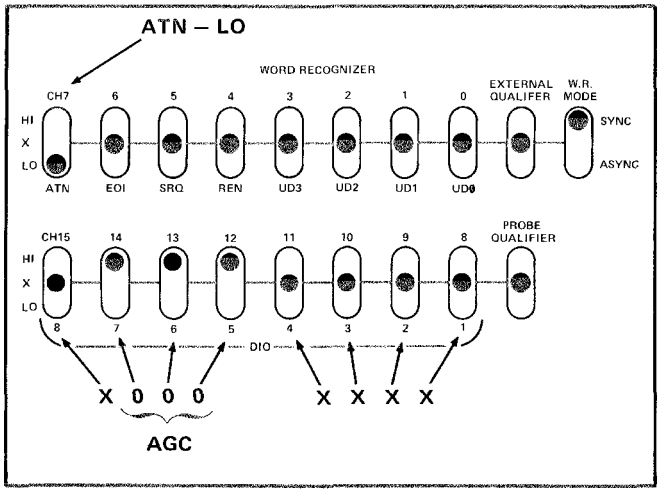
@

ACG (Addressed Command Group)

X 0 0 0 X X X X – Binary value

ATN – CH 7 LO

CH15-8 – X HI HI HI X X X X



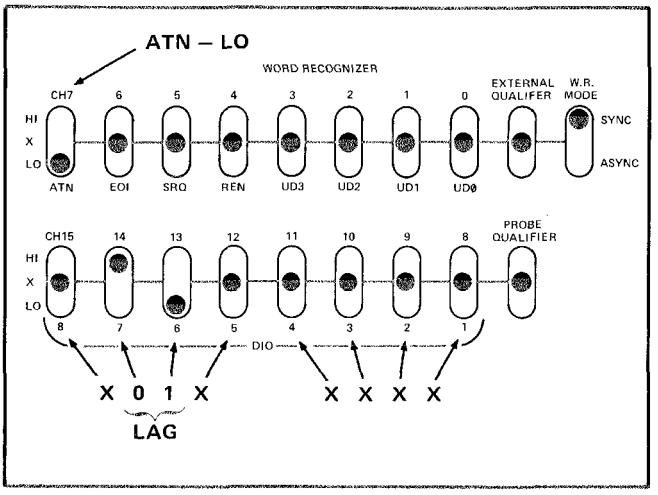
LAG (Listen Address Group)

$20 – $3F – Hex value range

X 0 1 X X X X – Binary value

ATN – CH 7 –LO

CH15-8 – X HI LO X X X X X

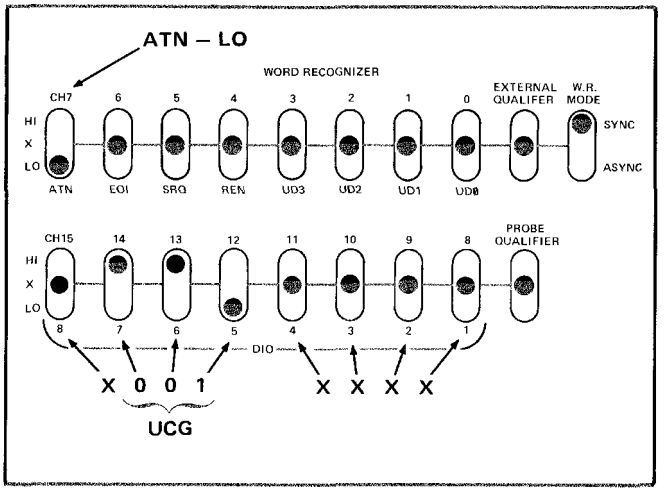


UCG (Universal Command Group)

X 0 0 1 X X X X – Binary value

ATN – CH 7 LO

CH15-8 – X HI HI LO X X X X



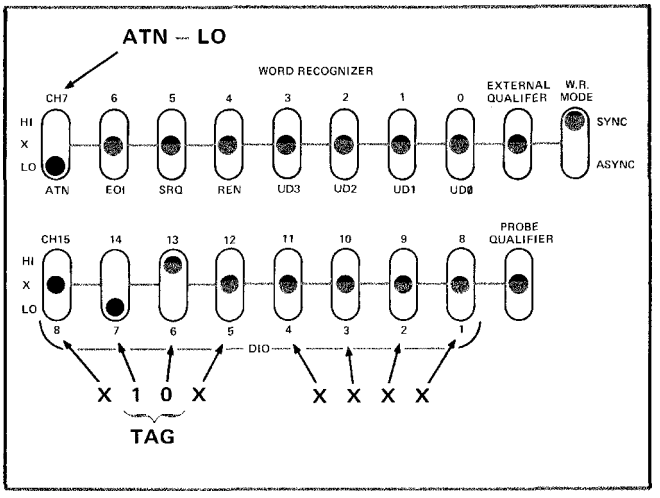
TAG (Talk Address Group)

$40 – $5F – Hex value range

X 1 0 X X X X X – Binary value

ATN – CH7 – LO

CH15-8 – X LO HI X X X X X



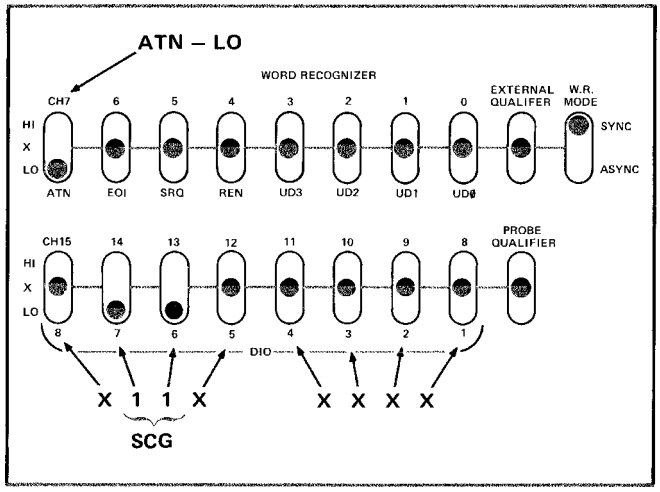
SCG (Secondary Command Group)

$60 – $7F –Hex value range

X 1 1 X X X X X – Binary value

ATN – CH7 –LO

CH15-8 – X LO LO X X X X X



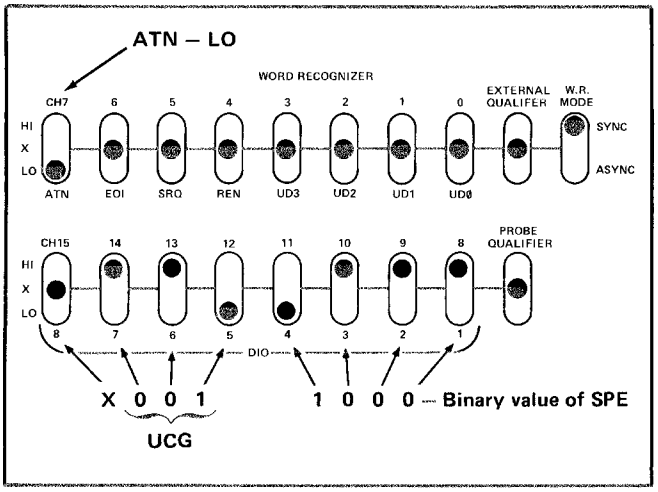
SPE (Serial Poll Enable)

$18 – Hex value

X 0 0 1 1 0 0 0 –Binary value

ATN – CH7 –LO

CH15-8 – X HI HI LO LO HI HI HI



TRIGGER ON A SPECIFIC ATN MESSAGE

The 7D01 may be triggered on any specified ATN message within any of the five groups. See Figure 3-8 for a complete listing of all ATN messages with their hex and binary values.

The lower order bits of the data lines define the specific address or message within any of the five groups previously listed. To trigger the 7D01 on a specific ATN message set the W. R. switches as defined in the following examples.

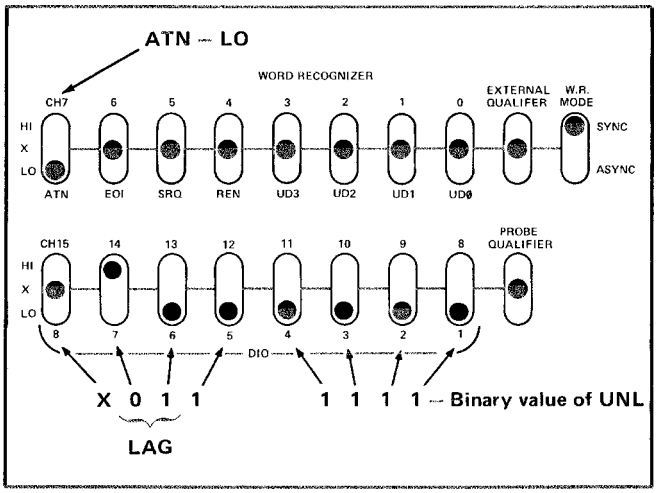
UNL (Unlisten)

$3F – Hex value

X 0 1 1 1 1 1 1 – Binary value

ATN – CH7 –LO

CH15-8 – X HI LO LO LO LO LO LO



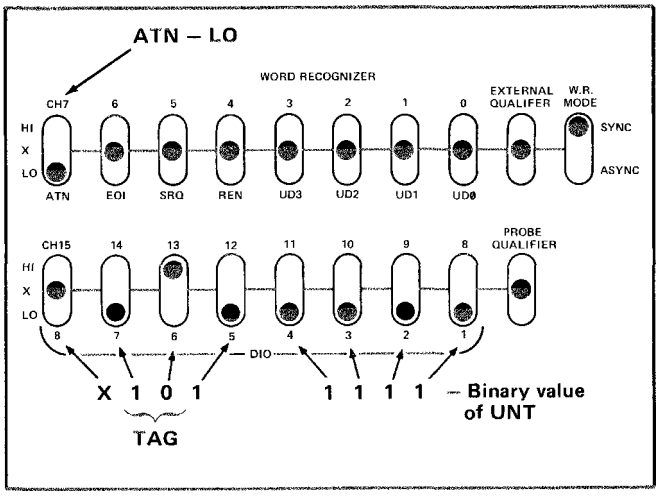
UNT (Untalk)

$5F – Hex value

X 1 0 1 1 1 1 1 –Binary value

ATN – CH7 –LO

CH15-8 – X LO HI LO LO LO LO LO



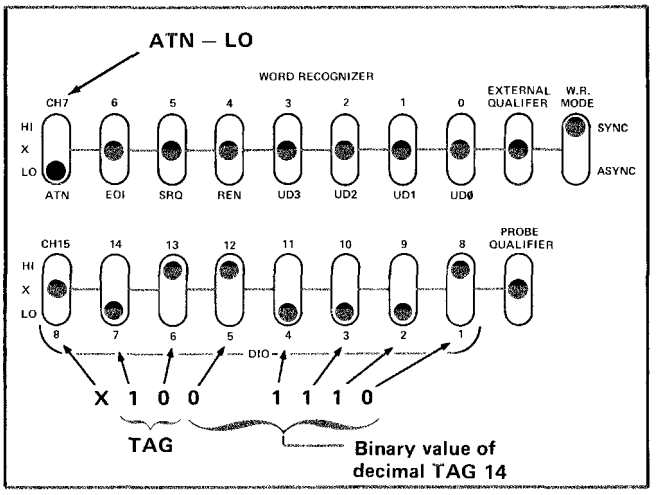
TAG 14

$4E – Hex value

X 1 0 0 1 1 1 0 –Binary value

ATN – CH7 –LO

CH15-8 – X LO HI HI LO LO LO HI



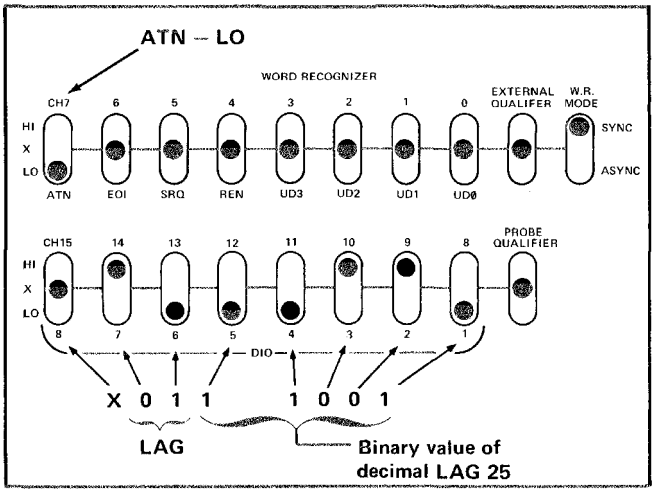
LAG 25

$39 – Hex value

X 0 1 1 1 0 0 1 –Binary value

ATN – CH7 –LO

CH15-8 – X HI LO LO LO HI HI LO



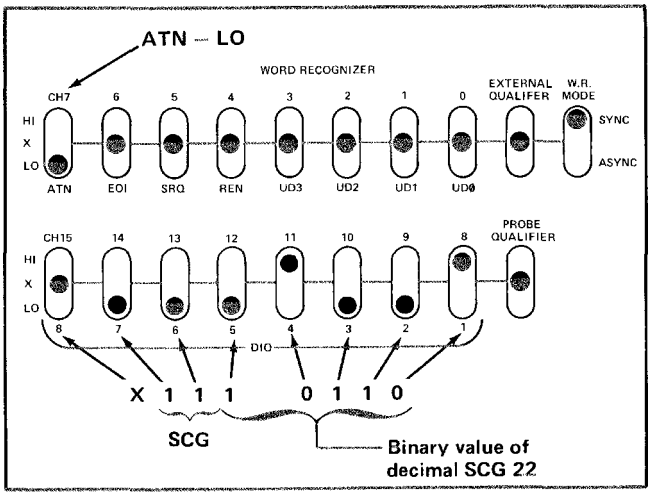
SCG 22

$76 – Hex value

X 1 1 1 0 1 1 0 –Binary value

ATN – CH7 –LO

CH15-8 – X LO LO LO HI LO LO HI



NON-ATN MESSAGE TRIGGERING

TRIGGERING ON ANY NON-ATN MESSAGE

Non-ATN messages are device-dependent messages transferred over the GPIB when the ATN line is false (passive high). To trigger the 7D01 on any non-ATN message, set the CH 7 W. R. switch HI and all the other W. R. switches to X (don't care). The 7D01 will be triggered on the first non-ATN message after the Reset button is pushed.

TRIGGERING ON A SPECIFIC NON-ATN MESSAGE

To trigger on a specific non-ATN message the W. R. switches (CH15-8), corresponding to the data lines, must be set to the negative logic value of the data byte for that specific message. Figure 3-9 depicts device-dependent messages for the ASCII code. To trigger on "carriage return" (CR), set the W. R. switches as shown in the following example:

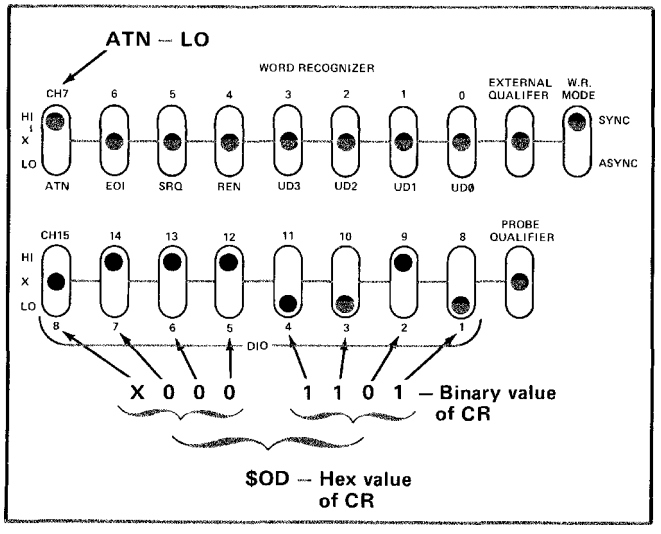
CR (Carriage Return)

$0D – Hex value

X 0 0 0 1 1 0 1 – Binary value

ATN – CH7 –HI

CH15-8 – X HI HI HI LO LO HI LO



Some controllers such as the TEKTRONIX 4051, have the capability to drive data line DI08. In instances when transmitting non-ASCII data, the user may want to trigger on a data byte containing all eight-bits. The W. R. switch for Channel 15 may then be set for either a LO or HI, along with the other seven data switches.

CONTROL LINE TRIGGERING

The 7D01 may also be triggered on any of the other control lines (EOI, SRQ, and REN) or the user definable lines (UDØ thru UD3). To trigger on any of these lines set the corresponding W. R. switch to LO, and the W. R. switches for all other channels to X (don't care). The user-definable lines may be connected to any of the single-pin connectors (DAV, NRFD, NDAC, and IFC) provided in the GPIB Adapter for additional GPIB triggering capability. Refer to Figure 3-4.

GPIB TIMING

The ability to display and evaluate transactions over the GPIB in asynchronous timing mode can uncover problems that would not be found with synchronous data acquisition. Ansynchronous timing can show errors in the implementation of the state diagrams that define the GPIB in IEEE Standard 488-1975. It can also be used to observe and determine the GPIB speed of operations.

CORRECT HANDSHAKE

When observing GPIB operations, look first at the handshake cycle, especially if the GPIB is not working properly. The following procedure lists the steps required to observe the GPIB handshake cycle.

1. Connect the user-definable lines in the GPIB Adapter as follows: (Refer to Figure 3-4.)

   a. Connect UDØ (black lead) to DAV (Data Valid).

   b. Connect UD1 (brown lead) to NRFD (Not Ready For Data).

   c. Connect UD2 (red lead) to NDAC (Not Data Accepted).

2. Connect the GPIB Adapter to a GPIB connector of the system being tested.

3. Use the following 7D01 Front Panel Control Settings:

Data Channels	Ø – 3
Threshold Voltage	TTL (+1.4 V)
Sample Interval	Set between 5 ms and 10 10 ns. Setting depends on how fast the GPIB handshake is operating and what the user wants to observe.
W. R. Mode	ASYNC

4. Push the Manual Reset button to start the 7D01 acquiring new data.

5. Push the Manual Trigger button to switch the 7D01 from acquisition mode to display mode.

6. Push the TIMING DIAGRAM button on the DF and adjust the 7D01 Horizontal and Vertical controls for a full scale display of channels 0 through 3 on the crt.

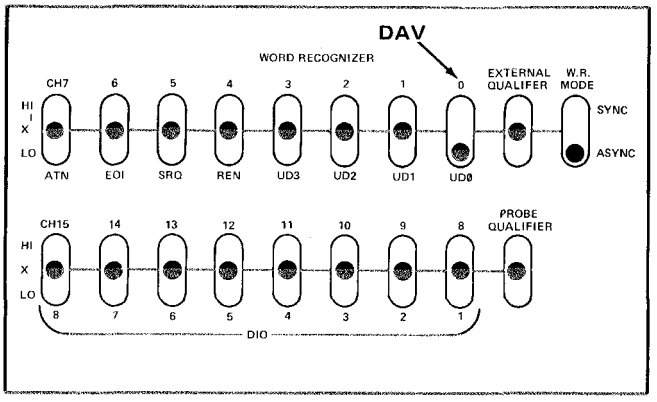
7. Adjust the sample interval switch and push the Reset button to reacquire data, until the timing diagram on the crt resembles the handshake timing diagram shown in Figure 3-10.

All six states, A thru F, must be in the exact order depicted in Figure 3-10 for the handshake cycle to be working correctly. (Refer to GPIB Overview previously described in this section.) If no handshake is occurring on the crt display, the level of the three lines will indicate what state the handshake is in. For additional information refer to the AH (Acceptor Handshake) State Diagram in Figure 3-11 and IEEE Standard 488-1975.

ASYNCHRONOUS TRIGGERING

The ability to observe a specific event across the GPIB is important in finding errors or studying the speed and execution of the GPIB. The 7D01 triggering versatility makes possible the observation of these events. To trigger the 7D01 on any DAV signal going low, set the W. R. switches as follows:

CH Ø = UDØ = DAV	LO
CH 1 = UD1 = NRFD	X
CH 2 = UD2 = NDAC	X
CH 3 = UD3	X
External Qualifier	X
All other W. R. switches	X



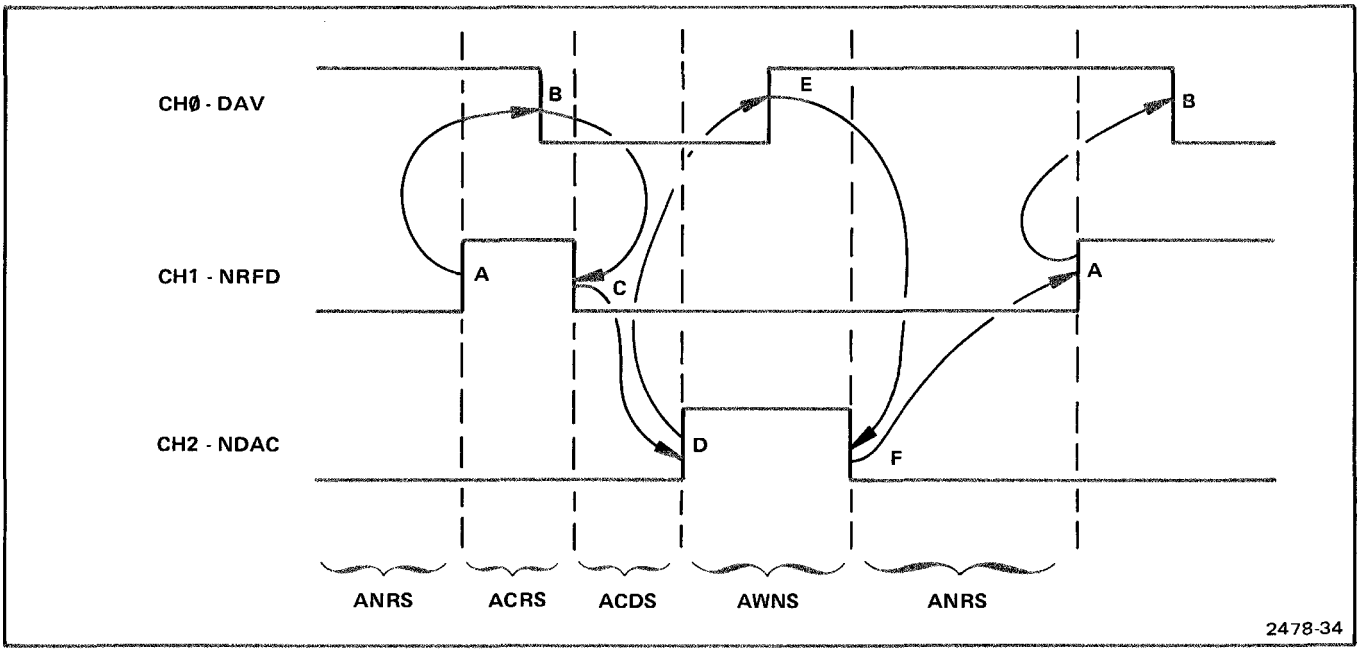


Figure 3-10. GPIB handshake timing diagram.

The user can observe the three GPIB handshake lines on the crt, after the 7D01 has been triggered by some event internal to the circuitry of the device under test or evaluation. For example, the UD3 line can be attached to the user circuitry, trigger the 7D01, and be displayed on the crt as a fourth channel along with the GPIB handshake lines.

When observing the handshake cycle in the four channel mode, only channels 0 through 3 are sampled and displayed on the crt. However, all 16 channels, plus the probe and external qualifier signals, can be used to qualify the triggering of the 7D01. The External Trig/Qualifier Input (BNC) connector on the 7D01 front panel is also available for user qualification. Set the corresponding polarities to whichever edge is to trigger the W. R. (Switch is set HI for the positive-going edge, or LO for the negative-going edge).

The W. R. Mode switch should be in the ASYNC (asynshronous mode) position when sampling with the 7D01 internal clock.

NOTE

In the asynchronous mode the Filter knob, on the front panel of the 7D01, controls the time that the word recognizer output must be true before the 7D01 is triggered. If the Filter is set for 300 ns (fully clockwise), the input word to the W. R. switches has to be true for at least 300 ns, or the 7D01 will not be triggered. This feature prevents the 7D01 from being triggered falsely on a glitch lasting less than the time setting of the Filter knob.

If it is necessary to observe the control and data lines of the GPIB along with the handshake lines, the 7D01 Data Channels switch should be set to 16 channel mode (0-15 position). It may be useful to look at the handshake lines in relationship to ATN (Attention – Channel 7). The handshake lines may be observed after, or before and after, the occurrence of ATN.

To observe the handshake lines after the first occurrence of ATN, set the 7D01 switches as follows:

Data Position	Post Trigger
CH 7 = ATN	LO
All other W. R. switches	X (don't care)

To observe the handshake lines both before and after ATN is unasserted (line goes HI), set the 7D01 switches as follows:

Data Position	Center Trigger
CH 7 = ATN	HI
All other W. R. switches	X

To look at the handshake or timing on the last data byte handshaked in a device-dependent message (assuming the talker asserts EOI on the last byte), set the W. R. switches as follows:

CH 6 = EOI	LO
CH 7 = ATN	HI
All other W. R. switches	X

To observe how a parallel poll is handled over the GPIB and how long it takes, set the W. R. switches as follows:

CH 6 = EOI	LO
CH 7 = ATN	LO
All other W. R. switches	X

Further details on GPIB triggering is provided in detail earlier in this section under GPIB TRIGGERING.

TIME MEASUREMENTS

The measurement of time between GPIB events is required for evaluation of system speed and individual device speed. It is useful in the design stages for studying and improving the bus performance. It is also useful in determining what portion of the bus design should be implemented in hardware and what should be handled by a microprocessor.

The following text describes how to obtain differential time measurements using the 7D01 cursor-to-trigger readout and cursor controls. Push the TIMING DIAGRAM push button on the DF and obtain a timing display of the crt. The Data Channels switch on the 7D01 may be in either 4, 8, or 16 channel position, depending on what timing measurements the user desires. Using fewer lines on the crt allows more data storage and hence more accuracy, if the time of the sample interval is decreased. Adjust the display positioning controls as desired. To measure the differential time between two negative-going edges for the same channel, follow this sequence:

1. Position the intensified cursor immediately past the first negative edge. (Cursor course and fine controls may be used; however, the final setting of the above position should be set with the fine control.)

2. Record the decimal number of the trigger-to-cursor readout. This value will be referred to as T_1.

3. Move the intensified cursor to the right (using both course and fine cursor controls) until it is immediately past the second negative edge.

4. Record this value as T_2.

5. Subtract T_1 from T_2 ($T_2 - T_1$). This value is the number of samples taken between the two negative-going edges. (Subtract the numbers algebraically, observing the proper sign.)

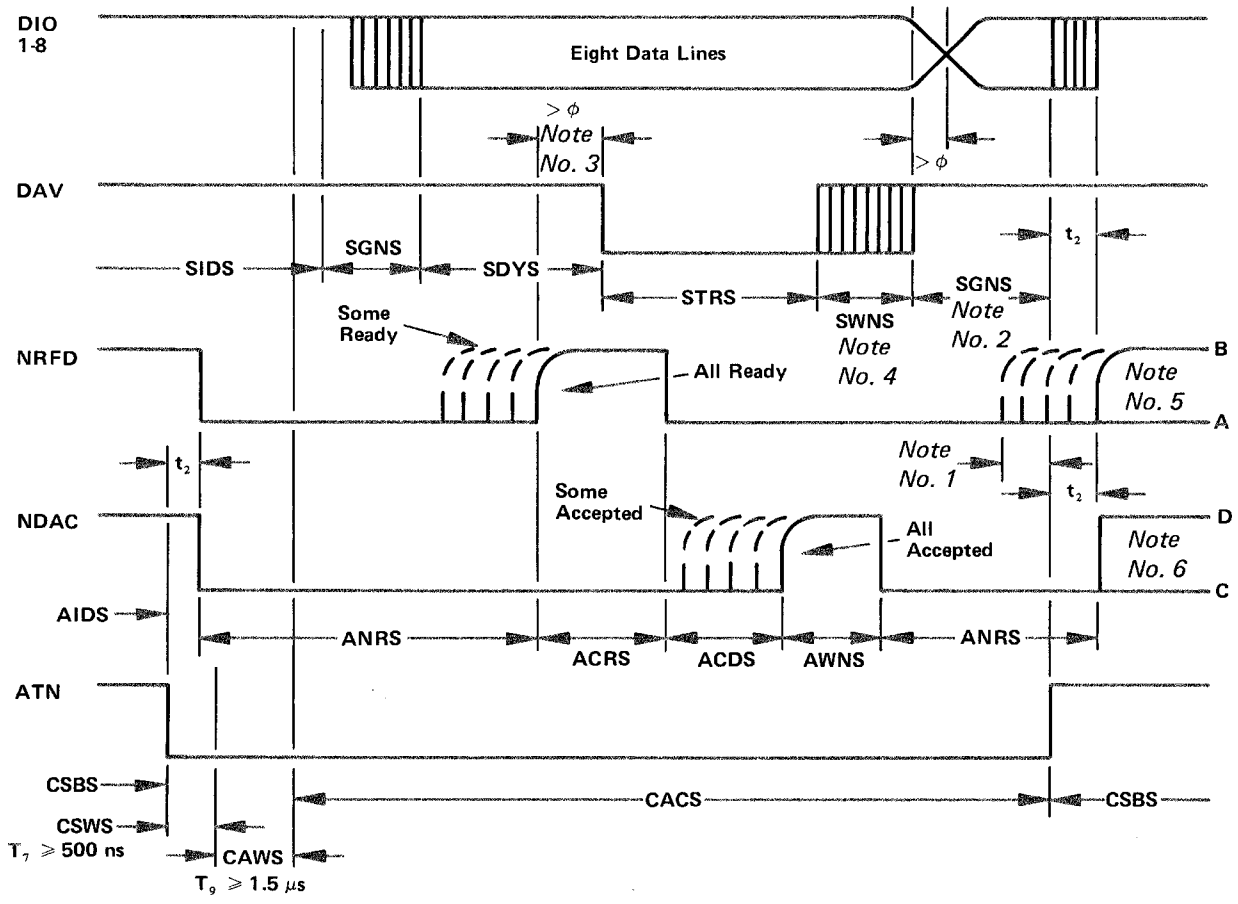
6. Multiply this number of samples by the value of the sample interval, taken from the Sample Interval switch. This value equals the time between the two negative-going edges.

The same procedure should be followed for calculating the differential time measurement between an event on one channel and an event on a different channel.

NOTE

The Sample Interval switch position may need adjusting, and acquisition of new data may be necessary, depending on the kind of information desired and the operating speed of the bus. If there is too much extraneous information on the crt, the internal clock speed should be increased. This also provides more resolution for differential time measurements. It may be necessary to change the Data Position switch from Post Trigger to Center Trigger, or from Center Trigger to Pre-Trigger in order to get the desired information on the crt as it relates to events before or after the trigger. For very slow sample speeds (e.g., 1 ms or 5 ms), the 7D01 may need a digital latch in order to catch and store faster transitions than the sample rate would acquire. The TEKTRONIX DL2 (7000-Series plug-in) and DL 502 (TM 500-Series plug-in) digital latches cover this requirement. For example, if the Sample Interval switch were set to 5 ms, but DAV went from low and back to high in 100 µs, the 7D01 would often miss this occurrence. The digital latch in series with the data would latch this 100 µs pulse for the duration of the sample interval, and the transaction would show on the crt.

It may be desirable to measure the bus response of just one device with a controller. This can be accomplished by connecting the two together and measuring their responses. To evaluate a system for overall speed, connect all the devices together; the handshake cycle goes only as fast as the slowest device participating in the handshake.



The following footnotes are referenced in the above GPIB handshake timing diagram. The state diagrams on the opposite page are provided as an aid in interpreting the above timing diagram and associated footnotes. For additional information refer to the IEEE Standard 488-1975.

NOTES:

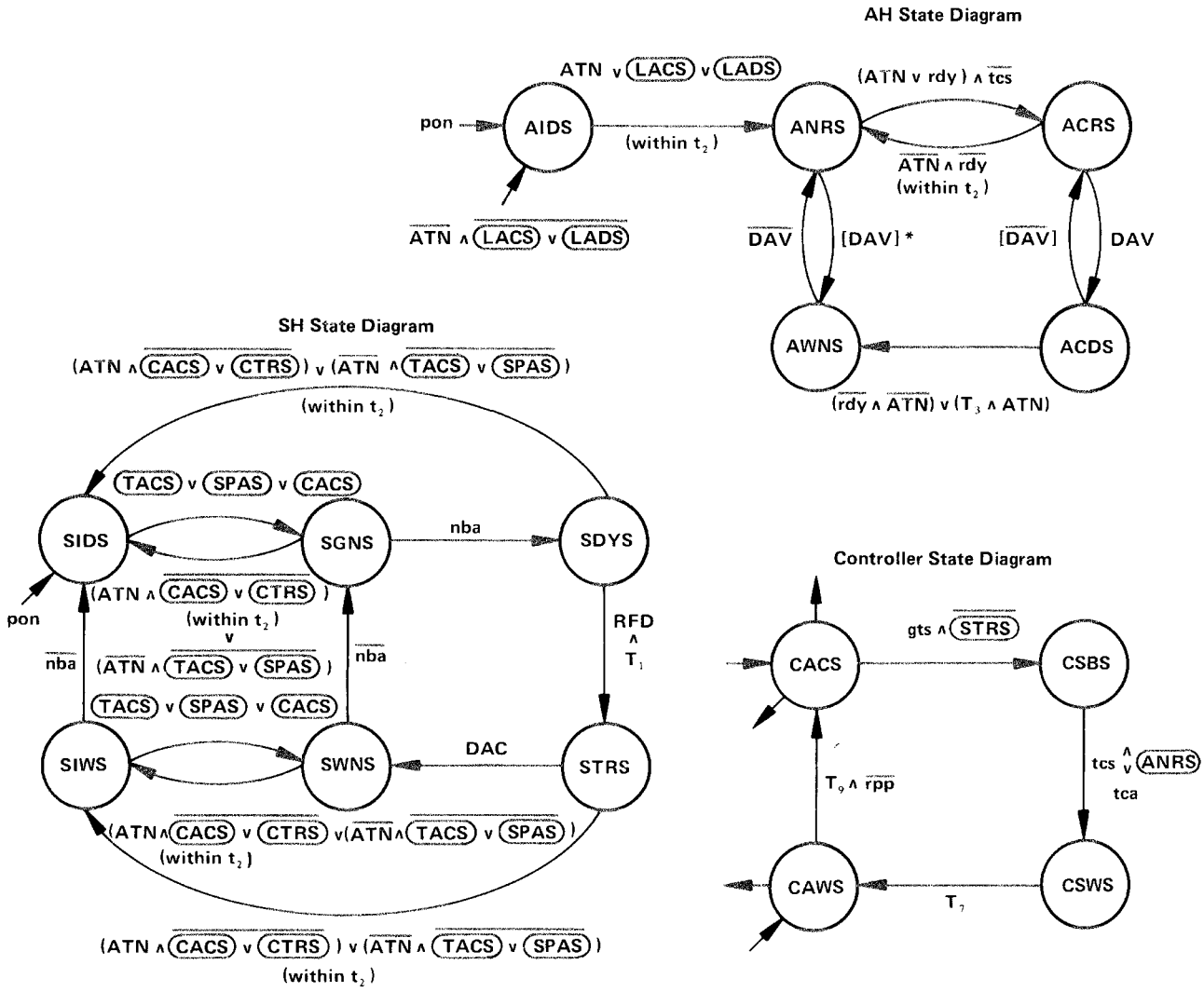
1. NRFD can go high any time within this period. If it does, the AH (Acceptor Handshake) goes to the ACRS (Acceptor Ready State) before going to the AIDS (Acceptor Idle State).

2. The SH (Source Handshake) may actually be in the SGNS (Source Generate State), SWNS (Source Wait for New Cycle State), or SDYS (Source Delay State) when ATN goes high. This is specified in the Controller State Diagram which shows that the controller cannot go into CSBS (Controller Standby State) when the SH is in the STRS (Source Transfer State).

2478-35

Figure 3-11A. GPIB handshake and ATN with associated state diagrams.

@



NOTES: (Continued)

3. The time between NRFD going false and DAV going true is dependent on how fast the talker can put out a new data byte (nba) and react to NRFD going false. The requirements for the source handshake going from SDYS (Source Delay State) to STRS (Source Transfer State) are RFD true and at least T_1 has elapsed. T_1 is the minimum settling time for multiline messages placed on the data bus by the talker. If the talker puts the nba (new byte available) on the data bus at least T_1 before RFD goes true, then the talker can assert DAV true immediately after RFD goes true.

4. In the SWNS (Source Wait for New Cycle State) the DAV message may be sent either true or false.

5. If NDAC is low after ATN goes high, it means that a device on the bus is a listener. Two possibilities exist for NRFD:

"A" occurs in which NRFD goes true within t_2 after ATN is released, if the listener is not ready for the next message ($\overline{rdy}$). This moves the AH from ACRS to ANRS.

"B" occurs in which NRFD stays high if the listener is ready for the next message (rdy).

6. If the UNL (unlisten) command was sent when ATN was true, then releasing ATN sends the AH into the idle state (AIDS). NDAC will go high within t_2 after ATN goes high. The NRFD and NDAC lines will be in the "B" state and "D" state, respectively.

2478-36

Figure 3-11B. GPIB handshake and ATN with associated state diagrams.

The following time measurement examples illustrate GPIB evaluation.

1. Measuring Timing Events of The GPIB Handshake

Figure 3-11 is a GPIB handshake timing diagram with the ATN and data lines added. Refer to this figure during the following examples.

a. t_2 = response to ATN. If NRFD and NDAC are not low when ATN goes low (true), they must go low within 200 ns. Set W. R. switches to trigger on ATN (CH 7) – LO and measure the time it takes NRFD and NDAC to go low.

b. t_2 is also a constraint when ATN goes high (false). If NRFD is false when ATN goes false, the listeners must be ready to handshake the next data byte or they must pull NRFD low (true) within 200 ns. Set W. R. switches to trigger on ATN (CH 7) – HI and measure the time it takes NRFD to be pulled low.

c. Handshake speed. The time between handshake bytes; the time between two consecutive DAV negative-going edges specifies how fast the bus is running. This time will vary, depending on the devices connected to the bus and the type of message going across the bus. To calculate this time, set the W. R. switches to trigger on ATN (CH 7) – LO. Measuring the DAV-to-DAV time while ATN is low indicates how fast the ATN messages are being handled. A particular ATN message can be used to trigger the 7D01 by setting data channels 8 thru 15 to the value of that interface message. (See GPIB Triggering explanation earlier in this section.)

For device dependent message speed analysis, set the W. R. switches to trigger on ATN (CH 7)–HI. While ATN is false (high), the handshake lines indicate the speed of the messages between the talker and the listener(s), depending on how the system is configured.

d. Talker timing for a new byte available (nba). The measurement of a talker's speed of placing new bytes of data on the bus can be made in the timing mode of the 7D01. The handshake speed can be measured as the time between DAV pulses, but this measurement of how fast a talker puts a new data byte on the bus is slightly more involved. This measurement is the time between DAC going true and when the new device-dependent message is put on the data bus (nba).

This measurement requires a sequence of data across the bus in which one byte is different from the next. For example, suppose a device outputs "5.0" on the GPIB when it is talked. The speed of putting a new byte on the bus is measured as follows:

1) Set the 7D01 to 16 channel data acquisition mode.

2) Set the W. R. switches to trigger on the ASCII character "." (period).

"." (Period)

$2E – Hex value

X 0 1 0 1 1 1 0 –Binary value

CH 15-8 – X HI LO HI LO LO LO HI

NDAC – CH 2 –HI

ATN – CH 7 –HI

All others – X (don't care)

3) Push TIMING DIAGRAM push button on DF.

4) Obtain a handshake cycle display as shown in Figure 3-10. The trigger should have occurred on NDAC going high indicating that the listener(s) accepted the decimal point (the ASCII period) on the GPIB.

5) Push the MENU push button, then the DISPLAY No. 1 push button to select GPIB operation mode.

6) Starting with a trigger-to-cursor readout of "+0", increment the cursor switch until the first occurrence of the new data byte, ASCII character "Ø" ($3Ø), is moved to the top line of the crt display. This first occurrence of the nba is the time that the talker took to put the new byte on the data bus.

7) The decimal value of the trigger-to-cursor readout is the number of internal samples taken between the time NDAC went high and the time when the nba was put on the bus. Multiply this decimal number by the Sample Interval switch setting on the 7D01 to obtain the absolute time.

2. IFC (Interface Clear) Occurrence

The IFC (Interface Clear) may be displayed by connecting UD3 to the IFC connection in the GPIB Adapter. Set the W. R. switch CH 3 to LO and all other W. R. switches to X (don't care). The controller in the system must be programmed to assert IFC (for a TEKTRONIX 4051, use the INIT statement). The timing readout can reveal the duration of the IFC pulse and its relationship to the other handshake lines: is it truly asynchronous to the other GPIB lines, or does the controller only assert IFC when in a particular state of the GPIB? The GPIB lines can also be studied after IFC is asserted to insure that the interface was, indeed, cleared according to the IEEE Standard 488-1975, and that it occurred in less than the 100 μs allowed by the standard.

3. SRQ (Service Request) Occurrence

Any device on the bus except the controller, can assert SRQ in order to request service. Service is requested to relay an error message, to indicate a valid reading has been taken, or for many other reasons. It may be useful to measure the time between when the instrument receives some illegal message and when it pulls SRQ. It may also be useful to determine when SRQ is pulled in relation to the handshake cycle.

ERROR MESSAGE DISPLAY

In GPIB mode of operation, an error message appears on the crt to identify an operator error.

REQUIRES 16 CHANNEL MODE

This error message indicates that the 7D01 Data Channels switch is in the 0-3 or 0-7 position, and must be placed in the 0-15 position for correct acquisition of all the GPIB lines.

IRREGULAR OPERATING SYMPTOMS FOR GPIB

In addition to the Irregular Operating Symptoms contained in Section 2, the following table lists irregular symptoms associated with GPIB operation.

TABLE 3-2
Irregular Operating Symptoms for GPIB

Symptom	Additional Symptoms	Probable Cause and Correction
1. a. No data display. b. TRIG'D indicator not lit.	Pressing HEX, OCTAL or BINARY push buttons has no effect on display.	No external clock signal. Either the hand-shake cycle is not operating, or the GPIB adapter combs are connected incorrectly to the opposite channel probes.
	TRIG'D indicator lights when Manual Trigger is pushed but goes off when button is released.	
2. a. Menu List is displayed after MENU push button is pressed, no change in display when DISPLAY No. 1 push button is pressed. b. Pressing any STATE TABLE or DISPLAY push buttons has no effect on display. c. TRIG'D indicator not lit.	Pressing TIMING DIAGRAM or MAP push buttons removes Menu List and blanks crt.	No external clock signal. Either the hand-shake cycle is not operating, or the GPIB adapter combs are connected incorrectly to the opposite channel probes.
	TRIG'D indicator lights when Manual Trigger is pushed but goes off when button is released.	
3. a. Display is blank or Menu List only is displayed after MENU and DISPLAY No. 1 push buttons are pressed. b. TRIG'D indicator is lit.		Memory is not filled. This is caused by a short burst of GPIB transactions, not enough to fill up all the memory. a. Change Full Display/First Trigger (P617) selector to First Trigger. –OR– Set Sample Interval to 5 ms position until the memory fills up and the display appears. Then reset the Sample Interval switch back to EXT position.
4. Error message "REQUIRES 16 CHANNELS" is displayed on the crt when the 7D01 is in 16-channel mode.		Occasionally happens when a trigger occurs after the Manual Reset is pushed but before memory becomes full. Push the Manual Reset button again.

GPIB APPLICATIONS

The DF/7D01 is a versatile measuring and display tool capable of providing detailed analysis of a GPIB system. The following hypothetical problem and solution demonstrates what can be done with the DF/7D01.

PROBLEM

A GPIB system that is operational occasionally hangs up (the three-line handshake cycle stops) for no apparent reason. To determine the cause for such a hang-up, it is necessary to examine the GPIB transactions that occurred prior to the hang-up.

PROCEDURE

1. Connect the GPIB Adapter to one of the GPIB system cables. Connect the combs to the two P6451 probes and the probes to the 7D01. (These connections are described earlier in this Section under the heading Setup Procedure for GPIB Operation.)

NOTE

Make sure Ch 0-7 and CH 8-15 are connected properly in the adapter, probes, and 7D01.

2. Set 7D01 Front Panel to:

Sample Interval	Ext
Data Position	Pre Trig
Word Recognizer	Ch 0 thru 15 -- Set all switches on X (don't care)
External and Probe Qualifier	X (don't care)

3. Connect user-definable lines in the GPIB adapter to:

UDØ	DAV
UD1	NRFD
UD2	NDAC

4. Set DF for GPIB display:

Press MENU then DISPLAY No. 1 push button.

5. Run the system and wait for it to hang up. The 7D01, in pre-trigger mode, has stored in memory all the GPIB transactions (clocked by the falling edge of DAV) up to where handshaking stopped. The W.R. trigger switches were set to X (don't care); therefore, the 7D01 would not have been triggered anytime prior to the hang-up, i.e., the stopping of DAV which is the external clock.

6. Change the 7D01 from data acquisition to data display mode by turning the Sample Interval switch to 5 ms position and pushing the Manual Trigger button to fill the remaining memory. Approximately 250 events prior to the handshake cycle hang-up can be viewed and studied. Examining the commands and/or data that were sent across the bus can reveal the reason for the hang-up, and possibly the device causing the problem.

It is also useful to know where in the handshake cycle the bus became hung up. Turn the Cursor control knobs until the trigger word (blinking line) is located at the top line of the crt. The user-definable lines (which were connected to DAV, NFRD, and NDAC prior to data acquisition) now indicate the state of the handshake after the hang-up. These states are shown as ones and zeros in the four columns on the right side of the crt. By analyzing the state of the handshake after the hang-up, the device (whether it is the talker or a listener) causing the hang-up can be identified.

NOTE

If any of these situations is suspected, the user-definable lines can be useful in examing the hanshake lines in the timing mode, and/or looking at a device's internal logic to discover if the signals are finding their way into, and out of, the interfacing logic.

POSSIBLE CAUSES

1. The GPIB will not work correctly if the devices are set to different addresses than those specified in the controller program, or if two or more devices are set to the same address. This is one of the first possible causes to check. Compare the controller program or the DF displayed address commands against the actual switch settings on each device.

2. A controller may have talk-addressed a device that:

   a. has no talker capability.

   b. is at a different address.

   c. has nothing to say; the device was not first programmed to take a reading, or send a message, or was not queried in some manner.

NOTE

No common condition exists for the state of the handshake lines or the actions of the controller. Various devices handle each situation differently.

3. Hardware problems in a device may cause intermittent errors or may totally disable the bus handshake.

   a. A device may be holding down on NRFD or NDAC so that the handshake cycle progresses no further than ANRS (Accept or Not Ready State) or ACDS (Accept Data State).

   b. A talker may never sense that NRFD or NDAC goes true; in this case, the handshake cycle does not progress past the SDYS (Source Delay State) or the STRS (Source Transfer State).

   c. A talker may internally assert DAV, but a faulty buffer or gate may not allow the signal to pass through to the GPIB.

GPIB FUNCTIONAL CHECK

1. Perform the Setup Procedure described earlier in Section 2 under the heading Basic Functional Check.

2. Set the trigger-to-cursor readout to "Ø".

3. Press the STATE TABLE HEX, then the MENU push buttons. Check for a Menu List display on the crt. Press the DISPLAY No. 1 push button, and check for a tabular GPIB display. Note that the trigger word at the bottom of the crt is in hex code.

4. Hold the COLUMN BLANK → push button in. Note that the four right columns on the crt are blanked one at a time. Hold the COLUMN BLANK ← push button in. Note that the four columns are restored one at a time.

5. Press the STATE TABLE OCTAL pushbutton, then the MENU and DISPLAY No. 1 buttons in that order. Note that the trigger word is in octal code.

6. Press the STATE TABLE BINARY push button, then the MENU and DISPLAY No. 1 buttons in that order. Note that the trigger word is now in binary code.

7. Press the LOGIC NEG push button. Note that all zeros become ones and all ones become zeros in the four right columns and the trigger word. Press the LOGIC POS push button and note that the zeros and ones change back again.

DETAILED OPERATING INSTRUCTIONS FOR ASCII OPERATION

ASCII ACQUISITION AND DISPLAY

GENERAL

In ASCII mode of operation, the DF provides a representation of the data in all 128 possible ASCII characters. The appropriate ASCII character is displayed, along with its binary, octal, or hex value to the right of the character. The crt display permits 17 ASCII character lines (events) to be displayed at one time. See Figure 4-1.

MENU DISPLAY

When the MENU push button is depressed, the DF displays a Menu List on the crt, as shown in Figure 4-1. Various operational modes are displayed in a numerical listing. Select the numbered Display push button that corresponds to the number in the Menu List, to obtain the desired operational mode. Before selecting a new operational mode, first depress the MENU push button.

ASCII DISPLAY

ASCII mode of operation is assigned position No. 2 in the Menu List. (See Figure 4-1.) This function enables data, recorded in the 7D01 memory from the P6451 probes, to be displayed in a tabular format. In 8-channel mode of data acquisition, up to 508 words (events) may be stored in memory; the data is displayed on the left side of the crt, as shown in Figure 4-1. In 16-channel mode, up to 254 words (events) may be stored in memory. The data is displayed on both the left and right sides of the crt. The left side represents channels 0 thru 7, and the right side represents channels 8 thru 15. See Figure 4-2.

ASCII Crt Display

The tabular format consists of:

1. Trigger-to-cursor readout.
   a. Located at the top (first line) of the crt.

   b. Indicates the position of the cursor, relative to the trigger. Readout is in a + or − decimal number of external clocks.

   c. The work "ASCII" is also displayed on the top line, indicating that the crt is displaying ASCII data information.

2. Trigger word readout.
   a. Located at the bottom (19th line) of the crt.

   b. Trigger word is displayed in its equivalent hex, octal, or binary value, depending on which STATE TABLE push button (HEX, OCTAL, or BINARY) was depressed prior to selecting the MENU push button.

   c. When the trigger word is displayed in octal, the octal value readout consists of the entire sixteen bits. It is not displayed as two 8-bit octal values.

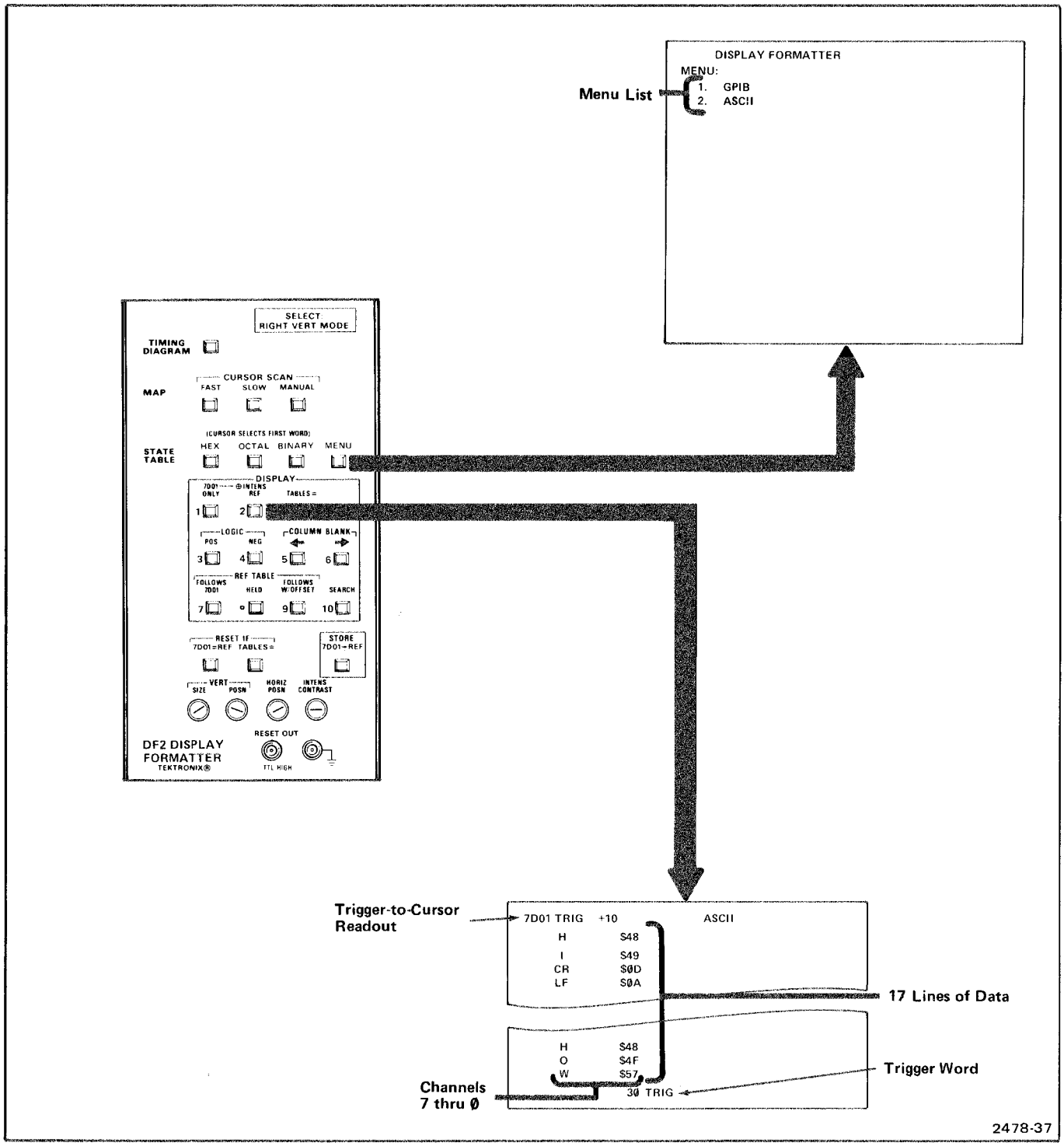
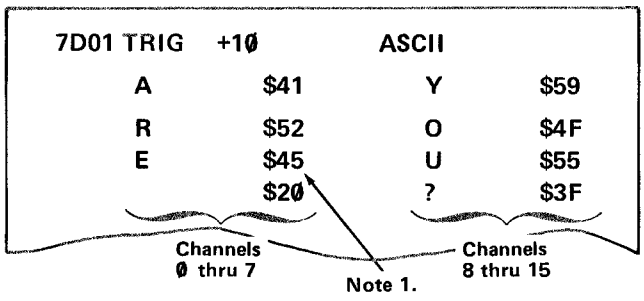
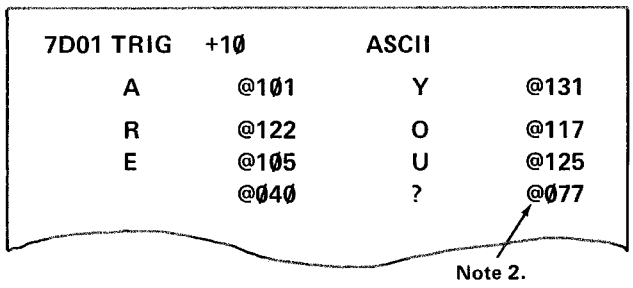


Figure 4-1. ASCII operational mode display.

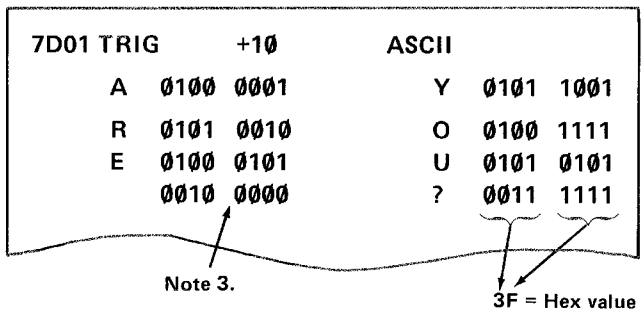
a. Hex Display



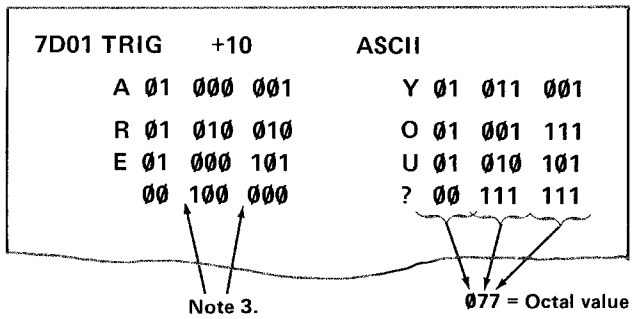
b. Octal Display



c. Binary Display (Byte switch = 4 Bit)



d. Binary Display (Byte switch = 3 Bit)



NOTES:

1. The hex values of ASCII characters displayed on the crt are identified by the "$" sign preceding the numeric or alphanumeric value.
2. The octal values of ASCII characters displayed on the crt are identified by the "@" sign preceding the numeric value.
3. To display the binary value in four column groups, position the byte switch on the 7D01 to "4 Bit". To display the binary value in three column groups, position the byte switch on the 7D01 to "3 Bit".

2478-38

Figure 4-2. ASCII state table displays of hex, octal, and binary values.

3. Seventeen lines of data displayed in standard ASCII mnemonic format.

   a. Located between the top and bottom lines (trigger-to-cursor and trigger word readouts).

   b. The information contained in the 17 lines appearing on the crt at any one time, is a data segment of the 508 words (8-channel mode) or 154 words (16-channel mode) stored in the 7D01 memory. As the data is "scrolled" manually (by the 7D01 cursor control) all of the stored memory may be viewed.

   c. The number to the right of the ASCII character (or mnemonic) is its value in either hex ("$" precedes the value), octal ("@" precedes the value), or binary depending on which STATE TABLE push button (HEX, OCTAL, or BINARY) was depressed prior to selecting the MENU push button. See Figure 4-3.

NOTE

In ASCII operation both the trigger word readout and the 17-line table are always displayed in the same mode (hex, octal, or binary).

   d. Figure 4-2 illustrates the various state table displays (hex, octal, and binary) available with ASCII operation. Figure 4-4 and 4-5 provide tables for converting ASCII mnemonic code to equivalent hex, octal, and binary values.

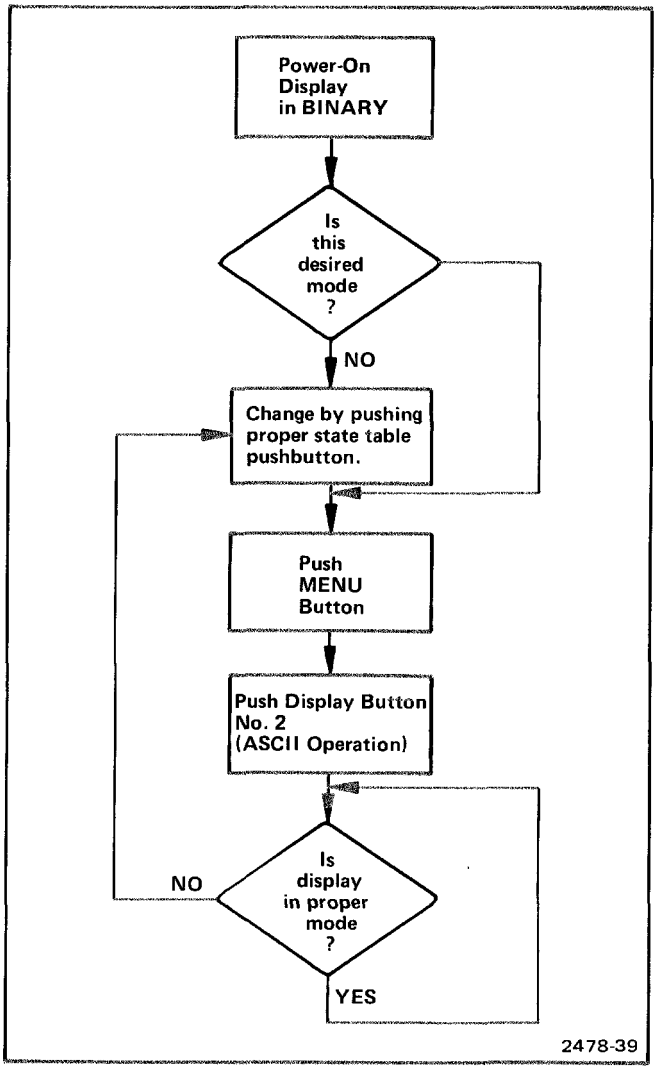


Figure 4-3. Changing display mode in ASCII operation.

@

LEAST SIGNIFICANT BITS →					MOST SIGNIFICANT BITS →							
b_7 →					Ø	Ø	Ø	Ø	1	1	1	1
b_6 →					Ø	Ø	1	1	Ø	Ø	1	1
Bits b_5 →					Ø	1	Ø	1	Ø	1	Ø	1
BINARY b_4	BINARY b_3	BINARY b_2	BINARY b_1	HEX	$\emptyset$	$1	$2	$3	$4	$5	$6	$7
Ø	Ø	Ø	Ø	Ø	NUL	DLE	SP	Ø	@	P	<'>	<P>
Ø	Ø	Ø	1	1	SOH	DC1	!	1	A	Q	<A>	<Q>
Ø	Ø	1	Ø	2	STX	DC2	"	2	B	R	<B>	<R>
Ø	Ø	1	1	3	ETX	DC3	#	3	C	S	<C>	<S>
Ø	1	Ø	Ø	4	EOT	DC4	$	4	D	T	<D>	<T>
Ø	1	Ø	1	5	ENQ	NAK	%	5	E	U	<E>	<U>
Ø	1	1	Ø	6	ACK	SYN	&	6	F	V	<F>	<V>
Ø	1	1	1	7	BEL	ETB	'	7	G	W	<G>	<W>
1	Ø	Ø	Ø	8	BS	CAN	(	8	H	X	<H>	<X>
1	Ø	Ø	1	9	HT	EM	)	9	I	Y	<I>	<Y>
1	Ø	1	Ø	A	LF	SUB	*	:	J	Z	<J>	<Z>
1	Ø	1	1	B	VT	ESC	+	;	K	[	<K>	<[>
1	1	Ø	Ø	C	FF	FS	,	<	L	\	<L>	<\>
1	1	Ø	1	D	CR	GS	-	=	M	]	<M>	<]>
1	1	1	Ø	E	SO	RS	.	>	N	^	<N>	<^>
1	1	1	1	F	SI	US	/	?	O	—	<O>	DEL

2478-40

Figure 4-4. Hex and binary to ASCII conversion table.

MOST SIGNFICANT BITS

OCTAL	@ØØ	@Ø2	@Ø4	@Ø6	@1Ø	@12	@14	@16
Ø	NUL	DLE	SP	Ø	@	P	<'>	<P>
1	SOH	DC1	!	1	A	Q	<A>	<Q>
2	STX	DC2	"	2	B	R	<B>	<R>
3	ETX	DC3	#	3	C	S	<C>	<S>
4	EOT	DC4	$	4	D	T	<D>	<T>
5	ENQ	NAK	%	5	E	U	<E>	<U>
6	ACK	SYN	&	6	F	V	<F>	<V>
7	BEL	ETB	'	7	G	W	<G>	<W>

OCTAL	@Ø1	@Ø3	@Ø5	@Ø7	@11	@13	@15	@17
Ø	BS	CAN	(	8	H	X	<H>	<X>
1	HT	EM	)	9	I	Y	<I>	<Y>
2	LF	SUB	*	:	J	Z	<J>	<Z>
3	VT	ESC	+	;	K	[	<K>	<[>
4	FF	FS	,	<	L	\	<L>	<\>
5	CR	GS	-	=	M	]	<M>	<] >
6	SO	RS	.	>	N	^	<N>	<^>
7	SI	US	/	?	O	—	<O>	DEL

2478-41

LEAST SIGNIFICANT BITS

Figure 4-5. Octal to ASCII conversion table.

SECONDARY FUNCTIONS OF DISPLAY PUSH BUTTONS

In ASCII display, the Display push buttons, 3, 4, 5 and 6 (LOGIC POS, LOGIC NEG, COLUMN BLANK←, and COLUMN BLANK→) are functional; however, their function varies depending on the mode of operation. Table 4-1 defines the functions of these Display push buttons for hex, octal, and binary display modes. The remaining Display push buttons (7, 8, 9 and 10) have no effect on the ASCII displays.

Switching from positive logic to negative logic for either hex, octal, or binary display mode changes both the displayed ASCII character or mnemonic and the ASCII value. For example, in positive logic, the ASCII character "5" is displayed with a binary value of 0011 0101. When the LOGIC NEG push button is pressed the display changes to "J 1100 1010" (the complement of 0011 0101). This feature is useful when ASCII data is recorded in negative logic. Refer to Figures 4-4 and 4-5 for ASCII conversion tables.

When operating in either hex or octal mode of ASCII display, pushing the COLUMN BLANK→ push button will zero or remove the eighth bit from the displayed ASCII value. For example, the character "B" has a displayed hex value of "$C2" which is converted to "$42" after the COLUMN BLANK→ push button is pressed. Removing the eighth bit insures that the displayed value of ASCII characters is always between $ØØ and $7F for hex displays, and between @ØØØ and @177 for octal displays. This feature enables users who are not interested in the parity bit (eighth bit) to easily read the value of the 7-bit ASCII character or mnemonic.

TABLE 4-1

Secondary Functions of Display Push Buttons.

DISPLAY PUSH BUTTON	DISPLAY MODE		
	HEX	OCTAL	BINARY
COLUMN BLANK→	Zeros CH 7 (and CH 15 in 16-channel mode). Displays hex value of only CH 0-6 (and CH 8-14 in 16-channel mode). See note 1.	Zeros CH 7 (and CH 15 in 16-channel mode). Displays octal value of only CH 0-6 (and Ch 8-14 in 16-channel mode). See note 1.	Column blanks each bit data from CH 7 thru 0 (and CH 15 thru 8 in 16-channel mode). Holding button in, automatically blanks all binary data columns from crt. See note 1.
COLUMN BLANK←	Restores the display of all eight data bits in hex. See note 2.	Restores the display of all eight data bits in octal. See note 2.	Restores each column of binary data, one column at a time. Holding button in automatically restores all binary data columns to crt. See note 2.
LOGIC POS	Trigger word, ASCII characters, and equivalent hex values displayed in positive logic. See note 3.	Trigger word, ASCII characters, and equivalent octal values displayed in positive logic. See note 3.	Trigger word, ASCII characters, and equivalent binary values displayed in positive logic. See note 3.
LOGIC NEG	Trigger word, ASCII characters, and equivalent hex values displayed in negative logic. See note 4.	Trigger word, ASCII characters, and equivalent octal values displayed in negative logic. See note 4.	Trigger word, ASCII characters, and equivalent binary values displayed in negative logic. See note 4.

Notes:

1. Turns on backlit LEDs of both blanking push buttons.
2. Turns off backlit LEDs of both blanking push buttons.
3. Positive logic: Ø = logic low and 1 = logic high.
4. Negative logic: Ø = logic high and 1 = logic low.

The eighth bit can be useful when recorded and displayed with the 7-bit ASCII character. In some cases it represents the horizontal parity of the lower seven bits. The user can verify the correct parity with those lower seven bits. (Ordinarily, this is most easily done when in the binary display mode.) The eighth bit can also be used to indicate either of two states; this may be dependent on, or independent of, the stored ASCII character. For example, the eighth bit could indicate the direction of a bus when an ASCII character was clocked into the 7D01. If connected to a UART (Universal Asynchronous Receiver Transmitter), this line could indicate whether the data originated from a computer or a terminal.

In the binary display mode of ASCII, the user can column blank all of the binary data columns. Taking out the extraneous data can be useful for photographic documentation.

The column-blanking push buttons have no effect on the trigger word in either hex, octal, or binary mode of operation.

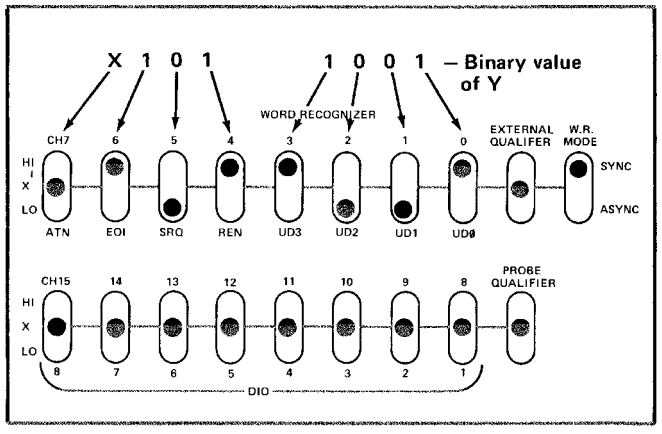
ASCII TRIGGERING

By using the word recognizer feature of the 7D01, it is possible to trigger the 7D01 on individual events in an ASCII display. The features of 8-channel and 16-channel triggering are described separately.

8-CHANNEL ASCII TRIGGERING

In 8-channel ASCII, the eight channels are displayed on the left half of the crt. These eight correspond to the W.R. switches CH 0 thru 7. If it is desired to trigger on a specific event, the binary value of the event is set in the W.R. switches CH 0 thru 7. All other W.R. switches should be set to "X" (don't care). To trigger the 7D01 on the ASCII character "Y", set the W.R. switches as follows:

"Y" Uper Case ASCII character
$59 --- Hex value
@131 --- Octal value
X 1 0 1 1 0 0 1 --- Binary value
CH 7-0 --- X HI LO HI HI LO LO HI
CH 15-8 --- All switches on X (don't care)



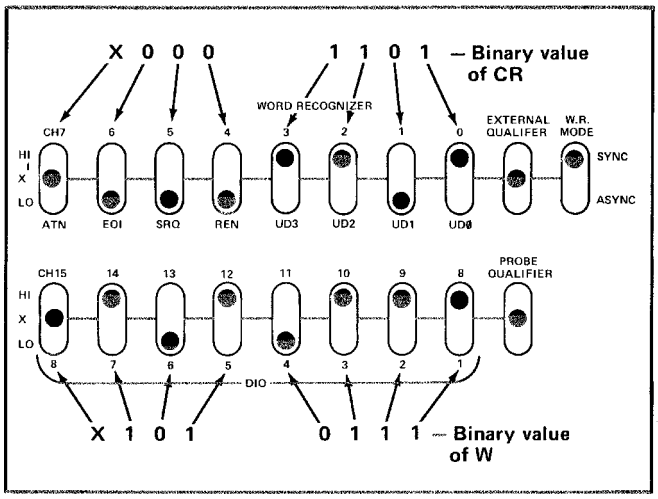
16-CHANNEL ASCII TRIGGERING

In 16-channel ASCII, the first eight channels are displayed on the left side of the crt as an ASCII character or mnemonic along with its value in hex, octal, or binary. The other eight channels are displayed on the right side of the crt in the same manner. The eight channels on the right side correspond to W.R. switches CH 8 thru 15. It is possible to trigger the left display (CH 0-7) on a specific event concurrently with another specific event on the right side (CH 8-15). For example, to trigger the 7D01 on the ASCII character "CR" (carriage return) for the left display and "W" for the right display, set the W.R. switches as follows:

"CR" ASCII mnemonic for carriage return
$ØD --- Hex value
@Ø15 --- Octal value
X 0 0 0 1 1 0 1 --- Binary value
CH 7-0 --- X LO LO LO HI HI LO HI

"W" Upper case ASCII character
$57 --- Hex value
@127 --- Octal value
X 1 0 1 0 1 1 1 --- Binary value
CH 15-8 --- X HI LO HI LO HI HI HI

@



When the trigger-to-cursor readout is on "+Ø", the trigger word contains the hex, octal, or binary values of both characters "CR" and "W". The left display contains the character "CR" in the top line of the table, and the right display contains the character "W" in the top line of the table.

TRIGGER WORD

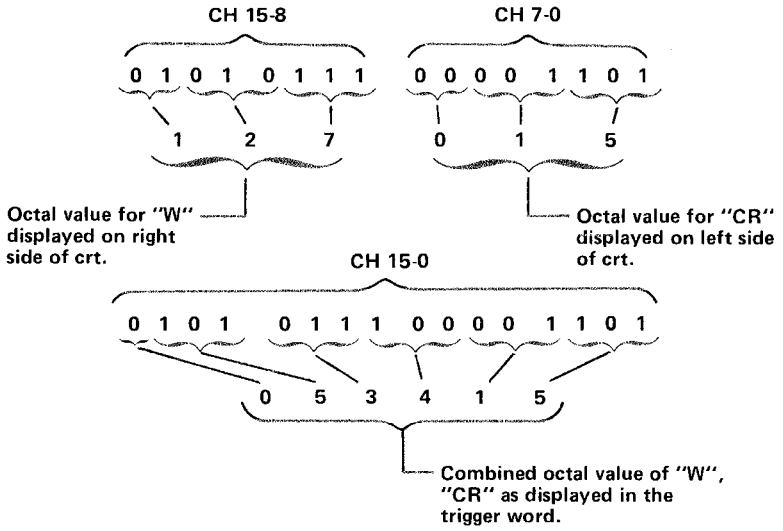
In 16-channel mode, the trigger word is displayed with channels 8-15 first, followed by channels 0-7. For the previous example, the trigger word would be displayed for the selected mode, as follows:

Binary --- 0101 0111 0000 1101

Hex --- 57ØD

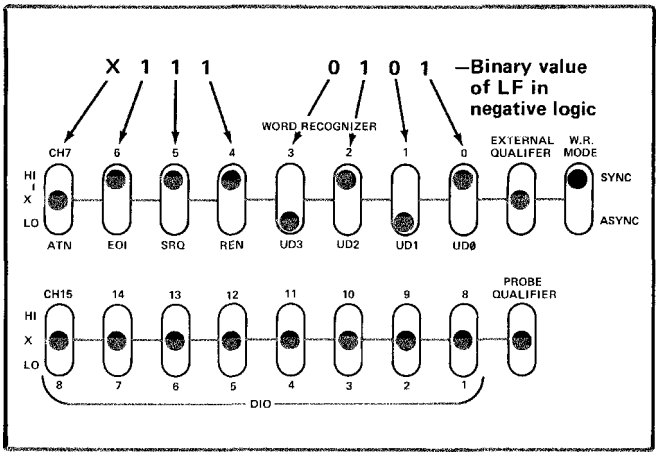
Octal --- Ø53415

In the trigger words displayed above, note that the binary and hex trigger words are directly related to the binary and hex values of "CR" and "W". The octal trigger word is not directly related; the octal derivation from two 8-bit binary values is not the same as the derivation from a 16-bit binary value. This difference is shown as follows:



NEGATIVE LOGIC ASCII TRIGGERING

In the preceding examples of ASCII triggering, data was assumed to be in positive logic. It is also possible to display ASCII data in negative logic, where a logic high = Ø and logic low = 1. To trigger the 7D01 on an ASCII character in negative logic, set the W.R. switches on the 7D01 in negative logic. For example, to trigger the 7D01 on an ASCII character "LF" (line feed) in negative logic, set the W.R. switches as follows.



"LF" ASCII mnemonic for line feed

X 0 0 0 1 0 1 0 --- Binary value positive logic

X 1 1 1 0 1 0 1 --- Binary value negative logic

CH 7-0 --- X HI HI HI LO HI LO HI
(W.R. switch settings for "LF" in negative logic)

CH 15-8 --- All switches on X (don't care)

ERROR MESSAGE DISPLAY

In ASCII mode of operation, an error message appears on the crt to identify an operator error.

REQUIRES 8 OR 16-CHANNEL MODE

This error message indicates that the 7D01 Data Channels switch is in the 0-3 position when operating in the ASCII mode. Change the switch to either 0-7 or 0-15 position.

IRREGULAR OPERATING SYMPTOMS FOR ASCII

In addition to the Irregular Operating Symptoms contained in Section 2, the following table lists irregular symptoms associated with ASCII operation.

TABLE 4-2

Irregular Operating Symptoms for ASCII

Symptom	Additional Symptoms	Probable Cause and Correction
1. a. No data display. b. TRIG'D indicator not lit.	Pressing HEX, OCTAL or BINARY push buttons has no effect on display.	No external clock signal. Check that the clock signal is applied through the Data Acquisition Probe P6451.
	TRIG'D indicator lights when Manual Trigger is pushed but goes off when button is released.	
2. a. Menu List is displayed after MENU push button is pressed, no change in display when DISPLAY No. 2 push button is pressed. b. Pressing any STATE TABLE or DISPLAY push buttons has no effect on display. c. TRIG'D indicator not lit.	Pressing TIMING DIAGRAM or MAP push buttons removes Menu List and blanks crt.	No external clock signal. Check that the clock signal is applied through the Data Acquisition Probe P6451.
	TRIG'D indicator lights when Manual Trigger is pushed but goes off when button is released.	
3. a. Display is blank or Menu List only is displayed after MENU and DISPLAY No. 2 push buttons are pressed. b. b. TRIG'D indicator is lit.		Memory is not filled. This is caused by a short burst of ASCII data, not enough to fill up all the memory. a. Change Full Display/First Trigger (P617) selector to First Trigger. —OR— Set Sample Interval to 5 ms position until the memory fills up and the display appears. Then reset the Sample Interval switch back to EXT position.

ASCII FUNCTIONAL CHECK

1. Perform the Setup Procedure described earlier in Section 2 under the heading Basic Functional Check.

2. Set the trigger-to-cursor readout to "Ø".

3. Press the STATE TABLE HEX and MENU push buttons, in that order. Check for a Menu List displayed on the crt. Press the DISPLAY No. 2 push button and observe a tabular ASCII display on the crt. Note that the trigger word at the bottom of the crt is in hex code and that the value of the ASCII characters are also displayed in hex. The "$" sign preceding the ASCII value in the display indicates that the value is in hex.

4. Press the COLUMN BLANK→ push button. Note that the displayed ASCII values have changed. The top line in the left display, before pressing the COLUMN BLANK→ button, was "NUL $8Ø". It is now "NUL $ØØ". After pressing the COLUMN BLANK→ button, all displayed ASCII values should be between "$ØØ" and "$7F".

5. Press the STATE TABLE OCTAL push button, then the MENU and DISPLAY No. 2 buttons, in that order. Note that the trigger word and ASCII values have changed to octal code. The "@" sign preceding the ASCII value in the display indicates the value is in octal code.

6. Press the COLUMN BLANK→ push button. Note that the displayed ASCII values have changed. After pressing the COLUMN BLANK→ button all displayed ASCII values should be between "@ØØØ" and "@177".

7. Press the STATE TABLE BINARY push button, then the MENU and DISPLAY No. 2 buttons, in that order. Note that the trigger word and ASCII values have changed to binary code.

8. Press the LOGIC NEG push button. Note that all zeros become ones and all ones become zeros in the ASCII value and trigger word readouts. Press the LOGIC POS push button and note that the zeros and ones change back again.

9. Hold the COLUMN BLANK→ push button in. Note that the binary columns are blanked from left to right one at a time. Hold the COLUMN BLANK← push button in. Note that the binary columns are restored one at a time.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

THEORY OF OPERATION

The functions of the DF are controlled by a microprocessor system built into the instrument. Data and control functions are transferred within the DF by an 8-bit data bus and a 16-bit address bus. The microprocessor acquires data from the associated 7D01 Logic Analyzer and performs the functions indicated by the push buttons on the DF front panel. The various output displays are coupled back through the 7D01 to the oscilloscope mainframe. Due to the complexity of the DF circuitry (especially the microprocessor) normal troubleshooting techniques may not apply to this instrument. See the Maintenance section of this manual for Troubleshooting procedures.

The following descriptions refer to the functional blocks shown on the schematic diagrams in the back of this manual.

FRONT PANEL ①

The desired function of the DF is selected by pressing one of the front-panel switches. When one of the switches is pressed, one of the keyboard lines ($\overline{\text{KYBD 1}}$ - $\overline{\text{KYBD 4}}$) drops to a LO level.

The microprocessor must then determine which switch is being pressed. The keyboard line which is being held LO indicates the proper switch column. The row is indicated by clocking a HI level through shift register U65 until the keyboard line returns to a HI level. The shift register is then cleared (all outputs LO). This procedure is repeated five times to eliminate any contact bounce.

EXAMPLE: If the OCTAL button is pressed, KYBD 2 line will go LO. The outputs of U65 are then sequentially driven HI until KYBD 2 goes HI. This occurs on the third clock pulse, identifying the OCTAL switch.

DATA ACQUISITION ②

The circuitry shown on the Data Acquisition diagram acquires data, cursor, and status information from the 7D01, and connects the keyboard information ($\overline{\text{KYBD 1}}$ - $\overline{\text{KYBD 4}}$) to the Data Bus.

Address Decoder

The Address Decoder, U102, provides a single line output for each of eight addresses. Table 5-1 is a truth table for the Data Acquisition Address Decoder.

TABLE 5-1
Data Acquisition Address Decoder

Inputs					Outputs[2]
A0	A1	A2	A3	$\overline{\text{HZP}}$[1]	
LO	LO	LO	LO	LO	$\overline{\text{00B0}}$
HI	LO	LO	LO	LO	$\overline{\text{00B1}}$
LO	HI	LO	LO	LO	$\overline{\text{00B2}}$
HI	LO	HI	LO	LO	$\overline{\text{00B5}}$
LO	HI	HI	LO	LO	$\overline{\text{00B6}}$
HI	HI	HI	LO	LO	$\overline{\text{00B7}}$

[1] *Hi Zero Page.*
[2] **Outputs change state on rising edge of $\emptyset_2$L signal.**

7D01 Cursor Acquisition

The cursor position count is received by the DF as ten bits of parallel data. This data is converted to serial data by U132 and U138 and is then clocked through U162 (1D to 1Q) to DB0 (Data Bus line 0).

7D01 Status Acquisition

The operating mode of the 7D01 (store or display) is used by the DF to ensure the validity of the acquired data. If the 7D01 goes into store mode while the DF is acquiring data, the data acquired would not be valid. The 2Q and 3Q outputs of U162 indicate the status of the 7D01.

Keyboard Latch

The Keyboard Latch, U172, connects the keyboard signal lines ($\overline{\text{KYBD 1}}$ - $\overline{\text{KYBD 4}}$) to the data bus (DB4 - DB7).

7D01 Data Acquisition

Data stored by the 7D01 is transferred to the DF and stored for faster access by the microprocessor. The data is transferred in serial form and is connected to DB4 (Data Bus line 4) through input 1D and output 1Q of U182.

The frame pulse indicates the beginning of the serial data. When the frame pulse clocks the Q output of U158B LO, the microprocessor starts clocking in the serial data, one bit at a time, by addressing ØØB1 to pulse the Display Clock Off line LO for each bit of data.

MPU, PROGRAM, AND DATA STORAGE ③

This diagram shows the microprocessor, the program ROM (Read Only Memory), and the data-storage and scratch-pad RAMs (Random Access Memories).

Microprocessor

The microprocessor, U264, is the heart of the DF. All other stages of the circuitry either provide or accept data and/or instructions for (or from) the microprocessor. Due to the complexity of the microprocessor operation, a description of the microprocessor will not be attempted in this manual. If detailed information is needed, refer to the microprocessor manufacturer's specification books.

Program ROM

The Program ROM (Read Only Memory), U284 and U294, provides the permanent storage for the microprocessor instructions. When the microprocessor addresses a location in the Program ROM, the Program ROM connects the addressed information to the Data Bus, which the microprocessor reads and acts on.

Scratch-Pad RAM

The Scratch-Pad RAM (Random Access Memory), U274, provides temporary storage of data or addresses for the microprocessor. The Scratch-Pad RAM can store up to 128 eight-bit bytes of information.

Data Storage RAM

The Data Storage RAM consists of eight RAMs and three Bus Driver integrated circuits. Drivers U304 and half of U308 buffer the address lines to the RAMs. U354 and the other half of U308 provide buffered 3-state outputs for the RAMs to drive the data bus.

VERT AND HORIZ DISPLAY OUTPUT ④

The Vertical and Horizontal Display Output circuits provide the X-axis and Y-axis deflection for each dot of the State Table or Map displays.

The State Table display consists of 32 columns and 19 rows of characters. Each character contains 5 columns and 7 rows of dots. The State Table display is presented in the following manner: The top row of information (cursor position) is written first. The bottom row of information (trigger word) is written next. The rest of the display is then written, starting with the first row of data and working down. Each row of the display is written from left to right on the crt.

The characters are each written by starting at the top left corner of the character and proceeding across the character to the right edge, then returning to the left edge and dropping to the next row of the character.

The Map display consists of 256 columns and 256 rows of possible dot locations.

Display Column Counter

The Display Column Counter sets the horizontal position of each character of the State Table display. Counter U402 provides the column number (1 to 16) to the ROM, U422. The output of U422 determines the horizontal spacing of the characters. The other 16 columns (columns 17 through 32) are spaced the same as columns 1 through 16, except that they are offset to the right half of the crt display by the HI level at the Q output of U404B. The three-bit or four-bit byte spacing is determined by the level at the E address input of U422. When the E address input is LO, 4-bit byte spacing is provided by the ROM. When the E address line is HI, the other half of the ROM is addressed, providing 3-bit bytes.

Character Column Counter

Character Column Counter U412 provides the horizontal spacing of the five columns of dots for each character. The output of U412 is added to the output of U422 to set the horizontal position of each dot.

Display Row Counter

The Display Row Counter sets the vertical position of each line of the State Table display. Counter U504/U404A provides the row number (1 through 19) to the ROM, U522. The output of U522 determines the vertical spacing of the

rows. Row 1 (cursor location) is written at the top of the crt. Row 2 (trigger word) is written at the bottom of the crt. The other 17 rows are written, in order, starting just below row 1.

Character Row Counter

Character Row Counter U502 provides the vertical spacing of the seven rows of dots for each character. The output of U502 is added to the output of U522 to set the vertical position of each dot.

Display Finish Detector

The Display Finish Detector stops the Display Clock signal after completion of the second or ninteenth display row. The State Table display is finished at completion of row ninteen. The Map and Timing Diagram displays require only the information in rows 1 and 2 (top and bottom). The rest of these displays are provided from other sources.

Character and Dot Position Adders

Adders U432 and U434 combine the outputs of the Display and Character Column Counters to drive the Horizontal D-to-A (digital-to-analog) converter. Adders U532 and U534 combine the outputs of the Display and Character Row Counters to drive the Vertical D-to-A converter.

Map Location Latches

The Map Location Latches accept data directly from the microprocessor, via the Data Bus, to asign dot positions for the Map display. These latches are enabled when the DF is in the Map mode.

Map Display Multiplexer

The Map Display Multiplexer selects either State Table or Map display. When the State Table display is selected, the outputs from the adders are coupled through to the Horizontal and Vertical D-to-A converters.

When the Map display is selected, the first two lines (top and bottom) of the State Table are displayed, then the Map Display Multiplexer switches to the Map Location Latch outputs for the remainder of the display.

Vert and Horiz D-to-A Converter

The Digital-to-Analog converters, U468 and U568, each convert eight lines of digital data input to one line of analog data output. The output of each converter is amplified and connected as a push-pull signal to the Vertical or Horizontal outputs to drive the mainframe.

CHARACTER MEMORY AND GENERATOR ⑤

The Character Memory and Generator circuitry provides the Z-axis (intensity) control for the display.

Next Character Row Counter

The Next Character Row Counter provides the number of the next row of the character being displayed.

Character Latch Decoder

The Character Latch Decoder provides the signals to clock the character address information into U674 and U676.

Next Character Counter

The Next Character Counter provides the address for the next character to be displayed.

RAM Address Switch

The RAM Address Switch allows the Character RAM to be addressed by either the microprocessor (to load the RAM) or by the Next Character Counter (for display).

Character RAM

The Character RAM stores the data required to display each character (as supplied by the microprocessor). The data is then fed to the Present Character Latch one character at a time.

Present Character Latch

The Present Character Latch holds the data from the Character RAM while it is being used. Once this information is latched, the Next Character Counter advances to the address of the next character to be displayed. This "pipeline" effect increases the speed of the display by effectively reducing the access time of the Character RAM to zero.

Present Character Generator and Shift Register

The Present Character Generator, U684, provides five outputs, one for each character column. The five outputs indicate whether the corresponding dots are bright or dark. The five outputs from U684 are loaded into Shift Register U694 and clocked out in sequence to provide the Z-axis (intensity) information for each row of each character.

DISPLAY CONTROL AND Z-AXIS ⑥

The circuits on this diagram provide the clock and control signals for the display.

65-Hz Clock

The 65-Hz Clock, U640, provides the "refresh" timing for the display.

Blinking Character Counter

The Blinking Character Counter, U648, causes the trigger word to blink when it appears in the State Table display by disabling the z-axis every fourth time the trigger word is displayed.

4-MHz Clock

The 4-MHz Clock provides the display clock signal when gated by the Character Dot Detector. Flip-flop U714A and gate U724D ensure a full-width pulse output for the first enabled clock pulse.

Character Dot Detector

The Character Dot Detector speeds up the display by allowing display time only if a dot is to be displayed. If no dot is to be displayed at the present address, the next pulse from the 4-MHz Clock is coupled to the DSPL CLK line to advance the counters (diagrams 4 and 5) to the next address. If a dot is to be displayed, the Character Dot Detector allows one 4-MHz Clock pulse for the D-to-A converters (diagram 4) to settle, then enables the Z-axis for two 4-MHz Clock pulses before advancing the counters to the next address.

Map Z-Axis

The Map Z-Axis stage enables the z-axis (intensity) for each dot of the Map display. Monostable multivibrator U748A is triggered by the output of U714B to allow the D-to-A converters (diagram 4) to settle. U748B then enables the z-axis to display each dot.

Display Control

The Display Control stage determines the source of the display and readout signals. The readout source is selected by jumper P754. When the jumper is in the MFR (mainframe readout) position, the cursor position and cursor word readout is supplied by the 7D01 in the Timing Diagram mode (the DF provides the readout for the other display modes). When the jumper is in the FOR R (formatter readout) position, the DF provides the readout for all display modes.

All display information is supplied by the DF, except for the Timing Diagram display which is provided by the 7D01 directly.

Output Buffers

The Output Buffers provide the final amplification required by the control signals used by the oscilloscope mainframe.

DISPLAY ⑦

The Display diagram shows the three shift registers and associated emitter followers and LED's which make up the front-panel lighting for the DF.

ROM EXTENSION ⑨

This diagram show the program ROM extension, extended ROM decoder, regulated +5 V power supply and the troubleshooting plugs.

Program ROM Extension

The Program ROM (Read Only Memory) Extension (U820, U830, U840, and U850) provides additional permanent storage for the microprocessor instructions. This additional storage extends the basic program (provided by the Program ROMs, U284 and U294) by 2048 eight-bit bytes of instruction for each ROM chip added.

Extended ROM Decoder

The Extended ROM Decoder, U860, provides a chip select line output for each ROM. Table 5-2 is a truth table for the Extended ROM Decoder.

TABLE 5-2
Extended ROM Decoder

INPUTS					BEGINNING ADDRESSES
A15	A14	A13	A12	A11	
LO	HI	LO	LO	LO	$4000 — U820
LO	HI	LO	LO	HI	$4800
LO	HI	LO	HI	LO	$5000
LO	HI	LO	HI	HI	$5800

Regulated +5 V Power Supply

The regulated +5 V power supply provides a regulated power source for the program ROM extension sockets (U820, U830, U840, and U850) and is derived from the +15 V supply on the Intelligence Board (A3). The extended ROM decoder, U860, derives its +5 V supply from the instruments common +5 V supply. U860 has a different supply than the ROMs in order to keep the address lines from being pulled down if the regulated +5 V supply should go down. If this happens all the features of the DF, except the Menu mode, would still be operational.

Troubleshooting Pins

A double row of parallel connected square pins make up P807, P808, P809, and P810. One row of pins interconnects the ROM Extender Board (A5) to the Intelligence Board (A3). The other row of pins provide a convenient access for all (non-buffered) address, data and control lines from the microprocessor.

MAINTENANCE

This section of the manual contains information for performing preventive maintenance, troubleshooting, and corrective maintenance.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, etc. Preventive maintenance performed on a regular basis may prevent instrument breakdown and will improve the reliability of the instrument. The severity of the environment to which the instrument is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is preceding adjustment of the instrument.

CLEANING

The instrument should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation which can cause overheating and component breakdown.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a non-residue type of cleaner, preferably isopropyl alcohol, total denatured ethyl alcohol, or TP35. Before using any other type of cleaner, consult your local Tektronix Service Center or representative.

Exterior

Loose dust accumulated on the front panel can be removed with a soft cloth dampened in a mild detergent and water solution. Abrasive cleaners should not be used.

Interior

Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-pressure air.

Remove any dirt which remains with a soft brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces.

VISUAL INSPECTION

The instrument should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged circuit boards, and heat-damaged parts.

The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

Switch Contacts

Switch contacts and pads are designed to operate without lubrication for the life of the switch. However, as the switches are not sealed, dust attracted to the contact area may cause the switch contacts to become electrically noisy. Cleaning may be accomplished by flushing the contact area with isopropyl alcohol or kelite (1 part kelite to 20 parts water). Do not use chemical cleaning agents that leave a film or that might damage plastic parts. Do not use cotton swabs or similar applicators to apply cleaning agents, as they tend to snag and leave strands of cotton on the switch contacts. Should it become necessary to remove a switch for replacement or cleaning refer to Component Removal and Replacement in this section.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors in the instrument are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on checking semiconductor operation are given under Troubleshooting.

TROUBLESHOOTING

The following information is provided to help you troubleshoot the instrument. Information contained in other sections of the manual should be used along with the following information to aid in locating the defective component. An understanding of the circuit operation is very helpful in locating troubles, particularly where integrated circuits are used.

TROUBLESHOOTING AIDS

Diagrams

Complete schematic diagrams are given on the foldout pages in section 10, Diagrams and Circuit Board Illustrations. The component number and electrical value of each component in this instrument are shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in this instrument.) Important waveforms, and the numbered test points where they were obtained, are located adjacent to each diagram. The portions of circuits mounted on circuit boards are enclosed with heavy, solid-black lines.

Circuit Board Illustrations

To aid in locating circuit boards, a circuit board location illustration appears on the back of the foldout page facing the schematic diagram. In addition, an illustration of the circuit board(s) is included here, with the physical location of the components and waveform test points that appear on the schematic diagram identified. Each circuit board illustration is arranged in a grid locator with an index to facilitate rapid location of components contained in the schematic diagrams.

Troubleshooting Chart

A troubleshooting chart is given in section 10, Diagrams and Circuit Board Illustrations, to aid in locating a defective circuit. Circuit operation is discussed in detail in section 5, Theory of Operation.

Error Messages on Crt

Table 6-1 indicates the action to be taken in the event an error message is displayed on the crt.

TROUBLESHOOTING EQUIPMENT

The following equipment, in addition to that listed in the Performance Check and Adjustment section, is useful for troubleshooting this unit.

System Test Fixture

Description: Effectively replaces microprocessor U264, and allows operator control of the DF's data bus, address bus, and R/W line. Tektronix Part 067-0746-00.

TABLE 6-1

Error Messages and Responses

Error Message	Action
SEE MANUAL CUR CAN'T MOVE	1. Check that 7D01 cursor position switch (both fine and course) is firmly seated in detent. 2. Check DF and 7D01 cursor circuitry. 3. Contact your local Tektronix Field Office or representative for factory repair.
BAD RAM SEE MANUAL	1. Check RAMs U314, U316, U318, U320, U334, U336, U338, and U340, or associated circuitry (see Data Bus and RAM Test in this section). Refer to diagram 3 in section 10. 2. Contact your local Tektronix Field Office or representative for factory repair.
REQUIRES 16 CHANNEL MODE	1. When operating in GPIB mode, this error message indicates that the 7D01 Data Channels switch is in the 0-3 or 0-7 position. Change switch to the 0-15 position.
REQUIRES 8 or 16 CHANNEL MODE	1. When operating in ASCII mode, this error message indicates that the 7D01 Data Channels switch is in the 0-3 position. Change switch to 0-7 or 0-15 position.

@

Interface Test Fixture

Description: Serves as a buffer between the System Test Fixture (067-0746-00) and the DF. Tektronix Part 067-0804-00.

Cable Extender

Description: Allows the DF to operate remote from the 7D01 plug-in unit. Tektronix Part 067-0805-00.

Power Supply

Description: Dc voltage supply; voltage +5 volts, within 5%, with a current capability of at least 1 ampere. Recommended TEKTRONIX types: PS501, PS502, or PS505 Power Supplies.

Transistor Tester

Description: Dynamic-type tester. Purpose: Test semiconductors. Recommended TEKTRONIX types: 576 Curve Tracer, 577/177 Curve Tracer system, 7CT1N Curve Tracer unit and a 7000-series oscilloscope, or a 5CT1N Curve Tracer unit and a 5000-series oscilloscope.

Multimeter

Description: Voltmeter, 10 megohm input impedance and a range from 0 to at least 50 volts dc; accuracy, within 0.1%. Ohmmeter, 0 to 20 megohms. Test probes should be insulated to prevent accidental shorting. Purpose: Check voltage and resistance.

Test Oscilloscope (Storage Type Preferred)

Description: Frequency response, dc to 100 megahertz minimum; vertical deflection factor, 5 millivolts to 5 volts/division. A 10X, 10 megohm voltage probe should be used to reduce circuit loading. Purpose: Check operating waveforms.

Plug-In Extender

Description: Two types of extenders are available. (1) Flexible Plug-In Extender: Tektronix Part 067-0616-00 (two required). (2) Rigid Plug-In Extender: Tektronix Part 067-0589-00 (two required). Purpose: Allows plug-in operation outside the mainframe.

TROUBLESHOOTING TECHNIQUES

Preliminary Troubleshooting Procedure

This preliminary troubleshooting procedure is arranged to check the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection, operation, and adjustment. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, it should be replaced using the replacement procedure given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS. Incorrect control settings can indicate a trouble that does not exist. If there is any question about the function or operation of any control, see the Functional Check in the Operating Instructions section of this manual.

2. CHECK ASSOCIATED EQUIPMENT. Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Check that the signal is properly connected and that interconnecting cables are not defective. Also check the power source. If the trouble persists, this instrument is probably at fault.

3. VISUAL CHECK. Visually check that portion of the instrument in which the trouble is located. Many troubles can be located by visible indications such as unsoldered connections, broken wires, damaged circuit boards, damaged components, etc.

4. CHECK INSTRUMENT ADJUSTMENT. This instrument contains only one adjustment; check the adjustment, or the affected circuit if the trouble appears in one circuit. Complete adjustment instructions are given in the Performance Check and Adjustment section.

5. ISOLATE TROUBLE TO A CIRCUIT. To isolate trouble to a circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check the affected circuits by taking voltage and waveform readings. Also check for the correct output signals at the front-panel connector with a test oscilloscope. Incorrect operation of all circuits often indicates trouble in the power supply, microprocessor, ROM's, or bus drivers. Check for correct voltages of the individual supplies. A defective component elsewhere in the instrument can appear as a power-supply trouble and may also affect the operation of other circuits.

6. CHECK VOLTAGES AND WAVEFORMS. Often the defective component can be located by checking for the correct voltage or waveform in the circuit.

7. CHECK INDIVIDUAL COMPONENTS. The following procedures describe methods of checking individual components. Two-lead components that are soldered in place are best checked by first disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

WARNING

To avoid electric shock, disconnect the power source before removing or replacing semiconductors.

Transistors. A good check of transistor operation is actual performance under operating conditions. A transistor can be effectively checked by substituting a new component or one that has been checked previously. However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static-type testers are not recommended, since they do not check operation under simulated operating conditions.

Integrated Circuits. IC's (integrated circuits) can be checked with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is desirable when troubleshooting circuits using IC's. Use care when checking voltages and waveforms around the IC's so that adjacent leads are not shorted together. A convenient means of clipping a test probe to the 14-, 16-, 20-, and 40-pin IC's is with an IC test clip. This device also serves as an extraction tool. The lead configuration for the semiconductors used in this instrument are shown on a pullout page in the front of the diagrams section.

Diodes. A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter. Use a scale having a low internal source current, such as the R X 1 kΩ scale. The resistance should be very high in one direction and very low when the meter leads are reversed.

CAUTION

Do not use the ohmmeter on a scale that has high internal current. High currents may damage the diode.

The cathode end of each glass-encased diode is indicated by a stripe, a series of stripes, or a dot. The cathode and anode ends of metal-encased diodes are identified by the diode symbol marked on the case.

Resistors. Check resistors with an ohmmeter. See the Replaceable Electrical Parts list for the tolerance of the resistors used in this instrument. Resistors normally do not need to be replaced unless the measured value varies widely from that specified.

Inductors. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit. Partial shorting often reduces high-frequency response (roll off).

Capacitors. A leaky or shorted capacitor can usually be detected by checking resistance with an ohmmeter set on its highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after the initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking if the capacitor passes ac signals.

8. REPAIR AND ADJUST. If any defective parts are located, follow the replacement procedures given in Corrective Maintenance. Be sure to check the performance of any circuit that has been repaired or had any electrical components replaced.

Troubleshooting with the System Test Fixture

Index to troubleshooting the DF with the 067-0746-00 System Test Fixture.

	PAGE
Preliminary Setup Information	6-4
Data Bus and RAM Test	6-6
ROM Test	6-6
Keyboard Test	6-7
Button Lights Test	6-8
Display Test	6-8
7D01 Control Signals	6-10
7D01 Acquisition	6-11
Reset Output	6-13

PRELIMINARY SETUP INFORMATION. Perform the following steps before proceeding to any of the individual procedures.

a. Connect test equipment as shown in Figure 6-1. The Interface Test Fixture is connected to the DF ROM Extension circuit board as shown in Figure 6-2.

b. Set the System Test Fixture (067-0746-00) control switches (LATCH, FIXTURE, BREAK, INSTR CYCLE) to the Off position.

@

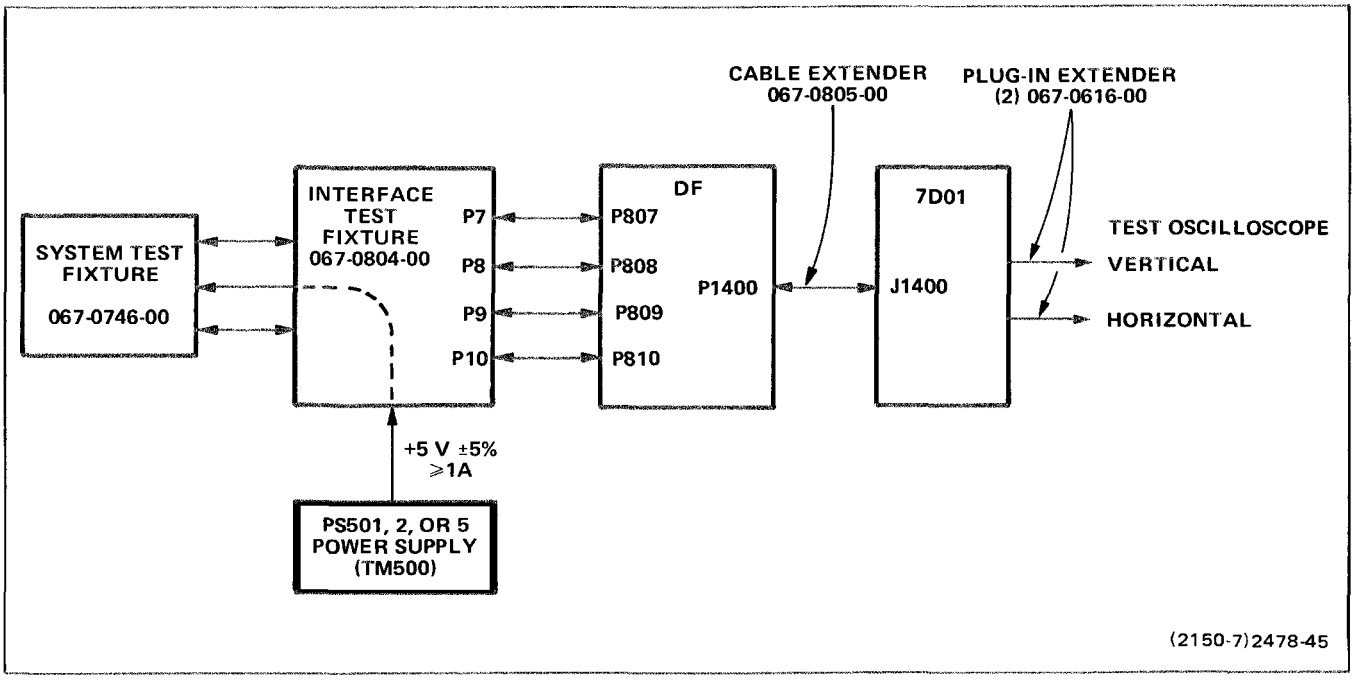


Figure 6-1. Test equipment setup for troubleshooting the DF Digital Formatter.

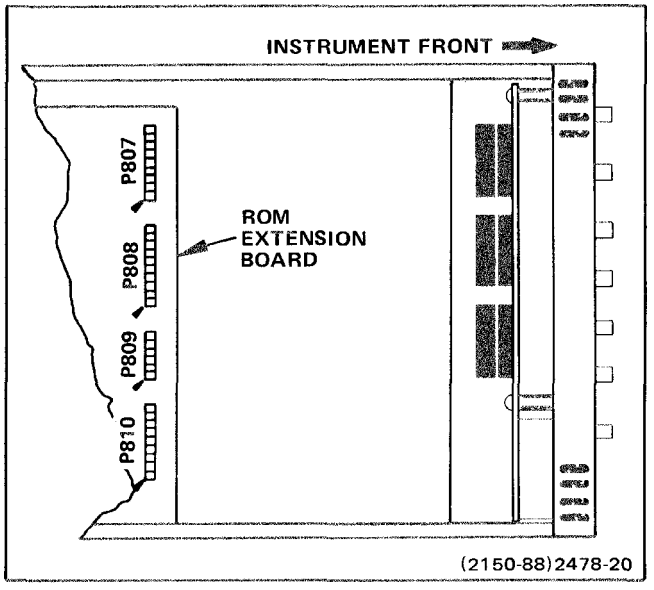


Figure 6-2. Partial view of ROM Extension board. Shows pin location and indexing for connection to the Interface Test Fixture.

c. Press the STOP button; the ABA (address bus available) indicator should light. If the ABA indicator does not light, press the RESTART button. If the ABA indicator still does not light, recheck the test equipment setup illustrated in Figure 6-1. Also, check the DF clock circuits (01, 02), reset circuit, power supplies, and the Halt line (pin 2 of U264). Check that the BA output (pin 7 of U264) is not excessively loaded or shorted (low). If the ABA indicator does not light, and all the above functions operate properly, either the test fixture or U264 is defective.

d. Once the ABA indicator is on, the 067-0746-00 System Test Fixture is effectively replacing the DF microprocessor (U264).

NOTE

The System Test Fixture DATA and ADDRESS switches, and the EXAMINE and DEPOSIT push buttons control the DF's data bus, address bus, and R/W line. At all times during this troubleshooting procedure, disregard the condition of the Address lights on the System Test Fixture.

e. All references to the setting of the ADDRESS and DATA switches will be in base 16 (hexadecimal) to indicate how each group of 4 switches is set, or each group of 4 lights is read. Refer to Table 6-2 for Hex-to-Binary conversion.

f. In general, if a peripheral does not operate properly on a Deposit or Examine function of one of its addresses, the line that generates that address should be checked (with a logic analyzer or a storage scope) to determine if it is pulsed low. If the line is not pulsed low, the defect will be in either the address coding circuitry or the System Test Fixture.

TABLE 6-2

Hex-to-Binary Conversion

Hex	Binary	Hex	Binary
0	0000	8	1000
1	0001	9	1001
2	0010	A	1010
3	0011	B	1011
4	0100	C	1100
5	0101	D	1101
6	0110	E	1110
7	0111	F	1111

DATA BUS AND RAM TEST. The object of this test is to ensure that the data bus lines are independent of each other, and no other peripheral is controlling the bus.

NOTE

A complete cell-by-cell test of only the Data RAM is executed by the DF microprocessor upon Restart. A defective cell is indicated on the crt display as "SEE MANUAL BAD RAM".

The testing method used is to address a RAM cell, write into it (Deposit), then read it (Examine). This is accomplished as follows:

a. Set the System Test Fixture (ADDRESS switches) to correspond to an address in one of the following RAM's.

1. Scratch pad RAM (Hex addresses 0000 through 007F).
2. Data RAM (Hex addresses 6000 through 63FF).

EXAMPLE:

The Scratch pad RAM, Hex address 007F, converted to binary is – 0000 0000 0111 1111. Select the ADDRESS switches on the System Test Fixture to match this address.

b. Set all (except one) of the System Test Fixture DATA switches to 0.

c. Press the DEPOSIT button, then the EXAMINE button, and note how the Data lights compare with the switches. The information you have put in the DATA switches should match the Data lights. Continue testing the data buses with a different switch high (1) each time. If, at any point the lights don't agree with the switch positions, check the RAM addressing and support circuits.

d. Set all (except one) of the System Test Fixtures DATA switches to 1. Repeat step c with a different switch set low (0) each time.

NOTE

If at any time the Data lights do not match the DATA switches in steps c and d, the problem is either a bad RAM IC, some other IC on the bus not being disabled, or the buses are either shorted together, to ground, open, or tied to Vcc. A good method to isolate an IC, which is not getting off the bus, is to disconnect the IC's on the data bus, one at a time, until the problem disappears.

ROM TEST. The object of this test is to ensure that the ROM IC's (U284, U294) are being addressed, and that they drive the data bus.

The method is to read (Examine) several addresses in each of the above ROM's and check that the proper output appears on the System Test Fixture Data lights. This is accomplished as follows:

a. Set the System Test Fixture (ADDRESS switches) to correspond to an address of one of the ROM IC's shown in Table 6-3.

EXAMPLE: ROM U284

Hex address F800 converted to binary is – 1111 1000 0000 0000 (refer to Table 6-2). Select the ADDRESS switches on the System Test Fixture to match this address.

b. Press the System Test Fixture EXAMINE button, and note how the Data lights compare with the Data Output listed for that address in Table 6-3.

c. If the Data lights do not match the Data Output listed, the address pins of the IC in question should be checked with a storage type test oscilloscope, or a logic analyzer to determine if:

1. The IC is being enabled (chip selects are correct).
2. The address lines A0-A10 levels correspond to the ADDRESS switch.

@

TABLE 6-3

ROM Hexadecimal Output Program

ROM U284		ROM U294	
Address	Data Output	Address	Data Output
F800	38	F000	CE
F801	39	F001	00
F802	8D	F002	00
F804	86	F004	00
F808	26	F008	7F
F810	10	F010	55
F820	39	F020	26
F840	97	F040	25
F880	F0	F080	C1
F900	13	F100	DF
FA00	73	F200	97
FC00	84	F400	5C

If the IC in question passes these last two checks (and the DF passed the previous test, Data Bus and RAM Test), substitute the IC with a known good ROM.

KEYBOARD TEST. The object of this test is to check for proper operation of the Keyboard circuit.

NOTE

A failure could originate in the Keyboard circuit IC's (U65, U172), the address decoding for them, or the interconnections on one of the specific push buttons used in the test.

If a specific push button switch appears to malfunction, first review the Basic Operating Instructions (in section 2 of this manual). This will confirm the normal operation for that switch in a particular mode. If the malfunction persists, and the problem is not a defective switch or dirty contacts, proceed to the Keyboard Circuit Checkout Procedure in Table 6-4.

The Keyboard Circuit Checkout Procedure (Table 6-4) checks the operation of a shift register. Therefore, the procedural steps must be performed in the exact sequence listed. An operator error incurred during the performance of this procedure invalidates the sequence, and step 1 of the Keyboard Circuit Checkout Procedure must be started again.

TABLE 6-4

Keyboard Circuit Checkout Procedure

Step	System Test Fixture		Comment
	Address	Data Light Display[1]	
1	00B6	XX[2]	Clears U65. No check; proceed to step 2.
2	Hold down TIMING DIAGRAM button on DF.		
3	00B0	EX[2]	Reads a Kybd 1 key down.[3]
4	00B0	FX[2]	Reads TIMING DIAGRAM key.
5	Hold down OCTAL button on DF.		
6	00B0	DX[2]	Reads a Kybd 2 key down.[3]
7	00B0	FX[2]	Reads OCTAL key down.
8	Hold down COL BLANK← button on DF.		
9	00B0	BX[2]	Reads Kybd 3 key down.[3]
10	00B0	FX[2]	Reads ← down.
11	Hold down STORE 7D01→ REF button on DF.		
12	00B0	7X[2]	Reads Kybd 4 key down.[3]
13	00B0	FX[2]	Reads STORE key down.

[1] The X means "disregard the lights in that part of the display".

[2] Press the System Test Fixture EXAMINE button.

[3] Refer to diagram 1 in the Diagrams and Circuit Board Illustrations section.

BUTTON LIGHTS TEST. The object of this test is to assure that each of the DF button lights operate properly.

NOTE

The DF SEARCH and STORE 7D01→ REF buttons do not have lights.

The button lights in the DF are driven by the outputs of a serial-to-parallel shift register. The System Test Fixture data bus 7 (DATA switch number 7) is the input, and a press of the DEPOSIT button (address 00B2) is the clock of this shift register.

Table 6-5 lists the number of times the DEPOSIT button must be pushed in order to control a given DF button light.

TABLE 6-5

Manual Clock Pulses Required To Control Button Lights

Number of Deposits (Clock)	Button Light
1	TIMING DIAGRAM
2	FAST
3	SLOW
4	MANUAL
5	Not Used
6	HEX
7	OCTAL
8	BINARY
9	MENU
10	7D01 ONLY
11	⊙ INTENS REF
12	TABLES= (Indicator light)
13	POS
14	NEG
15	←
16	→
17	FOLLOWS 7D01
18	HELD
19	FOLLOWS W/OFFSET
20	Not Used
21	7D01=REF
22	TABLES= (button light)

To completely check the button lights, proceed as follows:

a. Set the System Test Fixture DATA switch number 7 HI (1), and the ADDRESS switches for 00B2 (refer to Table 6-2).

b. Press the System Test Fixture DEPOSIT (manual clock) button the required number of times shown in Table 6-5, and note that the specified button light comes on.

NOTE

All button lights that are on at the start of this test will be shifted to the right and down with each each press of the Deposit button.

c. Set the System Test Fixture DATA switch number 7 LO (0).

d. Repeat step b and note the button light goes off.

If a button light fails to either turn on or off, check the LED, associated transistor, shift register, or the LED power supply (VR62, CR62, and R62).

DISPLAY TEST. There are four control bits with which the microprocessor controls the display. Two of these are at address 00A8. The other two (at address 0098) are used to control operation when in the 7D01 Timing Diagram mode. Checkout for proper display function is accomplished as follows:

a. Connect the DF Readout Source multi-pin jumper (internal) to display the formatter readout (FOR R). Refer to Figure 6-3.

Insure that the system Test Fixture ABA indicator light is on. Turn off the oscilloscope power momentarily. This action will load WOM RAM with random data for future display. Disregard the actual data that is displayed in the following checks. It's only purpose is to provide a method to check the mode of operation.

b. Set the System Test Fixture ADDRESS switches to 00A8, and the DATA switches as shown for that address on line 1 of Table 6-6.

c. Press the DEPOSIT button.

d. Set the System Test Fixture ADDRESS switches to 0098, and the DATA switches as shown for that address on line 1 in Table 6-6.

e. Press the DEPOSIT button.

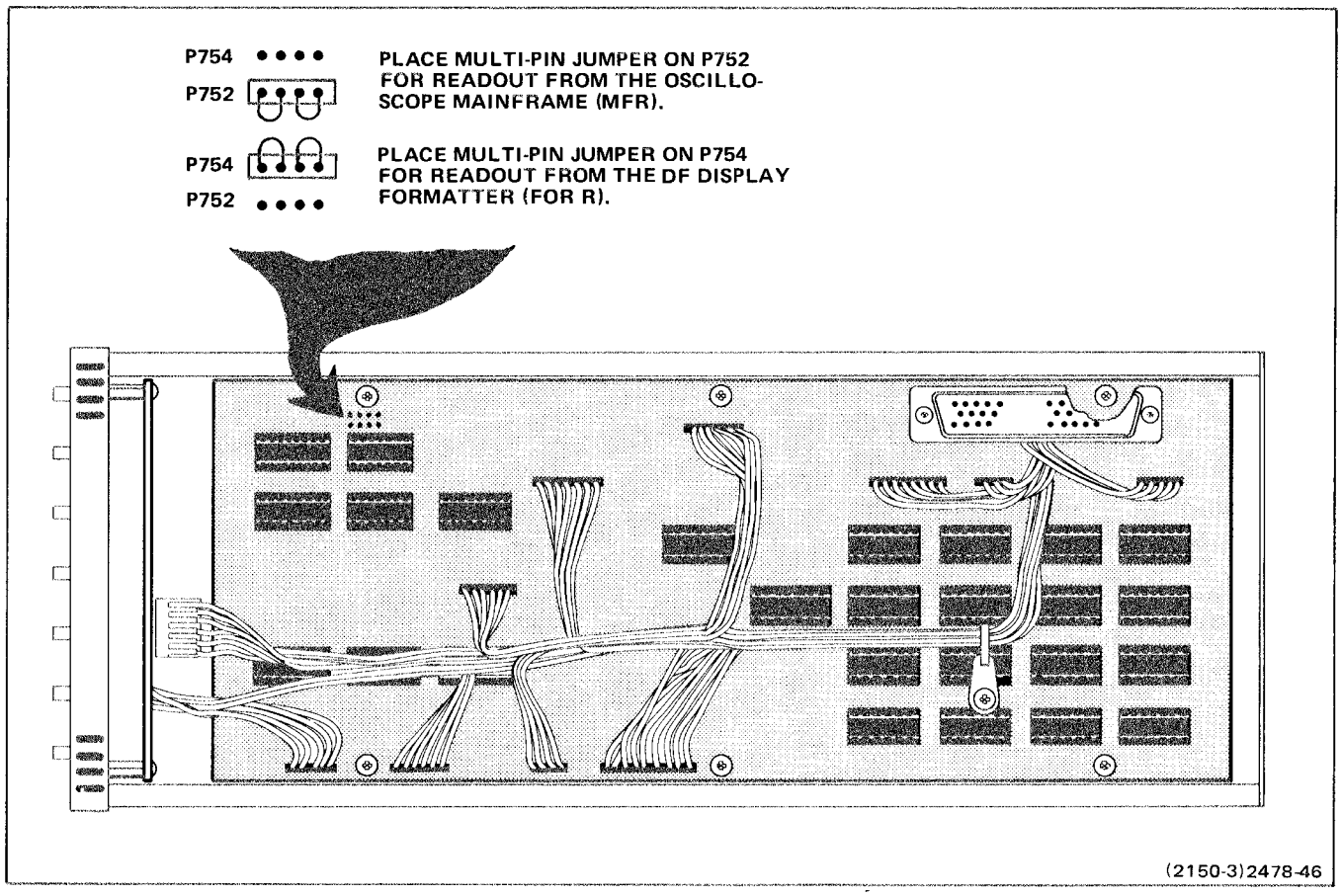


Figure 6-3. Location of readout source multi-pin jumper.

TABLE 6-6

Formatter Readout Truth Table

Line #	Data Switch Number (Address 00A8) 3*	1	0	(Address 0098) 3	0*	Display
1	X	0	0	1	X	Map mode, with 2 lines of DF readout. (No map is visible.)
2	1	1	0	1	1	7D01 Timing diagram display with 2 lines of DF readout, if triggered.[1]
3	1	1	0	0	1	Display 7D01 Timing diagram only—no DF readout, if triggered.[1]
4	X	1	1	X	X	Displays 19 lines of DF readout.

1 = HI, 0 = LO, X = DON'T CARE

*Control signals necessary only to produce a Timing Diagram display.

[1] If the 7D01 is not triggered, check that 7D01 Sample Interval switch is not in the EXTERNAL position, and press the Manual Trigger button; verify performance of the 7D01. Check DFs "7D01 reset" circuit.

f. Check for the proper display (as shown in Table 6-6 for line 1). If the display is correct, repeat the above procedure for lines 2, 3, and 4 of Table 6-6.

g. Connect the DF Readout Source multi-pin jumper (internal) to display mainframe readout (MFR). Refer to Figure 6-3.

h. Repeat steps b through f, using Table 6-7.

NOTE

If the display does not match that shown in Tables 6-6 and 6-7, first check the mode decoding circuitry, then the display. HINT—If the display doesn't work, follow the counter clocks around to assure they are all operating.

7D01 CONTROL SIGNALS. There are three control lines with which the microprocessor can directly control the 7D01.

Set up conditions as follows:

a. Connect the DF Readout Source multi-pin jumper (internal) to display the mainframe readout (MFR). Refer to Figure 6-3.

b. Set the System Test Fixture ADDRESS switches to 0098, and DATA switch number 0 to HI (1).

c. Press the DEPOSIT button.

d. Set the System Test Fixture ADDRESS switches to 00A8. Set DATA switches: number 3 to HI (1), number 1 to HI (1), and number 0 to LO (0).

e. Press the DEPOSIT button.

f. Press the 7D01 manual trigger button.

1. Cursor Increment. Check as follows:

a. Set the System Test Fixture ADDRESS switches for 00B7.

b. Press the EXAMINE button and observe that the cursor display on the crt moves one increment. Check that the cursor moves one increment each time the EXAMINE button is pressed. See note below.

NOTE

If the cursor does not perform properly, check that the 7D01 cursor position switch (both course and fine) are firmly seated in a detent; also check the cursor clock circuitry.

2. Display Clock. Check as follows:

TABLE 6-7

Mainframe Readout Truth Table

Line #	Data Switch Number (Address 00A8) 3*	1	0	Data Switch Number (Address 0098) 0	Display
1	X	0	0	0	Map mode, except for 2 lines DF readout.
2	X	1	0	0	No 7D01 display or readout.
3	1	1	0	1	Display 7D01 only, with readout, if triggered.[1]
4	X	0	1	X	Not a valid display.
5	X	1	1	0	Displays 19 lines of DF readout.

1 = HI, 0 = LO, X = DON'T CARE

*Control signals necessary only to produce a Timing Diagram display.

[1] If the 7D01 is not triggered, verify performance of the 7D01; check DF's "7D01 reset" circuit; check that 7D01 sample interval switch is not in the external position.

@

a. Set the System Test Fixture ADDRESS switches to 0098. Set DATA switch number 0 to LO (0).

b. Press the DEPOSIT button. The crt display should disappear.

c. Set the System Test Fixture DATA switch number 0 to HI (1).

d. Press the DEPOSIT button. The crt display should return.

NOTE

Address 0098 determines if the 7D01 display clock is on or off.

3. 7D01 Reset. Check as follows:

a. Set the System Test Fixture ADDRESS switches to 00A8. Set DATA switches: number 1 to HI (1), number 0 to LO (0), and number 3 to LO (0).

b. Press the DEPOSIT button. The 7D01 trig'd light should go out, and the crt display should disappear.

c. Set the System Test Fixture DATA switch number 3 to HI (1).

d. Press the DEPOSIT button.

e. Press the 7D01 manual trigger button. The crt display should return, and the trig'd light should stay on.

NOTE

DATA switch number 3 at address 00A8 controls the 7D01 reset.

7D01 ACQUISITION. Since the DF's acquisition of the 7D01's data is handled entirely by the microprocessor, this is the most complex interface. Check the Acquiring states of cursor counters, Acquiring 7D01 status, and Acquiring contents of 7D01 memory, as outlined in the following procedures.

Set up conditions as follows:

a. Connect the DF Readout Source multi-pin jumper (internal) to display the mainframe readout (MFR). Refer to Figure 6-3.

b. Set the System Test Fixture ADDRESS switches to 0098, and DATA switch number 0 to HI (1).

c. Press the DEPOSIT button.

d. Set the System Test Fixture ADDRESS switches to 00A8. Set the DATA switches: number 3 to HI (1), number 1 to HI (1), and number 0 to LO (0).

e. Press the DEPOSIT button.

f. Press the 7D01 manual trigger button.

1. CURSOR ACQUISITION. Check as follows:

a. Set the 7D01 data channels switch to 0-3.

b. Rotate the 7D01 cursor position switch (fine and course) to position the intensified dot one click before it disappears from the right side of the crt display.

c. Set the System Test Fixture ADDRESS switches to 00B6.

d. Press the EXAMINE button.

e. Set the System Test Fixture ADDRESS switches to 00B0.

f. Press the EXAMINE button 8 times, and observe that the Data light number 0 stays off.

g. Press the EXAMINE button 6 times. Data light number 0 should turn on and remain on.

h. Press the EXAMINE button once, and observe that Data light number 0 turns off.

i. Press the EXAMINE button once, and observe that Data light number 0 turns on again.

@

j. Rotate the 7D01 cursor position switch (fine) one click (dot disappears from the display).

k. Set the System Test Fixture ADDRESS switches to 00B6.

l. Press the EXAMINE button.

m. Set the System Test Fixture ADDRESS switches to 00B0.

n. Press the Examine button exactly 14 times. The Data bus light number 0 should remain lit through all 14 Examines.

o. Press the EXAMINE button 2 more times. The Data light number 0 should be off both times.

2. 7D01 STATUS. Check as follows:

NOTE

The 7D01 should be in external trigger, with no input.

a. Press the 7D01 manual reset button.

b. Set the System Test Fixture ADDRESS switches to 00B0.

c. Press the EXAMINE button.

d. Check that Data light number 2 is off.

e. Press the 7D01 manual trigger button.

f. Press the EXAMINE button. Observe that Data light number 2 is on.

g. Set the System Test Fixture ADDRESS switches to 00B5.

h. Press the EXAMINE button.

i. Set the System Test Fixture ADDRESS switches to 00B0.

j. Press the EXAMINE button. Observe that Data light number 1 is off.

k. Press the 7D01 manual reset button.

l. Press the 7D01 manual trigger button.

m. Press the EXAMINE button. Observe that Data light number 1 is on.

3. 7D01 Memory. Check as follows:

a. Connect the two P6451 probes (7D01 standard accessories) to the 7D01 connectors.

b. Set the 7D01 front-panel controls as follows:

Threshold Voltage . . . . . .TTL
Sample Interval. . . . . .External
Ext Clock Polarity. . . . . .⌐
Data Channels. 0-15
Data Position . . . . . .Post Trig

c. Connect the P6451 probe test leads as follows:

(1) Both probe ground leads to the Interface Test Fixture ground terminals.

(2) Channel 12 probe lead to terminal 0.

(3) External clock probe lead to terminal C.

d. Press the 7D01 manual reset button.

e. Press the 7D01 manual trigger button (if trig'd light is not on).

f. Set the System Test Fixture ADDRESS switches to 0098. Set DATA switches: number 3 to HI (1), and number 0 to LO (0).

g. Press the DEPOSIT button.

@

NOTE

If a bright dot appears on the crt display, either position it off-screen, or reduce the oscilloscope intensity.

h. Set the System Test Fixture ADDRESS switches to 00B1.

i. Press the EXAMINE button.

j. Check that Data light number 5 is on, number 6 is on, and number 7 is off.

k. Press the EXAMINE button once. Data light number 4 should change state.

l. Press the EXAMINE button once. Data light number 5 should go off, and Data light number 4 should change state again.

m. Continually press the EXAMINE button. Note that Data light number 5 remains off, light number 6 remains on, and light number 4 changes state with each press of EXAMINE. Stop pressing the EXAMINE button when Data light number 7 comes on (approximately 15-20 Examines).

n. Press the EXAMINE button once more. Check that Data light number 7 is off, and that light number 4 changes state.

RESET OUTPUT. The logic level of the DF reset output (RESET OUT jack on DF front panel) is the inverse of whatever is deposited into the System Test Fixture DATA switch 1 at address 0098.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques required to replace components in this instrument are given here.

OBTAINING REPLACEMENT PARTS

All electrical and mechanical part replacements can be obtained through your Tektronix Field Office or representative. However, many of the standard electronic components can be obtained locally in less time than is required to order them from Tektronix, Inc. Before purchasing or ordering replacement parts, check the parts list for value, tolerance, rating, and description.

NOTE

When selecting replacement parts, it is important to remember that the physical size and shape of a component may affect its performance in the instrument, particularly at high frequencies. All parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance.

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements, or are manufactured for Tektronix, Inc. to our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine the manufacturer of parts, refer to parts list, Cross Index Mfg. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.
2. Instrument serial number.
3. A description of the part (if electrical, include circuit number).
4. Tektronix part number.

WARNING

To avoid electric shock, disconnect the instrument from the power source before soldering.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument. Use only 60/40 rosin-core electronic-grade solder. The choice of soldering iron is determined by the repair to be made. When soldering on circuit boards, use a 15- to 25-watt pencil-type soldering iron with a 1/8-inch wide, wedge-shaped tip. Keep the tip properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the wiring from the base material. Avoid excessive heat; apply only enough heat to remove the component or to make a good solder joint. Also, apply only enough solder to make a firm solder joint; do not apply too much solder.

CAUTION

The Acquisition, Intelligence, and Button Lights circuit boards in this instrument are multilayer type boards with a conductive path(s) laminated between the top and bottom board layers. All soldering on these boards should be done with extreme care to prevent breaking the connections to the center conductor(s); only experienced maintenance personnel should attempt repair of these boards.

For metal terminals, (e.g., coaxial connector, ground lug, etc.) a higher wattage soldering iron may be required. Match the soldering iron to the work being done. For example, if the component is connected to the chassis or other large heat-radiating surface, it will require a 40-watt or larger soldering iron.

The following technique should be used to replace a component on a circuit board:

1. Grip the component lead with long-nose pliers. Touch the soldering iron to the lead at the solder connection. Do not lay the iron directly on the board, as it may damage the board.

2. When the solder begins to melt, gently pull the lead out. If unable to pull the lead out of the circuit board without using force, try removing the other end of the component as it may be more easily removed.

NOTE

The reason that some component leads seem troublesome to remove is due to a bend placed in each lead during the manufacturing process. The purpose of the bent leads is to hold the component in place during a flow-soldering manufacturing process that solders all components at one time.

If a component lead is extremely difficult to remove, it may be helpful to straighten the leads on the back side of the board with a small screwdriver or pliers while heating the soldered connection.

Unsolder the component from the circuit board using heat on the component lead so that the solder will stay behind on the board. If you desire to remove solder from a circuit board hole for easier installation of a new component, use a solder-removing wick.

3. Bend the leads of the new component to fit the holes in the board. If the component is replaced while the board is mounted in the instrument, cut the leads so they will just protrude through the board. Insert the leads into the holes in the board so the component is firmly seated against the board (or as positioned originally). If it does not seat properly, heat the solder and gently press the component into place.

4. Touch the iron to the connection and apply a small amount of solder to make a firm solder joint. To protect heat-sensitive components, hold the lead between the component body and the solder joint with a pair of long-nose pliers or other heat sink.

5. Clip the excess lead that protrudes through the board (if not clipped in step 3).

6. Clean the area around the solder connection with a flux-removing solvent. Be careful not to remove information printed on the board.

COMPONENT REMOVAL AND REPLACEMENT

WARNING

To avoid electric shock, disconnect the instrument from the power source before replacing components.

The exploded-view drawing associated with the Replaceable Mechanical Parts list may be helpful in the removal or disassembly of individual components or subassemblies. Component locations are shown in the Diagrams and Circuit Board Illustrations section.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are given in the Replaceable Electrical Parts list for completely wired boards. Refer to Figure 6-4 for circuit board locations.

A2–BUTTON LIGHTS CIRCUIT BOARD. To remove the circuit board:

1. Position instrument upside down with front panel facing you. Carefully pry front panel away from sub-panel using a small screwdriver in slot provided on sub-panel bottom. Carefully remove front panel.

2. Note colors of the three multi-pin connectors and the P number to which each connects on the two front sub-panel mounted circuit board assemblies.

3. Remove 4 screws (A, B, C, and D on Figure 6-5) from front sub-panel assembly.

4. Remove 4 screws (A, B, C, and D on Fig. 6-6) from Button Lights circuit board. Carefully lift board away from sub-panel assembly.

5. To replace Button Lights circuit board, reverse order of removal, and snap panel back into position.

A1–FORMATTER KEYBOARD CIRCUIT BOARD. To remove the circuit board:

1. Remove A2–Button Lights circuit board as previously described.

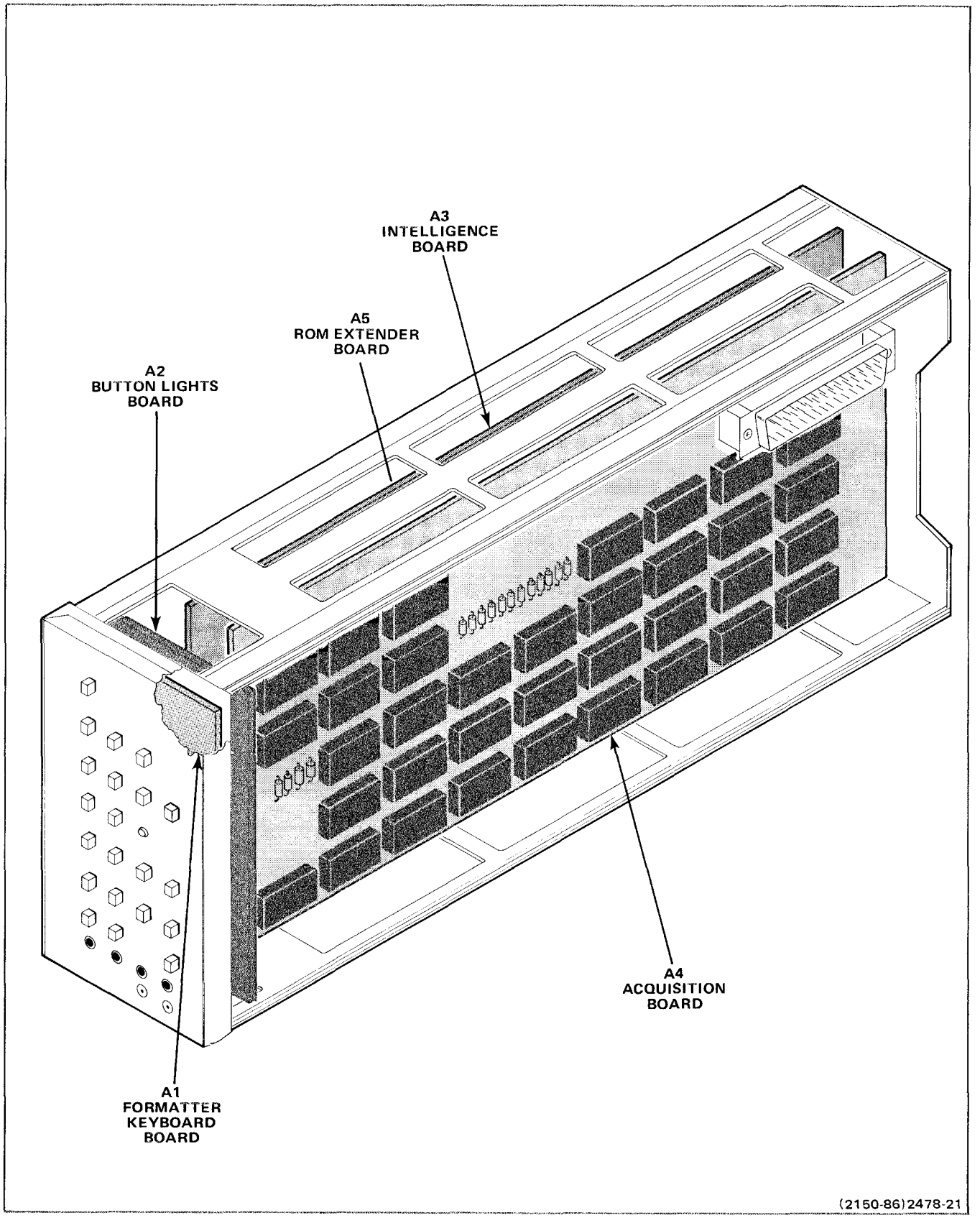


Figure 6-4. Circuit board locations.

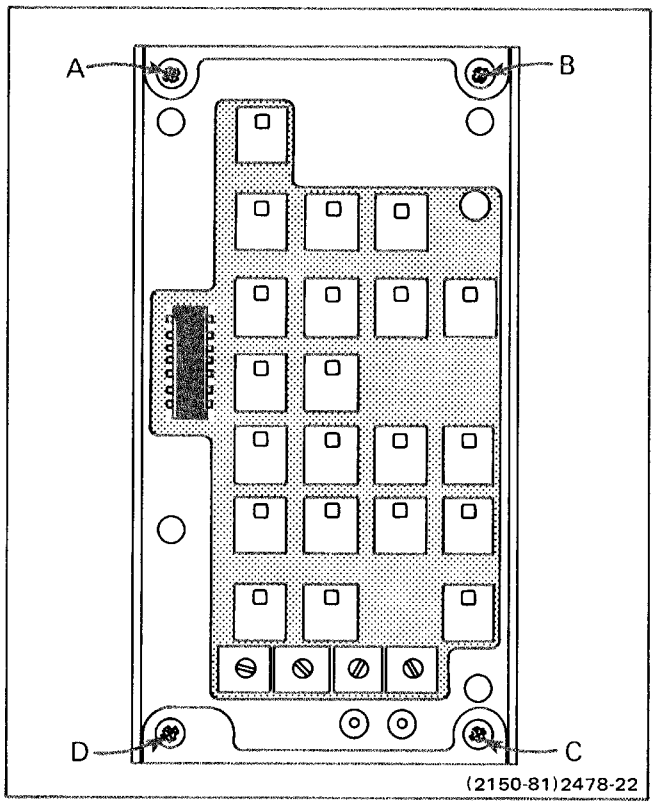


Figure 6-5. Locations of securing screws on the front sub-panel.

2. Disconnect 2 wires (W1 and W2 on Figure 6-7). Remove 4 hexagonal spacers (A, B, C, and D on Figure 6-7), and lift board away from front sub-panel.

3. To replace A1—Formatter Keyboard circuit board, reverse order of removal.

A5—ROM EXTENDER CIRCUIT BOARD. To remove the circuit board.

1. Note the color of all multi-pin connectors and the P number to which each connects.

2. Disconnect all cables that terminate on A5—ROM Extender circuit board.

3. Remove 3 screws (G, H, and I on Figure 6-8).

4. Lift circuit board clear of instrument.

5. To replace A5—ROM Extender circuit board, reverse order of removal.

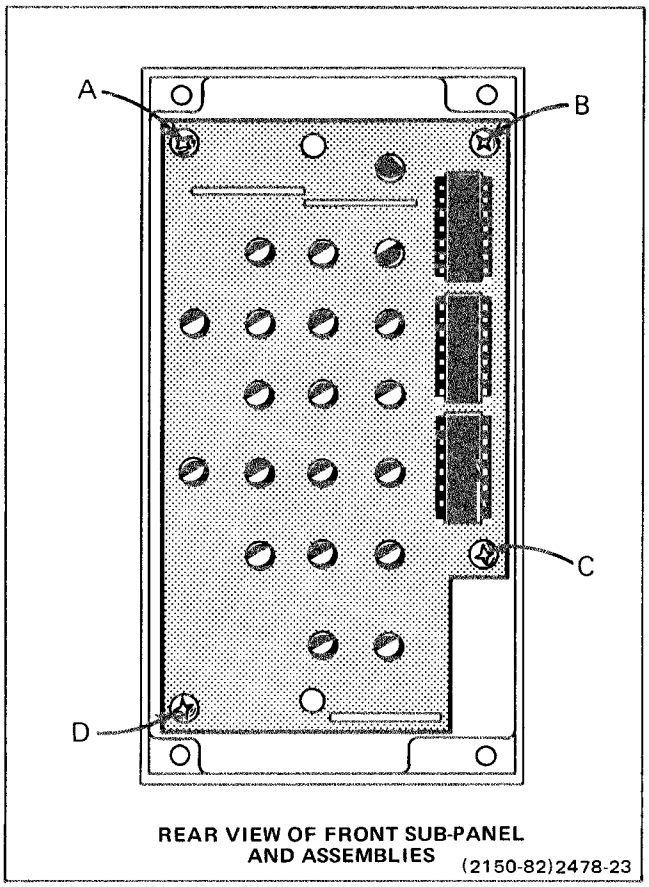


Figure 6-6. Locations of securing screws on A2 Button Lights circuit board.

A3—INTELLIGENCE CIRCUIT BOARD. To remove the circuit board:

1. Remove A5—ROM Extender circuit board as previously described.

2. Remove 6 screws (A, B, C, D, E, and F on Figure 6-8).

3. Carefully disengage interconnecting board pins (one row of interconnecting pins at front panel end of board, and one row near rear panel). Lift board clear of instrument between top and bottom frame rails.

4. To replace A3—Intelligence circuit board, reverse order of removal. The use of a small screwdriver may aid in aligning the circuit board connecting pins with their sockets.

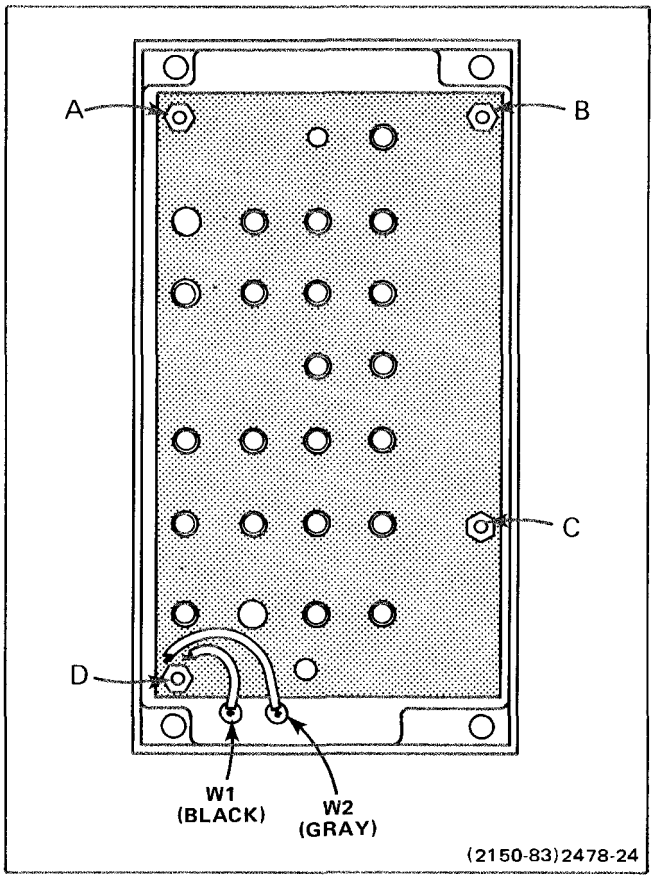


Figure 6-7. Locations of hex securing spacers and wiring to be disconnected on A1 Formatter Keyboard circuit board.

A4—ACQUISITION CIRCUIT BOARD. To remove the circuit board:

1. Remove 3 screws (A, B, and C on Figure 6-9).

2. Note color of all multi-pin connectors and the P number to which each connects.

3. Disconnect all cables that terminate on A4— Acquisition circuit board.

4. Remove 6 screws (D, E, F, G, H, and I on A4—Acquisition circuit board).

5. Carefully disengage interconnecting board pins (one row of interconnecting pins at front panel end of board, and one row near rear panel). Lift board clear of instrument between top and bottom frame rails.

6. To replace A4—Acquisition circuit board, reverse order of removal. The use of a small screwdriver may aid in aligning the circuit board connecting pins with their sockets.

PUSHBUTTON SWITCHES

All the pushbutton switches used in this instrument are mounted on the A1—Formatter Keyboard circuit board. First, remove the A1—Formatter Keyboard circuit board following the procedure given under Circuit Boards in this section. To remove any switch from the board, simply push from the rear of the switch until the two plastic retainers disengage from the board. To replace the switch, align the two plastic retainers with the mating holes in the circuit board and snap into position.

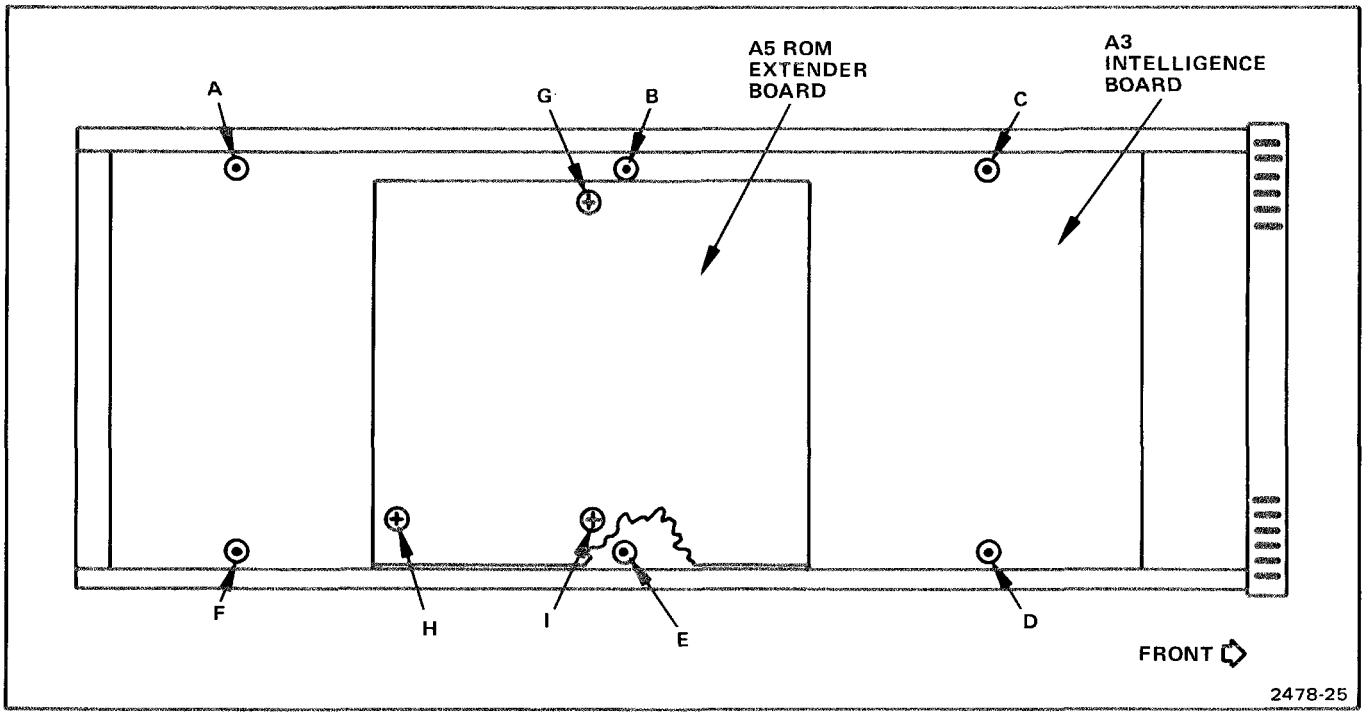


Figure 6-8. Locations of securing screws on A3 Intelligence circuit board and A5 ROM Extender circuit board.

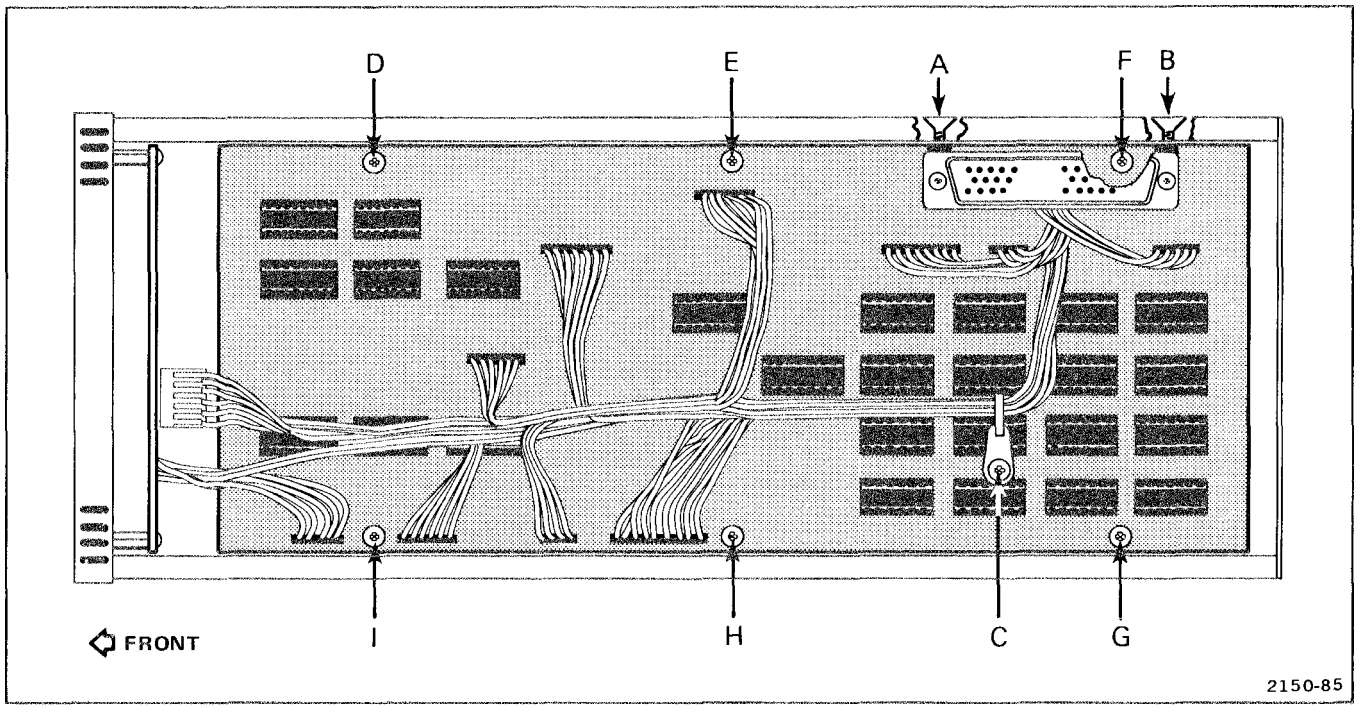


Figure 6-9. Locations of securing screws and hardware mounting screws on A4 Acquisition circuit board.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of this instrument. When semiconductors are replaced, check the operation of the part of the instrument which may be affected.

WARNING

To avoid electric shock, power must be turned off before removing or replacing semiconductors.

Replacement devices should be of the original type or a direct replacement. The lead configurations of the semiconductor devices used in this instrument are shown in the Diagrams and Circuit Board Illustrations section. When replacing, check the manufacturer's basing diagram for correct basing.

An extracting tool should be used to remove the 14-, 16-, 20-, and 40-pin integrated circuits to prevent damage to the pins. This tool is available from Tektronix, Inc. Order Tektronix Part 003-0619-00. If an extracting tool is not available when removing one of these integrated circuits, pull slowly and evenly on both ends of the device. Try to avoid having one end of the integrated circuit disengage from the socket before the other, as the pins may be damaged.

INTERCONNECTING PINS

All interconnections in this instrument are made utilizing pins soldered into the board. Two types of mating connectors are used for these interconnecting pins. If the mating connector is mounted on a plug-on circuit board, a special socket is soldered into the board. If the mating connector is on the end of a lead, an end-lead pin connector is used which mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

CIRCUIT-BOARD PINS. A circuit-board pin replacement kit (including necessary tools, instructions, and replacement pins with attached ferrules) is available from Tektronix, Inc. Order Tektronix Part 040-0542-00. Replacing circuit-board pins on multi-layer boards is not recommended; refer such repairs to your local Tektronix Field Office or representative.

To replace a damaged pin, first disconnect any pin connectors. Then unsolder (see Soldering Techniques) the damaged pin and pull it from the board with a pair of pliers, leaving the ferrule (see Fig. 6-10) in the circuit board if possible. If the ferrule remains in the circuit board, remove the spare ferrule from the replacement pin and press the new pin into the hole in the circuit board. If the ferrule is removed with the damaged pin, clean out the hole using a solder-removing wick and a scribe. Then press the

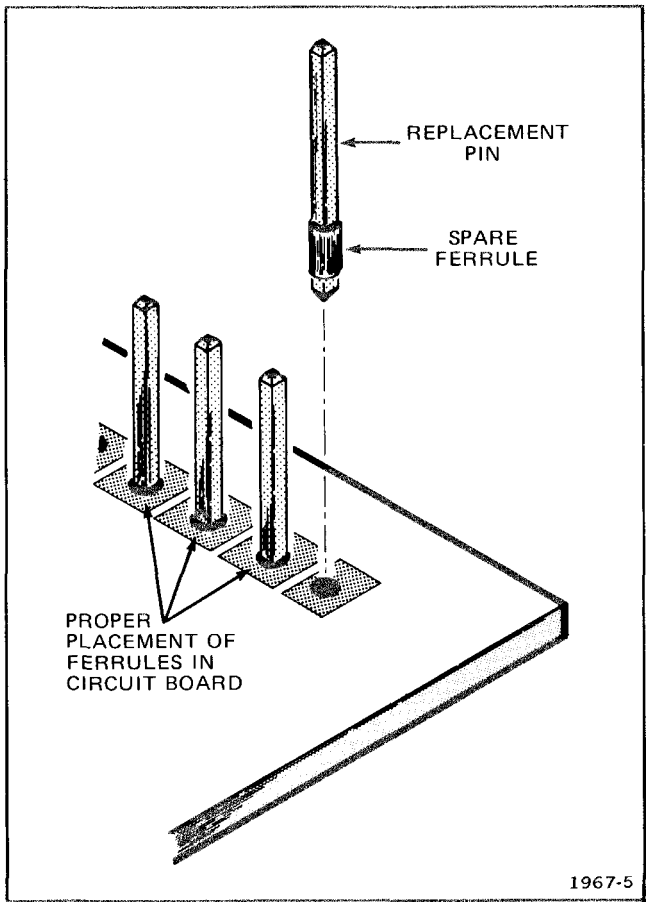


Figure 6-10. Exploded view of circuit-board pin and ferrule.

replacement pin, with attached spare ferrule, into the circuit board. Position the replacement pin in the same manner as the original pin had been. Solder the pin to the circuit board on each side of the board. If the original pin was bent at an angle to mate with a connector, carefully bend the new pin to the same angle. Replace the pin connector.

CIRCUIT-BOARD PIN SOCKETS. The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (use a vacuum-type desoldering tool to remove excess solder). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit board; be careful not to get solder inside the socket.

CAUTION

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

END-LEAD PIN CONNECTORS. The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged end-lead pin connectors, remove the old pin connector from the end of the lead and clamp the replacement connector to the lead.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and installed as a multi-pin connector (see Troubleshooting Aids). If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as other closely related circuits. See Section 7 for a complete Adjustment procedure.

PERFORMANCE CHECK AND ADJUSTMENT

This section provides information necessary to check performance requirements, functions which require removal of side panels, detailed checks of the DF memory, and to make internal adjustments. An additional Functional Check procedure, in the Operating Instruction section, checks the functions of the front-panel controls.

PRELIMINARY INFORMATION

ADJUSTMENT INTERVAL

To maintain instrument accuracy, check the performance of the DF every 1000 hours of operation, or every 6 months if used infrequently. Before complete adjustment, thoroughly clean and inspect this instrument as outlined in section 4, Maintenance.

TEKTRONIX FIELD SERVICE

Tektronix Field Service Centers and Factory Service Centers provide instrument repair and adjustment services. Contact your Tektronix Field Office or representative for further information.

PERFORMANCE CHECK

Performance of this instrument can be checked by performing only the Performance Check. This procedure checks the instrument against the tolerances listed in the Performance Requirement column of the DF Specifications, and also checks the DF memory. Performance Check Table 7-1 (derived from the Specifications in the General Information section) briefly describes the test method to check the performance requirement for a given characteristic. To completely check all instrument functions, as well as instrument performance, perform the Functional Check (located in the Operating Instructions section) and Performance Check procedures.

ADJUSTMENT PROCEDURE

Completion of the Adjustment procedure ensures that the instrument is correctly adjusted. Instrument performance is checked before an adjustment is made.

PARTIAL PROCEDURE

A partial performance check or adjustment may be desired after replacing components or to touch up the adjustment portion of the instrument. Each Performance Check and Adjustment step is written to stand alone. Therefore to perform a partial procedure proceed to the desired numbered step (1, 2, 5, etc.) and follow the procedure.

TABLE 7-1

Performance Check Description

Characteristic	Performance Requirement	Test Method
External Read Clock		
Frequency Range	100 kHz to 500 kHz.	Not Tested.
Duty Cycle	50% within 5%.	Not Tested.
Display		
Vertical Size	Adjustable from 6.9 div, or less, to at least 8.1 div from the top of the first line of DF readout to the bottom of the last line of DF readout.	Not Tested.
Vertical Position	Adjustable to vertical center of display area in any calibrated 7000-series mainframe.	Not Tested.
Horizontal Position	Adjustable to horizontal center of display area in any calibrated 7000-series mainframe.	Not Tested.

TABLE 7-1 (CONT.)

Performance Check Description

Characteristic	Performance Requirement	Test Method
Output Signals		
Reset Logic Voltage Level	LO: +0.4 V, or less, at 2 mA.	LO tested by connecting 7D01 channel 0 probe and 2 mA source (2.4 kilohm to +5 V) to RESET OUT jack. (7D01 Threshold Voltage set to +0.4 V.)
	HI: at least +2.4 V at 2 mA.	HI tested by connecting 7D01 channel 0 probe and 2 mA drain (1.2 kilohm to gnd.) to RESET OUT jack. (7D01 Threshold Voltage set to +2.4 V.)
Waveshape	Positive-going rectangular pulse.	Checked indirectly above.
Duration	100 μs within 50 μs when used with the 7D01 internal read clock.	Checked by using trigger-to-cursor readout on displayed pulse (1 μs sample interval).

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 7-2 is required for a complete performance check and adjustment of this instrument. The specifications for test equipment, given in Table 7-2, are the minimum required to meet the Performance Requirements. Detailed operating instructions for test equipment are omitted in this procedure. Refer to the test equipment instruction manual if more information is needed.

SPECIAL FIXTURES

Special fixtures are used only where they facilitate instrument adjustment. These fixtures are available from Tektronix, Inc. Order by part number from Tektronix Field Offices or representatives.

TEST EQUIPMENT ALTERNATIVES

The test equipment listed in the Examples of Applicable Test Equipment column, Table 7-2, is required to check and adjust this instrument. The Performance Check and Adjustment procedure is based on the first item of equipment given as an example. If other equipment is substituted, control settings or setups may need to be altered. If the exact item of equipment given as an example is not available, refer to the Minimum Specifications column to determine if other equipment may be substituted. Then check the Purpose column. If you determine that your measurement requirements will not be affected, the item and corresponding step(s) can be deleted.

TABLE 7-2

Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
1. Oscilloscope mainframe	Tektronix 7000-series with 2 vertical and 1 horizontal plug-in compartments.	Provides display for 7D01 and DF.	a. TEKTRONIX 7603 Oscilloscope. b. Refer to the TEKTRONIX catalog for a compatible oscilloscope mainframe.
2. Logic Analyzer with Data Acquisition Probes.	Tektronix 7D-series compatible with DF.	The DF is operable only with a companion Logic Analyzer.	a. TEKTRONIX 7D01 Logic Analyzer with two P6451 Data Acquisition Probes.
3. TTL Signal Source	Clock and 8-bit counter. Clock frequency; approximately 1 kilohertz.	Provides standard input signals to 7D01.	a. TEKTRONIX 067-0804-00 TEST FIXTURE. b. Circuit as shown in Figure 7-2.
4. +5-Volt Power Supply	Current; at least 100 mA.	Provides power to TTL Signal Source and provides 2 mA source for Reset Out check.	a. TEKTRONIX PS501 Power Supply with TM500-series Power Module.
5. Voltmeter	Range; +0.4 V to +2.4 V.	Set 7D01 Variable Threshold Voltage during Reset Out check.	a. Triplett 630-NA VOM. b. Simpson 262.

INDEX TO PERFORMANCE CHECK AND ADJUSTMENT

PAGE

PRELIMINARY PROCEDURE 7-3

PERFORMANCE CHECK PROCEDURE

1. Check Trigger Points 7-4
2. Check Old Data 7-5
3. Check Data Acquisition 7-6
4. Check Mainframe Readout 7-6
5. Check Reset Out Pulse 7-7

ADJUSTMENT PROCEDURE

1. Adjust Horizontal Gain 7-8

PRELIMINARY PROCEDURE

1. Before connecting the DF Display Formatter to the 7D01 Logic Analyzer, set the 7D01 for "first trigger" operation (see Fig. 7-1), and check that the DF is set for Formatter Readout (FOR R).

2. Attach the DF to the 7D01 and install the three-wide plug-in assembly into the oscilloscope mainframe (refer to Installation, in the General Information section, for assembly instructions).

3. Connect the Interface Test Fixture to the 7D01 as shown in Figure 7-2.

4. Set the 7D01 Logic Analyzer controls as follows:

Sample Interval	Ext
Record Display Time	∞
Data Position	Post Trig
Data Channels	0-15
Trigger Source	W.R.
Word Recognizer	
Ch 0 through Ch 15	Lo
External Qualifier	X
Probe Qualifier	X
W.R. Mode	Sync.
Threshold Voltage	TTL (+1.4 V)
Ext Clock Polarity	⌐

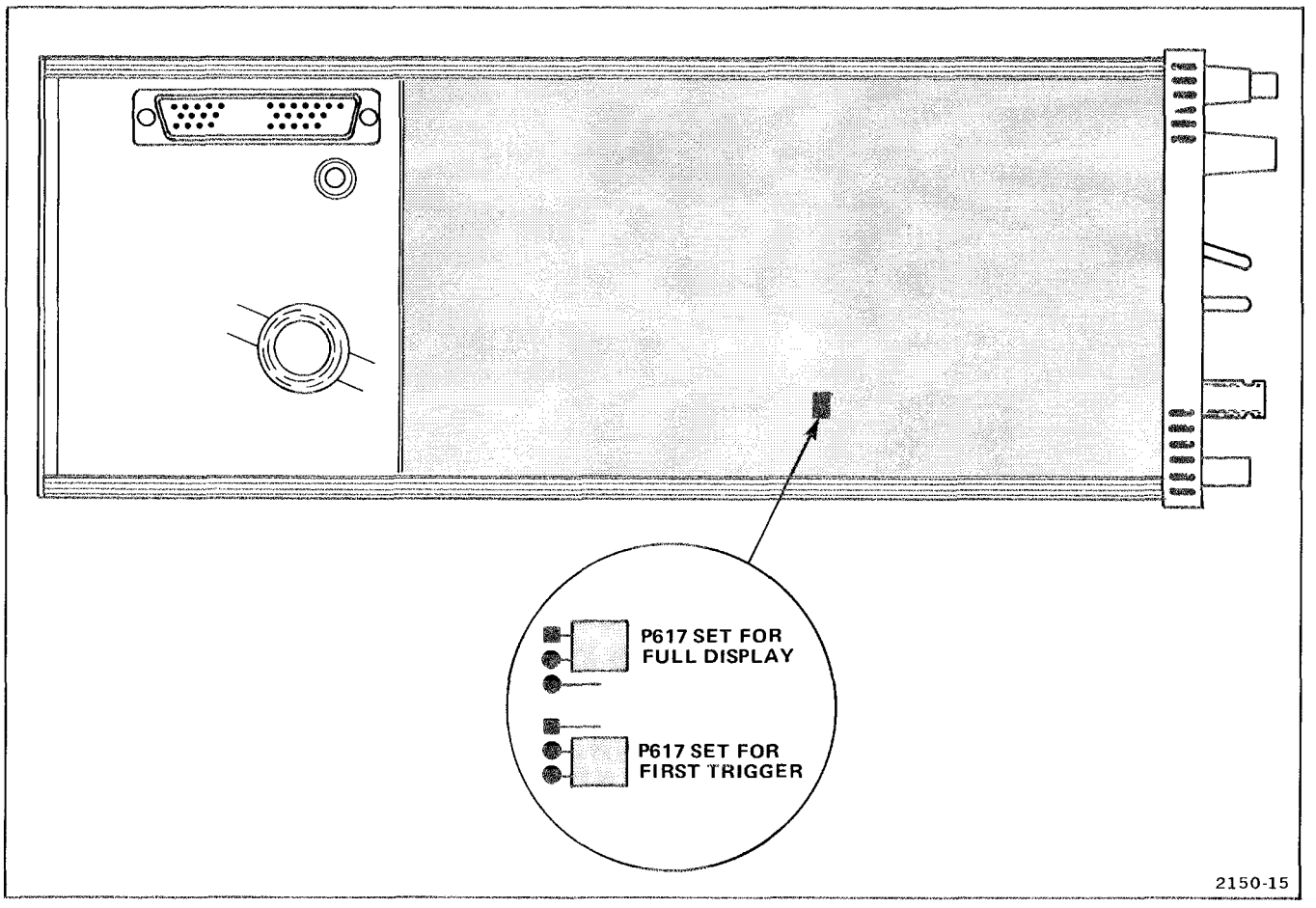


Figure 7-1. Location of 7D01 Full Display/First Trigger jumper.

5. Perform the Power-On function (turn mainframe power off, wait approximately 10 seconds, and turn power on).

PERFORMANCE CHECK PROCEDURE

1. Check Trigger Points

a. Perform the Preliminary Procedure.

b. Adjust mainframe intensity and 7D01 Vert and Horiz controls for a well-defined Timing Diagram display.

c. Check that the trigger-to-cursor readout (top of display) is +0 and the cursor word readout (bottom of display) is 0000 0000 0000 0000 when the trigger and cursor intensified spots are superimposed.

d. Change the 7D01 Data Channels switch to 0-7 position and press the Record Manual Reset push button.

e. Set the 7D01 Cursor position controls to superimpose the cursor tnd trigger intensified spots on the display.

f. Check that the trigger-to-cursor readout is +0 and the cursor word readout is 0000 0000.

g. Change the 7D01 Data Channels switch to 0-3 position and press the Record Manual Reset push button.

h. Set the 7D01 Cursor position controls to superimpose the cursor and trigger intensified spots on the display.

i. Check that the trigger-to-cursor readout is +0 and that the cursor word readout is 0000.

j. Change the 7D01 Data Channels switch to 0-15 position and the Data Position switch to Center position.

@

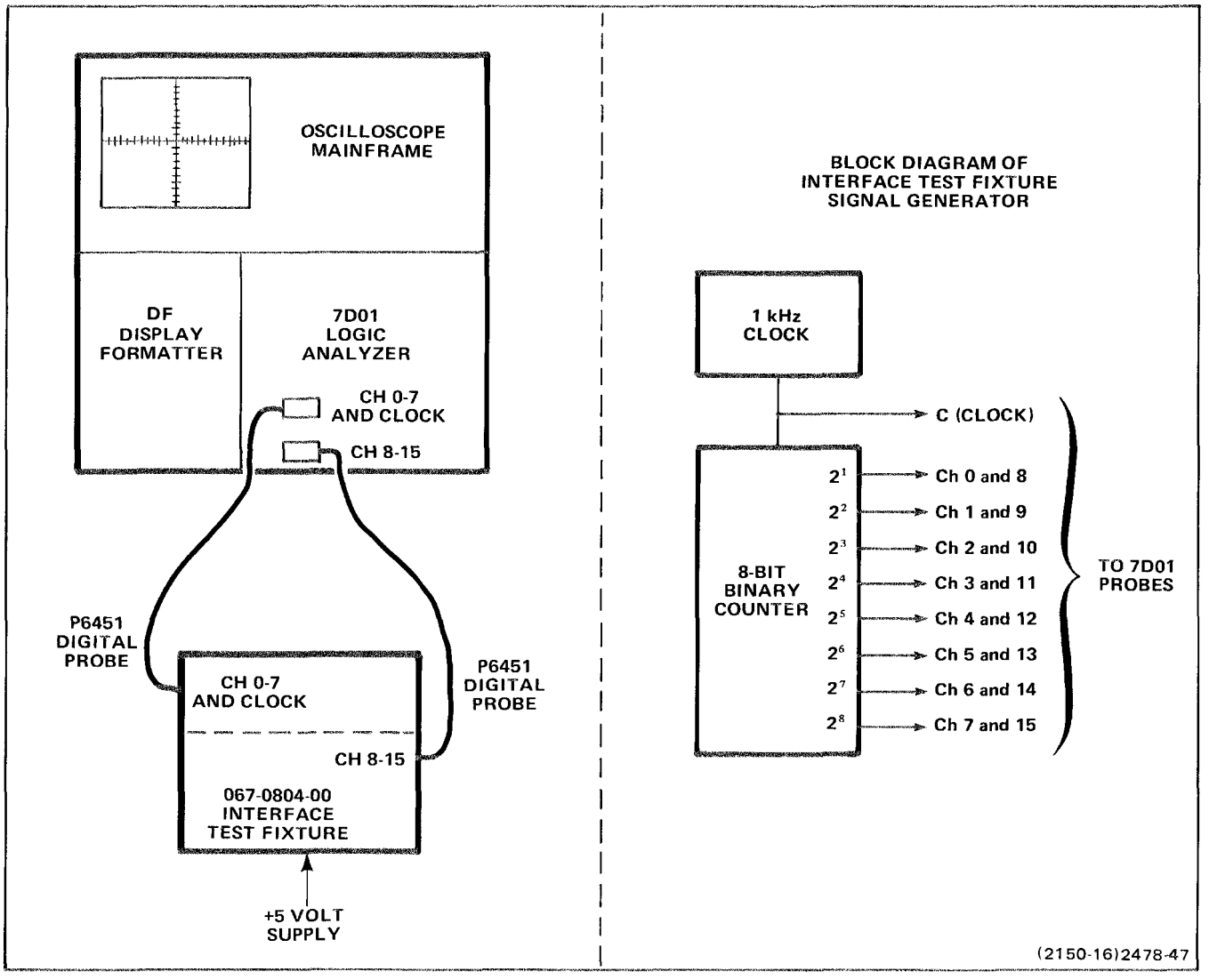


Figure 7-2. Test setup for Performance Check and Adjustment Procedure.

k. Press the Record Manual Reset push button and repeat parts c through i.

l. Change the 7D01 Data Channels switch to 0-15 position and the Data Position switch to Pre Trig position.

m. Press the Record Manual Reset push button and repeat parts c through i.

2. Check Old Data.

a. Perform Preliminary Procedure.

b. Adjust mainframe intensity and 7D01 Vert and Horiz controls for a well-defined Timing Diagram display.

c. Change 7D01 Trigger Source switch to Ch 0 position and press the Record Manual Reset push button.

d. Rotate the 7D01 Cursor Fine Pos control counter-clockwise until the cursor intensified spots disappear.

e. Check that the cursor readout (bottom of display) disappears at the same time as the cursor intensified spots.

f. Repeat parts c through e for all positions of the 7D01 Data Position and Data Channels switches.

3. Check Data Acquisition

a. Perform the Preliminary Procedure.

b. Press the STATE TABLE HEX push button.

c. Adjust mainframe intensity for a well-defined display.

d. Check that the top 16 rows of columns 1 and 3 display 0 through F (see Figure 7-3).

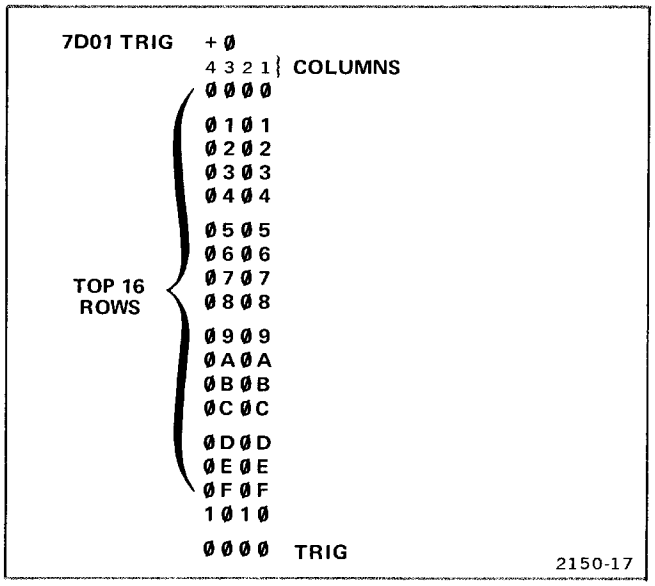


Figure 7-3. Hexadecimal State Table display.

e. Rotate the 7D01 Cursor Coarse position switch one position clockwise at a time. Check that the data displayed in columns 1 and 3 remain the same, and that the top 16 rows of columns 2 and 4 change from all 0's (7D01 TRIG +0), to all 1's (7D01 TRIG +16), etc., through all F's (7D01 TRIG —16). Ignore any X's or *'s in the displays.

f. Change the 7D01 Data Channels switch to 0-7 position and press the Record Manual Reset push button.

g. Rotate the 7D01 Cursor position controls to set the trigger-to-cursor readout to +0.

h. Check that the top 16 rows of column 1 display 0 through F.

i. Rotate the 7D01 Cursor Coarse position switch one position clockwise at a time. Check that the data displayed in column 1 remain the same, and that the top 16 rows of column 2 change from all 0's through all F's twice while the trigger-to-cursor readout advances from +0 through —16. Ignore any X's or *'s in the displays.

j. Change the 7D01 Data Channels switch to 0-3 position and press the Record Manual Reset push button.

k. Rotate the 7D01 Cursor position controls to set the trigger-to-cursor readout to +0.

l. Check that the top 16 rows display 0 through F.

m. Rotate the 7D01 Cursor Coarse position switch clockwise and check that the display remains the same, while the trigger-to-cursor readout advances from +0 through —16. Ignore any X's or *'s in the display.

4. Check Mainframe Readout

a. Perform Preliminary Procedure.

b. Adjust mainframe intensity for a well-defined Timing Diagram display.

c. Note the normal (formatter) readout at the top and bottom of the display.

d. Turn off power to the mainframe and remove the 7D01-DF (do not disconnect the probes from the 7D01). Disconnect the DF from the 7D01 (refer to Installation, in the General Information section, for instructions).

e. Set the DF Readout Source jumper to the MFR (mainframe readout) position.

f. Connect the DF to the 7D01 and install into the main mainframe.

g. Adjust the mainframe readout intensity control and check that crt readout can be obtained.

@

h. Press the MAP FAST push button and check that normal (formatter) readout is present.

i. Press the STATE TABLE HEX push button and check that normal readout is present.

j. Turn off power to the mainframe and remove 7D01-DF1.

k. Disconnect the DF from the 7D01 and set the DF Readout Source jumper to FOR R (formatter readout).

l. Reconnect the DF to the 7D01.

5. Check Reset Out Pulse

a. Set the 7D01 for First Trigger mode (internal jumper). Set 7D01 controls as follows:

Sample Interval . . . . . .1 μs
Record Display Time . . . . . .∞
Data Channels. 0-3
Data Position . . . . . .Post Trig
Trigger Source . . . . . .Ch 0
Threshold Voltage . . . . . .Var (±12 V)

Leave all probe tips open.

b. Turn on power to mainframe.

c. Press 7D01 Manual Trigger push button and adjust mainframe intensity and 7D01 Vert and Horiz controls for a well-defined Timing Diagram display (four traces).

d. Connect a voltmeter between the 7D01 Threshold Voltage Monitor jack and ground and set to +2.4 volts.

e. Connect a 1.2-kilohm resistor between the DF RESET OUT jack and ground (Figure 7-4A).

f. Connect the Channel 0 probe tip to the RESET OUT jack.

g. Press the RESET IF 7D01=REF push button and check that the 7D01 resets once and displays a HI pulse on channel 0 of the Timing Diagram.

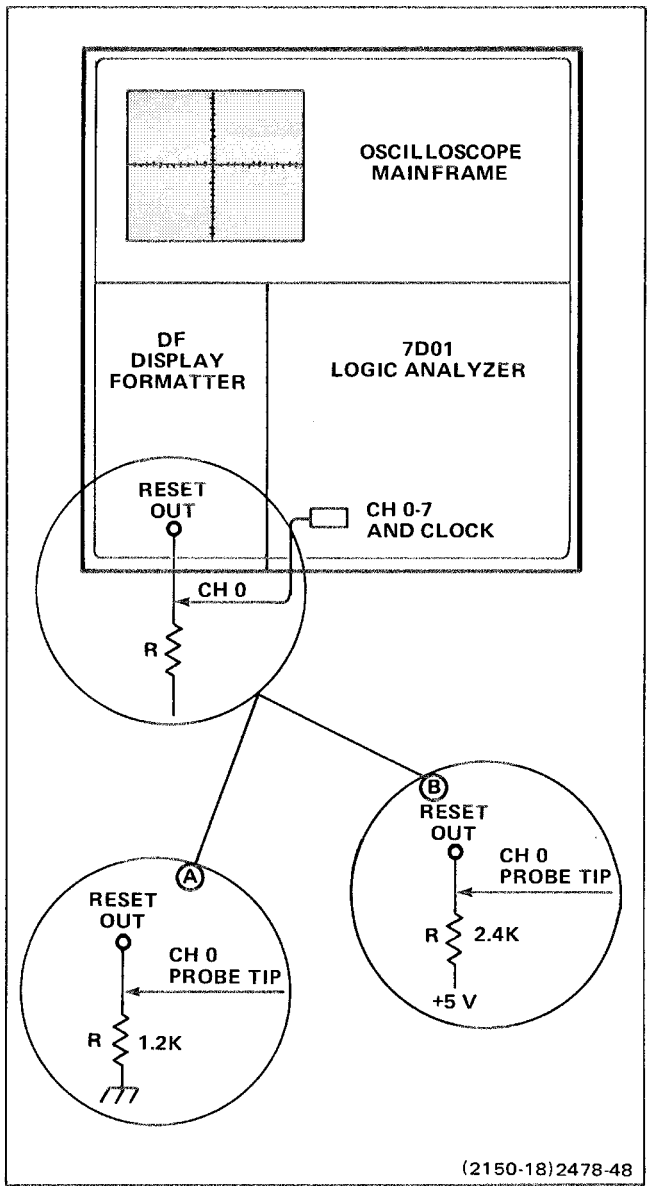


Figure 7-4. Reset Out check test setup.

h. Rotate the 7D01 Cursor position controls to set the cursor intensified dot to the falling edge of the displayed pulse.

i. Check that the trigger-to-cursor readout is at least +50 and less than or equal to +150.

j. Set the 7D01 Threshold Voltage Monitor for +0.4 volts.

k. Disconnect the 1.2-kilohm resistor and Channel 0 probe from the RESET OUT jack.

l. Press the 7D01 Record Manual Reset and Manual Trigger push buttons (in that order).

m. Connect a 2.4-kilohm resistor from a +5-volt supply to the RESET OUT jack (Figure 7-4B).

n. Connect the Channel 0 probe to the RESET OUT jack.

o. Press the RESET IF 7D01=REF push button and check that the 7D01 resets once and displays a HI pulse on channel 0 of the Timing Diagram display.

p. Disconnect the 2.4-kilohm resistor and Channel 0 probe from the RESET OUT jack.

q. Turn off power to the mainframe and remove the 7D01-DF.

r. Disconnect the DF from the 7D01 and set the 7D01 to the Full Display mode (internal jumper).

ADJUSTMENT PROCEDURE

1. Adjust Horizontal Gain

a. Perform the Preliminary Procedure. (Do NOT set 7D01 to First Trigger mode.)

b. Press MAP FAST push button and adjust mainframe intensity control for well-defined Map display (diagonal line).

c. Adjust the front-panel HORIZ POSN screwdriver adjustment to position the left end of the Map display to the left edge of the crt graticule.

d. Note the position of the right end of the Map display relative to the edge of the crt graticule. The right end of the display should be within 0.2 division from the right edge of the graticule.

e. If adjustment of the horizontal gain is required; turn off the power to the mainframe, partially remove the 7D01-DF from the mainframe, and adjust the Horiz Gain screwdriver adjustment (accessible through the top rail of the DF). (Clockwise rotation of the control reduces the horizontal gain.)

f. Check the resultant adjustment by re-inserting the 7D01-DF into the mainframe, applying power, and pressing the MAP FAST push button.

g. Repeat parts e and f as required.

INSTRUMENT OPTIONS

No options were available for this instrument at the time of this printing.

Information on any subsequent options may be found in the CHANGE INFORMATION section in the back of this manual.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00213	NYTRONICS, COMPONENTS GROUP, INC., SUBSIDIARY OF NYTRONICS, INC.	ORANGE STREET	DARLINGTON, SC 29532
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
07910	TELEDYNE SEMICONDUCTOR	12515 CHADRON AVE.	HAWTHORNE, CA 90250
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50579	LITRONIX INC.	19000 HOMESTEAD RD.	CUPERTINO, CA 95014
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-4663-01			CKT BOARD ASSY:KEYBOARD	80009	670-4663-01
A2	670-4664-01			CKT BOARD ASSY:BUTTON LIGHTS	80009	670-4664-01
A3	670-4662-00			CKT BOARD ASSY:INTELLIGENCE	80009	670-4662-00
A4	670-4661-00			CKT BOARD ASSY:ACQUISITION	80009	670-4661-00
A5	670-5506-00			CKT BOARD ASSY:ROM EXTENDER	80009	670-5506-00
C72	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
C73	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C74	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C75	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C76	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C77	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C78	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C79	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C81	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C82	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C83	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C84	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C85	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C86	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C87	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C93	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C95	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
C96	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C97	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C98	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C99	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C187	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C206	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C233	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	72982	8005H9AADW5R472K
C243	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	72982	8005H9AADW5R472K
C254	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	56289	502D225
C257	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C310	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	390049X5P0151K
C311	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	390049X5P0151K
C467	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C468	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	72982	390-049X5P0270M
C470	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C472	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C481	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C492	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C493	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C494	290-0782-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	56289	503D475G035AS
C567	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C568	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	72982	390049X5P0470K
C570	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C572	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C581	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C583	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C604	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	390-049X5P0220K
C605	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	72982	390-049X5P0220K
C624	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
C625	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	72982	8005H9AADW5R471K
C641	285-1076-00			CAP.,FXD,PLSTC:0.2UF,5%,100V	14752	230B1B204J

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C642	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C691	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	72982	390049X5P0680K
C704	281-0791-00	B010100	B010219	CAP.,FXD,CER DI:270PF,10%,100V	80009	281-0791-00
C704	281-0773-00	B010220		CAP.,FXD,CER DI:0.01UF,10%,100V	72982	8005H9AADW5R103K
C705	281-0762-00	B010100	B010219X	CAP.,FXD,CER DI:27PF,20%,100V	72982	390-049X5P0270M
C706	283-0115-00	XB010220		CAP.,FXD,CER DI:47PF,5%,200V	72982	805-509C0G470J
C748	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	390049X5P0151K
C749	281-0786-00			CAP.,FXD,CER DI:150PF,10%,100V	72982	390049X5P0151K
C825	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N147 C 104K
C835	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N147 C 104K
C845	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075 E474M
C855	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N147 C 104K
CR62	152-0107-00			SEMICOND DEVICE:SILICON,400V,400MA	80009	152-0107-00
CR151	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR152	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR254	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR471	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR564	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR565	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR571	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR691	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	07910	1N4152
CR865	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
DS8	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS10	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS12	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS14	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS18	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS20	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS22	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS24	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS26	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS28	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS30	150-1029-00			LAMP,LED:2.0V,GREEN	53184	XC209G
DS34	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS36	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS38	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS40	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS42	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS44	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS46	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS52	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
DS54	150-1036-00			LAMP,LED:RED,3.0V,40MA	50579	RL4484
L73	108-0574-00			COIL,RF:30UH	80009	108-0574-00
L81	108-0574-00			COIL,RF:30UH	80009	108-0574-00
L704	108-0736-00	B010100	B010219X	COIL,RF:825NH	80009	108-0736-00
LR72	108-0184-00			COIL,RF:3.2UH(WOUND ON A 10 OHM RESISTOR)	80009	108-0184-00
LR95	108-0184-00			COIL,RF:3.2UH(WOUND ON A 10 OHM RESISTOR)	80009	108-0184-00
Q8	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q10	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q12	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q14	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q18	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
Q20	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q22	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q24	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q26	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q28	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q30	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q34	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q36	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q38	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q40	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q42	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q44	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q46	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q52	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q54	151-0254-00			TRANSISTOR:SILICON,NPN	80009	151-0254-00
Q141	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q151	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q184	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q188	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q202	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q206	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q234	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q244	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q254	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q258	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q472	151-0460-00			TRANSISTOR:SILICON,NPN	07263	2N3947
Q482	151-0460-00			TRANSISTOR:SILICON,NPN	07263	2N3947
Q482	151-0460-00			TRANSISTOR:SILICON,NPN	07263	2N3947
Q486	151-0459-00			TRANSISTOR:SILICON,PNP	04713	2N3251
Q572	151-0460-00			TRANSISTOR:SILICON,NPN	07263	2N3947
Q582	151-0459-00			TRANSISTOR:SILICON,PNP	04713	2N3251
Q586	151-0459-00			TRANSISTOR:SILICON,PNP	04713	2N3251
Q592	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q594	156-0065-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	80009	156-0065-00
Q752	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q754	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q756	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q760	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q762	151-0223-00			TRANSISTOR:SILICON,NPN	80009	151-0223-00
Q764	151-0220-00			TRANSISTOR:SILICON,PNP	80009	151-0220-00
Q770	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
Q772	151-0223-00			TRANSISTOR:SILICON,NPN	80009	151-0223-00
Q774	151-0220-00			TRANSISTOR:SILICON,PNP	80009	151-0220-00
Q782	151-0342-00			TRANSISTOR:SILICON,PNP	80009	151-0342-00
Q792	151-0435-00			TRANSISTOR:SILICON,PNP	80009	151-0435-00
Q796	151-0435-00			TRANSISTOR:SILICON,PNP	80009	151-0435-00
R8	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R9	307-0489-00			RES,NTWK,FXD,FI:THICK FILM,100 OHM,20%,1W	32997	4408R0011010
R19	307-0489-00			RES,NTWK,FXD,FI:THICK FILM,100 OHM,20%,1W	32997	4408R0011010
R21	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R29	307-0489-00			RES,NTWK,FXD,FI:THICK FILM,100 OHM,20%,1W	32997	4408R0011010
R30	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R39	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R40	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R62	303-0360-00			RES.,FXD,CMPSN:36 OHM,5%,1W	01121	GB3605
R65	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R66	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R67	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R68	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R141	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R142	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R150	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
R151	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
R152	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
R156	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R184	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R187	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
R188	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
R201	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R202	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R203	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
R204	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
R205	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
R206	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R232	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R233	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R234	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R235	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R242	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R243	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R244	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
R245	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R251	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R252	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R254	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
R255	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R256	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R257	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R258	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R259	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R262	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
R263	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R284	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R310	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
R311	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
R463	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
R467	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
R469	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
R470	311-1248-00			RES.,VAR,NONWIR:500 OHM,10%,0.50W	73138	72X-23-0-501K
R471	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
R472	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	01121	CB1635
R475	311-1228-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	32997	3386F-T04-103
R480	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R481	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R482	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R483	323-0195-00			RES.,FXD,FILM:1.05K OHM,1%,0.50W	75042	CECTO-1051F
R484	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	MFF1816G130R0F
R485	321-0155-00			RES.,FXD,FILM:402 OHM,1%,0.125W	91637	MFF1816G402R0F
R486	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R491	321-0270-00			RES.,FXD,FILM:6.34K OHM,1%,0.125W	91637	MFF1816G63400F
R492	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
R494	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
R495	315-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.25W	01121	CB3005
R502	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R503	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R505	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
R506	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R508	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
R562	315-0124-00			RES.,FXD,CMPSN:120K OHM,5%,0.25W	01121	CB1245
R563	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
R564	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R565	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
R566	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
R567	315-0200-00			RES.,FXD,CMPSN:20 OHM,5%,0.25W	01121	CB2005
R569	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
R570	311-1225-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	32997	3386F-T04-102
R571	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
R572	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
R575	311-1228-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	32997	3386F-T04-103
R580	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R581	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R582	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
R583	323-0195-00			RES.,FXD,FILM:1.05K OHM,1%,0.50W	75042	CECTO-1051F
R584	321-0108-00			RES.,FXD,FILM:130 OHM,1%,0.125W	91637	MFF1816G130R0F
R585	321-0155-00			RES.,FXD,FILM:402 OHM,1%,0.125W	91637	MFF1816G402R0F
R586	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
R590	315-0113-00			RES.,FXD,CMPSN:11K OHM,5%,0.25W	01121	CB1135
R591	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R592	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R594	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	01121	CB3615
R595	315-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.25W	01121	CB3005
R604	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
R605	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
R624	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
R625	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
R641	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
R642	321-0352-00			RES.,FXD,FILM:45.3K OHM,1%,0.125W	91637	MFF1816G45301F
R691	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R692	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R704	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R705	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R736	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
R737	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R748	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R749	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	01121	CB3625
R751	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
R752	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R753	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R754	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R755	311-1231-00			RES.,VAR,NONWIR:25K OHM,20%,0.50W	32997	3386F-T04-253
R756	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
R757	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
R760	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R761	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R762	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R763	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R764	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
R770	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R771	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R772	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R773	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
R774	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
R781	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
R782	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
R790	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
R791	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
R792	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
R810	308-0402-00			RES.,FXD,WW:30 OHM,5%,5W	00213	1250S-30R00J
S8	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S10	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S12	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S14	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S18	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S20	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S22	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S24	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S26	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S28	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S34	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S36	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S38	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S40	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S42	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S44	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S46	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S48	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S52	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S54	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
S58	263-0019-00			ACTR ASSY,PB:	80009	263-0019-00
U8	156-0572-00			MICROCIRCUIT,DI:8 BIT SERIAL IN-PRL OUT	80009	156-0572-00
U26	156-0572-00			MICROCIRCUIT,DI:8 BIT SERIAL IN-PRL OUT	80009	156-0572-00
U42	156-0572-00			MICROCIRCUIT,DI:8 BIT SERIAL IN-PRL OUT	80009	156-0572-00
U65	156-0572-00			MICROCIRCUIT,DI:8 BIT SERIAL IN-PRL OUT	80009	156-0572-00
U102	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U110	156-0503-00			MICROCIRCUIT,DI:HEX INVERTER BUFFER	80009	156-0503-00
U132	156-0625-00			MICROCIRCUIT,DI:8 BIT PRL LOAD SHIFT RGTR	80009	156-0625-00
U138	156-0625-00			MICROCIRCUIT,DI:8 BIT PRL LOAD SHIFT RGTR	80009	156-0625-00
U152	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U156	156-0349-01			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0349-01
U158	156-0366-00			MICROCIRCUIT,LI:DUAL D-TYPE F-F	80009	156-0366-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U162	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U172	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U182	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U216	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U217	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U218	156-0171-00			MICROCIRCUIT,DI:QUAD 2-INPUT OR GATE	01295	SN7432N
U222	156-0403-00			MICROCIRCUIT,DI:HEX. INV W/OPEN COLL OUTPS	01295	SN74S05N
U264	156-0426-00			MICROCIRCUIT,DI:MICROPROCESSOR 6800	04713	MC6800L
U268	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U274	156-0716-00			MICROCIRCUIT,DI:128 X 8 BIT STATIC RAM	04713	6810A
U284	156-0899-00			MICROCIRCUIT,DI:2048 X 8 ROM,CUSTOM MASK	80009	156-0889-00
U294	156-0900-00			MICROCIRCUIT,DI:2048 X 8 ROM,CUSTOM MASK	80009	156-0900-00
U304	156-0649-00			MICROCIRCUIT,DI:3 STATE HEX. NON INVT BFR	80009	156-0649-00
U308	156-0649-00			MICROCIRCUIT,DI:3 STATE HEX. NON INVT BFR	80009	156-0649-00
U310	156-0733-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	27014	DM74LS221N
U314	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U316	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U318	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U320	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U334	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U336	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U338	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U340	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U354	156-0649-00			MICROCIRCUIT,DI:3 STATE HEX. NON INVT BFR	80009	156-0649-00
U402	156-0741-00			MICROCIRCUIT,DI:4-BIT BINARY COUNTER	80009	156-0741-00
U404	156-0387-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG	01295	SN74LS73N
U409	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U412	156-0656-00			MICROCIRCUIT,DI:DECADE COUNTER	80009	156-0656-00
U415	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U417	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U422	156-0785-09			MICROCIRCUIT,DI:PROM U522 PROGRAMMED	80009	156-0785-09
U432	156-0679-00			MICROCIRCUIT,DI:4-BIT BINARY FULL ADDER	01295	SN74LS283N
U434	156-0679-00			MICROCIRCUIT,DI:4-BIT BINARY FULL ADDER	01295	SN74LS283N
U452	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U454	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U462	156-0530-00			MICROCIRCUIT,DI:SEL/MULTIPLEXE,16 PIN DIP	80009	156-0530-00
U464	156-0530-00			MICROCIRCUIT,DI:SEL/MULTIPLEXE,16 PIN DIP	80009	156-0530-00
U468	156-0509-00			MICROCIRCUIT,LI:8 BIT BIN,MULT,CURRENT OUTPUT	04713	SC20803LH
U492	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	80009	156-0067-00
U502	156-0741-00			MICROCIRCUIT,DI:4-BIT BINARY COUNTER	80009	156-0741-00
U503	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	01295	SN74LS20N
U504	156-0741-00			MICROCIRCUIT,DI:4-BIT BINARY COUNTER	80009	156-0741-00
U522	156-0785-08			MICROCIRCUIT,DI:PROM U422 PROGRAMMED	80009	156-0785-08
U532	156-0679-00			MICROCIRCUIT,DI:4-BIT BINARY FULL ADDER	01295	SN74LS283N
U534	156-0679-00			MICROCIRCUIT,DI:4-BIT BINARY FULL ADDER	01295	SN74LS283N
U552	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U554	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U562	156-0530-00			MICROCIRCUIT,DI:SEL/MULTIPLEXE,16 PIN DIP	80009	156-0530-00
U564	156-0530-00			MICROCIRCUIT,DI:SEL/MULTIPLEXE,16 PIN DIP	80009	156-0530-00
U568	156-0509-00			MICROCIRCUIT,LI:8 BIT BIN,MULT,CURRENT OUTPUT	04713	SC20803LH
U604	156-0733-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	27014	DM74LS221N
U614	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U624	156-0733-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	27014	DM74LS221N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U632	156-0412-00			MICROCIRCUIT,DI:4-BIT BIN UP/DOWN COUNTER	01295	SN74LS193N
U634	156-0412-00			MICROCIRCUIT,DI:4-BIT BIN UP/DOWN COUNTER	01295	SN74LS193N
U636	156-0412-00			MICROCIRCUIT,DI:4-BIT BIN UP/DOWN COUNTER	01295	SN74LS193N
U638	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U640	156-0402-00			MICROCIRCUIT,DI:TIMER	18324	NE555V
U641	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U642	156-0547-00			MICROCIRCUIT,DI:QUAD TOW-INPUT MULTIPLEXER	80009	156-0547-00
U644	156-0547-00			MICROCIRCUIT,DI:QUAD TOW-INPUT MULTIPLEXER	80009	156-0547-00
U646	156-0547-00			MICROCIRCUIT,DI:QUAD TOW-INPUT MULTIPLEXER	80009	156-0547-00
U648	156-0387-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG	01295	SN74LS73N
U652	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U654	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U656	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U658	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U662	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U664	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U666	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U668	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC ROM	34649	2102
U674	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U676	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U684	156-0882-00			MICROCIRCUIT,DI:ROM CHAR GEN	80009	156-0882-00
U694	156-0073-00			MICROCIRCUIT,DI:SGL 10MHZ SHIFT REG	01295	SN7496N
U704	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U714	156-0388-00			MICROCIRCUIT,DI:DUAL D-TYPE FLIP-FLOP	01295	SN74LS74N
U724	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U735	156-0574-00			MICROCIRCUIT,DI:TRI-STATE QUAD D F-F	80009	156-0574-00
U738	156-0387-00			MICROCIRCUIT,DI:DUAL J-K NEG EDGE TRIG	01295	SN74LS73N
U746	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U748	156-0733-00			MICROCIRCUIT,DI:DUAL MONOSTABLE MV	27014	DM74LS221N
U752	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U756	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U810	156-0277-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM340T-5
U820	156-1132-00			MICROCIRCUIT,DI:2048 X 8 ROM,CUSTOM MASK	80009	156-1132-00
U860	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
VR62	152-0481-00			SEMICOND DEVICE:ZENER,1W,5.1V,5%	04713	1N3826A
Y704	158-0056-00			XTAL UNIT,QTZ:4 MHZ,0.003%,SERIES RESN	80009	158-0056-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it goes to the low state.

Abbreviations are based on ANSI Y1.1-1972.

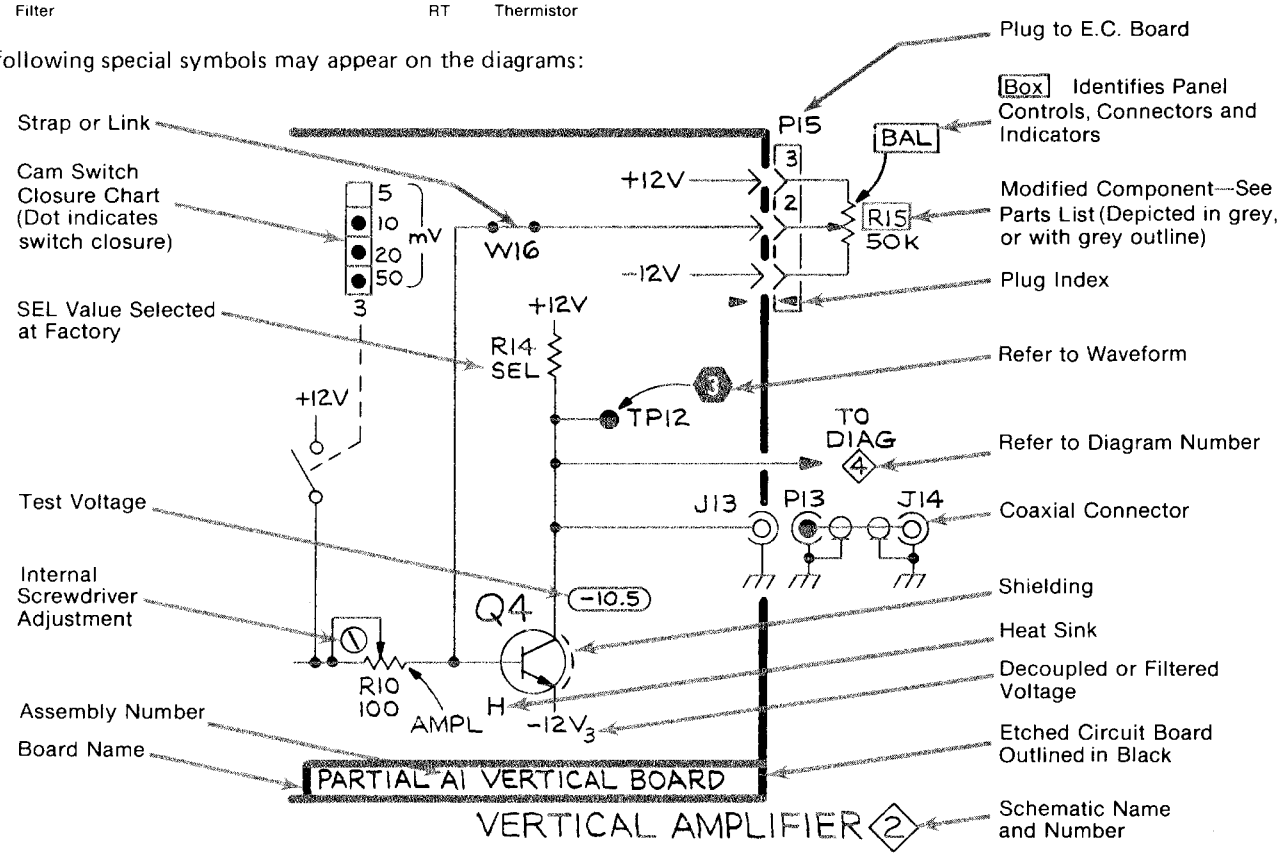
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)	H	Heat dissipating device (heat sink, heat radiator, etc)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



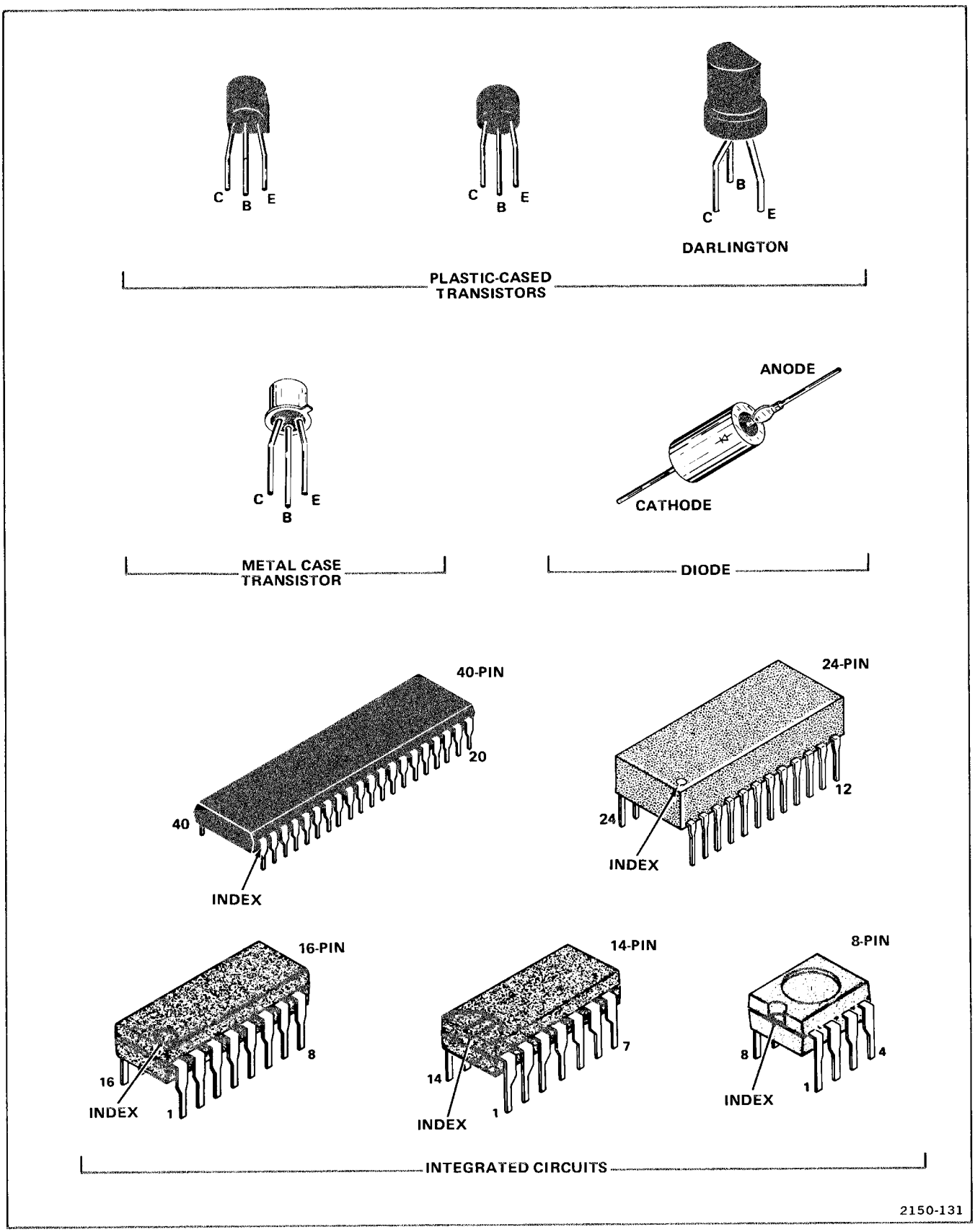
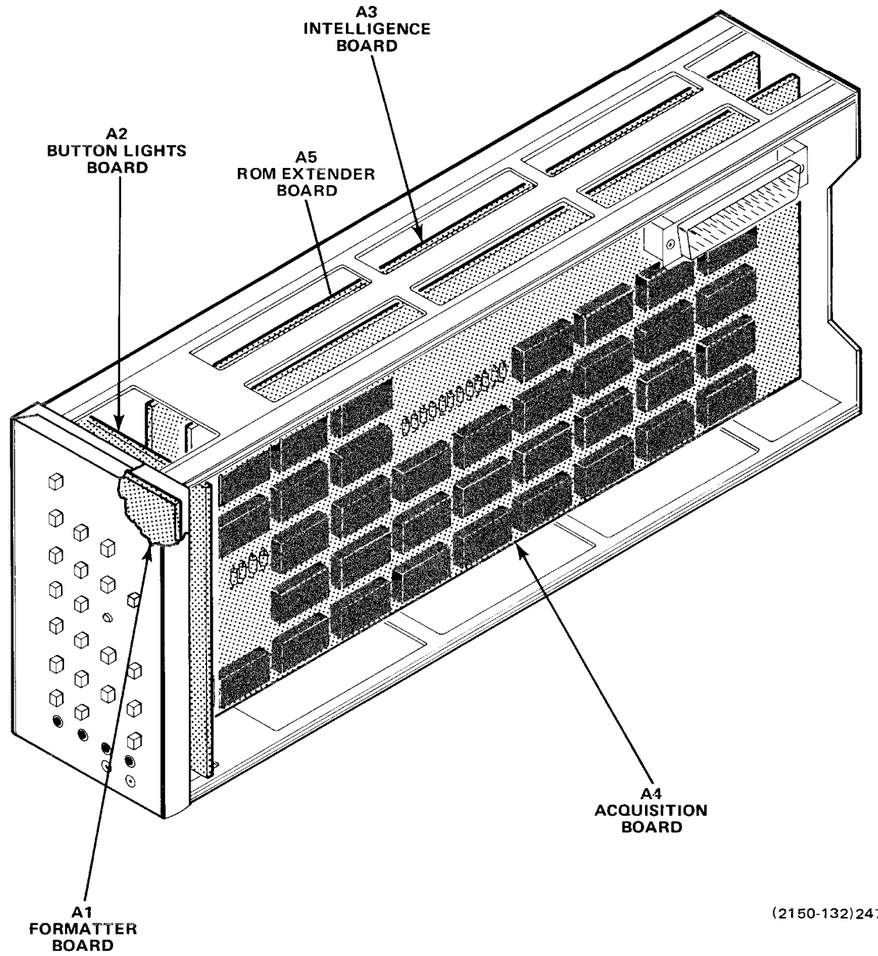


Figure 10-1. Semiconductor lead configurations.

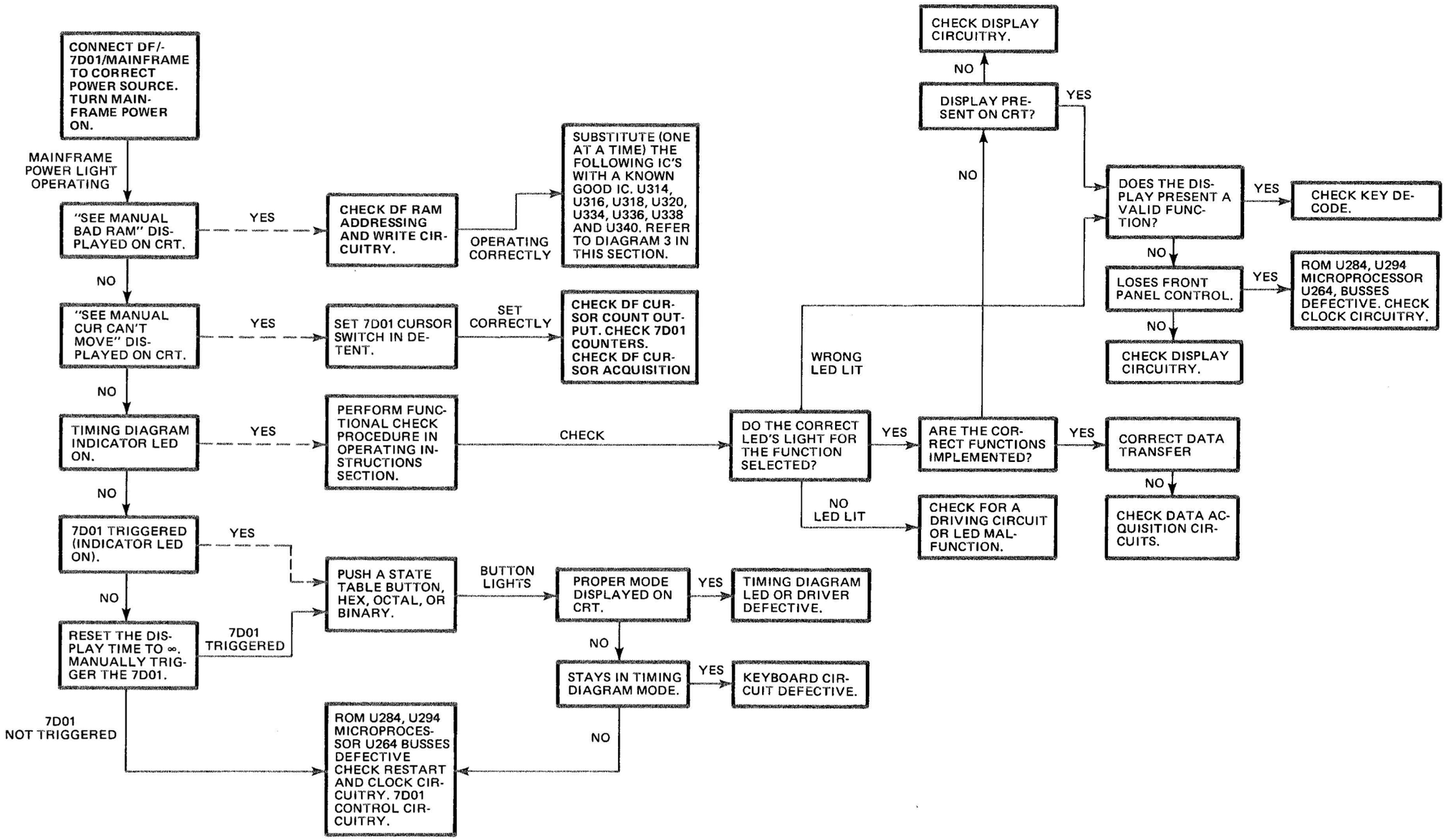


(2150-132)2478-16

@

Figure 10-2. Circuit board locations.

DF2 TROUBLESHOOTING CHART



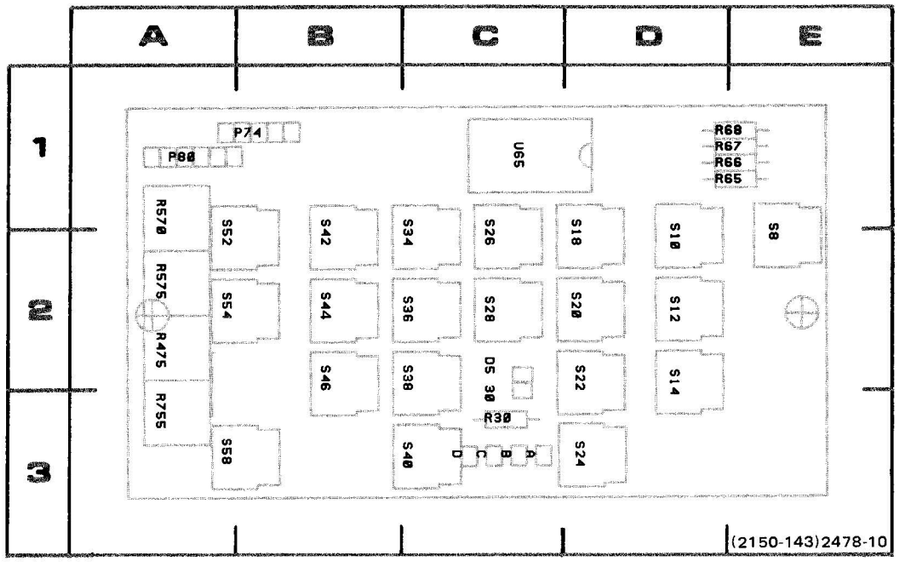
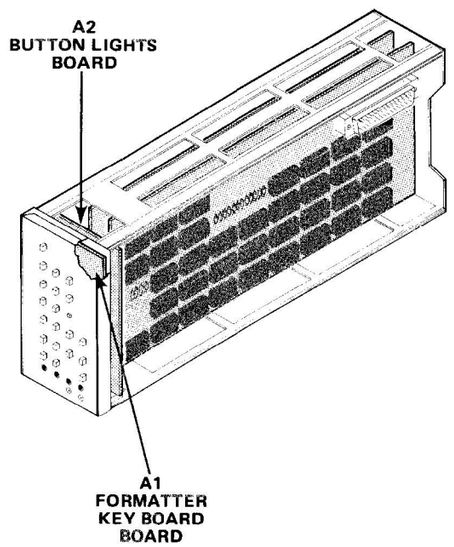


Figure 10-3. A1—Formatter Keyboard circuit board locations as viewed from front of instrument.

CKT NO	GRID COORD	CKT NO	GRID COORD
DS30	2C	S18	2D
P74	1B	S20	2D
P80	1A	S22	2D
		S24	3D
R30	3C	S26	2C
R65	1D	S28	2C
R66	1D	S34	2C
R67	1D	S36	2C
R68	1D	S38	2C
R475	2A	S40	3C
R570	1A	S42	2B
R575	2A	S44	2B
R755	3A	S46	2B
		S48	2B
S8	2E	S52	2A
S10	2D	S54	2A
S12	2D	S58	3A
S14	2D	U65	1C



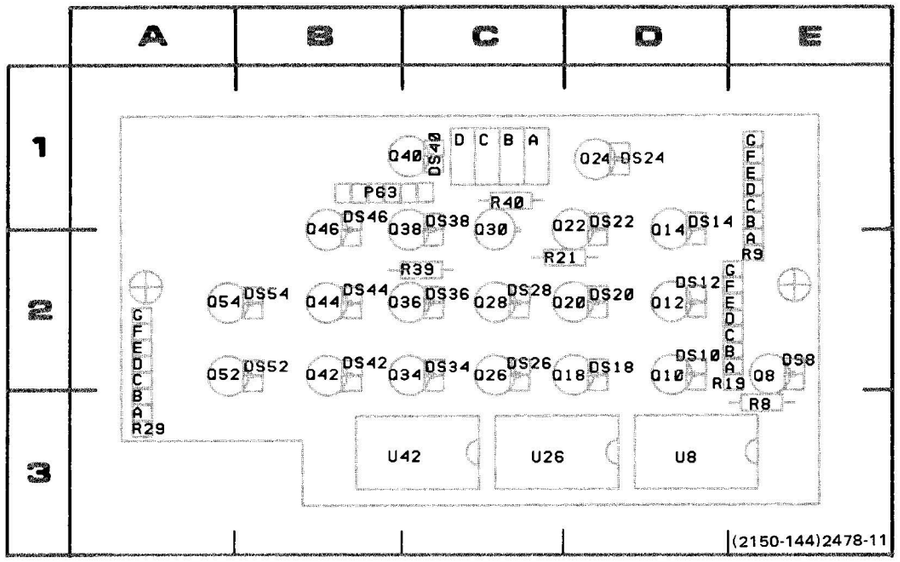
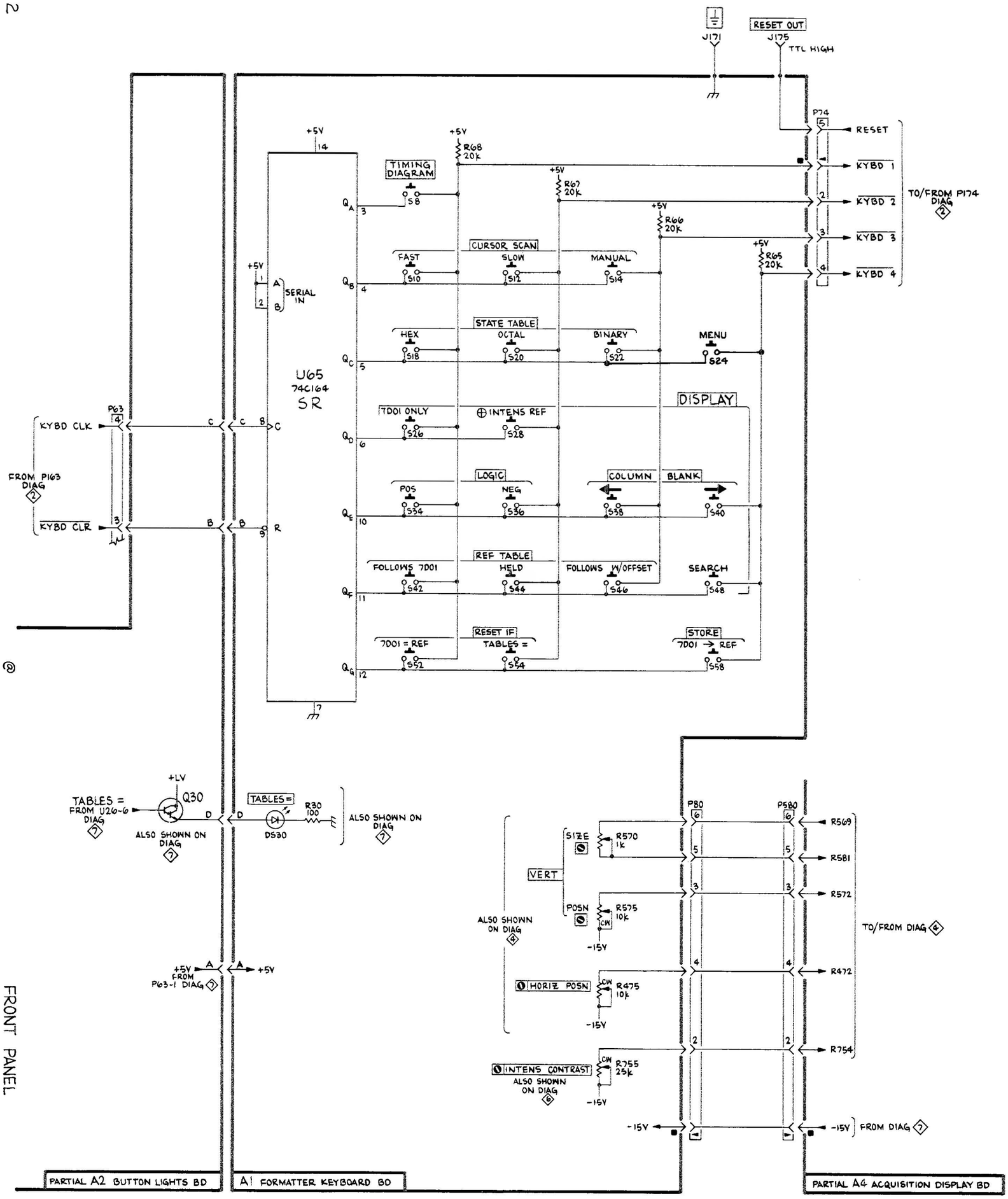


Figure 10-4. A2—Button Lights circuit board component locations as viewed from the component side of the board.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
DS8	2E	P63	1B	Q46	1B
DS10	2D	Q8	2E	Q52	2A
DS12	2D	Q10	2D	Q54	2A
DS14	1D	Q12	2D		
DS18	2D	Q14	1D	R8	3E
DS20	2D	Q18	2C	R9	2E
DS22	1D	Q20	2C	R19	2E
DS24	1D	Q22	1D	R21	2C
DS26	2C	Q24	1D	R29	3A
DS28	2C	Q26	2C	R39	2C
DS34	2C	Q28	2C	R40	1C
DS36	2C	Q30	1C		
DS38	1C	Q34	2B	U8	3D
DS40	1C	Q36	2B	U26	3C
DS42	2B	Q38	1B	U42	3C
DS44	2B	Q40	1C		
DS46	1B	Q42	2B		
DS52	2B	Q44	2B		
DS54	2B				

DF 2



FRONT PANEL

1 B1 P2 L.I.C.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

1 FRONT PANEL

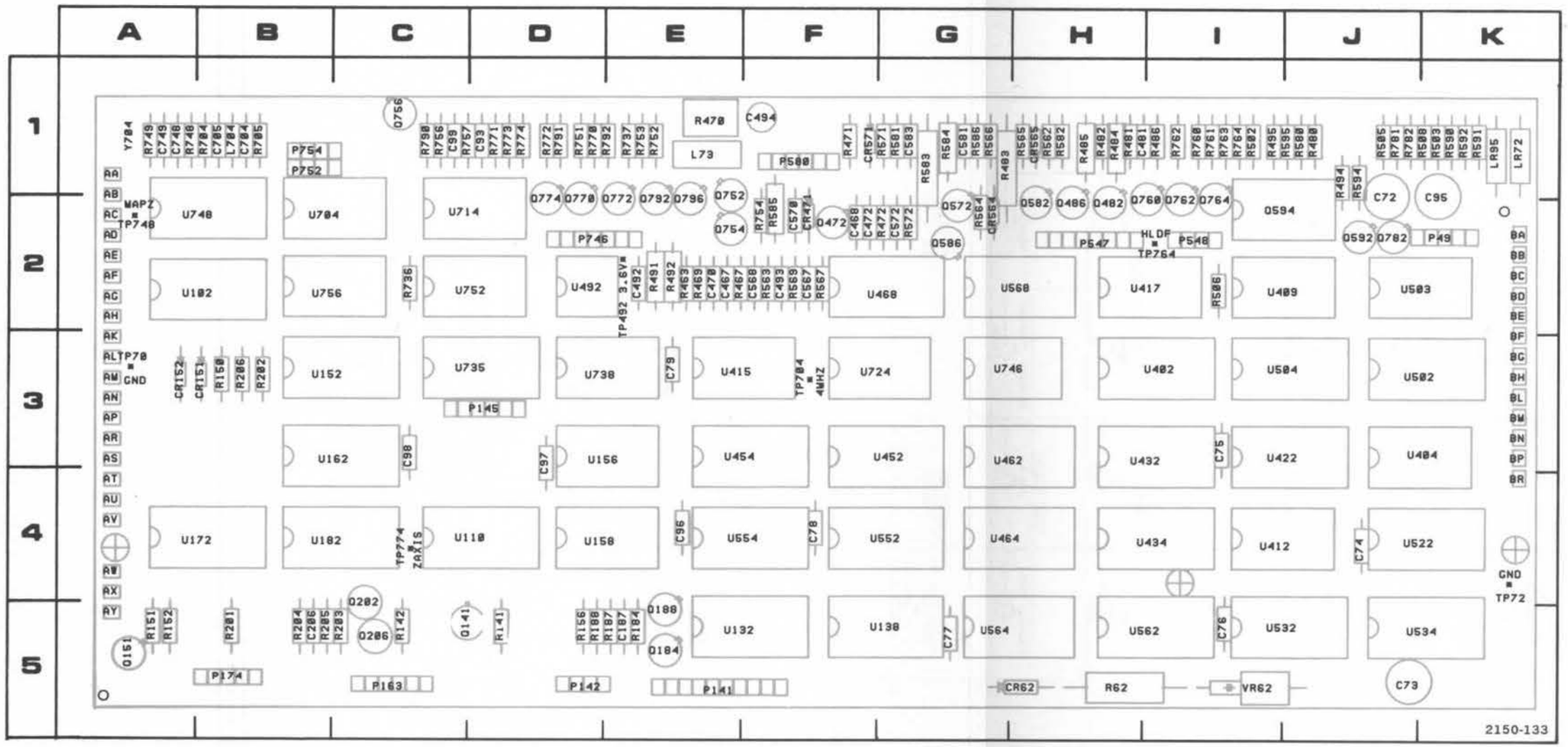
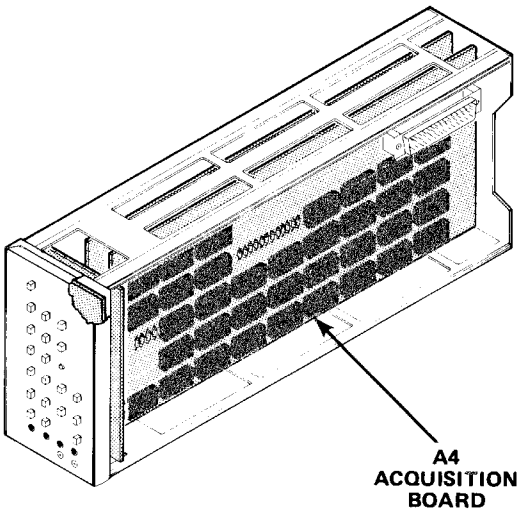
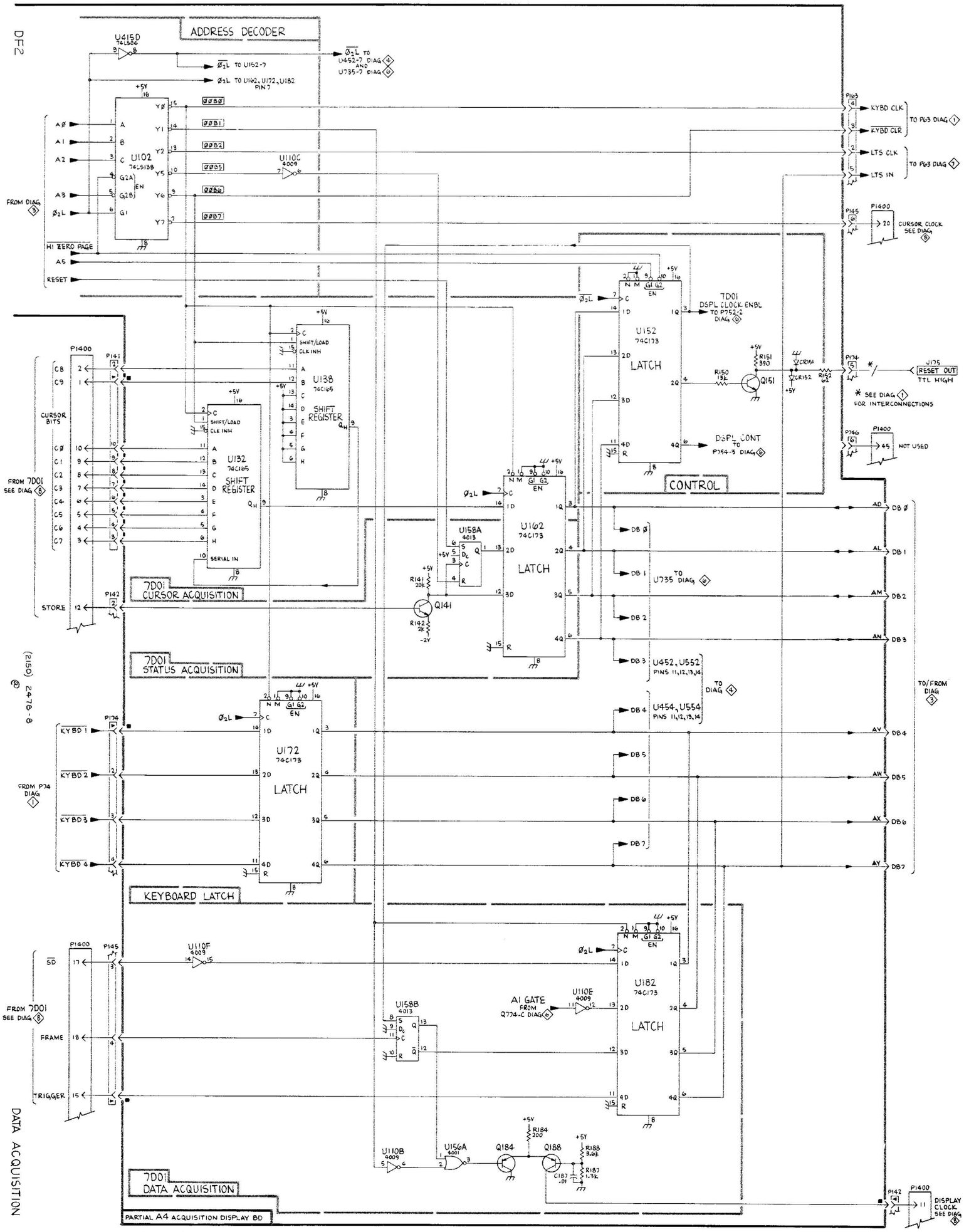


Figure 10-5. A4—Acquisition circuit board component locations.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
C72	1J	Q141	5C	R503	1K	U110	4C
C73	5J	Q151	5A	R505	1J	U132	5E
C74	4J	Q184	5E	R506	2I	U138	5G
C75	3I	Q188	5E	R508	1K	U152	3B
C76	5I	Q202	5C	R562	1H	U156	3D
C77	5G	Q206	5C	R563	2F	U158	4D
C78	4F	Q472	2F	R564	2G	U162	3B
C79	3E	Q482	2H	R565	1H	U172	4A
C93	1D	Q486	2H	R566	1G	U182	4B
C95	1K	Q572	2G	R567	2F	U402	3I
C96	4E	Q582	2H	R569	2F	U404	3K
C97	3D	Q586	2G	R571	1G	U409	2I
C98	3C	Q592	2I	R572	2G	U412	4I
C99	1C	Q594	2I	R580	1J	U415	3E
C187	5E	Q752	1E	R581	1G	U417	2I
C206	5B	Q754	2E	R582	1H	U422	3I
C467	2E	Q756	1C	R583	1G	U432	3I
C468	2F	Q760	2I	R584	1G	U434	4I
C470	2E	Q762	2I	R585	2F	U452	3E
C472	2F	Q764	2I	R586	1G	U454	3E
C481	1H	Q770	2D	R590	1K	U462	3G
C492	2E	Q772	2E	R591	1K	U464	4H
C493	2F	Q774	2D	R592	1K	U468	2F
C494	1F	Q782	2I	R594	1J	U492	2D
C567	2F	Q792	2E	R595	1J	U502	3K
C568	2F	Q796	2E	R704	1B	U503	2I
C570	2F			R705	1B	U504	3I
C572	2G	R62	5H	R736	2C	U522	4K
C581	1G	R141	5D	R737	1E	U532	5I
C583	1G	R142	5C	R748	1A	U534	5J
C704	1B	R150	3B	R749	1A	U552	4G
C705	1B	R151	5A	R751	1D	U554	4E
C748	1A	R152	5A	R752	1E	U562	5I
C749	1A	R156	5D	R753	1E	U564	5G
		R184	5E	R754	2F	U568	2H
CR62	5H	R187	5E	R756	1C	U704	2B
CR151	3B	R188	5D	R757	1C	U714	2C
CR152	3A	R201	5B	R760	1I	U724	3E
CR471	2F	R202	3B	R761	1I	U735	3D
CR564	2G	R203	5C	R762	1I	U738	3D
CR565	1H	R204	5B	R763	1I	U746	3G
CR571	1F	R205	5B	R764	1I	U748	2B
		R206	3B	R770	1D	U752	2C
L73	1E	R463	2E	R771	1D	U756	2B
L704	1B	R467	2E	R772	1D		
		R469	2E	R773	1D	VR62	5I
LR72	1K	R470	1E	R774	1D		
LR95	1K	R471	1F	R781	1J	Y704	1A
		R472	2F	R790	1C		
P49	2K	R480	1J	R791	1D		
P141	5E	R481	1H	R792	1E		
P142	5D	R482	1H				
P145	3D	R483	1G	TP70	3A		
P163	5C	R484	1H	TP72	4K		
P174	5B	R485	1H	TP492	2E		
P547	2H	R486	1I	TP704	3E		
P548	2I	R491	2E	TP748	2A		
P580	1F	R492	2E	TP764	2I		
P746	2D	R494	1J	TP774	4C		
P752	1B	R495	1I				
P754	1B	R502	1I	U102	2B		


A4
ACQUISITION
BOARD



TYPE	Vcc (+5V)	GND
74LS04	14	7
4001	14	7
4009	14	7
4013	14	7

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

L.I.C. P1 P2

2

DATA ACQUISITION

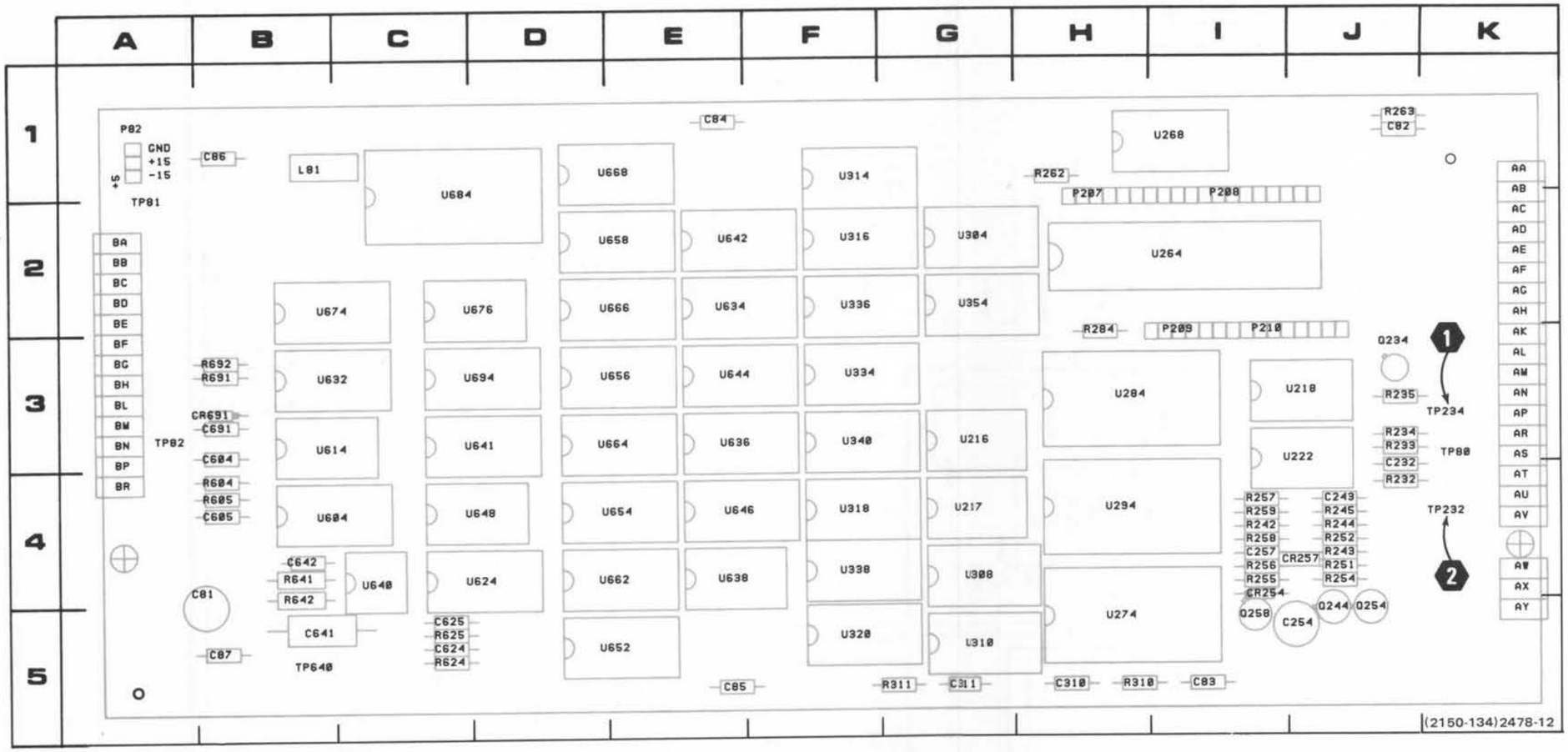


Figure 10-6. A2—Intelligence circuit board component locations.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
C81	4B	R311	5G	U666	2E
C82	1J	R604	4B	U668	1E
C83	5I	R605	4B	U674	2B
C84	1E	R624	5C	U676	2D
C85	5E	R625	5C	U684	1C
C86	1B	R641	4B	U694	3D
C87	5B	R642	4B		
C232	3J	R691	3B	VR687	2B
C243	4J	R692	3B		
C254	5J				
C257*	4I	TP80	3K		
C310	5H	TP81	1A		
C311	5G	TP82	3A		
C604	3B	TP232	4K		
C605	4B	TP234	3K		
C624	5C	TP640	5B		
C625	5C				
C641	5B	U216	3G		
C642	4B	U217	4G		
C691	3B	U218	3J		
		U222	3J		
CR254	4I	U264	2I		
CR257*	4J	U268	1I		
CR691	3B	U274	5H		
		U284	3H		
L81	1B	U294	4H		
		U304	2G		
P207	1H	U308	4G		
P208	1I	U310	5G		
P209	3I	U314	1F		
P210	3I	U316	2F		
		U318	4F		
Q234	3J	U320	5F		
Q244	5J	U334	3F		
Q254	5J	U336	2F		
Q258	5I	U338	4F		
		U340	3F		
R232	4J	U354	2G		
R233	3J	U604	4C		
R234	3J	U614	3C		
R235	3J	U624	4D		
R242	4I	U632	3C		
R243	4J	U634	2E		
R244	4J	U636	3E		
R245	4J	U638	4E		
R251	4J	U640	4C		
R252	4J	U641	3D		
R254	4J	U642	2E		
R255	4I	U644	3E		
R256	4I	U646	4E		
R257	4I	U648	4D		
R258	4I	U652	5E		
R259	4I	U654	4E		
R262	1H	U656	3E		
R263	1J	U658	2E		
R284	3H	U662	4E		
R310	5H	U664	3E		

*See Parts List for serial number ranges.

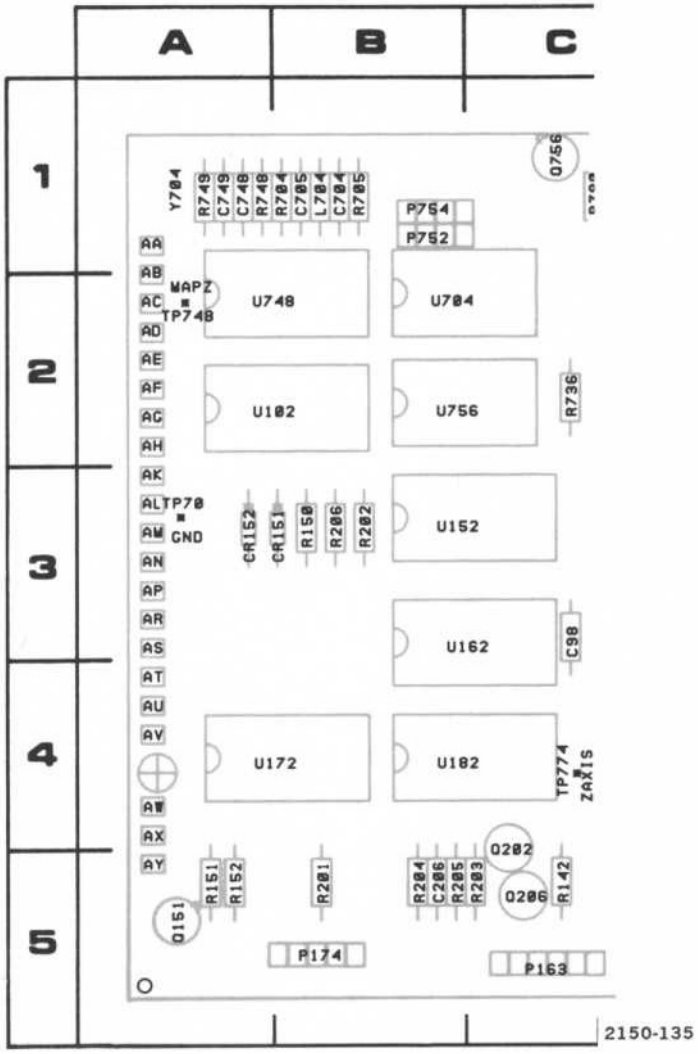
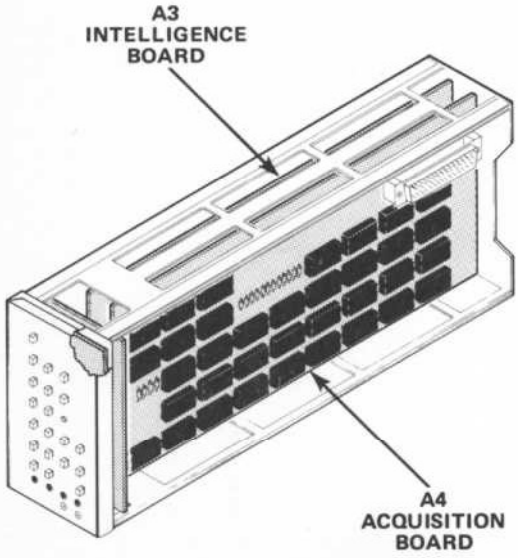


Figure 10-7. Partial A4—Acquisition circuit board. Component locations as viewed from component side of the board.

CKT NO	GRID COORD	CKT NO	GRID COORD
C206	5B	R203	5C
		R204	5B
Q202	5C	R205	5B
Q206	5C	R206	3B
R201	5B	U102	2B
R202	3B	U152	3B



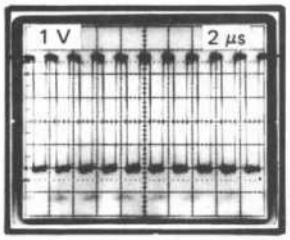
VOLTAGE AND WAVEFORM CONDITIONS

Voltages and waveforms shown are typical, but may vary between instruments.

TEST SETUP: The 7D01 is connected to the 7000-series mainframe Right-Vertical and A-Horizontal compartments through two 067-0616-00 Flexible Plug-in Extenders. The DF is connected to the 7D01 through a 067-0805-00 Cable Extender. The DF is set for a STATE TABLE BINARY, 7D01 ONLY display.

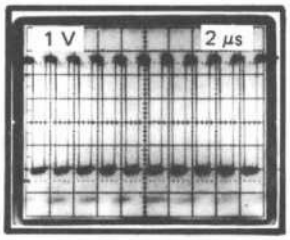
The test oscilloscope is dc coupled and internally triggered.

1



2 V

2



2 V

DF2

MICRO PROCESSOR

PARTIAL A3 INTELLIGENCE BD

PARTIAL A4 ACQUISITION BD

MAIN ADDRESS DECODER

MICRO PROCESSOR U264 6800

PROGRAM ROM

U284

U294

VOLTAGE & WAVEFORM CONDITIONS

PARTIAL A4 ACQUISITION DISPLAY BD

SCRATCH-PAD RAM

DATA STORAGE RAM

RAM

BUS DRIVER

SEE PARTS LIST FOR SEMICONDUCTOR TYPES.

TYPE	Vcc (+5V)	GND
74LS00	14	7
74LS04	14	7
7405	14	7
7432	14	7
74LS125	16	8

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

MPU, PROGRAM, AND DATA STORAGE

(2150) 2478-7
REV A, AUG 1978

MPU, PROGRAM, AND DATA STORAGE

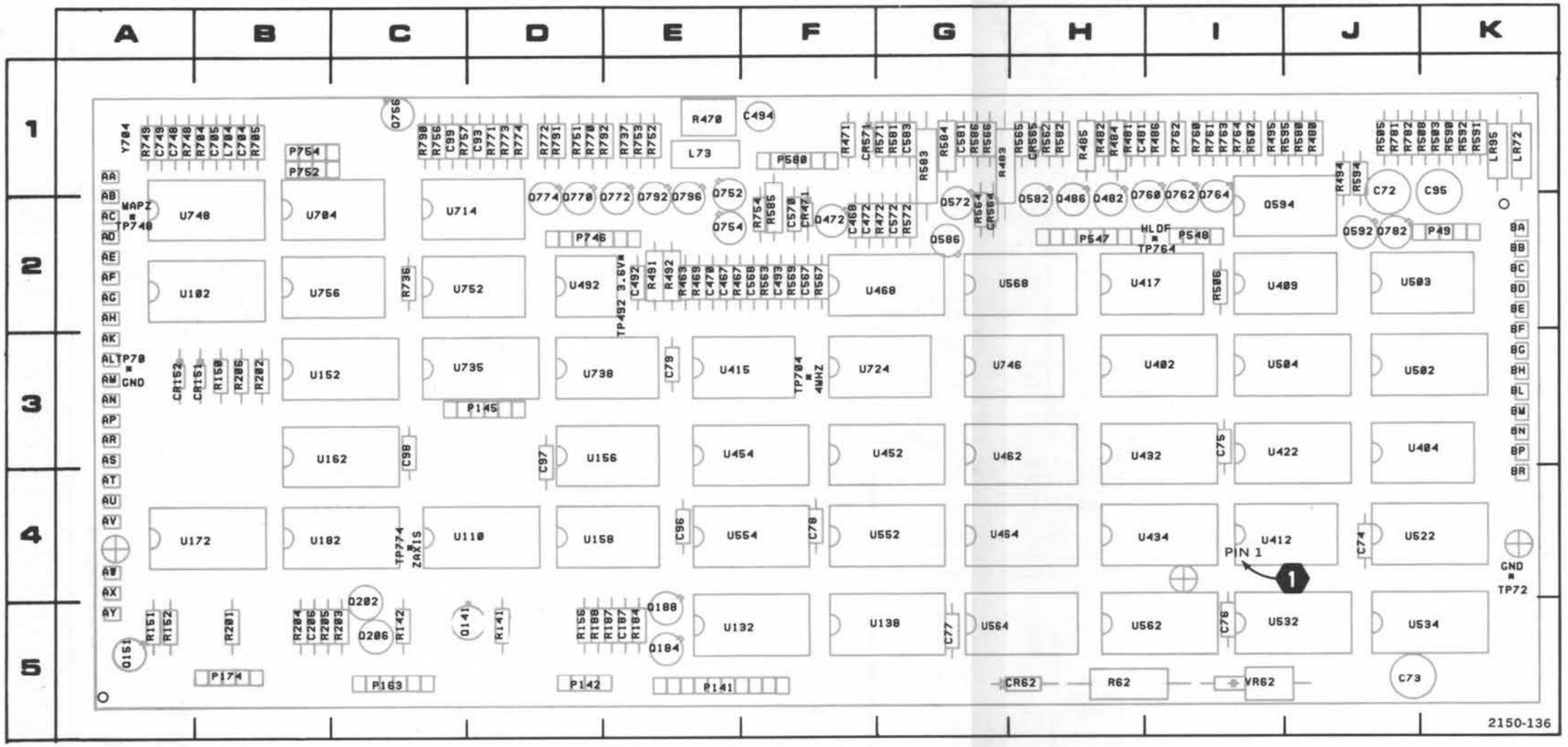
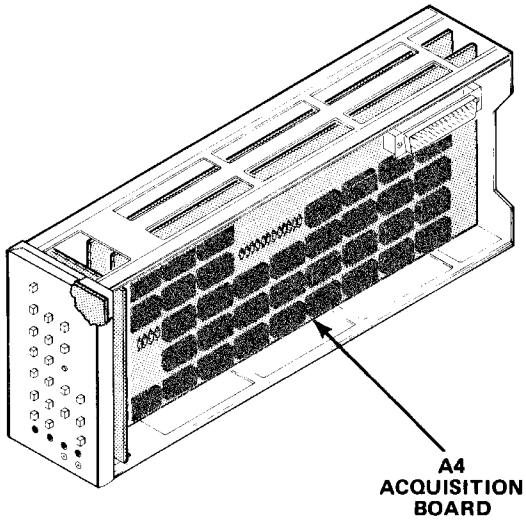


Figure 10-8. A4—Acquisition circuit board component locations.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
C72	1J	Q141	5C	R503	1K	U110	4C
C73	5J	Q151	5A	R505	1J	U132	5E
C74	4J	Q184	5E	R506	2I	U138	5G
C75	3I	Q188	5E	R508	1K	U152	3B
C76	5I	Q202	5C	R562	1H	U156	3D
C77	5G	Q206	5C	R563	2F	U158	4D
C78	4F	Q472	2F	R564	2G	U162	3B
C79	3E	Q482	2H	R565	1H	U172	4A
C93	1D	Q486	2H	R566	1G	U182	4B
C95	1K	Q572	2G	R567	2F	U402	3I
C96	4E	Q582	2H	R569	2F	U404	3K
C97	3D	Q586	2G	R571	1G	U409	2I
C98	3C	Q592	2I	R572	2G	U412	4I
C99	1C	Q594	2I	R580	1J	U415	3E
C187	5E	Q752	1E	R581	1G	U417	2I
C206	5B	Q754	2E	R582	1H	U422	3I
C467	2E	Q756	1C	R583	1G	U432	3I
C468	2F	Q760	2I	R584	1G	U434	4I
C470	2E	Q762	2I	R585	2F	U452	3E
C472	2F	Q764	2I	R586	1G	U454	3E
C481	1H	Q770	2D	R590	1K	U462	3G
C492	2E	Q772	2E	R591	1K	U464	4H
C493	2F	Q774	2D	R592	1K	U468	2F
C494	1F	Q782	2I	R594	1J	U492	2D
C567	2F	Q792	2E	R595	1J	U502	3K
C568	2F	Q796	2E	R704	1B	U503	2I
C570	2F			R705	1B	U504	3I
C572	2G	R62	5H	R736	2C	U522	4K
C581	1G	R141	5D	R737	1E	U532	5I
C583	1G	R142	5C	R748	1A	U534	5J
C704	1B	R150	3B	R749	1A	U552	4G
C705	1B	R151	5A	R751	1D	U554	4E
C748	1A	R152	5A	R752	1E	U562	5I
C749	1A	R156	5D	R753	1E	U564	5G
		R184	5E	R754	2F	U568	2H
CR62	5H	R187	5E	R756	1C	U704	2B
CR151	3B	R188	5D	R757	1C	U714	2C
CR152	3A	R201	5B	R760	1I	U724	3E
CR471	2F	R202	3B	R761	1I	U735	3D
CR564	2G	R203	5C	R762	1I	U738	3D
CR565	1H	R204	5B	R763	1I	U746	3G
CR571	1F	R205	5B	R764	1I	U748	2B
		R206	3B	R770	1D	U752	2C
L73	1E	R463	2E	R771	1D	U756	2B
L704	1B	R467	2E	R772	1D		
		R469	2E	R773	1D	VR62	5I
LR72	1K	R470	1E	R774	1D		
LR95	1K	R471	1F	R781	1J	Y704	1A
		R472	2F	R790	1C		
P49	2K	R480	1J	R791	1D		
P141	5E	R481	1H	R792	1E		
P142	5D	R482	1H				
P145	3D	R483	1G	TP70	3A		
P163	5C	R484	1H	TP72	4K		
P174	5B	R485	1H	TP492	2E		
P547	2H	R486	1I	TP704	3E		
P548	2I	R491	2E	TP748	2A		
P580	1F	R492	2E	TP764	2I		
P746	2D	R494	1J	TP774	4C		
P752	1B	R495	1I				
P754	1B	R502	1I	U102	2B		

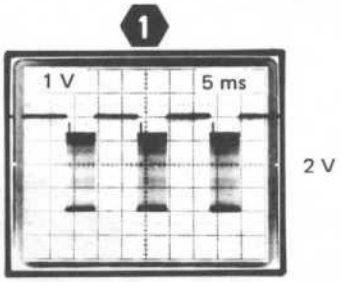

A4
ACQUISITION
BOARD

VOLTAGE AND WAVEFORM CONDITIONS

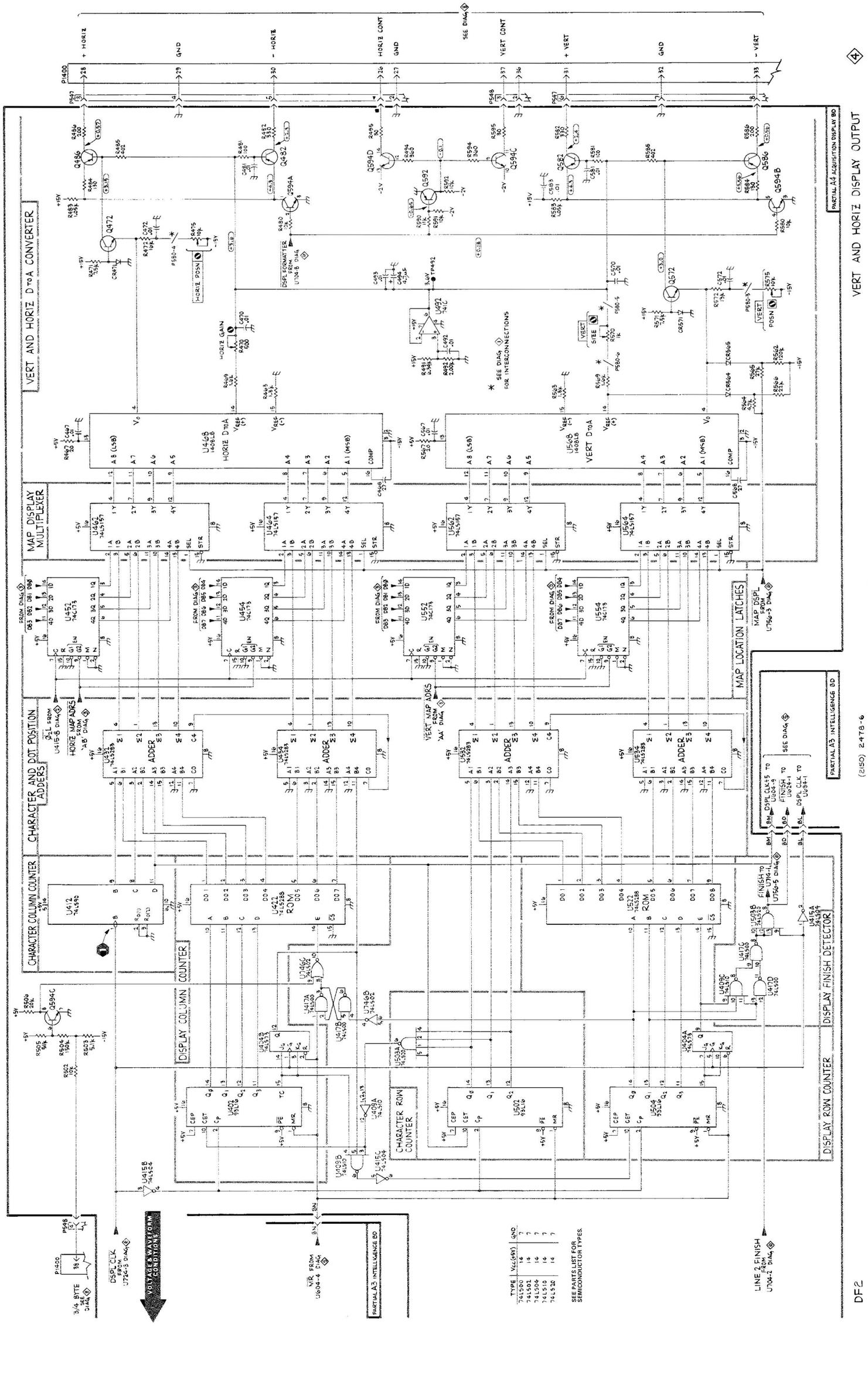
Voltages and waveforms shown are typical, but may vary between instruments.

TEST SETUP: The 7D01 is connected to the 7000-series mainframe Right-Vertical and A-Horizontal compartments through two 067-0616-00 Flexible Plug-in Extenders. The DF is connected to the 7D01 through a 067-0805-00 Cable Extender. The DF is set for a STATE TABLE BINARY, 7D01 ONLY display.

The test oscilloscope is dc coupled and internally triggered.



VERT AND HORIZ DISPLAY OUTPUT



VERT AND HORIZ DISPLAY OUTPUT

DF2

(2150) 2478-6

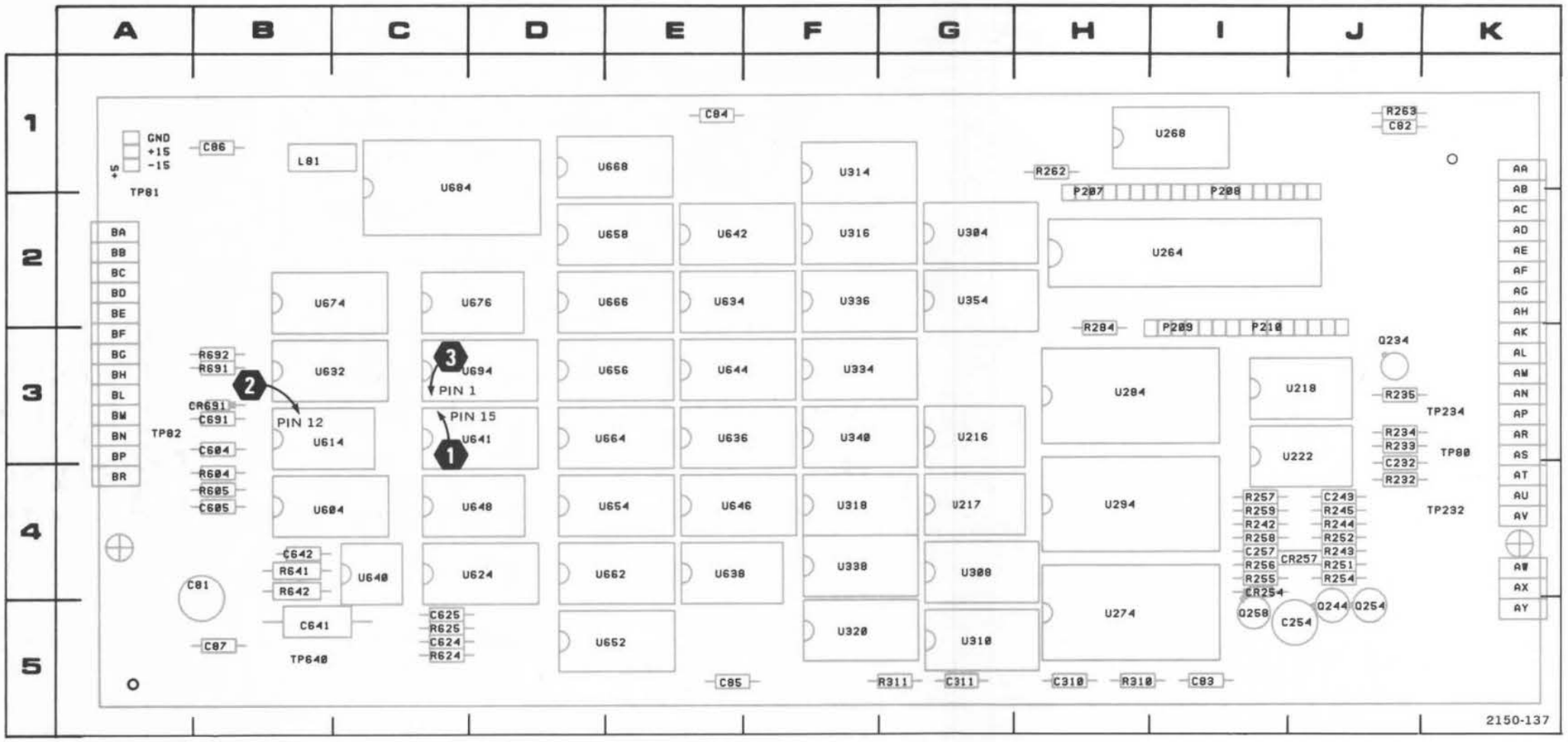
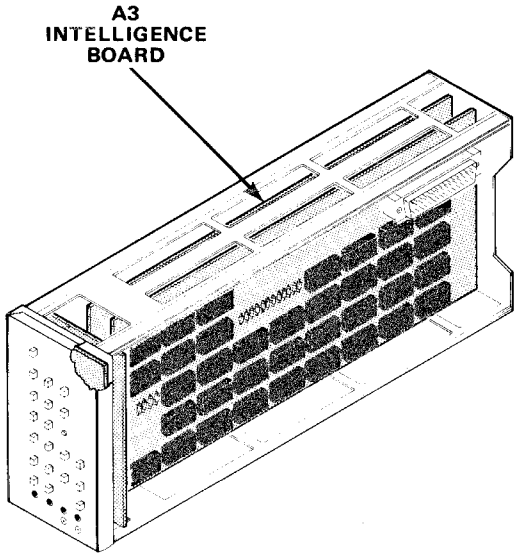


Figure 10-9. A3—Intelligence circuit board component locations.

CKT NO	GRID COORD
C81	4B
C82	1J
C83	5I
C84	1E
C85	5E
C86	1B
C87	5B
C232	3J
C243	4J
C254	5J
C257*	4I
C310	5H
C311	5G
C604	3B
C605	4B
C624	5C
C625	5C
C641	5B
C642	4B
C691	3B
CR254	4I
CR257*	4J
CR691	3B
L81	1B
P207	1H
P208	1I
P209	3I
P210	3I
Q234	3J
Q244	5J
Q254	5J
Q258	5I
R232	4J
R233	3J
R234	3J
R235	3J
R242	4I
R243	4J
R244	4J
R245	4J
R251	4J
R252	4J
R254	4J
R255	4I
R256	4I
R257	4I
R258	4I
R259	4I
R262	1H
R263	1J
R284	3H
R310	5H
R311	5G
R604	4B
R605	4B
R624	5C
R625	5C
R641	4B
R642	4B
R691	3B
R692	3B
TP80	3K
TP81	1A
TP82	3A
TP232	4K
TP234	3K
TP640	5B
U216	3G
U217	4G
U218	3J
U222	3J
U264	2I
U268	1I
U274	5H
U284	3H
U294	4H
U304	2G
U308	4G
U310	5G
U314	1F
U316	2F
U318	4F
U320	5F
U334	3F
U336	2F
U338	4F
U340	3F
U354	2G
U604	4C
U614	3C
U624	4D
U632	3C
U634	2E
U636	3E
U638	4E
U640	4C
U641	3D
U642	2E
U644	3E
U646	4E
U648	4D
U652	5E
U654	4E
U656	3E
U658	2E
U662	4E
U664	3E
U666	2E
U668	1E
U674	2B
U676	2D
U684	1C
U694	3D
VR687	2B

*See Parts List for serial number ranges.


A3
INTELLIGENCE
BOARD

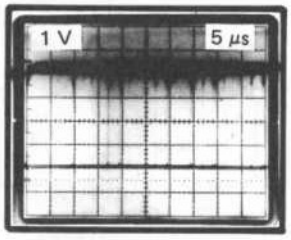
VOLTAGE AND WAVEFORM CONDITIONS

Voltages and waveforms shown are typical, but may vary between instruments.

TEST SETUP: The 7D01 is connected to the 7000-series mainframe Right-Vertical and A-Horizontal compartments through two 067-0616-00 Flexible Plug-in Extenders. The DF is connected to the 7D01 through a 067-0805-00 Cable Extender. The DF is set for a STATE TABLE BINARY, 7D01 ONLY display.

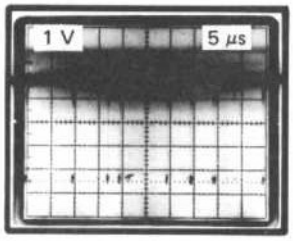
The test oscilloscope is dc coupled and internally triggered.

1



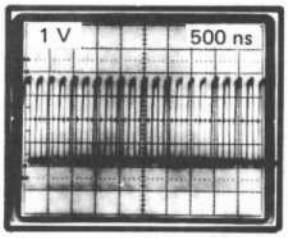
2 V

2

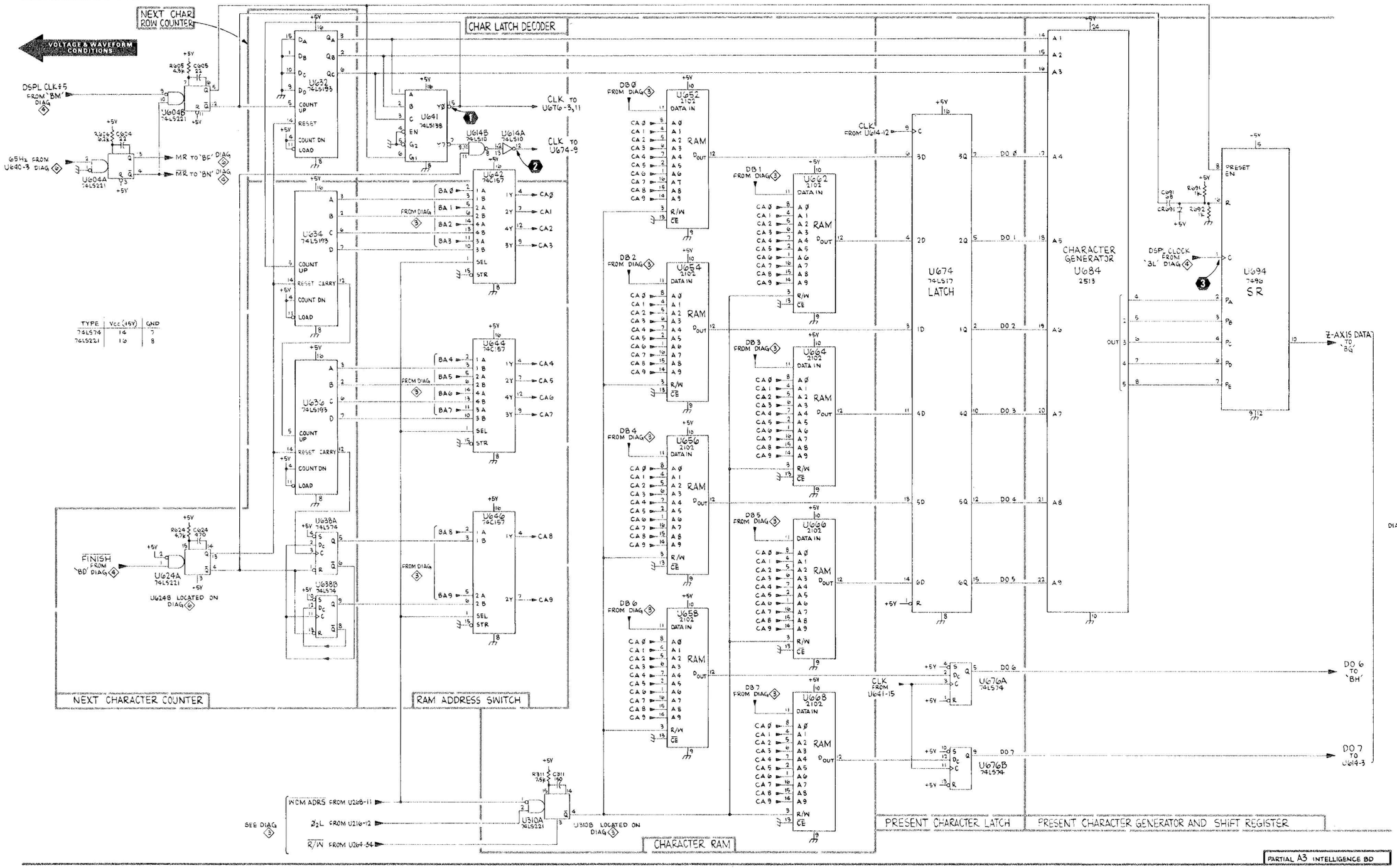


2 V

3



2 V



TYPE	Vcc (+5V)	GND
74LS74	14	7
74LS221	16	8

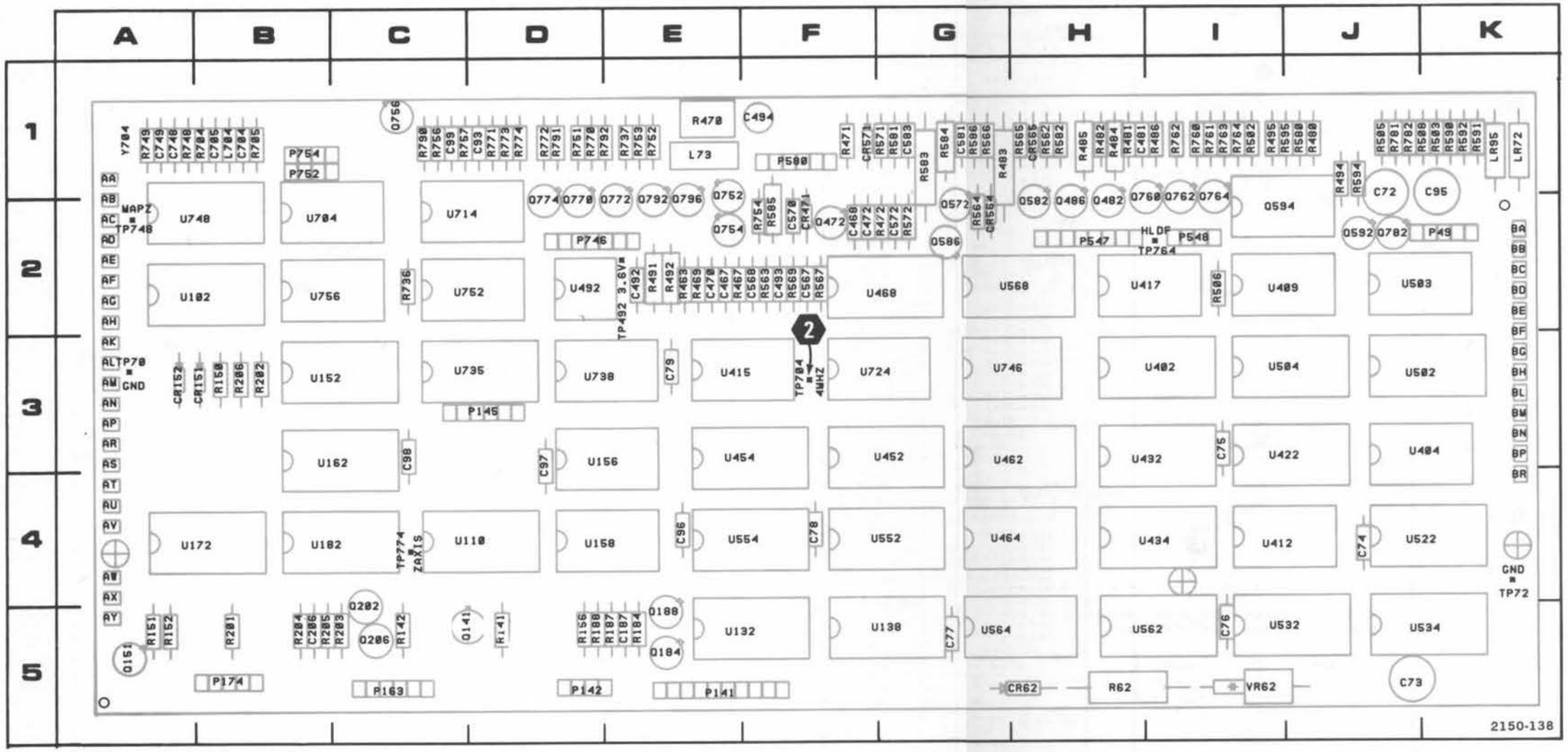


Figure 10-10. A4—Acquisition circuit board component locations.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
C72	1J	Q141	5C	R503	1K	U110	4C
C73	5J	Q151	5A	R505	1J	U132	5E
C74	4J	Q184	5E	R506	2I	U138	5G
C75	3I	Q188	5E	R508	1K	U152	3B
C76	5I	Q202	5C	R562	1H	U156	3D
C77	5G	Q206	5C	R563	2F	U158	4D
C78	4F	Q472	2F	R564	2G	U162	3B
C79	3E	Q482	2H	R565	1H	U172	4A
C93	1D	Q486	2H	R566	1G	U182	4B
C95	1K	Q572	2G	R567	2F	U402	3I
C96	4E	Q582	2H	R569	2F	U404	3K
C97	3D	Q586	2G	R571	1G	U409	2I
C98	3C	Q592	2I	R572	2G	U412	4I
C99	1C	Q594	2I	R580	1J	U415	3E
C187	5E	Q752	1E	R581	1G	U417	2I
C206	5B	Q754	2E	R582	1H	U422	3I
C467	2E	Q756	1C	R583	1G	U432	3I
C468	2F	Q760	2I	R584	1G	U434	4I
C470	2E	Q762	2I	R585	2F	U452	3E
C472	2F	Q764	2I	R586	1G	U454	3E
C481	1H	Q770	2D	R590	1K	U462	3G
C492	2E	Q772	2E	R591	1K	U464	4H
C493	2F	Q774	2D	R592	1K	U468	2F
C494	1F	Q782	2I	R594	1J	U492	2D
C567	2F	Q792	2E	R595	1J	U502	3K
C568	2F	Q796	2E	R704	1B	U503	2I
C570	2F			R705	1B	U504	3I
C572	2G	R62	5H	R736	2C	U522	4K
C581	1G	R141	5D	R737	1E	U532	5I
C583	1G	R142	5C	R748	1A	U534	5J
C704	1B	R150	3B	R749	1A	U552	4G
C705	1B	R151	5A	R751	1D	U554	4E
C748	1A	R152	5A	R752	1E	U562	5I
C749	1A	R156	5D	R753	1E	U564	5G
		R184	5E	R754	2F	U568	2H
CR62	5H	R187	5E	R756	1C	U704	2B
CR151	3B	R188	5D	R757	1C	U714	2C
CR152	3A	R201	5B	R760	1I	U724	3E
CR471	2F	R202	3B	R761	1I	U735	3D
CR564	2G	R203	5C	R762	1I	U738	3D
CR565	1H	R204	5B	R763	1I	U746	3G
CR571	1F	R205	5B	R764	1I	U748	2B
		R206	3B	R770	1D	U752	2C
L73	1E	R463	2E	R771	1D	U756	2B
L704	1B	R467	2E	R772	1D		
		R469	2E	R773	1D	VR62	5I
LR72	1K	R470	1E	R774	1D		
LR95	1K	R471	1F	R781	1J	Y704	1A
		R472	2F	R790	1C		
P49	2K	R480	1J	R791	1D		
P141	5E	R481	1H	R792	1E		
P142	5D	R482	1H				
P145	3D	R483	1G	TP70	3A		
P163	5C	R484	1H	TP72	4K		
P174	5B	R485	1H	TP492	2E		
P547	2H	R486	1I	TP704	3E		
P548	2I	R491	2E	TP748	2A		
P580	1F	R492	2E	TP764	2I		
P746	2D	R494	1J	TP774	4C		
P752	1B	R495	1I				
P754	1B	R502	1I	U102	2B		

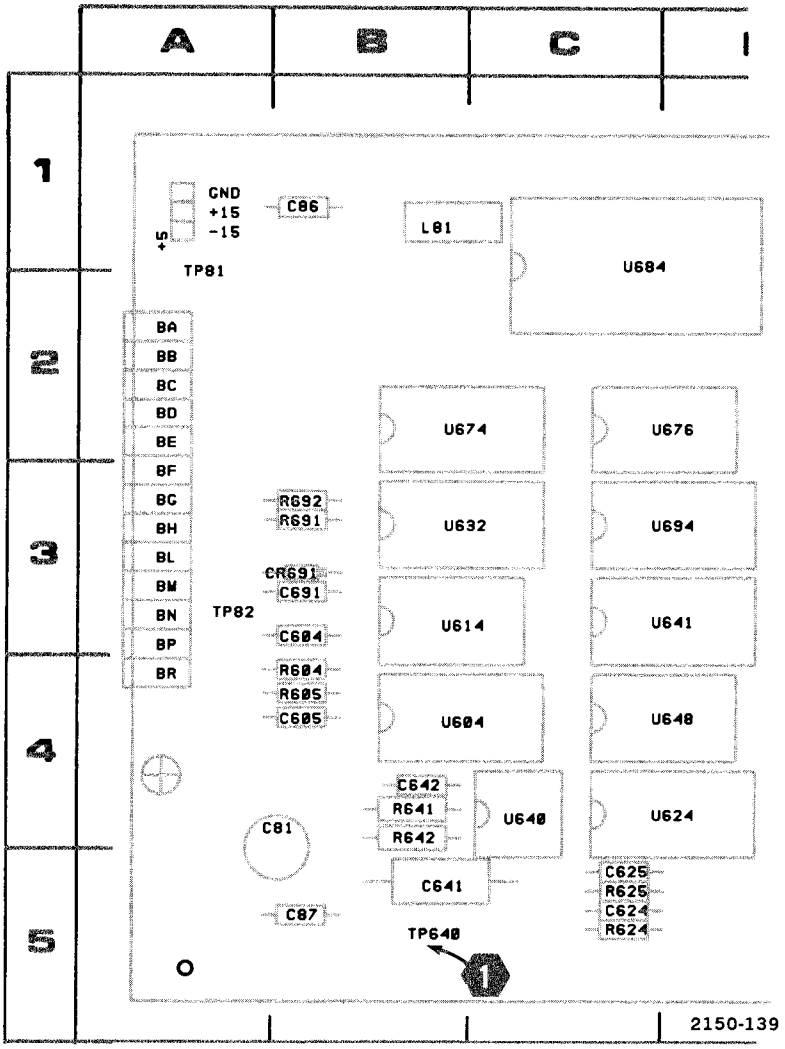
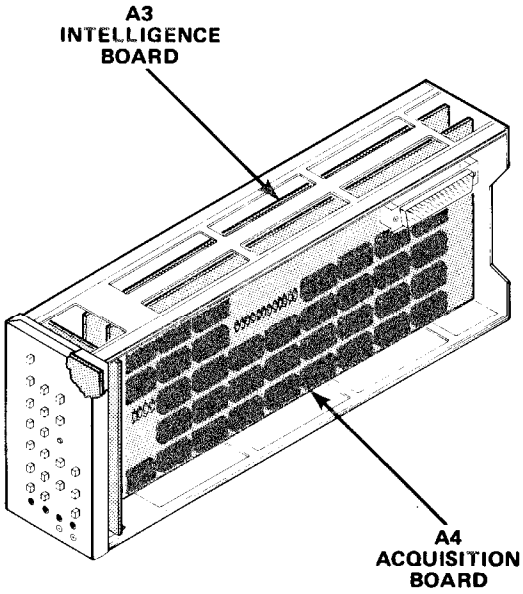


Figure 10-11. Partial A3--Intelligence circuit board. Component locations as viewed from the component side of the board.



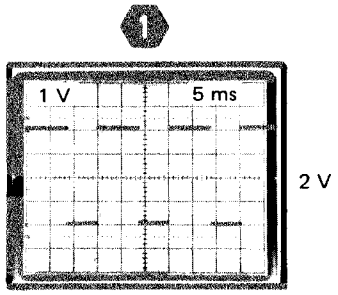
CKT NO	GRID COORD	CKT NO	GRID COORD
C625	5C	U614	3C
C641	5B	U624	4D
C642	4B	U640	4C
		U641	3D
		U642	2E
R625	5C	U648	4D

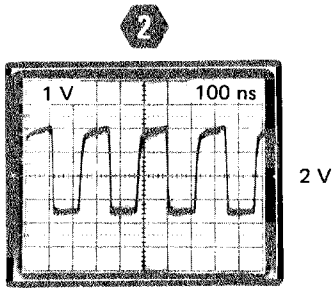
VOLTAGE AND WAVEFORM CONDITIONS

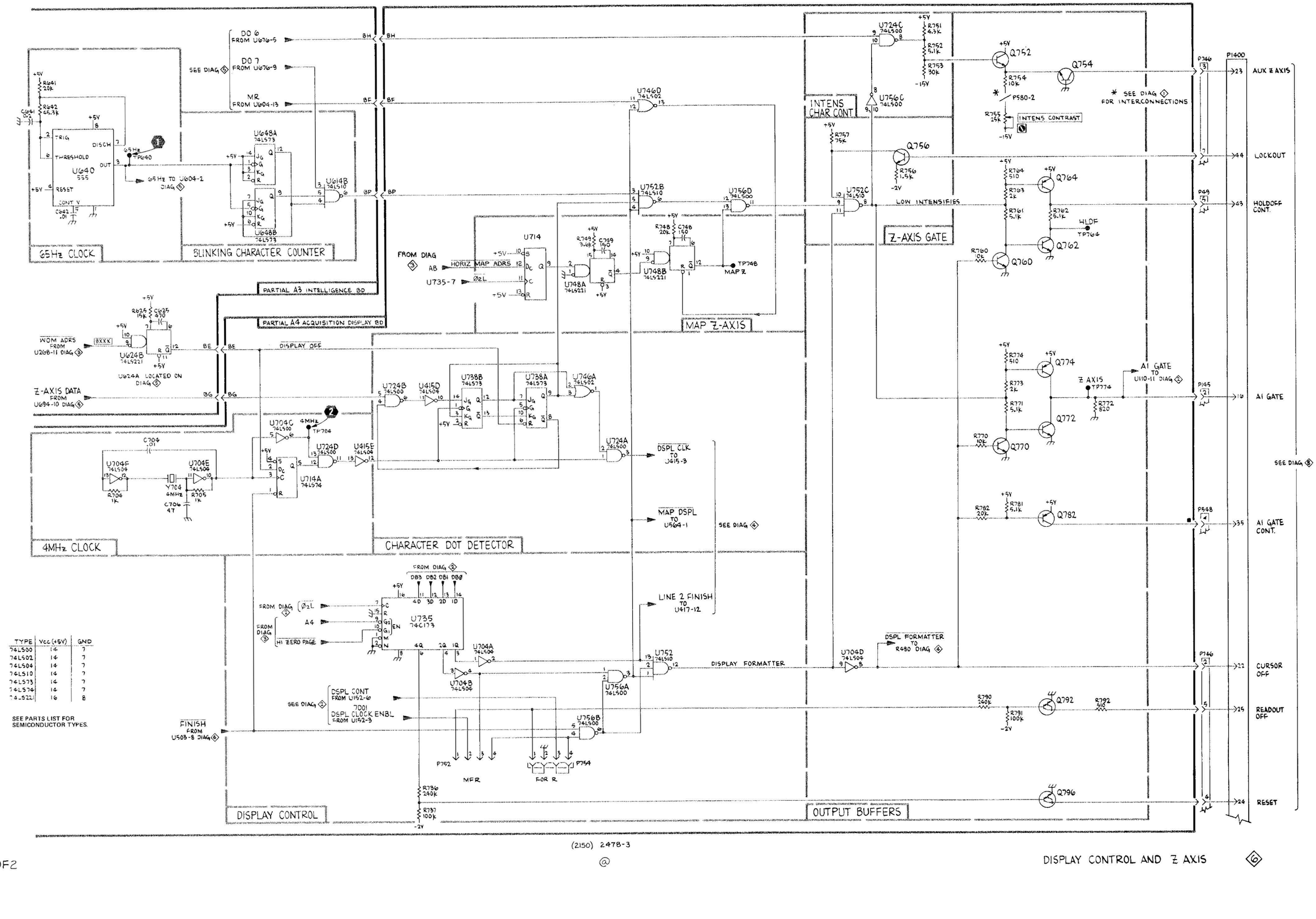
Voltages and waveforms shown are typical, but may vary between instruments.

TEST SETUP: The 7D01 is connected to the 7000-series mainframe Right-Vertical and A-Horizontal compartments through two 067-0616-00 Flexible Plug-in Extenders. The DF is connected to the 7D01 through a 067-0805-00 Cable Extender. The DF is set for a STATE TABLE BINARY, 7D01 ONLY display.

The test oscilloscope is dc coupled and internally triggered.







(2150) 2478-3

DF2

@

DISPLAY CONTROL AND Z AXIS 6

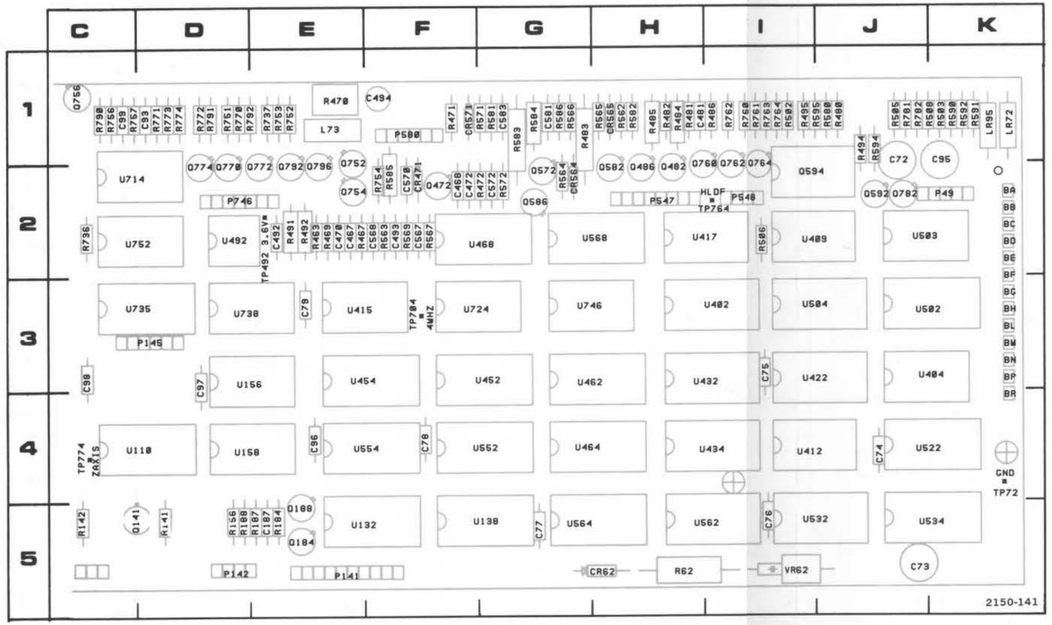
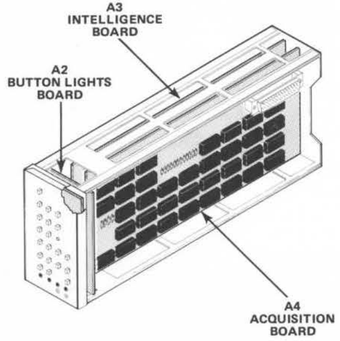


Figure 10-12. Partial A4—Acquisition circuit board. Component locations as viewed with board installed.

CKT NO	GRID COORD	CKT NO	GRID COORD
C72	1J	C99	1C
C73	5J		
C74	4J	CR62	5H
C76	5I		
C77	5G	L73	1E
C78	4F		
C79	3E	LR72	1K
C93	1D	LR95	1K
C95	1K		
C96	4E	R62	5H
C97	3D		
C98	3C	VR62	5I



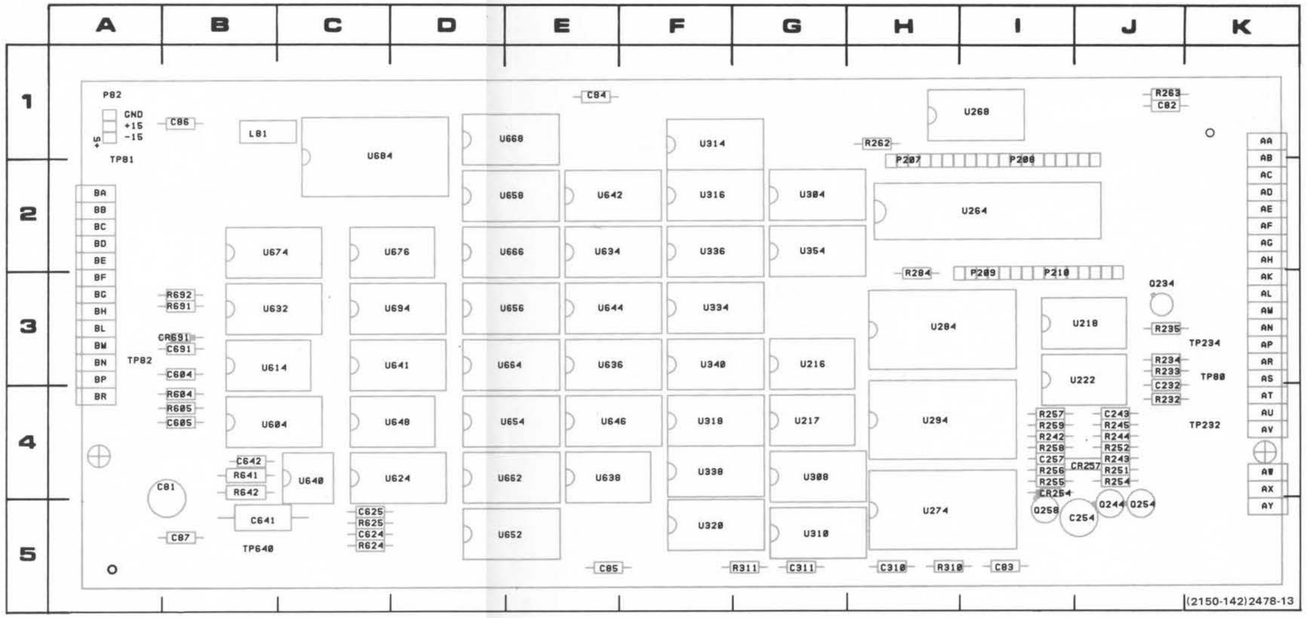


Figure 10-13. Partial A3—Intelligence circuit board component locations.

CKT NO	GRID COORD	CKT NO	GRID COORD
C81	4B	C87	5B
C82	1J		
C83	5I	L81	1B
C84	1E	P82	1A
C85	5E	TP81	1A
C86	1B	TP82	3A

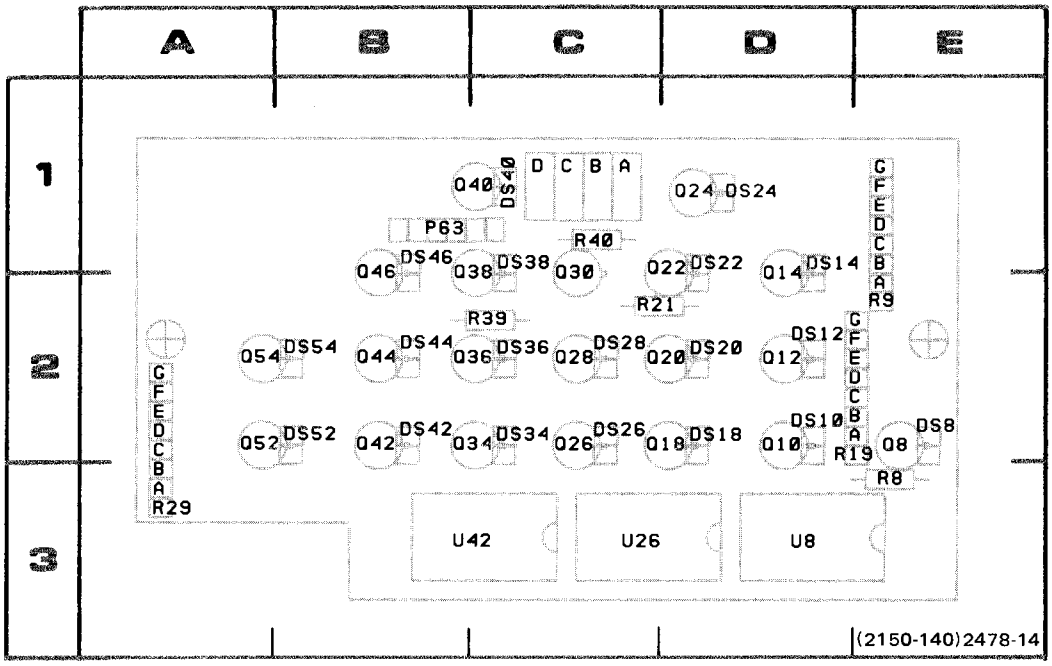
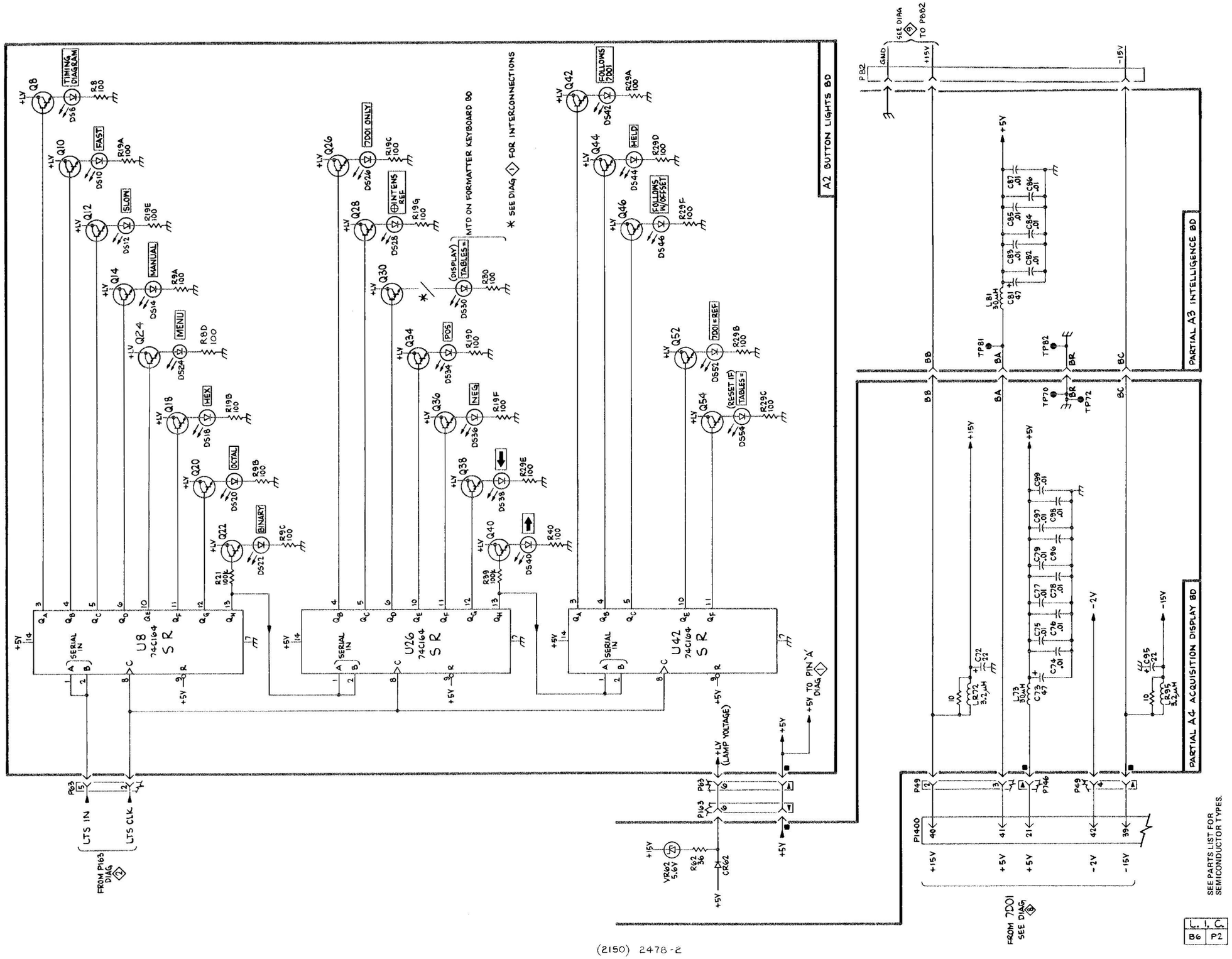


Figure 10-14. A2—Button Lights circuit board component locations, as viewed from component side of the board.

CKT NO	GRID COORD	CKT NO	GRID COORD	CKT NO	GRID COORD
DS8	2E				
DS10	2D	P63	1B	Q46	1B
DS12	2D	Q8	2E	Q52	2A
DS14	1D	Q10	2D	Q54	2A
DS18	2D	Q12	2D		
DS20	2D	Q14	1D	R8	3E
DS22	1D	Q18	2C	R9	2E
DS24	1D	Q20	2C	R19	2E
DS26	2C	Q22	1D	R21	2C
DS28	2C	Q24	1D	R29	3A
DS34	2C	Q26	2C	R39	2C
DS36	2C	Q28	2C	R40	1C
DS38	1C	Q30	1C		
DS40	1C	Q34	2B	U8	3D
DS42	2B	Q36	2B	U26	3C
DS44	2B	Q38	1B	U42	3C
DS46	1B	Q40	1C		
DS52	2B	Q42	2B		
DS54	2B	Q44	2B		


A2 BUTTON LIGHTS BD
PARTIAL A3 INTELLIGENCE BD
PARTIAL A4 ACQUISITION DISPLAY BD
U8 74C164 SR
U26 74C164 SR
U42 74C164 SR
SERIAL IN
MTD ON FORMATTER KEYBOARD BD
* SEE DIAG 1 FOR INTERCONNECTIONS
TIMING DIAGRAM
FAST
SLOW
MANUAL
MENU
HEX
OCTAL
BINARY
7D01 ONLY
INTENS REF
(DISPLAY) TABLES=
POS
NEG
FOLLOWS 7D01
HELD
FOLLOWS W/OFFSET
7D01=REF
(RESET IF) TABLES=
LTS IN
LTS CLK
FROM P163 DIAG 2
+LV (LAMP VOLTAGE)
+5V TO PIN 'A' DIAG 1
FROM 7D01 SEE DIAG 8
SEE DIAG 9 TO P882
SEE PARTS LIST FOR SEMICONDUCTOR TYPES.
L. I. C.
B6 P2

(2150) 2478-2

U860-3 Ø1H, R/W, HALT, VMA, Ø2L, BA, D0–D7 → P807 P207 → U216-10 (R/W 34, HALT 2, VMA 5, Ø2L 36, BA 7, D0 33, D1 32, D2 31, D3 30, D4 29, D5 28, D6 27, D7 26) U264 (U820 9–17; U860 5–2)

A15, A14, A13, A12 → P808 P208 → U264 (A15 25, A14 24, A13 23, A12 22) (U860 5–2)

R252 → P809 P209 → R252

CS3 → P809 P209 → U284-13

A0–A5 → P810 P210 → U264 (A0 9, A1 10, A2 11, A3 12, A4 13, A5 14) (U820 8–3)

A6, A7, A8, A9, A10, A11 → P810 P210 → U264 (A6 15, A7 16, A8 17, A9 18, A10 19, A11 20) (U820 2–1, 23–19)

+5V → P810 P210 → +5V (U860 1, 16)

P802 P82

GND, +15V → P802 → DIAG 3

A5 ROM EXTENDER BD

+15V

−15V

A3 INTELLIGENCE BD

U268-10, U268-9, U264-13 → DIAG 3

U264-12, U217-6, U264-11, U264-10, U264-9 → DIAG 4

U264-16, Q202-C, Q206-C, U222-2, U216-12 → DIAG 3

TO/FROM DIAG 3

TP81 +5V → DIAG 4

U503-8 → U624-1 DIAG 5

U624-12, U604-13, U694-10, U670-5 → U714-2, U738-6, U746-11, U724-5, U724-9 DIAG 6

U415-2, U412-11 → U694-1, U604-9 DIAG 5

U604-4 → U402-1 DIAG 4

U614-6 → U752-3 DIAG 6

TP82 TP70 TP72

P83 P163

+5V, U65-9, U65-8, DS 30 → Q30E SEE DIAG 1

+5V → U102-13 DIAG 1

PIN 8 U8, U16, U42 → U102-9 DIAG 2

U8-1,2 +1V → U102-16

+1V (LAMP VOLTAGE) DIAG 7

U172-6 DIAG 2

A2 BUTTON LIGHTS BD

A1 FORMATTER KEYBOARD BD

P74 P174

R68, R67, R66, R65 → U172-14, U172-13, U172-12, U172-11 DIAG 2

R152 −15V

RESET OUT J175

J171

P80 P580

−15V → R754 DIAG 6

R755 → R572 DIAG 4

R575, R574, R570, R570 → R472, R581, R569

A4 ACQUISITION DISPLAY BD

DF

P/J1400

SEE DIAG 2 U132 PIN 6, 5, 4, 3, 14, 13, 12, 11 → P141 U138-12, U138-11 → C8, C9, C2, C7, C3, C6, C0, C4, C1, C5

P141 → P1367 U1366-3, U1366-2, U1346-6, U1356-7, U1346-7, U1356-6, U1346-3, U1356-3, U1346-2, U1356-2 DIAG 8

P1351 Q1312-C, Q1316-C, U1370-8, U1344-13, U1332-6, R1696, P1493-1, Q1406-B, P1363-8 DIAG 8

PARTIAL A4 CURSOR BD

P142

DIAG 4 Q188-C, Q141-B → DISPLAY CLOCK, STORE

DIAG 3 Q202-B → 500KHz

PAD → +5VL

P112 U110-9, P560-4 DIAG 3

PARTIAL A2 MEMORY BD

P135

U182-11 → TRIGGER

DIAG 6 Q772-C, Q774-C → A1 GATE

DIAG 4 U110-14 → SD

U158-11 → FRAME

U102-7 → CURSOR CLOCK

P927 P967-1 DIAG 7; +5V DIAG 8; A17 DIAG 8; A11, GND DIAG 7, B11; −15V, +15V DIAG 8

PARTIAL A5 INTERCONNECT BD

P746

+5V → +5V

U704-8 → CURSOR OFF

DIAG 6 Q754-C → AUX Z AXIS

Q796-C → RESET

R792 → READOUT OFF

P612 U621-3 DIAG 4; P738-2; Q748-B DIAG 7

P547

R495 → HORIZ CONT.

R486 → GND

DIAG 4 R482 → + HORIZ

R582 → GND

R580 → − HORIZ

+ VERT

GND

− VERT

P382 Q762E; U838-14 DIAG 5

P568

DIAG 6 Q782-C → A1 GATE CONT

GND

DIAG 4 R595 → VERT CONT

R502 → 3/4 BYTE SW

P684 P694-2, P694-1 DIAG 6; Q682-E, R684

PARTIAL A3 OUTPUT BD

P99

−5V

+15V

+5V

DIAG 7 −2V → −2V

R762, Q769-C → HOLDOFF CONT

DIAG 6 Q756-B → LOCKOUT

P796

NOT USED

P950 +5V DIAG 8; +5V; −2V

PARTIAL A6 POWER SUPPLY BD

7D01

(2150) 2478-4

INTERCONNECTIONS 8

DF2

P/O A3 INTELLIGENCE BD.

P82 3 NC

P882 2 +15V

GND

REGULATED POWER SUPPLY

CR810

U810 μA7805 1 2 3

R810 30

C810 .47μf

+5V

C812 .1μf GND

PROGRAM ROM EXTENSION

SEE NOTE 2

A4 A3 A2 A1 AØ

P/O P209 P/O P809

P/O P210 P/O P810

A5 A6 A7 A8 A9 A10

SEE NOTE 2

A10 A9 A8 A7 A6 A5

P/O P208 P/O P808

P/O P210 P/O P810

A13 A14 A15 A11

P/O P207 P/O P807

$Ø_1L$

SEE NOTE 2

$Ø_1L$ A11 A12 A15 A14 A13

AØ-A4

A5-A10

DØ-D2

C820 .1μf

U820 6831B

24 21 E2 12 20 $\overline{E1}$ 18 $\overline{EØ}$

AØ 8 A1 7 A2 6 A3 5 A4 4

DØ 9 D1 10 D2 11 D3 13 D4 14

A5 3 A6 2 A7 1 A8 23 A9 22 A10 19

D5 15 D6 16 D7 17

SEE NOTE 1

C850 .1μf

D3-D7

EXTENDED ROM DECODER

FROM P810-8

+5V

U860 74LS138

16 G2A G1 G2B A B C 8

$Ø $4000 1 $4800 2 $5000 3 $5800

P/O P808 P/O P208

RESET

TO R252

SEE NOTE 2

P/O P809 P/O P209

$\overline{CS3}$

DØ D1 D2

P/O P807 P/O P207

DØ D1 D2

P/O P808 P/O P208

D3 D4

D5 D6 D7

D7 D6 D5 D4 D3

P/O P807 P/O P207

R/W HALT VMA $Ø_2L$ BA

BA $Ø_2L$ VMA HALT R/W GND +5V

TO U860-16

P/O P810 P/O P210

+5V GND

1 ONLY SOCKETS PROVIDED

2 TROUBLESHOOTING PINS

2478-1

A5 ROM EXTENDER BD.

DF2

@

ROM EXTENSION 9 DH

ROM EXTENSION 9

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
\- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
\- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
\- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

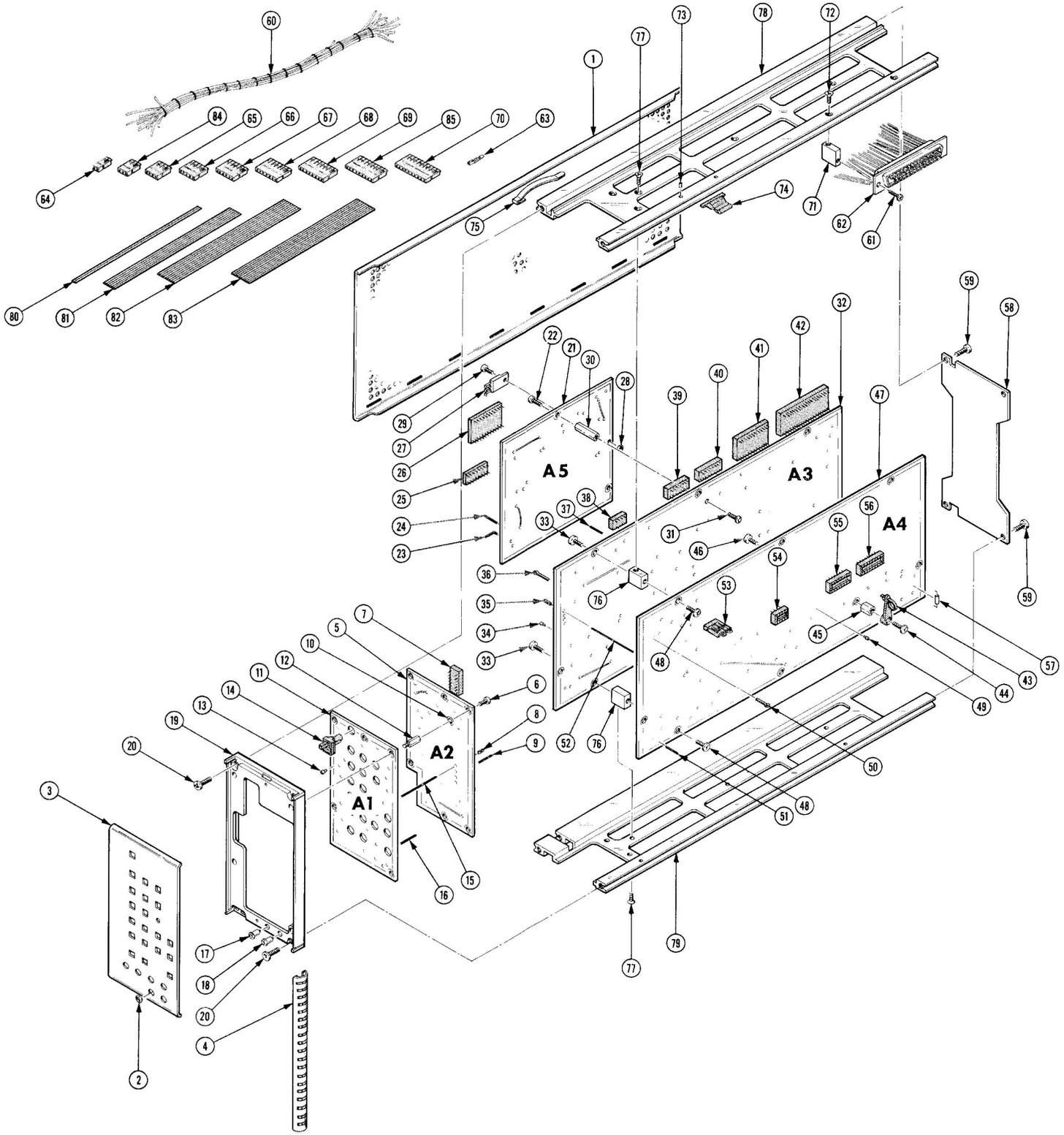
Mfr. Code	Manufacturer	Address	City, State, Zip
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
06540	AMATOM ELECTRONIC HARDWARE, DIV. OF MITE CORP.	446 BlAKE ST.	NEW HAVEN, CT 06515
08261	SPECTRA-STRIP CORP.	7100 LAMPSON AVE.	GARDEN GROVE, CA 92642
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
55210	GETTIG ENG. AND MFG. COMPANY	PO BOX 85, OFF ROUTE 45	SPRING MILLS, PA 16875
59730	THOMAS AND BETTS COMPANY	36 BUTLER ST.	ELIZABETH, NJ 07207
71279	CAMBRIDGE THERMIONIC CORP.	445 CONCORD AVE.	CAMBRIDGE, MA 02138
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82647	TEXAS INSTRUMENTS, INC., CONTROL PRODUCTS DIV.	34 FOREST ST.	ATTLEBORO, MA 02703
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
87308	N. L. INDUSTRIES, INC., SOUTHERN SCREW DIV.	P. O. BOX 1360	STATESVILLE, NC 28677

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	337-1064-04			1	SHIELD,ELEC:RIGHT SIDE	80009	337-1064-00
-2	358-0378-00			4	BUSHING,SLEEVE:GRAY PLASTIC	80009	358-0378-00
-3	333-2437-00			1	PANEL,FRONT:	80009	333-2437-00
-4	348-0235-00			2	SHLD GSKT,ELEC:4.734 INCH LONG	80009	348-0235-00
-5	----- -----			1	CKT BOARD ASSY:BUTTON LIGHTS(SEE A2 EPL)		
					(ATTACHING PARTS)		
-6	211-0007-00			4	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					- - - * - - -		
	----- -----			-	. CKT BOARD ASSY INCLUDES:		
-7	136-0269-02			3	. SOCKET,PLUG-IN:14 CONTACT,LOW CLEARANCE	01295	C951401
-8	136-0263-04			4	. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-9	131-0608-00			6	. CONTACT,ELEC:0.365 L X 0.25 PH BRZ GOLD PL	22526	47357
-10	210-1002-00			4	WASHER,FLAT:0.125 ID X 0.25 INCH OD,BRS	12327	OBD
-11	----- -----			1	CKT BOARD ASSY:KEYBOARD(SEE A1 EPL)		
					(ATTACHING PARTS)		
-12	129-0236-00			4	SPACER,POST:0.188 HEX X 0.375 INCH LONG	06540	9726-A-0440
					- - - * - - -		
	----- -----			-	. CKT BOARD ASSY INCLUDES:		
-13	136-0252-04			14	. SOCKET,PIN TERM:0.188 INCH LONG	22526	75060
-14	----- -----			21	. ACTR ASSY,PB:(SEE S8,S10,S12,S14,S18,S20		
	----- -----			-	. S22,S26,S28,S34,S36,S38,S40,S42,S44,S46,		
	----- -----			-	. S48,S52,S54,S58 EPL)		
-15	136-0591-00			4	. SOCKET ASSY,CRT:	80009	136-0591-00
-16	131-0608-00			11	. CONTACT,ELEC:0.365 L X 0.25 PH BRZ GOLD PL	22526	47357
-17	136-0387-00			1	JACK,TIP:GRAY	71279	450-4352-01-0318
-18	136-0387-01			1	JACK,TIP:BLACK	71279	450-4352-01-0310
-19	386-3632-00			1	SUBPANEL,FRONT:	80009	386-3632-00
					(ATTACHING PARTS)		
-20	213-0192-00			4	SCR,TPG,THD FOR:6-32 X 0.50 INCH,PNH STL	87308	OBD
					- - - * - - -		
-21	----- -----			1	CKT BOARD ASSY:ROM EXTENDER(SEE A5 EPL)		
					(ATTACHING PARTS)		
-22	211-0007-00			3	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					- - - * - - -		
	----- -----			-	. CKT BOARD ASSY INCLUDES:		
-23	131-0589-00			36	. CONTACT,ELEC:0.46 INCH LONG	22526	47350
-24	131-0608-00			36	. CONTACT,ELEC:0.365 L X 0.25 PH BRZ GOLD PL	22526	47357
-25	136-0260-02			1	. SOCKET,PLUG-IN:16 CONTACT,LOW CLEARANCE	82647	C951601
-26	136-0578-00			4	. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-27	----- -----			1	. TRANSISTOR:(SEE U810 EPL)		
					(ATTACHING PARTS)		
-28	210-0406-00			1	. NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	2X12161-402
-29	211-0008-00			1	. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
					- - - * - - -		
-30	129-0700-00			3	SPACER,POST:0.45 LONG,0.188 HEX,AL	80009	129-0700-00
					(ATTACHING PARTS FOR EACH)		
-31	211-0007-00			1	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					- - - * - - -		
-32	----- -----			1	CKT BOARD ASSY:INTELLIGENCE(SEE A3 EPL)		
					(ATTACHING PARTS)		
-33	211-0007-00			6	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					- - - * - - -		
	----- -----			-	. CKT BOARD ASSY INCLUDES:		
-34	136-0252-04			12	. SOCKET,PIN TERM:0.188 INCH LONG	22526	75060
-35	136-0263-04			34	. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-36	214-0579-00			6	. TERM.,TEST PT:0.40 INCH LONG	80009	214-0579-00
-37	131-0608-00			34	. CONTACT,ELEC:0.365 L X 0.25 PH BRZ GOLD PL	22526	47357
-38	136-0514-00			1	. SOCKET,PLUG IN:MICROCIRCUIT,8 CONTACT	73803	C950802
-39	136-0269-02			8	. SOCKET,PLUG-IN:14 CONTACT,LOW CLEARANCE	01295	C951401
-40	136-0260-02			32	. SOCKET,PLUG-IN:16 CONTACT,LOW CLEARANCE	82647	C951601
-41	136-0578-00			4	. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-42	136-0623-00			1	. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	C954002

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-43	346-0121-00			1		STRAP,ELEC COMP:TIE DOWN,5.0 LONG	59730	T4-34M
						(ATTACHING PARTS)		
-44	211-0507-00			1		SCREW,MACHINE:6-32 X 0.312 INCH,PNH STL	83385	OBD
						- - - * - - -		
-45	385-0127-00			1		SPACER,POST:ALUM HEX,0.25X 0.281	80009	385-0127-00
						(ATTACHING PARTS)		
-46	211-0503-00			1		SCREW,MACHINE:6-32 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
-47	----- -----			1		CKT BOARD ASSY:ACQUISITION(SEE A4 EPL)		
						(ATTACHING PARTS)		
-48	211-0007-00			6		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
-49	136-0252-04			75		. SOCKET,PIN TERM:0.188 INCH LONG	22526	75060
-50	214-0579-00			7		. TERM.,TEST PT:0.40 INCH LONG	80009	214-0579-00
-51	131-0608-00			67		. CONTACT,ELEC:0.365 L X 0.25 PH BRZ GOLD PL	22526	47357
-52	131-0592-00			34		. CONTACT,ELEC:0.885 INCH LONG	22526	47353
-53	131-1207-00			1		. LINK,TERM.CONNE:4 WIRE BLACK	80009	131-1207-00
-54	136-0514-00			1		. SOCKET,PLUG IN:MICROCIRCUIT,8 CONTACT	73803	C950802
-55	136-0269-02			17		. SOCKET,PLUG-IN:14 CONTACT,LOW CLEARANCE	01295	C951401
-56	136-0260-02			30		. SOCKET,PLUG-IN:16 CONTACT,LOW CLEARANCE	82647	C951601
-57	131-0566-00			2		. LINK,TERM.CONNE:0.086 DIA X 2.375 INCH L	55210	L-2007-1
-58	386-3633-01			1		PANEL,REAR:	80009	386-3633-01
						(ATTACHING PARTS)		
-59	213-0192-00			4		SCR,TPG,THD FOR:6-32 X 0.50 INCH,PNH STL	87308	OBD
						- - - * - - -		
-60	179-2505-00			1		WIRING HARNESS:CONNECTOR	80009	179-2505-00
						(ATTACHING PARTS)		
-61	211-0007-00			2		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. WIRING HARNESS INCLUDES:		
-62	131-1344-00			1		. CONNECTOR,PLUG,:50 CONT,MALE D	71468	DD-50P
-63	131-0707-00			78		. CONNECTOR,TERM.:0.48" L,22-26AWG WIRE	22526	75691-005
-64	352-0169-00			1		. CONN BODY,PL,EL:2 WIRE BLACK	80009	352-0169-00
-65	352-0162-00			1		. CONN BODY,PL,EL:4 WIRE BLACK	80009	352-0162-00
	352-0162-02			1		. CONN BODY,PL,EL:4 WIRE RED	80009	352-0162-02
	352-0162-08			1		. CONN BODY,PL,EL:4 WIRE GRAY	80009	352-0162-08
-66	352-0163-04			2		. CONN BODY,PL,EL:5 WIRE YELLOW	80009	352-0163-04
	352-0163-09			1		. CONN BODY,PL,EL:5 WIRE WHITE	80009	352-0163-09
-67	352-0164-00			1		. CONN BODY,PL,EL:6 WIRE BLACK	80009	352-0164-00
	352-0164-03			2		. CONN BODY,PL,EL:6 WIRE ORANGE	80009	352-0164-03
	352-0164-05			1		. CONN BODY,PL,EL:6 WIRE GREEN	80009	352-0164-05
-68	352-0165-06			1		. CONN BODY,PL,EL:7 WIRE BLUE	80009	352-0165-06
-69	352-0166-07			1		. CONN BODY,PL,EL:8 WIRE VIOLET	80009	352-0166-07
-70	352-0168-01			1		. CONN BODY,PL,EL:10 WIRE BROWN	80009	352-0168-01
-71	220-0790-00			2		NUT,BLOCK:0.188 X 0.5 INCH SQUARE	80009	220-0790-00
						(ATTACHING PARTS FOR EACH)		
-72	211-0025-00			1		SCREW,MACHINE:4-40 X 0.375 100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-73	214-1337-00			2		PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-74	214-2488-00			3		LATCH:GRAY PLASTIC	80009	214-2488-00
-75	214-1061-00			1		SPRING,GROUND:FLAT	80009	214-1061-00
-76	220-0793-00			6		NUT BLOCK:(1)4-40 THRU,(1)4-40 CROSS	80009	220-0793-00
						(ATTACHING PARTS FOR EACH)		
-77	211-0105-00			1		SCREW,MACHINE:4-40 X 0.188"100 DEG,FLH STL	83385	OBD
						- - - * - - -		
-78	426-0505-20			1		FR SECT,PLUG-IN:TOP	80009	426-0505-20
-79	426-0499-20			1		FR SECT,PLUG-IN:BOTTOM	80009	426-0499-20
	198-3888-00			1		WIRE SET,ELEC:	80009	198-3888-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-	131-0707-00			72		. CONNECTOR,TERM.:0.48" L,22-26AWG WIRE	22526	75691-005
-80	175-0825-00			FT		. WIRE,ELECTRICAL:2 WIRE RIBBON	08261	OBD
-81	175-0829-00			FT		. WIRE,ELECTRICAL:6 WIRE RIBBON	08261	OBD
-82	175-0832-00			FT		. WIRE,ELECTRICAL:9 WIRE RIBBON	08261	OBD
-83	175-0833-00			FT		. WIRE,ELECTRICAL:10 WIRE RIBBON	08261	OBD
-84	352-0161-02			2		. CONN BODY,PL,EL:3 WIRE RED	80009	352-0161-02
	352-0164-00			2		. CONN BODY,PL,EL:6 WIRE BLACK	80009	352-0164-00
	352-0164-09			2		. CONN BODY,PL,EL:6 WIRE WHITE	80009	352-0164-09
-85	352-0167-00			2		. CONN BODY,PL,EL:9 WIRE BLACK	80009	352-0167-00
	352-0167-07			2		. CONN BODY,PL,EL:9 WIRE VIOLET	80009	352-0167-07
	352-0168-09			2		. CONN BODY,PL,EL:10 WIRE WHITE	80009	352-0168-09

FIG. 1 EXPLODED



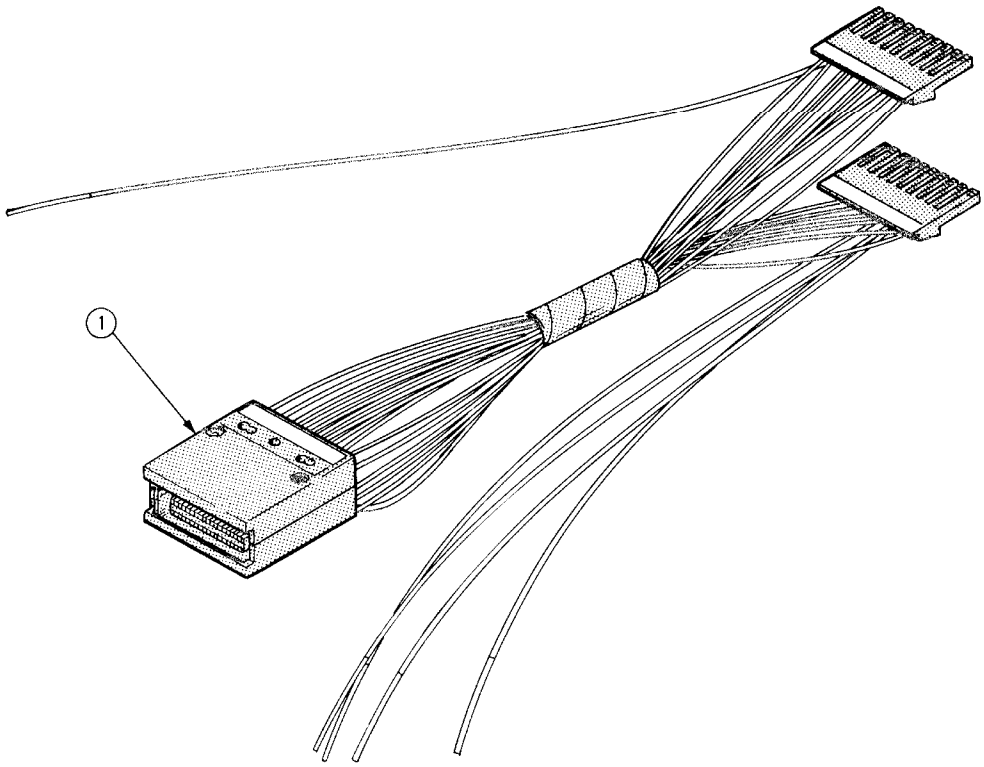


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
-1	103-0209-00			1		ADAPTER,CONN:GPIB TO PROBE	80009	103-0209-00
	070-2478-00			1		MANUAL,TECH:INSTRUCTION	80009	070-2478-00

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

TEKTRONIX®
committed to technical excellence

MANUAL CHANGE INFORMATION

PRODUCT DF1 and DF2
070-2150-00 & 070-2478-00

CHANGE REFERENCE M33349
DATE 4-19-78

CHANGE:	DESCRIPTION

EFF SN B040000 (DF1)

EFF SN B020000 (DF2)

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

CHANGE TO:

A3	670-4662-01	CKT BOARD ASSY:INTELLIGENCE
R257	315-0152-00	RES.,FXD,CMPSN:1.5K OHM,5%,0.25W

REMOVE:

C257	281-0773-00	CAP.,FXD,CER DI:0.01UF,10%,100V

ADD:

CR257	152-0075-00	SEMICOND DEVICE:GE,22V,40MA,G0238

DIAGRAM 3 MPU,PROGRAM AND DATA STORAGE

CR257 replaces C257 (cathode points toward R257).

TEKTRONIX®
committed to technical excellence

MANUAL CHANGE INFORMATION

PRODUCT DF1 and DF2
070-2150-00 & 070-2478-00

CHANGE REFERENCE M33554
DATE 5-16-78

CHANGE:	DESCRIPTION

EFF SN B044085 (DF1)

EFF SN B020515 (DF2)

ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

U422	160-0149-00	MICROCIRCUIT,DI:256 BIT PROM,IM561D

U422 is located on the ACQUISITION circuit board assembly and shown on diagram 4 VERT AND HORIZ DISPLAY OUTPUT.