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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

5D10 WAVEFORM DIGITIZER

WITH OPTIONS

SERVICE (Volume 1)

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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ACCESSORIES

CHANGE INFORMATION

RELATED DOCUMENTATION

The tabbed "ACCESSORIES" page at the rear of this manual lists the Tektronix part numbers of all Standard Accessories provided with this product. Also, Section 1 (General Information) contains a brief basic-content description for the following support-related publications:

MANUALS (Standard Accessories)

5D10 Operators

5D10 Service (Volume 1)

5D10 Diagnostic Troubleshooting (Volume 2)

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SAFETY SUMMARY

The general safety information contained in this summary is for servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL

Static-Sensitive Devices.

This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—refer to manual.

WARNINGS

POWER SOURCE

This product is intended to operate in a mainframe connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation.

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the mainframe power cord. To avoid electrical shock, plug the mainframe power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the mainframe power cord is essential for safe operation

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating), can render an electric shock.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

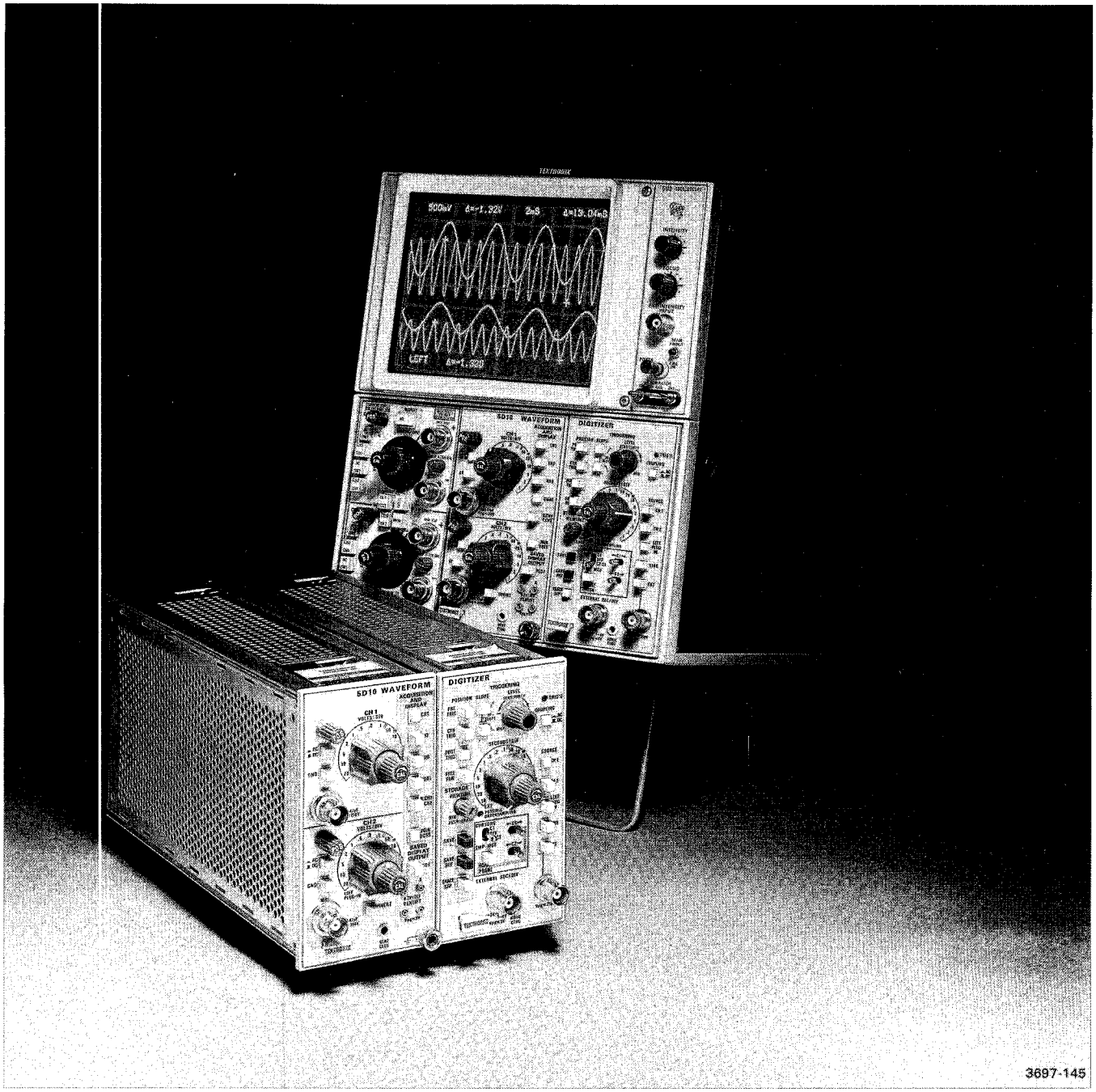
USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases.



5D10 FEATURES

The 5D10 Waveform Digitizer is designed to enhance the capabilities of 5000-series oscilloscope mainframes. Waveform storage, crt readout, two cursors for point-to-point measurements, pretrigger viewing, user adjustable viewtime, X-Y display, and analog plot output are just a few of the features this double-wide plug-in unit provides.

Waveform storage using digital memory eliminates the need for a storage crt and allows viewing information which occurred prior to a triggering event. Acquisition may be halted by a triggering event and automatically restarted at the end of the user-adjustable viewtime.

A complete numerical display, of cursor measurement values, and time base and amplitude settings is generated by the 5D10 (a readout-equipped mainframe is not required).

The front panel XY plot output properly connected to an XY recorder provides a hard copy of all information on the crt.

The 5D10 is capable of displaying and storing three channels simultaneously when used with a dual channel vertical amplifier such as the 5A18N.

GENERAL INFORMATION

This section contains a basic content description of both the Operators and Service manuals, information on instrument installation, power requirements, packaging for shipment, and specifications. The specification portion consists of three tables; Electrical, Environmental, and Physical Characteristics.

A Standard Accessories list and full-page dimensional drawing of the 5D10 is contained in this section.

OPERATORS MANUAL

The Operators Manual is divided into the following four sections:

Section 1—General Information contains content descriptions of the Operators and Service manuals, instrument description, mainframe and plug-in compatibility, packaging instructions and instrument specifications.

Section 2—Operating Instructions contains description of all front-panel controls, connectors and indicators and the crt readout fields generated by the 5D10.

A two part operators checkout procedure provides a basic operating procedure for the first-time user followed by a systematic demonstration of all front-panel controls.

Section 3—Applications explains in detail the procedure for making general oscilloscope measurements using the cursor function followed by some specific uses such as making color plots, measuring the settling time of a stepper motor shaft and viewing the events prior to a power supply failure.

Section 4—Instrument Options contains a description of available options.

SERVICE MANUAL

WARNING

THE SERVICE MANUAL CONTAINS INSTRUCTIONS FOR USE BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

The Service Manual is divided into 2 volumes. Volume 1 contains the following:

Section 1—General Information contains content descriptions of the Operators and Service manuals, mainframe and plug-in compatibility, packaging instructions and instrument specifications.

Section 2—Operating Instructions contains descriptions of all front-panel controls, connectors and indicators and the crt readout fields generated by the 5D10.

A two part operators checkout procedure provides a basic operating procedure for the first-time user followed by a systematic demonstration of all front-panel controls.

Section 3—Theory of Operation contains basic and general circuit analysis that will be useful for servicing the instrument.

Section 4—Maintenance describes routine and corrective maintenance procedures with detailed instructions for replacing assemblies, subassemblies, and individual components.

Section 5—Calibration contains procedures to check the operational performance and electrical characteristics of the instrument. Procedures also include methods for adjustment of the instrument to meet specifications.

Section 6—Instrument Options contains a description of available options.

Section 7—Replaceable Electrical Parts contains information necessary to order replaceable parts and assemblies related to the electrical functions of the instrument.

Section 8—Diagrams and Circuit Board Illustrations includes detailed circuit schematics, locations of assembled boards within the instrument, voltage and waveform information and circuit board component locators.

Section 9—Replaceable Mechanical Parts includes information necessary to order replaceable mechanical parts and shows exploded drawings which identify assemblies.

Volume 2 of the Service Manual contains the diagnostics necessary for troubleshooting the digital circuitry of the 5D10.

INSTALLATION

INITIAL INSPECTION

This instrument was inspected both mechanically and electrically before shipment. It should be free of mars or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the instrument for physical damage incurred in transit and check the basic instrument functions by following the Detailed Checkout Procedure in Section 2, Operating Instructions. Performance Requirements can be verified by referring to the Calibration section of this manual. If there is damage or deficiency, contact your local Tektronix Field Office or representative.

OPERATING TEMPERATURE

The 5D10 can be operated where the ambient air temperature is between 0° and +45° C and can be stored in ambient temperatures from −55° to +75° C. After storage at temperatures outside the operating limits, allow the chassis temperature to reach operating limits before applying power.

MAINFRAME COMPATIBILITY

The 5D10 operates in the right vertical and horizontal compartments of any 5000-series mainframe, however some mainframes may require modification. Refer to Table 1-1 for 5100-series mainframes that require modification to the Interface board before the Left Plug-in mode may be used for channel 2 signal acquisition.

WARNING

Only qualified service personnel are authorized to make modifications.

We recommend that all mainframes requiring modification number M45180 also incorporate modification number M44151 to prevent changes in display vertical position and gain when the left plug-in is installed or removed. Modifications are described in the Maintenance section of this manual.

TABLE 1-1
Mainframe Compatibility

Mainframe	Serial No.	Modification No.
5110	below B126109	M45180
5111	below B134580	
5112	All	
5113	below B116870	
5115	below B094140	

If the 5D10 is used in the 5111, 5111A, 5113, 5115, or the 5441 Storage Oscilloscope, the mainframe should be operated only in the non-storage mode.

If the 5D10 is used in the 5115 Storage Oscilloscope, the Enhance control must be rotated fully counterclockwise.

When the 5D10 is installed in the 5223 Digitizing Oscilloscope, the mainframe is used only for real-time displays. The 5223 digitizing functions are inoperative.

We do not recommend use of the LEFT PLUG-IN function when the 5D10 is installed in the 5223, 5440, 5441, or the 5444 Oscilloscope mainframe.

INSTALLING THE 5D10 IN THE MAINFRAME

The 5D10 is designed to operate in the right vertical and horizontal plug-in compartments.

NOTE

Switch off the mainframe power before installing or removing the 5D10.

To install the 5D10 in the mainframe, align the grooves in the top and bottom of the instrument with the guides at the top and bottom of the plug-in compartment. Then push the 5D10 in until its front panel is flush with the front panel of the mainframe. See Figure 1-1.

NOTE

Make sure that both halves of the 5D10 are firmly seated against the mainframe front panel.

To remove the unit, pull both release latches simultaneously to disengage the unit from the mainframe, then pull it from the plug-in compartments leaving the mainframe on the bench.

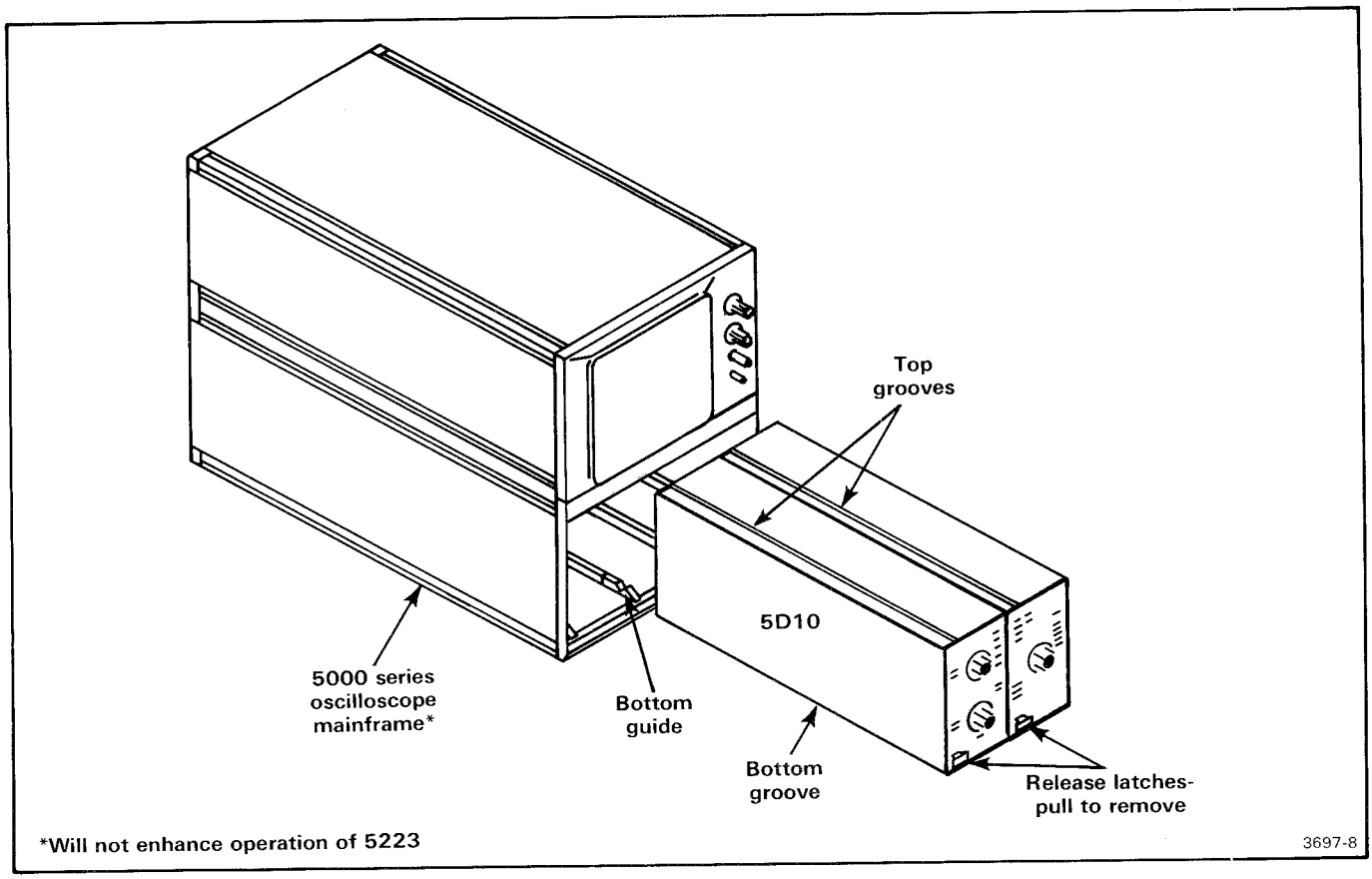


Figure 1-1. Installing the 5D10 in the mainframe.

PLUG-IN COMPATIBILITY

Any 5000-series amplifier plug-in may be used in the left vertical compartment of the oscilloscope mainframe as a single-trace signal source for 5D10 channel 2 however, we recommend the incorporation of a noise reduction modification to some differential amplifier units. The modification number and affected plug-in units are listed in Table 1-2. For dual-trace acquisition, compatibility considerations listed in Table 1-3 must be observed.

TABLE 1-2
Recommended Modification to Differential Amplifier Plug-Ins

Plug-in	Serial No.	Modification No.
5A13N	below B051988	M44783
5A20N	All	M44686
5A21N	below B084949	M44686

The 5CT1N Curve Tracer is usable with the 5D10 (proper acquisition speed must be selected for proper XY display). However, cursor operation is somewhat difficult, especially if SAVE REF is selected.

PACKAGING FOR SHIPMENT

If this instrument is to be shipped for long distances by commercial transportation, we recommend that the instrument be packaged in the original manner. The carton and packaging material in which your instrument was shipped should be saved and used for this purpose.

NOTE

Package and ship Plug-Ins and Mainframes separately.

Also, if this instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: Owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

TABLE 1-3
Plug-In Compatibility

Plug-In	Operating Conditions	Symptom	Cause
5A18N (SN below B128131)	Dual Trace; 5D10 Sec/Div = 1 ms or faster.	Waveforms distorted.	Plug-in channel switch settling time too slow. 5A18N and 5A26 may be updated with kit, Tektronix Part 040-0963-01 (5A18N) or kit 040-0964-00 (5A26).
5A26 (SN below B051662)			
5B12N	Dual Sweep; 5D10 Sec/Div = 1 ms or faster.	Waveforms distorted.	Plug-in channel switch settling time too slow.
5A14N	Any two channels on; 5D10 Sec/Div = 1 ms or faster.	Waveforms distorted.	Plug-in channel switch settling time too slow.
	Three or four channels on.	Display smeared or poor quality.	5D10 not designed to accommodate three- or four-channel Left Vertical acquisition.
	Channel 1 or 2 on; and Channel 3 or 4 on.	Display smeared or poor quality	Dual trace operation requires Channel 1 and 2, or Channel 3 and 4.

If the original packaging is unfit for use or not available, package the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions; refer to Table 1-4 for carton test strength requirements.

2. Enclose the instrument with polyethylene sheeting or equivalent to protect the finish of the instrument.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches of packing on each side.

4. Seal the carton with shipping tape or with an industrial stapler.

5. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

TABLE 1-4
Shipping Carton Test Strength

Gross Weight (lb)	Carton Test Strength (lb)
0-10	200
10-30	275
30-120	375
120-140	500

SPECIFICATION

The electrical characteristics listed in Table 1-5 apply when the following conditions are met: (1) Calibration of the instrument must have taken place at an ambient temperature between +20° and +30° C, (2) the instrument must be allowed a 20-minute warm-up period, (3) all specifications are valid at an ambient temperature of 0° to +45° C, unless otherwise stated, (4) the instrument must be in an environment that meets the limits described in Table 1-6.

Any applicable conditions not listed above are expressly stated as part of that characteristic. Environmental characteristics are listed in Table 1-6 and Physical characteristics are listed in Table 1-7.

TABLE 1-5
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL SYSTEM	
Deflection Factor	
Calibrated Steps	1 mV to 20 V per div; 14 steps in a 1-2-5 sequence. Additional position of Channel 2 VOLTS/DIV switch selects signal from Left Plug-In.
Variable Range (Uncal)	Continuously variable between steps.
Accuracy	
Input to Readout Numbers	
1 mV/Div & 2 mV/Div	±2%.
5 mV/Div to 1 V/Div	±1%.
2 V/Div to 20 V/Div	±2%.
Input to Crt Graticule	±2%.
From Left Vertical Plug-In	Add ±1% to above specifications.
Added	Add ±1% to above specifications.
Readout Numbers to CRT	±2%.
Bandwidth	
Single Channel	Suitable for dc to 100 kHz.
Dual Channel	Suitable for dc to 50 kHz.
Input	
R and C	1 MΩ, ±0.5%; 47 pF approximately.
Voltage (Maximum)	250 V (dc + peak ac); 250 V ac p-p at 1 kHz or less.
AC Coupling (-3 dB Point)	10 Hz or less (1 Hz with 10X probe).
Position Range	At least ±5 div.

TABLE 1-5 (Cont)
Electrical Characteristics

Characteristic	Performance Requirement
VERTICAL SYSTEM (Cont)	
Common Mode Rejection Ratio (Add, CH 2 Invert)	At least 50:1, dc to 100 kHz.
Channel Isolation	
Input Related	At least 80 dB, dc to 100 kHz.
Display Related	At least 40 dB, dc to 100 kHz (between Ch 1 and Ch 2).
	At least 34 dB, dc to 100 kHz (between) left plug-in channels acquired by Ch 2).
Phase Shift	
DC to 100 kHz	Less than 1.0 degree phase shift between Ch 1 and Ch 2.
Resolution	
X-Y and Y-T	0.04 div (8-bit digitizer).
HORIZONTAL SYSTEM	
Time Base	
Calibrated Rates	0.1 ms to 50 sec/div, 18 steps in a 1-2-5 sequence.
Uncalibrated	Continuously variable between steps.
Accuracy	±1% (to readout numbers).
External Input	Allows external pulse generator to determine acquisition rate. Sampling occurs on negative-going edge of input pulse.
Voltage	TTL levels.
Frequency (Max)	1 MHz.
Resolution	
X-Y	0.04 div (8-bit digitizer).
Y-T	0.01 div (1024 memory locations shared among all traces acquired).
POSSIBLE UNDERSAMPLING Indicator	Indicator lights when fewer than eight sample pulses occur during interval between successive threshold crossings of triggering signal. Depends on Trigger SOURCE, LEVEL, and SLOPE control settings.

TABLE 1-5 (Cont)
Electrical Characteristics

Characteristic	Performance Requirement
TRIGGERING SYSTEM	
Sources	Channel 1, Channel 2, Left plug-in (via mainframe), Line, External.
Coupling	Dc, ac.
Sensitivity	
+ or − Slope	
External	100 mV, dc to 50 kHz or pulse width greater than 5 μs. 250 mV, 50 kHz to 250 kHz or pulse width greater than 1 μs.
CH 1, CH 2, Left	0.4 div, dc to 50 kHz, or pulse width greater than 5 μs. 1.0 div, 50 kHz to 250 kHz, or pulse width greater than 1 μs.
Bi-Slope Trigger	Amplitude, frequency, and pulse width of + or − specifications apply to absolute value of signal (i.e., rectified).
External Input	
R and C	1 MΩ, ±2%; 47 pF approximately.
Voltage (Max)	250 V (dc + peak ac); 250 V p-p ac at 1 kHz or less.
TRIG'D Indicator	Indicator lights when triggering signal passes through threshold.
RECORDER SYSTEM	
Penlift	
Logic	Isolated (floating) switch, SPST; normally open or normally closed contacts, modification to be performed only by qualified service personnel.
Voltage (Max)	5 V, dc or rms.
Current (Max)	50 mA, dc or rms.
Pen-up (blanking) Duration	180 ms, ±20%.
Display Output (X and Y)	
Amplitude	0.2 V/div, within 2%.
Speed	Accomodates recorders with slew rate at least 20 inches/second.

TABLE 1-6
Environmental Characteristics

Characteristic	Performance Requirement
Temperature	
Operating	0°C to +45°C.
Storage	-55°C to +75°C.
Altitude	
Operating	To 15,000 feet (4,500 m). Maximum operating temperature decreases 1°C per 1,000 feet above 5,000 feet.
Storage	To 50,000 feet (15,000 m).
Humidity	
Operating and Storage	5 days, per MIL-STD-810C, method 507-1, Procedure 4, except 90-95% RH.
Vibration	
Operating	Tested to MIL-T-28800B SECT. 4.5.5.3.1 Type 2, Class 5, Style E & F.
Shock	Tested to MIL-T-28800B SECT. 4.5.5.4.1 Type 2, Class 5, Style E & F.
Bench Handling	Tested to MIL-T-28800B SECT. 4.5.5.4.4 Type 2, Class 5, Style E & F.
Transportation	National Safe Transit Assoc., Preshipment Test Procedure.
Vibration and Bounce (packaged product)	NSTA. PROJECT 1 A-B-1.
Drop (packaged product)	NSTA. PROJECT 1 A-B-2.

TABLE 1-7
Physical Characteristics

Characteristic	Information
Weight	2.3 kg (5 lb).
Overall Dimensions	See Figure 1-2, the dimensional drawing.

STANDARD ACCESSORIES

1 ea ..... Operators Manual
1 ea ..... Service Manual (Volume 1)
1 ea ..... 5D10 Diagnostic Troubleshooting Service Manual (Volume 2)

For more detailed information, refer to the tabbed Accessories page at the rear of this manual.

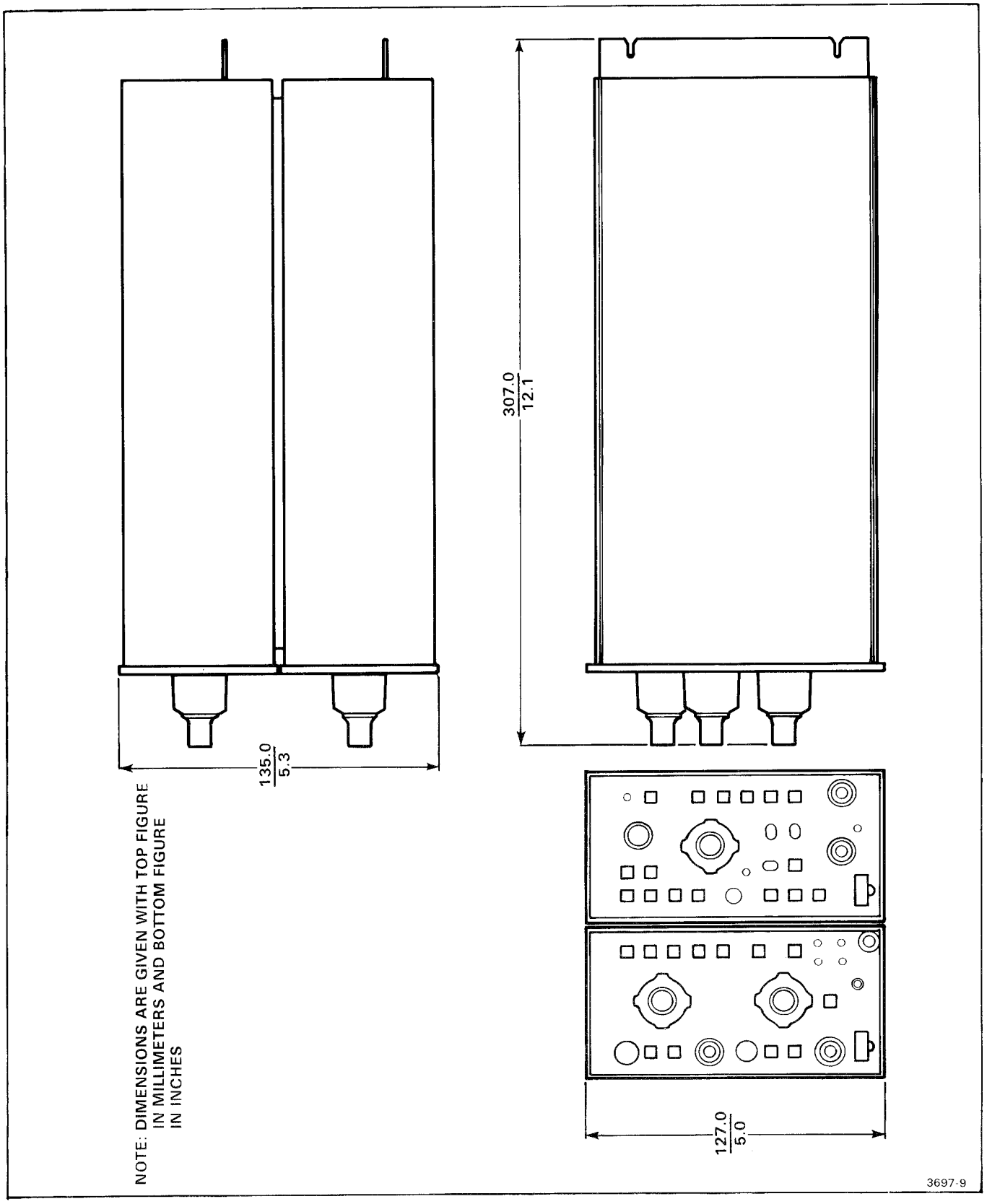


Figure 1-2. Dimensional drawing.

OPERATING INSTRUCTIONS

This section will familiarize you with the capabilities and operation of the 5D10 Waveform Digitizer. A thorough understanding of this information will remove later uncertainty when troubleshooting your equipment.

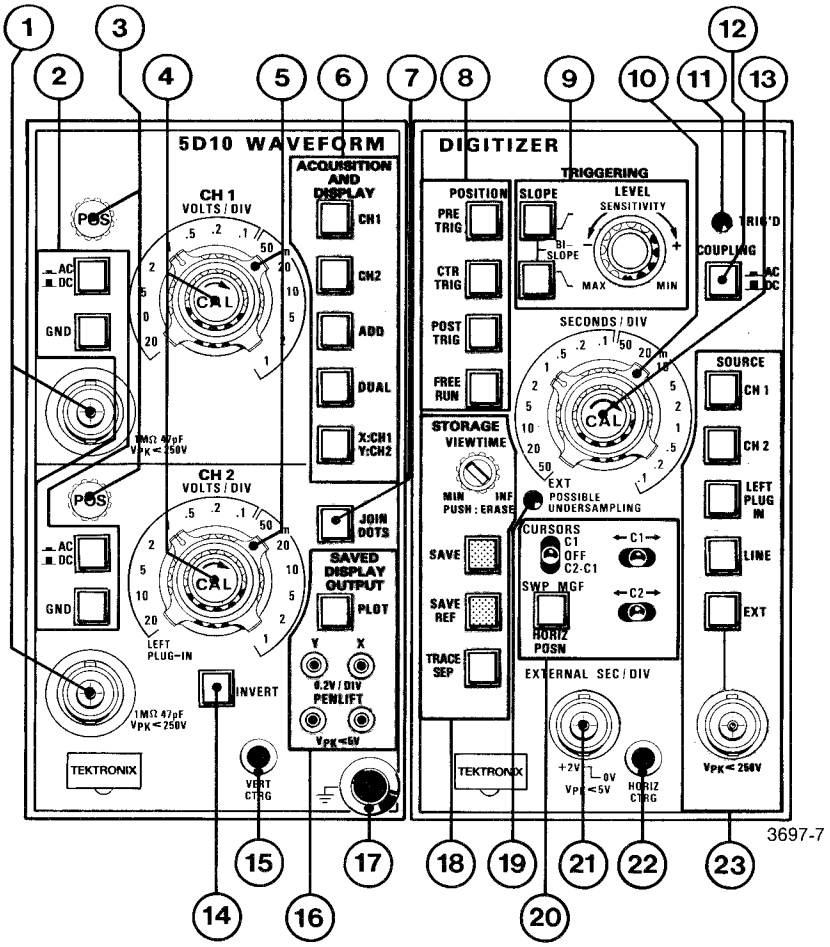
Familiarization begins with illustrations and descriptions of all front panel controls, connectors and indicators followed by explanations of the crt readout fields generated by the 5D10.

A two-part operators checkout procedure provides a basic operating procedure for the first-time user followed by a systematic demonstration of all front-panel controls.

CONTROLS, CONNECTORS, AND INDICATORS

All controls, connectors, and indicators required for the normal operation of the 5D10 Waveform Digitizer unit are located on the front panel; however, recorder pen-lift control can be altered by positioning the internal Link-Plug (jumper J1050) on the A3 Output circuit board (refer to "Setting the Penlift Polarity (J1050)" at the end of this section). Also, the triggering logic can be altered by positioning the internal Link-Plug (jumper J106) on the A4 Data circuit board (refer to "Triggering" later in this section).

Figure 2-1 is provided with numbered controls and connectors to identify the control descriptions that follow.



(1) **Input Connectors**—Bnc connectors (CH 1, CH 2) for applying signals to the amplifiers. A probe coding ring is provided for activating the correct readout when using a 10X probe.

(2) **Input Coupling push-buttons**

AC—DC—Button pushed "in" selects capacitive coupling of the signal applied to the amplifier. When GND & AC are both "in" the capacitor precharges to the input signal dc level. The "out" position provides direct coupling of the input signal.

GND—Grounds the amplifier input while connecting the input signal to ground through a 1 MΩ resistor. If ground is pushed "in" during an ERASE operation, then the ground reference data in the cursor readout system is updated.

(3) **POSition Controls**—Vertically positions the signal being acquired[1].

(4) **CAL (Variable Volts/Div)**—Provides continuously variable deflection factors between the calibrated settings of the VOLTS/DIV switch and extends the deflection-factor range to (approx) 50 volts/division.

(5) **VOLTS/DIV (CH 1, CH 2)**—Volts per major graticule division. This control selects the calibrated deflection factors from 1 mV to 20 V/DIV, 14 steps in a 1-2-5 sequence. The LEFT PLUG-IN may be selected as the amplifier input for CH 2 only.

(6) **ACQUISITION AND DISPLAY**

CH 1—Selects Channel 1 signal to be acquired[1] and displayed.

CH 2—Selects Channel 2 signal to be acquired[1] and displayed.

ADD—Channel 1 and Channel 2 signals are algebraically added, and the result is acquired[1] and displayed.

DUAL—Channel 1 and Channel 2 signals are separately acquired[1], and displayed as 2 waveforms, in y-t format.

X:CH1, Y:CH2—Channel 1 and Channel 2 signals are separately acquired[1] and displayed as one waveform in X-Y format.

(7) **JOIN DOTS**—Out position, waveform display consists of dots representing sampled signal values. In position, vectors are displayed between sampled signal values. The dots representing the sampled signal values are not displayed.

[1]Acquired, is defined as: Sampled, digitized, and stored in memory.

Figure 2-1. Front panel controls and connectors.

(8) **TRIGGERING POSITION**—Selects the trigger point on the saved waveform or defeats triggering (FREE RUN).

After a trigger event is recognized, acquisition continues until enough data to display a full horizontal trace (refer to Triggering Logic in Detailed Operating Instructions) has been acquired[1] then:

in PRE TRIG	7/8 of memory data prior to trigger, 1/8 following is displayed.
in CTR TRIG	1/2 of memory data prior to trigger and 1/2 following is displayed.
in POST TRIG	1/8 of memory data prior to the trigger and 7/8 following is displayed.
in FREE RUN	Acquisition is continuous and stops only when SAVE or SAVE REF is pushed manually.

(9) **TRIGGERING SLOPE, LEVEL, SENSITIVITY**—Selects the amplitude of the window or ± excursion that will cause triggering.

SLOPE—Selects + or − triggering slope signal. If both are pushed in, BI-SLOPE triggering recognizes signal excursion away from zero in either direction (+,−).

LEVEL/SENSITIVITY—With + or − TRIGGERING SLOPE selected, controls the amplitude point at which triggering occurs. With BI-SLOPE triggering selected, controls the sensitivity, or absolute value of signal to cause triggering.

(10) **SECONDS/DIV**—Selects the sampling rate of the digitizing circuits, or in EXT position, selects EXT SEC/DIV input.

(11) **TRIG'D indicator**—Illuminates when the acquired[1] signal is triggered.

(12) **COUPLING**—Selects ac (button in) or dc (button out) coupling of triggering signals.

(13) **CAL**—Selects calibrated or uncalibrated sampling rates. Uncalibrated sampling rates can be continuously reduced to at least the next slowest rate.

(14) **INVERT**—Inverts the Channel 2 signal during acquisition. − symbol in crt readout indicates inverted setting. Triggering signal is not inverted.

(15) **VERT CTRG**—Screwdriver adjustment of the display vertically. (Compensates for mainframe offsets.)

(16) **SAVED DISPLAY OUTPUT** (SAVE depressed)—

PLOT—Pushing the Plot button causes the screen display to blank, and the display information to be output to the Saved Display Output connectors.

Output connectors—X and Y signal outputs at 0.2 v/div, 10 kΩ, mimic the crt display during Plot activity.

PENLIFT—Connectors provide normally open or normally closed connection for recorder pen control.

Jumper position selectable. Refer to "Setting the Penlift Polarity" at the end of this section.

(17) **Ground Connector**—Provides binding post for convenient chassis ground connections.

(18) **STORAGE**—

VIEWTIME—Controls the time the waveform is displayed before being erased and new data acquired[1] and displayed. Viewtime is variable from 1 second to infinity. Infinite viewtime provides single-shot trigger and save capability.

PUSH:ERASE—Push to erase the display before end of timer cycle without disturbing the setting of the viewtime control.

SAVE—Causes acquisition to stop. Memory contents are displayed with no further updating.

SAVE REFerence—Acquisition continues after SAVE REF is pressed. The data displayed prior to pressing SAVE REF is displayed with no further updating. All subsequent data is displayed then updated at the end of the VIEWTIME interval. The data last acquired before SAVE REF was pressed and the new acquired data are displayed simultaneously.

Acquisition continues, but half of memory contents are displayed with no further updating, and half continues being updated.

TRACE SEParation—Causes "reference" trace to be displayed downward 0.8 division for identification purposes. Active only if SAVE REF button is in.

(19) **POSSIBLE UNDERSAMPLING**—The indicator will be on if fewer than 8 samples are taken during each cycle of the triggering signal.

(20) **CURSORS**—(The following 4 functions described are inactive during signal acquisition).

C1/OFF/C2-C1

(1) C1—If selected, provides a single cursor with crt readout of value relative to center screen or ground reference information, or trigger point.

(2) C2-C1—If selected, 2 cursors with crt readout of difference values in time and amplitude are displayed. 1/ΔT crt readout is also displayed.

(3) OFF—No cursors. (SWP MGF is disabled)

SWP MGF (HORIZ POSN)—Magnifies y-t displays by X10, horizontally. Use C1 to select the portion of the waveform to be displayed.

<**C1**>—Moves cursor C1 along trace in direction toggle is pressed (either left or right).

<**C2**>—Moves cursor C2 along trace in direction toggle is pressed (either left or right).

(21) **EXTERNAL SEC/DIV**—Bnc connector for applying TTL clock signal to control sample rate.

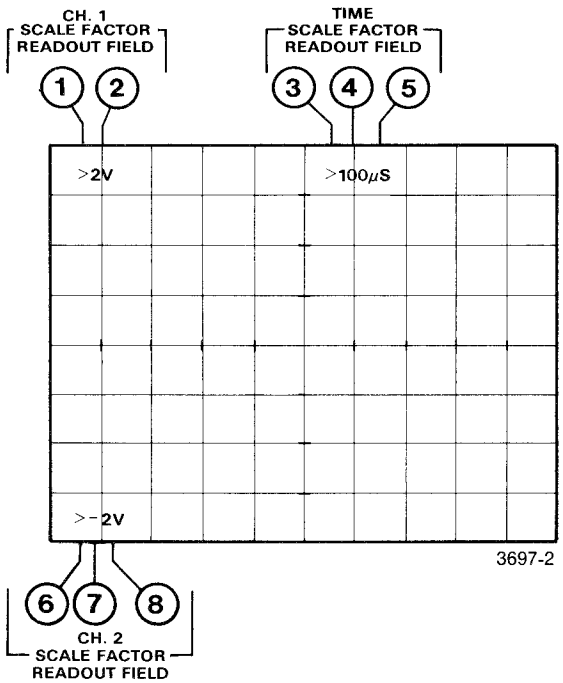
(22) **HORIZ CTRG**—Screwdriver adjustment of the display horizontal centering (compensates for mainframe offsets).

(23) **SOURCE**—Selects the source of the triggering signal:

CH 1	Channel 1 of the 5D10
CH 2	Channel 2 of the 5D10
LEFT PLUG-IN	via interface board in the mainframe
LINE	Power line frequency, from mainframe
EXT	External input, through bnc connector

[1]Acquired, is defined as: Sampled, digitized, and stored in memory.

Figure 2-1. Front panel controls and connectors (cont).



SCALE FACTOR READOUT FIELDS:

CH 1 Scale Factor Readout Field

NOTE

In addition to the conditions given after each value or symbol, the following condition will also apply:

The ACQUISITION AND DISPLAY switch is in CH 1, ADD, DUAL or XY.

(1) > is displayed when the CH 1 CAL knob is out of the CAL (detent) position.

(2) 2V is the present CH 1 VOLTS/DIV switch setting when both SAVE and SAVE REF buttons are out and a 1X probe is used. If a 10X probe is used, 20 V will be displayed.

Figure 2-2. Mainframe crt scale factor readout fields generated by the 5D10.

MAINFRAME CRT READOUT FIELDS

The 5D10 provides the readout information to the mainframe circuitry. The scale factor readout fields generated by the 5D10 are shown in Figure 2-2. The cursor readout fields generated by the 5D10 are shown in Figure 2-3. Each value or symbol in the illustrations are identified with a circled number. Following each illustration are definitions, numbered to coincide with those in the illustrations.

NOTE

The particular numbers relating to time and voltage in the following text and illustrations are used for explanation only.

Refer to Operation and Interaction of Save and Save Reference in the Detailed Operating Instructions following the Operators Checkout when SAVE or SAVE REF is mentioned in the following descriptions.

If SAVE has been pressed, the CH 1 VOLTS/DIV switch setting at the time SAVE was pressed is displayed. Any subsequent change of the VOLTS/DIV switch setting will not change the readout until SAVE is released, at which time the new VOLTS/DIV switch setting will be displayed.

If SAVE REF has been pressed (SAVE out), the VOLTS/DIV switch setting at the time SAVE/REF was pressed is displayed. The field will be blank in all other settings of the VOLTS/DIV switch.

Time Scale Factor Readout Field

NOTE

This field is blank in XY mode. Refer to number 14 for more information.

(3) > is displayed when the SECONDS/DIV switch is in the UNCAL position.

(4) 100μs (Scale Factor) displays:

a. The present SECONDS/DIV switch setting when both the SAVE and SAVE REF buttons are out.

b. EXT, if external sample is selected.

If SAVE has been pressed, the SECONDS/DIV setting at the time SAVE was pressed is displayed. Any subsequent change of the SECONDS/DIV switch setting will not change the readout until SAVE is released, at which time the new SECONDS/DIV switch setting will be displayed.

If SAVE REF has been pressed (SAVE out), the SECONDS/DIV switch setting at the time SAVE REF was pressed is displayed. The field will be blank for all other settings of the SECONDS/DIV switch.

(5) 10 μs is displayed if the SWP MFG switch is pressed in and CURSORS switch is not in the OFF position.

CH 2 Scale Factor Readout Field

NOTE

In addition to the conditions given after each value or symbol, the following condition will also apply:

The ACQUISITION AND DISPLAY switch is in CH 2, ADD, DUAL or XY.

(6) > is displayed when the CH 2 CAL knob is not in the CAL position.

(7) – is displayed if the INVERT button is pressed in.

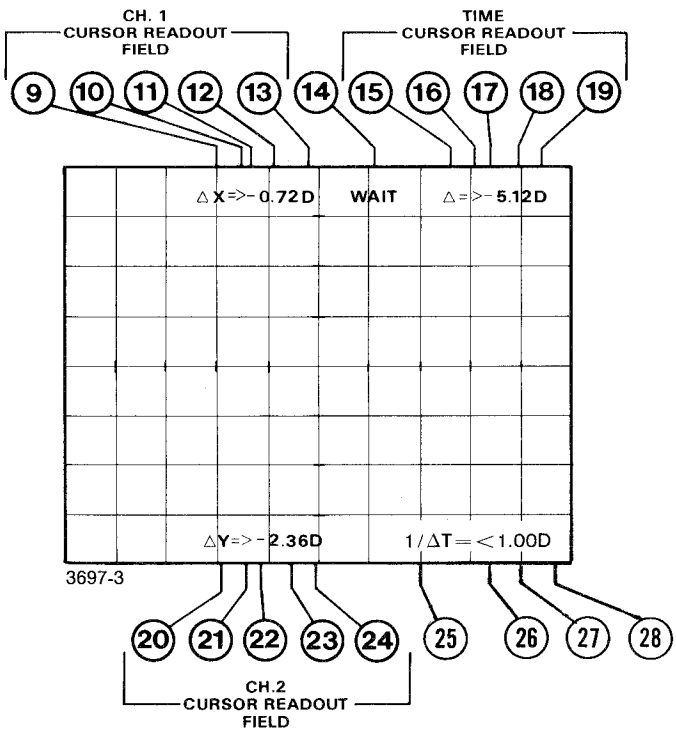
(8) 2V is the present CH 2 VOLTS/DIV switch setting when both SAVE and SAVE REF buttons are out and a 1X probe is used. If a 10X probe is used, 20 V will be displayed.

LEFT is displayed if the VOLTS/DIV switch is set to LEFT PLUG-IN.

If SAVE has been pressed, the CH 2 VOLTS/DIV switch setting at the time SAVE was pressed is displayed. Any subsequent change of the VOLTS/DIV switch setting will not change the readout until SAVE is released, at which time the new VOLTS/DIV switch setting will be displayed.

If SAVE REF has been pressed (SAVE out), the VOLTS/DIV switch setting at the time SAVE REF was pressed is displayed. The field will be blank for all other settings of the VOLTS/DIV switch.

Figure 2-2. Mainframe crt scale factor readout fields generated by the 5D10 (cont).



CURSOR READOUT FIELD

CH1 Cursor Readout Field

(9) ΔX= is displayed when X:CH1/Y:CH2 (ACQUISITION AND DISPLAY) is pressed and CURSORS switch is in C2-C1 position.
Δ= is displayed when CURSORS switch is in C2-C1 position.
X= is displayed when X:CH1/Y:CH2 (ACQUISITION AND DISPLAY) is pressed and CURSORS switch is in C1 position.

(10) > is displayed when a data point at which a cursor is to be displayed is off screen.

(11) - is displayed if the cursor value (see number 12) is below center screen or negative with respect to ground reference.

NOTE

See "Setting the Ground Reference" under Part II—Detailed Checkout Procedure later in this section.

(12) 0.72 (cursor value)

a. If CURSORS is in C1 position, the cursor value relative to ground reference or center screen is displayed.
b. If CURSORS is in C2-C1 position, the cursor value of C2-C1 is displayed.
c. In ADD mode, the cursor value relative to the ground reference of the added channels is displayed, or D (divisions) is displayed if ground reference is not acquired.

Figure 2-3. Mainframe crt cursor readout fields generated by the 5D10.

(13) D (Divisions) is displayed when:

a. The CH 1 ground reference has not been set since power up or the last scale factor change.
b. The CAL knob is not in CAL position.
c. Both LEFT PLUG-IN and ADD have been selected.
d. ADD is selected and CH 1 and CH 2 VOLTS/DIV switch settings are different.

V (Volts) is displayed when a ground reference is set with cursor C1 on; also, the difference V is displayed when cursors C2-C1 are on.

(14) WAIT is displayed after SAVE or SAVE REF has been pressed and until acquisition stops. Visible only at slow SECONDS/DIV switch settings. An ERASE will occur if any controls are switched during WAIT.

Time Cursor Readout Field

(15) △= is displayed when CURSORS is in C2-C1 position.

(16) > is displayed when a cursor is displayed greater than +500 points from center screen.

(17) – is displayed (CURSORS in C1 position) when the data point at which the cursor is displayed is prior to the selected TRIGGERING point (POST TRIG, CTR TRIG, PRE TRIG), or if cursor C2 is earlier than C1 (CURSORS in C2-C1 position).

(18) 5.12 (cursor value)

a. If CURSORS is in C1 position, the cursor value relative to the trigger point is displayed.
b. If CURSORS is in C2-C1 position, the cursor value of C2-C1 is displayed.

(19) D (Divisions) is displayed when (1) the SECONDS/DIV CAL knob is not in the CAL (detent) position (2) the SECONDS/DIV switch is in EXT otherwise μS, mS or S will be displayed. See number 18.

CH 2 Cursor Readout Field

NOTE

The CH 2 Cursor Readout Field is blank when in the ADD mode.

(20) △Y= is displayed when X:CH1/Y:CH2 (ACQUISITION AND DISPLAY) is pressed and CURSORS switch is in C2-C1 position.

△= is displayed when CURSORS switch is in the C2-C1 position.

Y= is displayed when X:CH1/Y:CH2 (ACQUISITION AND DISPLAY) is pressed and CURSORS switch is in C1 position.

(21) > is displayed when a data point at which a cursor is to be displayed is off screen.

(22) – is displayed if the cursor value is below center screen or negative with respect to ground reference.

NOTE

See "Setting the Ground Reference" under Part II—Detailed Checkout Procedure later in this section.

(23) 2.36 (cursor value)

a. If CURSORS is in C1 position, the cursor value relative to ground reference or center screen is displayed.
b. If CURSORS is in C2-C1 position, the cursor value of C2-C1 is displayed.

(24) D (Divisions) is displayed when:

a. CH 2 ground reference has not been set since power up or the last scale factor change.
b. CAL knob not in CAL position.
c. Left plug-in has been selected.

V (Volts) is displayed when ground reference is set with cursor C1 on; also, the difference V is displayed when cursors C2-C1 are on.

(25) 1/ΔT readout field is displayed when in C1-C2 CURSORS mode.

(26) < is displayed when the left cursor is off screen on the left edge.

(27) 1.00 (frequency value) is displayed when CURSORS is in C1-C2 position.

(28) D (divisions) or mD (millidivisions) is displayed when (1) the SECONDS/DIV CAL knob is not in the CAL (detent) position (2) the SECONDS/DIV switch is set to EXT; otherwise, the display will be in Hz, kHz, or MHz.

NOTE

This field value will always be positive, even when the cursors are reversed.

Figure 2-3. Mainframe crt cursor readout fields generated by the 5D10 (cont).

OPERATORS CHECKOUT

The Operators Checkout procedures are provided for familiarization with the 5D10 and for checking basic instrument functions. The Operators Checkout is divided into two parts: Part I—Get Acquainted Exercise, and Part II—Detailed Checkout Procedure.

Part I—Get Acquainted Exercise is provided primarily for first time operation. The Get Acquainted Exercise leads the first time user through the basic 5D10 operating functions.

Part II—Detailed Checkout Procedure is provided for a detailed demonstration of 5D10 capabilities and to check instrument functions.

Refer to the description of the controls, connectors, and indicators given earlier in this section while performing these procedures. If performing the Part II—Detailed Checkout Procedure reveals a malfunction or possible maladjustment, refer to the service manuals for maintenance and adjustment procedures.

POWER-UP SEQUENCE

The Power-Up Sequence must be performed prior to the Part I—Get Acquainted exercise or Part II—Detailed Checkout Procedure. The Power-Up Sequence lists the equipment required and provides the preliminary steps necessary to perform either procedure.

EQUIPMENT REQUIRED

The following test equipment is recommended for the Operators Checkout procedures. Other test equipment which meets these requirements may be substituted. When other equipment is substituted, the control settings or setup may need to be altered.

1. Oscilloscope

   Type Used: TEKTRONIX 5110 Oscilloscope. See Mainframe and Plug-In Compatibility considerations in Section 1, General Information.

2. Function Generator

   Description: Frequency range 1 Hz to 10 kHz; output amplitude, 15V p-p into 50 Ω.

   Type Used: TEKTRONIX FG501A, 2 MHz Function Generator (used with TM501 Power Module).

3. Amplifier Plug-In Unit

   Description: Two independent differential amplifiers in one plug-in, compatible with the Tektronix 5000-series Oscilloscope Mainframes.

   Type Used: TEKTRONIX 5A26 Dual Differential Amplifier.

4. Cables (2 Required)

   Description: Length 42 inches; connectors, bnc.

   Type Used: Type RG-58/U, 50-Ω coaxial, Tektronix Part 012-0057-01.

5. T-Connector

   Description: Connectors, bnc-to-bnc.

   Type Used: Bnc-to-bnc connectors, Tektronix Part 103-0030-00.

6. Terminator

   Description: Connector, bnc female to bnc male.

   Type Used: 50 Ω, 2W, Tektronix Part 011-0049-01.

7. Probe

   Description: Input resistance 10 MΩ, compensation 47 pF, connector, bnc.

   Type Used: TEKTRONIX P6062B passive dual attenuation probe, Part 010-6062-13.

POWER UP SELF-TEST

1. Install the 5D10 Waveform Digitizer in the right vertical and horizontal compartments of the oscilloscope mainframe.

2. Press SAVE, then turn on the oscilloscope mainframe power.

3. Set the oscilloscope mainframe Intensity control to midrange.

The 5D10 Waveform Digitizer automatically performs a Self-Test each time power is applied to the instrument. At power-on, a reset signal is generated internally which initiates the running of a series of internal routines. These routines verify the proper operation of the waveform memory system and associated hardware. See "Self-Test Routine Modes" below, to verify which routine your 5D10 is exercising.

If the 5D10 passes the self-test and, if either or both SAVE or SAVE REF button(s) are in, the crt of the

mainframe in which the 5D10 is installed will display a graticule, and, in the upper left corner, display 5D10 READY'. See Figure 2-4. If neither SAVE nor SAVE REF has been pressed, the 5D10 will function in the normal fashion.

If an error is encountered an error message may be displayed on the crt.

The operator may ignore the error and attempt to continue normal operation by releasing the SAVE button or pressing, then releasing, the SAVE button if the SAVE button was not pressed in initially.

NOTE

Accuracy of measurements is not guaranteed if an error message is ignored.

Self-Test Routine Modes

The 5D10 may be set to any one of three basic self-test routine modes by position selection of the internal Link-Plugs (jumpers). Refer to Section 4, Maintenance, in this manual, and to the 5D10 Diagnostic Troubleshooting Service Manual (Volume 2) for additional information.

The three basic self-test routines can be identified (at power-up and with the SAVE button in) as follows:

1. Normal Mode—A condition report will be displayed at the top of the screen (i.e., "5D10 READY," or "ERROR"). The Normal Mode routine is exercised each time the 5D10 is powered-up, and is utilized as a "normal operating function" of the 5D10.

2. Report Mode—A condition report will be displayed on the screen as follows:

   a. If all self-tests pass, "5D10 READY" will be displayed at the top of the screen, and the firmware version (i.e., "VER 10") will be displayed at the bottom of the screen.

   b. If any test fails, all operation halts. To continue the tests, press the PUSH:ERASE button; this will allow the tests to either achieve completion, or halt at the next failure. When all tests have been completed a condition report will be displayed (i.e., "5D10 ERROR", with the numbers of each test failure at the top of the screen, and the firmware version at the bottom of the screen).

   The Report Mode is used only for troubleshooting. Refer to the 5D10 Diagnostic Troubleshooting Service Manual, Volume 2.

3. Cycle Mode—A condition report will be displayed on the screen at the conclusion of the self-test routine. After about ten seconds the processor will repeat the self-test routine and condition report display. The Cycle Mode is used for factory testing only and has no practical use for the field technician.

VERTICAL AND HORIZONTAL CENTERING

Minor correction in the vertical and horizontal centering of the display is accomplished with the VERT CTRG and HORIZ CTRG front-panel screwdriver adjustments.

Proceed with the following instructions:

1. Adjust mainframe Intensity and Focus for a well-defined display.

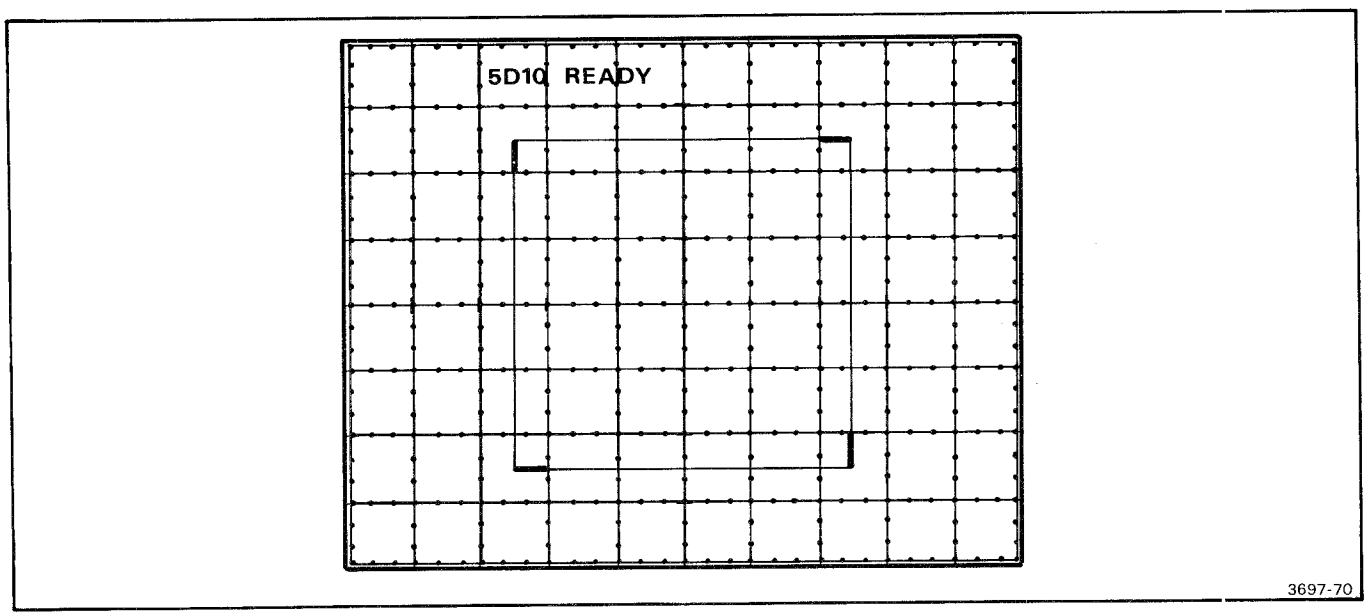


Figure 2-4. Power-up self-test display graticules (passed message shown).

2. Adjust HORIZ CTRG so the 2nd and 10th displayed vertical graticule lines match the 2nd and 10th crt graticule lines.

3. Adjust VERT CTRG so the 2nd and 8th display horizontal graticule lines match the 2nd and 8th crt graticule lines.

4. Observe that the dots and vectors match, and that the corners of the box pattern are in line. Refer to Figure 2-4.

NOTE

If the horizontal and vertical display requirements cannot be met using the front-panel adjustments, refer to Section 4, Maintenance, and to Section 5, Calibration.

The instrument can be used; however, measurement accuracy and full function capability is not guaranteed.

OPERATORS CHECKOUT SETUP

The Operators Checkout Setup must be completed prior to performing either the Part I—Get Acquainted Exercise or the Part II—Detailed Checkout Procedure.

1. Set the 5D10 controls as follows:

TRIGGERING
- POSITION ..... CTR TRIG
- SLOPE ..... ⌡ (+ slope)
- LEVEL ..... Midrange
- COUPLING ..... DC
- SOURCE ..... CH 1

SECONDS/DIV ..... 0.1 m
- CAL ..... Fully clockwise (in detent)

CURSORS ..... OFF
- SWP MGF ..... Off (button out)

VOLTS/DIV (CH 1) 0.5

STORAGE
- VIEWTIME ... MIN (fully counterclockwise)
- SAVE ..... Off (button out)
- SAVE REF ..... Off (button out)

Input Coupling (CH 1) ..... DC (button out)
- GND ..... button out

ACQUISITION AND DISPLAY
- CH 1 ..... On (button in)
- JOIN DOTS ..... On (button in)

SAVED DISPLAY OUTPUT
- PLOT ..... Off (button out)

2. Turn on the function generator.

3. Adjust the intensity and focus for a well-defined display. See the oscilloscope mainframe instruction manual for detailed operating instructions.

Proceed to Part I—Get Acquainted Exercise or Part II—Detailed Checkout Procedure.

PART I—GET ACQUAINTED EXERCISE

The Part I—Get Acquainted Exercise is provided primarily for first time operation. The exercise leads the first time user through the basic operation of the 5D10. Refer to Part II—Detailed Checkout Procedure for a detailed demonstration of 5D10 capabilities and to check for correct operation of instrument functions.

1. ACQUIRING A SIGNAL

Once a signal has been acquired (that is sampled, digitized, and stored into memory) and displayed on the crt, the 5D10 has the information necessary to perform selected functions as determined by front-panel control settings. Such features include scale factor readout (signal acquisition not required for scale-factor readout), stored displays on the crt, point-to-point cursor measurements with values displayed on crt readout, etc.

SETUP Perform the Operators Checkout Power-Up Sequence.

Set the 5D10 controls as follows:

TRIGGERING POSITION ... FREE RUN
- SECONDS/DIV 0.2
- POS ..... Vertically Centered

Connect an approximate 1-volt (2 divisions) 5-hertz sine-wave signal from the function generator to the 5D10 CH 1 input with a coaxial cable and 50-ohm termination.

OBSERVE 500 mV readout corresponding to the 0.5 CH 1 VOLTS/DIV setting.

200 ms readout corresponding to the 0.2 SECONDS/DIV setting.

SETUP Vary the function generator amplitude.

OBSERVE The acquired display moves from right to left with the most recently acquired data at the right of the crt display.

2. SELECTING THE TRIGGERING POSITION

The TRIGGERING POSITION buttons provide three choices to select the triggering position on the displayed waveform. (1) In the PRE TRIG position the display occurs before the triggering event. (2) In the CTR TRIG position one-half the display occurs before the triggering event and one-half the display occurs after the triggering event. (3) In the POST TRIG position the display occurs after the triggering event. An intensified dot on the displayed waveform denotes the triggering point.

SETUP Set the function generator amplitude for a two-division display.

Set the 5D10 controls as follows:

POS ..... Vertically centered on crt
SECONDS/DIV ..... 10 m
VIEWTIME ..... Midrange
TRIGGERING
POSITION ..... CTR TRIG
LEVEL ..... TRIG'D light on

OBSERVE Triggered sine-wave display with an intensified dot (trigger point) near crt center. The display to the left of the trigger point is acquired before the triggering event and the display to the right of the trigger point is acquired after the triggering event.

SETUP Set the TRIGGERING POSITION to PRETRIG.

OBSERVE The intensified dot (trigger point) is displayed at the right side of display area. The display to the left of the trigger point is acquired before the triggering event. Pretrigger is unique to digital storage.

SETUP Set the TRIGGERING POSITION to POST TRIG.

OBSERVE The intensified dot (trigger point) is displayed at left side of the display area. The display to the right of the trigger point is acquired after the triggering event. Post Trigger is common to conventional oscilloscope triggering.

3. STORING A WAVEFORM

After signals have been stored into memory, the display may be stored on the crt display by simply pressing the SAVE button. When the SAVE button is released the crt is blanked and a new signal is acquired and displayed for a time determined by the VIEWTIME control.

SETUP Press SAVE (button in).

OBSERVE The 5-hertz signal is now stored on the crt.

4. USING DISPLAY CURSORS

Cursors are provided for waveforms stored on the crt (SAVE mode) to delimit or identify portions of the waveform to be measured. The cursors can be positioned to the desired points on the display by use of the appropriate front-panel controls. The cursor values are displayed on the crt readout.

SETUP Set the 5D10 controls as follows:

TRIGGERING POSITION .... CTR TRIG
CURSORS C2-C1
SECONDS/DIV ..... 1 m
SAVE ..... Off (button out)
VIEWTIME ..... MIN

Set the function generator for a 2 division 1 kHz output.

Press SAVE (button in).

OBSERVE The 1 ms display is now stored on crt.

SETUP Press C1 cursor motion switch to the left and then to the right.

OBSERVE The cursor moves on displayed waveform to the left and right respectively.

SETUP Move Cursors C1 and C2 to be approximately 4 divisions horizontally apart.

OBSERVE △ time readout of approximately △ = 4.00 mS (1 ms SECONDS/DIV setting times approximately 4 horizontal divisions between cursors results in delta time of approximately 4.00 mS).

SETUP Set the function generator for square-wave output.

Release SAVE (button out) so that the square-wave signal may be acquired.

Set the SECONDS/DIV to 0.2 m.

Press SAVE (button in) to store the square wave.

Position Cursor C1 to the bottom of the square wave and move Cursor C2 to the top of the square wave.

OBSERVE Channel 1 cursor field readout for delta volts readout of approximately △ 1.00 V (0.5 CH 1 VOLTS/DIV setting times the approximate 2 division vertical step of the square-wave signal results in delta volts reading of approximately 1 volt).

SETUP Set CURSORS to C1.

Ensure that the TRIGGERING POSITION is set to CTR TRIG.

Position cursor C1 to the intensified dot at the trigger point.

OBSERVE The delta time readout has been replaced with a readout display of approximately 0 μs. With CURSORS switch in C1 position, the readout corresponds to the time between cursor C1 and the trigger point.

SETUP Move cursor C1 to the left of the trigger point.

OBSERVE The time-cursor readout increases in the negative direction (e.g., −122 μs).

SETUP Move cursor C1 to the right of the trigger point.

OBSERVE The time-cursor readout increases in the positive direction (e.g., 136 μs).

5. OBTAINING A SAVE REFERENCE DISPLAY

The SAVE REF function allows comparison of two traces. A stored display from previously acquired data can be compared to the information presently being acquired and displayed (the display time of the new data is determined by the setting of the VIEWTIME control).

SETUP Set the 5D10 controls as follows:

SAVE..... Off (button out)
SECONDS/DIV..... 5 m (Allow 1 ms signal to be acquired)
SAVE REF.....On (button in)
TRACE SEP.....On (button in)
SECONDS/DIV.....0.5 m

OBSERVE The 1 ms reference display is stored on the crt and a new acquired signal is displayed (approximately 1 cycle in 2 divisions).

6. SETTING GROUND REFERENCE

When making voltage measurements in the C1 CURSORS switch position all cursor measurements are relative to the ground reference. The ground reference may be set at any point within five divisions of the center horizontal graticule line. Or, if the ground reference is not set, it will default to the center horizontal graticule line.

SETUP Set the 5D10 controls as follows:

SECONDS/DIV.....0.2 m
SAVE REF..... Off (button out)
TRACE SEP..... Off (button out)

Increase the function generator amplitude for a 4-division display vertically centered on the crt.

Engage the SAVE button to store the display on the crt.

Move cursor C1 to the top of square-wave step.

OBSERVE The channel 1 cursor field readout of approximately 2.00D (divisions) relating to 2 divisions from center screen. When the ground reference has not been set, the CH 1 cursor field readout is measured from crt center in divisions.

SETUP Set 5D10 controls as follows:

CH 1 input coupling . GND (button in)
SAVE..... Off (button out)

Position the horizontal trace to 1 division above crt center.

Set the 5D10 controls as follows:

ERASE ..... Press and release
CH 1 input coupling ..... GND off (button out)
SAVE.....On (button in)

OBSERVE The CH 1 cursor field readout has changed to volts with an approximated reading of 1.00 V. The 1-volt reading corresponds to 2 divisions above ground reference at 0.5 VOLTS/DIV.

This ends the 5D10 short form Part I—Get Acquainted Exercise. If a more detailed exercise of the 5D10 features is desired, continue with Part II—Detailed Checkout Procedure.

PART II—DETAILED CHECKOUT PROCEDURE

The Part II—Detailed Checkout Procedure provides a systematic demonstration of all the front panel controls. Further information about certain controls can be found in the Detailed Operating instructions that follow. Refer to Figure 2-1, front-panel Controls, Connectors and Indicators given earlier in this section while performing this procedure for additional information.

If performing this checkout procedure reveals a malfunction or possible maladjustment, refer to the Maintenance and Calibration sections of this manual.

SETUP

To begin with Part II—Detailed Checkout Procedure, first perform the Power-Up Sequence. Then proceed to Setting the Ground Reference procedure, which follows.

To proceed from Part I—Get Acquainted Exercise perform the Operators Checkout control settings (part of Operators Checkout Power-Up Sequence) then proceed to Setting the Ground Reference procedure.

Setting the Ground Reference

When making voltage measurements with the CURSORS switch in the C1 position, voltage readouts are relative to ground reference, providing the ground reference has been set.

NOTE

At power up, the readout is calibrated in divisions (D) with the center graticule line the zero level (reference).

The following procedure should be used when setting the ground reference:

1. Press GND of the appropriate channel (CH 1 or CH 2).

NOTE

The ADD mode requires both GND pushbuttons pressed in and the same VOLTS/DIV switch settings.

2. Press FREE RUN, then adjust the trace(s) to the desired position.

3. Press PUSH: ERASE button then release the GND pushbutton.

4. The ground reference has now been stored in memory.

GND reference values become invalid and need to be re-acquired for the following conditions:

- CH 1 or CH 2 VOLTS/DIV switch setting is changed (affects only that channel's GND reference; however, in ADD mode a change in either will cause both to be lost).

- The CH 1 or CH 2 CAL knob is changed to or from the CAL position (affects only that channel's GND reference; however, in ADD mode a change in either will cause both to be lost).

- The CH 2 INVERT switch is changed to or from the INVERT position (affects only CH 2 GND reference; however, in ADD mode a change in the INVERT switch setting will cause both to be lost).

- ADD (ACQUISITION AND DISPLAY) is selected or deselected (affects both channel 1 and channel 2 ground references).

Adjustment of the POSition knob will affect the cursor values relative to the GND reference, so a new ground reference should be acquired after each position adjustment.

NOTE

The 5D10 will not acquire a ground reference more than ±5 divisions from center screen.

The readout will display [D]ivisions rather than [V]olts if the ground reference is invalid.

Sweep Functions

NORMAL SWEEP

Perform the following procedure to obtain a normal sweep and to demonstrate the function of the related controls:

1. Connect a 1-volt, 1-kilohertz (approximately) signal from the function generator to the CH 1 input. Rotate the amplitude control of the function generator until a two-division signal is displayed. Set TRIGGERING POSITION to CTR TRIG.

2. Adjust the LEVEL/SENSITIVITY control for a triggered display.

3. Rotate the VIEWTIME control slowly in the clockwise direction. Notice the time is increased between erase operations (blank screen). The VIEWTIME controls the time the waveform is displayed before being erased and new data acquired and displayed.

4. Press PUSH:ERASE. Notice the display is blanked then new data acquired and displayed without changing the VIEWTIME setting.

5. Rotate VIEWTIME to MIN (fully counterclockwise), and check that the SWP MGF button is released (out).

6. Press each POSITION (TRIGGERING) control in turn (POST TRIG, CTR TRIG, PRE TRIG). Notice the trigger indicator "dot" jumps to the left of center screen approximately 4 divisions, to center screen, then, approximately 4 divisions to the right of center screen.

7. Switch SECONDS/DIV to 0.1 and disconnect the function generator.

8. Rotate the CH 1 POSition control and observe that the trace moves vertically. The most recently acquired data is displayed at the right most point on the crt display.

9. Connect a 10 hertz signal from the function generator to the CH 1 input. Press CTR TRIG. Turn the CAL control fully counterclockwise and observe that the displayed waveform sweep rate is continuously variable between SECONDS/DIV switch settings. Turn the CAL knob to the calibrated (detent) position.

Return the function generator output frequency to 1 kHz.

NOTE

The symbol > (greater than) in the readout indicates uncalibrated settings.

EXTERNAL SWEEP

10. Disconnect the 1 kHz signal from CH 1 input and connect it to the EXTERNAL SEC/DIV input connector.
11. Switch SECONDS/DIV to EXT (fully counterclockwise).
12. Connect a probe (see Equipment Required list) to the CH 1 input and to the mainframe calibrator loop.
13. If acquisition does not occur:
    a. Increase the amplitude of the Function Generator, and/or
    b. Add a DC offset to the output of the generator, so that the output swings between ground (0 volts) and a more-positive voltage.

NOTE

The EXTERNAL SEC/DIV is compatible with TTL voltage levels.

CAUTION

Do not apply more than +5 volts (dc plus peak ac) to the EXTERNAL SEC/DIV input.

14. Rotate the frequency multiplier of the function generator. Observe than an external signal will control the sample rate.

POSSIBLE UNDERSAMPLING INDICATOR

15. Disconnect the probe from the calibrator loop and the CH 1 input connector.
16. Disconnect the signal to the EXTERNAL SEC/DIV input and connect it to the CH 1 input.
17. Switch SECONDS/DIV to 0.1 m.
18. Provide a 1 kHz, 1 volt signal from the function generator.
19. Turn the SECONDS/DIV control counterclockwise 1 step at a time. Notice that when the switch is in the 20 m and slower positions the POSSIBLE UNDERSAMPLING indicator lights (red indicator). The POSSIBLE UNDERSAMPLING indicator shows that the system is taking two few samples to accurately reconstitute the input signal.

MAGNIFIED HORIZONTAL SWEEP (SWP MGF)

20. Switch SECONDS/DIV to 1 m.
21. Switch CURSORS to the C1 position.
22. Press SAVE, then press the SWP MGF button (button in). Observe that approximately 1 cycle is magnified to about 10 divisions.

    The part of the unmagnified display that will be enlarged is that portion immediately preceding (1/8) and following (7/8) the position of cursor C1. Refer to Figure 2-5.

    Once SWP MGF is pressed, moving C1 in the desired direction will allow the operator to control the portion of the original waveform that is displayed.

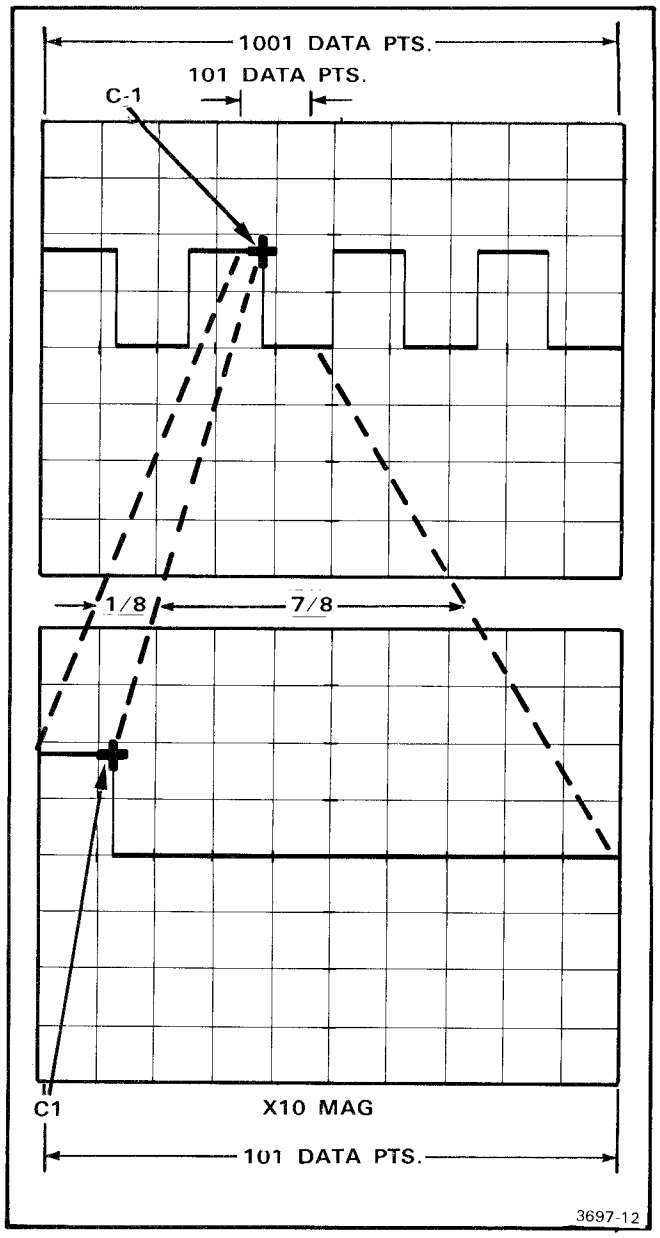


Figure 2-5. Sweep magnify.

The readout will reflect the new scale factor (SECONDS/DIV setting ÷ 10).

NOTE

When the CURSORS switch is set to C2-C1 and SECONDS/DIV is not in the CAL setting, the ΔT readout will be measured in [D]ivisions not [S]econds. Sine ΔT is now measured in [D]ivisions, the 1/ΔT also shows a measurement in [D]ivisions. When SWP MAG is pressed the 1/ΔT measurement is not recalculated since, of course, the measurement in [D]ivisions from the ΔT is not a valid calculation.

23. Press SWP MGF (button out) and switch CURSORS to OFF.

Readout

SCALE FACTOR SETTINGS

24. Rotate the CH 1 VOLTS/DIV switch throughout its range.

a. Notice the CH 1 scale factor readout (500 mV) remains unchanged, because the SAVE function is engaged.

25. Release SAVE, then press SAVE REF. Press TRACE SEP button in.

a. Notice while rotating the SECONDS/DIV control that the SECONDS/DIV readout display occurs only when the stored time and new time are the same, otherwise the SECONDS/DIV readout is blanked.

b. Notice that the display continues to update, (unlike pressing the SAVE button) over the reference waveform.

c. Notice that the repetition rate of the new trace changes as the SECONDS/DIV switch is rotated, while the reference waveform remains unchanged.

26. Release, then press SAVE REF; the reference waveform will update to the new SECONDS/DIV setting. Release SAVE REF.

27. Set the ACQUISITION AND DISPLAY to CH 2, then set the CH2 VOLTS/DIV to LEFT PLUG-IN.

a. Notice that the readout at the bottom left corner of the screen displays LEFT (the left plug-in unit is not installed at this time).

b. Set the CH 2 VOLTS/DIV to 0.5 and return the ACQUISITION AND DISPLAY to CH 1.

Triggering Functions

Perform the following procedure to obtain a triggered display and to demonstrate the functions of the related controls:

INTERNAL TRIGGERING

28. Return the SECONDS/DIV switch to 1 m and VOLTS/DIV to 0.5.

29. Turn the LEVEL/SENSITIVITY control to obtain a freerunning (not triggered) display. Then set the LEVEL/SENSITIVITY control for a stable display (TRIG'D light on).

30. Press the AC and DC COUPLING button for both the + and − positions of the SLOPE switch and check for a triggered display. The LEVEL/SENSITIVITY control may be adjusted to obtain a triggered display (TRIG'D light on).

31. Press FREE RUN. Observe that the display is freerunning (not triggered) and the TRIG'D light remains on. Press CTR TRIG.

EXTERNAL TRIGGERING

32. Apply a 1-volt, 1-kilohertz signal from the Function Generator to the EXTernal SOURCE connector.

33. Press in the EXT (TRIGGERING SOURCE) button.

34. Set the SLOPE control to BISLOPE (both SLOPE buttons in). Turn the LEVEL/SENSITIVITY control to the MAXimum position (fully counterclockwise). Observe that the signal is triggered.

35. Turn the LEVEL/SENSITIVITY control towards the MINimum position (clockwise).

Observe that the display becomes untriggered and is freerunning. The adjustment between this point and maximum is the sensitivity threshold "window" of the BISLOPE mode.

36. Adjust the LEVEL/SENSITIVITY control for a triggered display and press the STORAGE VIEWTIME (PUSH:ERASE) button. Note that the trace disappears when the button is depressed and reappears when it is released, (updated with the latest points in memory.)

37. Press CH 1 (TRIGGERING SOURCE) and disconnect the external triggering signal.

NOTE

For more information, see Triggering in Detailed Operating Instructions.

38. Connect the 1-volt, 1-kilohertz signal from the function generator to the CH 1 input connector.

Cursors

YT MODE

39. Press SAVE (button in) then switch CURSORS to C1 position.

40. Notice that cursor C1 is displayed on the waveform.

NOTE

Cursors are normally displayed as a +.

If a data point at which a cursor is to be displayed is off screen horizontally the cursor is displayed as a horizontal bar. If a data point at which a cursor is to be displayed is offscreen vertically the cursor is displayed as a vertical bar.

If both cases are true, then an intensified dot is displayed. When the cursor is displayed as something other than a + (dot, vertical or horizontal bar) then the cursor field readout will display a > symbol.

When <C1> is activated, C1 will move 1 data point in the indicated direction. Notice that the rate increases as the switch is held in position.

41. Move the cursor to the left-most graticule position. Notice the cursor appears as a horizontal bar.

43. Move the cursor C1 one graticule division from the left. Using C2 cursor motion switch, move C2 to the left. Notice that C2 will not move past C1. Move C1 to the right. Notice the C1 cursor will move C2. Notice also that when the cursors are coincident, the 1/ΔT readout is blanked.

44. Place cursors C1 and C2 one cycle apart on the center horizontal graticule line. Notice that when Δ=1.00 mS (approx) that Δ=0.00 V (approx) and 1/ΔT=1.00 kHz (approx).

45. Move cursor C1 to the bottom of the waveform. Notice the readout Δ = 0.50 V (500 mV/div).

46. Release SAVE (button out).

XY MODE

Connect a T-connector (bnc) to the output of the Function Generator, and connect the output to both CH 1 and CH 2 inputs (5D10). Set the output to a sine wave of approximately 10 Hz. (Ensure there is no dc offset on the generator output).

47. Set CH 1 and CH 2 VOLTS/DIV to 0.5. Set CH 1 and CH 2 coupling to DC (buttons out).

48. Switch SECONDS/DIV to 50 m, then adjust the amplitude of the Function Generator for a 2 division display.

49. Center the display vertically.

50. Press CH 2 (ACQUISITION AND DISPLAY), then center the display vertically.

51. Press X:CH 1/Y:CH 2. Observe the vector at approximately 45°.

52. Press CH 2 AC/DC (input coupling) to AC (button in).

53. Observe the oval XY display. (If the output of the Function Generator has a dc offset, switching from AC to DC will shift the XY display). Press SAVE. Switch CURSORS to C2-C1. Notice that C1 and C2 move the length of the vector and that C2 will not stop at C1; also C1 will not move C2 as in YT mode.

54. Release SAVE.

NOTE

1/ΔT readout is blanked when in XY mode.

Refer to Phase Measurements in Operators Manual, Section 3, Applications, for more information about the XY mode.

Obtaining a Multiple Trace Display

Perform the following procedure to demonstrate dual trace displays, and use of the Left Plug-In.

NOTE

The maximum frequency that can be reconstructed accurately is limited by the number of traces to be displayed at any one time. Refer to Table 2-2, Measurement Frequency Limitations, at the end of this section.

TWO-TRACE DISPLAY (DUAL MODE)

55. Perform the "Operators Checkout Setup" given at the beginning of the Operators Checkout Procedure.

56. Set the function generator to display 2 divisions of amplitude at a frequency of 1 kHz.

57. Set the SECONDS/DIV to 1 m, and position the CH 1 display to the top half of the graticule.

58. Set the ACQUISITION AND DISPLAY to CH 2, and the CH 2 VOLTS/DIV to 1. Position the CH 2 display to the bottom-half of the graticule.

59. Set the ACQUISITION AND DISPLAY to DUAL. Notice that the Channel 1 and Channel 2 signals are displayed simultaneously.

60. Press SAVE (button in) and set the CURSORS to C1.

    a. Notice that cursor C1 is displayed on both the Channel 1 and Channel 2 traces at the same horizontal point.

    b. Notice that the cursor voltage readout is displayed at the top of the screen for Channel 1, and at the bottom of the screen for Channel 2.

61. Move cursor C1 across the display area.

    a. Notice that the cursor time readout (refer to Fig. 2-3) corresponds to the time (+ or −) from the trigger point (intensified dot).

    b. Notice the cursor voltage readout (refer back to Fig. 2-3) for both Channel 1 (top) and Channel 2 (bottom) with respect to the ground reference.

NOTE

When the ground reference has not been set, the cursor voltage readout for both Channel 1 (top) and Channel 2 (bottom) is the distance in divisions, from the crt vertical center.

The ground reference can be set individually for Channel 1 and Channel 2, (see Setting the Ground Reference, at the beginning of the Detailed Checkout Procedure). When the ground reference has been set, the cursor voltage readout will correspond to the voltage difference between the cursor and the appropriate ground reference, (i.e., 0.72 V).

62. Set CURSORS to C2-C1. Position cursors C1 and C2 approximately 3.5 divisions apart.

    a. Notice that cursors C1 and C2 are displayed at the same horizontal points on their respective waveforms.
    b. Notice that the cursor time readout corresponds to the time difference between cursors C1 and C2 (e.g., 3.5 divisions between cursors and a SECONDS/DIV setting of 1 m corresponds to a cursor time readout of Δ=3.50 mS). (The correct frequency is displayed on the 1/ΔT readout when the cursors are placed one cycle apart).
    c. Notice that the cursor voltage readout for Channel 1 is displayed at the top of the screen, and Channel 2 is displayed at the bottom. The cursor voltage readout is the algebraic difference between cursors C1 and C2 (i.e., Δ = −1.16 V). Release SAVE (button out).

63. Set CURSORS to OFF. Press the SAVE REF button in, then press the TRACE SEP button in. Set the CH 1 VOLTS/DIV to 1, the CH 2 VOLTS/DIV to 2, and the SECONDS/DIV to 2 m.

    a. Notice that the scale readouts for time and voltage are blanked. When the scale factors for the reference displays and the new displays differ, neither scale factor is displayed.

    b. Set CURSORS to C2-C1 and position the cursors on the reference trace. Notice that the cursor voltage and cursor time readout displays correspond to the reference (saved) display.

    c. Press SAVE (button in). Move the Cursor motion switches to alternate the cursors between the new and reference displays.

    d. Notice that the scale-factor readout reflects the appropriate VOLTS/DIV settings as the cursors are moved between the new and reference displays.

TWO-TRACE DISPLAY (LEFT PLUG-IN MODE)

64. Turn oscilloscope mainframe power off.

65. Install an amplifier plug-in unit in the left vertical compartment of the oscilloscope mainframe. (Refer to Amplifier Unit Manual for operating instructions.)

NOTE

Refer to Mainframe Compatibility and Plug-In Compatibility in Section 1, General Information, before using the 5D10 Left Plug-In mode.

66. Turn on oscilloscope mainframe power.

67. Release the SAVE, SAVE REF and TRACE SEP buttons (out), set ACQUISITION AND DISPLAY to CH 2, set CH 2 VOLTS/DIV to 20, and push CH 2 GND.

68. Center the trace with the CH 2 POSition control. Do not disturb this section throughout the remainder of the "Two Trace Display" procedure.

69. Switch CH 2 VOLTS/DIV to LEFT PLUG-IN. Notice that LEFT is displayed in the scale factor readout position on the screen. Set the amplifier unit controls (dual amplifier unit installed in the left vertical compartment) for a Channel 1 display.

70. Vertically position the left plug-in trace (with its Ch 1 Position control) to the bottom-half of the screen. Set the left plug-in CH 1/Volts/Division to 2 volts.

71. Move the 1 kHz signal from the 5D10 CH 2 input connector to the CH 1 input of the left plug-in unit.

72. Set ACQUISITION AND DISPLAY to DUAL. Notice that the CH 1 and left plug-in signals are displayed simultaneously.

    Cursor and Save Reference functions are the same as those described in steps 60 through 63 of the "Two-Trace Display (Dual Mode)" instructions, except:

    a. When CURSORS is set at C1, the LEFT PLUG-IN cursor readout is always in divisions (D) from screen center. When CURSORS is set at C2-C1, the cursor readout is in Δ divisions (ΔD).

THREE-TRACE DISPLAY (LEFT PLUG-IN MODE)

A three trace display can be achieved with a dual-trace amplifier unit installed in the left plug-in compartment of the oscilloscope mainframe.

73. Connect a 1 kHz signal to the 5D10 CH 1 input, and to both inputs of the dual-trace amplifier unit (in left plug-in compartment of the oscilloscope mainframe). Set the dual-trace amplifier for dual-trace operation; position traces as necessary.

    a. Press the SAVE button (in).

    b. Observe a three-trace display on the screen.

    c. Note that the cursors on the dual-trace portion of the display (from the left plug-in unit) are shared between the two traces. Cursor measurements can be made on any of the displayed waveforms. Care should be exercised on either of the left plug-in traces to ensure that both cursors are on the trace to be measured.

74. Release SAVE (button out). Press SAVE REF and TRACE SEP (buttons in). Notice that three reference traces and three newly acquired traces are displayed. Press SAVE button in.

    Cursor measurements can be made on any of the displayed waveforms. Care should be exercised to ensure that both cursors are on the proper trace to be measured.

75. Release the SAVE, SAVE REF, and TRACE SEP (buttons out). Set the ACQUISITION AND DISPLAY to X:CH1/Y:CH2.

    a. Observe a two-vector display; the 5D10 CH 1 input provides the X-axis for both vectors, and the left plug-in dual amplifier unit provides the Y-axis inputs. One Y-axis is input through Channel 1, and the other Y-axis is input through Channel 2 of the left plug-in unit.

This completes the Part II—Detailed Checkout Procedure.

DETAILED OPERATING INSTRUCTIONS

SIGNAL CONNECTIONS

Probes

Generally, probes offer the most convenient means of connecting input signals to the instrument. They are shielded to prevent pickup of electromagnetic interference, and the 10X probe offers a high input impedance that minimizes circuit loading. This allows the circuit under test to operate with a minimum of change from the normal condition of the circuit when measurements are being made. Signal amplitude is attenuated by a factor of 10 by the probe, and the scale-factor readout is switched to indicate the correct scale factor.

Probe Compensation. Maladajustment of probe compensation is one of the sources of measurement error. Most attenuator probes are equipped with a compensation adjustment. To ensure optimum measurement accuracy, always compensate the oscilloscope probe before making measurements. Probe compensation is acomplished as follows:

NOTE

The range of adjustment of the probe compensation network must be compatible with the input capacitance of the 5D10 (47 pF).

1. Connect a 10X probe to the channel(s) to be used.

NOTE

Recommended probes are TEKTRONIX P6105 (10X) and P6062B (Selectable, 1X or 10X).

2. Set the VOLTS/DIV switch to 10 m, the input coupling to DC, and the SECONDS/DIV to 5 ms.

3. Connect the probe attached to the input bnc connector to the oscilloscope calibrator loop.

4. Obtain a triggered display of several cycles of the Calibrator signal.

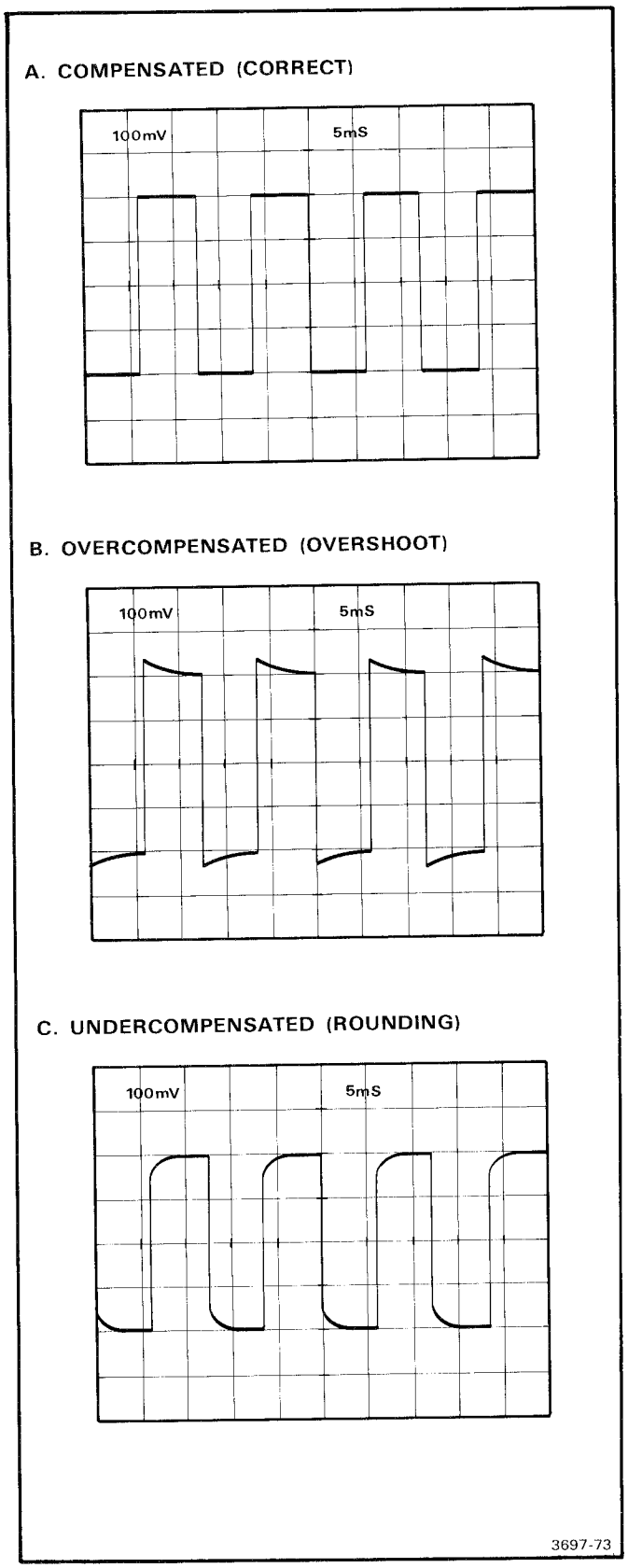


Figure 2-6. Probe compensation.

5. Check the waveform presentation for overshoot and rounding (see Fig. 2-6B, C). Readjust the probe compensation, if necessary, for flat tops on the waveforms (Fig. 2-6A). Refer to the instructions supplied with the probe for the compensation adjustment procedure.

NOTE

Pause following each increment of the compensation adjustment to allow the memory to update and display the new data.

Coaxial Cables

Cables also may be used to connect signals to the input connectors, but they may have considerable effect on the accuracy of the displayed waveform. To maintain the original frequency characteristics of an applied signal, use only low-loss, high-quality coaxial cable. Also, cables should be terminated at both ends in the characteristic impedance. If this is not possible, use suitable impedance-matching devices.

INPUT COUPLING CAPACITOR PRECHARGING

With GND and AC depressed, the input signal is connected to ground through the coupling capacitor and a high resistance to form a precharging network for the coupling capacitor. This network allows the input coupling capacitor to change to the average dc-voltage level of the signal applied to the probe. Thus, large voltage transients are not generated that could be applied to the amplifier input when the input coupling is switched from GND to AC. The precharging network also provides a measure of protection to the external circuitry by reducing the current levels that can be drawn from the external circuitry during coupling capacitor charging.

If AC input coupling is used, the following procedure should be followed whenever the probe tip is connected to a signal source having a different dc level than that previously applied. This procedure becomes especially useful if the dc level difference is more than 10 times the VOLTS/DIV switch setting.

1. Press GND before connecting the probe tip to a signal source.

2. Touch the probe tip to the oscilloscope chassis ground.

3. Wait several seconds for the input coupling capacitor to discharge.

4. Connect the probe tip to the signal source.

5. Wait several seconds for the input coupling capacitor to charge.

6. Release GND (button out). A signal with a large dc component can be vertically positioned within the graticule area, and the ac component of the signal can be measured in the normal manner.

TRIGGERING

Triggering Logic Modes

The operation of the triggering logic mode can be modified (TRIGGERING not set to FREERUN) by moving the Link-Plug (jumper J106) on the A4 Data circuit board.

The two Link-Plug (jumper) positions are First Trig and Full Dspy (First Trigger and Full Display). In First Trig position acquisition stops after recognition of the first trigger event following an erase.

NOTE

A partial trace may be displayed due to insufficient time to acquire data between pressing erase and the first trigger event.

In the Full Dspy position a full horizontal trace will be displayed after an erase. Any triggering event which occurs prior to acquiring a full horizontal trace will be disqualified. The 5D10 is shipped from the factory with the Link-Plug (jumper) in the Full Dspy position.

Applications

The following information describes the results of waveform acquisition using either the "Full Display" or "First Trigger" triggering logic modes.

1. **Full Display Mode**. This mode is useful for most applications. However, trigger events that occur at the beginning of the trace, depending upon the TRIGGERING POSITION selected, may be "disqualified" (not recognized). Trigger events will be "disqualified" if they occur:

   a. Within the first 1.25 divisions of the trace, (TRIGGERING POSITION in POST TRIG).

   b. Within the first 5 divisions of the trace, (TRIGGERING POSITION in CTR TRIG).

   c. Within the first 8.75 divisions of the trace, (TRIGGERING POSITION in PRE TRIG).

Waveform acquisition will not stop when a triggering event has been "disqualified"; that is, acquisition will continue, and that portion of the waveform which occurred during the "disqualified" trigger event will continue to move across the screen, and eventually be lost.

2. **First Trigger Mode.** This mode is useful when slow SECONDS/DIV switch settings are selected, and single events, rather than repetitive waveforms are being acquired. Unlike the Full Display Triggering Mode, single triggering events can be recognized soon after the acquisition begins (after erase). This will allow single-waveform events that occur early in the acquisition process to be saved.

LEVEL/SENSITIVITY Control

The TRIGGERING LEVEL/SENSITIVITY control has two functions, both of which depend on the position of the SLOPE selector pushbuttons.

When the SLOPE selector is set to ⌋ (+) or ⌉ (−), the LEVEL/SENSITIVITY control functions as a LEVEL control. See Figure 2-7A, B. Rotating the LEVEL control clockwise selects a more positive part of the input signal as the trigger point.

When the SLOPE selector is set to BISLOPE (both pushbuttons in) the LEVEL/SENSITIVITY control functions as a SENSITIVITY control. The counterclockwise extreme is MAXimum sensitivity, and the clockwise extreme is MINimum sensitivity.

The adjustable sensitivity/threshold level performs two functions (1) allows the operator to view a signal which exceeds a selected positive or negative level and (2) aids in the capture of transient waveforms of unknown polarity by triggering on the first waveform transition. Figure 2-7C shows the operation of bislope triggering.

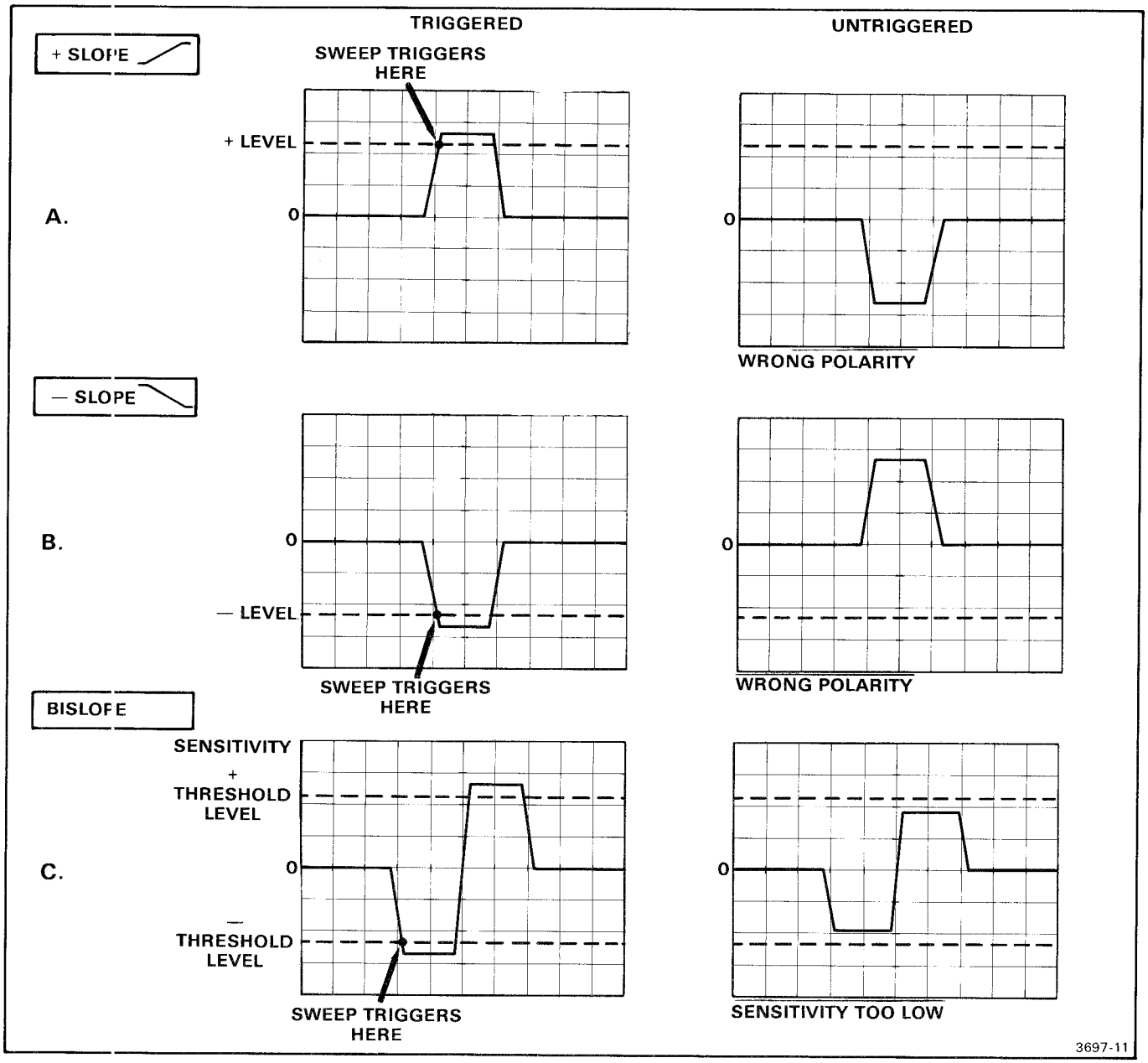


Figure 2-7. Operating characteristics of the triggering slope functions.

To set the LEVEL control, first select TRIGGERING (COUPLING, SOURCE, POSITION and SLOPE). Then set the LEVEL/SENSITIVITY control fully counterclockwise and rotate it clockwise until the the desired trigger point (level) is attained.

To set the SENSITIVITY control, first select TRIGGERING (POSITION COUPLING, SOURCE and BISLOPE). Then set the SENSITIVITY control fully counterclockwise to MAX. If the input signal is of sufficient amplitude (see Specification in Section 1), the trigger circuit will stabilize the display. Rotating the SENSITIVITY control clockwise from its MAX sensitivity position, moves the + and − trigger threshold levels away from their maximum sensitivity levels. The + level becomes more positive and the − level becomes more negative, and the trigger circuit will require a larger input signal to operate. The trigger circuit will stabilize the display when the input crosses either the + or − threshold level.

The bislope feature is useful for detecting randomly occurring events and storing them for continuous viewing. Because SENSITIVITY is adjustable, it may be set to ignore low-level, but capture higher-level, transitions.

TRIGGERING SOURCE

The Triggering Source push buttons select the source of the trigger signal that is connected to the internal trigger circuits.

CH 1, CH 2, Left Plug-In

Normally the triggering signal source will be the same as that selected at the ACQUISITION AND DISPLAY selector. (The CH 1 TRIGGERING SOURCE push-button provides a trigger signal obtained from the signal applied to the CH 1 input bnc connector.) However, some applications require special triggering which cannot be obtained internally. In such cases, the LINE or EXT positions of the SOURCE switches must be used.

LINE. The LINE position connects a sample of the power-line voltage from the mainframe to the trigger circuit. Line triggering is useful when the input signal is time-related (multiple or submultiple) to the line frequency. It is also useful for providing a stable display of a line-frequency component in a complex waveform.

EXTernal. The EXT position connects the signal from the EXT input connector to the trigger circuit.

An external trigger signal can be used to provide a triggered display when the internal signal is either too low in amplitude for correct triggering or contains signal components on which triggering is not desired. It is also useful when signal tracing in amplifiers, phase-shift networks, wave-shaping and logic circuits, etc.

The signal from a single point in the circuit can be connected to the EXT input connector through a probe or cable. The display is then triggered by the same signal at all times and allows amplitude, time relationship, or waveshape changes of signals at various points in the circuit to be examined without readjustment of the triggering controls.

JOIN DOTS (ACQUISITION AND DISPLAY)

The JOIN DOTS switch (button in) causes vectors (straight lines) to be drawn between consecutive data points of a dot display. See Figure 2-8A. Figure 2-8B shows the same display without vectors to illustrate the phenomenon called perceptual aliasing. Perceptual aliasing is a type of optical illusion that causes the eye to visually connect adjacent points in a dot display.

In addition to perceptual aliasing, dot displays can also show an envelope error even though vectors are drawn between the data points. This occurs when the sampled points do not fall on the peaks of the incoming signal. An increased sample rate will minimize this condition.

Each type of display construction (dots or vectors) yields a different useful storage bandwidth. Dot displays will need more samples-per-cycle on the crt screen to minimize perceptual aliasing and envelope errors. Vector displays need fewer samples-per-cycle since the vectors eliminate perceptual aliasing.

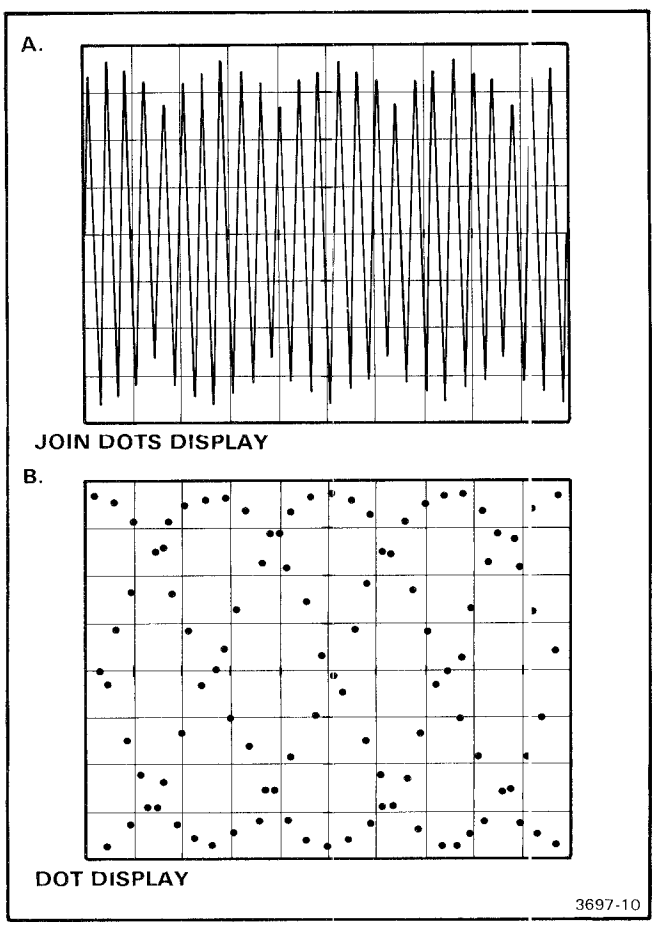


Figure 2-8. Perceptual aliasing illustrated.

OPERATION AND INTERACTION OF SAVE AND SAVE REFERENCE

The following description details the operation and interaction of the SAVE and SAVE REF buttons with the cursor and scale factor readout fields, and the display and acquisition modes.

There are five acquisition and display modes—CH 1, CH 2, ADD, DUAL and XY. (The acquisition mode is DUAL when the display mode is XY). These modes are selected by pushing the front-panel button with the same name. When the SAVE and SAVE REF buttons are out, the display and acquisition modes are the same as the mode selected by the front-panel buttons. Scale Factor fields on the crt screen will display the selected scale factor setting. After either the SAVE or SAVE REF button has been pushed, further changes in the front-panel ACQUISITION AND DISPLAY buttons will not change the acquisition mode. Refer to Table 2-1.

The CH 2, ADD, DUAL and XY modes are modified when the LEFT PLUG-IN is selected and is in dual-channel mode. The CH 2 portion of memory is split into two parts—one for LEFT CH 1 and one for LEFT CH 2. No changes are made in the acquisition or display modes (with regard to LEFT dual or single) if changes are made to the left plug-in after the SAVE or the SAVE REF buttons have been pushed.

NOTE

While the SAVE REF button is pressed and the left plug-in amplifier is set to Dual-Trace mode, do not enter or leave the LEFT PLUG-IN mode.

When both SAVE and SAVE REF buttons are out, the acquisition and display modes are the same as the mode selected by the front-panel buttons. If CURSORS is OFF, cursor readout fields are not displayed. Scale factor fields display the present scale settings.

When the SAVE button is out, SAVE REF button is in, and CURSORS is OFF, changes in the scale factor settings will cause the associated scale factor readout field to be blanked. When CURSORS is in C1 or C2-C1 position, CURSORS scale readout settings will be blanked during waveform acquisition or if the display is not triggered. The display mode will be determined by the front-panel buttons according to Table 2-1. The acquisition mode will not change.

MEASUREMENT CONSIDERATIONS

The maximum frequency that can be reconstructed accurately is limited by the number of traces to be displayed at any one time. Selection of the ACQUISITION AND DISPLAY mode, SAVE REF or LEFT PLUG-IN determines the number of traces and the number of data points available to display each trace.

If, for example, you pressed DUAL (single channel left plug-in), the number of data points available to each trace width would be 512 (1024 ÷ 2 = 512 data points). If SAVE REF was then pressed, the data points available to reconstruct each of the four traces would be reduced to 256 (1024 ÷ 4 = 256). See Table 2-2

As the number of data points per trace is reduced, the maximum frequency that can be reconstructed accurately is also reduced. The POSSIBLE UNDERSAMPLING indicator will light when fewer than 8 samples (data points) are taken of each cycle of incoming signal. This light signals the operator that too few samples are being taken to accurately reconstruct the incoming signal.

TABLE 2-1
Interaction of SAVE and SAVE REF on ACQUISITION AND DISPLAY

The ACQUISITION AND DISPLAY Mode Switch setting selected after SAVE or SAVE REF is pressed (button in).		CH 1	CH 2	ADD	DUAL	XY
		Resultant display format				
The ACQUISITION AND DISPLAY mode switch setting when the signal was acquired and SAVEd.	CH1	CH1	CH1	CH1	CH1	CH1
	CH2	CH2	CH2	CH2	CH2	CH2
	ADD	ADD	ADD	ADD	ADD	ADD
	DUAL	CH1*	CH2*	DUAL	DUAL	XY
	XY	CH1*	CH2*	DUAL	DUAL	XY

* **The display in these modes is either the CH 1 or the CH 2 portion of the data in memory which is stored in dual-channel format.**

TABLE 2-2
Measurement Frequency Limitations

Number of Traces	Data Points per Trace		Maximum Useful Input Frequency
	CH 1	CH 2	
1	1024	1024	100 kHz
2	512	512	50 kHz
3	512	256	25 kHz
4	256	256	25 kHz
6	256	128	12 kHz

ERASE CONDITIONS

An erase will occur if, during acquisition, any of the following occurs:

1. The SAVE or SAVE REF button is depressed then released.
2. The ACQUISITION AND DISPLAY mode, TRIGGERING POSITION, VOLTS/DIV, SECONDS/DIV or INVERT is switched.
3. The CH 1 or CH 2 VOLTS/DIV, or SECONDS/DIV CAL control is switched out of its calibrated detent, or a probe is connected which changes the vertical scale factor readout.

At any time during the operation of the instrument (if SAVE button is not in) either pressing ERASE or interrupting the mainframe power will cause an erase.

SETTING THE PENLIFT POLARITY (J1050)

The position of jumper J1050 determines logic polarity at the front-panel PENLIFT jacks. Jumper J1050 is preset at the factory to the UP-OP position (pins 1 and 2 linked together); this means the recorder pen will lift ("UP") when the relay contacts open ("OPen"). Refer to illustration in Figure 2-9. Normally-closed contacts can be obtained by moving the jumper to the UP-CL position (pins 2 and 3 linked together). Refer to the instruction manual for the XY recorder being used to determine the penlift logic polarity required for proper operation.

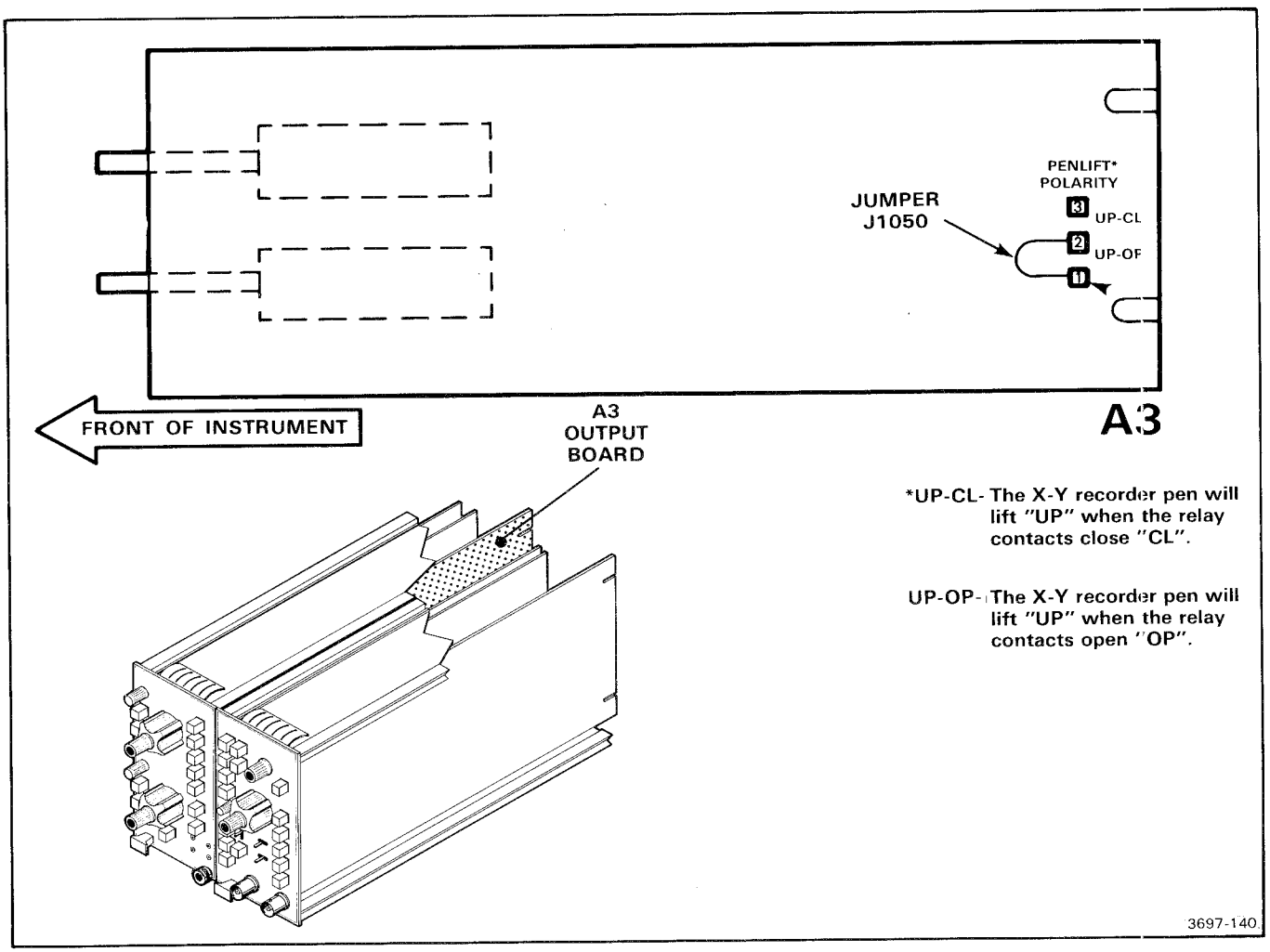


Figure 2-9. Penlift-polarity jumper location and settings.

COLOR OPERATION

When used with an oscilloscope capable of displaying color, such as the TEKTRONIX 5116 Oscilloscope, the 5D10 provides the signals for a three-color display (orange, cyan and neutral). See the 5D10 Waveform Digitizer Operators manual for color operating instructions, color applications, and color rules using an XY recorder.

THEORY OF OPERATION

The Block Diagram Description gives an overview of the entire instrument operation. The Detailed Circuit Description gives circuit operation to the component level. A glossary of signal names with a brief description of the signal function is also included at the end of this section.

Some digital circuits are troubleshot using signature analysis. These circuits are not described in detail. See the Maintenance section of this manual for troubleshooting information.

BLOCK DIAGRAM DESCRIPTION

The numbers in the blocks of the block diagrams refer to the schematic number where the circuitry is shown. Refer to Figure 3-1 for the following discussion.

The 5D10 samples the input-signal voltage at a specific instant in time. This sample voltage is digitized (converted to an eight-bit binary number) and stored in the Waveform Memory. During display, the binary number that represents the voltage of the input waveform is converted to a voltage. This voltage determines the position of the crt beam. The position of the dot on the X axis is with respect to time in the Y-T mode, or with another input signal in the X-Y mode.

The resolution of the 5D10 is 25 points per vertical division on the crt and 100 points per horizontal division

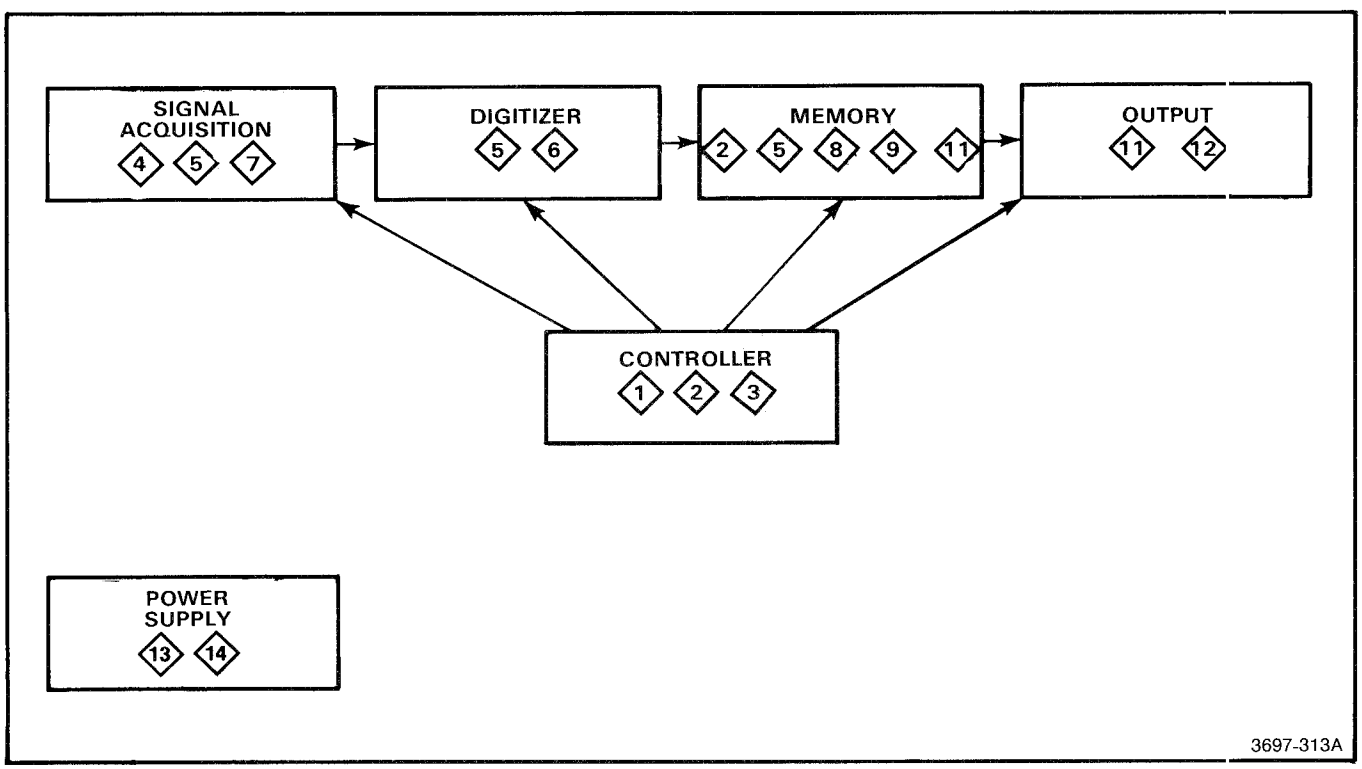


Figure 3-1. Overall block diagram.

in the vertical vs time (Y-T) mode. In the X-Y mode, the horizontal resolution changes to 25 points per division. To determine the time per sample, divide the time per horizontal division as set by the SECONDS/DIV switch by 100.

The Controller block, containing the microprocessor, manages functions in the other blocks. The Power Supply provides ± 7.5 V and +5 V from the mainframe power (+ and −38 V unregulated).

SIGNAL ACQUISITION BLOCK DIAGRAM

Figure 3-2 shows the Signal Acquisition Block Diagram. The input signals are applied through the front-panel input connectors to the CH 1 and CH 2 Preamps. Gain switching occurs here. The trigger pickoff signal is taken before the input signals reach the positioning controls. This is done to prevent trace positioning from affecting the triggering point. The outputs from the CH 1 and CH 2 Preamps feed to the Intermediate Amplifiers. In the ADD mode, addition of the channel one and channel two signals occurs in the Intermediate Amplifier.

The output from the Intermediate Amplifier feeds the Sample/ Hold circuitry. This circuitry isolates the input signal from the digitizer while analog-to-digital conversion is occuring. The input signal voltage charges a capacitor. The capacitor stores the charge while the input disconnects from the capacitor.

There is one Sample/Hold circuit for each channel, permitting simultaneous sampling in both channels. This is necessary for accurate X-Y displays.

The voltage output from the Sample/Hold circuits feeds the Channel Switch.

Output from the Trigger Pickoffs feeds the Source Select Coupling and Input Buffer circuitry. This circuitry selects from the available trigger sources such as LINE, CH 1, CH 2, LEFT PLUG-IN or EXT, and buffers the selected signal.

The comparator in the Comparators and One Shot block compares the triggering signal with a voltage from the TRIGGERING LEVEL control. This determines the voltage point on the triggering signal at which waveform digitizing stops. The oneshot portion of circuitry in this block forms uniform (amplitude and duration) pulses at the selected trigger times, for use by the Triggered Indicator, Loadstop Logic, and Undersampling Indicator.

The TRIG'D light on the front panel illuminates when the pulse output from the oneshot multivibrator is present. The Triggered Indicator circuitry increases the duration of the triggering pulse to illuminate the lamp for short duration trigger pulses.

The POSSIBLE UNDERSAMPLING light illuminates when less than eight sample-pulses-per-waveform-cycle occur. The Loadstop Logic circuitry generates signals to stop loading of the waveform memory at the proper time.

The Viewtimer circuitry determines the time the waveform information (stored in waveform memory) is displayed on the crt.

The Power Decoupling circuitry generates −10 V via VR541. The Bias Supplies provide low current −5 V and −20 V.

DIGITIZER BLOCK DIAGRAM

Figure 3-3 shows the Digitizer Block Diagram. Waveform digitizing operates continuously. The digital information is stored in memory while the memory is read for the display. There is a time delay from the storing of information to the reading of the same information. Digitizing continues until the trigger signal is sensed. Now the most recently stored waveform data is repeatedly displayed until the viewtimer circuitry causes a new digitizing cycle to commence.

The 1 MHz Oscillator controls the sampling rate. The Timebase N divides the 1 MHz frequency (to a minimum of 2 Hz at 50 SECONDS/DIV setting) depending on the SECONDS/DIV switch setting. The output of this circuit drives the Digitizer Control block. The Digitizer Control generates signals which control the entire digitizing process (sampling the input waveform at uniform time intervals and converting the voltage to a binary word).

The Left Plug-In Channel Switch Logic controls the input signal from the plug-in unit residing in the mainframe's left plug-in compartment.

The Clock Generator circuitry provides the timing signal for the digitizing of the sampled voltage from the Sample and Hold circuitry. The output from the Clock Generator feeds the Timing circuitry. This circuitry provides clock signals for the Successive Approximation Register. This register generates the binary word stored in the waveform memory, along with the Digitial-to-Analog Converter. Successive approximations occur until the output from the Digital-to-Analog Converter is equal to the Sample and Hold voltage.

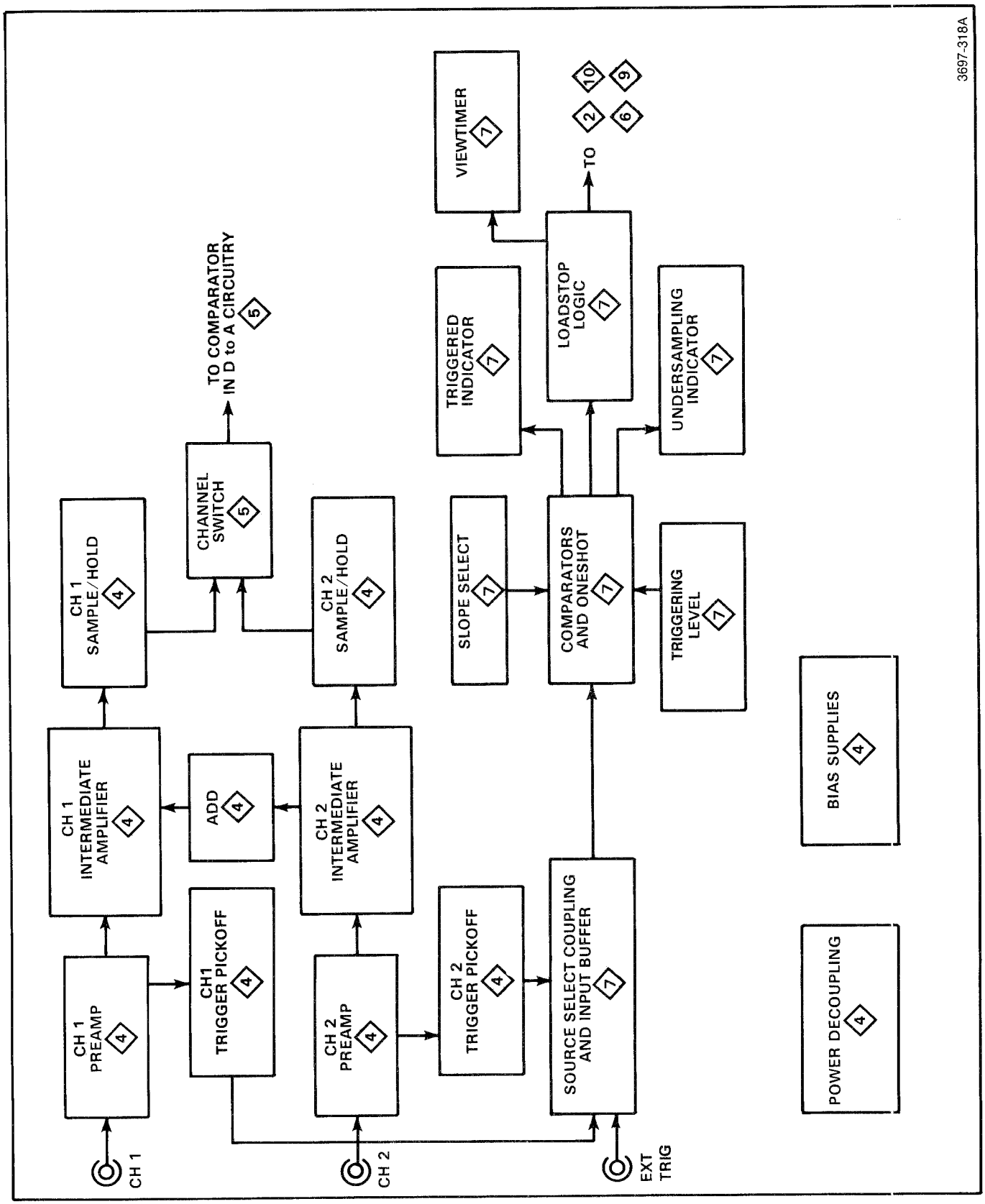


Figure 3-2. Signal acquisition block diagram.

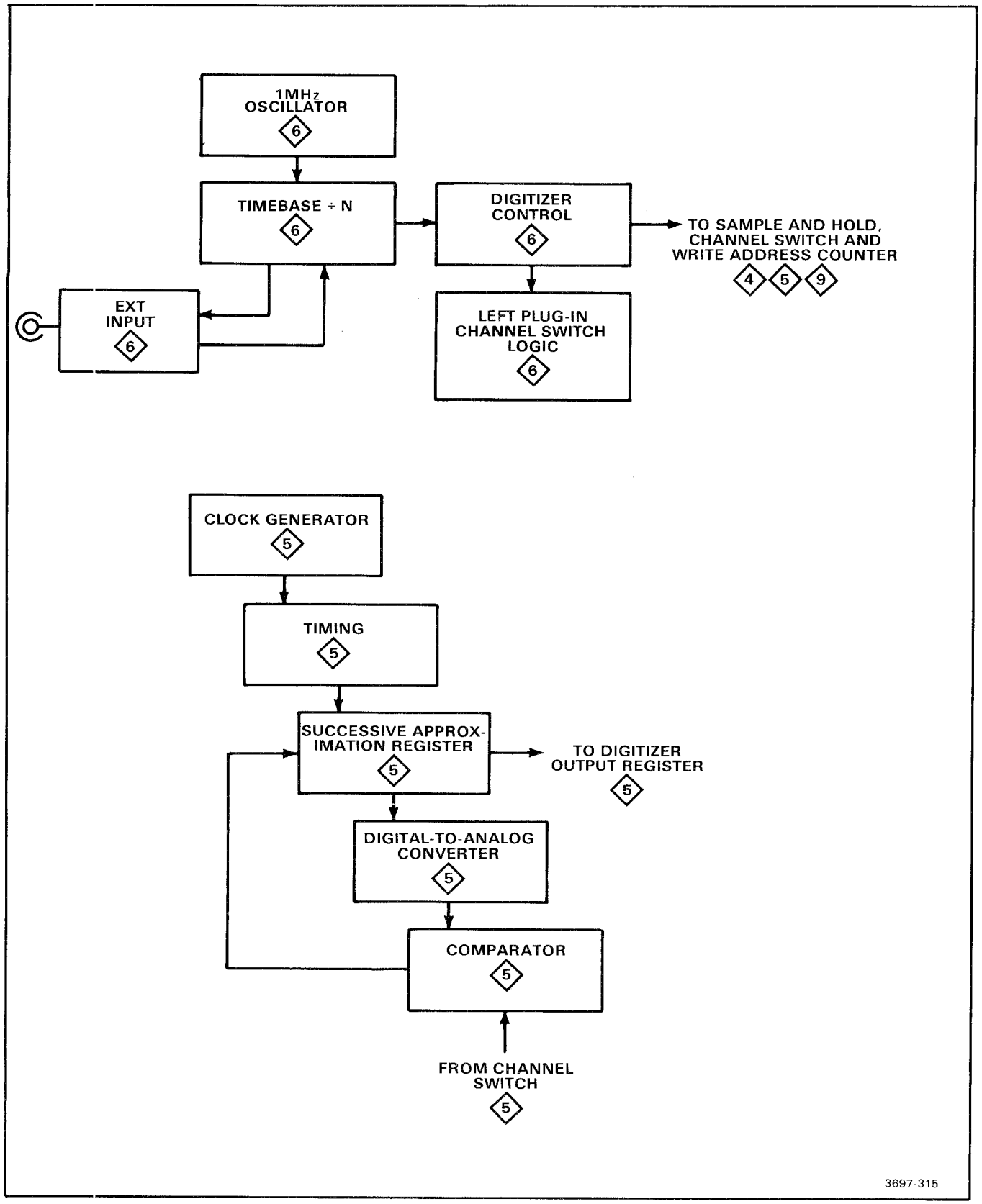


Figure 3-3. Digitizer block diagram.

MEMORY SYSTEM BLOCK DIAGRAM

Figure 3-4 shows the Memory System Block Diagram. Digital data from the Successive Approximation Register (described above) feeds the Digitizer Output Register. Binary control data from the microprocessor appears on the Numbers (N0 through N9) bus. These data include start-point information for the waveform, read increment information for the Time Register, and self test data. The Memory Data Selector chooses between the numbers input from the microprocessor or the digitizer output. The Write Address Counter steps the write addresses in sequence. The Write Address Modifier alters bits W0 through W2 from the counter when a reference waveform has been saved.

The Memory Address Selector chooses write addresses from the Write Address Counter and Write Address Modifier, or read addresses from the Read Address Register. These addresses go to the Waveform Memory, the B Selector, and the Memory Data And Address selector. The Memory Data And Address selector chooses either the waveform addresses or the Waveform Memory output for data feedback to the microprocessor.

The Waveform Memory stores the binary data from the digitizer. The output from the memory is applied to the X and Y Display registers. The X display register also displays output from the Time Register when the 5D10 operates in the Y-T mode (time for the X axis).

The B Selector chooses either the output from the Memory Address Selector or the Numbers bus and directs them to the Adder. The Scratchpad saves the write addresses for the trigger point and the last point on each waveform. The output from the Scratchpad is added to the B Selector output by the Adder and applied to the Time Register and the Read Address Register. The A Selector chooses either the Time Register or the Read Address Register output for the A input to the Adder. All of these elements together generate a sequence of read addresses and time points used in displaying the stored waveform, and provide information to the Loadstop Logic circuitry used during acquisition. The Read and Write Controller provides control signals for these blocks.

OUTPUT BLOCK DIAGRAM

Figure 3-5 shows the Output Block Diagram. Binary data from the Waveform Memory passes to the X and Y Display Registers. The Y Display Register is an eight-bit register and the X Display Register is a 10-bit register, as more data points are included in the X axis. The X And Y Register Clocks update the contents of the display registers. Outputs from the Display Registers feed the D to A Converters.

The D to A Converters change the binary word (stored in memory) to an analog voltage corresponding to the position on the input waveform of the sampled voltage. This voltage feeds the X and Y Output circuits. The X and Y Output circuits amplify the voltage for the display in dots, or integrate from the voltages representing the dots for a continuous trace (JOIN DOTS). The Display Timer block determines the duration of the dot or vector display. Blanking and unblanking of the crt is controlled through circuitry in the mainframe and the Z axis circuitry. The functions performed in the X and Y Output circuitry are controlled by the Controller block.

CONTROLLER BLOCK DIAGRAM

Figure 3-6 shows the Controller Block Diagram. The CPU block consists of an eight-bit microprocessor that obtains its instructions from 16 k bytes of ROM. Also available is 1 k byte of RAM. The Control Clock Oscillator provides timing for the CPU and the waveform memory read and write controller. The CPU outputs information to the instrument through the I/O Control and the Controller Outputs. The instrument reports to the CPU, concerning its status and the conditions of the front-panel controls, via the Front Panel Switches and Machine States.

POWER SUPPLY BLOCK DIAGRAM

Figure 3-7 shows the Power Supply Block diagram. The Oscillator circuitry generates a sawtooth waveform at a frequency of about 100 kHz. This waveform feeds the Comparator block along with voltage and current information from the Voltage Regulator. The output from the Comparator is a varying-duty-cycle square wave depending on the voltage or current demands from the power supply. The Comparator output feeds the Gate Driver circuitry. This circuitry drives the switching transistors in the Switching Transistor And Transformer block providing input for the transformer. The output from this block drives the Rectifiers, Filters And Current Senses block. The Protection block prevents damage to the power supply from fault conditions.

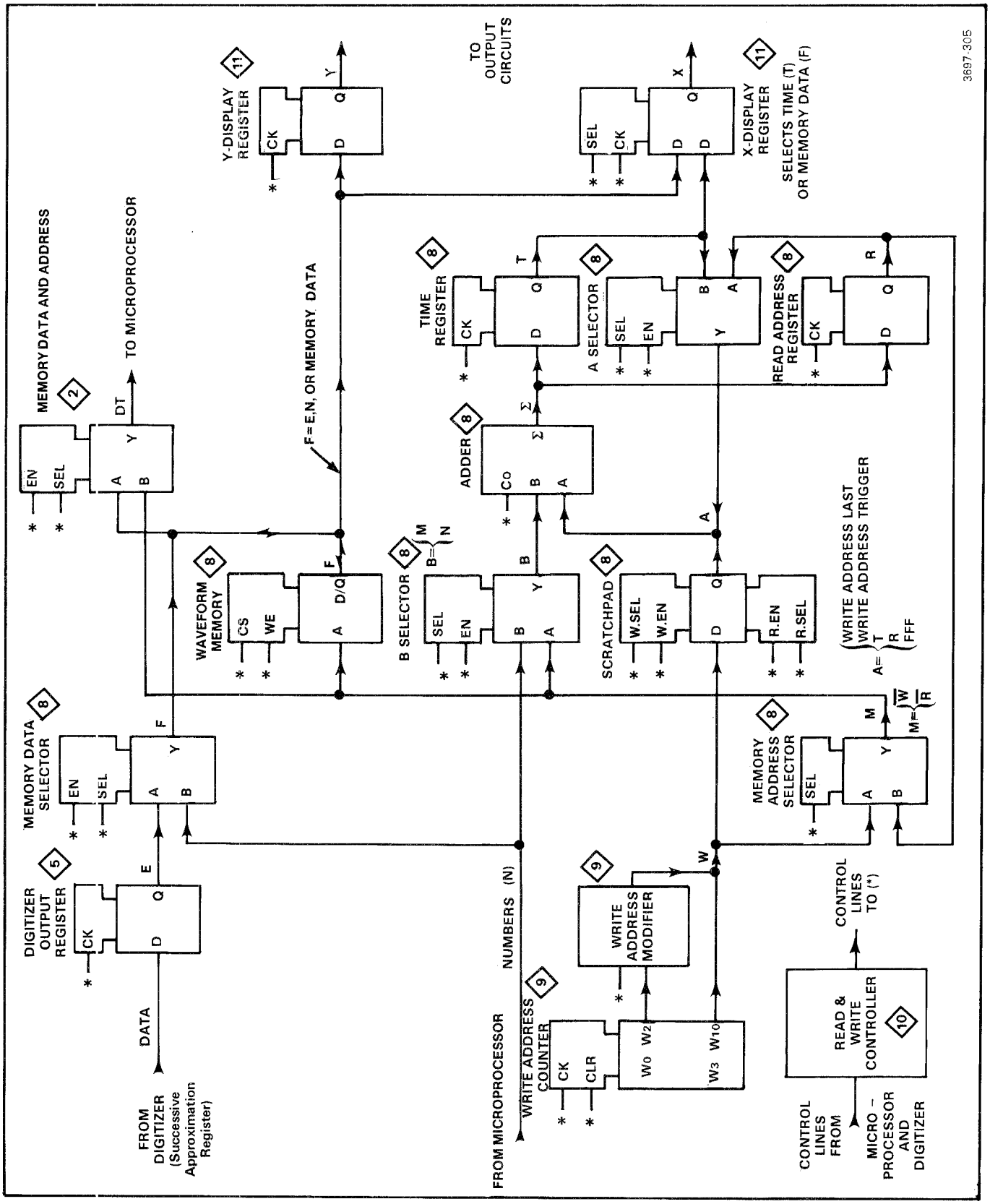


Figure 3-4. Memory system block diagram.

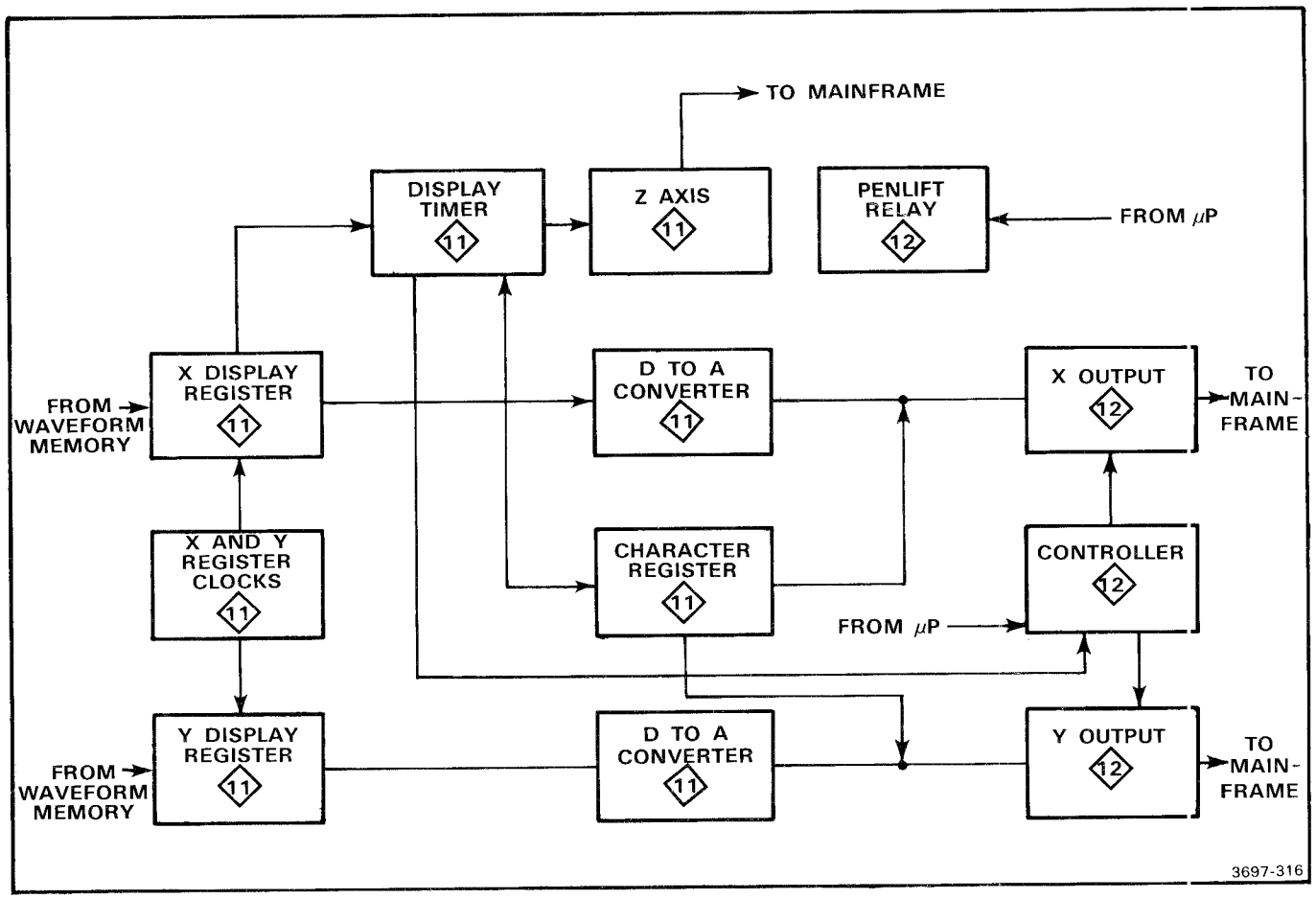


Figure 3-5. Output block diagram.

DETAILED CIRCUIT DESCRIPTION

This discussion provides a detailed description of the electrical operation of the circuits in the 5D10. Unique circuits in this instrument are described in detail. Circuits commonly used in the electronics industry are not described in detail.

Complete schematic diagrams are provided in Section 8, Diagrams and Circuit Board Illustrations. The number inside the diamond preceeding a heading in the following discussions refers to the schematic diagram for that circuit. The schematic diagrams contain wide shaded borders around the major stages of the circuits to conveniently locate the components mentioned in the following discussions. The name of each stage is shown in a shaded box on the diagram, and appears as a sub-heading in the discussion of that schematic diagram.

Detailed circuit discussion is not provided where signature analysis is used to diagnose circuit faults. See the Maintenance section of this manual and the 5D10 Diagnostic Troubleshooting Service Manual, Volume 2, for further information.

TEKTRONIX DRAFTING CONVENTION

Logic symbols on the schematics are drawn according to the function performed by the device in its particular application. By so doing, some deviations from the manufacturers assigned symbology occur (although device electrical function is identical). An example of this is an AND gate (all inputs high-output high; any input low-output low) drawn as an OR gate for low inputs. For operational characteristics of individual devices not covered in this manual, refer to the manufacturers data book or other appropriate source.

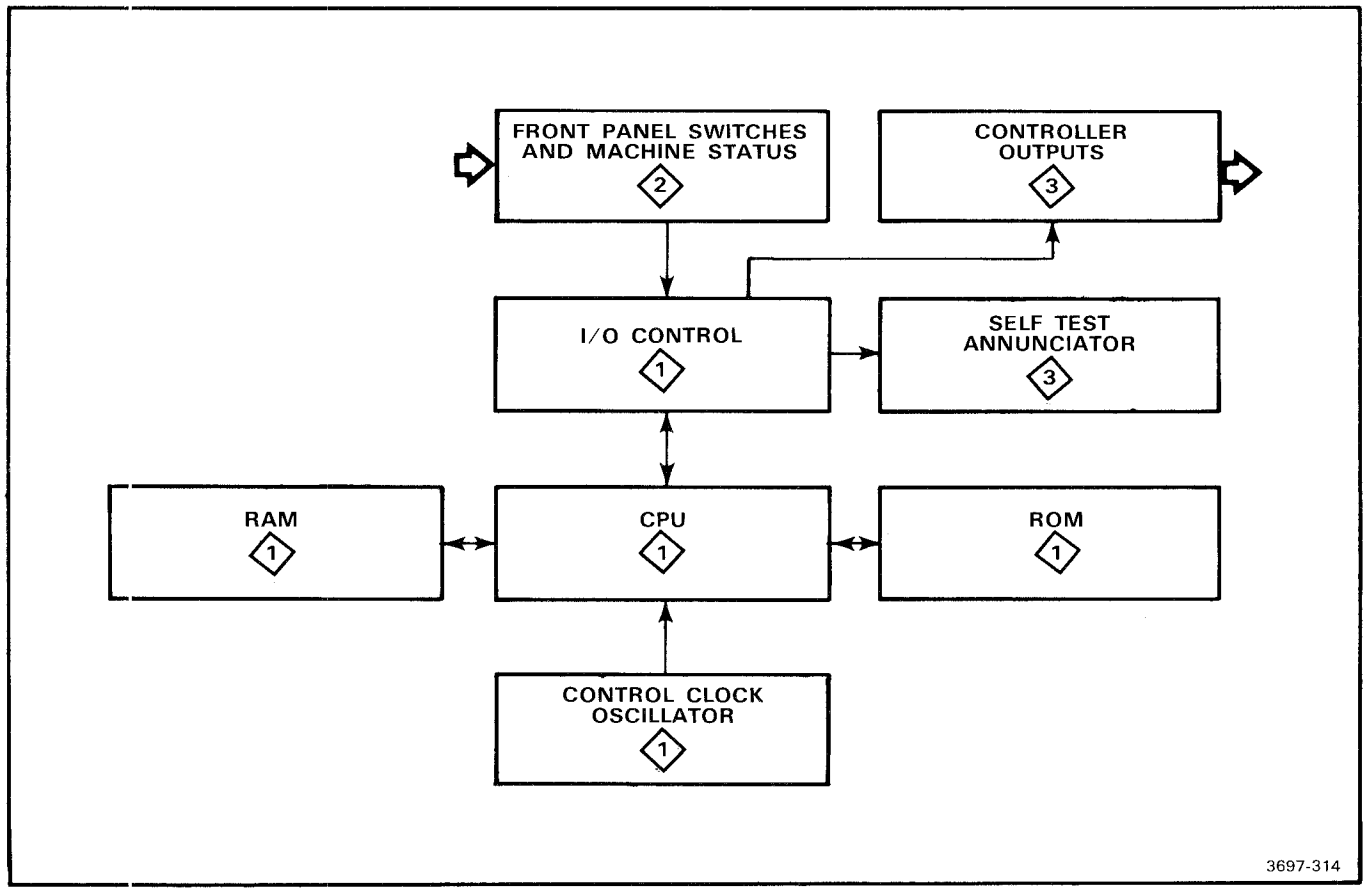


Figure 3-6. Controller block diagram.

1

CPU, ROM, RAM, CLOCK AND I/O CONTROL

CONTROL CLOCK OSCILLATOR

This Boze or emitter coupled oscillator operates at 10 MHz. Emitter coupling occurs through C500. A slight frequency change is possible by adjusting R501. The output signal passes through inverter U630A, whose output provides the clock signal. The clock signal also feeds the input of U630B, which provides the $\overline{\text{Clock}}$ signal.

CPU

Microprocessor U230 is clocked at a 10 MHz rate. The clock signal at 10 MHz is buffered by U322A and U322C. The microprocessor has eight data lines and sixteen address lines. Addresses A0 through A7 are multiplexed with the eight data lines, DBO through DB7. The lower eight address and data lines are demultiplexed by U121. When ALE, pin 30 of the microprocessor, transits from high to low an address on the AD0 through AD7 lines is latched into U121. These lines are now available for data. The upper three address lines A13, LA14, and A15 feed demultiplexer U123.

ROM

Address lines A0 through A12 and data output lines DB0 through DB7 connect to ROMs U201 and U213.

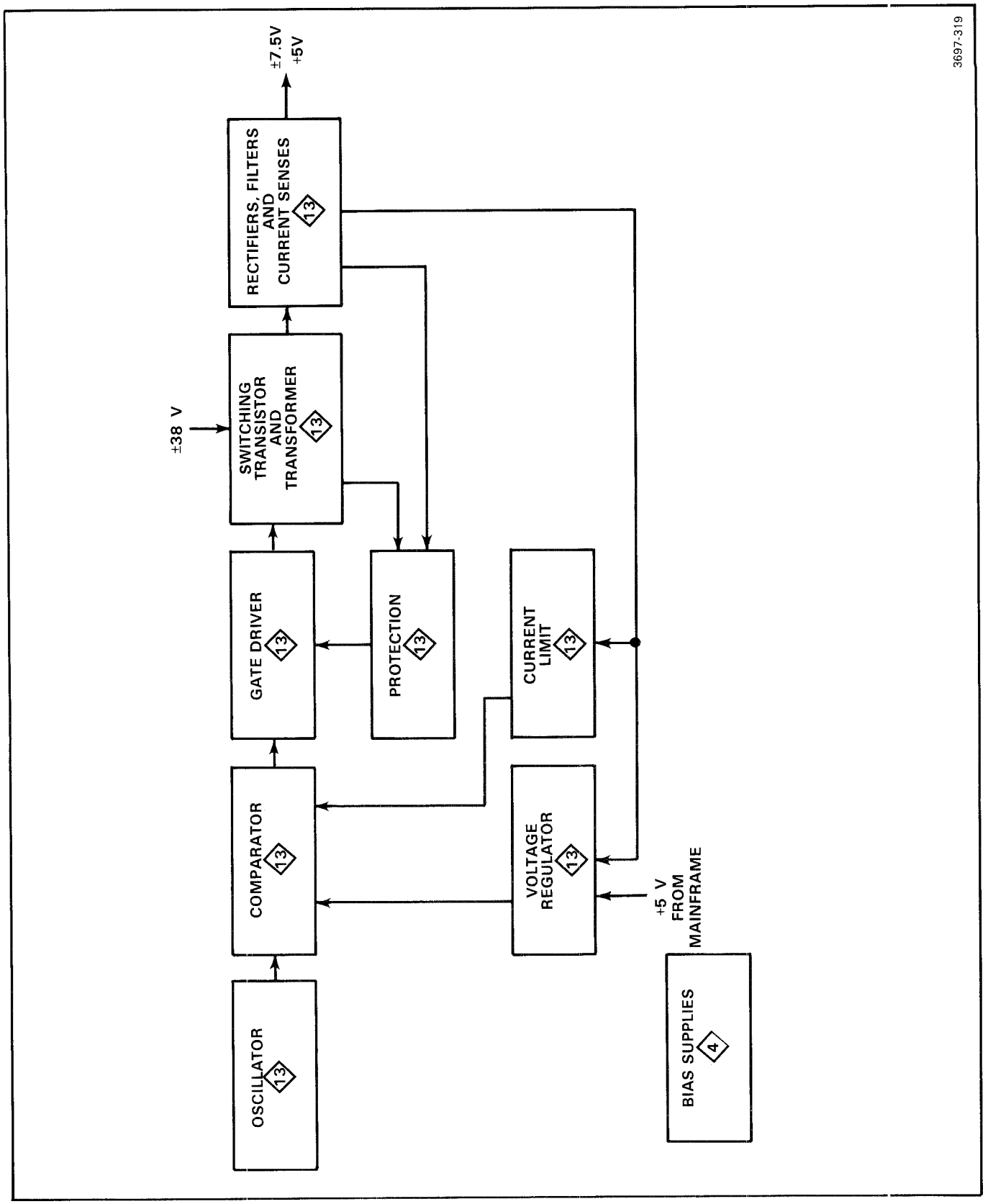


Figure 3-7. Power supply block diagram.

RAM

Address lines A0 through A9 connect to both RAMs, U101 and U111. Output data lines DB0 through DB3 connect to U111 while data lines DB4 through DB7 connect to U101.

I/O CONTROL

Buffers for the data lines are contained in U930. These buffers operate in either direction or are both off, depending on the state of the DIR and Enable input lines, pins 1 and 9. When the DIR line is high data flows from the microprocessor. When this line is low, data flows to the microprocessor.

Address lines A0 through A3 provide input data for decoders U300 and U650. The output from decoder U650 controls the data selectors shown on schematic 2 and the outputs from U300 control the registers shown on schematics 3 and 11.

When P440 is removed, the data lines to the microprocessor are opened, and the microprocessor is placed in the forced instruction mode. Resistor R340 raises all data lines for hexidecimal instruction of 7F (DB7 is low during $\overline{RD}$ through the action of U223D and U223B). This produces a NOP (no operation) instruction causing the microprocessor to cycle continuously through all addresses.

2 CONTROLLER INPUTS

FRONT-PANEL SWITCHES AND MACHINE STATUS

This circuitry applies the logic from the front panel controls to the CPU. All data passes through quad tri-state multiplexers to the microprocessor. The charts on the schematic list the switch positions for the various front-panel control settings.

MEMORY DATA AND ADDRESS

This circuitry is an interface between the microprocessor and the F and M buses. The F bus provides data from the digitizer and data memory. The M bus provides addresses from the Waveform Memory.

3 CONTROLLER OUTPUTS AND SELF-TEST ANNUNCIATOR

CONTROLLER OUTPUTS

The registers are controlled by the microprocessor via the I/O Control decoders shown on schematic 1. The register outputs are control lines to various parts of the instrument.

SELF-TEST ANNUNCIATOR

These LEDs, located at the rear of the instrument, connect to the N bus. When the bus lines are low the LEDs illuminate (if jumper J100 is installed). See the maintenance section of this manual and the 5D10 Volume II Service Manual for more information.

4 SIGNAL ACQUISITION CH 1 AND CH 2

CH 1 PREAMP

This block provides input signal attenuation, ac coupling and conversion to double-ended output. The output of this circuitry drives the CH 1 Intermediate Amplifier. A simplified block diagram of this circuit is shown in Figure 3-8.

The input signal applied to the front-panel bnc connector passes through DS1, a current limiting lamp, to S1200A and C1221, the ac coupling capacitor. This capacitor is connected in series with the input to Q1020A (when S1200A is pressed). Precharging current for C1221 is supplied through R1225. The input is grounded to obtain 0 V reference by pushing S1200B. Adjustment of the input capacitance is provided by C1120. Further input capacitance adjustment in the higher input-attenuation positions is provided by C1002. The chart showing the switch closures for the various attenuation ratios is shown below the circuitry on the schematic.

The input signal is not attenuated in the 1 mV through 0.2 V positions. A 100X attenuator consisting of R1226 and R1120, and compensated by C1000 and C1121 is switched in the circuit for the 0.5 V through 20 V per division vertical sensitivity.

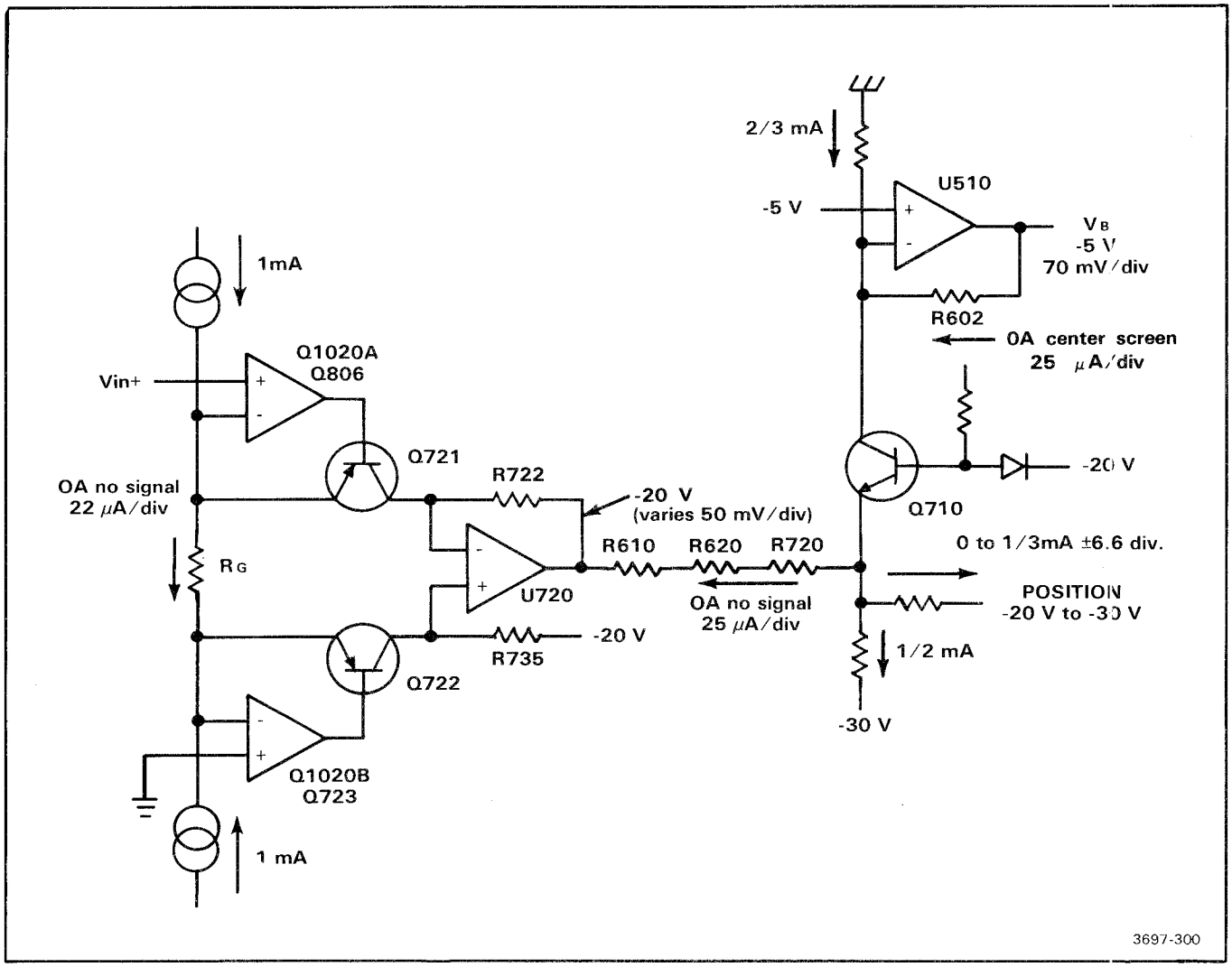


Figure 3-8. Simplified block diagram of CH 1 Preamp and Intermediate Amplifier, channel 2 amplifier is similar. See text.

The signal then passes through R1021 and C1021 to the gate of Q1020A. Overvoltage protection for Q1020A is provided by CR1027 in conjunction with R1020.

The single-ended input converts to a differential signal via Q1020A and Q1020B. These FETs are connected as a differential pair with source degeneration. The source degeneration varies depending on the setting of the VOLTS/DIV front-panel switch. Current balance for the two input FETs is provided by R920.

Referring to Figure 3-8, the input circuit operates as a voltage to current converter. Sensitivity is determined by the value of Rg. The current through the gain set resistors is quiescently zero.

The collectors of output transistors Q721 and Q722 current drive the input of operational amplifier U720.

CH 1 INTERMEDIATE AMPLIFIER

The signal current and the positioning current are mixed at transistor Q710. The single ended output from U720 drives the emitter of common base transistor Q710. The gain is calibrated by R620 and adjusted by front-panel control R610. The position control, R500, varies the bias current in Q710. As the emitter of Q710 is a virtual ground, no voltage change can be seen at this point.

The collector of Q710 drives the minus input of operational amplifier U510. This amplifier operates as a current-to-voltage converter.

When channel 1 and channel 2 are operating in the add mode the base of Q430 is high (≈+3 V) and the transistor is conducting. This saturates Q630 and causes Q610 to conduct, passing the signal from channel 2 through Q610 to the input of U510, where it is added to the

signal from channel one. The four diodes CR507, CR601, CR604 and CR605 prevent the output from going more than two diode drops from the input of the operational amplifier. Gain for U510 is determined by R602, and is ac compensated by C601.

CH 1 SAMPLE AND HOLD

The diode bridge, CR410, acts as a switch for the output of U510 to charge C403. The high impedance of the reversed biased diodes in the bridge prevents the current from leaking off C403 during the hold cycle.

During the sample time CR434 is reversed biased, Q400 is off and Q401 is conducting. All diodes in the bridge are conducting. The signal voltage charges C403 to the level at pin 6 of U510. The voltage is also present at the gate of Q410A. When the Hold pulse comes from the digital control circuitry, Q400 conducts and Q401 turns off. This action reverse-biases the diodes in the bridge, presenting a high impedance to C403.

CH 1 TRIGGER PICKOFF

Signal from the output of U720 is applied to the anode of CR630. This diode and Q536 form the equivalent of a differential pair. The negative input is the base of Q536 and the positive input is the anode of CR630. The collector of Q536 drives emitter follower Q436. Feedback occurs through R537 and the triggering signal passes through R434.

CH 2 PREAMP

This circuitry operates in an identical manner with the channel one circuitry from the input to the junction of R1044 and R1047. When the CH 2 VOLTS/DIV switch is set for LEFT PLUG-IN, the plus and minus signal lines from the left vertical plug-in pass through the mainframe, switch S930, and to the gates of the input amplifier, Q1040A and Q1040B. The gate of Q1040B is ungrounded by section 1 of S340. Input overload protection for Q1040A and Q1040B is provided by diodes CR1048 and CR1041 in conjunction with R949 and C947.

The other difference in the CH 2 Preamp circuitry is the addition of invert switch, S740. This switch connects to the collectors of Q730 and Q731. When pressed, it switches the minus output from the collector of Q730 to the minus input of U640. The collector of Q731 then connects to the plus input of U640.

CH 2 INTERMEDIATE AMPLIFIER

This circuitry operates in a manner similar to the CH 1 Intermediate Amplifier except in the ADD mode. In the ADD mode Q610 conducts passing the channel 2 signal to the channel 1 current summing point; this also saturates Q625. No current flows through CR622, which disables Q528. The signal path for channel 2 is now open, and the channel 2 signal passes to channel 1 and is added at the summing point for the input of U510.

CH 2 SAMPLE AND HOLD

This circuitry is identical in operation with the CH 1 Sample and Hold circuitry described previously.

CH 2 TRIGGER PICKOFF

This circuitry operates identically to the channel 1 circuitry except for the 180 degree phase inversion accomplished when channel 2 operates in the inverted mode. When channel 2 is inverted, the anode of CR542 is connected to −20 V. The channel 2 signal feeds through R546 to the base of Q541. The action of Q541 provides the phase inversion. The output trigger signal from the emitter of Q540 is now the same phase as in normal operation.

BIAS SUPPLIES

Bias voltages of −5 V and −20 V are provided from U710A and U710B. The output voltage levels are set by a resistance divider composed of R802, R705 and R704. The operational amplifiers, U710A and U710B provide a constant voltage with varying currents as required. Filtering is provided by C800 and C900.

The −10 V is provided from −30 V from the mainframe via zener diode VR541.

5 DIGITIZER

CLOCK GENERATOR

This circuitry generates the timing signals for the Digitizer circuitry. A Boze (emitter-coupled) oscillator is formed by Q520 and Q521. The oscillator is controlled by the $\overline{\text{End}}$ signal, connected to the base of Q422, and the Hold signal, connected to the base of Q421. When the Hold signal or the $\overline{\text{End}}$ signal is low, the cathode of CR520 is held at approximately −5 V; this stops the

oscillator. When both signals are high, the oscillator runs. When the Dig 4 signal goes high the current available to charge C520 is increased and the pulse width shortens from 106 nanoseconds to 83 nanoseconds. This action occurs after the fourth digit or timeslot. See Figure 3-9.

The oscillator output and the $\overline{\text{End}}$ are "ANDed" in U630C, with the output taken from pin 8.

TIMING

The Clock Generator output drives 4-bit binary counter U135. The output lines are set to zero by the $\overline{\text{End}}$ pulse. The counter increments to binary eight and resets to zero in each digitizing cycle. The output from the four-bit counter drives the inputs of U230, a binary to one-of-eight decoder.

SUCCESSIVE APPROXIMATION REGISTER

This circuit, in conjunction with the Digital-To-Analog Converter and the Comparator, provides an eight bit digital word representing the vertical voltage. This word is sent to the memory through the Output Register. See Figure 3-10.

The circuitry consists of eight J-K flip flops. The K terminal is grounded and the J terminal connects to the comparator output. The common J line is also the least significant bit of the eight bit word. The $\overline{\text{End}}$ line connects to the reset terminal of the most significant bit flip flop, and to the set terminals of the remainder of the flip flops. At the start of conversion the $\overline{Q}$ of the most significant bit flip flop (U245B) is set high (the Q low) and the remainder of the $\overline{Q}$ terminals are low. The $\overline{Q}$ outputs from the flip flops form the digital word.

The comparator output switches high or low depending on the current from the digital to analog converter compared to the sample and hold output voltage. The J input level transfers to the Q output as the binary to digital decoder clocks each flip flop, starting with the most significant bit and ending with the least significant bit. See Figure 3-11. The $\overline{Q}$ output from each flip flop determines the digitally generated comparison voltage.

The clock signal to each flip flop resets the next (less significant) flip flop. This action progresses to the LSB flip flop (U130A) as the counter increments.

DIGITAL-TO-ANALOG CONVERTER

This circuitry consists of constant current transistors Q121C, Q226C, Q121E, Q226E, Q210, Q220, Q222 and Q224. The current steering transistors are Q121D, Q226D, Q121A, Q121B, Q226A, Q226B, Q211, Q312, Q221, Q320, Q223, Q323, Q225 and Q324. Bias voltage for eight of the current steering transistors and the constant current transistors is provided by divider R123, R124, R121 and CR123. A voltage of 2.1 V for the Channel Switch and D-to-A Converter is provided by Q110 in conjunction with this divider chain. Figure 3-10 shows a simplified block diagram of this circuit.

This circuitry operates by steering the different currents passing through the constant current transistors to either one side or the other of the comparator. The current steering continues until the input voltages are nearly balanced against he signal voltage from the Sample and Hold circuit.

COMPARATOR

The comparator, U330, compares the output of the Digital-To-Analog Converter with the output from the Sample and Hold circuitry.

CHANNEL SWITCH

This circuitry switches the output from the sample and hold gates for each channel to the comparator. The bases of Q330 and Q325 are high when channel 1 is selected, and low for channel 2. The bases of Q331 and Q332 are high when channel 2 is selected, and low for channel 1. The base voltages on the channel switch are such that, for the unused channel, the current flows through the diodes in the emitters of the channel switch transistors, through R432 and to the +5 V supply. Transistors Q310 and Q311 form a differential amplifier for the signal from the CH 1 Sample and Hold circuit, and Q321 and Q322 operate in the same manner for channel 2.

DIGITIZER OUTPUT REGISTER

Register U800 stores the digitial word from the A to D converter. The information on the D inputs transfers to the Q outputs on the low to high clock transition. The clock signal is the least significant digit output, Y7, from the one-of-eight decoder, U230. This signal passes through buffer U940A. All outputs are set low when the reset line at pin 1 of U800 goes low.

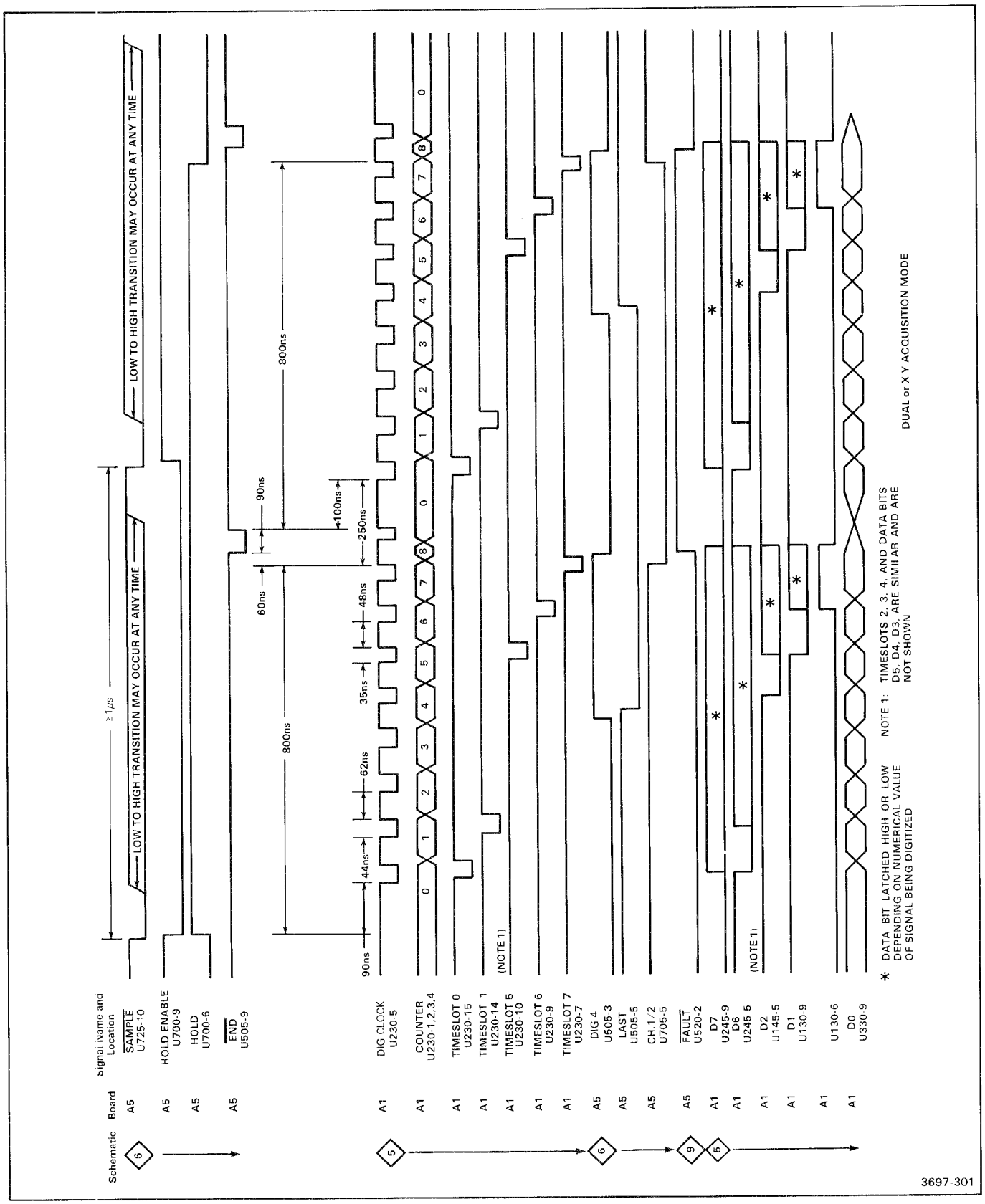


Figure 3-9. Digitizer waveform diagram.

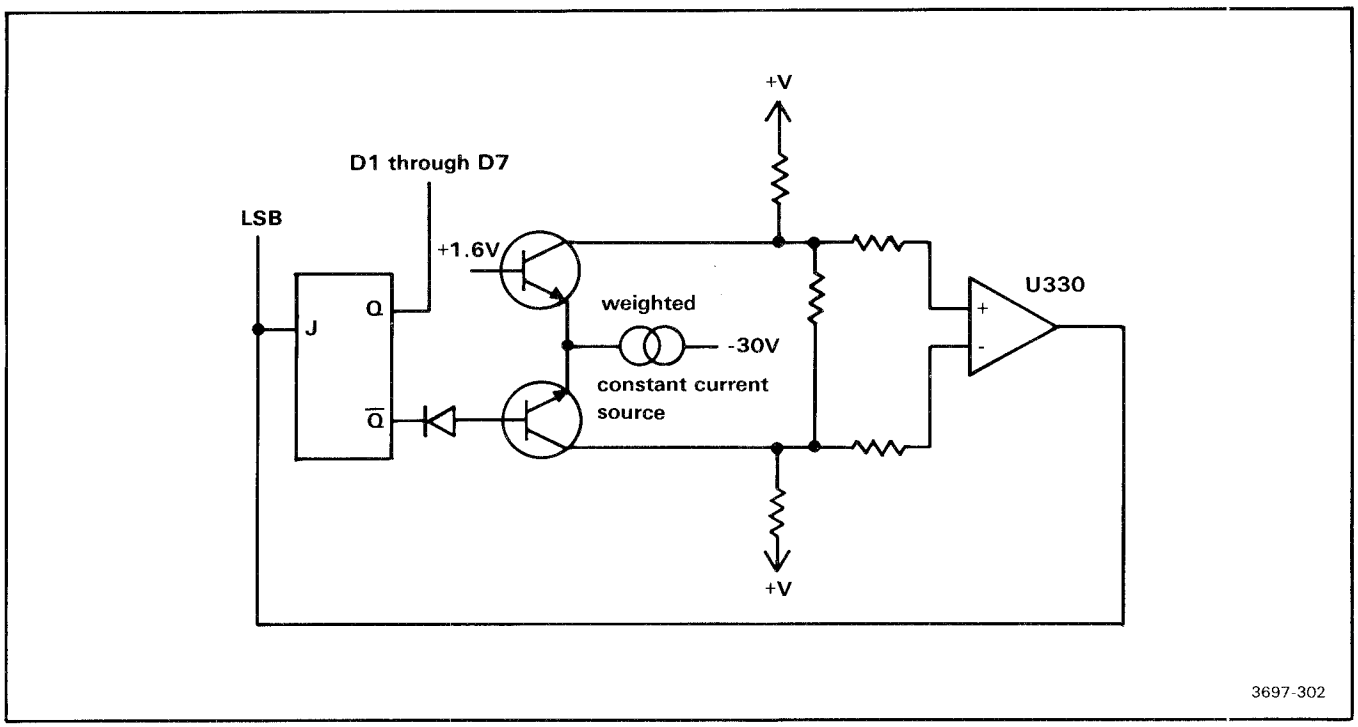


Figure 3-10. Simplified successive approximation register and digital to analog converter.

6 TIMEBASE AND DIGITIZER CONTROL

1 MHz OSCILLATOR

The sampling oscillator is a Boze (emitter-coupled) oscillator composed of Q610 and Q611, along with output inverter U630D. The frequency of this oscillator is 1 MHz with the front-panel CAL control in the CAL position. The 1 MHz frequency is accurately set (when R621 is in the fully clockwise position, presenting no resistance in the circuit) by R612. When the CAL control is adjusted from the detent position, the current available to charge capacitor C600 is reduced, lowering the frequency of the oscillator to about 300 kHz. This action provides at least a 2.5 to 1 ratio for the time per division rates between steps. The feedback capacitor is C600. Diode CR610 prevents the collector of Q611 from going more negative than -0.6 V. The signal appearing at pin 11 of U630D is a modified square wave.

TIMEBASE ÷ N

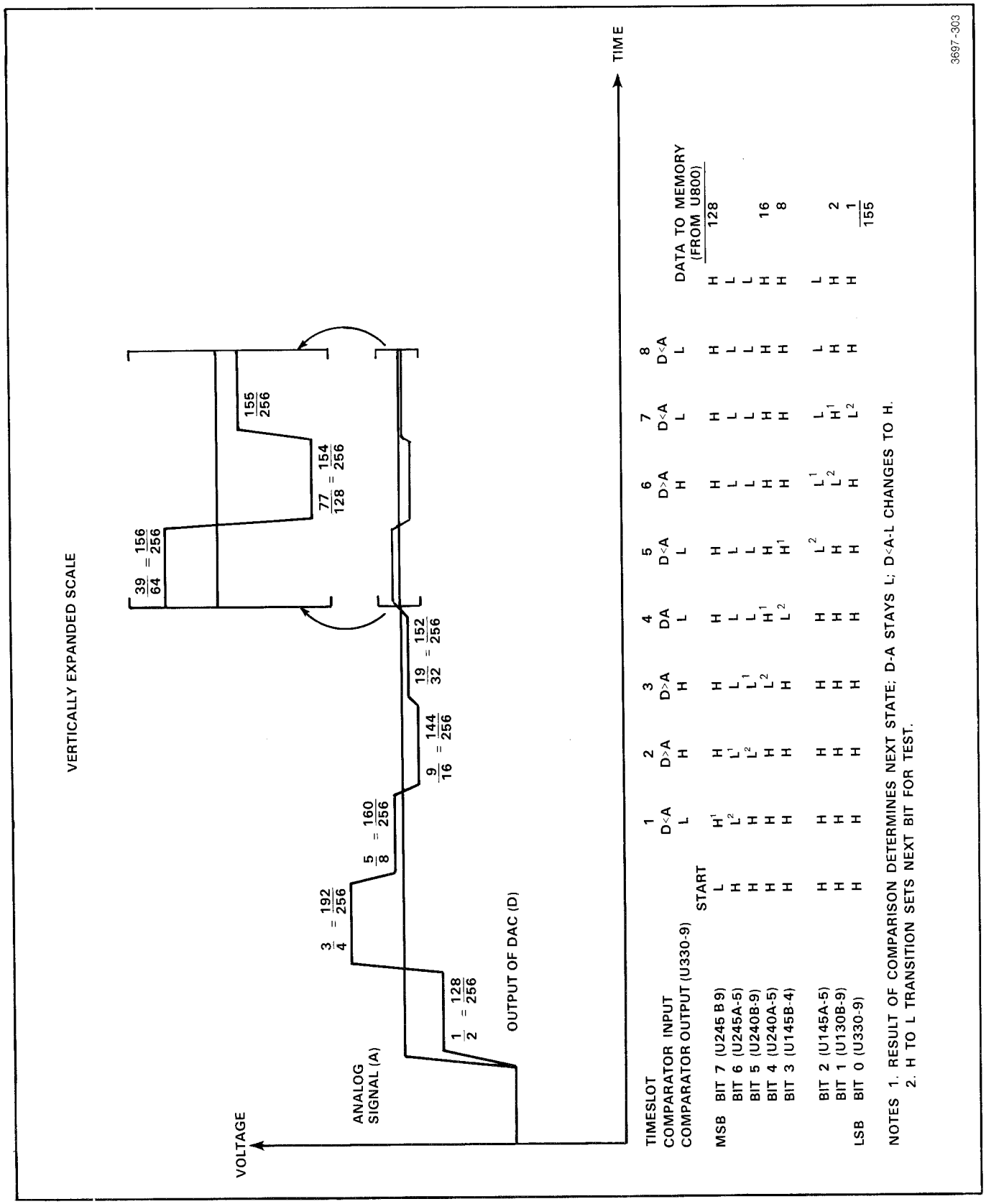
The clock signal from U630 is applied to U441A and U440. Integrated circuits U441, U540, and U541 divide the clock signal in decade steps. The output from U541A is the clock signal divided by 100,000. The outputs from this decade counter feed to the inputs of U440, a data selector. When the ERASE line goes high, the decade counters reset and all outputs go low.

The Y output from the data selector, U440, is the clock frequency for U541B, a divide-by-two (pin 13) and divide-by-five (pin 9) counter. These outputs feed data selector U340. The Erase pulse at pin 14 resets U541B (all outputs low). Depending on the SECONDS/DIV switch setting, the output of U340, pin 5, is the selected time-per-division divided by 100. For example, if S320 is set to 50 seconds per division, the period of the output from U440 is 0.1 seconds, and the output from U340 is one sampling pulse per 0.5 seconds. This is the SECONDS/DIV switch setting of 50 divided by 100.

In the external mode, pin 12 of U440 connects to pin 5, then to pin 12 of U340 and to pin 5 of U340. In this mode the sampling rate is the rate of the external seconds per division input signal.

EXT INPUT

A positive-going signal at the EXTERNAL SEC/DIV bnc connector causes the collector of Q150 to go low. This causes pin 6 of U440 to transit from low to high when the SECONDS/DIV switch is in the EXT position.



TIMESLOT		1	2	3	4	5	6	7	8	DATA TO MEMORY (FROM U800)
COMPARATOR INPUT		D<A	D>A	D>A	DA	D<A	D>A	D<A	D<A	
COMPARATOR OUTPUT (U330-9)	START	L	H	H	L	L	H	L	L	128
MSB	BIT 7 (U245 B 9)	L	H^1	H	H	H	H	H	H	H
	BIT 6 (U245A-5)	H	L^2	L^1	L	L	L	L	L	L
	BIT 5 (U240B-9)	H	H	L^2	L^1	L	L	L	L	L
	BIT 4 (U240A-5)	H	H	H	H^1	H	H	H	H	H 16
	BIT 3 (U145B-4)	H	H	H	L^2	H^1	H	H	H	H 8
	BIT 2 (U145A-5)	H	H	H	H	L^2	L^1	L	L	L
	BIT 1 (U130B-9)	H	H	H	H	H	L^2	H^1	H	H 2
LSB	BIT 0 (U330-9)	H	H	H	H	H	H	L^2	H	H 1
										155

NOTES 1. RESULT OF COMPARISON DETERMINES NEXT STATE; D-A STAYS L; D<A-L CHANGES TO H.
2. H TO L TRANSITION SETS NEXT BIT FOR TEST.

Figure 3-11. Operation of successive approximation register D to A converter and comparator.

Hysteresis develops in the circuit by positive feedback through Q150, U440, and R154.

DIGITIZER CONTROL

This circuitry generates logic signals to control the digitizer circuitry. Refer to Figure 3-9 for waveforms. The sample pulses, at a rate of 100 per SECONDS/DIV switch setting, operate OR gate U725C. The other input to this gate is the microprocessor SAMPLE signal. This signal comes from the microprocessor, and is used for some self test functions and other specialized functions.

A high to low transition on pin 10 of U725C clocks flip flops U700B and U700A. When pin 10, $\overline{\text{Erase}}$, of U700B goes low pin 9 goes high. Pin 9 of U700B is the hold enable signal. This line is high during sampling in the single trace mode and toggles in the dual-trace mode on alternate sampling pulses. This toggling is caused by the Dig Dual/Sgl signal connected to the K input, pin 12, of U700B. This signal is high in the dual trace mode and low in the single trace mode. The remaining inputs to U700B not yet described are the J input and the reset input. The J input is always high. The reset input, pin 14 is the $\overline{\text{Loadstop}}$ signal. This signal inhibits the digitizer when signals are not being digitized.

The Q output, pin 9, of U700B connects to the K input of U700A. The preset to this flip flop is low when the timeslot 7 line from the Timing circuitry goes low. This action ends the digitizer conversion cycle by placing a low on the $\overline{Q}$ output, pin 6. The J input to this flip-flop is always low. The clock signal is the sampling pulse from U725C. The K signal is the Q output from U700B. When this input is low the output states of U700A do not change with the sample pulse (clock) signal. This action causes the sampler to either recognize or ignore a sample pulse.

The channel switches, as previously described, are operated by flip flop U705A in conjunction with U605D, U605C and U600E. The signal driving U600E, an inverter, is Dig 1/2. This signal is high to digitize channel 1 first in the Dual Trace or X-Y modes, or to digitize only channel 1 in the Ch 1 or Add modes. This signal is low to digitize channel 2 only in the Ch 2 mode. With this signal high, the output of U605D is low during the sampling time. This places pin 5 of U705 high and pin 6 low and selects channel 1. Conversely, with pin 11 of U600E low, pins 10 of U600E and U605C are high during sampling time, causing a reset on U705A. Pin 5 of U705A is now low and pin 6 high, selecting channel 2.

Flip flop U505A generates the $\overline{\text{Last}}$ and the reset signal for U700A. This action, through U700A, prevents $\overline{\text{TS7}}$ from ending the digitizing sequence after one cycle in the dual or X-Y mode. In the single trace mode pin 4 of U505A is low. This presets U505A generating the $\overline{\text{Last}}$ at pin 6. In the dual trace mode pin 4 of U505A is high. When channel 1 is being digitized the CH 2/1 line from U705A is low. When the Dig 4 line goes high, this low is clocked to the Q output (pin 5), preventing the end of the digitizing sequence until channel two is digitized. If however, channel 2 is being digitized, the D input to U505A is high. This causes the Q output, pin 5, to go high allowing the next $\overline{\text{TS7}}$ pulse to end the digitizing sequence. Reset for this flip flop is the $\overline{\text{F EN Clr}}$ signal from U500, pin 6, on schematic 3. This signal is used in self test only.

$\overline{\text{End}}$, a short pulse at the end of the conversion cycle, is generated by U505B. When the $\overline{\text{TS7}}$ line goes high, $\overline{Q}$ goes high. This causes a high to low transition at pin 10 of U505B, which presets U505B and makes it ready for the next time slot $\overline{\text{TS7}}$ pulse to trigger the flip flop. The width of $\overline{\text{End}}$ is set by R500 and C500. The reset for this flip flop is connected to +5 V through R610. This disables the reset permanently.

LEFT PLUG-IN CHANNEL SWITCH LOGIC

This circuitry controls the channel switch in the left plug-in, when a dual-trace plug-in is being used, and prevents a crt display of the left plug-in's output signal. Two different designs of interface board have been used in 5100-series mainframes; the 5D10 operates differently with the different mainframes. "Old" interface boards are used in 5110, 5111, 5112, 5113, and 5115 mainframes. "New" interface boards are used in 5111A mainframes. The 5D10 circuitry and the mainframe circuitry for the "new" and "old" mainframes are illustrated together in Figure 3-12 and Figure 3-13.

Waveforms and troubleshooting information are included in the Maintenance section.

Use of the left plug-in is not recommended with 5200 or 5400 series mainframes.

Operation With "Old" Interface Board

The 5D10 senses an "old" interface board by the absence of voltage on Horizontal plug-in interface connector contact A6. Q1010 is therefore off, and a high appears at inputs of U1000 and U1020.

The output of U1000B is driven low. This forces the mainframe's vertical channel switch flipflop (U640C-U640D) to drive the vertical channel switch to display only the output from the right vertical plug-in (5D10

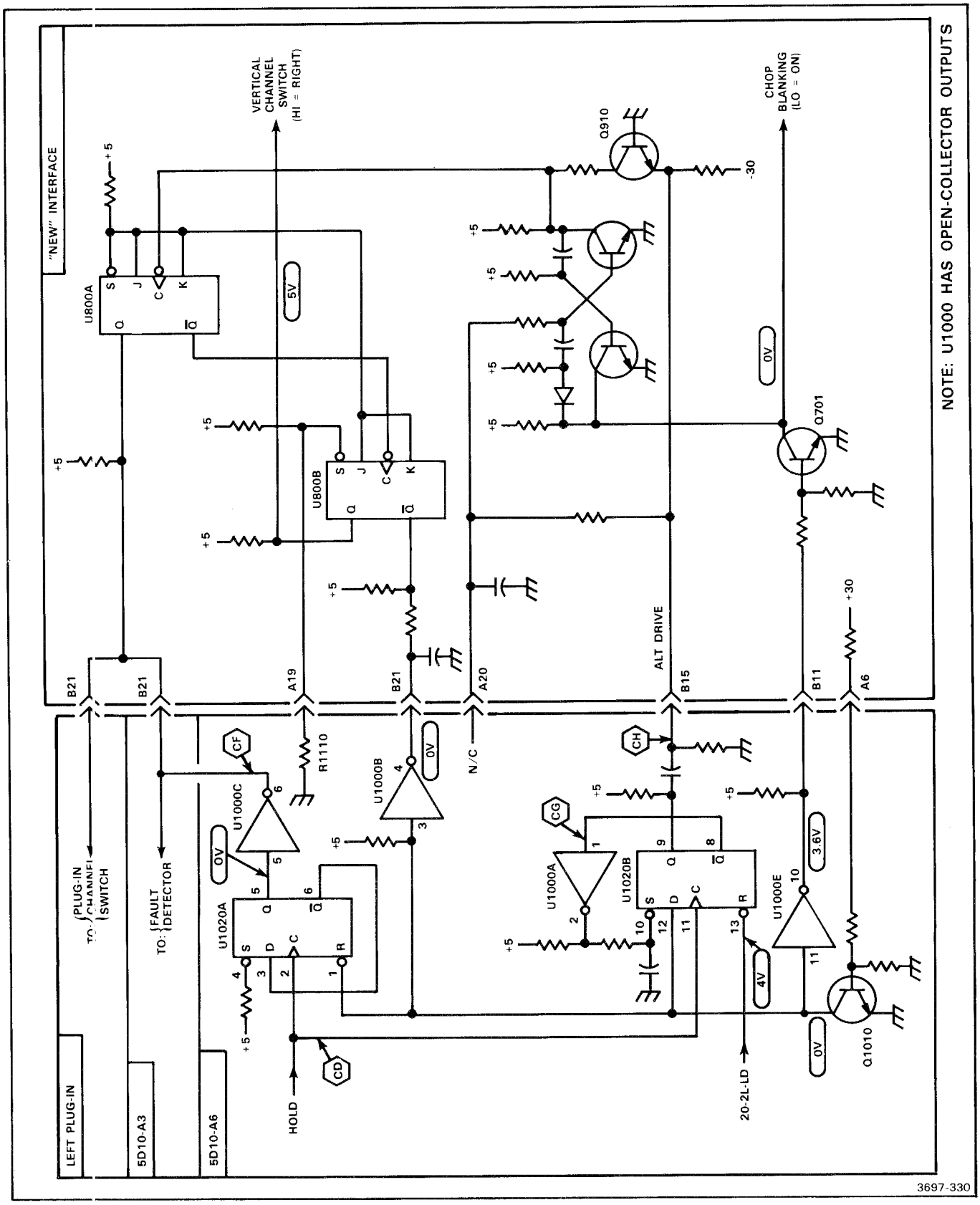


Figure 3-12. 5D10 Left plug-in channel switching "new" mainframes.

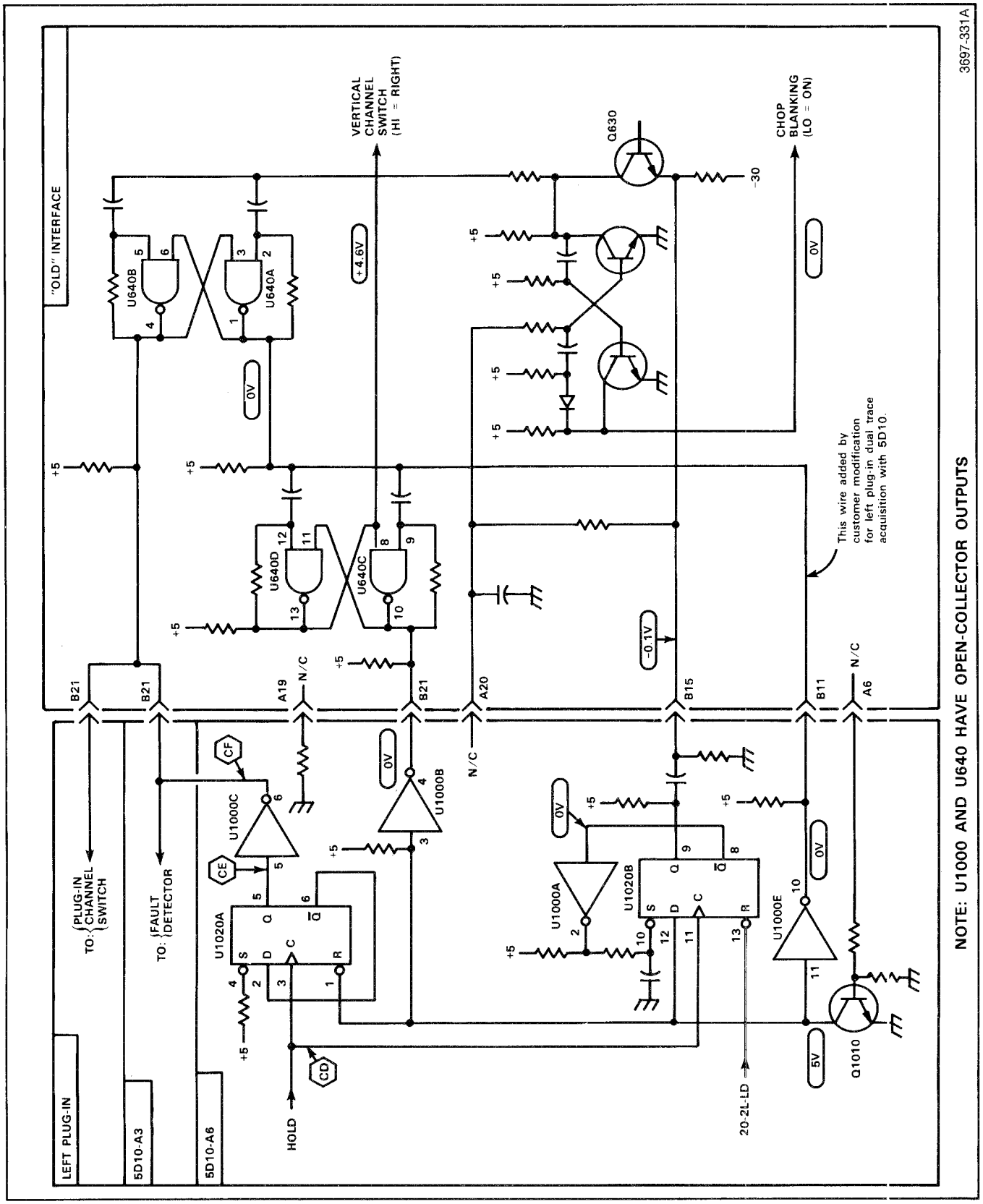


Figure 3-13. 5D10 Left plug-in channel switching, "old" mainframes.

vertical signal), and not the output from the left vertical plug-in. (Signals from the left vertical plug-in can be observed only after having been acquired by the 5D10.)

The output of U1000E is driven low. This disables the mainframe's plug-in channel switch flipflop (U640A-U640B). Because U640 is an open-collector gate, Plug-in Channel Switch (contact B21 at both Left and Right Vertical plug-in interface connectors) can be driven by open-collector gate U1000C.

The reset input of U1020A is high, allowing U1020 to toggle on every positive-going transition of HOLD. Immediately after each digitizing cycle begins, U1020 changes state, driving Plug-in Channel Switch to select the other channel of the Left Vertical plug-in for the next sampling and digitizing cycle.

The D input of U1020B is high, preventing activity on the Alternate Drive signal to the mainframe.

The mainframe chop oscillator is inactive.

Operation With "New" Interface Board

The 5D10 senses a "new" interface board by the presence of voltage on Horizontal plug-in interface connector contact A6. Q1010 is therefore on, and a low appears at inputs of U1000 and U1020.

The open-collector output of U1000B is disabled, to prevent shorting the output of U800B. Horizontal plug-in interface connector contact A19 is grounded through R1110, asserting the set input of U800B. This causes the mainframe's vertical channel switch flipflop (U800B) to drive the vertical channel switch to display only the output from the right vertical plug-in (5D10 vertical signal), and not the output from the left vertical plug-in. (Signals from the left vertical plug-in can be observed only after having been acquired by the 5D10.)

The D input of U1020B is low. When the left plug-in is operating in the dual-trace mode, and its output is being acquired by the 5D10, the reset input of U1020B is high. Both of these conditions allow U1020B to operate as a one-shot, generating a pulse on the Alternate Drive line after every positive-going transition of HOLD. The Alternate Drive pulse causes the mainframe's plug-in channel switch flipflop (U800A) to toggle. Thus, immediately after each digitizing cycle begins, U800A changes state, driving Plug-in Channel Switch to select the other channel of the Left Vertical plug-in for the next sampling and digitizing cycle.

The reset input of U1020A is low, causing the Q output to be low, disabling the output of open-collector gate U1000C. This prevents the output of U800A from being shorted.

The input of U1000E is low, disabling its open-collector output. This allows Q701 to turn on, disabling the mainframe chop oscillator.

7 TRIGGERING

SOURCE SELECT, COUPLING AND INPUT BUFFER

This circuitry selects and buffers the triggering signal. See Figure 3-14. Switch S211 selects the desired source for the triggering signal. Lamp DS4 limits the input current for the EXT source. A constant 1 MΩ input impedance for the triggering signal is provided by R111. This resistance is ac compensated by R110 and C110.

An operational amplifier with a virtual ground at pin 2 is formed by U200 and associated components. This unity gain amplifier inverts the triggering signal. The feedback resistor is R203. Ac compensation for this resistor is provided by C200. Should the input signal overdrive U200, a feedback circuit composed of diodes CR211, CR210, CR100 and CR101 limits the output voltage. Voltages for diodes CR211 and CR210 are set by R201, R202, R212 and R213.

COMPARATORS AND ONE SHOT

See Figure 3-15. The triggering signal is fed to the negative input of U300A, the minus slope comparator, and the positive input of U300B, the plus slope comparator. The outputs from these comparators are OR'ed to provide the clock signal for one shot flip flop U330A.

The comparison voltage for U300A is applied to R403 and the plus input of U300A. The comparison voltage for U300B is applied to R410 and the minus input of U300B. The comparison voltage range is ±2.5 V in plus and minus slope, and 0 V to +2.5 V and 0 V to −2.5 V in the bislope mode. Hysteresis is provided by R403 and R402 for the minus comparator, and by R311 and R312 for the plus comparator. This hysteresis is necessary to prevent trigger jitter (oscillations in the comparator circuitry) when the triggering voltage is near the threshold voltage. Input protection for the comparators is provided by CR301, CR302, CR411 and CR410. The minus comparator is enabled when Q300 conducts. This occurs when the minus slope switch is pressed. When the plus

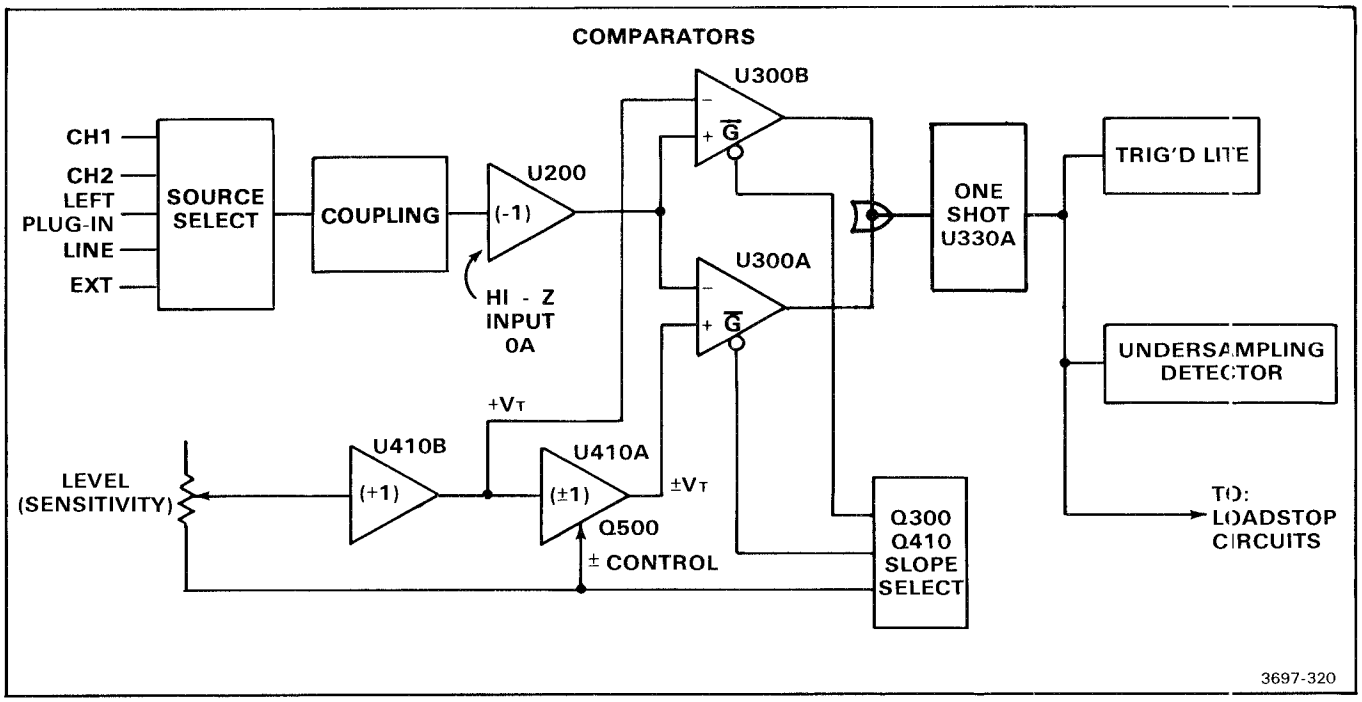


Figure 3-14. Triggering block diagram.

slope switch is pressed Q410 conducts and U300B is enabled. Both comparators are enabled in the BI-SLOPE mode.

The negative-going triggering signal from the comparators clocks one-shot flip flop U330A, and causes the Q output to go low. The Q output goes high after about 60 ns, determined by the time constant of R230 and C221. This creates a positive-going pulse at the $\overline{Q}$ output, pin 6, of U330A. The $\overline{\text{We Cir}}$ and the $\overline{\text{F=N}}$ signals are used for self test only, and are high during normal operation.

SLOPE SELECT

This circuitry selects the comparator for triggering on the plus, minus or both slopes. When the minus slope is selected, +30 V is present through the plus slope switch S901A and the minus slope switch S901B to the LEVEL potentiometer. The base of Q300 is disconnected from ground and Q300 conducts. When the plus slope is selected, the base of Q410 is disconnected from ground and Q410 conducts. When the plus slope is selected, +30 V is connected to the LEVEL potentiometer through the minus slope switch. When BI-SLOPE triggering is selected the LEVEL control connects to ground through CR809; the bases of Q410 and Q300 are released from ground and both comparators are enabled.

THRESHOLD LEVEL

This circuitry provides the plus and minus comparison voltage for the trigger comparators. Comparison voltage for the plus comparator is provided by U410B. Comparison voltage for negative comparator is provided by U410A. As the LEVEL control is varied from stop to stop, when either the plus or minus triggering is selected, the voltage at the input of U410B varies. This provides an inphase output voltage of about ±2.5 V at pin 7 of U410B. See Figure 3-16.

When either the plus or minus slope is selected FET Q500 conducts. The output of U410B also feeds through Q500 to the + input of U410A. This in turn provides comparison voltage for the − slope comparator. The gain of U410A is unity (+1). In the BI-SLOPE mode, FET Q500 is off as its gate is at −10 V. This causes the signal feed path to occur at the minus input of U410A. Amplifier U410A has a gain of −1. As a result, the level control provides plus and minus comparison voltages at equal amplitudes but opposite polarity.

TRIGGERED INDICATOR

This circuitry provides an indication of proper triggering. Flip flop U330B, in conjunction with Q250, forms a pulse stretcher that turns the TRIG'D light on for about one third of a second, irrespective of the trigger rate. See schematic 7 for waveforms associated with this circuitry.

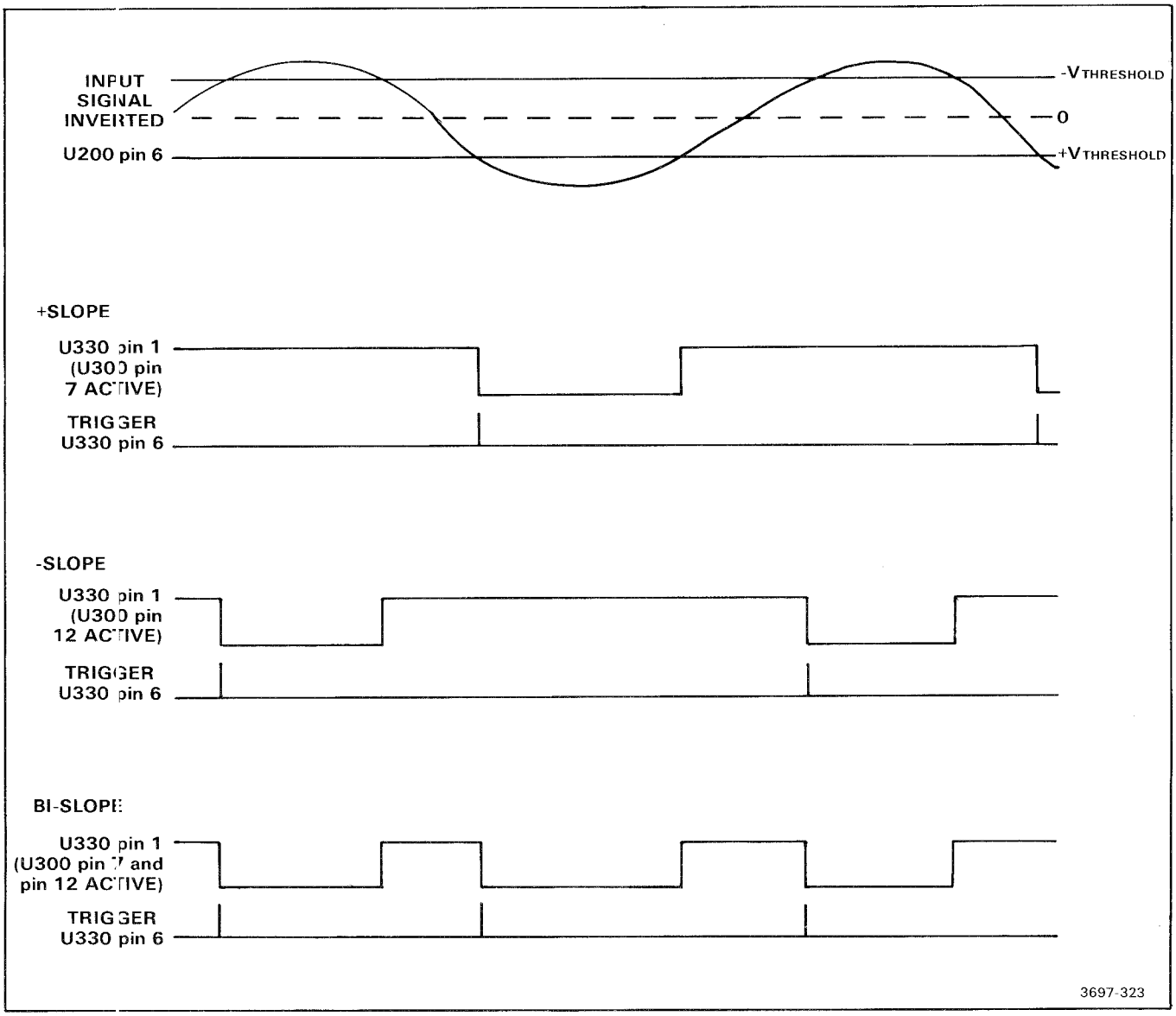


Figure 3-15. Typical triggering waveforms.

The trigger pulse from U330A clocks flip flop U330B. Pin 7 of U330B goes high as the J input connects to ground and the K input is high. This positive-going pulse turns Q250 on, thereby discharging C250. When the base of Darlington transistor Q140 reaches about 3.8 V, Q140 turns on and the TRIG'D light illuminates. When the voltage at the collector of Q250 reaches 1.4 V the preset, pin 10 of U330B, lowers the $\overline{Q}$ output. The base of Q250 is still at about 0.6 V and starts toward ground. The time constant for this discharge is determined by R340, R250, and C250. The collector commences toward +5 V, operating as an integrator. When the collector reaches about +3.8 V Q140 stops conducting and the TRIG'D light goes out. If the triggering signal occurs more frequently than about one-third second the TRIG'D light remains continuously on, as C250 does not have sufficient time to discharge between trigger pulses.

UNDERSAMPLING INDICATOR

This circuitry compares trigger pulses and sampling pulses to detect possible undersampling. The criterion for possible undersampling is less than eight samples per waveform cycle.

The sampling pulses connect to pin 9 of U625C. Pin 10 of U625C is high during normal operation unless the counter reaches a count of eight, or is reset to nine. ($\overline{\text{We}}$

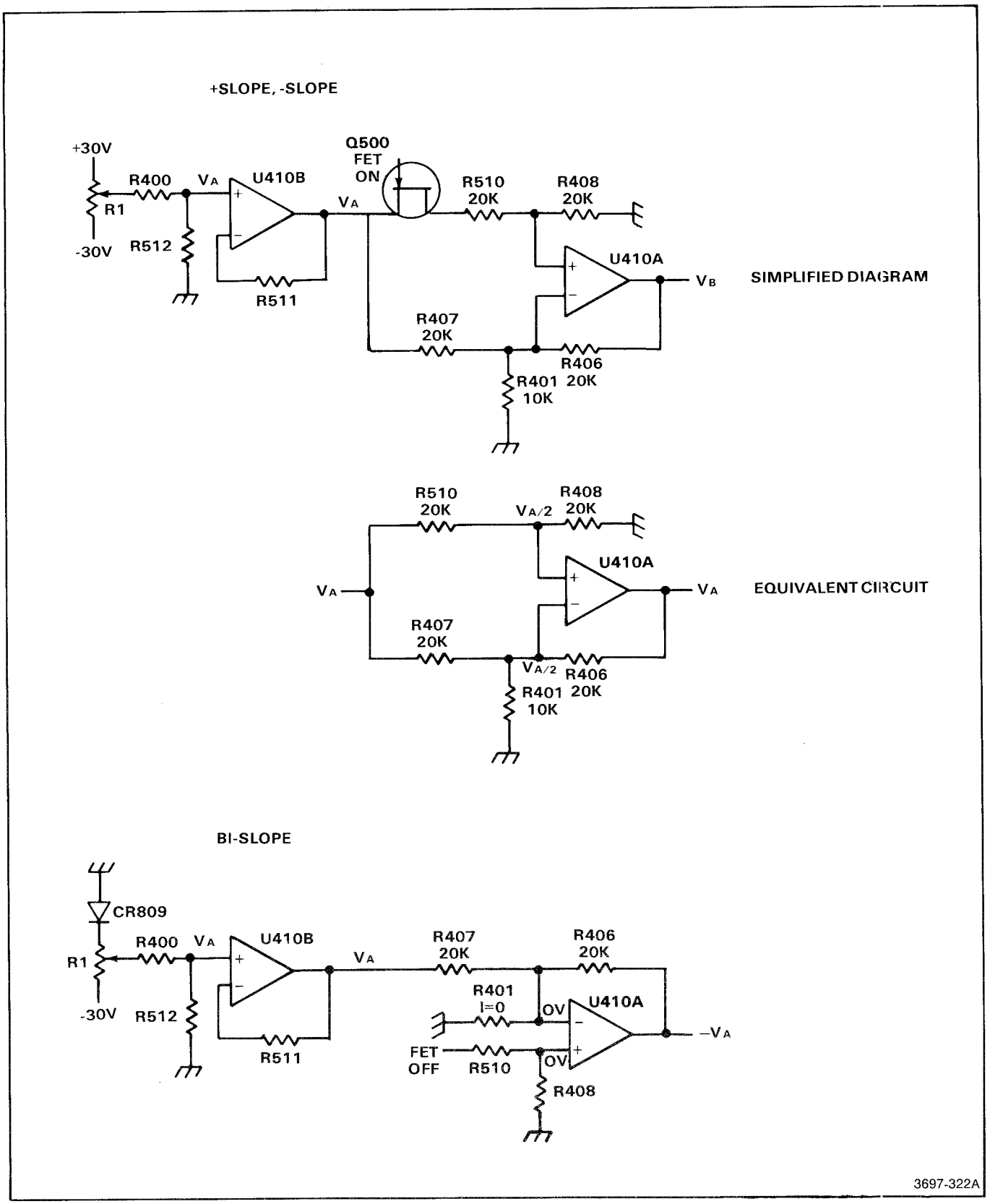


Figure 3-16. Simplified diagrams and equivalent circuit for Threshold Level circuitry.

$\overline{\text{Set}}$ is high in all modes except self test and signature analysis.) The Sample pulses increment the counter. If eight Sample pulses occur before a trigger occurs, pin 9 of U627B goes high, setting U610A and turning off the POSSIBLE UNDERSAMPLING light. If a trigger pulse occurs before eight sample pulses occur, the counter is reset and the D input of U610A is clocked to the Q output, illuminating the POSSIBLE UNDERSAMPLING light. See Figure 3-17. The Erase signal sets the counter to nine. This presets Q610A and turns off the POSSIBLE UNDERSAMPLING light (if it was on) by raising pin 5 of U610A.

VIEWTIMER

This circuitry generates the Erase pulses. When the Loadstop signal goes high, Miller integrator, Q820, starts to conduct. The collector of Q820 moves in a negative direction from +15 V. The time necessary for the collector of Q820 to reach +4.4 V (the conduction voltage for Q911) is determined by the setting of the VIEWTIME control and the value of C821. See schematic 7 for waveforms associated with this circuitry. If the ERASE button is pushed, the collector of Q820 immediately drops below +4.4 V.

When Q911 conducts, a low appears at pin 11 of U225E. The falltime of the waveform at pin 11 of U225E is decreased and hysteresis is provided by CR811 and R813. This pulse is inverted by U225E generating the Erase pulse. The $\overline{\text{Erase}}$ pulse is generated by U225D. The μP Erase pulse generates the Erase pulse by causing Q910 to conduct. The Save All pulse inhibits the Viewtimer by raising the emitter voltage to Q910.

LOADSTOP LOGIC

This circuitry stops the loading of data into the waveform memory at the proper time. It also stops the write cycles and indicates that data acquisition is complete. No detailed description is provided because troubleshooting is done by signature analysis.

8 MEMORY ADDRESSES

For an overall view of the entire memory system refer back to Figure 3-4. Detailed description is not provided because troubleshooting is done by signature analysis.

MEMORY ADDRESS SELECTOR

This circuitry selects the waveform memory address for reading or writing. When the select inputs are high the addresses transmitted are write addresses. When the select inputs are low the addresses transmitted are read addresses.

SCRATCHPAD

This circuitry saves the addresses of the trigger point, and the last point, for reference and new waveforms. Inputs to this circuitry are the time the trigger event occurred, the time when the Loadstop signal went high, and the write address.

READ ADDRESS REGISTER

This circuitry contains the read addresses for the waveform memory.

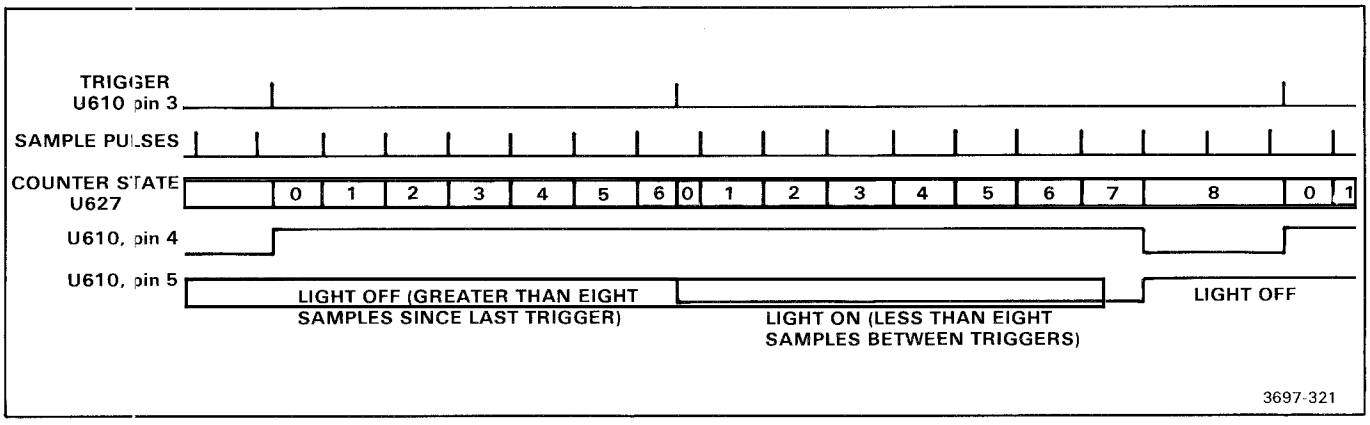


Figure 3-17. Waveforms associated with the Undersampling Detector.

N2 MODIFIER

The N2 data bit is modified (read address modified) for certain waveform display conditions.

B SELECTOR

This circuitry selects the memory address bus or Numbers bus for output to the Adder circuitry.

A SELECTOR

This circuitry selects either the output of the Read Address register or the output of the Time Register and applies these data to the Adder.

MEMORY DATA SELECTOR

The circuit selects the E lines or the N lines and supplies them to the memory data inputs, and the X and Y display registers.

ADDER

This circuitry adds the 12 bit A word, the 12 bit B word, and the one bit carry (C), and outputs the sum to the Time Register, the Read Address Register, and the Loadstop Logic.

WAVEFORM MEMORY

This circuitry stores the binary words representing the values of the acquired signals.

TIME REGISTER

This register stores the time data for Y-T displays (time as the X dimension).

9 WRITE ADDRESS COUNTER

This circuitry increments the write addresses for the Waveform Memory each time a waveform data byte from the digitizer has been stored.

Under certain conditions, during dual-channel signal acquisition, a channel's memory locations can mix with the other channels locations. This possible fault is checked and corrected for by U900A, U900B, in conjunction with U940C, U520A and U525C.

The status of the plug-in channel switches is checked by U900A and U900B during each write operation under the following four conditions:

1. Erase asserted,
2. WG 12 and W0 asserted,
3. WG 4 and W0 and W1 asserted,
4. W0 and W1 and W2 asserted.

The above conditions cause the Group signal to go high. Flip flop U520A is clocked at the end of write group by S7. If the $\overline{\text{Fault}}$ is unasserted, U525C is enabled and the Write Address Counter increments. If the Fault signal is low, U525C is disabled, stopping the Write Address Counter from incrementing.

The $\overline{\text{Fault}}$ goes low when the Plug-In Channel Switch signal at pin 2 of U900A is low, or $\overline{\text{Last}}$ is high, during $\overline{\text{TS7}}$ time (end of digitizing cycle). The Plug-In Channel Switch and the $\overline{\text{Last}}$ signal connect to the D inputs of U900A and U900B respectively. Both flip flops are clocked by the $\overline{\text{TS7}}$ signal.

If the Dig Dual/Sgl is low (single trace) U900B is disabled. If two traces are not being acquired from the left plug-in, then 20.2L.LD is not asserted and U900A is disabled. The $\overline{\text{Disp Swp Mgf}}$ is high during normal operation.

WRITE ADDRESS MODIFIER

This circuitry modifies bits W0 through W2 of the write address, when a reference waveform has been saved.

10 READ AND WRITE CONTROL

This circuitry provides direct control of the waveform memory. During acquisition the Waveform Memory is successively written to, and read from. When acquisition is not occurring, the Waveform Memory is only read from. See Figure 3-18.

SYNCHRONIZE EXTERNAL REQUIREMENTS

This circuitry synchronizes the external inputs that affect memory operation. These include the 10 MHz clock frequency, input from the microprocessor, and the digitizer. The 10 MHz clock frequency varies by plus or minus 5% to time the vector displays. (Digitizer timing is independent of vector display timing.) Internal delays in the microprocessor, depending on the operation performed, are compensated for in this circuitry.

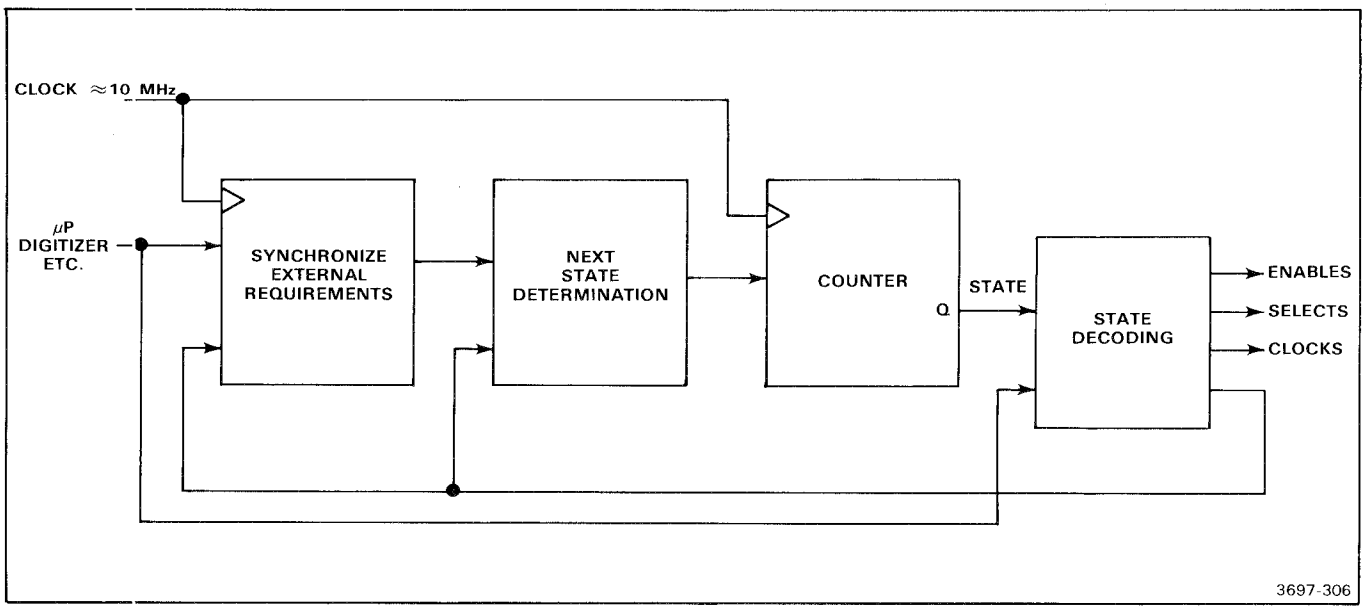


Figure 3-18. Read and write controller block diagram.

NEXT STATE DETERMINATION

The output from the external requirements circuitry and the present state of the Counter determine the next Counter state.

COUNTER

This circuitry consists of four bit synchronous counter, U115. This counter times the memory events. The sequence of states and the transition commands are shown in Figures 3-19, 3-20, and 3-21.

STATE DECODING

This circuitry takes the output of the Memory Controller and decodes these signals into enables, selects and clocks for the memory.

11 DISPLAY REGISTERS, DACS AND TIMER

The purpose of this circuitry is to convert the binary data stored in memory to specific dots on the cathode-ray tube and to connect these dots (vectors) for a continuous trace. The X and Y channels, as shown on the schematic, relate to the horizontal and vertical dimensions of the cathode-ray tube respectively. As the two channels are virtually identical to each other, only the Y channel is described in detail.

X AND Y REGISTER CLOCKS

This circuitry provides clock signals to update the contents of the display registers.

X DISPLAY REGISTER

These flip flops store the binary word representing the X dimension for application to the D-to-A Converter. The Time register is the data source for YT displays. Waveform memory is the data source for XY displays.

Y DISPLAY REGISTER

These flip flops store the binary word representing the Y dimension for application to the D-to-A Converter.

D-TO-A CONVERTERS

Binary words from the display registers are converted into varying currents by U410 for the Y channel and U520 for the X channel. The D-to-A Converter for the Y channel is an 8 bit DAC with 2 mA output for full scale operation. The D to A converter for the X channel is a 10 bit DAC with 4 mA full scale output. Calibration or gain setting is accomplished by R351 and R352.

The output from U410 or U520 is a current, varying with the value of the binary word in the display registers. The output current from U710D is summed with the output of the DAC. When the front-panel control TRACE SEP is out, a high exists on the input of U710D. This causes a low at the output of U710D. No current is added to the summing junction of operational amplifier U530. If the

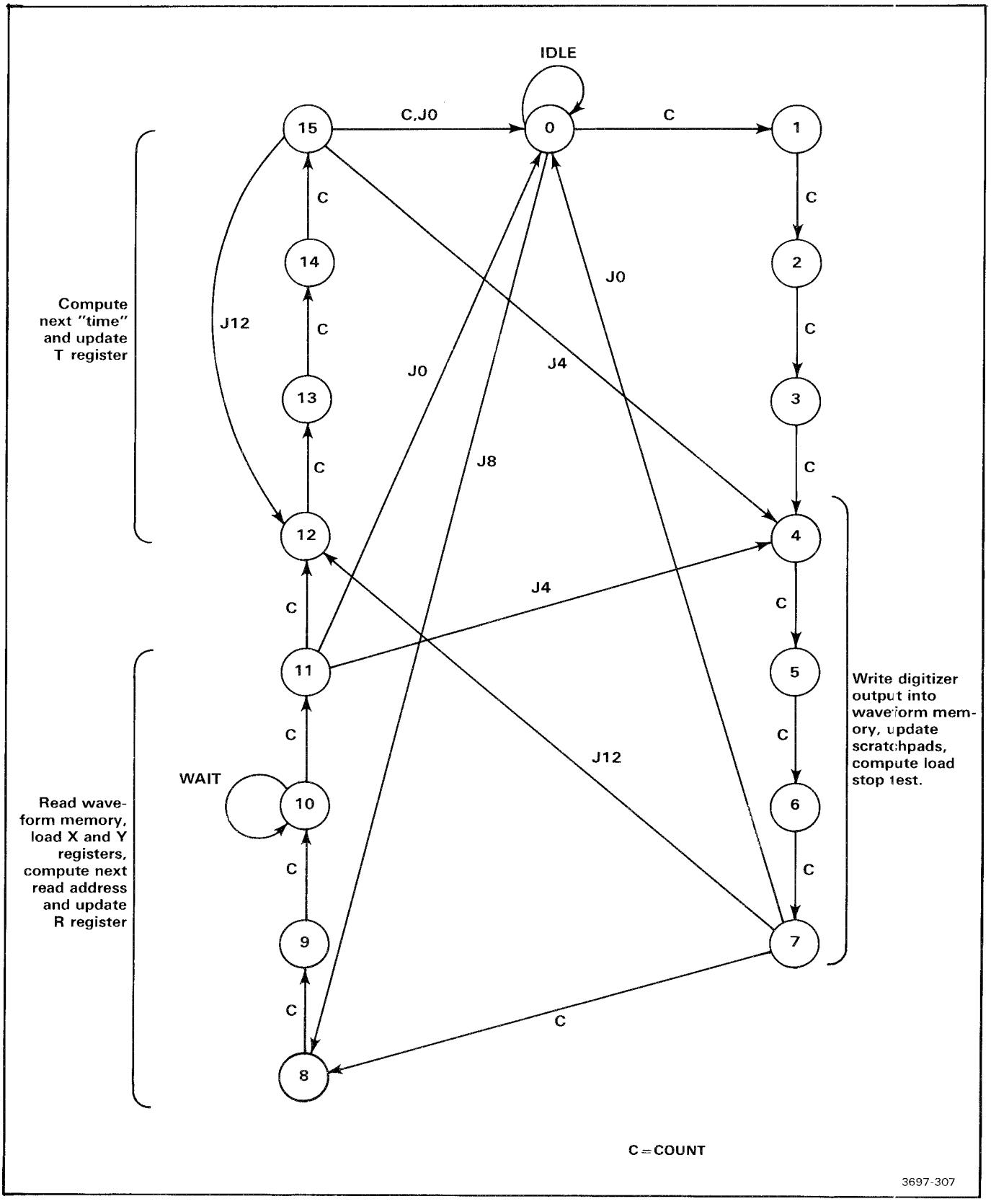


Figure 3-19. Memory controller state transition diagram.

CONTROL SIGNAL	ASSERTED BY PRESENT CONDITION	NEXT STATE
IDLE	S0, no READ REQUEST, no WRITE REQUEST	S0
J0	S7 (end of write cycle), no READ REQUEST, no TIME REQUEST, or: S11 (end of read cycle), WRITE REQUEST, but not requested prior to S10, or: S15 (end of time cycle), WRITE REQUEST, but not requested prior to S14.	S0
J4	S11 (end of read cycle), WRITE REQUEST, waiting since S9, or: S15 (end of time cycle), WRITE REQUEST, waiting since S13.	S4
J8	S0 (idle state), READ REQUEST, no WRITE REQUEST	S8
J12	S7 (end of write cycle), TIME REQUEST, or: S15 (end of time cycle), MAGNIFIED DISPLAY, 10th time cycle not completed.	S12
WAIT	S10 (middle of read cycle), FETCHing memory data or address to microprocessor, microprocessor not finished with read operation.	S10

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Figure 3-20. Memory controller state transition (jump) commands.

TRACE SEP control is pressed, sufficient current is added to shift the trace 0.8 division, when a reference trace is displayed.

The operation of the X-Y shift signal through U710F is similar. During a Y-T display the end of the trace is displayed at the rightmost graticule line. However, during X-Y display, the display is centered.

The Display Character signal activates U710B. This action shifts both the horizontal and vertical trace positions during character display times.

The varying current from each D to A converter is changed to a voltage by U530 and U425. The output from U410 is 0 to a plus current. R501 adds an offset current giving a ± current change to the input of U530. All lows at the input of the D-to-A Converters places the trace below the screen bottom while all highs places the trace above the screen top. When the most significant bit is high, and the others low, the current from the D-to-A Converter is equal to the current from R501 and R302 and there is 0 V output from U530 and U425.

The feedback resistors for the X and Y DACs are different. The maximum full scale input current for U530 is 2 mA and for U425, 4 mA. Therefore, R302 and R407 are one-half the value of R501 and R533.

Attached to the output of the voltage to current converters is a comparator, U610C. This is used only for self-test during power-up. The output of this comparator tells the microprocessor that the DACs are working.

IDLE = S0 AND $\overline{WR}$ AND $\overline{RR}$
WAIT = S10 AND FETCH AND (μP not finished reading M or F)
C COUNTS IF $\overline{IDLE}$ AND $\overline{WAIT}$ AND $\overline{J0}$ AND $\overline{J4}$ AND $\overline{J8}$ AND $\overline{J12}$
J0 = [S7 AND $\overline{RR}$ AND $\overline{TR}$] OR [S11 AND WR AND $\overline{WW}$] OR [S15 AND WR AND $\overline{WW}$] (from table, with redundancy)
J0 = [S7 AND $\overline{RR}$ AND $\overline{TR}$] OR [(S11 OR S15) AND (WR AND $\overline{WW}$)] (implemented)
J4 = (S11 AND WW) OR (S15 AND WW) (from table)
J4 = (S11 OR S15) AND WW (implemented)
J8 = S0 AND $\overline{WR}$ AND RR (from table; implemented)
J12 = (S7 AND TR) OR (S15 AND MGF AND $\overline{NINE}$) (from table)
J12 = (S7 AND TR) OR [S7 AND MGF AND $\overline{NINE}$] OR (S15 AND MGF AND $\overline{NINE}$) OR [S15 AND TR] add [zeroes]
J12 = (S7 OR S15) AND (MGF AND $\overline{NINE}$ OR TR) NOTE: (MGF AND $\overline{NINE}$=$\overline{NINE}$)
J12 = (S7 OR S15) AND ($\overline{NINE}$ OR TR) (implemented)

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Figure 3-21. Implementation of memory controller state transition commands.

CHARACTER REGISTER

This circuitry displaces the crt beam in a manner necessary to write characters. The octal D-type flip flop, U600, in conjunction with R508, and R408, R504 and R411 for the Y channel and R506, R507, and R505 for the X channel, provides binary weighted currents to displace the crt beam to write the characters. Input to the flip flop is binary data from the microprocessor for the displayed character.

DISPLAY TIMER

This circuitry times the duration of the dot or vector. See schematic 11 for waveforms associated with this circuitry.

Z-AXIS

This circuitry controls the crt beam on and off times.

12 DISPLAY OUTPUT

Y OUTPUT

This circuitry provides the actual output voltage to the mainframe to produce a trace, characters or dot pattern. The circuitry consists of a differential amplifier, U550, a sample and hold circuit, U445, and an integrator, U330, all with associated components. See Figure 3-22.

In the dot mode this circuit operates as a voltage follower. In the join dots mode this circuit samples and integrates the difference of the output and input voltages.

The Y signal feeds to the − input of U550 an operational amplifier. The plus input connects to the output of the integrator or amplifier. This circuit essentially subtracts the output of the D-to-A Converter from the output of U330.

During the vector mode sample interval the output signal from operational amplifier U550 passes through U435A. This integrated circuit functions as a switch. When the $\overline{\text{Vector}}$ signal is high this switch is closed. See Figure 3-23 and Figure 3-24. (Other waveforms for this circuitry are shown on schematic 12.) This action applies the output of the differential amplifier to the sample and hold capacitor. This capacitor charges to the voltage difference between the integrator output (pin 6 of U330) and the output of the current to voltage converter, U530. The input to the integrator is disconnected from U445 by U440A and grounded by U440B which holds the voltage at the integrator output (integral of 0 is no change).

When the $\overline{\text{Vector}}$ signal goes low, the output circuitry goes to the integration interval. Operational amplifier U550 disconnects from the sample and hold capacitor(s) and the integrator (U330) is connected to the output of the sample and hold amplifier. The output of U330 changes at a rate proportional to the voltage on the sample and hold capacitor.

In the dot mode, U330 functions as a buffer amplifier; the sample and hold circuitry is disconnected. The output of the buffer amplifier rapidly changes so that no voltage difference exists at the input of U550.

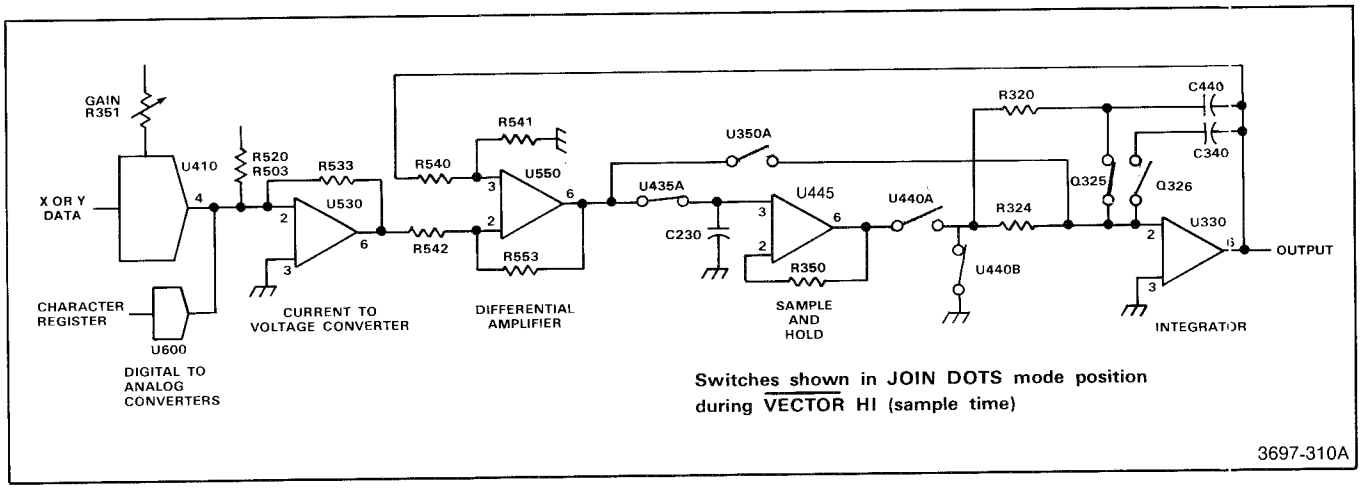


Figure 3-22. Simplified output block diagram shown on Schematics 11 and 12. Only the Y channel is shown; the X channel is identical.

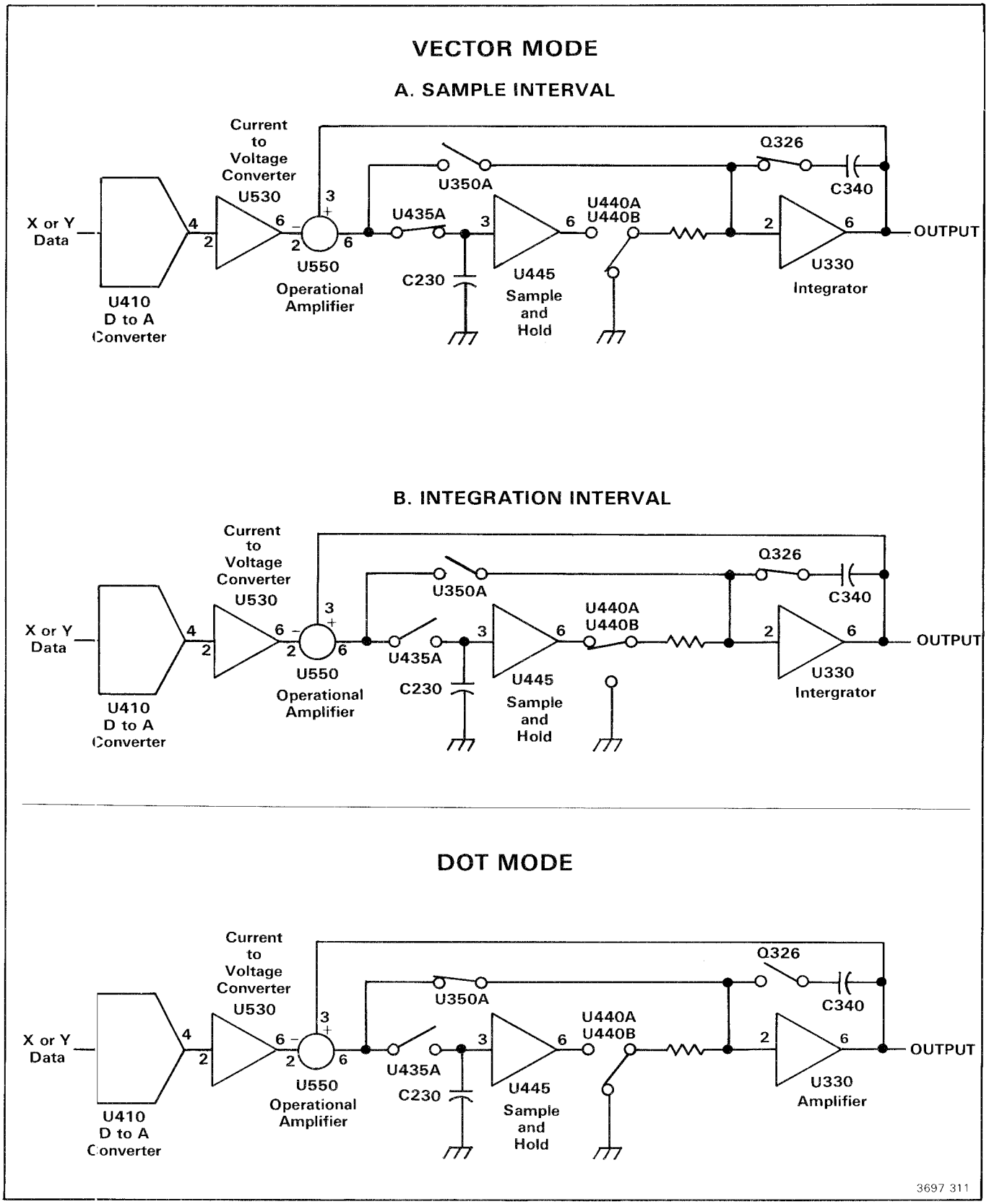


Figure 3-23. Simplified output circuitry in the vector and dot modes.

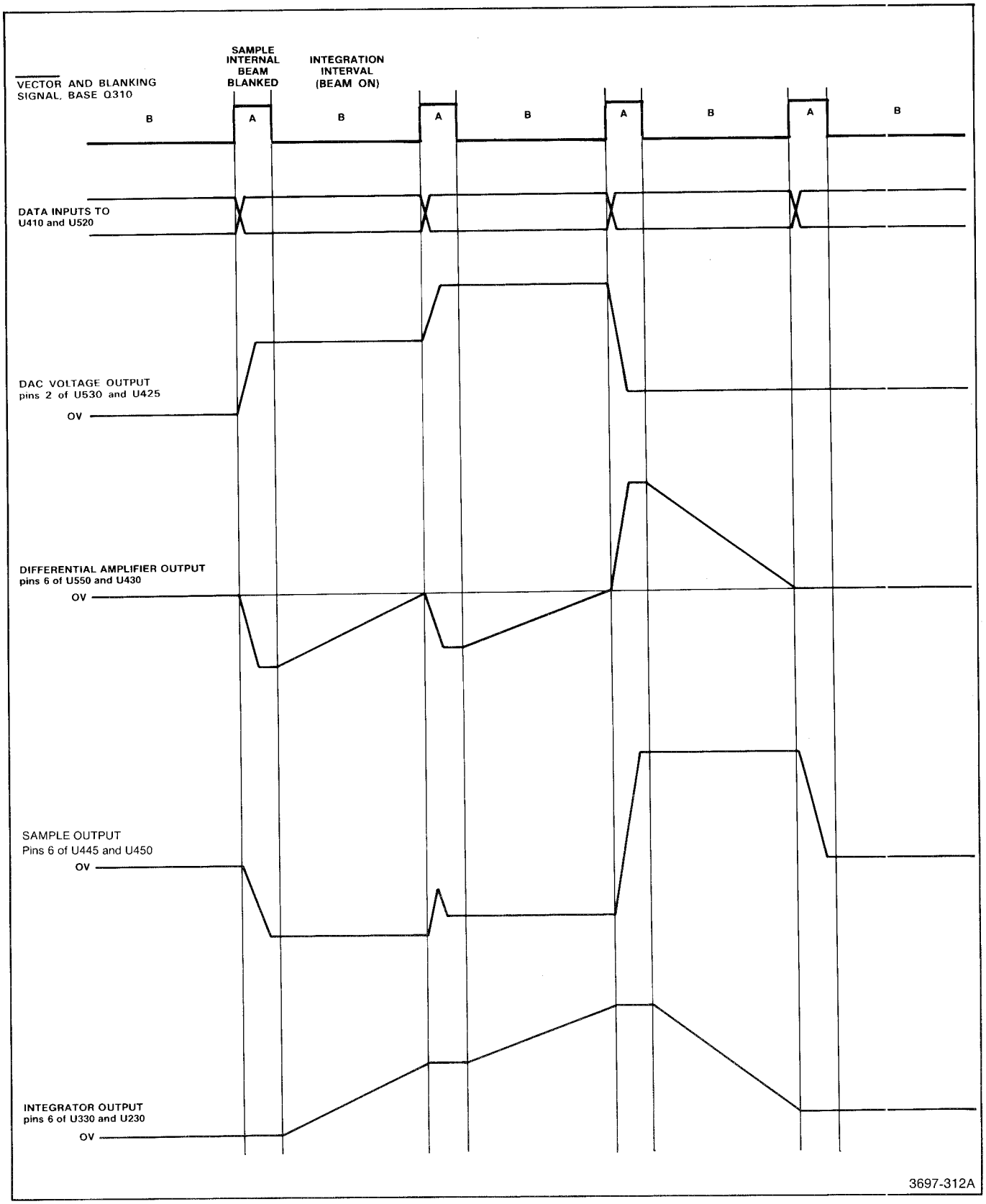


Figure 3-24. Waveforms for the output circuitry shown on Schematics 11 and 12.

In the plot output mode, C349 is switched in parallel with C230; the switching is accomplished by U435B. The 0.1 microfared capacitor is necessary, as the vector times in the plot mode are 20,000 times longer than in the normal mode. In the plot mode, additional integrating capacitance is required. FET Q325 conducts when the Plot Out signal is high, switching C440 in parallel with C340.

When the circuitry operates in the vector mode, resistor R552, in conjunction with capacitor C451, compensates for input offset in U445 and for the charge dumped into C230 when U435A switches. Integrator input offset is adjusted by R452, through R327, to pin 3 of U330.

The integrator output is applied to the plotter output terminals through U350B for the Y channel and U350C for the X channel. Divider network R325, R242 and R250 provides attenuation of the output waveform. The display waveform to the mainframe is applied from the junction of R250 and R242 to A13 on the rear interface connector. Vertical centering is accomplished by R150 on the A3 Output board, and horizontal centering by R150 on the A6 Trigger Board.

X OUTPUT

This circuit operation is identical with the Y Output circuitry. Only the circuit numbers are different.

CONTROLLER

This circuitry controls the switches in the X and Y Output circuitry.

When the Plot Out signal at pin 3 of U610A is high, the output of U610A is high. (The outputs from U610A and U610D are about +7 V high and −7 V low.) This action closes U350B and U350C, thereby connecting the output of the X and Y channel integrators-amplifiers to the plotter output connections on the front panel. (This action also closes U435B and U435C.) The output signal from U610A is divided by R200 in series with CR200 and R100. The junction of CR200 and CR100 (CR320 and CR430 also) is always 0.6 V below ground. Therefore, the gates of Q325 and Q226 (Q326 and Q225 also) vary from 0 V to −7 V.

When the Display Join/Dots signal is high, the output of U610D is high (+7 V). This action turns on Q326 in the Y channel and Q225 in the X channel. The purpose of these switches is discussed under the Y Output heading.

When either the Plot Out or the Disp Join/Dots signals or both are high, pin 5 of U610B is low. This causes a low at pin 7 of U610B. This action opens switches U350A and U350D placing the sample and hold circuitry in operation. This action also places lows on pin 9 of U620C and pin 12 of U620D. This enables the $\overline{\text{Vector}}$ signal to control switches U435A, D and U440A, D.

During the integration interval, $\overline{\text{Vector}}$ is low. (The $\overline{\text{Vector}}$ signal is generated by OR gate, U725A, from the output of the display timer or the μP Vector signal as shown on schematic 2.) This causes a high on pins 5 and 6 of U620B and a high on pin 13 of U620D. This action opens switches U435A and U435D by a low on pin 11 of U620D. It also causes pin 8 of U620C to be low. This sets pin 10 of U620C high closing U440A and U440D and opening U440B and U440C via U620A.

A wired AND is formed by U710C and U710E. The Plot Out and the Disp. Join / Dots signals must both be low for a high to exist at pin 5 of U610B. This high also exists on pin 9 of U620C and pin 12 of U620D. This action disables OR gates U620C and U620D, disabling the $\overline{\text{Vector}}$ signal at these points.

PENLIFT RELAY

When the Pen Lift signal goes high current flows through relay coil K230, closing the relay.

13 POWER SUPPLIES AND POWER DISTRIBUTION

The Power Supplies and Power Distribution diagram shows the mainframe source of all 5D10 operating power. This diagram also shows the 5D10 internal switching-power-supply circuit. This power-supply circuit, powered by the mainframe, provides an additional +7.5, −7.5 volt source, and a high-current +5 volt source not directly available from the mainframe.

OSCILLATOR

The Oscillator circuit is composed of transistors Q740 and Q741. This circuit generates a 100 kHz sawtooth output signal to drive the base of comparator transistor Q841.

COMPARATOR

The Comparator circuit is composed of emitter-coupled amplifier Q841 and Q840. The 100 kHz sawtooth output signal from the oscillator drives the base of Q841, while

the base of Q840 receives dc feedback signals from the voltage regulator and current limit operational amplifiers. The resultant output signal at the collector of Q840 provides a varying duty cycle, 100 kHz square wave to the emitter of Q842 in the gate driver circuit.

GATE DRIVER

The varying duty cycle, 100 kHz square wave is emitter coupled to Q842 of the Gate Driver circuit. The signal at the collector of Q842 is level shifted to −38 volts and amplified to a 10 volt amplitude by Q843, Q844, and Q845 to drive the gate of switching transistor, Q800.

SWITCHING TRANSISTOR AND TRANSFORMER

The output signal from the Gate Driver circuit is emitter-coupled to the gate of switching transistor Q800. The source of Q800 connects directly to −38 volts and the drain connects, through the primary of transformer T810, to +38 volts. This provides a nominal 76 volt difference, which is algebraically added to a 62 volt flyback ring generated by damping capacitor C910. The resultant 138 volt peak-to-peak, varying duty cycle, constant-frequency signal generated at the drain of Q800 drives the primary of transformer T810.

RECTIFIERS, FILTERS AND CURRENT SENSES

The secondary outputs of Transformer T810 are rectified and filtered to provide three voltages; +7.5 volts, −7.5 volts, and +5 volts. These voltages supply power throughout the 5D10 circuitry. Sense lines from each common of the three supplies connect to current limit operational amplifiers to provide overcurrent protection. Further, the +5 volt supply is voltage regulated by feedback to the Comparator circuit from operational amplifier U740C.

CURRENT LIMIT

Current output from the switching-power-supply +7.5, −7.5, and +5 volt supplies is limited by operational amplifiers U740D, A, and B, respectively.

A sense line from each secondary winding is connected to a current-sense voltage divider at the negative input of each current limit operational amplifier. The switching supply normally regulates to the mainframe +5 volt reference. However, when the current of any output supply exceeds its limit, the operational amplifier for that supply will pull the base of Q840 high, thereby reducing drive to the Gate Driver circuit.

VOLTAGE REGULATOR

Operational amplifier U740C regulates the +5 volt supply. A +5 volt reference voltage from the mainframe supply is input through R750 to pin 9 of U740C, and +5 volts from the switching-power-supply is input through R651 to pin 10 of U740C. These two voltage inputs are compared against each other to provide a dc voltage output at pin 8 of U740C, which in turn controls the base of comparator transistor Q840.

PROTECTION

The Protection circuit has three inputs to protect the switching-power-supply from over-voltage or fault conditions. The first input protects the drain of Q800 from excessive high voltage. If this condition occurs, zener diodes VR801 and VR802 will conduct, thereby firing silicon controlled rectifier Q831. Transistor Q835 will saturate and apply zero bias to the gate of Q800 and shut down the supply.

The second input protects Schottky barrier diode CR601 from excessive reverse voltage. If this condition occurs, VR730 and Q731 will conduct and fire Q831 to shut down the supply.

The third input will protect the switching-power-supply +5 volt output if a fault condition occurs. If the +5 volt supply were to go more positive than approximately 6 volts, zener diode VR731 will conduct, biasing Q731 on, and thereby fire Q831 to shut down the supply.

SIGNAL NAMES GLOSSARY

The following information includes signal names as shown on the schematics, and a brief description of the signal function. Some signal names are followed by (SA) at some points, but not others. Without (SA), the signal is performing its primary function; with (SA) the signal is inactive during normal operation of the circuit, and is applied only for self-test and signature analysis operation.

Signal Name	Description
	Originated on Schematic 1
Clock	Output (10 MHz) from Control Clock Oscillator.
$\overline{\text{Clock}}$	Inverted output from Control Clock Oscillator.
DT 0-7	Data to (and from) the microprocessor and the input and output ports.
$\overline{\text{EN 12}}$	Enables the CH 1 and CH 2 VOLTS/DIV switch input multiplexer.
$\overline{\text{EN 34}}$	Enables the F and M bus input multiplexer. The positive going edge tells the Read and Write Control that the microprocessor has finished reading the memory address or data.
$\overline{\text{EN 56}}$	Enables a front-panel control input multiplexer.
$\overline{\text{EN 78}}$	Enables a front-panel control input multiplexer.
$\overline{\text{EN 9}}$	Enables a front-panel control input multiplexer.
N1 CK	Clocks the N bus register.
N2 CK	Clocks register, U450, in the Self Test Annunicator, and initiates the display sequence in the Read and Write Control machine and display timer.
M1 CK	Clocks a register in the Controller Outputs circuit.
M2 CK	Clocks a register in the Controller Outputs circuit.
M3 CK	Clocks a register in the Controller Outputs circuit.
M4 CK	Clocks a register in the Controller Outputs circuit.
CHAR CK	Clocks the character register; used in drawing a character on the crt screen.
$\overline{\text{SWR SET}}$	Used in self test and signature analysis modes only.
μP A0	One bit on the address bus; controls input multiplexer to select appropriate inputs.
$\overline{\text{RESET}}$	Inverted reset from the microprocessor.
	Originated on Schematic 2.
$\overline{\text{SEC } 10^4}$, $\overline{\text{SEC } 10^2}$, $\overline{\text{SEC } 10^1}$, $\overline{\text{SEC .4}}$, $\overline{\text{SEC .2}}$	SECONDS/DIV switch settings encoded in bcd and powers of 10 multiplier.

Signal Name	Description
	Originated on Schematic 3
INTL MEM	Enables the reading of data from the Waveform Memory onto F bus.
$\overline{\text{INTL MEM}}$	Inversion of the above signal.
SAVE ALL	Causes acquisition to stop (and remain stopped) at the end of the next write group.
μP ERASE	Asserts erase function; same as operator pushing erase button.
DIG DUAL/SGL	High for dual trace, low for single trace acquisition. Causes digitizing of one channel only, or both.
DIG 1/2	High digitizes channel 1, low digitizes channel 2, when DIG DUAL/SINGLE is low. Digitizes channel 1, then channel 2, when DIG DUAL/SINGLE is high.
XY SHIFT	Displaces display on screen horizontally 0.12 div in X-Y display mode.
2O and 2L and LD	Channel 2 is on (being acquired) and CH 2 VOLTS/DIV switch is at LEFT PLUG-IN position and left plug-in is operating in the dual trace mode. Controls channel switch logic.
ADD	Ch 1 and Ch 2 algebraically added during acquisition.
DISP REF/NEW	High displays reference waveform. Low displays new waveform.
DISP XY/YT	High causes XY display. Low causes YT display.
$\overline{\text{DISP SWP MGF}}$	Low for sweep magnification.
μP SAMPLE	Microprocessor stimulates digitizer cycle; same function as sample pulses from timebase.
DISP. JOIN/DOTS	High to join dots on crt display. Low for dots only.
PLOT OUT	μP sets display output integrator for slow time constant in plot operation.
PEN LIFT	μP controls penlift relay.
μP VECTOR	μP performs vector timing in plot operation (replaces Display Timer).
$\overline{\text{F=N}}$	Select N bus as driver for F bus; allows μP to write data to Waveform Memory or X or Y Display Registers via the DT to N to F buses.
$\overline{\text{F EN SET}}$ / $\overline{\text{F EN CLEAR}}$	Allow μP to enable or disable Memory Data Selector to drive F bus with data from E or N buses.
$\overline{\text{WE SET}}$ / $\overline{\text{WE CLR}}$	Allow μP to write data into Waveform Memory.
DISP CYCLE TRIG	Pulse occurs once every complete cycle of display activity. Useful for triggering test scope when troubleshooting the output circuits.
N0 - N9	10 bit number output from μP. Used in controlling display functions and reading memory data.
$\overline{\text{OPN:R}}$	μP causes memory controller to load R register (U640, U650).
$\overline{\text{R+T}}$	μP causes memory controller to load R or T register (U740, U750).
Modify	Asserted during display of Ch 1 waveform if in DUAL Channel LEFT PLUG-IN and SAVE REF Mode. Causes unequal spacing of waveform points.
OPN:T	μP causes memory controller to load T register (U740, U750).
CLR	Color signal line.

Signal Name	Description
SP. L/T	μP selects Scratch Pad output, trigger point address or latest address written.
OPN: FETCH	Asserted when μP reads Waveform Memory contents.
ACQ. SAVE REF	Causes 1/2 of memory locations to cease updating (saves reference waveform).
WG. 2 WG. 4 WG. 8	Write Groups of 2, 4, or 8 data points. Data must be acquired in groups for proper display and cursor management. Loadstop occurs only at the end of a write group
$\overline{\text{PRE. TRIG}}$ $\overline{\text{CTR. TRIG}}$ $\overline{\text{POST TRIG}}$	μP mimics front-panel pushbutton settings of trigger position.
$\overline{\text{TEST T->R}}$	Places T register (U740, U750) contents into R register (U640, U650) during read cycle.
$\overline{\text{DISP. CHAR}}$ DISP. CHAR	Asserted during display of readout characters and cursors.

Originated on Schematic 4

CH 1 SIGNAL	Channel 1 output signal (from Sample and Hold circuitry) to Channel Switch.
CH 1 TRIG	Channel 1 triggering signal to Source Select Coupling and Input Buffer.
CH 2 SIGNAL	Channel 2 output signal from Sample and Hold circuitry to Channel Switch.
CH 2 TRIG	Channel 2 triggering signal to Source Select Coupling and Input Buffer.
CH 1 PROBE CODING	Channel 1 probe coding information to Front-Panel Switches and Machine Status.
CH 2 PROBE CODING	Channel 2 probe coding information to Front-Panel Switches and Machine Status.

Originated on Schematic 5

Dig 4	High during second half of digitizer cycle. See Figure 3-9.
$\overline{\text{TS 7}}$	Seventh time slot from one of eight decoder in the timing circuitry. See Figure 3-9.
TS 7	Inversion of the above signal. See Figure 3-9.
E0 - E7	Latched digitizer output data.

Originated on Schematic 6

SAMPLE	Rising edge causes sample-hold and digitize cycle.
$\overline{\text{HOLD}}$	High during data conversion.
CH 1/2	Channel Switch control; high when channel one is digitized, low when channel two is digitized.
CH 2/1	Channel Switch control; high when channel two is digitized, low when channel one is digitized.
$\overline{\text{LAST}}$ $\overline{\text{END}}$	See Figure 3-9.

Signal Names	Description
PLUG-IN CHANNEL SWITCH	Controls left plug-in channel switch.
LEFT DISPLAY DISABLE	Disables left plug-in display.
HORIZONTAL PLUG-IN CHANNEL SWITCH	Disables left plug-in display.
ALTERNATE DRIVE	Controls left plug-in channel switch.

Originated on Schematic 7

ERASE	Stops display of previously acquired waveform and begin acqusition of new waveform.
$\overline{\text{ERASE}}$	Inversion of the above signal.
LOADSTOP	Stops digitizing and writing to Waveform Memory. Indicates waveform acquisition is complete.
$\overline{\text{LOADSTOP}}$	Inversion of the previous signal.
GROUP S7	High during State 7 of the memory controller at the end of the write group.
$\overline{\text{XY RO}}$	Low if read address is even number during XY display.
RO	LSB of read address.
T10	MSB of Time Register. Signifies end of trace.
$\Sigma 7$, $\Sigma 8$, $\Sigma 9$	Results of comparison between present write address and write address at triggering time. Used to control Loadstop Logic.
F0 - F7	Waveform Memory data bus.
M0 - M11	Waveform Memory address bus.
T0 - T9	Time register. Generates horizontal display.

Originated on Schematic 8

R11	MSB of read address. Used to detect memory full.
$\overline{\text{WE}}$	Enables Waveform Memory for writing.
F. EN	Enables data input to Waveform Memory during write cycle.

Originated on Schematic 9

WE GROUP	High during waveform memory write enable at end of write group.
W0 - W10	Write addresses.
W7, $\overline{\text{W8}}$, $\overline{\text{W9}}$	Bits of write address counter. Used to control trigger enable logic.

Signal Name	Description
	Originated on Schematic 10
EOT	End of trace.
$\overline{\text{EOT}}$	Inverse of the above signal line.
A SEL T/R	Selects T (U740, U750) or R (U640, U650) register.
R CK and M SEL W/R	High sets M=W, low sets M=R; rising edge clocks R register.

Signal Name	Description
2^1, 2^2, 2^3	Binary weighted state machine counter outputs.
S10, $\overline{\text{S10}}$, $\overline{\text{S10 + S11}}$, $\overline{\text{S9}}$, S15, S0, $\overline{\text{S3 + J4}}$, $\overline{\text{S7 + S15}}$	S=State. Decoded Read and Write Control outputs. Number signifies counter state. See Transistion commands, Figure 3-21.

	Originated on Schematic 11
EOC	High for last stroke of a character. Control state machine.
Y	Y axis analog voltage output from D-to-A converters.
X	X axis analog voltage output from D-to-A converters.
DAC COMP	X and Y compared: X>Y or Y>X. Used in the self test mode.
READ NEXT	Asserted by the display timer to cause memory controller to begin another read cycle and update X-Y registers to next values.
XY and RO	True in XY display with even read address.
$\overline{\text{VECTOR}}$	Causes integration between successive points in JOIN DOTS display.
B SWEEP Z-AXIS TO MAINFRAME	Controls mainframe crt intensity.

	Originated on Schematic 12
PENLIFT	Controls penlift relay.
Y	Y front-panel output connection.
X	X front-panel output connection.
DISPLAY SIGNAL	X or Y channel output signal combined with centering control voltage.

MAINTENANCE

This section contains information for performing preventive maintenance, troubleshooting, and corrective maintenance for the 5D10 Waveform Digitizer.

PREVENTIVE MAINTENANCE

Preventive maintenance, when performed on a regular basis, can prevent or forestall instrument breakdown and may improve instrument reliability. The severity of the environment to which the instrument is subjected will determine the frequency of maintenance. A convenient time to perform preventive maintenance is preceding electrical adjustment of the instrument.

PLUG-IN PANEL REMOVAL

CAUTION

Disconnect the power before cleaning the instrument or replacing parts.

The side panels and top-and-bottom frame rails as well as the front panel reduce radiation of electromagnetic interference from the instrument. The side panels are held in place by grooves in the frame rails. To remove the panels pry out with fingers, beginning at the rear of the appropriate side cover. To install the covers, position them over the frame rail grooves then press down with fingers until the cover snaps into place (the front edge of the side covers must be seated in the groove in the 5D10 front-panel). Pressure must be exerted all along the rails to secure the panels. See the exploded view drawing in Section 9, Replaceable Mechanical Parts, for additional information.

NOTE

The 5D10 will not slide into the mainframe if the side panels have been improperly installed (not firmly seated in the rails).

CLEANING

The 5D10 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path which can result in instrument failure.

NOTE

The cabinet panels of the mainframe in which the 5D10 is installed reduce the amount of dust reaching the the interior of the instrument. Operation without the panels in place necessitates more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use only Isopropyl alcohol or totally denatured ethyl alcohol. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

EXTERIOR

Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. The brush is particularly useful for dislodging dirt in and around the side-panel ventilation holes and front-panel switches.

NOTE

Remove the side panels before cleaning them.

INTERIOR

Cleaning the interior of the instrument should only be occasionally necessary. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2). Remove any dirt which remains with a soft brush or a cloth dampened with alcohol A cotton-tipped applicator is useful for cleaning in narrow spaces, or for cleaning more delicate circuit components.

CAUTION

Circuit boards and components must be dry before applying power to prevent damage from electrical shorts.

LUBRICATION

Generally, there are no parts in this instrument that require a regular lubrication program during the life of the instrument.

CAM SWITCH LUBRICATION

In most cases, factory lubrication should be adequate for the life of the instrument. However, if the switch has been disassembled for replacement of switch sub-parts, a lubrication kit containing the necessary lubricating materials and instructions is available through any Tektronix Field Office. Order Tektronix Part 003-0342-02. General Electric Versilube™ silicone grease should be applied sparingly so that the lubricant does not get on the contacts. Refer to Figure 4-1 for lubrication instructions.

VISUAL INSPECTION

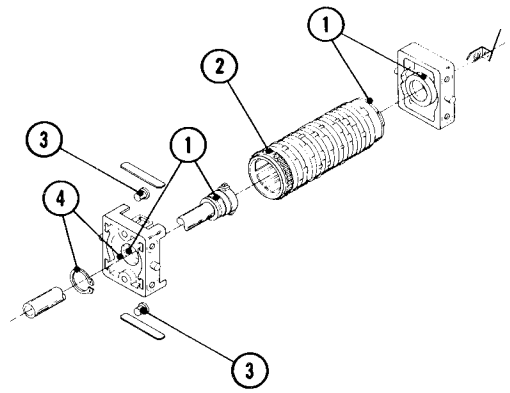
The 5D10 should be inspected occasionally for loosely seated semiconductors or heat-damaged parts. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged parts are found. Overheating usually indicates other trouble in the instrument; therefore, correcting the cause of overheating is important to prevent recurrence of the damage.

SEMICONDUCTOR CHECKS

Periodic checks of semiconductors are not recommended. The best check of semiconductor performance is actual operation in the instrument. More details on semiconductors are given under Troubleshooting later in this section.

ELECTRICAL ADJUSTMENT

To ensure accurate measurments, check the electrical adjustment of this instrument after each 2000 hours of operation, or every twelve months if used infrequently. In addition, replacement of components may necessitate adjustment of the affected circuits. Complete adjustment instructions are given in Section 5, Calibration. This procedure can be helpful in localizing certain troubles in the instrument, and in some cases, may correct them.



(1) Apply lubricant to the drum journals and mating surface in the mounting bearings.

(2) Apply lubricant to the wear surface of the index wheel.

(3) Apply lubricant to the index roller and roller guide in the front bearing. A thin film should be applied to the inner face of the detent springs if more than one spring is replaced.

(4) Ensure that some lubricant is present at the interface between the bearing and retainer clip.

3697-61

Figure 4-1. Camswitch lubrication and assembly.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of other closely related circuits. The Performance Check procedure in Section 5, Calibration, provides a quick and convenient means of checking instrument operation. In some cases, minor troubles may be revealed or corrected by adjustment.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting of the 5D10 Waveform Digitizer. Information contained in other sections of this manual should be used in conjunction with the following data to aid in locating a defective component. An understanding of the circuit operation is helpful in locating troubles. See Section 3, Theory of Operation, for this information.

TROUBLESHOOTING AIDS

DIAGRAMS

Complete schematic diagrams are given on the foldout pages in Section 8, Diagrams and Circuit Board Illustrations. The component circuit number and electrical value of each component in this instrument are shown on these diagrams. (See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the reference designators and symbols used to identify components in this instrument.) Important voltages and numbered waveform test points are also shown on some diagrams. Important waveforms, and the numbered test points where they were obtained, are located adjacent to each diagram. The portions of circuits mounted on circuit boards are enclosed with heavy, solid-black lines. Each schematic diagram is divided into functional stage blocks, as indicated by the wide shaded lines. These functional blocks are described in detail in Section 3, Theory of Operation.

CIRCUIT BOARD ILLUSTRATIONS

To aid in locating circuit boards, an illustration showing the circuit board location appears on the back of the foldout page facing the schematic diagram. An illustration of the circuit board(s) is also included here to identify the physical location of components and waveform test points that appear on the respective schematic diagram. Each circuit board illustration and diagram is arranged in a grid locator with an index to facilitate rapid location of components.

SIGNATURE ANALYSIS TROUBLESHOOTING

The 5D10 Waveform Digitizer was designed to accommodate signature analysis for troubleshooting the digital circuitry. Signature Analysis is a data compression technique that reduces a complex data stream (a sequence of logic levels occurring during a specific time window) to a series of unique four-digit hexadecimal signatures. The test procedure relies on stimulating (using a program stored in ROM) circuit nodes in a repeatable and predictable fashion. For example, a microprocessor system can be easily made to repeatedly increment through its address field, exercising much of the instruments circuitry.

The "5D10 Diagnostic Troubleshooting" Service Manual, Volume 2, contains the signature analysis troubleshooting procedures for the 5D10.

Self-Test Routine Modes

Each time the 5D10 receives a power-up reset (i.e., when mainframe power is turned on), a self-test routine is executed. The 5D10 has three basic self-test routine modes, individually selectable via internal Link-Plugs (jumpers). These three modes function as follows:

1. Normal Mode

This self test is to be exercised as a function of normal operation and provides the operator with a condition report display on the screen (i.e., 5D10 READY, or ERROR).

The 5D10 is shipped from the factory with the Link-Plugs connected for Normal Mode self-test operation. Refer to Table 4-1. In the Normal mode at power-up, the 5D10 will execute all self-test routines.

If either the SAVE or the SAVE REF button has been pressed before power-up, the 5D10 will display a graticule and box pattern on the screen. If errors are encountered during the diagnostic tests, the screen will also display "ERROR", and possibly a number. Number 26 indicates the data memory test has failed, and numbers 21 or 22 indicate the output DAC tests have failed. No number displayed indicates failure of other circuits.

To troubleshoot an "ERROR", proceed to the Report Mode for diagnostic troubleshooting (refer to Volume 2 Service Manual).

To proceed with normal operation, release the SAVE or SAVE REF buttons.

2. Report Mode

This self test provides the troubleshooter with the details of all errors encountered via the internal LED array (Self-Test Annunciator). To use this mode, the 5D10 halves must be separated, some circuit boards put on extender cables, and the Link-Plugs configured as shown in Table 4-1. Complete troubleshooting procedures, using the Report Mode, are contained in the 5D10 Diagnostic Troubleshooting Service Manual, Volume 2.

3. Cycle Mode

This self test is for use by factory test personnel only, and has no practical value to the troubleshooter in the field.

In Cycle Mode (Link-Plug on A5 J100 removed) the 5D10 will execute the self-test routine, and display a graticule, box pattern, and "5D10 READY" or "ERROR" report on the screen. After about five seconds, the processor will execute a power-up reset, and repeat the self-test routine. This loop will continue until the Link-Plug for A5 J100 is replaced.

COMPONENT COLOR CODING

This instrument contains composition resistors, metal-film resistors, and wire-wound resistors. The resistance values of wire-wound resistors are usually printed on the component body. The resistance values of composition resistors and metal-film resistors are color coded on the components using the EIA color code (some metal-film resistors may have the value printed on the body). The

TABLE 4-1
Self-Test-Routine Mode Selection

CIRCUIT BOARD CONNECTOR			NORMAL MODE	REPORT MODE	CYCLE MODE
A2 J410					
	PINS	1-2	OPEN	OPEN	OPEN
		3-4	OPEN	OPEN	OPEN
		5-6	OPEN	OPEN	OPEN
		7-8	OPEN	OPEN	OPEN
		9-10	OPEN	OPEN	OPEN
		11-12	OPEN	OPEN	OPEN
		13-14	OPEN	OPEN	OPEN
		15-16	LINK-PLUG	LINK-PLUG	LINK-PLUG
		17-18	LINK-PLUG	LINK-PLUG	LINK-PLUG
		19-20	LINK-PLUG	LINK-PLUG	LINK-PLUG
A2 J440					
	PINS	1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG
		3-4	LINK-PLUG	LINK-PLUG	LINK-PLUG
		5-6	LINK-PLUG	LINK-PLUG	LINK-PLUG
		7-8	LINK-PLUG	LINK-PLUG	LINK-PLUG
		9-10	LINK-PLUG	LINK-PLUG	LINK-PLUG
		11-12	LINK-PLUG	LINK-PLUG	LINK-PLUG
		13-14	LINK-PLUG	LINK-PLUG	LINK-PLUG
		15-16	LINK-PLUG	LINK-PLUG	LINK-PLUG
		17-18	LINK-PLUG	LINK-PLUG	LINK-PLUG
		19-20	LINK-PLUG	LINK-PLUG	LINK-PLUG
A4 J100					
	PINS	1-2	OPEN	LINK-PLUG	OPEN
A4 J106					
	FIRST TRIG/FULL DSPY		FULL DSPY	FULL DSPY	FULL DSPY
A5 J100	PINS	1-2	LINK-PLUG	LINK-PLUG	OPEN
J101		1-2	LINK-PLUG	OPEN	LINK-PLUG
J102		1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG
J103		1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG
J104		1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG
J105		1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG
J106		1-2	OPEN	OPEN	OPEN
A6 J620					
	PINS	1-2	LINK-PLUG	LINK-PLUG	LINK-PLUG

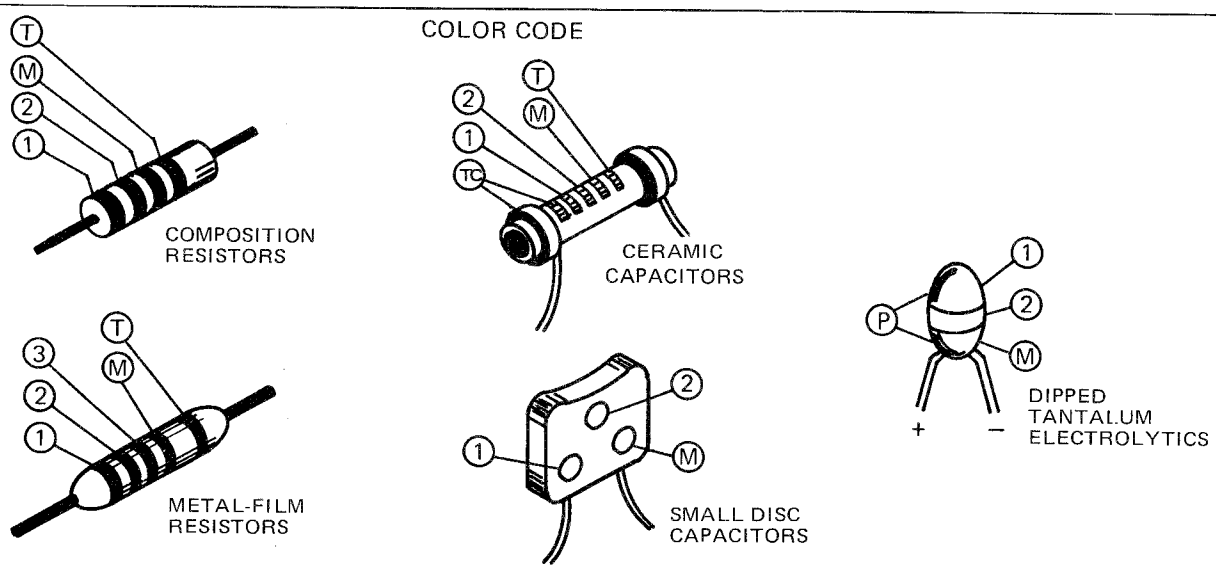
color code is read starting with the stripe nearest the end of the resistor. Composition resistors have four stripes, which consist of two significant figures, a multiplier, and a tolerance value (see Fig. 4-2).

Metal-film resistors have five stripes consisting of three significant figures, a multiplier, and a tolerance value.

The values of common disc capacitors and small electrolytics are marked on the side of the component body. The white ceramic and epoxy-coated tantalum capacitors used in the instrument are color coded using a modified EIA code (see Fig. 4-2).

The cathode end of glass-encased diodes is indicated by a stripe, a series of stripes, or a dot. The cathode and

COLOR CODE



(1) (2) and (3) - 1ST, 2ND, AND 3RD SIGNIFICANT FIGS.
(M) - MULTIPLIER (T) - TOLERANCE;
(TC) - TEMPERATURE COEFFICIENT.

(T) AND/OR (TC) COLOR CODE MAY NOT BE PRESENT ON SOME CAPACITORS;
(P) - POLARITY AND VOLTAGE RATING

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER (OHMS)	TOLERANCE	MULTIPLIER (pF)	TOLERANCE		
					OVER 10pF	UNDER 10pF	
BLACK	0	1	---	1	±20%	±2pF	4VDC
BROWN	1	10	±1%	10	±1%	±0.1pF	6VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	---	10VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	---	15VDC
YELLOW	4	10^4 or 10K	±4%	10^4 or 10,000	+100% –0%	---	20VDC
GREEN	5	10^5 or 100 K	±1/2%	10^5 or 100,000	±5%	±0.5pF	25VDC
BLUE	6	10^6 or 1 M	±1/4%	10^6 or 1,000,000	---	---	35VDC
VIOLET	7	---	±1/10%	10^7 or 10,000,000	---	---	50VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% –20%	±0.25pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1pF	3VDC
GOLD	---	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	---	10^{-2} or 0.01	±10%	---	---	---	---
NONE	---	---	±20%	---	±10%	±1pF	---

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Figure 4-2. Color code for resistors and capacitors.

anode ends of metal-encased diodes can be identified by the diode symbol marked on the body.

SEMICONDUCTOR LEAD CONFIGURATIONS

Lead configurations and index locators for semiconductor devices used in the 5D10 Waveform Digitizer are shown in Figure 4-3.

STATIC-SENSITIVE DEVICE CLASSIFICATION

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 4-2 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers on a metal rail, or conductive foam. Label any package that contains static-sensitive assemblies or components.
3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static free work station by qualified service personnel. We recommend use of the Static Control Mat, Tektronix Part 006-3414-00, and Wrist Strap, Tektronix Part 006-3415-00.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only special anti-static suction type desoldering tools.

TABLE 4-2
Relative Susceptibility to Damage from Static Discharge

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits or discretes or linear microcircuits with MOS inputs (most sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (least sensitive)	9

[1] Voltage equivalent for levels.

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (exs.)
8 = 900 V
9 = 1200V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 ohms).

MULTI-PIN CONNECTOR IDENTIFICATION

Pin 1 on multi-pin (harmonica, ribbon cable) connectors is designated with a triangle. A triangle, dot or square printed on circuit boards denotes pin 1. When a connection is made to a circuit board, the orientation of the triangle on the multi-pin holder is determined by the index (triangle, dot or square) printed on the circuit board (see Fig. 4-4).

TROUBLESHOOTING EQUIPMENT

The following equipment is useful for troubleshooting the 5D10 Waveform Digitizer:

1. Transistor Tester

   Description: Dynamic-type tester.

   Purpose: Test semiconductors.

   Recommended type: TEKTRONIX 577/177 Curve Tracer, TEKTRONIX 576 Curve Tracer, 7CT1N Curve Tracer plug-in unit and a 7000-series oscilloscope system, or a 5CT1N Curve Tracer plug-in unit and a 5000-series oscilloscope system.

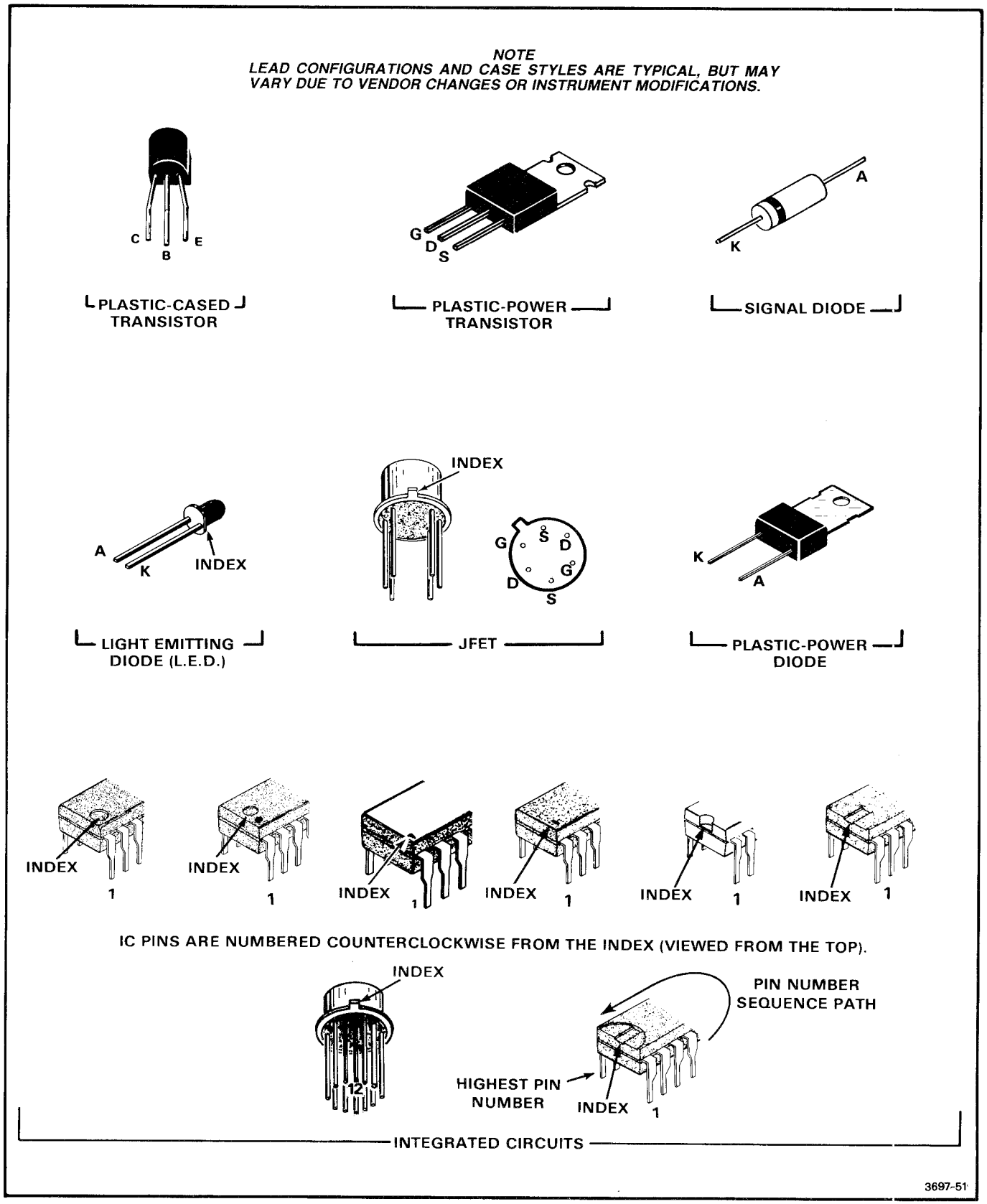


Figure 4-3. Semiconductor lead configuration.

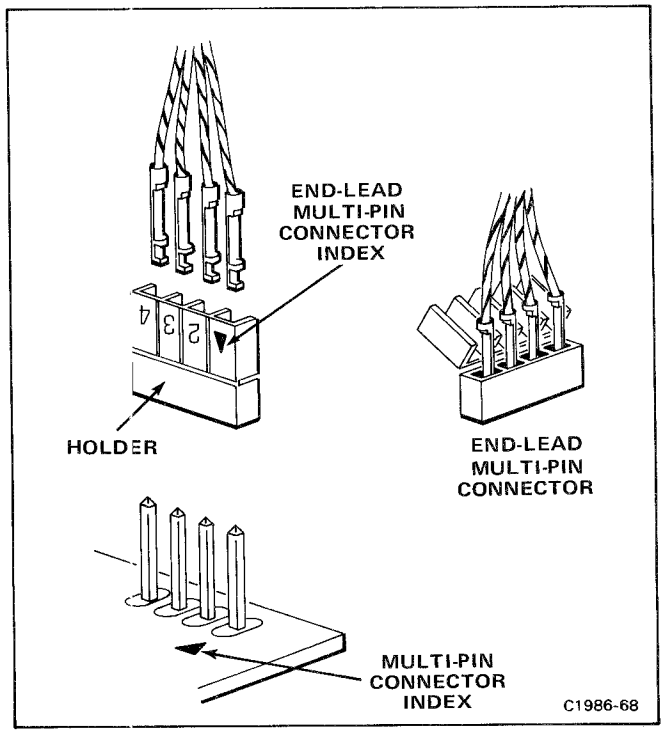


Figure 4-4. Orientation of multi-pin connectors.

2. Digital Multimeter

Description: 10 megohm input impedance and 0 to 1 kilovolt range, ac and dc; ohmmeter, accuracy, within 0.1%. Test probes must be insulated to prevent accidental shorting.

Purpose: Check voltages and resistances.

Recommended type: TEKTRONIX DM501A Digital Multimeter.

3. Test Oscilloscope

Description: Frequency response, dc to 50 megahertz minimum; deflection factor, 1 millivolt to 5 volts/division. A 10X, 10-megohm voltage probe should be used to reduce circuit loading for voltage measurements.

Purpose: Check operating waveforms.

4. Calibration Fixtures

(A) Extender Set (board)

Purpose: Troubleshooting the A2 and A5 boards (see Fig. 4-5).

Recommended type: Tektronix 067-1068-00 Cable Set (board extender).

(B) Extender Set (plug-in)

Purpose: Troubleshooting with 5D10 extended. (See Fig. 4-5).

Recommended type: Tektronix 067-0645-03. (2 required)

(C) Signature Analyzer

Description: Start/Stop gating inputs, 4 digit hexadecimal readout, Logic level indicator.

Purpose: Digital circuits troubleshooting.

Recommended types: a. TEKTRONIX 067-1090-00 Signature Analyzer.

b. SONY/TEKTRONIX 308 Data Analyzer.

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure is arranged to check the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection and operation of associated equipment. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, replace it using the replacement procedures given under Corrective Maintenance.

1. CHECK CONTROL SETTINGS

Incorrect control settings can indicate a trouble that does not exist. If there is any question about the correct function or operation of any control on the 5D10, refer to Section 2, Operating Instructions.

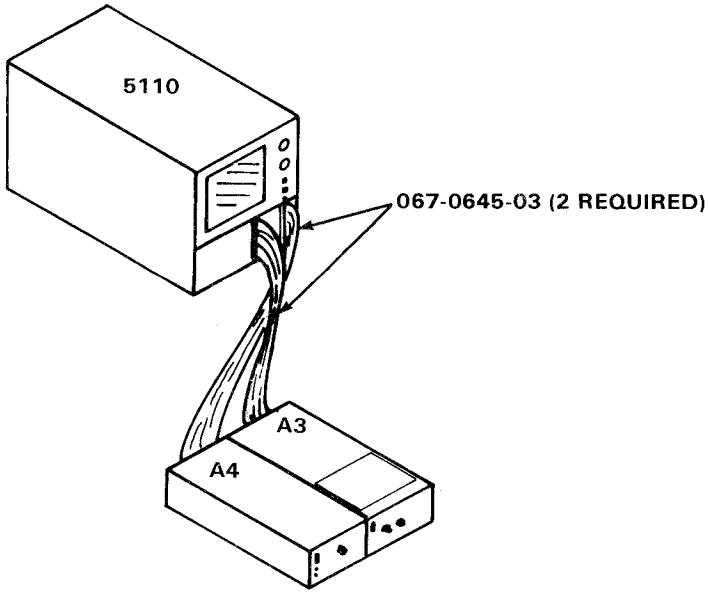
2. CHECK ASSOCIATED EQUIPMENT

Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Also, check that the input signals are properly connected and that the interconnecting cables are not defective. Check the line-voltage source.

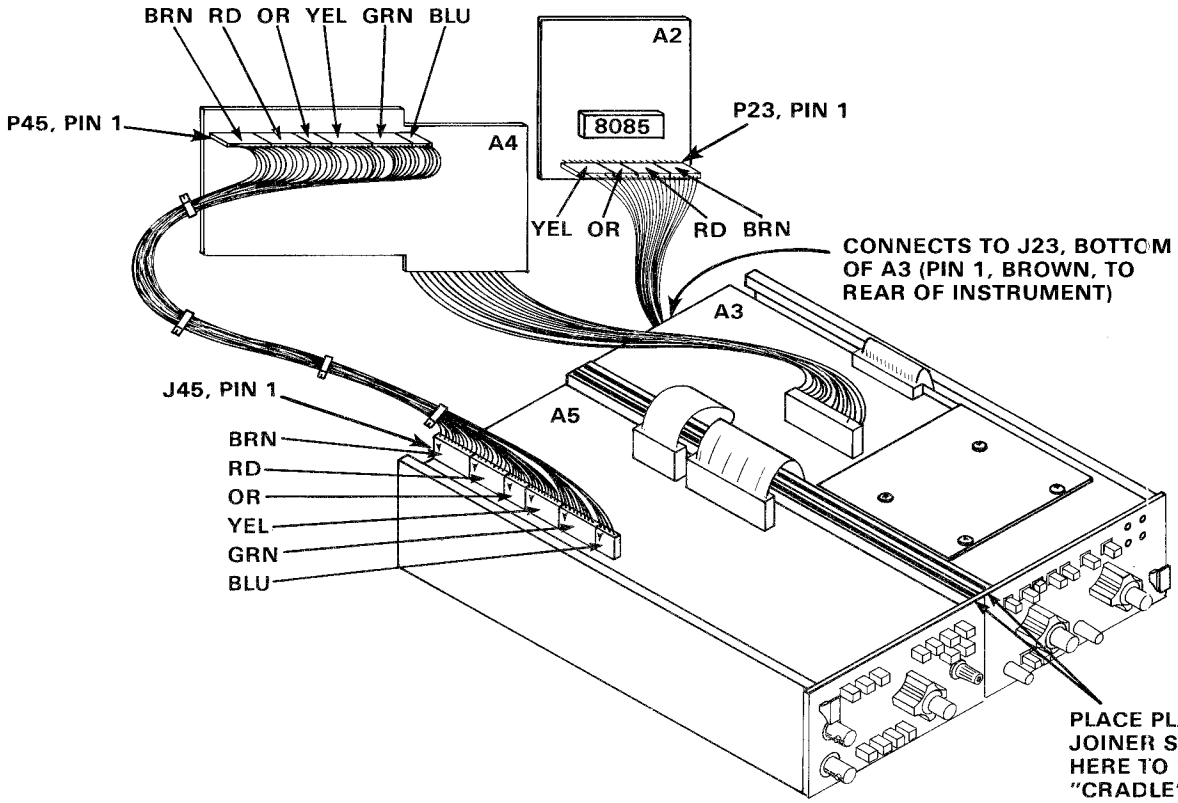
3. VISUAL CHECK

Visually check any part of the instrument where the trouble may be located. Many troubles can be found by visible indications such as unsoldered connections, broken wires, damaged circuits, and damaged components. Especially check that all cables and link plugs are properly installed (see Table 4-1) and fully engaged.

A. 067-0645-03 PLUG-IN EXTENDER SET



B. 067-1068-00 BOARD EXTENDER CABLE SET (2 CABLES SHOWN; OTHERS PROVIDED FOR SIGNATURE ANALYSIS TROUBLESHOOTING)



3697-53

Figure 4-5. Proper connection of the 067-1068-00 board extender cable set and 067-0645-03 plug-in extender set.

4. ISOLATE TROUBLE TO A CIRCUIT

To isolate the trouble to a circuit the 5D10 provides a Power-up Self Test routine when mainframe power is turned on. When either the SAVE or SAVE REF button is pressed (before power-up) the 5D10 displays a graticule and box pattern (for vertical and horizontal centering) when mainframe power is turned on. If errors are encountered during the diagnostic tests, the crt may display "ERROR" and possibly a number. When this occurs the service technician should refer to the Volume II 5D10 Diagnostic Troubleshooting Manual.

During self test, in addition to the box pattern display and readout messages, the TRIG'D and POSSIBLE UNDERSAMPLING indicators blink off and on several times. Failure of this activity to occur usually indicates that the self test has failed to run. Failure of the self test to run usually indicates a failure in the microprocessor circuits. Refer to the Volume II 5D10 Diagnostic Troubleshooting Service Manual.

An absence of a crt display (or distorted crt display) usually indicates a failure of the Display Output circuits. Refer to Troubleshooting the Display Output Circuits in this section.

Incorrect operation in all circuits often indicates trouble in the power-supply circuits. Refer to Troubleshooting the Power Supply in this section and to the power-supply Calibration and Maintenance information in the oscilloscope mainframe service manual. A defective component elsewhere in the oscilloscope system may appear as a power-supply symptom and also may affect the operation of other circuits.

5. CHECK INSTRUMENT ADJUSTMENT

Check the electrical adjustment of this instrument, or of the affected circuit if the trouble appears in one circuit. If the apparent trouble cannot be isolated to a defective component, the trouble may only be a result of maladjustment. Complete adjustment instructions are given in Section 5, Calibration.

6. CHECK VOLTAGES AND WAVEFORMS

Often the defective component can be located by checking for the correct voltages or waveforms in the circuit. Typical voltages and waveforms are given in Section 8, Diagrams and Circuit Board Illustrations.

NOTE

Voltages and waveforms given in Section 8, Diagrams and Circuit Board Illustrations, are not absolute and may vary slightly between 5D10 Waveform Digitizers. To obtain operating conditions used to take these readings, see the Voltage and Waveform Conditions adjacent to the schematic.

The Voltages and Waveforms aid in troubleshooting even if the circuit is not operating to produce a time-voltage signal. Observe the voltage and waveform at each point and compare with the voltage and waveform found in the manual. Is the voltage observed normally present at sometime during the operating waveform? Is this voltage intermediate between normal values? Is this voltage beyond the range of those given in the manual? Is the timing of the waveform within the correct range? The answers to these questions give important clues to the cause of the problem.

7. CHECK INDIVIDUAL COMPONENTS

The following procedures describe methods of checking individual components in the 5D10. Components which are soldered in place (excluding Integrated Circuits) are best checked by first disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

WARNING

To avoid electric-shock hazard, always turn off the mainframe power switch before removing or replacing components.

Fuses

Check for open fuses by checking continuity with an ohmmeter.

CAUTION

Before replacing an open fuse, determine the cause of the failure. Refer to the Power Supplies and Power Distribution diagram and the adjacent board dolly, in the foldout section at the rear of this manual, for component locations. Refer also to Troubleshooting the Power Supply in this section.

Refer to Replaceable Electrical Parts for correct fuse part numbers. Refer to Figure 4-6 for location of fuses.

Transistors

A good check of transistor operation is actual performance under operating conditions. A transistor can most effectively be checked by substituting a new component for it (or one which has been previously checked). However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static type testers are not recommended, since they do not check operation under simulated operating conditions.

Integrated Circuits

Integrated circuits can be checked with a test oscilloscope, signature analyzer, digital tester or by direct substitution.

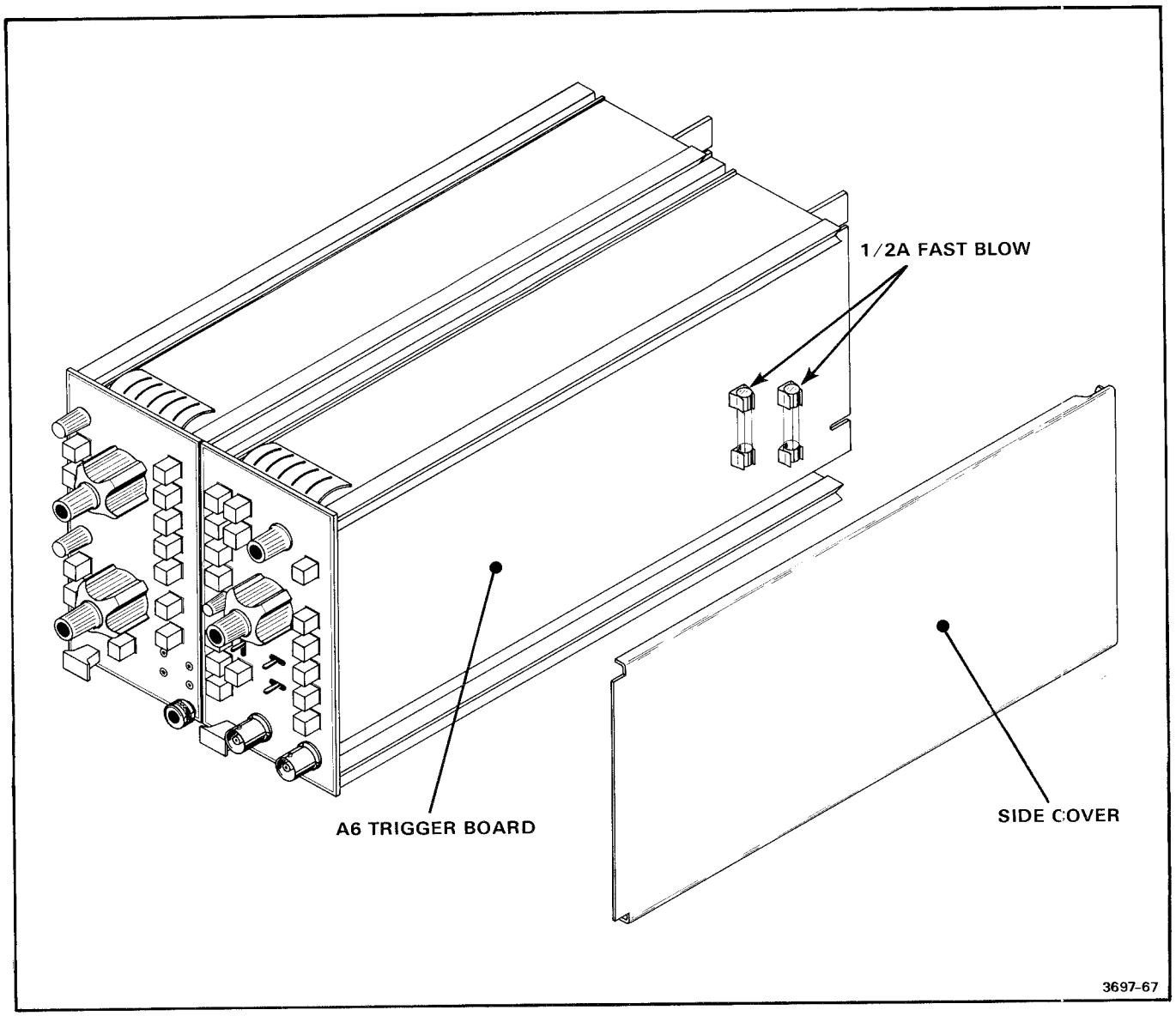


Figure 4-6. Location of fuses in the 5D10.

CAUTION

Direct substitution must not be attempted with soldered in integrated circuits. The I.C., circuit board or both could be damaged due to the heat required to melt the solder from the connections. Refer to Soldering Techniques later in this section. Use care when checking voltages and waveforms around the integrated circuits so that adjacent leads are not shorted together. The integrated circuit test clip provides a convenient means of clipping a test probe to the in-line, multi-pin integrated circuits.

A good understanding of the circuit operation is essential to troubleshooting circuits using integrated circuits if a signature analyzer is not available. Operating conditions and other information for the Integrated circuits are given in Section 3, Theory of Operation and Section 8, Diagrams and Circuit Board Illustrations.

Diodes

A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter on a scale having a low internal source current, such as the R×1k scale. The resistance should be very high in one direction and very low when the meter leads are reversed.

CAUTION

When checking diodes, do not use an ohmmeter scale that has a high internal current, since high currents may damage the diodes under test.

Resistors

Check the resistors with an ohmmeter. Resistor tolerances are given in Section 7, Replaceable Electrical Parts. Normally, resistors do not need to be replaced unless the measured value varies widely from the specified value.

Capacitors

A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking if the capacitor passes ac signals.

8. REPAIR AND ADJUST THE CIRCUIT

If any defective parts are located, follow the replacement procedures given under Component Replacement in this section. Check the performance of any circuit that has been repaired or that has had any electrical components replaced. Adjustment of the circuit may be necessary.

TROUBLESHOOTING SPECIFIC CIRCUITS

The following information is provided as a guideline for troubleshooting circuits not covered in the 5D10 Diagnostic Troubleshooting Service Manual (Volume 2).

TROUBLESHOOTING THE POWER SUPPLY

1. Failure to supply correct output voltages may be due to causes other than a defect in the power supply itself; a blown fuse, defective extender cable (or interface connector), or a current overload in either the mainframe or the 5D10 may be causing the problem. First check the −30 volt, +30 volt, +5 volt ("+5 VA"), +38 volt, and the −38 volt power supplies provided by the mainframe. (See steps 2 and 3 below.)

   The 5D10 power supply may be operating properly, but be in the current-limit mode, caused by an overload or short-circuit on its outputs. (See step 4).

2. If the 5D10 causes a short or overload of the mainframe +30 volt, −30 volt, or +5 volt ("+5 VA") power supplies, try locating the fault as follows:

   a. Isolate the fault to the vertical (left) or horizontal (right) module by disconnecting one plug-in extender cable, then the other.

   b. If the fault is in the 5D10 vertical module, isolate the fault to the A1 or A3 board by disconnecting A3 P13 and A1 P13. If the fault is in the horizontal module, isolate the fault to the A5 or A6 board by disconnecting A5 P56 and A6 P56. (Remember, the short circuit might be in the interconnecting cables.)

   c. On each board, remove decoupling inductors or resistors, or other low impedance loads, one at a time.

3. If one or both fuses for the +38 volt (A6 F940) and −38 volt (A6 F1040) power supplies are blown:

   a. Look for short circuits caused by solder splashes or metal objects such as wire clippings;

   b. Try disconnecting the +38 volt power supply (A6 P90), and observe waveforms shown opposite diagram 13 for the case of "A6 P90 open."

4. Check the outputs of A6 U740 to determine if the power supply is operating in the current-limit mode (this will identify which of the three outputs is overloaded) as follows:

   a. In normal operation, pin 8 of A6 U740 will be about 1.2 volts, and pins 1, 7, and 14 will be about 0 volts.

   b. In current-limit operation, pin 8 of A6 U740 will be about 0.7 volts; pin 7 will be about 3 volts if the +5 volt output is overloaded, pin 14 will be about 3 volts if the +7.5 volt output is overloaded, or pin 1 will be about 3 volts if the −7.5 volt is overloaded. (Remember that operation in the current-limit mode may be due to either a real overcurrent condition or to a failure of the current-limit circuitry itself.)

5. A short circuit or overload on the +5 volt ("+5 VL"), +7.5 volt, or −7.5 volt power supplies may be located as follows:

   a. Determine which supply is overloaded. (See step 4)

   b. Isolate the fault to the vertical (left) or horizontal (right) module by disconnecting A6 P99 and A3 P99.

   c. If the fault is in the vertical module, isolate the fault to the A1 board, or to the A2 and A3 boards together, by disconnecting A1 P13 and A3 P13. If the fault is on the A2 and A3 boards, isolate the fault to the A2 or A3 board by removing the A2 board. (See removal instructions, Section 4, Maintenance.) If the fault is in the horizontal module, isolate the fault to the A6 board, or to the A4 and A5 boards together, by disconnecting A6 P56 and A5 P56. If the fault is on the A4 and A5 boards, isolate the fault to the A4 or A5 board by removing the A4 board. (See removal instructions, Section 4, Maintenance.)

NOTE

If both P99 and P56 are disconnected simultaneously, the power supply will not function correctly unless a resistor (about 5 to 10 ohms, 5 watts) is connected between pin 2 and 3 of A6 P99. (Do not solder to the pins !)

NOTE

This procedure will directly locate a short-circuit fault. If the fault draws excessive current, but is not a "dead short", disconnecting a normally operating load may relieve the power supply overcurrent condition. Beware of this possibility.

6. Proper operation of the current-limit mode may be checked by introducing a "dead short" on each output, but only at the **RISK OF DOING SERIOUS DAMAGE** if the protection is defective. A safe alternative would be to overload the supplies just beyond the point where current-limit operation should cause the output voltages to decrease, and observe the response. With the instrument completely connected and operating, connect a 100 ohm, 1 watt resistor between chassis ground and A6 P99 pin 1 and then A6 P99 pin 4, and observe the voltages drop from 7.5 volts to about 3 or 4 volts. Then connect a 3 ohm, 10 watt resistor between chassis ground and A6 P99 pin 2; observe the voltage drop from 5 volts to about 3 or 4 volts. If these responses do not occur, the current-limit circuitry is not operating properly, and must be repaired immediately.

NOTE

When +7.5 volt or −7.5 volt faults cause current-limit operation, an audible buzzing may be heard. The control loop oscillates in this condition, but this is not abnormal or harmful.

7. Controlled rectifier A6 Q831 and associated components operate to protect against damage caused by higher-than-normal voltages at the +5 volt output, diode A6 CR601, and transistor A6 Q800. Overvoltage at any of these devices will trigger the controlled rectifier, and shut down the power supply, by removing the drive at the gate of A6 Q800. Troubleshooting this circuit may be difficult.

   a. If all power supply voltages from the mainframe are correct, and the voltage across A6 VR940 is approximately 1.4 volts, A6 Q831 has probably been triggered and latched in the conducting state. The voltage across A6 VR940 should be about 10 volts, and A6 Q831 should not be conducting. If the voltage across A6 VR940 is less than one volt, a shorted component should be suspected.

   b. If A6 Q831 is latched, turn off the power and wait a few seconds before turning on the power again. Capacitors must discharge before A6 Q831 will unlatch.

   c. Try disconnecting the +38 volt power supply at A6 P90. Observe waveforms shown opposite diagram 13 for the case of "A6 P90 open." If A6 Q831 triggers and latches in this condition, the defect is probably in the protection circuit itself.

   d. Try operating the mainframe from a variable transformer at reduced line voltage. Compare observed waveforms with illustrations opposite diagram 13 ; look for correct shape with reduced amplitude. Check to see that the supply regulates; that is, the +5 volt output ("+5 VL") is no higher than the +5 volt supply from the mainframe ("+5 VA").

   e. If A6 Q831 is latching immediately after the power is turned on, try observing operation of the circuit during this brief period using a storage oscilloscope. Trigger the storage oscilloscope sweep on the negative slope of the −38 volt power supply (as it rises from zero when power is turned on).

   f. If you suspect that A6 Q831 is being triggered by excessive drain voltage at A6 Q800, (rather than overvoltage at the +5 volt secondary or output) do NOT attempt to prove this by disconnecting A6 VR801, A6 VR802, or A6 R809 to observe circuit operation with the protection disabled, because excessive drain voltage will quickly destroy A6 Q800.

TROUBLESHOOTING THE DISPLAY OUTPUT CIRCUITS

The display output circuit consists of identical vertical and horizontal sections, and are driven by common control circuits. If both the vertical and horizontal sections exhibit the same symptoms, the common circuits would be suspect. If only one circuit is malfunctioning, defects may be isolated by comparing the operation of the circuit in question with the operation of the working circuit. Each circuit operates in one of two modes; dot or vector. In dot mode, each circuit acts as a unity-gain voltage follower. In vector mode, each circuit consists of a differential amplifier, a sample/hold, and an integrator inside a feedback loop. Defects appearing in only one mode would make any circuit function unique to that mode suspect.

Preliminary Setup Instructions

The self-test graticule pattern provides the best approach to troubleshooting. This pattern provides the necessary displays for checking nearly all of the display output circuits, particularly those that follow.

To start, assure the Link-Plug (jumpers) are connected for the Report Mode self-test routine. Refer to the Volume 2 5D10 Diagnostic Troubleshooting Service Manual. Turn the mainframe power off, press the SAVE button in, then turn the power back on. (Be certain that the self test has actually run and completed.) The steady calibration pattern that appears on the screen is a composite of both dot mode and vector mode information, displayed in alternating frames. The signal on A3 U710 pin 6 may be used to trigger an oscilloscope when troubleshooting

these circuits. The signals and voltages specified for dot or vector mode in the following procedures apply when the signal on A3 U710 pin 6 indicates the corresponding state. A high TTL level indicates dot mode, and a low TTL level indicates vector (or join) mode.

Troubleshooting Methods

The above Preliminary Setup Instructions must be performed before proceeding.

1. Check Inputs and Outputs

   a. Check the signal at the points listed in Table 4-3 against the waveforms shown on the appropriate diagrams in the foldout section (at the rear of this manual). An incorrect signal at any of these points may indicate the problem does not originate in the output circuits; check for incorrect signals at the corresponding source circuits.

   b. Check for correct signals at P96, pin 1 and P95, pin 1; the signals at these points should be the attenuated (8X) version of the signals at A3 U330, pin 6 and A3 U230, pin 6, respectively (shown on Schematic 12). If these signals are correct, the problem may originate in the mainframe. If the 5D10 is operating normally, but no display is visible on screen, check the +200V supply in the oscilloscope mainframe.

2. Check Common Circuits

   Check signals as shown in Table 4-4. If any of these signals are incorrect, check the associated components for proper operation.

3. Dot Mode

   Check Dot Mode on schematic diagram 12 as follows:

   a. Switches U350A and U350D should be closed in Dot Mode and open in Vector Mode.

   b. Transistors Q326 and Q225 should be biased off (gate at approximately −7.5 V) in Dot Mode, and biased on (gate at 0 V) in Vector Mode.

TABLE 4-3
Display Output Signals

Test Point	Signal	Schematic
A3 U530, pin 6	Y	11
A3 U425, pin 6	X	11
Q310 Base	$\overline{\text{Vector}}$	12
A3 U710, pin 5	Disp. Join/Dots	12
U710, pin 11	Plot Out	3 (<0.4V, TTL low level)

TABLE 4-4
Common Circuit Signals
(Voltage values given are approximate)

Test Points (see schematic 12)	Dot	MODE Vector	Plot Out
A3 U620, pin 10	−7.5 V	Vector	Vector
A3 U620, pin 3	+7.5 V	$\overline{\text{Vector}}$	$\overline{\text{Vector}}$
A3 U620, pin 11	−7.5 V	$\overline{\text{Vector}}$	Vector
A3 U610, pin 14	−7.5 V	+7.5 V	−7.5 V
A3 CR427, anode	−7.5 V	0 V	−7.5 V
A3 U610, pin 1	−7.5 V	−7.5 V	+7.5 V
A3 CR200, anode	−7.5 V	−7.5 V	0 V

4. Vector Mode

   Check Vector Mode on schematic diagram 12 as follows:

   a. Switches U435A and U435D should be open in Dot Mode. In Vector Mode they should be closed when the Vector signal line is low, and open when it is high.

   b. The signal on pin 6 of voltage followers U445 and U450 should be the same as the signal on C230 and C240, respectively.

   c. Check for correct operation of Q326 and Q225 as described earlier in step 3, Dot Mode.

   d. U435B and U435C should be open in both the Dot and Vector Modes.

5. General Waveforms

   Set the test oscilloscope to trigger on the + slope of the signal at pin 6 of A3 U710. Other test oscilloscope settings and 5D10 test points are located with their associated waveforms in Figure 4-7. Proceed to waveform A instructions in Figure 4-7.

NOTE

The dc level on pin 6 of A3 U445 or A3 U450 during the Dot Mode portion of the display may vary between instruments. However, there should be no voltage droop apparent. Droop may be caused by excessive leakage current in A3 U435, A3 C230, A3 C240, or excessive bias current on A3 U445 or A3 U450.

6. Plot Out Mode

   First check the "3. Dot Mode" and "4. Vector Mode" operation before proceeding with the Plot Out Mode troubleshooting checks.

a. Push the PLOT button in, and perform the proceeding "2. Check Common Circuits" operation. Remember that after the Plot Out function has completed plotting the display, the 5D10 will return to the normal display mode. Assure the Plot Out function is active (Plot Out TTL high level at A3 U710, pin 11) when checking the Plot Out circuit operation.

b. Check for proper operation of A3 Q325 and A3 Q226. In Plot Out Mode, they should be biased on (gate at 0 V). Check for proper operation of switches A3 U350B and C; they should be closed in Plot Out Mode.

Check that zener diodes A3 VR130, VR131, VR140, and VR250 are not shorted.

Check the integrity of integrator and sample-hold capactors A3 C440, C300, C349 and C351.

Check operation of switches A3 U435B and C; they should be closed in Plot Out Mode. Droop of the voltage at A3 U445, pin 6, or A3 U450, pin 6, during hold time (Vector Low) may be caused by excessive leakage current in A3 C349, C351, A3 U435B or C, or by excessive bias current in A3 U445 or A3 U450. This will be most noticeable during the plotting of the box pattern.

If the X and Y - axis deflection is operating correctly, but the display is always blanked or never blanked, check the Z-Axis circuits. Start at A6 U1000, pin 8 and trace back to A5 U620B. Signature Analysis Test 15 may be helpful. Refer to Volume 2 5D10 Diagnostic Troubleshooting Service Manual.

TROUBLESHOOTING LEFT PLUG-IN CHANNEL SWITCH LOGIC

Channel switch logic circuits in 5100-series oscilloscopes have been modified since they have been in production. The "Old" and "New" versions work differently with the 5D10. Refer to Section 3, Theory of Operation, for description of the two modes of operation of this circuitry.

"Old" mainframes are the 5110, 5111 (no "A" suffix), and the 5112, 5113, and 5115. The "New" mainframe, as of this printing is the 5111A. (Use of the 5D10 Left Plug-In feature with 5400 and 5200 mainframes is not recommended.)

When servicing this circuitry (because the 5D10 will not work properly with a dual-trace amplifier installed in the left vertical compartment) it is necessary to know the mainframe version in which the problem occurred. Therefore, troubleshooting this circuitry is best done in the mainframe in which the 5D10 was used when the problem was observed. Second best would be to use a mainframe of the same type — "new" or "old." (Remember that the failure might be due to an improperly installed modification on the interface-board wire from J603, pin B11 to U640, pin 1.) As a last resort, a mainframe of opposite type may be used, by following the procedures suggested below.

"New" Mainframes Used with the 5D10

If a "new" mainframe is used with the 5D10, operation of parts required to work with "old" mainframes may be checked by applying small pieces of tape to interface contacts B21 and A6 on the A6-Trigger Board, and B21 on the A3-Output Board, to disconnect these circuits. Refer to Figure 4-8. Observe waveform "CF" at A6 U1000, pin 6, with a high level of about 1.5 volts, and slower than normal risetime. Observe a high level, with no activity, at A6 U1020, pin 9. Observe approximately 0 volt at A6 U1000, pin 10. Verify that A6 U1000, pin 4 is active low by measuring (approximately 5 volts) between A6 U1000, pin 4 and A6 U1000, pin 14 with a digital voltmeter. The left plug-in will NOT switch channels while this test is being performed. Remember to remove the tape from the interface contacts when finished.

"Old" Mainframes Used with the 5D10

If an "old" mainframe is used with the 5D10, the operation of components required to work with the "new" mainframes may be checked by connecting a 100 kΩ resistor from A6 R1010 to the +30 volt power supply (see Fig. 4-9). Observe waveform "CG" at A6 J1020, pin 8, and waveform "CH" at A6 R1021-A6 C1020. Observe waveform "CF" at A6 U1000, pin 6. Measure approximately 0 volt at A6 U1000, pin 5. Observe a square wave, at half the frequency of waveform "CF", at A6 U1000, pin 4. The left plug-in will switch channels correctly while this test is being performed, providing that the SECONDS/DIV switch is set to 1 m or slower. Remember to remove the extra 100 kΩ resistor when finished.

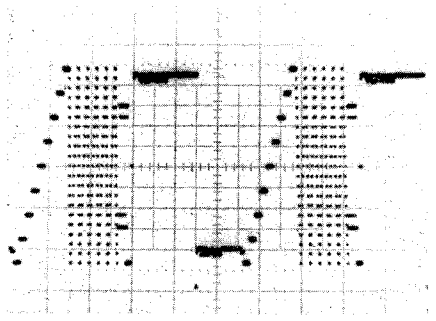
POSSIBLE UNDERSAMPLING INDICATOR

The Possible Undersampling Indicator normally is driven by two asynchronous signals: the sampling clock (internal or external, selected by the SECONDS/DIVISION switch) and the trigger. Troubleshooting is difficult and confusing in this condition. As a troubleshooting aid, use a signal from the sample clock divider chain as the triggering signal.

Connect a 10X probe from A6 U440, pin 1 to the CH1 bnc input. Set the CH1 VOLTS/DIV switch to 50m (500 mV/division with probe) and position the waveform to midscreen. Select TRIGGERING SOURCE CH1, ⎍ SLOPE, and adjust LEVEL control; the TRIG'D indicator must be on. "Trigger" at A6 U330, pin 6 is a pulse occurring at a 10 kHz rate (the SECONDS/DIV CAL knob must be fully clockwise, in detent). Set the SECONDS/DIV switch to 1m and 2m positions, and observe the waveforms shown in Figure 4-10. For both cases, the test scope should be triggered by "Trigger" (A6 U330, pin 6).

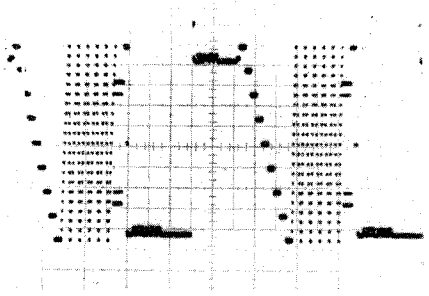
GROUND PIN 3 OF A3 U550 FOR WAVEFORMS A THROUGH E (SN B020099 & BELOW).

A.



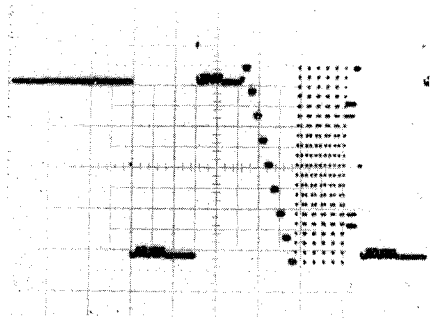
A. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U530, pin 6

B.



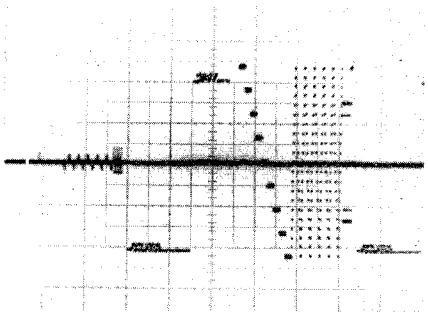
B. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U550, pin 6

C.



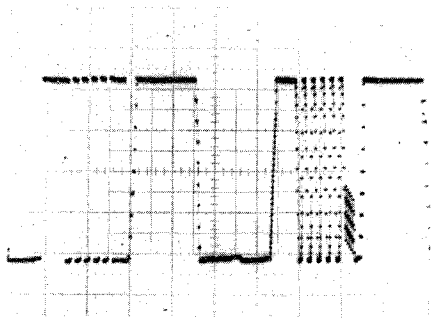
C. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U445, pin 6

D.



D. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U440, pin 2

E.



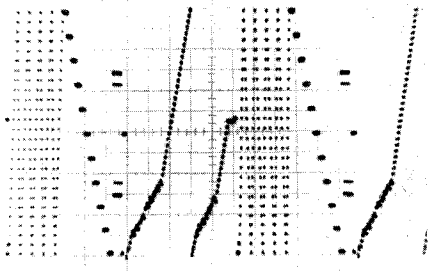
E. Test Oscilloscope:
VOLTS/DIV ..... 2 V
TIME/DIV.....2 mS
5D10 Test Point:
A3 U330, pin 6

3697-14

Figure 4-7. Display output waveforms.

GROUND PIN 3 OF A3 U430 FOR WAVEFORMS F THROUGH J (SN B020099 & BELOW).

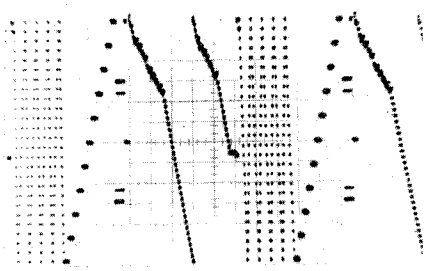
F.



F. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U425, pin 6

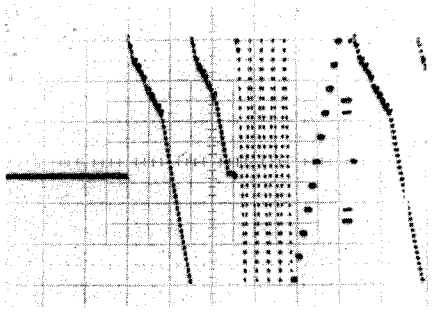
G.



G. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U430, pin 6

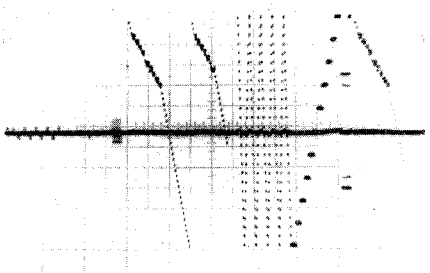
H.



H. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U450, pin 6

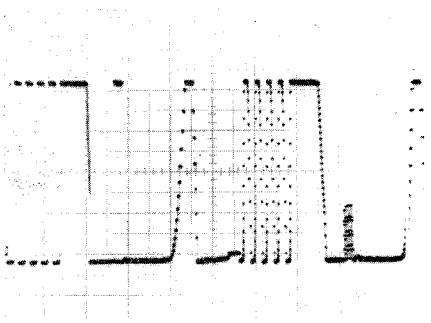
I.



I. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U440, pin 10

J.



J. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

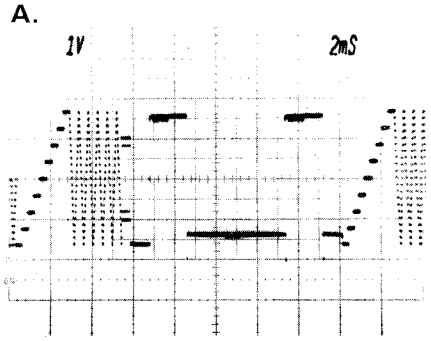
5D10 Test Point:
A3 U230, pin 6

3697-15

Figure 4-7. Display output waveforms (cont).

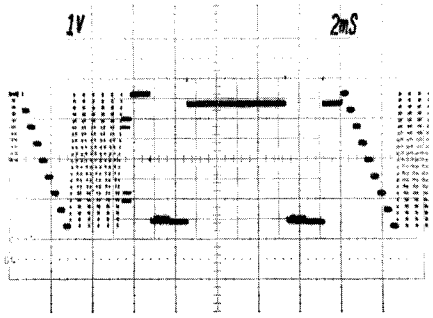
GROUND PIN 3 OF A3 U550 FOR WAVEFORMS A THROUGH E (SN B020100 & UP).

A.



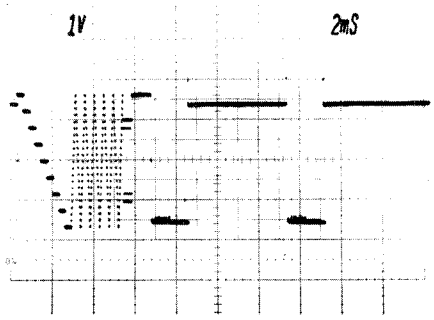
A. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U530, pin 6

B.



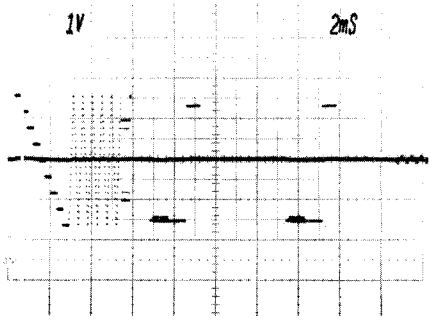
B. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U550, pin 6

C.



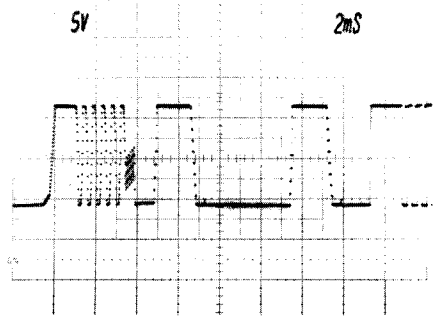
C. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U445, pin 6

D.



D. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS
5D10 Test Point:
A3 U440, pin 2

E.



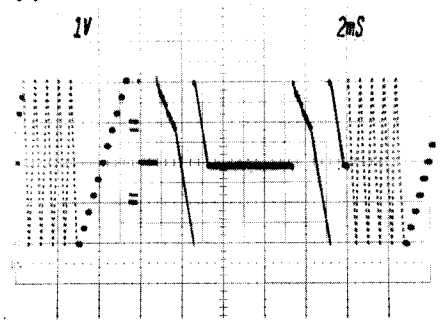
E. Test Oscilloscope:
VOLTS/DIV ..... 2 V
TIME/DIV.....2 mS
5D10 Test Point:
A3 U330, pin 6

3697-325

Figure 4-7. Display output waveforms.

GROUND PIN 3 OF A3 U430 FOR WAVEFORMS F THROUGH J (SN B020100 & UP).

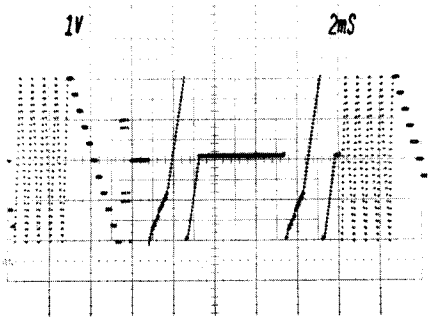
F.



F. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U425, pin 6

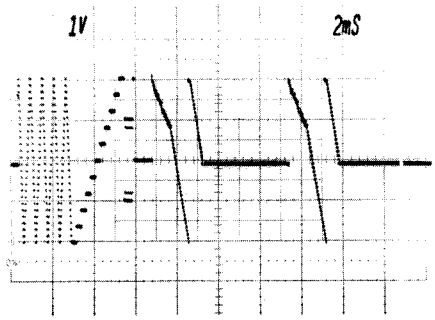
G.



G. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U430, pin 6

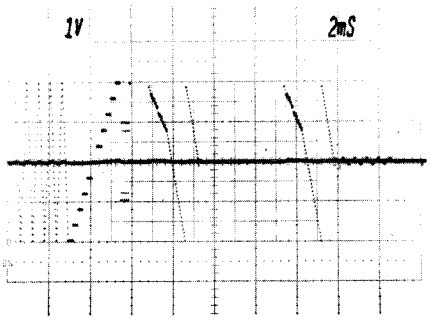
H.



H. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U450, pin 6

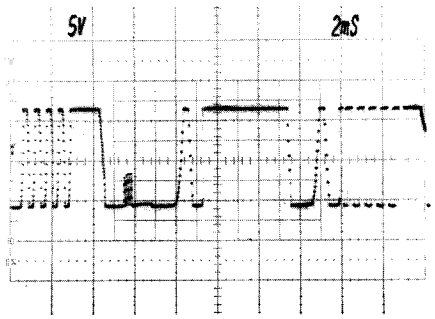
I.



I. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U440, pin 10

J.



J. Test Oscilloscope:
VOLTS/DIV ..... 500 mV
TIME/DIV.....2 mS

5D10 Test Point:
A3 U230, pin 6

3697-326

Figure 4-7. Display output waveforms (cont).

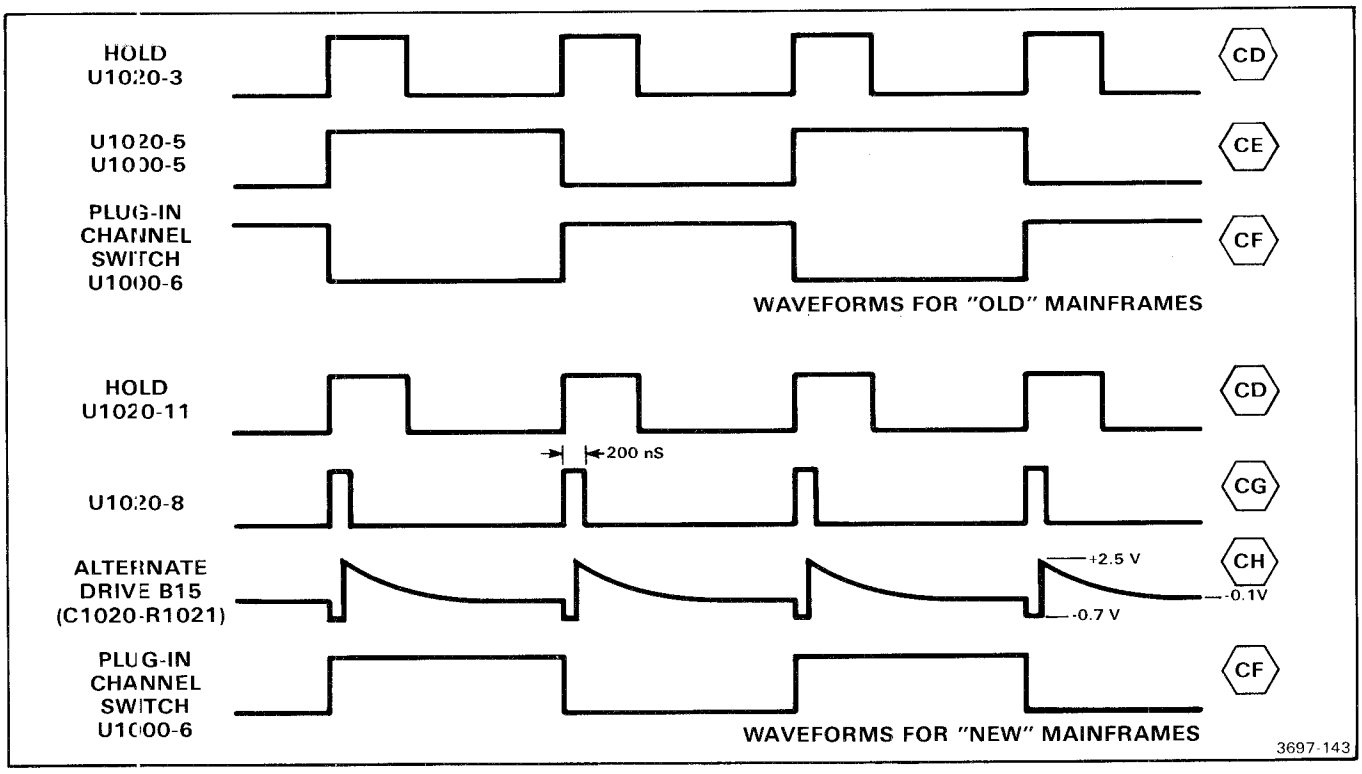


Figure 4-8. Test points and waveforms for checking operation of components unique to "New" mainframes.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and assembly repair. Special techniques required to replace components in the 5D10 Waveform Digitizer are given here.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from any source other than Tektronix, Inc., please check the electrical parts list for the proper value, rating, tolerance and description.

SPECIAL PARTS

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements, or are manufactured for Tektronix, Inc. to our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine manufacturer of parts, refer to Parts List, Cross Index Mfr. Code Number to Manufacturer.

ORDERING PARTS

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type.
2. Instrument serial number
3. A description of the part; if electrical, include circuit number.
4. Tektronix part number.

MAINFRAME COMPATIBILITY MODIFICATION

Most 5100-series mainframes need Interface Board modifications in order to be completely compatible with the 5D10 Waveform Digitizer. For a list of those mainframes requiring modification, refer to Table 1-1 in Section 1, General Information.

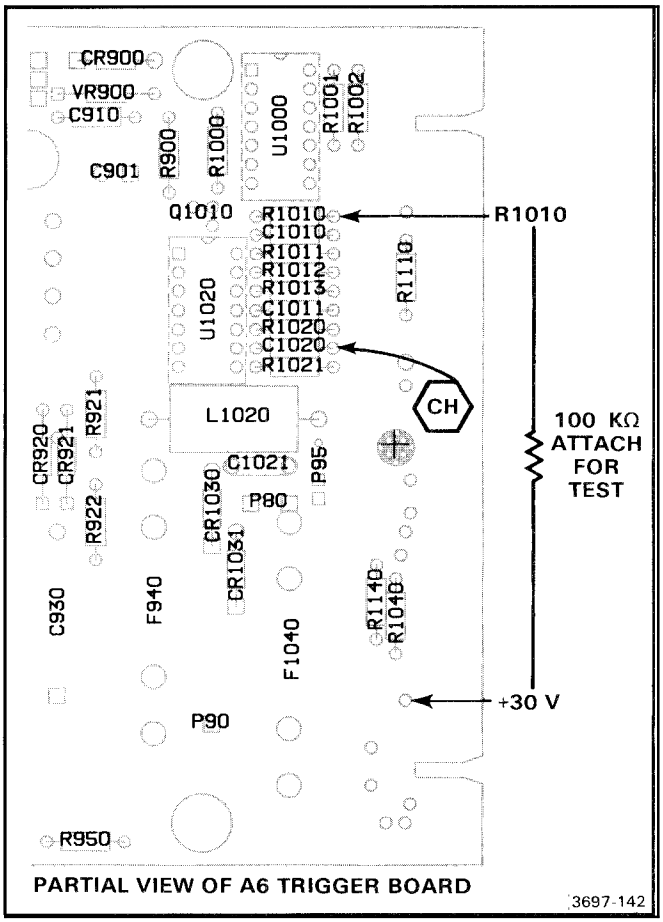


Figure 4-9. Connection of 100k Ohm resistor to +30 V supply to check operation of components unique to "New" mainframes.

MODIFICATION INSTRUCTIONS

Modifications need to be installed on the early 5100-series mainframe Interface Boards to allow operation with the 5D10 as specified below (refer to Table 1-1, in section 1):

- Add capability to digitize left plug-in compartment from 5D10 (M45180).
- Eliminate vertical trace shift that occurs when plug-ins are installed or removed (M44151).

To install these modifications, proceed as follows:

1. Add Left Plug-In Digitizing Capability

CAUTION

When this mainframe modification is installed, the 5B10N and 5B12N Time-Base units must not be used in the right vertical compartment if the left vertical compartment is also being used. The display signal output of the left plug-in will be loaded (nondestructively) by a time-base unit in the right-vertical compartment. If a vertical sweep is desired, install the Time-base unit in the Left Vertical compartment.

a. Remove the mainframe's Interface Board according to removal procedures provided in the Instruction Manual for that mainframe.

b. Install two 5 1/2-inch, 26 guage wires,on back (non-component side) of Interface Board as shown in Figure 4-11. The two wires connect the left vertical plug-in connector J601, pins A13 and B13 to the right vertical plug-in connector J602, pins A17 and A16, respectively.

c. Install one 2 3/4-inch, 26 gauge wire on back of Interface Board as shown in Figure 4-11. This wire connects the horizontal plug-in connector J603 pin B11, to U640, pin 1.

d. Proceed to step 2.

2. Eliminate Vertical Trace Shift

a. Install four 470k, 5%, 0.25 watt carbon resistors as shown in Figure 4-11.

b. Replace the Interface Board according to the board replacement procedures in the mainframe Instruction Manual.

SOLDERING TECHNIQUES

WARNING

To avoid electric-shock hazard, and instrument damage disconnect the 5D10 from the power source before soldering.

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts.

The desoldering and removal of parts is especially critical and should be done only with a vacuum solder extractor; preferably, one approved by a Tektronix Inc., Service Center.

Use wire solder with rosin core, 63% tin, 37% lead. Contact your local Tektronix Inc. representative or field office for approved solders.

All circuit boards used in this instrument are multilayer. Conductive paths between the top and bottom board layers may connect with one or any number of inner layers. Once this inner conductive path is broken (due mainly to poor soldering practices) between the layers, the board is unusable and must be replaced. Damage can void warranty.

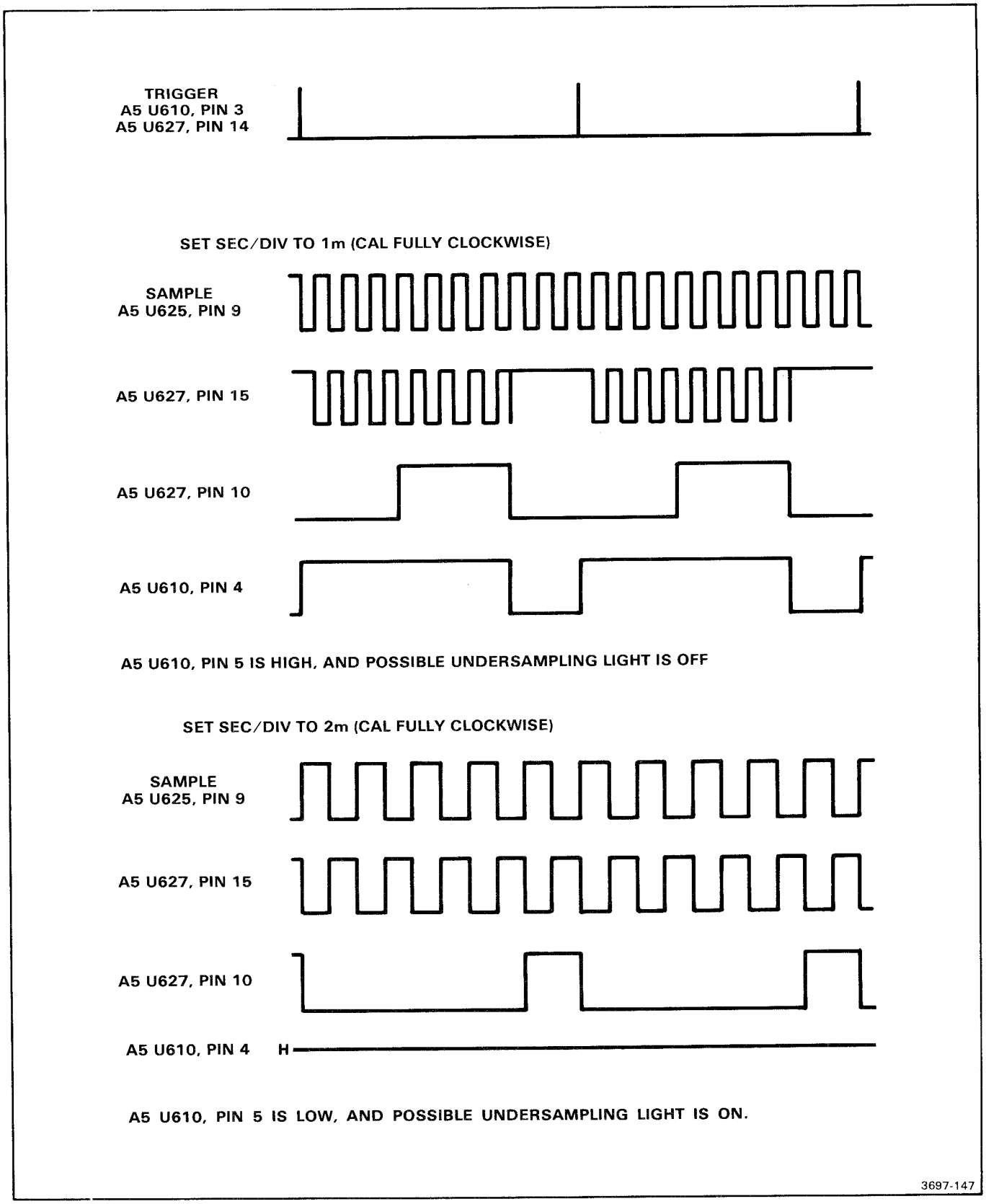


Figure 4-10. Troubleshooting waveforms for the Possible Undersampling circuits.

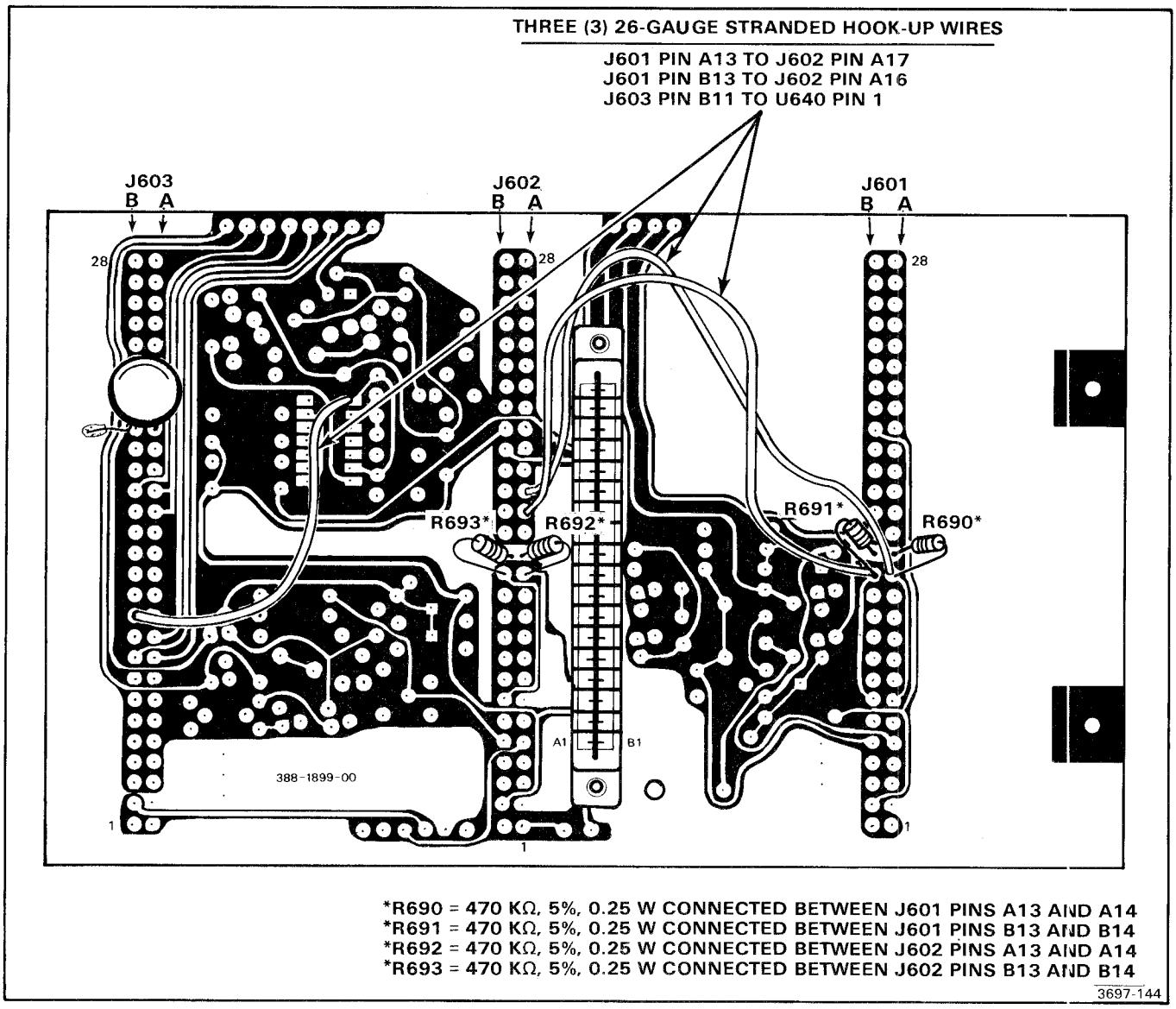


Figure 4-11. Modifications necessary on the early 5100-series Mainframe Interface boards to achieve compatibility with the 5D10.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum type desoldering equipment, should attempt repair of any board in this instrument.

When soldering on circuit boards or small wiring, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material, and melt the insulation from small wiring. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint.

The following technique should be used to replace a component on any of the circuit boards.

Touch the tip of the vacuum desoldering tool directly to the solder to be removed.

CAUTION

Excessive heat can cause the etched circuit wiring to separate from the board base material.

Never allow the solder extractor to remain on the board for more than three (3) seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for multi-pin components) must not be used. Damage can void warranty.

NOTE

Some components are difficult to remove from the circuit boards due to a bend placed in each lead during machine insertion of the component. The purpose of the bent leads is to hold the component in position during a flow-solder manufacturing process which solders all components at once. To make removal of machine inserted components easier, first remove the solder from the joint then straighten the leads of the component on the back of the circuit board using a small screwdriver or pliers.

When removing multi-pin components i.e., IC's, do not heat adjacent conductors consecutively (see Fig. 4-12). Allow a moment for the circuit board to cool before proceeding to the next pin.

Bend the leads of the replacement components to fit the holes in the circuit board. Insert the leads into the holes in the board, or as originally positioned.

Touch the iron to the connection and apply enough solder to make a firm solder joint.

Cut off any excess lead protruding through the board.

Clean the areas around the solder connection with a flux removing solvent. Be careful not to remove the information printed on the circuit board.

COMPONENT REMOVAL AND REPLACEMENT

CAUTION

To avoid component damage, always disconnect the assembly from the power source before removing or replacing components.

The exploded-view drawing associated with the Replaceable Mechanical Parts list (located at the rear of this manual) may be helpful in the disassembly procedures that follow.

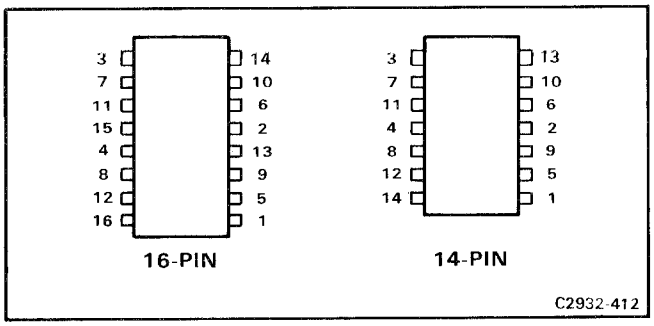


Figure 4-12. Recommended desoldering sequence.

SEMICONDUCTORS

Semiconductors should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of semiconductors may affect the adjustment of the instrument. When semiconductors are replaced, check the operation of circuits which may be affected.

Replacement semiconductors should be of the original type or a direct replacement. Lead configurations of the semiconductors used in this instrument are shown in Figure 4-3.

CAUTION

Do not remove stickers affixed to the top of EPROM's. Removal of this sticker will allow light into the chip, and may cause partial erasure of its data.

An extracting tool should be used to remove the in-line integrated circuits to prevent damaging the pins. This tool is available from Tektronix, Inc,; order Tektronix Part 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid one end disengaging from the socket before the other end.

Once an in-line integrated circuit is removed, a socket should be installed to prevent damage to the circuit board due to repeated soldering and desoldering. Recommended part numbers are as follows:

8 pin 136-0727-00;
14 pin 136-0728-00;
16 pin 136-0729-00;
20 pin 136-0752-00.

U213 Pin-To-Socket Alignment

If ROM U213 is removed from the socket on the A2 Microprocessor Board, be sure it is reinstalled properly. Figure 4-13 illustrates proper pin placement of the 24-pin ROM in the 28-pin socket. In instruments with serial number B020100 and above, U213 is a 28-pin ROM.

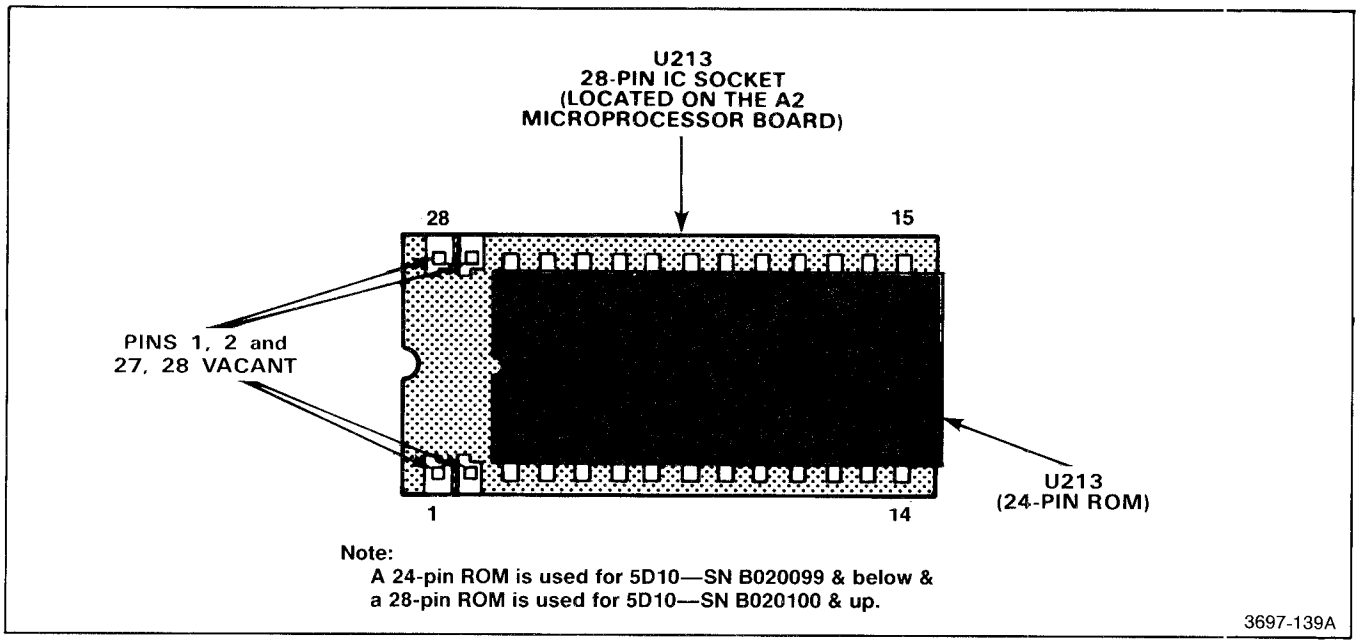


Figure 4-13. Proper insertion of U213 (24-pin ROM) into the 28-pin I.C. socket.

CIRCUIT BOARDS

If a circuit board is damaged beyond repair, replace the entire board assembly. Part numbers are given in Section 7, Replaceable Electrical Parts, for completely wired boards.

Some parts mounted on the board must be retained for use with the new assembly such as extension shafts, support posts, switch push-button knobs, lamps and board to front-panel wiring.

NOTE

Refer to Adjustment After Repair earlier in this section.

A1—Amplifier board replacement.

Refer to Figure 4-14 for location of parts mentioned in the following removal and installation procedures.

Remove the A1-Amplifier board as follows:

1. Remove the left side cover.
2. Rotate both CAL and both POS controls fully clockwise then loosen the 4 setscrews (.050 Hex key) from the extension shaft-to-pot couplers.

Remove the 4 extension shafts. Do not remove the couplers.

NOTE

Locate the 2 CAL setscrews through the large access holes in the board. Do not remove the couplers.

3. Unplug the 4 cables.
4. Unsolder the wires to the front-panel bnc connectors (at the bnc; not at the board).

NOTE

If a new A1 board is to be installed remove the 4 wires and 2 lamps from the board (after removing the board from the instrument) and solder them into the new board. Refer to Figure 4-15 and Soldering Techniques earlier in this section. Save the pushbutton knobs and extension shaft and the four shaft couplers.

5. Remove the 10 screws marked with arrows in Figure 4-14.
6. Lift the rear of the board to clear the camswitch alignment pegs, then slide the board toward the rear until the push buttons clear the front panel.
7. Install cam contact protectors if available; otherwise place the board on a tray or other uncluttered flat surface to avoid damage to switch contacts.

Install the A1-Amplfiier board as follows (refer to Figure 4-14):

CAUTION

Do not drag cam switch contacts (located on back side of board in areas shown in Fig. 4-19) across alignment pegs. Damage or misalignment of the contact wipers could result.

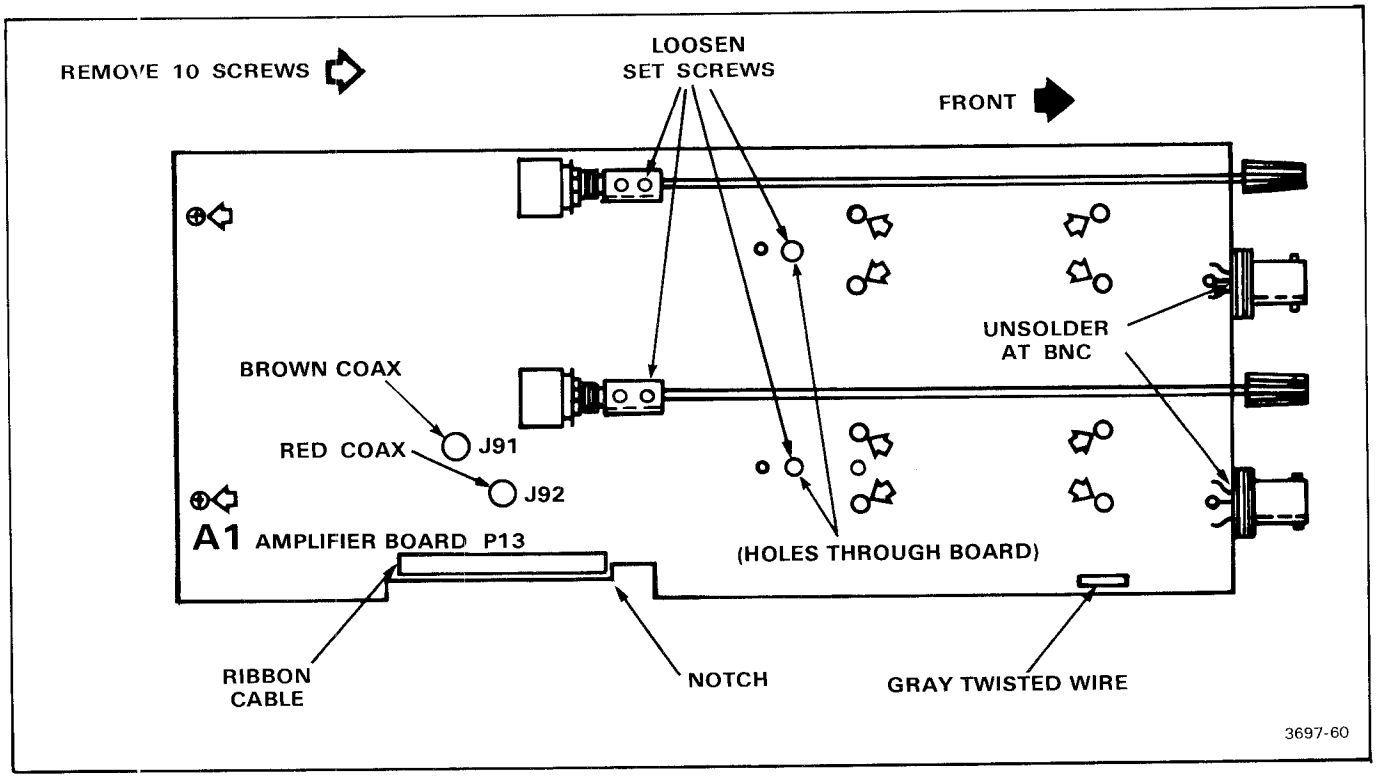


Figure 4-14. Securing screw and connector locations.

1. Align the push-buttons with the front panel. Guide the shaft extender for the INVERT switch into the front-panel while maintaining as much height as possible on the rear of the board to clear the camswitch contacts. Dress the cabling into the notch in the board.

2. Install 10 securing screws.

3. Solder the 6 wires to the front-panel bnc connectors.

4. Connect the 4 cables to the appropriate connectors. Refer to Figure 4-14.

5. Install extension shafts (4).

6. Install the side cover.

A2-Microprocessor board replacement.

Refer to Figure 4-16 for location of parts mentioned in the following removal and installation procedures.

Remove the A2-Microprocessor board as follows:

1. Remove the A1 board. Follow the A1-Amplifier board removal procedure.

2. Remove 2 screws; then remove the shield.

3. Separate the multipin connector by pulling the A2 board vertically away from the A3 board.

Install the A2-Microprocessor board as follows:

1. Reverse the removal procedure. Care should be exercized in aligning the board-to-board multipin connector.

A3-Output board replacement.

Refer to Figure 4-17 for location of parts mentioned in the following removal and installation procedures.

Remove the A3-Output board as follows:

1. Remove boards A1 and A2. Follow the removal procedures given earlier.

2. Separate the 2 plug-in halves. Refer to Figure 4-17.

3. Unplug 6 harmonica connectors and 4 ribbon cables.

4. Unsolder 4 wires (plotter output jacks) at the front panel.

5. Remove 2 cam switch actuator drum assemblies as follows. Record their location (CH 1 or CH 2). The actuator drums are different.

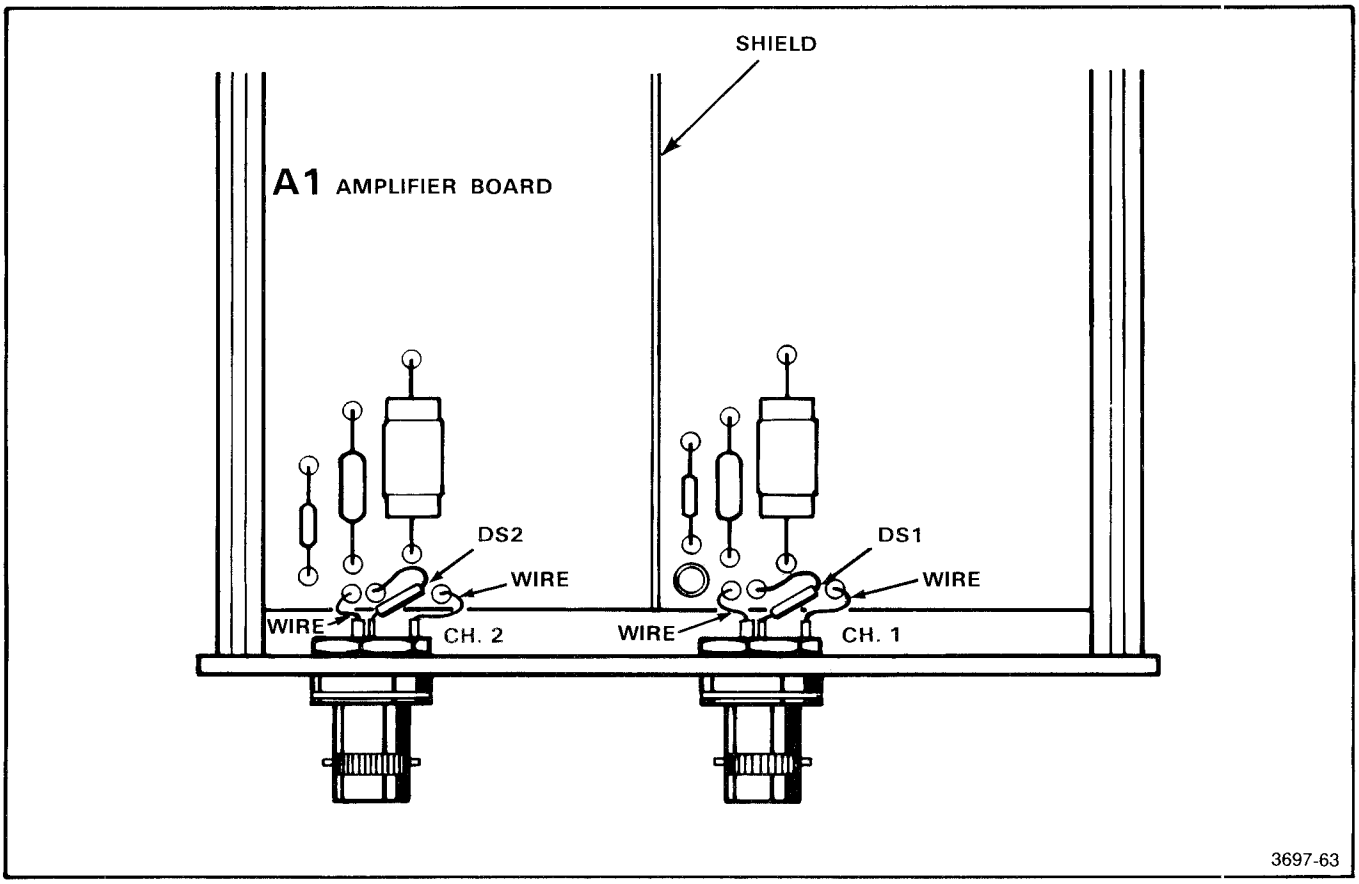


Figure 4-15. Board to bnc connections (A1)

a. Remove both Volts/Div knobs (1/16 HEX key, 2 each)

b. Remove shield covering the front portion of the A3 board (4 screws).

c. Remove 4 support posts (3/16 nut driver) and 4 screws.

CAUTION

Do not drag cam switch contacts across alignment pegs. Damage or misalignment of the contact wipers could result.

d. Lift the rear of each actuator to clear the alignment peg holes then slide back until the shaft clears the front panel.

6. Remove 2 shield securing screws. Lift out the plastic shield.

7. Remove 2 board securing screws located at the rear of the board then slide the A3-Output board from the frame.

8. Install a cam switch contact protector if available, otherwise place the board on a tray or other flat, uncluttered surface to avoid damage.

NOTE

If the A3 Output board is to be replaced with a new board, save the front-panel pushbutton knobs, cam-switches and shields. These components will be needed for the new board. If new components are desired, part numbers may be found in the Replaceable Electrical Parts list and the Replaceable Mechanical Parts list in this manual.

Install the A3-Output board as follows:

1. Slide the board into the frame.

2. Install the 2 securing screws at the rear of the board.

3. Position the shield and secure with 2 shield securing screws.

4. Install 2 cam actuator drums. Refer to Figure 4-18 to identify CH 1 and CH 2 drums.

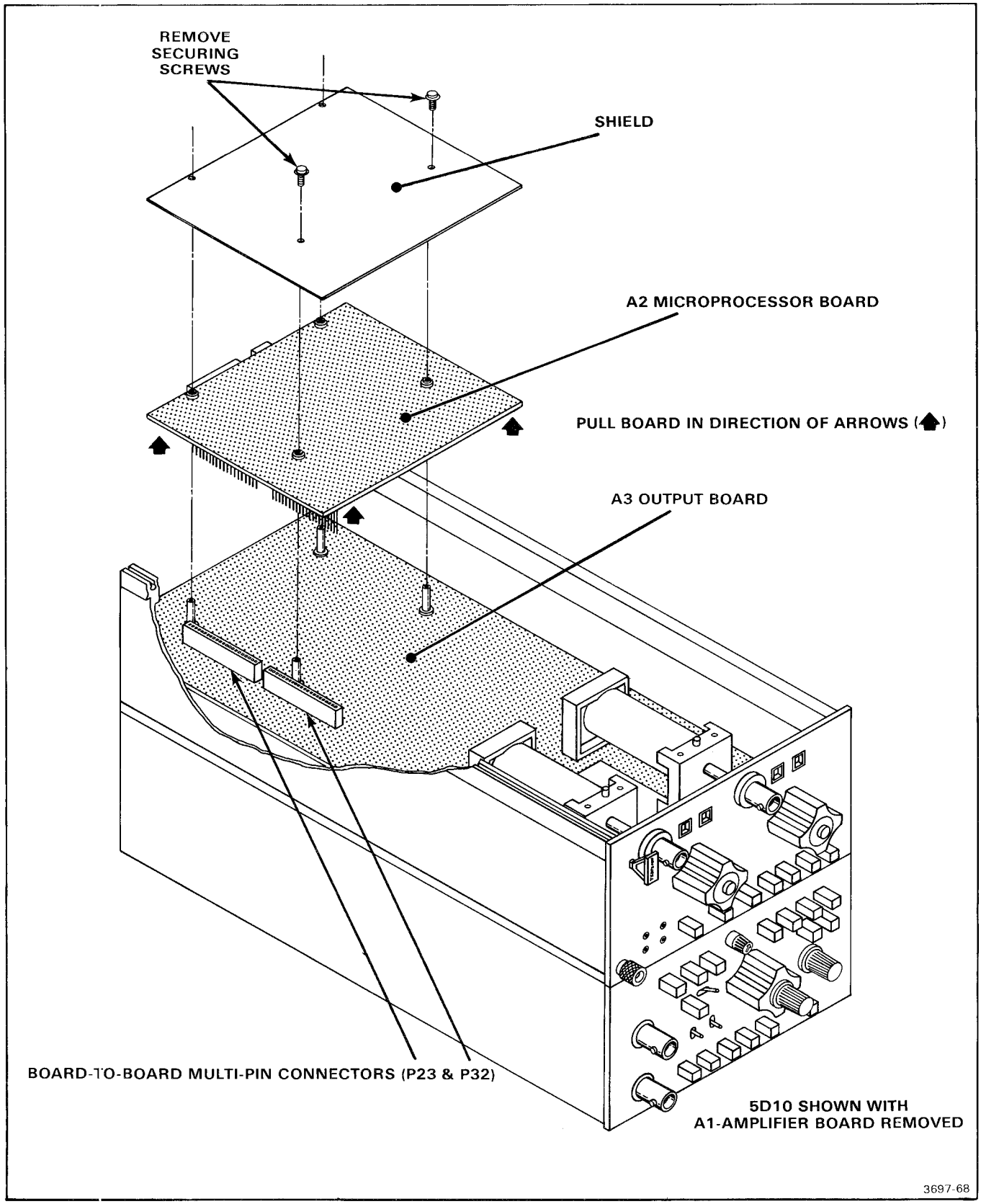


Figure 4-16. A2 board replacement.

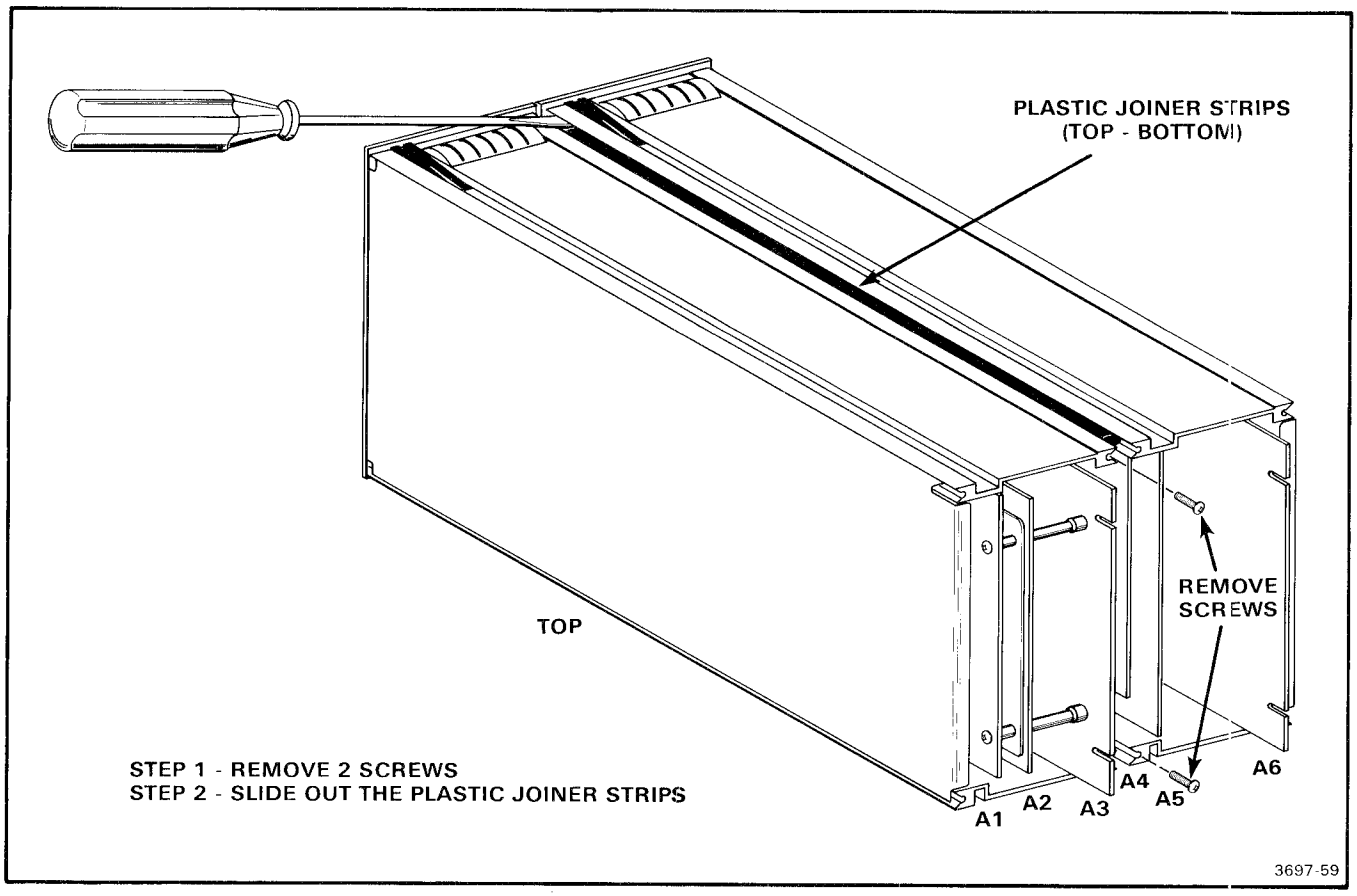


Figure 4-17. Separating the frame sections.

NOTE

The long alignment pegs on the cam drum bearings must engage the A3 board.

5. Rotate the instrument half while supporting the actuators. Install 4 support posts and 4 screws. Refer to Figure 4-19 for location of screws and support posts. Do one switch at a time.

6. Install Volt/Div knobs. Check alignment with front-panel nomenclature; verify that each switch rotates correct number of positions.

7. Solder the 4 wires to the front-panel plotter output jacks.

8. Install shield and four screws.

9. Plug in 10 connectors (6 harmonica, 4 ribbon cable). Refer to Figure 4-19 for harmonica location.

10. Connect the plug-in halves. (Install joiner strips and retainer screws.)

NOTE

After the plug-in halves are joined together, check the ribbon-wire cables for tight connection. The ribbon cables may be viewed from the rear through the top ventilating holes.

11. Install A2-Microprocessor board.

12. Install A1-Amplifier board.

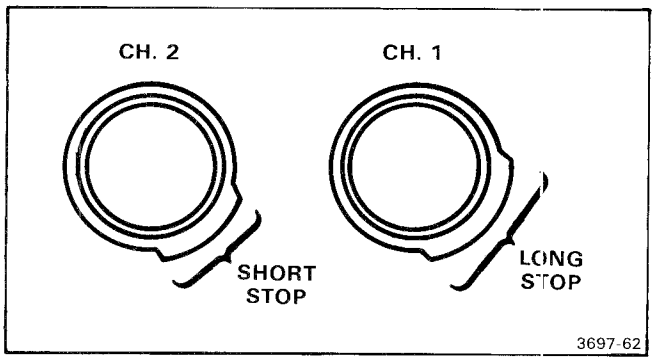


Figure 4-18. Identifying camswitch actuator drums for CH1 and CH2 VOLTS/DIV switches.

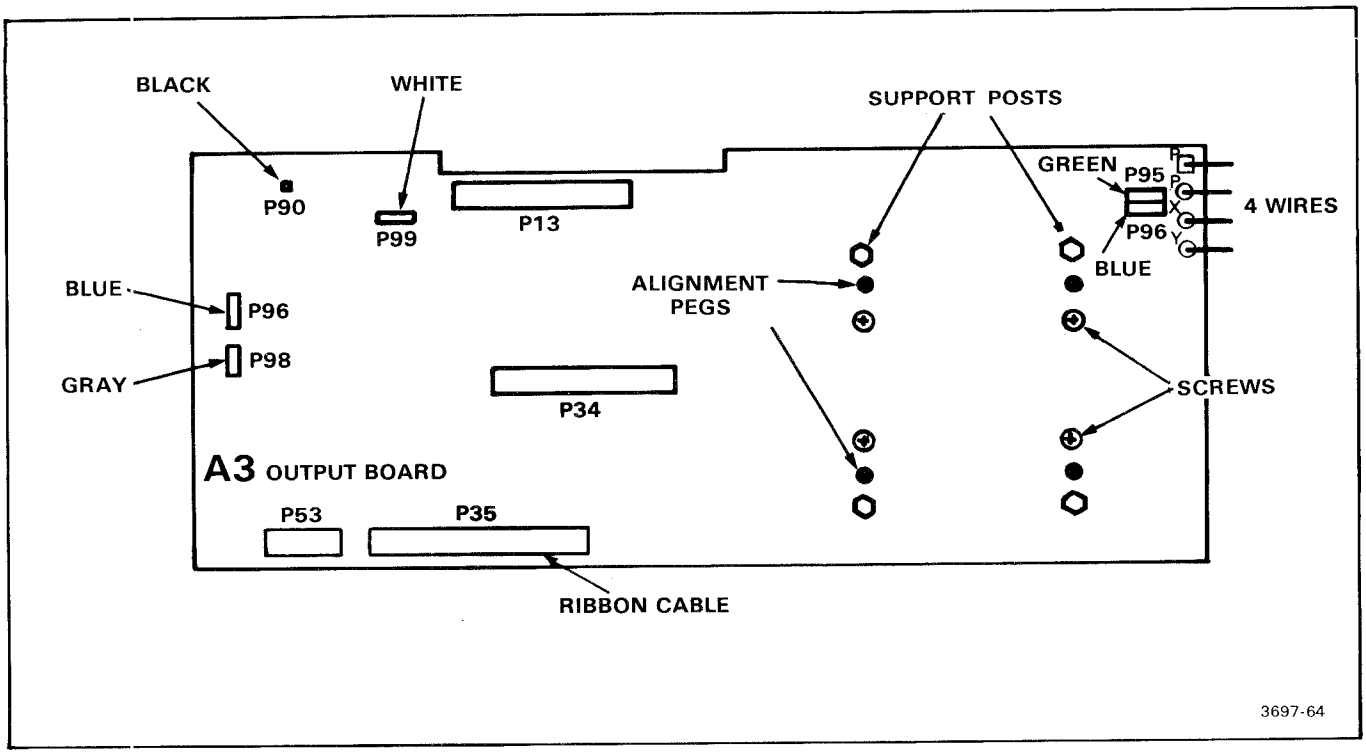


Figure 4-19. Location of alignment pegs and connectors on the A3 board.

A4-Data board replacement.

Refer to Figure 4-20 for location of parts mentioned in the following removal and installation procedure.

Remove the A4-Data board as follows:

1. Separate the 2 halves of the plug-in. Refer back to Figure 4-17.

2. Unplug the multi-pin ribbon cable.

NOTE

Observe the fold of this cable for later installation.

3. Remove 5 securing screws.

4. To lift the A4-Data board from the chassis, exert upward pressure (to disengage the multi-pin connector) at the two points shown in Figure 4-20.

Install the A4-Data board as follows:

1. Align the board-to-board multi-pin connector with its mating pins, then press firmly until the board is firmly seated against the spacer posts.

NOTE

The receptacle does not go all the way down to the A5 board.

2. Install the 5 screws, cable clamp with washer, and ribbon cable. Align the index on the cable plug housing with the index on the board. Observe the dress and fold (see Fig. 4-21).

3. Join the 2 plug-in halves. Refer back to Figure 4-17.

NOTE

After the plug-in halves are joined together, check the ribbon-wire cables for tight connection. The ribbon cables may be viewed from the rear through the top ventilating holes.

4. Install the side cover.

A5-Control board replacement.

Remove the A5-Control board as follows:

Refer to Figure 4-22 for location of parts mentioned in the following removal and installation procedures.

1. Remove the A4-Data board. Refer to the A4-Data board replacement procedure.

NOTE

Keep the board hardware separated for ease of assembly.

2. Unplug 3 multi-pin ribbon cables.

3. Unsolder the wire from board to front panel lug.

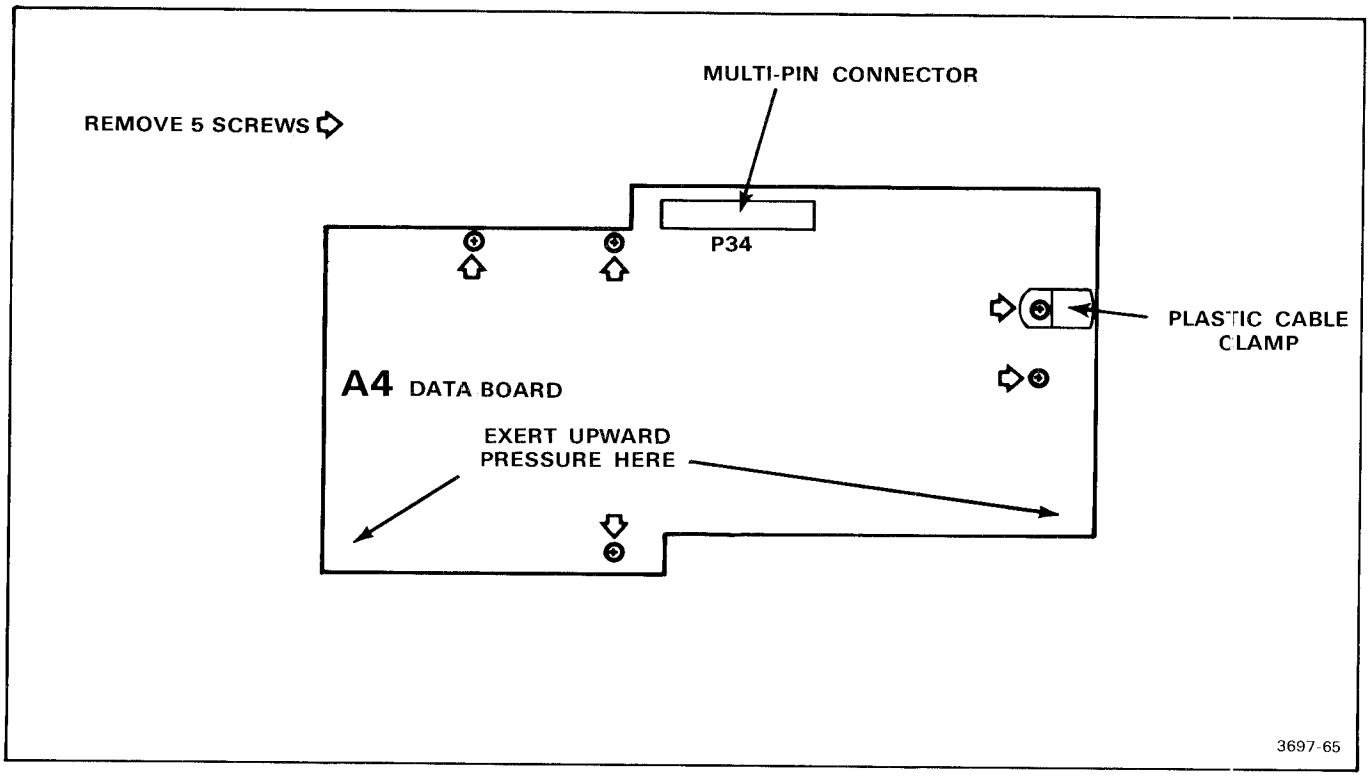


Figure 4-20. A4 board removal.

4. Remove the VIEWTIME knob (pull).

5. Remove 2 screws and 5 posts (3/16 Hex driver)

6. Lift the rear of the board to clear the cam switch alignment pegs. Slide the board to the rear until the pushbuttons clear the front panel then lift the board from the instrument.

NOTE

If the A5-Control board is to be replaced with a new one, retain the front-panel push switch knobs. They will be used on the new board.

Install the A5-Control board as follows:

1. Reverse the order of removal. Use care to align the pushbuttons and the POSSIBLE UNDERSAMPLING indicator in their respective holes in the front panel. See Figure 4-22 for location of securing hardware especially the cam switch securing screws.

Check correct alignment of the recessed pointer on the front of the VIEWTIME knob.

A6-Trigger board replacement.

Remove the A6 -Trigger board as follows:

Refer to Figure 4-23 for the location of parts mentioned in the following removal and installation procedures.

1. Remove the A4 and A5 boards.

2. Unsolder 3 wires at the bnc connectors (EXT TRIGGERING, EXTERNAL SEC/DIV).

NOTE

If a new A6 board is to be installed, save the support posts, screws and push-button knobs, remove the bulb and wires from the board and solder them into the new board(See Figure 4-23). Refer to Soldering Techniques earlier in this section. If new parts are desired, part numbers may be found in the Replaceable Electrical Parts list and Replaceable Mechnical Parts list in this manual.

3. Unplug the interconnecting cabling. Note the location of the 2 coax cables.

4. Loosen the setscrew at the coupler (.050 Hex key) then pull the CAL knob and shaft from the SECONDS/DIV switch. Do not remove the coupler from the pot shaft.

5. Remove the SECONDS/DIV knob (2 setscrews, 1/16 HEX key)

CAUTION

The cam switch contacts are located beneath the cam drum. Exercise care when removing the actuator drum.

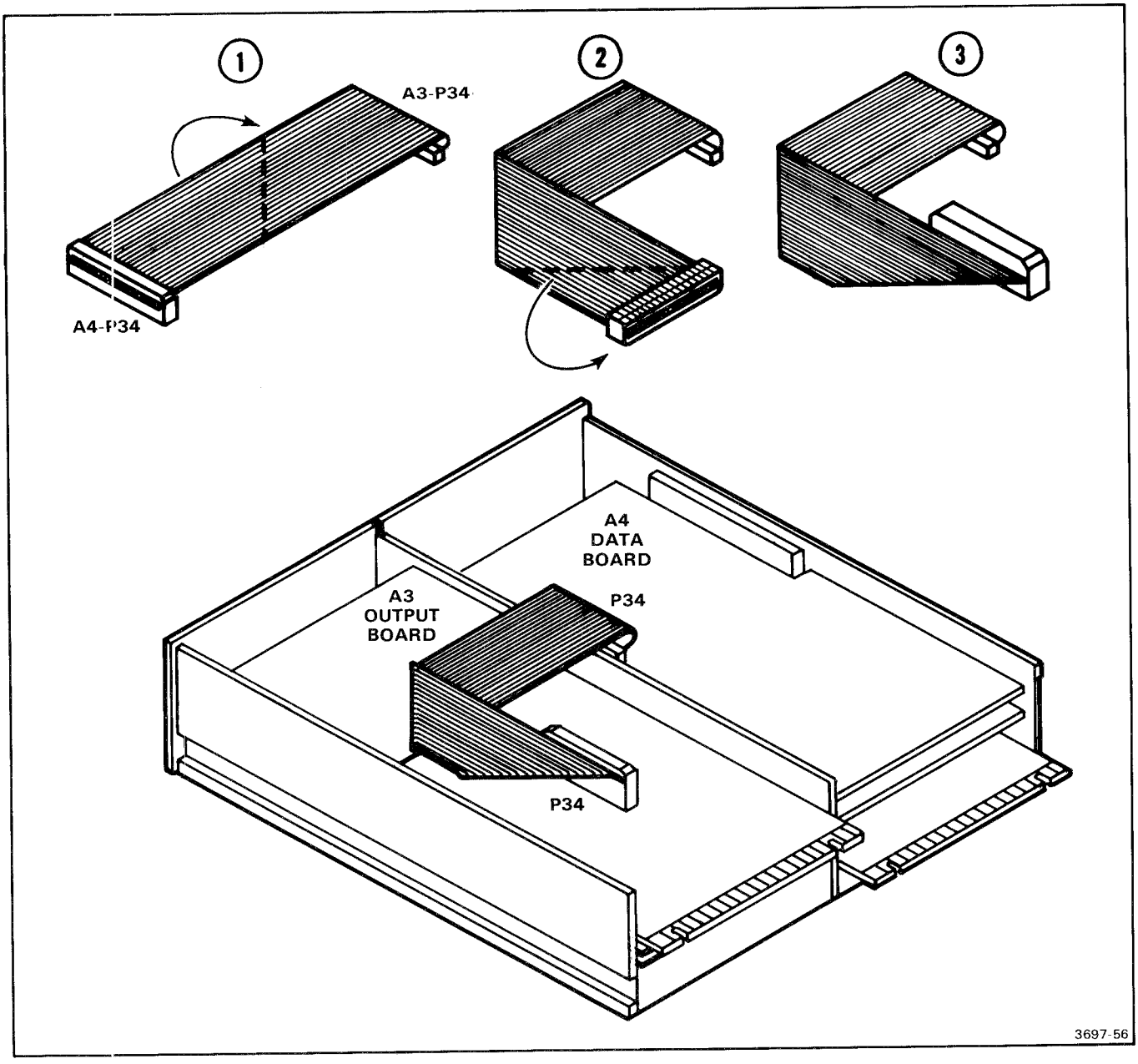


Figure 4-21. Cabling configuration and dress between A3 (P34) and A4 (P34).

6. Remove 4 cam switch securing screws, then remove the cam switch actuator. Install a cam-switch contact protector, if available.

7. Remove the board securing screws (4). Slide the board from the frame then place the board on a tray or other uncluttered flat surface to avoid damage to switch contacts.

Install the A6 -Trigger board as follows:

1. Reverse the order of removal (see Fig. 4-23).

Use care when installing the cam switch actuator drum. The individual switch wipers could be damaged.

NOTE

The long pegs on the connected bearings engage the A6 board.

INTERCONNECTING PINS

Two methods of interconnection are used in this instrument to electrically connect the circuit boards with other boards and components. When the interconnection

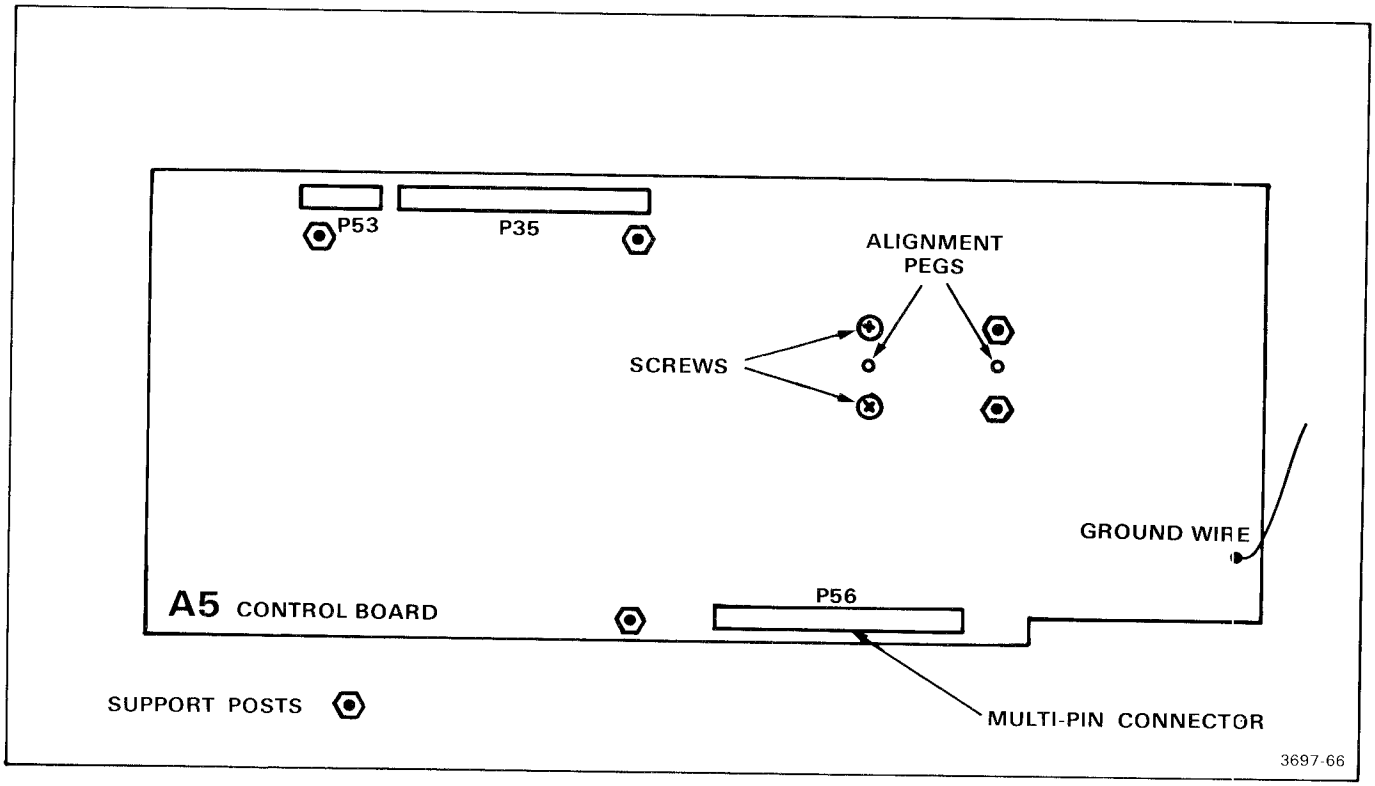


Figure 4-22. A5 board securing hardware.

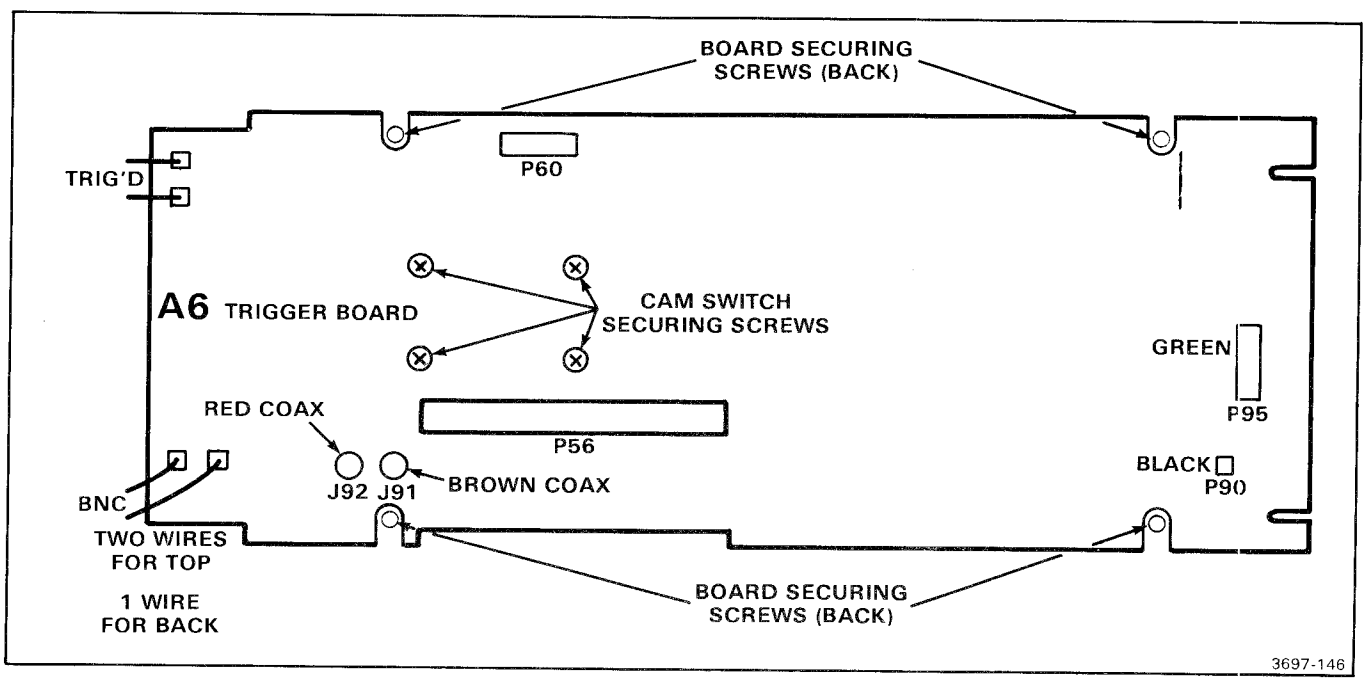


Figure 4-23. A6 board securing hardware and connector locations.

is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with a pin soldered into the board. Two types of mating connectors are used for these interconnecting pins. If the mating connector is mounted on a plug-on circuit board, a special socket is soldered into the board. If the mating connector is on the end of a lead, an end-lead pin connector is used which mates with the interconnecting pin. The following information provides the removal and replacement procedure for the various types of interconnecting methods.

Coaxial-Type End-Lead Connectors

Replacement of the coaxial-type end-lead connectors requires special tools and techniques; only experienced maintenance personnel should attempt to remove or replace these connectors. We recommend that the damaged cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see Section 9, Replaceable Mechanical Parts. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative. Figure 4-24 gives an exploded view of a coaxial end-lead connector assembly.

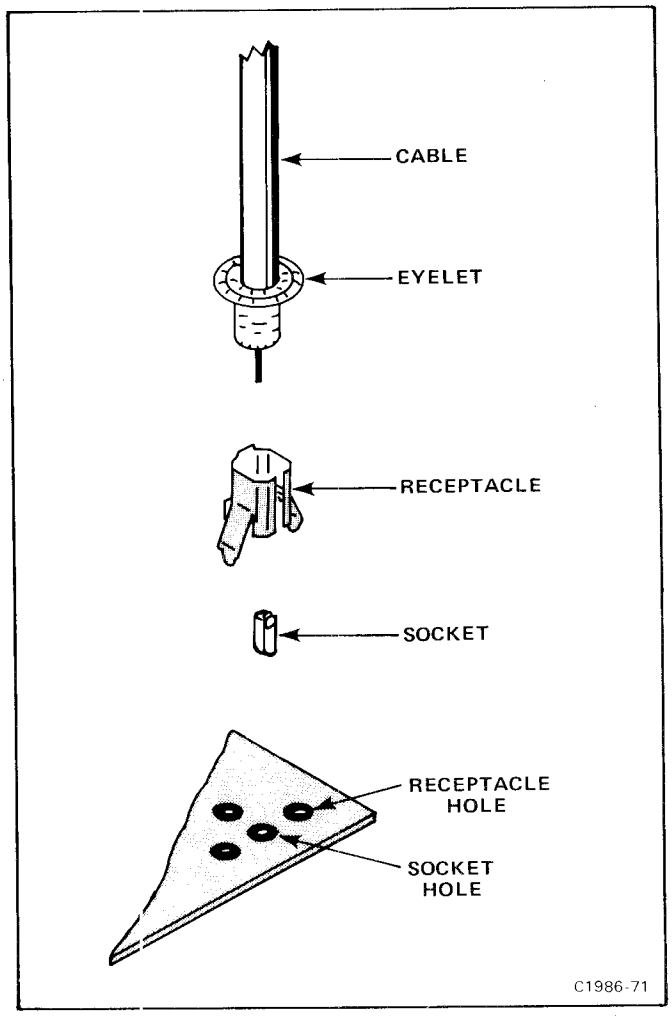


Figure 4-24. Coaxial-end lead connector assembly.

Circuit-Board Pins

A circuit board pin replacement kit (including necessary tools, instructions, and replacement pins with attached ferrules) is available from Tektronix, Inc. Order Tektronix Part. 040-0542-00.

NOTE

All circuit boards in the 5D10 are multi-layer boards. Replacing circuit-board pins on multi-layer boards is recommended only to service personnel experienced with the process. The process is explained in the following instructions. For further information, contact your Tektronix Service Center.

To replace a damaged pin, first disconnect any pin connectors. Then remove the solder from the connection using a vacuum, desoldering tool. See Soldering Techniques. Remove the damaged pin from the board with a pair of pliers, leaving the ferrule (see Fig. 4-25) in the circuit board if possible. If the ferrule remains in the circuit board, remove the spare ferrule from the replacement pin and press the new pin into the hole in the circuit board. If the ferrule is removed with the damaged pin, then press the replacement pin, with attached spare ferrule, into the circuit board. Position the replacement pin in the same manner as the original.

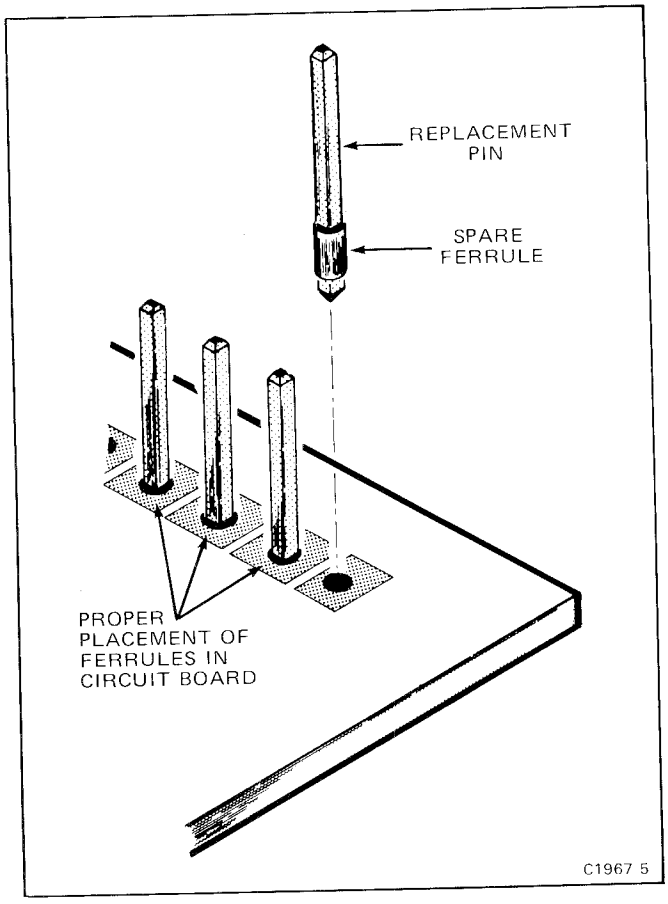


Figure 4-25. Exploded view of circuit-board pin and ferrule.

Solder the pin to the circuit board on each side of the board. If the original pin was bent at an angle to mate with a connector, carefully bend the new pin to the same angle. Replace the pin connector.

Circuit-Board Pin Sockets

The pin sockets on the circuit boards are soldered to the back of the board. To remove or replace one of these sockets, first unsolder the pin (see Soldering Techniques). Then straighten the tabs on the socket and remove the socket from the board. Place the new socket in the circuit board hole and press the tabs down against the board. Solder the tabs of the socket to the circuit board; be careful not to get solder inside the socket.

NOTE

The spring tension of the pin sockets ensures a good connection between the circuit board and the pin. This spring tension can be destroyed by using the pin sockets as a connecting point for spring-loaded probe tips, alligator clips, etc.

Multi-Pin Connectors

The pin connectors used to connect the wires to the interconnecting pins are clamped to the ends of the associated leads. To remove or replace damaged multi-pin connectors, remove the old pin connectors from the end of the lead and clamp the replacement connector to the lead.

NOTE

Some multi-pin connectors are equipped with a special locking mechanism. These connectors cannot be removed by pulling the the wire(s). To remove the connectors from the pin(s) grasp the plastic holder and pull.

To remove an individual wire from the holder insert a scribe in the hole on the side of the holder and slide the extended portion under the holder. This will allow the wire to be removed from the holder.

Some of the pin connectors are grouped together and mounted in a plastic holder; the overall result is that these connectors are removed and installed as a multi-pin connector (see Troubleshooting Aids). If the individual end-lead pin connectors are removed from the plastic holder, note the order of the individual wires for correct replacement in the holder.

Ribbon wire assemblies are not repairable. Replace the assembly if damaged. Refer to the Replaceable Mechanical Parts list at the rear of this manual.

ADJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustment of that particular circuit should be checked, as well as the adjustment of any closely related circuits. See Section 5 for a complete adjustment procedure.

SELECTABLE R626 TABLE

TO MOVE TRACE	TRY THIS RESISTOR	
up 2.7 divisions	321-0271-00	6.49 k
up 1.8 divisions	321-0272-00	6.65 k
up 1.0 divisions	321-0273-00	6.81 k
down 0.6 divisions	321-0275-00	7.15 k
down 1.3 divisions	321-0276-00	7.32 k
down 2.0 divisions	321-0277-00	7.50 k

EXAMPLE—How to use the Table above:

If your 5D10 trace jumps up 2 major divisions when you go into ADD mode, change A14626 from 6.98 k to 7.50 k. That should eliminate most of the trace shift.

NOTE

1. Before you switch the 5D10 into ADD mode, ground the CH 1 and CH 2 inputs; then, be sure that the CH 1 and CH 2 traces are centered on the CRT (use the POSition controls to center the traces).

2. Choose a resistor that gets the trace as close to the CRT centerline as possible. This will make sure that temperature changes don't move the trace outside of the EIS limits (<1.5 divisions trace shift when switching to ADD mode).

CALIBRATION

This section contains procedures for calibrating the 5D10 Waveform Digitizer. These procedures are designed to compare the performance of this instrument with measurement instruments of known accuracy to detect, correlate, or eliminate by adjustment, any variation from the electrical specifications. These procedures also verify that the controls function properly.

This section has two parts: Part I—Performance Check, for those who wish to verify that this instrument meets the applicable electrical specifications in section 1 without making internal adjustments. Part II—Adjustment and Performance Check is a complete calibration procedure that includes adjustments and performance checks in addition to verifying that the controls function properly. The procedures in Part I and Part II are written so that the entire instrument, or any major circuit or part of a circuit, can be checked or adjusted.

Table 5-1, Calibration Procedure Electives, lists the choices available and instructions for performing complete or partial calibration procedures. Also refer to Using These Procedures, for more detailed information.

TABLE 5-1
Calibration Procedure Electives

Electives	Procedures
Function Check	1. A functional check only is provided in the Checkout Procedure in section 2. 2. A functional check is also accomplished by performing Part II—Adjustment and Performance Check.
Performance Check Only	Perform Part I—Performance Check.
Complete Calibration	Perform Part II—Adjustment and Performance Check.
Partial Procedures	Proceed to the desired step(s) (e.g., A2, A3, B2, B3, etc.; as listed in the Index to Part I—Performance Check or Index to Part II—Adjustment and Performance Check). **NOTE** *When adjustments are made we recommend that the entire major function circuit procedure be performed (e.g., B. INPUT COMPENSATION AND ACQUISITION).*

USING THESE PROCEDURES

NOTE

In these procedures, capital letters within the body of the text identify front-panel controls, indicators and connectors on the 5D10 (e.g., TRIGGERING). Initial capitals identify all the associated test equipment controls, indicators, and connectors (e.g., Amplitude) used in the procedures. Initial capitals also identify internal adjustments of the 5D10 (e.g., 1-Gain).

These procedures are divided into subsections by major functional circuits (e.g., A. Display, B. Input Compensation and Acquisition, etc.). The order in which the subsections and procedures appear is the recommended sequence for a complete performance check or calibration of the instrument.

The first step in each subsection (A1, B1, C1, etc.) contains reference information and control settings that must be performed before proceeding.

The Setup Conditions provide equipment connection information and control settings for both this instrument and any associated test equipment. Also, the Setup Conditions are written so that if desired, each subsection (A, B, C, etc.) or step (A2, A3, B2, B3, etc.) can be performed independently.

The terms CHECK, EXAMINE, ADJUST, or INTERACTION when used as the first word of an instruction are defined as follows:

1. **CHECK**—indicates the instruction accomplishes an electrical specification check. Each electrical specification checked is listed in Table 5-2, Performance Check Summary (see the following Performance Check Summary discussion for more information).

2. **EXAMINE**—usually precedes an ADJUST instruction and indicates that the instruction determines whether adjustment is necessary. If no ADJUST instruction appears in the same step, the EXAMINE instruction concerns measurement limits that have no related adjustment. Measurement limits following the word EXAMINE are not to be interpreted as electrical specifications. They are provided as indicators of a properly functioning instrument and to aid in the adjustment process.

3. **ADJUST**—describes which adjustment to make and the desired result. We recommend that adjustments not be made if a previous CHECK or EXAMINE instruction indicates that no adjustment is necessary.

4. **INTERACTION**—indicates that the adjustment described in the preceding instruction interacts with other circuits. The nature of the interaction is described and reference is made to the step(s) affected.

PERFORMANCE CHECK SUMMARY

Table 5-2, Performance Check Summary, lists the electrical specifications that are checked in Part I and Part II of this section. Table 5-2 is intended to provide a convenient means for locating the procedures in Part I and Part II that check or adjust the instrument to meet the applicable electrical specifications. For example: if the Vertical System had been repaired, use Table 5-2 to locate the electrical specifications affected by the repair. Then note the title of the procedure in Part I or Part II in which those specifications are checked and/or adjusted. Use the index provided at the front of Part I and Part II to determine the page number of the desired procedures.

ADJUSTMENT INTERVAL

To maintain instrument accuracy, check performance **every 2000 hours of operation, or every 12 months if used infrequently. Before complete adjustment, thoroughly clean and inspect this instrument as outlined in the Maintenance section.**

TEKTRONIX FIELD SERVICE

Tektronix Field Service Centers and the Factory Service Center provide instrument repair and adjustment services. Contact your Tektronix Field Office or representative for further information.

TABLE 5-2
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL SYSTEM			
Deflection Factor			
Calibrated Steps	1 mV to 20 V per div; 14 steps in a 1-2-5 sequence.	B3. Check Amplifier Gain.	B5. Check/Adjust Amplifier Gain.
	Additional position of CH 2 VOLTS/DIV switch selects signal from Left Plug-In.	G2. Check Left Plug-In Accuracy and Triggering.	G2. Check Left Plug-In Accuracy and Triggering.
Variable Range (Uncal)	Continuously variable between steps.	B3. Check Amplifier Gain.	B5. Check/Adjust Amplifier Gain.

TABLE 5-2 (Cont)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL SYSTEM (Cont)			
Accuracy			
Input to Readout Numbers		B3. Check Amplifier Gain.	B5. Check/Adjust Amplifier Gain.
1 mV/Div & 2 mV/Div	±2%.		
5 mV/Div to 1 V/Div	±1%.		
2 V/Div to 20 V/Div	±2%.		
Input to CRT Graticule	±2%.		
From Left Vertical Plug-In	Add ±1% to above specifications.	G2. Check Left Plug-In Accuracy and Triggering.	G2. Check Left Plug-In Accuracy and Triggering.
Added	Add ±1% to above specifications.	B3. Check Amplifier Gain.	B5. Check/Adjust Amplifier Gain.
Readout Numbers to CRT	±2%.	A2. Check X and Y Centering and Gain.	A5. Check/Adjust X and Y Centering and Gain.
Bandwidth			
Single Channel	Suitable for dc to 100 kHz.	C2. Check Bandwidth, X-Y Phase Shift and CMR.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.
Dual Channel	Suitable for dc to 50 kHz.		
Input			
R and C	1 MΩ, within 0.5 %; 47 pF approximately.	B2. Check Input Compensation.	B4. Check/Adjust Input Compensation.
Voltage (Maximum)	250 V (dc + peak ac); 250 V ac p-p at 1 kHz or less.	Specification applicable under fault conditions; therefore, this is not a procedural check.	
AC Coupling (-3 dB Point)	10 Hz or less (1 Hz with 10X probe).	C2. Check Bandwidth, X-Y Phase Shift, and CMR.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.
Position Range	At least ±5 div.	B3. Check Amplifier Gain.	B5. Check/Adjust Amplifier Gain.
Common Mode Rejection (Add, CH 2 Invert)	At least 50:1, dc to 100 kHz.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.

TABLE 5-2 (Cont)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
VERTICAL SYSTEM (Cont)			
Channel Isolation			
Input Related	At least 80 dB, dc to 100 kHz.	D2. Check Display-Related and Input-Related Signal Isolation.	D2. Check Display-Related and Input-Related Signal Isolation.
Display Related	At least 40 dB, dc to 100 kHz (between Ch 1 and Ch 2).		
	At least 34 dB, dc to 100 kHz (between left plug-in channels acquired by Ch 2).		
Phase Shift	Less than 1.0 degree phase shift between Ch 1 and Ch 2, dc to 100 kHz.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.	C2. Check Bandwidth, X-Y Phase Shift, and CMR.
Resolution			
X-Y and Y-T	0.04 div (8-bit digitizer).	Customer verification normally not required. Satisfactory operation is substantiated by other tests in the procedures.	
HORIZONTAL SYSTEM			
Time Base			
Calibrated Rates	0.1 ms to 50 sec/div, 18 steps in a 1-2-5 sequence.	F2. Check Timing Accuracy.	F2. Check Timing Accuracy.
Uncalibrated	Continuously variable between steps.		
Accuracy	±1% (to readout numbers).		B2. Adjust Acquisition Timing. F2. Check/Examine Timing Accuracy.
External Input	Allows external pulse generator to determine acquisition rate. Sampling occurs on negative-going edge of input pulse.	F3. Check External Sec/Div Input.	F3. Check External Sec/Div Input.
Voltage	TTL levels.		
Frequency (Max.)	1 MHz.		

TABLE 5-2 (Cont)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
HORIZONTAL SYSTEM (Cont)			
Resolution			
X-Y	0.04 div (8-bit digitizer).	Customer verification normally not required. Satisfactory operation is substantiated by other tests in the procedures.	
Y-T	0.01 div (1024 memory locations shared among all traces acquired).		
POSSIBLE UNDERSAMPLING Indicator	Indicator lights when fewer than eight sample pulses occur during interval between successive threshold crossings of triggering signal. Depends on Trigger SOURCE, LEVEL, and SLOPE control settings.	E3. Check Triggering Sensitivity and Ground-Reference Update.	E3. Check Triggering Sensitivity and Ground-Reference Update.
TRIGGERING SYSTEM			
Sources	Channel 1, Channel 2, Left Plug-in (via mainframe), Line, External.	Customer verification normally not required. Satisfactory operation is substantiated by other tests in the procedures.	
Coupling	Dc, ac.	G2. Check Left Plug-in Accuracy and Triggering.	G2. Check Left Plug-in Accuracy and Triggering.
Sensitivity			
+ or − Slope			
External	100 mV, dc to 50 kHz or pulsewidth greater then 5 μs. 250 mV, 50 kHz to 250 kHz or pulsewidth greater than 1 μs.	E3. Check Triggering Sensitivity and Ground-Reference Update.	E3. Check Triggering Sensitivity and Ground-Reference Update.
Ch 1, Ch 2 Left	0.4 div, dc to 50 kHz, or pulsewidth greater than 5 μs. 1.0 div, 50 kHz to 250 kHz, or pulsewidth greater than 1 μs.		

TABLE 5-2 (Cont)
Performance Check Summary

Characteristic	Performance Requirement	Part I Performance Check Procedure Title	Part II Adjustment and Performance Check Procedure Title
TRIGGERING SYSTEM (Cont)			
Sensitivity (Cont)			
Bi-Slope Trigger	Amplitude, frequency, and pulse-width specifications apply to absolute value of signal (rectified).	E2. Check Triggering Level Range.	E2. Check Triggering Level Range.
External Input			
R and C	1 MΩ, within 2%; 47 pF approximately.	Customer verification normally not required. Input resistance and capacitance can be determined with appropriate testing bridge if necessary.	
Voltage (Max)	250 V (dc + peak ac); 250 V p-p ac at 1 kHz or less.		
TRIGGERED Indicator	Indicator lights when triggering signal passes through threshold.	E2. Check Triggering Level Range.	E2. Check Triggering Level Range.
PLOTTER SYSTEM			
Penlift			
Logic	Isolated switch, SPST (floating); normally open or normally closed contacts, selectable by internal jumper.	H2. Check Plot Output. H3. Alternate Check Plot Output.	H2. Check Plot Output. H3. Alternate Check Plot Output.
Voltage (Max)	5 V, dc or rms.	Customer verification normally not required.	
Current (Max)	50 mA, dc or rms.		
Pen-up (blanking) Duration	180 ms, ±20%.	H2. Check Plot Output. H3. Alternate Check Plot Output.	H2. Check Plot Output. H3. Alternate Check Plot Output.
Display Output (X and Y)			
Amplitude	0.2 V/div, within 5%.		
Speed	Accomodates Recorders with slew rate of at least 20 inches/second.	Proper operation verified when used with the recommended XY recorder.	

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 5-3 is required for a complete Adjustment and Performance Check of the instrument. If only a Performance Check is to be performed, the items listed for Adjustment are not required and are indicated by footnote 2. The remaining test equipment is common to both procedures.

The specifications for test equipment given in Table 5-3 are the minimum required to meet the performance requirements. Detailed operating instructions for test equipment are omitted in these procedures. Refer to the test equipment instruction manual if more information is needed.

SPECIAL FIXTURES

Special fixtures are used only where they facilitate instrument adjustment. These fixtures are available from Tektronix, Inc. Order by part number from Tektronix Field Offices or representatives.

TEST EQUIPMENT ALTERNATIVES

All of the listed test equipment is required to completely calibrate this instrument. However, complete checking or adjusting may not always be necessary or desirable. You may be satisfied with checking only selected characteristics, thereby reducing the amount of test equipment actually required.

The calibration procedures in Part I and Part II are based on the first item of equipment given as an example. When other equipment is substituted, control settings or setups may need to be altered. If the exact item of equipment given as an example in Table 5-3 is not available, first check the Minimum Specifications column carefully to see if any other equipment might suffice. Then check the Purpose column to see why this item is used. If used for a Performance Check or Adjustment that is of little or no importance for your measurement requirements, the item and corresponding step(s) can be deleted.

TABLE 5-3
Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
1. Oscilloscope Mainframe	Bandwidth, dc to 2 MHz.	Works with 5D10.	a. TEKTRONIX 5110 Oscilloscope. b. TEKTRONIX 5116 Oscilloscope. c. Any Tektronix 5100-series oscilloscopes.
2. Dual-Trace Amplifier (2 required)	Bandwidth, 1 MHz; sensitivity, 0.2 V per division.	Permits input to mainframe left vertical system.	a. TEKTRONIX 5A18N Dual Trace Amplifier.[1] b. TEKTRONIX 5A26 Dual Differential Amplifier.[1]
3. Frequency Counter[2]	Frequency, 1 Mhz; accuracy, 0.01%.	Set acquisition timing.	a. TEKTRONIX DC 504 Counter/Timer (operates in TM 500-series Power Module). b. TEKTRONIX DC 509 Universal Counter/Timer (operates in TM 500-series Power Module.
4. Calibration Generator	Square-wave output; frequency, 10 Hz to 250 kHz; output voltage, 5 V into 1 MΩ.	Set input compensation. Check left plug-in accuracy and triggering.	a. TEKTRONIX PG 506 Calibration Generator (operates in TM 500-series Power Module).
5. Low-Frequency Oscillator	Sine-wave output; frequency, 10 Hz, 1 kHz, 100 kHz, 250 kHz; accuracy within 10%; output voltage 5 V rms into 1 MΩ.	Check bandwidth, X-Y phase shift, CMR, channel isolation, triggering level and sensitivity, external Second/Division input, left plug-in accuracy and triggering.	a. TEKTRONIX SG 502 Oscillator (operates in TM 500-series Power Module). b. TEKTRONIX FG 503 Function Generator (operates in TM 500 series Power Module).

TABLE 5-3 (Cont)
Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
6. Time-Mark Generator	Markers, 0.1, 0.5, and 5 mS; amplitude, 1 V into 50 Ω; trigger output signal, 0.1 mS.	Check time-base accuracy.	a. TEKTRONIX TG 501 Time Mark Generator (operates in TM 500-series Power Module).
7. Power Module Mainframe (TM 500-series)	Capable of housing and powering two TM 500-series test instruments.	Provide housing and power for TM 500-series test instruments	a. TEKTRONIX TM 503. b. TEKTRONIX TM 504. c. TEKTRONIX TM 506.
8. Normalizer	Resistance, 1 MΩ capacitance, 47 picofarads; connectors, bnc.	See input compensation.	a. Tektronix 067-0541-00 Calibration Fixture.
9. Attenuator	Attenuation factor, 0.75 (1.33X); connectors, bnc.	Check amplifier gain.	a. Tektronix 067-1067-00 Calibration Fixture.
10. Coaxial Cables (2 required)	Impedance, 50 Ω; length, 42 inches; connectors, bnc male.	Provide signal interconnection.	a. Tektronix Part 012-0057-01.
11. Terminator	Impedance, 50 Ω; connectors, bnc; power, 2-W maximum.	Terminate output of calibration generator.	a. Tektronix Part 011-0049-01.
12. Alignment Tool[2]	Nonconductive shaft and screwdriver tip.	Adjust internal variable resistors and capacitors.	a. Tektronix Part 003-0675-00.
13. Dual-Input Coupler	Impedance, 50 Ω; connectors, bnc; male 2, female 1; the two lengths of RG58 cable are matched to less than 0.1 inch.	Inserting identical signals into both vertical channels simultaneously, for checking CMR.	a. Tektronix Part 067-525-02.
14. Probe[2]	Attenuation, 1X voltage probe; connector, bnc.	Used with Item 3 to adjust acquisition timing.	a. Tektronix P6062B 1X, 10X Probe. b. Tektronix P6101 1X Probe.
15. X-Y Recorder	Input voltage (X and Y), 100 to 500 mV/inch; input resistance operation. (X and Y), 1 MΩ; slewing speed, 50 cm/sec (20 inches/sec) minimum; penlift, remotely controllable by either normally open or normally closed contacts, 5 V maximum (supplied by Recorder).	Used to check for proper Plotter System Operation.	a. Hewlett-Packard Models 7045A, and 7045B X-Y Recorders.

TABLE 5-3 (Cont)
Test Equipment

Description	Minimum Specifications	Purpose	Examples of Applicable Test Equipment
16. Ramp Generator	Output amplitude 2V; ramp duration, 10 μs; polarity, positive; externally triggered.	Used to check external seconds/div, (step F3).	a. TEKTRONIX RG 501 Ramp Generator.
17. Test Storage Oscilloscope	XY mode capabilities and have Z-axis input, +5 volts turns beam on from totally off display.	Used to check plot output when XY recorder is not available (step H3).	a. TEKTRONIX 5111A Storage Oscilloscope. b. TEKTRONIX 5441 Storage Oscilloscope.
18. Cable	Connectors, tip-plugs on one end, and male bnc on other end.	Used to check plot output when XY recorder is not available (step H3).	a. Tektronix Part 175-1178-00, 20-inch (four required).
19. Power Supply	Output voltage, +5 volts; output current, 100 mA.	Used to check plot output when XY recorder is not available (step H3).	a. TEKTRONIX PS 501-2 Power Supply. b. TEKTRONIX PS 501-1 Power Supply. c. TEKTRONIX PS 503A Dual Power Supply.
20. Adapter	Connectors, Dual banana to bnc female.	Used to check plot output when XY recorder is not available. (step H3).	a. Tektronix Part 103-0090-00.

[1] Refer to Plug-In Compatibility Table in Section 1, General Information.
[2] Used for calibration only; NOT used for performance check.

PART I—PERFORMANCE CHECK

The following procedure (Part I—Performance Check) verifies electrical specifications without making internal adjustments. All tolerances given are as specified in the Specification tables (Section 1, General Information, or Table 5-2 Performance Check Summary) in this manual.

Part II—Adjustment and Performance Check provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

A separate Checkout Procedure is provided in Section 2, Operating Instructions to provide instrument familiarization and to verify that the controls function properly.

See Table 5-2, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part I—Performance Check procedure.

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PERFORMANCE CHECK INITIAL SETUP AND POWER-UP SEQUENCE

NOTE

The performance of this instrument can be checked at any ambient temperature from 0° to +45°C unless otherwise stated. Adjustments must be performed at an ambient temperature between +20° to 30°C for specified accuracies.

1. Install the 5D10 in the right vertical and horizontal plug-in compartments of the oscilloscope mainframe.

2. Connect the oscilloscope mainframe to a power source.

3. Press the 5D10 SAVE button in, and switch the oscilloscope mainframe power on.

4. Set the Oscilloscope Intensity and Focus controls for a comfortable viewing level.

5. Set the front-panel HORIZ CTRG and VERT CTRG screwdriver adjustments to center the graticule display on the screen.

6. Observe a graticule pattern display on the screen with the readout "5D10 READY" displayed at the top of the screen.

NOTE

If the graticule pattern does not appear, or the readout displays "5D10 ERROR", refer to the troubleshooting information in Section 4, Maintenance.

7. Switch on the appropriate test equipment and allow 20 minutes warmup before proceeding.

CAUTION

To prevent instrument damage, switch oscilloscope mainframe off before installing or removing plug-in units.

A. DISPLAY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe

Shaded lines identify Performance Requirement CHECK.

A1. DISPLAY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

A2. CHECK X AND Y CENTERING AND GAIN

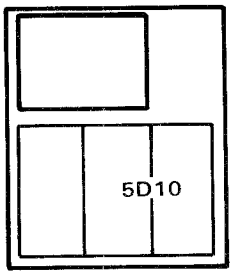
NOTE

First perform step A1, then proceed.

A2. SETUP CONDITIONS

5D10 Controls:
Make no changes in the control settings:

Oscilloscope Mainframe



Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... As Required
Focus ..... As Required

3697-122

a. **CHECK**—the 2nd and 10th displayed vertical lines correspond to the 2nd and 10th crt graticule lines; adjust the front-panel screwdriver HORIZ CTRG adjustment as necessary. All displayed vertical lines must correspond to their respective crt graticule lines within 0.1 division.

b. **CHECK**—the 2nd and 8th displayed horizontal lines correspond to the 2nd and 8th crt graticule lines; adjust the front-panel screwdriver VERT CTRG adjustment as necessary. All displayed horizontal lines must correspond to their respective crt graticule lines within 0.1 division.

c. Observe the displayed graticule is superimposed on the displayed graticule vectors.

d. Observe the corners of the large-square pattern centered on the screen. The intensified portions should be within 0.1 division of their corner dots.

B. INPUT COMPENSATION AND ACQUISITION

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
4. Calibration Generator
7. Power Module Mainframe
8. Normalizer
9. Attenuator
10. Coaxial Cable (42-inch)
11. Terminator (50Ω)

Shaded lines identify Performance Requirement CHECK.

B1. INPUT COMPENSATION AND ACQUISITION PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

c. Set the 5D10 controls as follows:

ACQUISITION AND DISPLAY
- CH 1 ..... On (pressed in)
- JOIN DOTS ..... On (pressed in)

TRIGGERING
- POSITION ..... POST TRIG
- SLOPE ..... / (pressed in)
- SOURCE ..... LINE

SECONDS/DIV .....).2 m

STORAGE
- VIEWTIME ..... MIN
- SAVE ..... Off (released)

All other pushbuttons ..... Off (released)

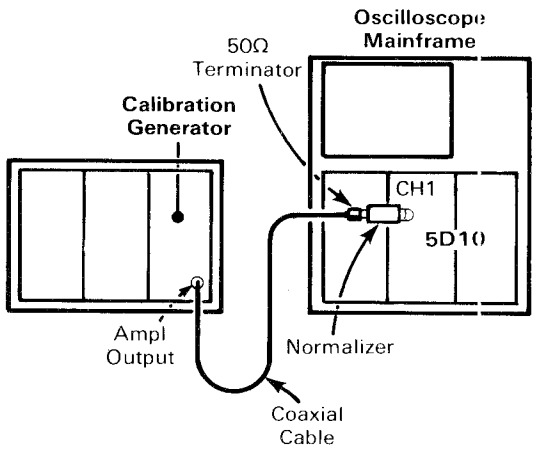
B2. CHECK INPUT COMPENSATION

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

5D10 Controls:
- VOLTS/DIV (CH 1 and CH 2) 0.5
- TRIGGERING
  - SOURCE ..... CH 1



Test Equipment Controls:
- Oscilloscope Mainframe
  - Intensity and Focus ..... Adjust as necessary
- Calibration Generator
  - Period ..... 1 ms
  - Var ..... Fully counterclockwise
  - Amplitude Selector ..... High Ampl

3697-120

a. Set the calibration generator Pulse Amplitude control to display 5 divisions of amplitude centered on the screen.

b. Set the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—that pulse aberration rolloff and overshoot is less than 0.1 division peak and less than 0.15 division peak-to-peak. Refer to Figure 5-1 for method of measurement.

d. Set the CH 1 VOLTS/DIV switch to 0.2.

e. Set the calibration generator Pulse Amplitude control to display 7 divisions of signal amplitude centered on the screen.

f. **CHECK**—that pulse aberrations rolloff and overshoot is less than 0.15 division peak and less than 0.2 division peak-to-peak.

g. Move the signal from the Channel 1 input to the Channel 2 input connector.

h. Set the ACQUISITION AND DISPLAY to CH 2.

i. Set the TRIGGERING SOURCE to CH 2.

j. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude centered on the screen.

k. Set the TRIGGERING LEVEL control for a stable display.

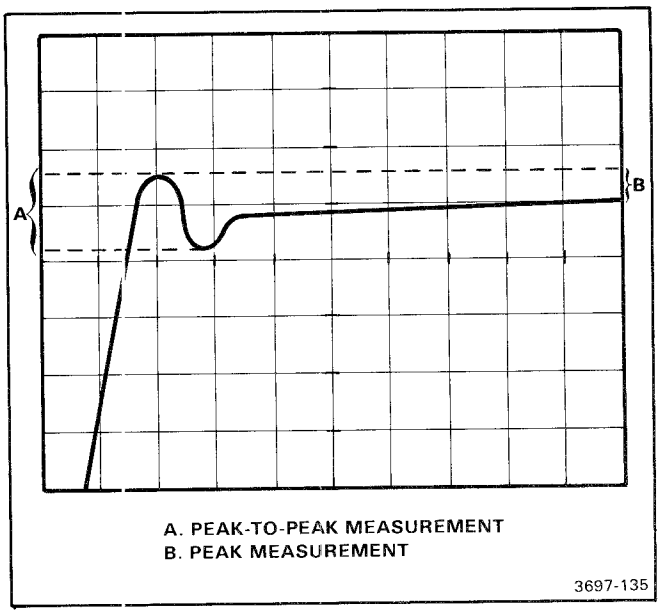


Figure 5-1. Measurement of waveform aberrations.

l. **CHECK**—that pulse aberration rolloff and overshoot is less than 0.1 division peak and less than 0.15 division peak-to-peak.

m. Set the CH 2 VOLTS/DIV switch to 0.2.

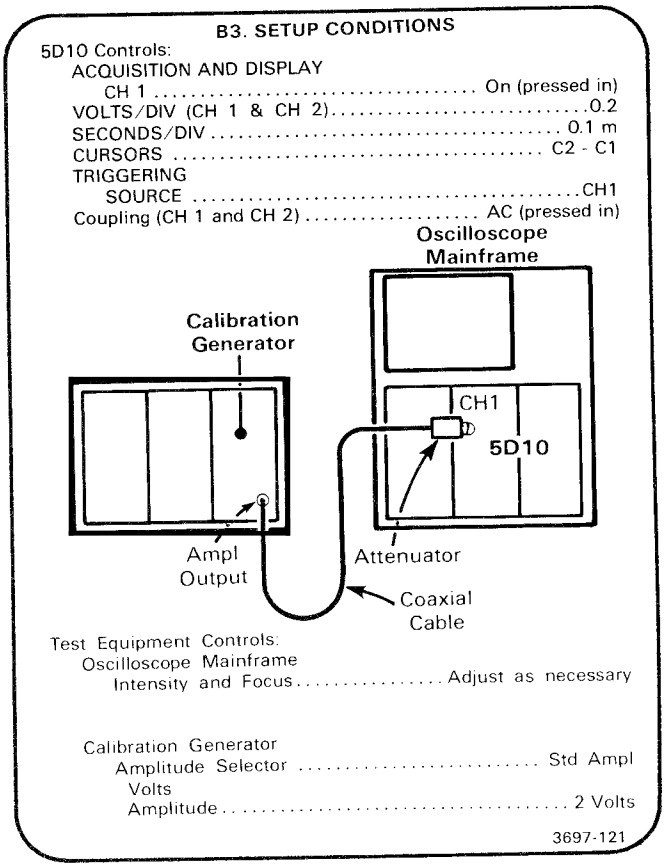
n. Set the calibration generator Pulse Amplitude control to display 7 divisions of signal amplitude centered on the screen.

o. **CHECK**—that pulse aberrations rolloff and overshoot is less than 0.15 division peak and less than 0.2 division peak-to-peak.

B3. CHECK AMPLIFIER GAIN

NOTE

If the preceding step was not performed, first perform step B1, then proceed.



a. Rotate the CH 1 POS control to center the waveform on the screen.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE button in.

d. Position CURSORS C1 and C2 to measure peak-to-peak voltage of the waveform (Cursor 1 on the top and Cursor 2 on the bottom of the waveform).

e. Release the SAVE button.

f. **CHECK**—the CH 1 ΔVoltage readout for a reading of 1.500 volts, within the limits of 1.485 to 1.515 volts. (Refer to Fig. 5-2, for location of readout display information.)

g. **CHECK**—that the displayed waveform amplitude is 7.5 divisions, within the limits of 7.35 to 7.65 divisions.

h. **CHECK**—the CH 1 vertical accuracy as shown in Table 5-4.

i. Rotate the CH 1 CAL control fully counterclockwise.

j. **CHECK**—the signal for 2 divisions or less amplitude.

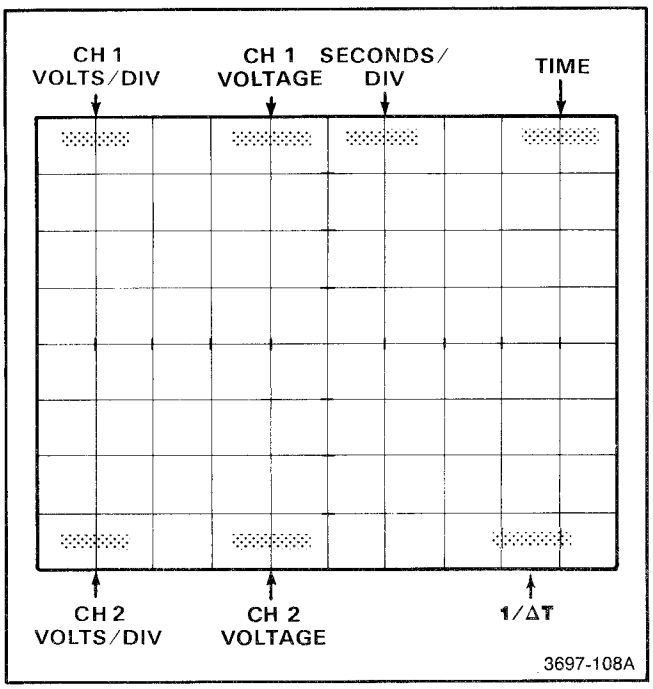


Figure 5-2. Location of readout information.

k. Set the CH 1 CAL control to display exactly 2 divisions of signal amplitude.

l. Set the CH 1 input coupling to AC (button in).

m. **CHECK**—rotate the CH 1 POS control throughout its range and check that the signal display moves completely off screen at each extreme setting of the CH 1 POS control.

n. Return the CH 1 CAL control to the calibrated position (in detent).

o. Disconnect the calibration generator signal from the CH 1 input and reconnect it (through the attenuator) to the CH 2 input connector.

p. Set the ACQUISITION AND DISPLAY to CH 2, and the TRIGGERING SOURCE to CH 2.

q. Set the CH 2 VOLTS/DIV switch to 0.2.

r. Set the calibration generator Amplitude control to 2 volts.

s. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

t. Rotate the CH 2 POS control to center the waveform on the screen.

u. **CHECK**—the CH 2 ΔVoltage readout for a reading of 1.500 volts, within the limits of 1.485 to 1.515 volts.

v. **CHECK**—that the displayed waveform amplitude is 7.5 divisions, within the limits of 7.35 to 7.65 divisions.

w. **CHECK**—the CH 2 vertical accuracy as shown in Table 5-4.

x. Rotate the CH 2 CAL control fully counterclockwise.

y. **CHECK**—the signal amplitude for 2 divisions or less.

z. Set the CH 2 CAL control to display exactly 2 divisions of signal amplitude.

aa. Set the CH 2 input coupling to AC (button in).

bb. **CHECK**—rotate the CH 2 POS control throughout its range and check that the signal display moves completely off screen at each extreme setting of the CH 2 POS control.

cc. Return the CH 2 CAL control to the calibrated position (in detent).

dd. Press the CH 1 GND button in.

ee. Set the ACQUISITION AND DISPLAY to ADD.

ff. **CHECK**—the signal amplitude is 5 divisions, within the limits of 4.85 to 5.15 divisions.

gg. Set the CH 1 VOLTS/DIV to 20.

hh. **CHECK**—the CH 1 △Voltage readout display reads 100.0 volts, within the limits of 98.0 to 102.0 volts.

ii. Set the CH 1 VOLTS/DIV control to 10.

jj. **CHECK**—the CH 1 △Voltage readout display reads 5.00 D, within the limits of 4.90 D to 5.10 D at all settings (except 20) of the CH 1 VOLTS/DIV control.

TABLE 5-4
CH 1 and CH 2 VOLTS/DIV Accuracy

Calibration Generator Amplitude	VOLTS/DIV Setting (CH 1 & CH 2)	Displayed Amplitude (Divisions)	△Voltage Readout (CH 1 & CH 2)
10 m	1 m	7.35 to 7.65	7.35 to 7.65 mV
20 m	2 m	7.35 to 7.65	14.70 to 15.30 mV
50 m	5 m	7.35 to 7.65	37.1 to 37.9 mV
0.1	10 m	7.35 to 7.65	74.3 to 75.8 mV
0.2	20 m	7.35 to 7.65	148.5 to 151.5 mV
0.5	50 m	7.35 to 7.65	371 to 379 mV
1	0.1	7.35 to 7.65	743 to 758 mV
2	0.2	7.35 to 7.65	1.485 to 1.515 V
5	0.5	7.35 to 7.65	3.71 to 3.79 V
10	1	7.35 to 7.65	7.43 to 7.58 V
Remove the 067-1067-00 Attenuator			
10	2	4.9 to 5.1	9.80 to 10.20 V
20	5	3.92 to 4.08	19.6 to 20.4 V
50	10	4.9 to 5.1	49.0 to 51.0 V
100	20	4.9 to 5.1	98.0 to 102.0 V

C. BANDWIDTH, X-Y PHASE SHIFT, AND CMR

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable (42-inch)
13. Dual-Input Coupler

Shaded lines identify Performance Requirement CHECK.

C1. BANDWIDTH, X-Y PHASE SHIFT, AND CMR PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

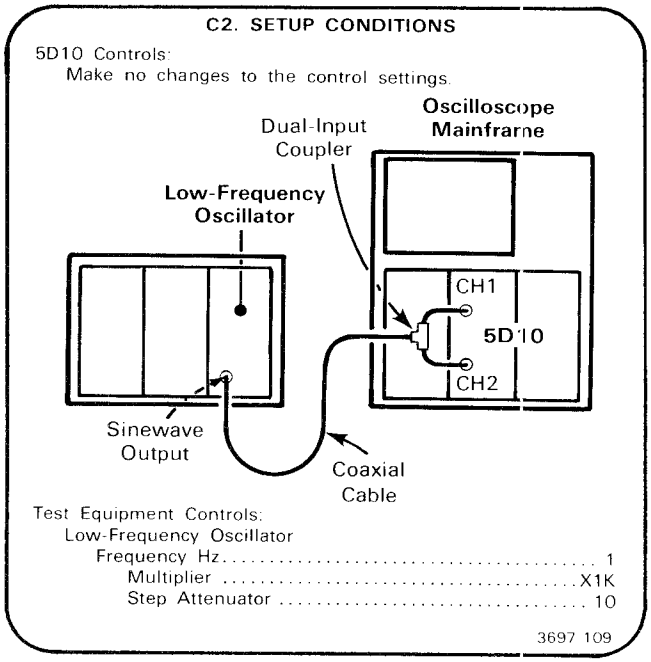
c. Set the 5D10 controls as follows:

ACQUISITION AND DISPLAY
CH 1 ..... On (pressed in)
VOLTS/DIV (CH 1 and CH 2) 0.2
TRIGGERING
POSITION ..... FREERUN
SLOPE ..... / (pressed in)
SOURCE ..... CH 1
CURSORS ..... OFF
SECONDS/DIV ..... 5 m
STORAGE
VIEWTIME ..... MIN
Coupling (CH 1 and CH 2) ..... AC (pressed in)
All other pushbuttons ..... Off (released)

C2. CHECK BANDWIDTH, X-Y PHASE SHIFT, AND CMR

NOTE

First perform step C1, then proceed.



a. Set the low-frequency oscillator Var Attenuator control to display exactly 6 divisions of signal amplitude at 1 kilohertz.

b. Set the low-frequency oscillator Multiplier to X10 (10 hertz).

c. **CHECK**—that the displayed signal amplitude is 4.2 divisions or more.

d. Set the ACQUISITION AND DISPLAY to CH 2.

e. **CHECK**—that the displayed signal amplitude is 4.2 divisions or more.

f. Set the CH 1 and CH 2 coupling pushbuttons to DC (released).

g. Set the low-frequency oscillator Multiplier to X100K (100 kHz).

h. Set the SECONDS/DIV switch to 0.1 m.

i. **CHECK**—that the displayed signal amplitude is at least 4.2 divisions peak-to-peak.

j. Set the ACQUISITION AND DISPLAY to X:CH 1 Y:CH 2.

k. **EXAMINE**—the CH 1 POS control should move the display horizontally and the CH 2 POS control should move the display vertically.

l. If necessary, readjust the low-frequency oscillator Var Attenuator control to display 6 divisions vertically.

m. **CHECK**—for 0.1 division or less of horizontal opening in the Lissajous pattern.

n. Press the CH 2 INVERT button in.

o. Set the CH 1 and CH 2 VOLTS/DIV switches to 0.1.

p. Set the ACQUISITION AND DISPLAY to ADD.

q. **CHECK**—that the signal display amplitude is 0.24 division or less (peak-to-peak).

D. CHANNEL ISOLATION

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
7. Power Module Mainframe
5. Low-Frequency Oscillator
10. Coaxial Cable

Shaded lines identify Performance Requirement CHECK.

D1. CHANNEL ISOLATION PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

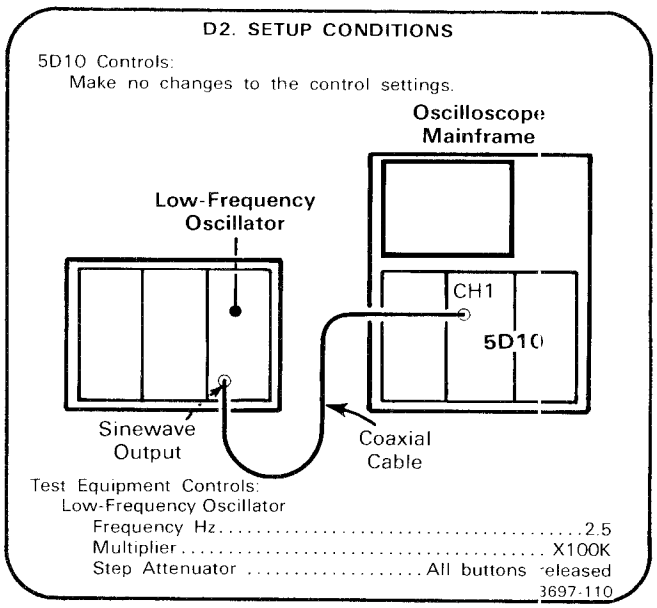
c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 2
VOLTS/DIV (CH 2) 20
ACQUISITION AND DISPLAY ..... CH 1
Coupling (CH 2) ..... GND (pressed in)
TRIGGERING
  POSITION ..... FREERUN
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1 (pressed in)
SECONDS/DIV ..... 0.1 m
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

D2. CHECK DISPLAY-RELATED AND INPUT-RELATED SIGNAL ISOLATION

NOTE

First perform step D1, then proceed.



a. Set the low-frequency oscillator Var Attenuator control to display a signal amplitude of 5 divisions at 250 kHz.

b. Set the CH 1 VOLTS/DIV switch to 0.5.

c. Set the ACQUISITION AND DISPLAY to CH 2.

d. **CHECK**—that the displayed signal amplitude is 0.2 division or less.

e. Release the CH 2 GND button.

f. Press the CH 1 GND button in.

g. Move the signal input from the CH 1 input to the CH 2 input connector.

h. Set the CH 2 VOLTS/DIV switch to 0.5.

i. Set the CH 1 VOLTS/DIV switch to 20.

j. Set the ACQUISITION AND DISPLAY to CH 1.

k. **CHECK**—that the displayed signal amplitude is 0.2 division or less.

l. Release the CH 1 GND button.

m. Set the CH 2 VOLTS/DIV switch to 20.

n. Press the CH 2 GND button in.

o. Set the CH 1 VOLTS/DIV switch to 1 m.

p. **CHECK**—that the displayed signal amplitude is 1 division or less.

q. Release the CH 2 GND button.

r. Press the CH 1 GND button in.

s. Set the CH 1 VOLTS/DIV switch to 20.

t. Set the CH 2 VOLTS/DIV switch to 1 m.

u. Move the signal input from the CH 2 input to the CH 1 input connector.

v. Set the ACQUISITION AND DISPLAY to CH 2.

w. **CHECK**—that the displayed signal amplitude is 1 division or less.

E. TRIGGERING LEVEL AND SENSITIVITY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable
13. Dual-Input Coupler

Shaded lines identify Performance Requirement CHECK.

E1. TRIGGERING LEVEL AND SENSITIVITY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1 and CH 2) 0.2
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
CURSORS ..... OFF
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

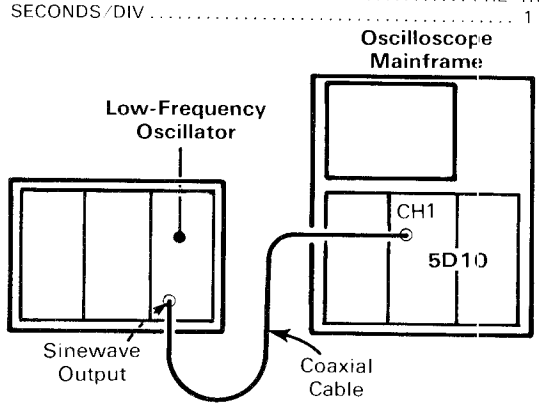
E2. CHECK TRIGGERING LEVEL RANGE

NOTE

First perform steps E1, then proceed.

E2. SETUP CONDITIONS

5D10 Controls:
  TRIGGERING
    COUPLING ..... DC (released)
    POSITION ..... PRE TRIG
  SECONDS/DIV ..... 1 m



Test Equipment Controls:
  Low-Frequency Oscillator
    Frequency Hz 1
    Multiplier X1K
    Step Attenuator ..... All buttons released

3697-111

a. Set the low-frequency oscillator Var Attenuator to display an 8 division 1 kHz signal on the screen.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—the green TRIG'D indicator light is on, and an intensified dot (triggering point) is displayed on the rising edge of the waveform approximately 1.25 divisions in from the right side of the screen.

d. Set the TRIGGERING SLOPE to \ (pushbutton in), and the POSITION to CTR TRIG.

e. **CHECK**—the green TRIG'D indicator light remains on, and the intensified dot (triggering point) is displayed on the falling edge of the waveform at the approximate horizontal center of the screen.

f. Set the TRIGGERING POSITION to POST TRIG, the SLOPE to BI-SLOPE (both buttons pressed in), and the TRIGGERING COUPLING to AC (button pressed in).

g. Rotate the TRIGGERING SENSITIVITY control to the MAX position.

h. **CHECK**—the green TRIG'D indicator light remains on, the intensified dot (triggering point) is displayed approximately 1.25 divisions in from the left side of the screen, and the intensified dot may occur on either the rising or falling edge of the waveform.

i. Set the TRIGGERING POSITION to FREE RUN.

j. **CHECK**—the green TRIG'D indicator light remains on and the signal display is free-running (not triggered).

k. Press the STORAGE SAVE button in.

l. **CHECK**—that the intensified dot (triggering point) is displayed at the end of the trace (right side of screen).

m. Release the STORAGE SAVE button.

n. Set the TRIGGERING POSITION to CTR TRIG.

o. Set the CH 1 VOLTS/DIV switch to 0.1.

p. Rotate the TRIGGERING LEVEL control fully clockwise.

q. **CHECK**—that the display is not triggered.

r. Set the TRIGGERING SLOPE to / (button in).

s. **CHECK**—rotate the TRIGGERING LEVEL control through it's range and check that the trace is not triggered at the fully clockwise and counterclockwise position of the TRIGGERING LEVEL control.

t. Set the TRIGGERING SLOPE to \ (button in).

u. **CHECK**—rotate the TRIGGERING LEVEL control through its range and check that the trace is not triggered at the fully clockwise and counterclockwise position of the TRIGGERING LEVEL control.

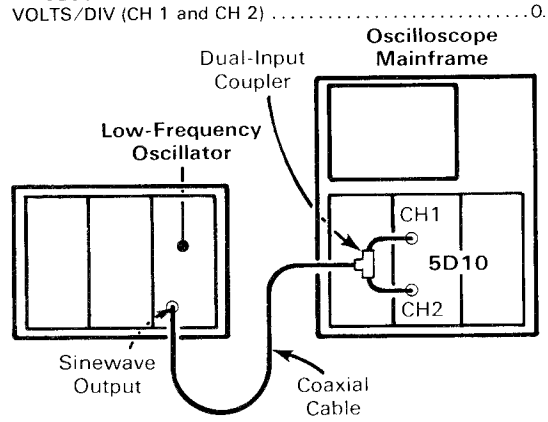
E3. CHECK TRIGGERING SENSITIVITY AND GROUND-REFERENCE UPDATE

NOTE

If the preceding step was not performed, first perform step E1, then proceed.

E3. SETUP CONDITIONS

5D10 Controls:
- TRIGGERING
  - POSITION ..... CTR TRIG
  - COUPLING ..... AC (pressed in)
  - SECONDS/DIV ..... 0.1 m
- VOLTS/DIV (CH 1 and CH 2) 0.1



Test Equipment Controls:
- Low-Frequency Oscillator
  - Frequency Hz 5
  - Multiplier X10K
  - Step Attenuator ..... 10 and 20 (pressed in)

3697-112

a. Set the low-frequency oscillator to display a signal amplitude of 0.4 division at 50 kHz.

b. Rotate the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE.

d. Set the ACQUISITION AND DISPLAY to CH 2.

e. Set the TRIGGERING SOURCE to CH 2.

f. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

g. Set the low-frequency oscillator to display a signal amplitude of 1 division at 250 kHz.

h. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

i. Set the ACQUISITION AND DISPLAY to CH 1.

j. Set the TRIGGERING SOURCE to CH 1.

k. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

l. Set both the CH 1 and CH 2 VOLTS/DIV switches to 50 m.

m. Move the CH 2 input signal to the TRIGGERING SOURCE EXT input connector (the other half of the dual-input coupler remains on the CH 1 input connector).

n. Set the TRIGGERING SOURCE to EXT.

o. Set the low-frequency oscillator to display a signal amplitude of 5 divisions at 2.5 kHz.

p. Set the low-frequency oscillator frequency to 250 kHz; do not disturb the low-frequency oscillator amplitude setting.

q. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

r. Set the low-frequency oscillator to display a signal amplitude of 2 divisions at 50 kHz.

s. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

t. Remove all cables.

u. Set the TRIGGERING SOURCE to LINE.

v. Set the SECONDS/DIV switch to 0.2.

w. **CHECK**—that the green TRIG'D light remains on as the TRIGGERING LEVEL control is rotated throughout its range.

x. **CHECK**—that the POSSIBLE UNDERSAMPLING indicator lights when the SECONDS/DIV CAL knob is rotated counterclockwise approximately 90 degrees.

y. Return the SECONDS/DIV CAL knob to its calibrated (detent) position.

z. Set the SECONDS/DIV switch to 1 m.

aa. Set the CURSORS switch to C1.

bb. **EXAMINE**—rotate the CH 1 POS control throughout its range. Note the CH 1 Voltage readout display reads the number of divisions the trace is above or below the vertical graticule center, and the readout suffix is always D.

cc. Position the trace to graticule center with the CH 1 POS control.

dd. Press the CH 1 GND button in, wait at least one update, then release the CH 1 GND button.

ee. **EXAMINE**—the CH 1 Voltage readout now displays 0 mV.

ff. **EXAMINE**—position the trace to the second graticule line from the top and check that the CH 1 Voltage readout reads approximately 150 mV. Press the CH 1 GND button in and note the readout display changes to 0 mV after the next update.

gg. Release the CH 1 GND button.

hh. Set the ACQUISITION AND DISPLAY to CH 2.

ii. Repeat parts bb through ee for the CH 2 Voltage readout display.

F. TIME-BASE ACCURACY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
6. Time-Mark Generator
7. Power Module Mainframe
10. Coaxial Cable (three required)
11. Terminator
16. Ramp Generator

Shaded lines identify Performance Requirement CHECK.

F1. TIME-BASE ACCURACY PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

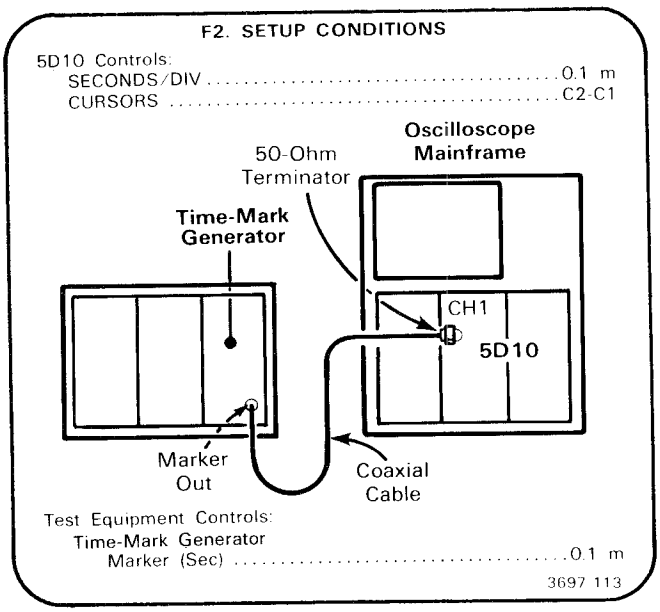
c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 0.5
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... POST TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
STORAGE
  VIEWTIME ..... INF
All other pushbuttons ..... Off (released)

F2. CHECK TIMING ACCURACY

NOTE

First perform step F1, then proceed.



a. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

b. Position CURSORS (C1 and C2) to the second and tenth time markers.

c. **CHECK**—that the ΔTime readout on the screen (refer to Fig. 5-2 in step B) reads between 792 and 808 μs and frequency readout (1/ΔT) equals between 1.26 and 1.24 kHz.

d. **CHECK**—the horizontal timing accuracy as shown in Table 5-5. Press and release the STORAGE VIEWTIME

control and, reposition the cursors to the top of the second and tenth time markers for each SECONDS/DIV and time-mark generator setting. Observe the display does not update until the STORAGE VIEWTIME control is pressed and released.

e. Set the SECONDS/DIV switch to 1 m and the STORAGE VIEWTIME control to MIN.

f. Set the time-mark generator Marker (Sec) switch to 5 m.

g. Rotate the SECONDS/DIV CAL knob fully counterclockwise.

h. **CHECK**—for 2 divisions or less between time markers.

i. Return the SECONDS/DIV CAL knob to the calibrated (detent) position.

j. Set the time-mark generator Marker (Sec) switch to 0.5 ms.

k. Press the STORAGE SAVE button in.

l. Position CURSORS (C1 and C2) to the top of two adjacent time markers.

m. **CHECK**—that when the SWP MGF (sweep magnification) is pressed in, the Seconds/Div readout display changes from 1 ms to 100 μs, and the displayed Time markers are 5 divisions apart.

n. Release the JOIN DOTS pushbutton.

o. **EXAMINE**—the time markers are displayed with dots.

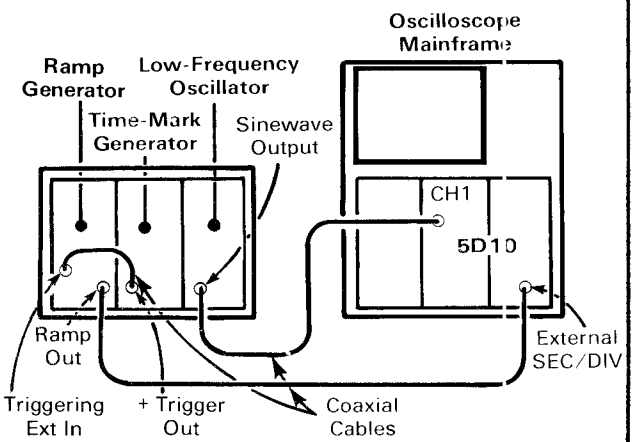
F3. CHECK EXTERNAL SEC/DIV INPUT

NOTE

If the preceding step was not performed, first perform step F1, then proceed.

F3. SETUP CONDITIONS

5D10 Controls:
- ACQUISITION AND DISPLAY
  - JOIN DOTS ..... On (pressed in)
- SECONDS/DIV ..... 10 m
- CURSORS ..... OFF
- STORAGE
  - VIEWTIME ..... MIN



Test Equipment Controls:
- Time-Mark Generator
  - Marker (Sec) ..... 0.1 m
- Low Frequency Oscillator
  - Frequency Hz 1
  - Multiplier X100
  - Step Attenuator 10
- Ramp Generator
  - Triggering ..... Ext
    - Level ..... Centered
  - Ramp Duration ..... 10 μs
    - Polarity ..... +
  - Ramp Amplitude ..... 2 V

3697-114

a. Set the low-frequency oscillator Var Attenuator to display an amplitude of 5 divisions at 100 hertz.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE REF in.

d. Set the SECONDS/DIV switch to EXT.

e. **CHECK**—that the reference waveform matches the acquired waveform within 0.2 division (measured 1 division in from the right graticule edge).

f. Press the STORAGE TRACE STEP button in.

g. **EXAMINE**—the reference waveform shifts downward approximately 0.8 division from the acquired waveform.

h. Release the STORAGE SAVE REF and TRACE SEP pushbuttons.

TABLE 5-5
Horizontal Timing Accuracy

SECONDS/DIV and Marker Switch Settings	Seconds/Div Readout	Δ Time Readout	SN B020100 & Up 1/ΔT Readout
0.1 m	100 μs	792 to 808 μs	1.26 to 1.24 kHz
0.2 m	200 μs	1.584 to 1.616 ms	631 to 619 Hz
0.5 m	500 μs	3.960 to 4.040 ms	253 to 248 Hz
1 m	1 ms	7.92 to 8.08 ms	126 to 124 Hz
2 m	2 ms	15.84 to 16.16 ms	63.1 to 61.9 Hz
5 m	5 ms	39.60 to 40.40 ms	25.3 to 24.8 Hz
10 m	10 ms	79.2 to 80.8 ms	12.6 to 12.4 Hz
20 m	20 ms	158.4 to 161.6 ms	6.31 to 6.19 Hz
50 m	50 ms	396.0 to 404.0 ms	2.53 to 2.48 Hz
0.1	100 ms	792 to 808 ms	1.26 to 1.24 Hz
0.2	200 ms	1.584 to 1.616 s	631 to 619 mHz
0.5	500 ms	3.960 to 4.040 s	253 to 248 mHz
1	1 s	7.92 to 8.08 s	126 to 124 mHz
2	2 s	15.84 to 16.16 s	63.1 to 61.9 mHz
5	5 s	39.60 to 40.40 s	25.3 to 24.8 mHz
10	10 s	Rotate the SECONDS/DIV switch to 10, 20, and 50, and note the readout display is 10, 20, and 50 s respectively. The 10, 20, and 50 second timing accuracy is verified as a function of the 0.1 m through 5 second accuracy checks.	
20	20 s		
50	50 s		

G. LEFT PLUG-IN FUNCTIONS

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
2. Dual-Trace Amplifier
4. Calibration Generator
5. Low-Frequency Oscillator
7. Power Module Mainframe
9. Attenuator
10. Coaxial Cable

Shaded lines identify Performance Requirement CHECK.

G1. LEFT PLUG-IN FUNCTIONS PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 2) 20
ACQUISITION AND DISPLAY
  CH 2 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... PRE TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... LEFT PLUG-IN
CURSORS C2-C1
SECONDS/DIV ..... 0.1 m
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

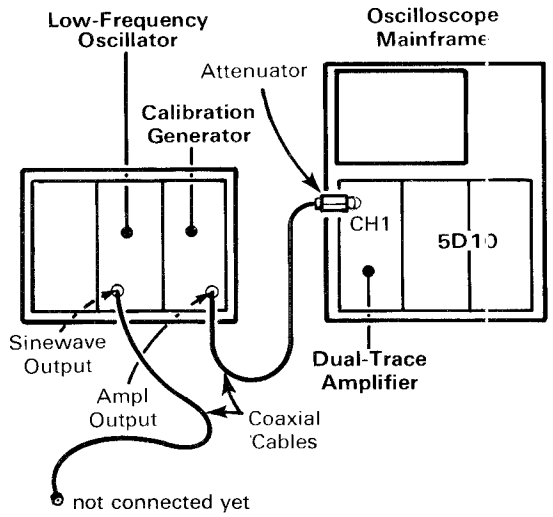
G2. CHECK LEFT PLUG-IN ACCURACY AND TRIGGERING

NOTE

First perform step G1, then proceed.

G2. SETUP CONDITIONS

5D10 Controls:
Make no changes to the control settings.



Test Equipment Controls:
Dual-Trace Amplifier
  Display ..... ON (pressed in)
  Mode CH1
  Trigger CH1
  Volts/Div (CH 1 and CH 2) 0.2
  All other pushbuttons ..... Out (released)

Low-Frequency Oscillator
Frequency Hz 5
  Multiplier X10K
  Step Attenuator 10

Calibration Generator
  Amplitude Selector ..... Std Ampl
  Amplitude ..... 2 Volts

3697-115

a. Center the waveform on the screen, using the CH 2 POS control; then set the CH 2 VOLTS/DIV switch to LEFT PLUG-IN. Center the waveform on the screen using the dual-trace amplifier Channel 1 Position control. Do not disturb the setting of the CH 2 POS control throughout the remainder of this step.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE button in.

d. Position cursor C1 to the top and cursor C2 to the bottom of the waveform to measure peak-to-peak amplitude.

e. **CHECK**—that the displayed signal amplitude is 7.5 divisions, within the limits of 7.275 to 7.725 divisions.

f. **CHECK**—that the CH 2 volts/division readout reads LEFT, and that the CH 2 ΔD (divisions) readout reads between 7.35 and 7.65.

g. Release the STORAGE SAVE pushbutton.

h. Set the dual-trace amplifier Mode to Dual Trace (both Ch 1 and Ch 2 buttons pressed in).

i. **CHECK**—that both Channel 1 and Channel 2 traces are displayed on the screen.

j. Disconnect CH 1 of the dual-trace amplifier from the calibration generator and connect it to the Sine-Wave Output of the low-frequency oscillator.

k. Set the dual-trace amplifier Mode to CH 1.

l. Set the low-frequency oscillator Var Attenuator control to display a signal amplitude of 0.4 division at 50 kHz.

m. **EXAMINE**—for a stable display with the SLOPE in both / and \ adjust the TRIGGERING LEVEL control as necessary.

n. Set the low-frequency oscillator to display a signal amplitude of 1 division at 250 kHz.

o. Repeat part m.

p. Set the low-frequency oscillator to display an amplitude of 2 divisions at 2.5 kHz.

q. Center the dual-trace amplifier Channel 1 Position Control.

r. Set the TRIGGERING SOURCE to CH 2.

s. Set the TRIGGERING COUPLING to AC.

t. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

u. Position the top of the sine-wave display to the top line of the crt graticule using the dual-trace amplifier Channel 1 Position control.

v. Set the TRIGGERING COUPLING to DC.

w. **CHECK**—that the signal display is no longer stable.

H. PLOT OUTPUT

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
2. Dual-Trace Amplifier
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable
15. X-Y Recorder
16. Ramp Generator
17. Test Storage Oscilloscope
18. Cable (4 required)
19. Power Supply
20. Adapter

Shaded lines identify Performance Requirement CHECK.

H1. PLOT OUTPUT PRELIMINARY SETUP

a. Perform the Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part I—Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any change which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 1
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... PRE TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
STORAGE
  VIEWTIME ..... MIN
CURSORS ..... OFF
All other pushbuttons ..... Off (released)

d. Proceed to step "H2. Check Plot Output" if the 5D10 plot circuitry is to be checked using an XY recorder. If an XY recorder is not available, skip step H2 and proceed to step "H3. Alternate Check Plot Output."

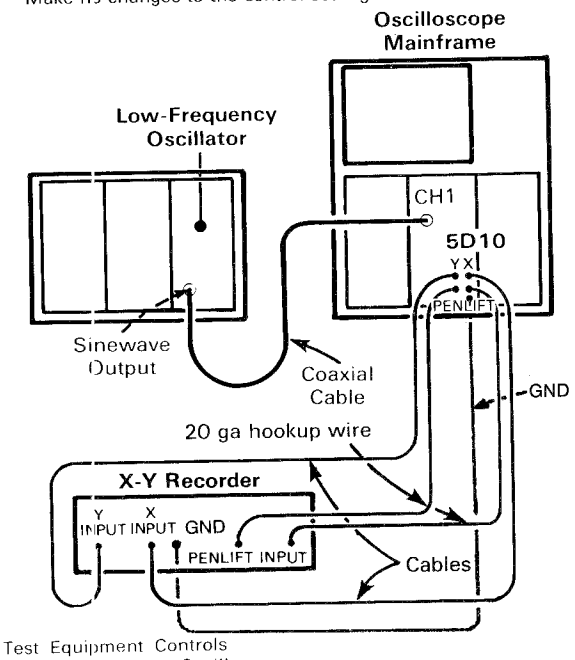
H2. CHECK PLOT OUTPUT

NOTE

First perform step H1, then proceed.

H2. SETUP CONDITIONS

5D10 Controls:
Before starting this procedure, remove the 5D10 from the oscilloscope mainframe and position the Penlift jumper for appropriate pen-lift logic for your X-Y recorder. Refer to the H2. Penlift Jumper Location illustration on the adjacent page.
Make no changes to the control settings.



Test Equipment Controls
Low-Frequency Oscillator
Frequency Hz 1
Multiplier X1K
Step Attenuator 10

X-Y Recorder
Range
X Volts/Inch 0.5
Y Volts/Inch 0.5

3697-119A

a. Set the low-frequency oscillator Var Attenuator to display a signal amplitude of 4 divisions at 1 kHz.

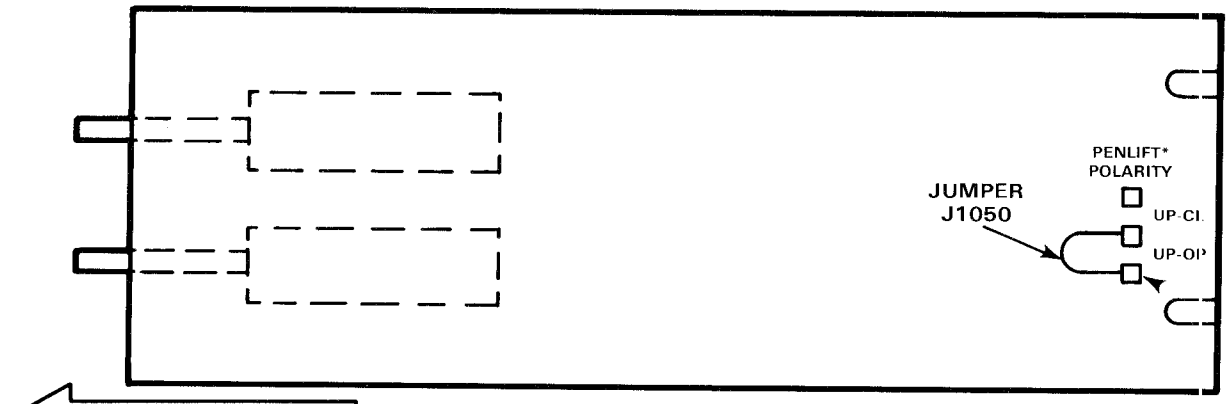
b. Set the X-Y recorder controls as recommended by the manufacturer (refer to the X-Y recorder manufacturer's instruction manual).

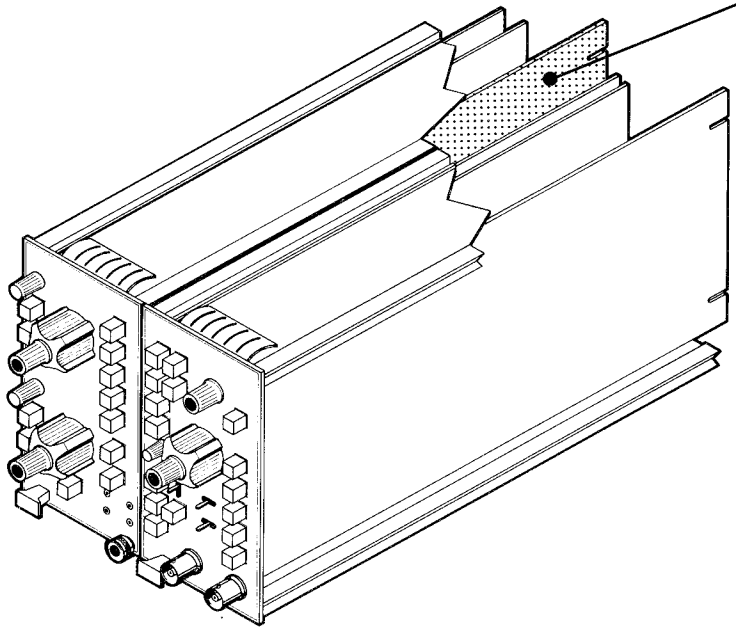
c. Press the STORAGE SAVE button in.

d. Press the SAVED DISPLAY PLOT button in. Notice the screen will blank until the first channel of the plot is completed then display the message "CHANGE PEN COLOR IF DESIRED/RELEASE THEN PUSH PLOT TO CONTINUE". When PLOT is released, the next message "PUSH PLOT TO CONTINUE" appears. Push PLOT button as instructed. (If, at this time, you wish not to continue, release PLOT button).

e. **CHECK**—that the X-Y recorder duplicates the display (including the graticule) and that the pen lift operates properly.

H2. PENLIFT JUMPER LOCATION





*UP-CL-The X-Y recorder pen will lift "UP" when the relay contacts close "CL".

UP-OP-The X-Y recorder pen will lift "UP" when the relay contacts open "OP".

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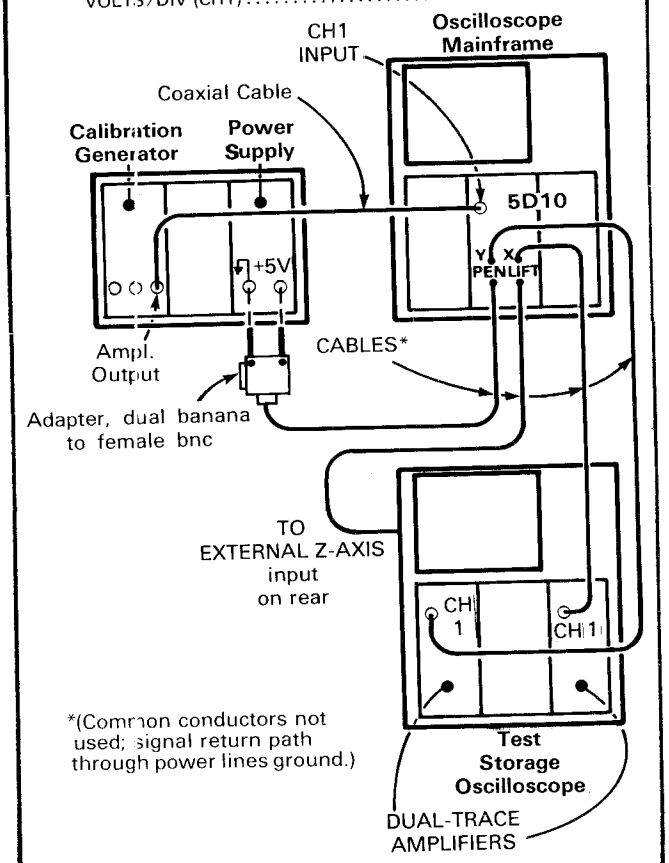
H3. ALTERNATE CHECK PLOT OUTPUT

NOTE

First perform step H1, then proceed.

H3. SETUP CONDITIONS

5D10 Controls:
Before starting this procedure, remove the 5D10 from the oscilloscope mainframe and connect the Penlift jumper (J1050) on the back of the A3 Output Board to the UP-OP position.
SECONDS/DIV ..... 0.2 m
VOLTS/DIV (CH1) 0.1



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H3. SETUP CONDITIONS (Cont)

Test Equipment Controls:
- Oscilloscope Mainframe
  - Intensity ..... 2 O'clock
- Dual Trace Amplifiers (both)
  - Display ..... On (pressed in)
  - Input coupling (channel 1) ..... dc (both buttons out)
  - Mode
    - Ch1 ..... On (pressed in)
  - Position (channel 1) ..... Centered
  - Ch1 Volts/Div 0.2
- Calibration Generator
  - Amplitude Mode ..... Std Ampl
    - Amplitude Selector (Volts) 0.2
    - Varible ..... Off (button in)
- Test Storage Oscilloscope
  - Intensity ..... 11 O'clock
  - Store
    - UPR ..... Off (button out)
    - LWR ..... Off (button out)
  - Erase/Enhance
    - UPR ..... Off (button out)
    - LWR ..... Off (button out)
  - Enhance Control ..... Off

a. Center the oscilloscope mainframe waveform display on the screen, and adjust the TRIGGERING LEVEL control for a stable display.

b. Press the 5D10 SAVE button in.

c. Center the test storage oscilloscope dot display on the screen (position to graticule center) using both dual-trace amplifier Channel 1 Position controls.

d. Rotate the test storage oscilloscope Intensity control fully counterclockwise.

e. Press in the test storage oscilloscope Store buttons (both UPR and LWR) and the Erase/Enhance buttons (both UPR and LWR).

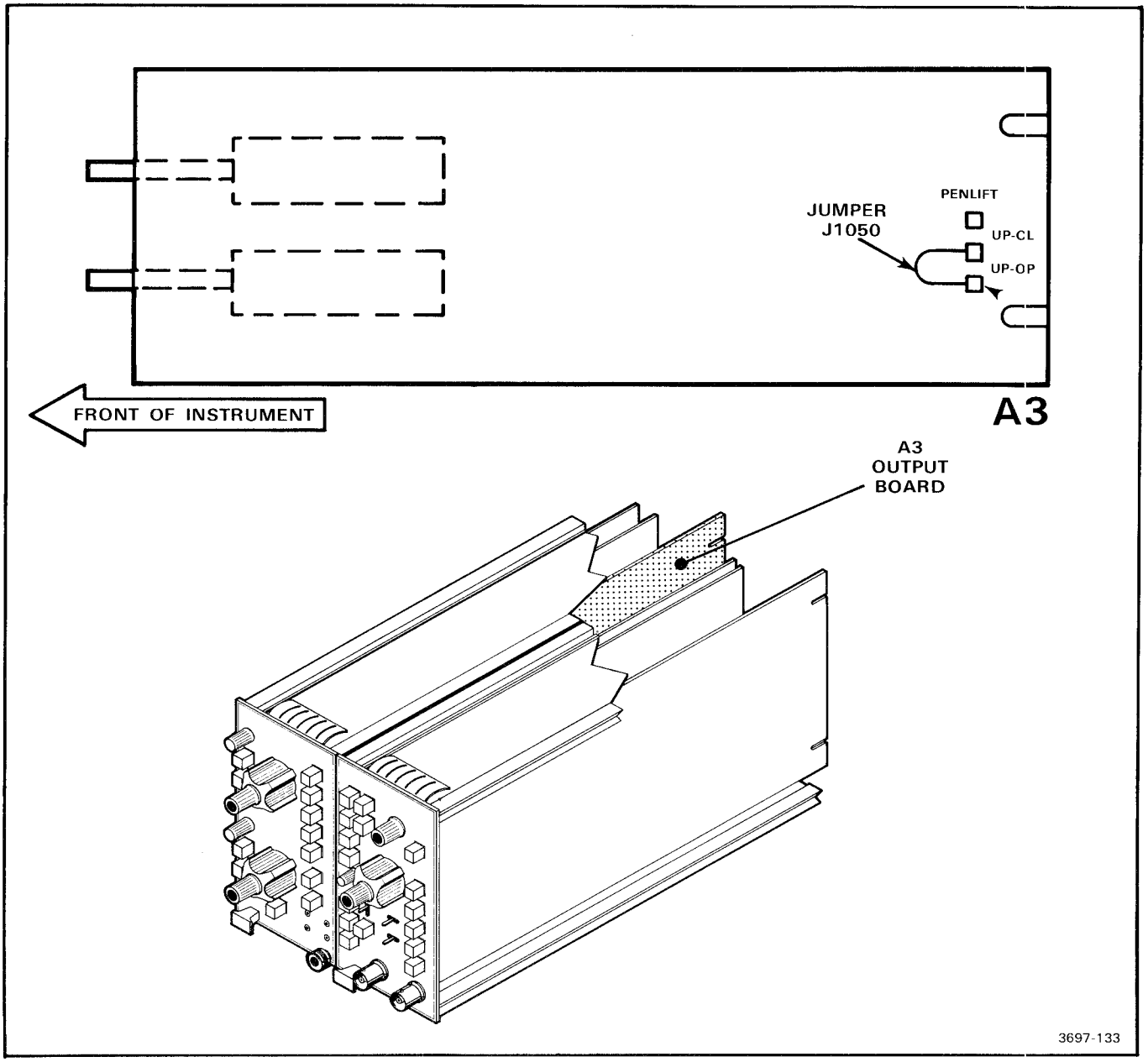
f. Press and release the test storage oscilloscope Erase button.

g. Press the 5D10 SAVED DISPLAY PLOT button in. Notice the screen will blank until the first channel of the plot is completed then display the message "CHANGE PEN COLOR IF DESIRED/RELEASE THEN PUSH PLOT TO CONTINUE". When PLOT is released, the next message "PUSH PLOT TO CONTINUE" appears. Push PLOT button as instructed. (If, at this time, you wish not to continue, release PLOT button).

h. Observe test storage oscilloscope screen duplicates the oscilloscope mainframe display (including readout information) and draws a graticule pattern.

This concludes the Performance Check.

H3. PENLIFT JUMPER LOCATION



PART II—ADJUSTMENT AND PERFORMANCE CHECK

The following procedure (Part II—Adjustment and Performance Check) provides the information necessary to: (1) verify that the instrument meets the electrical specifications, (2) verify that the controls function properly, and (3) perform all internal adjustments.

Part I—Performance Check verifies electrical specifications without making internal adjustments. All tolerances given are as specified in the Specification tables (Section 1, General Information) in this manual).

A separate Checkout Procedure is provided in Section 2, Operating Instructions to provide instrument familiarization and to verify that the controls function properly.

See Table 5-1, Calibration Procedure Electives, at the beginning of this section, for information on performing a Partial Part II—Adjustment and Performance Check Procedure.

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ADJUSTMENT AND PERFORMANCE CHECK INITIAL SETUP AND POWER-UP SEQUENCE

NOTE

The performance of this instrument can be checked at any ambient temperature from 0° to +45°C unless otherwise stated. Adjustments must be performed at an ambient temperature between +20° to 30°C for specified accuracies.

1. Remove the side and bottom cabinet covers from the oscilloscope mainframe.

2. Remove the side covers from the 5D10 Waveform Digitizer.

3. Install the 5D10 into the right vertical and horizontal plug-in compartments of the oscilloscope mainframe.

4. Connect the oscilloscope mainframe to a power source.

5. Press the 5D10 SAVE button in, and switch the oscilloscope mainframe power on.

6. Set the oscilloscope mainframe Intensity and Focus controls for comfortable viewing level.

7. Set the front-panel HORIZ CTRG and VERT CTRG screwdriver adjustments to center the display on the screen.

8. Observe a graticule pattern display on the screen with the readout '5D10 READY' at the top of the screen.

NOTE

If the graticule pattern does not appear, or the readout displays '5D10 ERROR', refer to the troubleshooting information in Section 4, Maintenance.

9. Switch on the appropriate test equipment and allow 20 minutes warmup before proceeding.

CAUTION

To prevent instrument damage, switch oscilloscope mainframe off before installing or removing plug-in units.

A. DISPLAY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
12. Alignment Tool

Shaded lines identify Performance Requirement CHECK.

A1. DISPLAY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

A2. ADJUST INTEGRATOR OFFSET (A3R451, A3R452)

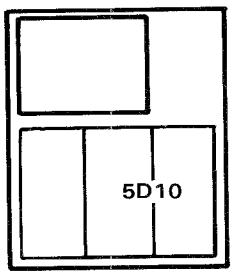
NOTE

First perform step A1, then proceed.

A2. SETUP CONDITIONS

5D10 Controls:
SAVE ..... On (pressed in)

Oscilloscope Mainframe



Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... As required
Focus ..... As required

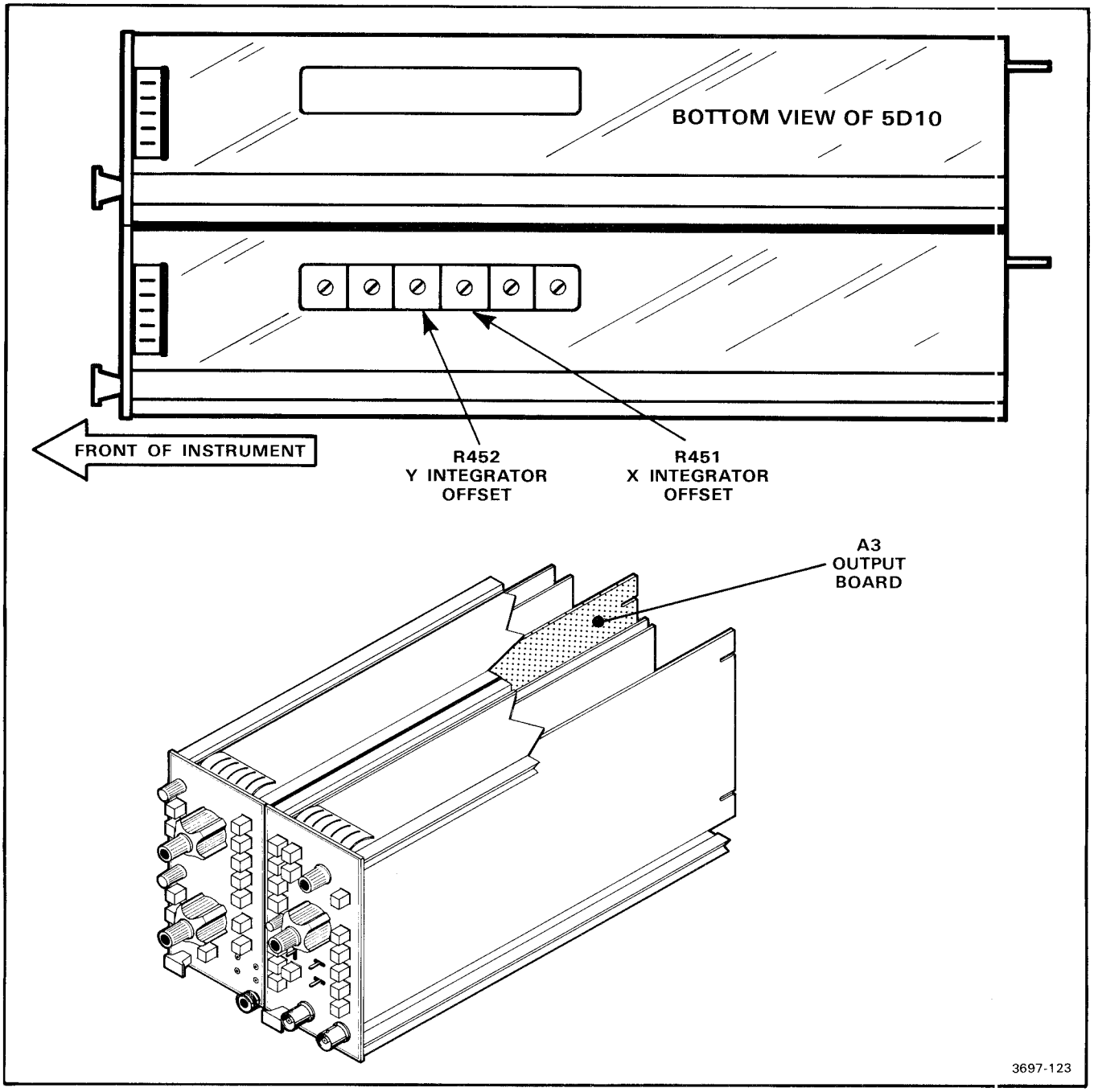
3697-100

a. **EXAMINE**—the last dot in the lower-screen readout character string for symmetry (no enlongated smearing).

b. **ADJUST**—X Integrator Offset, R451, and Y Integrator Offset, R452 (on Output Board A3) to display a symmetrical dot.

c. Rotate the INTENSITY control counterclockwise to a comfortable viewing level; set Focus as necessary.

A2. ADJUSTMENT LOCATIONS



A3. ADJUST X AND Y SAMPLE-HOLD OFFSET (A3R551, A3R552)

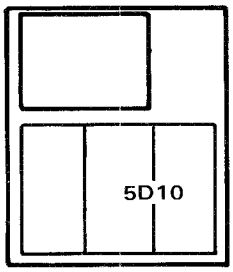
NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A3. SETUP CONDITIONS

5D10 Controls:
SAVE ..... On (pressed in)

Oscilloscope Mainframe



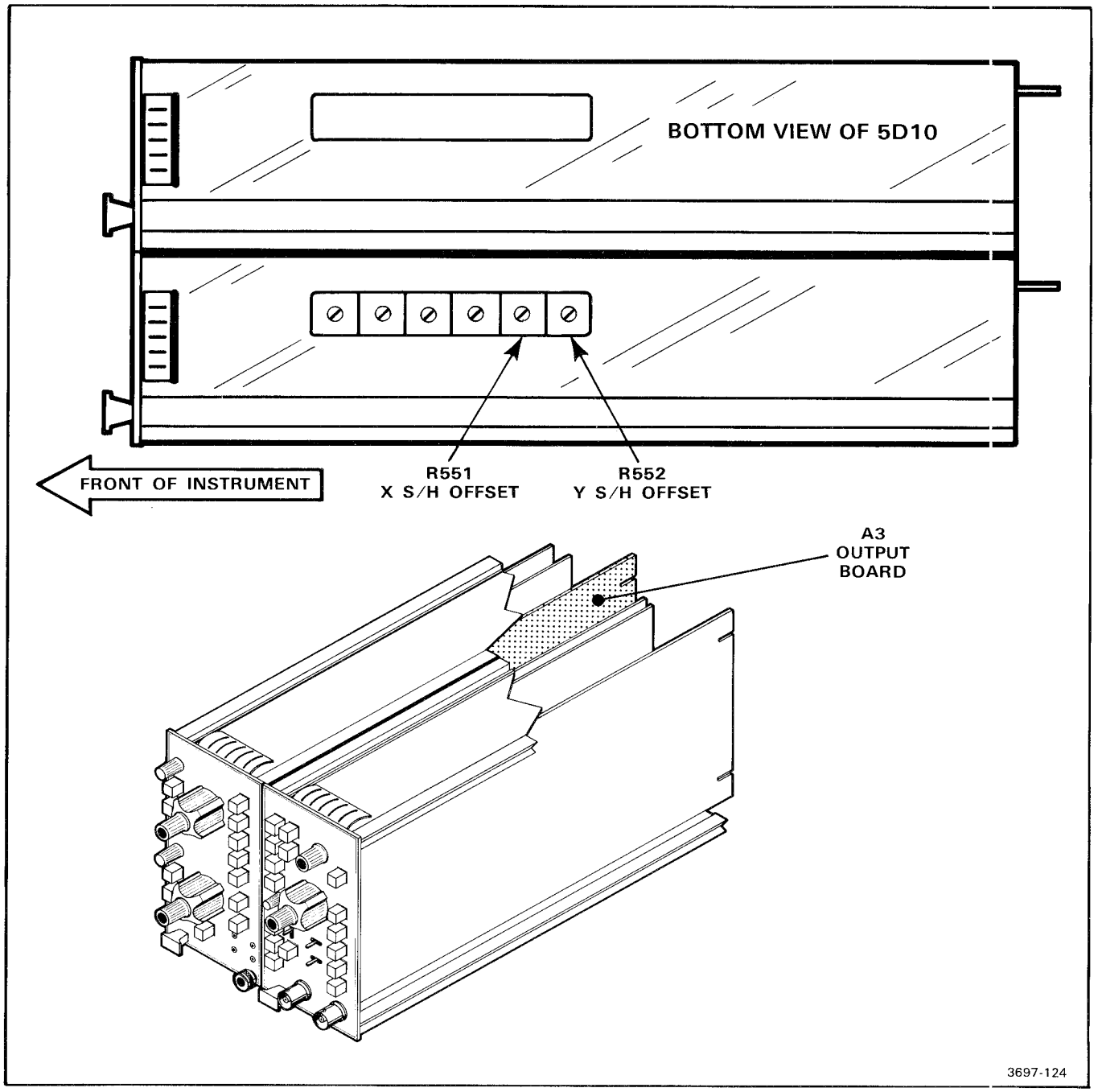
Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... 2 O'clock

3697-101

a. **EXAMINE**—the displayed graticule dots are superimposed on the displayed graticule vectors.

b. **ADJUST**—X S/H Offset, R551, and Y S/H Offset, R552 (on Output Board A3) to superimpose the graticule dots on the graticule vectors.

A3. ADJUSTMENT LOCATIONS



A4. ADJUST VECTOR TIME (A6R501)

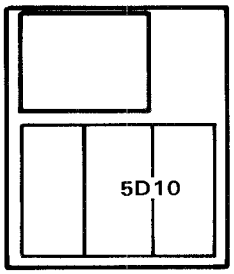
NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A4. SETUP CONDITIONS

5D10 Controls:
Make no changes in the control settings.

Oscilloscope Mainframe



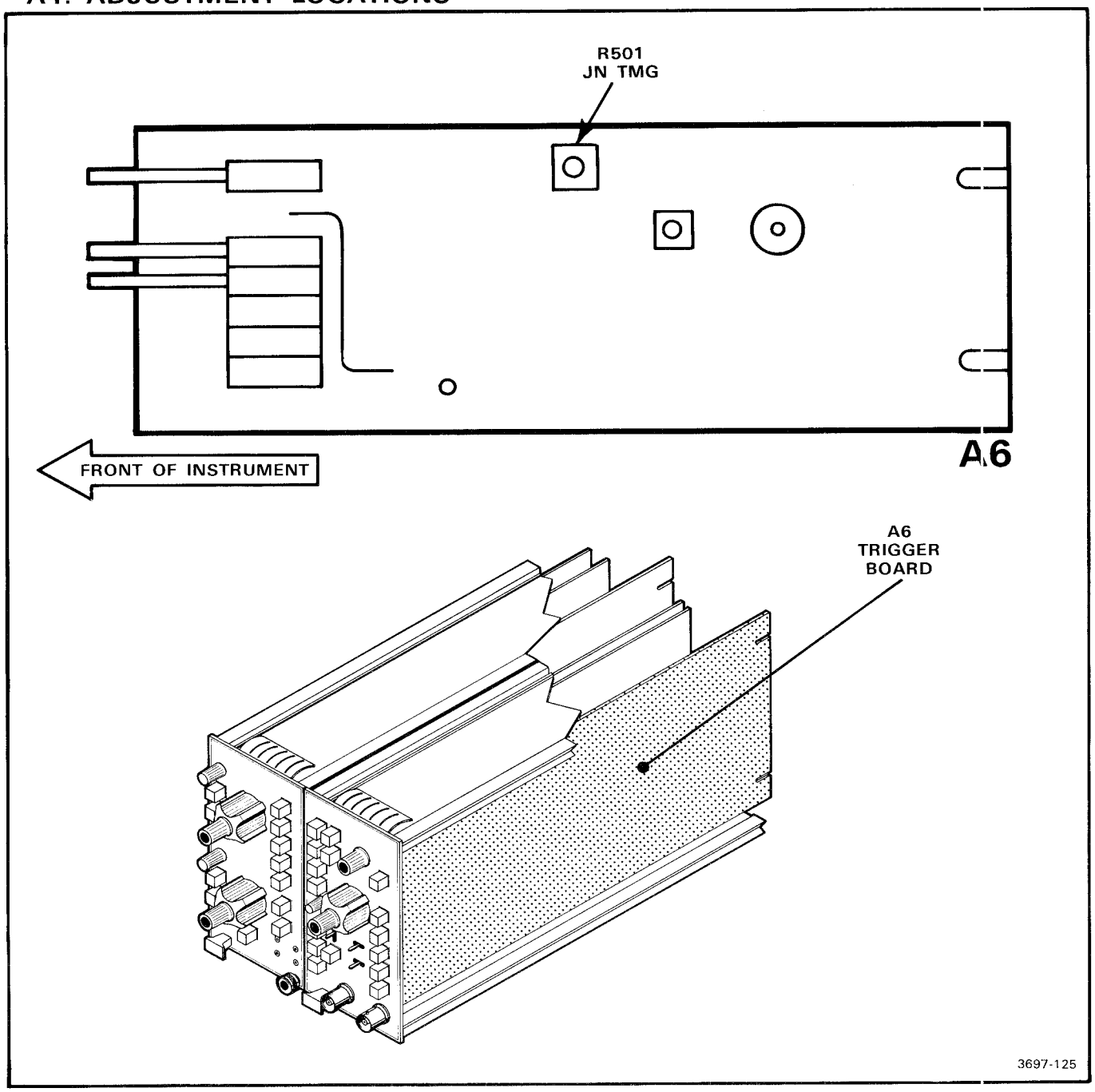
Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... 2 O'clock

3697-102

a. **EXAMINE**—the corners of the large-square pattern centered on the screen. The intensified portions should be within 0.1 division of their corner dots.

b. **ADJUST**—JN Tmg, R501 (on Trigger Board A6) to align the upper-right and lower-left intensified portions with their corner dots.

A4. ADJUSTMENT LOCATIONS



A5. CHECK/ADJUST X AND Y CENTERING AND GAIN (A3R351, A3R352)

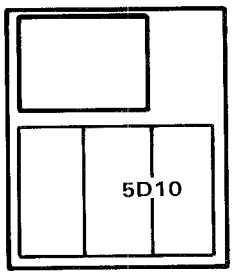
NOTE

If the preceding step was not performed, first perform step A1, then proceed.

A5. SETUP CONDITIONS

5D10 Controls:
Make no changes in the control settings:

Oscilloscope Mainframe



Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... 2 O'clock

3697-103

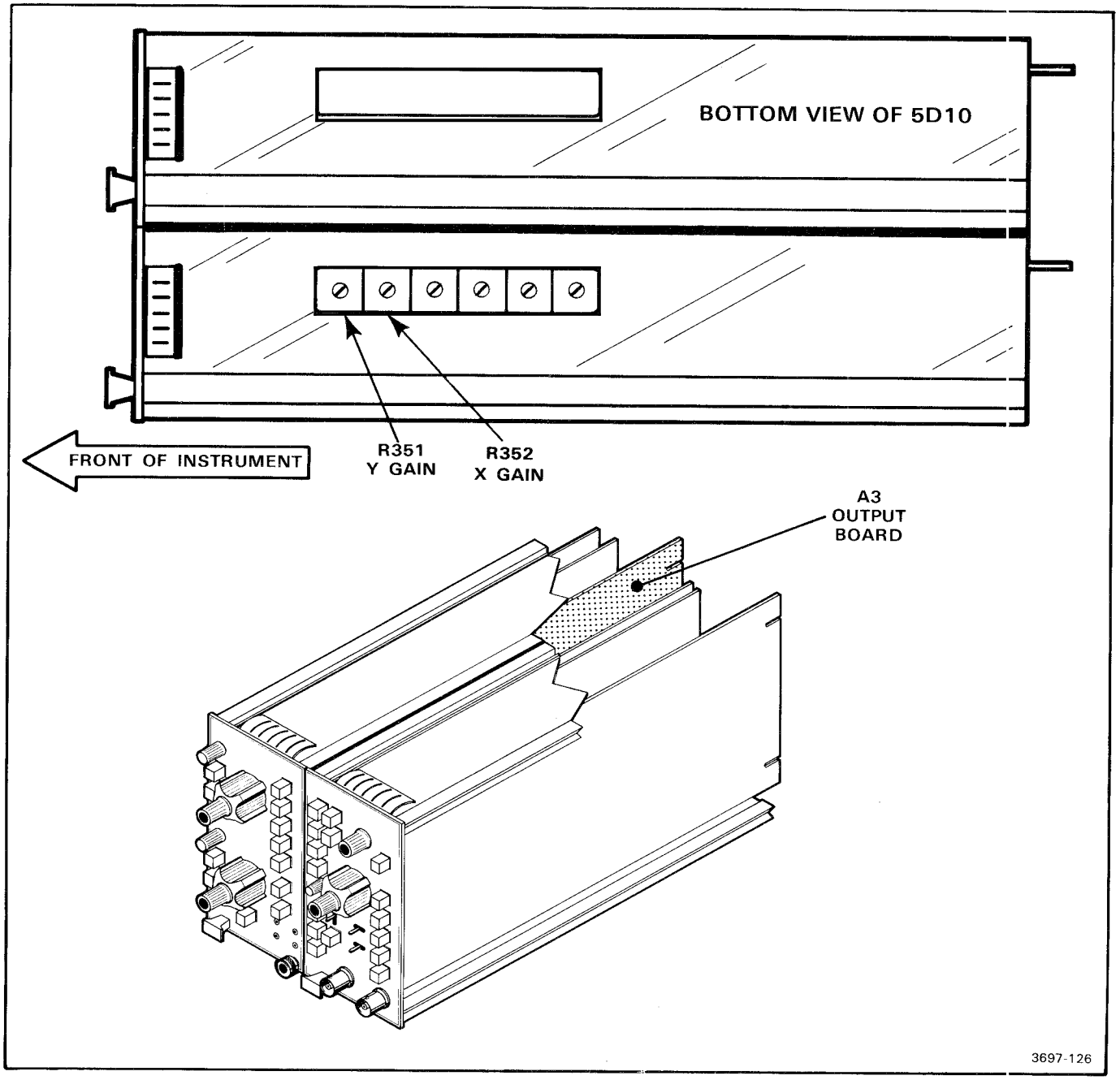
a. **CHECK**—the 2nd and 10th displayed vertical lines correspond to the 2nd and 10th crt graticule lines. All displayed vertical lines must correspond to their respective crt graticule lines within 0.1 division.

b. **ADJUST**—X Gain adjustment, R352 (on Output Board A3) and the front-panel HORIZ CTRG adjustment so that the 2nd and 10th displayed vertical graticule lines match the 2nd and 10th crt graticule lines. All displayed vertical lines must match their respective crt graticule lines within 0.1 division.

c. **CHECK**—the 2nd and 8th displayed horizontal lines correspond to the 2nd and 8th crt graticule lines. All displayed horizontal lines must correspond to their respective crt graticule lines within 0.1 division.

d. **ADJUST**—Y Gain adjustment, R351 (on Output Board A3) and the front-panel VERT CTRG adjustment so that the 2nd and 8th displayed horizontal lines match the 2nd and 8th crt graticule lines. All displayed horizontal lines must match their respective crt graticule lines within 0.1 division.

A5. ADJUSTMENT LOCATIONS



B. INPUT COMPENSATION AND ACQUISITION

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
3. Frequency counter
4. Calibration Generator
7. Power Module Mainframe
8. Normalizer
9. Attenuator
10. Coaxial Cable (42-inch)
11. Terminator (50Ω)
12. Alignment Tool
14. Probe

Shaded lines identify Performance Requirement CHECK.

B1. INPUT COMPENSATION AND ACQUISITION PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II, Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

c. Set the 5D10 controls as follows:

Coupling (CH 1 and CH 2) ..... GND (pressed in)
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... FREERUN
  SLOPE ..... / (pressed in)
  SOURCE ..... LINE
SECONDS/DIV ..... 0.1 m
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

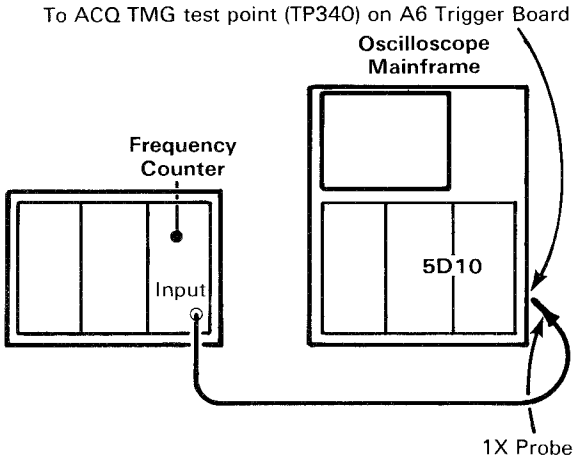
B2. ADJUST ACQUISITION TIMING (A6R612)

NOTE

First perform step B1, then proceed.

B2. SETUP CONDITIONS

5D10 Controls:
  SAVE ..... Off (released)
  VOLTS/DIV (CH 1 and CH 2) ..... 0.2 V
  TRIGGERING
    SOURCE ..... LINE (pressed in)
  CURSORS C1
  STORAGE
    VIEWTIME ..... MIN



Test Equipment Controls:
  Oscilloscope Mainframe
    Intensity & Focus ..... Adjust as necessary

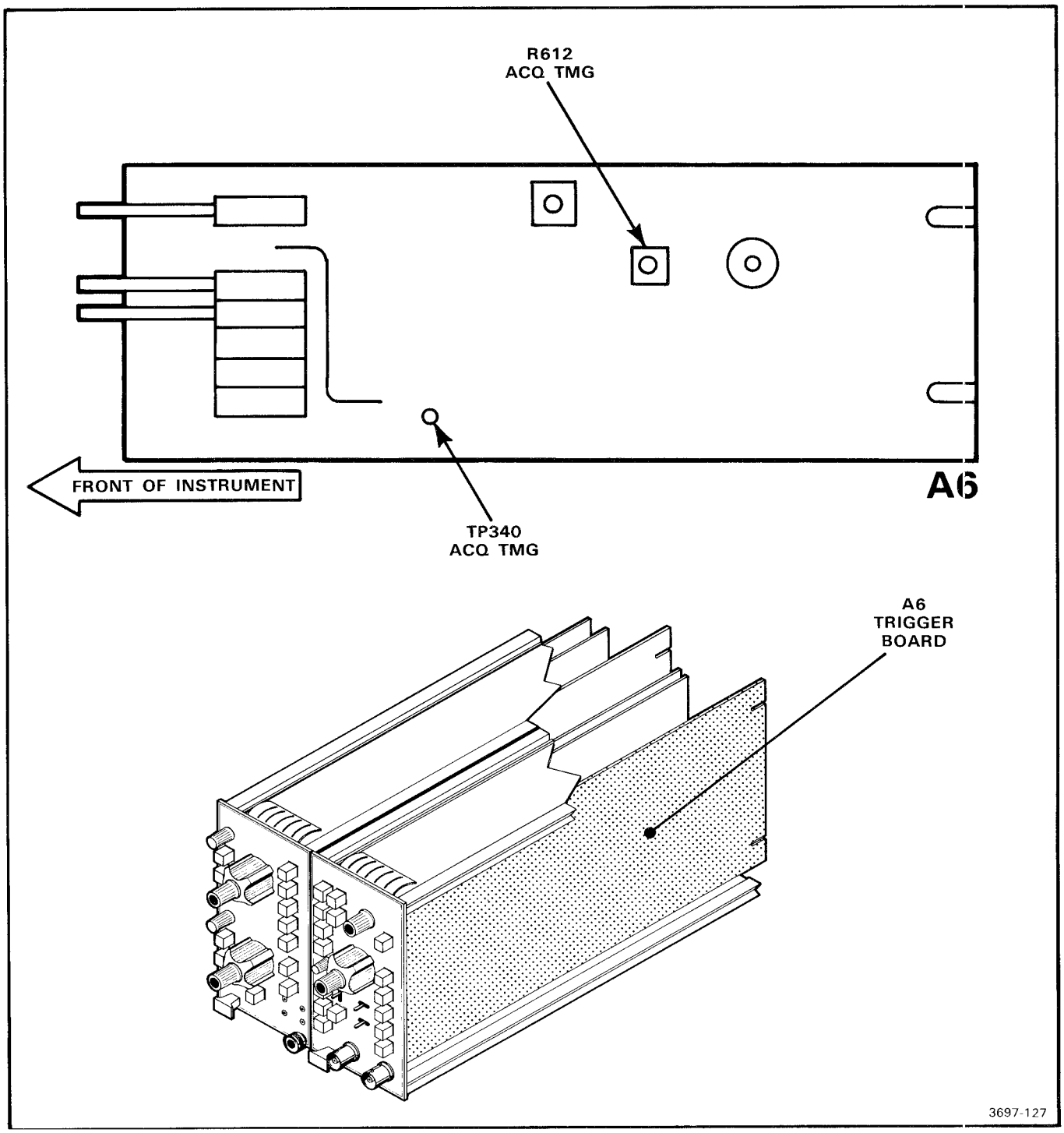
  Frequency Counter
    Function
      Frequency ..... MHz
      Resolution ..... 0.1 kHz
    Display Time ..... Fully counterclockwise

3697-104

a. **EXAMINE**—the frequency-counter readout should be 1.0000 MHz, within the range of 1.0100 to 0.9900.

b. **ADJUST**—ACQ TMG adjustment, R612 (on Trigger Board A6) for a frequency-counter readout of 1.0000 MHz.

B2. ADJUSTMENT LOCATIONS



B3. ADJUST AMPLIFIERS DC BALANCE (A1R920, A1R940)

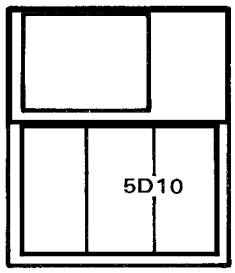
NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B3. SETUP CONDITONS

5D10 Controls:
- Coupling (CH 1 and CH 2) ..... GND (pressed in)
- VOLTS/DIV (CH 1 and CH 2) ..... 1 m
- STORAGE
  - SAVE ..... Off (released)
- CURSORS C1

Oscilloscope Mainframe



3697-105

a. Rotate the CH 1 POS control to center the trace on the screen.

b. **EXAMINE**—the vertical trace shifts less than 1.5 divisions as the CH 1 VOLTS/DIV switch is rotated throughout its range.

c. **ADJUST**—1-Bal adjustment, R920 (on Amplifier Board A1) for minimum vertical trace shift as the CH 1 VOLTS/DIV switch is alternated between the 1 m and 2 m settings.

d. **EXAMINE**—the CH 1 Volts/Div readout (refer to Fig. 5-3) corresponds to the CH 1 VOLTS/DIV switch setting throughout its range.

e. Return the CH 1 VOLTS/DIV switch to the 1 m setting.

f. Position the trace to graticule center.

g. **EXAMINE**—vertical trace shift is 1.5 divisions or less as the CH 1 VOLTS/DIV CAL knob is rotated fully counterclockwise from the detent position. A > symbol should appear in the CH 1 Volts/Div readout display when the CAL knob is out of the detent position.

h. Set the CAL knob back to the calibrated position (in detent).

i. Short the X10 sense ring (on the CH 1 input bnc connector) to ground.

j. **EXAMINE**—the CH 1 Volts/Div readout information is multiplied by a factor of 10.

k. Set the ACQUISITION AND DISPLAY to CH 2.

l. Rotate the CH 2 POS control to center the trace on the screen.

m. **EXAMINE**—the vertical trace shifts less than 1.5 divisions as the CH 2 VOLTS/DIV switch is rotated throughout its range.

n. **ADJUST**—2-Bal adjustment, R940 (on Amplifier Board A1) for minimum vertical trace shift as the CH 2 VOLTS/DIV switch is alternated between the 1 m and 2 m settings.

o. **EXAMINE**—the CH 2 Volts/Div readout information (refer to Fig. 5-2) corresponds to the CH 2 VOLTS/DIV switch setting throughout its range.

p. Return the CH 2 VOLTS/DIV switch to the 1 m setting.

q. Position the trace to graticule center.

r. **EXAMINE**—vertical trace shift is 1.5 divisions or less as the CH 2 VOLTS/DIV CAL knob is rotated fully counterclockwise from the detent position. A > symbol should appear in the CH 2 Volts/Div readout display when the CAL knob is out of the detent position.

s. Set the CAL knob back to the calibrated position (in detent).

t. Short the X10 sense ring (on the CH 2 input bnc connector) to ground.

u. **EXAMINE**—the CH 2 Volts/Div readout information is multiplied by a factor of 10.

v. Press the CH 2 INVERT button in.

w. **EXAMINE**—the vertical trace shift is 1 division or less, and that the CH 2 Volts/Div readout displays a – character.

x. Set the CH 2 INVERT button back to normal polarity (button out).

y. Set the ACQUISITION AND DISPLAY to DUAL.

z. Position both traces to graticule center.

aa. Set the ACQUISITION AND DISPLAY to ADD.

bb. **EXAMINE**—the vertical trace shifts no more than 1.5 divisions.

cc. Press the TRIGGERING POSITION PRETRIG button in.

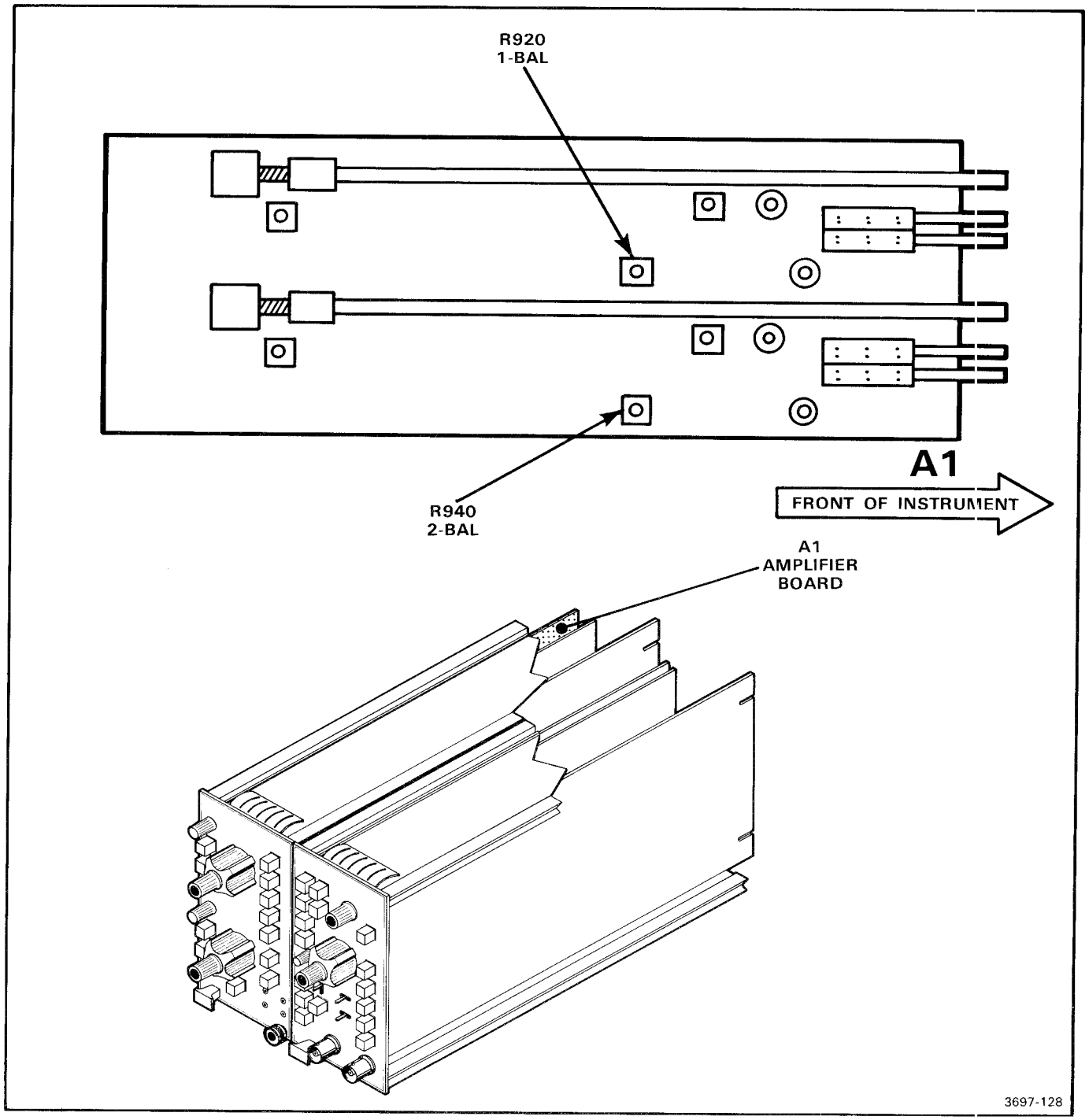
dd. **EXAMINE**—the CH 1 Voltage readout (refer to Fig. 5-3) displays the Voltage information from C1 (Cursor 1).

ee. Set the ACQUISITION AND DISPLAY to DUAL.

ff. Position both traces anywhere in the viewing area.

gg. **EXAMINE**—both CH 1 and CH 2 Volts/Div Voltage readouts appear, and that both read approximately 0.00 mV (within 0.08 mV).

B3. ADJUSTMENT LOCATIONS



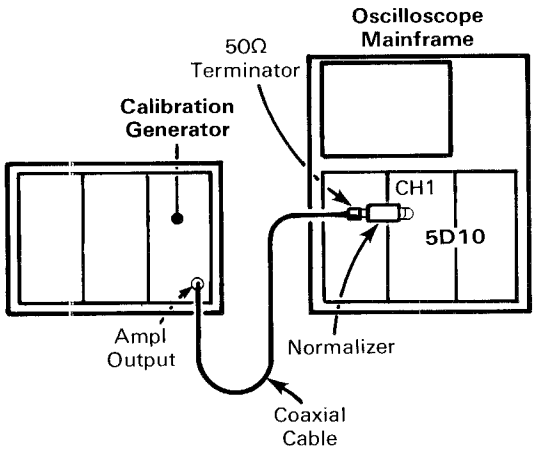
B4. CHECK/ADJUST INPUT COMPENSATION (A1C1000, A1C1002, A1C1030, A1C1032, A1C1120, A1C1140)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B4. SETUP CONDITIONS

5D10 Controls:
- VOLTS/DIV (CH 1 and CH 2) 0.5
  - ACQUISITION ..... GND (button out)
  - AND DISPLAY ..... CH 1
- TRIGGERING
  - POSITION ..... PRE TRIG
  - SOURCE ..... CH 1
- SECONDS/DIV ..... 0.2 m
- Coupling (CH 1 and CH 2) ..... DC (button out)



Test Equipment Controls:
- Oscilloscope Mainframe
  - Intensity and Focus ..... Adjust as necessary
- Calibration Generator
  - Period ..... 1 ms
  - Var ..... Fully counterclockwise
  - Amplitude Selector ..... High Ampl

3697-106

a. Set the calibration generator Pulse Amplitude control to display 5 divisions of amplitude centered on the screen.

b. Set the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—that pulse aberration rolloff and overshoot is less than 0.1 division peak and less than 0.15 division peak-to-peak. Refer to Figure 5-1 in the Performance Check portion of this section.

NOTE

If the aberrations exceed these limits, proceed with parts d through k. If the aberrations are within these limits, proceed to part l.

d. Set the CH 1 VOLTS/DIV switch to 0.2.

e. Set the calibration generator Pulse Amplitude control to display 7 divisions of signal amplitude centered on the screen.

f. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

g. **ADJUST**—1-CX1 adjustment, C1120 (on Amplifier Board A1) for optimum flat top on the waveform.

h. Set the CH 1 VOLTS/DIV switch to 0.5.

i. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude centered on the screen.

j. **ADJUST**—1-CX100, C1002, and 1-Comp, C1000 (on Amplifier Board A1) for minimum aberrations and flat top on the waveform.

k. Repeat part c of this step.

l. Move the signal from the Channel 1 input to the Channel 2 input connector.

m. Set the ACQUISITION AND DISPLAY to CH 2.

n. Set the TRIGGERING SOURCE to CH 2 and the CH 2 input coupling to DC (button out).

o. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude centered on the screen.

p. Set the TRIGGERING LEVEL control for a stable display.

q. **CHECK**—that pulse aberration rolloff and overshoot is less than 0.1 division peak and less than 0.15 division peak-to-peak.

NOTE

If the aberrations exceed these limits, proceed with parts r through y.

r. Set the CH 2 VOLTS/DIV switch to 0.2.

s. Set the calibration generator Pulse Amplitude control to display 7 divisions of signal amplitude centered on the screen.

t. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

u. **ADJUST**—2-CX1 adjustment, C1140 (on Amplifier Board A1) for optimum flat top on the waveform.

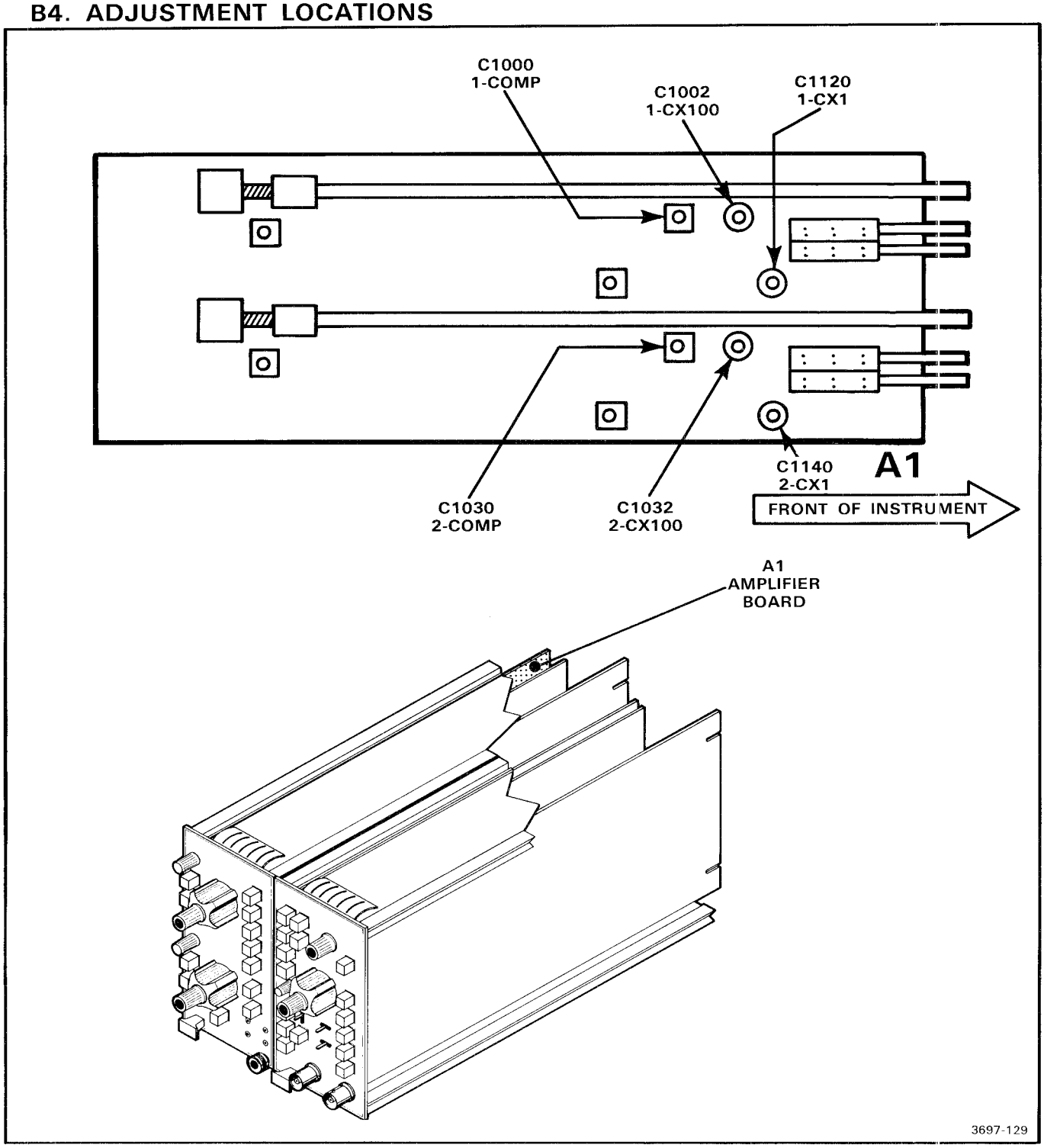
v. Set the CH 2 VOLTS/DIV switch to 0.5.

w. Set the calibration generator Pulse Amplitude control to display 5 divisions of signal amplitude centered on the screen.

x. **ADJUST**—2-CX100, C1032, and 2-Comp, C1030 (on Amplifier Board A1) for minimum aberrations and flat top on the waveform.

y. Repeat part q of this step.

B4. ADJUSTMENT LOCATIONS



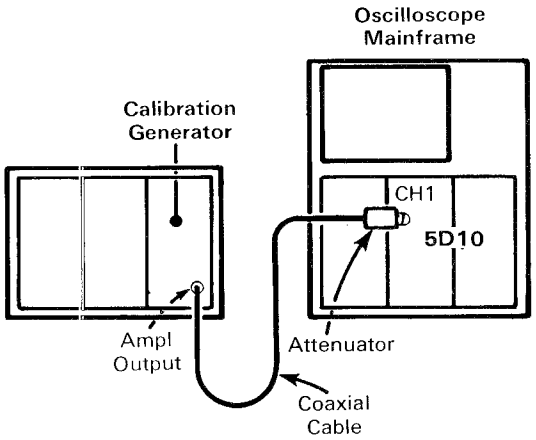
B5. CHECK/ADJUST AMPLIFIER GAIN (A1R620, A1R630)

NOTE

If the preceding step was not performed, first perform step B1, then proceed.

B5. SETUP CONDITIONS

5D10 Controls:
- ACQUISITION AND DISPLAY ..... CH 1
- VOLTS/DIV (CH 1 and CH 2) 0.2
- TRIGGERING
  - POSITION ..... PRE TRIG
  - SOURCE ..... CH 1
- SECONDS/DIV ..... 0.1 m
- CURSORS ..... C2 - C1



Test Equipment Controls:
- Oscilloscope Mainframe
  - Intensity and Focus ..... Adjust as necessary
- Calibration Generator
  - Amplitude Selector ..... Std Ampl
  - Volts
  - Amplitude ..... 2 Volts

3697-107

a. Rotate the CH 1 POS control to center the waveform on the screen.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE button in.

d. Position CURSORS C1 and C2 to measure peak-to-peak voltage of the waveform (Cursor 1 on the top and Cursor 2 on the bottom of the waveform).

e. Release the SAVE button.

f. **CHECK**—the CH 1 ΔVoltage readout for a reading of 1.500 volts, within the limits of 1.485 to 1.515 volts. (Refer to Fig. 5-3, for location of readout display information.)

g. **ADJUST**—1-Gain, R620 (on Amplifier Board A1) for a CH 1 ΔVoltage reading of 1.500 volts, within the limits of 1.485 to 1.515 volts.

h. **CHECK**—that the displayed waveform amplitude is 7.5 divisions, within the limits of 7.35 to 7.65 divisions.

i. **CHECK**—the CH 1 vertical accuracy as shown in Table 5-6.

j. Rotate the CH 1 CAL control fully counterclockwise.

k. **CHECK**—the signal for 2 divisions or less amplitude.

l. Set the CH 1 CAL control to display exactly 2 divisions of signal amplitude.

m. Set the CH 1 input coupling to AC (button in).

n. **CHECK**—rotate the CH 1 POS control throughout its range and check that the signal display moves completely

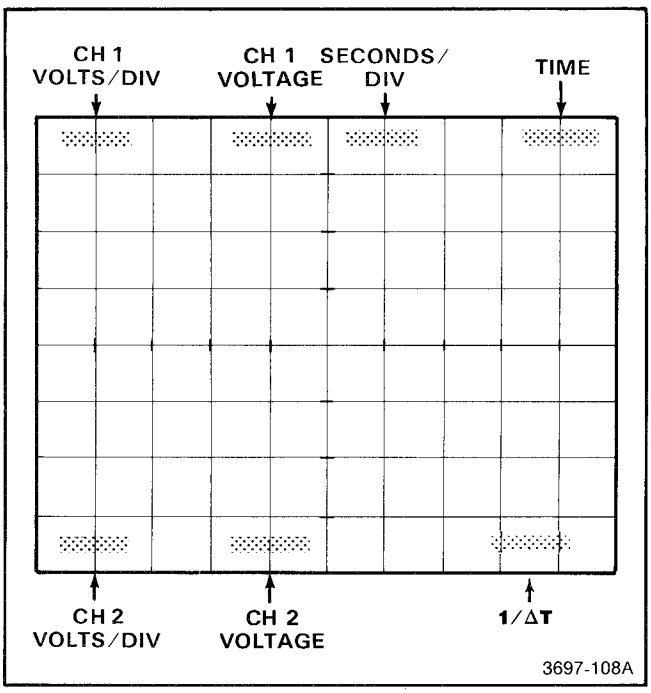


Figure 5-3. Location of readout information.

off screen at each extreme setting of the CH 1 POS control.

o. Return the CH 1 CAL control to the calibrated position (in detent).

p. Disconnect the calibration generator signal from the CH 1 input and reconnect it (through the attenuator) to the CH 2 input connector.

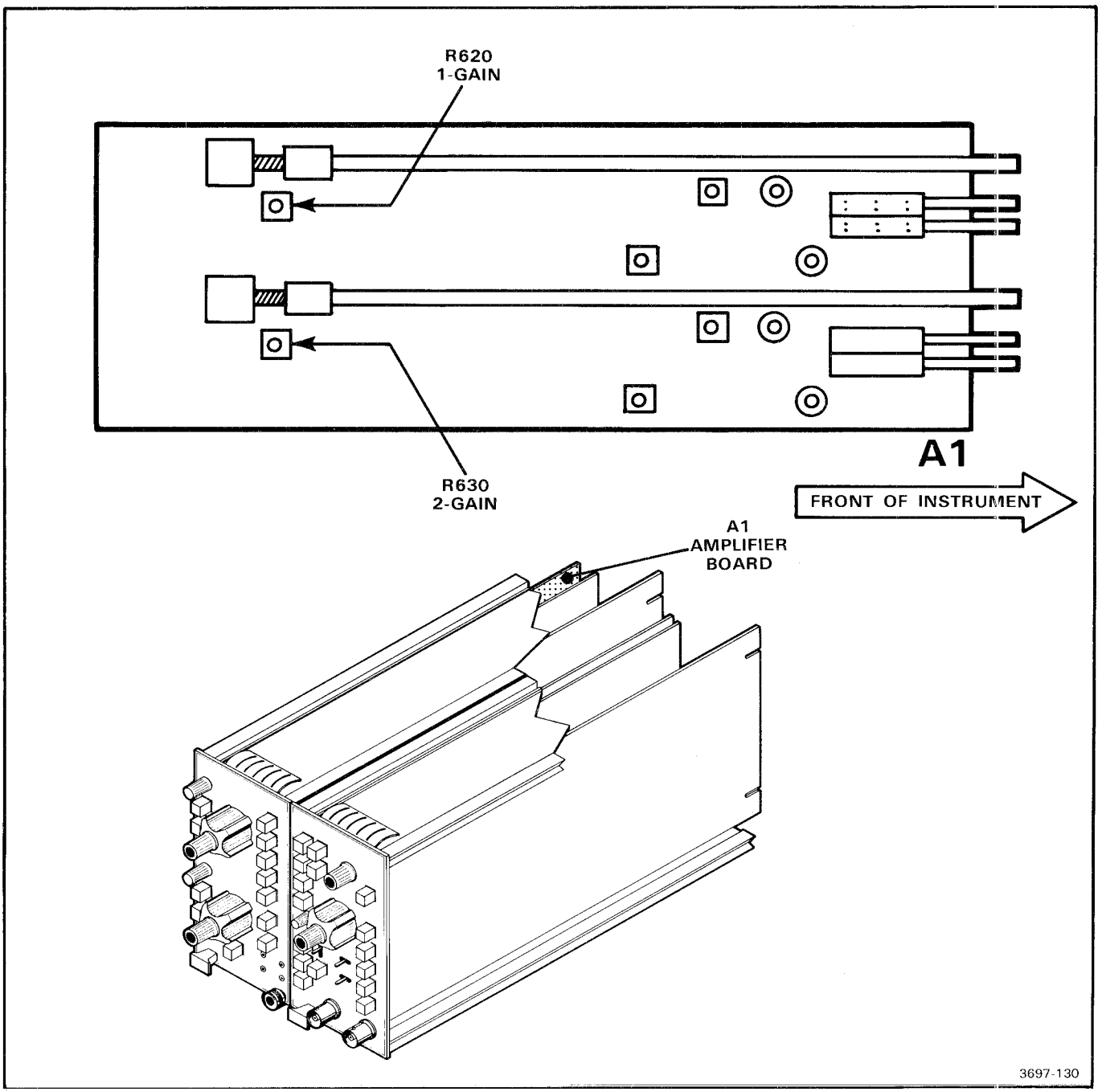
q. Set the ACQUISITION AND DISPLAY to CH 2, and the TRIGGERING SOURCE to CH 2.

r. Set the CH 2 VOLTS/DIV switch to 0.2.

s. Set the calibration generator Amplitude control to 2 volts.

t. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

B5. ADJUSTMENT LOCATIONS



u. Rotate the CH 2 POS control to center the waveform on the screen.

v. **CHECK**—the CH 2 △Voltage readout for a reading of 1.500 volts, within the limits of 1.485 to 1.515 volts.

w. **ADJUST**—2-Gain, R630 (on Amplifier Board A1) for a CH 2 △Voltage reading of 1.500 volts, within the limits of 1.485 to 1.515 volts.

x. **CHECK**—that the displayed waveform amplitude is 7.5 divisions, within the limits of 7.35 to 7.65 divisions.

y. **CHECK**—the CH 2 vertical accuracy as shown in Table 5-6.

z. Rotate the CH 2 CAL control fully counterclockwise.

aa. **CHECK**—the signal amplitude for 2 divisions or less.

bb. Set the CH 2 CAL control to display exactly 2 divisions of signal amplitude.

cc. Set the CH 2 input coupling to AC (button in).

dd. **CHECK**—rotate the CH 2 POS control throughout its range and check that the signal display moves completely off screen at each extreme setting of the CH 2 POS control.

ee. Return the CH 2 CAL control to the calibrated position (in detent).

ff. Press the CH 1 GND button in.

gg. Set the ACQUISITION AND DISPLAY to ADD.

hh. **CHECK**—the signal amplitude is 5 divisions, within the limits of 4.85 to 5.15 divisions.

ii. Set the CH 1 VOLTS/DIV to 20.

jj. **CHECK**—the CH 1 △Voltage readout display reads 100.0 volts, within the limits of 98.0 to 102.0 volts.

kk. Set the CH 1 VOLTS/DIV control to 10.

ll. **CHECK**—the CH 1 △Voltage readout display reads 5.00 D, within the limits of 4.90 D to 5.10 D at all settings (except 20) of the CH 1 VOLTS/DIV control.

TABLE 5-6
CH 1 and CH 2 VOLTS/DIV Accuracy

Calibration Generator Amplitude	VOLTS/DIV Setting (CH 1 & CH 2)	Displayed Amplitude (Divisions)	△Voltage Readout (CH 1 & CH 2)
10 m	1 m	7.35 to 7.65	7.35 to 7.65 mV
20 m	2 m	7.35 to 7.65	14.70 to 15.30 mV
50 m	5 m	7.35 to 7.65	37.1 to 37.9 mV
0.1	10 m	7.35 to 7.65	74.3 to 75.8 mV
0.2	20 m	7.35 to 7.65	148.5 to 151.5 mV
0.5	50 m	7.35 to 7.65	371 to 379 mV
1	0.1	7.35 to 7.65	743 to 758 mV
2	0.2	7.35 to 7.65	1.485 to 1.515 V
5	0.5	7.35 to 7.65	3.71 to 3.79 V
10	1	7.35 to 7.65	7.43 to 7.58 V
Remove the 067-1067-00 Attenuator			
10	2	4.9 to 5.1	9.80 to 10.20 V
20	5	3.92 to 4.08	19.6 to 20.4 V
50	10	4.9 to 5.1	49.0 to 51.0 V
100	20	4.9 to 5.1	98.0 to 102.0 V

C. BANDWIDTH, X-Y PHASE SHIFT, AND CMR

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable (42-inch)
13. Dual-Input Coupler

Shaded lines identify Performance Requirement CHECK.

C1. BANDWIDTH, X-Y PHASE SHIFT, AND CMR PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1 and CH 2) 0.2
Coupling (CH 1 and CH 2) ..... AC (pressed in)
ACQUISITION AND DISPLAY ..... CH 1
TRIGGERING
POSITION ..... FREERUN
SLOPE ..... / (pressed in)
SOURCE ..... CH 1
CURSORS ..... OFF
SECONDS/DIV ..... 5 m
STORAGE
VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

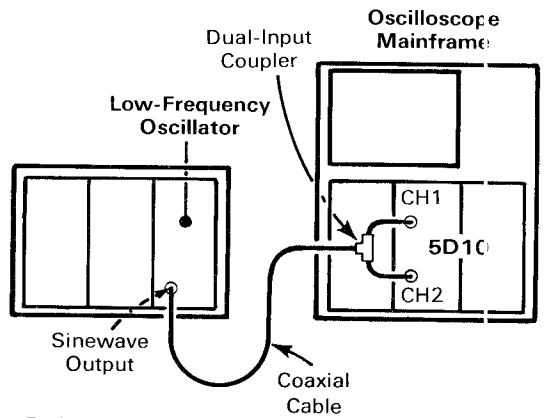
C2. CHECK BANDWIDTH, X-Y PHASE SHIFT, AND CMR

NOTE

First perform step C1, then proceed.

C2. SETUP CONDITIONS

5D10 Controls:
Make no changes to the control settings.



Test Equipment Controls:
Low-Frequency Oscillator
Frequency Hz 1
Multiplier X1K
Step Attenuator 10

3697-109

a. Set the low-frequency oscillator Var Attenuator control to display exactly 6 divisions of signal amplitude at 1 kilohertz.

b. Set the low-frequency oscillator Multiplier to X10 (10 hertz).

c. **CHECK**—that the displayed signal amplitude is 4.2 divisions or more.

d. Set the ACQUISITION AND DISPLAY to CH 2.

e. **CHECK**—that the displayed signal amplitude is 4.2 divisions or more.

f. Set the CH 1 and CH 2 coupling pushbuttons to DC (released).

g. Set the low-frequency oscillator Multiplier to X100K (100 kHz).

h. Set the SECONDS/DIV switch to 0.1 m.

i. **CHECK**—that the displayed signal amplitude is at least 4.2 divisions peak-to-peak.

j. Set the ACQUISITION AND DISPLAY to X:CH 1 Y:CH 2.

k. **EXAMINE**—the CH 1 POS control should move the display horizontally and the CH 2 POS control should move the display vertically.

l. If necessary, readjust the low-frequency oscillator Var Attenuator control to display 6 divisions vertically.

m. **CHECK**—for 0.1 division or less of horizontal opening.

n. Press the CH 2 INVERT button in.

o. Set the CH 1 and CH 2 VOLTS/DIV switches to 0.1.

p. Set the ACQUISITION AND DISPLAY to ADD.

q. **CHECK**—that the signal display amplitude is 0.24 division or less (peak-to-peak).

D. CHANNEL ISOLATION

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable

Shaded lines identify Performance Requirement CHECK.

D1. CHANNEL ISOLATION PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any changes which may affect this procedure.

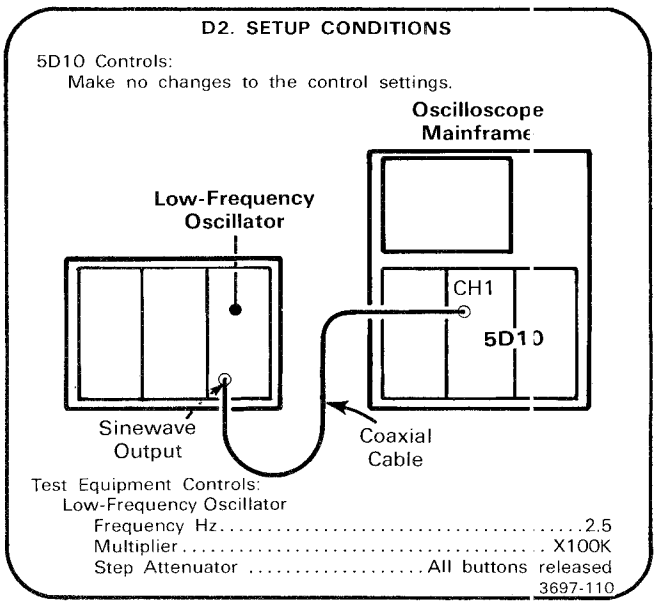
c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 2
VOLTS/DIV (CH 2) 20
ACQUISITION AND DISPLAY ..... CH 1
Coupling (CH 2) ..... GND (pressed in)
TRIGGERING
  POSITION ..... FREERUN
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1 (pressed in)
SECONDS/DIV ..... 0.1 m
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

D2. CHECK DISPLAY-RELATED AND INPUT-RELATED SIGNAL ISOLATION

NOTE

First perform step D1, then proceed.



a. Set the low-frequency oscillator Var Attenuator control to display a signal amplitude of 5 divisions at 250 kHz.

b. Set the CH 1 VOLTS/DIV switch to 0.5.

c. Set the ACQUISITION AND DISPLAY to CH 2.

d. **CHECK**—that the displayed signal amplitude is 0.2 division or less.

e. Release the CH 2 GND button.

f. Press the CH 1 GND button in.

g. Move the signal input from the CH 1 input to the CH 2 input connector.

h. Set the CH 2 VOLTS/DIV switch to 0.5.

i. Set the CH 1 VOLTS/DIV switch to 20.

j. Set the ACQUISITION AND DISPLAY to CH 1.

k. **CHECK**—that the displayed signal amplitude is 0.2 division or less.

l. Release the CH 1 GND button.

m. Set the CH 2 VOLTS/DIV switch to 20.

n. Press the CH 2 GND button in.

o. Set the CH 1 VOLTS/DIV switch to 1 m.

p. **CHECK**—that the displayed signal amplitude is 1 division or less.

q. Release the CH 2 GND button.

r. Press the CH 1 GND button in.

s. Set the CH 1 VOLTS/DIV switch to 20.

t. Set the CH 2 VOLTS/DIV switch to 1 m.

u. Move the signal input from the CH 2 input to the CH 1 input connector.

v. Set the ACQUISITION AND DISPLAY to CH 2.

w. **CHECK**—that the displayed signal amplitude is 1 division or less.

E. TRIGGERING LEVEL AND SENSITIVITY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable
13. Dual-Input Coupler

Shaded lines identify Performance Requirement CHECK.

E1. TRIGGERING LEVEL AND SENSITIVITY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any change which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1 and CH 2) 0.2
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
CURSORS ..... OFF
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

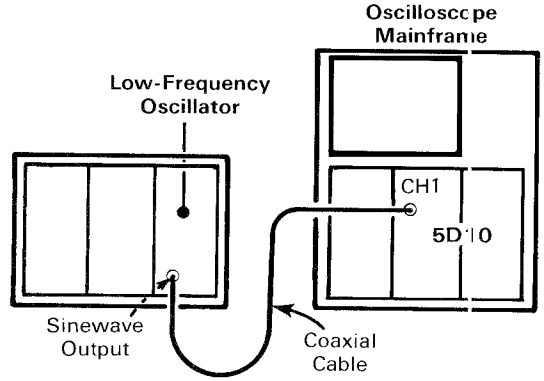
E2. CHECK TRIGGERING LEVEL RANGE

NOTE

First perform steps E1, then proceed.

E2. SETUP CONDITIONS

5D10 Controls:
  TRIGGERING
    COUPLING ..... DC (released)
    POSITION ..... PRE TRIG
  SECONDS/DIV ..... 1 m



Test Equipment Controls:
  Low-Frequency Oscillator
    Frequency Hz 1
    Multiplier X1K
    Step Attenuator ..... All buttons released

3697-111

a. Set the low-frequency oscillator Var Attenuator to display an 8 division 1 kHz signal on the screen.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—the green TRIG'D indicator light is on, and an intensified dot (triggering point) is displayed on the rising edge of the waveform approximately 1.25 divisions in from the right side of the screen.

d. Set the TRIGGERING SLOPE to \ (pushbutton in), and the POSITION to CTR TRIG.

e. **CHECK**—the green TRIG'D indicator light remains on, and the intensified dot (triggering point) is displayed on the falling edge of the waveform at the approximate horizontal center of the screen.

f. Set the TRIGGERING POSITION to POST TRIG, the SLOPE to BI-SLOPE (both buttons pressed in), and the TRIGGERING COUPLING to AC (button pressed in).

g. Rotate the TRIGGERING SENSITIVITY control to the MAX position.

h. **CHECK**—the green TRIG'D indicator light remains on, the intensified dot (triggering point) is displayed approximately 1.25 divisions in from the left side of the screen, and the intensified dot may occur on either the rising or falling edge of the waveform.

i. Set the TRIGGERING POSITION to FREE RUN.

j. **CHECK**—the green TRIG'D indicator light remains on and the signal display is free-running (not triggered).

k. Press the STORAGE SAVE button in.

l. **CHECK**—that the intensified dot (triggering point) is displayed at the end of the trace (right side of screen).

m. Release the STORAGE SAVE button.

n. Set the TRIGGERING POSITION to CTR TRIG.

o. Set the CH 1 VOLTS/DIV switch to 0.1.

p. Rotate the TRIGGERING LEVEL control fully clockwise.

q. **CHECK**—that the display is not triggered.

r. Set the TRIGGERING SLOPE to / (button in).

s. **CHECK**—rotate the TRIGGERING LEVEL control through its range and check that the trace is not triggered at the fully clockwise and counterclockwise position of the TRIGGERING LEVEL control.

t. Set the TRIGGERING SLOPE to \ (button in).

u. **CHECK**—rotate the TRIGGERING LEVEL control through it's range and check that the trace is not triggered at the fully clockwise and counterclockwise position of the TRIGGERING LEVEL control.

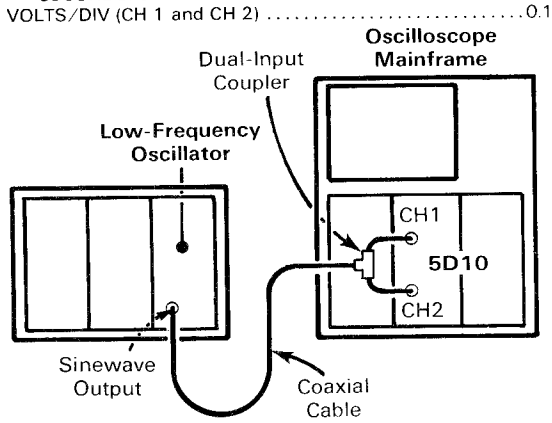
E3. CHECK TRIGGERING SENSITIVITY AND GROUND-REFERENCE UPDATE

NOTE

If the preceding step was not performed, first perform step E1, then proceed.

E3. SETUP CONDITIONS

5D10 Controls:
- TRIGGERING
  - POSITION ..... CTR TRIG
  - COUPLING ..... AC (pressed in)
  - SECONDS/DIV ..... 0.1 m
- VOLTS/DIV (CH 1 and CH 2) 0.1



Test Equipment Controls:
- Low-Frequency Oscillator
  - Frequency Hz 5
  - Multiplier X10K
  - Step Attenuator ..... 10 and 20 (pressed in)

3697-112

a. Set the low-frequency oscillator to display a signal amplitude of 0.4 division at 50 kHz.

b. Rotate the TRIGGERING LEVEL control for a stable display.

c. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE.

d. Set the ACQUISITION AND DISPLAY to CH 2.

e. Set the TRIGGERING SOURCE to CH 2.

f. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

g. Set the low-frequency oscillator to display a signal amplitude of 1 division at 250 kHz.

h. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

i. Set the ACQUISITION AND DISPLAY to CH 1.

j. Set the TRIGGERING SOURCE to CH 1.

k. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

l. Set both the CH 1 and CH 2 VOLTS/DIV switches to 50 m.

m. Move the CH 2 input signal to the TRIGGERING SOURCE EXT input connector (the other half of the dual-input coupler remains on the CH 1 input connector).

n. Set the TRIGGERING SOURCE to EXT.

o. Set the low-frequency oscillator to display a signal amplitude of 5 divisions at 2.5 kHz.

p. Set the low-frequency oscillator frequency to 250 kHz; do not disturb the low-frequency oscillator amplitude setting.

q. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

r. Set the low-frequency oscillator to display a signal amplitude of 2 divisions at 50 kHz.

s. **CHECK**—that a stable display can be obtained in both / SLOPE and \ SLOPE; rotate the TRIGGERING LEVEL control as necessary.

t. Remove all cables.

u. Set the TRIGGERING SOURCE to LINE.

v. Set the SECONDS/DIV switch to 0.2.

w. **CHECK**—that the green TRIG'D light remains on as the TRIGGERING LEVEL control is rotated throughout its range.

x. **CHECK**—that the POSSIBLE UNDERSAMPLING indicator lights when the SECONDS/DIV CAL knob is rotated counterclockwise approximately 90 degrees.

y. Return the SECONDS/DIV CAL knob to its calibrated (detent) position.

z. Set the SECONDS/DIV switch to 1 m.

aa. Set the CURSORS switch to C1.

bb. **EXAMINE**—rotate the CH 1 POS control throughout its range. Note the CH 1 Voltage readout display reads the number of divisions the trace is above or below the vertical graticule center, and the readout suffix is always D.

cc. Position the trace to graticule center with the CH 1 POS control.

dd. Press the CH 1 GND button in, wait at least one update, then release the CH 1 GND button.

ee. **EXAMINE**—the CH 1 Voltage readout now displays 0 mV.

ff. **EXAMINE**—position the trace to the second graticule line from the top and check that the CH 1 Voltage readout reads approximately 150 mV. Press the CH 1 GND button in and note the readout display changes to 0 mV after the next update.

gg. Release the CH 1 GND button.

hh. Set the ACQUISITION AND DISPLAY to CH 2.

ii. Repeat parts bb through ff for the CH 2 Voltage readout display.

F. TIME-BASE ACCURACY

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
5. Low-Frequency Oscillator
6. Time-Mark Generator
7. Power Module Mainframe
10. Coaxial Cable (three required)
11. Terminator
16. Ramp Generator

Shaded lines identify Performance Requirement CHECK.

F1. TIME-BASE ACCURACY PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any change which may affect this procedure.

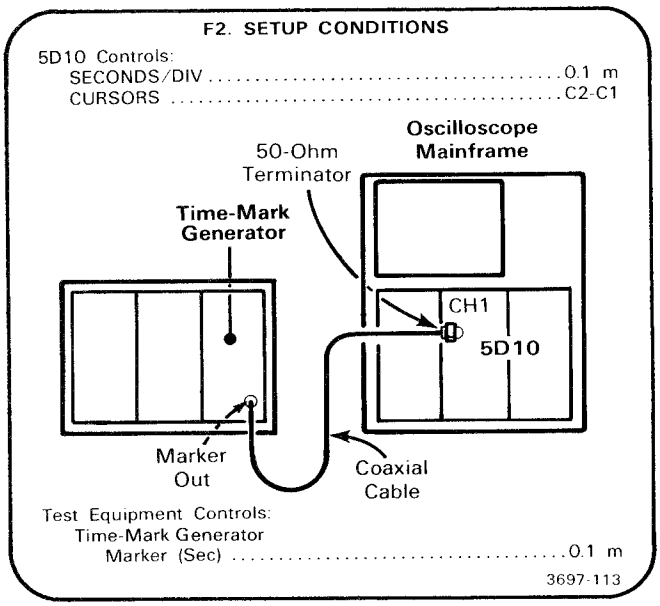
c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 0.5
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... POST TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
STORAGE
  VIEWTIME ..... INF
All other pushbuttons ..... Off (released)

F2. CHECK TIMING ACCURACY

NOTE

First perform step F1, then proceed.



a. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

b. Position CURSORS (C1 and C2) to the second and tenth time markers.

c. **CHECK**—that the ΔTime readout on the screen (refer to Fig. 5-3 in step B, Input Compensation And Acquisition) reads between 792 and 808 μs and frequency readout (1/ΔT) equals between 1.26 and 1.24 kHz.

d. **CHECK**—the horizontal timing accuracy as shown in Table 5-7. Press and release the STORAGE VIEWTIME control, and reposition the cursors to the top of the second and tenth markers for each SECONDS/DIV and time mark generator setting. Observe the display does not update until the STORAGE VIEWTIME control is pressed and released.

e. Set the SECONDS/DIV switch to 1 m, and the STORAGE VIEWTIME control to MIN.

f. Set the time-mark generator Marker (Sec) switch to 5 m.

g. Rotate the SECONDS/DIV CAL knob fully counterclockwise.

h. **CHECK**—for 2 divisions or less between time markers.

i. Return the SECONDS/DIV CAL knob to the calibrated (detent) position.

j. Set the time-mark generator Marker (Sec) switch to 0.5 ms.

k. Press the STORAGE SAVE button in.

l. Position CURSORS (C1 and C2) to the top of two adjacent time markers.

m. **CHECK**—that when the SWP MGF (sweep magnification) is pressed in, the Seconds/Div readout display changes from 1 ms to 100 μs, and the displayed Time markers are 5 divisions apart.

n. Release the JOIN DOTS pushbutton.

o. **EXAMINE**—the time markers are displayed with dots.

p. Release the STORAGE SAVE button and SWP MGF buttons.

TABLE 5-7
Horizontal Timing Accuracy

SECONDS/DIV and Marker Switch Settings	Seconds/Div Readout	Δ Time Readout	SN B020100 & Up 1/ΔT Readout
0.1 m	100 μs	792 to 808 μs	1.26 to 1.24 kHz
0.2 m	200 μs	1.584 to 1.616 ms	631 to 619 Hz
0.5 m	500 μs	3.960 to 4.040 ms	253 to 248 Hz
1 m	1 ms	7.92 to 8.08 ms	126 to 124 Hz
2 m	2 ms	15.84 to 16.16 ms	63.1 to 61.9 Hz
5 m	5 ms	39.60 to 40.40 ms	25.3 to 24.8 Hz
10 m	10 ms	79.2 to 80.8 ms	12.6 to 12.4 Hz
20 m	20 ms	158.4 to 161.6 ms	6.31 to 6.19 Hz
50 m	50 ms	396.0 to 404.0 ms	2.53 to 2.48 Hz
0.1	100 ms	792 to 808 ms	1.26 to 1.24 Hz
0.2	200 ms	1.584 to 1.616 s	631 to 619 mHz
0.5	500 ms	3.960 to 4.040 s	253 to 248 mHz
1	1 s	7.92 to 8.08 s	126 to 124 mHz
2	2 s	15.84 to 16.16 s	63.1 to 61.9 mHz
5	5 s	39.60 to 40.40 s	25.3 to 24.8 mHz
10	10 s	Rotate the SECONDS/DIV switch to 10, 20, and 50, and note the readout display is 10, 20, and 50 s respectively. The 10, 20, and 50 second timing accuracy is verified as a function of the 0.1 m through 5 second accuracy checks.	
20	20 s		
50*	50 s		

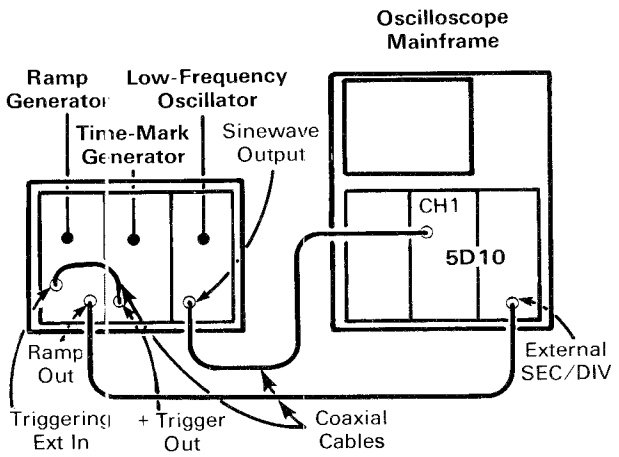
F3. CHECK EXTERNAL SEC/DIV INPUT

NOTE

If the preceding step was not performed, first perform step F1, then proceed.

F3. SETUP CONDITIONS

5D10 Controls:
- ACQUISITION AND DISPLAY
  - JOIN DOTS ..... On (pressed in)
- SECONDS/DIV ..... 10 m
- CURSORS ..... Off
- STORAGE
  - VIEWTIME ..... MIN



Test Equipment Controls:
- Time-Mark Generator
  - Marker (Sec) ..... 0.1 m
- Low Frequency Oscillator
  - Frequency Hz 1
  - Multiplier X100
  - Step Attenuator 10
- Ramp Generator
  - Triggering ..... Ext
    - Level ..... Centered
  - Ramp Duration ..... 10 μs
    - Polarity ..... +
  - Ramp Amplitude ..... 2 V

3697-114

a. Set the low-frequency oscillator Var Attenuator to display an amplitude of 5 divisions at 100 hertz.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE REF in.

d. Set the SECONDS/DIV switch to EXT.

NOTE

If there is no acquired waveform, adjust the Ramp Generator Triggering Level control as necessary.

e. **CHECK**—that the reference waveform matches the acquired waveform within 0.2 division (measured 1 division in from the right graticule edge).

f. Press the STORAGE TRACE STEP button in.

g. **EXAMINE**—the reference waveform shifts downward approximately 0.8 division from the acquired waveform.

h. Release the STORAGE SAVE REF and TRACE SEP pushbuttons.

G. LEFT PLUG-IN FUNCTIONS

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
2. Dual-Trace Amplifier
4. Calibration Generator
5. Low-Frequency Oscillator
7. Power Module Mainframe
9. Attenuator
10. Coaxial Cable

Shaded lines identify Performance Requirement CHECK.

G1. LEFT PLUG-IN FUNCTIONS PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any change which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 2) 20
ACQUISITION AND DISPLAY
  CH 2 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... PRE TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... LEFT PLUG IN
CURSORS C2-C1
SECONDS/DIV ..... 0.1 m
STORAGE
  VIEWTIME ..... MIN
All other pushbuttons ..... Off (released)

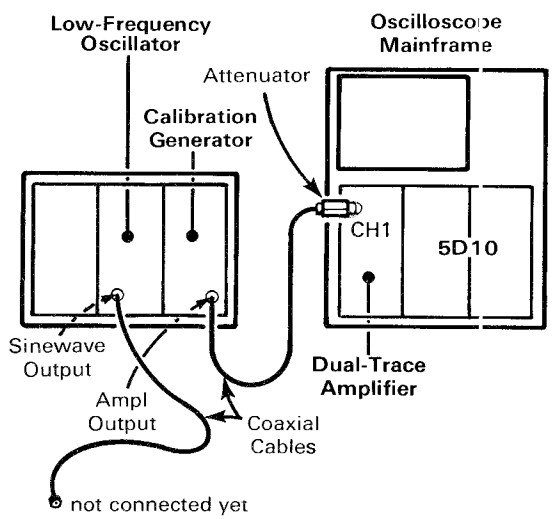
G2. CHECK LEFT PLUG-IN ACCURACY AND TRIGGERING

NOTE

First perform step G1, then proceed.

G2. SETUP CONDITIONS

5D10 Controls:
Make no changes to the control settings.



Test Equipment Controls:
Dual-Trace Amplifier
  Display ..... ON (pressed in)
  Mode CH1
  Trigger CH1
  Volts/Div (CH 1 and CH 2) 0.2
  All other pushbuttons ..... Out (released)

Low-Frequency Oscillator
  Frequency Hz 5
  Multiplier X10K
  Step Attenuator 10

Calibration Generator
  Amplitude Selector ..... Std Ampl
  Amplitude ..... 2 Volts

3697-115

a. Center the waveform on the screen, using the CH 2 POS control; then set the CH 2 VOLTS/DIV switch to LEFT PLUG-IN. Center the waveform on the screen using the dual-trace amplifier Channel 1 Position control. Do not disturb the setting of the CH 2 POS control throughout the remainder of this step.

b. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

c. Press the STORAGE SAVE button in.

d. Position cursor C1 to the top and cursor C2 to the bottom of the waveform to measure peak-to-peak amplitude.

e. **CHECK**—that the displayed signal amplitude is 7.5 divisions, within the limits of 7.275 to 7.725 divisions.

f. **CHECK**—that the CH 2 volts/division readout reads LEFT, and that the CH 2 ΔD (divisions) readout reads between 7.35 and 7.65.

g. Release the STORAGE SAVE pushbutton.

h. Set the dual-trace amplifier Mode to Dual Trace (both Ch 1 and Ch 2 buttons pressed in).

i. **CHECK**—that both Channel 1 and Channel 2 traces are displayed on the screen.

j. Disconnect Ch 1 of the dual-trace amplifier from the calibration generator and connect it to the Sine-Wave Output of the low-frequency oscillator.

k. Set the dual-trace amplifier Mode to Ch 1.

l. Set the low-frequency oscillator Var Attenuator control to display a signal amplitude of 0.4 division at 50 kHz.

m. **EXAMINE**—for a stable display with the SLOPE in both / and \ ; adjust the TRIGGERING LEVEL control as necessary.

n. Set the low-frequency oscillator to display a signal amplitude of 1 division at 250 kHz.

o. Repeat part m.

p. Set the low-frequency oscillator to display a signal amplitude of 2 divisions at 2.5 kHz.

q. Center the dual-trace amplifier Channel 1 Position Control.

r. Set the TRIGGERING SOURCE to CH 2.

s. Set the TRIGGERING COUPLING to AC.

t. If necessary, adjust the TRIGGERING LEVEL control for a stable display.

u. Position the top of the sine-wave display to the top line of the crt graticule using the dual-trace amplifier Channel 1 Position control.

v. Set the TRIGGERING COUPLING to DC.

w. **CHECK**—that the signal display is no longer stable.

H. PLOT OUTPUT

Equipment Required: (Numbers correspond to those listed in Table 5-3, Test Equipment.)

1. Oscilloscope Mainframe
2. Dual-Trace Amplifier
5. Low-Frequency Oscillator
7. Power Module Mainframe
10. Coaxial Cable
15. X-Y Recorder
16. Ramp Generator
17. Test Storage Oscilloscope
18. Cable (4 required)
19. Power Supply
20. Adapter

Shaded lines identify Performance Requirement CHECK.

H1. PLOT OUTPUT PRELIMINARY SETUP

a. Perform the Adjustment and Performance Check Initial Setup and Power-Up Sequence procedure, which appears at the beginning of Part II—Adjustment and Performance Check.

b. Refer to Section 6, Instrument Options, and to the Change Information section at the back of this manual for any change which may affect this procedure.

c. Set the 5D10 controls as follows:

VOLTS/DIV (CH 1) 1
ACQUISITION AND DISPLAY
  CH 1 ..... On (pressed in)
  JOIN DOTS ..... On (pressed in)
TRIGGERING
  POSITION ..... PRE TRIG
  SLOPE ..... / (pressed in)
  SOURCE ..... CH 1
STORAGE
  VIEWTIME ..... MIN
CURSORS ..... OFF
All other pushbuttons ..... Off (released)

d. Proceed to step 'H2. Check Plot Output' if the 5D10 plot circuitry is to be checked using an XY recorder. If an XY recorder is not available, skip step H2 and proceed to step 'H3. Alternate Check Plot Output.'

H2. CHECK PLOT OUTPUT

NOTE

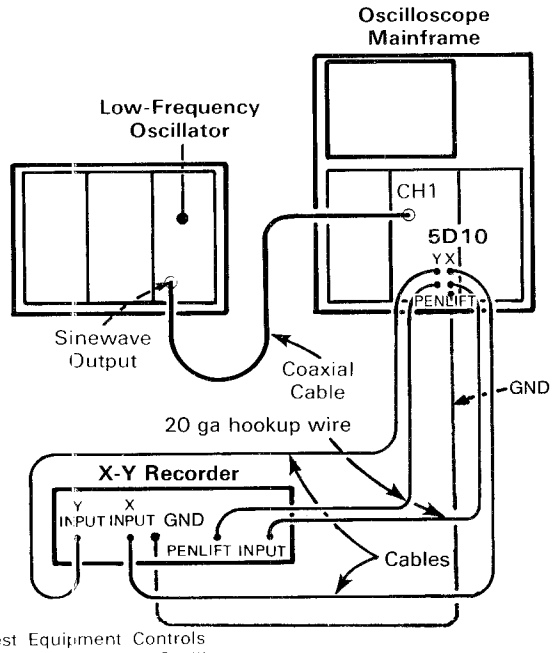
First perform step H1, then proceed.

H2. SETUP CONDITIONS

5D10 Controls:

Before starting this procedure, remove the 5D10 from the oscilloscope mainframe and position the Penlift jumper for appropriate pen-lift logic for your X-Y recorder. Refer to the H2. Penlift Jumper Location illustration on the adjacent page.

Make no changes to the control settings.



Test Equipment Controls

Low-Frequency Oscillator

Frequency Hz 1

Multiplier X1K

Step Attenuator 10

X-Y Recorder

Range

X Volts/Inch 0.5

Y Volts/Inch 0.5

3697-119A

a. Set the low-frequency oscillator Var Attenuator to display a signal amplitude of 4 divisions at 1 kHz.

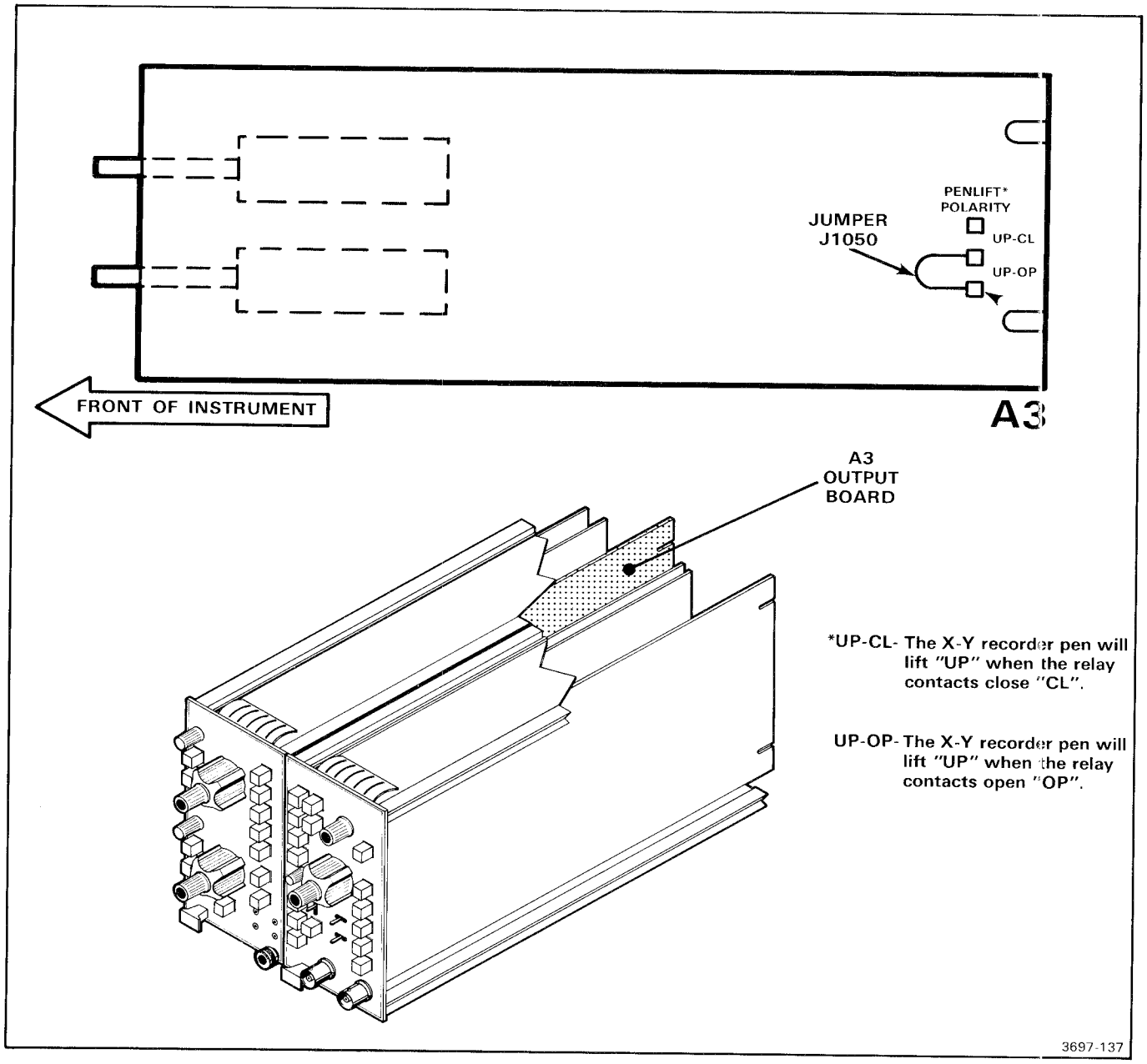
b. Set the X-Y recorder controls as recommended by the manufacturer (refer to the X-Y recorder manufacturer's instruction manual).

c. Press the STORAGE SAVE button in.

d. Press the SAVED DISPLAY PLOT button in. Notice the screen will blank until the first channel of the plot is completed, then display the message "CHANGE PEN COLOR IF DESIRED/RELEASE THEN PUSH PLOT TO CONTINUE". When PLOT is released, the next message "PUSH PLOT TO CONTINUE" appears. Press PLOT as instructed. (If, at this time, you wish not to continue, release PLOT button).

e. **CHECK**—that the X-Y recorder duplicates the display (including the graticule) and that the pen lift operates properly.

H2. PENLIFT JUMPER LOCATION



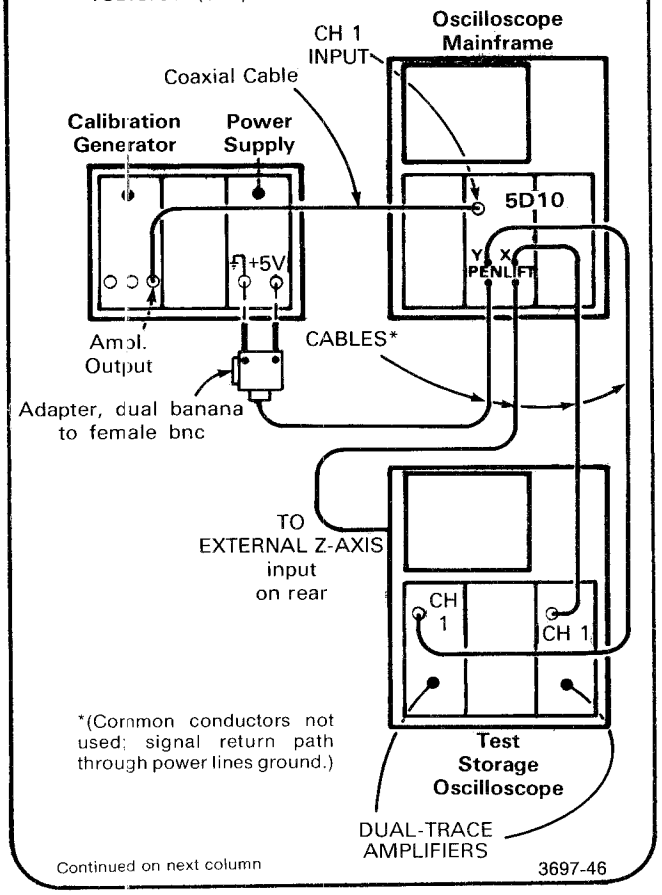
H3. ALTERNATE CHECK PLOT OUTPUT

NOTE

First perform step H1, then proceed.

H3. SETUP CONDITIONS

5D10 Controls:
Before starting this procedure, remove the 5D10 from the oscilloscope mainframe and connect the Penlift jumper (J1050) on the back of the A3 Output Board to the UP-OP position.
SECONDS/DIV ..... 0.2 m
VOLTS/DIV (CH1) 0.1



Continued on next column

H3. SETUP CONDITIONS (Cont)

Test Equipment Controls:
Oscilloscope Mainframe
Intensity ..... 2 O'clock

Dual Trace Amplifiers (both)
Display ..... On (pressed in)
Input coupling (channel 1) ..... dc (both buttons out)
Mode
Ch1 ..... On (pressed in)
Position (channel 1) ..... Centered
Ch1 Volts/Div 0.2

Calibration Generator
Amplitude Mode ..... Std Ampl
Amplitude Selector (Volts) 0.2
Variable ..... Off (button in)

Test Storage Oscilloscope
Intensity ..... 11 O'clock
Store
UPR ..... Off (button out)
LWR ..... Off (button out)
Erase/Enhance
UPR ..... Off (button out)
LWR ..... Off (button out)
Enhance Control ..... Off

a. Center the oscilloscope mainframe waveform display on the screen, and adjust the TRIGGERING LEVEL control for a stable display.

b. Press the 5D10 SAVE button in.

c. Center the test storage oscilloscope dot display on the screen (position to graticule center) using both dual-trace amplifier Channel 1 Position controls.

d. Rotate the test storage oscilloscope Intensity control fully counterclockwise.

e. Press in the test storage oscilloscope Store buttons (both UPR and LWR) and the Erase/Enhance buttons (both UPR and LWR).

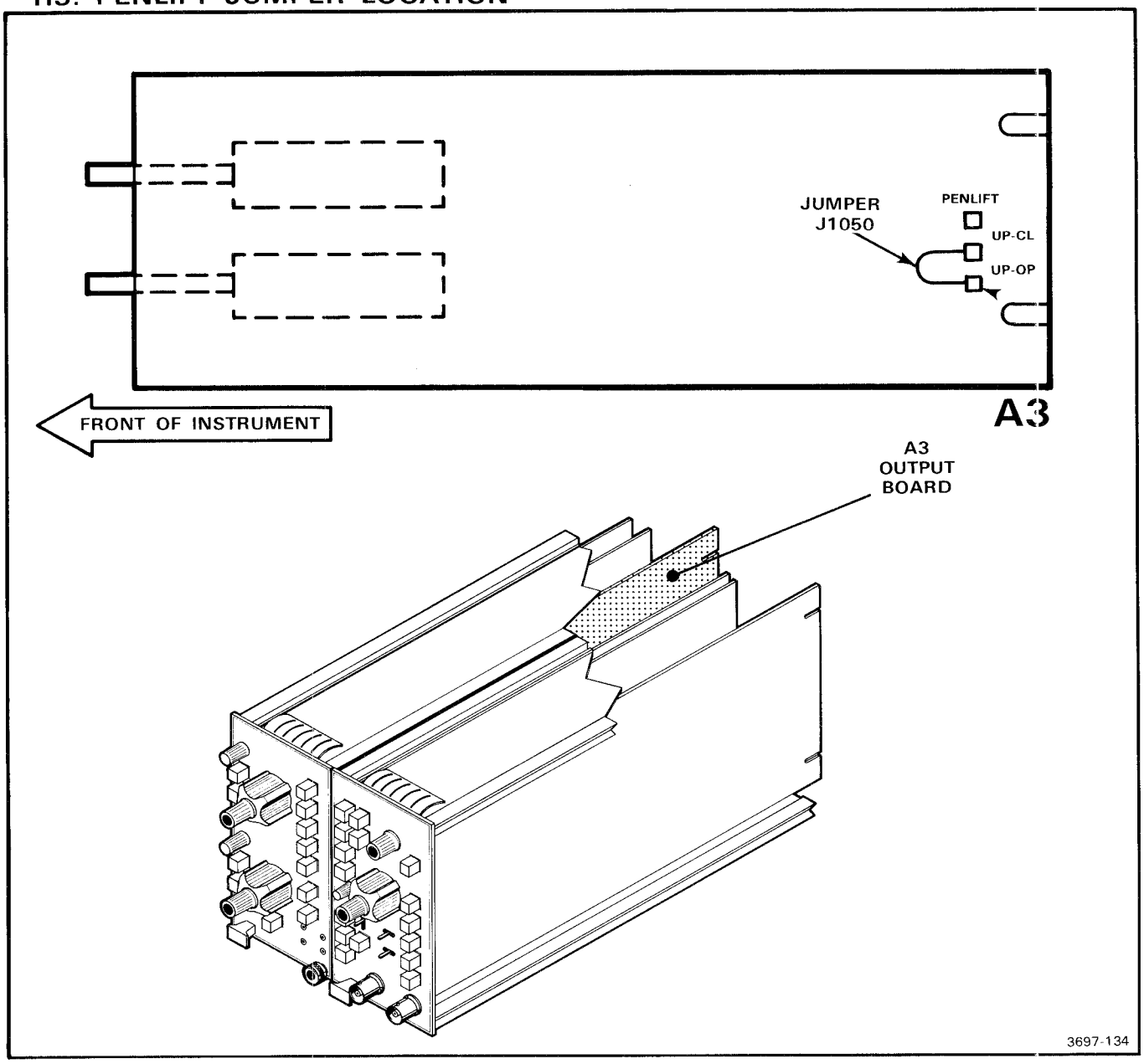
f. Press and release the test storage oscilloscope Erase button.

g. Press the 5D10 SAVED DISPLAY PLOT button in. Notice the screen will blank until the first channel of the plot is completed then display the message "CHANGE PEN COLOR IF DESIRED/RELEASE THEN PUSH PLOT TO CONTINUE". When PLOT is released, the next message "PUSH PLOT TO CONTINUE" appears. Push PLOT as instructed. (If, at this time, you wish not to continue, release PLOT button).

h. Observe test storage oscilloscope screen duplicates the oscilloscope mainframe display (including readout information) and draws a graticule pattern.

This concludes the Adjustment and Performance Check.

H3. PENLIFT JUMPER LOCATION



INSTRUMENT OPTIONS

No options were available at the time of this printing.

Information about any subsequent options will be included in the CHANGE INFORMATION section at the rear of this manual.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P.O. BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05828	GENERAL INSTRUMENT CORP ELECTRONIC SYSTEMS DIV.	600 W JOHN ST.	HICKSVILLE LI, NY 11802
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12954	SIEMENS CORPORATION, COMPONENTS GROUP	8700 E THOMAS RD, P O BOX 1390	SCOTTSDALE, AZ 85252
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
15238	ITT SEMICONDUCTORS, A DIVISION OF INTER NATIONAL TELEPHONE AND TELEGRAPH CORP.	P.O. BOX 168, 500 BROADWAY	LAWRENCE, MA 01841
15605	CUTLER-HAMMER, INC.	4201 27TH STREET	MILWAUKEE, WI 53216
17856	SILICONIX, INC.	2201 LAURELWOOD DRIVE	SANTA CLARA, CA 95054
19396	ILLINOIS TOOL WORKS, INC. PAKTRON DIV.	900 FOLLIN LANE, SE	VIENNA, VA 22180
19701	ELECTRA-MIDLAND CORP., MEPCO ELECTRA INC.	P O BOX 760	MINERAL WELLS, TX 76067
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
25403	AMPEREX ELECTRONIC CORP., SEMICONDUCTOR AND MICROCIRCUITS DIV.	PROVIDENCE PIKE	SLATERSVILLE, RI 02876
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34649	INTEL CORP.	3065 BOWERS AVE.	SANTA CLARA, CA 95051
50157	MIDWEST COMPONENTS INC.	P. O. BOX 787 1981 PORT CITY BLVD.	MUSKEGON, MI 49443
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52043	GENERAL TELEPHONE AND ELECTRONICS CORP	730 THIRD AVE	NEW YORK, NY 10017
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
56699	MEPCO/ELECTRA INC.	6071 ST. ANDREWS RD.	COLUMBIA, SC 29210
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
57924	BOURNS INC NETWORKS DIV 12155	MAGNOLIA AVE	RIVERSIDE, CA 92503
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO, TX 79915
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
71590	CENTRALAB ELECTRONICS, DIV. OF GLOBE-UNION, INC.	P O BOX 858	FORT DODGE, IA 50501
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80031	ELECTRA-MIDLAND CORP., MEPCO DIV.	22 COLUMBIA ROAD	MORRISTOWN, NJ 07960
81483	INTERNATIONAL RECTIFIER CORP.	9220 SUNSET BLVD.	LOS ANGELES, CA 90069
84411	TRW ELECTRONIC COMPONENTS, TRW CAPACITORS	112 W. FIRST ST.	OGALLALA, NE 69153
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
95348	GORDOS CORPORATION	250 GLENWOOD AVENUE	BLOOMFIELD, NJ 07003
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				ASSEMBLIES		
A1	670-7413-00	B010100	B010319	CKT BOARD ASSY:AMPLIFIER	80009	670-7413-00
A1	670-7413-01	B010320	B020099	CKT BOARD ASSY:AMPLIFIER	80009	670-7413-01
A1	670-7413-02	B020100		CKT BOARD ASSY:AMPLIFIER	80009	670-7413-02
A2	670-7414-00	B010100	B020099	CKT BOARD ASSY:PROCESSOR	80009	670-7414-00
A2	670-7414-01	B020100		CKT BOARD ASSY:PROCESSOR	80009	670-7414-01
A3	670-7415-00			CKT BOARD ASSY:OUTPUT	80009	670-7415-00
A4	670-7416-00			CKT BOARD ASSY:DATA	80009	670-7416-00
A5	670-7417-00			CKT BOARD ASSY:CONTROL	80009	670-7417-00
A6	670-7418-01			CKT BOARD ASSY:TRIGGER	80009	670-7418-01
A1	670-7413-00	B010100	B010319	CKT BOARD ASSY:AMPLIFIER	80009	670-7413-00
A1	670-7413-01	B010320	B020099	CKT BOARD ASSY:AMPLIFIER	80009	670-7413-01
A1	670-7413-02	B020100		CKT BOARD ASSY:AMPLIFIER	80009	670-7413-02
A1C140	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020NFL
A1C141	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C230	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C337	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C340	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C403	283-0602-00			CAP.,FXD,MICA D:53PF,5%,300V	00853	D155E53OJ0
A1C410	283-0602-00			CAP.,FXD,MICA D:53PF,5%,300V	00853	D155E53OJ0
A1C426	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C427	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C430	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C432	290-0527-00			CAP.,FXD,ELCTLT:15UF,20%,20V	90201	TDC156M020NFL
A1C526	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035B3C0G330
A1C601	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035B3C0G330
A1C636	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	173D105X0050V
A1C640	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C641	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A1C647	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	173D105X0050V
A1C722	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A1C732	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A1C740	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A1C747	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	173D105X0050V
A1C800	290-0167-00			CAP.,FXD,ELCTLT:10UF,20%,15V	56289	150D106X0015B2
A1C806	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A1C824	281-0797-00			CAP.,FXD,CER DI:15PF,10%,100V	04222	MA106A150KAA
A1C830	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C900	290-0177-00			CAP.,FXD,ELCTLT:1UF,20%,50V	56289	173D105X0050V
A1C947	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1000	281-0178-00			CAP.,VAR,PLSTC:1-3.5PF,500V	80031	2805D013R5BH02F0
A1C1002	281-0182-00			CAP.,VAR,PLSTC:1.8-10PF,500V	80031	2805D1R810BH02F0
A1C1020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1021	283-0001-00			CAP.,FXD,CER DI:0.005UF,+100-0%,500V	59821	2DDH61L502P
A1C1030	281-0178-00			CAP.,VAR,PLSTC:1-3.5PF,500V	80031	2805D013R5BH02F0
A1C1032	281-0182-00			CAP.,VAR,PLSTC:1.8-10PF,500V	80031	2805D1R810BH02F0
A1C1044	283-0001-00			CAP.,FXD,CER DI:0.005UF,+100-0%,500V	59821	2DDH61L502P
A1C1120	281-0182-00			CAP.,VAR,PLSTC:1.8-10PF,500V	80031	2805D1R810BH02F0
A1C1121	283-0691-00			CAP.,FXD,MICA D:650PF,1%,300V	00853	D153F651F0
A1C1140	281-0182-00			CAP.,VAR,PLSTC:1.8-10PF,500V	80031	2805D1R810BH02F0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1C1200	281-0874-00			CAP.,FXD,CER DI:10F,5%,500V	04222	MA407A100JAA
A1C1201	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1220	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1221	285-1124-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	19396	PP721E223M
A1C1230	281-0874-00			CAP.,FXD,CER DI:10F,5%,500V	04222	MA407A100JAA
A1C1231	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1240	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C1241	285-1124-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	19396	PP721E223M
A1C1242	283-0691-00			CAP.,FXD,MICA D:650PF,1%,300V	00853	D153F651F0
A1CR123	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR130	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR131	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR133	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR135	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR230	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR231	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR233	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR235	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR237	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR239	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR323	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR324	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR325	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR326	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR342	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR410	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	02735	CA3039
A1CR420	156-0106-00			MICROCIRCUIT,LI:MONOLITHIC,6-DIODE ARRAY	02735	CA3039
A1CR434	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR440	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR505	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR507	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR510	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR520	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR523	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR542	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR601	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR604	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR605	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR607	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR622	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR623	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR625	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR630	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR640	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR701	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR745	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR806	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR820	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR822	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR828	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR840	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR842	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR1027	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK
A1CR1041	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A1CR1048	152-0246-00			SEMICOND DEVICE:SW,SI,40V,200MA	14433	WG1537TK

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A1L342	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A1L441	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A1L541	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A1L542	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A1Q110	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q121	156-0048-02			MICROCIRCUIT,LI:5 XSTR ARRAY	80009	156-0048-02
A1Q210	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q211	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q220	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q221	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q222	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q223	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q224	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q225	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q226	156-0048-02			MICROCIRCUIT,LI:5 XSTR ARRAY	80009	156-0048-02
A1Q310	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q311	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q312	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q320	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q321	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q322	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q323	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q324	151-0192-00			TRANSISTOR:SELECTED	04713	SPS8801
A1Q325	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q330	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q331	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q332	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q400	151-0188-00	B010100	B020099	TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A1Q400	151-0221-00	B020100		TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q401	151-0188-00	B010100	B020099	TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A1Q401	151-0221-00	B020100		TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q410	151-1049-00			TRANSISTOR:SILICON,JFE,N -CHANNEL,DUAL	17856	DN872
A1Q420	151-1049-00			TRANSISTOR:SILICON,JFE,N -CHANNEL,DUAL	17856	DN872
A1Q424	151-0188-00	B010100	B020099	TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A1Q424	151-0221-00	B020100		TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q426	151-0188-00	B010100	B020099	TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A1Q426	151-0221-00	B020100		TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q430	151-0190-00	B010100	B010182	TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q430	151-0207-00	B010183		TRANSISTOR:SILICON,NPN	03508	X32D6191
A1Q436	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q528	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q536	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q540	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q541	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q610	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q625	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q630	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q635	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q710	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A1Q721	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q722	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q723	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q730	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q731	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928

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A1Q732	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q806	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A1Q830	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q1010	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A1Q1020	151-1049-00			TRANSISTOR:SILICON,JFE,N -CHANNEL,DUAL	17856	DN872
A1Q1040	151-1049-00			TRANSISTOR:SILICON,JFE,N -CHANNEL,DUAL	17856	DN872
A1R100	321-0145-00			RES.,FXD,FILM:316 OHM,1%,0.125W	91637	CMF55116G316R0F
A1R101	321-0145-00			RES.,FXD,FILM:316 OHM,1%,0.125W	91637	CMF55116G316R0F
A1R102	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A1R103	321-0720-03			RES.,FXD,FILM:60K OHM,0.25%,0.125W	91637	MFF1816D60001C
A1R104	321-0603-00			RES.,FXD,FILM:15K OHM,0.25%,0.125W	91637	MFF1816D15001C
A1R105	321-0604-00			RES.,FXD,FILM:30K OHM,0.25%,0.125W	91637	MFF1816D30001C
A1R106	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	CMF55116G30101F
A1R107	321-0226-00			RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A1R110	321-0364-00			RES.,FXD,FILM:60.4K OHM,1%,0.125W	91637	CMF55116G60401F
A1R120	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R121	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A1R122	307-0503-00			RES NTWK,THK FI:(9)510 OHM,20%,0.125W	91637	MSP10A01-511G
A1R123	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R124	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	57668	NTR25J-E620E
A1R140	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R200	321-0277-03			RES.,FXD,FILM:7.5K OHM,0.25%,0.125W	24546	NC55C7501C
A1R201	321-0604-00			RES.,FXD,FILM:30K OHM,0.25%,0.125W	91637	MFF1816D30001C
A1R202	321-0226-00			RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A1R204	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	57668	NTR25J-E04K7
A1R205	321-0116-00			RES.,FXD,FILM:158 OHM,1%,0.125W	91637	CMF55116G158R0F
A1R206	321-0116-00			RES.,FXD,FILM:158 OHM,1%,0.125W	91637	CMF55116G158R0F
A1R239	321-0116-00			RES.,FXD,FILM:158 OHM,1%,0.125W	91637	CMF55116G158R0F
A1R300	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A1R301	321-0118-04			RES.,FXD,FILM:165 OHM,0.1%,0.125W	91637	MFF1816D165R0B
A1R303	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A1R304	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A1R305	321-0118-04			RES.,FXD,FILM:165 OHM,0.1%,0.125W	91637	MFF1816D165R0B
A1R308	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A1R331	321-0116-00			RES.,FXD,FILM:158 OHM,1%,0.125W	91637	CMF55116G158R0F
A1R340	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R341	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A1R342	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R349	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R401	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	57668	NTR25J-E 1K6
A1R402	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A1R403	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R407	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R424	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R425	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	57668	NTR25J-E24K0
A1R426	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	57668	NTR25J-E 1K6
A1R427	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A1R432	321-0170-00			RES.,FXD,FILM:576 OHM,1%,0.125W	91637	CMF55116G576R0F
A1R433	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R434	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R439	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A1R441	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A1R500	311-1298-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	01121	W-7909
A1R505	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	57668	NTRERJ-E 560E

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A1R507	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A1R510	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A1R520	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A1R523	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	57668	NTRERJ-E 560E
A1R524	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R525	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A1R527	321-1723-07			RES.,FXD,FILM:3.15K OHM,0.1%,0.125W	24546	NE55.3151.B
A1R528	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF 816G75000F
A1R529	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A1R532	311-1298-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	01121	W-7909
A1R536	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R537	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF 816G20001F
A1R538	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF 816G10001F
A1R539	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	57668	NTR25J-E 6K2
A1R543	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R544	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF 816G10001F
A1R545	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF 816G20001F
A1R546	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R547	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A1R548	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R602	321-1723-07			RES.,FXD,FILM:3.15K OHM,0.1%,0.125W	24546	NE55.3151.B
A1R605	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A1R607	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A1R609	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF 816G75000F
A1R610	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A1R620	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A1R621	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R624	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A1R626	321-0274-00	B010100	B020099	RES.,FXD,FILM:6.98K OHM,1%,0.125W	91637	CMF55116G69800F
A1R626	321-0271-00	B020100		RES.,FXD,FILM:6.49K OHM,1%,0.125W	91637	MFF1816G64900F
A1R626	321-0272-00	B020100		RES.,FXD,FILM:6.65K OHM,1%,0.125W	91637	MFF1816G66500F
A1R626	321-0273-00	B020100		RES.,FXD,FILM:6.81K OHM,1%,0.125W	91637	MFF1816G68100F
A1R626	321-0275-00	B020100		RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A1R626	321-0276-00	B020100		RES.,FXD,FILM:7.32K OHM,1%,0.125W	91637	MFF1816G73200F
A1R626	321-0277-00	B020100		RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A1R627	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R628	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A1R630	311-1224-00			RES.,VAR,NONWIR:500 OHM,20%,0.50W	32997	3386F-T04-501
A1R631	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A1R632	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R635	321-0217-00			RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	CMF55116G17800F
A1R639	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A1R641	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	CMF55116G11300F
A1R642	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	CMF55116G11300F
A1R702	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A1R704	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A1R705	321-0402-00			RES.,FXD,FILM:150K OHM,1%,0.125W	24546	NA55D1503F
A1R710	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R720	321-0217-00			RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	CMF55116G17800F
A1R721	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A1R722	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	CMF55116G11300F
A1R732	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A1R735	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	CMF55116G11300F
A1R742	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0

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A1R745	321-0320-00			RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F
A1R802	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A1R805	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R820	321-0320-00			RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F
A1R821	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R822	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R823	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A1R824	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R826	321-0320-00			RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F
A1R827	321-0774-03			RES.,FXD,FILM:4.5K OHM,0.25%,0.125W	91637	MFF1816D45000C
A1R829	321-0612-03			RES.,FXD,FILM:500 OHM,0.25%,0.125W	91637	MFF1816D500R0C
A1R830	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R832	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	57668	NTR25J-E150K
A1R833	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R838	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R839	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A1R840	321-0320-00			RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F
A1R841	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R842	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A1R843	321-0774-03			RES.,FXD,FILM:4.5K OHM,0.25%,0.125W	91637	MFF1816D45000C
A1R845	321-0612-03			RES.,FXD,FILM:500 OHM,0.25%,0.125W	91637	MFF1816D500R0C
A1R847	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R900	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	57668	NTR25J-E03K9
A1R920	311-1222-00			RES.,VAR,NONWIR:100 OHM,20%,0.50W	32997	3386F-T04-101
A1R921	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R930	321-0612-03			RES.,FXD,FILM:500 OHM,0.25%,0.125W	91637	MFF1816D500R0C
A1R932	321-0774-03			RES.,FXD,FILM:4.5K OHM,0.25%,0.125W	91637	MFF1816D45000C
A1R940	311-1222-00			RES.,VAR,NONWIR:100 OHM,20%,0.50W	32997	3386F-T04-101
A1R941	321-0068-00			RES.,FXD,FILM:49.9 OHM,1%,0.125W	91637	CMF55116G49R90F
A1R943	321-0612-03			RES.,FXD,FILM:500 OHM,0.25%,0.125W	91637	MFF1816D500R0C
A1R945	321-0774-03			RES.,FXD,FILM:4.5K OHM,0.25%,0.125W	91637	MFF1816D45000C
A1R949	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R1000	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A1R1001	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	57668	NTR25J-E150K
A1R1020	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A1R1021	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A1R1022	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R1026	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R1040	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R1044	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A1R1047	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A1R1120	321-0289-03			RES.,FXD,FILM:10K OHM,0.25%,0.125W	91637	MFF1816D10001C
A1R1122	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A1R1140	321-0289-03			RES.,FXD,FILM:10K OHM,0.25%,0.125W	91637	MFF1816D10001C
A1R1142	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	57668	NTR25J-E 10E0
A1R1225	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A1R1226	322-0624-03			RES.,FXD,FILM:990K OHM,0.25%,0.25W	91637	MFF1421D99002C
A1R1240	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A1R1241	322-0624-03			RES.,FXD,FILM:990K OHM,0.25%,0.25W	91637	MFF1421D99002C
A1RT200	307-0124-00			RES.,THERMAL:5K OHM,10%	50157	1D1618
A1S610	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A1S639	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A1S740	260-1209-00			SWITCH,PUSH:4PDT,1A,25VDC	31918	601347
A1S1200	260-1353-01			SWITCH,PUSH:DPDT,2 STA,NON-SHORTING	80009	260-1353-01
A1S1230	260-1353-01			SWITCH,PUSH:DPDT,2 STA,NON-SHORTING	80009	260-1353-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U130	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A1U135	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A1U145	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A1U230	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A1U240	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A1U245	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A1U330	156-1324-00			MICROCIRCUIT,LI:COMPARATOR	27014	LM361N/A+
A1U510	156-1149-01	B010100	B010319	MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A1U510	156-1156-01	B010320		MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A1U520	156-1149-01	B010100	B010319	MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A1U520	156-1156-01	B010320		MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A1U640	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A1U710	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A1U720	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A1VR541	152-0304-00			SEMICOND DEVICE:ZENER,0.4W,20V,5%	15238	Z5411
A1VR932	152-0149-00			SEMICOND DEVICE:ZENER,0.4W,10V,5%	04713	SZG35009K3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	670-7414-00	B010100	B020099	CKT BOARD ASSY:PROCESSOR	80009	670-7414-00
A2	670-7414-01	B020100		CKT BOARD ASSY:PROCESSOR	80009	670-7414-01
A2C121	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C130	290-0136-00			CAP.,FXD,ELCTLT:2.2UF,20%,20V	56289	162D225X0020CD2
A2C133	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A2C210	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C211	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C301	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2C330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A2CR131	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A2Q152	151-0190-02			TRANSISTOR:SILICON,NPN	04713	SM7706
A2Q155	151-0190-02			TRANSISTOR:SILICON,NPN	04713	SM7706
A2R130	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A2R133	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A2R221	307-0637-00			RES NTWK,FXD,FI:5,2K OHM,2%,0.125W	01121	206A202
A2R251	315-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.25W	57668	NTR25J-E 360E
A2R255	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A2R257	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A2R340	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A2U101	156-1461-00			MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2U111	156-1461-00			MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A2U121	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A2U123	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A2U130	156-0480-02	B010100	B020099	MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A2U130	156-0382-02	B020100		MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U201	160-1475-01	B010100	B020099	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1475-01
A2U201	160-1704-00	B020100		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1704-00
A2U213	160-1330-01	B010100	B020099	MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-1330-01
A2U213	160-1705-00	B020100		MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1705-00
A2U223	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05
A2U230	156-1088-00	B010100	B020099	MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	34649	D8085AH
A2U230	156-1088-03	B020100		MICROCIRCUIT,DI:8 BIT MICROPROCESSOR	34649	D8085AH
A2U322	156-0567-02	B010100	B020099	MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG FF	01295	SN74LS113NP3
A2U322	156-0385-02	B020100		MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2VR251	152-0744-00			SEMICOND DEVICE:ZEN,SI,3.6V,5%,0.4W	04713	1N747A

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	670-7415-00			CKT BOARD ASSY:OUTPUT	80009	670-7415-00
A3C200	281-0799-00			CAP.,FXD,CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C210	295-0195-00			CAP SET,MATCHED:2EA,1.0UF,0.001UF,3.0%	80009	295-0195-00
A3C230	285-0659-00			CAP.,FXD,PLSTC:0.001UF,10%,100V	84411	TEK24-10291
A3C240	285-0659-00			CAP.,FXD,PLSTC:0.001UF,10%,100V	84411	TEK24-10291
A3C300	295-0195-00			CAP SET,MATCHED:2EA,1.0UF,0.001UF,3.0%	80009	295-0195-00
A3C310	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C311	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C320	281-0558-00			CAP.,FXD,CER DI:18PF,10%,500V	59660	301-000C0G0180K
A3C326	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C331	281-0799-00			CAP.,FXD,CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C332	281-0558-00			CAP.,FXD,CER DI:18PF,10%,500V	59660	301-000C0G0180K
A3C340	295-0195-00			CAP SET,MATCHED:2EA,1.0UF,0.001UF,3.0%	80009	295-0195-00
A3C349	285-1189-00			CAP.,FXD,MTLZD:0.1UF,5%,100V	56699	719A1CA104PJ101S
A3C350	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A3C351	285-1189-00			CAP.,FXD,MTLZD:0.1UF,5%,100V	56699	719A1CA104PJ101S
A3C405	283-0629-00			CAP.,FXD,MICA D:62PF,1%,500V	00853	D105E620F0
A3C440	295-0195-00			CAP SET,MATCHED:2EA,1.0UF,0.001UF,3.0%	80009	295-0195-00
A3C450	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C451	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A3C452	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C510	281-0799-00			CAP.,FXD,CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C515	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C520	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C521	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C530	281-0799-00			CAP.,FXD,CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C531	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	96733	R2737
A3C541	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	MA101A470KAA
A3C543	281-0785-00			CAP.,FXD,CER DI:68PF,10%,100V	04222	MA101A680KAA
A3C550	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	96733	R2737
A3C630	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C720	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C810	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C830	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C950	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C951	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C1000	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3C1030	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A3C1050	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A3CR100	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3CR200	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3CR240	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3CR305	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3CR427	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3CR430	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A3K230	148-0076-00			RELAY,REED:1 FORM A,5V,0.25A,100V	95348	F81-1447
A3L950	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A3Q225	151-1022-00			TRANSISTOR:FET,N-CHAN,SI,F1782,T0-18	17856	FN1234
A3Q226	151-1022-00			TRANSISTOR:FET,N-CHAN,SI,F1782,T0-18	17856	FN1234
A3Q230	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A3Q310	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A3Q311	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A3Q325	151-1022-00			TRANSISTOR:FET,N-CHAN,SI,F1782,T0-18	17856	FN1234

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3Q326	151-1022-00			TRANSISTOR:FET,N-CHAN,SI,F1782,T0-18	17856	FN1234
A3Q1050	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A3R100	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A3R140	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A3R141	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A3R150	311-1243-00			RES.,VAR,NONWIR:500K OHM,10%,0.50W	73138	72-34-0
A3R151	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A3R152	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	57668	NTR25J-E130K
A3R153	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	57668	NTR25J-E130K
A3R154	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A3R155	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	19701	5043CX510K0J
A3R200	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A3R220	321-0222-07			RES.,FXD,FILM:2K OHM,0.1%,0.125W	91637	CMF55116C20000B
A3R221	321-0249-07			RES.,FXD,FILM:3.83K OHM,0.1%,0.125W	24546	NE55E383
A3R222	321-0993-07			RES.,FXD,FILM:90K OHM,0.1%,0.125W	91637	MFF1816C90001B
A3R223	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A3R230	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A3R231	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A3R239	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A3R240	321-0210-07			RES.,FXD,FILM:1.5K OHM,0.1%,0.125W	24546	NE55E1501B
A3R241	321-0612-07			RES.,FXD,FILM:500 OHM,0.1%,0.125W	91637	MFF1816C500R0B
A3R242	321-0210-07			RES.,FXD,FILM:1.5K OHM,0.1%,0.125W	24546	NE55E1501B
A3R250	321-0612-07			RES.,FXD,FILM:500 OHM,0.1%,0.125W	91637	MFF1816C500R0B
A3R251	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	19701	5043CX510K0J
A3R301	321-0303-09			RES.,FXD,FILM:14.0K OHM,1%,0.125W	24546	NE55E1402F
A3R302	321-0603-07			RES.,FXD,FILM:15K OHM,0.1%,0.125W	91637	MFF1816C15001B
A3R304	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	57668	NTR25J-E03K3
A3R320	321-0926-07			RES.,FXD,FILM:4K OHM,0.1%,0.125W	91637	MFF1816C40000B
A3R324	321-0993-07			RES.,FXD,FILM:90K OHM,0.1%,0.125W	91637	MFF1816C90001B
A3R325	321-0222-07			RES.,FXD,FILM:2K OHM,0.1%,0.125W	91637	CMF55116C20000B
A3R326	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A3R327	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A3R350	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A3R351	311-1918-00			RES.,VAR,NONWIR:2K OHM,10%,0.50W	73138	72-199-0
A3R352	311-1918-00			RES.,VAR,NONWIR:2K OHM,10%,0.50W	73138	72-199-0
A3R400	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	57668	NTR25J-E02K2
A3R401	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A3R402	315-0304-00			RES.,FXD,CMPSN:300K OHM,5%,0.25W	57668	NTR25J-E300K
A3R403	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A3R404	315-0624-00			RES.,FXD,CMPSN:620K OHM,5%,0.25W	57668	NTR25J-E 620K
A3R405	321-0303-09			RES.,FXD,FILM:14.0K OHM,1%,0.125W	24546	NE55E1402F
A3R406	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A3R407	321-0193-07			RES.,FXD,FILM:1K OHM,0.1%,0.125W	91637	MFF1816C10000B
A3R408	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	57668	NTR25J-E130K
A3R411	315-0564-00			RES.,FXD,CMPSN:560K OHM,5%,0.25W	57668	NTR25J-E 560K
A3R425	321-0249-07			RES.,FXD,FILM:3.83K OHM,0.1%,0.125W	24546	NE55E383
A3R426	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R427	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K
A3R428	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	57668	NTR25J-E07K5
A3R431	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R432	321-0926-07			RES.,FXD,FILM:4K OHM,0.1%,0.125W	91637	MFF1816C40000B
A3R451	311-1247-00			RES.,VAR,NONWIR:1M OHM,10%,0.5OW	73138	72-35-0
A3R452	311-1247-00			RES.,VAR,NONWIR:1M OHM,10%,0.5OW	73138	72-35-0
A3R500	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	57668	NTR25J-E 15K

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A3R501	321-0685-07			RES.,FXD,FILM:30K OHM,0.1%,0.125W	91637	MFF1816C30001B
A3R502	321-0382-00			RES.,FXD,FILM:93.1K OHM,1%,0.125W	91637	MFF1816G93101F
A3R503	321-0382-00			RES.,FXD,FILM:93.1K OHM,1%,0.125W	91637	MFF1816G93101F
A3R504	315-0274-00			RES.,FXD,CMPSN:270K OHM,5%,0.25W	57668	NTR25J-E270K
A3R505	315-0274-00			RES.,FXD,CMPSN:270K OHM,5%,0.25W	57668	NTR25J-E270K
A3R506	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	57668	NTR25J-E68K0
A3R507	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	57668	NTR25J-E130K
A3R508	307-0597-00			RES NTWK,FXD,FI:7,6.8K OHM,2%,1.0W	01121	208A682
A3R509	315-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.25W	57668	NTR25J-E 3K6
A3R510	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A3R512	321-0433-00			RES.,FXD,FILM:316K OHM,1%,0.125W	91637	MFF1816G31602F
A3R513	321-0433-00			RES.,FXD,FILM:316K OHM,1%,0.125W	91637	MFF1816G31602F
A3R520	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R521	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A3R522	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A3R530	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R531	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R532	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A3R533	321-0222-07			RES.,FXD,FILM:2K OHM,0.1%,0.125W	91637	CMF55116C20000B
A3R540	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R541	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R542	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R543	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A3R551	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A3R552	311-1245-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	73138	72-28-0
A3R553	321-0207-07			RES.,FXD,FILM:1.4K OHM,0.1%,0.125W	24546	NE55E140LB
A3R630	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A3R640	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A3R650	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R710	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A3R711	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A3R730	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A3R830	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A3R950	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A3R951	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A3S100	260-1424-01			SWITCH,PUSH:5 STA,2 POLE INTERLOCK	59821	2KBC050000684
A3S130	260-2103-00			SWITCH,PUSH:2 BUTTON,2 POLE,PLOT	71590	2KCE0200001856
A3U230	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A3U330	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A3U350	156-0644-03			MICROCIRCUIT,DI:QUAD BILATERAL SW,BURN-IN	80009	156-0644-03
A3U410	156-1255-01			MICROCIRCUIT,LI:D/A CONVERTER,BURN-IN	04713	DAC-08HQDS
A3U425	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A3U430	156-1156-01			MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A3U435	156-0644-03			MICROCIRCUIT,DI:QUAD BILATERAL SW,BURN-IN	80009	156-0644-03
A3U440	156-0644-03			MICROCIRCUIT,DI:QUAD BILATERAL SW,BURN-IN	80009	156-0644-03
A3U445	156-1156-01			MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A3U450	156-1156-01			MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A3U520	156-0927-02			MICROCIRCUIT,LI:DIGITAL/ANALOG CONVERTER	04713	MC3410CLD
A3U530	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A3U550	156-1156-01			MICROCIRCUIT,LI:OPERATIONAL AMPL	27014	LF356N/A+
A3U600	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74_S273NP3
A3U610	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A3U620	156-0349-06			MICROCIRCUIT,DI:QUAD 2 INP NOR GATE,CHK	80009	156-0349-06
A3U630	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74_S257(NP3)

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A3U640	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U650	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A3U700	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U710	156-0153-02			MICROCIRCUIT,DI:HEX INVERTER BUFFER	27014	DM7406N
A3U720	156-1388-00			MICROCIRCUIT,DI:QUAD 2-INP MUX W/STOR,SCRN	04713	SN74LS399
A3U730	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U740	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U800	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A3U810	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A3U820	156-1388-00			MICROCIRCUIT,DI:QUAD 2-INP MUX W/STOR,SCRN	04713	SN74LS399
A3U830	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U840	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U900	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A3U910	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A3U920	156-1388-00			MICROCIRCUIT,DI:QUAD 2-INP MUX W/STOR,SCRN	04713	SN74LS399
A3U930	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245 N3ORJ4
A3U940	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A3U1010	156-1461-00			MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A3U1020	156-1461-00			MICROCIRCUIT,DI:1024 X 4 SRAM	34649	D2114AL-4/S7127
A3VR130	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A3VR131	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A3VR140	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A3VR224	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	TD3810983
A3VR250	152-0279-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZG35010RL
A3W30	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

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A4	670-7416-00			CKT BOARD ASSY:DATA	80009	670-7416-00
A4C310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C340	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C350	281-0811-00	B020100		CAP.,FXD,CER DI:10PF,10%,100V	96733	R29-1
A4C420	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C510	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C530	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C620	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C710	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C730	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C750	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C820	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4C840	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A4DS140	150-1083-00			LAMP,LED RDOUT:RED,10 ELEM BAR GRAPH	50434	HDSP-4820
A4R107	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A4R108	307-0540-00			RES,NTWK,FXD,FI:(5) 1K OHM,10%,0.7W	57924	4306R-101-102
A4R160	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A4R350	315-0511-00	B020100		RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A4R450	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A4R830	307-0475-00			RES,NTWK,FXD,FI:10K OHM,(15)RES,DIP 16 LD	32997	4116R-002-103
A4U210	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U220	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U230	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U240	156-0567-02			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE-TRIG FF	01295	SN74LS113NP3
A4U250	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A4U260	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A4U310	156-0452-02			MICROCIRCUIT,DI:4-WIDE,2-INP AOI,SCREENED	01295	SN74LS54 NP3 JP4
A4U320	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A4U330	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A4U340	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A4U350	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U360	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U410	156-0989-02			MICROCIRCUIT,DI:4 X 4 RGTR FILE,BURN-IN	04713	SN74LS670NDS
A4U420	156-0989-02			MICROCIRCUIT,DI:4 X 4 RGTR FILE,BURN-IN	04713	SN74LS670NDS
A4U430	156-0989-02			MICROCIRCUIT,DI:4 X 4 RGTR FILE,BURN-IN	04713	SN74LS670NDS
A4U440	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A4U450	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A4U460	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A4U510	156-0679-01			MICROCIRCUIT,DI:4 BIT BINARY ADDER,BURN-IN	04713	SN74LS283NDS
A4U520	156-0679-01			MICROCIRCUIT,DI:4 BIT BINARY ADDER,BURN-IN	04713	SN74LS283NDS
A4U530	156-0679-01			MICROCIRCUIT,DI:4 BIT BINARY ADDER,BURN-IN	04713	SN74LS283NDS
A4U540	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U550	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A4U560	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A4U610	156-1395-01			MICROCIRCUIT,DI:QUAD 2 LINE DATA SEL/MUX	01295	SN74LS158NP3 JP4
A4U620	156-1395-01			MICROCIRCUIT,DI:QUAD 2 LINE DATA SEL/MUX	01295	SN74LS158NP3 JP4
A4U630	156-1395-01			MICROCIRCUIT,DI:QUAD 2 LINE DATA SEL/MUX	01295	SN74LS158NP3 JP4
A4U640	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A4U650	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A4U720	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A4U730	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A4U740	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174

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A4U750	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A4U810	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A4U820	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A4U840	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A4U850	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U900	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5	670-7417-00			CKT BOARD ASSY:CONTROL	80009	670-7417-00
A5C100	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C120	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C330	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C400	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C500	281-0861-00			CAP.,FXD,CER DI:270 PF,5%,50V	51642	G17: 0-050-NP0-27
A5C610	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C730	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C820	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5C821	290-0536-00			CAP.,FXD,ELCTLT:10UF,20%,25V	90201	TDC106M025FL
A5C900	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A5CR809	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP)263 (1N4152)
A5CR810	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP)263 (1N4152)
A5CR811	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP)263 (1N4152)
A5Q131	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS'969
A5Q820	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A5Q822	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS'969
A5Q910	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS'969
A5Q911	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A5R100	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R110	307-0542-00			RES,NTWK,FXD,FI:10K OHM,5%,0.125W	01121	106A103
A5R130	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R131	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R132	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R133	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A5R134	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R200	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R500	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A5R610	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R720	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A5R800	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A5R810	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A5R811	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R812	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A5R813	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A5R820	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A5R821	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A5R822	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	57668	NTR25J-E75K0
A5R823	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R824	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A5R825	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	57668	NTR25J-E 510E
A5R826	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A5R830	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A5R910	311-1977-00			RES.,VAR,NONWIR:PNL,10K OHM,20%,0.50W	12697	CM47 733
A5S900	260-1381-00			SWITCH,PUSH:4 STA,NON-SHORT,INTLK	71590	2KBC040000-618
A5S901	260-1570-01			SWITCH,PUSH:2 BTN,2 POLE,PULSE	80009	260-1570-01
A5S910	311-1977-00			RES.,VAR,NONWIR:PNL,10K OHM,20%,0.50W	12697	CM47 733
A5S920	260-1448-00			SWITCH,PUSH:3 STA,NON-SHORT	59821	2KBE030000-638
A5S935	260-1208-00			SWITCH,PUSH:DPDT,28VDC,PUSH-PUSH	31918	ORDER BY DESCR
A5S1020	260-2106-00			SWITCH,TOGGLE:SPDT,0.4VA,20V,ON-OFF-ON	15605	A12132Y9ABE
A5U100	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A5U105	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A5U110	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5U115	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A5U120	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A5U125	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A5U130	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A5U200	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U205	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U210	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A5U215	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A5U220	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U225	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A5U235	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U300	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A5U310	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A5U320	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A5U400	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A5U405	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A5U420	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U425	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A5U430	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED	01295	SN74LS109A
A5U500	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A5U505	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U515	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U520	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U525	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U600	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A5U605	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U610	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U620	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A5U625	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5U627	156-1448-01			MICROCIRCUIT,DI:DUAL Y-BIT DECADE COUNTER	07263	74LS490
A5U700	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A5U705	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A5U720	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A5U725	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A5U800	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A5U820	156-0529-02			MICROCIRCUIT,DI:DATA SELECTOR,SCRN	01295	SN74LS257(NP3)
A5W330	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5W430	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	670-7418-01			CKT BOARD ASSY:TRIGGER		
A6C110	281-0626-00			CAP.,FXD,CER DI:3.3PF,1%,500V	59660	301000C0J0339B
A6C140	281-0510-00			CAP.,FXD,CER DI:22PF,+/-4.4PF,500V	59660	301-000C0G0220M
A6C200	281-0593-00			CAP.,FXD,CER DI:3.9PF,10%,500V	04222	7001-C0J-3R9C
A6C211	283-0001-00			CAP.,FXD,CER DI:0.005UF,+100-0%,500V	59821	2DDH61L502P
A6C220	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A6C221	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	MA101A271KAA
A6C250	290-0534-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	196D105X0035HA1
A6C251	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C300	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A6C330	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C400	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C500	283-0633-00			CAP.,FXD,MICA D:77PF,1%,100V	00853	D155E770F0
A6C502	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C520	283-0631-00			CAP.,FXD,MICA D:95PF,1%,500V	00853	D155F950F0
A6C521	281-0768-00			CAP.,FXD,CER DI:470PF,20%,100V	56289	292C00G471M100B
A6C523	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C600	283-0625-00			CAP.,FXD,MICA D:220PF,1%,500V	00853	D105F221F0
A6C620	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A6C630	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C700	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C710	290-0773-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,10V	56289	500D154
A6C711	281-0826-00			CAP.,FXD,CER DI:2200PF,5%,100V	96733	R3207
A6C720	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A6C740	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	MA201C472KAA
A6C750	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C751	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C820	290-0846-00			CAP.,FXD,ELCTLT:47UF,-10+75%,35 WVDC	54473	ECE-A35V47LU
A6C830	281-0626-00			CAP.,FXD,CER DI:3.3PF,1%,500V	59660	301000C0J0339B
A6C831	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C840	281-0773-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA201C103KAA
A6C848	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	MA201C472KAA
A6C901	290-0767-00			CAP.,FXD,ELCTLT:4.7UF,+75-10%,160V	56289	5020228
A6C910	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A6C930	290-0763-00			CAP.,FXD,ELCTLT:1UF,+50-20%,250V	56289	500D151
A6C931	290-0891-00			CAP.,FXD,ELCTLT:1UF,+75-10%,50V	55680	ULA1H010TEA
A6C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C1011	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A6C1020	281-0767-00			CAP.,FXD,CER DI:330PF,20%,100V	12969	CGB331MEN
A6C1021	283-0167-00			CAP.,FXD,CER DI:0.1UF,10%,100V	72982	8131N145X5R0104K
A6CR100	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR150	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR152	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR210	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR211	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR301	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR302	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR410	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR411	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR412	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR413	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR510	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6CR511	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR520	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR521	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR522	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR530	152-0153-00			SEMICOND DVC,DI:SW,SI,10V,50MA,D0-7	07263	FD7003
A6CR601	152-0754-00			SEMICOND DEVICE:RECT,SI,SCHOTTKY,40V,8A	81483	95-4421
A6CR610	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR611	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR630	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR631	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR640	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR700	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A6CR701	152-0720-00			SEMICOND DEVICE:SILICON,100V,7A	25403	BYW29-100
A6CR731	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	1N4936
A6CR732	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	1N4936
A6CR740	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR840	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	12969	NDP0263 (1N4152)
A6CR900	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A6CR920	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	1N4936
A6CR921	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	1N4936
A6CR1030	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A6CR1031	152-0066-00			SEMICOND DVC DI:RECT,SI,400V,1A,D0-41	05828	GP10G-020
A6F940	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC-CW-1/2
A6F1040	159-0025-00			FUSE,CARTRIDGE:3AG,0.5A,250V,FAST-BLOW	71400	AGC-CW-1/2
A6L630	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A6L640	108-0245-00			COIL,RF:3.9UH	76493	B6310-1
A6L710	108-1116-00			COIL,RF:FIXED,97UF POT CORE	80009	108-1116-00
A6L730	108-1117-00			COIL,RF:6.5MH POT CORE	80009	108-1117-00
A6L830	108-1117-00			COIL,RF:6.5MH POT CORE	80009	108-1117-00
A6L1020	108-0422-00			COIL,RF:FIXED,82UH	80009	108-0422-00
A6Q140	151-0435-00			TRANSISTOR:SILICON,PNP	04713	SPS8335
A6Q150	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A6Q250	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A6Q300	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A6Q410	151-0341-00			TRANSISTOR:NPN,SI,TO-106	04713	SPS6919
A6Q420	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A6Q421	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q422	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q500	151-1025-00			TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A6Q510	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A6Q511	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A6Q520	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A6Q521	151-0198-00			TRANSISTOR:SELECTED	04713	SPS8802-1
A6Q610	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A6Q611	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A6Q731	151-0350-00			TRANSISTOR:SILICON,PNP	04713	SPS6700
A6Q740	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q741	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q800	151-1147-00			TRANSISTOR:FE,N-CHANNEL	04713	STP3001
A6Q831	151-0503-00			SCR:SILICON,TO-92	04713	SCR5138
A6Q835	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A6Q840	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q841	151-0188-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6868
A6Q842	151-0350-00			TRANSISTOR:SILICON,PNP	04713	SPS6700

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A6Q843	151-0223-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8026
A6Q844	151-0223-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8026
A6Q845	151-0223-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS8026
A6Q1010	151-0190-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7969
A6R100	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R110	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A6R111	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	91637	CMF55116G10003F
A6R140	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R141	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R142	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R150	311-1243-00			RES.,VAR,NONWIR:500K OHM,10%,0.50W	73138	72-34-0
A6R151	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R152	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6R153	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R154	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R200	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R201	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	57668	NTR25J-E043K
A6R202	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	57668	NTR25J-E043K
A6R203	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	91637	CMF55116G10003F
A6R211	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A6R212	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	57668	NTR25J-E 13K
A6R213	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	57668	NTR25J-E 13K
A6R214	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R230	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A6R240	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A6R241	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A6R242	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A6R250	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A6R301	315-0624-00			RES.,FXD,CMPSN:620K OHM,5%,0.25W	57668	NTR25J-E 620K
A6R310	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A6R311	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A6R312	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R313	315-0624-00			RES.,FXD,CMPSN:620K OHM,5%,0.25W	57668	NTR25J-E 620K
A6R314	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R320	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R330	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R331	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R340	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A6R400	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	57668	NTR25J-E 200K
A6R401	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R402	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R403	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A6R404	315-0205-00			RES.,FXD,CMPSN:2M OHM,5%,0.25W	01121	CB2055
A6R405	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	57668	NTR255-E 1M
A6R406	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A6R407	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A6R408	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R410	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	57668	NTR25J-E750E
A6R411	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	57668	NTR25J-E 430E
A6R412	321-0246-00			RES.,FXD,FILM:3.57K OHM,1%,0.125W	91637	CMF55116G35700F
A6R422	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	57668	NTR25J-E 130E
A6R430	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R431	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R500	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E

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A6R501	311-1221-00			RES.,VAR,NONWIR:50 OHM,20%,0.50W	32997	3386F-T04-500
A6R503	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R504	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A6R505	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	CMF55116G82500F
A6R509	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R510	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R511	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R512	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	57668	NTR25J-E20K0
A6R513	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6R514	321-0157-00			RES.,FXD,FILM:422 OHM,1%,0.125W	91637	CMF55116G422R0F
A6R515	321-0330-00			RES.,FXD,FILM:26.7K OHM,1%,0.125W	91637	MFF1816G26701F
A6R516	321-0273-00			RES.,FXD,FILM:6.81K OHM,1%,0.125W	91637	MFF1816G68100F
A6R517	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A6R518	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A6R519	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6R520	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R522	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	57668	NTR25J-E470E
A6R530	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6R600	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A6R601	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A6R602	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R610	321-0313-00			RES.,FXD,FILM:17.8K OHM,1%,0.125W	91637	MFF1816G17801F
A6R611	321-0307-00			RES.,FXD,FILM:15.4K OHM,1%,0.125W	91637	MFF1816G15401F
A6R612	311-1226-00			RES.,VAR,NONWIR:2.5K OHM,20%,0.50W	32997	3386F-T04-252
A6R613	321-0262-00			RES.,FXD,FILM:5.23K OHM,1%,0.125W	91637	MFF1816G52300F
A6R620	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R621	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A6R630	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R631	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R632	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R633	321-0330-00			RES.,FXD,FILM:26.7K OHM,1%,0.125W	91637	MFF1816G26701F
A6R644	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R645	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R646	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R648	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6R651	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A6R700	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	57668	NTR25J-E 18E
A6R721	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A6R731	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R732	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R740	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R741	321-0230-00			RES.,FXD,FILM:2.43K OHM,1%,0.125W	24546	CT552431F
A6R743	315-0624-00			RES.,FXD,CMPSN:620K OHM,5%,0.25W	57668	NTR25J-E 620K
A6R746	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A6R747	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	57668	NTR25J-E220E
A6R750	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	57668	NTR25J-E 30K
A6R751	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6R752	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R753	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	57668	NTR25J-E220K
A6R809	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	57668	NTR25J-E03K0
A6R810	308-0678-00			RES.,FXD,WW:0.1 OHM,5%,2W	75042	BWH-R1000J
A6R811	308-0678-00			RES.,FXD,WW:0.1 OHM,5%,2W	75042	BWH-R1000J
A6R831	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R832	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A6R833	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0

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A6R834	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R841	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A6R842	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	57668	NTR25J-E16K0
A6R843	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R845	321-0218-00			RES.,FXD,FILM:1.82K OHM,1%,0.125W	91637	MFF816G18200F
A6R846	321-0185-00			RES.,FXD,FILM:825 OHM,1%,0.125W	91637	CMF55116G825R0F
A6R847	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	57668	NTR25J-E 430E
A6R848	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R849	315-0363-00			RES.,FXD,CMPSN:36K OHM,5%,0.25W	57668	NTR25J-E36K0
A6R900	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R921	307-0103-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A6R922	315-0624-00			RES.,FXD,CMPSN:620K OHM,5%,0.25W	57668	NTR25J-E 620K
A6R940	301-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.5W	57668	TR50J-E 4K7
A6R950	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	57668	NTR25JE01K0
A6R1000	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	57668	NTR25J-E51K0
A6R1001	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	57668	NTR25J-E10K0
A6R1002	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	57668	NTR25J-E05K1
A6R1010	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	57668	NTR25J-E100K
A6R1011	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1012	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A6R1013	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A6R1020	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	57668	NTR25J-E330E
A6R1021	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	57668	NTR25J-E01K5
A6R1040	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6R1110	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A6R1140	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	57668	NTR25J-E02K0
A6S130	260-2107-00			SWITCH,TOGGLE:SPDT,0.4VA,20V,MOM-OFF-MOM	15605	A12732Y9AV2BE
A6S140	260-2107-00			SWITCH,TOGGLE:SPDT,0.4VA,20V,MOM-OFF-MOM	15605	A12732Y9AV2BE
A6S210	260-1771-00			SWITCH,PUSH:DPDT,1 BUTTON,2 POLE	59821	2KAB010000759
A6S211	260-1424-00			SWITCH,PUSH:5 STA,INTERLOCK,NON-SHORT	59821	2KBC050000607
A6S621	311-1403-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	01121	18M651
A6T810	120-1420-00			TRANSFORMER,RF:POWER,CONVERTER POT CORE	80009	120-1420-00
A6TP340	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A6TP651	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A6TP652	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A6U200	156-1149-01			MICROCIRCUIT,LI:OPER AMPL,JFET,BURN-IN	27014	AL160307
A6U300	156-1226-01			MICROCIRCUIT,LI:DUAL COMPTR,14 DIP,SCRN	27014	LM319J/A+
A6U330	156-1258-01			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A6U340	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A6U410	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A6U440	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A6U441	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A6U540	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A6U541	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A6U630	156-0466-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	01295	SN74LS37
A6U740	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A6U1000	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05
A6U1020	156-0041-05			MICROCIRCUIT,DI:DUAL D-FLIP FLOP	01295	SN7474
A6VR600	152-0227-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ13903
A6VR730	152-0241-00			SEMICOND DEVICE:ZENER,0.4W,33V,5%	04713	SZG35009K5
A6VR731	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A6VR801	152-0287-00			SEMICOND DEVICE:ZENER,0.4W,110V,5%	12954	1N986B
A6VR802	152-0287-00			SEMICOND DEVICE:ZENER,0.4W,110V,5%	12954	1N986B
A6VR900	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	14552	TD381 0983
A6VR940	152-0149-00			SEMICOND DEVICE:ZENER,0.4W,10V,5%	04713	SZG35009K3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
DS1	150-0049-00			LAMP,INCAND:5V,0.06A,#6835,AXIAL LEAD	52043	6835AS15
DS2	150-0049-00			LAMP,INCAND:5V,0.06A,#6835,AXIAL LEAD	52043	6835AS15
DS3	150-1031-00			LT EMITTING DIO:RED,650NM,40MA MAX	53184	XC209R
DS4	150-0049-00			LAMP,INCAND:5V,0.06A,#6835,AXIAL LEAD	52043	6835AS15
DS5	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
R1	311-0467-00			RES.,VAR,NONWIR:100K OHM,20%,0.50W	01121	W7705B
S310	263-1208-00			SW,CAM ACTR AS:VOLTS/DIV	80009	263-1208-00
S320	263-1207-00			SW,CAM ACTR AS:TIME/DIV	80009	263-1207-00
S340	263-1209-00			SW,CAM ACTR AS:VOLTS/DIV	80009	263-1209-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

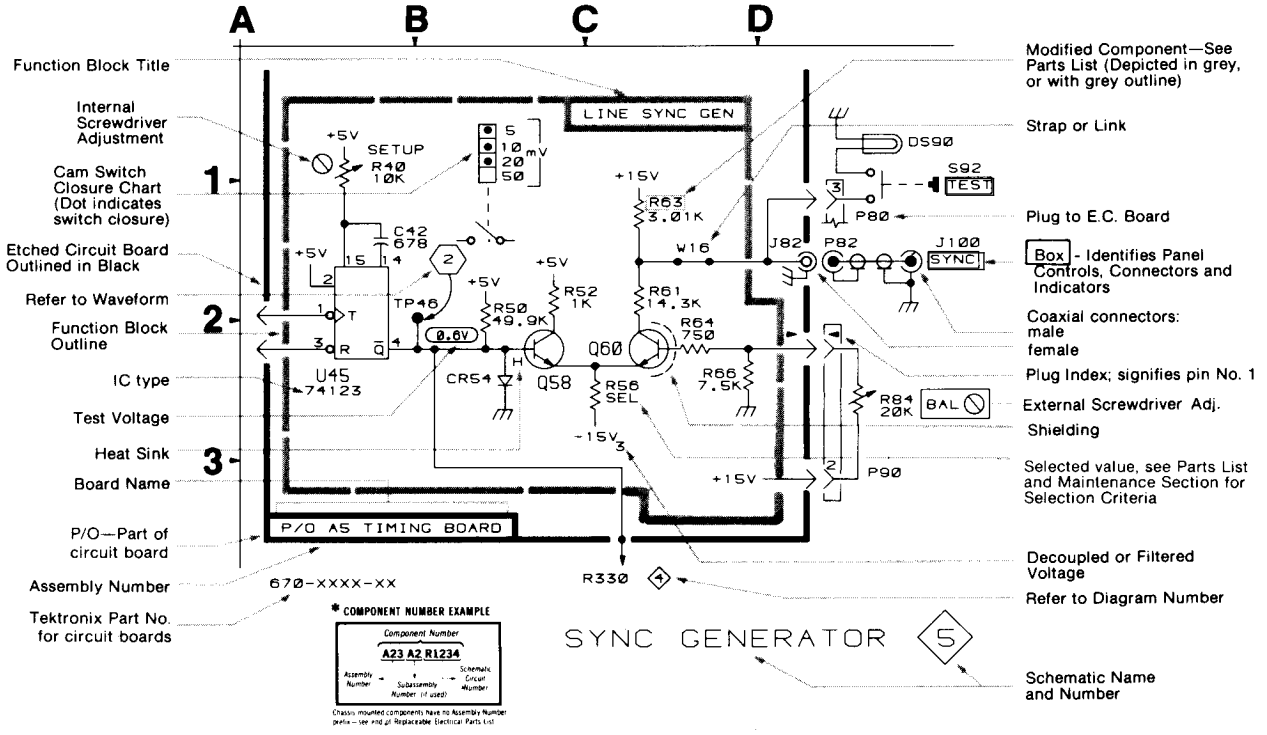
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



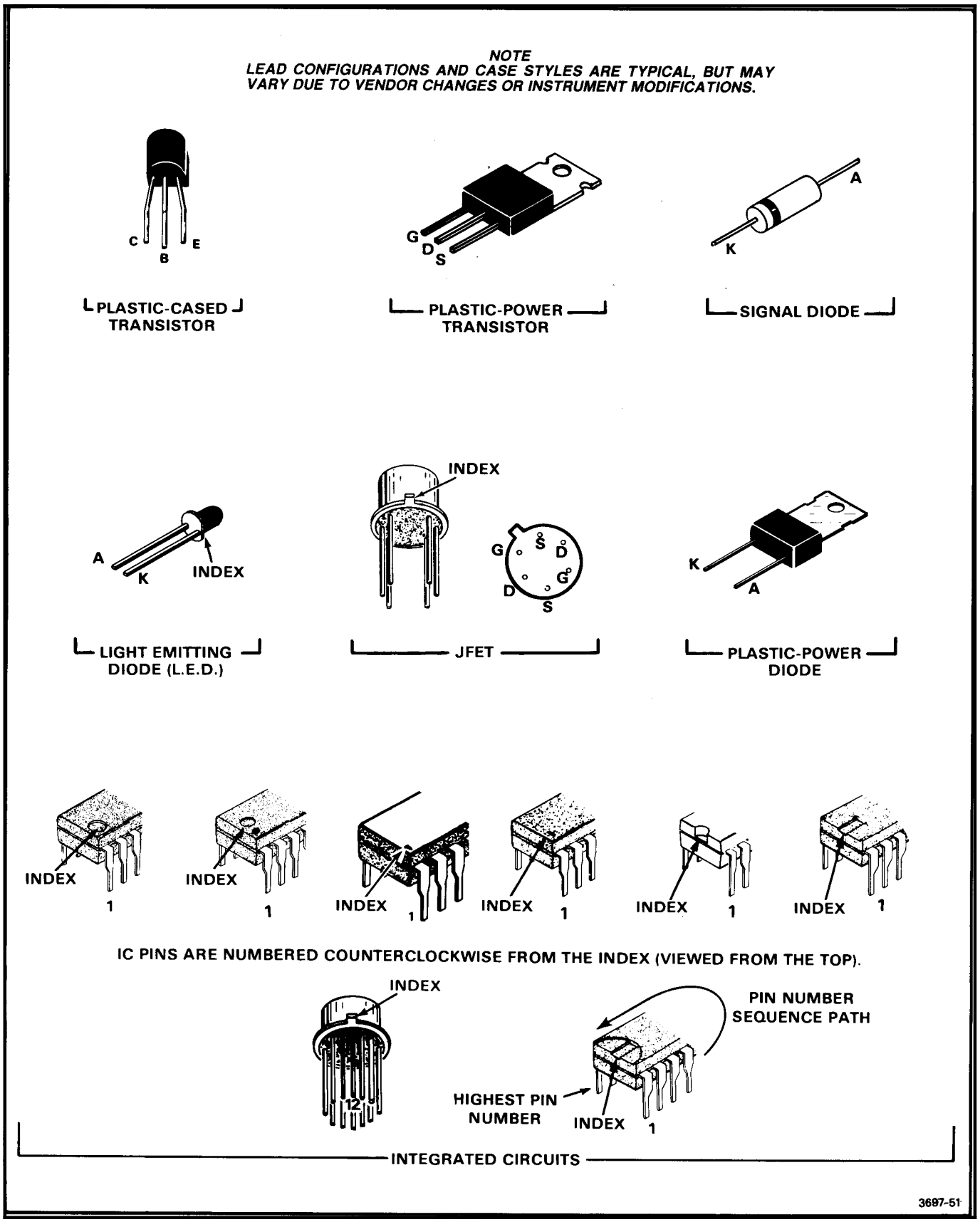
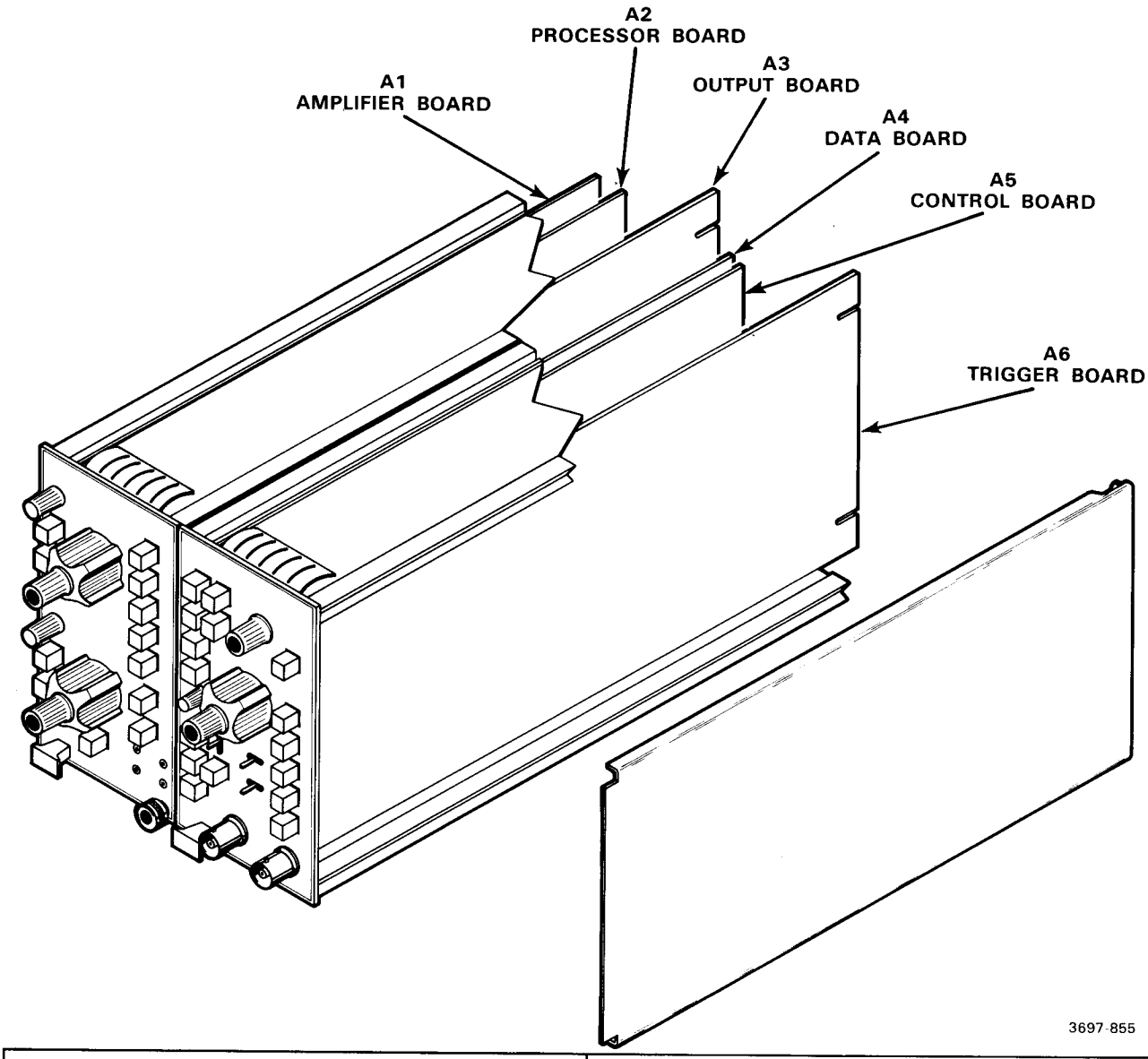


Figure 8-1. Semiconductor Lead Configurations.



BOARD LOCATOR BY ASSEMBLY NUMBER			BOARD LOCATOR BY BOARD NAME		
Assembly Number	Board Name	Diagram Number	Board Name	Assembly Number	Diagram Number
A1	Amplifier	2,4,5,13,14	Amplifier	A1	2,4,5,13,14
A2	Microprocessor	1,13,14	Control	A5	1,2,3,5,6,7,8,9 10,11,12,13,14
A3	Output	1,2,3,4,5,6,8,9, 10,11,12,13,14,15	Data	A4	3,7,8,9,10,13,14
A4	Data	3,7,8,9,10,13,14	Microprocessor	A2	1,13,14
A5	Control	1,2,3,5,6,7,8,9, 10,11,12,13,14	Output	A3	1,2,3,4,5,6,8,9, 10,11,12,13,14,15
A6	Trigger	1,2,5,6,7, 11,12,13,14,15	Trigger	A6	1,2,5,6,7, 11,12,13,14,15

Figure 8-2. 5D10 Circuit Board Locator Illustration.

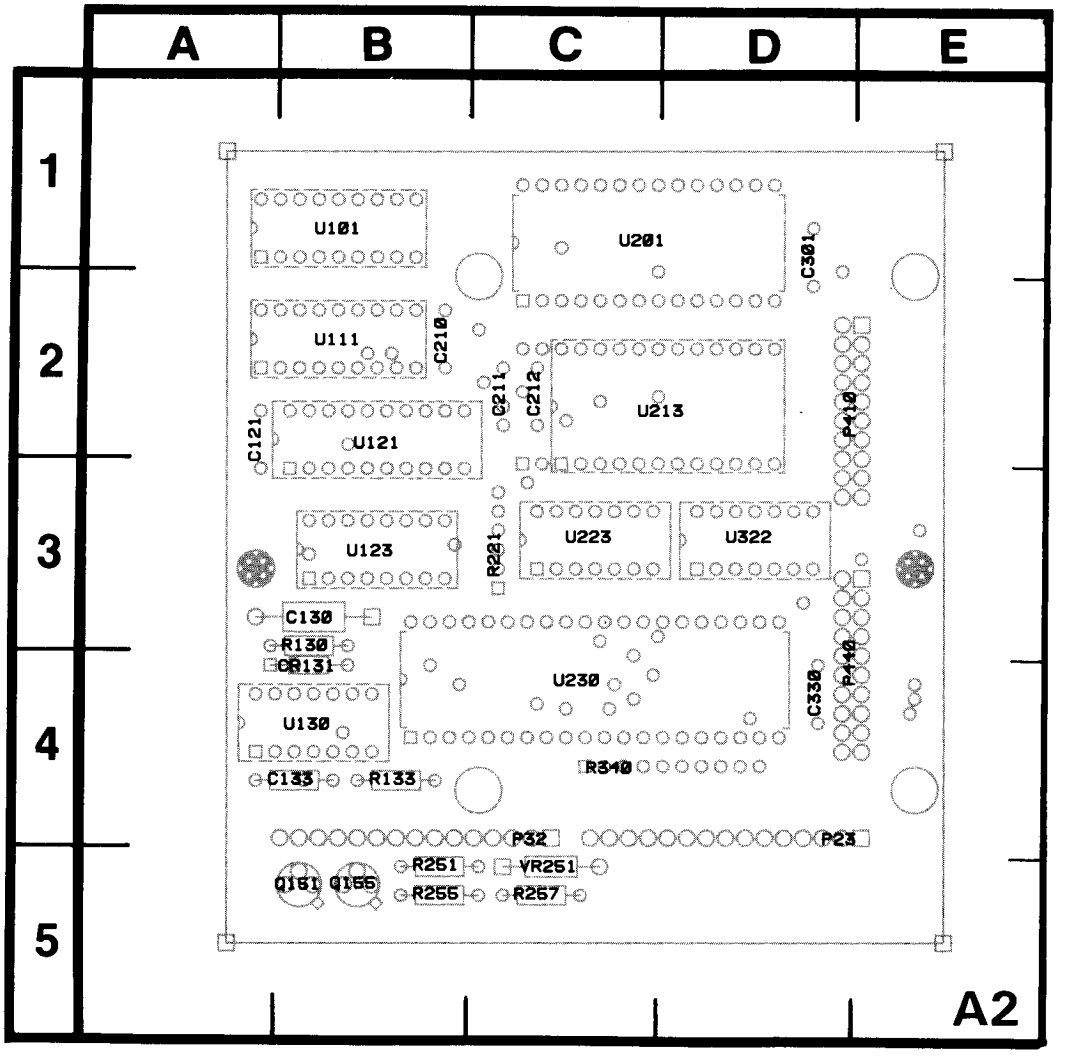
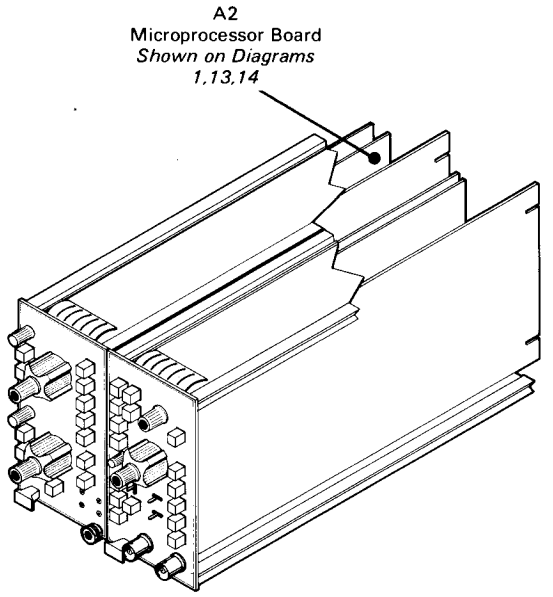


Figure 8-3. A2—Microprocessor circuit board assembly.

3697-317



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CPU, ROM, RAM, CLOCK AND I/O CONTROL DIAGRAM 1
(SN B020100 & ABOVE)

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	C3	A3	R130	C3	A3	U130B	F4	B4
C133	C2	B4	R133	C2	B4	U130C	F4	B4
			R221B	C3	C3	U130D	D4	B4
CR131	C4	B4	R221C	E1	C3	U201	E2	C1
			R221D	D3	C3	U213	E3	C2
P32	C1	C4	R221E	E3	C3	U223A	C3	C3
P410	C2	D2	R251	C4	B5	U223B	E1	C3
P410	C3	D2	R255	C4	B5	U223D	E1	C3
P410	D3	D2	R257	C4	C5	U223F	D3	C3
P410	E4	D2	R340	D1	C4	U230	D2	C4
P410	F4	D2	R340J	C3	C4	U322A	C2	D3
P440	E1	D4	U101	F2	B1	U322B	C2	D3
P440	E4	D2	U111	F3	B2	U322D	E4	D3
P440	F1	D4	U121	E1	B2	U322E	F4	D3
Q151	C4	B5	U123	E3	A3	U322F	F4	D3
Q155	C4	B5	U130A	E4	B4	VR251	C4	C5

Partial A2 also shown on diagram 13.

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J23	G1	K4	P53	B2	J1	U650	H2	G4
J32	C1	H4	P53	G4	J1	U930	G2	K3
P30	B1	K3	R650	G3	G5			

Partial A3 also shown on diagrams 2, 3, 4, 5, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P53	B2	C1	R200	H4	C1			
P53	G4	C1						
P56	B2	G5	U300	H3	D2			

Partial A5 also shown on diagrams 2, 3, 5, 6, 7, 8, 9, 10, 11, 12 and 13

ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR510	A3	F2	Q511	A2	F2	R513	A2	E2
CR511	A3	F2				R514	A2	E2
			R501	A2	F1			
P56	B2	E4	R503	A3	F1	U630A	A2	F3
P620	A2	F3	R504	A3	F1	U630B	B3	F3
			R505	A3	F1			
Q510	A3	F2	R509	A2	F2			

Partial A6 also shown on diagrams 2, 5, 6, 7, 11, 12 and 13.

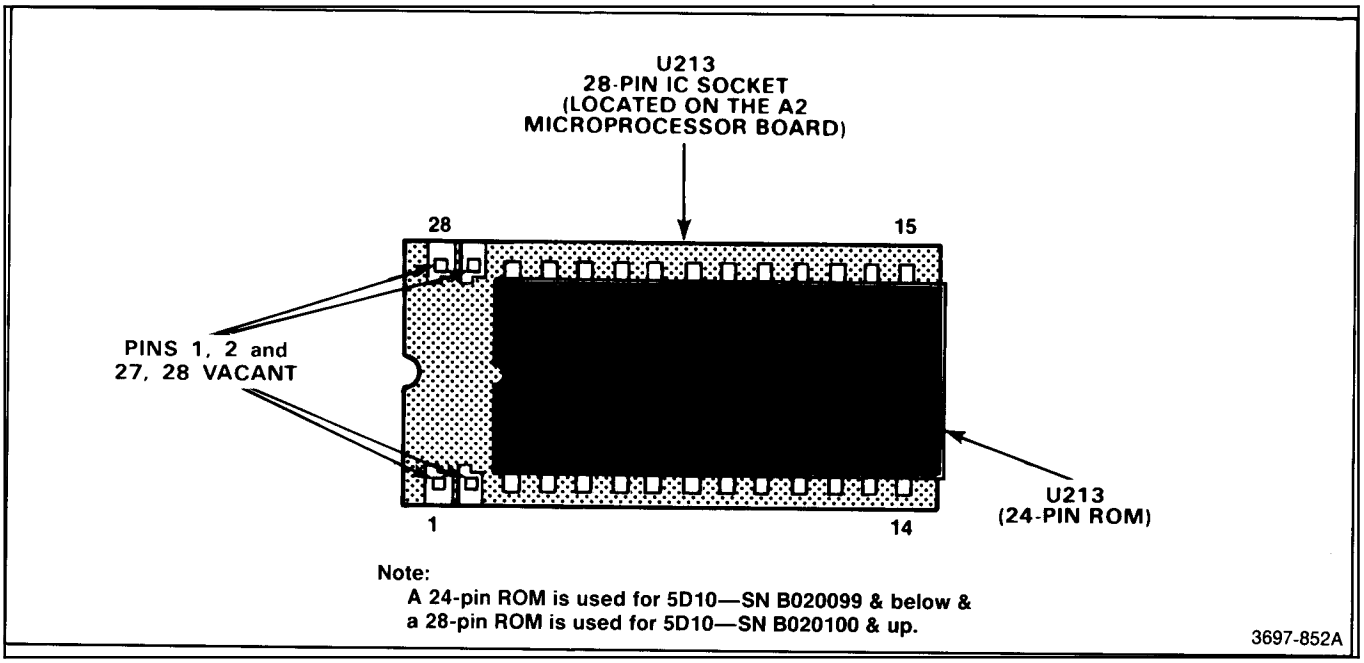
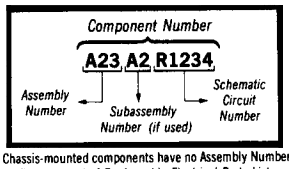


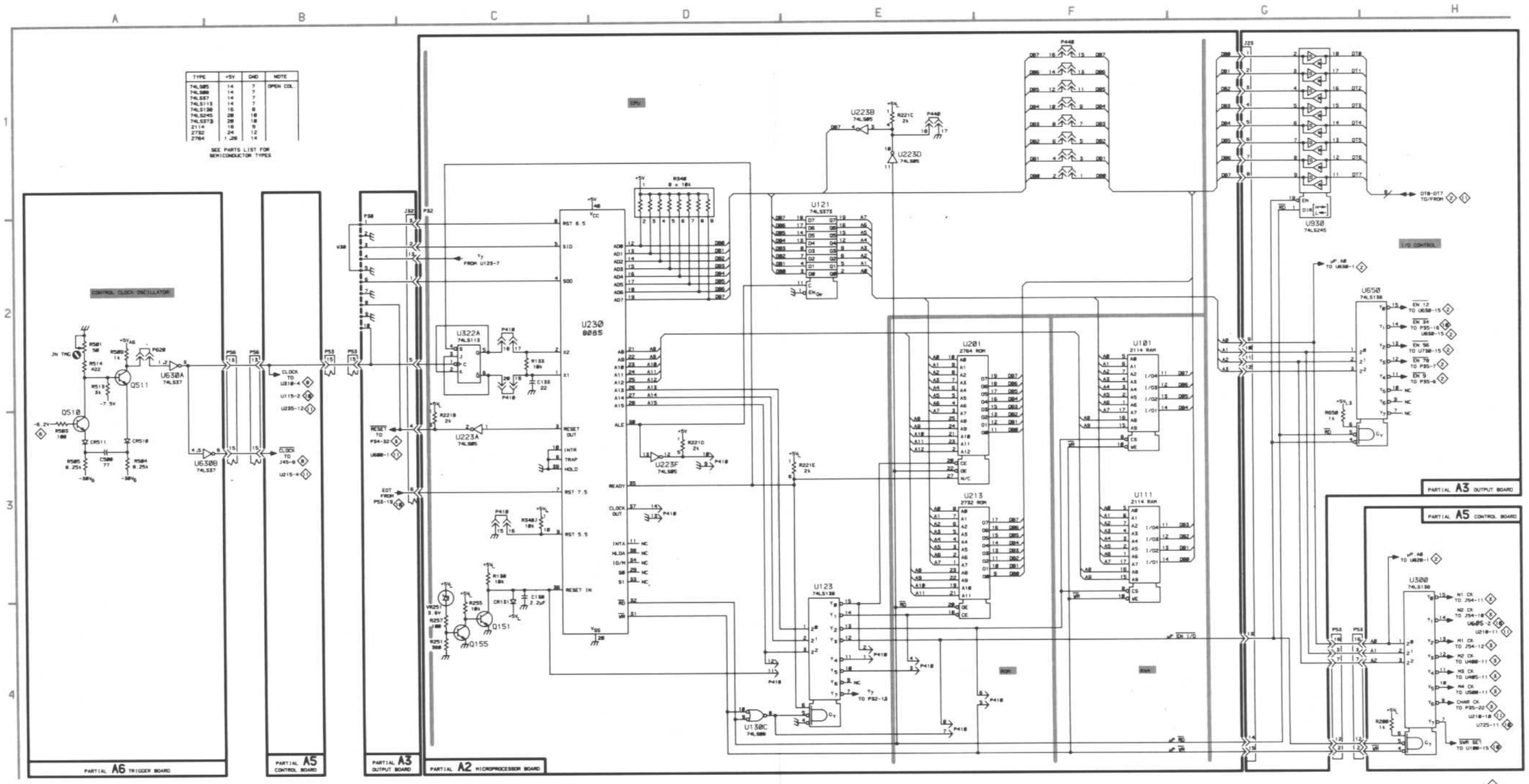
Figure 8-4. Proper insertion of U213 (24-pin ROM) into the 28-pin I.C. socket.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



SN B020099 & below

5D10

(SN B020099 & BELOW) CPU ,ROM ,RAM ,CLOCK AND I/O CONTROL 1

CPU, ROM, RAM, CLOCK AND I/O CONTROL DIAGRAM 1
(SN B020099 & BELOW)

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C130	C3	A3	P440	F1	D4	U101	F2	B1
C133	C2	B4				U111	F3	B2
			Q151	C4	B5	U121	E1	B2
CR131	C4	B4	Q155	C4	B5	U123	E3	A3
						U130C	D4	B4
P32	C1	C4	R130	C3	A3	U201	E2	C1
P410	C2	D2	R133	C2	B4	U213	E3	C2
P410	C3	D2	R221B	C3	C3	U223A	C3	C3
P410	D3	D2	R221C	E1	C3	U223B	E1	C3
P410	D3	D2	R221D	D3	C3	U223D	E1	C3
P410	D4	D2	R221E	E3	C3	U223F	D3	C3
P410	E4	D2	R251	C4	B5	U230	D2	C4
P410	E4	D2	R255	C4	B5	U322A	C2	D3
P410	E4	D2	R257	C4	C5			
P410	F4	D2	R340	D1	C4	VR251	C4	C5
P440	E1	D4	R340J	C3	C4			

Partial A2 also shown on diagram 13.

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J23	G1	K4	P53	B2	J1	U650	H2	G4
J32	C1	H4	P53	G4	J1	U930	G2	K3
P30	B1	K3	R650	G3	G5			

Partial A3 also shown on diagrams 2, 3, 4, 5, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P53	B2	C1	R200	H4	C1			
P53	G4	C1						
P56	B2	G5	U300	H3	D2			

Partial A5 also shown on diagrams 2, 3, 5, 6, 7, 8, 9, 10, 11, 12 and 13

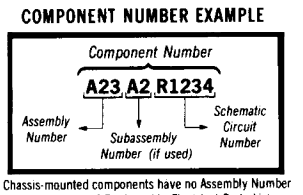
ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR510	A3	F2	Q511	A2	F2	R513	A2	E2
CR511	A3	F2				R514	A2	E2
			R501	A2	F1			
P56	B2	E4	R503	A3	F1	U630A	A2	F3
P620	A2	F3	R504	A3	F1	U630B	B3	F3
			R505	A3	F1			
Q510	A3	F2	R509	A2	F2			

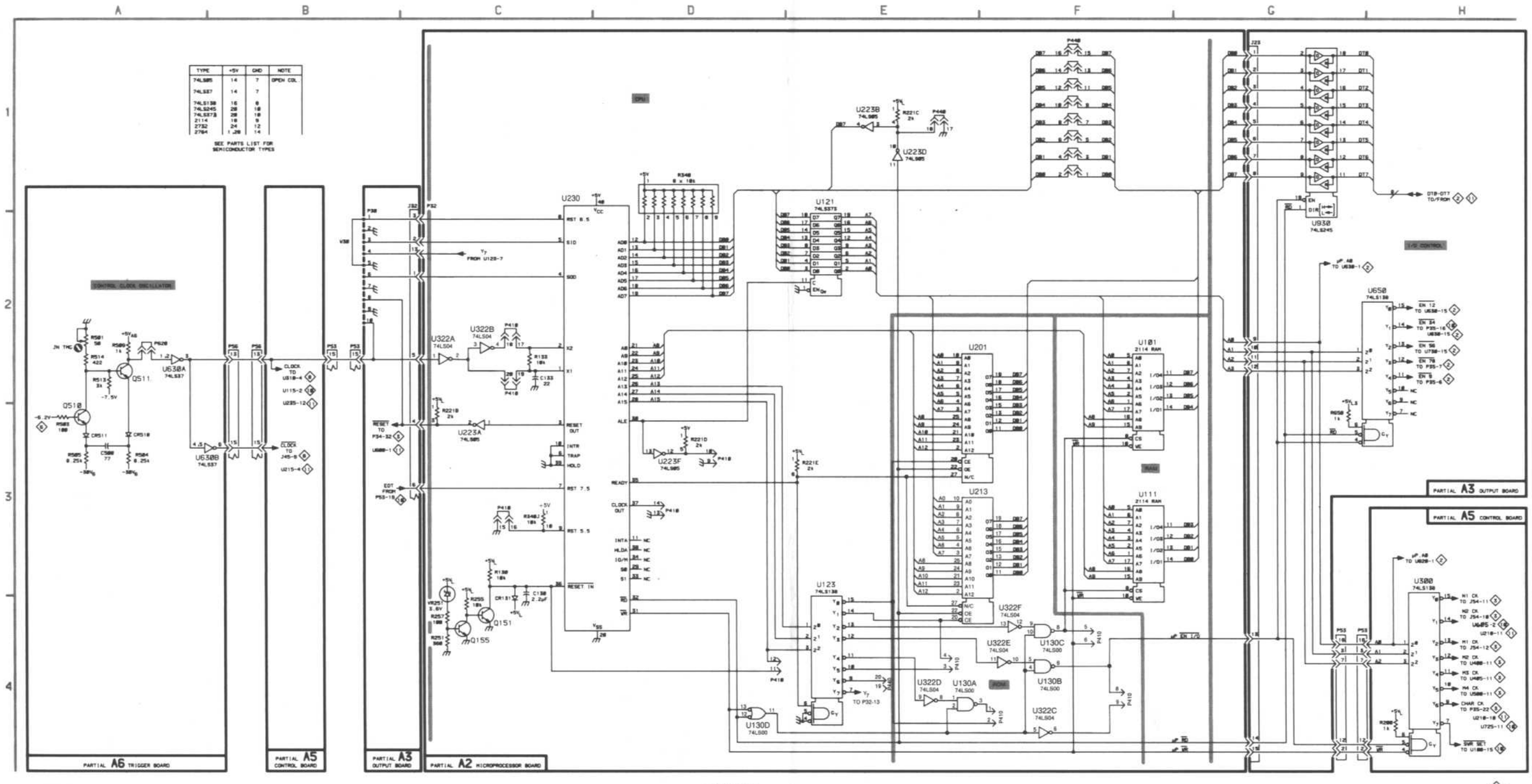
Partial A6 also shown on diagrams 2, 5, 6, 7, 11, 12 and 13.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



TYPE	+5V	GND	NOTE
74LS05	14	7	OPEN COL
74LS27	14	7	
74LS138	16	8	
74LS245	20	10	
74LS373	20	10	
2114	18	9	
2732	24	12	
2764	1.28	14	

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

5D10

(3697-800)3697-815
ADD APR 1985

(SN B020100 & ABOVE) CPU ,ROM ,RAM ,CLOCK AND I/O CONTROL 1

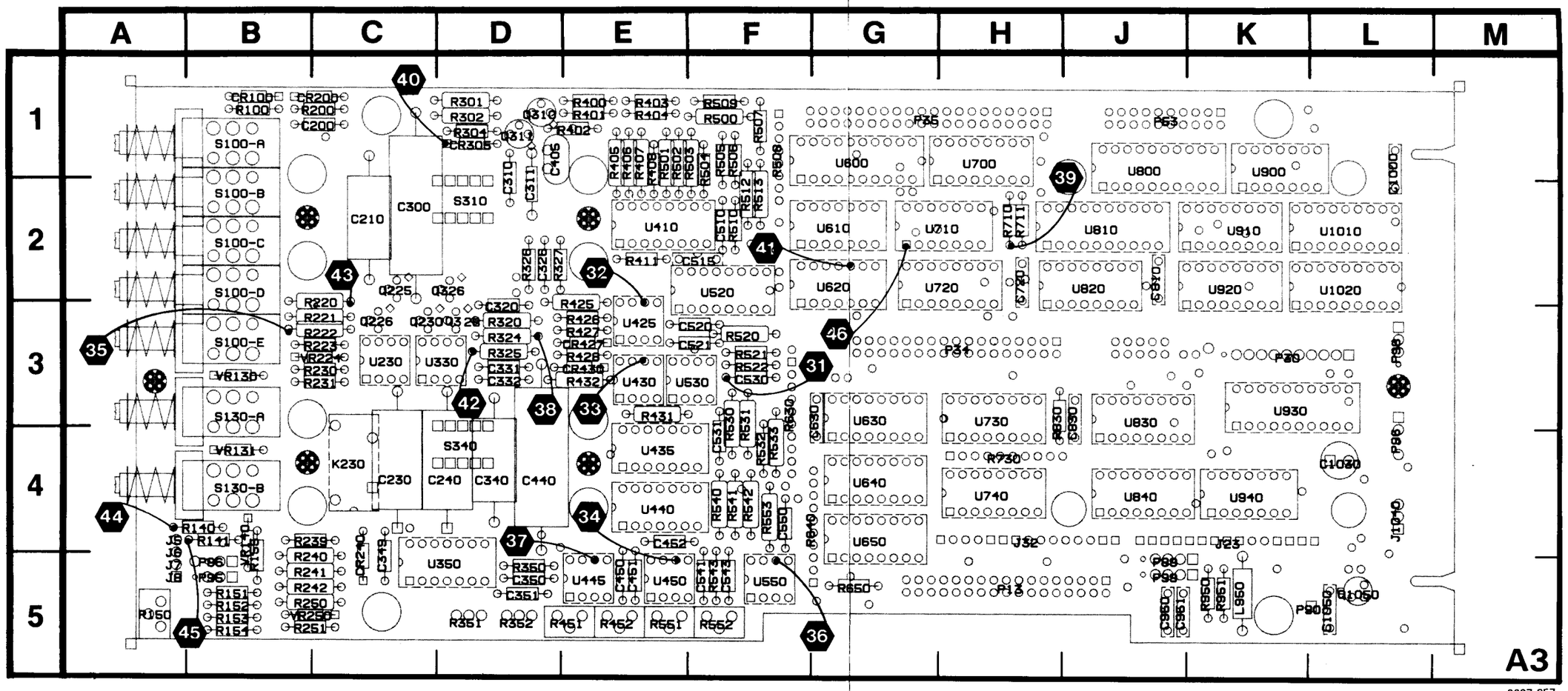
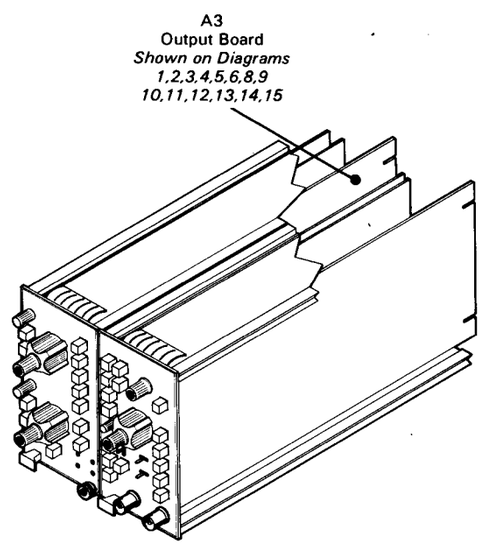
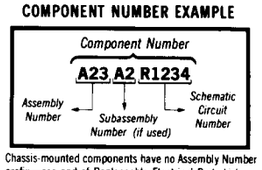


Figure 8-5. A3—Output circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CONTROLLER INPUTS DIAGRAM 2

ASSEMBLY A1 *Figure 8-7 illustrates circuit board A1.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1201	C4	K1	Q1010	C4	J1	S639	D4	F4
C1220	D5	K2				S740	D5	F5
C1231	C4	K3	R832	C4	G3	S1200B	D5	K2
C1240	C5	K4	R833	C4	G3	S1200B	D5	K2
			R1000	C4	J1	S1230A	C5	K4
P13	D4	D5	R1001	C4	J1	S1230B	C5	K4
						S1230B	C5	K4
Q830	C4	G4	S610	D4	F2			

Partial A1 also shown on diagrams 4, 5 and 13.

ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1040	G5	L4	R730	F5	H4	S100E	E4	B2
			R830	G4	H3	S130A	E5	B4
P13	D4	H5	R950	E5	K5	S130A	E5	B3
P35	D1	G1	R951	E5	K5	S130B	E5	B4
						S130B	E5	B4
Q1050	E5	L5	S100A	E3	B2	S310	F3	D2
			S100A	E4	B1	S340	E3	D4
R630A	F4	F3	S100B	E4	B2			
R630D	F4	F3	S100B	E4	B2	U630	G1	G3
R630	G1	F3	S100C	E4	B2	U640	G2	G4
R630	G2	F3	S100C	E4	B2	U730	G4	H3
R640	F1	F4	S100D	E4	B2	U740	G4	H4
R640	F2	F4	S100D	E4	B2	U830	G2	J3
R730A	F4	H4	S100E	E4	B3	U840	G3	J4

Partial A3 also shown on diagrams 1, 3, 4, 5, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	C3	A1	S900A	B3	K1	S920B	B3	K4
J101	C3	A1	S900A	B3	K1	S920B	B3	K4
			S900B	B3	K1	S920C	B3	K4
P35	D1	D1	S900B	B3	K2	S920C	B3	K4
P56	B1	G5	S900C	B3	K1	S935	B2	J4
			S900C	B3	K2	S1020	B2	K4
R720	C2	H4	S900D	B3	K2			
R800	C3	J2	S900D	B4	K1	U720	D2	H3
R830	C1	J5	S920A	B3	K4	U800	D3	J2
			S920A	B3	K4	U820	D1	H4

Partial A5 also shown on diagrams 1, 3, 5, 6, 7, 8, 9, 10, 11, 12 and 13

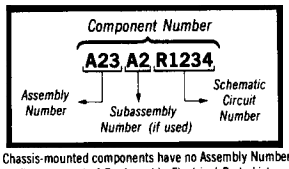
ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P56	B1	E4	S130	A1	B4	S320	A3	D3
			S140	A1	B4	S621	A1	G3

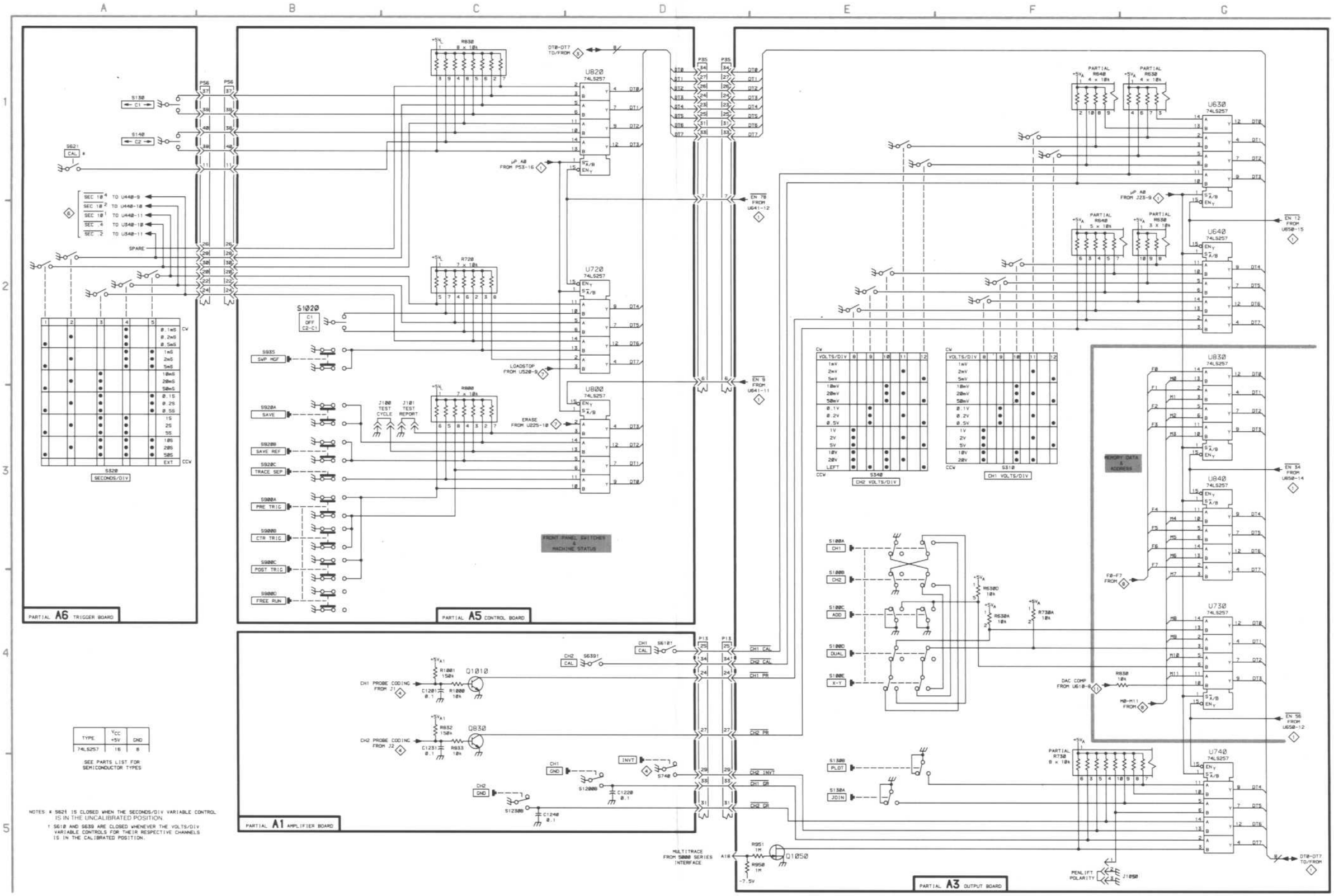
Partial A6 also shown on diagrams 1, 5, 6, 7, 11, 12 and 13.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



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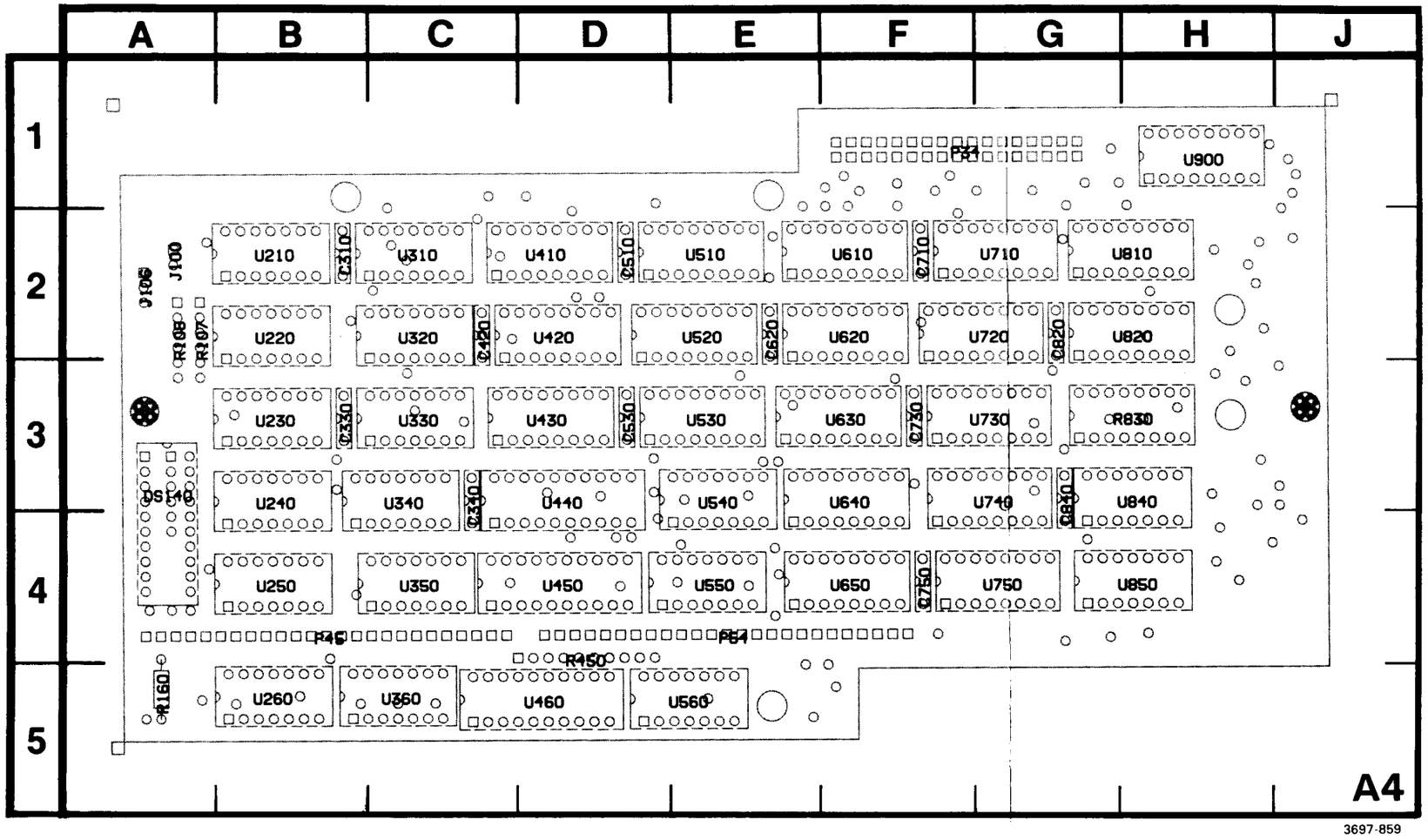
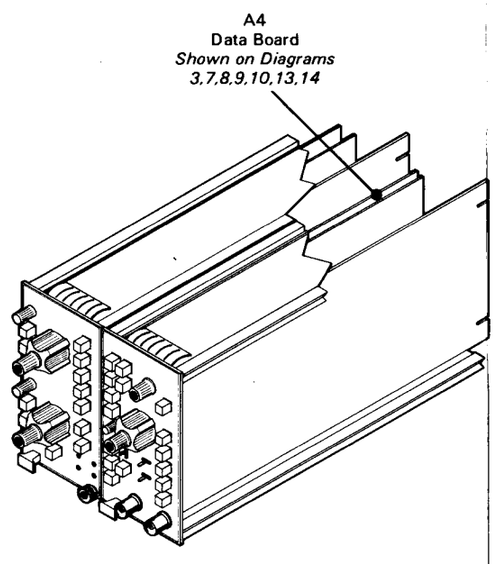
REV APR 1985



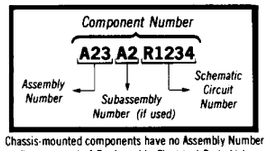
3697-859

Figure 8-6. A4—Data circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

CONTROLLER OUTPUTS AND SELF-TEST ANNUNCIATOR DIAGRAM 3

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P34	F1	H3	P35	F2	G1			
P35	C2	G1	P53	C2	J1			

Partial A3 also shown on diagrams 1, 2, 4, 5, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS140	E2	A3	P54	E3	E4	U340F	E3	C3
						U440	D2	D3
J100	D1	A2	R107	E1	A2	U450	D3	D4
			R108	D1	A2	U460	D4	D5
P34	F1	F1	R450	C1	D4	U560D	E3	E5
P45	E3	B4						
P54	C1	E4	U340C	D4	C3			

Partial A4 also shown on diagrams 7, 8, 9, 10 and 13.

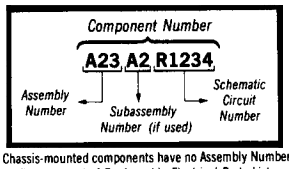
ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	B2	D1	TP120	A4	A3	U405	A3	E2
P35	F2	D1				U500	A4	E2
P53	B2	C1	U225C	A2	C4			
			U400	A2	D2			

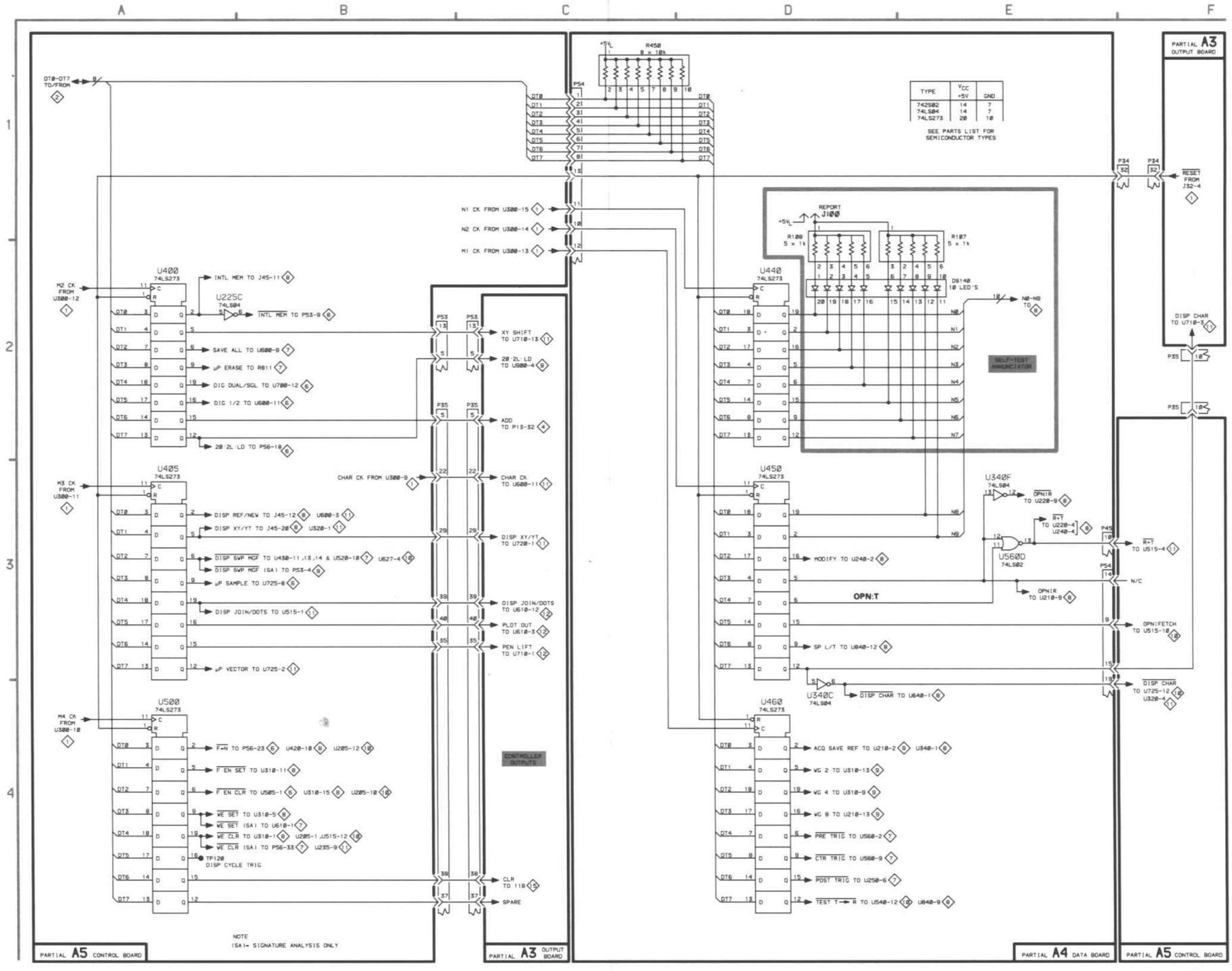
Partial A5 also shown on diagrams 1, 2, 5, 6, 7, 8, 9, 10, 11, 12 and 13

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



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CONTROLLER OUTPUTS AND SELF-TEST ANNUNCIATOR 3

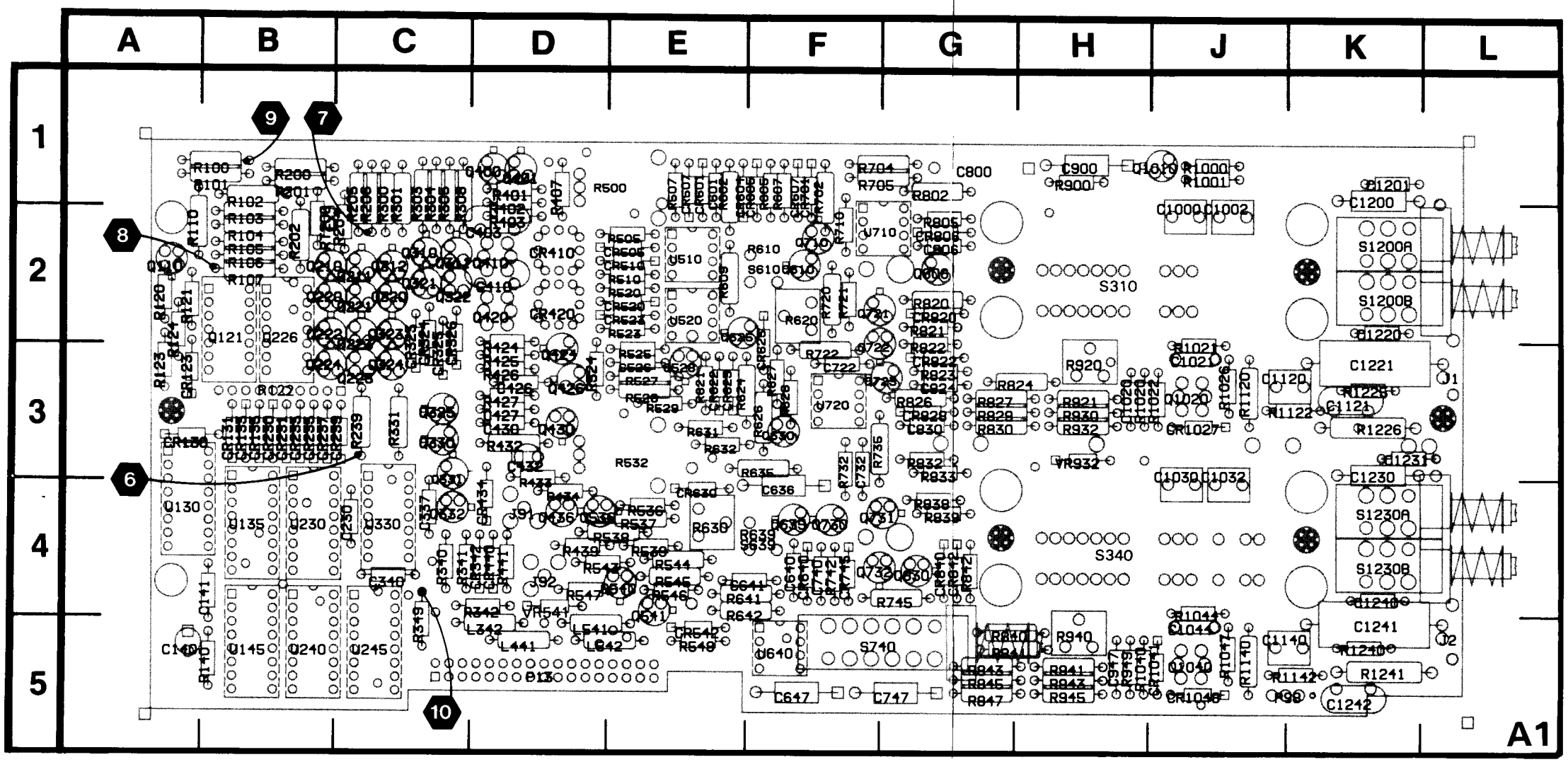
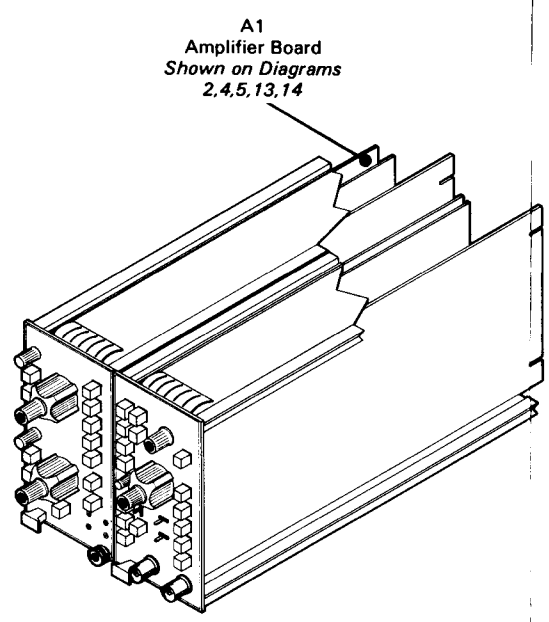
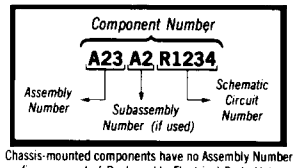


Figure 8-7. A1—Amplifier circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

SIGNAL ACQUISITION - CH1 AND CH2 DIAGRAM 4

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C403	G1	D2
C410	G4	D2
C426	G4	D3
C526	F4	E3
C601	F2	E1
C636	F5	F4
C640	D1	F4
C641	D4	F4
C722	D1	F3
C732	D4	F3
C740	D5	F4
C800	G4	G1
C806	D1	G2
C824	D2	G3
C830	D1	G3
C900	G4	H1
C947	C4	H5
C1000	B1	J2
C1002	B2	J2
C1020	C1	H3
C1021	C1	J3
C1030	B4	J3
C1032	B4	J3
C1044	C4	J5
C1120	B1	J3
C1121	B1	K3
C1140	B4	K5
C1200	B2	K1
C1221	A1	K3
C1230	B4	K3
C1241	A4	K5
C1242	B4	K5
CR410	F1	D2
CR410	G5	D2
CR420	F3	D2
CR420	G5	D2
CR434	G1	D4
CR505	G2	E2
CR507	F1	E1
CR510	F1	E2
CR520	F3	E2
CR523	G4	E2
CR542	E5	E5
CR601	F1	E1
CR604	F1	E1
CR605	F1	F1
CR607	E2	F1
CR622	E4	E3
CR623	E4	E3
CR625	E1	F3
CR630	E3	E4
CR640	D5	F4
CR701	E1	F1
CR745	D4	F4
CR806	D1	G2
CR820	D2	G2
CR822	D2	G3
CR828	D2	G3
CR840	D4	G4
CR842	D3	G4
CR1027	C1	J3
CR1041	C4	J5
CR1048	C4	J5
J91	G2	D4
J92	G5	D4
P13	G1	D5
P98	A4	K5
Q400	G1	D1
Q401	F1	D1
Q410A	G1	D2
Q410B	G1	D2
Q420A	G4	D2
Q420B	G4	D2
Q424	G3	D3
Q426	F3	D3
Q430	E1	D3
Q436	E2	D4
Q528	F4	E3
Q536	E3	D4
Q540	E5	E4
Q541	E5	E4
Q610	E4	F2
Q625	E4	E2
Q630	E1	F3
Q635	D5	F4
Q710	F1	F2
Q721	D2	F2
Q722	D2	F3
Q723	D2	F3
Q730	D4	F4
Q731	D4	F4
Q732	D4	F4
Q806	D1	G2
Q1020A	C1	J3
Q1020B	C2	J3
Q1040A	C4	J5
Q1040B	C5	J5
R401	G1	D1
R402	F1	D2
R403	F1	D2
R407	F1	D1
R424	F3	D3
R425	F4	D3
R426	G3	D3
R427	G1	D3
R433	E2	D4
R434	F2	D4
R439	F3	D4
R500	F2	E1
R505	G1	E2
R507	F1	E1
R510	F1	E2
R520	F3	E2
R523	G4	E2
R524	F3	D3
R525	F3	E3
R527	F4	E3
R528	E4	E3
R529	E4	E3
R532	F4	E3
R536	E3	E4
R537	F3	E4
R538	F3	D4
R539	F5	E4
R543	E5	D4
R544	F5	E4
R545	F5	E4
R546	E5	E4
R547	F5	D4
R548	E5	E5
R602	F1	E1
R605	E2	F1
R607	E2	F1
R609	E1	E2
R610	E2	F2
R620	E2	F2
R621	E4	E3
R624	E4	E3
R626	E1	F3
R627	E4	F3
R628	E4	F3
R630	E4	E4
R631	E4	E3
R632	E1	E3
R635	E4	F3
R639	E4	F4
R641	D4	F4
R642	D4	F4
R702	E2	F1
R704	F4	F1
R705	F4	F1
R710	E1	F2
R720	E2	F2
R721	D1	F2
R722	D2	F3
R732	D4	F3
R735	D2	F3
R742	D5	F4
R745	C5	G4
R802	F4	G1
R805	C1	G2
R820	C1	G2
R821	D2	G2
R822	D2	G3
R823	D2	G3
R824	C2	G3
R826	C2	G3
R827	C2	G3
R829	C2	G3
R830	C2	G3
R838	D4	G4
R839	D4	G4
R840	C3	G5
R841	C4	G5
R842	C1	G4
R843	C4	G5
R845	C4	G5
R847	C4	G5
R900	C1	H1
R920	C2	H3
R921	C1	H3
R930	C2	H3
R932	C2	H3
R940	C4	H5
R941	C4	H5
R943	C4	H5
R945	C4	H5
R949	C4	H5
R1020	C1	H3
R1021	C1	J3
R1022	C2	J3
R1026	C1	J3
R1040	C4	H5
R1044	C4	J4
R1047	C4	J5
R1120	B1	J3
R1122	B1	K3
R1140	B4	J5
R1142	B4	K5
R1225	B1	K3
R1226	B1	K3
R1240	B4	K5
R1241	B4	K5
S310	B3	H2
S340	B5	H4
S740	D4	F5
S1200A	B1	K2
S1200A	B1	K2
S1200B	B1	K2
S1200B	B1	K2
S1230A	B3	K4
S1230A	B4	K4
S1230B	B3	K4
S1230B	B4	K4
U510	F1	E2
U510	F5	E2
U520	F3	E2
U520	F5	E2
U640	D4	F5
U640	F5	F5
U710A	G4	F2
U710B	G4	F2
U710	G5	F2
U720	D2	F3
U720	F5	F3
VR541	F5	D4
VR932	C1	H3

Partial A1 also shown on diagrams 2, 5 and 13.

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P13	H1	H5
P98	A4	L3

Partial A3 also shown on diagrams 1, 2, 3, 5, 6, 8, 9, 10, 11, 12 and 13

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS1	A1	CHASSIS
DS2	A3	CHASSIS
J1	A1	CHASSIS
J2	A4	CHASSIS

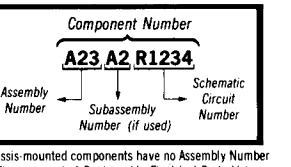
VOLTAGE CONDITIONS

Voltage Conditions: Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module or a TEKTRONIX 7D13 Digital Multimeter in a readout-equipped Tektronix 7000-series oscilloscope mainframe.

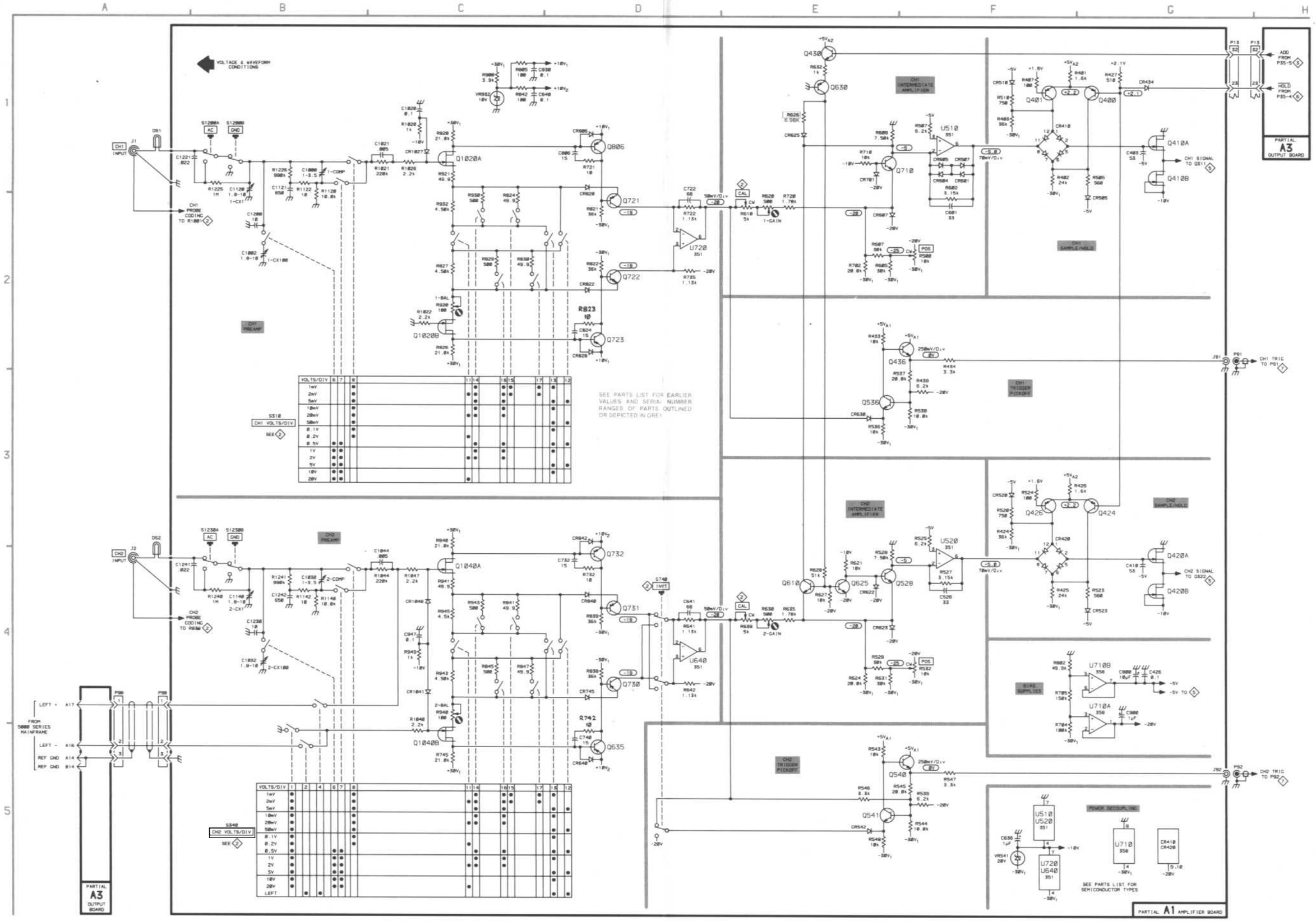
Set the 5D10 controls as follows: Push the GND pushbuttons for both channels and mechanically center both vertical channel POS controls. Check that −25 V to ground is present at the wiper contacts of the POS controls. If not, adjust the controls for −25 V.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



5D10

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SIGNAL ACQUISITION-CH1 AND CH2 4

DIGITIZER DIAGRAM 5

ASSEMBLY A1 *Figure 8-7 illustrates circuit board A1.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C230	G3	C4	Q226B	E2	B2	R201	E3	B1
C340	G3	C4	Q226C	E2	B2	R202	F2	B2
C427	F1	D3	Q226D	E1	B2	R204	F4	C2
C430	F1	D3	Q226E	E2	B2	R205	F4	C1
			Q310	F5	C2	R206	F4	C1
CR123	F2	A3	Q311	F5	C2	R239	F3	C3
CR130	E1	A3	Q312	E3	C2	R300	G5	C1
CR131	E2	B3	Q320	E3	C2	R301	G5	C1
CR133	E2	B3	Q321	G5	C2	R303	G5	C1
CR135	E2	B3	Q322	G5	C2	R304	G5	C1
CR230	E1	B3	Q323	E4	C2	R305	F5	C1
CR231	E2	B3	Q324	E4	C3	R308	F5	C1
CR233	E3	B3	Q325	F4	C3	R331	F3	C3
CR235	E3	B3	Q330	F4	C3	R340	H3	C4
CR237	E4	B3	Q331	G5	C3	R341	F5	C4
CR239	E4	C3	Q332	G5	C4	R342	H3	D4
CR323	G5	C3				R349	D1	C5
CR324	F5	C3	R100	F2	B1	R432	G4	D3
CR325	G5	C3	R101	F2	B1	R441	F4	D4
CR326	F5	C3	R102	E3	B1			
CR342	F5	D4	R103	E3	B2	RT200	F4	B2
CR440	F4	D4	R104	E2	B2			
			R105	E2	B2	U130A	D1	A4
P13	C2	D5	R106	E1	B2	U130B	D1	A4
P13	G1	D5	R107	F2	B2	U135	C1	B4
			R110	E1	A2	U135	C3	B4
Q110	F1	A2	R120	F1	A2	U145A	D2	B5
Q121A	E2	B2	R121	F2	A2	U145B	D2	B5
Q121B	E2	B2	R122A	E4	B3	U145	C3	B5
Q121C	E1	B2	R122B	E3	B3	U230	C3	B4
Q121D	E1	B2	R122C	E3	B3	U230	D1	B4
Q121E	E2	B2	R122D	E3	B3	U240A	D3	B5
Q210	E3	B2	R122E	E2	B3	U240B	D3	B5
Q211	E3	C2	R122F	E2	B3	U240	C3	B5
Q220	E3	B2	R122G	E1	B3	U245A	D3	C5
Q221	E3	C2	R122H	E1	B3	U245B	D4	C5
Q222	E3	B2	R122J	E1	B3	U245	C3	C5
Q223	E3	C3	R123	F1	A3	U330	G3	C4
Q224	E4	B3	R124	F1	A2	U330	G3	C4
Q225	E4	C3	R140	C1	B5			
Q226A	E2	B2	R200	E4	B1			

Partial A1 also shown on diagrams 2, 4 and 13.

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P13	C2	H5	U800	G1	J1	U940B	G1	K4
P13	G1	H5	U800	H2	J1			
P53	B2	J1	U940A	G1	K4			

Partial A3 also shown on diagrams 1, 2, 3, 4, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P53	B2	C1	P56	A1	G5	P56	B2	G5

Partial A5 also shown on diagrams 1, 2, 3, 6, 7, 8, 9, 10, 11, 12 and 13

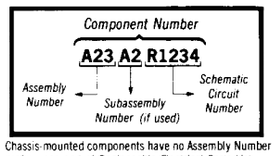
ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C520	B3	F3	Q420	B2	E3	R516	A3	E3
C521	A2	E3	Q421	A3	E3	R517	B3	F3
			Q422	A2	E3	R518	B3	F3
CR412	A3	E2	Q520	B2	F3	R519	B2	F3
CR413	A3	E2	Q521	B2	F3	R520	A2	E3
CR520	B3	E3				R522	B2	F3
CR521	B3	F3	R411	A2	E3	R530	B2	F3
CR522	B2	F3	R412	A2	E3	R632	B2	F3
CR530	B2	E3	R422	A2	E3			
			R430	A3	E3	U630C	B1	F3
P56	A1	E4	R431	A2	E3			
P56	B2	E4	R515	A2	E3			

Partial A6 also shown on diagrams 1, 2, 6, 7, 11, 12 and 13.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions: Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module or a TEKTRONIX 7D13 Digital Multimeter in a readout equipped Tektronix 7000-series oscilloscope mainframe.

Set the 5D10 controls as follows: Push the GND pushbuttons, mechanically center both vertical channel POS controls and press the SAVE pushbutton. Check that −25 V to ground is present at the wiper contacts of the POS controls. If not, adjust the controls for −25 V.

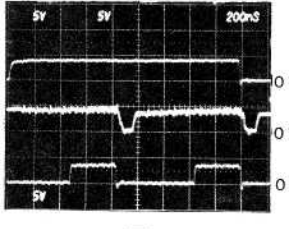
Waveform Conditions: Apply a 1 kHz sine-wave to either CH 1 or CH 2 of the 5D10. Press the CH 1 or CH 2 pushbutton for the channel selected. Set the VOLTS/DIV control on the 5D10 for a 6.5 division display. Center the display vertically with the POS control around the middle horizontal graticule line. Set the SECONDS/DIV control on the 5D10 to the 0.1 m position. Freerun (not triggered) the trigger.

Use a 50 MHz oscilloscope and a low-capacitance probe such as the P6106 probe connected to a 7A13 Differential Comparator Amplifier with a 7B50A Time Base and a 7603 Mainframe. The Differential Comparator Amplifier permits the voltage offsets shown by the photographs. An ac coupled vertical amplifier can be substituted with possible light low-frequency changes in the waveform pictures. The multiple trace photographs can be taken using a 7A18 Dual Trace Amplifier with two P6106 V probes, or the traces can be viewed individually.

For waveform pictures 6 through 10 trigger the test oscilloscope from the sinewave generator and for pictures 1 through 5 trigger the test oscilloscope on the Hold signal at the base of Q421 on the A6 board.

See Section 3, Theory of Operation, for further information.

1 2 3

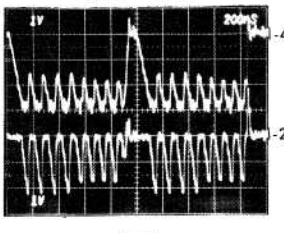


0 V HOLD A6Q421-B 1

0 V $\overline{\text{END}}$ A6Q422-B 2

0 V DIG 4 A6R431 3

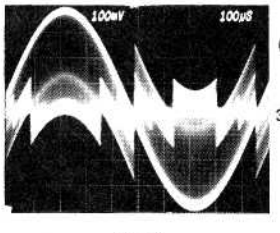
4 5



-4.9 V A6CR520-C 4

-2.4 V A6CR521-C 5

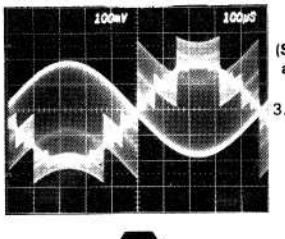
6



U330-4 (Similar waveform at U330-3)

3.5 V

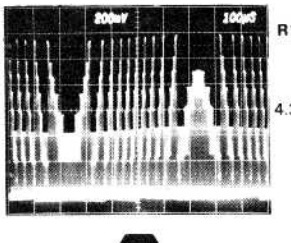
7



R239 - R107 (Similar waveform at R331 - R202)

3.9 V

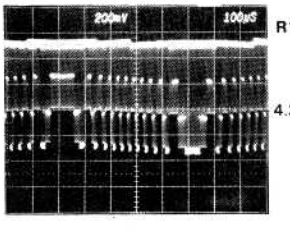
8



R107 - R101

4.3 V

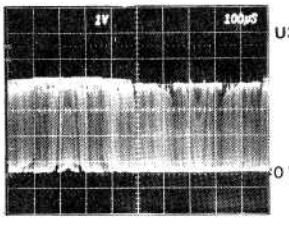
9



R100 - R202

4.3 V

10

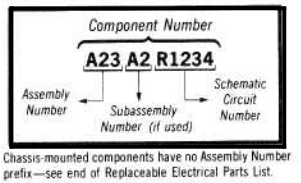


U330-9

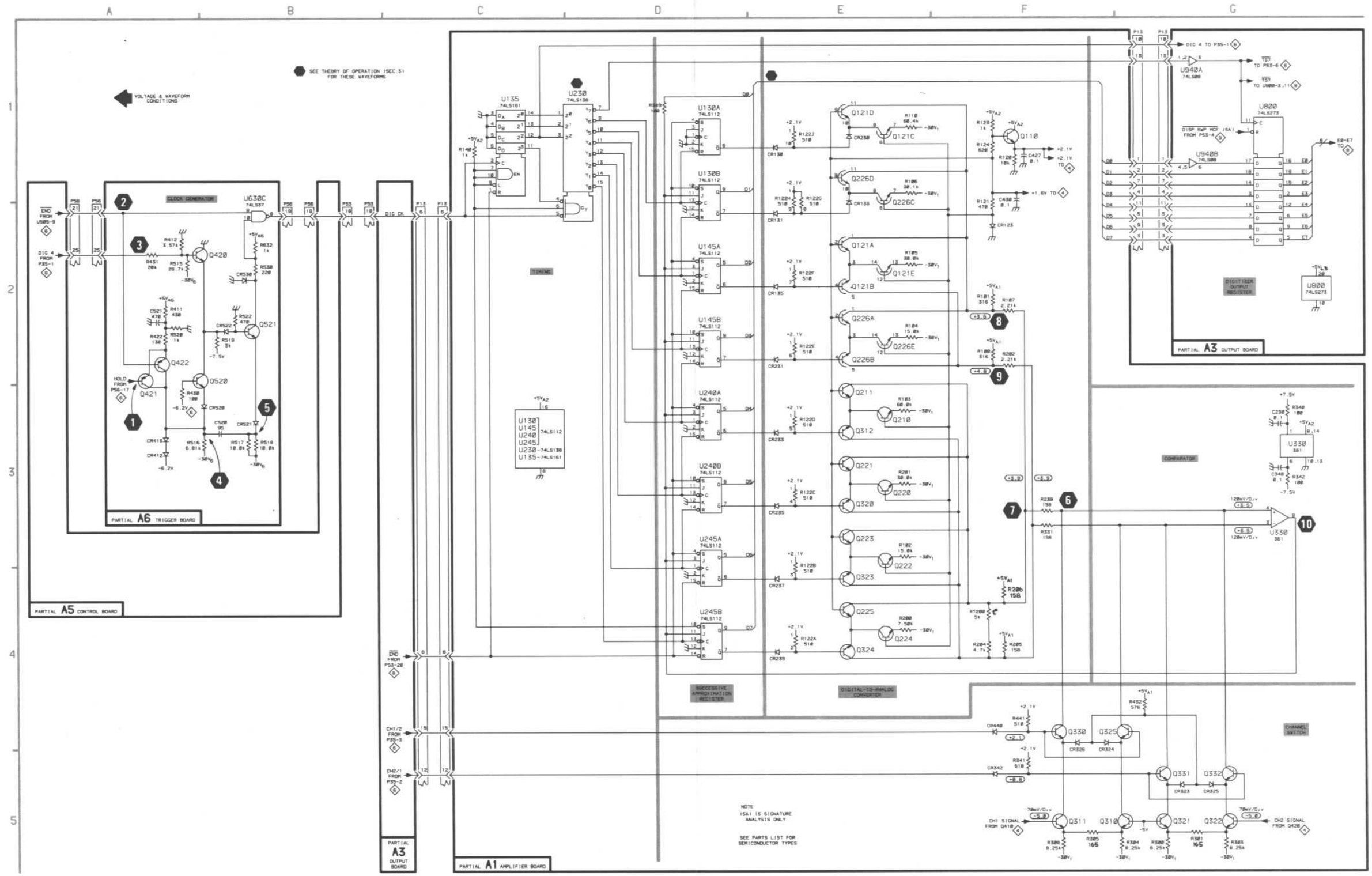
0 V at 0% line

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


SEE THEORY OF OPERATION (SEC. 5) FOR THESE WAVEFORMS
VOLTAGE & WAVEFORM CONDITIONS
CLOCK GENERATOR
TIMING
SUCCESSIVE APPROXIMATION REGISTER
DIGITAL-TO-ANALOG CONVERTER
COMPARATOR
CHANNEL SWITCH
DIGITIZER OUTPUT REGISTER
PARTIAL A6 TRIGGER BOARD
PARTIAL A5 CONTROL BOARD
PARTIAL A3 OUTPUT BOARD
PARTIAL A1 AMPLIFIER BOARD
NOTE
(SA) IS SIGNATURE ANALYSIS ONLY
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

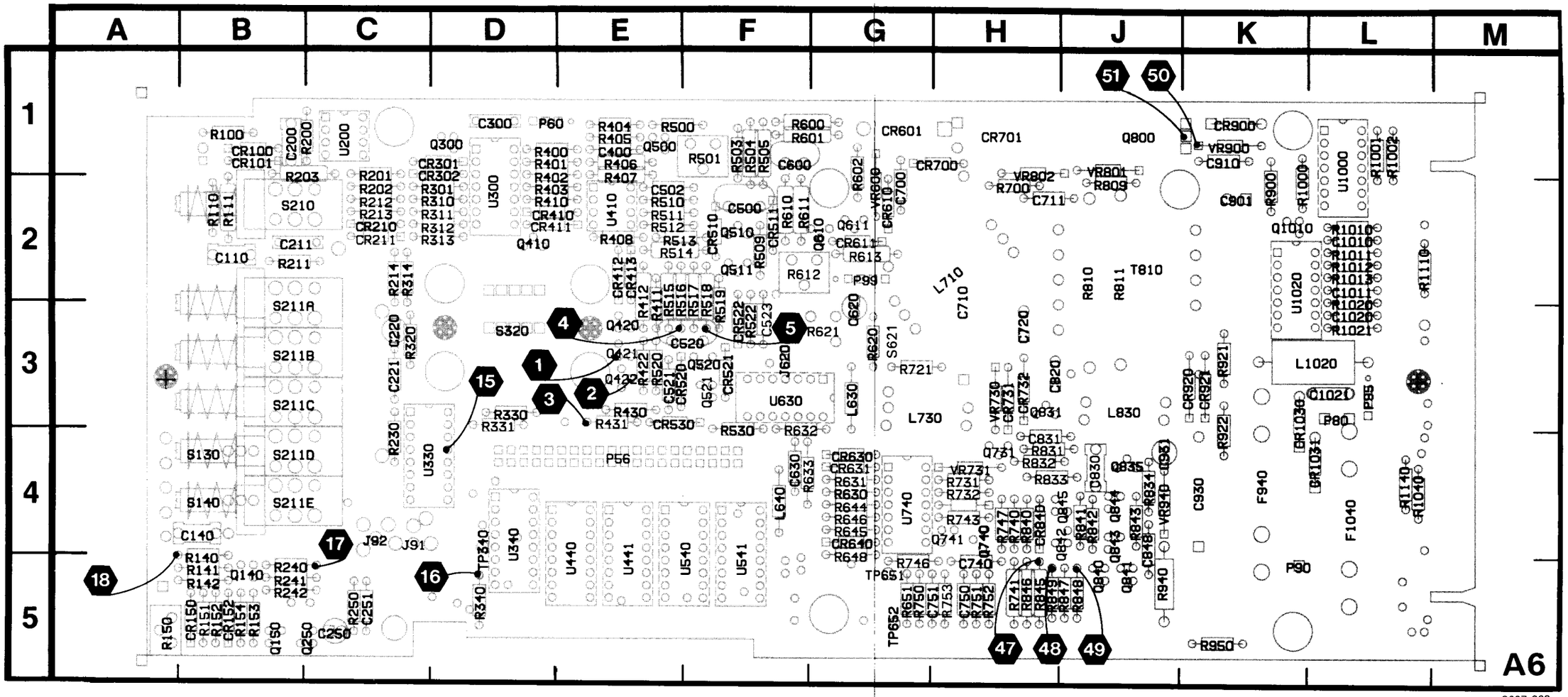
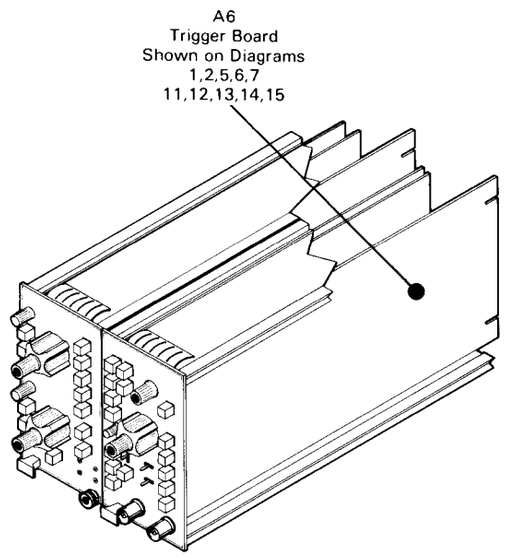


Figure 8-8. A6—Trigger circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TIME BASE AND DIGITIZER CONTROL DIAGRAM 6

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	H1	G1	P35	H2	G1	P53	H2	J1

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 8, 9, 10, 11, 12 and 13

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C500	G2	F1	R500	G2	F2	U605D	F1	G2
			R610	E1	F3	U700A	F1	H2
P35	H1	G1				U700B	E1	H2
P35	H2	G1	U505A	G2	F2	U705A	G1	H2
P53	H2	J1	U505B	G2	F2	U725C	E1	H4
P53	H2	J1	U600A	G2	E2			
P56	A1	G5	U600E	F1	E2	W330	A1	D5
P56	E1	G5	U600F	F1	E2			
P56	F3	G5	U605C	F1	G2			

Partial A5 also shown on diagrams 1, 2, 3, 5, 7, 8, 9, 10, 11, 12 and 13

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C523	A2	F3	R151	B4	B5	R1110	H3	L2
C600	A2	F1	R152	B4	B5			
C1010	F4	L2	R153	B3	B5	TP340	D1	D4
C1011	G4	L2	R154	B4	B5			
C1020	G4	L3	R600	A2	F1	U340	D1	D4
			R601	A2	F1	U440	C1	E5
CR150	B4	B5	R602	A2	G1	U441A	B2	E5
CR152	B4	B5	R610	A2	F2	U441B	B2	E5
CR610	A2	G2	R611	A2	F2	U540A	B2	F5
CR611	A2	G2	R612	A2	F2	U540B	C3	F5
			R613	A2	G2	U541A	C3	F5
P56	A1	E4	R621	A2	G3	U541B	D1	F5
P56	E1	E4	R633	A1	F4	U630D	A1	F3
P56	F3	E4	R900	G4	K2	U1000A	G4	L1
			R1000	H4	K2	U1000B	H4	L1
Q150	B4	B5	R1001	H3	L1	U1000C	G4	L1
Q610	A2	G2	R1002	H3	L1	U1000E	H4	L1
Q611	A2	G2	R1010	H4	L2	U1020A	G3	K2
Q1010	H4	K2	R1012	G4	L2	U1020B	G4	K2
			R1013	G4	L2			
R141	A4	B5	R1020	G4	L3	VR600	A2	G2
R142	A4	B5	R1021	H4	L3			

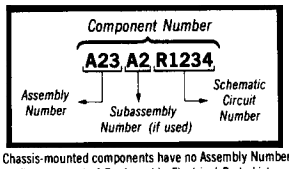
Partial A6 also shown on diagrams 1, 2, 5, 7, 11, 12 and 13.

CHASSIS MOUNTED PARTS

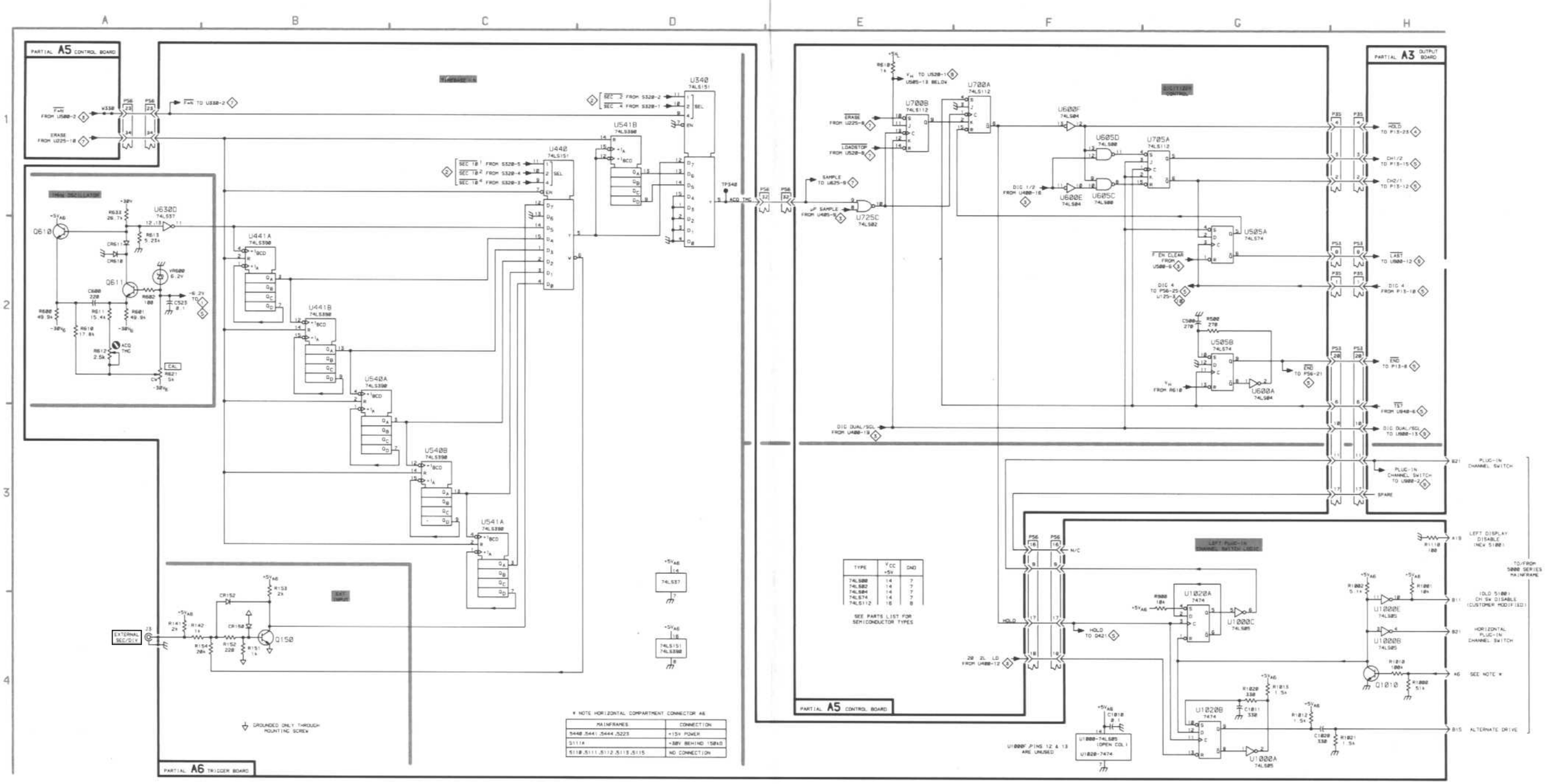
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J3	A4	CHASSIS						

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



5D10

3697-005

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TIMEBASE AND DIGITIZER CONTROL 6

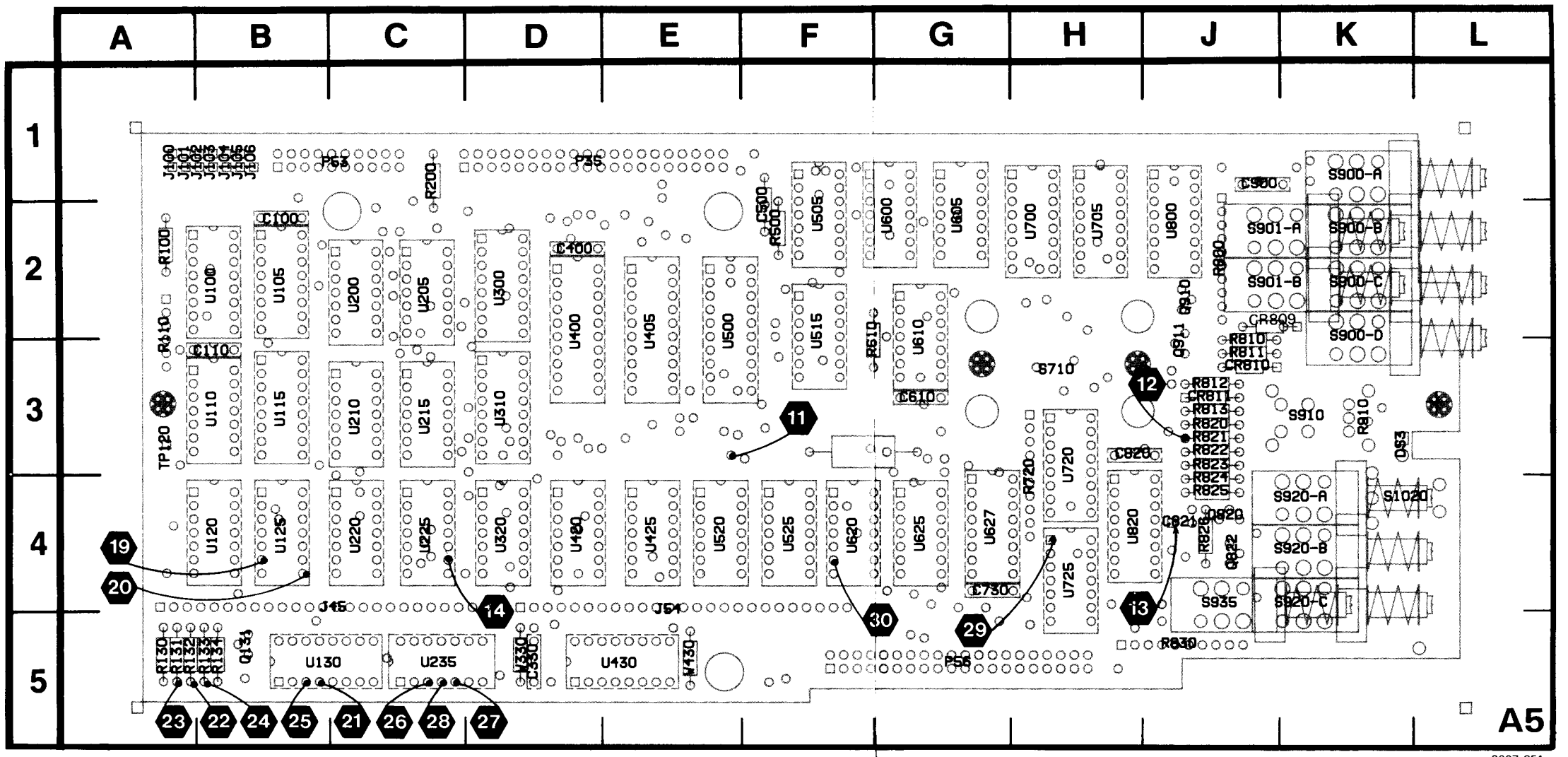
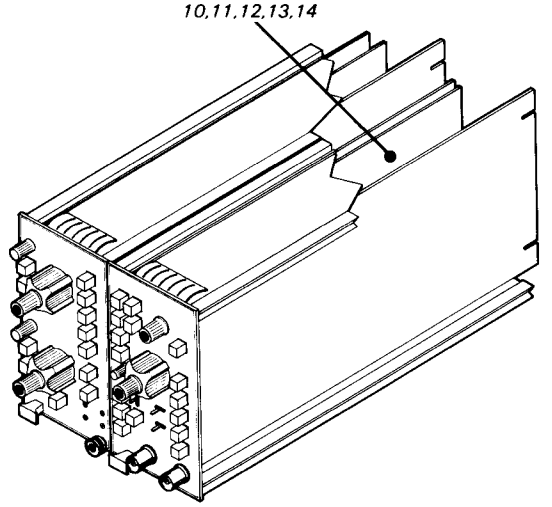
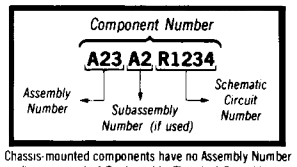


Figure 8-9. A5—Control circuit board assembly.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TRIGGERING DIAGRAM 7

ASSEMBLY A4 *Figure 8-6 illustrates circuit board A4.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J106	D4	A2	U250B	D4	B4	U550B	D5	E4
			U250D	D4	B4	U550C	D5	E4
P45	E3	B4	U260A	D4	B5	U560A	D5	E5
			U540A	D4	E3	U560C	D5	E5
U220A	C4	B2	U540C	C5	E3			
U250A	D5	B4	U550A	D4	E4			

Partial A4 also shown on diagrams 3, 8, 9, 10 and 13.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C821	G3	J4	R800H	G3	J2	S901B	A2	J2
			R800J	G3	J2	S910	F3	K3
CR809	A3	J2	R810	G3	J2			
CR810	G3	J3	R811	G3	J3	U225D	G4	C4
CR811	G3	J3	R812	G3	J3	U225E	G3	C4
			R813	G3	J3	U425A	F5	E4
DS3	H2	K3	R820	F3	J3	U430B	F4	E5
			R821	F3	J3	U520B	F4	E4
J45	E3	C4	R822	G3	J3	U525A	F4	F4
			R823	F3	J3	U525B	F5	F4
P56	B2	G5	R824	G3	J4	U525D	F4	F4
P56	E2	G5	R825	G2	J4	U600D	E4	E2
			R826	F4	J4	U610A	G2	G2
Q820	G3	J4	R910	F3	K3	U625C	F2	G4
Q822	F3	J4				U625D	G2	G4
Q910	G3	J2	S901A	A2	J2	U627B	F2	G4
Q911	G3	J2	S901A	A3	J2	U705B	E4	H2
			S901B	A2	J2			

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 8, 9, 10, 11, 12 and 13

ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C110	B1	B2	Q410	D3	D2	R406	C3	E1
C140	A2	B4	Q500	B3	E1	R407	C3	E1
C200	C1	B1				R408	C3	E2
C211	B2	B2	R100	B2	B1	R410	C3	D2
C220	B1	C3	R110	B1	B2	R500	B1	E1
C221	D2	C3	R111	B2	B2	R510	C3	E2
C250	E1	C5	R140	F1	B5	R511	B3	E2
C251	A1	C5	R200	B2	C1	R512	B4	E2
C300	C1	D1	R201	C1	C2	R620	B1	G3
C400	B4	E1	R202	C2	C2	R950	A1	K5
C502	C1	E2	R203	B1	B2			
C630	C1	F4	R211	B2	B2	S210	B1	B2
			R212	C2	C2	S211A	A1	B3
CR100	B2	B1	R213	C2	C2	S211A	A1	B3
CR101	B2	B1	R214	D3	C2	S211B	A1	B3
CR210	C2	C2	R230	D2	C4	S211B	A1	B3
CR211	C1	C2	R240	F1	B5	S211C	A1	B3
CR301	C2	D1	R241	F1	B5	S211C	A1	B3
CR302	C2	D2	R242	E1	B5	S211D	A1	B4
CR410	C2	D2	R250	E1	C5	S211D	A1	B3
CR411	C2	D2	R301	C1	D2	S211E	A1	B4
			R310	C2	D2	S211E	A2	B3
J91	A1	C4	R311	C2	D2			
J92	A1	C4	R312	D2	D2	U200	C2	C1
			R313	C2	D2	U200	D1	C1
L640	B1	F4	R314	D1	C2	U300A	D2	D2
			R320	E1	C3	U300B	D3	D2
P56	B2	G5	R330	C3	D3	U300	D1	D2
P56	E2	G5	R331	C2	D3	U330A	D2	C4
P60	B3	D1	R340	E1	D5	U330B	E1	C4
P91	A1	C4	R400	B3	D1	U330	D1	C4
P92	A1	C4	R401	C3	D1	U410A	C3	E2
			R402	D1	D2	U410B	B4	E2
Q140	F1	B5	R403	C1	D2	U410	C1	E2
Q250	E1	C5	R404	C3	E1			
Q300	D2	D1	R405	B3	E1			

Partial A6 also shown on diagrams 1, 2, 5, 6, 11, 12 and 13.

CHASSIS MOUNTED PARTS

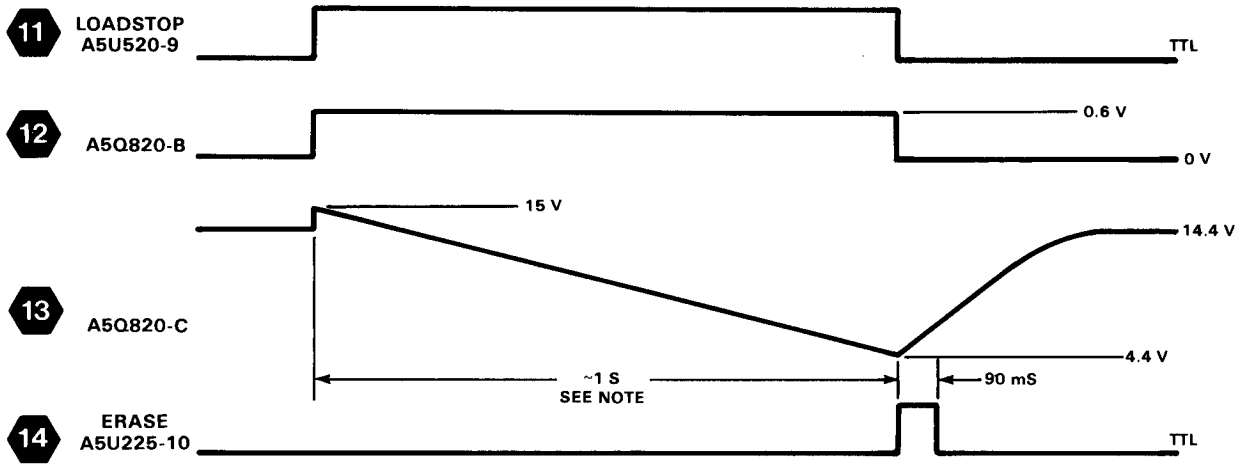
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS3	H2	CHASSIS	J4	A2	CHASSIS			
DS4	A2	CHASSIS						
DS5	H1	CHASSIS	R1	A4	CHASSIS			

WAVEFORM CONDITIONS

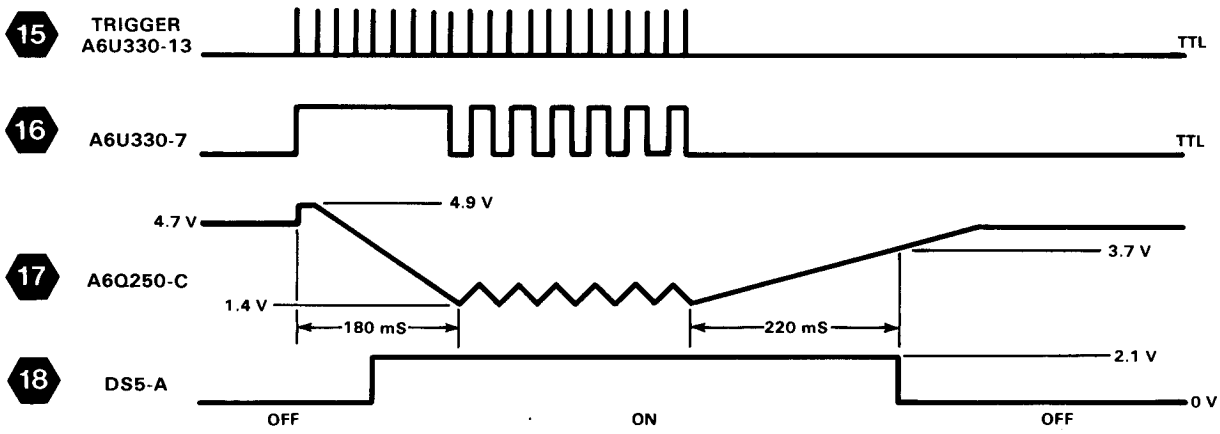
Waveform Conditions: To view the waveforms on this schematic use a digital storage oscilloscope such as a 5D10 operating in a 5110 Mainframe.

For the TRIG'D Indicator Waveforms, trigger the test oscilloscope on the waveform at U330 pin 7, located on the A6 Trigger board. Press the LINE SOURCE pushbutton. Press either SLOPE pushbutton and adjust the LEVEL control for a signal similar to the waveform shown at U330 pin 13. Obtain the pulse bursts by pressing the EXT and then the LINE pushbutton.

To obtain the Viewtimer Waveforms, trigger the test oscilloscope on the Loadstop signal at U520 pin 9. Press the LINE SOURCE and CTR TRIG pushbuttons. Set the SECONDS/DIV switch to the 0.1 (seconds) position. Turn the VIEWTIME control fully ccw.

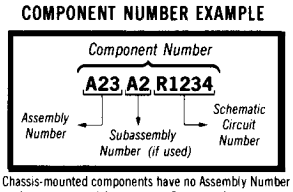


NOTE: VIEWTIME VARIES FROM APPROXIMATELY ONE SECOND MINIMUM (FULLY CCW) TO INFINITY.

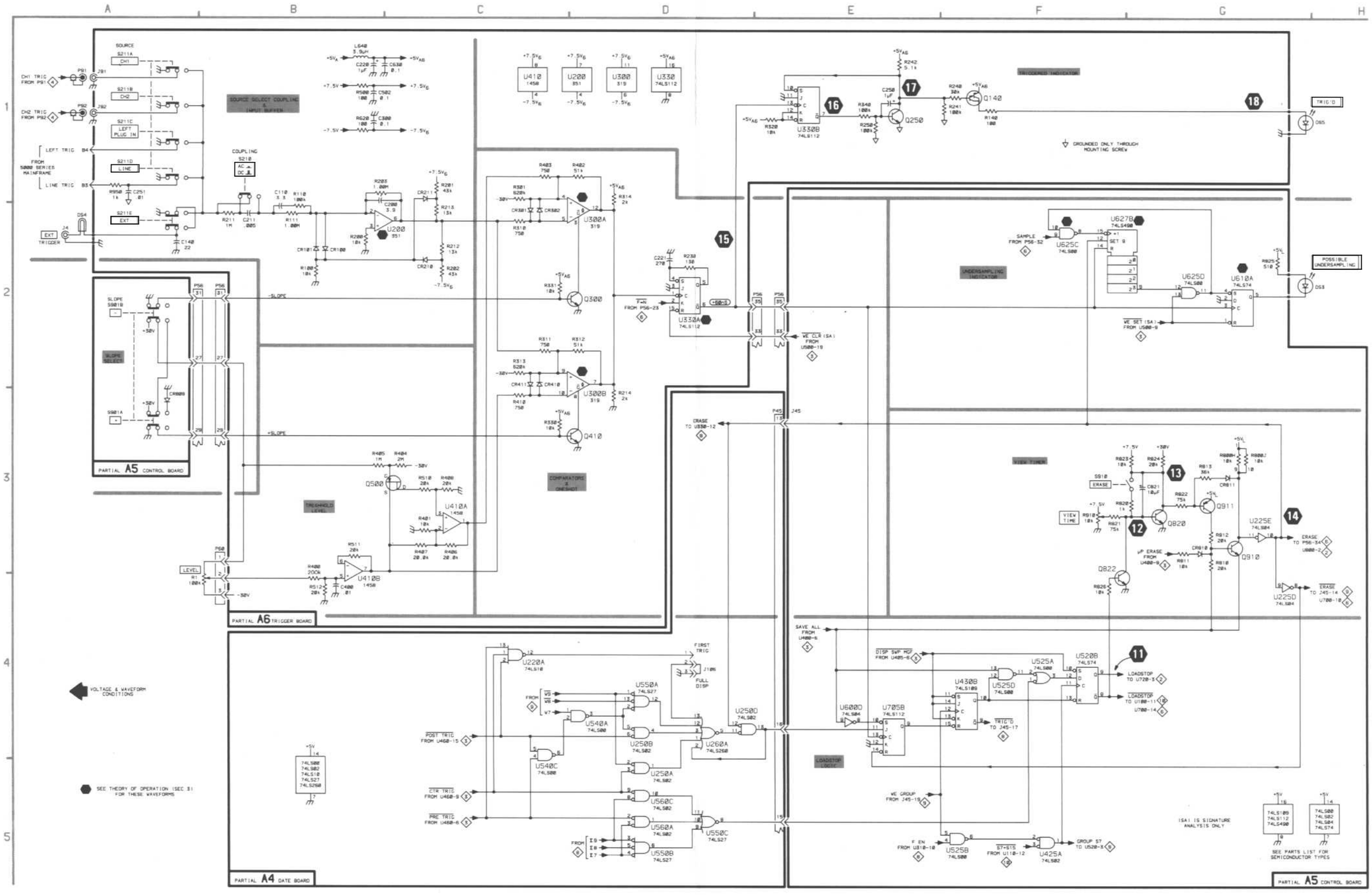


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


SOURCE SELECT COUPLING & INPUT BUFFER
TRIGGERED INDICATOR
UNDERSAMPLING INDICATOR
SLOPE SELECT
PARTIAL A5 CONTROL BOARD
TRESHOLD LEVEL
COMPARATORS & ONESHOT
VIEW TIMER
PARTIAL A6 TRIGGER BOARD
LOADSTOP LOGIC
PARTIAL A4 DATE BOARD
PARTIAL A5 CONTROL BOARD
VOLTAGE & WAVEFORM CONDITIONS
SEE THEORY OF OPERATION (SEC 3) FOR THESE WAVEFORMS
GROUNDED ONLY THROUGH MOUNTING SCREW
ISA) IS SIGNATURE ANALYSIS ONLY
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

MEMORY ADDRESSES DIAGRAM 8

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P34	E2	H3	U700	G2	H1	U1010	G2	L2
P35	G1	G1	U910	G2	K2	U1020	G2	L2
P53	G1	J1	U940D	G1	K4			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 9, 10, 11, 12 and 13

ASSEMBLY A4 *Figure 8-6 illustrates circuit board A4.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P34	E2	F1	U320D	B3	C2	U650	B5	F4
P34	H5	F1	U340A	A3	C3	U710	D3	G2
P45	A1	B4	U350A	B3	C4	U720	D4	G2
P45	A3	B4	U350B	B4	C4	U730	D4	G3
P54	A2	E4	U350C	B3	C4	U740	G4	G3
			U410	C3	D2	U750	G5	G4
R160	C1	A5	U420	C4	D2	U810	D1	H2
R830	D3	H3	U430	C4	D3	U820	D2	H2
R830	F5	H3	U510	E3	E2	U840A	D1	H3
			U520	E4	E2	U840C	D3	H3
U210C	B3	B2	U530	E4	E3	U840D	B4	H3
U220B	C3	B2	U610	B1	F2	U850A	A3	H4
U220C	F4	B2	U620	B1	F2	U850B	A3	H4
U240A	C1	B3	U630	B2	F3	U850D	B4	H4
U250C	C2	B4	U640	B4	F3	U900	D1	H1

Partial A4 also shown on diagrams 3, 7, 9, 10 and 13.

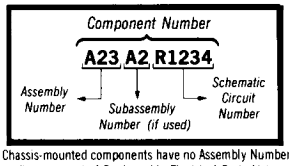
ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	G1	D1	R134	A5	B5	U310B	F1	D3
P53	G1	C1				U420C	G1	D4
			U310A	F1	D3			

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 9, 10, 11, 12 and 13

Static Sensitive Devices
See Maintenance Section

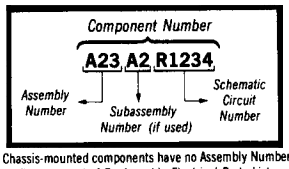
COMPONENT NUMBER EXAMPLE



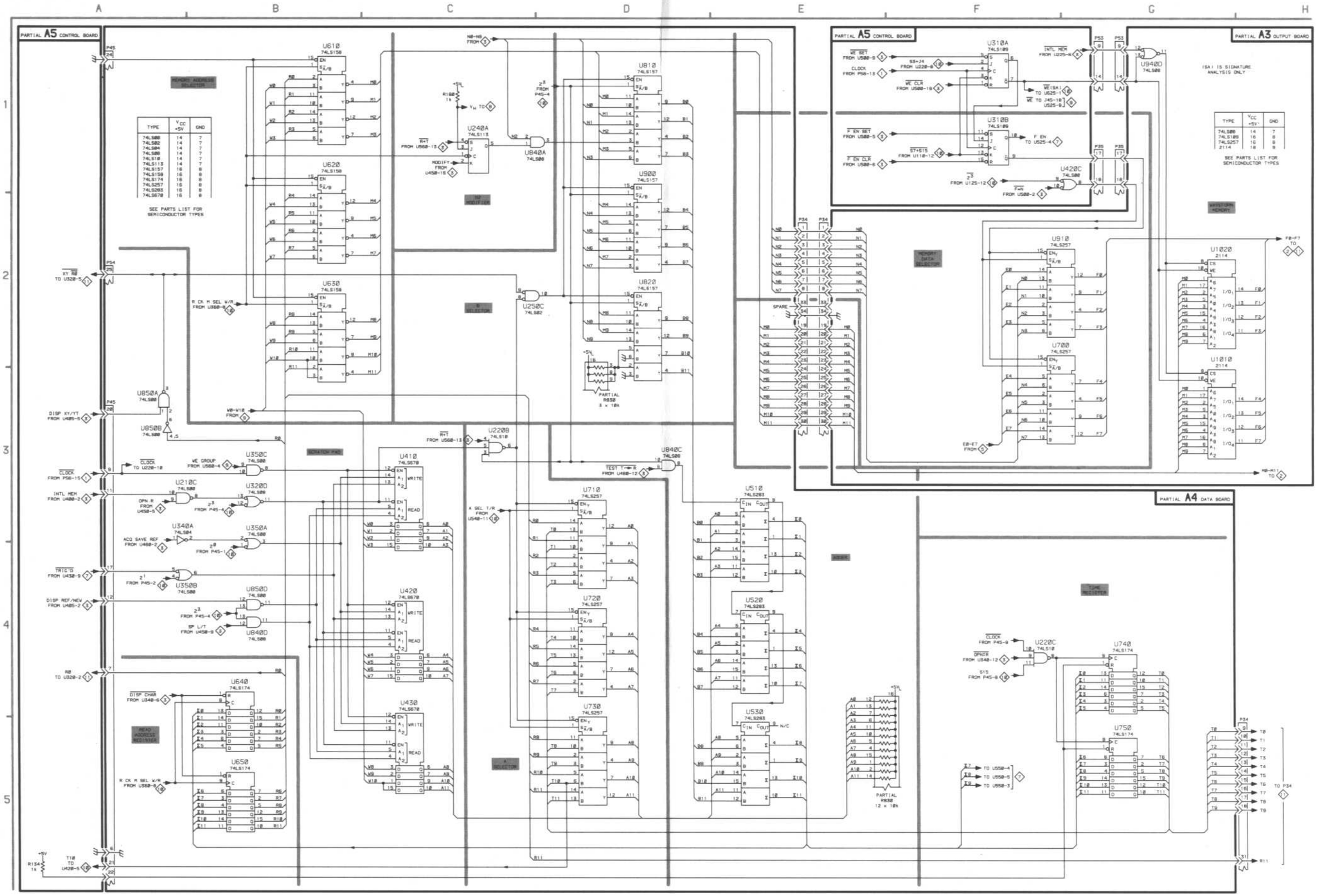
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



TYPE	V_{CC} +5V	GND
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS00	14	7
74LS10	14	7
74LS113	14	7
74LS157	16	8
74LS158	16	8
74LS174	16	8
74LS257	16	8
74LS283	16	8
74LS670	16	8

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

TYPE	V_{CC} +5V	GND
74LS00	14	7
74LS109	16	8
74LS257	16	8
2114	18	9

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

WRITE ADDRESS COUNTER DIAGRAM 9

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P53	A3	J1	U900A	B2	K1	U940C	B3	K4
P53	C3	J1	U900B	B3	K1			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 8, 10, 11, 12 and 13

ASSEMBLY A4 *Figure 8-6 illustrates circuit board A4.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P45	D1	B4	U210D	E2	B1	U320B	E3	C2
P45	D3	B4	U230A	E4	B3	U320C	E3	C2
P54	D1	E4	U230B	F4	B3	U330A	D3	C3
			U240B	E4	B3	U330B	E3	C3
U210A	E2	B1	U310	E2	C2	U560B	F1	E5
U210B	E2	B1	U320A	E2	C2	U850C	E1	H4

Partial A4 also shown on diagrams 3, 7, 8, 10 and 13.

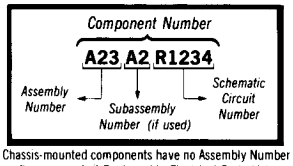
ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P53	A3	C1	R610	C3	F3	U525C	D3	F4
P53	C3	C1	U520A	C3	E4			

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 8, 10, 11, 12 and 13

Static Sensitive Devices
See Maintenance Section

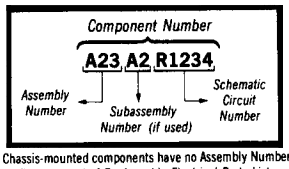
COMPONENT NUMBER EXAMPLE



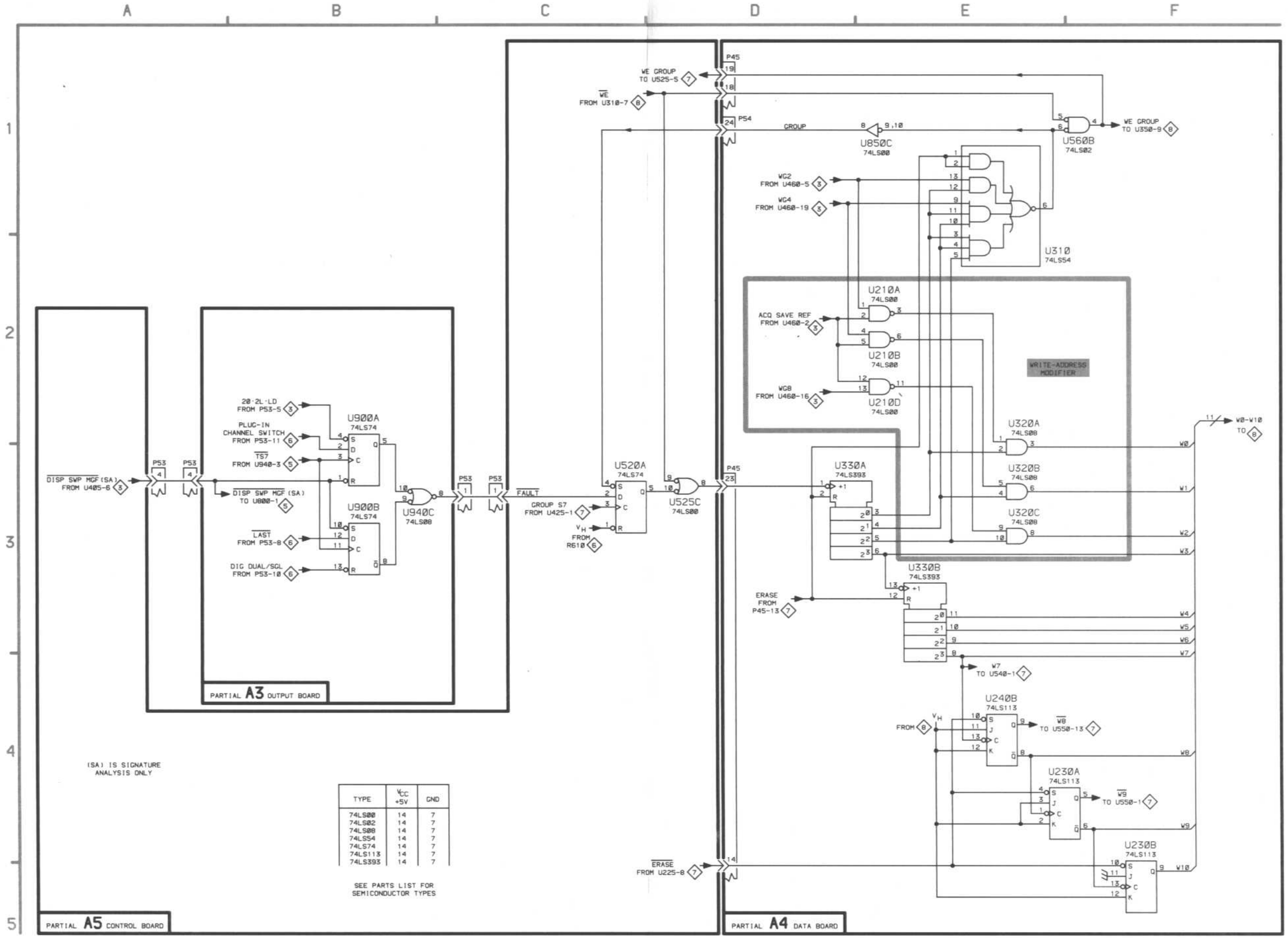
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



TYPE	V_{CC} +5V	GND
74LS00	14	7
74LS02	14	7
74LS08	14	7
74LS54	14	7
74LS74	14	7
74LS113	14	7
74LS393	14	7

READ AND WRITE CONTROL DIAGRAM 10

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	A1	G1	P35	A3	G1	P53	A2	J1

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 8, 9, 11, 12 and 13.

ASSEMBLY A4 *Figure 8-6 illustrates circuit board A4.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATIoN	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P45	F1	B4	U340B	F1	C3	U360B	G2	C5
P45	G2	B4	U340D	G1	C3	U360C	G1	C5
P54	G1	E4	U340E	G2	C3	U540C	G1	E3
			U350D	F1	C4	U540D	G1	E3
U260B	F2	B5	U360A	G2	C5			

Partial A4 also shown on diagrams 3, 7, 8, 9 and 13.

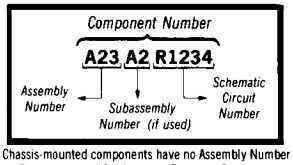
ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J102	E3	B1	U110C	D2	B3	U220C	G4	C4
J103	E3	B1	U115	F1	B3	U220D	B1	C4
J104	E2	B1	U120A	E2	B4	U225F	D4	C4
J105	E2	B1	U120B	F4	B4	U320C	B3	D4
J106	E2	B1	U125A	B1	B4	U320D	E2	D4
			U125B	B2	B4	U420A	B1	D4
P35	A1	D1	U125D	F3	B4	U420B	B2	D4
P35	A3	D1	U125E	F4	B4	U420D	B1	D4
P53	A2	C1	U125F	F3	B4	U425B	G1	E4
			U200A	E3	C2	U425C	F3	E4
R100	C1	A2	U200B	D4	C2	U425D	D2	E4
R110	E1	A2	U200D	C1	C2	U430A	C2	E5
			U205A	C2	C2	U515B	B3	F2
U100A	C3	B2	U205B	B1	C2	U600C	B2	E2
U100B	C2	B2	U210A	F4	C3	U605A	B1	G2
U105A	C1	B2	U210B	E2	C3	U605B	B1	G2
U105B	D4	B2	U215A	D2	C3	U625A	A4	G4
U110A	F4	B3	U220A	D3	C4	U627A	B3	G4
U110B	D3	B3	U220B	F3	C4	U725D	A1	H4

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 8, 9, 11, 12 and 13.

Static Sensitive Devices
See Maintenance Section

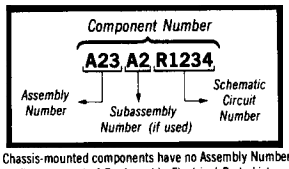
COMPONENT NUMBER EXAMPLE



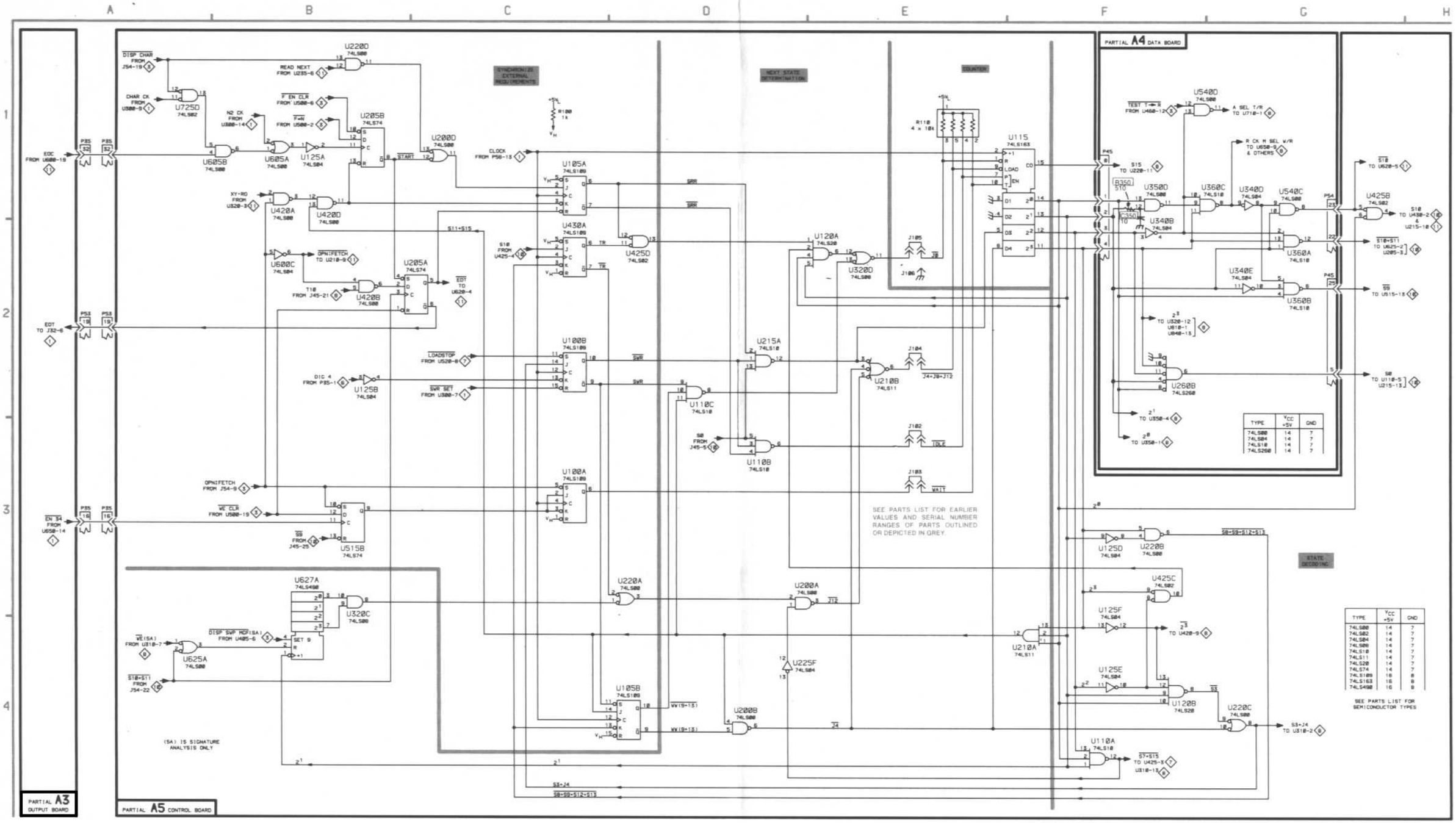
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



5D10

3687-009
REV APR 1985

READ AND WRITE CONTROL 10

DISPLAY REGISTERS, DACS and TIMER DIAGRAM 11

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C310	C1	D1	R405	D3	E1	U410	C4	E2
C326	C3	D2	R405	D3	E1	U410	D1	E2
C405	D1	D1	R406	D1	E1	U425	C4	E3
C510	F3	F2	R407	F3	E1	U425	F3	E3
C530	F1	F3	R408	E2	E1	U520	B4	F2
			R411	E2	E2	U520	D3	F2
P34	B1	H3	R426	F3	E3	U530	C4	F3
P34	B1	H3	R500	D3	F1	U530	F1	F3
P35	B2	G1	R501	F1	E1	U600	E2	G1
P35	C5	G1	R502	E1	E1	U610C	G2	G2
P35	G4	G1	R503	E1	F1	U610	C5	G2
			R504	E2	F1	U710B	F2	H2
Q230	B4	C3	R505	E2	F1	U710D	D1	H2
			R506	E2	F1	U710F	D3	H2
R230	B4	C3	R507	E2	F1	U720	C3	H2
R231	B4	C3	R508	E2	F1	U810	C1	J2
R301	D1	D1	R512	E3	F2	U820	C2	J2
R302	F3	D1	R513	E3	F2	U920	C2	K2
R351	C1	D5	R521	G2	F3			
R352	C3	D5	R522	G2	F3	VR224	B4	C3
R402	F3	E1	R532	F1	F4			
R403	F2	E1	R533	F1	F4			
R404	F1	E1	R711	C1	H2			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 8, 9, 10, 12 and 13.

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	B2	D1	S920C	A1	K4	U235D	D4	C5
P35	C5	D1	S920C	A2	K4	U320A	F4	D4
P35	G4	D1				U320B	A3	D4
P56	G5	G5	U130A	E4	B5	U515A	D5	F2
			U130B	E4	B5	U600B	A2	E2
Q131	E4	B5	U210C	D4	C3	U620A	D4	F4
			U215B	B3	C3	U620B	F5	F4
R130	E4	A5	U215C	B3	C3	U625B	F5	G4
R131	E4	A5	U225A	E5	C4	U725A	G4	H4
R132	E5	A5	U225B	A4	C4	U725B	F4	H4
R133	E4	B5	U235A	E4	C5			
R830J	B2	J5	U235B	F4	C5	W430	F4	E5
			U235C	E5	C5			

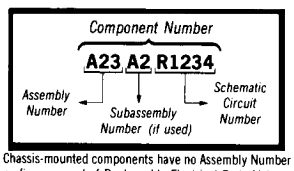
Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 8, 9, 10, 12 and 13.

ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P56	G5	E4	R1011	G5	L2	U1000D	G5	L1

Partial A6 also shown on diagrams 1, 2, 5, 6, 7, 12 and 13.

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

VOLTAGE AND WAVEFORM CONDITIONS

Voltage Conditions: Use a digital voltmeter with a 10 MΩ input impedance such as the TEKTRONIX DM 501A Digital Multimeter installed in a TM 500- or TM 5000-series power module, or a TEKTRONIX 7D13 Digital Multimeter in a readout equipped Tektronix 7000-series oscilloscope mainframe.

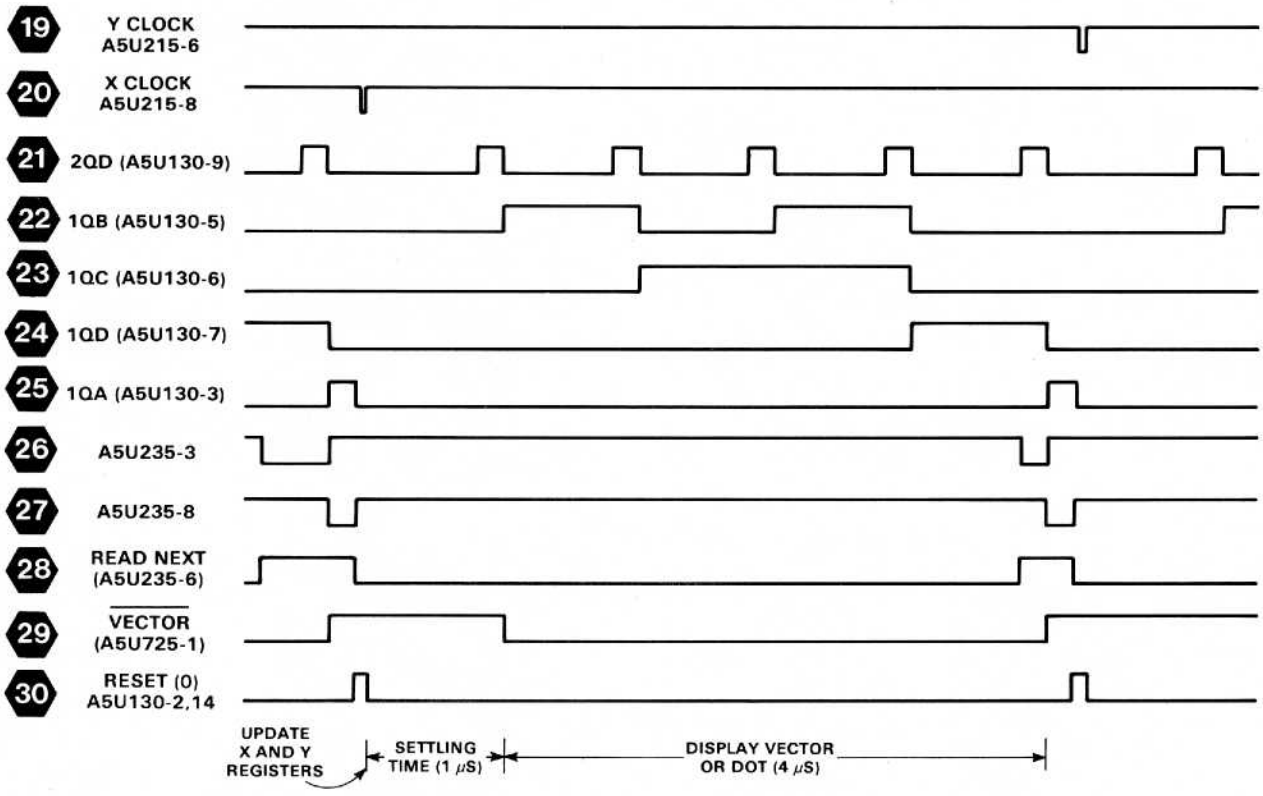
Waveform Conditions: Before applying power to the 5D10, press the SAVE pushbutton. Then apply power. The self-test pattern should be displayed.

Use a 50 MHz oscilloscope and a low-capacitance probe such as the P6106 probe connected to a 7A18 Amplifier with a 7B50 Time Base and a 7603 Mainframe.

Trigger the test oscilloscope on the signal at U710C pin 6 shown on schematic 12. This component is located on the A3 Output board.

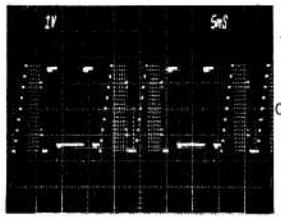
To view the waveform drawings, trigger the oscilloscope on the Y Clock signal at U215 pin 6, located on the A5 Control board. All waveform diagram levels are TTL.

DISPLAY TIMER WAVEFORMS



SN B020100 & up.

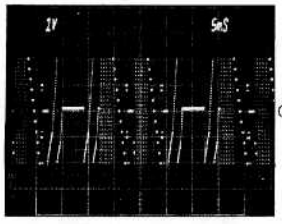
31



A3U530-6

0 V (50%)

32

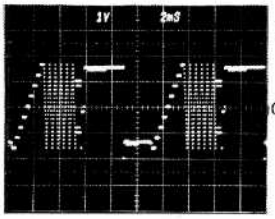


A3U425-6

0 V (50%)

SN B020099 & below.

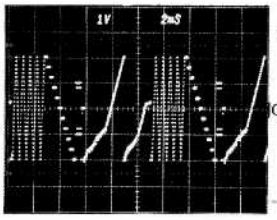
31



A3U530-6

0 V (50%)

32

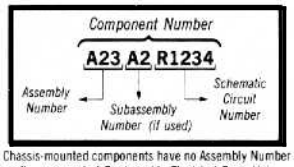


A3U425-6

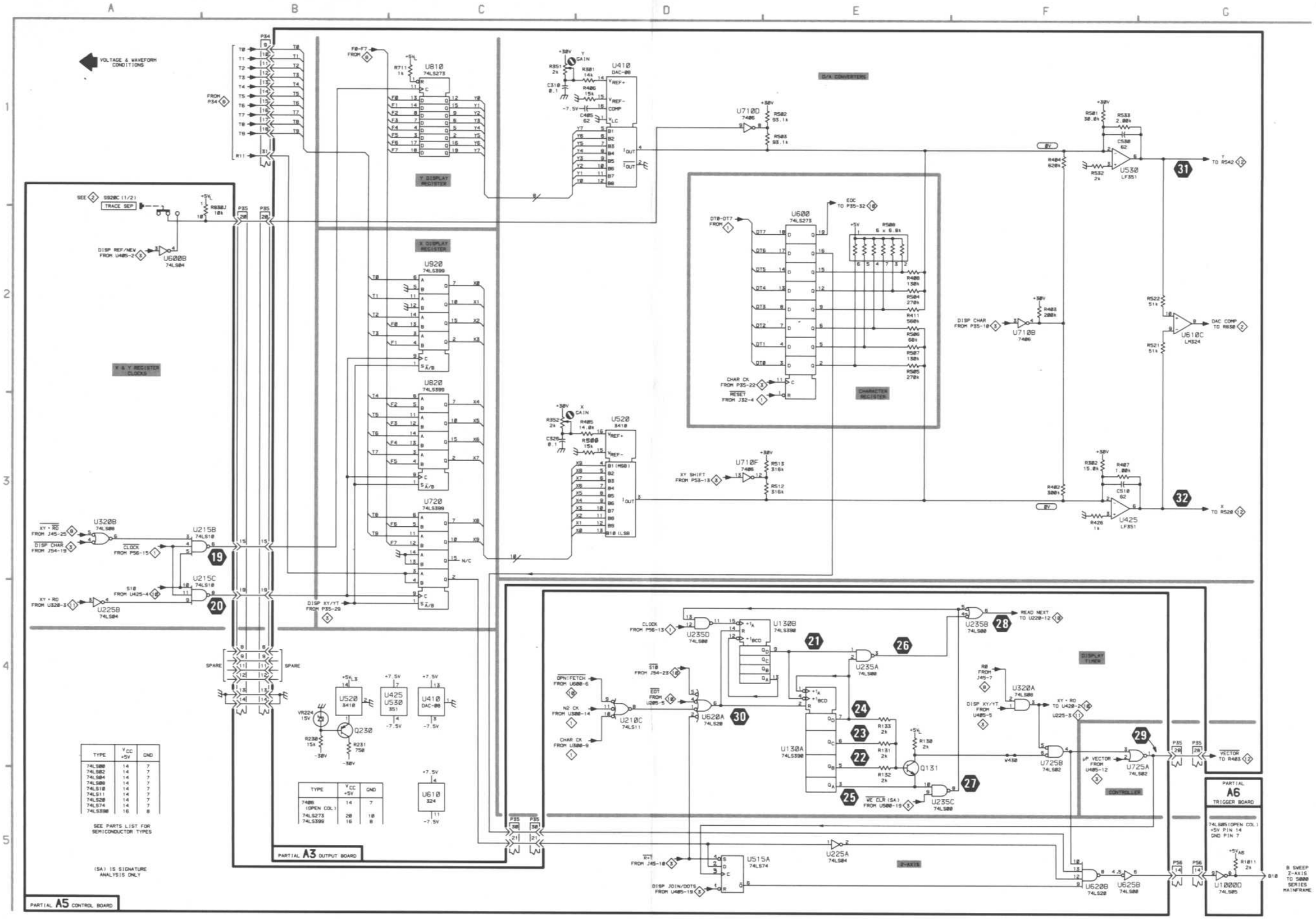
0 V (50%)

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List


VOLTAGE & WAVEFORM CONDITIONS
Y DISPLAY REGISTER
X DISPLAY REGISTER
X & Y REGISTER CLOCKS
D/A CONVERTERS
CHARACTER REGISTER
DISPLAY TIMER
CONTROLLER
Z-AXIS
PARTIAL A3 OUTPUT BOARD
PARTIAL A5 CONTROL BOARD
PARTIAL A6 TRIGGER BOARD
SPARE
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
(SA) IS SIGNATURE ANALYSIS ONLY
B SWEEP Z-AXIS TO 5000 SERIES MAINFRAME

DISPLAY OUTPUT DIAGRAM 12

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C200	E4	C1	R141	F4	B4	U230	B5	C3
C210	E4	C2	R150	F3	A5	U230	E4	C3
C230	C3	C4	R151	F5	B5	U330	B5	D3
C240	C4	D4	R152	F5	B5	U330	E3	D3
C300	E4	C2	R153	F3	B5	U350A	B2	D5
C320	C4	D3	R154	F3	B5	U350B	E2	D5
C331	E3	D3	R155	F2	B4	U350C	E4	D5
C332	C2	D3	R200	D1	C1	U350D	B4	D5
C340	E2	D4	R220	E4	C2	U350	C5	D5
C349	C3	C4	R221	D4	C3	U430	B4	E3
C350	C2	D5	R222	D4	C3	U430	B5	E3
C351	C4	D5	R223	E4	C3	U435A	B3	E4
C440	E2	D4	R239	E4	B4	U435B	C3	E4
C451	C2	E5	R240	E4	C5	U435C	C4	E4
C531	B4	F4	R241	E4	C5	U435D	B4	E4
C541	C4	F5	R242	E3	C5	U435	C5	E4
C543	C4	F5	R250	E3	C5	U440A	D3	E4
C550	B3	F4	R251	F4	C5	U440B	D3	E4
			R304	A2	D1	U440C	D4	E4
CR100	D1	B1	R320	C4	D3	U440D	D4	E4
CR200	D1	C1	R324	D3	D3	U440	C5	E4
CR240	F1	C4	R325	E3	D3	U445	B5	E5
CR305	A2	D1	R326	E3	D2	U445	C3	E5
CR427	D1	E3	R327	E3	D2	U450	B5	E5
CR430	D1	E3	R350	C3	D5	U450	C4	E5
			R400	A2	E1	U550	B3	F5
J5	F2	A4	R401	A2	E1	U550	B5	F5
J6	F4	A5	R425	D3	E2	U610A	B1	G2
J7	F1	A5	R427	D1	E3	U610B	B1	G2
J8	F1	A5	R428	D1	E3	U610D	B1	G2
			R431	B4	E3	U610	B5	G2
K230	F1	C4	R432	C2	E3	U620A	D2	G2
			R451	E4	E5	U620B	B2	G2
P35	E5	G1	R452	E3	E5	U620C	B2	G2
P95	F4	B5	R509	B1	F1	U620D	B2	G2
P96	F3	L4	R510	B2	F2	U620	B5	G2
P96	F3	L4	R520	B4	F3	U710A	F1	H2
			R530	B4	F3	U710C	A1	H2
Q225	E4	C2	R531	B4	F3	U710E	A2	H2
Q226	E4	C3	R540	B3	F4	U710	C5	H2
Q310	A2	D1	R541	B3	F4			
Q311	A2	D1	R542	B3	F4	VR130	F2	B3
Q325	E2	D3	R543	C4	F5	VR131	F2	B4
Q326	E3	D2	R551	D4	E5	VR140	F4	B4
			R552	D3	F5	VR250	F4	C5
R100	D1	B1	R553	B3	F4			
R140	F2	B4	R710	B1	H2			

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 8, 9, 10, 11 and 13.

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P35	E5	D1	P56	E5	G5			

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 8, 9, 10, 11 and 13.

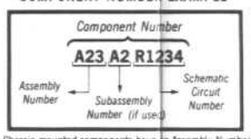
ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P56	E5	E4	R150	E5	A5			
P95	F4	L3						

Partial A6 also shown on diagrams 1, 2, 5, 6, 7, 11 and 13.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

WAVEFORM CONDITIONS

Waveform Conditions: Use a 50 MHz oscilloscope and a low-capacitance probe such as the P6106 probe connected to a 7A18 Dual Trace Amplifier with a 7B50 Time Base and a 7603 Mainframe. The multiple trace photographs can be taken using two 7A18 Dual Trace Amplifiers with four 6106 probes, or the traces can be viewed individually.

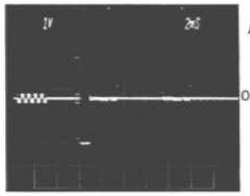
Trigger the test oscilloscope on U710C pin 6 located on the A3 Output board.

Before applying power to the 5D10, press the SAVE pushbutton. Then apply power. The self-test pattern should be displayed.

Use a digital storage oscilloscope such as a 5D10 operating in a 5110 Mainframe to view the X and Y, pinlift and the waveforms at U620 pins 1 and 2 in the dots and join modes.

SN B020100 & up.

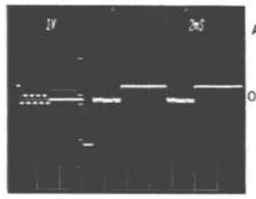
33



A3U430-6

0 V (50%)

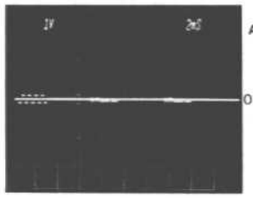
34



A3U450-6

0 V (50%)

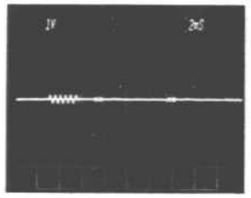
35



A3U440-10

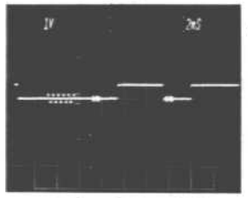
0 V (50%)

36



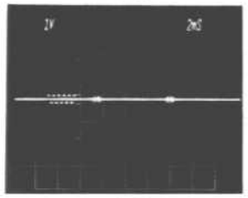
A3U550-6

37



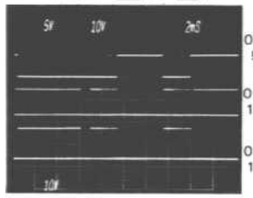
A3U445-6

38



A3U440-2

39 40 41



0 V (90%) 5 V/div — DISP. JOIN/DOTS A3U710-6 39

0 V (50%) 10 V/div — VECTOR A3U620-5 40

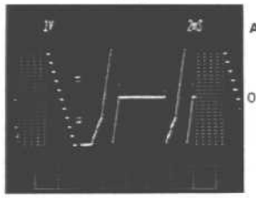
0 V (10%) 10 V/div — A3U620-10 41

42

A3U330-6

0 V (50%)

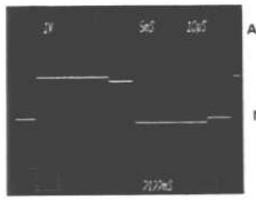
43



A3U230-6

0 V (50%)

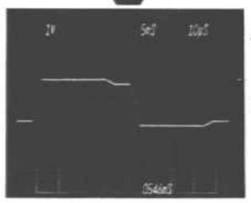
43



A3U230-6

BOX PATTERN (PARTIAL) DURING DOT DISPLAY. NOTE FAST TRANSITIONS.

43

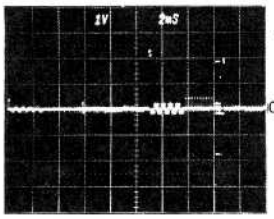


A3U230-6

BOX PATTERN (PARTIAL) DURING JOIN DOTS DISPLAY. NOTE TRANSITION TIMES OF 4 μS.

SN B020099 & below.

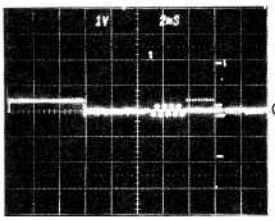
33



A3U430-6

0 V (50%)

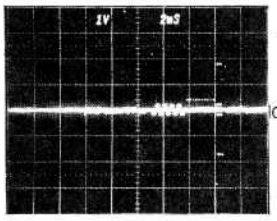
34



A3U450-6

0 V (50%)

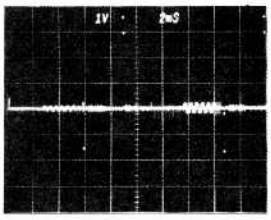
35



A3U440-10

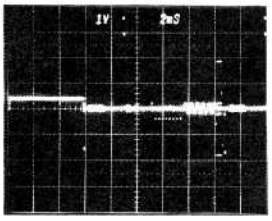
0 V (50%)

36



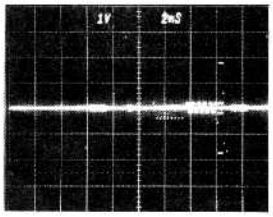
A3U550-6

37



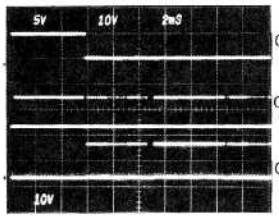
A3U355-6

38



A3U440-2

39 40 41



0 V (90%)
5 V/div

DISP. JOIN/DOTS
A3U710-6 39

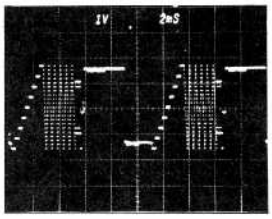
0 V (50%)
10 V/div

VECTOR
A3U620-5 40

0 V (10%)
10 V/div

A3U620-10 41

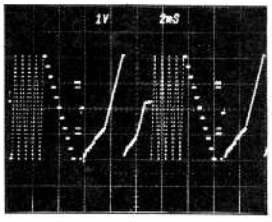
42



A3U330-6

0 V (50%)

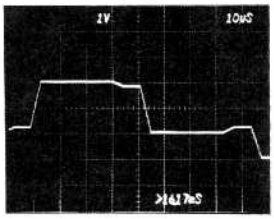
43



A3U230-6

0 V (50%)

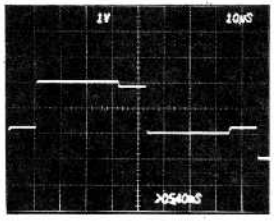
43



A3U230-6

BOX PATTERN (PARTIAL)
DURING JOIN DOTS DISPLAY.
NOTE TRANSITION TIMES
OF 4 μS.

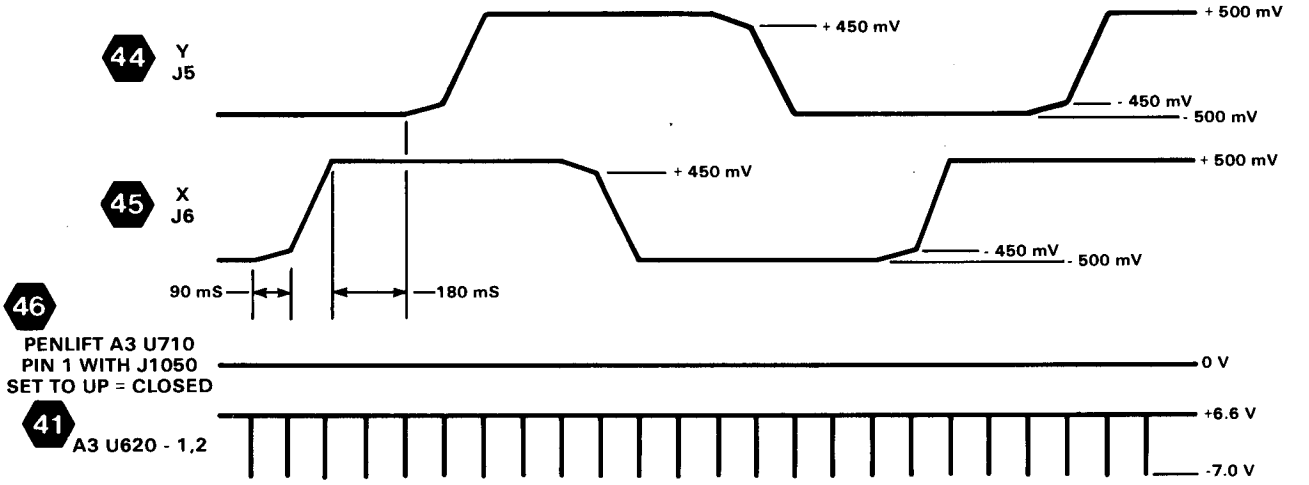
43



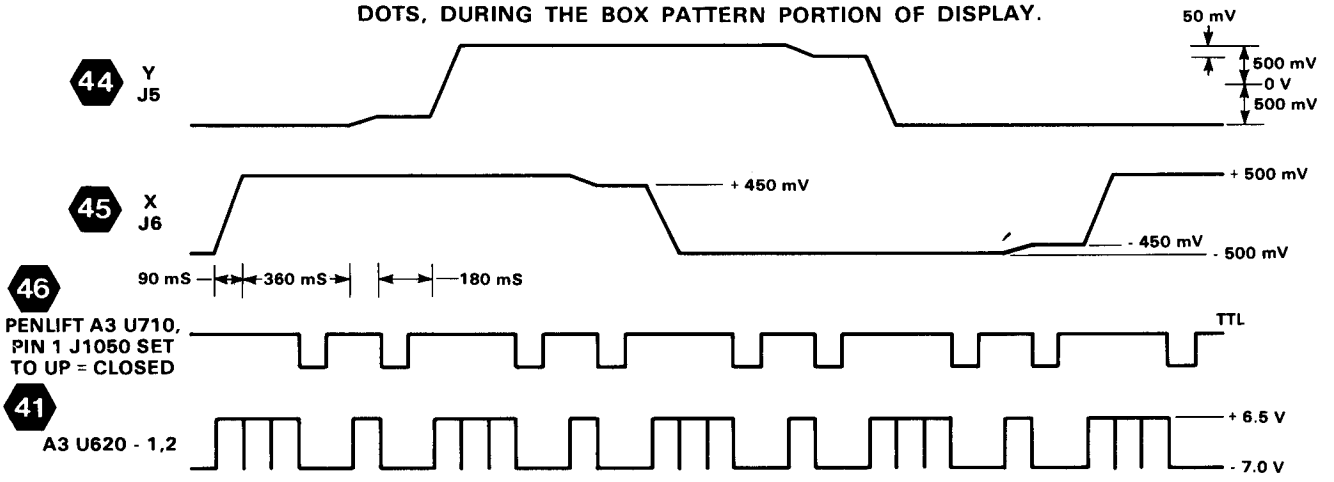
A3U230-6

BOX PATTERN (PARTIAL)
DURING DOT DISPLAY.
NOTE FAST TRANSITIONS.

5D10 DISPLAY OUTPUT WAVEFORMS IN THE PLOT MODE, JOIN, DURING THE BOX PATTERN PORTION OF DISPLAY.

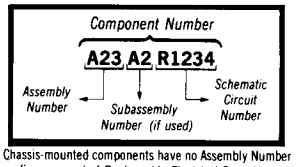


5D10 DISPLAY OUTPUT WAVEFORMS IN THE PLOT MODE, DOTS, DURING THE BOX PATTERN PORTION OF DISPLAY.

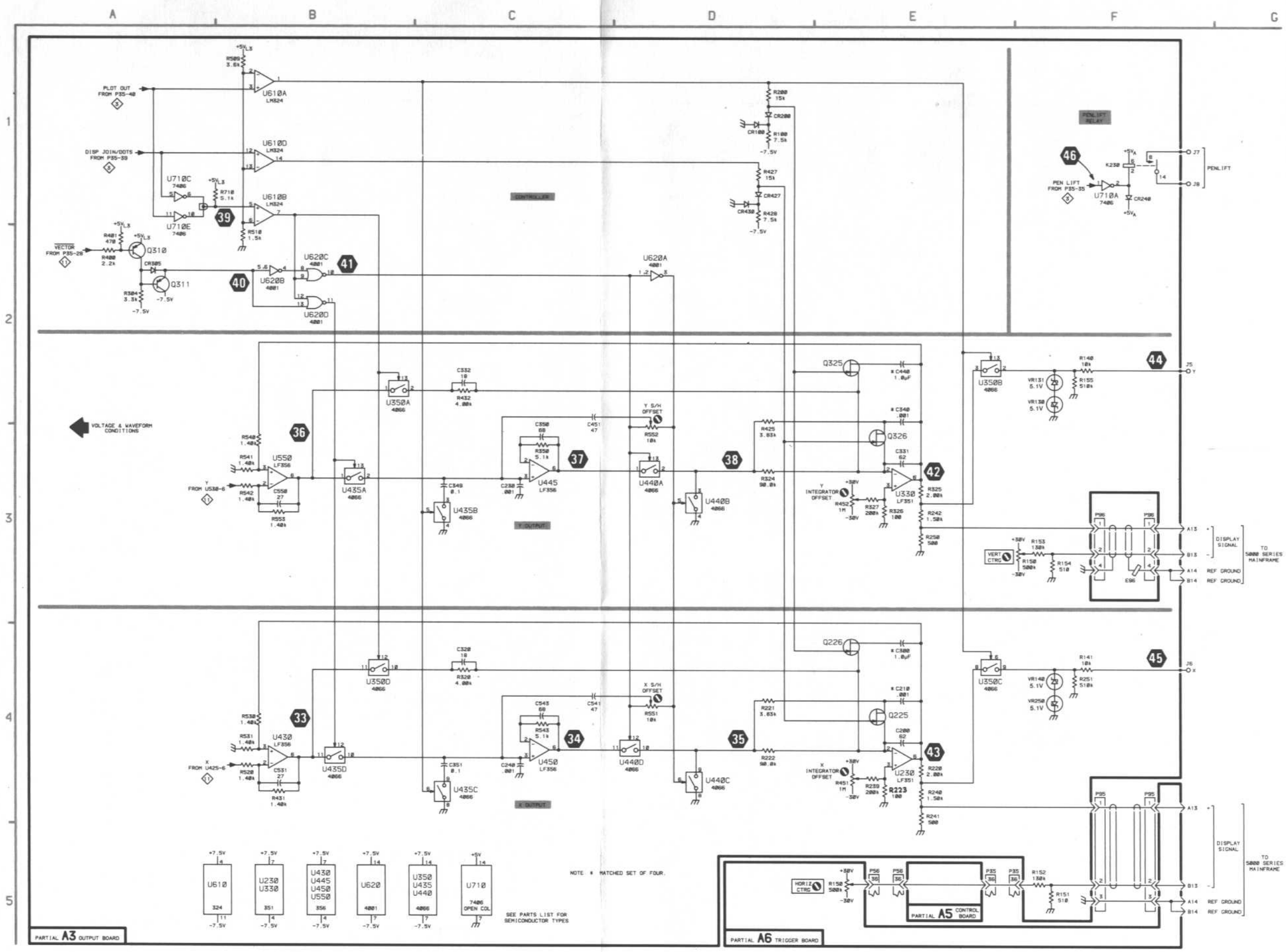


Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.


PLOT OUT FROM P35-40
DISP JOIN/DOTS FROM P35-39
VECTOR FROM P35-28
PEN LIFT FROM P35-35
CONTROLLER
PENLIFT RELAY
PENLIFT
VOLTAGE & WAVEFORM CONDITIONS
Y FROM U530-6
X FROM U425-6
Y OUTPUT
X OUTPUT
Y S/H OFFSET
X S/H OFFSET
Y INTEGRATOR OFFSET
X INTEGRATOR OFFSET
VERT CTRL
HORIZ CTRL
DISPLAY SIGNAL
REF GROUND
TO 5000 SERIES MAINFRAME
NOTE * MATCHED SET OF FOUR.
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
PARTIAL A3 OUTPUT BOARD
PARTIAL A5 CONTROL BOARD
PARTIAL A6 TRIGGER BOARD

POWER SUPPLIES AND POWER DISTRIBUTION DIAGRAM 13

ASSEMBLY A1 *Figure 8-7 illustrates circuit board A1.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C140	H2	A5	C647	H1	F5	L441	H1	D5
C141	H2	B4	C747	H1	G5	L541	H1	D5
C337	H2	C4				L542	H1	D5
C432	H1	D3	L342	H2	D5			

Partial A1 also shown on diagrams 2, 4 and 5.

ASSEMBLY A2 *Figure 8-3 illustrates circuit board A2.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C121	H4	A2	C301	H4	D1	P32	H3	C4
C212	H4	C2	C330	H4	D4			

Partial A2 also shown on diagram 1.

ASSEMBLY A3 *Figure 8-5 illustrates circuit board A3.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C311	G2	D1	C810	G4	J2	J32	H3	H4
C450	G2	E5	C830	G4	J3			
C452	G2	E4	C950	G2	J5	L950	G2	K5
C515	G4	F2	C951	G1	J5			
C520	G2	F3	C1000	G4	L1	P13	H1	H5
C521	G2	F3	C1030	G3	L4	P89	H3	J5
C630	G4	G3	C1050	A1	L5	P90	B2	L5
C720	G4	H2				P99	G1	J5

Partial A3 also shown on diagrams 1, 2, 3, 4, 5, 6, 8, 9, 10, 11 and 12.

ASSEMBLY A4 *Figure 8-6 illustrates circuit board A4.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C310	H5	B2	C530	H5	D3	C820	H5	G2
C330	H5	B3	C620	H5	E2	C840	H5	G3
C340	H5	C3	C710	H5	F2			
C420	H5	C2	C730	H5	F3	P54	H5	E4
C510	H5	D2	C750	H5	F4			

Partial A4 also shown on diagrams 3, 7, 8, 9 and 10.

ASSEMBLY A5 *Figure 8-9 illustrates circuit board A5.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	G5	B2	C610	G5	G3	J54	H5	E4
C110	G5	B3	C730	G5	G4			
C330	G5	D5	C820	G5	H3	P56	G5	G5
C400	G5	D2	C900	G5	J1			

Partial A5 also shown on diagrams 1, 2, 3, 5, 6, 7, 8, 9, 10, 11 and 12.

ASSEMBLY A6 *Figure 8-8 illustrates circuit board A6.*

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C620	A5	G3	L1020	C2	L3	R809	E4	J2
C700	F2	G2				R810	E3	J2
C710	E2	H3	P56	F5	E4	R811	E3	J2
C711	E2	H2	P80	B2	L3	R831	E4	H4
C720	E2	H3	P90	B2	K5	R832	E4	H4
C740	B4	H5	P99	F1	G2	R833	E4	H4
C750	A4	H5				R834	C4	J4
C751	C4	H5	Q731	E4	H4	R841	D3	J4
C820	E1	H3	Q740	A4	H4	R842	D3	J4
C830	D3	J4	Q741	B4	H4	R843	D4	J4
C831	E4	H4	Q800	E3	J1	R845	B3	H5
C848	C4	J4	Q831	E4	H3	R846	B4	H5
C901	D2	K2	Q835	D4	J4	R847	B4	J5
C910	D2	K1	Q840	B4	J5	R848	B4	J5
C930	C2	K4	Q841	B4	J5	R849	C4	H5
C931	C3	J4	Q842	C4	J4	R921	E2	K3
C1021	B2	L3	Q843	D4	J4	R922	C2	K3
			Q844	D4	J4	R940	C3	J5
CR601	E2	G1	Q845	D3	J4	R1040	A5	L4
CR630	C5	G4				R1140	A5	L4
CR631	C5	G4	R630	C5	G4			
CR640	C5	G4	R631	C5	G4	T810	E1	J2
CR700	F2	H1	R644	B5	G4			
CR701	E2	H1	R645	C5	G4	TP651	A4	G5
CR731	E2	H3	R646	C5	G4	TP652	F2	G5
CR732	E2	H3	R648	C5	G5			
CR840	D3	H4	R651	C4	G5	U740A	C5	G4
CR900	E4	K1	R700	E2	H2	U740B	C5	G4
CR920	E1	K3	R721	F2	G3	U740C	C5	G4
CR921	E2	K3	R731	C6	H4	U740D	C6	G4
CR1030	B2	K3	R732	C5	H4	U740	B5	G4
CR1031	B4	L4	R740	F4	H4			
			R741	B3	H5	VR730	E3	H3
F940	B2	K4	R743	E3	H4	VR731	F3	H4
F1040	B4	L4	R746	C4	G5	VR801	E3	J1
			R747	F4	H4	VR802	E3	H2
L630	A5	G3	R750	C4	G5	VR900	D4	K1
L710	E2	H2	R751	A4	H5	VR940	C3	J4
L730	E2	G3	R752	A4	H5			
L830	E1	J3	R753	C4	H5			

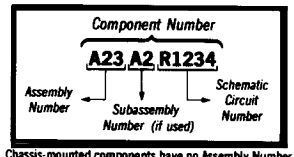
Partial A6 also shown on diagrams 1, 2, 5, 6, 7, 11 and 12.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
DS1	4	A1	DS5	7	H1	J3	6	A4
DS2	4	A3				J4	7	A2
DS3	7	H2	J1	4	A1			
DS4	7	A2	J2	4	A4			

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

WAVEFORM CONDITIONS

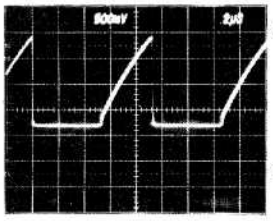
Waveform Conditions: Use a 50 MHz oscilloscope and a low-capacitance probe such as the P6016 probe connected to a 7A18 Dual Trace Amplifier with a 7B50 Time Base and a 7603 Mainframe.

Trigger the test oscilloscope from the base of Q850 on the + slope. The test oscilloscope vertical sensitivity and horizontal sweep speed are shown on the waveform pictures.

All waveforms except 51 are shown in normal operation and with P90 removed. P90 is located on the A6 Trigger board. At 51, with P90 removed, the waveform is a constant dc level equal to the -38 V unregulated supply.

NORMAL:

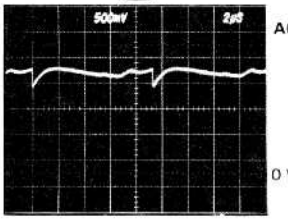
47



A6Q841-B

0 V (10%)

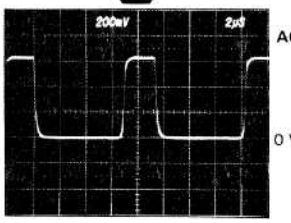
48



A6Q840-B

0 V (10%)

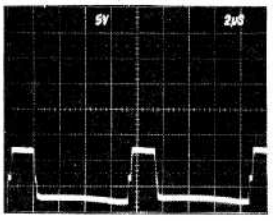
49



A6Q842-E

0 V (30%)

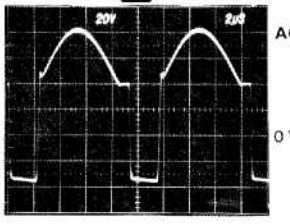
50



0 V (TOP)

A6Q800-G

51



A6Q800-D

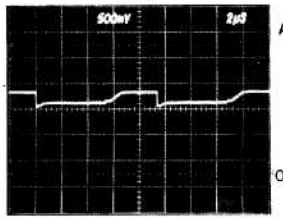
0 V (30%)

P90 OPEN:

47

SAME

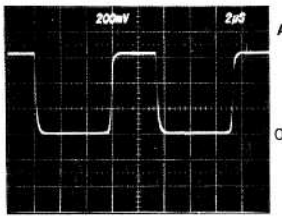
48



A6Q840-B

0 V (10%)

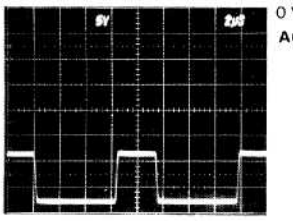
49



A6Q842-E

0 V (30%)

50



0 V (TOP)

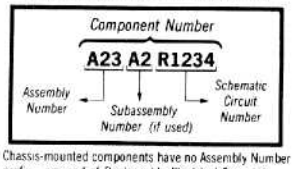
A6Q800-G

51

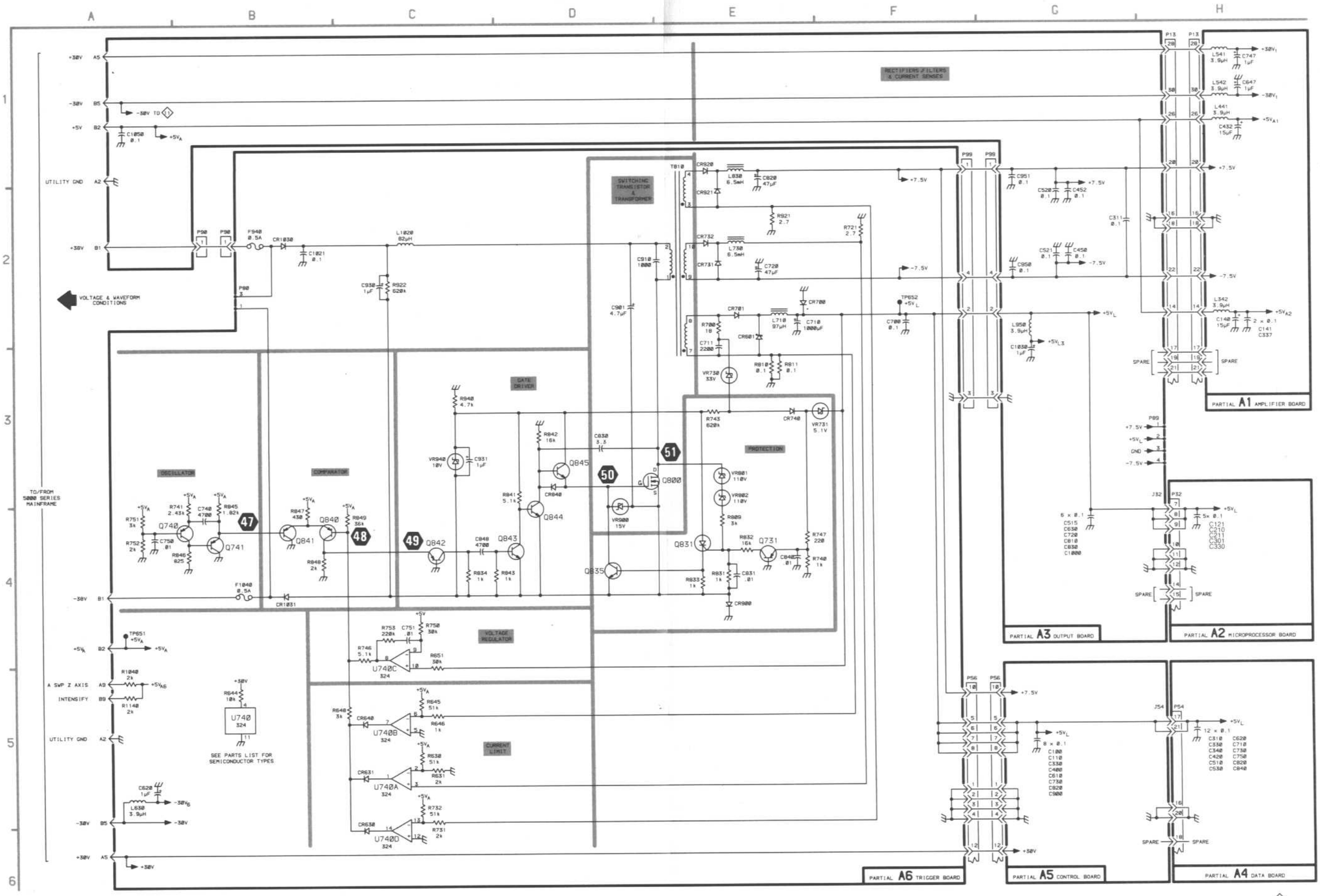
NONE

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List


RECTIFIERS/FILTERS & CURRENT SENSORS
SWITCHING TRANSISTOR & TRANSFORMER
GATE DRIVER
OSCILLATOR
COMPARATOR
PROTECTION
VOLTAGE REGULATOR
CURRENT LIMIT
VOLTAGE & WAVEFORM CONDITIONS
TO/FROM 5000 SERIES MAINFRAME
UTILITY GND
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
PARTIAL A1 AMPLIFIER BOARD
PARTIAL A3 OUTPUT BOARD
PARTIAL A2 MICROPROCESSOR BOARD
PARTIAL A6 TRIGGER BOARD
PARTIAL A5 CONTROL BOARD
PARTIAL A4 DATA BOARD

P13 (A1 TO A3)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	DØ	5	18	GND	13
2	D1	5	19	SPARE	13
3	D7	5	20	+7.5 V	13
4	D3	5	21	SPARE	13
5	D5	5	22	-7.5 V	13
6	DIG CK	5	23	$\overline{\text{HOLD}}$	4
7	D2	5	24	$\overline{\text{CH 1 PR}}$	2
8	$\overline{\text{END}}$	5	25	$\overline{\text{CH 1 CAL}}$	2
9	D6	5	26	+5 V_{A1}	13
10	DIG 4	5	27	$\overline{\text{CH 2 PR}}$	2
11	D4	5	28	+30 V	13
12	CH 2/1	5	29	$\overline{\text{CH 2 INVT}}$	2
13	$\overline{\text{TS 7}}$	5	30	-30 V	13
14	+5 V_{A2}	13	31	$\overline{\text{CH 2 GR}}$	2
15	CH 1/2	5	32	ADD	4
16	GND	13	33	$\overline{\text{CH 1 GR}}$	2
17	SPARE	13	34	$\overline{\text{CH 2 CAL}}$	2

P23 (A2 TO A3)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	DBØ	1	9	μPAØ	1
2	DB1	1	10	μPA1	1
3	DB2	1	11	μPA2	1
4	DB3	1	12	μPA3	1
5	DB4	1	13	μP $\overline{\text{EN I/O}}$	1
6	DB5	1	14	μP $\overline{\text{RD}}$	1
7	DB6	1	15	μP $\overline{\text{WR}}$	1
8	DB7	1			

P32 (A2 TO A3)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	SOD	1	9	+5 V_L	13
2	SID	1	10	GND	13
3	RST 6.5	1	11	GND	13
4	$\overline{\text{RESET}}$	1	12	GND	13
5	CLOCK ÷ 2	1	13	Y_7	1
6	EOT	1	14	SPARE	13
7	+5 V_L	13	15	SPARE	13
8	+5 V_L	13			

P34 (A3 TO A4)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	NØ	8	18	T9	8,11
2	N1	8	19	MØ	8
3	N2	8	20	M1	8
4	N3	8	21	M2	8
5	N4	8	22	M3	8
6	N5	8	23	M4	8
7	N6	8	24	M5	8
8	N7	8	25	M6	8
9	TØ	8,11	26	M7	8
10	T1	8,11	27	M8	8
11	T2	8,11	28	M9	8
12	T3	8,11	29	M10	8
13	T4	8,11	30	M11	8
14	T5	8,11	31	R11	8,11
15	T6	8,11	32	$\overline{\text{RESET}}$	3
16	T7	8,11	33	SPARE	8
17	T8	8,11	34	GND	8

P35 (A3 TO A5)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	DIG 4	6	21	X11	11
2	CH 2/1	6	22	CHAR CK	3
3	CH 1/2	6	23	DT4	2
4	$\overline{\text{HOLD}}$	6	24	DT3	2
5	ADD	3	25	DT5	2
6	$\overline{\text{EN 9}}$	2	26	DT2	2
7	$\overline{\text{EN 78}}$	2	27	DT1	2
8	SPARE	11	28	$\overline{\text{VECTOR}}$	11
9	SPARE	11	29	DISP XY/YT	3
10	DISP CHAR	3	30	CHAR Z	11
11	SPARE	11	31	DT6	2
12	SPARE	11	32	EOC	10
13	GND	11	33	DT7	2
14	GND	11	34	DTØ	2
15	Y CK	11	35	PEN LIFT	3
16	$\overline{\text{EN 34}}$	10	36	HORIZ CTRG	12
17	F EN	8	37	SPARE	3
18	F SEL	8	38	CLR	3
19	X CK	11	39	DISP JOIN/DOTS	3
20	TRACE SEP	11	40	PLOT OUT	3

P53 (A3 TO A5)

PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	$\overline{\text{FAULT}}$	9	11	PICS	6
2	μP $\overline{\text{WR}}$	1	12	μP $\overline{\text{EN I/O}}$	1
3	μP A1	1	13	XY SHIFT	3
4	$\overline{\text{DISP SWP MGF}}$	9	14	$\overline{\text{WE}}$	8
5	20.2L.LD	3	15	CLOCK ÷ 2	1
6	$\overline{\text{TS7}}$	6	16	μP AØ	1
7	μP A2	1	17	SPARE	6
8	$\overline{\text{LAST}}$	6	18	DIG CK	5
9	$\overline{\text{INTL MEM}}$	8	19	EOT	10
10	DIG DUAL/SGL	6	20	$\overline{\text{END}}$	6

Figure 8-10. Connector-Pin Locator Tables.

P45 (A4 TO A5)					
PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	2^0	10	14	$\overline{\text{ERASE}}$	9
2	2^1	10	15	$\overline{\text{LOADSTOP TEST}}$	7
3	2^2	10	16	TRIG EN	7
4	2^3	10	17	$\overline{\text{TRIG'D}}$	8
5	SØ	10	18	$\overline{\text{WE}}$	9
6	GND	8	19	WE GROUP	9
7	RØ	8	20	DISP XY/YT	8
8	SI5	10	21	T10	8
9	$\overline{\text{CLOCK}}$	8	22	$\overline{\text{T CLR}}$ (=1)	8
10	$\overline{\text{R+T}}$	3	23	WAC CK	9
11	INTL MEM	8	24	$\overline{\text{M EN}}$	8
12	DISP REF/NEW	8	25	$\overline{\text{S9}}$	10
13	ERASE	7			

P54 (A4 TO A5)					
PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	DTØ	3	14	OPN:R	3
2	DT1	3	15	DISP CHAR	3
3	DT2	3	16	GND	13
4	DT3	3	17	+5 V_L	13
5	DT4	3	18	SPARE	13
6	DT5	3	19	$\overline{\text{DISP CHAR}}$	3
7	DT6	3	20	GND	13
8	DT7	3	21	+5 V_L	13
9	OPN: FETCH	3	22	$\overline{\text{S10 + S11}}$	10
10	N2 CK	3	23	$\overline{\text{S10}}$	10
11	N1 CK	3	24	GROUP	9
12	M1 CK	3	25	XY.$\overline{\text{RØ}}$	8
13	$\overline{\text{RESET}}$	3			

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P56 (A5 TO A6)					
PIN NO.	LINE NAME	DIAG. NO.	PIN NO.	LINE NAME	DIAG. NO.
1	GND	13	21	$\overline{\text{END}}$	5
2	GND	13	22	$\overline{\text{SEC } 10^2}$	2
3	GND	13	23	F=N	6
4	GND	13	24	$\overline{\text{SEC } 10^4}$	2
5	+5 V_L	13	25	DIG 4	5
6	+5 V_L	13	26	SPARE	2
7	+5 V_L	13	27	BI SLOPE	7
8	+5 V_L	13	28	$\overline{\text{SEC .2}}$	2
9	PICS	6	29	+ SLOPE	7
10	+7.5 V	13	30	$\overline{\text{SEC .4}}$	2
11	$\overline{\text{SEC CAL}}$	2	31	-SLOPE	7
12	+30 V	13	32	SAMPLE	6
13	CLOCK	1	33	$\overline{\text{WE CLR}}$	7
14	Z AXIS ON/OFF	11	34	ERASE	6
15	$\overline{\text{CLOCK}}$	1	35	TRIGGER	7
16	SPARE	6	36	HORIZ CTG	12
17	HOLD	6	37	$\overline{\text{CUR 1+}}$	2
18	20.2L.LD	6	38	$\overline{\text{CUR 2-}}$	2
19	DIG CK	5	39	$\overline{\text{CUR 1-}}$	2
20	$\overline{\text{SEC } 10^1}$	2	40	$\overline{\text{CUR 2+}}$	2

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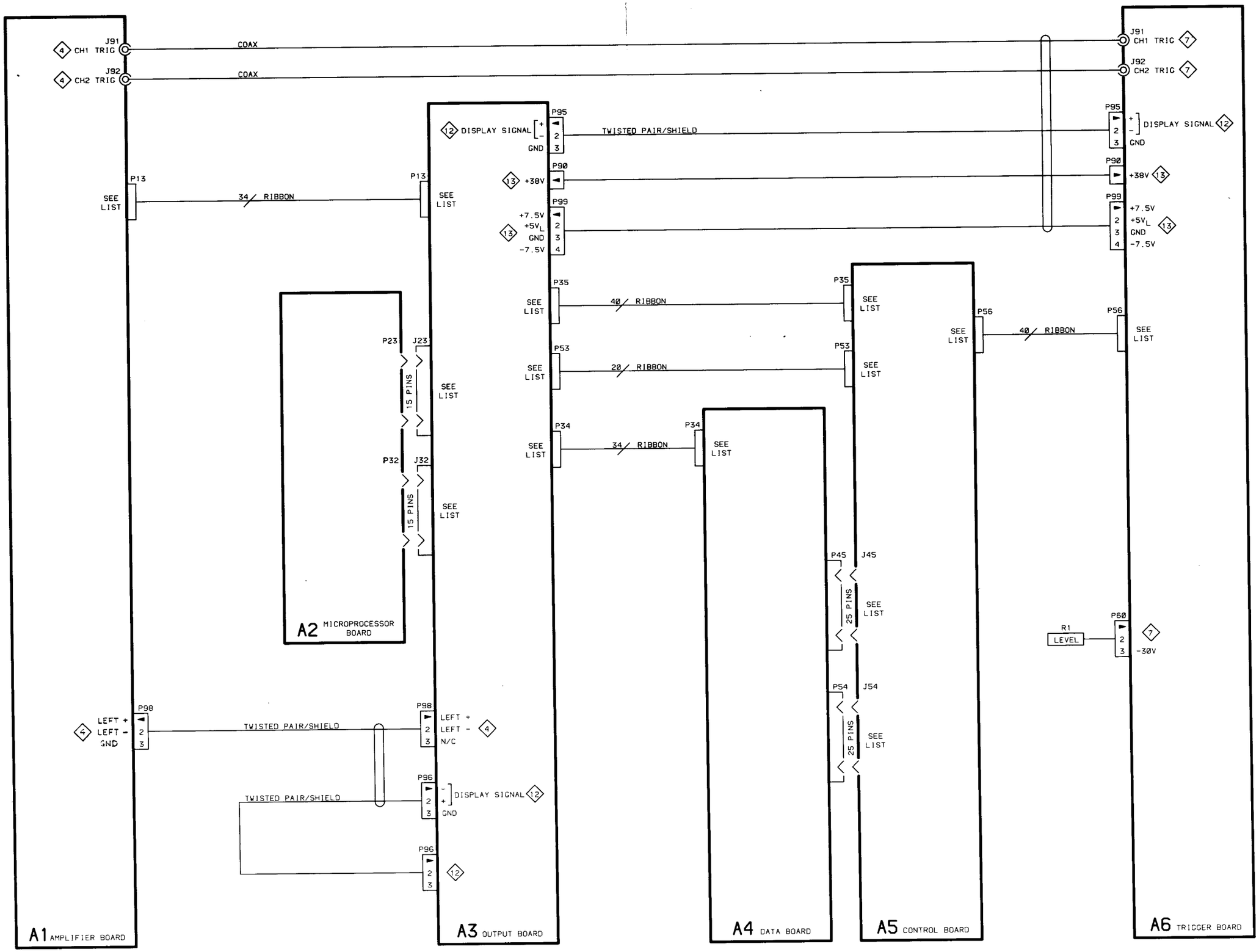
Figure 8-10. Connector-Pin Locator Tables (continued).



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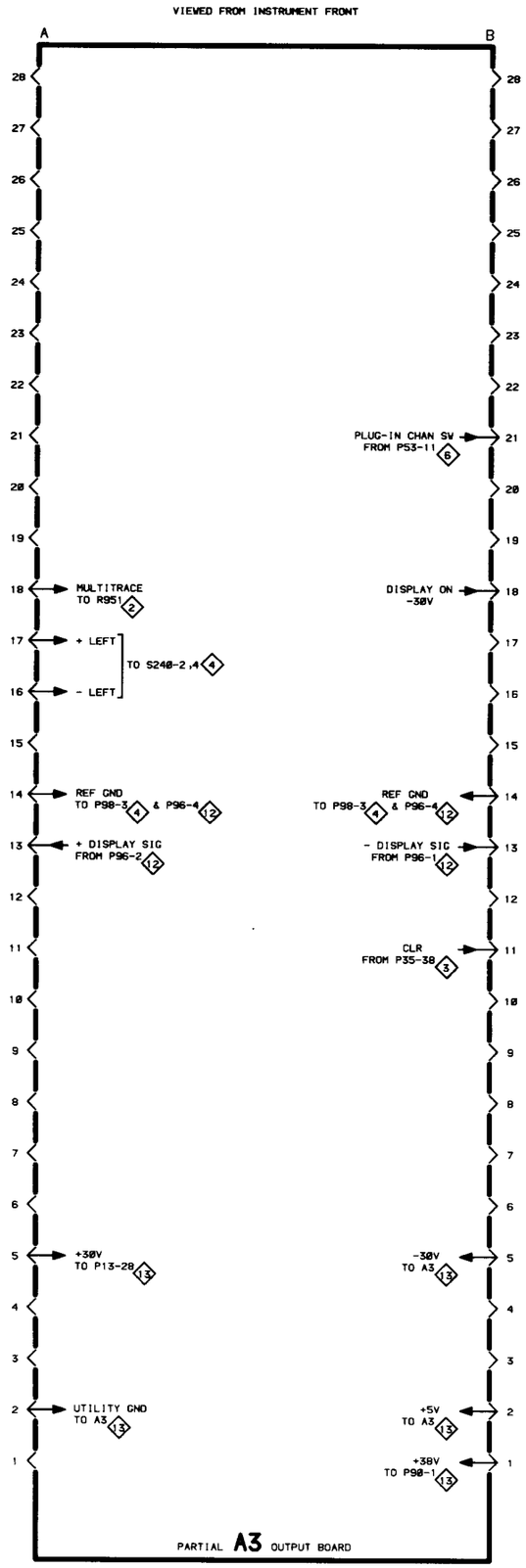
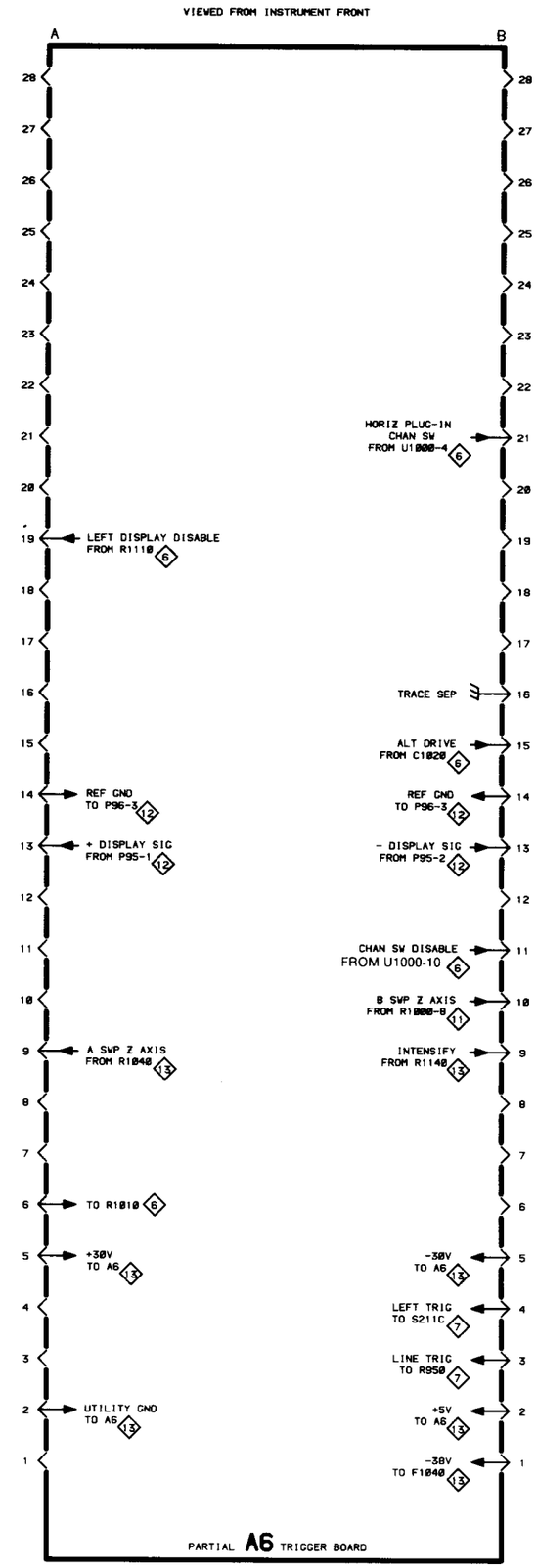

VIEWED FROM INSTRUMENT FRONT
A
B
PLUG-IN CHAN SW FROM P53-11 6
MULTITRACE TO R951 2
DISPLAY ON -30V
+ LEFT
- LEFT
TO S240-2,4 4
REF GND TO P98-3 4 & P96-4 12
REF GND TO P98-3 4 & P96-4 12
+ DISPLAY SIG FROM P96-2 12
- DISPLAY SIG FROM P96-1 12
CLR FROM P35-38 3
+30V TO P13-28 13
-30V TO A3 13
UTILITY GND TO A3 13
+5V TO A3 13
+38V TO P90-1 13
PARTIAL A3 OUTPUT BOARD


VIEWED FROM INSTRUMENT FRONT
A
B
HORIZ PLUG-IN CHAN SW FROM U1000-4 6
LEFT DISPLAY DISABLE FROM R1110 6
TRACE SEP
ALT DRIVE FROM C1020 6
REF GND TO P96-3 12
REF GND TO P96-3 12
+ DISPLAY SIG FROM P95-1 12
- DISPLAY SIG FROM P95-2 12
CHAN SW DISABLE FROM U1000-10 6
B SWP Z AXIS FROM R1000-8 11
INTENSIFY FROM R1140 13
A SWP Z AXIS FROM R1040 13
TO R1010 6
+30V TO A6 13
-30V TO A6 13
LEFT TRIG TO S211C 7
LINE TRIG TO R950 7
UTILITY GND TO A6 13
+5V TO A6 13
-38V TO F1040 13
PARTIAL A6 TRIGGER BOARD

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

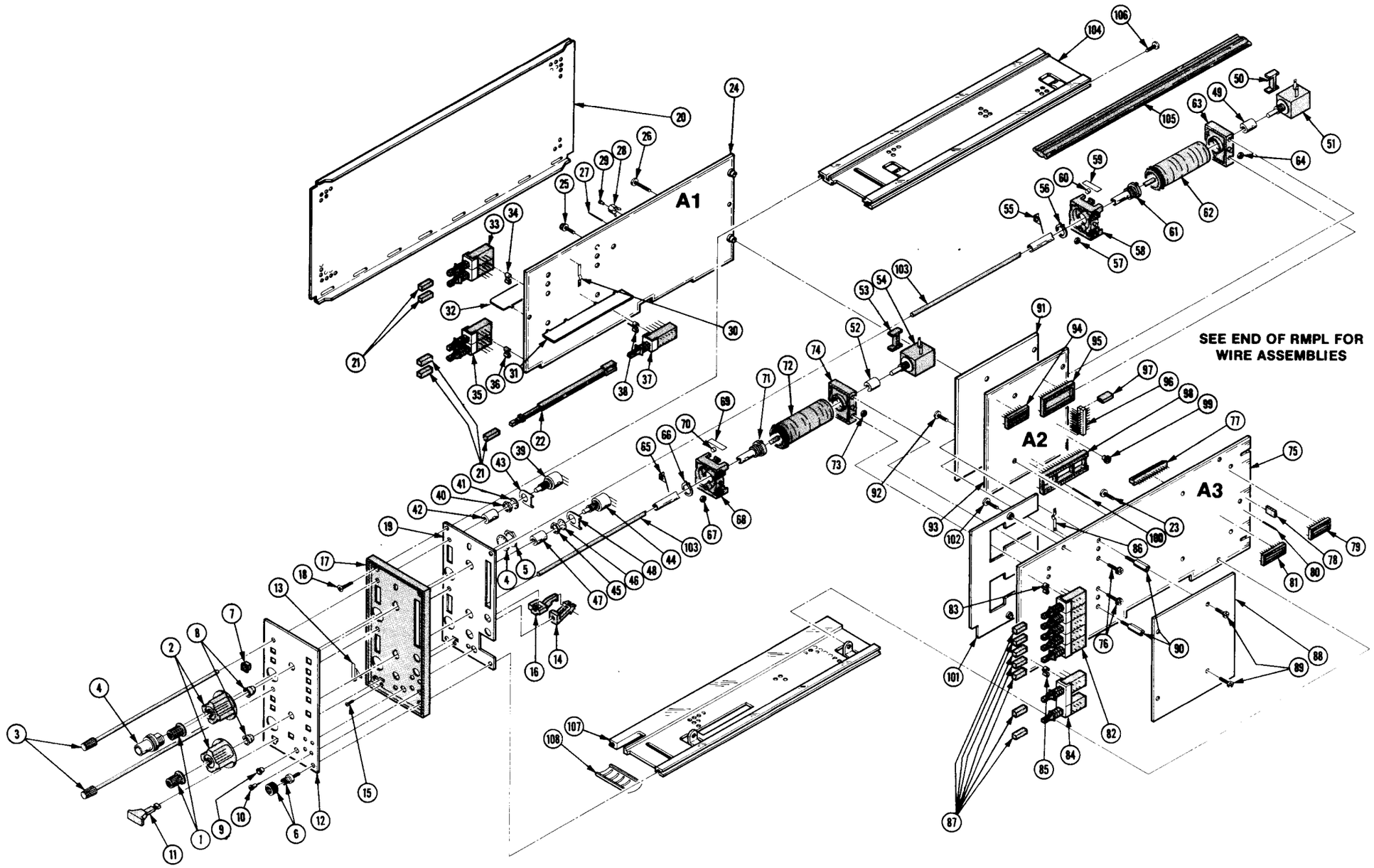
CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

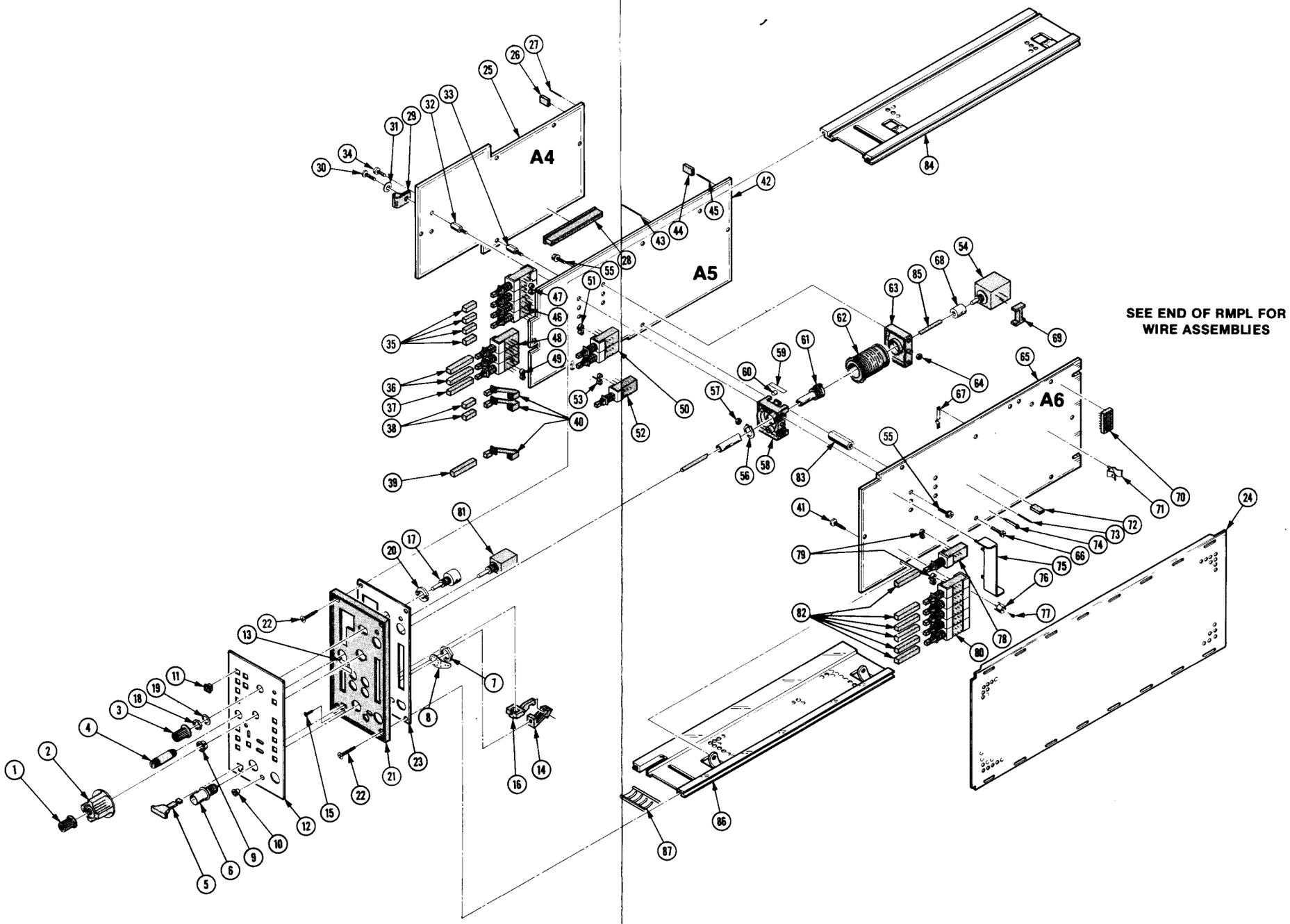
Mfr. Code	Manufacturer	Address	City, State, Zip
000CY	NORTHWEST FASTENER SALES, INC.	7923 SW CIRRUS DRIVE	BEAVERTON, OR 97005
000EO	ZEPHER ELECTRONIC SALES CORP.	647 INDUSTRY DRIVE	SEATTLE, WA 98188
000EX	O'HARA METAL PRODUCT COMPANY	542 BRANNAN STREET	SAN FRANCISCO, CA 94107
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
06540	AMATOM ELECTRONIC HARDWARE, DIV. OF MITE CORP.	446 BLAKE ST.	NEW HAVEN, CT 06515
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
71159	BRISTOL SOCKET SCREW, DIV. OF AMERICAN CHAIN AND CABLE CO., INC.	P O BOX 2244, 40 BRISTOL ST.	WATERBURY, CT 06720
71279	CAMBRIDGE THERMIONIC CORP.	445 CONCORD AVE.	CAMBRIDGE, MA 02138
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
79136	WALDES, KOHINOOR, INC.	47-16 AUSTEL PLACE	LONG ISLAND CITY, NY 11101
79807	WROUGHT WASHER MFG. CO.	2100 S. O BAY ST.	MILWAUKEE, WI 53207
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	366-1707-04			2	KNOB:GY,CAL,0.127 ID X 0.5 OD X 0.53 H	80009	366-1707-04
	213-0246-00			2	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-2	366-1001-00			2	KNOB:GY,0.252 ID X0.925 OD X 0.67	80009	366-1001-00
	213-0153-00			4	.SETSCREW:5-40 X 0.125,STL BK OXD,HEX SKT	000CY	OBD
-3	384-1114-02			2	EXTENSION SHAFT:5.937 L X 0.123 OD,PLASTIC	80009	384-1114-02
-4	131-0679-02			2	CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR168-2
					**********(ATTACHING PARTS)**********		
-5	220-0497-00			2	NUT,PLAIN,HEX.:0.5-28 X 0.562 INCH HEX,BRS	73743	OBD
					**********(END ATTACHING PARTS)*********		
-6	220-0633-00			1	NUT,PLAIN,KNURL:0.25-28 X 0.25 INCH L,BRS	80009	220-0633-00
-7	426-1072-00			12	FRAME,PUSH BTN:PLASTIC	80009	426-1072-00
-8	358-0216-00			2	BUSHING,PLASTIC:0.257 ID X 0.412 INCH OD	80009	358-0216-00
-9	358-0378-00			1	BUSHING,SLEEVE:0.131 ID X 0.125 L	80009	358-0378-00
-10	136-0387-00			4	JACK,TIP:GRAY	71279	450-4352-01-0318
-11	366-1690-00			1	KNOB:SIL GY,0.53 X0.23 X 1.059	80009	366-1690-00
-12	333-2879-00			1	PANEL,FRONT:	80009	333-2879-00
-13	131-1075-00			2	CONTACT,ELEC:GROUNDING,CU BE HEAT TRTD	80009	131-1075-00
-14	105-0719-00			1	LATCH,RETAINING:PLUG-IN	80009	105-0719-00
					**********(ATTACHING PARTS)**********		
-15	213-0113-00			1	SCR,TPG,THD FOR:2-32 X 0.312 INCH,PNH STL	93907	OBD
					**********(END ATTACHING PARTS)*********		
-16	105-0718-01			1	BAR,LATCH RLSE:	80009	105-0718-01
-17	386-4798-00			1	SUBPANEL,FRONT:	80009	386-4798-00
					**********(ATTACHING PARTS)**********		
-18	213-0229-00			3	SCR,TPG,THD FOR:6-20 X0.375"100 DEG,FLH ST	93907	OBD
					**********(END ATTACHING PARTS)*********		
-19	337-2968-00			1	SHIELD,ELEC:WAVEFORM	80009	337-2968-00
-20	337-1399-04			1	SHIELD,ELEC:SIDE	80009	337-1399-04
-21	366-1559-00			5	PUSH BUTTON:SIL GY,0.18 SQ X 0.43	80009	366-1559-00
-22	384-0490-00			1	EXTENSION SHAFT:0.123 OD X 5.93 INCH LONG	80009	384-0490-00
	672-1023-00			1	CKT BOARD ASSY:OUTPUT	80009	672-1023-00
					**********(ATTACHING PARTS)**********		
-23	213-0146-00			2	SCR,TPG,THD FOR:6-20 X 0.313 INCH,PNH STL	83385	OBD
					**********(END ATTACHING PARTS)*********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-24	----- -----			1	.CKT BOARD ASSY:AMPLIFIER(SEE A1 REPL)		
					.**********(ATTACHING PARTS)**********		
-25	211-0292-00			8	.SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	OBD
-26	211-0017-00			2	.SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
					.**********(END ATTACHING PARTS)*********		
	----- -----			-	.CKT BOARD ASSY INCLUDES:		
-27	131-0608-00			37	..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-28	131-1003-00			2	..CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-29	136-0252-07			26	..SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-30	131-0604-00			23	..CONTACT,ELEC:CKT BD SW,SPR,CU BE	80009	131-0604-00
-31	337-2228-00			1	..SHIELD,ELEC:CIRCUIT CARD	80009	337-2228-00
-32	337-1400-00			1	..SHIELD,ELEC:	80009	337-1400-00
-33	----- -----			1	..SWITCH,PUSH:(SEE A1S1200 REPL)		
-34	361-0385-00			4	..SPACER,PB SW:0.164 INCH LONG	80009	361-0385-00
-35	----- -----			1	..SWITCH,PUSH:(SEE A1S1230 REPL)		
-36	361-0385-00			4	..SPACER,PB SW:0.164 INCH LONG	80009	361-0385-00
-37	----- -----			1	..SWITCH,PUSH:(SEE A1S740 REPL)		
-38	361-0382-00			2	..SPACER,PB SW:BROWN,0.275 INCH LONG	80009	361-0382-00
-39	----- -----			1	..RES.,VAR:(SEE A1R500 REPL)		
					..**********(ATTACHING PARTS)**********		
-40	210-0583-00			1	..NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-41	210-0046-00			1	..WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
					..*********(END ATTACHING PARTS)*********		
-42	376-0029-00			1	..CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5	80009	376-0029-00
-43	387-0794-00			1	..PLATE,CMPNT MTG:VAR RESISTOR,BRASS	80009	387-0794-00
-44	----- -----			1	..RES.,VAR:(SEE A1R532 REPL)		
					..**********(ATTACHING PARTS)**********		
-45	210-0583-00			1	..NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-46	210-0046-00			1	..WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
					..*********(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-47	376-0029-00			1	..CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5	80009	376-0029-00
-48	387-0794-00			1	..PLATE,CMPNT MTG:VAR RESISTOR,BRASS	80009	387-0794-00
-49	376-0029-00			1	..CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5	80009	376-0029-00
-50	361-0515-00			1	..SPACER,SWITCH:PLASTIC	80009	361-0515-00
-51	----- -----			1	..RES.,VAR:(SEE A1R610,S610 REPL)		
-52	376-0029-00			1	..CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5	80009	376-0029-00
-53	361-0515-00			1	..SPACER,SWITCH:PLASTIC	80009	361-0515-00
-54	----- -----			1	..RES.,VAR:(SEE A1R639,S639 REPL)		
	----- -----			1	.SW CAM ACTR AS:(SEE S310 REPL)		
-55	131-0963-00			1	..CONTACT,ELEC:GROUNDING	000EX	OBD
-56	354-0390-00			1	..RING,RETAINING:0.338 ID X 0.025" THK,STL	79136	5100-37MD
-57	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-58	401-0180-00			1	..BEARING,CAM SW:FRONT & REAR	80009	401-0180-00
-59	214-1139-02			1	..SPRING,FLAT:GREEN COLORED	80009	214-1139-02
	214-1139-03			1	..SPRING,FLAT:RED COLORED	80009	214-1139-03
-60	214-1752-00			2	..ROLLER,DETENT:	80009	214-1752-00
-61	384-0878-17			1	..SHAFT,CAM SW:OUTER CNCTR,W/DRVR,VOLTS/DI	80009	384-0878-17
-62	105-0926-00			1	..ACTUATOR,CAM SW:VOLTS/DIV,CHAN 1	80009	105-0926-00
-63	401-0178-00			1	..BEARING,CAM SW:CENTER	80009	401-0178-00
-64	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
	----- -----			1	.SW CAM ACTR AS:(SEE S340 REPL)		
-65	131-0963-00			1	..CONTACT,ELEC:GROUNDING	000EX	OBD
-66	354-0390-00			1	..RING,RETAINING:0.338 ID X 0.025" THK,STL	79136	5100-37MD
-67	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-68	401-0180-00			1	..BEARING,CAM SW:FRONT & REAR	80009	401-0180-00
-69	214-1139-02			1	..SPRING,FLAT:GREEN COLORED	80009	214-1139-02
	214-1139-03			1	..SPRING,FLAT:RED COLORED	80009	214-1139-03
-70	214-1752-00			1	..ROLLER,DETENT:	80009	214-1752-00
-71	384-0878-17			1	..SHAFT,CAM SW:OUTER CNCTR,W/DRVR,VOLTS/DI	80009	384-0878-17
-72	105-0927-00			1	..ACTUATOR,CAM SW:VOLTS/DIV,CHAN 2	80009	105-0927-00
-73	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-74	401-0178-00			1	..BEARING,CAM SW:CENTER	80009	401-0178-00
-75	----- -----			1	.CKT BOARD ASSY:OUTPUT(SEE A3 REPL)		
					.**********(ATTACHING PARTS)**********		
-76	211-0292-00			4	.SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	OBD
					.**********(END ATTACHING PARTS)*********		
	----- -----			-	.CKT BOARD ASSY INCLUDES:		
-77	131-2173-00			2	..CONN,RCPT,ELEC:CIRCUIT BD,15CONTACT	22526	65780-015
-78	131-0993-09			1	..LINK,TERM,CONNE:2 WIRE WHITE	00779	530153-1
-79	136-0756-00			2	..SKT,PL-IN ELEK:MICROCIRCUIT,18 DIP	09922	DILB18P-108
-80	131-0608-00			149	..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-81	136-0752-00			1	..SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-82	----- -----			1	..SWITCH,PUSH:(SEE A3S100 REPL)		
-83	361-0384-00			4	..SPACER,PB SW:0.133 INCH LONG	80009	361-0384-00
-84	----- -----			1	..SWITCH,PUSH:(SEE A3S130 REPL)		
-85	361-0384-00			4	..SPACER,PB SW:0.133 INCH LONG	80009	361-0384-00
-86	131-0604-00			10	..CONTACT,ELEC:CKT BD SW,SPR,CU BE	80009	131-0604-00
-87	366-1559-00			7	PUSH BUTTON:SIL GY,0.18 SQ X 0.43	80009	366-1559-00
-88	337-2970-00			1	SHIELD,ELEC:CIRCUIT BOARD	80009	337-2970-00
					**********(ATTACHING PARTS)**********		
-89	211-0007-00			3	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					**********(END ATTACHING PARTS)*********		
-90	129-0354-00			4	SPACER,POST:0.54 L,W/4-40THD ONE END	80009	129-0354-00
-91	337-2970-00			1	SHIELD,ELEC:CIRCUIT BOARD	80009	337-2970-00
					**********(ATTACHING PARTS)**********		
-92	211-0007-00			1	SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
					**********(END ATTACHING PARTS)*********		
-93	----- -----			1	CKT BOARD ASSY:PROCESSOR(SEE A2 REPL)		
-94	136-0756-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,18 DIP	09922	DILB18P-108
-95	136-0755-00			2	.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-96	131-2514-00			2	.CONN,RCPT,ELEC:CKT BD,2 X 10,MALE	00779	86479-1
-97	131-0993-00			13	.BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-98	136-0757-00			1	.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-99	361-0765-00			4	.SPACER,SLEEVE:0.226 L X 0.125 ID,BRS	80009	361-0765-00
-100	131-0787-00			30	.CONTACT,ELEC:0.64 INCH LONG	22526	47359

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-101	337-2989-00			1	SHIELD,ELEC:CIRCUIT BOARD **********(ATTACHING PARTS)**********	80009	337-2989-00
-102	213-0183-00			2	SCR,TPG,THD FOR:6-20 X 0.5 TYPE B,PNH,STL **********(END ATTACHING PARTS)*********	83385	OBD
-103	384-0490-00			2	EXTENSION SHAFT:0.123 OD X 5.93 INCH LONG	80009	384-0490-00
-104	426-1885-00			1	FR SECT,PLUG-IN:TOP	80009	426-1885-00
-105	214-3316-00			2	CPLR,PL-IN UNIT: **********(ATTACHING PARTS)**********	80009	214-3316-00
-106	213-0054-00			2	SCR,TPG,THD FOR:6-32 X 0.312 INCH,PNH STL **********(END ATTACHING PARTS)*********	93907	OBD
-107	426-1884-00			1	FR SECT,PLUG-IN:BOTTOM	80009	426-1884-00
-108	131-1372-01			2	CONTACT,ELEC:PLUG-IN GND,CU BE BRT DIP	80009	131-1372-01


A1
A2
A3
SEE END OF RMPL FOR
WIRE ASSEMBLIES



5D10

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
2-1	366-1707-04			1	KNOB:GY,CAL,0.127 ID X 0.5 OD X 0.53 H	80009	366-1707-04
	213-0246-00			1	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-2	366-1001-00			1	KNOB:GY,0.252 ID X0.925 OD X 0.67	80009	366-1001-00
	213-0153-00			2	.SETSCREW:5-40 X 0.125,STL BK OXD,HEX SKT	000CY	OBD
-3	366-0494-00			1	KNOB:GRAY WITH SETSCREW	80009	366-0494-00
	213-0246-00			1	.SETSCREW:5-40 X 0.093 ITL BK OXD,HEX SKT	71159	OBD
-4	366-1564-00			1	KNOB:GRAY PLASTIC,PRESS MT	80009	366-1564-00
-5	366-1690-00			1	KNOB:SIL GY,0.53 X0.23 X 1.059	80009	366-1690-00
-6	131-0955-01			2	CONN,RCPT,ELEC:BNC,FEMALE,MODIFIED	80009	131-0955-01
					**********(ATTACHING PARTS)**********		
-7	220-0495-00			2	NUT,PLAIN,HEX.:0.375-32 X 0.438 INCH BRS	73743	OBD
-8	210-0255-00			2	TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	80009	210-0255-00
					**********(END ATTACHING PARTS)*********		
-9	358-0216-00			1	BUSHING,PLASTIC:0.257 ID X 0.412 INCH OD	80009	358-0216-00
-10	358-0378-00			1	BUSHING,SLEEVE:0.131 ID X 0.125 L	80009	358-0378-00
-11	426-1072-00			16	FRAME,PUSH BTN:PLASTIC	80009	426-1072-00
-12	333-2878-00			1	PANEL,FRONT:	80009	333-2878-00
-13	131-1075-00			1	CONTACT,ELEC:GROUNDING,CU BE HEAT TRTD	80009	131-1075-00
-14	105-0719-00			1	LATCH,RETAINING:PLUG-IN	80009	105-0719-00
					**********(ATTACHING PARTS)**********		
-15	213-0113-00			1	SCR,TPG,THD FOR:2-32 X 0.312 INCH,PNH STL	93907	OBD
					**********(END ATTACHING PARTS)*********		
-16	105-0718-01			1	BAR,LATCH RLSE:	80009	105-0718-01
-17	----- -----			1	RES.,VAR,NONWW:(SEE R1 REPL)		
					**********(ATTACHING PARTS)**********		
-18	210-0583-00			1	NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
-19	210-0940-00			1	WASHER,FLAT:0.25 ID X 0.375 INCH OD,STL	79807	OBD
-20	361-0143-00			1	WASHER,KEY:0.281 ID X 0.562 INCH OD	80009	361-0143-00
					**********(END ATTACHING PARTS)*********		
-21	386-4797-00			1	SUBPANEL,FRONT:	80009	386-4797-00
					**********(ATTACHING PARTS)**********		
-22	213-0229-00			4	SCR,TPG,THD FOR:6-20 X0.375`100 DEG,FLH ST	93907	OBD
					**********(END ATTACHING PARTS)*********		
-23	337-2967-00			1	SHIELD,ELEC:STORAGE	80009	337-2967-00
-24	337-1399-04			1	SHIELD,ELEC:SIDE	80009	337-1399-04
-25	----- -----			1	CKT BOARD ASSY:DATA(SEE A4 REPL)		
-26	131-0993-09			1	.LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-27	131-0608-00			39	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-28	131-2174-00			2	.CONN,RCPT,ELEC:CIRCUIT BD,125 CONTACTS	22526	65780-025
-29	343-0003-00			1	CLAMP,LOOP:0.25 INCH DIA	95987	1-4 6R
					**********(ATTACHING PARTS)**********		
-30	211-0012-00			1	SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	OBD
-31	210-0949-00			1	WASHER,FLAT:0.141 ID X 0.50 INCH OD,BRS	12327	OBD
-32	129-0236-00			1	SPACER,POST:0.188 HEX X 0.375 INCH LONG	06540	9726-A-0440
					**********(END ATTACHING PARTS)*********		
-33	129-0236-00			4	SPACER,POST:0.188 HEX X 0.375 INCH LONG	06540	9726-A-0440
					**********(ATTACHING PARTS)**********		
-34	211-0008-00			4	SCREW,MACHINE:4-40 X 0.250 INCH,PNH STL	83385	OBD
					**********(END ATTACHING PARTS)*********		
-35	366-1559-00			4	PUSH BUTTON:SIL GY,0.18 SQ X 0.43	80009	366-1559-00
-36	366-1512-01			2	PUSH BUTTON:CHARCOAL GY,0.18 SQ X 0.8	80009	366-1512-01
-37	366-1512-00			1	PUSH BUTTON:GRAY,0.18 SQ X 0.83 INCH LG	80009	366-1512-00
-38	366-1559-00			2	PUSH BUTTON:SIL GY,0.18 SQ X 0.43	80009	366-1559-00
-39	366-1512-00			1	PUSH BUTTON:GRAY,0.18 SQ X 0.83 INCH LG	80009	366-1512-00
-40	384-1354-00			3	EXTENSION SHAFT:1.585 INCH LONG,OFFSET,NYL	80009	384-1354-00
	672-1022-00			1	CKT BOARD ASSY:TRIGGER	80009	672-1022-00
					**********(ATTACHING PARTS)**********		
-41	213-0146-00			4	SCR,TPG,THD FOR:6-20 X 0.313 INCH,PNH STL	83385	OBD
					**********(END ATTACHING PARTS)*********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-42	----- -----			1	.CKT BOARD ASSY:CONTROL(SEE A5 REPL)		
-43	131-0589-00			50	..TERMINAL,PIN:0.46 L X 0.025 SQ	22526	47350
-44	131-0993-09			6	..LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-45	131-0608-00			114	..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-46	----- -----			1	..SWITCH,PUSH:(SEE A5S900A-D REPL)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
2-47	361-0899-00			4	..SPACER,PB SW:0.144 L,ORANGE	80009	361-0899-00
-48	----- -----			1	..SWITCH,PUSH:(SEE A5S920 REPL)		
-49	361-0899-00			4	..SPACER,PB SW:0.144 L,ORANGE	80009	361-0899-00
-50	----- -----			1	..SWITCH,PUSH:(SEE A5S901 REPL)		
-51	361-0385-00			4	..SPACER,PB SW:0.164 INCH LONG	80009	361-0385-00
-52	----- -----			-	..SWITCH,PUSH:(SEE A5S935 REPL)		
-53	361-0382-00			2	..SPACER,PB SW:BROWN,0.275 INCH LONG	80009	361-0382-00
-54	----- -----			1	..RES.,VAR NONWW:(SEE A5R910,S910 REPL)		
	----- -----			1	..SWITCH,TOGGLE:(SEE A5S1020 REPL)		
	----- -----			1	.SW,CAM ACTR AS:(SEE S320 REPL)		
					.**********(ATTACHING PARTS)**********		
-55	211-0292-00			4	.SCR,ASSEM WSHR:4-40 X 0.29,BRS NI PL	78189	OBD
					.**********(END ATTACHING PARTS)*********		
-56	354-0390-00			1	..RING,RETAINING:0.338 ID X 0.025" THK,STL	79136	5100-37MD
-57	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-58	401-0180-00			1	..BEARING,CAM SW:FRONT & REAR	80009	401-0180-00
-59	214-1139-02			2	..SPRING,FLAT:GREEN COLORED	80009	214-1139-02
-60	214-1752-00			2	..ROLLER,DETENT:	80009	214-1752-00
-61	384-0878-03			1	..SHAFT,CAM SW:3.779 L X 0.248 OD	80009	384-0878-03
-62	105-0925-00			1	..ACTUATOR,CAM SW:TIME/DIV	80009	105-0925-00
-63	401-0178-01			1	..BEARING,CAM SW:CENTER/REAR	80009	401-0178-01
-64	210-0406-00			4	..NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-65	----- -----			1	.CKT BOARD ASSY:TRIGGER(SEE A6 REPL)		
					.**********(ATTACHING PARTS)**********		
-66	211-0097-00			3	.SCREW,MACHINE:4-40 X 0.312 INCH,PNH STL	83385	OBD
					.**********(END ATTACHING PARTS)*********		
	----- -----			-	.CKT BOARD ASSY INCLUDES:		
-67	131-0604-00			5	..CONTACT,ELEC:CKT BD SW,SPR,CU BE	80009	131-0604-00
-68	376-0029-00			1	..CPLG,SHAFT,RGD:0.128 ID X 0.312 OD X 0.5	80009	376-0029-00
-69	361-0515-00			1	..SPACER,SWITCH:PLASTIC	80009	361-0515-00
-70	136-0728-00			1	..SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-71	344-0326-00			4	..CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-72	131-0993-09			1	..LINK,TERM.CONNE:2 WIRE WHITE	00779	530153-1
-73	131-0608-00			55	..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-74	----- -----			3	..TERM,TEST PT:(SEE A6TP340,651,652 REPL)		
-75	337-0994-00			1	..SHIELD,ELEC:CIRCUIT BOARD	80009	337-0994-00
-76	131-1003-00			2	..CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-77	136-0252-07			2	..SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-78	----- -----			1	..SWITCH,PUSH:(SEE A6S210 REPL)		
-79	361-0384-00			6	..SPACER,PB SW:0.133 INCH LONG	80009	361-0384-00
-80	----- -----			1	..SWITCH,PUSH:(SEE A6S211A-E REPL)		
	----- -----			2	..SWITCH,TOGGLE:(SEE A6S130,S140 REPL)		
-81	----- -----			1	..RES.,VAR,NONWW:(SEE A6R621,S621 REPL)		
-82	366-1512-00			6	PUSH BUTTON:GRAY,0.18 SQ X 0.83 INCH LG	80009	366-1512-00
-83	129-0323-00			3	POST,ELEC-MECH:HEX,0.25 X 1 INCH LONG	80009	129-0323-00
	334-3438-00			1	MARKER,IDENT:MARKED TURN OFF POWER	80009	334-3458-00
-84	426-1885-00			1	FR SECT,PLUG-IN:TOP	80009	426-1885-00
-85	384-0490-00			1	EXTENSION SHAFT:0.123 OD X 5.93 INCH LONG	80009	384-0490-00
-86	426-0724-10			1	FR SECT,PLUG-IN:BOTTOM	80009	426-0724-10
-87	131-1372-01			2	CONTACT,ELEC:PLUG-IN GND,CU BE BRT DIP	80009	131-1372-01

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
					WIRE ASSEMBLIES		
	175-4473-00			1	CA ASSY,SP,ELEC:3,26 AWG,6.0 L,RIBBON	80009	175-4473-00
	----- -----			-	(A6P60 TO R1)		
	214-2629-00			1	.PIN,ACTUATOR:	80009	214-2629-00
	352-0162-03			1	.CONN BODY,PL,EL:4 WIRE ORANGE	80009	352-0162-03
	175-4544-00			1	CA ASSY,SP,ELEC:20,28 AWG,3.0 L RIBBON	000EO	OBD
	----- -----			-	(A3P53 TO A5P53)		
	175-4545-00			1	CA ASSY,SP,ELEC:34,28 AWG,5.0 L,RIBBON	000EO	OBD
	----- -----			-	(A1P13 TO A3P13)		
	175-4546-00			1	CA ASSY,SP,ELEC:34,28 AWG,6.6 L,RIBBON	000EO	OBD
	----- -----			-	(A4P34 TO A3P34)		
	175-4547-00			1	CA ASSY,SP,ELEC:40,28 AWG,3.0 L,RIBBON	000EO	OBD
	----- -----			-	(A3P35 TO A5P35)		
	175-4548-00			1	CA ASSY,SP,ELEC:40.28 AWG,6.0 L,RIBBON	000EO	OBD
	----- -----			-	(A6P56 TO A5P56)		
	179-2857-00			1	WIRING HARNESS:INTER CONNECT CABLE	80009	179-2857-00
	214-2629-00			4	.PIN,ACTUATOR:	80009	214-2629-00
	352-0162-05			2	.CONN BODY,PL,EL:4 WIRE GREEN	80009	352-0162-05
	352-0163-09			2	.CONN BODY,PL,EL:5 WIRE WHITE	80009	352-0163-09
	352-0171-00			2	.HLDR,TERM CONN:1 WIRE BLACK	80009	352-0171-00
	198-4650-00			1	WIRE SET,ELEC:	80009	198-4650-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-3696-00			1		MANUAL,TECH:OPERATORS	80009	070-3696-00
	070-3697-00			1		MANUAL,TECH:SERVICE	80009	070-3697-00
	070-4323-00			1		MANUAL,TECH:SERVICE,DIAGNOSTICS	80009	070-4323-00

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.