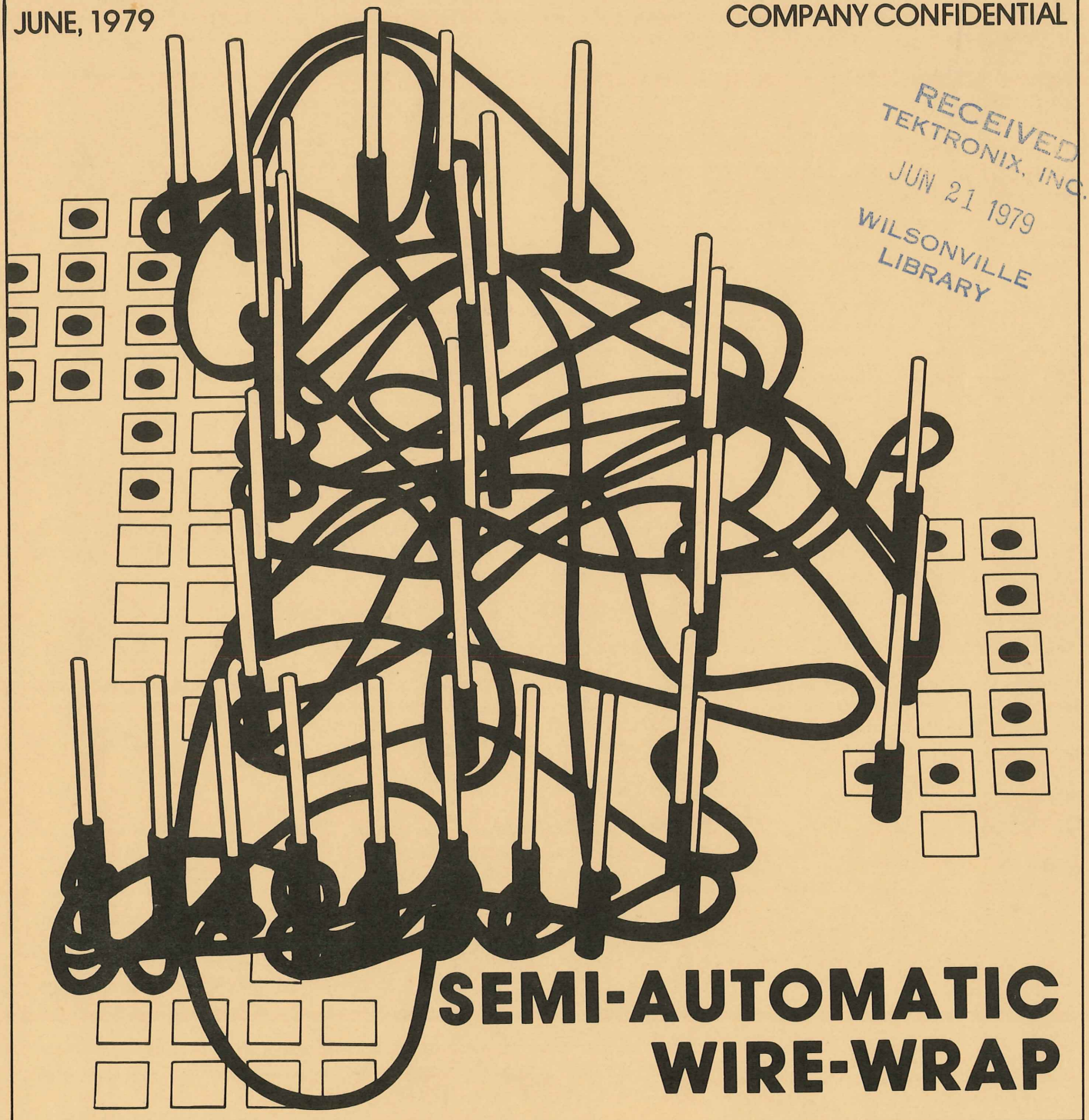
ENGINEERING NEWS

JUNE, 1979

COMPANY CONFIDENTIAL



SEMI-AUTOMATIC WIRE-WRAP

SEMI-AUTOMATIC WIRE-WRAP OFFERS MANY BENEFITS

Glenna Jones, Computer-Aided Design Wire-Wrap, ext. 5781 (Beaverton).

CAD Wire-Wrap (a department of Electrochemical Support) now offers Tektronix engineers semi-automatic wire-wrapping as an alternative to etching for design- and evaluation-phase circuit boards.

Wire-wrapping is an interconnection scheme that provides circuit board transmission paths with wire rather than with etched runs. A wire-wrapped connection is a permanent, solderless, gas-tight, pressure connection. At Tektronix there are two ways to produce a wire-wrapped board: manually and semi-automatically. Compared to manual wire-wrapping, semi-automatic wire-wrapping offers many benefits that are well established by user experience.

The inset on this page compares the wire-wrapped (whether manual or automatic) boards to etched circuit boards.

MANUAL VS SEMI-AUTOMATIC

Compared to manual wire-wrapping, semi-automatic wire-wrapping of multiple board-orders provides much faster turnaround because all the boards in a multiple board order are produced from a single instruction tape.

Though factors such as the number of wires and degree of board and schematic preparation before submission to CAD Wire-Wrap determine turnaround for a

WIRE-WRAPPING VS ECB

For some engineering circuit boards, wire-wrapping (whether semi-automatic or manual) offers four benefits not provided by etching.

The first benefit is faster turnaround time. Many factors affect turnaround time (complexity and preparation of the order, workload, and project priorities), but wire-wrapping is usually much faster than etching circuit boards.

As a second benefit, changing completed wire-wrapped boards is easier because the wires are readily accessible on the back of the board. Cutting and reconnecting wires is much easier than cutting runs on an etched circuit board ... especially if the runs are on the inner layers of a multilayer etched circuit board.

A third benefit is that wire-wrapping costs less than etching. For example, for a board having 75 integrated circuits, the cost of wire-wrapping is about $694 (excluding the cost of the sockets and components). Etching the same board would cost about $2796. Refer to table 1.

As a fourth benefit, creating a new version of a circuit design is easier with wire-wrapping. For semi-automatic wire-wrapping, the designer needs only to edit the output file listing and ask CAD Wire-Wrap to make a new tape, a much faster process than again passing through the lengthy process of revising an etched circuit board. This is a very effective way to reduce the number of versions of a circuit board, thus reducing the time and cost of the project.

CONSTRAINTS

Despite its benefits, wire-wrapping is not suitable for some circuits that contain emitter-coupled and other high-speed logic. Depending on the speed of the circuit and the length of the circuit's transmission lines, problems such as line ringing and crosstalk can be minimized on wire-wrapped boards by (1) avoiding parallel lines through the use of point-to-point wire-wrap (as opposed to routed or picture-frame wrapping); (2) providing proper return paths for fast signals by using twisted pairs; and (3) properly terminating all long lines.

Some instruments with very dense packaging can not accept a wire-wrapped board because the wire-wrap leads protrude 0.6 inches from the back of the board.

For more information about electrical constraints, call Glenna Jones on ext. 5781.

MULTILAYER HAND-TAPED ECB		
PROCESS	COST	HRS.
Engineer gives schematic to EC Design. Mock-up is created.	$2240	140
Mock-up goes to Q.C. and scheduling, then Photography generates film. Film then goes to Fab Lab through Drill, Image, Lay-up/Press, Drill, Through-Hole Plating, Image, Gold Plate, Etch, Routing, and Final Q.C.	$ 430	56
Finished raw ECB goes to Prototype. Load sockets, discrete components, and IC's, and solder everything.	$ 126	6
TOTAL FOR 1 BOARD ORDER	$2796	202
5 BOARD ORDER	4040	226.5
10 BOARD ORDER	5185	258
15 BOARD ORDER	6505	288.5
20 BOARD ORDER	7825	319

MANUAL WIRE WRAP		
PROCESS	COST	HRS.
Engineer gives schematic to Prototype person. Load sockets, discrete components and labels.	$ 144	12
Prototype generates wire list.	$ 96	8
Prototype wraps board.	$ 384	32
Prototype plugs in IC's.	$ 12	1
The cost of an available raw wire wrap board for this particular job.	$ 40	
TOTAL FOR 1 BOARD ORDER	$ 676	53
5 BOARD ORDER	2420	185
10 BOARD ORDER	4600	350
15 BOARD ORDER	6780	515
20 BOARD ORDER	8960	680

SEMI-AUTOMATIC WIRE WRAP		
PROCESS	COST	HRS.
Engineer gives schematic to CAD Wire-Wrap. Load sockets, discrete components and labels.	$ 144	12
Measure board geometry; enter schematic and geometry into Cyber. Edit output listing.	$ 432	36
Punch tape. Set up and wrap board. Final check. Prepare finished board for delivery.	$ 66	5.5
Prototype plugs in IC's.	$ 12	1
The cost of an available raw wire wrap board for this particular job.	$ 40	
TOTAL FOR 1 BOARD ORDER	$ 694	54.5
5 BOARD ORDER	1106	73
10 BOARD ORDER	1636	98
15 BOARD ORDER	2166	123
20 BOARD ORDER	2696	148

Table 1. This table compares costs and turnaround times for manual wire-wrapping, semi-automatic wire-wrapping, and etching prototype circuit boards. The comparison assumes a 9-inch-by-12-inch circuit board having 75 integrated circuits and requiring 1000 wires (for wire-wrapped boards). Costs exclude cost of all sockets and components.

particular project, feedback from engineers indicates turnaround time is lower than for manual wire-wrapping ... except for single-board orders. Semi-automatic wire-wrap turnaround ranges from one day to three weeks, depending on the number of components used, the clarity of the schematic, and CAD Wire-Wrap's workload. Forecasted orders have higher priority than unforecasted orders (if CAD Wire-Wrap's workload exceeds its capacity, farmout is available).

Semi-automatically wire-wrapped boards are less expensive to produce than manually-wrapped boards, except for single-board orders. Refer to table 1 for more information about costs.

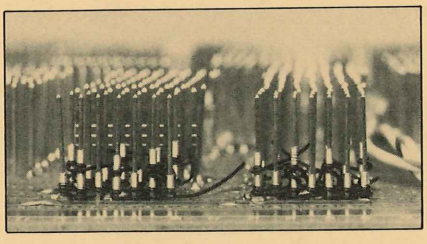


Figure 1. A close-up cross-section of a semi-automatically wire-wrapped board. Using a Standard Logic, Inc. semi-automatic controller, CAD Wire-Wrap personnel can wrap up to 300 wires per hour on boards as large as 26-inches-by-26-inches.

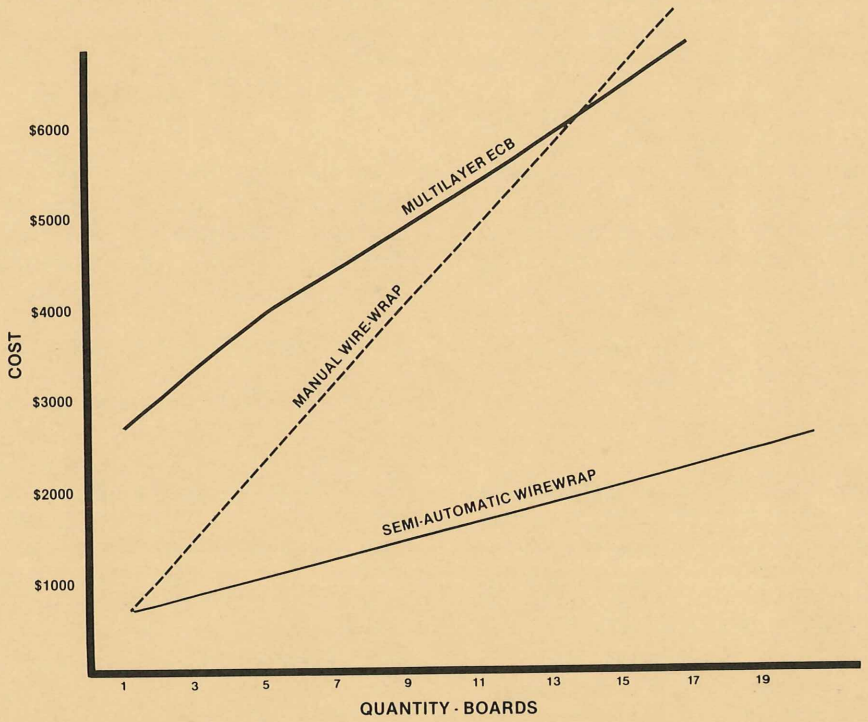


Figure 2. This graph summarizes the data presented in Table 1.

As a third advantage, semi-automatic wire-wrapping frees engineers and prototype support people from long hours spent manually wrapping circuit boards. Semi-automatic wire-wrapping requires as little as one-third the time required to manually wrap a board.

As a fourth advantage, semi-automatically wire-wrapped boards usually require less troubleshooting because the engineer receives a signal-pin listing for editing before the board is wrapped. (The engineer can also use the listing as a reference after the board is wrapped.) Further, troubleshooting multiple-order wire-wrapped boards is easier because all boards are wrapped identically and because changes made on the first board are

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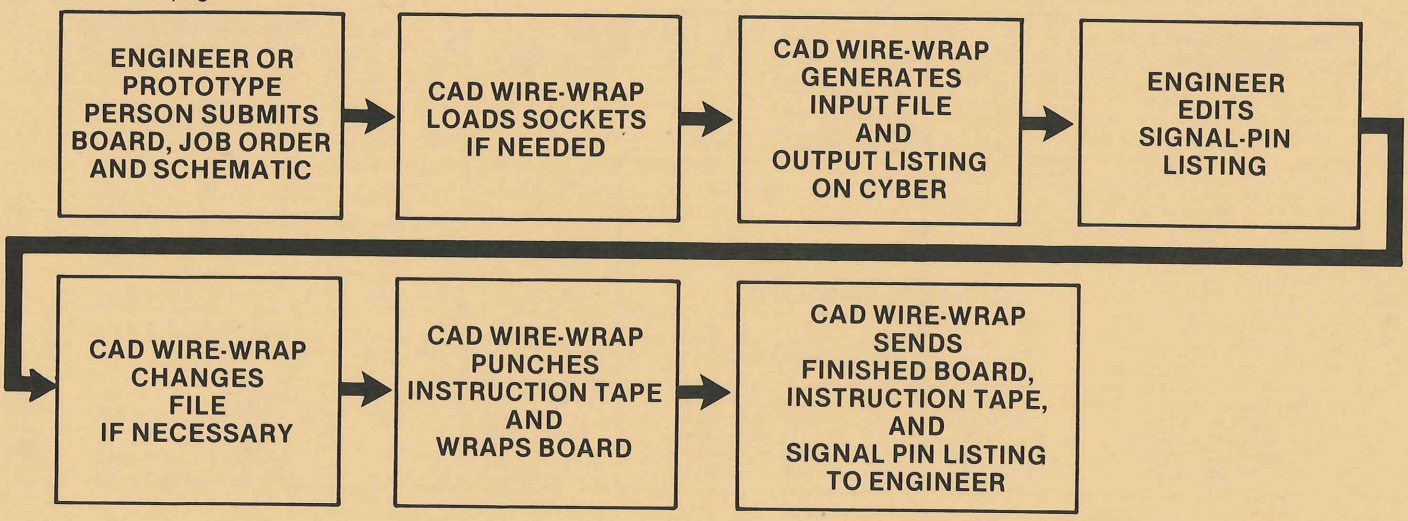


Figure 3. The semi-automatic wire-wrap process.

also made on duplicate boards. CAD Wire-Wrap's error rate is about 0.04% of the wires wrapped.

CAD Wire-Wrap stores wire-wrap numerical control tape files on magnetic tape, providing easy access for later orders of the same board. If an engineer requests additional, but modified boards, CAD Wire-Wrap can more quickly edit the existing file and produce new boards than a manual wire-wrapper could working from a new schematic.

CONSTRAINTS

As figure 1 shows, wire-wrapped pins protrude 0.6 inches from the back of the board. Each connection consists of a helix of eight loops of uninsulated wire wrapped tightly around a pin and one loop of insulated wire leaving the pin (forming one level). Two-level wraps are common; V_{CC} and ground pins sometimes require more levels.

CAD Wire-Wrap's Standard Logic, Inc. controller can accommodate boards up to 26-inches-by-26-inches. CAD Wire-Wrap uses blue 30 AWG Kynar™ wire (silver-coated, annealed copper with 0.005-inch Kynar™ insulation, Underwriters Laboratory certified to 105°C).

RELIABILITY

Bell Telephone Laboratory and military organizations have thoroughly tested wire-wrapped connections. The Army's wire-wrap military specification is Mil Standard 1130A; the Navy's is WS 6119.

The wire-wrap connection holds up well under high temperature, corrosive atmosphere, and high humidity. A wire-wrap connection's life expectancy is about 40 years.

COMPONENT CARRIERS

CAD Wire-Wrap uses new discrete-component carriers to make semi-automatic wire-wrapping faster and more reliable. Wrapping a wire directly to a discrete component having round leads produces a poor electrical connection. Using component carriers assures good connections. The May 1979 (No. 270) **Component News** described these carriers. For a copy, call Technical Communications on ext. 6867.

EXPERIENCE

Engineers and prototype people in the following areas report good results with semi-automatic wire-wrapping: Integrated Circuits Manufacturing, CAD Development, Frequency Domain Instrumentation Engineering, Graphic Computing Systems Engineering, Information Display Products Engineering, Logic Development Products Engineering, Accessories Engineering, and T.V. Products Engineering.

FOR MORE INFORMATION

For more information about semi-automatic wire-wrapping, call Glenna Jones on ext. 5781. □

BYPASSING AND DECOUPLING SEMINAR SET

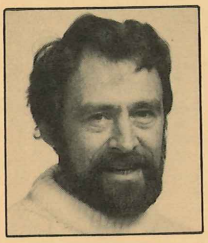
A seminar on bypassing and decoupling will be held in the Tek auditorium, Bldg. 50 June 12 at 2:30 p.m. Laudie Doubrava will present his paper titled **"Design Techniques for Controlling Point-of-Load High Frequency Performance of Power Supplies,"** which was given at POWERCON VI in May.

The seminar will cover several topics, with an overall view of bypassing and decoupling in power supply circuits. Emphasis will be on control and suppression of power supply noise.

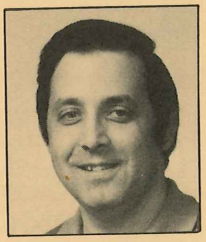
For more information, call Laudie Doubrava, ext. 1119. □

PATENT RECEIVED

COBALT COLLECTOR-TARGET FABRICATION PRODUCES HIGH YIELDS



Jerry McTeague, Storage CRT Engineering, ext. 5378 (Beaverton).

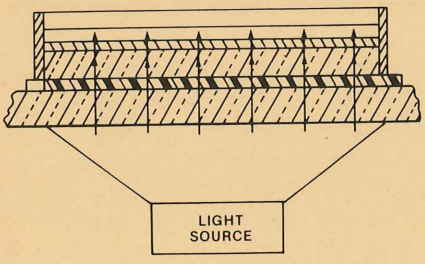


Ken Stinger, Electronic Technology Applications, ext. 7111 (Beaverton).

Developed over a six-year period, the patented storage-tube target fabrication process described here produces targets for most Tektronix storage tubes, ranging from the 214 500KHz Dual-Trace Storage Oscilloscope to the 25-inch tube 4016 Computer Display Terminal.

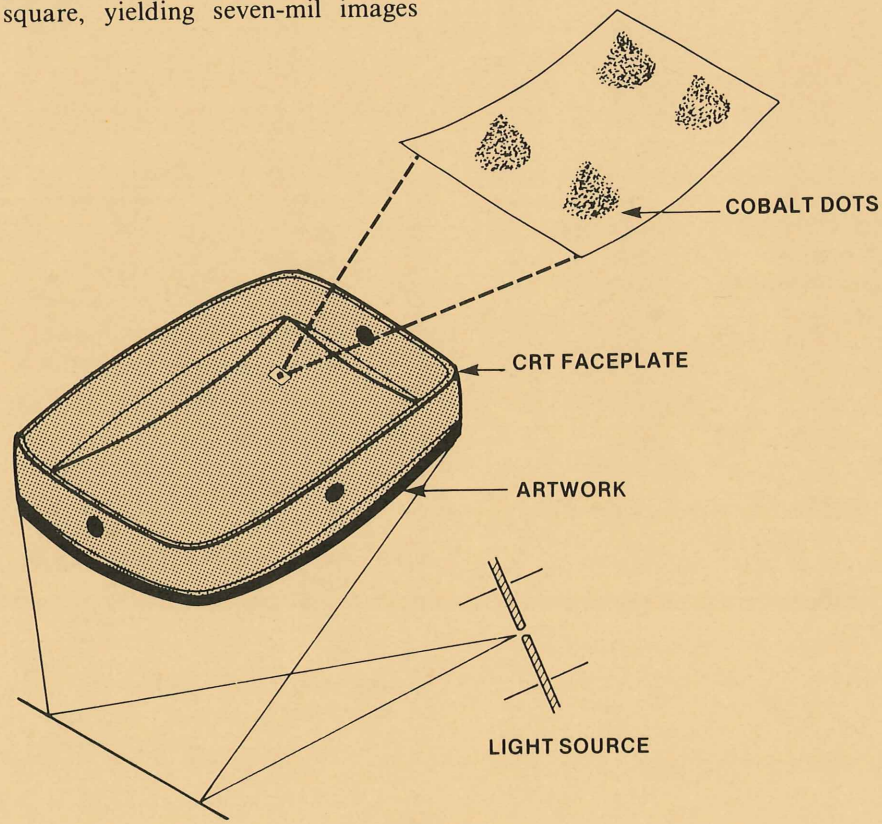
A direct-view bistable storage tube is a low voltage (200 volt) display that has flood guns as well as a writing gun. Unlike conventional crt screens, the bistable storage crt screen is not aluminized. A transparent conductive film coating on the faceplate conducts the writing gun charge and maintains the proper operating voltage. A path through the screen's phosphor provides secondary electron collection and conduction. Storage CRT Engineering thoroughly investigated the configuration of this path because it largely determines the tube's resolution, luminance, and contrast. A regular dot configuration works best. Using a low-power magnifier, you can see this configuration on a 4051 BASIC Computing System screen. The configuration is similar to the dot pattern of a high-quality halftone magazine reproduction.

During fabrication, an exposed film or screen mask touches the outside of the crt faceplate. A light source, six feet away, forms an image of the configuration through the glass and onto the internal surface of the faceplate.



An operator pours an aqueous slurry of dichromated polyvinyl alcohol, alcohol, and cobalt metal powder onto the internal surface of the faceplate, exposes it for three minutes, pours off the slurry, rinses with water, and dries with alcohol or acetone. This last step also shrinks the gelatinous polyvinyl alcohol (PVA) metal powder images to form three-mil diameter dots, one to two mils thick. This shrinkage is necessary on large curved screens because the dot pattern apertures are 4.5 mils square, yielding seven-mil images before shrinking. This shrinking can be performed only with a wet PVA process.

In a manner similar to PVA metal dot deposition, phosphor is deposited with the black cobalt dots serving as a photomask. Using a wet deposition process (rather than dry films) and an exposure scheme that doesn't require contact between artwork and working surface is a versatile, fast, and economic process. Though this fabrication process doesn't require clean-room conditions, target yields are close to 90% (typically fewer than ten of the more than 4,000,000 dots on a given 25-inch faceplate are defective). □



SEVEN NEW MEMBERS JOIN ENGINEERING ACTIVITIES COUNCIL

In February, seven new members joined the Engineering Activities Council. At the same time, other Council members, who have been with the Council since mid-1977, left the Council (members serve for about 18 months). The new members are Jim Besemer, Ron Bohlman, Elske Cordell, Wayne Kelsoe, John Moore, Tom Woody, and Jim Zook. Table 1 lists the Council members.

EAC CHARTER

The Council's primary objective is to provide engineers with a forum in which to present directly to management what engineers themselves consider to be important in technology. To meet their charter, the Council has sponsored 13 Engineering Forums ("Engineers Talk to Managers").

In each forum, four or five engineers discuss their viewpoints on the problems and progress of new technology. The forum chairpersons are Council members. They select forum speakers from the engineering community. The audience consists of approximately 125 corporate, divisional, and departmental managers. Attendance is limited by the capacity of the auditorium, but the forum presentations are published as **Forum Reports** (to add your name to the **Forum Report** distribution list, fill out the coupon on the inside back cover and mail it to 19-313).

FOR MORE INFORMATION

To suggest a forum topic or if you have questions about the Council, call one of the members (table 2 lists their phone numbers).

Table 2 lists past forums. Technical Marketing Communications has published **Forum Reports** for forums 1-12. For a copy of any of these **Forum Reports,** call ext. 6795. □

Bruce Ableidinger	LID, LDP Engineering	1742
Tim Flegal	LID, TM500 Engineering	1533
Jim Tallman	LID, 7000 Series	7076
Dave Armstrong	SID, Accessories Engineering Design	5244
Jim Besemer	SID, DSI Firmware	7604
Wayne Kelsoe	SID, Portables Engineering	6255
Ron Bohlman	Technical Support, CAD Development (Town Center)	221
Lynn Saunders	Technical Support, Software Engineering Research	5616
Hal Cobb	Tek Labs, Hybrid Circuits	6564
Elske Cordell	Tek Labs, Hybrid Packaging	7079
Hock Leow	Tek Labs, Signal Processing Research	5654
Mike Rieger	Tek Labs, Signal Processing Research	6907
Binoy Rosario	Tek Labs, IC Design	6362
Tom Woody	Tek Labs, Display Devices	7147
Mike McMahon	Communications, FDI Engineering	5678
Jim Zook	Communications, TV Engineering	7457
John Moore	IDD, IDP Engineering	2648

Table 1. Bill Walker, executive vice president, selects Council members from a list of candidates who are nominated through three channels: (1) by managers of engineering departments, (2) by current Council members, or (3) through the candidates' own initiative (Engineering News articles announce Council openings). The current Council members are listed here.

	FORUMS	CHAIRPERSONS
1.	General Purpose Interface Bus	Robert Chew, Paul Williams
2.	A-D and D-A Converters	Bob Nordstrom, Mike Boer
3.	Video Display Techniques	Steve Joy, Phil Crosby
4.	New Technologies: I	John Addis, Bob Burns
5.	New CRT Technologies	Bob Oswald, Cal Diller
6.	Creative Microprocessor Hobby Projects	Dave Chapman, Joyce Lekas
7.	Managers Talk to Engineers	Mike Boer, John Mutton
8.	Microprocessor Design Pitfalls	Robert Chew, Paul Williams
9.	New Technologies: II	Hock Leow, Binoy Rosario
10.	Packaging	Bob Burns, Cal Diller
11.	Creative Microprocessor Hobby Fair Projects: II	Steve Joy, Hock Leow
12.	Reliability	Tim Flegal, Mike McMahon
13.	Managing Firmware Throughout Its Life Cycle	Lynn Saunders, Jim Tallman, Dave Armstrong

Table 2. In the last two years, the Engineering Council has sponsored 13 forums in which engineers presented (to corporate, divisional, and departmental managers) engineers' views of the problems and progress of new technology at Tektronix. The forum presentations are described in forum reports, which are distributed over the Engineering News mailing list. For a copy of a forum report listed here, call ext. 6795. Forum Report 13 available 15 July 1979.

Engineering Activities Council members and support people: *front row, left to right,* **Jim Tallman, Hock Leow, Tom Woody, Bill Walker, Hal Cobb, Elske Cordell, Wayne Kelsoe, George Dunn (support), and Karen Hall (support).** *Back row, left to right,* **Lynn Saunders, Mike Rieger, John Moore, Bruce Ableidinger, Dave Armstrong, Tim Flegal, Jim Zook, Ron Bohlman, and Jim Besemer. Council members not shown are Mike McMahon and Binoy Rosario.**

ENGINEERING NOTEBOOKS

Engineering notebooks are valuable because they provide evidence in patent disputes and because they are a convenient reference for engineering information. In the following article, the Patents and Licensing Department answers some of the questions frequently asked about engineering notebooks.

WHY ARE THEY USED?

Engineering notebooks have two main functions. One is to provide the information Tektronix may need to prove that disputed inventions were conceived and reduced to practice by Tektronix employees. The other function is to provide a reference source for engineering concepts and data.

In disputes concerning inventions, time is a critical element. Engineering notebooks can show when the concept of the invention was recorded and when the working model of the invention was made and tested. Evidence of those dates is required by the U.S. Patent and Trademark Office when more than one inventor is attempting to patent the same invention.

WHAT ARE THEY?

Tektronix engineering notebooks are bound volumes of lined and consecutively-numbered pages. Each notebook is assigned a number and is issued to the person who signs for it. If you have a notebook but you are leaving Tektronix, you must return it to the Patents and Licensing Department because the notebook is Tektronix property.

HOW SHOULD THEY BE USED?

When you start a new project or experiment, go to Patents and Licensing and pick up a notebook. This book is assigned to you by name and number. As your project develops, include sketches, block diagrams, schematics, theory of operation, test data and anything else that will establish the concept and the working model of the invention. Of course, unnecessary information clutters the book and weakens its value as a reference.

Concepts and data should be recorded as soon as they are available to avoid the inaccuracies and omissions that seem to occur with the passage of time. The pages must be dated and signed by two witnesses. While it isn't necessary to witness every page, witnessing every five or ten pages should include a statement about which pages are being covered.

WHERE DO I GET ONE?

You can obtain an engineering notebook from the Patents and Licensing Department by calling ext. 7787. □

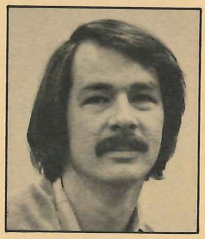
NASA TECHNICAL BRIEFS

Technical Standards has an Index to the National Aeronautic and Space Administration **Technical Briefs.** These briefs are short articles on a wide field of new technology derived from NASA's research and development activities.

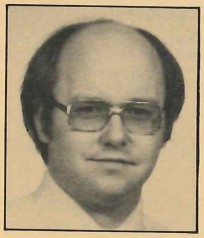
To use the index, drop by d.s. 58-187. To borrow a **Brief,** call ext. 7976. □

PATENT RECEIVED

FEEDBESIDE CIRCUIT CORRECTS FOR "THERMALS"



John Addis, Laboratory Instruments Division Engineering, ext. 6596 (Beaverton).



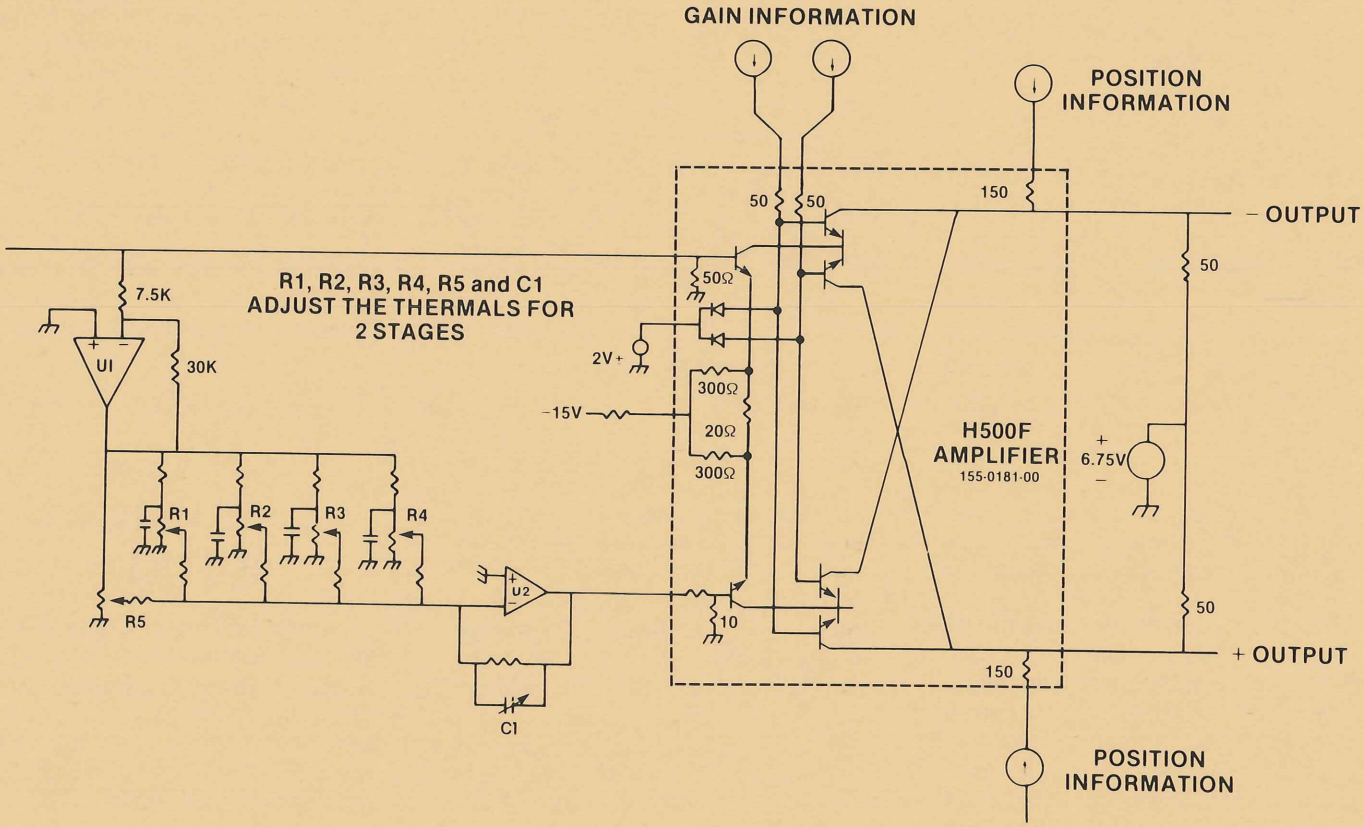
Bruce Hofer, TM500 Engineering, ext. 1522 (Walker Road).

The patented circuit shown here corrects amplifier output signals for "thermals," low-frequency deviations from a perfect step response in very wideband amplifiers.

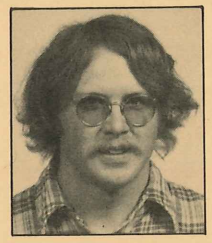
Previous correction circuits placed several resistor-capacitor series networks in parallel with a common-emitter amplifier's emitter gain-setting resistor. Such designs have a serious disadvantage for amplifiers having less than a 300 picosecond risetime: the networks' large parasitic lead inductance introduces a time constant.

Instead of increasing the high-frequency amplifier gain with resistor-capacitor networks, this feedbeside circuit reduces low-frequency gain to the level of the mid-frequency gain. Consequently, feedbeside circuits don't require high-frequency circuitry or critical lead lengths.

The 7A29 Amplifier and the 7104 1-GHz Oscilloscope use feedbeside circuitry. □



AUTOMATIC METAL MONITOR SUPPORTS RELIABILITY ASSURANCE



John Richartz, Integrated Circuits Manufacturing, ext. 7930 (Beaverton).

Integrated Circuits Manufacturing Reliability Assurance has developed an Automatic Metal Monitor (AMM), a microprocessor-based system that tracks performance of metallized runs on integrated circuit dies undergoing stress tests.

The monitor automatically calculates the resistance of the metallized runs from voltage measurements across each run. Each test die has a constant current flowing through it at an ambient temperature of 175°C. This high temperature and current density cause electron migration resulting in voids in the metal line much sooner than at normal temperatures and currents.

The AMM sequentially measures the voltage across each die in a test array in the oven. Analog signals characterizing the current flow through the die and the voltage drop across the die pass through an analog-to-digital converter and then to processing circuitry.

An internal real-time clock enables the AMM to record the time that each die begins a test and the time of failure. The AMM also stores each previous resistance and current measurement in case a run opens between readings (performed approximately every ten minutes).

TIME SAVINGS

THE AMM eliminates the need for an operator to make time-consuming, tedious, and error-prone manual measurements. The AMM measures resistance with .2 ohm accuracy and a five-minute time-of-failure accuracy (the AMM requires 10 minutes to scan a full load of devices). Manual measurements would have required three hours to measure the 250 dies that the Monitor now measures in ten minutes. Using the AMM greatly improved measurement accuracy and greatly facilitated continuous monitoring.

SOFTWARE

AMM software performs several functions: identifying die and test limits, controlling device scanning, calculating device resistance, and recording device failures and failure times.

The software has six operator commands available through front-panel pushbuttons. For a device or group of devices, STATUS prints a summary of such information as device identification, test start-time, failure time, and present and previous current and resistance measurements. INITIATE TEST enters devices into the test scan. POWER SUPPLY displays the most recent power supply reading. CLEAR invalidates the preceding

Continued on page 11

BACKGROUND

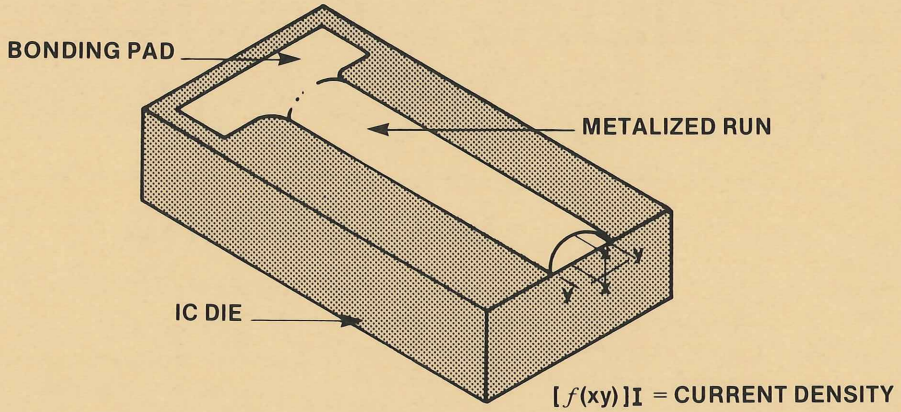
To ensure the reliability of Integrated Circuits Manufacturing's monolithic and hybrid components, the ICM Reliability Assurance Group regularly conducts life-tests on those components and (to monitor the metallization production process) on the metallization that interconnects circuit elements on component dies.

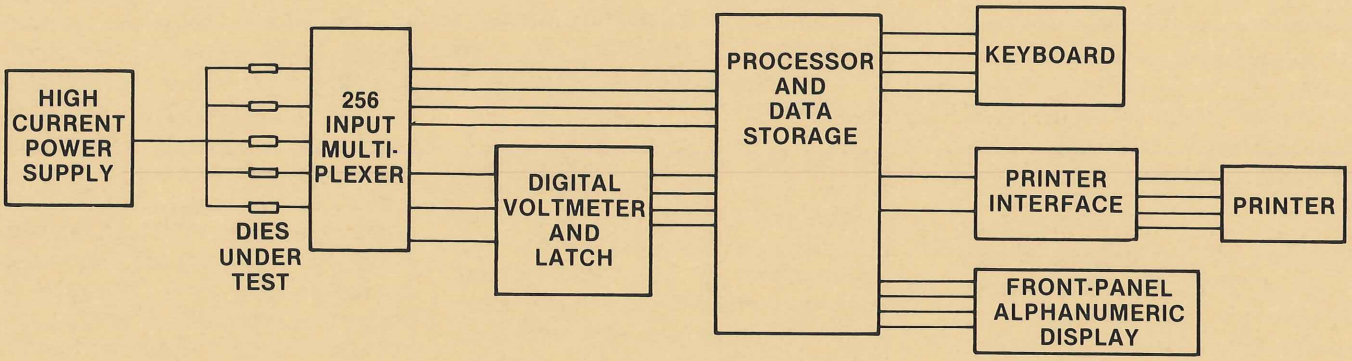
Every two weeks, two test wafers are run through the metal evaporation process. Reliability Assurance subjects some dies (packaged in TO-5 cans) from these wafers to life tests. Each die contains several metallized runs, one of which is life-tested.

High current density (as high as 10^6 amperes/square centimeter) and high temperature (typically 175°C) accelerate the testing, producing failures much more rapidly than under normal operating conditions. The failure mode is an open metallized run, resulting from metal migration due to high temperature and high current density. (Metal migration is an irregular movement of metal molecules in the direction of current flow.)

Until recently, Reliability Assurance periodically tested small quantities of dies by using a digital voltmeter to manually measure the resistance of each metallized run. High or infinite resistance indicates a failure. Even for just a few test wafers, this manual procedure is very time consuming. Another drawback to manual testing is that there is no way to accurately determine when a failure occurs. Reliability Assurance process engineers use time-of-failure to determine metal lifetime, to compare various metal schemes, and to monitor variations in production processes and activation energy.

Reliability Assurance planned to regularly monitor ICM production metallization, but doing so manually would be prohibitively expensive. Therefore, in January 1978 Reliability Assurance studied the feasibility of automating the testing process and decided to build an Automatic Metal Monitor.





THE HARDWARE

SYSTEM OPERATION

The Automated Metal Monitor consists of a data-processing section, a data-acquisition section, and a power supply.

The data-processing section consists of the microprocessor and its associated components, a front-panel alphanumeric display, a printer, and a keyboard for entering operator commands.

The data-acquisition section is a 256-input multiplexer associated with 256 current sources and an analog-to-digital converter.

THE MICROPROCESSOR

As a processor, the Mostek/Fairchild F-8 serves the Monitor well by providing truly bidirectional input/output ports that allow a system designer to easily interface the processor to a data acquisition section (the processor can send control and receive data signals through the same ports with only IN and OUT commands).

The F-8 performs all housekeeping functions: accepting operator keyboard commands, controlling the input multiplexer and analog-to-digital conversion circuitry, calculating resistance, recording failures, and displaying data summaries on a printer and on a front-panel alphanumeric display.

POWER SUPPLY PROBLEMS

The power supply design required a solution to special problems. An industrial environment (such as the one Reliability Assurance operates in) is especially hard on microprocessor-based equipment. The power line to which the AMM is connected also serves 20 ovens and their associated power supplies and signal sources. Radio-frequency heaters for semiconductor and crt production also operate in the building.

While being assembled and tested, the AMM ran on a "clean" power line and presented no operating problems.

However, when placed in the working environment, the AMM performed strangely (for example, it tried to execute the data storage area). Power transients produced by other equipment on the same power line were the cause. Power line filters didn't remove the transients, but rf bypassing circuits in the system power supply output did remove them.

Continued from page 9

data entry. STORE DISPLAY indicates valid input data.

AMM PROM-resident test, diagnostic, and calibration routines enable the system operator to easily locate system failures and to verify system calibration. Connecting an RS-232-compatible terminal to the AMM makes these routines available to the operator.

The AMM has 4K bytes of ram for data storage, and 5K bytes of rom for storing the operating system, test routines, diagnostic routines, calibration routines, and output routines.

FOR MORE INFORMATION

For more about the Automatic Metal Monitor, call John Richartz on ext. 7930 (Beaverton). □

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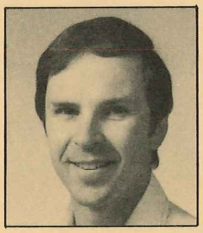
PATENT RECEIVED

HOUSING SHIELDS STRIPLINE MICROWAVE CIRCUITRY

Carlos L. Beeck, Frequency Domain Instrumentation Engineering, ext. 7996 (Beaverton).

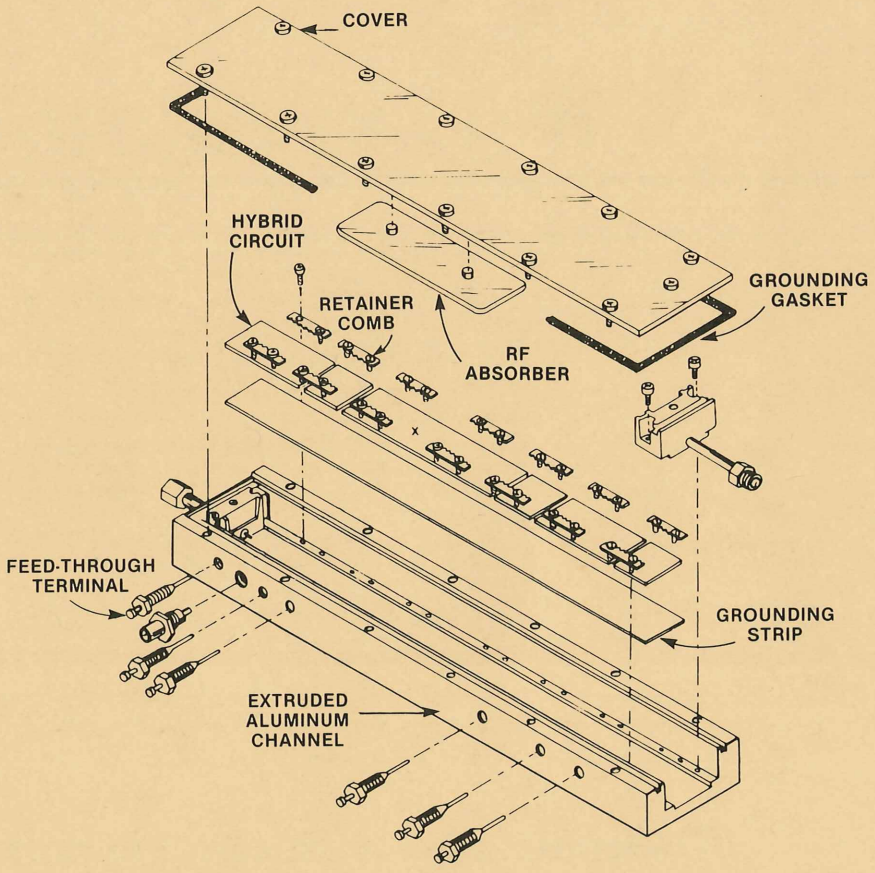


Phil Snow, Spectrum Analyzers Electrical Engineering, ext. 6146 (Beaverton).

The device shown here provides stable, shielded housing for stripline hybrid microwave circuitry. This modular housing consists of an extruded aluminum channel (which may be any length) and standardized subparts such as a grounding plane, substrates, substrate retainers, end-caps, a grounding seal, and interconnections.

The TR501 and TR502 Tracking Generators and the 492 Spectrum Analyzer use this housing for microwave stripline circuitry.

During housing assembly, Manufacturing personnel position stripline circuits (printed on substrates) on resilient conductive grounding strips in the channel extrusion, hold the circuits in place with retainer combs, and use feed-through terminals on the side of the housing to connect the circuits outside the housing. RF signals pass through end-caps or side-walls. □



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How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle and the timeliness of the content). But the *minimum* is six weeks for simple announcements and about ten weeks for major articles.

The most important step for the contributor is to put the message on paper so that the editor will have something with which to work. Don't worry about organization, spelling and grammar. The editor will take care of those when he puts the article into shape for you.

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