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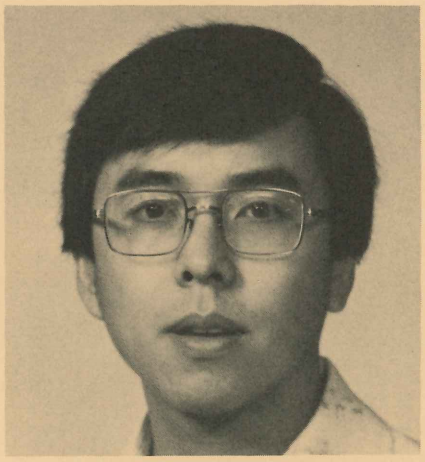
FORUM REPORT 9

NEW TECHNOLOGIES: II

Bill Walker (T&M Group vice president), in November 1976, formed the Engineering Activities Council to provide engineers with a forum in which to present directly, to multiple levels of management, what engineers themselves consider important in technology.

The subject of the ninth forum, presented in March 1978, was New Technologies: II (the first New Technologies forum was presented in 1977). **Bill Walker** introduced the forum chairmen: **Hock Leow** (Applied Research) and **Binoy Rosario** (Monolithic Circuits Engineering). In turn, Hock and Binoy introduced the forum panel members: **Sal Emmi** (Applied Research), **Barrie Gilbert** (Monolithic Circuits Engineering), and **Chris King** (Materials Research), **Ron Robinder** (ext. 6643, Display Device Engineering), and **Tadanori Yamaguchi** (ext. 6005, Applied Research).



Hock Leow (Applied Research).

Binoy Rosario (Monolithic Circuits Engineering).

COCHAIRMEN

FINE-LINE PHOTOLITHOGRAPHY

Sal Emmi, Applied Research (Tek Labs), ext. 5713.

Fine-line lithography is an essential key to opening the door to another generation of phenomenal progress in microelectronics. Those companies with the foresight and desire to profit from the market opportunities that will be created by advances in this area are already vigorously scrambling toward the development of electron-beam lithographic techniques, dry plasma etching and other advanced process technologies.

PHOTOLITHOGRAPHY

Photolithography is a combination of microscopic photoimaging and etch procedures. As shown in Figure 1, the photolithographic process starts with a wafer of single-crystal silicon on which a protective layer of silicon dioxide has been thermally grown. It is next coated with photoresist, a light-sensitive material, and then the whole wafer surface is exposed to ultra-violet light through a photomask which duplicates the pattern for the first layer of the circuit. Just as in any photo process, this image is now developed. Here, this means removing the photoresist in selected areas. The wafer is then ready to be chemically etched in hydrofluoric acid after which the photoresist is removed. This leaves a wafer protected with silicon dioxide except in the etched pattern area where the bare silicon is exposed.

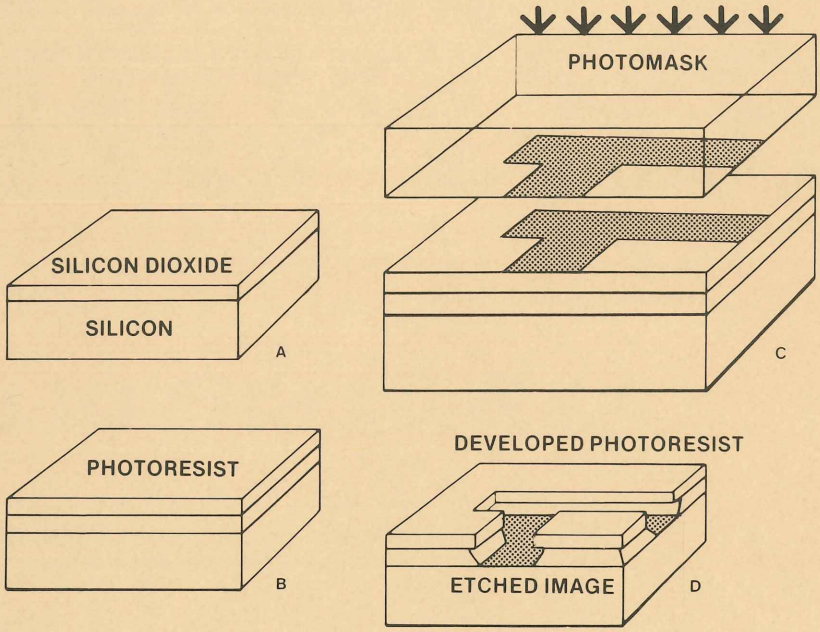


Figure 1. There are four steps in the photolithographic process. Step A: The silicon wafer goes through a thermal oxidation process that grows a silicon dioxide layer. Step B: The wafer is coated with photoresist, a light-sensitive material, and baked. Step C: The wafer is exposed to ultraviolet light through a photomask to duplicate the circuit image. Step D: After developing the photoresist image, the wafer is immersed in hydroflouric acid to remove the silicon dioxide not protected by photoresist. Photoresist is then stripped away by another chemical treatment.

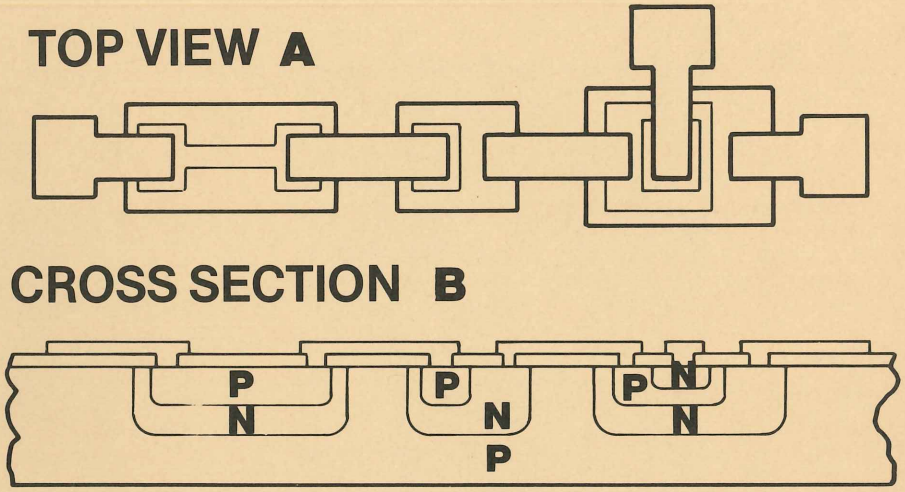


Figure 2. This is a top (A) and cross-sectional (B) view of a circuit composed of a resistor, diode and transistor. The precise alignment of consecutive masking steps is an exacting and difficult challenge.

The wafer is now ready for one of several stages of impurity ion diffusion, a process that forms the semiconductor circuit elements. After fabricating these elements, which typically involves many layers and photolithographic processes, the wafer is coated with metal. The metal can be patterned to form the interconnect structure that ties all the circuit elements together.

PHOTOLITHOGRAPHIC CHALLENGES

The precise alignment of consecutive images is one of the most difficult and exacting challenges facing the photolithographic engineer. Alignment often requires sophisticated and expensive equipment. Figure 2 illustrates a simple integrated circuit and indicates the challenges photolithographic engineers face.

The illustration is a top and cross-sectional view of a circuit composed of a resistor, a diode and a transistor. In recently-produced integrated circuits, spacing between circuit elements is so critical to circuit performance that the allowable variation in distance between elements is often less than a micron. Besides alignment problems, photolithographic engineers also face difficulties with the resolution of geometries less than .1 mil.

ADVANCES

The photolithographic process was first used for making transistors in the mid-1950's. At that time, engineers fabricated devices with minimum line widths of only 5 mils, about twice the thickness of human hair.

Today, some semiconductor houses are working with line widths less than 0.1 mil. Many firms hope to print line widths less than a micron (0.04 mils) by the 1980's. This is part of an expensive and fiercely competitive race to build a giant computer on a single silicon chip.

Figure 3 shows how much circuit area for electronic calculators has been reduced since the 1960's.

Photolithography shares credit for reducing circuit size with numerous circuit and process innovations developed in the 1960's. Along with reduced circuit area, industry has made many other impressive improvements in circuit performance, reliability and cost reduction.

It's difficult to adequately convey the magnitude of these past accomplishments in microelectronics. As an analogy, imagine automotive technology advancing as far as electronics in 15 years. Our cars would be capable of speeds up to one-quarter million miles per hour, would have a mileage rating of over 100,000 miles per gallon, and would be cheaper to throw away than park for a day in downtown Portland.

THE FUTURE

For commercial applications, lower costs are as important as performance advances. Keep in mind that photolithographic engineers' primary goal is to greatly increase the logic and memory capacity of a single silicon chip. However, bigger memory is not acceptable if it is more expensive. Memory costs must drop enough to allow integrated circuits to compete with other memory technologies. There are three ways to reduce costs: develop more complex circuits (and therefore larger chips), automate production, and use higher packing densities.

Unfortunately, the larger chip area required by more complex circuits increases the chance of defective circuit elements because of particulate contamination. This disadvantage has forced many manufacturers to introduce extensive process and contamination control procedures for every stage of the fabrication process. Yields have increased as a result, but not enough.

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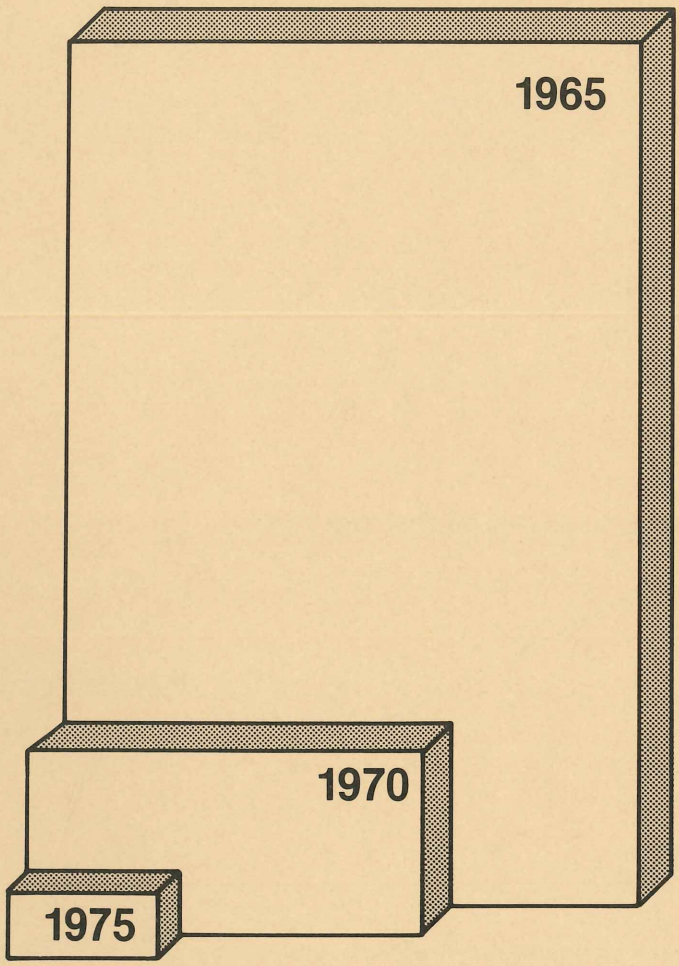

Figure 3. Since 1965, advances in fine-line photolithography have allowed electronic calculator manufacturers to greatly decrease circuit area.

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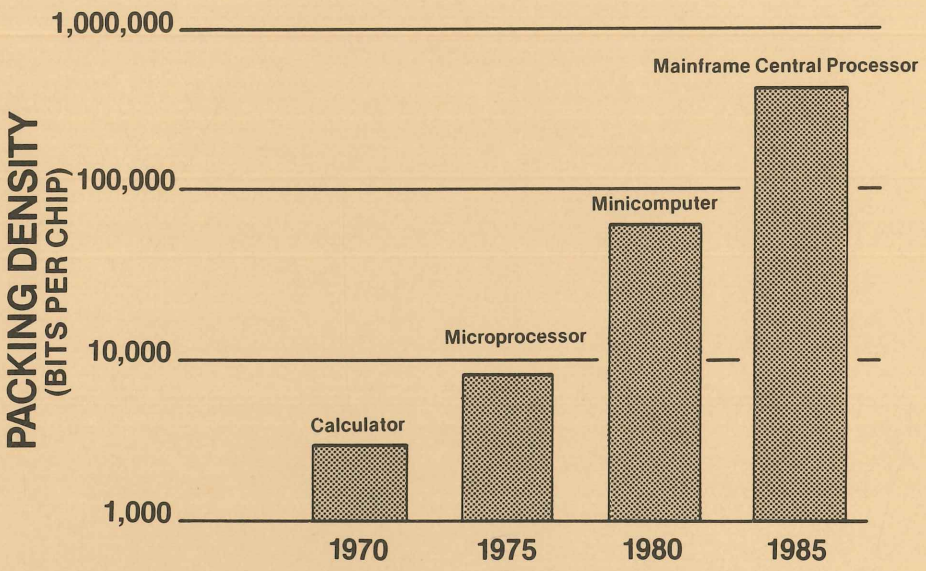


Figure 4. Higher packing density is one way to produce more complex circuits. The increase in higher packing density in the past 10 years has been dramatic.

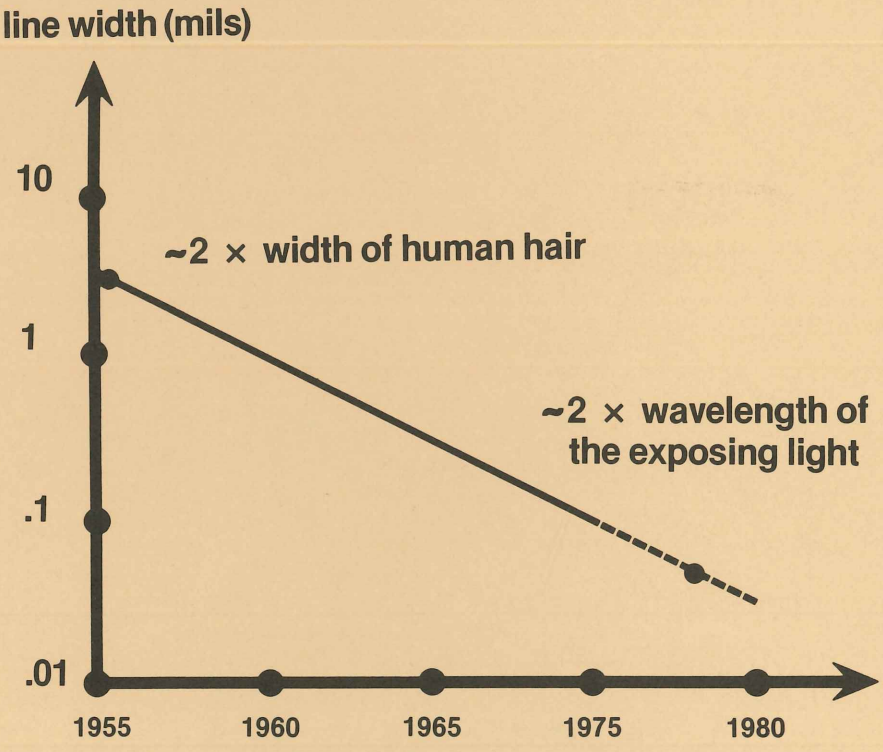


Figure 5. With existing photolithographic systems, lines can be made as narrow as one micron. Only electron-beam exposure systems can achieve smaller line widths.

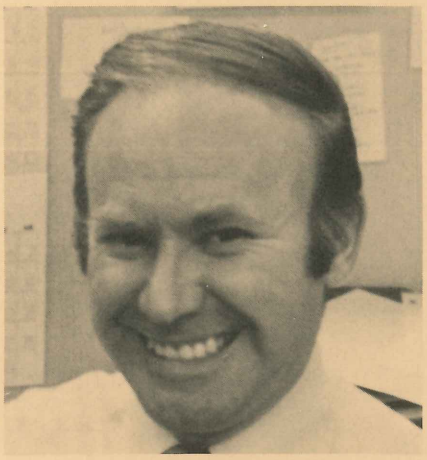
So, some companies are developing automated fabrication processes. In-line continuous-processing equipment is replacing traditional batch-processing. Automation of many processes is improving yields and efficency by eliminating operator errors and by bringing many processes together in one piece of equipment.

Higher packing densities are another way to produce more complex circuits. (Figure 4 shows the packing density trend.) But higher packing densities require new photolithographic technologies. Because optical lithographic systems have limits in the one micron/linewidth region, the semiconductor industry must use electron-beam exposure systems for integrated circuits that have line widths less than one micron. Electron-beam exposure systems can write circuit patterns directly on the coated silicon wafer. They can also prepare high resolution masks that can be used to pattern wafers with X-ray exposure.

Commercialization of these new photolithographic techniques could cause a tenfold reduction in the size of individual circuit elements and a hundred-fold reduction in circuit area. (See figure 5.) Because this potential is so great, many U.S.-based companies such as IBM and Texas Instruments have entered a multimillion dollar international competition to achieve very large scale integration (VLSI) with these new lithographic techniques. The primary tools of the VLSI race are electron-beam direct-wafer writing, dry plasma etching, and computer-controlled processing.

Although Tektronix is not in the VLSI race, we will be affected by its outcome. There is little doubt that submicron photolithography will be a commercial reality in the 1980's. We cannot ignore the potential impact this will have on our long range planning. Further performance improvements in many of our custom integrated circuits may not be possible without the use of submicron photolithographic techniques. Furthermore, we cannot afford to willfully give to our competition any advantages that submicron capabilities will provide. □

WAFER LASER-TRIMMING



Barrie Gilbert, Monolithic Circuit Engineering (Tek Labs) ext. 6283 (Beaverton).

Since the founding of Tektronix, an enemy has been lurking in our midst. Though plainly visible, the enemy has not been recognized as such, and, apart from engineering wit, the weapons for ousting him were not available. Open any Tektronix-made instrument and the enemy, the Notorious Tweak, glares back at you. Laser-trimming is the weapon that promises to greatly curtail his number if not wipe him out altogether.

Why limit the number of potentiometers? Primarily because traditional (post-assembly) adjustments are expensive. First, the potentiometers cost money and require board space. Second, the labor cost for adjusting instruments with potentiometers is high. Third, calibration equipment for several locations is expensive. And, fourth, manual writers must carefully explain to field people each step of an adjustment procedure.

Apart from these overt costs, there are invisible costs of field miscalibrations due to mechanical shock, humidity and misguided tweaking. In the long run, our reputation as a manufacturer of well-conceived and reliable equipment is involved.

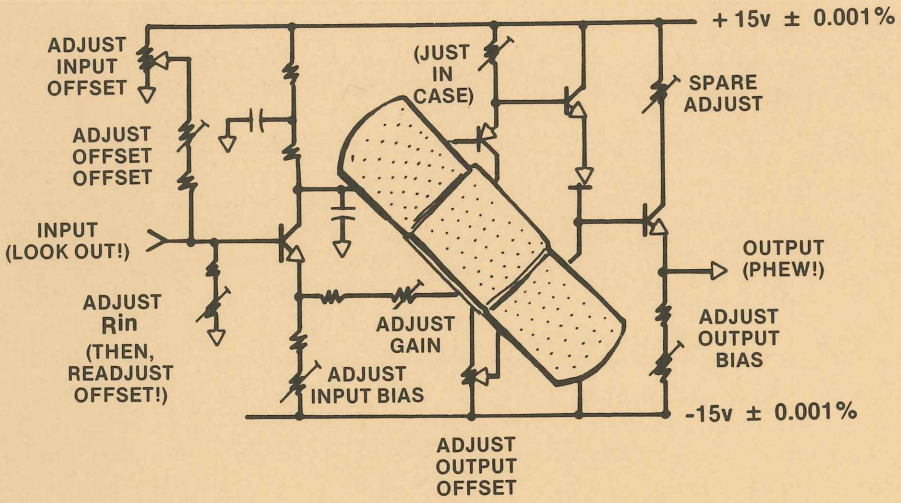


Figure 1. An extreme example of a circuit in which potentiometers are used as Band Aids for a carelessly designed circuit.

AVOIDING BAND-AIDS

The Notorious Tweak poses another danger. All too often, adjustments are design "Band-Aids," because it's not too clear to the designer what the circuit is really doing. Perhaps the example in figure 1 is extreme, but I have known of circuits in which two tweaks were used where one, or better yet, none, might have been used if more thought had been applied at design time.

Of course, the advent of laser-trimmed hybrid and monolithic circuits will not eliminate all post-assembly adjustments overnight. And, as we design more digital products, there will be less need for adjustments. Nevertheless, we still have a continuing commitment to the noble analog circuit and Tektronix will manufacture many more such circuits in monolithic integrated form.

Let's briefly review the benefits of laser wafer-trimming.

LASER-TRIMMING BENEFITS

Lower manufacturing costs is the greatest benefit. To achieve lower manufacturing costs, we use special thin-film nickel-chromium or silicon-chromium resistors instead of the usual diffused resistors. We use a laser beam to adjust the resistor to an exact value. Computer-directed precision measurement systems control the laser beam. Trimming typically adds about 25 cents to the cost of manufacturing monolithic circuits in large quantities, a real bargain. The trimming process is fully automated: one wafer containing typically 300 circuits can be measured and trimmed in less than ten minutes. In the trimming set-up, all calibration systems are near the laser system, eliminating expensive distributed equipment and its maintenance.

Unlike manual adjustments, on-the-chip adjustments are very **stable**. Manufacturers such as Analog Devices (laser trimming pioneers)

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and Harris Semiconductor routinely achieve differential temperature coefficients as small as a few ppm/°C. Once trimmed, a glass-like passivation layer protects the resistors from contamination and humidity. Also, microtrimmed resistors are out of reach of well-intentioned, but tweak-happy hands.

A subtle benefit of trimming is the **discipline** it requires of the designer. For a monolithic circuit having external adjustments, the designer may defer defining the required trim range or, worse (but common), even how the adjustment will be made. With laser-trimmed circuits, the designer can't defer these important considerations but instead must define the exact tolerances to be absorbed by trimming and must plan, in detail, the circuit-trimming strategy. Thus, the designer must consider basic questions, with consequent benefits for designer and product alike.

Laser-trimming is also making possible **new circuits** that were previously unattainable. For example, monolithic 10- and 12-bit A/D and D/A converters are now available at a fraction of the cost of circuits formerly made of high-precision discrete parts. Sixteen-bit monolithic devices will be available within the next decade, and a half-bit error with 16 bits is an error of only eight parts per million! Just as impressive is the **functional complexity** of the new analog IC's. The next generation of monolithic devices will be fully-specified, programmable signal processing *systems*. They will be as easy to use as digital parts are today.

As a final benefit, laser-trimming makes it much harder for potential competitors to duplicate our circuits. Duplication requires a large investment in specialized equipment and expertise and a lot of software to implement the trim algorithm which can't be deduced from observing device performance.

LASER-TRIMMING SYSTEMS

An example of a laser-trimming system is the ESI44 trimmer made by Electro-Scientific Industries. Tektronix owns two of these systems and has ordered a third.

The system uses an infrared laser and an extremely precise servo-mechanical beam-positioner. Two massive linear motors position the beam with an accuracy of 2.5 micrometers over a 3-inch square on the wafer with less than one millisecond settling time. Probes attached to the wafer being trimmed connect to a data-acquisition subsystem which feeds the system controller, a PDP-11-04. Other equipment includes a step-and-repeat table for wafer positioning, a hard-disk unit for data storage, and a closed-circuit color TV system for observing the workpiece.

The complete system, costing about $250,000, performs *all* IC production tests. Thus, we need only one handling station between wafer fabrication and packaging. The system marks defective chips and can even grade the chips by using the laser to write identifying characteristics directly on a corner of each silicon chip.

APPLICATIONS

For seven years we have trimmed thick-film and thin-film resistors on ceramic substrates. Now we are preparing to trim monolithic silicon circuits.

High-power-dissipation circuits may be trimmed after attaching the chip to the metal or ceramic package. However, we are more interested in trimming circuits while they are still in wafer form. The trimming cost is much lower than trimming packaged circuits, because we can trim hundreds of circuits in one pass.

The laser can also alter circuit configurations by cutting interconnects or even by operating directly on bipolar and FET transistors. For example the base-emitter voltage may be adjusted as much as 3 millivolts.

In the immediate future, laser trimming will be used mostly for thin-film resistors. We are looking closely at two films. The first is nickel chromium with which we have worked for many years and which is very stable. It has a sheet resistance in the range 10 to 200 ohms per square.

A second film, silicon chromium, has been used by other companies for several years, but we need more experience with it before we use it in production circuits. It has a sheet resistance range of 500 - 2000 ohms per square, making it more suitable for low-power, high-precision circuits. Ultimately, circuits may use both films simultaneously thus reducing the chip area required.

These films are *very* thin. A typical layer is only 100 angstroms thick, *one-fiftieth* of yellow light's wave length. Such a film intercepts very little beam energy. We have a lot to learn about these very thin films.

TRIMMING TECHNIQUES

There are two basic approaches to trimming circuits. The traditional approach is the simplest: measure the value of each resistor and trim it to an exact value. This method doesn't assure accuracy for active circuits because there are many other sources of error.

Philosophically, what is required is to achieve a certain *function*. A more sophisticated method treats a circuit as a black box: apply a stimulus to the input, and measure the output. Under software control, the ESI44 then follows a prescribed trim algorithm. This "functional" trimming produces more precise and stable circuits; in the main, resistors are trimmed to equal each other or ratio exactly, rather than to an absolute value.

Two methods are currently used to effect the trim. In the first, dummy links are built into the resistor, usually in binary sequence. The laser beam slices across selected links, severing them completely. Since the material so treated is no longer in the conduction path, the resulting resistor value is extremely stable.

The second approach is to cut into the resistor to continuously alter its value under the close control of the measurement system. This allows

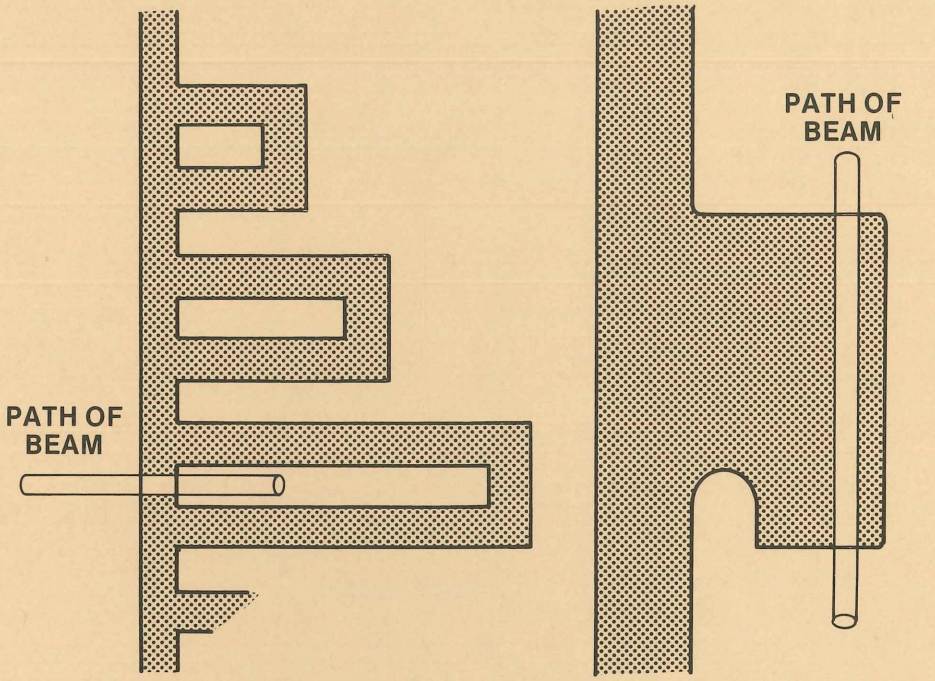

Figure 2. Thin-film resistors can be trimmed in several ways. Here are two popular methods.

fine tuning (to as close as 0.01% of value). However, with the conduction path now including altered material, laser operating conditions must be much more carefully controlled to avoid large differential temperature coefficients.

THE FUTURE

We expect many new Tek analog integrated circuits will be designed for laser trimming. This means we will produce several hundred thousand die each year. To reach that goal, we are pioneering in four areas.

First, because we've decided to use beam-tape packaging techniques, we must learn how to trim through thick passivation layers. Other companies have reported problems, but we think we have a solution. Second, we hope ultimately to combine nickel chromium and silicon chromium on the same chip. So far as I am aware, no one else is using or, even developing, such a dual-film process. Third, we are combining very exotic microwave monolithic processes (involving state-of-the-art techniques) with laser wafer trimming. Finally, we are seeking reliable ways to trim high-power-dissipation circuits such as crt deflection amplifiers. Almost all other manufacturers trim circuits dissipating less than 200 milliwatts; we are considering 5 watt devices. These may not be trimmable in wafer form, but the advantages of trimming will doubtless lead us to consider the alternative of trimming packaged parts.

I believe in laser wafer trimming. I'm convinced that it will bring us very tangible benefits in the years ahead and will be as indispensable as wave-solder machines and Tek-blue paint. I envisage the day when even the most advanced analog-based instruments will be assembled completely from precalibrated parts and with *no* post-assembly adjustment, just as calculators are today with similar cost and reliability advantages.

Someday, I hope, if you want to show your grandchildren that old enemy, the Tweak, you'll have to take them to OMSI, or maybe to the Smithsonian. There, alongside the coherer, the Audion tube, and the tunnel diode, you'll find him where he belongs, locked-in forever, under glass.□

ELECTROLUMINESCENT DISPLAYS

Chris King, Materials Research, ext. 5377.

Electroluminescent (EL) displays are solid-state, flat-paneled devices which have potential applications for Tektronix in alphanumeric and graphic storage displays. EL technology seems well-adapted to medium-sized displays (displays larger than possible with LED's, but smaller than a large crt). For storage display, EL technology may provide an improvement over our current DVST technology but that remains to be verified in the laboratory.

STRUCTURE

Figure 1 shows the structure of an EL display. An active, light-emitting layer of manganese-doped zincsulfide is sandwiched between the display's two insulating layers. The two insulating thin films are deposited on a glass substrate coated with a transparent conductor. The rear aluminum electrode is the second plate forming a capacitor-like structure. The EL display lights when sufficient voltage is applied to the two electrodes.

CHARACTERISTICS

Figure 2 shows the brightness-voltage characteristic of an EL display. The display gives off light when an electric field of approximately 20 million

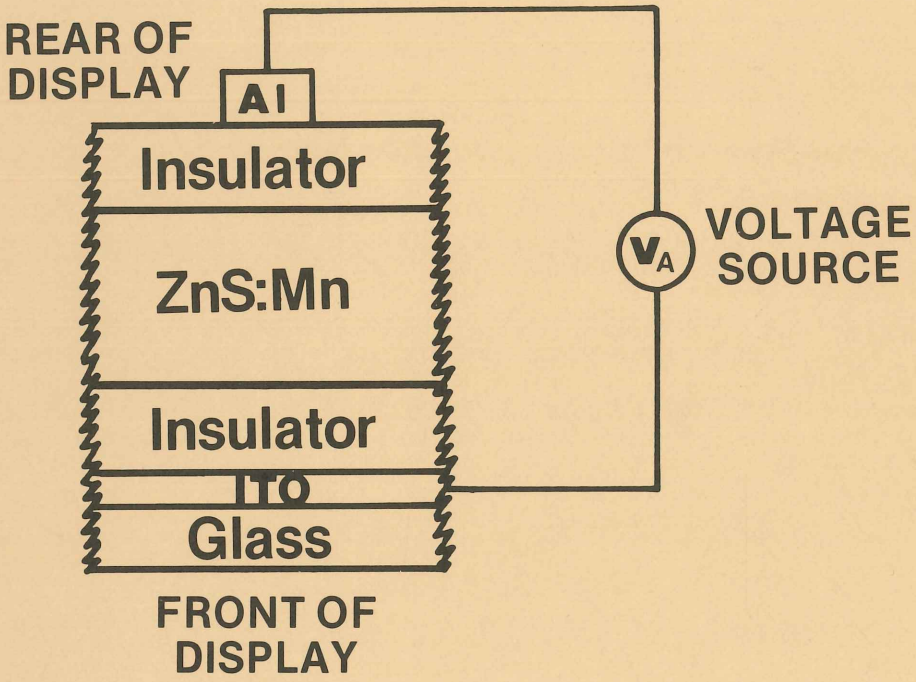

Figure 1. In this cross-sectional top view of an EL display, an active light-emitting layer of manganese-doped zincsulfide is sandwiched between two insulating layers. The EL display lights when sufficient voltage is applied to the two electrodes.

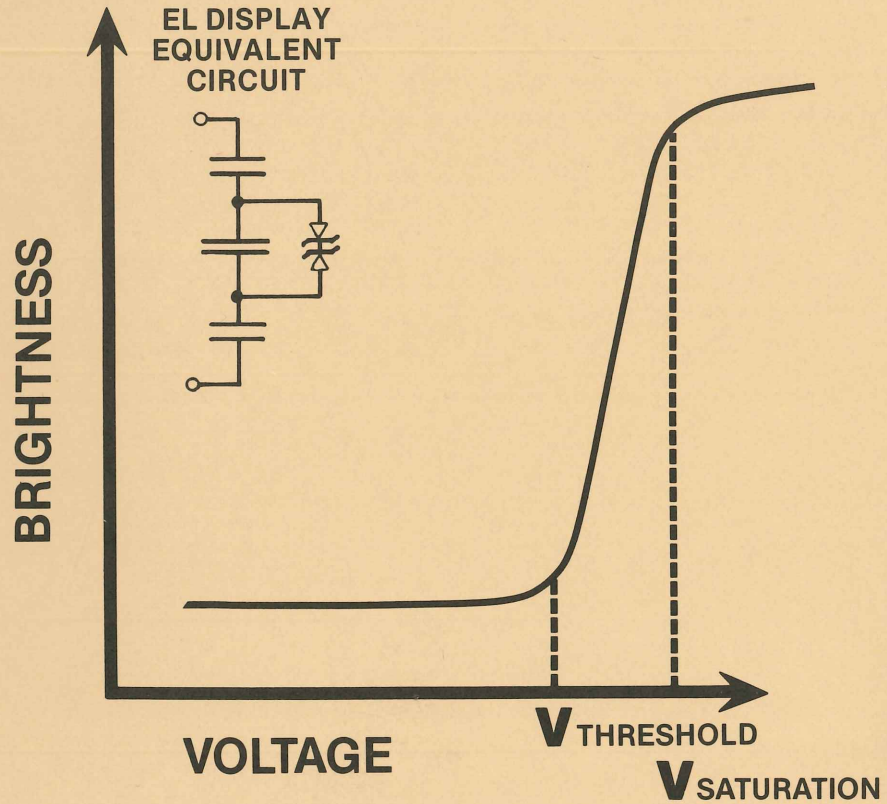

Figure 2. This graph of EL display brightness-voltage characteristics shows that, at the threshold voltage, the thin-film insulators emit light. Increased voltage greatly increases brightness until the saturation voltage is reached. In the upper left corner is an equivalent circuit schematic of the EL display.

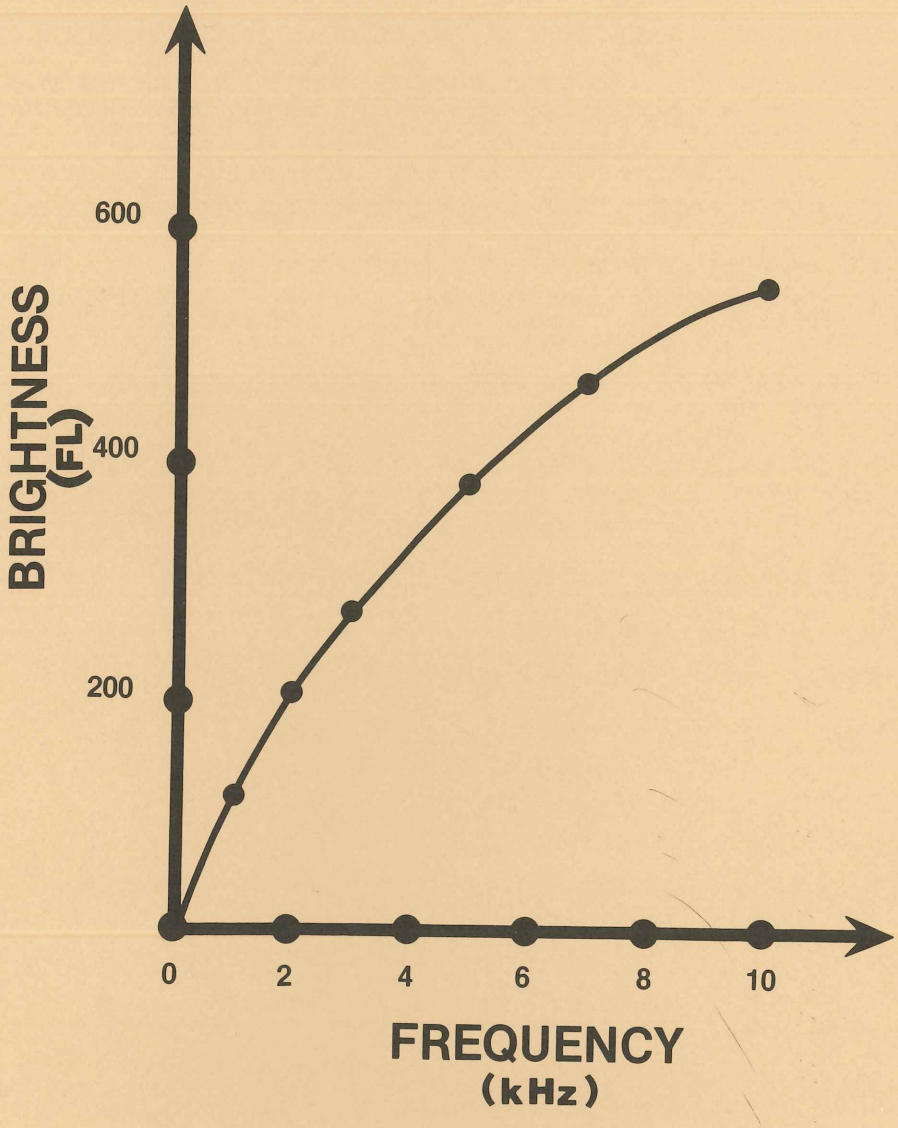

Figure 3. In EL displays, brightness increases with drive voltage frequency.

volt/centimeters breaks down the zincsulfide layer. Excess electrons resulting from the zincsulfide breakdown excite the maganese atoms which then emit a yellow light.

EL displays have high contrast ratios because brightness increases sharply above the threshold voltage as shown in figure 2.

Figure 3 shows that brightness increases with the drive voltage frequency. Although blinding brightness can be achieved at high frequencies, large capacitive-displacement currents seem to dictate economical EL operation at less than 1kHz where the brightness is in the in the 10- to 100-foot Lamberts range.

It is possible to have a hysteretic brightness-voltage characteristic in some light-emitting films (figure 4). Such a B-V curve gives the films both a memory- and light-writing capability. Memory operation is provided by driving the EL display with a sustaining voltage that falls inside the bottom leg of the hysteresis triangle. As a memory unit, a display element is "written" by applying a high voltage pulse to switch the display to the upper leg of the triangle. Temporarily reducing the voltage erases the display. Also, one can locally switch any point on the display with an ultraviolet light pulse from a light pen.

EL DISPLAY TRADEOFFS

As with most technologies, EL displays have advantages and disadvantages. The advantages are the capability to produce a solid-state flat-panel display with very high steady-state brightness, excellent contrast, high resolution, potentially long life, ease of configuration, and light-writing and memory capabilities. There are some disadvantages. EL displays require complex driver circuits, excellent internal insulators, high voltages, and they require capacitive displacement current as well as current that causes the light emission. Also, line-at-a-time addressing reduces average brightness, and there is a fan-out connector problem in driving high-resolution matrix displays (the number of display lines is limited by the number of connections that can be attached to the panel).

EL DEVELOPMENT IN TEK LABS

Figure 5 diagrams the evaporation system that deposits the zincsulfide films. A co-evaporation technique lets us vary the zincsulfide manganese doping by controlling the relative rates of depositing the two materials.

Last year we examined the factors that govern the brightness and hysteresis characteristics of EL films. We found that manganese doping-concentration is the main factor that controls brightness. Figure 6 shows the relationship between brightness and manganese concentration. We are still studying the hysteresis effect. Apparently hysteresis is governed not only by the bulk manganese concentration, but also by the zincsulfide insulator crystal structure.

If we can improve our displays' reliability by developing better insulators, EL displays will be a most exciting solution for the long sought-after solid-state flat-panel display.

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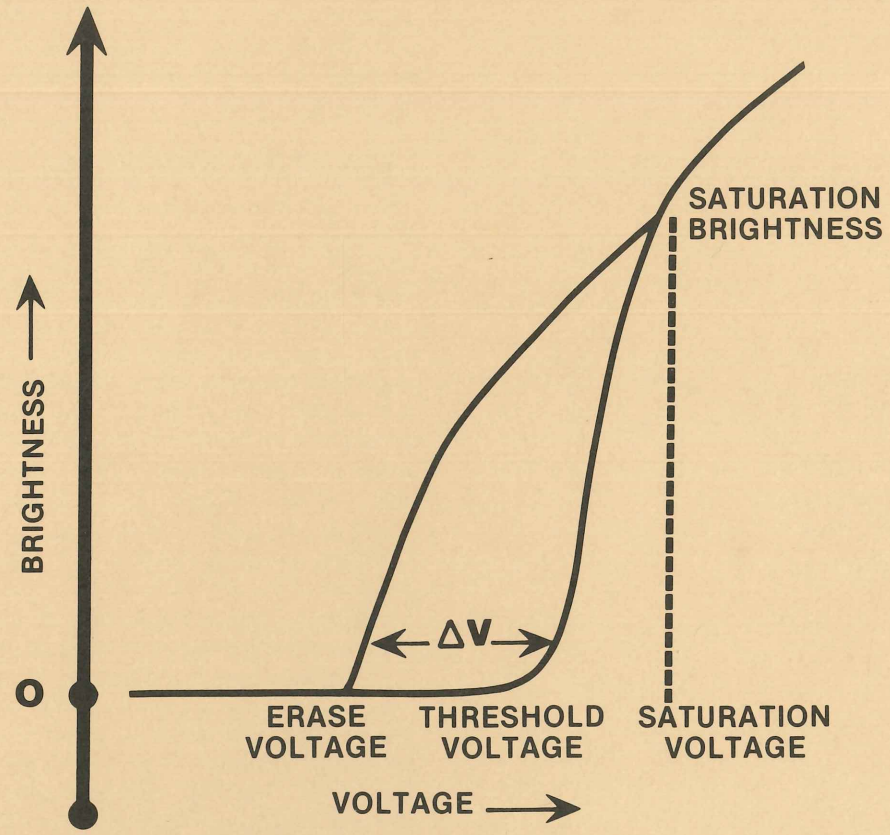


Figure 4. Some light-emitting films have a hysteretic brightness-voltage characteristic which gives the display memory- and light-writing capabilities.

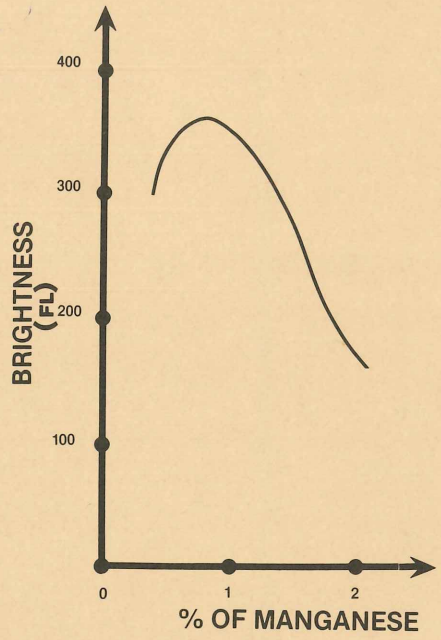


Figure 6. The effect of manganese doping concentration on EL brightness.□

ZnS:Mn Deposition System

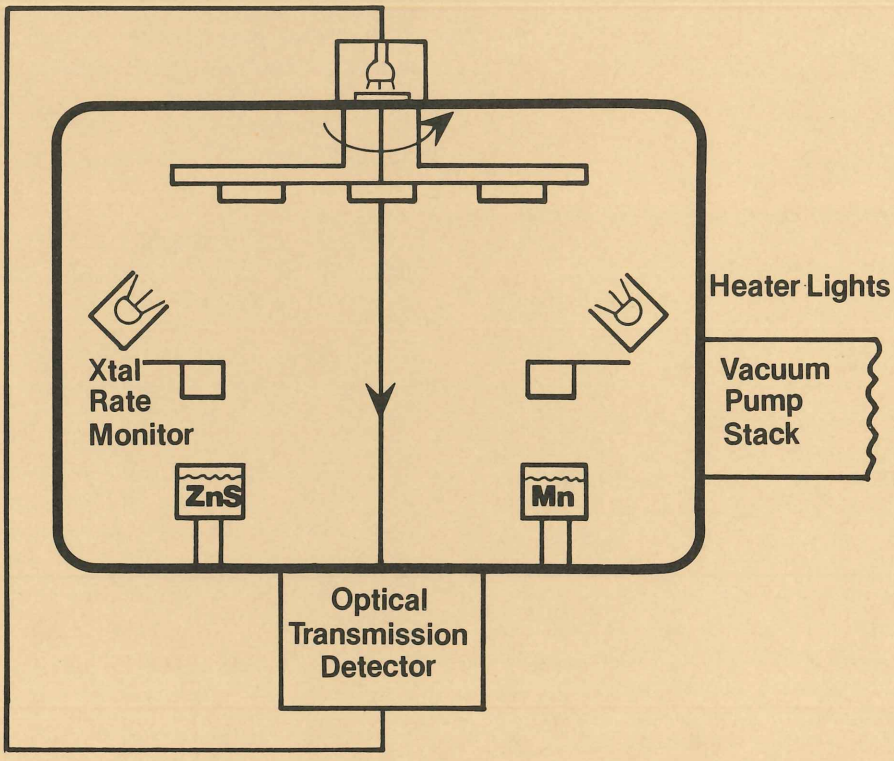
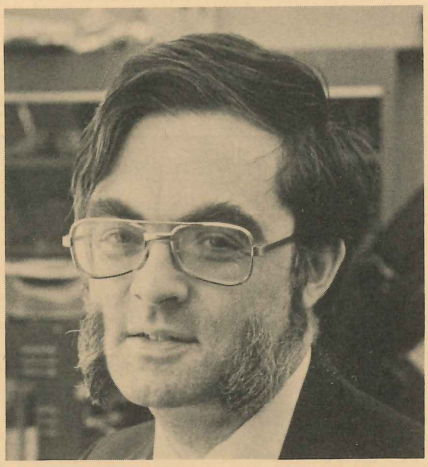


Figure 5. The evaporation system that deposits the light-emitting films uses a co-evaporation technique to vary the zincsulfide's doping.



Ron Robinder (Display Device Engineering) discussed color technology at Tektronix.

Tadanori Yamaguchi (Applied Research) discussed a new MOS technology.

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