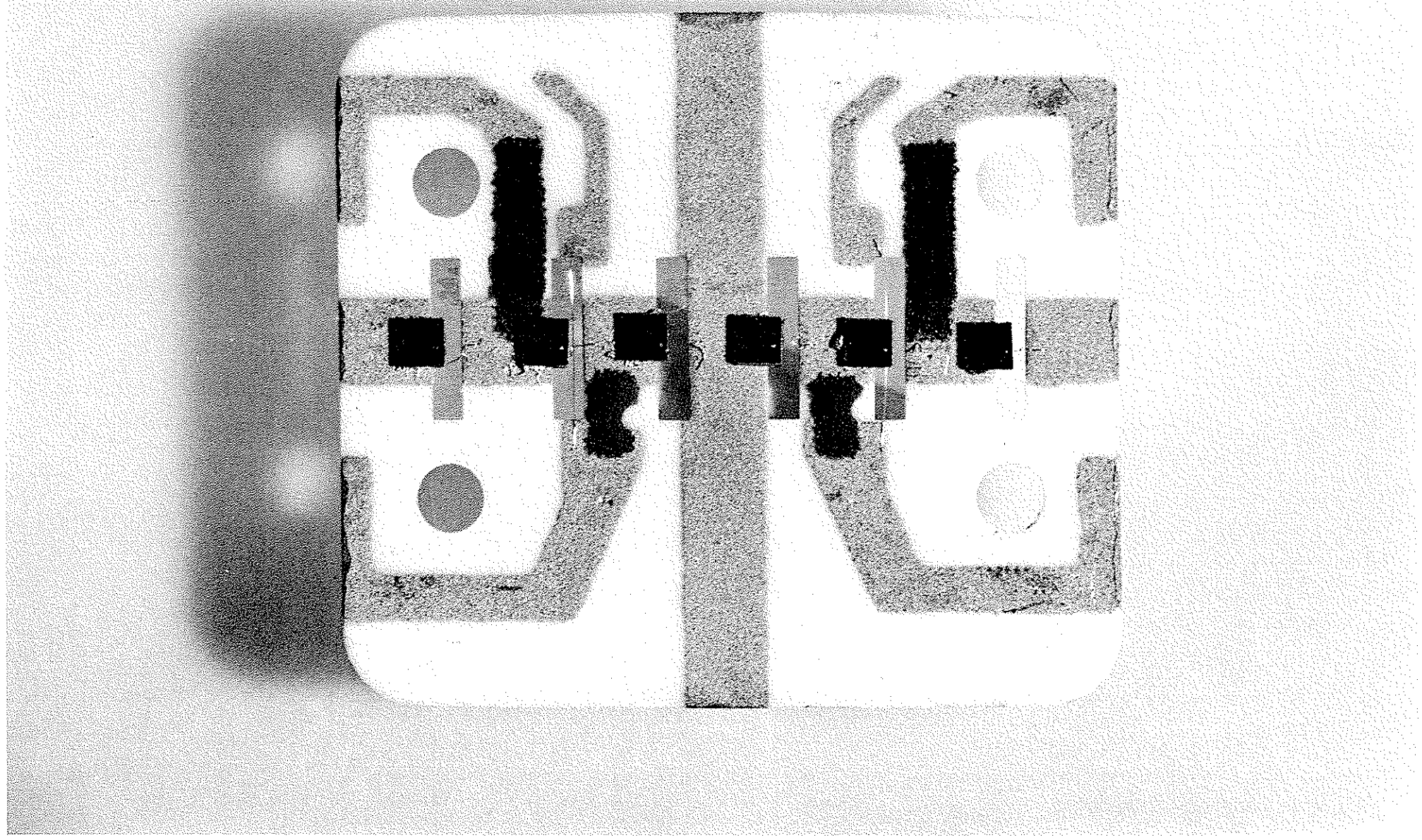
A New Approach to Fast Gate Design



A unique sampling gate eliminates risetime dependency upon strobe width. This new development offers the highest speed sampling system to date and offers promise for even faster gates.

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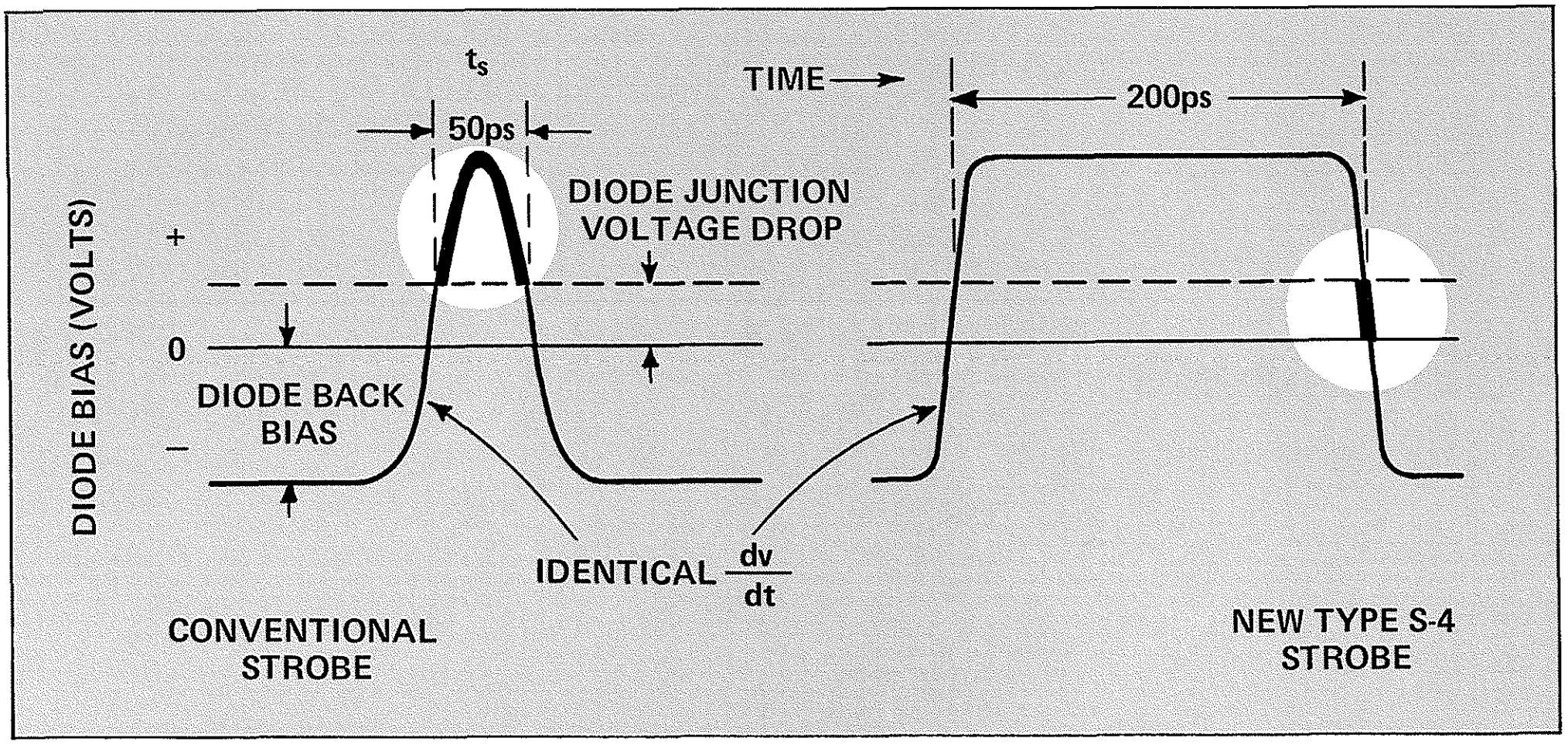
Fig 1 shows a section of delay line with switches inserted at point A and point C. A nonloading voltmeter placed at point B, measures the average of the voltage between the switches when the switch section is opened. When a fast step is applied to the line and the switches then opened, the following observations may be made.

If the step propagating down the line is at point A when the switch opens, 0 volts are observed. If the switches are reclosed and a second observation made at a later time, when the wavefront has reached point C, the voltage is 1. When the step is just entering the switch at point A, we observe 0; if it is just leaving the switch at point C, we observe 1. Thus, we may state that the system 0-100% risetime is determined by the length of the switch section or C-A. Since we know the line has capacitance and voltage, we have effectively "trapped" a quantity of charge (Q=CE). If we now apply this concept to the model shown in fig 2, we can note some very important observations.

The model in fig 2 illustrates a simplified form of the new sampling gate used in the Tektronix Type S-4 Sampling Head. Diodes replace the switches and instead of opening the switches simultaneously, we turn the diodes off one after another. Although it is a balanced system, only one half of the system will be described.

The leading edge of the strobe pulse turns the diodes on and the signal propagates into the conducting diodes and transmission line. The diodes remain on for the duration of the strobe pulse, being turned off by the trailing edge of the wave shape. The strobe pulse is designed to be longer than the transit time between the diodes.

Gate action begins when the strobe trailing edge turns D2 off. At the same time, suppose a signal front enters through conducting diode D1. When the front reaches D2, it is off since the strobe arrived there prior to the front. The signal front reflects and reaches D1 which is now off since the strobe trailing edge has preceded the front. Thus, the signal front has been effectively trapped in the transmission line between the two diodes. Note, however, that the gate characteristics are determined by the strobe trailing edge (only one transition).



The conventional sampling gate must take the diode from a fully-off condition, turn it fully-on, and return it to a fully-off condition. The time between the two fully-off conditions, t_S, is the strobe width and determines the risetime of the system. In the Type S-4 gate, the diodes are fully-on as gate action begins, and only one transition is needed. Risetime is determined by the length of the transmission line as pointed out in the text. The conventional strobe for a fast sampling gate is very narrow since the strobe width determines the system risetime. The Type S-4 uses a wide strobe and minimizes the problems inherent in narrow strobe generators.

In this system, the 0-100% risetime is determined by twice the propagation time between D1 and D2, since both the front and the strobe must traverse the distance.

The important points to note are the following: (1) Only one transition is required for the gate action (gate action occurs from a fully-on diode condition to a fully-off condition). Using one transition offers substantial noise reduction possibilities. (2) The risetime of the system is not dependent upon the strobe width. (3) The propagation time between diodes in this system (8 ps) is much less than the strobe period of approximately 200 ps. (4) Because the diodes currently used may be turned off in 5-10 ps, they do not present a significant risetime limitation.

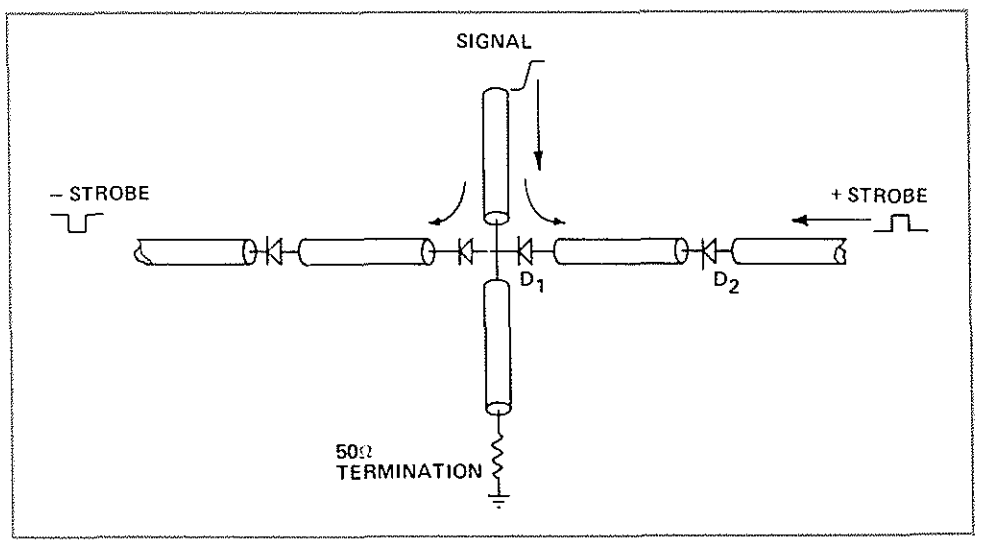


Fig 2. Simplified model of sampling gate for Type S-4.

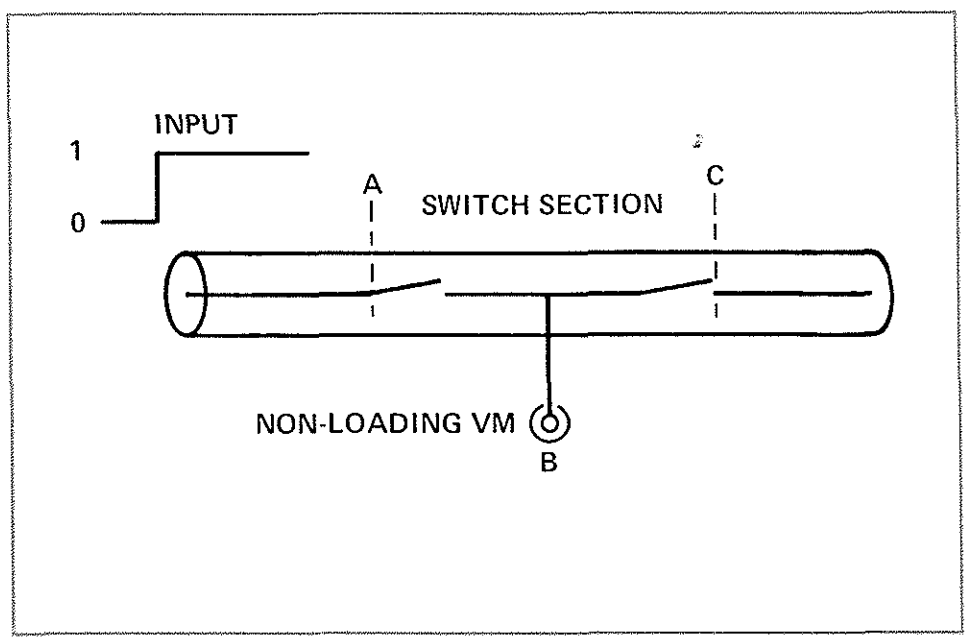


Fig 1. Delay-line section.

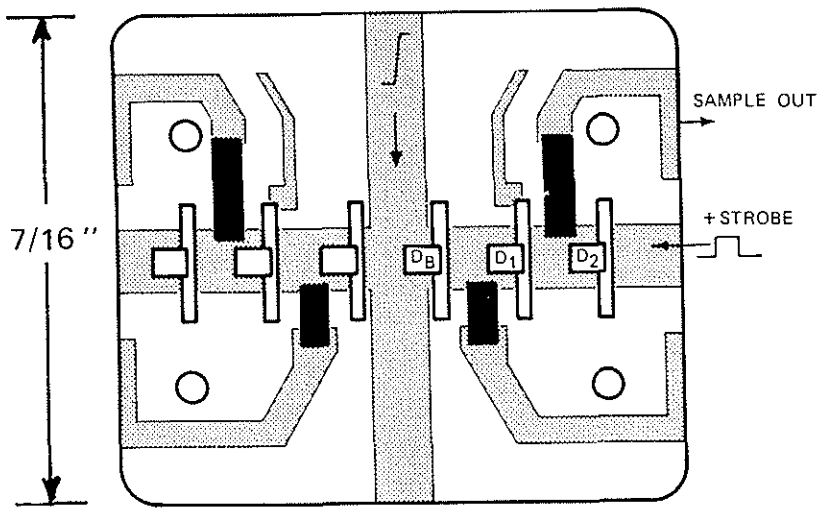


Fig 3. 25-ps hybrid gate. 6 Tektronix-manufactured diode chips are placed on a ceramic substrate. The substrate is formed with slots (0.020) which remove high dielectric constant material near the diodes to reduce shunt capacitance. The diode chips are set in place, extending over the slots, to minimize lead inductance. D_B is in the circuit to correct for signals capacitively coupled through the gate diodes when they are not conducting (blowby).