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PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

MI 5010/MX 5010 PROGRAMMABLE MULTIFUNCTION INTERFACE With Interface Extender

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-3712-00
Product Group 76

Serial Number _____

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equiment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified inthe parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

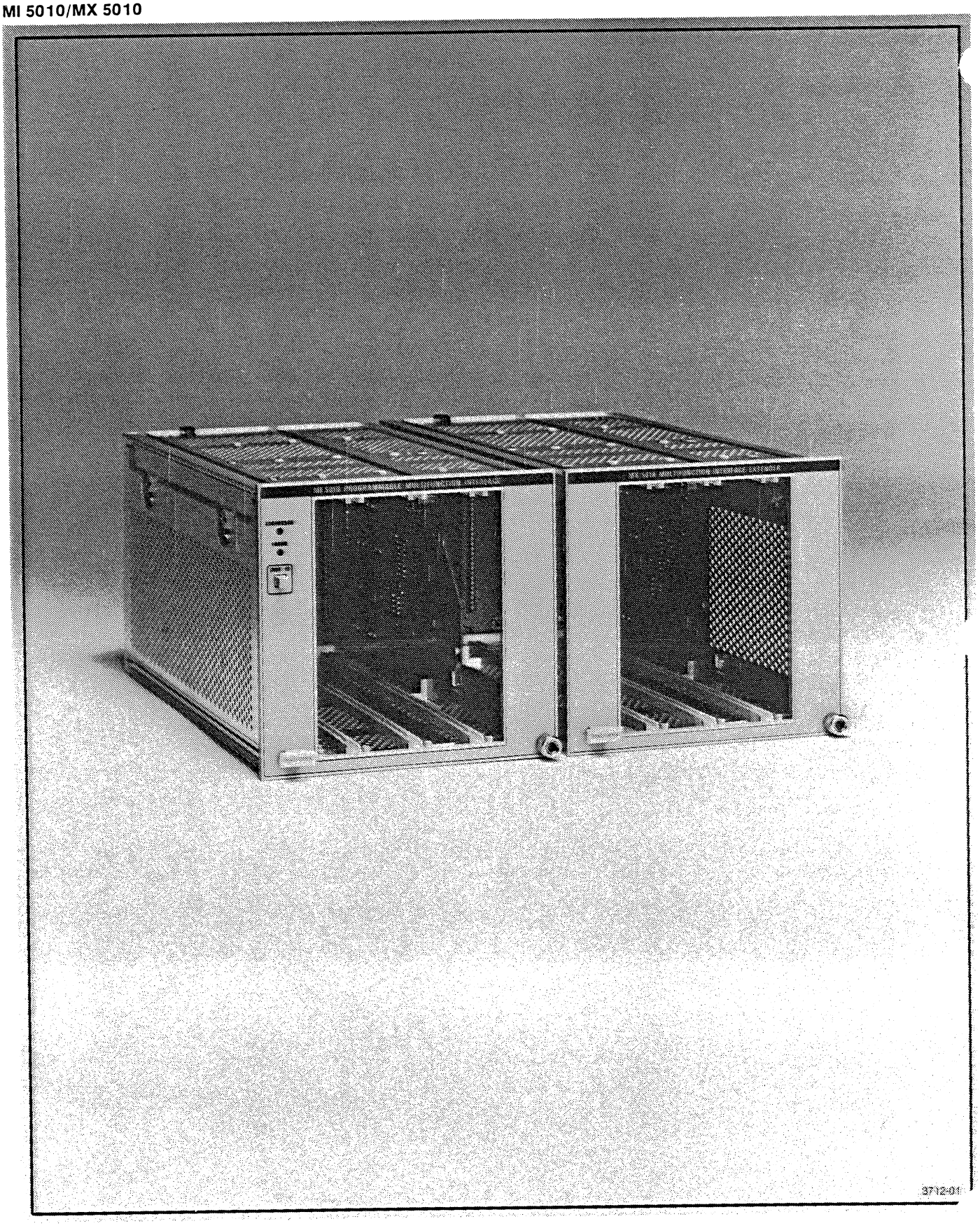
Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panel, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



MI 5010 Programmable Multifunction Interface
with
MX 5010 Multifunction Interface Extender

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SPECIFICATION

INTRODUCTION

General Information

This manual provides instructions and service information for the TEKTRONIX MI 5010 Programmable Multifunction Interface unit and the TEKTRONIX MX 5010 Multifunction Interface Extender unit. Instructions and service information for the function (input/output) cards designed to be used in the MI 5010/MX 5010 interface system are provided in separate instruction manuals.

NOTE

All references to the SA 501 in this manual now apply to the 067-1090-00 Signal Analyzer.

MI 5010 Description

The MI 5010 is a two-wide plug-in unit designed to operate in a TM 5000-Series power module. The MI 5010 accepts a maximum of three function cards, selected by the user. With the MX 5010 installed, six function cards can be selected. Typical function cards include the following Tektronix products:

- 50M30 Programmable Digital Input/Output Card
- 50M40 Programmable Relay Scanner Card
- 50M70 Programmable Development Card

A microprocessor based GPIB control board in the MI 5010 allows communciation between a GPIB controller and the input/output functions on any selected card. Function card selection and programming is via a digital interface specified and described in IEEE Standard 488-1978, "Standard Digital Interface for Programmable Instrumentation". With the proper function cards installed, the user can quickly develop a versatile interface between a controller and his external system, using high-level language programming.

NOTE

In this manual, the IEEE 488 digital interface is referred to as the General Purpose Interface Bus (GPIB).

All function cards have a 25-pin dual (50-pin total) edge connector available at the front panel of the MI 5010/MX 5010 interface system. These connectors are provided for the input/output interface wiring or cabling to external sensor points in the users specific measurement, test, or processing equipment. Each card has its own unique resident firmware and operational command list, separate from the MI 5010.

NOTE

A front panel interface cable assembly is provided as a standard accessory for each function card.

A built-in 24 hour "time-of-day" clock is also provided. This clock can be used with 50 Hz, 60 Hz, or 400 Hz ac power line frequency. The clock is set and read with data in the form of hours, minutes, and seconds with a resolution of one second.

A power supply board in the MI 5010 provides power for the microprocessor board and all three function cards installed in the MI 5010. A line-sync time base signal (one-tenth power line frequency) is also available from the power supply board and backplane connectors.

MX 5010 Description

The MX 5010 Multifunction Interface Extender unit is a two-wide plug-in that must be electrically attached to the right-hand side of the MI 5010. The MX 5010 also accepts a total of three function cards. When the two units are assembled, a maximum of six function cards can be programmed via the microprocessor in the MI 5010. The MX 5010 contains a power supply board and a backplane (main interconnect board) electrically identical to the backplane and power supply board in the MI 5010. The MX 5010 does not contain a microprocessor board; digital control signals are routed from the MI 5010 to the MX 5010 via a flat-ribbon cable at the backplane connectors.

Standard Accessories

1 Instruction Manual
1 Reference Guide

Optional Accessories

The following accessories for the MI 5010/MX 5010 interface system are available upon request. Contact your

nearest Tektronix Field Office or Service Facility for details and ordering information.

Blank Plug-in Card, Tektronix Part No. 020-0836-00
Rigid Extender Card, Test Fixture 067-1066-00.

NOTE

Refer to the tabbed Accessories page in the rear of this manual for more information.

IEEE 488 (GPIB) FUNCTION CAPABILITY

The IEEE Standard 488-1978 identifies the interface function repertoire of a programmable instrument on the digital interface in terms of interface function subsets. The subsets are defined in the standard. The subsets that apply to the MI 5010/MX 5010 interface system are listed in Table 1-1.

NOTE

Refer to IEEE Standard 488-1978 for more detailed information. The standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017.

Table 1-1
IEEE 488 INTERFACE FUNCTION SUBSETS

Function	Subset	Capability
Source Handshake	SH1	Complete.
Acceptor Handshake	AH1	Complete.
Basic Talker	T6	Responds to Serial Poll. Untalked if My Listen Address (MLA) is received.
Basic Listener	L4	Unlistened if My Talk Address (MTA) is received.
Service Request	SR1	Complete.
Remote-Local	RL0	No "local" capability (remote only).
Parallel Poll	PP0	Does not respond to Parallel Poll.
Device Clear	DC1	Complete.
Device Trigger	DT1	Complete.
Controller	C0	No Controller function.

NOTE

The GPIB control bus driver is a tri-state device. The data bus driver operates in either a normal open-collector mode, or in a tri-state mode when parallel polled. The MI 5010 does not respond to a parallel poll.

ELECTRICAL CHARACTERISTICS

Performance Conditions

The limits stated in the Performance Requirements column of Table 1-2 are valid only if the MI 5010/MX 5010 units are operating in an ambient temperature between 0°C and +50°C, unless otherwise stated.

Information given in the Supplemental Information column of the following tables is provided for user information only, and should not be interpreted as Performance Requirements.

Both units must be in an environment whose limits are described under Environmental Characteristics (Table 1-3).

Allow at least 5 minutes warm-up time for operation to specified accuracy, 60 minutes after storage in high humidity environment.

NOTE

Some function cards may have Specifications different than that listed in this section of the manual. When the complete system is installed, refer to the individual function card specifications.

Table 1-2
ELECTRICAL CHARACTERISTICS
MI 5010 or MX 5010 POWER SUPPLY

Characteristics	Performance Requirements	Supplemental Information
Output Voltage	+5 V, ±2% from no load to 5 A.	
Current Limit		Between 5.0 A and 6.3 A
Overvoltage Crowbar		Supply shuts down when output voltage exceeds 6 V, ±3%.
Undervoltage Restart		RESET line goes to a TTL low for a minimum of 100 μsec if output voltage drops below 4.8 V for 1 μsec or longer.
Line Sync Time Base (LSTB)		TTL square wave at one-tenth line frequency.

PHYSICAL CHARACTERISTICS

Table 1-3
ENVIRONMENTAL[a]
MI 5010 or MX 5010

Characteristics	Description	
Temperature		Meets MIL-T-28800B, class 5.
Operating	0°C to +50°C	
Non-operating	−55°C to +75°C	
Humidity	95% RH, 0°C to 30°C 75% RH, to 40°C 45% RH, to 50°C	Exceeds MIL-T-28800B, class 5.
Altitude		Exceeds MIL-T-28800B, class 5.
Operating	4.6 km (15,000 ft)	
Non-operating	15 km (50,000 ft)	
Vibration	0.38 mm (0.015") peak-to-peak, 5 Hz to 55 Hz, 75 minutes.	Meets MIL-T-28800B, class 5, when installed in qualified power modules.[b]
Shock	30 g's (1/2 sine) 11 ms duration, 3 shocks in each direction[c] along 3 major axes, 18 total shocks.	Meets MIL-T-28800B, class 5, when installed in qualified power modules.[b]
Bench Handling[d]	12 drops from 45°, 4" or equilibrium, whichever occurs first	Meets MIL-T-28800B, class 5.
Transportation[d]	Qualified under National Safe Transit Association Preshipment Test Procedures 1A-B-1 and 1A-B-2.	
EMC[e]	Within limits of F.C.C. Regulations, Part 15, Subpart J, Class A; VDE 0871; and MIL-461A tests RE01, RE02, CE01, CE03, RS01, RS03, CS01, CS02, and CS06. User cable not attached to function cards.	
Electrical Discharge	20 kV maximum charge applied to instrument case.	

[a] With power module.
[b] Refer to TM 5000 power module specifications.
[c] Requires retainer clip in plug-in exit direction.
[d] Without power module.
[e] System performance subject to exceptions of power module or other individual plug-ins.

Table 1-4
MECHANICAL CHARACTERISTICS

Characteristics	Description
Nominal Overall Dimensions (MI 5010 or MX 5010)	
Height	4.91 inches (126 mm).
Width	5.295 inches (134.4 mm).
Length	10.855 inches (255.7 mm).
Net Weight	
MI 5010	2.75 lbs. (1.25 kg).
MX 5010	2.250 lbs. (1.02 kg).
Finish (Front Panel)	Plastic/aluminum laminate.

SYSTEM INSTALLATION

PREPARATION FOR USE

Operating Environment

The MI 5010/MX 5010 system should be operated in a clean, controlled environment that does not exceed the environmental limitations listed in Section 1, Table 1-3.

NOTE

Before installing any unit, refer to the Operators Safety Summary in the front of this manual and to the Change Information section at the rear of this and other associated instruction manuals. Also refer to the power module instruction manual for line voltage requirements and power module operation.

Front Panel Controls

The INST ID pushbutton on the MI 5010 (see Fig. 2-1) is the only front panel control for the MI 5010. The MX 5010 has no front panel controls. This pushbutton is under program control via the USER ON and USER OFF commands sent over the IEEE 488 (GPIB) digital interface. At power-up, the INST ID function defaults to the USER OFF condition. Refer to the Programming Information section of this manual for more information.

IEEE 488 Address and Message Terminator Switches

A bank of six switches is located in a cut-out in the upper right-hand corner of the rear panel on the MI 5010. These switches are used before installation to set the IEEE 488 talk-listen address and message terminator for the operating system.

The lower five swiches are set to select the primary address; secondary addrssing is not implemented in the operating system. Setting a single switch to the right (up) sets the binary weight for that bit. Adding the binary weights establishes the decimal address. For example, Fig. 2-2 shows the switches set to decimal address 23 and message terminator to the EOI position.

NOTE

Do not set the MI 5010 address to the same address as the controller being used.

Valid addresses are from 1 to 30. Address 0 is reserved for maintenance and servicing the instrument. Address 31 is the IEEE 488 UNT (Untalk) and UNL (Unlisten) interface address message; setting address 31 effectively prevents the MI 5010 from communicating over the IEEE 488 digital interface.

NOTE

When shipped, the MI 5010 address is set to decimal 23 and message terminator set to EOI.

The top switch sets the message terminator so that the operating system can respond to one of two possible message terminators controllers may send on the IEEE 488 digital interface, EOI only or LF/EOI. Message terminators are as follows.

Input message terminator:

EOI position —Only the EOI line on IEEE 488 digital interface asserted with last data byte as the message terminator.

LF/EOI position —<CR> <LF and EOI> are added to the end of the message being sent (EOI is asserted with the <LF> character). If the <LF> character without EOI, EOI with <LF>, or EOI asserted with any data byte is sent anywhere in the message string, the MI 5010 recognizes it as a message terminator.

Output message terminator:

EOI position —<;> with EOI asserted.

LF/EOI position —<;><CR> then <LF> with EOI asserted.

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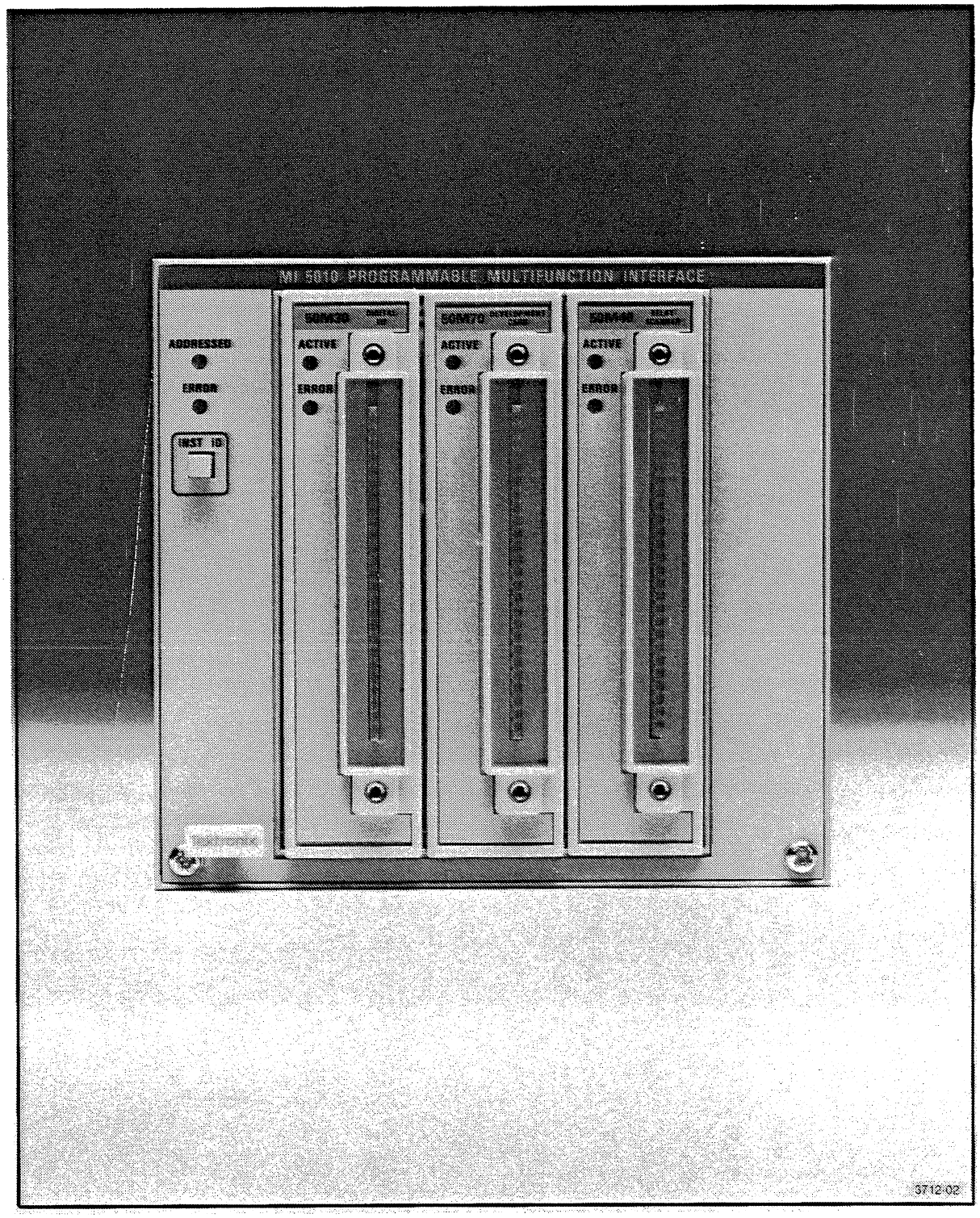

Fig. 2-1. Front panel controls and indicators; all under program control (see text).

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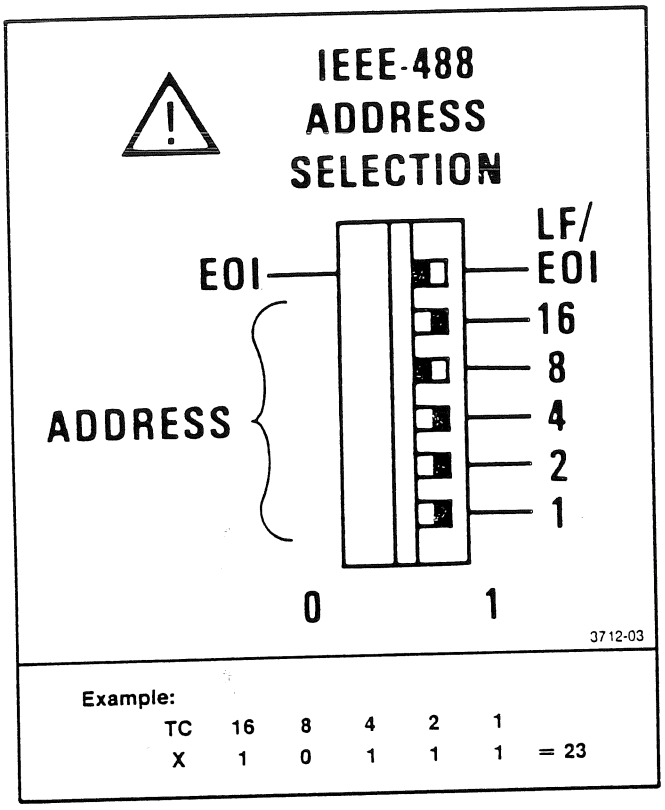

Fig. 2-2. IEEE 488 bus address and message terminator switches.

System Installation and Removal

CAUTION

To prevent damage to the MI 5010/MX 5010 operating system, turn off the power module before installing or removing any unit or function card. Do not use excessive force when installing or removing the plug-in units or any function card.

As a single unit, the MI 5010 can be installed in the power module with or without function cards installed. See Fig. 2-3. The MX 5010 should not be installed without first being electrically attached to the MI 5010 via the Bus Extension Assembly shipped with the MX 5010 unit. Figure 2-4 shows how the two units are connected together. There are no mechanical connections between the two units, other than inserting the MX 5010 pin guides in their respective holes on the MI 5010. The pin guides are also shipped with the MX 5010.

Before installing the MI 5010 or MX 5010 units in the power module, the function cards selected for the user's system must be installed. The MI 5010 provides space for three function cards in slots 1, 2, and 3; left to right, as viewed from the front panel. The MX 5010 provides space for three additional function cards in slots 4, 5, and 6; left to

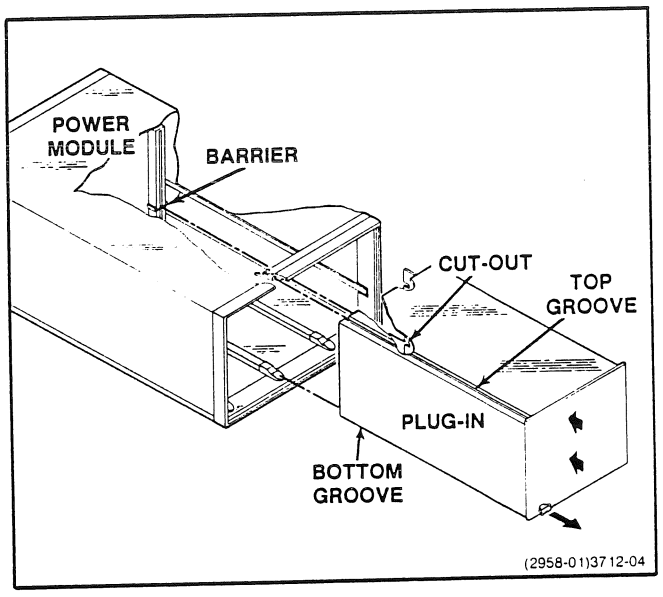

Fig. 2-3. MI 5010 installation and removal.

right. Since the function cards are selected by software by slot number, any card may be installed in any vacant slot. An error message is reported over the IEEE 488 digital interface if a vacant slot is selected by the program software.

WARNING

The front panel interface connections on some function cards can be elevated to hazardous high voltage levels above or below ground potential. To avoid personal injury when these types of cards are installed, the MI 5010/MX 5010 system must not be operated with empty adjacent card slots. If this condition exists, refer the installation of an optional blank plug-in card in the empty adjacent card slots to qualified service personnel. Also refer to the individual function card instruction manual(s).

When installing the function cards, be sure that they are aligned with their respective lock screws on the rear panels of the MI 5010 and MX 5010 and the lock screws used to secure the card in place. See Fig. 2-5.

CAUTION

Do not use excessive force when tightening the lock screws.

Before installing any plug-in unit in the power module, check to see if the plastic barrier on the interconnecting jack of the selected power module compartment matches the cut-out in the circuit board edge connectors at the rear interface.

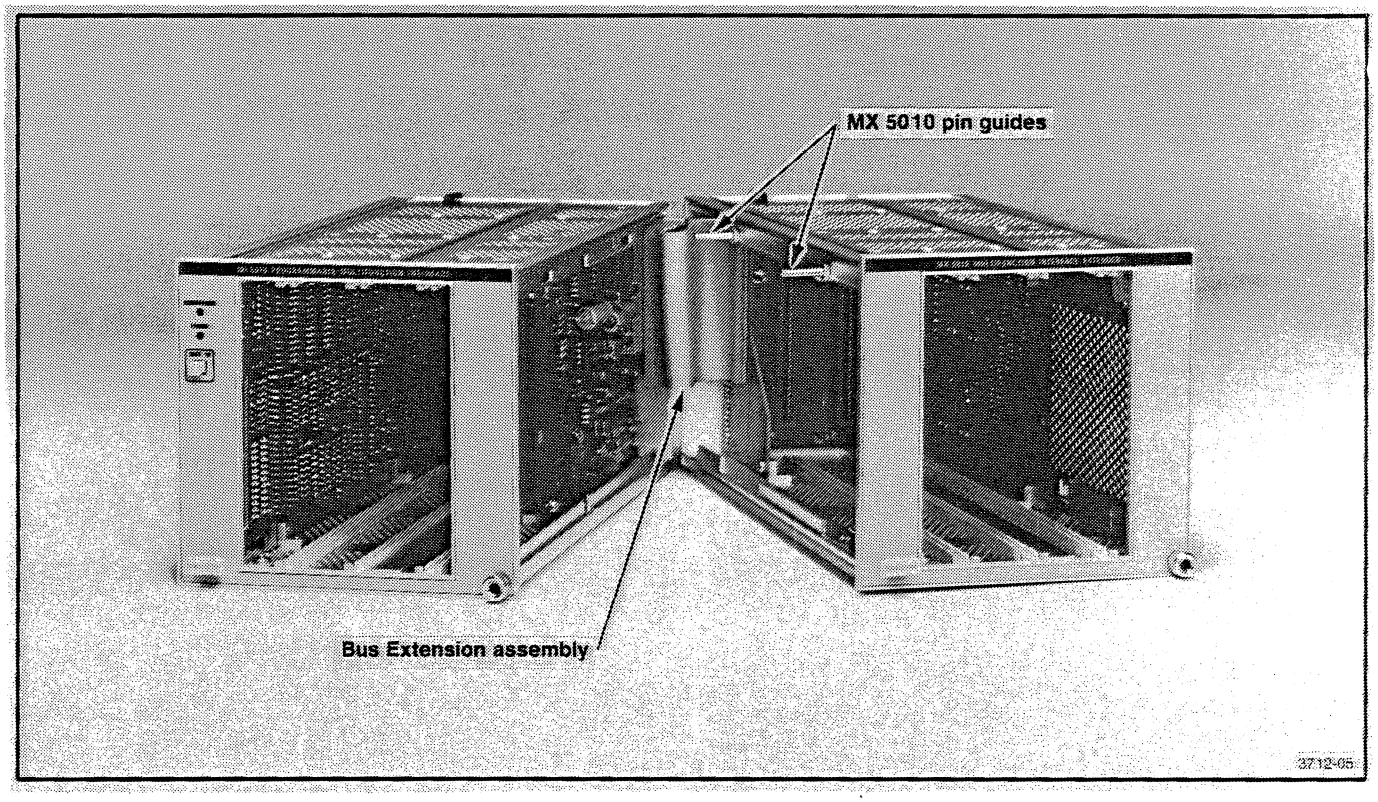

Fig. 2-4. MI 5010/MX 5010 interconnection assembly.

Align the chassis of the plug-in unit with the upper and lower guide rails of the selected compartment. Push inward and press firmly to seat the circuit board edge connectors in the interconnecting jacks.

CAUTION

When installing (or removing) the MX 5010 in (or from) an adjacent power module compartment along with the MI 5010, keep the two units aligned closely so that no strain is placed on the Bus Extension Assembly.

To remove the MI 5010 (if installed alone), turn off the power module and pull on the release latch (front panel, lower left corner) until the interconnecting jacks disengage. Pull straight forward to remove the plug-in from the power module.

NOTE

When the MX 5010 is removed along with the MI 5010, both release latches must be released and both units pulled simultaneously from the power module. Do not place any strain on the Bus Extension Assembly.

Power-Up and Front Panel Indications

CAUTION

Do not install or remove the MI 5010, MX 5010 or function cards with the power module POWER switch on.

Apply power to the MI 5010/MX 5010 system by activating the POWER switch on the TM 5000-Series power module. The system may be powered up with or without function cards installed.

When powered up, the system enters a power-up self-test mode. An ERROR light on the MI 5010 and on each installed function card are illuminated during this test and remain on until the power-up self-test has been completed.

If an internal hardware or firmware fault has been detected in the MI 5010 or on a function card, the associated ERROR light remains illuminated. If no internal fault is detected the ERROR lights will turn off. Communication or settings errors over the IEEE 488 digital interface are reported to the controller. Hardware errors will be reported to the controller

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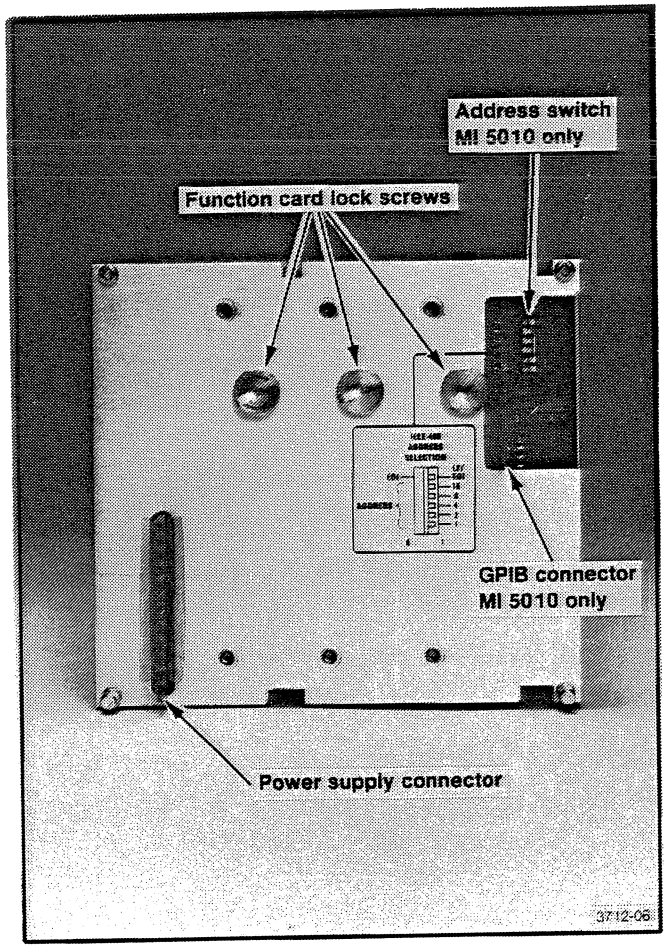

Fig. 2-5. MI 5010 rear panel. MX 5010 does not have the address switch or GPIB connector.

where possible (microprocessor/GPIB board is functional) if encountered after the power-up self-test. Hardware errors discovered during power-up self-test are reported only for the function cards. Such errors on the microprocessor/GPIB board are considered fatal at anytime and will cause the MI 5010 to cease operation.

NOTE

The ACTIVE indicator light on each function card is illuminated when that card is selected.

At the completion of the self-test, the MI 5010 asserts the Service Request (SRQ) line on the IEEE 488 digital interface. Refer to the Programming Information section of this manual for instructions on how to clear the power-up service request condition.

The ADDRESSED light on the MI 5010 is illuminated every time the MI 5010 is programmed (addressed) to talk or listen over the IEEE 488 digital interface; it should be off at power-up (not under program control).

The power-on conditions for the MI 5010/MX 5010 operating system, including the function cards, are restored by the INIT command sent over the IEEE 488 digital interface. For more information on this command and a list of power-up parameters, refer to the Programming Information section of this manual and the associated function card instruction manual(s).

Operator's Checkout Procedure

The operator's checkout procedure for the MI 5010 requires a controller, a TM 5000-Series power module, a standard GPIB cable, and at least one function card. If an operator's checkout is desired, use the MI 5010 Software Checkout procedure outlined in the Performance Check section of this manual.

The Software Checkout procedure does not fully check the performance of any function card; the function card is used only to verify the MI 5010. Complete performance checks for function cards are found in their individual instruction manuals.

Repackaging Information

The MI 5010 and MX 5010 are packaged in separate containers. If either unit is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner (with address) and the name of the individual at your firm that can be contacted. Include complete instrument description, serial number, and a description of the service required.

If the original package is not fit to use or not available, repackage the instrument as follows.

Surround the instrument with polyethylene sheeting, or other suitable material, to protect the exterior finish. Obtain a carton of corrugated cardboard of dequate strength that has inside dimensions no less than six inches more than the instrument dimensions. Cushion the instrument by tightly packing dunnage or urethane foam between the carton and the instrument, on all sides. Seal the carton with shipping tape or an industrial stapler.

The carton test strength for your instrument is 200 pounds.

PROGRAMMING INFORMATION

INTRODUCTION

GENERAL INFORMATION

NOTE

The MI 5010/MX 5010 system connects to the IEEE 488 digital interface through a TM 5000-Series power module. Refer to the System Installation section of this manual for information related to setting the primary address and message terminator switches before programming any system unit.

This section of the manual provides information for programming the MI 5010/MX 5010 Multifunction Interface system by remote control via the IEEE 488 digital interface. The digital interface is specified and described in the IEEE 488-1978 standard, "Standard Digital Interface for Programmable Instrumentation".

The following information assumes that the reader has some exposure in understanding the communication process between instruments on the IEEE 488 digital interface and some experience with controller programs. In this manual the IEEE 488 digital interface is called the General Purpose Interface Bus (GPIB).

NOTE

The IEEE 488-1978 standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, N.Y. 10017.

The MI 5010/MX 5010 system is designed to communicate with any GPIB-compatible controller that sends ASCII characters (ISO 7-bit coded representation) or messages over the digital interface. The messages are commands used to program the system or used to request information related to data events, conditions, or status of the system.

The commands are designed for compatibility among instrument types. The same command is used for different cards or instruments to control similar functions. In addition, commands are specified in mnemonics related to the functions they implement. For example, the INIT command initializes instrument settings to their power-up states.

The commands are presented in four different formats, as follows:

- A front panel illustration—showing command relationships to front panel controls (if any), plus a non-descriptive list of all commands related to internal parameters. See Fig. 3-1.
- System/Status Command Summary—a list of commands related to the complete operating system, with abbreviated descriptions.
- Card Control Command Summary—a list of commands resident in the MI 5010 for controlling function cards, with abbreviated descriptions.
- Detailed Command List—an alphabetical listing of all commands, with complete detailed descriptions.

NOTE

The specific commands used to program a selected function card are found in the individual instruction manual for any one particular card. See "SELECT" command.

SYSTEM/STATUS COMMAND SUMMARY

Introduction

The following System/Status commands may be sent from the controller to the MI 5010 in the mode(s) indicated by the letter I (immediate mode) and letter B (buffered mode). If a more detailed description is needed, see the Detailed Command List.

Header	Argument(s)	Mode	Description
ERR?		I/B	Error query. With RQS ON returns error code for most recent event reported when serial polled. With RQS OFF it returns the highest priority status. See Table 3-1.
ID?		I/B	Identify instrument query.
INIT		I	Initializes system to its power-up state.
OPC	ON	I/B	Operation complete SRQ. Buffered commands executed on completion of EXECUTE command.
	OFF	I/B	Disables operation complete function.
OPC?		I/B	Operation complete query.
RQS	ON	I/B	Enables SRQ assertion.
	OFF	I/B	Disables SRQ assertion (except power-on).
RQS?		I/B	Request for service query.
SET?		I/B	MI 5010 settings query.
TEST		I	Self-test command.
USER	ON	I/B	Enables user SRQ function (INST ID button).
	OFF	I/B	Disables user function.
USER?		I/B	User function query.

CARD CONTROL COMMAND SUMMARY

Introduction

The following commands are used to control function cards and may be sent from the controller to the MI 5010 in the mode(s) indicated by the letter I (immediate mode) and the letter B (buffered mode).

Header	Argument(s)	Mode	Description
BUF	ON	I	Opens command storage buffer.
	OFF	I	Closes command storage buffer.
COND	1	I/B	Sets flag for WAIT COND command.
	0	I/B	Resets flag for WAIT COND command.
COND?			Condition query.
EXEC	<num>	I	Closes command storage buffer, if open, and executes the number of times designated by the argument. Argument values 0 to 254. 0 causes no executions, but an SRQ is generated if OPC ON has been received.
	<−num>	I	Buffered commands executed indefinitely (always). Execution ceases on receipt of a STOP, EXEC <num>, INIT, or TEST command.
EXEC?		I/B	Execute query.
SEL	<slot num> [,card name]	I/B	Selects function card defined by argument(s).
SEL?		I/B	Card select query.
STOP		I/	Stops execution of buffered command sequence.
TIME	<hh>: <mm>: <ss> [,50 or 60 or 400]	I/B	Initializes time-of-day clock. Second argument equals power line frequency; default = 60 Hz.
TIME?		I/B	Time-of-day clock query.
TRIG		I/B	Performs same function as <GET> interface message. See IEEE 488 Interface Messages, and Detailed Command List.
UNTI	<hh>: <mm>: <ss>	I/B	Sets the time comparison value for the WAIT UNTIL command.
UNTI?		I/B	Time comparison value query.

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Header	Argument(s)	Mode	Description
WAI	TRIG	B	Suspends execution of the command storage buffer until receipt of the TRIG command or <GET>.
	COND	B	Suspends execution of the command storage buffer until an armed function card receives a condition defined for the selected card.
	UNTI	B	Suspends execution of the command storage buffer until the time-of-day clock equals the argument value specified in the UNTIL command.
	<num>	B	Suspends execution of the command storage buffer until <num> of seconds has passed.
	OFF	B	No waiting period for buffered mode execution.
WAI?		I/B	Wait status query.

COMMANDS AND MESSAGE FORMATS

Introduction

Each command begins with a header—a word that describes the function to be implemented. Many commands require an argument value following the header—a word or number that specifies the desired state of the implemented function.

The query commands have no arguments; the header contains the question mark character (?) to identify the header as a query command.

NOTE

Command headers and arguments must contain, as a minimum, the exact characters and minimum number of characters shown in the abbreviated examples listed in the Detailed Command List.

Operating Modes

The MI 5010/MX 5010 system has two operating modes; "immediate" and "buffered". In the immediate mode, commands are executed immediately after receipt of the message terminator (EOI ONLY or LF/EOI). In the buffered mode, commands are stored in a command execution buffer before execution. Loading the buffer is started with the BUFFER ON command. Loading of the buffer ceases when the BUFFER OFF command is received (system is returned to the immediate mode). Execution of the commands in the buffer requires an EXECUTE command, which causes the commands to be cycled in the sequence they were loaded.

NOTE

If the power-on self-test routine has been successfully completed, the system enters the immediate mode with the Service Request (SRQ) line on the IEEE 488 digital interface asserted.

Command Separator

A complete message contains one command or a series of commands, followed by a message terminator. Messages consisting of multiple commands must have the commands separated (delimited) by semicolons. A semicolon at the end of a complete message is optional. For example, each line immediately following is a complete message.

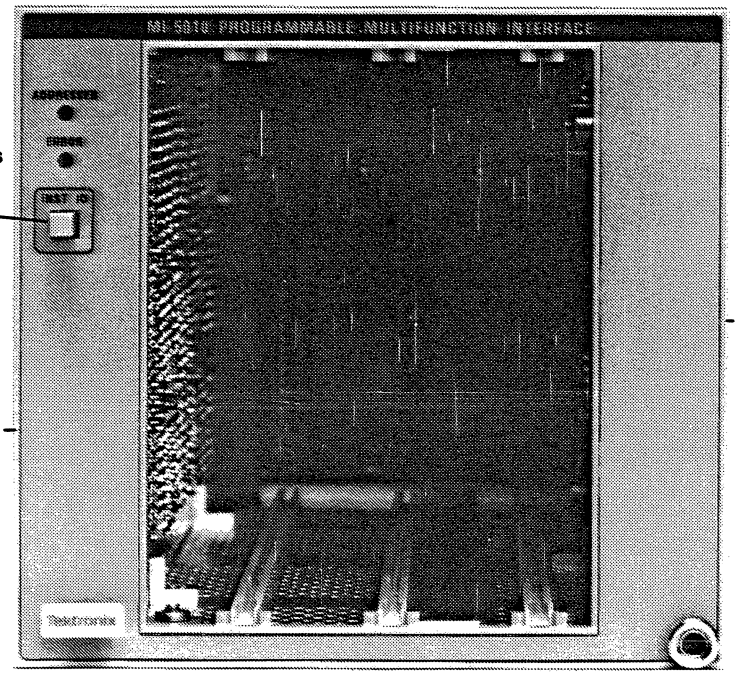
```
INIT
TEST;INIT;RQS ON;USER OFF;ID?;SET?
SET?;
```

Message Terminator

A complete message may be terminated with EOI or the ASCII line feed character (LF). Some controllers assert the EOI line on the GPIB concurrently with the last data byte in the message; others use only the LF character as a terminator. The MI 5010 can be set to accept either type of message terminator (see Preparation for Use).

With EOI ONLY selected as the terminator, the MI 5010 interprets a data byte received with the EOI line asserted as the end of an input message. The MI 5010 also asserts the EOI line concurrently with the last data byte of an output message.

If LF/EOI is selected as the message terminator, the MI 5010 interprets the LF character without EOI asserted, or any data byte received with EOI asserted, as the end of an input message. At the end of an output message, the MI 5010 transmits carriage return <CR>, followed by line feed <LF> with EOI asserted.



System/Status

- USER ON
- USER OFF
- USER?

- ERR?
- ID?
- INIT
- OPC ON
- OPC OFF
- OPC?
- RQS ON
- RQS OFF
- RQS?
- SET?
- TEST

Card Control

- BUF ON
- BUF OFF
- COND 1
- COND 0
- COND?
- EXEC<num>
- EXEC<−num>
- EXEC?
- SEL<slot num>[,name]
- SEL?
- STOP
- TIME<hh>:<mm>:<ss>[,num]
- TIME?
- TRIG
- UNTI<hh>:<mm>:<ss>
- UNTI?
- WAI TRIG
- WAI COND
- WAI UNTI
- WAI<num>
- WAI OFF
- WAI?

3712-07

Fig. 3-1. Front panel with command list.

@

NOTE

The MI 5010 is shipped with EOI ONLY selected as the message terminator and bus address set to decimal 23.

Formatting a Message

Commands must have the proper format (message syntax) to be understood. However, this format is flexible in that many variations are possible. The following describes this format and the acceptable variations.

The system expects all commands to be encoded in ASCII and will accept both upper and lower case characters. All data output returned to controller is in upper case.

A command consists of a header followed, if necessary, by an argument (or arguments). A command with argument must have a header delimiter which is the space character <SP> between the header and the first argument. The space character <SP>, carriage return <CR>, and line feed <LF> are shown as subscripts in the following examples. If extra formatting characters are added between the header delimiter and the argument, they are ignored.

Example 1:

RQS$_{SP}$ON;

Example 2:

RQS$_{SP\ SP}$ON;

Example 3:

RQS$_{SP\ CR\ LF}$
$_{SP\ SP}$ON

In general, these formatting characters are ignored after any delimiter and at the beginning and end of a message:

Example 4:

$_{SP}$RQS$_{SP}$ON;$_{CR\ LF}$

Example 5:

$_{SP}$USER$_{SP}$OFF

NOTE

All message units must be delimited with a semicolon (;) or a message terminator. Space characters <SP> are not allowed between the last alpha or numeric character in any message unit and the message unit delimiter (;) or message terminator. Also, the <LF> character cannot be used for format if the LF/EOI message terminator mode is selected.

In the command list some headers are listed in two forms, a full-length command version and an abbreviated version. Any header or argument containing at least the characters listed in the abbreviated form will be accepted. Any characters added to the abbreviated version must be those given in the full-length version.

For documentation of programs the user may add alpha characters to the full-length version. Alpha characters may also be added to a query header, provided that the question mark character (?) is added at the end of the alpha characters. For example:

USER?
USERE?
USEREQ?
USEREQUEST?

Multiple arguments are separated by commas. However, a space (SP) or spaces will be accepted as a delimiter. For example:

2,3
2$_{SP}$3
2,$_{SP}$3

NOTE

In the last example the space is treated as a format character because it follows the comma (the argument delimiter).

Numeric Argument Formats

The following kinds of numbers for any of the numeric arguments following the header will be accepted.

- Signed or unsigned integers (including +0 and −0). Unsigned integers are interpreted as positive. Examples:

  +1, 2, −1, 10

- Signed or unsigned decimal numbers. Unsigned decimal numbers are interpreted as positive. Examples:

  −3.2, +5.0, 1.2

- Floating point numbers expressed in scientific notation. Examples:

  +1.0E−2, 1.0E−2, 1.E−2, 0.01E+0

Numeric arguments are rounded to the nearest unit of resolution and then checked for out-of-range conditions.

MESSAGE PROCESSING

Introduction

When a message is received, it is stored in an input buffer, processed, and then executed. Processing a message consists of decoding commands, detecting delimiters, and checking the message syntax.

When commands are processed, the indicated changes are then stored in an execution buffer. If an error is detected during processing, the MI 5010 asserts the Service Request (SRQ) line, ignores the remainder of the message, and resets the execution buffer. Resetting the execution buffer avoids undesirable states, which could occur if some commands are executed while others in the same message are not.

Executing a message consists of performing the actions specified by its command(s). This involves updating the instrument settings and recording these updates in a current settings buffer. The commands are executed in groups; that is, a series of commands is processed and recorded in the execution buffer before execution takes place.

Normally, execution of the settings occurs when the instrument processes the message terminator. However, the normal execution of settings is modified by the DT SET and DT TRIG commands listed for the function cards.

When a query-output command is processed in a message, all preceding commands are reserved and will be executed prior to execution of the query command. The query command is executed by retrieving the appropriate data and loading it in the output buffer; processing and execution then continue for the rest of the message. The data in the output buffer are sent to the controller when the instrument is made a talker.

All commands are executed in the order received, so that the buffered mode of operation can be precisely defined.

Multiple Messages

The input buffer has finite capacity, and to avoid having a single message long enough to fill it, each portion of the message is processed before additional input data are accepted. During command processing, additional data are held off (NRFD line on the GPIB is asserted) until space is available in the buffer.

After a query command in a message is executed, the response is held in the output buffer until the controller makes the instrument a talker. If a new message is received before all of the data in the output buffer are read, the output buffer is cleared before executing the new message. This prevents the controller from getting unwanted data from old messages.

One other situation may cause the data in the output buffer to be deleted. The execution of a long message might cause the output buffer to become full. This occurs when a large number of queries (greater than 30) are being retained for transmission. This can be caused by a long input string or from buffered mode execution. When the MI 5010 detects this condition (output buffer full), it generates an error message, asserts the SRQ line, and deletes the data in the output buffer. This action informs the controller that the message was executed and that the output was deleted.

Talked With Nothing To Say

If the MI 5010 is made a talker without having received a message that specifies exactly what it should output, a single byte message with all data bits equal to 1 (with message terminator) is returned.

Power-Up Default and INIT Command Settings

When powered-up, a diagnostic self-test routine is performed to check the functionality of the memory space and internal circuits. If an internal error is detected, the associated ERROR light will remain illuminated. If no internal error is found, the immediate mode of operation is entered with the SRQ line on the digital interface asserted.

The power-up default settings are as follows:

SEL 0 (or lowest filled slot, 1-6), **OPC OFF, USER OFF, RQS ON,** plus function card default settings.

NOTE

The power-up default settings for the function cards are found in the function card instruction manuals. Function card settings are not reported via the SET? query.

The INIT command returns the system to the power-up default settings, clears the command storage buffer, and returns the MI 5010 to the immediate mode. It does not generate a power-up SRQ.

Remote-Local Operation

When powered up, the MI 5010/MX 5010 is in a remote state, ready to accept interface messages or device-dependent commands from the IEEE 488 digital interface. The system has no "local" mode of operation.

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DETAILED COMMAND LIST

BUFFER (BUF)

Type:
Setting

Setting Syntax:
BUFFER ON
BUFFER OFF

Examples:
BUF ON
or
BUF OFF

Discussion:

The buffer command opens and closes the command storage buffer. After BUF ON, all future commands except BUF OFF and EXECUTE are routed to the command buffer. If a routed command is not buffered, an error is generated. If an error is generated the buffer state returns to BUF OFF.

NOTE

The BUFFER, CONDITION, WAIT, and EXECUTE commands are closely related. Refer to all of these commands when loading the buffer with a command string.

CONDITION (COND)

Type:
Setting and Query

Setting Syntax:
CONDITION 1
CONDITION 0

Examples:
COND 1
or
COND 0

Query Syntax:
CONDITION?

Example:
COND?

Query Response:
COND 1;
or
COND 0;

Discussion:

The CONDITION command and query are used to alter the state of the "condition flag" used by the WAIT COND command. COND 1 sets the flag; COND 0 resets the flag.

COND 1 means that the first WAIT COND command in a buffered command string is ignored on the first execution of the command string, but recognized on the second and all succeeding executions.

COND 0 means that the first WAIT COND command in the command string will be recognized.

ERROR? (ERR?)

Type:
Query

Query Syntax:
ERROR?

Example:
ERR?

Query Responses:
Number codes for specific errors.
See Table 3-1..

Discussion:

With RQS ON, the error query returns the error code for the most recent SRQ generated. With RQS OFF the highest priority error code is returned. Returns error code 0 if no errors.

EXECUTE (EXEC)

Type:
Setting and Query

Setting Syntax:
EXECUTE <+num>
or
EXECUTE <−num>

Examples:
EXEC 10
EXEC −1

Query Syntax:
EXECUTE?

Example:
EXEC?

Query Response:
EXEC <+num>;
or
EXEC −1;

Discussion:

The EXECUTE command informs the operating system how many times the commands in the command buffer are to be executed. <+num> range is from 1 to 254. <−num> causes the buffer to be executed always (indefinitely). Zero (0) causes no executions, but an SRQ is generated if OPC is ON.

Execution ceases on receipt of a STOP, EXEC <num>, INIT, or TEST command.

The EXECUTION command closes the command buffer, if open, and executes the buffered commands in the sequence they were loaded.

IDENTIFY? (ID?)

Type:
Query

Query Syntax:
IDENTIFY?

Example:
ID?

Query Response:
ID TEK/MI5010,V79.1,Fxx;

Discussion:

The ID? query returns the name of the instrument, TEKTRONIX Codes and Format version, and firmware version.

INITIALIZE (INIT)

Type:
Operational

Setting Syntax:
INITIALIZE

Example:
INIT

Discussion:

The INIT command returns the complete operating system, including the function cards, to their power-up default values. This command does not cause a power-up SRQ, nor cause the operating system to go to a "local" mode.

Without function cards installed, the power-up defaults are:

OPC OFF, RQS ON, SEL 0 (or lowest occupied slot), and USER OFF.

NOTE

Refer to function card instruction manuals for their power-up default values.

OPERATION COMPLETE (OPC)

Type:
Setting and Query

Setting Syntax:
OPC ON
OPC OFF

Query Syntax:
OPC?

Query Response:
OPC ON;
or
OPC OFF;

Discussion:

The OPERATION COMPLETE function, when enabled with OPC ON, causes an SRQ to be generated when the execution of the command buffer is completed. Execution normally ceases due to the required number of executions being completed or on receipt of the STOP command.

REQUEST FOR SERVICE (RQS)

Type:
Setting and Query

Setting Syntax:
RQS ON
RQS OFF

Query Syntax:
RQS?

Query Response:
RQS ON;
or
RQS OFF;

Discussion:

The RQS command controls the generation of SRQ's. With RQS OFF no SRQ's (except the power-on SRQ) will be generated. Any pending SRQ's will be generated with SRQ ON.

SELECT (SEL)

Type:
Setting and Query

Setting Syntax:
SELECT <slot num>[,card name]

Examples:
SEL 1;
SEL 3,DEVM70;SEL 2,DEV
SEL 1,RSCM40;SEL 6,DIOM30
SEL 5;

Query Syntax:
SELECT?

Examples:
SEL?

Query Response (one of the following):
SEL 0; SEL 1; SEL 2;
SEL 3; SEL 4; SEL 5;
SEL 6;

Discussion:

This command selects a card so that future card-related commands are decoded by the selected card.

The second (optional) argument allows the SELECT command to guarantee that the card receiving the command is the originally intended card.

If no card is available in the selected slot, or the second argument does not match the intended card, an SRQ is generated and the error reported.

NOTE

The SELECT command is independent of the buffered mode execution process. Any card may be selected and communicated with in the immediate mode while any card is operating in the buffered mode.

SETTINGS? (SET?)

Type:
Query

Query Syntax:
SETTINGS?

Example:
SET?

Query Response:
SEL <slot number>;
OPC ON;
or
OPC OFF;

USER ON;
or
USER OFF;

RQS ON;
or
RQS OFF;

Discussion:

This settings query returns the settings for the MI 5010 only. For function card settings refer to the FSET? query listed in the function card instruction manuals.

STOP

Type:
Operational

Syntax:
STOP

Discussion:

The STOP command causes execution of the command storage buffer to cease. If OPC is ON, SRQ will be generated.

TEST

Type:
Operational

Syntax:
TEST

Discussion:

This command initiates a ROM check and function card power-on test. A ROM check error will cause the ERROR light on the MI 5010 to turn on and halt any further activity. A card error will return:

TEST <error code>;
or
TEST 0; (if no problem)

NOTE

See Table 3-1 for error codes.

TIME (TIM)

Type:
Setting and Query

Setting Syntax:
TIME <hh>:<mm>:<ss>[,num]

Examples:
TIME 01:15:30,60
TIME 08:00:00,50
TIME 23:15:00,400

Query Syntax:
TIME?

Query Response:
TIME <hh>:<mm>:<ss> [,num];

Discussion:

The TIME command initializes the time-of-day clock to the values of <hh>, <mm>, and <ss>. Maximum value for <hh> = 23; 59 for <mm> and <ss>.

The power line frequency is set to 50, 60, or 400 Hz depending on the value of the optional argument (power-up default value is 60). If no line frequency value is sent the present value remains.

The TIME? query returns the current value of the time-of-day clock and line frequency.

NOTE

Power-up default setting is TIME 99:99:99;60 (before clock is first initialized).

TRIGGER (TRIG)

Type:
Operational

Setting Sytax:
TRIGGER

Example:
TRIG

Discussion:

This command generates an immediate <GET> trigger.

If a function card is in the DT SET mode, decoded settings are buffered but not executed until receipt of this TRIG command.

In cards with DT TRIG mode, inputs and outputs will not change until the receipt of the TRIG command, but the internal status will show the changes.

UNTIL (UNTI)

Type:
Setting and Query

Setting Syntax:
UNTIL <hh>:<mm>:<ss>

Example:
UNTI 09:15:00

Query Syntax:
UNTIL?

Example:
UNTI?

Query Response:
UNTI <hh>:<mm>:<ss>;

Discussion:

The UNTIL command sets the time comparison value used by the WAIT UNTIL command. Power-on value is 00:00:00. Maximum value for <hh> = 23; 59 for <mm> and <ss>.

USEREQUEST (USER)

Type:
Setting and Query

Setting Syntax:
USEREQUEST ON
USEREQUEST OFF

Examples:
USER ON
or
USER OFF

Query Syntax:
USEREQUEST?

Example:
USER?

Query Response:
USER ON;
or
USER OFF;

Discussion:

The USER ON command allows the user to generate an SRQ to the controller when the INST ID button is pressed. With USER OFF, this function is disabled.

WAIT (WAI)

Type:
Setting and Query

Setting Syntax:
WAIT CONDITION
WAIT TRIGGER
WAIT UNTIL
WAIT <num>
WAIT OFF

Examples:
WAI COND, or WAI TRIG, or WAI UNTI, or WAI <num>, or WAI OFF

Query Syntax:
WAIT?

Example:
WAI?

Query Response:
WAIT COND; or WAIT TRIG; or WAIT UNTI; or WAIT <num> or WAIT OFF

Discussion:

The WAIT command suspends command buffer execution until the requirement of the specified argument is met. The available requirements are:

1. WAI COND—causes suspension until the detection of a logical condition specified by a function card ARM command and some external operation, or if the "condition flag" is set true by the CONDITION command. A "condition" may have occurred any time since the last WAIT COND or INIT command.

2. WAI TRIG—causes suspension until the receipt of <GET> message or TRIG command. This must occur after the beginning of the wait.

WAIT (continued)

3. WAI UNTI—causes suspension until the time comparison value set by the UNTIL command and the time-of-day clock (TIME command) agree. This must occur after the wait begins.

4. WAI <num>—causes delay in the execution of the command buffer. The range of the argument value is from 0 to 655.35 seconds. Resolution is 10 ms.

5. WAI OFF—causes no delay or wait period before execution of the command buffer.

NOTE

WAIT operations affect only the command storage buffer executions. WAIT settings cannot be sent in the immediate mode. If it becomes necessary to terminate a WAIT period, the following process is suggested:

Send WAI? in the immediate mode; do not precede with BUF ON. The response will describe which wait requirement is currently not satisfied.

If the response is:

1. WAI COND;—send COND 1 in immediate mode.

2. WAI UNTIL <hh>:<mm>:<ss>;—send TIME <hh>:<mm>:<ss>, where <ss> is 1 second less than <ss> in UNTIL argument.

3. WAIT TRIG;—send <GET> message or TRIG command.

4. WAI <num>;—the period cannot terminate until the length of time specified by <num> has been exhausted. The only immediate action that can be taken is to send STOP and terminate buffer execution.

IEEE 488 INTERFACE MESSAGES

Introduction

All of the IEEE 488 interface messages listed below are sent with the ATN line on the digital interface asserted. The low-level WBYTE form listed below for these messages is for TEKTRONIX 4050-Series controllers, and is representative of other controllers. See Fig. 3-2. For the following commands, A = 32 plus instrument address and B = 64 plus instrument address. Example for address 23: A = 32 + 23 = 55, B = 64 + 23 = 87.

NOTE

For Tektronix controllers, the SPE (Serial Poll Enable) and SPD (Serial Poll Disable) interface messages are implemented in the POLL statement. See Programming Examples. The TCT (Take Control), GTL (Go To Local), LLO (Local Lockout), PPC (Parallel Poll Configure), PPE (Parallel Poll Enable), and PPU (Parallel Poll Unconfigure) interface messages are not implemented in the current operating system.

The IFC (Interface Clear) message has the same effect as both the UNTalk and UNListen interface messages. If illuminted, the front panel ADDRESSED light will turn off.

Commands and Responses

Interface Messages	Command	Response
MLA My Listen Address	**WBYTE @A:**	Places instrument in listen mode.
MTA My Talk Address	**WBYTE @B:**	Places instrument in talk mode.
UNL Unlisten	**WBYTE @63:**	Places instrument in unlisten mode.
UNT Untalk	**WBYTE @95:**	Places instrument in untalk mode.
UNL/UNT Unlisten/ Untalk	**WBYTE @63,95:**	Unlistens and untalks the instrument.
DCL Device Clear	**WBYTE @20:**	Terminates the device-dependent message processing, resets the input and output buffers, stops and clears buffered mode operation, and clears the system status byte and SRQ (except for the power-on event).
SDC Selected Device Clear	**WBYTE @A,4:**	Same as for DCL, except instrument must be addressed.
GET Group Execute Trigger	**WBYTE @A,8:**	If a function card is in the DT SET mode, decoded settings are buffered but not executed until receipt of <GET>. In cards with DT TRIG mode, inputs or outputs will not change until receipt of <GET>, though internal status will show the changes. Also releases WAIT TRIG in buffered mode.
SPE Serial Poll Enable	**WBYTE @24:**	Enable MI 5010 to output serial poll status bytes when talked addressed.
SPD Serial Poll Disable	**WBYTE @25:**	Switches MI 5010 back to normal mode of outputting data.

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ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER	
0 0 0 0	0 NUL 0 (0)	20 DLE 10 (16)	40 SP 20 (32)	60 0 30 (48)	100 @ 40 (64)	120 P 50 (80)	140 ` 60 (96)	160 p 70 (112)
0 0 0 1	1 GTL SOH 1 (1)	21 LLO DC1 11 (17)	41 ! 21 (33)	61 1 31 (49)	101 A 41 (65)	121 Q 51 (81)	141 a 61 (97)	161 q 71 (113)
0 0 1 0	2 STX 2 (2)	22 DC2 12 (18)	42 " 22 (34)	62 2 32 (50)	102 B 42 (66)	122 R 52 (82)	142 b 62 (98)	162 r 72 (114)
0 0 1 1	3 ETX 3 (3)	23 DC3 13 (19)	43 # 23 (35)	63 3 33 (51)	103 C 43 (67)	123 S 53 (83)	143 c 63 (99)	163 s 73 (115)
0 1 0 0	4 SDC EOT 4 (4)	24 DCL DC4 14 (20)	44 $ 24 (36)	64 4 34 (52)	104 D 44 (68)	124 T 54 (84)	144 d 64 (100)	164 t 74 (116)
0 1 0 1	5 PPC ENQ 5 (5)	25 PPU NAK 15 (21)	45 % 25 (37)	65 5 35 (53)	105 E 45 (69)	125 U 55 (85)	145 e 65 (101)	165 u 75 (117)
0 1 1 0	6 ACK 6 (6)	26 SYN 16 (22)	46 & 26 (38)	66 6 36 (54)	106 F 46 (70)	126 V 56 (86)	146 f 66 (102)	166 v 76 (118)
0 1 1 1	7 BEL 7 (7)	27 ETB 17 (23)	47 ' 27 (39)	67 7 37 (55)	107 G 47 (71)	127 W 57 (87)	147 g 67 (103)	167 w 77 (119)
1 0 0 0	10 GET BS 8 (8)	30 SPE CAN 18 (24)	50 (28 (40)	70 8 38 (56)	110 H 48 (72)	130 X 58 (88)	150 h 68 (104)	170 x 78 (120)
1 0 0 1	11 TCT HT 9 (9)	31 SPD EM 19 (25)	51) 29 (41)	71 9 39 (57)	111 I 49 (73)	131 Y 59 (89)	151 i 69 (105)	171 y 79 (121)
1 0 1 0	12 LF A (10)	32 SUB 1A (26)	52 * 2A (42)	72 : 3A (58)	112 J 4A (74)	132 Z 5A (90)	152 j 6A (106)	172 z 7A (122)
1 0 1 1	13 VT B (11)	33 ESC 1B (27)	53 + 2B (43)	73 ; 3B (59)	113 K 4B (75)	133 [5B (91)	153 k 6B (107)	173 { 7B (123)
1 1 0 0	14 FF C (12)	34 FS 1C (28)	54 , 2C (44)	74 < 3C (60)	114 L 4C (76)	134 \ 5C (92)	154 l 6C (108)	174 | 7C (124)
1 1 0 1	15 CR D (13)	35 GS 1D (29)	55 - 2D (45)	75 = 3D (61)	115 M 4D (77)	135] 5D (93)	155 m 6D (109)	175 } 7D (125)
1 1 1 0	16 SO E (14)	36 RS 1E (30)	56 . 2E (46)	76 > 3E (62)	116 N 4E (78)	136 ^ 5E (94)	156 n 6E (110)	176 ~ 7E (126)
1 1 1 1	17 SI F (15)	37 US 1F (31)	57 / 2F (47)	77 ? UNL 3F (63)	117 O 4F (79)	137 UNT _ 5F (95)	157 o 6F (111)	1/7 RUBOUT 7F (DEL) (127)

ADDRESSED COMMANDS

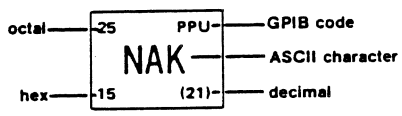
UNIVERSAL COMMANDS

LISTEN ADDRESSES

TALK ADDRESSES

SECONDARY ADDRESSES OR COMMANDS

KEY TO CHART



3888-24

Fig. 3-2. ASCII and IEEE 488 (GPIB) Code Chart.

STATUS AND ERROR REPORTING

Service Request, Status Byte, and Error Query

The IEEE 488 Service Request (SRQ) function may be used by the instrument to alert the controller that it needs service. The SRQ function is also a means of indicating that an event, status change, or error has occurred.

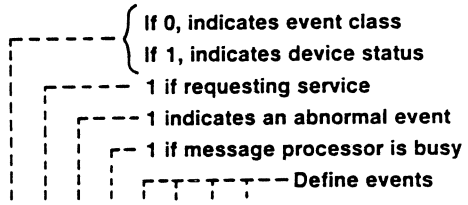
When the controller services the request it performs a serial poll routine. In response, the instrument returns a status byte (STB), indicating whether it needs service or not. The status byte provides a limited amount of information about the SRQ. See Fig. 3-3.

If there is more than one event or error to be reported, the instrument continues to assert SRQ until it reports all events. Each event or error is automatically cleared when it is reported via the serial poll.

NOTE

The DCL (Device Clear) interface message may be used to clear all events, except for the power-on SRQ.

Commands are provided to control the reporting of some individual events and disable all service requests. For example, the USEREQUEST command provides individual control over the reporting of the user request event (INST ID pushbutton pressed). The Request For Service (RQS) command controls whether the instrument reports any events by asserting SRQ. The RQS OFF command inhibits all SRQ's (except power-up event).



	Data Bits								Decimal	
STB Examples	8	7	6	5	4	3		1	Not busy	Busy
Power-on Event	0	1	0	X	0	0	0	1	65	81
Card Event	1	1	1	X	0	0	0	1	225	241
Execution Error	0	1	1	X	0	0	1	0	98	114

3712-08

Fig. 3-3. Status byte definition with examples.

With RQS OFF the controller may find out about events without first performing a serial poll. The error query (ERR?) may be sent at any time and the instrument returns an error code waiting to be reported. The controller can clear all errors by sending the error query (ERR?) until a zero (0) code is returned or send the DCL message.

With RQS OFF the controller may perform a serial poll, but the status byte only contains device-dependent status information. With RQS ON, the status byte contains the class of the event and a subsequent error query returns additional information about the previous event reported by the status byte. Status byte and error code responses are listed in Table 3-1.

Because the status byte conveys limited information about an event, the events are divided into classes; the status byte reports the class of event. The classes of events are defined as follows:

Command Error — indicates the instrument has received a command that is invalid or it cannot understand.

Execution Error — indicates that the instrument has received a command it cannot execute (argument value out of range, or settings conflict).

Internal Error — indicates that the instrument has detected a hardware condition or firmware problem that prevents operation.

System Events — events that are common to instruments in a system (Power On, User Request, etc.).

Execution Warning — instrument is operating but the user should be aware of potential problems.

Internal Warning — indicates that the instrument has detected an internal problem, but remains operational.

Device Status — device-dependent status.

Table 3-1
STATUS BYTE AND ERROR CODES

Description	ERR? Response	Serial Poll Response (STB)
No Errors or Events	0	0
Active, No Errors To Report	0	128
Command Errors		
Command header error	101	97
Header delimiter error	102	97
Command argument error	103	97
Argument delimiter error	104	97
Nonnumeric argument (numeric expected)	105	97
Missing argument	106	97
Invalid message unit delimiter	107	97
Execution Errors		
I/O buffers full, output dumped	203	98
Legal command, but settings conflict	204	98
Argument out of range	205	98
Group execute trigger ignored; busy processing last message	206	98
Select error. No card in that slot.	220	98
Internal Errors		
RAM error on card in slot x	34x	99
ROM error on card in slot x	36x	99
System Events		
Power on	401	65
Operation complete. Execution of buffered commands has been completed	402	66
User request (INST ID pressed)	403	67
Device Warnings		
Time-of-day clock not initialized and WAIT UNTIL command was to be executed.	605	102
Device Dependent (Card) Events		
Power on errors on card in slot x	74x	225
Hardware errors on card in slot x	77x	226
Armed condition warning on card in slot x	79x	192+x

NOTE

Number codes shown in decimal format. If instrument is busy when serial polled, the status byte (STB) code will be 16 higher than number listed. The 4050-Series controller POLL statement returns 0 for serial poll responses 128 to 192; these responses can be obtained by using the WBYTE and RBYTE statements.

TALKER-LISTENER PROGRAMS

The programs listed below can be used to input any high-level command (or query) listed for the multifunction interface system. Query responses or data will be returned to the controller.

TEKTRONIX 4050-Series Controller

```
100 REM MI5010 Talker/Listener Program
110 REM MI5010 Primary Address = 23
120 INIT
130 ON SRQ THEN 240
140 DIM A$(200)
150 PRINT "Enter Message(s): ";
160 INPUT C$
170 PRINT @23:C$
180 REM Check for queries
190 IF POS(C$,"?",1)=0 THEN 150
200 REM Input from device
210 INPUT @23:A$
220 PRINT A$
230 GO TO 150
240 REM Serial POLL Routine
250 POLL X,Y;23
260 PRINT "Status Byte: ";Y
270 RETURN
```

TEKTRONIX 4040-Series Controller

```
100 Rem MI5010 TALKER/LISTENER PROGRAM
110 Rem       PRIMARY ADDRESS = 23
120 Init all
130 On srq then gosub srqhdl
140 Enable srq
150 Dim respons$ to 200
160 Input prompt "ENTER MESSAGE(S): ":message$
170 Print #23:message$
180 Rem CHECK FOR QUERIES
190 If pos(message$,"?",1) then goto 240
200 Rem CHECK FOR 'TEST' COMMAND
210 If pos(message$,"TEST",1) then goto 240
220 Goto 160
230 Rem INPUT FROM DEVICE
240 Input #23:respons$
250 Print "RESPONSE: ";respons$
260 Goto 160
270 Rem SERIAL POLL ROUTINE
280 Srqhdl: poll stb,pri
290 Print "STATUS BYTE: ";stb
300 Resume
310 End
```

Programming Aids

Additional assistance in developing specific application oriented software is available in the following Tektronix manuals. Contact your Tektronix sales representative for more information or order by the following part numbers.

Part Number	Description
070-3985-00	GPIB Programming Guide. Specifically written for applications of Tektronix instruments in IEEE 488 systems. It contains programming instructions, tips, and some specific example programs.
070-2270-00	4051 GPIB Hardware Support manual. An in-depth discussion of IEEE 488 bus operation, explanations of bus timing details, and early bus interface circuits.
070-2058-01	Programming in BASIC.
070-2059-01	Graphic Programming in BASIC.
062-5971-01	4050-Series Programming Aids, T1 (includes software).
062-5972-01	4050-Series Programming Aids, T2, (includes softwre).
070-2380-01	4907 File Manager. Operator's manual.
070-2128-00	4924 User's manual.
070-1940-01	4050-Series Graphic System. Operator's manual.
070-2056-01	4050-Series Graphic System Reference.
070-3918-00	4041 Operator's manual.
061-2546-00	4041 Programming Reference manual.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

PERFORMANCE CHECK

INTRODUCTION

Overview

This Performance Check contains the following procedures:

- MI 5010 Power Supply Check.
- MX 5010 Power Supply Check.
- Software Procedures:

  Part 1, MI 5010 software check without function cards.

  Part 2, MI 5010 software check with function card(s).

  Part 3, MI 5010/MX 5010 combination with function card(s).

NOTE

Each function card requires its own Performance Check. Performance Check procedures for individual function cards are found in the associated function card instruction manual.

The MI 5010 and MX 5010 Power Supply Checks verify the electrical performance requirements listed in the Specification section of this manual.

The software check procedures ensure that the microprocessor in the MI 5010 is communicating properly with a controller on the IEEE 488 digital interface.

Performance Check Interval

Other than a first-time performance check, it is not necessary to check the performance of the MI 5010 or MX 5010 at regular intervals. The performance check should be performed under the following conditions:

- Incoming inspection.
- If used infrequently.
- After repair.
- Operating conditions indicate degradation of performance.

The MI 5010 and MX 5010 have no internal adjustments for calibration purposes. If the instrument fails the performance check, circuit troubleshooting is indicated.

Services Available

Tektronix, Inc. provides complete instrument repair facilities at local field service centers and at the factory service center. Contact your local Tektronix field office or representative for more information.

Test Equipment Required

The test equipment (or equivalent) listed in Table 4-1 is suggested to perform this Performance Check procedure.

Table 4-1
LIST OF TEST EQUIPMENT REQUIREMENTS

Description	Performance Requirements	Example
MI 5010 or MX 5010 POWER SUPPLY CHECKS		
Power Module	GPIB compatibility	TEKTRONIX TM 5003 or TEKTRONIX TM 5006
Calibration Fixture	Rigid Extender Board	TEKTRONIX 067-1066-00
Calibration Fixture	Flexible Plug-in Extender	TEKTRONIX 067-0645-02
Digital Voltmeter		TEKTRONIX DM 501A
Load Resistor	1.25 Ω, 1%, 20 watt	Obtain locally.
Load Resistor	2.0 Ω, 1%, 10 watt	Obtain locally.
Shorting Jumper	3 A capability	Obtain locally.
SOFTWARE CHECKOUT PROCEDURE		
Controller	GPIB compatibility	TEKTRONIX 4051, TEKTRONIX 4052, or TEKTRONIX 4041.
GPIB Cable	Standard GPIB interconnect, length 2 meters.	Tektronix Part No. 012-0630-01.
Power Module	GPIB compatibility	TEKTRONIX TM 5003 or TEKTRONIX TM 5006.
Function Card(s)		TEKTRONIX 50M30, 50M40, or 50M70.

MI 5010 POWER SUPPLY CHECK

1. Preliminary Preparations

a. Remove both side covers and all function cards from the MI 5010.

b. Insert Calibration Fixture, Rigid Extender Board 067-1066-00, into MI 5010 card slot number 1 (next to Microprocessor board).

c. Connect Calibration Fixture, Flexible Plug-in Extender Cable 067-0645-02, between the MI 5010 power connector and any one of the main interface connectors at the rear of the power module.

NOTE

If desired, the MI 5010 may be connected to the GPIB port at the main interface of the power module while it is out of the mainframe. If available, use Calibration Fixture, Extender Cable 067-0996-00.

d. Turn on the POWER to the power module. Allow 2-5 minutes for warm-up.

2. Check Output Voltage, Current Limit, and Under-voltage Restart

a. Connect DVM test leads between TP1311 (−5 V) and TP1120 (DIG GND) on the MI 5010 Power Supply circuit board.

b. CHECK—that DVM reads between −4.75 and −5.25 volts.

c. Disconnect DVM test leads from the Power Supply circuit board and connect them between TP1210 (+5 V LGC SPLY) and TP1201 (DIG GND) on the Microprocessor board.

d. CHECK—that the DVM reads between +4.90 and +5.10 volts.

e. Leave the DVM test leads connected to TP1210 and TP1201.

f. Connect the 1.25 Ω, 20 W resistor between +5 V and D GND test points on the Rigid Extender board. These test points are at the bottom of the board, near the front edge connector.

g. CHECK—that the DVM still reads between +4.90 and +5.10 volts.

h. Leave the DVM test leads connected to TP1210 and TP1201.

i. Connect the 2.0 Ω, 10 W resistor in parallel with the previously connected 1.25 Ω resistor.

j. CHECK—that the DVM reading drops below +4.75 volts, indicating that the power supply is in current limit.

k. Leave the two load resistors still connected and move the DVM test leads between TP1202 (RST) and TP1201 (DIG GND) on the Microprocessor board.

l. CHECK—that the DVM reads equal to or less than 0.4 volt (RESET line at a TTL low).

m. Remove the 1.25 Ω and 2.0 Ω load resistors from the Rigid Extender board.

n. CHECK—that DVM reads equal to or greater than 2.0 volts (RESET line at a TTL high).

NOTE

If available, a logic probe may be used to check the TTL levels on the RESET line.

o. Press and hold the manual reset switch, SW1001, on the Power Supply board.

p. CHECK—that the DVM reads equal to or less than 0.4 volt (TTL low).

q. Release the manual reset switch.

r. CHECK—that the DVM reads equal to or greater than 2.0 volts (TTL high).

s. Disconnect the DVM test leads and turn off the power.

3. Check Active Current Balance and Short Circuit Current

a. Connect a shorting jumper between +5 V and D GND test points on the Rigid Extender board. Turn on the power when connections have been completed.

b. Use the DVM to measure and record the voltage between TP1310 and TP1301 on the Power Supply board.

c. Use the DVM to measure and record the voltage between TP1310 and TP1300 on the Power Supply board.

d. CHECK—that the sum of the two voltages measured in parts 3b and 3c is between 5 mV and 27.5 mV.

NOTE

If a current probe is available, the short circuit current in the shorting jumper on the Rigid Extender board should measure between 0.2 A and 1.2 A.

e. Remove the shorting jumper from the Rigid Extender board.

f. Disconnect the DVM test leads from the Power Supply board and connect them between TP1210 and TP1201 on the Microprocessor board.

g. CHECK—that the DVM reads between +4.9 and +5.1 volts.

h. Disconnect the DVM test leads and remove the Rigid Extender board from the MI 5010.

i. This completes the Performance Check procedure for the MI 5010 power supply.

MX 5010 POWER SUPPLY CHECK

1. Preliminary Preparations

a. Remove the right side cover and all function cards from the MX 5010.

b. Insert Calibration Fixture, Rigid Extender board 067-1066-00, into MX 5010 card slot number 4 (left side slot).

c. Connect Calibration Fixture, Flexible Plug-in Extender Cable 067-0645-02, between the MX 5010 power connector and any one of the main interface connectors at the rear of the power module. Do not connect MX 5010 to MI 5010. Disconnect, if necessary.

d. Turn on the POWER to the power module. Allow 2-5 minutes for warm-up.

2. Check Output Voltage, Current Limit, and Under-voltage Restart

a. Connect DVM test leads between TP1311 (−5 V) and TP1120 (DIG GND) on the MX 5010 Power Supply circuit board.

b. CHECK—that the DVM reads between −4.75 and −5.25 volts.

c. Remove the DVM test leads and reconnect them between pins 24A (+5 V LGC SPLY) and 25A (DIG GND) on J1000 on the MI/MX Bus Extension assembly. If desired, pins 24B and 25B on J1000 may be used.

d. CHECK—that the DVM reads between +4.90 and +5.10 volts.

e. Leave the DVM test leads connected to pins 24A and 25A on J1000 and connect the 1.25 Ω load resistor between +5 V and D GND test points on the Rigid Extender board. These test points are at the bottom of the board, near the front edge connector.

f. CHECK—that the DVM still reads between +4.90 and +5.10 volts.

g. Connect the 2.0 Ω, 10 W resistor in parallel with the previously connected 1.25 Ω resistor on the Rigid Extender board.

h. CHECK—that the DVM reading drops below +4.75 volts, indicating that the power supply is in current limit.

i. With the load resistors still connected, move the positive test lead of the DVM to pin 17A (RESET) on J1000 on the MI/MX Bus Extension assembly.

NOTE

If available, a logic probe may be used to check the TTL levels on the RESET line.

j. CHECK—that the DVM reads equal to or less than 0.4 volt (TTL low).

k. Remove the two load resistors from the Rigid Extender board.

l. CHECK—that the DVM reading on pin 17A is now equal to or greater than 2.0 volts (TTL high).

m. Leave the DVM test leads conencted to pin 17A on J1000, then press and hold the manual reset switch, SW1001, on the Power Supply board.

n. CHECK—that the DVM reads equal to or less than 0.4 volt (TTL low).

o. Release the manual reset switch.

p. CHECK—that the DVM reads equal to or greater than 2.0 volts (TTL high).

q. Disconnect the DVM test leads and turn off the power.

3. Check Active Current Balance and Short Circuit Current

a. Connect a shorting jumper between +5 V and D GND test points on the Rigid Extender board. Turn on the power when connections have been completed.

b. Use the DVM to measure and record the voltage between TP1310 and TP1301 on the Power Supply board.

c. Use the DVM to measure and record the voltage between TP1310 and TP1300 on the Power Supply board.

d. CHECK—that the sum of the two voltages measured in parts 3b and 3c is between 5 mV and 27.5 mV.

NOTE

If a current probe is available, the short circuit current in the shorting jumper should measure between 0.2 A and 1.2 A.

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e. Remove the shorting jumper from the Rigid Extender board and use the DVM to measure the voltage between pins 24A and 25A on J1000 on the MI/MX Bus Extension assembly.

f. CHECK—that the DVM reads between +4.90 and +5.10 volts.

g. Disconnect the DVM test leads, remove the Rigid Extender board, and turn off the power.

h. This completes the Performance Check procedure for the MX 5010 power supply.

SOFTWARE CHECKOUT PROCEDURES

NOTE

This procedure checks the ability of the microprocessor in the MI 5010 to communicate with a controller on the IEEE 488 digital interface.

1. Preliminary Preparations

a. Set up IEEE 488 (GPIB) controller, GPIB cable, and the TM 5000-Series power module for programming operations over the IEEE 488 digital interface.

NOTE

Be certain that the MI 5010 address switches are set to decimal 23 and the message terminator switch is set for EOI.

b. Insert the MI 5010 or MI 5010/MX 5010 combination into the power module and turn on the power to the controller. Do not turn on the power to MI 5010/MX 5010.

c. Load the 4050-Series Talker-Listener program listed or the 4041 Talker-Listener program into the controller's memory. See Programming Information section.

NOTE

If a controller other than those listed above is being used, the Talker-Listener programs must be modified to be applicable to your controller.

d. Turn on the power to the MI 5010; response to the 4050-Series controller should be:

NO SRQ ON UNIT—MESSAGE NUMBER 43

e. Type <RUN>, then hit <RETURN> on controller keyboard; response should be:

ENTER MESSAGE(S): STATUS BYTE: 65

2. Part 1 (MI 5010 Without Function Cards)

a. Send the following messages in the order listed and note the responses. Messages are not sent until the <RETURN> key on the controller is pressed.

Send in Order Listed	Response
ERR?;ERR?	ERR 401;ERR 0;
SET?	SEL 0;OPC OFF;USER OFF;RQS ON;
TEST;ERR?	TEST 0;ERR 0;
USER ON;ERR?;ERR?—press INST ID button before hitting <RETURN>	ERR 403;ERR 0;
RQS OFF—hit <RETURN>, then press INST ID button and hit <RETURN> again	No code number response
RQS ON	STATUS BYTE 67
ERR?;ERR?	ERR 403; ERR 0;
TIME?	TIME 99:99:99,60;
TIME <time-of-day> Example: TIME 09:10:00	No code number response
TIME?	TIME <actual value depends on exact time passed since sending the TIME command>
INIT;SET?	SEL 0; OPC OFF;USER OFF;RQS ON;
SEL 1	STATUS BYTE: 98
ERR?;ERR?	ERR 220;ERR 0;
OPC ON	No code number response

Send in Order Listed	Response
EXECUTE 0	STATUS BYTE: 66
ERR?;ERR?	ERR 402;ERR 0
INIT;SET?;ERR?;ERR?	SEL 0;OPC OFF;USER OFF;RQS ON;ERR 0;ERR 0
WAI?;EXEC?; COND?;UNTI?	WAI OFF;EXEC 0;COND 0;UNTI 00:00:00;
BUF ON;WAI .01;BUF OFF;OPC ON:EXEC 1	STATUS BYTE: 66
ERR?;ERR?	ERR 402;ERR 0

g. This completes Part 1 of the Software Checkout procedure. Turn off the power and go to Part 2.

3. Part 2 (MI 5010 Only, With Function Cards)

NOTE

This procedure checks the ability of the microprocessor to select and communicate with a function card in the MI 5010 (slots 1, 2, and 3).

a. Install a single 50M30, 50M40, or 50M70 (or any three cards) in the MI 5010 and turn on the power. If a single card is used, install it in slot number 1.

b. CHECK—that the ACTIVE light(s) is momentarily illuminated and that the ERROR light turns off after completion of the power-up self-test routine. ACTIVE light on lowest filled slot will remain on.

c. If a single card is used, input the following command string to the controller:

SEL 1;NAME?

If all three card slots are filled, input the following command string:

SEL 1;NAME?;SEL 2;NAME?;SEL 3;NAME?

d. CHECK—for the appropriate response. The appropriate response(s) are:

For a 50M30—NAME DIOM30,V79.1,Fxx;
For a 50M40—NAME RSCM40,V79.1,Fxx;
For a 50M70—NAME DEVM70,V79.1,Fxx;

where xx in the last message unit is the firmware version number.

e. Input a misspelled NAME? command to the single card in slot 1 or to all three function cards in the MI 5010, for example:

SEL 1;NME

f. CHECK—that the response is:

ERR 101;

for each card selected.

g. If a single card has been used, turn off the power and reinstall the single card in slot 2. Turn on the power.

h. Repeat parts 3b through 3f.

i. Turn off the power and reinstall the single card in slot 3. Turn on the power.

j. Repeat parts 3b through 3f.

k. Turn off the power to the MI 5010 and go to Part 3 only if the MX 5010 is to be checked with the MI 5010. This completes the software checkout procedure for the MI 5010.

4. Part 3 (MI 5010/MX 5010 Combination)

NOTE

For this procedure, the MX 5010 must be electrically attached to the MI 5010 and installed in an adjacent power module compartment. Perform Part 1 and Part 2 of this procedure before Part 3.

a. Install a single 50M30, 50M40, or 50M70 (or any three cards) in the MX 5010 and turn on the power. If a single card is used, install it in slot number 4.

b. Repeat parts 3b through 3j, except use SEL 4, SEL 5, or SEL 6, as appropriate, for the SEL command input to the controller (slot numbers are 4, 5, and 6 instead of 1, 2, and 3).

c. This completes the software checkout procedure for the MI 5010/MX 5010 combination.

THEORY OF OPERATION

MICROPROCESSOR (KERNEL)

Microprocessor (U1111) ◇1

NOTE

For more detailed information on the internal operation of a microprocessor, refer to the manufacturer's data sheet.

Integrated circuit U1111 is an 8-bit microprocessor containing an internal 1 MHz clock, a divide-by-four clock input circuit, and 128 bytes of internal random-access-memory (RAM). The microprocessors internal RAM is located at hexidecimal addresses 0000 to 007F.

The internal, single phase, 1 MHz TTL clock output on pin 37 is derived from a 4 MHz crystal controlled oscillator, Y1100 and associated components. An external TTL compatible clock input on the auxiliary connector, J1214, may be used by connecting jumper plug P1102 to pins 2 and 3 of J1102 and removing P1101 from pins 1 and 2 of J1101. External clock frequencies greater than 1 MHz will cause the clock output on pin 37 to be one-fourth the external input frequency. The external clock should not be halted for more than 4.5 μs.

The crystal oscillator circuit operates in the series resonant mode with inductor L1100 ensuring that the crystal starts oscillating at 4 MHz. Capacitor C1109 and resistor R1109 are used to shock the circuit into oscillation. Resistor R1109 effectively disconnects C1109 from the ac circuit after start up, thereby preventing frequency pulling.

The RESET signal starts the microprocessor from a power down condition (power failure or initial start up) or when the RESET switch on the power supply board is pressed. This signal originates on the power supply board which, in turn, does not generate this signal until the PWR signal from the TM 5000 power module is received (see power module instruction manual). When a high level is detected on pin 40, the microprocessor begins the restart sequence. See Power Supply and Reset description (schematic 8).

Pin 3 of U1111 and pin 2 of U1003 (schematic 5) are tied high via logic gate U1116C. This causes the clock output of U1111 to operate normally (not stretched) and locks out the direct memory access request feature of the GPIB control chip, U1003. The high level output from U1116C is also used to set high levels on pin 9 of U1117C, pin 12 of U1214C (schematic 2), and pin 5 of U1214B (schematic 3).

Pin 36 of U1111 controls the microprocessor's internal RAM (addresses 0000 to 007F). Pin 36 is pulled high by R1112 (schematic 5) to enable the RAM and remains high unless the microprocessor board is configured for the forced instruction mode. The microprocessor's internal RAM is disabled for this mode by grounding pin 36 via P1212 (J1212) on schematic 5. This has the effect of disabling the microprocessor's output data buffer. The Non-Maskable Interrupt (NMI, pin 6) is held high by R1105.

Normal low level TTL interrupt request signals to U1111 occur on pin 4 ($\overline{IRQ}$) and can originate from any one of the four labeled sources connected to the wired-OR junction. All four of these interrupts are maskable. The microprocessor may or may not recognize these interrupts depending on the operating conditions when the signal occurs. When recognized, the microprocessor completes its current instruction before servicing the current interrupt condition. A memory map for interrupt vectors is listed in Table 5-1.

Table 5-1
MEMORY MAP FOR INTERRUPT VECTORS
(Hexidecimal Addresses)

Vector		Description
MS	LS	
FFFE	FFFF	RESET (restart)
FFFC	FFFD	Non-Maskable Interrupt (NMI)
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request (IRQ)

The $\overline{HALT}$ function for U1111 (pin 2) is tied high via R1107. The bus available (BA) signal is buffered by U1214A.

Two other output control lines (VMA, pin 5 and R/$\overline{W}$, pin 34) are used by the microprocessor to read data from and write data to peripheral devices. The R/$\overline{W}$ signal goes low to write data to or goes high to read data from the data buses.

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The VMA line goes low to indicate that the 16-bit code on the address bus is not a valid memory address. VMA does not go low between machine instructions unless the microprocessor is using the address register for some operation other than accessing a valid location in memory or input/output peripherals. VMA is not gated by nor necessarily related to the $\phi 2$ clock in any way. An operational flow chart for U1111 is illustrated in Fig. 5-1.

Address Buses ◇1

There are three separate address buses: the microprocessor address bus (A0–A15), the internal address bus (IBA0–IBA15), and the external address bus (EBA0–EBA15). In no case, are any of these buses tied directly to another.

Integrated circuits U1112, U1115, U1010, and U1011 operate as unidirectional buffers from the microprocessor address bus to the internal and external address buses. Buffer U1112 carries the low order address bits and U1115 carries the high order address bits to the internal address bus. The address bits to the external address bus (via U1010 and U1011) are not connected in a low and high order fashion. Under normal operating conditions these buffers are always enabled. All four of these address buffers are disabled when pin 19 on U1112 and pin 1 on U1115, U1010, and U1011 go high.

The external address bus on J1000 is used by the microprocessor to address the memory and peripheral devices located on a selected card. The internal address bus is used to address the memory and peripheral devices on the microprocessor board.

Data Buses ◇1

There are four data buses on the microprocessor board: the microprocessor data bus (D0–D7), the internal data bus (IBD0–IBD7), the external data bus (EBD0–EBD7), and the GPIB data bus (DIO1–DIO8) located on P1005 (schematic 5).

Both integrated circuits, U1014 and U1110, operate as unidirectional data buffers; U1014 is used by the microprocessor to read data from the internal bus and U1110 is used to write data to the internal data bus.

The write data buffer, U1110, is an octal D-type transparent latch. As long as pin 11 is held high by the system clock signal (Bϕ2), the outputs (1Q–8Q) follow the data inputs (D0–D7). When the clock signal goes low, the output is latched at the level of the data that was set up. This latch allows interfacing with slow memory devices because data can be held on the internal data bus for a finite amount of time longer than the microprocessor is capable of holding data on its data bus. Old data can be retained in or new data entered into U1110 even while the Q outputs are off. The Q outputs are off when pin 1 is high and data is written onto the internal data bus when pin 1 is set low via U1117C.

When pin 34 of U1111 is set high to read data from the internal data bus via U1014, pin 5 of U1116B is set high. In order to read data from the internal data bus pins 1 and 19 of U1014 must both be low. This condition will exist when the system clock on pin 4 of U1116B is high and the $\overline{\text{INT DATA ENBL}}$ signal on pin 19 of U1014 is low. The system clock is high for the last half of any given cycle.

Pin 19 of U1014 is low any time there is a read or write operation from or to hexidecimal addresses 0000 through 3FFF or addresses E000 through FFFF. For a write operation pin 1 is set high, disabling U1014. The internal and external data buses are never active at the same time.

Data communication to and from a selected function card is via U1012, an octal bus transceiver with tri-state outputs. The IBR/$\overline{\text{W}}$ signal on pin 1 controls the direction of data flow over the external bus; a high state for a read operation or a low state for a write operation. The external bus is selected for read or write operations that require hexidecimal addresses in the 4000–DFFF range.

ADDRESS AND BUS SELECT DECODERS

Page 0 Decoder ◇2

Table 5-2 lists the hexidecimal address ranges for the memory and peripheral devices in the MI 5010.

Integrated circuits U1102, U1113A, U1210E, U1113B, U1210B, U1113C, and U1210D comprise the Page 0 Decoder. These circuits decode the addresss for the devices in the 0000–00C7 range (see Table 5-2).

Integrated circuit U1102 operates to allow the microprocessor to communicate with its own internal RAM, the VIA IC (U1213, schematic 4), and the GPIB Control IC (U1003, schematic 5).

Pin 6 of U1102 remains high as long as none of the address bits IBA11 through IBA15 go high. Pin 5 remains high as long as none of the address bits IBA8 through IBA10 go high. Pins 5 and 6, when both are high, enable logic gates U1113A and U1113C. Whether U1113A or U1113C are addressed depends on the state of the IBA7 bit; if IBA7 is high

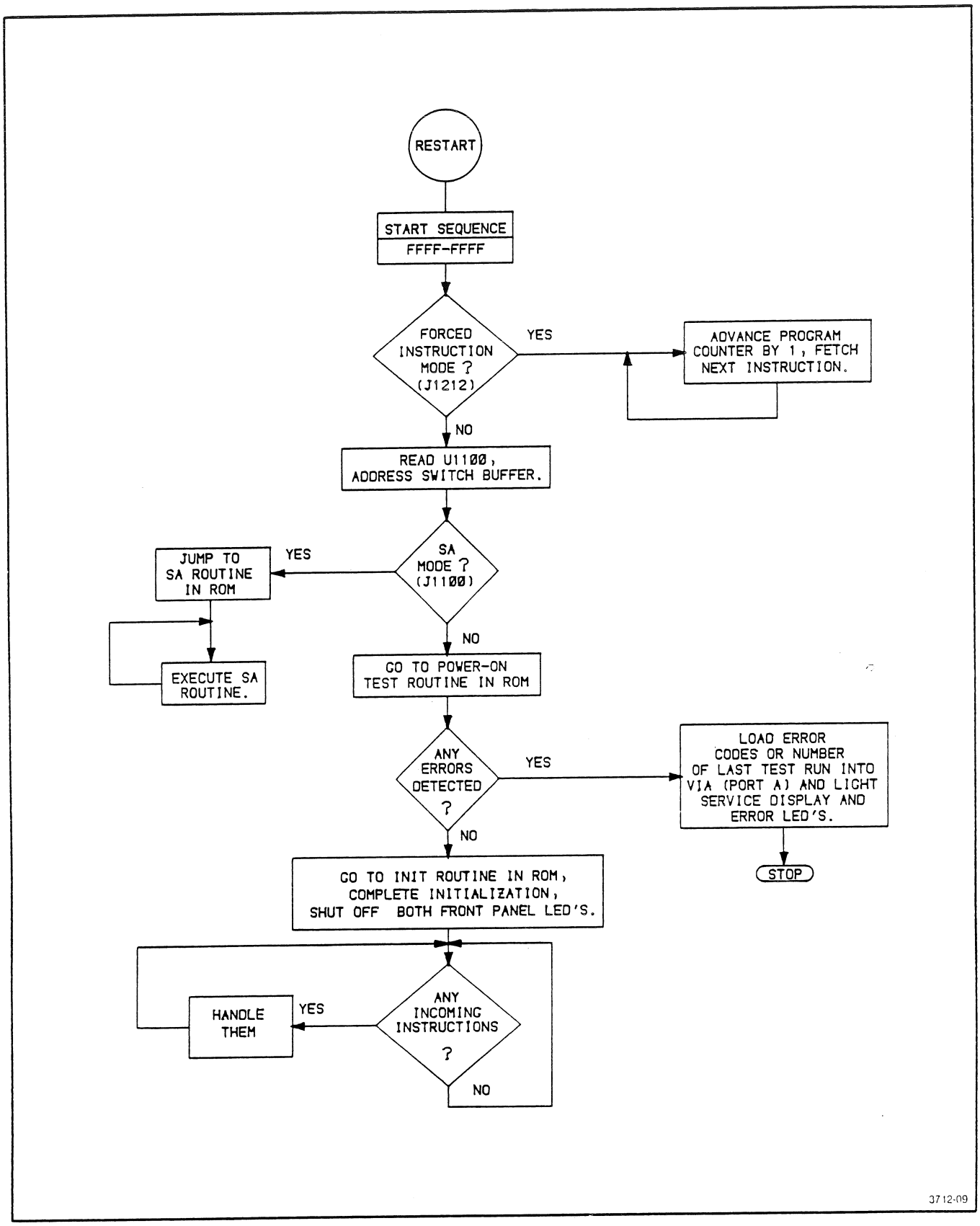

Fig. 5-1. Microprocessor operational flow chart.

Table 5-2
MEMORY ADDRESS RANGES

Device Selected/Schematic		Hexidecimal Addresses
Microprocessor RAM U1111	◇5	0000–007F
Versatile Interface Adapter, VIA U1213	◇4	0080–008F
GPIB Control U1003	◇5	00C0–00C7
System RAM U1201	◇3	2000–23FF (1k x 8) or 2000–27FF (2k x 8)
Expansion RAM U1202	◇3	2800–2BFF (1k x 8) or 2800–2FFF (2k x 8)
Address Switch Register S1000, U1000	◇5	3000 (Read Only)
Card Select Latch U1013	◇3	3000 (Write Only)
Bank Region ROM (External Bus)	Any selected card	4000–DFFF
System ROM U1103, U1200	◇3	F000–FFFF E000–EFFF

pin 12 of U1113A goes low, if IBA7 is low the inversion on pin 14 of U1210D causes pin 8 of U1113C to go low. During the time that the microprocessor is communicating with its internal RAM, pin 8 of U1113C is held low, disabling the internal data bus (IBD0–IBD7) via pins 3 and 6 of U1114.

Pin 12 of U1113A will be low for hexidecimal addresses in the 0080–00FF range. This 128-byte region is divided into two parts, the upper half dedicated to the GPIB Control IC and the lower half dedicated to the VIA IC. The VIA IC has two input select lines, $\overline{CS2}$ (U1113A, pin 12) and CS1 (U1210B, pin 16). The $\overline{CS2}$ signal must be low for the microprocessor to access either the GPIB or the VIA. The high level CS2 signal on pin 7 of U1210E enables logic gate U1113B at pin 5. With U1113B enabled and assuming a high level also on pin 4, the logical state of address bit IBA6 determines which of the two ICs are being accessed by the microprocessor. When IBA6 is high, the GPIB Control IC is being selected by the low level on pin 6 of U1113B. When IBA6 is low, the VIA is being selected by the high level CS1 signal on pin 16 of U1210B.

The GPIB Control and VIA ICs are accessed in different ways, due to different access and setup times. The GPIB is selected only during the time that the buffered clock (B02) and the buffered valid memory address (IBVMA) signals on pins 5 and 4 of U1101B are both high. The VIA IC, due to its very long access time, must be directly clocked by Bϕ2 from pin 14 of U1214D.

Primary and Secondary Decoders ◇2

Integrated circuits U1211 and U1212 comprise the Primary and Secondary Decoders, respectively. Address bits IBA13, IBA14, and IBA15 divide the 65-kbyte memory into eight 8-kbyte blocks (decimal) or eight 2-kbyte blocks (hexidecimal). For example, the hexidecimal range at pin 15 of U1211 is from 0000 through 1FFF, while the range at pin 7 is E000 through FFFF. The binary code on pins 3, 2, and 1 of U1211 is 000 through 111, selecting outputs Y0 through Y7. Five of the addressed outputs, Y2 through Y6, are not connected to any other devices because those addresses are dedicated to the 40-kbyte bank region on the external bus (see Table 5-2). BVMA is the only enable line for U1211. Pin 7 of U1211, when low, enables both ROM ICs on schematic 3.

The Secondary Decoder, U1212, is a dual one-of-four decoder, one-half of which is enabled with a low level on pin 1 for all addresses in the 2000–3FFF range. Address bit IBA12 and IBA11 are decoded on pins 3 and 2, respectively. The binary code for these address bits (00 through 11) selects outputs 1Y0 through 1Y3. The logical states of the signal lines on pin 13 and 14 are decoded by U1212 during the low-level clock period on pin 15 to select outputs 2Y0 or 2Y1.

When hexidecimal address 3000 appears on the address lines, the 1Y2 output (pin 6) goes low and sets a low on pin 13 of U1212. When the read/write signal on pin 14 goes low for a write operation, the binary code (00) on pins 13 and 14 selects the 2Y0 output to go low. A low on pin 12 enables the inputs of the Card Select Latch, U1013 (schematic 3), during the negative half of the clock period on pin 15 of U1212. The microprocessor never reads the Card Select Latch; a copy of which function card has been selected is stored in RAM.

When pin 14 of U1212 goes high for a read operation, the binary code for pins 13 and 14 is 01. This code selects the 2Y1 output (pin 11) to go low and disables logic gate U1117B at pin 3. This, in turn, sets a low on pin 9 of U1210G and disables the external and internal buses via pins 1, 12, 4, and 6 of U1114, respectively. With these two buses disabled, the microprocessor can then proceed to use its data bus (D0–D7) to read the contents of the Address Switch Register in U1000 (schematic 5). The Address Switch Register is enabled by the low level ASE signal on pin 19.

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The System RAM, U1201 (schematic 3), is selected when pin 4 of U1212 goes low. Pin 7 of U1212 goes low when the microprocessor enters the signature analysis mode.

Signature Analysis Test Point ◇2

The signal at test point TP1203 (pin 4 of U1216A) has two possible uses; troubleshooting the instrument using signature analysis methods, or using the signal to trigger a logic analyzer at the beginning and end of data transfer over the IEEE 488 digital interface. The MI 5010 can be configured for the signature analysis (SA) mode by physically relocating the position of P1100 with respect to J1100 (schematic 5).

Integrated circuit U1216A is a latched SR flip-flop with the output on pin 4 normally high. When the microprocessor places hexidecimal address 3800 on the internal bus, pin 7 of U1212 and pin 1 of U1216A go low. Pins 2 and 3 of U1216A must also be high (indicating a write operation with a valid memory address) to toggle U1216A from a high state to a low state. Pin 4 remains in the low state as long as the address remains on the internal bus. When the address is removed, pin 4 returns to its normally high state. Pin 1 of U1216A goes low for any hexidecimal address in the 3800–3FFF range.

Bus Select Decoder ◇2

Integrated circuit U1114, along with U1117B, U1210G, and U1210F, operates as the Bus Select Decoder.

Both of the external and internal buses can be disabled via U1117B, U1210G, and U1114 at the same time under three conditions: (1) when the microprocessor's internal RAM is disabled and a low is set on pin 5 of U1117B; (2) when the Address Switch Register, U1000 (schematic 5), is selected to be read and a low is set on pin 3 of U1117B; and (3) when pin 4 of U1117B is set low. Whenever both external and internal buses are disabled, the microprocessor is limited to reading the contents of the Address Switch Register via the D0–D7 data lines. The internal and external buses will never be enabled at the same time; if one is on, the other is off.

Pins 9, 10, and 11 of U1114 are connected to the decoded 0000, 2000, and E000 addressed outputs from U1212. The external bus (U1114, pin 12) is enabled via a high level on pin 12 of U1210F as long as these three inputs to U1114 (pins 9, 10, 11) remain high. If any pin (9, 10, 11) goes low, the external bus is disabled by a low level on pin 12 of U1210F and the internal bus is enabled by the high level on pin 5 of U1114. The external bus can also be disabled by a low level signal on pin 13 of U1114.

The external bus can be mechanically disabled, even when pin 12 of U1114 is low, by relocating P1011 from pins 2 and 3 of J1011 to pins 1 and 2. The low level output from U1100C is then changed to a high level, which disables the external data bus transceiver, U1012 (schematic 1). The low level external bus signal on pin 9 of U1100C is gated with the low level clock signal on pin 10. The gating of these two signals ensures that the external data bus is not enabled until the address and control lines have had time to settle.

The internal bus (U1114, pin 6) is enabled via a high level on pin 5 of U1114 as long as pins 3 and 4 remain high. If any pin (4, 3, 5) goes low, the internal bus is disabled. Note that the external and internal buses are both disabled when the microprocessor's internal RAM is active; pin 8 of U1113C and pins 3 and 2 of U1114 will all be low. Pin 2 of U1114 will be low because pin 9 (0000) will be low. The complete Bus Select Decoder circuit operates to ensure that only one of the three data buses or the microprocessor's internal RAM is operating at any given time. See Table 5-3.

Table 5-3
BUS SELECTION

Mode	Internal Bus	External Bus	Address Switch	Comment
Internal access	On	Off	Off	0000–3FFF/E000–FFFF
External access	Off	On	Off	4000–DFFF
Forced instruction	Off	Off	On	Cycle through all 65k memory continuously.
Address switch access	Off	Off	On	3000 (Read only)
Microprocessor internal RAM access	Off	Off	Off	0000–007F
Jumper inhibit of external bus	X	Off	X	External bus shut off via J1011.

Control Line Buffers ◇2◇

The control line buffer circuit is composed of U1215, U1100A, U1100D, U1214D, and U1214C. The valid memory address and read/write signals are first buffered by U1100A (pin 2) and U1100D (pin 12), respectively.

The outputs of the first buffers are then divided into four separate control signals at the output of U1215, two for the external bus areas of memory and two for the internal areas of memory. In normal operation, the input signals to U1100A, U1100D, and U1215 pass through without inversion.

The microprocessor clock output is buffered by U1214D with complementary outputs on pins 14 and 13. The buffered clock signal on pin 14 of U1214D is used by both the external and internal areas of memory; this signal is terminated by the parallel combination of R1010 and R1011. The voltage level at the junction of these two resistors biases the high level state of the clock signal to about 3.6 V.

Integrated circuit U1214C is always enabled at pin 12 and gates the internal bus read/write signal on pin 11 through to toggle the SA test point (TP1203) on a write operation.

INTERNAL MEMORY (ROM/RAM)

System RAM ◇3◇

The System RAM, U1201, provides the microprocessor with a random access memory space (2k x 8). The microprocessor uses hexidecimal addresses in the 2000–27FF range to address the System RAM.

The most significant bit (IBD7) is tied high via R1200. This resistor allows the operating system to determine how much RAM space is available. For example, the microprocessor writes 0s to the bottom half of each 1 k-byte block from locations 2000 through 2FFF (2000, 2400, 2800, and 2C00). If it then reads back, for example, 0 for 2000, 0 for 2400, F for 2800 and 2C00, it knows that a total of 2k bytes of RAM space is available and where it is located. The microprocessor looks at data bit IBD7, which will always be high if there is no memory at a given address to pull it low when read back.

System ROM ◇3◇

On initial shipment, integrated circuits U1103 and U1200 comprise an 8 k-byte system.

The hexidecimal address range for the System ROM is E000 through FFFF. Assuming ICs 4k x 8 ROM chips for U1103 and U1200, the operation is as follows:

When address E000 appears on the internal address bus, pin 18 of U1200 goes low and pin 2 of U1117A goes high. A high level is also set on pin 18 of U1103 due to U1214B inverting address bit IBA12. This action disables U1103 and enables (selects) U1200 to respond to all addresses in the E000–EFFF range. The read operation on the output data port of U1200 begins when the clock signal on pin 1 of U1117A goes high and sets a low on pin 20 of U1200 and U1103.

For a read operation in the F000–FFFF range, pin 18 of U1200 is high and pin 18 of U1103 is low, disabling U1200 and selecting U1103. The read operation on the output data ports of U1103 is the same as for U1200. The system ROM can be disabled via U1117A.

Card Select Latch ◇3◇

Integrated circuit U1013, with eight internal D-type flip-flops and single rail outputs, operates as the Card Select Latch. Outputs CSEL 1 through CSEL 6 are used to select function cards in slots 1 through 6. Slots 1, 2, and 3 are in the MI 5010 and slots 4, 5, and 6 are in the MX 5010 unit. Slot 1 and slot 4, respectively, are the first slots in each unit, left to right as observed from the front panel of each unit.

When the microprocessor enables the data inputs of U1013 with a low level on pin 1 (3000), it performs a write operation to select the desired function card. Data is presented at the 1D through 8D inputs and this data is latched on the output port (1Q through 8Q) about 30 ns after the inverted clock signal on pin 11 goes high. Only one card is selected for any given period of time by a high level on the appropriate CSEL line; all other CSEL lines will be low. After a card is selected, pin 1 of U1013 goes high and the card select data remains on the output port until pin 1 goes low again to enable U1013 for another card select operation. A read operation is not performed on U1013; card select information is stored in RAM.

Service Display, DS1216 ◇3◇

The Service Display circuit consists of DS1216, U1216C, U1216D, and associated components. The BCD decoder, clocked latch, and current limited LED are all contained within DS1216.

The readout is in hexidecimal format with one of sixteen characters (0...9, A...F) displayed. The display is blanked for every half-cycle of the buffered clock signal on pin 8 (pin 8

goes high). BCD data corresponding to error codes are stored in the peripheral data output registers for the PA port of U1213 (schematic 4). This data is transferred from U1213 to the internal latches of DS1216 each time the clock signal on DS1216 pin 5 goes high.

If the microprocessor board is properly initialized and no errors are detected, the digit 0 will be displayed. If initialization is incomplete, all of the BCD inputs will be high and the letter F will be displayed. Errors detected during the power-up self-test routine are displayed as one digit or alpha character.

Two decimal points, one left-hand and one right-hand, are used to indicate the condition of the inverted buffered clock signal on pin 6 of U1216C. When pin 6 goes low, pin 7 goes high, turning off the left-hand decimal point. The low-to-high transition on U1216C, pin 7 and U1216D, pin 12 also causes U1216D, pin 9 to go low, turning on the right-hand decimal point. With the right-hand decimal point on, if the RESET line (U1216D, pin 11) goes low pin 9 will go high, turning off the right-hand decimal point.

At power-on the RESET line goes low for about 2-3 seconds, blanking the right-hand decimal point for that period of time. It then goes high and remains high unless the RESET button on the power supply board is pressed or a momentary power failure occurs.

Since the outputs of U1216C (pin 7) and U1216D (pin 9) are complementary, the only way for both decimal points to appear to be on is for the clock signal to be running. If the clock signal is locked high or low, one or the other of the decimal points will be completely turned off. If the clock duty cycle is very far off from the normal 50% value, one or the other decimal points will appear brighter, due to intensity modulation. Observing the decimal points yields information about the clock and the RESET line.

NOTE

Refer to Service Display Codes in the Maintenance section of this manual for diagnostic codes associated with DS1216.

PERIPHERAL CONTROL

Versatile Interface Adapter (VIA) ◇4

The Versatile Interface Adapter, U1213, operates as an input/output control device. Control of peripheral devices is handled primarily through two 8-bit bidirectional ports, PA0–PA7 and PB0–PB7. Each PA and PB line can be programmed as either an input or an output.

NOTE

For more detailed information on the internal operation of U1213, refer to the manufacturer's data sheet.

Four register select inputs, RS0, RS1, RS2, and RS3, permit the microprocessor to address U1213 and select any one of 16 internal registers. Register select coding is with address bits IBA0 through IBA3 on pins 38, 37, 36, and 35, respectively. The address coding to select an internal register is shown in Table 5-4.

Two IC select inputs, $\overline{CS2}$ and CS1 (pins 23 and 24), are used to enable U1213 and allow access to an internal register. The selected (addressed) register is accessed when pin 24 is high and pin 23 is low. Refer to the discussion under Page 0 Decoder and Table 5-2 for address decoding (IC select) information.

At power up, or when the RESET button on the power supply circuit board is pressed, the reset signal on pin 34 goes low to clear all of the internal registers to logical 0 (except the internal timers at pins 16 and 17, and the internal shift register). Clearing the internal registers places all of the peripheral interface lines in an input state, disables the timers, shift register, and the interrupt output on pin 21. After the reset signal goes high, the microprocessor can then communicate with U1213.

Assuming that U1213 has been enabled on pins 23 and 24, communication is over the data lines on the internal bus, IBD0–IBD7 (pins 26 through 33). The direction of data transfers between U1213 and the microprocessor is controlled by the read/write signal on pin 22. When pin 22 is low, data will be transferred into a selected internal register; when pin 22 is high, data will be transferred out of a selected internal register. Data transfer in either direction occurs during the high level clock period on pin 25. When U1213 is not selected the internal data bus goes to the high-impedance state.

A microprocessor interrupt signal on pin 39 of U1213 is generated when the front panel INST ID button is pressed. The active negative edge of this signal sets a binary bit in the internal interrupt flag register. The microprocessor reads the internal register to detect if this button has been pushed. If it has been pushed by the operator and the USER OFF command has not been received via the IEEE 488 digital interface, the microprocessor causes the SRQ (Service Request) line on the digital interface to be asserted.

When S1200 is pressed, there is a point where neither the normally closed nor normally open contacts are con-

Table 5-4
U1213 INTERNAL REGISTERS

Register Number	Register Select Codes				Description	
	RS3	RS2	RS1	RS0	Write	Read
0	0	0	0	0	Output Register B	Input Register A
1	0	0	0	1	Output Register A	Input Register A
2	0	0	1	0	Data Direction Register B	
3	0	0	1	1	Data Direction Register A	
4	0	1	0	0	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1 High-Order Counter & Latch	T1 High-Order Counter
6	0	1	1	0	T1 Low-Order Latches	
7	0	1	1	1	T1 High-Order Latches	
8	1	0	0	0	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2 High-Order Counter	
10	1	0	1	0	Shift Register	
11	1	0	1	1	Auxiliary Control Register	
12	1	1	0	0	Peripheral Control Register	
13	1	1	0	1	Interrupt Flag Register	
14	1	1	1	0	Interrupt Enable Register	
15	1	1	1	1	Same as Reg 1 Except No "Handshake"	

nected to anything. When this occurs, pin 14 of U1216B stays high and pin 15 goes high. At that point, pin 13 stays high with no change until pin 14 is actually grounded by the wiper of S1200; pin 13 will then go low. If the switch bounces, pin 14 alternates between high and low, but this has no affect on the output of U1216B. The output stays low until S1200 is released and sets a low on pin 15. If S1200 bounces when released there is no affect on the output; it stays high until pin 14 of U1216B is again grounded by S1200.

Pin 19 of U1213 (CB2) is the input line for the line sync time base (LSTB) signal from the Power Supply board. This signal causes an interrupt at one-tenth power line frequency and is counted by the microprocessor in order to generate the time-of-day information. The number of interrupts counted per second is defined by the optional argument in the TIME command (50, 60, or 400). See Programming Information section.

The internal timers (TMR 1 and TMR 2, pins 17 and 16) are used for the WAIT INTERVAL command. Timer 2 generates a 10 ms period pulse string to Timer 1. Timer 1 contains the number of 10 ms periods that the microprocessor must wait before it executes the commands in the program storage buffer. This number of periods can be the equivalent of 0 seconds up to 655.35 seconds.

The two front panel indicators, DS1200 and DS1201, are illuminated whenever the microprocessor sets a high level on either U1213, pin 14 or pin 15. Both indicators are not normally illuminated at the same time.

Pin 21 of U1213 goes low to notify the microprocessor when an enabled interrupt occurs within U1213. Interrupts may be caused by the active edge of a signal applied to inputs CA1 (pin 40), CA2 (pin 39), CB1 (pin 18), CB2 (pin 19), and time out events of Timer 1 and Timer 2. The logical 0 state of pin 21 can only be cleared by clearing all enabled interrupts.

GPIB CONTROL

Address/Service Switch Register ◇5

The Address/Service Switch Register is composed of S1000, U1000, and associated components. Five internal contacts of S1000 are labeled as to their binary weight with the top switch (TC, pins 1 and 12) being the message terminator switch. An open switch equals a logical 1 (high) set on the inputs to U1000, A1 through A6; a closed switch equals a logical 0 (low). At power-up, the microprocessor reads the address switch via buffer U1000 and stores it in an address register located in the GPIB Control IC, U1003. A read only operation is performed on U1000 by enabling U1000 with a low on pin 19 during the time that pin 1 is also low.

Pin 8 of U1000 is used for placing the operating system in the signature analysis (SA) mode. The CAL mode (pin 6) is not used. Pin 8 of U1000 is normally high; it is pulled low by relocating P1100 and grounding pin 7 of U1100.

The microprocessor can be placed in a forced instruction mode by relocating P1212 so that pin 1 of J1212 is grounded. This action disables the internal data bus, the external data bus, and the microprocessor's internal RAM. Relocating P1212 allows the bases of Q1200B and Q1200C to both go high, turning these transistors on and pulling down on pins 6 and 8 of U1000.

After P1212 has been positioned on J1212 for the forced instruction mode, it is necessary to set S1000 so that the TC (message terminator) switch is open (high = 1) and all others closed (low = 0). This places hexidecimal code 01 on the microprocessor data bus (D0–D7). With the internal data bus, external data bus, and the microprocessor's internal RAM disabled, the microprocessor will always read hexidecimal code 01 on its data port. This is a NOP (no operation) code that tells the microprocessor to advance its internal program counter by one count. This causes the microprocessor to address all locations in the total memory space indefinitely, in a sequential manner. The internal address buffers and the control line buffers are enabled during this operation. As a result, all of the address select lines to the memory devices (except for pin 1 of U1013, schematic 3) are exercised when that devices address appears on the address bus. The microprocessor never performs a write operation on any memory device while in the forced instruction mode.

GPIB Control Circuits ◇5

NOTE

For more detailed information on the internal operation of the GPIB Control IC (U1003), refer to the manufacturer's data sheet for more detailed information.

Integrated circuit U1003 performs the interface function between the microprocessor and the digital interface specified in IEEE Standard 488-1978. The handshake process for the DAV, NRFD, and NDAC lines on the digital interface is handled automatically within U1003. The IC is selected by a low level on pin 3 for all addresses in the 00C0–00C7 range. See Table 5-2.

Communication between U1003 and the microprocessor is via the internal data bus (IBD0–IBD7) and fourteen internal memory-mapped registers. The logical state of the three least significant bits (IBA0, IBA1, and IBA2; pins 6, 7, and 8) determine which internal register is selected. A read operation clocks data out of an internal register back to the microprocessor and a write operation clocks data into an internal register. For a read operation on U1003, pins 4 and 5 will be high; for a write operation, pins 4 and 5 will be low. Data is transferred in both directions on the positive edge of the clock signal on pin 18. Reading and writing to the same address will not access the same register within U1003 because they are "read only" or "write only" registers. Internal register select coding is shown in Table 5-5.

Table 5-5
U1013 INTERNAL REGISTERS

Register Select Code			Description	
RS0 (IBA0)	RS1 (IBA1)	RS2 (IBA2)	Read Only (pins 4 and 5 high)	Write Only (pins 4 and 5 low)
0	0	0	Interrupt Status 0	Interrupt Enable 0
0	0	1	Interrupt Status 1	Interrupt Enable 1
0	1	0	Address Status	Auxiliary Command
0	1	1	Bus Status	Address Register
1	0	0	Address Switch 1	Serial Poll
1	1	0	Command Pass Through	Parallel Poll (not used)
1	1	1	Data Input	Data Output

When U1003 detects the IEEE 488 talk or listen address for the MI 5010, it responds by entering the required addressed state and generates a low-true interrupt signal on pin 9. Interrupts to the microprocessor are generated by the following basic events:

- A data byte has been received.
- Ready to accept the next (or first) data byte.
- The Group Execute Trigger <GET> message has occurred.
- Device Clear Active State (DCAS) has occurred.
- My talk or listen address has been received.
- A Serial Poll Active State (SPAS) has occurred with bit 7 set in the serial poll register.

The buffered trigger signal on pin 2 of U1101A and pin 39 of U1003 can be generated in one of two ways, either by the GET message over the IEEE 488 digital interface or by a forced GET command from the microprocessor. This output from U1003 goes to a selected card via the external bus.

The talk enable (TE) output on pin 21 of U1003 controls the direction of data byte transfer through bidirectional bus transceiver U1001 and direction of signal flow through line transceiver U1002. When pin 21 is high, data byte transfer is out to the IEEE 488 digital interface; when low, data byte transfer is input to U1003. None of the $\overline{CE}$, $\overline{TE}$, or $\overline{SYS}$ signal outputs on P1005 are connected to the IEEE 488 digital interface.

Integrated circuit U1001 contains active pull-up components for fast recovery of the changing data lines. The normal operating mode for U1001 is with pin 11 at a high level. However, the IEEE 488 standard requires that the data lines go to an open-collector state for a parallel poll. When both EOI and ATN lines on the digital interface are asserted low true, pin 11 of U1001 goes high, disabling the internal active pull-up components. Pin 11 returns to the high state at the end of a parallel poll. The MI 5010 does not respond to parallel poll messages from the IEEE 488 digital interface.

NOTE

Refer to IEEE Standard 488-1978 for complete definitions and detailed descriptions of the three data byte handshake lines (DAV, NDAC, NRFD), the five bus management lines (REN, IFC, ATN, EOI, SRQ), and the eight data bus lines (DIO1–DIO8). The standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017.

Main Interconnect and Bus Extension ◇6◇7

The MI 5010 and MX 5010 have identical Main Interconnect boards (schematic 6). When the MX 5010 is electrically connected to the MI 5010 via P1001 (schematic 6) and J1001 (Bus Extension, schematic 7), identical signals appear on the MX 5010 Main Interconnect board. Since the MI 5010 and MX 5010 have identical power supplies, there is no Bus Extension connection via J1003 (P1003) on schematic 6.

POWER SUPPLY CIRCUIT BOARDS

+5 V Power Supply ◇8

Introduction. The power supply circuit for the MX 5010 is identical to the MI 5010 power supply circuit; the circuit boards are directly interchangeable with no changes to either board. Each power supply contains the following circuits:

- +5 V voltage regulator.
- Active current balance.
- Foldback current limit.
- Overvoltage crowbar.
- System reset and under-voltage.
- Line sync time base (LSTB).

Voltage Regulator. The voltage regulator circuit is composed of a +2.5 V reference (U1100), npn driver transistors (Q1210 and Q1212), two series-pass transistors in the power module, and associated components. The input to the regulator is the +8 V on pins 2A and 2B of P1420. The +5 V Lgc Sply voltage is remotely sensed at the far end of the distribution system (P1003, pins 8, 9, 10, and 11). Resistors R1310 and R1311 (3.6 Ω each) complete the regulator loop if the power supply board is removed for troubleshooting. Diode CR1320 conducts under reverse voltage conditions.

The +2.5 V reference on pin 2 of U1100 is applied to the non-inverting input of U1110C (pin 10), while the +5 V Sense input on pin 9 is divided down by the voltage divider ratio of R1100 and R1101 (ratio = 2.02). If the reference voltage remains at +2.5 V, the output voltage where the sense line connects will be 2.5 (2.02) or 5.05 volts. The output will remain within 2% of this value from no load up to the current limit threshold of about 5.5 A.

Active Current Balance. The current balance circuit is composed of R1222, R1324, the two series-pass transistors, differential transistor pair (Q1223A and B), R1225, and R1210. This circuit compares the current flowing in R1222 and the pnp series-pass transistor with the current flowing in R1324 and the npn series-pass transistor. The difference voltage between TP1300 and TP1301 is applied to transistor pair, Q1223A and Q1223B. Resistor R1225 provides a relatively constant current that is shared by the transistor pair.

If the current flowing in R1222 is greater than that flowing in R1324, the collector current of Q1223B will increase, pulling the base of Q1210 negative with respect to the base of Q1212. This reduces the current in the pnp series-pass transistor and restores the current balance. The current through the series-pass transistor is maintained within 15% of one-half the total load current at full load.

Foldback Current Limit. The foldback current limit circuit is composed of integrated circuits U1110D, U1110A, U1110B, and associated components. Foldback current limiting is achieved by sensing the voltage drops across R1222 and R1324. Pin 5 of U1110B and pin 3 of U1110A are referenced to +2.5 V, while pin 12 of U1110D is referenced to +8 V through R1218. The output voltage from pin 14 of U1110D corresponds to:

$$\left[\left(\frac{-.025I_1 - .025I_2}{2\text{ k}}\right)\quad(-56.2\text{ k})\right]\quad +8\text{ V}$$

where $I_1 + I_2$ is the total load current.

At start up, with the load current below the threshold limit, pin 7 of U1110B will go positive until CR1015 is forward biased. Current then flows through CR1015 and R1010 to ground until the IR product raises pin 6 of U1110B to + 2.5 V. Under this condition CR1016 will not conduct and no current limiting takes place.

However, if the output current reaches the threshold limit of about 5.5 A, the voltage on pin 14 of U1110D goes to about +11.9 V. This causes sufficient current to flow through R1110 and R1010 to maintain pin 6 of U1110B slightly above +2.5 V without any current from CR1015. At this point CR1015 cuts off, opening the loop around U1110B and causing pin 7 to go negative. When pin 7 goes negative, CR1016 becomes forward biased, allowing current to flow through R1102 and R1103 and reducing the reference voltage level on pin 10 of U1110C. The voltage regulator circuit then responds by reducing the output voltage until the load current stablilizes at or below the threshold value. During this current limiting condition, the voltage regulator and the current limiting circuitry are in series within a single loop. Capacitor C1015 provides a dominant single-pole frequency compensation for this loop.

Under short-circuit conditions, where the fault impedance is low enough to force the output voltage to be much lower than +5 V, the voltage drops across the series-pass transistors may become great enough to cause excessive power dissipation.

To prevent excessive power dissipation, U1110A inverts the difference between the +5 V Sense level and +2.5 V. Pin 1 of U1110A is at 0 V when the +5 V Sense line is at +5 V. If the +5 V Sense line falls to +2.5 V, the output of U1110A rises to +2.5 V; if the Sense line falls to 0 V, the output rises to +5 V. The output of U1110A is inverted by U1110B. When pin 6 of U1110B goes positive, pin 7 goes negative.

A falling voltage level on the +5 V Sense line lowers the nominal reference voltage level on pin 10 of U1110C and reduces the drive to the series-pass transistors. The result is that the output current folds back with decreasing output voltage. The short-circuit current limit range is between .2 A to 1.1 A at, or near, 0 V.

Over-Voltage Crowbar. Over-voltage protection is provided by applying a voltage proportional to the +5 V Lgc Sply via R1116 and R1117 to pins 2 and 3 of U1120. If the output voltage rises to +6 V, SCR Q1120 will fire and pull the +8 V supply line down to near 0 V. Either the fuse F1220 will open or the power module will go into over-current shutdown.

System Reset and Under-Voltage Restart. Differential transistor pair, Q1200A and Q1200B, compare the +2.5 V reference with the output of a voltage divider (R1201 and R1203) connected to the + 5 V Sense line. If the + 5 V Sense line is above 4.8 volts, Q1200A will carry all of the current flowing in R1202. The collector of Q1200B will be near +8 V, and VR1200 will be conducting with pin 1 of U1300C near 3 V. Zener diode VR1207 will be conducting with about +5 V on the collector of Q1200A.

The PWR signal from the power module (P1420, pin 6B) remains low for about 0.5 seconds after the +8 V supply is fully up and then goes high. During the low level period of the PWR signal, the high level on the base of Q1300 causes it to conduct current through VR1200 and Q1200C. This holds pin 1 of U1300C low and C1301 charges through CR1300, increasing the base voltage of Q1200D until Q1200E saturates and pulls down on the RESET line to the microprocessor and function cards (P1003, pin 12). If pin 1 of U1300C remains low for at least 1 microsecond, C1301 stores sufficient charge to keep Q1200E saturated for more than 10 microseconds, or more than 10 clock cycles. When the PWR signal from the power module goes high Q1300 cuts off and the voltage level on pin 1 of U1300C rises to about 3 V. This cuts off CR1300, C1301 discharges through R1301 and Q1200E cuts off, allowing the RESET line to go to a high state. The microprocessor fetches its first instruction word from ROM when it sees the RESET line go high.

The system reset switch, S1001, turns off Q1200A when pushed. This causes Q1200B to then carry all of the current in R1202 and sets a low on pin 1 of U1300C. The RESET line is then asserted (as described previously) to restart the system. See Fig. 5-2 for RESET signal timing.

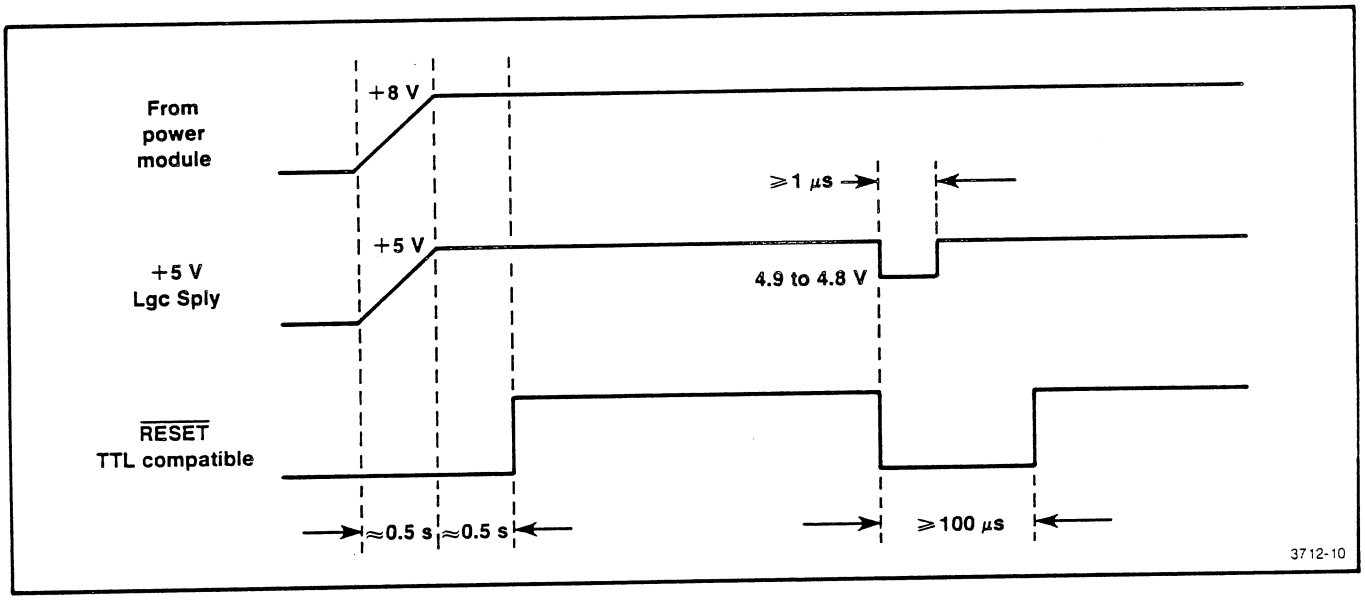

Fig. 5-2. $\overline{\text{RESET}}$ signal timing.

If the +5 V Sense line falls below 4.8 V (an under-voltage condition) all of the current in Q1200A switches to Q1200B and the emitter of Q1200C goes to about 3 V. This again cuts off VR1200, sets a low on pin 1 of U1300C and forces a valid restart signal via Q1200E.

Line Sync Time Base. The LSTB signal is produced by squaring the 26 V rms ac signal from the power module (P1420, pin 1B) and dividing it down to one-tenth the power line frequency. Resistors R1325 and R1326 operate as current limiters. Zener diode VR1320 clips the input waveform and U1300F operates as a Schmitt-trigger inverter, producing TTL compatible rise times and levels on pin 6 of U1302. Integrated circuit U1302 operates as a decade counter, producing a 50% duty cycle square wave on pin 1 of P1003.

MAINTENANCE AND DIAGNOSTICS

GENERAL MAINTENANCE

INTRODUCTION

Static-Sensitive Components

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 6-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic suction type or wick type desoldering tools.

Table 6-1
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a] **Voltage equivalent for levels:**

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V(est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

Cleaning

This instrument should be cleaned as often as operating conditions require. Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. Remove dirt that remains with a soft cloth dampened in a mild detergent and water solution. Do not use abrasive cleaners.

CAUTION

To clean the front panel use freon, isopropyl alcohol, or denatured ethyl alcohol. Do not use petroleum based cleansing agents. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air (approximately 5 lb/in^2) or use a soft brush or cloth dampened with one of the following cleaning solutions:

1. A 20:1 solution of distilled water and Kelite Spray White[1]. Flush cleaned area well with clean isopropyl alcohol.

2. A phosphate-free, pH normal detergent and water solution. Flush cleaned area well with distilled water, then with clean isopropyl alcohol.

3. Isopropyl alcohol. Flush the area with clean isopropyl alcohol.

Hold the board so the cleaning residue runs away from the connectors. Do not scrape or use an eraser to clean the edge connector contacts. Abrasive cleaning can remove the gold plating.

CAUTION

Circuit boards and components must be dry before applying power.

Drying can be accomplished by placing boards in an oven at 40°C to 60°C for approximately four hours.

[1]**Allied-Kelite Products Division of the Richardson Co., Los Angeles, California.**

Obtaining Replacement Parts

Electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, it may be possible to obtain many of the standard electrical components from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., check the Replaceable Electrical Parts list for the proper value, rating, tolerance, and description.

NOTE

When selecting replacement parts, remember that the physical size and shape of a component may affect its performance in the instrument.

Some parts are manufactured or selected by Tektronix, Inc., to satisfy particular requirements or are manufactured for Tektronix, Inc., to our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine the manufacturer, refer to the Replaceable Parts list and the Cross Reference index, Mfr. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type and option number.

2. Instrument serial number.

3. A description of the part (if electrical, include complete circuit number).

4. Tektronix part number.

Soldering Techniques

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts. General soldering techniques which apply to maintenance of any precision electronic equipment should be used when working on this instrument. Use only 60/40 rosin-core, electronic grade solder. The choice of soldering iron is determined by the repair to be made.

CAUTION

All circuit boards in this instrument are multilayer boards with a conductive path laminated between the top and bottom board layers. All soldering on this board should be done with extreme care to prevent breaking the connections to this conductive path.

When soldering on circuit boards or small wiring, use only a 15 watt, pencil type soldering iron. A higher wattage soldering iron can cause the etched circuit wiring to separate from the board base material and melt the insulation from small wiring. Always keep the soldering iron tip properly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to remove the component or to make a good solder joint. To protect heat sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint. Use a solder removing wick to remove excess solder from connections or to clean circuit board pads.

Integrated Circuits

To remove in-line integrated circuits use an extracting tool. This tool is available from Tektronix, Inc.; order Tektronix Part Number 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid disengaging one end before the other end.

Circuit Board Removal

To remove the circuit boards from the MI 5010 or MX 5010, remove the back panel. See Fig. 6-1. Remove the two screws at the top of the panel and the two fasteners at the bottom, using a 3/16 in. wrench. On both instruments, remove the power supply board screw at the top of the instrument shown in Fig. 6-2 and the power supply board screw at the bottom of the instrument shown in Fig. 6-3. If the instrument is an MI 5010, remove the two screws holding the Microprocessor board to the bottom of the instrument. The circuit boards and the back panel slide out the rear of the instrument. Unplug the Microprocessor board or the Power Supply board from the Main Interconnect board. To remove the Main Interconnect board, remove the six screws shown in Fig.6-4.

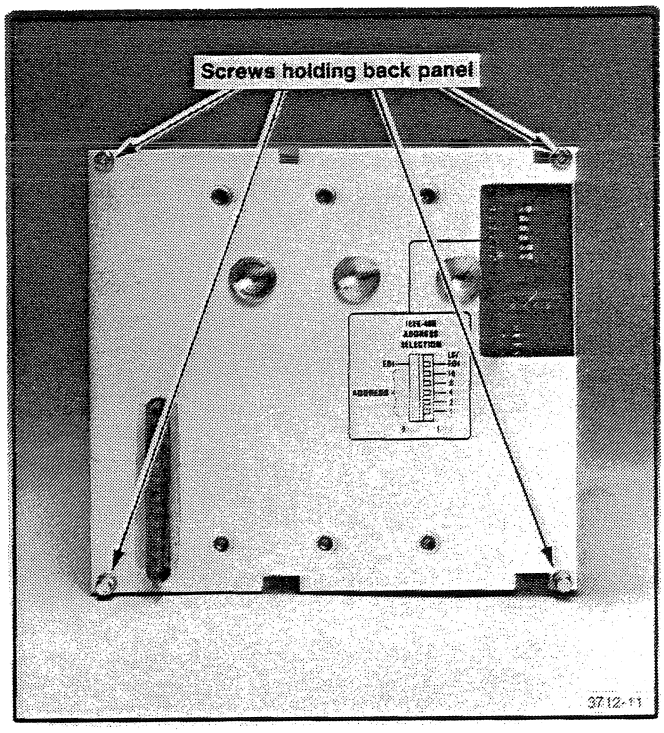

Fig. 6-1. Rear view of MI 5010. MX 5010 is similar.

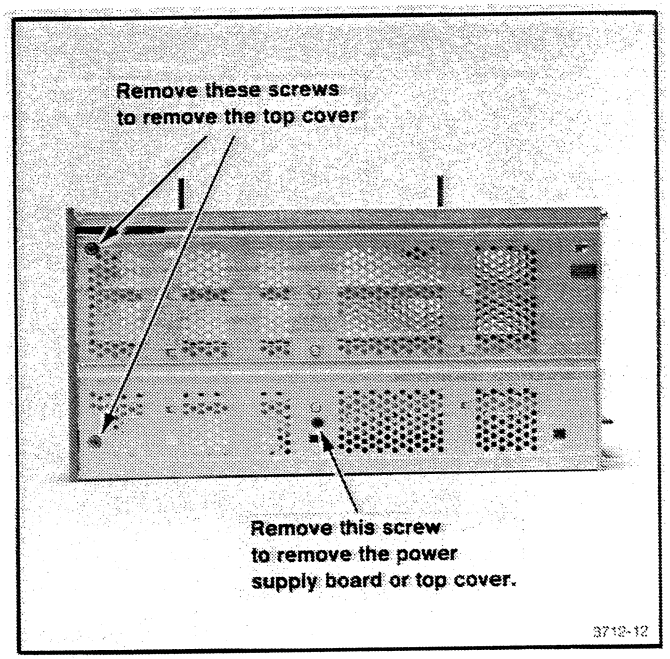

Fig. 6-2. Top view of MI 5010 or MX 5010.

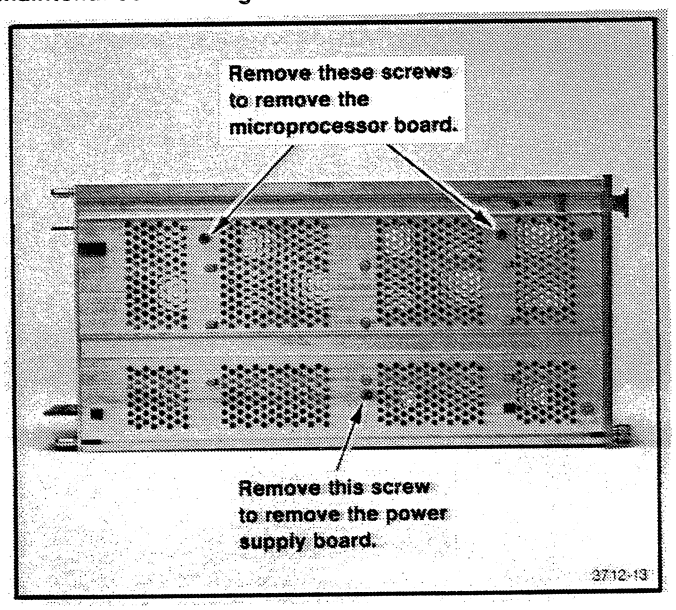

Fig. 6-3. Bottom view of MI 5010 or MX 5010.

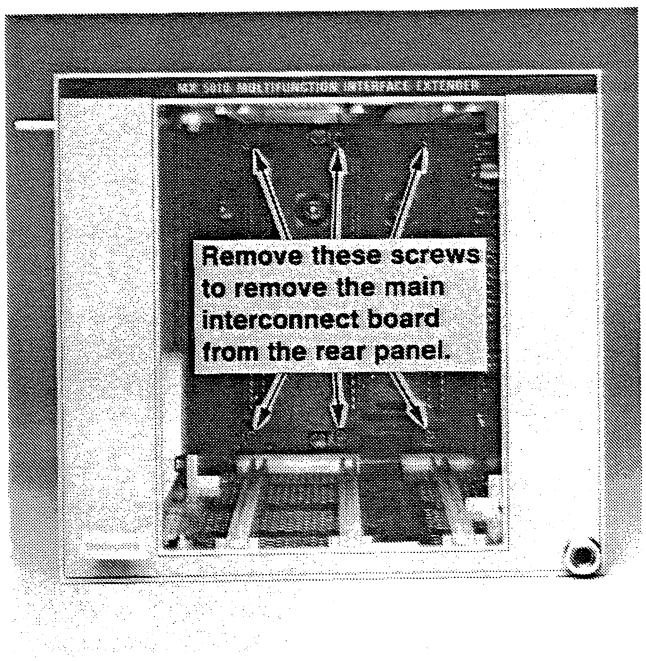

Fig. 6-4. Mounting of Main Interconnect boards to rear panels.

DIAGNOSTICS

INTRODUCTION

Overview

Troubleshooting the Power Supply board is straight forward. Review the Theory of Operation section for an understanding of the circuit operation. The software checkout procedures located in the Performance Check section of this manual may aid the diagnostic procedure. The Service Display (DS1216), located on the Microprocessor board may give clues as to the difficulty. See Table 6-2. The SA 501 signature analyzer setups and signatures are provided in the pullout pages at the rear of this manual. A troubleshooting example using signature analysis is also included in the following paragraphs.

Service Display Codes, DS1216

Upon power-up, the instrument goes through a self-test routine. If the self-test routine is completed with no errors, a .0. appears in the DS1216 display. This display is located in the lower right corner of the Microprocessor board. The relative brightness of the two decimal points indicates the duty cycle of the clock waveform. Both decimal points should be approximately the same brightness. This indicates the clock waveform is approximately at a 50% duty cycle. The rightmost decimal point will be illuminated with the RESET line is high.

During the self-test routine, if the microprocessor (U1111) internal RAM is defective, a 5 is displayed by DS1216. At this point, the MI 5010 halts operation. The ERROR and ADDRESSED indicator lights should remain on.

The next check performed is system RAM, U1201. If this test fails, a 4 is displayed by DS1216. Execution is halted and the front panel ERROR and ADDRESSED lights are illuminated.

The next step is a ROM check; the E0 ROM, U1200, and the F0 ROM, U1103, are checked. If one or more of the E0 ROM sections fail the test, a 1 is dispiayed; if the F0 ROM

fails, a 2 is displayed. If both fail the tests, a 3 is displayed. At this point the execution halts in a loop accessing each section. The ERROR and ADDRESSED lights are on.

The peripheral registers are checked next. If the GPIB IC, U1002, is missing, a 6 is displayed. If the VIA (Versatile Interface Adapter), U1213, is missing a 7 is displayed. If these IC chips are not present, execution halts. An F is displayed if the power-up routine is not completed and the error is not determined as above, or the unit is in the forced instruction mode.

Assuming all tests are passed, the kernel is verified, the GPIB IC is initialized, and power-on SRQ is asserted.

Table 6-2
SERVICE DISPLAY CODE (DS1216)

Displayed Digit	Associated Problem
0	No errors, self-test completed
1	E0 ROM (U1200)
2	F0 ROM (U1103)
3	E0 and F0 ROMs
4	System RAM (U1201)
5	Internal RAM (U1111)
6	GPIB (U1002) missing
7	VIA (U1213) missing
F	Self-test not completed, or in forced instruction mode

SIGNATURE ANALYSIS

Introduction

Four test modes, using signature analysis as a troubleshooting method, are available to aid in locating faults on the Microprocessor board.

- Signature analysis mode using internal clock (SA, INT CLOCK).
- Forced instruction mode using internal clock (FI, INT CLOCK).
- Signature analysis mode using external clock (SA, EXT CLOCK).
- Forced instruction mode using external clock (FI, EXT CLOCK).

The signature test modes, setups, and associated signature lists are found on a foldout page at the rear of this manual. Test mode verification procedures (notes) are listed in this section.

Test Mode Selection Guide

Assuming that the fault exists on the Microprocessor board, use the following information as a guide in selecting a particular test mode. Refer to test mode setups and associated list of signatures in the foldout pages.

Step A —Place the instrument in the SA, INT CLOCK mode. If this mode is entered properly (verified) and the problems not solved, go to Step C. If this mode cannot be entered, go to Step B.

Step B —Place the instrument in the FI, INT CLOCK mode. If this mode cannot be entered the trouble is probably in U1111, U1000, U1014, U1110, U1012, or in the circuitry associated with the forced instruction mode jumper, P1212/J1212.

Step C —Place the instrument in the SA, EXT CLOCK mode. If this mode cannot be entered, go to Step D. Also go to Step D if the problem cannot be solved in this mode.

Step D —Place the instrument in the FI, EXT CLOCK mode. If this mode cannot be entered, refer to Step B for possible troubles. If the instrument still does not enter the FI, EXT CLOCK mode, or if the mode is entered and the problem still not solved, digital troubleshooting methods other than signature analysis must be used.

NOTE

*Signal names are ordered in an alphabetical (or alphanumeric) format in the signature lists and match the signal nomenclature on the schematic diagrams. The signature for a particular signal name (***depending on which test mode the instrument is in***) will be valid anywhere that signal line (name) goes to on the board.*

Test Mode Verification Procedures

NOTE

Refer to Test Mode Setup table on foldout page.

Note 1: Insert any known good function card in MI 5010, slot 2. Both function card front panel indicator lights on. ADDRESSED and ERROR indicator lights on at one-half brightness. Service Display (DS1216) reads ".0".

Note 2: Connect FG 502 square-wave output to oscilloscope input, trigger output to counter input. Use oscilloscope and counter to set a TTL square-wave clock output waveform as illustrated on the foldout page, then connect FG 502 output to J1214-18.

Note 3: ADDRESSED and ERROR indicator lights on. Service Display (DS1216) reads "F". If you are uncertain about entry into this mode, perform the following steps:

a. Use SA 501 logic probe to verify that the following component pin numbers are toggling:

U1211-7, 9, 10, 11, 12, 13, 14, and 15

U1212-4, 5, 6, 7, 11, and 15

b. Check the following pin numbers for a TTL high:

U1211-6

U1212-12, 14

c. Check for a TTL low at the bottom of R1112. If all parts of steps a, b, and c are true, the instrument is in the FI mode. If any part is not true, perform the next steps.

d. Recheck for a TTL low at the bottom of R1112.

e. Check for the following conditions:

U1111-3; D0 must be at a TTL high.

U1111-32, 31, 30, 29, 28, 27, and 26; D1 through D7 must be at a TTL low.

f. If steps d and e are true, the instrument is in the FI mode; use the appropriate FI mode signature list. If step d or e is not true, the instrument is not in the FI mode; the trouble is in (or related to) U1111, U1000, U1014, U1110, or U1012.

FI/SA Mode Comparison

The FI modes are limited use modes intended to locate certain types of problems where the SA modes prove inadequate or useless. The types of faults where the FI modes are best suited involve the microprocessor, the address, data and control buffers, and to a lesser degree, the decoder circuits. The difficulty in using the FI modes is the verification of mode entry.

The SA modes are the easiest to enter and verify. Once entered, these modes yield more information about the microprocessor board as a whole. These modes cover most of the devices and circuits on the board; therefore, they are the logical starting points to locate most faults. The major areas where the SA modes are of little value are:

1. Where the SA mode depends on a circuit or device to run the SA routine; for example, certain ROM, microprocessor, or buffer faults.

2. Where the fault is directly or indirectly related to the microprocessor phase two ($\phi 2$) that also clocks the signature analyzer.

3. Where the Signature Analysis Test Point flip-flop (U1216A) fails to generate the Start/Stop pulses for the signature analyzer.

The external clock modes (FI or SA) will, in most cases, locate the faults involving the microprocessor phase two ($\phi 2$) clock or its derivatives. The choice of which external clock mode to use is based on the criteria discussed above.

Troubleshooting (All Modes)

Troubleshooting procedures using signature analysis is very similar to signal tracing in analog circuitry. Where a defective component in an analog circuit will cause the output voltage or waveform to be incorrect, a defective component in digital circuits will cause an incorrect signature. The troubleshooting procedure is as follows.

1. The observable symptoms should give you an indication of the area (block) that is causing the trouble. If so, follow steps 2 through 4 for that area. If not, follow steps 2 through 5 for the entire instrument.

2. Check for correct signatures at the important output point(s) of the block or device.

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3. If the signatures are good at the given output(s), it is not necessary to check for correct signatures at the input(s). If the signature is incorrect at an output, then check all inputs to that block. Ignore signal paths to an input that checks good. Trace back only from the point that had the incorrect signature.

4. Check the source point for a given signal path having the incorrect signature. If the source point signature is correct, the trouble must be between the source point and the last incorrect signature point. Try to find a common point with a number of inputs. If the common point signature is correct, all of the inputs and circuitry along those input paths are good.

5. Repeat steps 3 and 4 until you reach a block (device) where all inputs are good and the output is bad; the trouble must be in, or related to, that block.

Troubleshooting Example

This troubleshooting example is intended to be used as a guide to aid the service technician in gaining familiarity and experience with both the instrument and signature analysis procedures.

It is suggested that this example be studied at least once in order to become acquainted with the test modes, setups, and signature lists located in the foldout pages of this manual.

The steps in this example may not appear to be ordered in a manner logical troubleshooting would indicate. There may be steps included (or excluded) that seem inappropriate at a given point. This example attempts to cover all of the items a given test mode can adequately check. In this way the example, although dealing with one particular fault, becomes a useful aid in locating other faults that may be encountered.

Depending on the symptoms that another fault produces, the service technician may use the steps in whatever order that would be appropriate for that unknown fault.

The following test equipment was used for this troubleshooting example:

Test Equipment	Example
Signature Analyzer	TEKTRONIX SA 501
Oscilloscope	TEKTRONIX SC 502
Function Generator	TEKTRONIX FG 502
Universal Counter/Timer	TEKTRONIX DC 503A
Shorting Jumper, 4 inches	Obtain locally

The signatures in the individual signature lists are arranged alphabetically (or alphanumerically) by signal names that correspond to the signal line nomenclature on the schematics. For some cases in this example, certain signal names are not spelled out for the signal node being checked. In those cases, the functional block diagram and schematics must be used as supplemental tools to identify the signal name.

To identify an unknown signal name in this example, locate the specific signal node (pin number, etc.) on the associated schematic diagram and note the signal name going to and from that node. Then look up the signal name in the appropriate signature list **(depending on which mode the instrument is in)**. The signature for a particular signal line (name) will be valid anywhere that signal line goes to on the board.

NOTE

For this example, the instrument completed the power-up self-test routine but failed to operate properly over the IEEE 488 digital interface. The SA, INT CLOCK mode was entered and verified according to Note 1 in the Test Mode Verification Procedures. The following procedural steps were then followed.

1. Check the signatures for all test points (TP numbers) listed for the SA, INT CLOCK mode. No wrong signatures were found.

2. Check the device-enable pins on the following components:

System RAM (U1201), pin 18.

System ROM (U1103 and U1200), pin 18.

VIA (U1213), pins 23 and 24.

GPIB (U1003), pin 3.

Card Select Latch (U1013), pin 1.

All signature checks were correct.

3. Check the microprocessor (U1111) for correct signatures on all pins. All microprocessor signatures listed for SA, INT CLOCK mode were correct.

4. Check the internal address bus, IBA0 through IBA15, on U1112 and U1115. All address signatures at this point were correct.

5. Check the internal data bus, IBD0 through IBD7, on U1014 for signatures. All internal data bus signatures at this point were correct.

NOTE

The preceding steps have checked the address, data, and clock signals at their source and checked all of the buffered address and data lines used on the Microprocessor board.

6. Check the internal data bus signatures at the RAM (U1201) and ROM (U1103, U1200). These signatures will be the same as previously checked in step 5 if circuit board runs are not faulty. All signatures were correct.

7. Check the internal address bus signatures at the RAM (U1201) and ROM (U1103, U1200). This again checks for faulty circuit board runs. All signatures were correct.

8. Check the WE control line signature for the RAM and ROM; pin 21 on U1201 and pin 20 of U1103 and U1200. Signatures were correct.

9. Check Card Select Latch (U1013) outputs, CSEL 0 through CSEL 6 and CSEL EXP. If any of these outputs are incorrect, check the inputs to U1013 (IBD0 through IBD7, CLK, and ENBL). For this example, all signatures were correct.

10. Check five output lines from U1003 (GPIB):

DI01, pin 38.

DI08, pin 31.

EOI, pin 27.

TE, pin 21.

SRQ, pin 29.

Signatures were correct for this example.

NOTE

These are the only functional lines in the SA modes. They are not functional in the FI modes.

11. Check the following signatures at the GPIB buffers:

U1001, pins 2 and 9 (DI01 and DI08).
U1002, pins 7 and 9 (EOI and SRQ).

These signatures should be the same as checked for U1003. Signatures were correct. If any of these signatures are bad, check the data inputs and control lines for wrong signatures.

12. Check Address/Service Switch buffer, U1000. Use the SA 501 logic probe function to check the TC, 16, 8, 4, 2, 1 inputs to A1 through A6 and the D0 through D7 (Y1 through Y6) outputs of U1000. Each lever switch, when closed, sets a low level on both the associated input and output of U1000. For this example, all switches operated properly.

13. Check the PA0 through PA7 and PB0 through PB7 lines at the VIA (U1213). In the SA, INT CLOCK Signature List these lines are listed as PA (n) and PB (n), where n = 0 through 7.

Signatures were correct for this example.

NOTE

All signatures that can be checked in the SA, INT CLOCK mode have been checked as correct.

14. Place the instrument in the SA, EXT CLOCK mode and make certain that this mode is entered (verified). See Note 1 in Test Mode Verification Procedures.

NOTE

The FI, INT CLOCK mode was skipped because the instrument was able to run in the SA, INT CLOCK mode.

15. Check all of the test point (TP numbers) signatures listed for the SA, EXT CLOCK mode. For this example the following results were noted:

Test Point	Should Be	Was
TP1101	C082	2F20
TP1112	8PCA	034C
TP1114	UPU6	UUCH

Proceed to the next step.

16. Check for correct signatures on the microprocessor (U1111) signal lines (names) listed for the SA, EXT CLOCK mode. For this example, the signatures were correct.

17. Check for correct signatures at the following signal nodes:

IBVMA (U1101B, pin 14).

B02 (U1101B, pin 5).

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$\overline{B02}$ (U1214D, pin 13). This is the complement of the signal on U1101B, pin 5.

02 (U1214D, pin 15).

All four signatures for this example were incorrect.

NOTE

This mode has produced too many bad signatures. If all or most of the signatures in a given mode are incorrect, then that mode is of little value in diagnosing the trouble. For this example, the procedure continues on to the next step.

18. Place the instrument in the FI, EXT CLOCK mode. Verify mode entry according to Note 3 in the Test Mode Verification Procedures. Check for correct signatures at the test points (TP numbers) listed for the FI, EXT CLOCK mode. For this example, all signatures were correct.

19. Check for correct signatures at the microprocessor pin numbers (names) listed for the FI, EXT CLOCK mode. All signatures were correct for this example,

20. Check all of the remaining signatures listed for the FI, EXT CLOCK mode. For this example there was only one bad signature; it was:

B02•IBVMA (U1101, pin 6)

Correct signature should be 0077, readout was 00UP.

21. Recheck signatures on both inputs to U1101B. The signatures were correct.

22. Conclusion:

Either U1101B is defective or the output is being loaded down.

23. Actions:

First, change the suspected component.

If the problem is still not solved, find out what is causing the output to be loaded down and fix it.

NOTE

The actual fault that existed for this example was that the buffered clock (B02) input, internal to U1101B, was floating high.

Rear Interface Information

A slot (cut out) exists between pins 6 and 7 on the rear interface power supply connector. The slot identifies the circuit board as belonging to the TM 5000-Series family. A corresponding barrier in the TM 5000 power module prevents non-compatible plug-ins from being inserted in the power module. See power module instruction manual for more information.

The rear interface connections to the power supply and the IEEE 488 (GPIB) digital interface are shown in Fig. 6-5 and Fig. 6-6, respectively.

POWER SUPPLY BOARD (A30 ASSEMBLY) P1420				
OUTPUT OR INPUT	PIN B		PIN A	OUTPUT OR INPUT
NOT USED	13		13	NOT USED
+26V DC	12	TM 5000 BARRIER SLOT	12	+26V DC
COLLECTOR OF PNP SERIES PASS	11		11	BASE LEAD OF PNP SERIES PASS
NOT USED	10		10	EMITTER LEAD OF PNP SERIES PASS
NOT USED	9		9	NOT USED
-26V DC	8		8	-26V DC
COLLECTOR OF NPN SERIES PASS	7		7	EMITTER LEAD OF NPN SERIES PASS
PWR SIG INPUT	6		6	BASE LEAD OF NPN SERIES PASS
NOT USED	5		5	NOT USED
ANALOG GROUND	4		4	ANALOG GROUND
DIGITAL GROUND	3		3	DIGITAL GROUND
+8V FILTERED DC	2		2	+8V FILTERED DC
LSTB GROUND (25V AC)	1		1	LSTB SOURCE (25V AC)

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Fig. 6-5. Rear view of MI 5010 and MX 5010 power supply interface connector.

MICROPROCESSOR BOARD (A20 ASSEMBLY) P1005				
OUTPUT OR INPUT	PIN B		PIN A	OUTPUT OR INPUT
DIO1	1		2	DIO5
DIO2	3		4	DIO6
DIO3	5		6	DIO7
DIO4	7		8	DIO8
$\overline{CE}$	9		10	$\overline{TE}$
EOI	11		12	IFC
DAV	13		14	SRQ
NRFD	15		16	ATN
NDAC	17		18	REN
NO CONNECTION	19		20	$\overline{SYS}$

NOTE:

THE FOLLOWING LINES ARE CONNECTED ONLY TO THE GPIB CONNECTOR. THEY ARE NOT DEFINED BY THE IEEE 488-1978 STANDARD, NOR ARE THEY CONNECTED TO THE DIGITAL INTERFACE.

$\overline{CE}$ (PIN 9) - FOR DEVICES THAT CAN BE OR LOOK LIKE CONTROLLERS.

$\overline{TE}$ (PIN 10) - OPEN COLLECTOR TALK CONTROL, LOW = TALK.

$\overline{SYS}$ (PIN 20) - FOR DEVICES THAT CAN BE SYSTEM CONTROLLERS.

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Fig. 6-6. GPIB connector pin assignments.

MI5Ø1Ø INTERFACE ASSIGNMENTS				
PIN FUNCTION	PIN A	TOP	PIN B	PIN FUNCTION
ANALOG GND	1		1	ANALOG GND
SPARE	2		2	SPARE
N/C	3		3	N/C
ANALOG GND	4		4	ANALOG GND
+26V	5		5	-26V
DIG GND	6		6	DIG GND
+8V	7		7	+8V
EBA Ø	8		8	EBA 1
EBA 2	9		9	EBA 3
EBA 4	1Ø		1Ø	EBA 5
EBA 6	11		11	EBA 7
EBA 8	12		12	EBA 9
EBA 1Ø	13		13	EBA 11
EBA 12	14		14	EBA 13
EBA 14	15		15	EBA 15
N/C	16		16	CSEL X (1,2,3)
N/C	17		17	N/C
SPARE	18		18	SPARE
INT DIS	19		19	RET TRIG
SPARE	2Ø		2Ø	BFR TRIG
SPARE	21		21	SPARE
EBR/W	22		22	BØ2
RESET	23		23	EBVMA
LSTB	24		24	EBINT
EBD Ø	25		25	EBD 1
EBD 2	26		26	EBD 3
EBD 4	27		27	EBD 5
EBD 6	28		28	EBD 7
+5V	29		29	+5V
DIG GND	3Ø		3Ø	DIG GND

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Fig. 6-7. P1001, P1002, and P1004 Rear Interface Assignments (MI 5010).

MX5010 INTERFACE ASSIGNMENTS				
PIN FUNCTION	PIN A	TOP	PIN B	PIN FUNCTION
ANL GND	1		1	ANL GND
SPARE	2		2	SPARE
N/C	3		3	N/C
ANL GND	4		4	ANL GND
+26V	5		5	-26V
DIG GND	6		6	DIG GND
+8V	7		7	+8V
EBA 0	8		8	EBA 1
EBA 2	9		9	EBA 3
EBA 4	10		10	EBA 5
EBA 6	11		11	EBA 7
EBA 8	12		12	EBA 9
EBA 10	13		13	EBA 11
EBA 12	14		14	EBA 13
EBA 14	15		15	EBA 15
N/C	16		16	CSEL X (4,5,6)
SPARE	18		18	SPARE
INT DIS	19		19	RET TRIG
SPARE	20		20	BFR TRIG
SPARE	21		21	SPARE
EBR/W	22		22	B02
RESET	23		23	EBVMA
LSTB	24		24	EBINT
EBD 0	25		25	EBD 1
EBD 2	26		26	EBD 3
EBD 4	27		27	EBD 5
EBD 6	28		28	EBD 7
+5V	29		29	+5V
DIG GND	30		30	DIG GND

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Fig. 6-8. P1001, P1002, and P1004 Rear Interface Assignments (MX 5010).

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

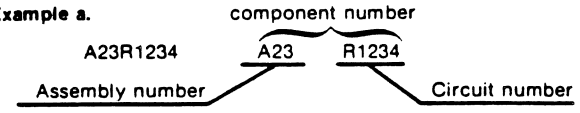
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

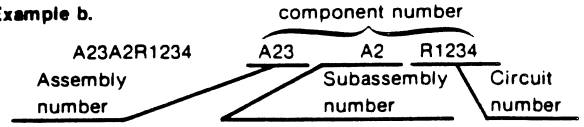
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00853	SANGAMO WESTON INC SANGAMO CAPACITOR DIV	SANGAMO RD P O BOX 128	PICKENS SC 29671
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPRESSWAY P O BOX 225012 M/S 49	DALLAS TX 75265
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR GROUP	5005 E MCDOWELL RD	PHOENIX AZ 85008
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP GOVERNMENT SYSTEMS DIV	600 W JOHN ST	HICKSVILLE NY 11802
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP SEMICONDUCTOR DIV	464 ELLIS ST	MOUNTAIN VIEW CA 94042
07716	TRW INC TRW ELECTRONICS COMPONENTS TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
14193	CAL-R INC	1601 OLYMPIC BLVD	SANTA MONICA CA 90404
15238	ITT SEMICONDUCTORS A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORP	500 BROADWAY P O BOX 168	LAWRENCE MA 01841
19701	MEPCO/ELECTRA INC A NORTH AMERICAN PHILIPS CO	P O BOX 760	MINERAL WELLS TX 76067
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051
32159	WEST-CAP ARIZONA	2201 E ELVIRA ROAD	TUCSON AZ 85706
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507
34576	ROCKWELL INTERNATIONAL CORP SEMICONDUCTOR PRODUCTS DIV	4311 JAMBOREE RD PO BOX C M/S 501-300	NEWPORT BEACH CA 92658-8902
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY	SECAUCUS NJ 07094
54583	TDK ELECTRONICS CORP	755 EASTGATE BLVD	GARDEN CITY NY 11530
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
57668	ROHM CORP	16931 MILLIKEN AVE	IRVINE CA 92713
59492	QUARTZTEK INC.	P.O. BOX 14738	PHOENIX, AZ 85063
71400	BUSSMANN MFG CO MCGRAW EDISION CO	114 OLD STATE RD PO BOX 14460	ST LOUIS MO 63178
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
81073	GRAYHILL INC	561 HILLGROVE AVE P O BOX 373	LA GRANGE IL 60525
91802	INDUSTRIAL DEVICES INC	982 RIVER ROAD	EDGEWATER NJ 07020
TK1015	MUSASHI WORKS OF HITACHI LTD	1450 JOSUIHON-CHO KODAIRA-SHI	TOKYO JAPAN

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	670-7200-00			CIRCUIT BD ASSY:MAIN INTERCONNECT (NO ELECTRICAL PARTS)	80009	670-7200-00
A12	670-7205-00			CIRCUIT BD ASSY:MI/MX INTERCONNECT (MX5010 ONLY-NO ELECTRICAL PARTS)	80009	670-7205-00
A20	670-7199-00			CIRCUIT BD ASSY:GPIB MICROPROCESSOR (MI5010 ONLY)	80009	670-7199-00
A30	670-7201-00			CIRCUIT BD ASSY:PWR SPLY	80009	670-7201-00
A10	670-7200-00			CIRCUIT BD ASSY:MAIN INTERCONNECT (NO ELECTRICAL PARTS)	80009	670-7200-00
A12	670-7205-00			CIRCUIT BD ASSY:MI/MX INTERCONNECT (MX5010 ONLY-NO ELECTRICAL PARTS)	80009	670-7205-00
A20	670-7199-00			CIRCUIT BD ASSY:GPIB MICROPROCESSOR (MI5010 ONLY)	80009	670-7199-00
A20C1000	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1001	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1002	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1003	290-0768-00			CAP,FXD,ELCTLT:10UF,+50-10%,100VDC	54473	ECE-A100V10L
A20C1004	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1005	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1010	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1011	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1012	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1100	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1101	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1102	283-0781-00			CAP,FXD,MICA DI:27PF,5%,500V	00853	D155E270J0
A20C1103	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1104	283-0781-00			CAP,FXD,MICA DI:27PF,5%,500V	00853	D155E270J0
A20C1105	283-0781-00			CAP,FXD,MICA DI:27PF,5%,500V	00853	D155E270J0
A20C1106	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1107	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1108	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1109	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	54583	MA12C0G1H271J
A20C1110	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1111	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1112	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1113	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1114	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1115	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1116	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1117	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1200	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1201	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1202	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1203	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1210	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1211	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1212	283-0422-00			CAP,FXD,CER DI:0.047UF,+80-20%,50V	04222	MD015E473ZAA
A20C1213	283-0421-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	MD015C104MAA
A20C1214	290-0804-00			CAP,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A20DS1200	150-1107-00			LT EMITTING DIO:RED,650NM,20MA	91802	5321F-1
A20DS1201	150-1107-00			LT EMITTING DIO:RED,650NM,20MA	91802	5321F-1
A20DS1216	150-1013-00			LAMP,LED RDOUT:RED,HEXADECIMAL W/LOGIC	01295	TIL 311
A20L1100	108-0317-00			COIL,RF:FIXED,15 UH	32159	71501M+10PERCENT
A20Q1200	156-0259-02			MICROCKT,LINEAR:5-XSTR ALL INDEPENDENT,SCRN	02735	CA3083EX-98
A20R1000	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A20R1001	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A20R1002	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25W	57668	NTR25J-E 100E
A20R1010	321-0249-00			RES,FXD,FILM:3.83K OHM,1%,0.125W,TC=TO	19701	5033ED3K83F

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20R1011	321-0281-00			RES,FXD,FILM:8.25K OHM,1%,0.125M,TC=T0	19701	5043ED8K250F
A20R1100	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A20R1101	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A20R1102	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A20R1103	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A20R1104	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A20R1105	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
A20R1106	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
A20R1107	315-0302-00			RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
A20R1108	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A20R1109	315-0105-00			RES,FXD,FILM:1M OHM,5%,0.25M	19701	5043CX1M000J
A20R1110	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A20R1111	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A20R1112	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A20R1115	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A20R1200	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A20R1201	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
A20R1202	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
A20R1204	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A20R1205	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A20R1209	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A20R1210	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
A20R1211	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
A20R1212	315-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.25M	57668	NTR25J-E02K7
A20R1214	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A20R1215	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A20R1216	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A20S1000	260-2064-00			SWITCH,ROCKER:(6)SPST,125MA,30VDC	81073	76YYXXXS
A20S1200	260-1421-01			SWITCH,PUSH:1 BTN,2 POLE,INSTRUMENT ID	80009	260-1421-01
A20TP1000	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1001	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1002	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1013	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1101	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1102	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1104	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1110	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1112	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1113	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1114	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1200	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1201	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1202	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1203	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1204	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1205	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1210	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1211	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1212	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20TP1213	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A20U1000	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1001	156-1414-01			MICROCKT,DGTL:TTL,OCTAL GPIB XCVR DATA BUS	01295	SN75160ANP3
A20U1002	156-1415-00			MICROCKT,DGTL:TTL,OCTAL GPIB XCVR MGT BUS	01295	SN75161A N
A20U1003	156-1444-00	B010100	B010289	MICROCKT,DGTL:GPIB ADAPTER	01295	TMS9914NL
A20U1003	156-1444-01	B010290		MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A (NL
A20U1010	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1011	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1012	156-1111-02			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N3

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20U1013	156-0913-02			MICROCKT,DGTL:OCTAL D FF W/ENABLE,SCRN	01295	SN74LS377NP3
A20U1014	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1100	156-0479-02			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A20U1101	156-0696-02			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND,SCRN	01295	SN74265N3/J4
A20U1102	156-0985-01			MICROCKT,DGTL:DUAL 5-INPUT NOR GATE	04713	SN74LS260NDS
A20U1103	160-1483-00			MICROCKT,DGTL:2048 X 8,EPROM,PRGM	80009	160-1483-00
A20U1110	156-1065-01			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	04713	SN74LS373 ND/JD
A20U1111	156-1342-00			MICROCKT,DGTL:NMOS,8 BIT M/CLOCK & RAM	04713	MC6802P
A20U1112	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1113	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	07263	74LS10PCQR
A20U1114	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	07263	74LS10PCQR
A20U1115	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A20U1116	156-0696-02			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND,SCRN	01295	SN74265N3/J4
A20U1117	156-0386-02			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	07263	74LS10PCQR
A20U1200	160-1484-00	B010100	B010221	MICROCKT,DGTL:2048 X 8,EPROM,PRGM	80009	160-1484-00
A20U1200	160-1484-01	B010222		MICROCKT,DGTL:4096 X 8 EPROM,PRGM	80009	160-1484-01
A20U1201	156-1594-00			MICROCKT,DGTL:NMOS,2048 X 8 SRAM	TK1015	HM6116P-3(DP-24)
A20U1210	156-1058-01			MICROCKT,DGTL:OCTAL ST BUFFER W/3 STATE OUT	01295	SN74S240JP4
A20U1211	156-0469-02			MICROCKT,DGTL:3/8 LINE DCDR	01295	SN74LS138NP3
A20U1212	156-0541-02			MICROCKT,DGTL:DUAL 2-TO 4-LINE DCDR/DEMUX	04713	SN74LS139NDS
A20U1213	156-1539-00			MICROCKT,DGTL:NMOS,6522,I/O PORT W/TIMER	34576	R6522AP
A20U1214	156-0696-02			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND,SCRN	01295	SN74265N3/J4
A20U1215	156-0396-02			MICROCKT,DGTL:QUAD 2-INP 3-STATE BFR SCRN	27014	DM8094NA+
A20U1216	156-0804-02			MICROCKT,DGTL:QUADRUPLE S-R LATCH	01295	SN74LS279NP3/JP4
A20M1200	131-0566-00			BUS,COND:DUMMY RES,0.094 OD X 0.225L	24546	OMA 07
A20Y1100	158-0256-00			XTAL UNIT,QTZ:4.000MHZ 0.0025% SER	59492	150-6070
A30	670-7201-00			CIRCUIT BD ASSY:PWR SPLY	80009	670-7201-00
A30C1014	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1015	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A30C1100	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1102	281-0770-00			CAP,FXD,CER DI:1000PF,20%,100V	04222	MA101C102MAA
A30C1104	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A30C1113	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1204	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1206	290-0217-00			CAP,FXD,ELCTLT:250UF,+75-10%,12V	00853	556DF251U012B
A30C1207	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1213	290-0743-00			CAP,FXD,ELCTLT:100UF,+50%-10%,16V	54473	ECE-B16V100L
A30C1220	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR302E105ZAATR
A30C1301	281-0772-00			CAP,FXD,CER DI:4700PF,10%,100V	04222	MA201C472KAA
A30C1310	290-0217-00			CAP,FXD,ELCTLT:250UF,+75-10%,12V	00853	556DF251U012B
A30C1319	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A30C1320	283-0203-00			CAP,FXD,CER DI:0.47UF,20%,50V	04222	SR305SC474MAA
A30CR1015	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1016	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1113	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1114	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1204	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1300	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V	03508	DA2527 (1N4152)
A30CR1320	152-0066-00			SEMICOND DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
A30F1210	159-0022-00			FUSE,CARTRIDGE:3AG,1A,250V,MEDIUM BLOW	71400	AGC-CM-1
A30F1220	159-0137-00			FUSE,CARTRIDGE:GLASS,8 AMP,32V,0.6 SEC	71400	AGC-CM-8
A30F1300	159-0022-00			FUSE,CARTRIDGE:3AG,1A,250V,MEDIUM BLOW	71400	AGC-CM-1
A30Q1120	151-0521-00			SCR:SI,MU-27	02735	C122B1
A30Q1200	156-0048-01	B010100	B011353	MICROCKT,LINEAR:5 XSTR ARRAY,INSP	80009	156-0048-01
A30Q1200	156-0048-00	B011354		MICROCKT,LINEAR:5 XSTR ARRAY (MI5010 ONLY)	02735	CA3046
A30Q1200	156-0048-01	B010100	B010379	MICROCKT,LINEAR:5 XSTR ARRAY,INSP	80009	156-0048-01
A30Q1200	156-0048-00	B010480		MICROCKT,LINEAR:5 XSTR ARRAY	02735	CA3046

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(MX5010 ONLY)		
A30Q1210	151-0460-00			TRANSISTOR:NPN,SI,TO-18	04713	2N3947
A30Q1212	151-0460-00			TRANSISTOR:NPN,SI,TO-18	04713	2N3947
A30Q1223	151-0353-00			TRANSISTOR:NPN,SI,TO-78	80009	151-0353-00
A30Q1300	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A30R1010	321-0242-00			RES,FXD,FILM:3.24K OHM,1%,0.125M,TC=TO	19701	5043ED3K240F
A30R1011	321-0305-00			RES,FXD,FILM:14.7K OHM,1%,0.125M,TC=TO	19701	5033ED14K70F
A30R1012	321-0258-00			RES,FXD,FILM:4.75K OHM,1%,0.125M,TC=TO	19701	5033ED4K750F
A30R1013	321-0258-00			RES,FXD,FILM:4.75K OHM,1%,0.125M,TC=TO	19701	5033ED4K750F
A30R1014	315-0333-00			RES,FXD,FILM:33K OHM,5%,0.25M	57668	NTR25J-E33K0
A30R1100	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125M,TC=TO	19701	5033ED1K00F
A30R1101	321-0194-00			RES,FXD,FILM:1.02K OHM,1%,0.125M,TC=TO	07716	CEAD10200F
A30R1102	321-0239-00			RES,FXD,FILM:3.01K OHM,1%,0.125M,TC=TO	19701	5043ED3K010F
A30R1103	321-0239-00			RES,FXD,FILM:3.01K OHM,1%,0.125M,TC=TO	19701	5043ED3K010F
A30R1104	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A30R1105	307-0107-00			RES,FXD,CMPSN:5.6 OHM,5%,0.25M	01121	CB56G5
A30R1106	321-0361-00			RES,FXD,FILM:56.2K OHM,1%,0.125M,TC=TO	07716	CEAD56201F
A30R1107	321-0193-00			RES,FXD,FILM:1K OHM,1%,0.125M,TC=TO	19701	5033ED1K00F
A30R1110	321-0289-00			RES,FXD,FILM:10.0K OHM,1%,0.125M,TC=TO	19701	5033ED10K0F
A30R1115	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A30R1116	321-0274-00			RES,FXD,FILM:6.98K OHM,1%,0.125M,TC=TO	19701	5043ED6K980F
A30R1117	321-0816-00			RES,FXD,FILM:5K OHM,1%,0.125M,TC=TO	24546	NA55D5001F
A30R1200	315-0204-00			RES,FXD,FILM:200K OHM,5%,0.25M	19701	5043CX200K0J
A30R1201	321-0162-00			RES,FXD,FILM:475 OHM,1%,0.125M,TC=TO	19701	5033ED475R0F
A30R1202	315-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.25M	57668	NTR25J-E06K8
A30R1203	321-0164-02			RES,FXD,FILM:499 OHM,0.5%,0.125M,TC=T2	01121	ADVISE
A30R1204	315-0562-00			RES,FXD,FILM:5.6K OHM,5%,0.25M	57668	NTR25J-E05K6
A30R1205	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
A30R1206	315-0202-00			RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
A30R1207	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25M	57668	NTR25J-E270K
A30R1208	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
A30R1210	315-0181-00			RES,FXD,FILM:180 OHM,5%,0.25M	57668	NTR25J-E180E
A30R1218	321-0361-00			RES,FXD,FILM:56.2K OHM,1%,0.125M,TC=TO	07716	CEAD56201F
A30R1219	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125M,TC=TO	19701	5033ED2K00F
A30R1222	308-0757-00			RES,FXD,MM:0.025 OHM,3%,5M	14193	SA50-R025H
A30R1223	321-0222-00			RES,FXD,FILM:2.00K OHM,1%,0.125M,TC=TO	19701	5033ED2K00F
A30R1225	303-0242-00			RES,FXD,CMPSN:2.4K OHM,5%,1M	01121	GB2425
A30R1300	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
A30R1301	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25M	57668	NTR25J-E270K
A30R1302	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
A30R1310	307-0111-00			RES,FXD,CMPSN:3.6 OHM,5%,0.25M	80009	307-0111-00
A30R1311	307-0111-00			RES,FXD,CMPSN:3.6 OHM,5%,0.25M	80009	307-0111-00
A30R1320	315-0221-00			RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
A30R1322	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
A30R1323	308-0643-00			RES,FXD,MM:0.10 OHM,3%,3M	14193	SA31 R100H
A30R1324	308-0757-00			RES,FXD,MM:0.025 OHM,3%,5M	14193	SA50-R025H
A30R1325	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A30R1326	315-0103-00			RES,FXD,FILM:10K OHM,5%,0.25M	19701	5043CX10K00J
A30S1001	260-0735-00			SWITCH,PUSH:T,NO CONTACT,RED BUTTON	81073	39-1
A30TP1100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1120	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1210	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1211	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1300	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1301	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1310	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1311	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30TP1315	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A30U1100	156-1173-00			MICROCKT,LINEAR:VOLTAGE REFERENCE	04713	MC1403U0S

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A30U1110	156-0495-02			MICROCKT,LINEAR:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A30U1120	156-1266-00			MICROCKT,LINEAR:OVERVOLTAGE SENSING CIRCUIT	04713	SC77113LH
A30U1300	156-0645-02			MICROCKT,DGTL:HEX INV ST NAND GATES	04713	SN74LS14NDS
A30U1302	156-0727-01			MICROCKT,DGTL:30 MHZ PRESETTABLE DECADE	01295	SN74LS196NP3
A30U1320	156-1150-00			MICROCKT,LINEAR:VOLTAGE REGULATOR,NEGATIVE	04713	MC79L05ACP
A30VR1110	152-0149-00			SEMICOND DVC,DI:ZEN,SI,10V,5%,0.4W,DO-7	15238	Z5406
A30VR1200	152-0278-00			SEMICOND DVC,DI:ZEN,SI,3V,5%,0.4W,DO-7	04713	SZG35009K20
A30VR1207	152-0278-00			SEMICOND DVC,DI:ZEN,SI,3V,5%,0.4W,DO-7	04713	SZG35009K20
A30VR1320	152-0195-00			SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4W,DO-7	04713	SZ11755RL

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

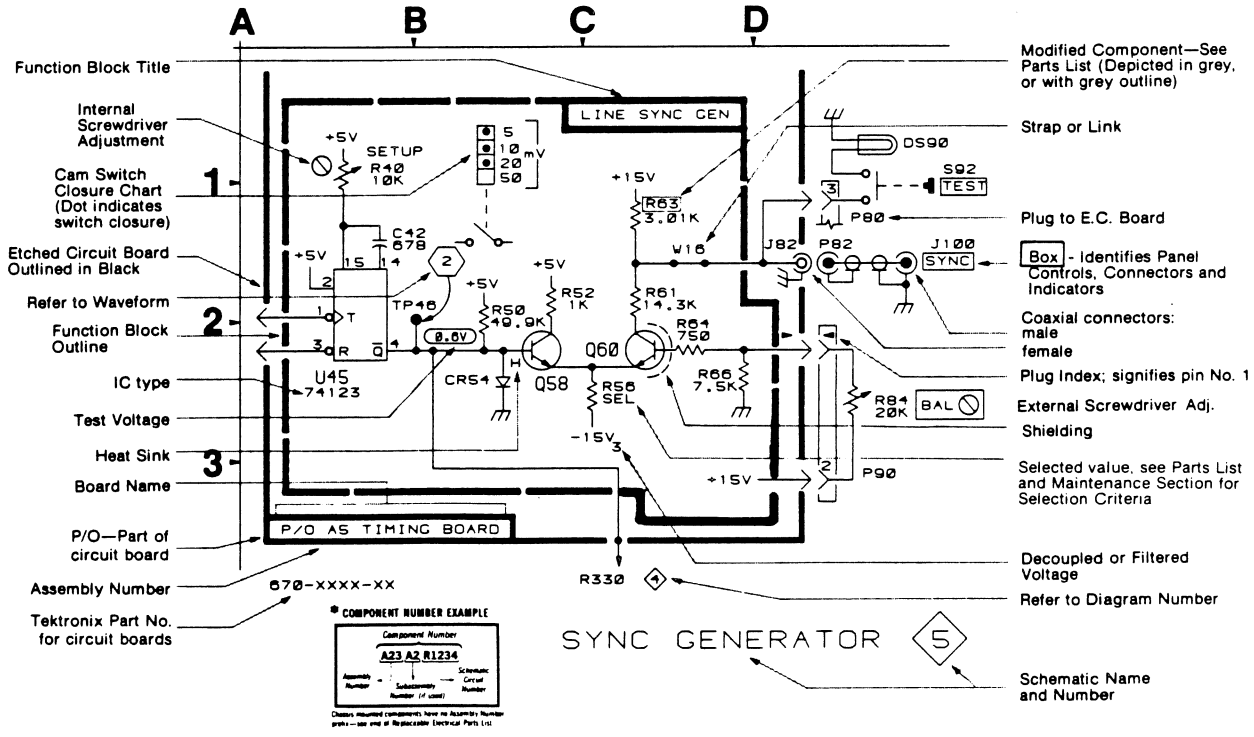
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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SIGNATURE LIST
SA MODE, INT CLOCK

SIGNAL	LOCATION	PIN	SIGNATURE
+5 V	TP1210 (+5 V)		7023
A0	U1111	9	01CU
A1	U1111	10	566H
A2	U1111	11	12H7
A3	U1111	12	0AHP
A4	U1111	13	09UP
A5	U1111	14	A8UA
A6	U1111	15	210P
A7	U1111	16	P31H
A8	U1111	17	6A33
A9	U1111	18	H3A7
A10	U1111	19	1C1U
A11	U1111	20	84C7
A12	U1111	22	HFHA
A13	U1111	23	8536
A14	U1111	24	A8AF
A15	U1111	25	3HUH
$\overline{\text{ADDR}}$	U1210	3	8911
ADD.SW.EN.	TP1002 (AS)		C2CF
ASE	U1210	11	F29U
$\overline{\text{ASE}}$[3000(R)]	U1000	19	C2CF
BA	U1111	7	0000
BA	U1214	1	0000
BANK	U1114	2	782C
$\overline{\text{BANK}}$	U1114	8	0808
BBA	U1214	2	0000
BR/$\overline{\text{W}}$	TP1102 (BR/$\overline{\text{W}}$)		U60U
BVMA	TP1100 (BVMA)		6P2A
CARD SEL EN	TP1013 (CS)		37C4
CSEL0	U1013	2	U58U
CSEL1	U1013	5	9CA8
CSEL2	U1013	6	UH73
CSEL3	U1013	9	PU1U
CSEL4	U1013	12	271H
CSEL5	U1013	15	8F44
CSEL6	U1013	16	H6UU
CSELEXP	U1013	19	050F
D0	U1111	33	A40U
D1	U1111	32	2PP2
D2	U1111	31	2U95
D3	U1111	30	A1C3
D4	U1111	29	2532
D5	U1111	28	4FP5
D6	U1111	27	FUUU
D7	U1111	26	AU09
DIO1	U1003	38	0AAP
DIO8	U1003	31	0AAP
$\overline{\text{E000}}$	U1211	7	F521
$\overline{\text{E000H}}$	U1117	13	C502
EBR/$\overline{\text{W}}$	TP1211 (EBR/$\overline{\text{W}}$)		U60U
EBVMA	TP1212 (EBVMA)		6P2A
EOI	U1003	27	AFA6
EXP RAM CE	TP1205 (ER)		471A
$\overline{\text{EXTBUS}}$	TP1112 (EB)		U36F
$\overline{\text{EXTBUS}}+\phi 2$	U1012	19	7226 *
$\overline{\text{EXTBUS}}+\phi 2$	U1012	19	U36F

* 7023 or U36F signatures possible

TEST MODES, SETUPS, AND SIGNATURES

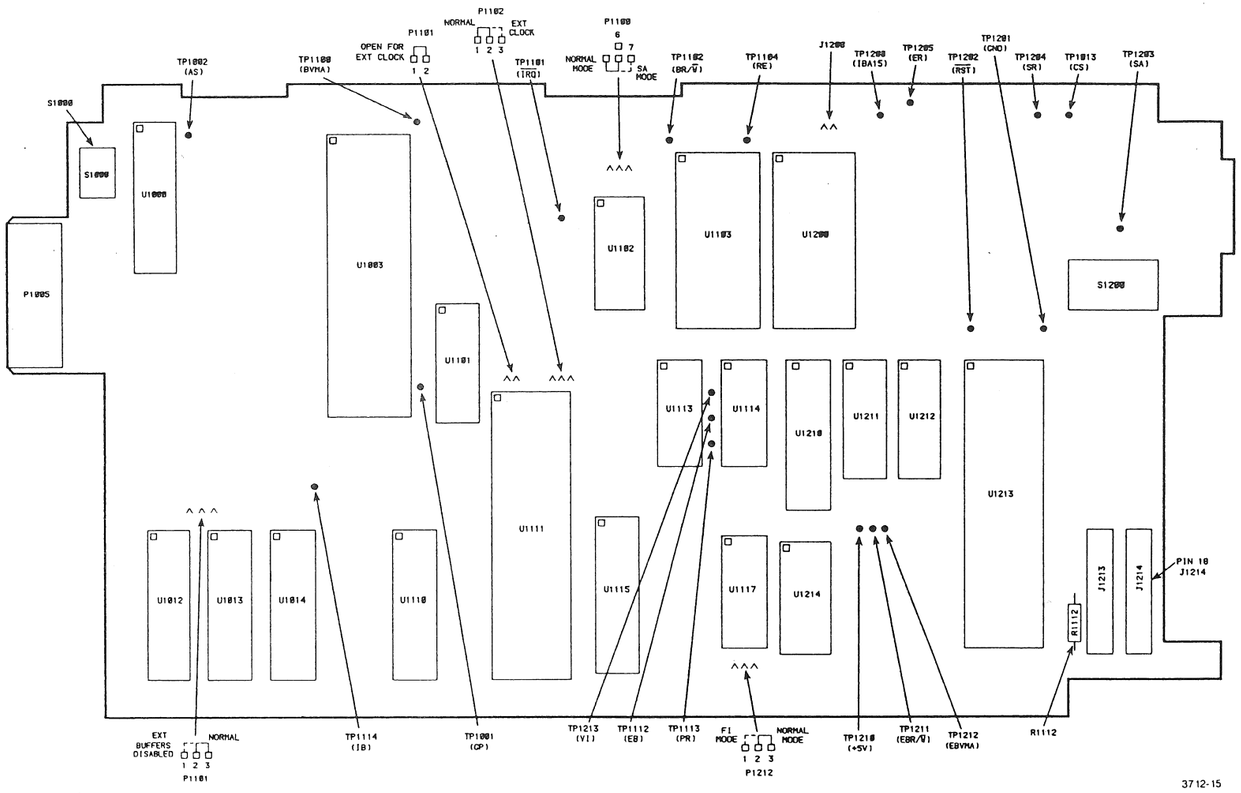


Fig. 8-1. Test points and jumper locations (A20 assembly).

TEST MODE SETUPS

Equipment Setup	SA INT CLOCK	SA EXT CLOCK	FI INT CLOCK	FI EXT CLOCK
SA 501 Probes	Connect/Set:	Connect/Set: See Note 2	Connect/Set:	Connect/Set: See Note 2
CLOCK	Ø2 (U1111-37)	J1214-18	Ø2 (U1111-37)	J1214-18
START	SA, TP1203	SA, TP1203	IBA15, TP1200	IBA15, TP1200
STOP	SA, TP1203	SA, TP1203	IBA15, TP1200	IBA15, TP1200
GROUND	DIG GND	DIG GND	DIG GND	DIG GND
SA 501 Pushbuttons				
CLOCK	⌐	⌐	⌐	⌐
START	⌐	⌐	⌐	⌐
STOP	⌐	⌐	⌐	⌐
THRESHOLD	TTL	TTL	TTL	TTL
Board Jumpers				
P1100	SA Mode	SA Mode	Normal	Normal
P1212	Normal	Normal	FI Mode	FI Mode
P1101	Normal	Remove	Normal	Remove
P1102	Normal	Ext Clock	Normal	Ext Clock
P1011	Normal	Normal	Normal	Normal
Address Switches (S1000)	LF/EOI, with address at binary 0 (01 hex)	Same	Same	Same
Shorting Jumper	J1214-16 to J1214-24	J1214-16 to J1214-24	NA (Disconnect)	NA (Disconnect)
Mode Verification	See Note 1	See Note 1	See Note 3	See Note 3
Signature List	SA, INT CLOCK MODE	SA, EXT CLOCK MODE	FI, INT CLOCK MODE	FI, EXT CLOCK MODE

EXT CLOCK INPUT TO J1214-18: 2.8 V, ±100 mV; 0 V, ±100 mV; 4.2 MHz, ±2 kHz

NOTE

See Test Mode Verification Procedures in the Maintenance section for Notes 1, 2, and 3.

SIGNAL	LOCATION	PIN	SIGNATURE
GND	TP1201 (GND)		0000
GPIB CHIP EN.	TP1001 (GP)		0H2F
$\overline{\text{HALT}}$	U1111	2	7023
$\overline{\text{IBA7}}$	U1113	9	933P
IBA12	U1200	18	HFHA
$\overline{\text{IBA12}}$	U1103	18	AFU9
IBA13	J1200	1	8536
IBA13	U1115	9	8536
IBA14	J1200	2	A8AF
IBA14	U1115	13	A8AF
IBA15	TP1200 (IBA15)		3HUH
IBD0	U1014	2	4H85
IBD1	U1014	18	AU88
IBD2	U1014	4	4P05
IBD3	U1014	16	F023
IBD4	U1014	6	44A2
IBD5	U1014	14	2H75
IBD6	U1014	8	6FU0
IBD7	U1014	12	P96C

SIGNAL	LOCATION	PIN	SIGNATURE
$\overline{\text{INTDATAEN}}$	U1014	19	5F18
$\overline{\text{INTDATAEN}}$	TP1114 (IB)		5F18
$\overline{\text{IRQ}}$	TP1101 ($\overline{\text{IRQ}}$)	-	3493
LOW 2K	U1102	6	6044
LOW 256	U1113	1	H2A8
$\overline{\text{MR}}$	U1111	3	7023
NC	U1101	7	1P09
$\overline{\text{NMI}}$	U1111	6	7023
PA($\overline{\text{N}}$)	U1213	Pins 2 through 9	3U93
PB($\overline{\text{N}}$)	U1213	Pins 10 through 17	U932
$\overline{\text{RAM ENBL}}$	U1111	36	7023
$\overline{\text{RST}}$	TP1202 ($\overline{\text{RST}}$)	-	7023
$\overline{\text{R}}$/W	U1214	9	862F
R/$\overline{\text{W}}$	U1111	34	U60U
SA STRT/STP	TP1203		C811
SRQ	U1003	29	6113
SYS RAM CE	TP1204 (SR)		9716
SYS ROM CE	TP1104 (RE)		F521
TE	U1003	21	0C8H

SIGNAL	LOCATION	PIN	SIGNATURE
VIA $\overline{\text{CE}}$	TP1213 (VI)		3C92
VIA$\overline{\text{CS2}}$	U1113	5	4CC1
$\overline{\text{VMA}}$	U1111	5	6P2A
$\overline{\text{WE}}$	U1101	9	U60U
$\overline{\text{WRITEENBL}}$	U1110	1	U60U
μP RAM ACT.	TP1113 (PR)		5CH6
$\overline{0000}$	U1211	15	501U
$\overline{2000}$	U1211	14	PH15
$\overline{2000H}$	U1212	4	9716
$\overline{2800H}$	U1212	5	471A
$\overline{3000H[W]}$	U1212	12	37C4
$\overline{3800H}$	U1212	7	C811
$\overline{3800H}$	U1212	13	U52C
$\overline{4000}$	U1211	13	PUC8
$\overline{8000}$	U1211	11	899A
$0000H	U1113	8	5CH6
$0080H	U1213	23	3C92
$0080H	U1213	24	512H
$00C0H	U1113	6	0H2F

FORCED INSTRUCTION MODE SIGNATURES

SIGNATURE LIST
SA MODE, EXT CLOCK

SIGNAL	LOCATION	PIN	SIGNATURE
+5 V	TP1210 (+5 V)		2A7C
BA	U1214	1	0000
BBA	U1214	2	0000
Bϕ2	U1214	14	F4P0
$\overline{\text{B}\phi\text{2}}$	U1214	13	PP9C
DMAEN	U1116	1	0000
$\overline{\text{DMAEN}}$	U1116	1	2A7C
$\overline{\text{EXTBUS}}$	TP1112 (EB)		8PCA
$\overline{\text{EXTBUS}}$&ϕ2	U1100	8	3HUC
GND	TP1201 (GND)		0000
$\overline{\text{HALT}}$	U1111	2	2A7C
IBVMA	U1101	4	P787
IBVMA&Bϕ2	U1101	6	2UH1
ID	U1213	39	2A7C *
$\overline{\text{INTDATAEN}}$	TP1114 ($\overline{\text{IB}}$)		UPU6
$\overline{\text{IRQ}}$	TP1101 ($\overline{\text{IRQ}}$)		C082
L. DEC.	U1216	7	F4P0
MR	U1111	3	2A7C
$\overline{\text{NMI}}$	U1111	6	2A7C
R.DEC.	U1216	9	PP9C
RE	U1117	5	2A7C
$\overline{\text{ROMDIS}}$	U1117	2	2A7C
$\overline{\text{RESET}}$	TP1202 ($\overline{\text{RST}}$)		2A7C
ϕ2	U1214	15	F4P0

* GOES TO 0000, IF ID PUSHED

SIGNATURE LIST
FI MODE, EXT CLOCK

SIGNAL	LOCATION	PIN	SIGNATURE
+5 V	TP1210 (+5 V)		00UP
BA	U1214	1	0000
BBA	U1214	2	0000
Bϕ2	U1214	14	0066
$\overline{\text{B}\phi 2}$	U1214	13	0098
Bϕ2·IBVMA	U1101	6	0077
DMAEN	U1116	3	0000
$\overline{\text{DMAEN}}$	U1116	1	00UP
$\overline{\text{EXTBUS}}$	TP1112 (EB)		00UP
$\overline{\text{EXTBUS}\&\phi 2}$	U1100	8	00UP
GND	TP1201 (GND)		0000
$\overline{\text{HALT}}$	U1111	2	00UP
IBVMA	U1101	4	00UP
ID	U1213	39	00UP*
$\overline{\text{INTDATAEN}}$	TP1114 (IB)		00UP
$\overline{\text{IRQ}}$	TP1101 ($\overline{\text{IRQ}}$)		00UP
L. DEC.	U1216	7	0066
$\overline{\text{MR}}$	U1111	3	00UP
$\overline{\text{NMI}}$	U1111	6	00UP
R.DEC.	U1216	9	0098
$\overline{\text{RE}}$	U1117	5	0000
$\overline{\text{ROMDIS}}$	U1117	2	00UP
$\overline{\text{RESET}}$	TP1202 ($\overline{\text{RST}}$)		00UP
ϕ2	U1214	15	0066

* GOES TO 0000, IF ID PUSHED

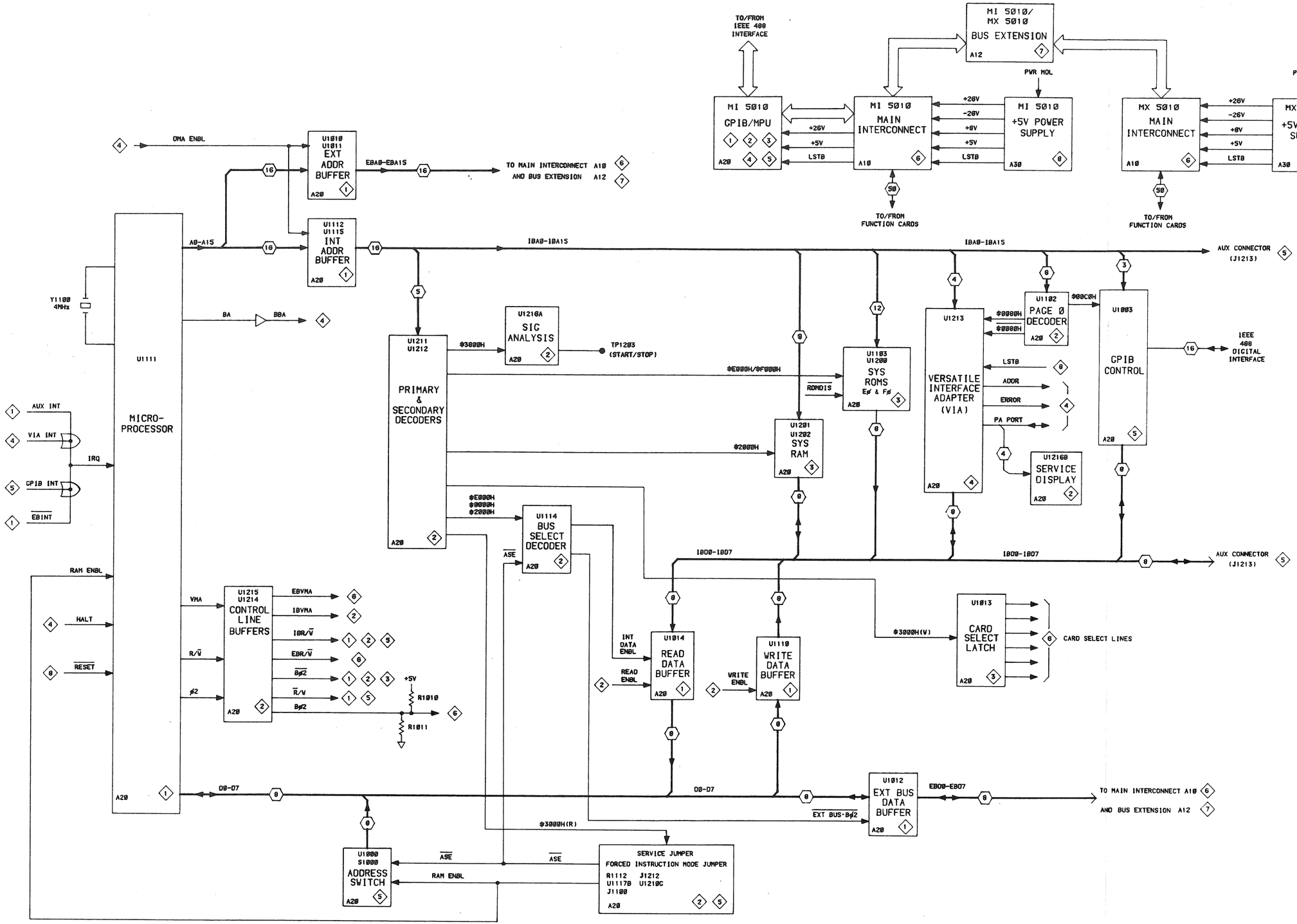

TO/FROM IEEE 488 INTERFACE
MI 5010/ MX 5010 BUS EXTENSION
A12
PWR MDL
MI 5010 GPIB/MPU
MI 5010 MAIN INTERCONNECT
MI 5010 +5V POWER SUPPLY
MX 5010 MAIN INTERCONNECT
MX 5010 +5V POWER SUPPLY
+26V
-26V
+8V
+5V
LSTB
TO/FROM FUNCTION CARDS
DMA ENBL
U1010 U1011 EXT ADDR BUFFER
EBA0-EBA15
TO MAIN INTERCONNECT A10
AND BUS EXTENSION A12
U1112 U1115 INT ADDR BUFFER
A0-A15
IBA0-IBA15
AUX CONNECTOR (J1213)
Y1100 4MHz
BA
BBA
U1111
MICRO-PROCESSOR
U1211 U1212 PRIMARY & SECONDARY DECODERS
U1216A SIG ANALYSIS
$3800H
TP1203 (START/STOP)
$E000H/$F000H
ROMDIS
U1103 U1200 SYS ROMS
U1201 U1202 SYS RAM
$2000H
U1213 VERSATILE INTERFACE ADAPTER (VIA)
$0080H
$0040H
U1102 PAGE 0 DECODER
$00C0H
U1003 GPIB CONTROL
IEEE 488 DIGITAL INTERFACE
LSTB
ADDR
ERROR
PA PORT
U1216B SERVICE DISPLAY
AUX INT
VIA INT
IRQ
GPIB INT
EBINT
$E000H
$0000H
$2000H
U1114 BUS SELECT DECODER
ASE
IBD0-IBD7
AUX CONNECTOR (J1213)
RAM ENBL
HALT
RESET
VMA
R/V
Φ2
U1215 U1214 CONTROL LINE BUFFERS
EBVMA
IBVMA
IBR/V
EBR/V
BΦ2
R/V
BΦ2
+5V
R1010
R1011
INT DATA ENBL
READ ENBL
U1014 READ DATA BUFFER
WRITE ENBL
U1110 WRITE DATA BUFFER
$3000H(W)
U1013 CARD SELECT LATCH
CARD SELECT LINES
D0-D7
U1012 EXT BUS DATA BUFFER
EBD0-EBD7
TO MAIN INTERCONNECT A10
AND BUS EXTENSION A12
EXT BUS-BΦ2
$3000H(R)
U1000 S1000 ADDRESS SWITCH
SERVICE JUMPER
FORCED INSTRUCTION MODE JUMPER
R1112 J1212
U1117B U1210C
J1100
A20

Fig. 8-2
COMPONENT LOCATION

PARTS LOCATION GRID

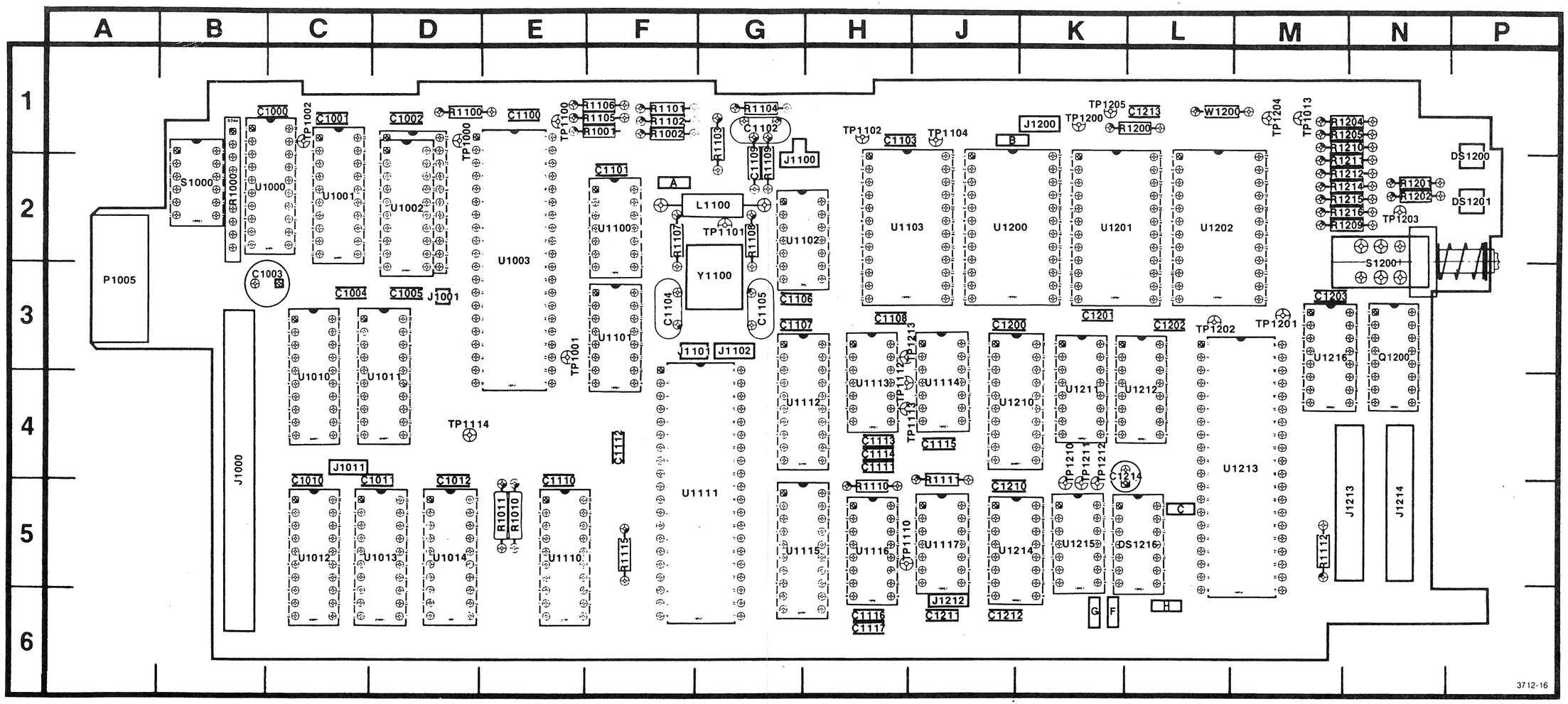
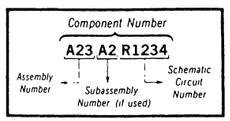


Fig. 8-2. Microprocessor board (A20 assembly).

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Static Sensitive Devices
See Maintenance Section

Table 8-1
COMPONENT REFERENCE CHART

P/O A20 ASSY — MICROPROCESSOR BOARD ◇1

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1003	B2	B3
C1004	H1	C3
C1005	H3	D3
C1010	I7	C5
C1012	F6	D5
C1104	C3	F3
C1105	C4	G3
C1107	F1	G3
C1109	C4	G2
C1110	H7	E4
C1111	F3	H4
C1112	D3	F4
C1117	C2	H6
J1000	L3	B4
J1101	C3	F3
J1102	B4	G3
L1100	C4	G2
P1101	B3	F3
P1102	B4	G3
R1000	D1	B2
R1105	C5	F1
R1106	D6	F1
R1107	D7	F2
R1108	C2	G2
R1109	C4	G2
R1115	C2	F5
TP1101	C6	G2
TP1201	B3	M3
TP1202	D2	L3
TP1210	B1	K4
U1010	I1	C4
U1011	I3	D4
U1012	J7	C5
U1014	G6	D5
U1110	H7	E5
U1111	E1	G5
U1112	G1	G4
U1115	G3	G5
U1116B	E8	H5
U1116C	C1	H5
U1117C	G8	J5
U1214A	H5	J5
Y1100	C4	G3

P/O A20 ASSY also shown on ◇2 ◇3 ◇4 ◇5

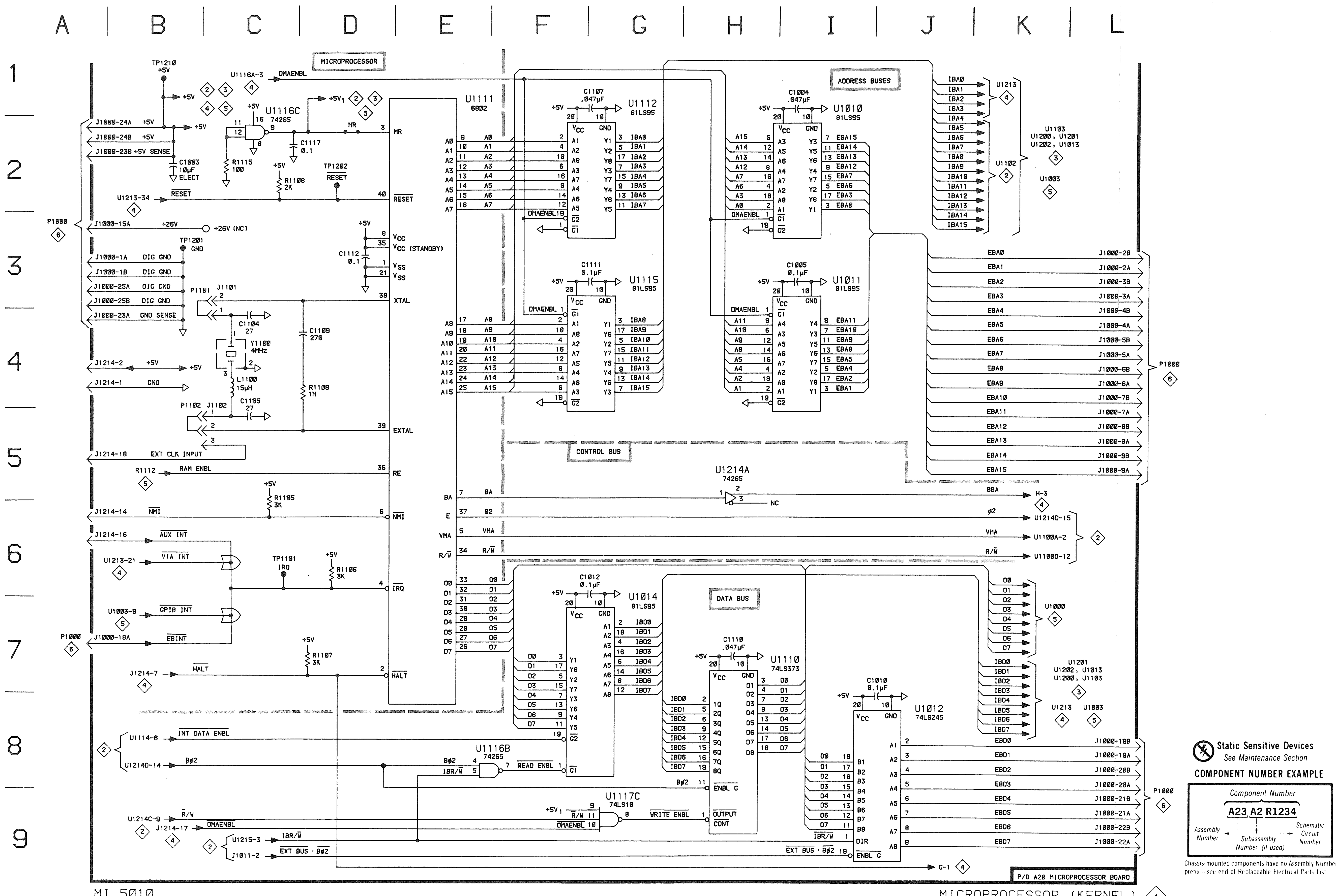
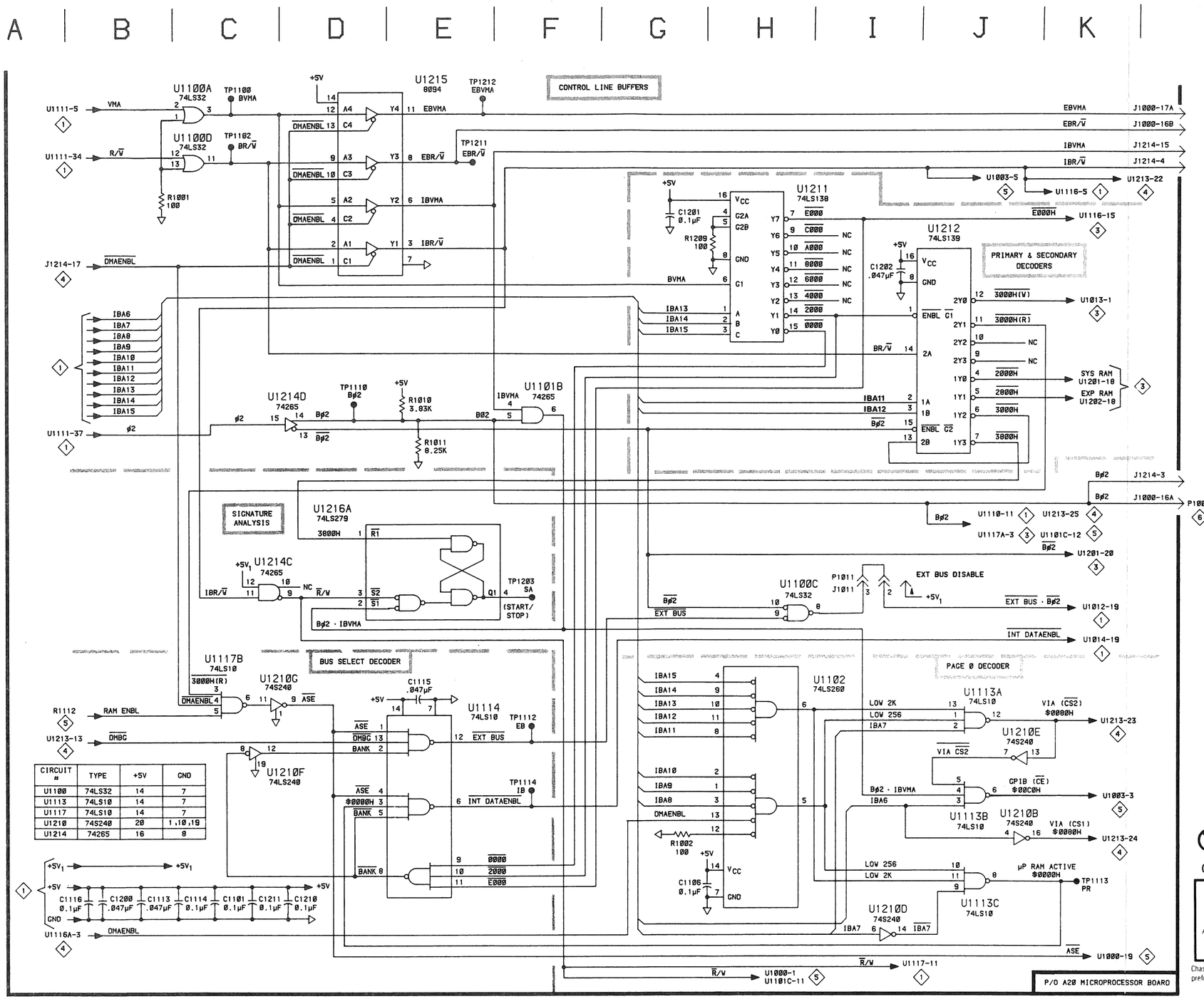

MICROPROCESSOR
ADDRESS BUSES
CONTROL BUS
DATA BUS
U1111 6802
U1112 81LS95
U1115 81LS95
U1010 81LS95
U1011 81LS95
U1014 81LS95
U1110 74LS373
U1012 74LS245
U1116C 74265
U1116B 74265
U1117C 74LS10
U1214A 74265
Y1100 4MHz
L1100 15µH
P1000
EXT CLK INPUT
RAM ENBL
AUX INT
VIA INT
GPIB INT
EBINT
HALT
INT DATA ENBL
READ ENBL
WRITE ENBL
EXT BUS · Bφ2
P/O A20 MICROPROCESSOR BOARD
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Table 8-2
COMPONENT REFERENCE CHART
(see Fig. 8-2)

P/O A20 ASSY — MICROPROCESSOR BOARD ◇2

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1101	C8	F2	TP1113	K8	H4
C1106	G8	G3	TP1114	F7	D4
C1113	B8	H4	TP1203	F6	N2
C1114	B8	H4	TP1211	E1	K4
C1115	E6	J4	TP1212	E1	K4
C1116	A8	H6			
C1200	B8	J3	U1100C	H6	F2
C1201	G2	K3	U1100D	B1	F2
C1202	I3	L3	U1101B	F4	F3
C1210	C8	J5	U1102	H6	G2
C1211	C8	J6	U1113A	J7	H4
			U1113B	J8	H4
J1011	I6	C4	U1113C	J9	H4
			U1114	E7	J4
P1011	I6	I6	U1117B	C6	J5
			U1210B	J8	J4
R1001	B2	F1	U1210D	I9	J4
R1002	G8	F1	U1210E	J7	J4
R1010	E4	E5	U1210F	C7	J4
R1011	E4	E5	U1210G	C6	J4
R1209	G2	M2	U1211	H2	K4
			U1212	I2	L4
			U1214C	C5	J5
TP1100	C1	E1	U1214D	C4	J5
TP1102	C1	H1	U1215	E1	K5
TP1110	D4	H5	U1216A	D5	M3
TP1112	F7	H4			

P/O A20 ASSY also shown on ◇1 ◇3 ◇4 ◇5



CIRCUIT #	TYPE	+5V	GND
U1100	74LS32	14	7
U1113	74LS10	14	7
U1117	74LS10	14	7
U1210	74S240	20	1,10,19
U1214	74265	16	8

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number · *Subassembly Number (if used)* · *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

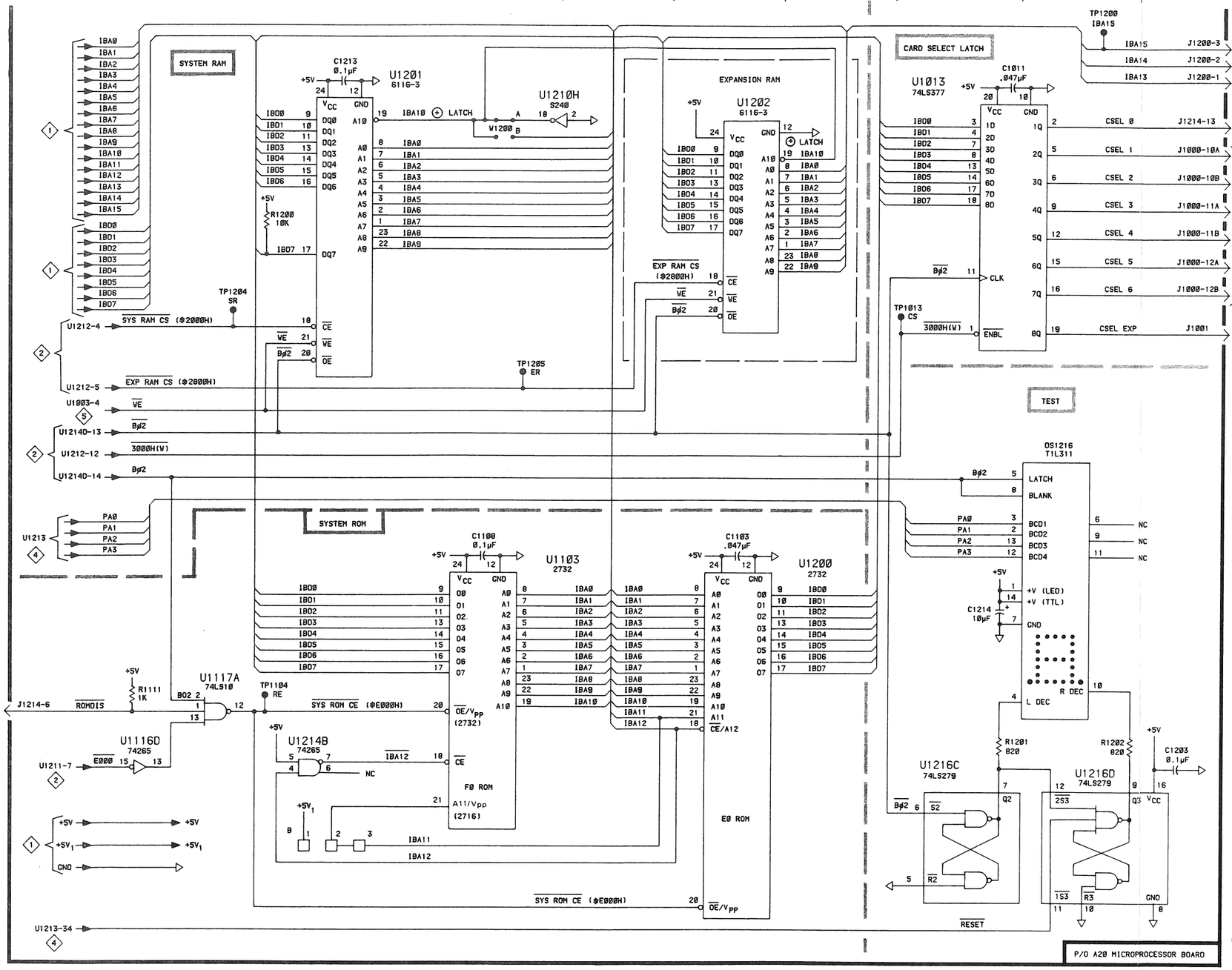
Table 8-3
COMPONENT REFERENCE CHART
(see Fig. 8-2)

P/O A20 ASSY — MICROPROCESSOR BOARD ◇3

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1011	J1	D5
C1103	H5	H1
C1108	F5	H3
C1203	L7	M3
C1213	D1	L1
C1214	J6	L4
DS1216	K4	L5
J1001	L3	D3
J1200	L1	K1
J1214	L2	N5
R1111	C7	J4
R1200	D3	L1
R1201	J7	N2
R1202	K7	N2

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
TP1013	I3	M1
TP1104	D7	J1
TP1200	K1	K1
TP1204	C3	M1
TP1205	F4	K1
U1013	J1	D5
U1103	F5	H2
U1116D	B7	H5
U1117A	C7	J5
U1200	I5	J2
U1201	E1	K2
U1202	H1	L2
U1210H	F1	J4
U1214B	D7	J5
U1216C	J7	M3
U1216D	K7	M3
W1200	F2	L1

P/O A20 ASSY also shown on ◇1 ◇2 ◇4 ◇5



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

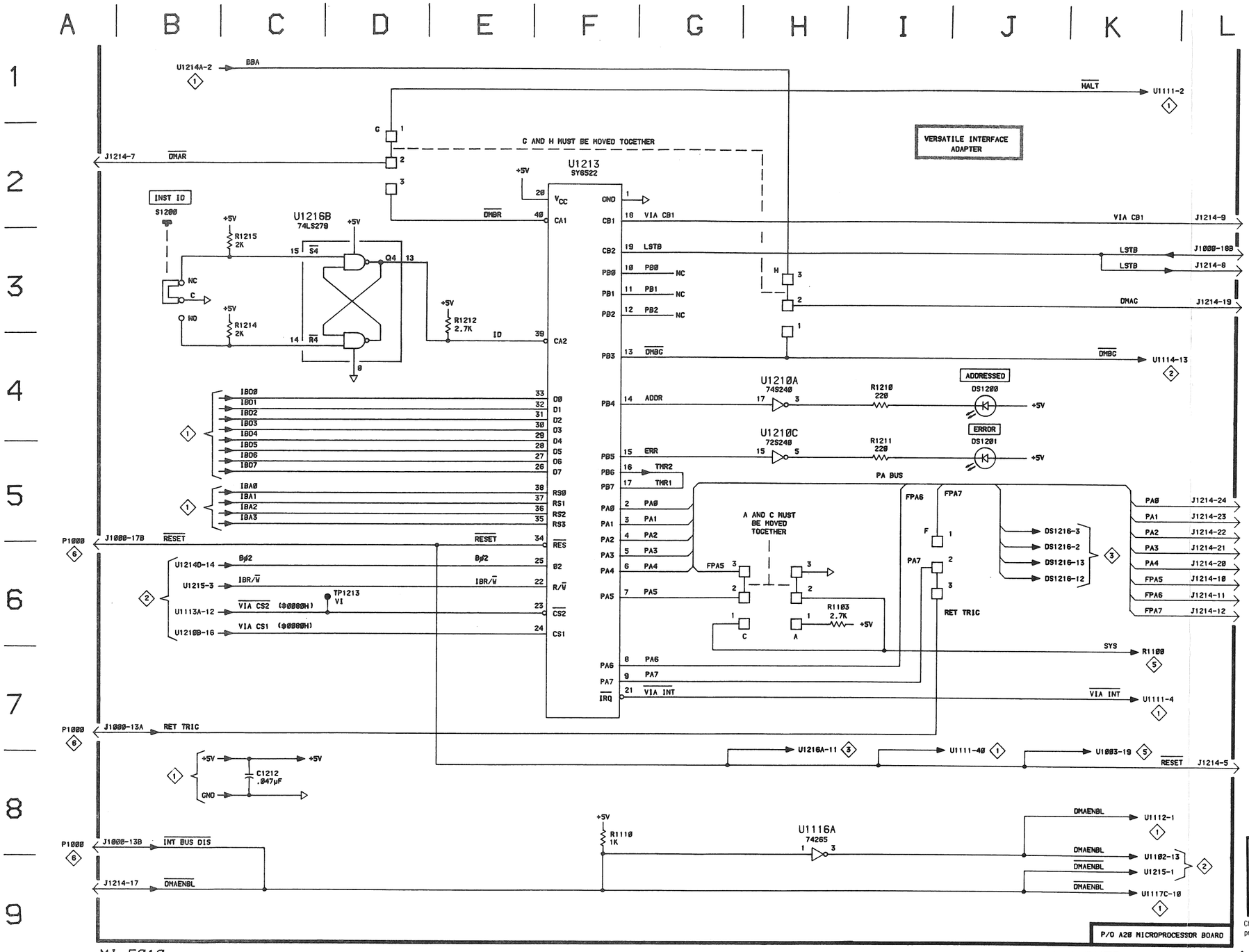
Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Table 8-4
COMPONENT REFERENCE CHART
(see Fig. 8-2)

P/O A20 ASSY			MICROPROCESSOR BOARD ◇4		
CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1212	C8	J6	S1200	B2	N2
DS1200	J4	P1	TP1213	C6	H3
DS1201	J4	P2			
			U1116A	H8	H5
R1103	H6	G1	U1210A	H4	J4
R1110	F8	H5	U1210C	H4	J4
R1210	I4	M1	U1213	F2	M4
R1211	I4	M2	U1216B	C2	M3
R1212	E3	M2			
R1214	C3	M2			
R1215	C2	M2			

P/O A20 ASSY also shown on ◇1 ◇2 ◇3 ◇5



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

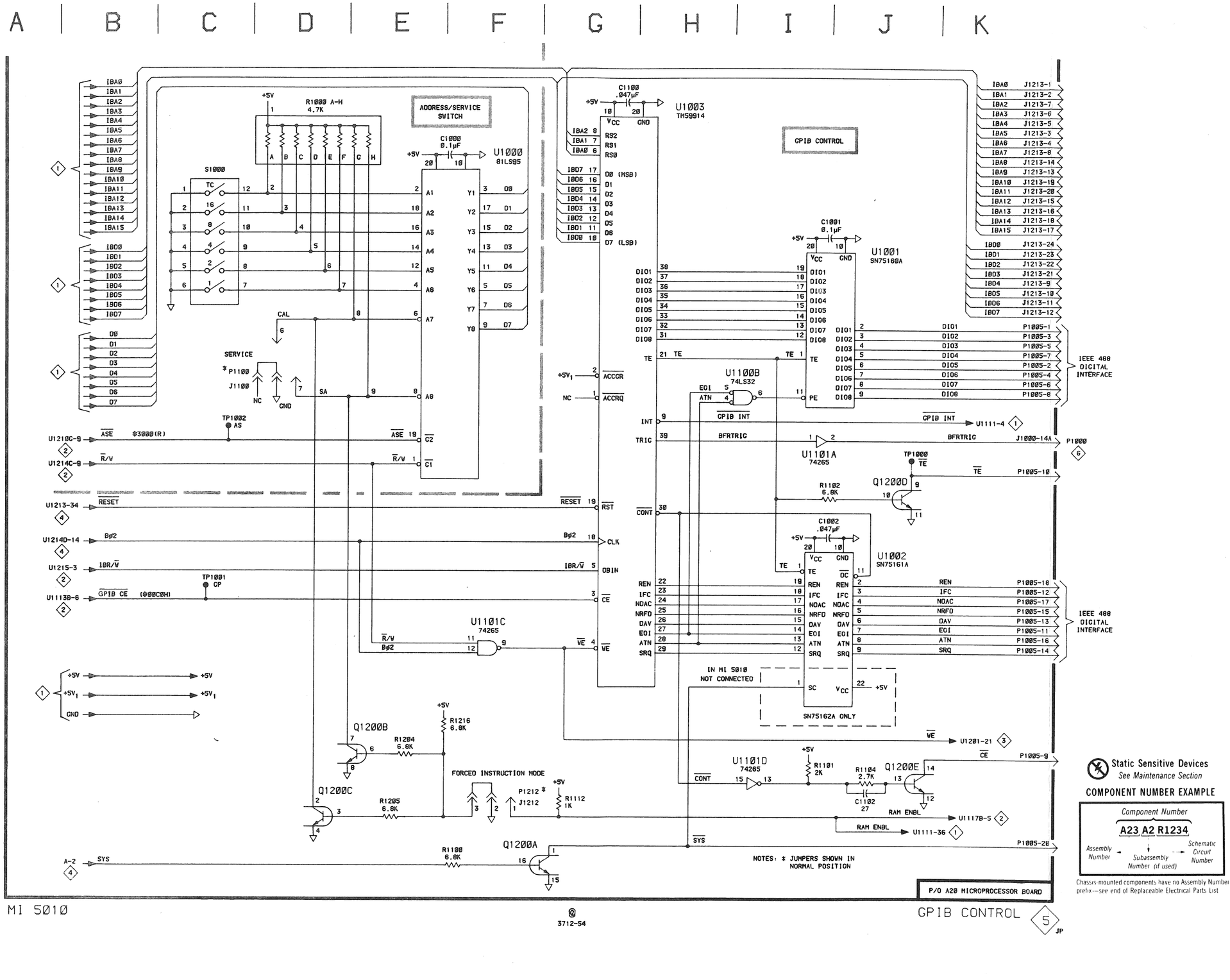
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Table 8-5
COMPONENT REFERENCE CHART
(see Fig. 8-2)

P/O A20 ASSY — MICROPROCESSOR BOARD ◇5

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1000	E2	C1
C1001	I2	C1
C1002	I6	D1
C1100	G1	E1
C1102	J8	G1
J1100	C4	G2
J1212	F8	J6
J1213	K1	N5
P1005	K3	A3
P1100	C4	G2
P1212	F8	J6
Q1200A	F9	N3
Q1200B	E8	N3
Q1200C	D8	N3
Q1200D	J5	N3
Q1200E	J8	N3
R1100	E9	D1
R1101	I8	F1
R1102	I5	F1
R1104	J8	G1
R1112	G8	M5
R1204	E8	M1
R1205	E8	M1
R1216	E8	M2
S1000	C2	B2
TP1000	J5	D1
TP1001	C6	E3
TP1002	C4	C1
U1000	F2	B2
U1001	J3	C2
U1002	J6	D2
U1003	H1	E2
U1100B	H4	F2
U1101A	I5	F3
U1101C	F7	F3
U1101D	H8	F3

P/O A20 ASSY also shown on ◇1 ◇2 ◇3 ◇4



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

PARTS LOCATION GRID

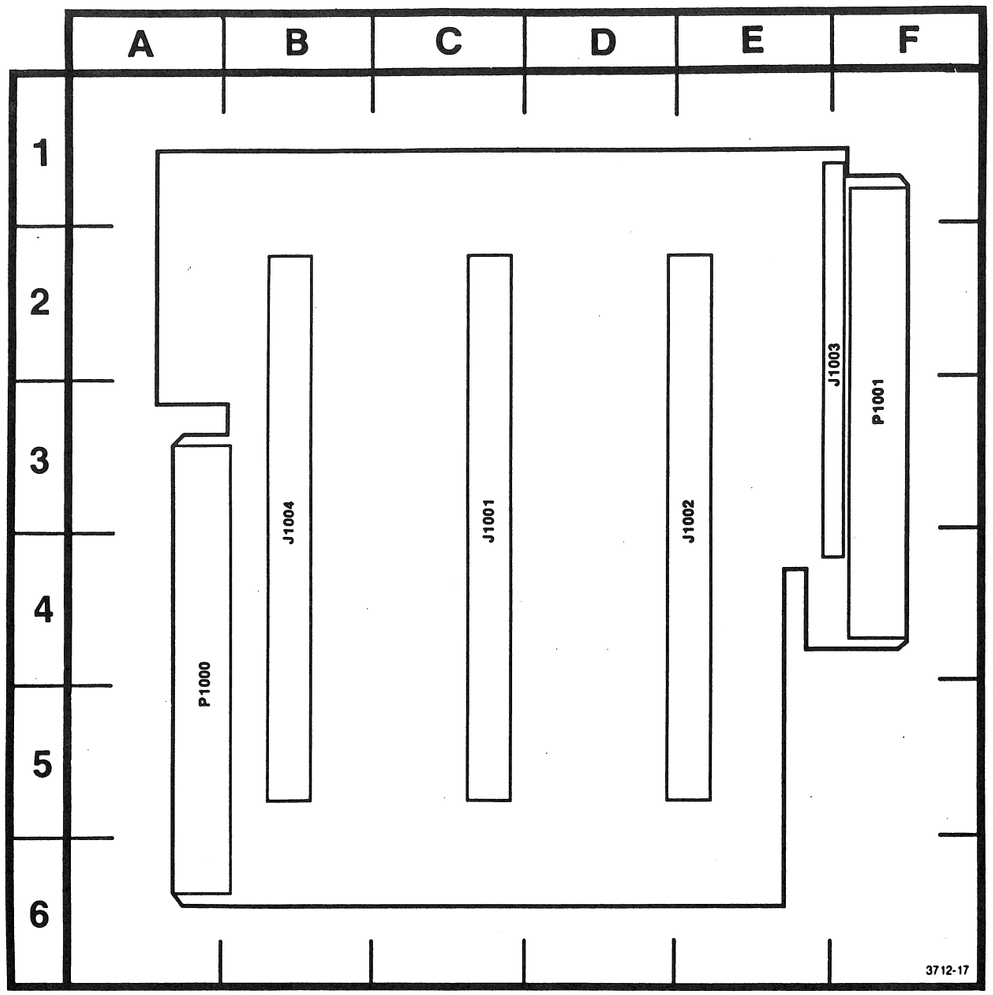
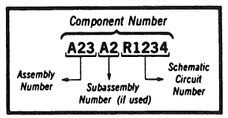


Fig. 8-3. Main Interconnect (A10 assembly).

COMPONENT NUMBER EXAMPLE



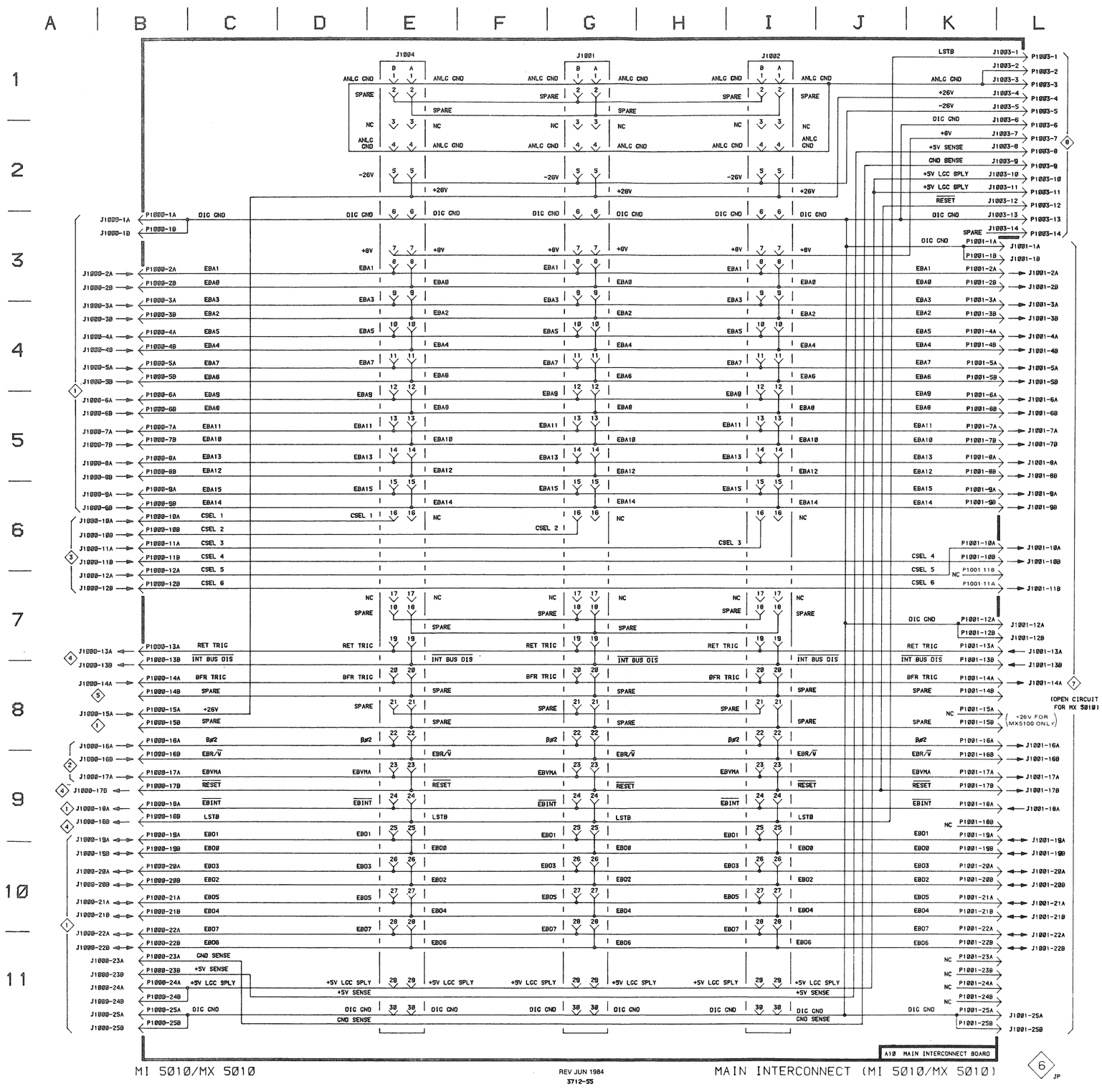
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

Table 8-6
COMPONENT REFERENCE CHART

P/O A10 ASSY			MAIN INTERCONNECT (MI 5010/MX 5010) ◇6		
CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J1001	G1	C3	P1000	B3	A4
J1002	I1	E3	P1001	L3	F3
J1003	L1	F2			
J1004	E1	B3			

@



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix - see end of Replaceable Electrical Parts List

PARTS LOCATION GRID

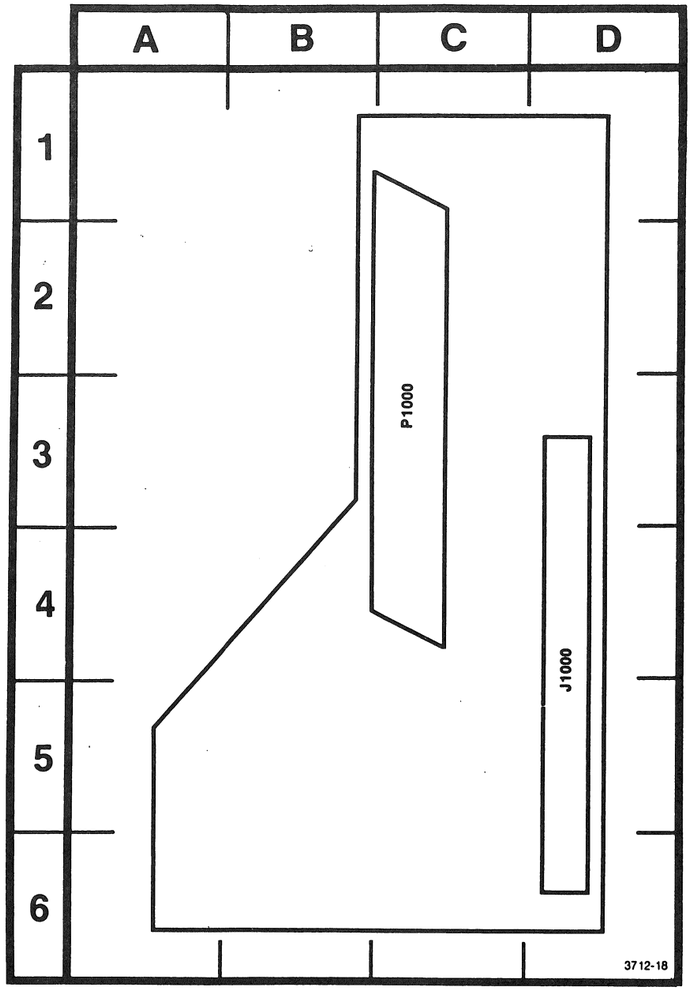
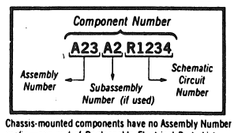


Fig. 8-4. Bus Extension (A12 assembly).

COMPONENT NUMBER EXAMPLE

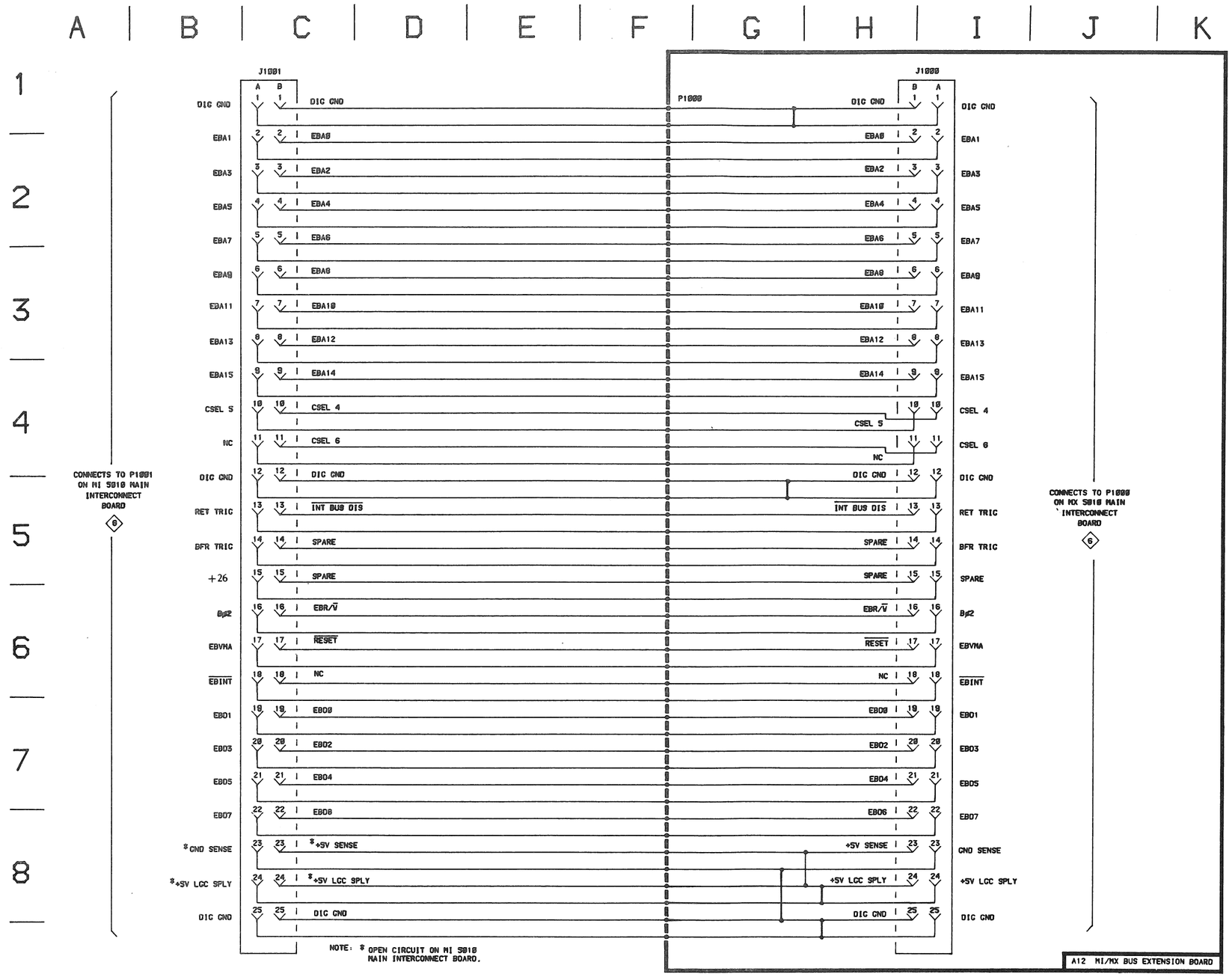


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

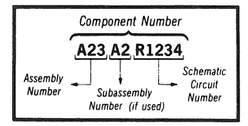
Table 8-7
COMPONENT REFERENCE CHART

P/O A12 ASSY			MI 5010/MX 5010 BUS EXTENSION BOARD ◇7		
CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
J1000	H1	D4	P1000	F1	C3



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

PARTS LOCATION GRID

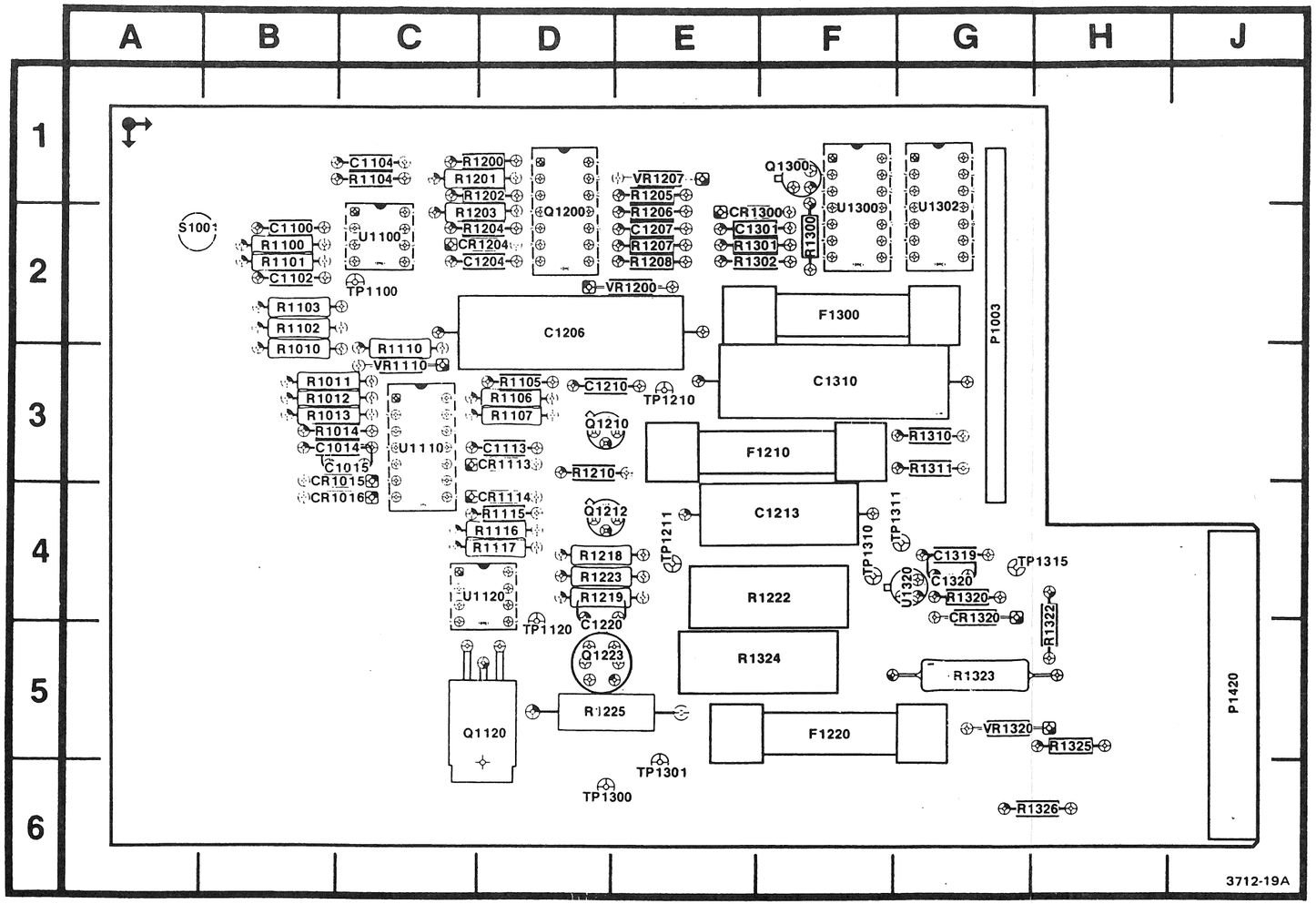
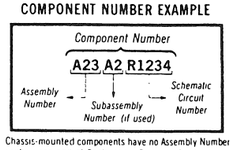


Fig. 8-5. Power Supply (A30 assembly).

COMPONENT NUMBER EXAMPLE



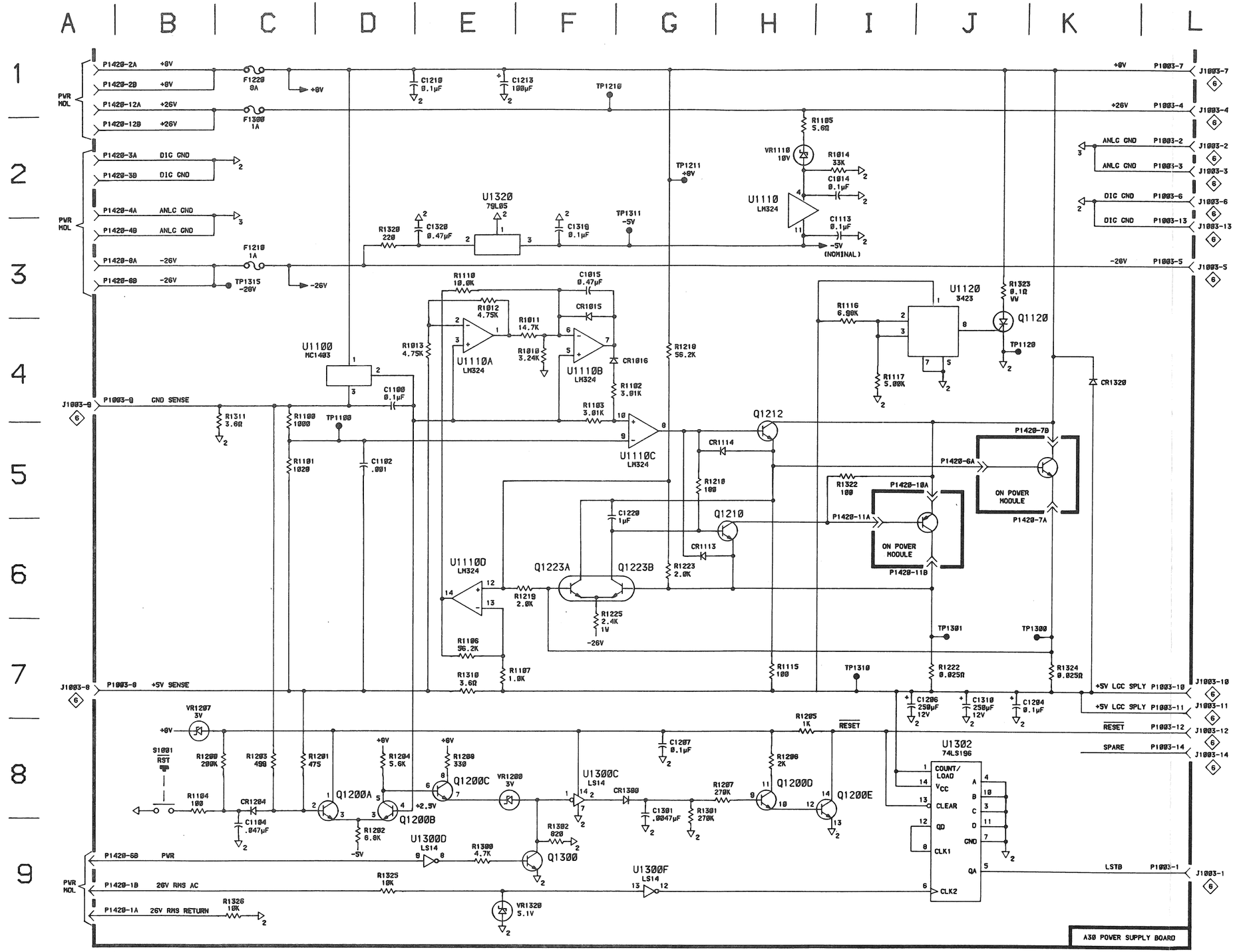
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Static Sensitive Devices
See Maintenance Section

Table 8-8
COMPONENT REFERENCE CHART

P/O A30 ASSY — POWER SUPPLY BOARD ◇8

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1014	I2	B3	R1116	I3	D4
C1015	F3	B3	R1117	I4	D4
C1100	D4	B2	R1200	B8	C1
C1102	D5	B2	R1201	C8	C1
C1104	C8	C1	R1202	D8	C1
C1113	I2	D3	R1203	C8	C2
C1204	J7	C2	R1204	D8	C2
C1206	I7	D2	R1205	H7	E1
C1207	G8	E2	R1206	H8	E2
C1210	D1	D3	R1207	G8	E2
C1213	E1	F4	R1208	E8	E2
C1220	F5	D4	R1210	G5	D3
C1301	G8	E2	R1218	G4	D4
C1310	J7	F3	R1219	E6	D4
C1319	F2	G4	R1222	J7	F4
C1320	D2	G4	R1223	G6	D4
			R1225	F6	D5
CR1015	F3	B3	R1300	E9	F2
CR1016	F4	B4	R1301	G8	E2
CR1113	G6	D3	R1302	F8	E2
CR1114	G5	D4	R1310	E7	G3
CR1204	C8	C2	R1311	B4	G3
CR1300	F8	E2	R1320	D2	G4
CR1320	K4	G4	R1322	I5	H5
			R1323	J3	G5
F1210	C3	F3	R1324	K7	F5
F1220	C1	F5	R1325	D9	H5
F1300	C1	F2	R1326	B9	H6
P1003	L9	G2	S1001	B8	A2
P1420	A9	J5			
			TP1100	D4	C2
Q1120	J3	D5	TP1120	J4	D5
Q1200A	D8	D2	TP1210	F1	E3
Q1200B	D8	D2	TP1211	G2	E4
Q1200C	E8	D2	TP1300	J6	D6
Q1200D	H8	D2	TP1301	J6	E6
Q1200E	I8	D2			
Q1210	G5	D3	TP1310	I7	F4
Q1212	H4	D4	TP1311	F2	F4
Q1223A	F6	D5	TP1315	C3	G4
Q1223B	F6	D5			
Q1300	F9	F1	U1100	C4	C2
			U1110A	E4	C3
R1010	E4	B3	U1110B	F4	C3
R1011	E3	B3	U1110C	G5	C3
R1012	E3	B3	U1110D	E6	C3
R1013	D4	B3	U1110E	H2	C3
R1014	I2	B3	U1120	J3	D4
R1100	C4	B2	U1300C	F8	F2
R1101	C5	B2	U1300D	D9	F2
R1102	F4	B2	U1300F	G9	F2
R1103	F4	B2	U1302	J8	G2
R1104	B8	C1	U1320	E2	G4
R1105	H1	D3			
R1106	E7	D3	VR1110	H2	C3
R1107	E7	D3	VR1200	E8	E2
R1110	E3	C3	VR1207	B7	E1
R1115	H7	D4	VR1320	E9	G5



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

```
1 2 3 4 5                    Name & Description
Assembly and/or Component
Attaching parts for Assembly and/or Component
                - - - * - - -
   Detail Part of Assembly and/or Component
   Attaching parts for Detail Part
                - - - * - - -
      Parts of Detail Part
      Attaching parts for Parts of Detail Part
                - - - * - - -
```

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
05574	VIKING CONNECTORS INC	21001 NORDHOFF ST	CHATSWORTH CA 91311
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS	30 HUNTER LANE	CAMP HILL PA 17011
27264	MOLEX INC CORPORATE HQ	2222 WELLINGTON COURT	LISLE IL 60532
71785	TRW INC TRW CINCH CONNECTORS	1501 MORSE AVE	ELK GROVE VILLAGE IL 60007
75915	LITTELFUSE INC	800 E NORTHWEST HWY	DES PLAINES IL 60016
78189	ILLINOIS TOOL WORKS INC SHAKEPROOF DIVISION	ST CHARLES ROAD	ELGIN IL 60120
79136	WALDES KOHINOOR INC	47-16 AUSTEL PLACE	LONG ISLAND CITY NY 11101
80009	TEKTRONIX INC	4900 S W GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
83486	ELCO INDUSTRIES INC	1101 SAMUELSON RD	ROCKFORD IL 61101
93907	TEXTRON INC CAMCAR DIV	600 18TH AVE	ROCKFORD IL 61101
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247
TK0435	LEWIS SCREW CO	4114 S PEORIA	CHICAGO IL 60609

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	337-2807-02			2	SHIELD,ELEC:SIDE,PLUG-IN UNIT	80009	337-2807-02
					(ATTACHING PARTS)		
-2	214-3364-00			4	FASTENER,LATCH:ACETAL,SIL GRAY	80009	214-3364-00
-3	105-0932-00			4	LATCH,PANEL:SIDE	80009	105-0932-00
					(END ATTACHING PARTS)		
-4	220-0633-00			1	NUT,PLAIN,KNURL:0.25-28 X 0.375 OD,BRS NP	80009	220-0633-00
-5	355-0170-00			1	STUD,SHLDR&STEP:BINDING POST	80009	355-0170-00
-6	210-1365-00			1	WASHER,FLAT:0.141 ID X 0.266 OD X 0.5,AL	80009	210-1365-00
-7	366-1851-01			1	KNOB,LATCH:IVORY GY,0.625 X 0.25 X 1.09	80009	366-1851-01
-8	366-1559-08			1	PUSH BUTTON:SLATE GRAY,0.18 SQ X 0.43	80009	366-1559-08
-9	333-2854-00			1	FRONT PNL ASSY:W/SUBPANEL	80009	333-2854-00
					(ATTACHING PARTS)		
-10	211-0541-00			4	SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-11	213-0886-00			3	BOLT,SHOULDER:0.25-20 X 0.743 L,HEX HD,STL	80009	213-0886-00
					(ATTACHING PARTS)		
-12	354-0184-00			3	RING,RETAINING:PRONG-LOCK EXT,U/O 0.25 ID	79136	5555-25-S-PP
-13	210-0839-00			3	WASHER,SPR TNSN:0.258 ID X 0.438 OD	78189	3539-14-01-0541C
					(END ATTACHING PARTS)		
-14	255-0581-00			AR	PLASTIC CHANNEL:0.156 X 0.156,POLYETHYLENE	80009	255-0581-00
-15	333-2824-01			1	PANEL,REAR:	80009	333-2824-01
					(ATTACHING PARTS)		
-16	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
-17	386-3657-01			2	SUPPORT,PLUG-IN:	93907	ORDER BY DESCR
-18	211-0007-00			6	SCREW,MACHINE:4-40 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-19	214-3089-00			2	LOCKOUT,PLUG-IN:PLASTIC	80009	214-3089-00
-20	214-1061-00			1	CONTACT,ELEC:GROUNDING,CU BE	80009	214-1061-00
-21	351-0675-00			6	GUIDE,CKT BOARD:DELRIN,7.855 L	80009	351-0675-00
-22	351-0672-00			5	GUIDE,CKT BOARD:PLASTIC	80009	351-0672-00
-23	426-1862-00			1	FR SECT,PLUG-IN:TOP	80009	426-1862-00
					(ATTACHING PARTS)		
-24	211-0105-00			2	SCREW,MACHINE:4-40 X 0.188,FLH,100 DEG	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-25	----- -----			1	CKT BOARD ASSY:MAIN INTERCONN(SEE A10 REPL)		
-26	131-1228-01			3	.CONN,RCPT,ELEC:CKT BD,30/60 CONT	80009	131-1228-01
-27	131-2725-00			1	.CONN,RCPT,ELEC:HEADER,14 CONT MALE	00779	1-640384-4
-28	407-2556-00			4	BRACKET,ANGLE:CIRCUIT BOARD,AL	80009	407-2556-00
					(ATTACHING PARTS)		
-29	211-0007-00			4	SCREW,MACHINE:4-40 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
-30	211-0105-00			2	SCREW,MACHINE:4-40 X 0.188,FLH,100 DEG	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-31	----- -----			1	CKT BOARD ASSY:GPIB MPU(SEE A20 REPL)		
-32	131-0993-00			5	.BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
-33	131-0608-00			67	.TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
-34	----- -----			1	.SWITCH,PUSH:(SEE A20S1200 REPL)		
-35	361-0384-00			2	.SPACER,PB SW:0.133 L,RED POLYCARBONATE	80009	361-0384-00
-36	361-0385-00			2	.SPACER,PB SW:0.164 L,GREEN POLYCARBONATE	80009	361-0385-00
-37	----- -----			22	.TERM,TEST POINT:(SEE A20TP1000,1001,1002, .1013,1100,1101,1102,1104,1110,1112,1113, .1114,1200,1202,1203,1204,1205,1210, .1211,1212,1213 REPL)		
-38	136-0269-02	B010100	B010164	7	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP	09922	DILB14P-108T
	136-0728-00	B010165		1	.SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-39	136-0260-02	B010100	B010164	7	.SKT,PL-IN ELEK:MICROCKT,16 DIP,LOW CL	09922	DILB16P-108T
-40	136-0634-00	B010100	B010164	12	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
	136-0752-00	B010165		10	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-41	136-0578-00	B010100	B010164	4	.SKT,PL-IN ELEK:MICROCIRCUIT,24 DIP,LOW PF	09922	DILB24P-108
	136-0751-00	B010165		4	.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-42	136-0623-00	B010100	B010164	3	.SKT,PL-IN ELEK:CMPNT,40 DIP,LOW PROFILE	09922	DILB40P-108
	136-0757-00	B010165		3	.SKT,PL-IN ELEK:MICROCIRCUIT,40 DIP	09922	DILB40P-108
-43	346-0032-00			1	.STRAP,RETAINING:0.075 DIA X 4.0 L	98159	2829-75-4
-44	131-2543-00			1	.CONN,RCPT,ELEC:CKT BD,25/50,FEMALE	05574	000201-4543
-45	----- -----			1	CKT BOARD ASSY:POWER SUPPLY(SEE A30 REPL)		
-46	136-0514-00	B010100	B010164	2	.SKT,PL-IN ELEK:MICROCIRCUIT,8 DIP	09922	DILB8P-108
-47	136-0269-00	B010100	B010164	4	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,PCB MT	71785	133-51-02-073
-48	344-0326-00			6	.CLIP,ELECTRICAL:FUSE,BRASS	75915	102071

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-49	----- -----			9	.TERM,TEST POINT:(SEE A30TP1100,1120,1210, .1211,1300,1301,1310,1311,1315 REPL)		
-50	131-2737-00			1	.CONN,RCPT,ELEC:CKT BD,RTANG,1 X 14	27264	26-11-6144
-51	105-0865-00			1	BAR,LATCH RLSE:	80009	105-0865-00
-52	105-0866-00			1	LATCH,RETAINING:SAFETY	80009	105-0866-00
-53	214-3143-00			1	SPRING,HLEXT:0.125 OD X 0.545 L,XLOOP	80009	214-3143-00
-54	426-1863-02			1	FR SECT,PLUG-IN:W/SPRING & EYELET	80009	426-1863-02

FIG. 1 EXPLODED
MI 5010

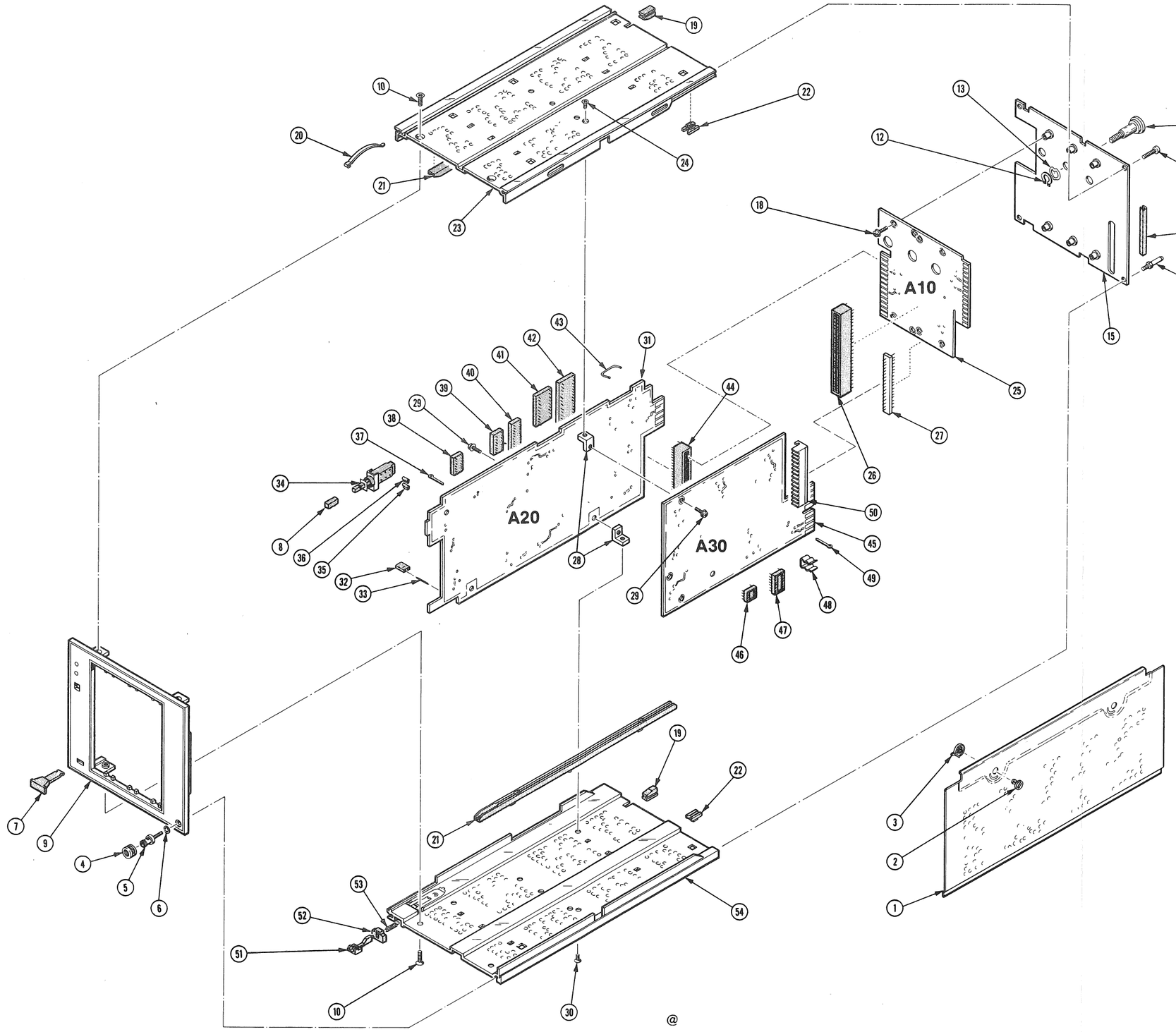


FIG. 2 EXPLODED
MX 5010

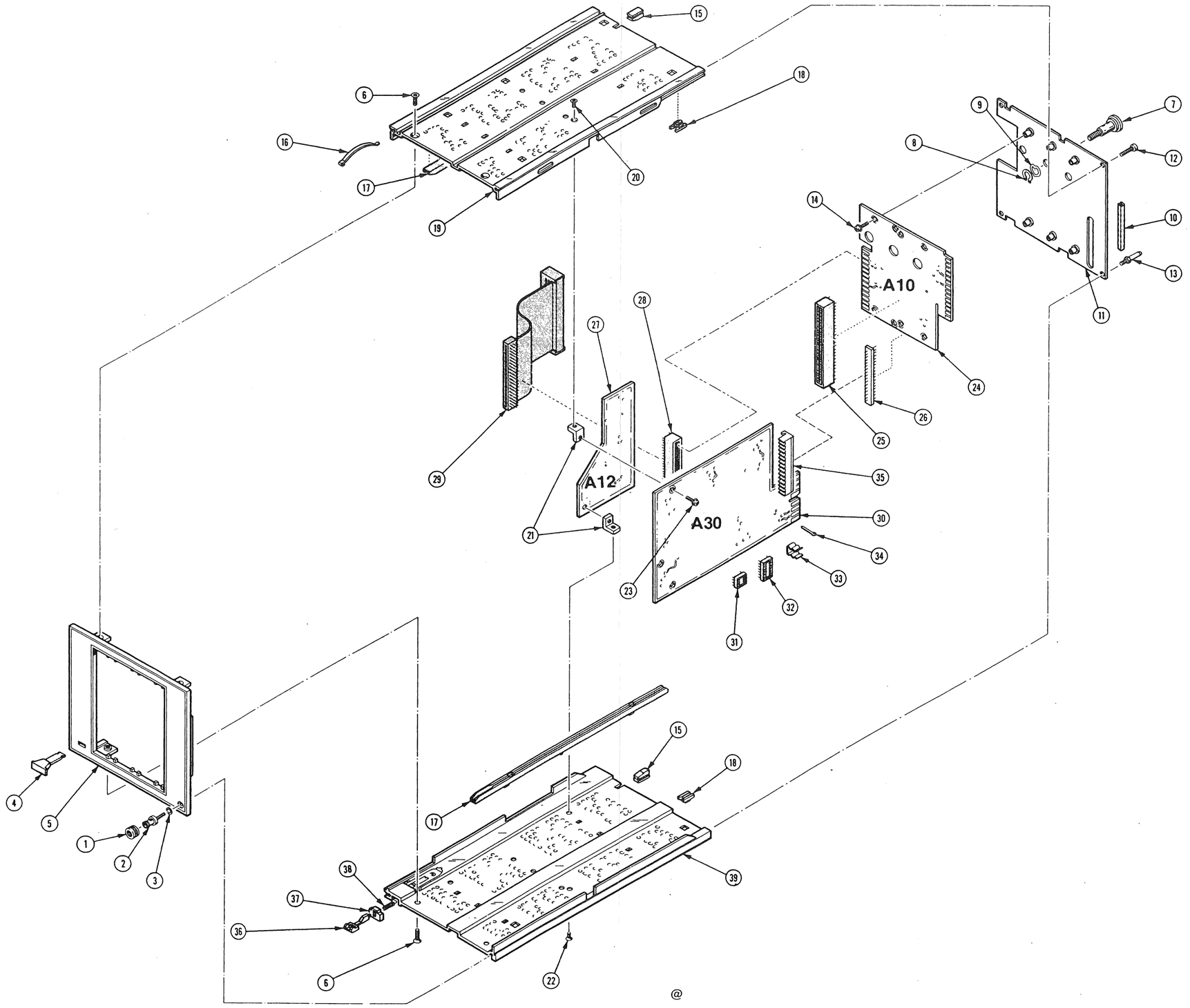


Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	220-0633-00			1	NUT,PLAIN,KNURL:0.25-28 X 0.375 OD,BRS NP	80009	220-0633-00
-2	355-0170-00			1	STUD,SHLDR&STEP:BINDING POST	80009	355-0170-00
-3	210-1365-00			1	WASHER,FLAT:0.141 ID X 0.266 OD X 0.5,AL	80009	210-1365-00
-4	366-1851-01			1	KNOB,LATCH:IVORY GY,0.625 X 0.25 X 1.09	80009	366-1851-01
-5	333-2855-00			1	FRONT PNL ASSY:M/SUBPANEL	80009	333-2855-00
					(ATTACHING PARTS)		
-6	211-0541-00			4	SCREW,MACHINE:6-32 X 0.25,FLH,100 DEG,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-7	213-0886-00			3	BOLT,SHOULDER:0.25-20 X 0.743 L,HEX HD,STL	80009	213-0886-00
					(ATTACHING PARTS)		
-8	354-0184-00			3	RING,RETAINING:PRONG-LOCK EXT,U/O 0.25 ID	79136	5555-25-S-PP
-9	210-0839-00			3	WASHER,SPR TNSN:0.258 ID X 0.438 OD	78189	3539-14-01-0541C
					(END ATTACHING PARTS)		
-10	255-0581-00			AR	PLASTIC CHANNEL:0.156 X 0.156,POLYETHYLENE	80009	255-0581-00
-11	333-2824-00			1	PANEL,REAR:	80009	333-2824-00
					(ATTACHING PARTS)		
-12	213-0793-00			2	SCREW,TPG,TF:6-32 X 0.4375,TAPTITE,FILH	83486	239-006-406043
-13	386-3657-01			2	SUPPORT,PLUG-IN:	93907	ORDER BY DESCR
-14	211-0007-00			6	SCREW,MACHINE:4-40 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-15	214-3089-00			2	LOCKOUT,PLUG-IN:PLASTIC	80009	214-3089-00
-16	214-1061-00			1	CONTACT,ELEC:GROUNDING,CU BE	80009	214-1061-00
-17	351-0675-00			6	GUIDE,CKT BOARD:DELRIN,7.855 L	80009	351-0675-00
-18	351-0672-00			3	GUIDE,CKT BOARD:PLASTIC	80009	351-0672-00
-19	426-1862-00			1	FR SECT,PLUG-IN:TOP	80009	426-1862-00
					(ATTACHING PARTS)		
-20	211-0105-00			2	SCREW,MACHINE:4-40 X 0.188,FLH,100 DEG	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-21	407-2556-00			3	BRACKET,ANGLE:CIRCUIT BOARD,AL	80009	407-2556-00
					(ATTACHING PARTS)		
-22	211-0105-00			1	SCREW,MACHINE:4-40 X 0.188,FLH,100 DEG	TK0435	ORDER BY DESCR
-23	211-0007-00			3	SCREW,MACHINE:4-40 X 0.188,PNH,STL	TK0435	ORDER BY DESCR
					(END ATTACHING PARTS)		
-24	----- -----			1	CKT BOARD ASSY:MAIN INTCON(SEE A10 REPL)		
-25	131-1228-01			3	.CONN,RCPT,ELEC:CKT BD,30/60 CONT	80009	131-1228-01
-26	131-2725-00			1	.CONN,RCPT,ELEC:HEADER,14 CONT MALE	00779	1-640384-4
-27	----- -----			1	CKT BOARD ASSY:MI/MX BUS EXT(SEE A12 REPL)		
-28	131-2543-00			1	.CONN,RCPT,ELEC:CKT BD,25/50,FEMALE	05574	000201-4543
-29	175-4272-00			1	.CA ASSY,SP,ELEC:50,28 AWG,4.79 L,RIBBON	TK0031	ZCA-08300
-30	----- -----			1	CKT BOARD ASSY:POWER SUPPLY(SEE A30 REPL)		
-31	136-0514-00	B010100	B010164	2	.SKT,PL-IN ELEK:MICROCIRCUIT,8 DIP	09922	DILB8P-108
-32	136-0269-02	B010100	B010164	4	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP	09922	DILB14P-108T
-33	344-0326-00			6	.CLIP,ELECTRICAL:FUSE,BRASS	75915	102071
-34	----- -----			9	.TERM,TEST POINT:(SEE A30TP1100,1120,1210,		
					.1211,1300,1301,1311,1315 REPL)		
-35	131-2737-00			1	.CONN,RCPT,ELEC:CKT BD,RTANG,1 X 14	27264	26-11-6144
-36	105-0865-00			1	BAR,LATCH RLSE:	80009	105-0865-00
-37	105-0866-00			1	LATCH,RETAINING:SAFETY	80009	105-0866-00
-38	214-3143-00			1	SPRING,HLEXT:0.125 OD X 0.545 L,XLOOP	80009	214-3143-00
-39	426-1863-02			1	FR SECT,PLUG-IN:M/SPRING & EYELET	80009	426-1863-02
					STANDARD ACCESSORIES		
	070-3712-00			1	MANUAL,TECH:INSTR,MI5010/MX5010	80009	070-3712-00
	070-3882-00			1	CARD,INFO:REFERENCE,MI5010/MX5010	80009	070-3882-00
	062-6009-00			1	DATA SHEET:	80009	062-6009-00
					(MX 5010 ONLY)		
					OPTIONAL ACCESSORIES		
	015-0466-00			1	ACCESSORY ASSY:CONNECTOR MODULE	80009	015-0466-00
	015-0473-00			1	INTFC MODULE:3 WIDE	80009	015-0473-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-3712-00			1		MANUAL,TECH:INSTRUCTION	80009	070-3712-00
	070-3882-00			1		CARD,INFO:REFERENCE	80009	070-3882-00
	062-6009-00			1		DATA SHEET:MX5010	80009	062-6009-00
	----- -----			-		(MX 5010 ONLY)		
						OPTIONAL ACCESSORIES		
	015-0466-00			1		ACCESSORY ASSY:CONNECTOR MODULE	80009	015-0466-00
	015-0473-00			1		INTFC MODULE:3 WIDE	80009	015-0473-00