National Semiconductor Corporation

PRELIMINARY

NMC98C10/NMC98C40 Electrically Erasable, Programmable Memories

General Description

The NMC98C10 and NMC98C40 are 128 by 8 and 512 by 8 5-volt programmable, non-volatile, parallel access memories built with 3-micron CMOS floating gate process. Data and address lines are multiplexed, enabling these devices to be packaged in an 18-pin DIP, saving board space. The pin-out is identical to the Intel 8185 static RAM and the 2001 non-volatile RAM, allowing the memories to directly interface with Intel and other popular 8-bit and 16-bit microprocessors and microcontrollers.

The write cycle is simplified by a self-timed erase before write circuit on-chip. The end of write cycle can be determined by polling the data pins or the controller can simply allow a minimum time between a write command and the subsequent command. To prevent undesirable modification of the memory contents during system power up or power down, a lockout circuit ignores write commands while V_{CC} is below the prescribed level of VLKO.

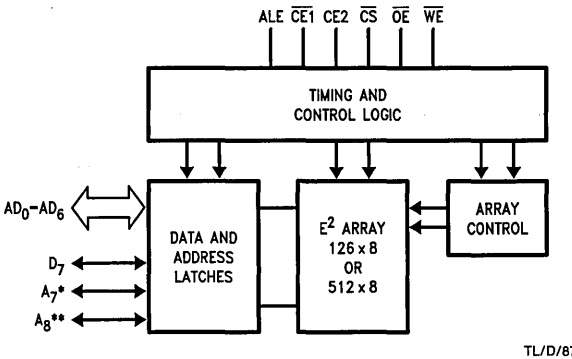
Applications for these memories include storing position data in robotic systems, storing local area network node address and parameter settings in data communications equipment, storing set-up and last position data in industrial control systems and storing PBX switch data in telecommunications equipment.

The NMC98C10 and NMC98C40 are compatible with Sierra Semiconductor SC22101, SC22104.

Features

- CMOS EE technology
- Single 5-volt supply
- Reliable CMOS floating gate process
- Eighteen-pin package
- Multiplexed address and data bus
- Self timed write operation
- $\overline{\text{DATA}}$ polling
- Minimum 10,000 erase/write cycles
- Very low power dissipation
- Ten year data retention
- Minimum board space
- Directly compatible with NSC800, NSC32000 and other standard microprocessors
- No external sequencing of erase/write cycle
- End of write cycle verified by polling
- Long product life

Block and Connection Diagrams



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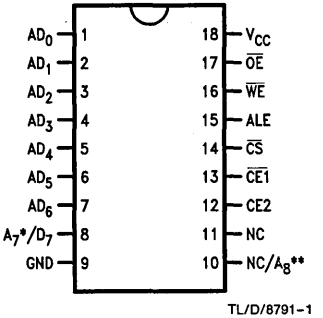

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Order Number NMC98C10N, NMC98C10N-1, NMC98C40N, NMC98C40N-1
See NS Package Number N18A

Absolute Maximum Ratings (Note 1)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage, V_{CC}	7V
Voltage on Any Pin	V_{CC} + 0.5V GND − 0.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @ 25°C (Note 2)	500 mW
Lead Temp. (Soldering, 10 seconds)	300°C

ESD rating is to be determined.

Operating Conditions

(Applies to DC and AC Characteristics)

Ambient Temperature	0°C to 70°C
Positive Supply Voltage	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = − 400 μA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
V_{LKO}	V_{CC} Level for Write Lockout		4.0		4.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}			±10.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}			±10.0	μA
I_{CC}	Operating Supply Current	TTL Inputs			15.0	mA
		CMOS Inputs			10.0	mA
I_{CCPD}	Standby Supply Current	TTL Inputs			5.0	mA
		CMOS Inputs			100	μA
I_{SC}	Short-Circuit Current	One Output Pin Shorted		40		mA

AC Electrical Characteristics

Symbol	Parameter	NMC98C10, NMC98C40		NMC98C10-1, NMC98C40-1		Units
		Min	Max	Min	Max	
T_{AL}	Address to Latch Setup Time	50		20		ns
T_{LA}	Address Hold Time after Latch	45		30		ns
T_{LC}	Latch to OE/WE Control	80		35		ns
T_{OE}	Valid Data Out Delay from Read Control		170		120	ns
T_{LD}	ALE to Data Out Valid		300		180	ns
T_{LL}	Latch Enable Width	100		60		ns
T_{OH}	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (Whichever Changes First)	0		0		ns
T_{OLZ}	$\overline{OE}$ Low to Output Driven	10		10		ns
T_{RDF}	Data Bus Float after Read	0	95	0	60	ns
T_{CL}	OE/WE Control to Latch Enable	0		0		ns
T_{CC}	OE/WE Control Width	250		150		ns
T_{DW}	Data In to Write Setup Time	150		150		ns
T_{WD}	Data In Hold Time after Write	20		15		ns
T_{SC}	Chip Select Set-Up to OE/WE Control	50		20		ns
T_{CS}	Chip Select Hold Time after OE/WE Control	10		10		ns
T_{ALCE}	Chip Enable Set-Up to ALE Falling	30		5		ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	NMC98C10, NMC98C40		NMC98C10-1, NMC98C40-1		Units
		Min	Max	Min	Max	
T_{LACE}	Chip Enable Hold Time after ALE Falling	45		40		ns
T_{WR}	Byte Write Cycle Time		20		20	ms
T_{WH}	Data Invalid Time after $\overline{WE}$ Falling		1		1	ms
	Number of Writes Per Byte	10,000		10,000		Cycles

Capacitance (T_A = 25°C, f = 1 MHz) (Note 3)

Parameter	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
$C_{I/O}$	Input/Output Capacitance	$\overline{OE}$ = $\overline{CE1}$ = $\overline{CS}$ = V_{IH}, CE2 = V_{IL}		10	pF

AC Test Conditions

Output Load .....1 TTL Gate + C_L = 100 pF

Input Rise and Fall Times (10% to 90%) .....20 ns

Input Pulse Levels.....0.0V to 3.0V

Input/Output Timing Reference Level.....0.8V to 2.0V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C.

Note 3: This parameter is sampled and not 100% tested.

Pin Descriptions

Pin Number	Pin Name	Function
1–8	AD_0–AD_7	Multiplexed address and data bits. Pin 8 is DATA only for NMC98C10.
9	GND	Ground, 0 volts.
10	A8	MSB of address for NMC98C40, NC for NMC98C10.
11	NC	No connection. No internal connection is made to this pin and it may be left floating.
12	CE2	Chip Enable 2 (see Table I)
13	$\overline{CE1}$	Chip Enable 1 (See Table I)
14	$\overline{CS}$	Chip Select (see Table I)
15	ALE	Address Latch Enable
16	$\overline{WE}$	Write Enable
17	$\overline{OE}$	Output Enable
18	V_{CC}	Positive power supply, 5 volts.

Functional Description

Table I shows the different modes of operation as a function of the control signals. Standby powered down mode: both write and read are inhibited and the device's power consumption is greatly reduced. Standby powered up mode: the device consumes the operating power, but read and write are inhibited. Inhibit mode: the device is write protected to avoid inadvertent modifications while the read and write pins are changing.

READ OPERATION

Figure 2 shows the timing diagram for READ operation. The address is latched on the falling edge of ALE. For the NMC98C10 only pins 1 through 7 are used for address bits. NMC98C40 uses pins 8 and 10 in addition to pins 1 through 7 for address bits.

Data appear on pins 1 through 8 after $\overline{OE}$ becomes active (low).

WRITE OPERATION

Write operation's timing is shown in *Figure 3*. Address is latched on the falling edge of the ALE. After the address is latched, the $\overline{WE}$ becomes active (low) for the minimum time of TCC and returns to inactive state. This initiates the internally timed write operation. No external erase before write operation is needed and data lines as well as control lines may change after the write operation is initiated.

TABLE I. Mode Table

Mode	$\overline{CE1}$	CE2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	AD_0–AD_7
Standby Powered Down	V_{IH}	X	X	X	X	Hi-Z
Standby Powered Down	X	V_{IL}	X	X	X	Hi-Z
Standby Powered Up	V_{IL}	V_{IH}	V_{IH}	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Data In
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Inhibit	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Hi-Z

V_{IL} = Logical Low Input

V_{IH} = Logical High Input

Hi-Z = High Impedance State

X = Don't Care

Functional Description (Continued)

$\overline{\text{DATA}}$ POLLING

After the write operation is initiated, its conclusion can be monitored by putting the device in the READ mode and polling the D7 data bit. The data bit will be logical inverse of the bit being written to a location in memory until the write operation is completed. At this time the D7 data bit will be the same as the last D7 data bit written into memory.

WRITE LOCKOUT

During system power up or power down, an on-chip write lockout circuit prevents spurious WRITES into the memory locations while V_{CC} is lower than the specified lockout voltage VLKO. This frees the system designer from having to design external write protection circuits.

Timing Waveforms

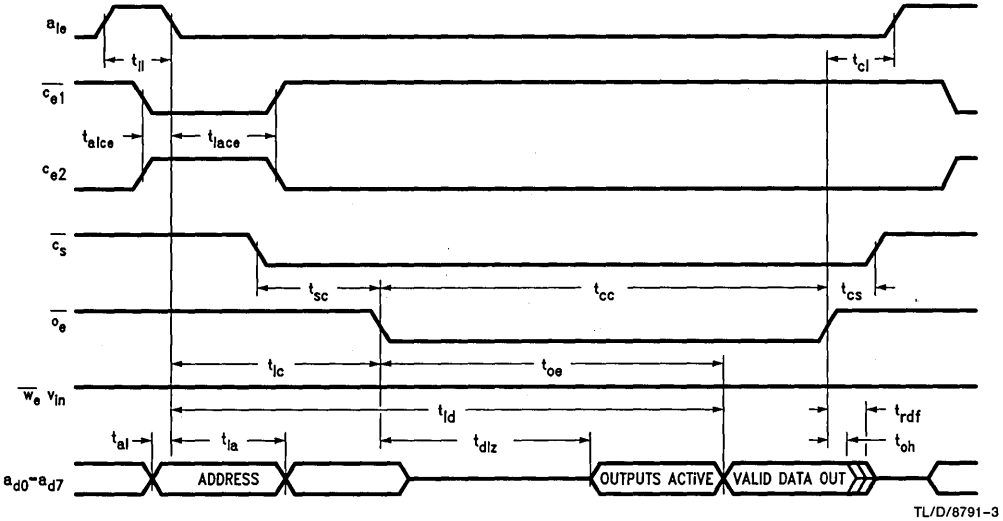


FIGURE 1. Read Timing

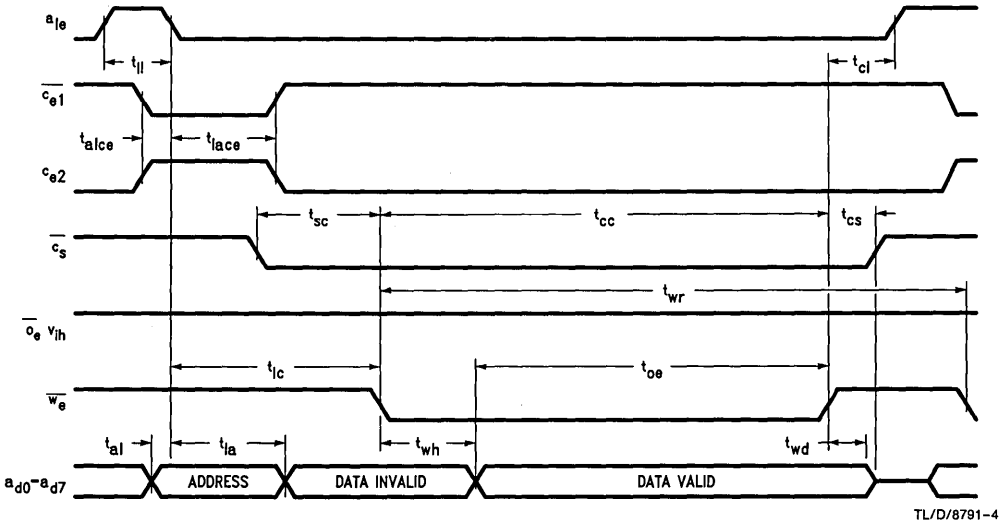
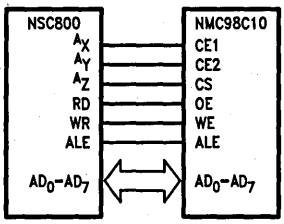


FIGURE 2. Write Timing

Timing Waveforms (Continued)



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Note: A_X, A_Y, A_Z are any three of the 8051 address pins A8–A15. By connecting $\overline{CE1}$, CE2, and CS to specific address lines. The NMC98C10 and NMC98C40 can be mapped to a particular range in memory, without the need for an external memory address decoder.

FIGURE 3. Using the NMC98C10 with an NSC800 Microcontroller

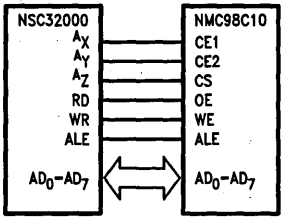

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FIGURE 4. Using the NMC98C10 with the HPC 16040 Microcontroller or NSC32000