CONNECTING TO THE 6502

CONNECTION OVERVIEW

Table 1 provides an overview of the connections between the 1240 Logic Analyzer equipped with a 6502 Mnemonics ROM Pack and your 6502 microprocessor.

NOTE

Regardless of the connection scheme, be sure to connect a USER'S GND lead from each acquisition probe to the microprocessor ground (Vss, pin 1 or pin 21). Otherwise, invalid data may be acquired.

Table 1
1240 SCREEN TO 6502 PINOUT MAP

1240 SCREEN			CONNECTIONS		6502	
GROUP	BIT	C/Q	POD*	CHAN	SIGNAL	PIN
CNTL	4	-	**2**	4	$\overline{IRQ}$	4
	3	-	**2**	3	$\overline{NMI}$	6
	2	-	**2**	2	SO	38
	1	-	**2**	1	SYNC	7
	0	-	**2**	0	R/$\overline{W}$	34
ADDR	15	-	**3**	7	A15	25
	14	-	**3**	6	A14	24
	13	-	**3**	5	A13	23
	12	-	**3**	4	A12	22
	11	-	**3**	3	A11	20
	10	-	**3**	2	A10	19
	9	-	**3**	1	A9	18
	8	-	**3**	0	A8	17
	7	-	**0**	7	A7	16
	6	-	**0**	6	A6	15
	5	-	**0**	5	A5	14
	4	-	**0**	4	A4	13
	3	-	**0**	3	A3	12
	2	-	**0**	2	A2	11
	1	-	**0**	1	A1	10
	0	-	**0**	0	A0	9
DATA	7	-	**1**	7	D7	26
	6	-	**1**	6	D6	27
	5	-	**1**	5	D5	28
	4	-	**1**	4	D4	29
	3	-	**1**	3	D3	30
	2	-	**1**	2	D2	31
	1	-	**1**	1	D1	32
	0	-	**1**	0	D0	33
(none)	-	P0	**0**	C/Q	ϕ2	39
	-	P2	**2**	C/Q	RDY	2

* Pod numbers are shown for a 1240 with a total of two acquisition cards installed. For each additional acquisition card installed, add 2 to the pod numbers given.