INDEX

M021

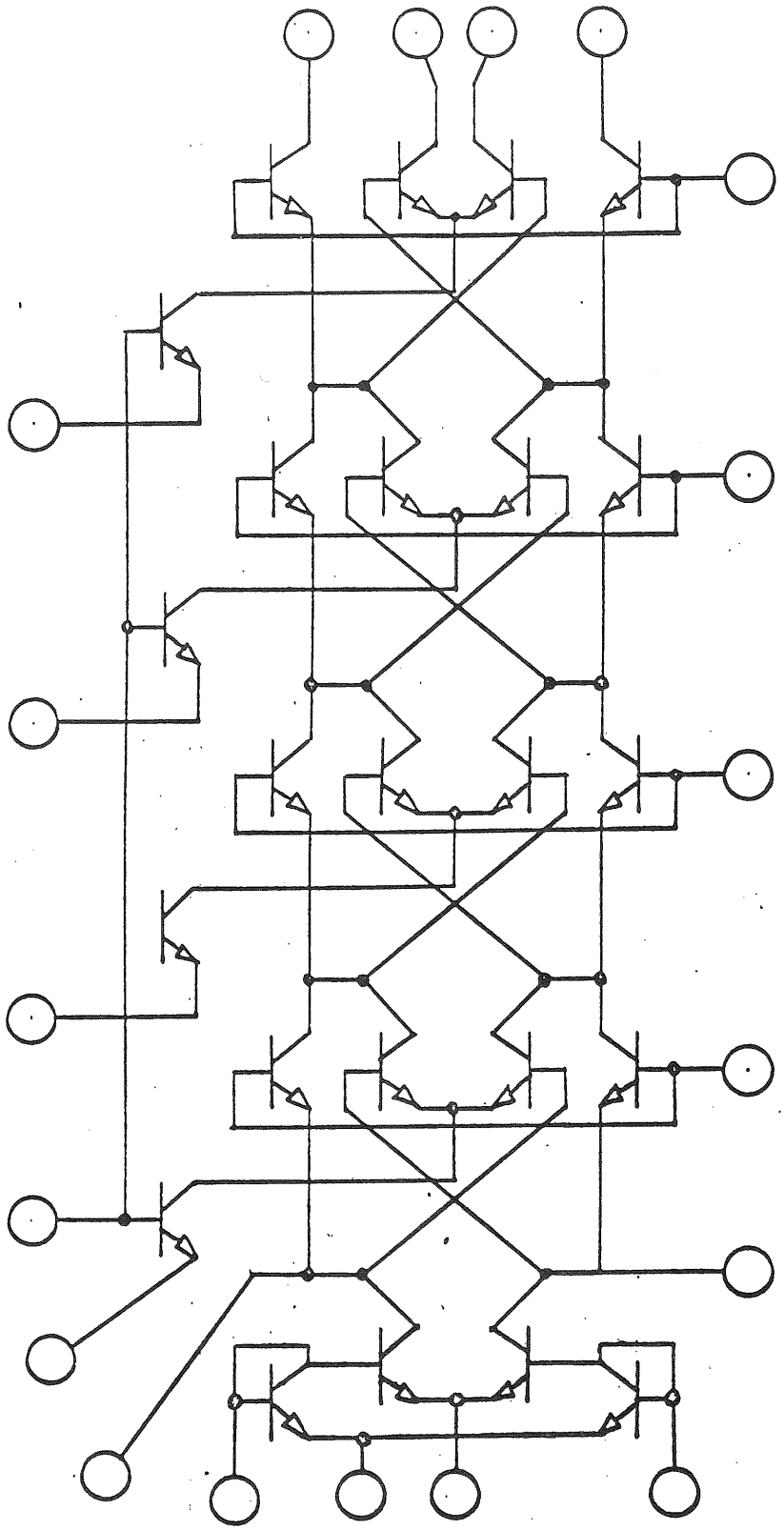
Gain Cell Amplifier

Description:

Consists of five stages on a 60 X 50 mil chip, with a variety of configurations possible. A breadboard resistor-patching area is included. In a typical configuration, a gain of X 25 with a bandwidth of D.C. - 300 MHz can be realized, with output swing of ± 50 mA into 50 Ω.

Designer:

Barrie Gilbert



M021 GAIN CELL

M013

Controlled Temperatures FET's

T05-10 pin

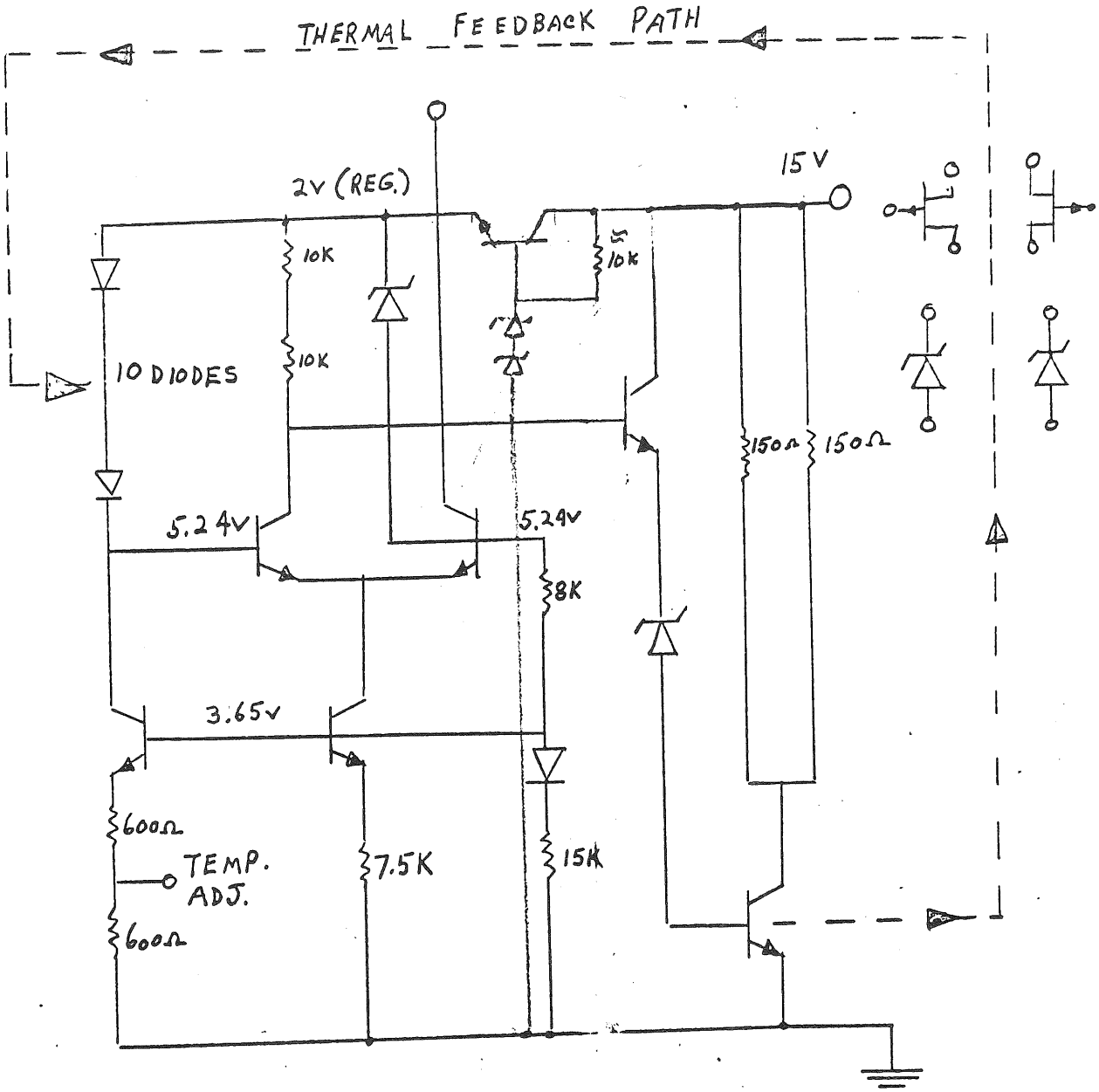
Description:

This circuit provides a constant temperature chip. On the chip is a matched pair of FET's and a pair of Zener diodes.

The temperature control is accomplished by balancing the inverse temperature characteristics of a Zener diode and a string of diodes, and detecting the off-set to activate a driver stage and increase the chip temperature. The chip temperature can be externally adjusted by changing the current through diodes. The nominal chip temperature is 80°C and has a thermal loop gain around 200.

Designer:

Einar Traa



M013

TEMP. CONTROLLED CHIP WITH FETS

M036

Channel Switch

Description:

This IC selects one or mixes two input analog signals in response to a digital input. In its simple application, it is a double-pole double-throw selector of one of two balanced input signals. Its more sophisticated role is in providing signal steering in dual-trace vertical and horizontal amplifiers.

It is designed for two balanced input signals of 25mV/division per side into 50 ohms per side (0.5ma/division). The 50 ohm terminations to ground are external to the package. A current gain of one is intended. The gain setting resistors are external to the package. Total dynamic range is ± 15 divisions (± 8ma).

The switch output is at a + 5V DC level. It is a current output which may be shifted back to 0 V DC level with a PNP stage or delivered directly into a resistance of 50 ohms per side. Side-to-side diodes are included inside the IC for limiting the differential voltage swing of the output. The risetime of the switch is less than 1 ns.

There are three signal selection input CH1 - CH2, OFF and ADD. The CH1 - CH2 input permits high speed switching between the two inputs suitable for "CHOPPED" or ALTERNATE operation at frequencies up to 1 MHz or greater. Drive levels are -0.5 V CH1 and +0.0 V CH1 into a high impedance. The OFF input inhibits both inputs from reachinf the output. Logic levels and input impedance are the

M036

Description: (Cont'd.)

same as the CH1 - CH2 selections with the OFF level being +1.0 volt. The ADD input requires a +5 volts input to sum the two input signals at the output terminals. The OFF mode supercedes the other two inputs while the ADD mode requires the other two inputs to be negative.

The common-mode current output of the signal channel is maintained constant for the various modes.

Characteristics:

Low frequency current gain ---------- 60 min

Low frequency α ---------- 0.94 min

Output impedance ---------- 100 kΩ nominal

Output current swing ---------- ±7.5 mA max

Input capacitance each side ---------- 2.3 pF nominal

Output capacitance each side ---------- 5.2 pF nominal

Switching time ---------- 20 ns maximum

Signal risetime ---------- 1.5 ns maximum
Rs = 100 R_e = 82 R_L <50

Differential DC offset ---------- 20 mV maximum
between modes

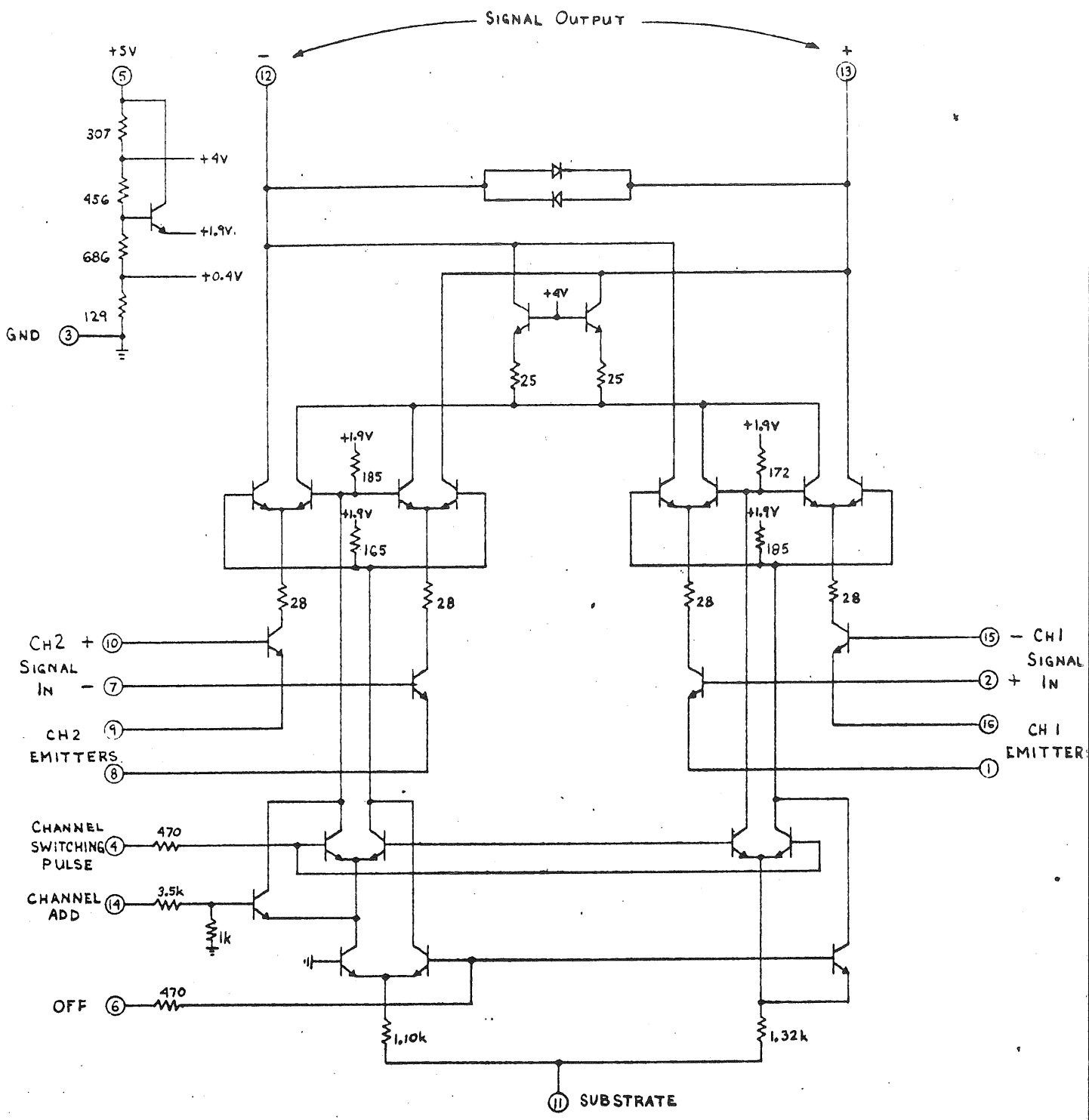
Gain difference between modes ---------- 0.5% maximum
A_I = 1

output current swing <±2.5 mA

Low frequency opposite channel ---------- 750:1 min
isolation F <10 kc

100 MHz opposite channel ---------- 100:1 nominal
isolation

Other characteristics are described in
the listing of the terminals



M 036 CHANNEL SWITCH~~ING~~

M045-01A

D-A Converter

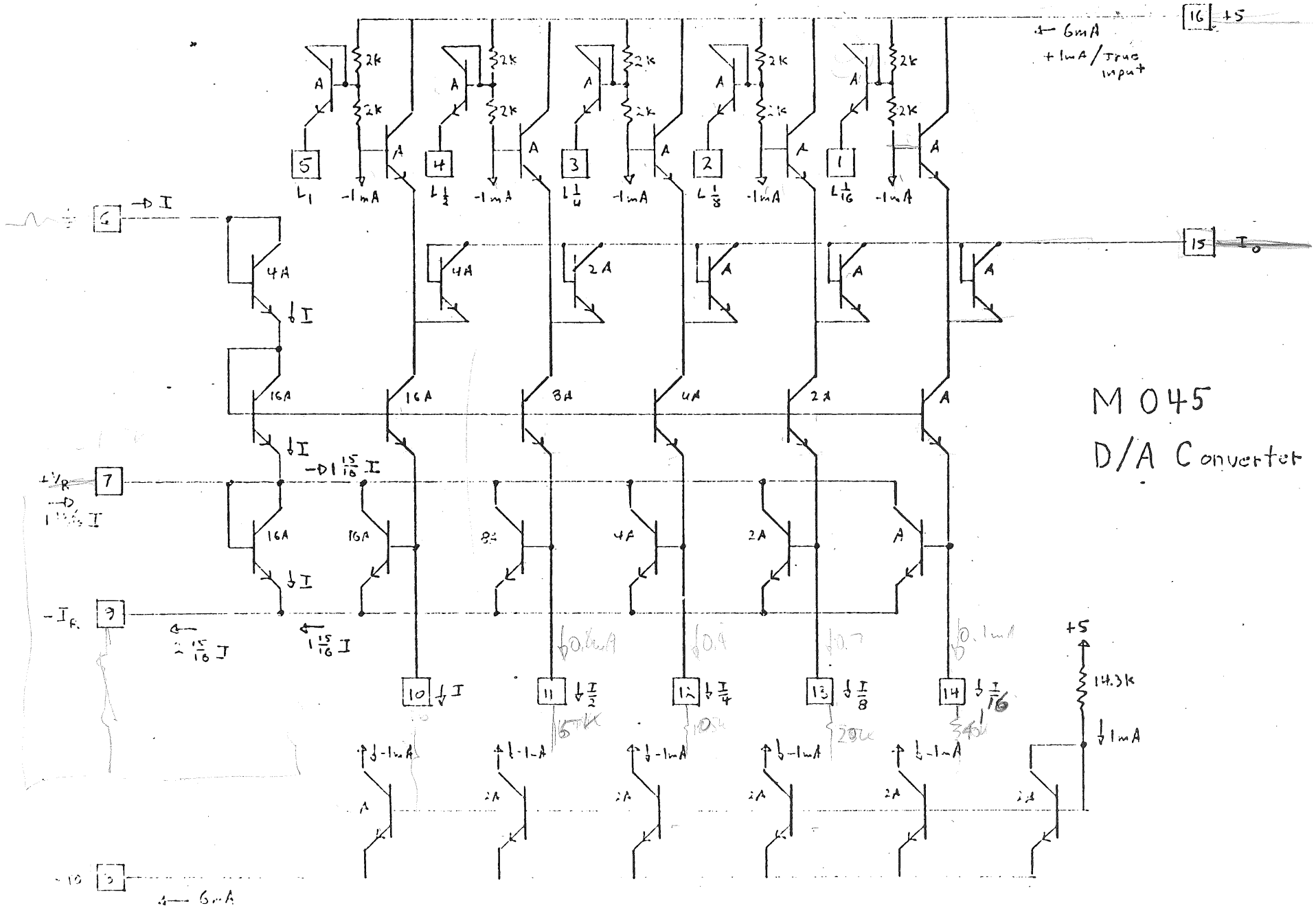
Description:

The M045 is a 5-bit precision current source digital to analog converter. The currents are set by external resistors between compensated voltage. The range of the MSB is 5 mA to 30 μA. Two packages may be used together for a 10-bit D/A with ± ½ LSB accuracy.

The output is designed to sum into 0 V. Power supplies are +5, -15 and a negative reference current of -I MSB.

Designer:

Mike Metcalf


M 045
D/A Converter
+5
6mA
+1mA/True input
-1mA
14.3k
1mA
-10
6mA

M048

Probe Power Supply

Description:

Provides +7 and -10 volts from ±12 to ±15 volts input voltages with an output impedance of less than 10Ω and temperature coefficient of less than two millivolts per ^{o}C. The supplies can deliver upwards from 100mW, depending on heatsinking and ambient termperature requirements.

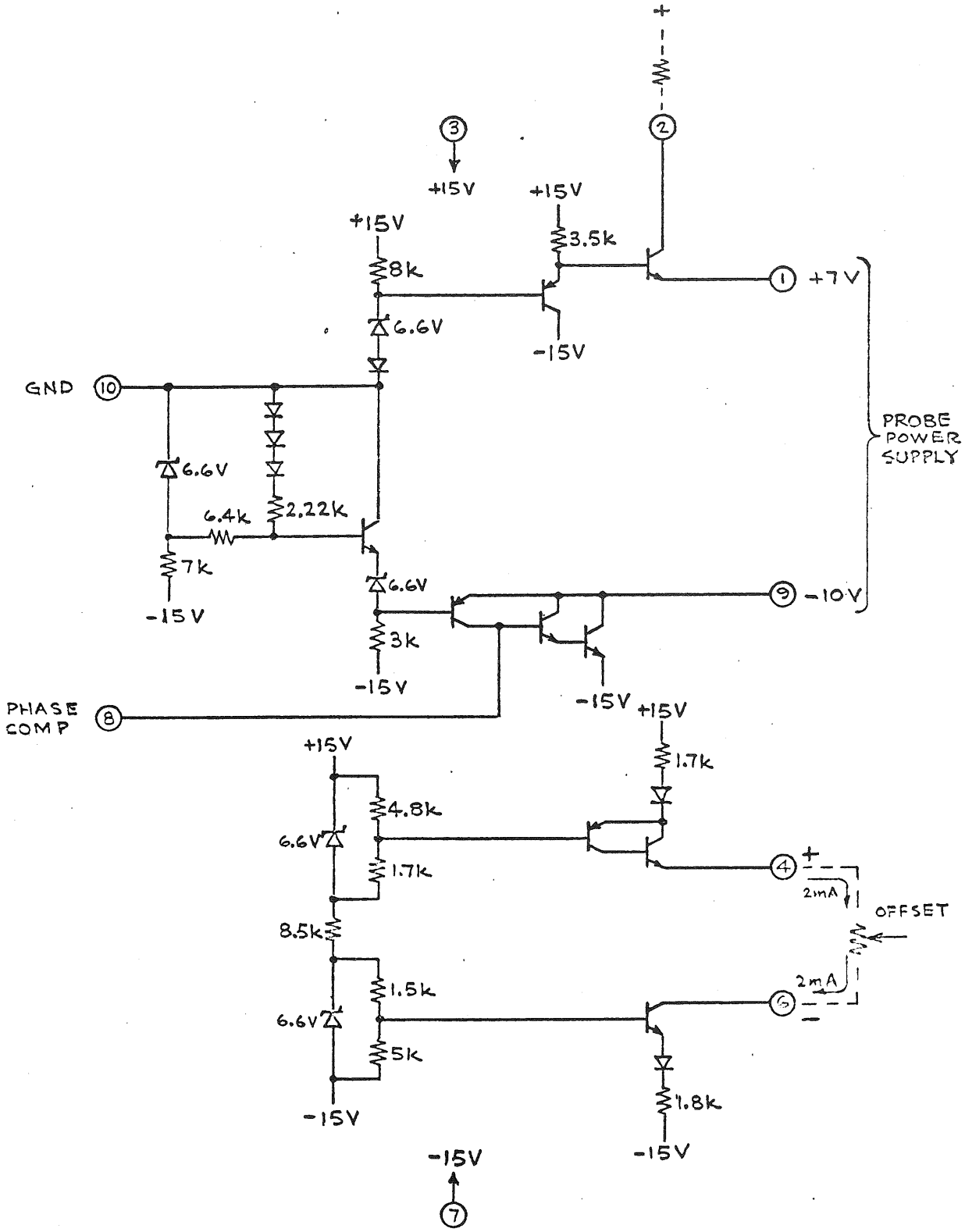
It also provides constant current sources of

+ 2mA @ V_6<+10 V and

- 2mA @ V_4<-10 V.

Designer:

Glenn Bateman



PROBE POWER SUPPLY

M048

M051

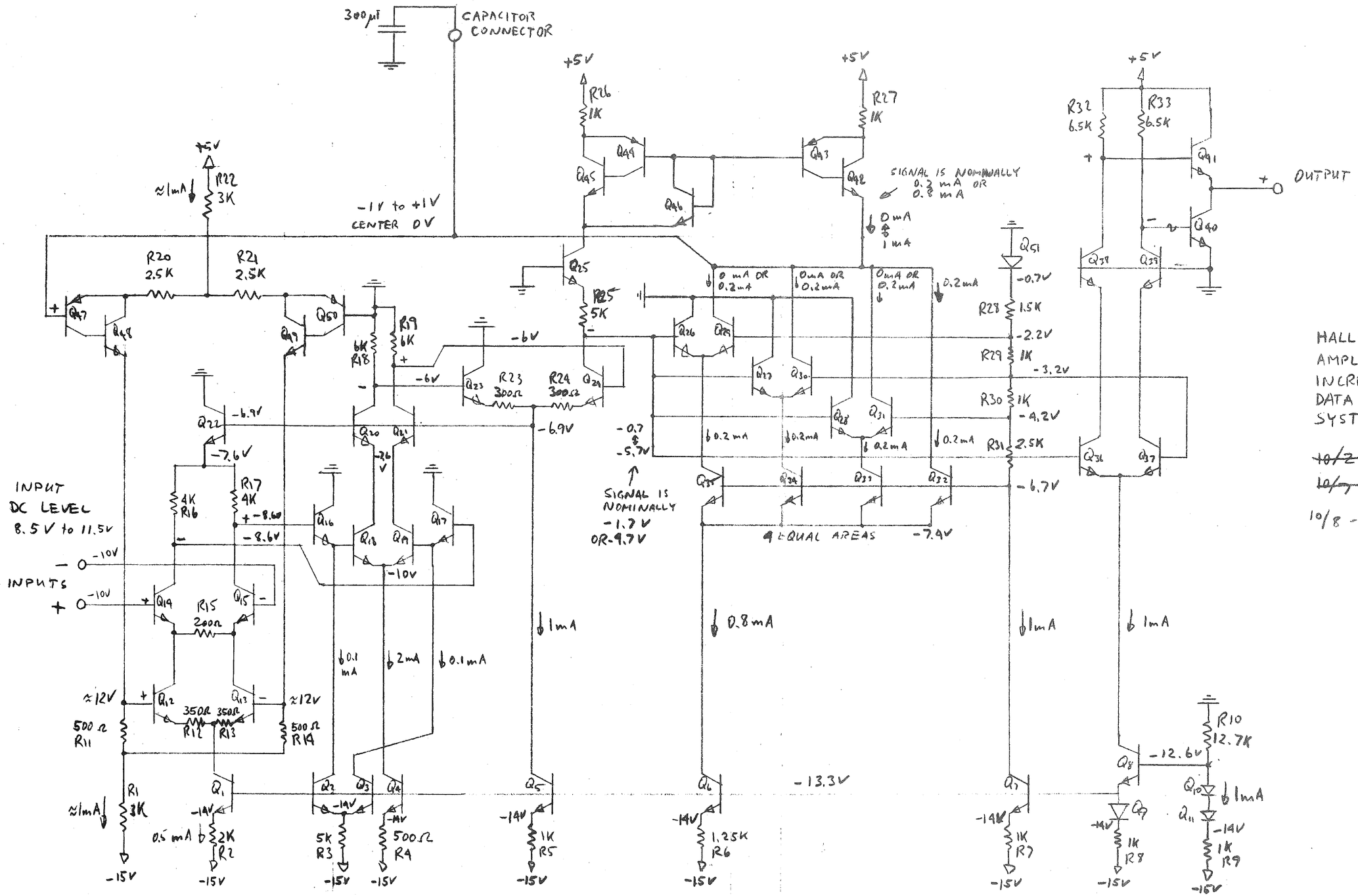
Hall Preamp

Description:

To be mounted in the tape read-head of an incremental data acquisition system. Amplifies a signal of ±200μV from a Hall effect transducer into standard logic levels of 0 V and +5 V. The negative integral of the difference between the closest standard logic level and the analog output is fed back to the input, thus rejecting slowly varying signals (drift) at the input.

Designer:

Einar Traa



HALL-HEAD AMPLIFIER FOR INCREMENTAL DATA ACQUISITION SYSTEM

~~10/2 - '68 E. Trac~~

~~10/7 - '68 E. Trac~~

10/8 - '68 E. Trac

M 051

M050

Dual Output Amplifier

Description:

Two variable gain amplifiers on a single chip. The input is a single-ended voltage and the output a differential current. Intended to be used as mini-scope output amplifiers. Electrical specifications are:

Gain: Adjustable from 0.5 to 5 mA/volt (current output)

Bandwidth: Determined by load and source impedances

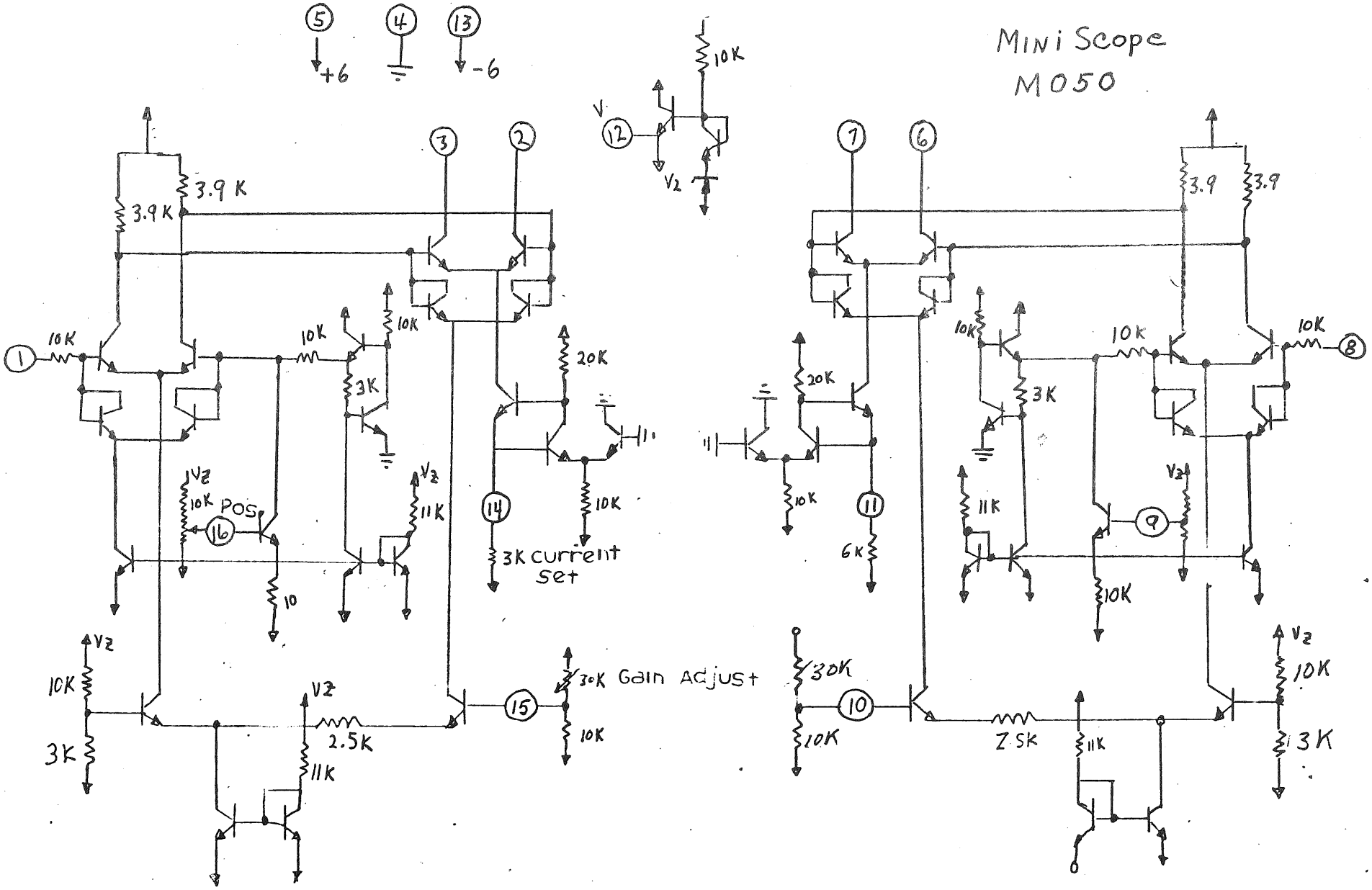
Input Impedance: 20 k

DC Balance: Adjustable internally over entire dynamic range

Designer:

David Allen

Mini Scope
M050



M023

Operational Amplifier

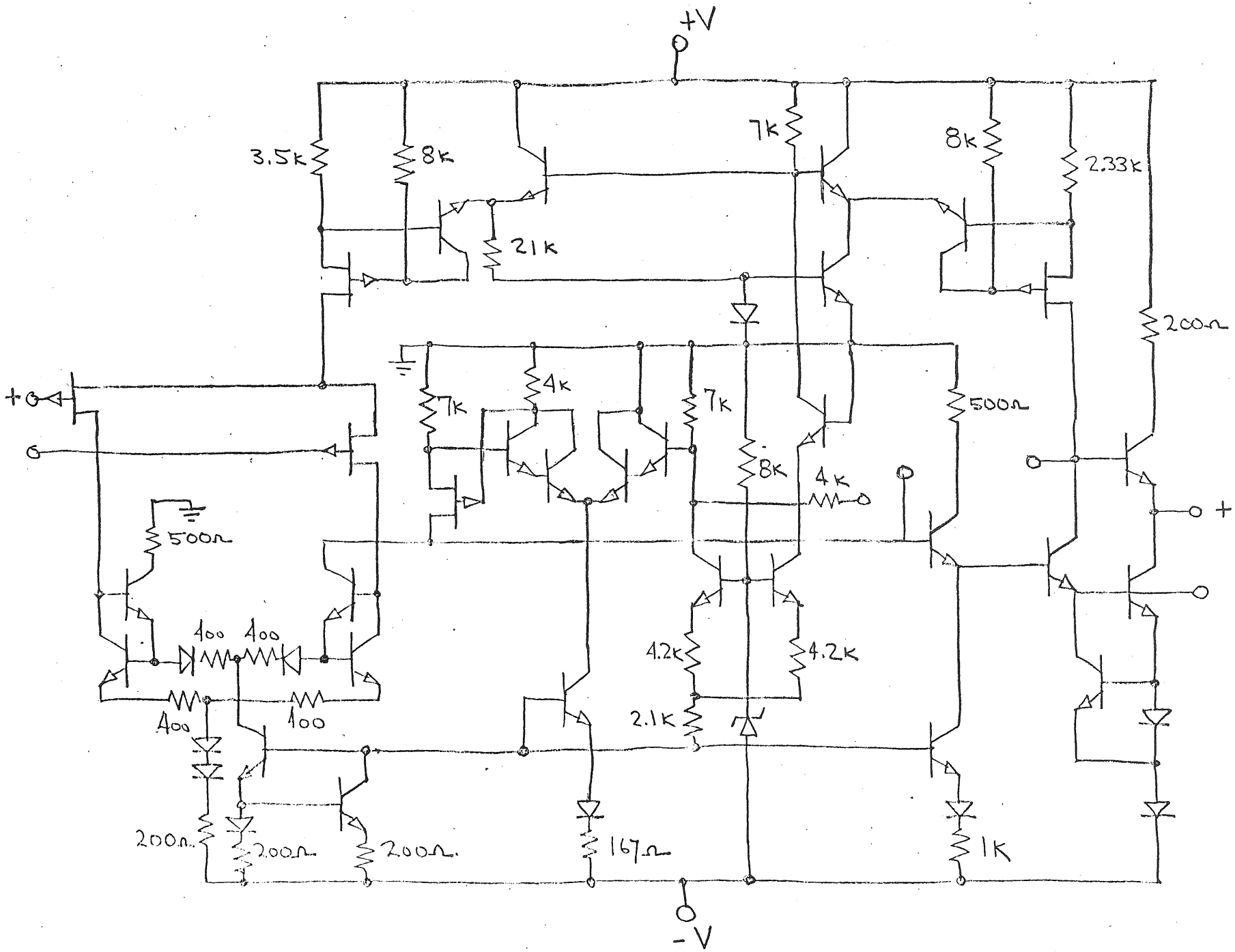
Description:

A general purpose Op Amp with FET inputs, a voltage gain of 50,000 input currents less than 1nA at 25°C, CMRR of 3000 and a unity gain bandwidth of 50 MC. It can be compensated to unity gain with a single 10 pF capacitor.

Designer:

George Wilson

M023


+V
3.5k
8k
21k
7k
8k
2.33k
200Ω
4k
7k
7k
500Ω
8k
4k
+
500Ω
400
400
400
100
4.2k
4.2k
2.1k
200Ω
200Ω
200Ω
167Ω
1k
-V

M049

Dual Operational Amplifier

Description:

Two operational amplifiers with FET inputs on a chip. Input currents are less than 1 nA. The primary function of this circuit is a vertical input amplifier for the miniscope. The first half being switch attenuated for vertical sensitivity, and the second half as a X20 buffer amplifier.

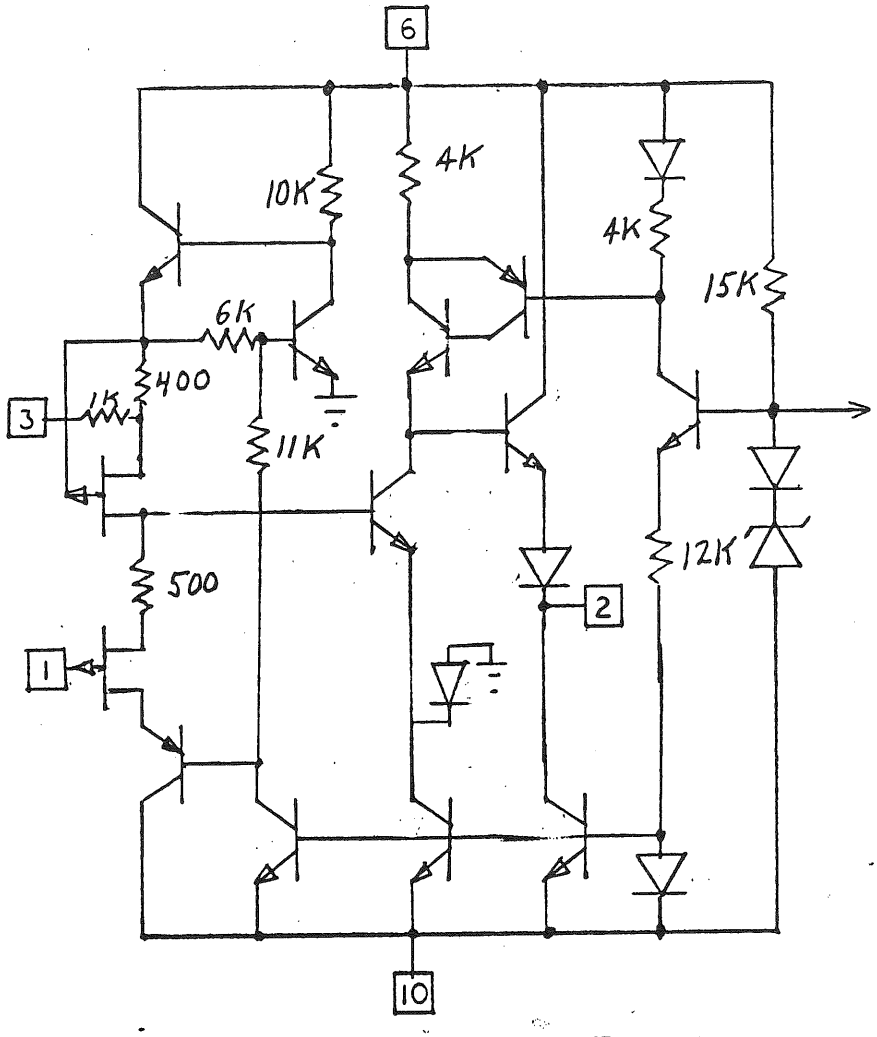
Characteristics:

Power Dissipation	150 mW maximum
Power Supplies	± 6 V with ± 1 V toll.
Output Voltages	2 V to +3 V minimum
D.C. Balance	100 k pot to ground
Open Loop Gain	1000
Gain B.W.	20 JHz

Designer:

Dave Allen

M049
DUAL OP AMP



AMP NO. 2 MIRRORED

GROUND	PIN 4
+6V	6
−6V	10
INPUTS	1&9
OUTPUTS	2&8
D C BALANCE	3&7

M053

Quad Operational Amplifier

Description:

Four operational amplifiers on a chip with the following specifications:

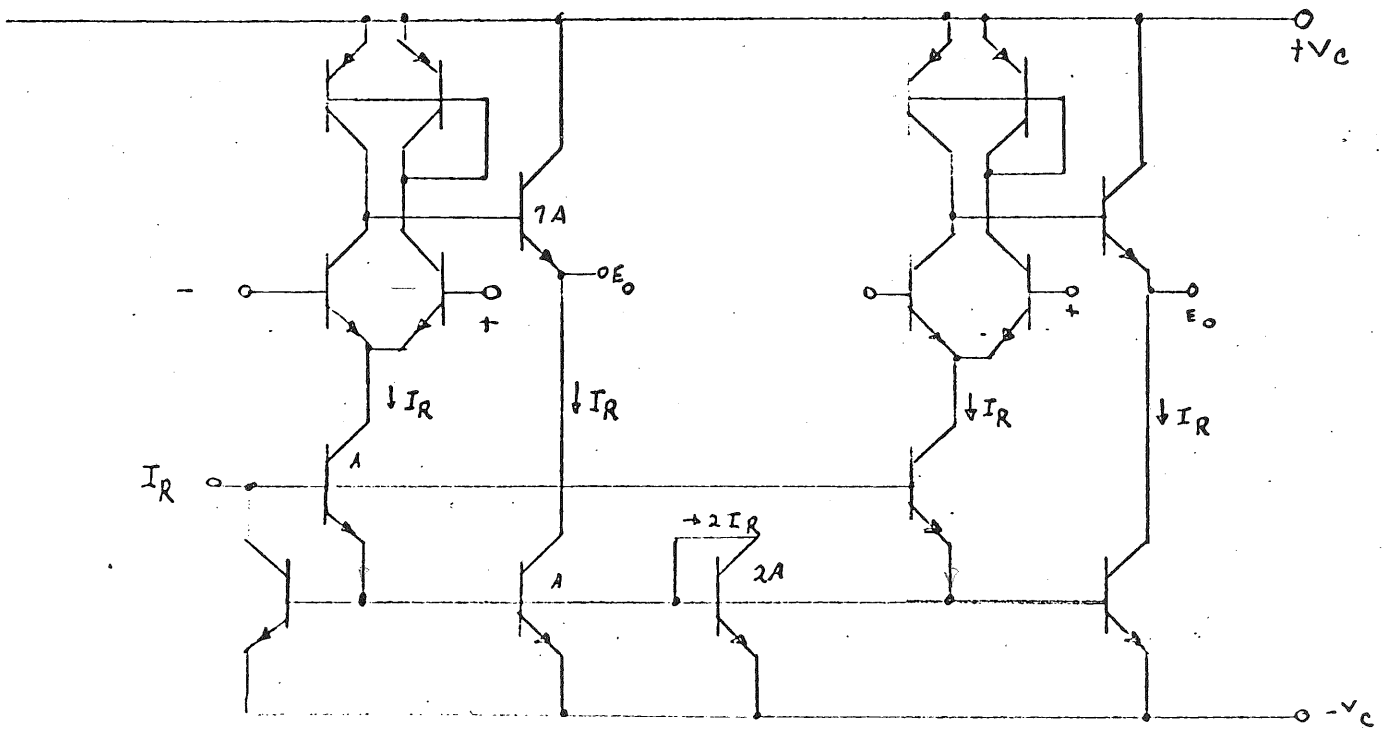
Power Supplies	± 5 to ± 15 V
Open Loop Gain	$\geq$ 1500
Gain Bandwidth	$\geq$ 80 MHz
Input Offset	$\leq$ 1 mV
Output Swing	- 0.7 V w.r.t. input level to $+V_C$ - 1.5 V
Maximum Output Current	20 mA

The amplifier is stable in all modes without external compensation.

Disgner:

Mike Metcalf

M053 Quad Op-Amp



PIN	FUNCTION
1	Output A
2	- Input A
3	+ Input A
4	Ref I, A · B
5	+ B
6	- B
7	O B
8	- Vc
9	O C
10	- C
11	+ C
12	I_R, C · D
13	+ D
14	- D
15	O D
16	+ Vc

M052 CONTAINS TWO OF ABOVE CIRCUITS

Reference Circuit = $E_{REF} - (-V_{cc} + 2\phi)$

$E_{REF} + V_{cc} - 2\phi$

M001

Horizontal Lockout Logic

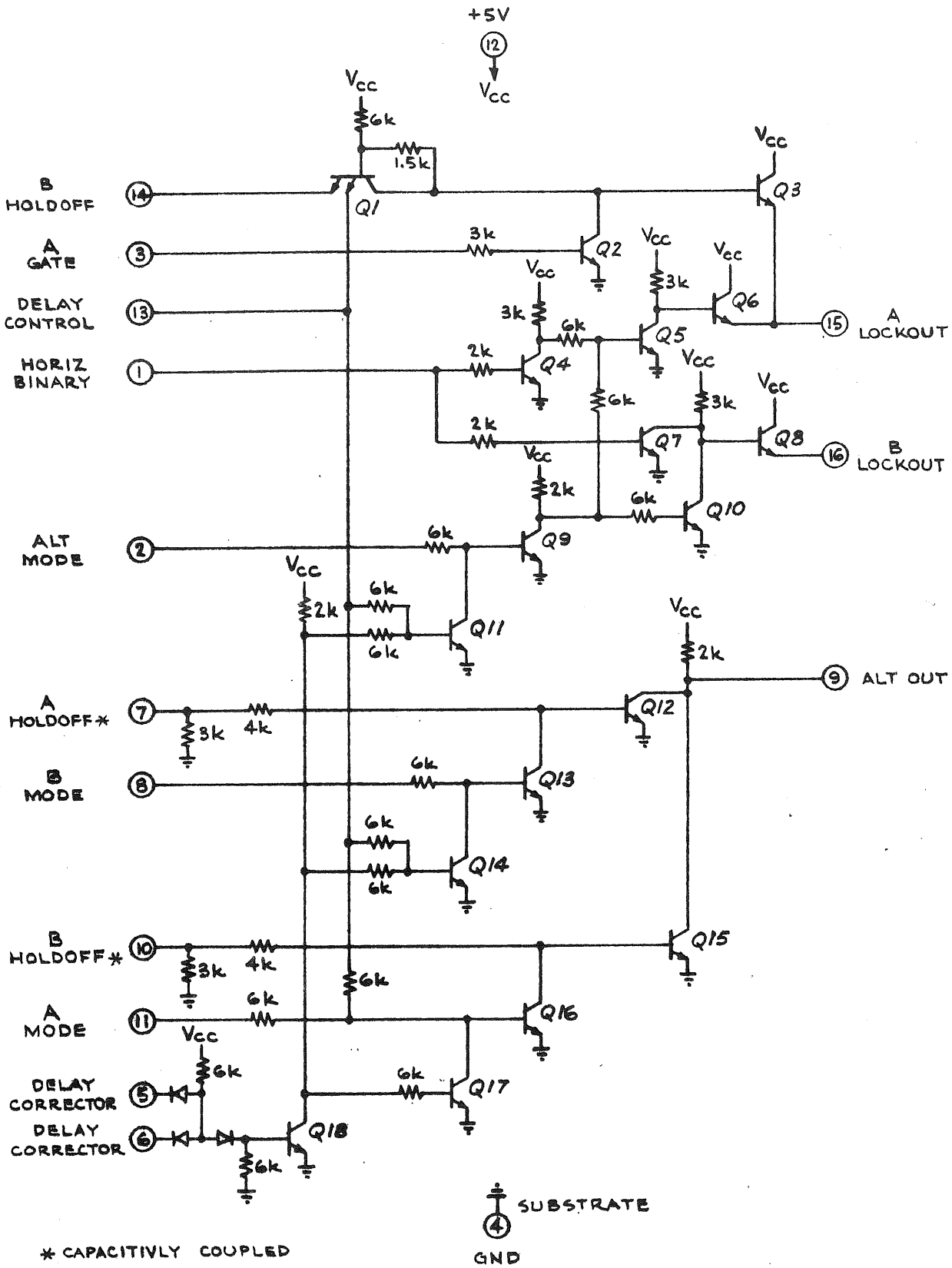
16 pin dil.

Description:

The horizontal lockout logic receives inputs from the horizontal chop and alt. binary, A sweep delay control, A sweep gate, B sweep holdoff and B sweep gate. Logic is performed on these signals to provide lockout for A sweep or B sweep and alternating signals for the horizontal chop and alt. binary.

Designer:

Les Larson



HORIZONTAL LOCKOUT

M001-A

M004

Chop Divider and Blanking (Type 3)

Description:

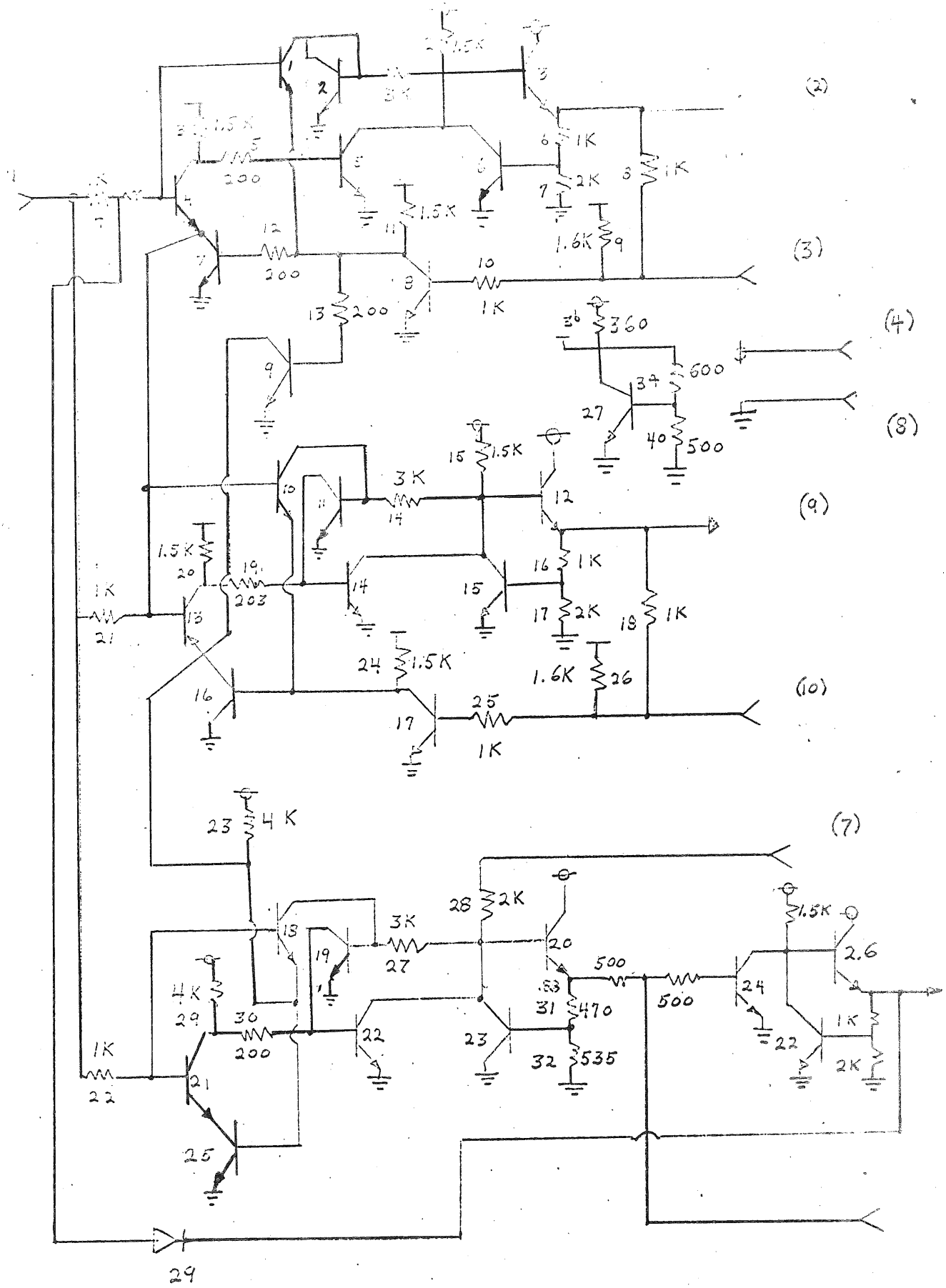
The chop divider receives a clock signal from the chop decoder and blanking circuit and counts it down by two for the vertical switch chop, and by four for the plug-in chop. It also provides a horizontal chop blanking pulse if the horizontal mode switch is in chop.

Designer:

Les Larson

CHOP COUNTER

M004



M012

Clock and Chop Blanking

16 pin dil.

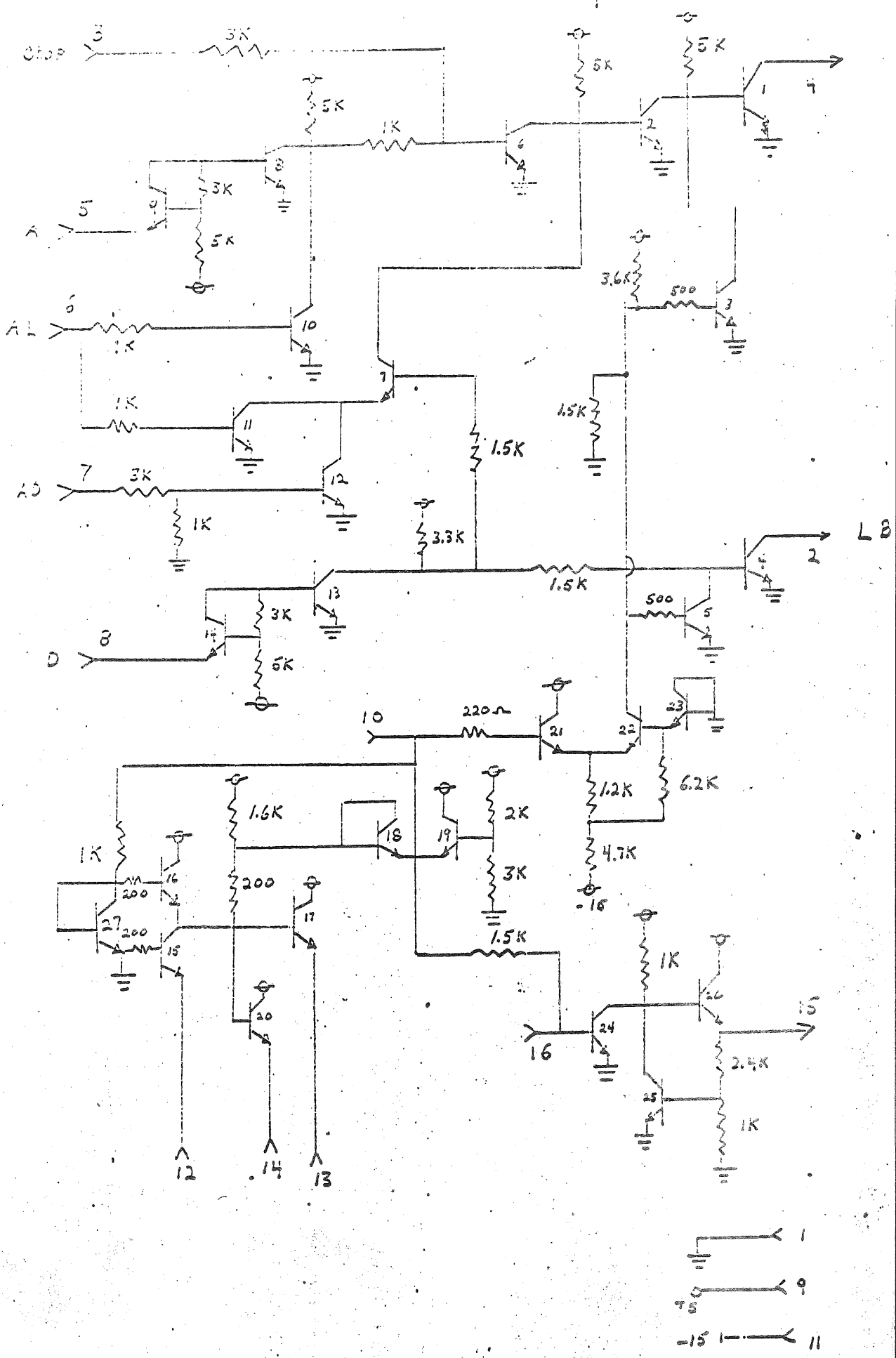
Description:

This IC generates the 2 MHz chop clock signal for triggering the chop counter (M004) as well as the chop blanking waveform. The blanking waveform can be delayed in time and varied in width over a certain range to accommodate different delay lines. It also has fine logical inputs which are the plug-in and mainframe modes that are used to decide if chop blanking should be used at a certain time.

Designer:

Les Larson

M012 Clock + Blanking



M015

Z Axis Logic

Description:

This IC is a signal conditioner for the main Z axis amplifier.

It is under control of the horizontal switch drive. A gate, B gate, delay control, A intensity control and B intensity control. With these signals, it properly selects at one output either A intensity, B intensity or A intensified by B for delaying modes.

Additional functions are chop blanking for vertical and horizontal, external and plug-in Z axis input, and fast limiting of the composite signal. The signals are further limited at slow sweep speeds to prevent burning of the CRT.

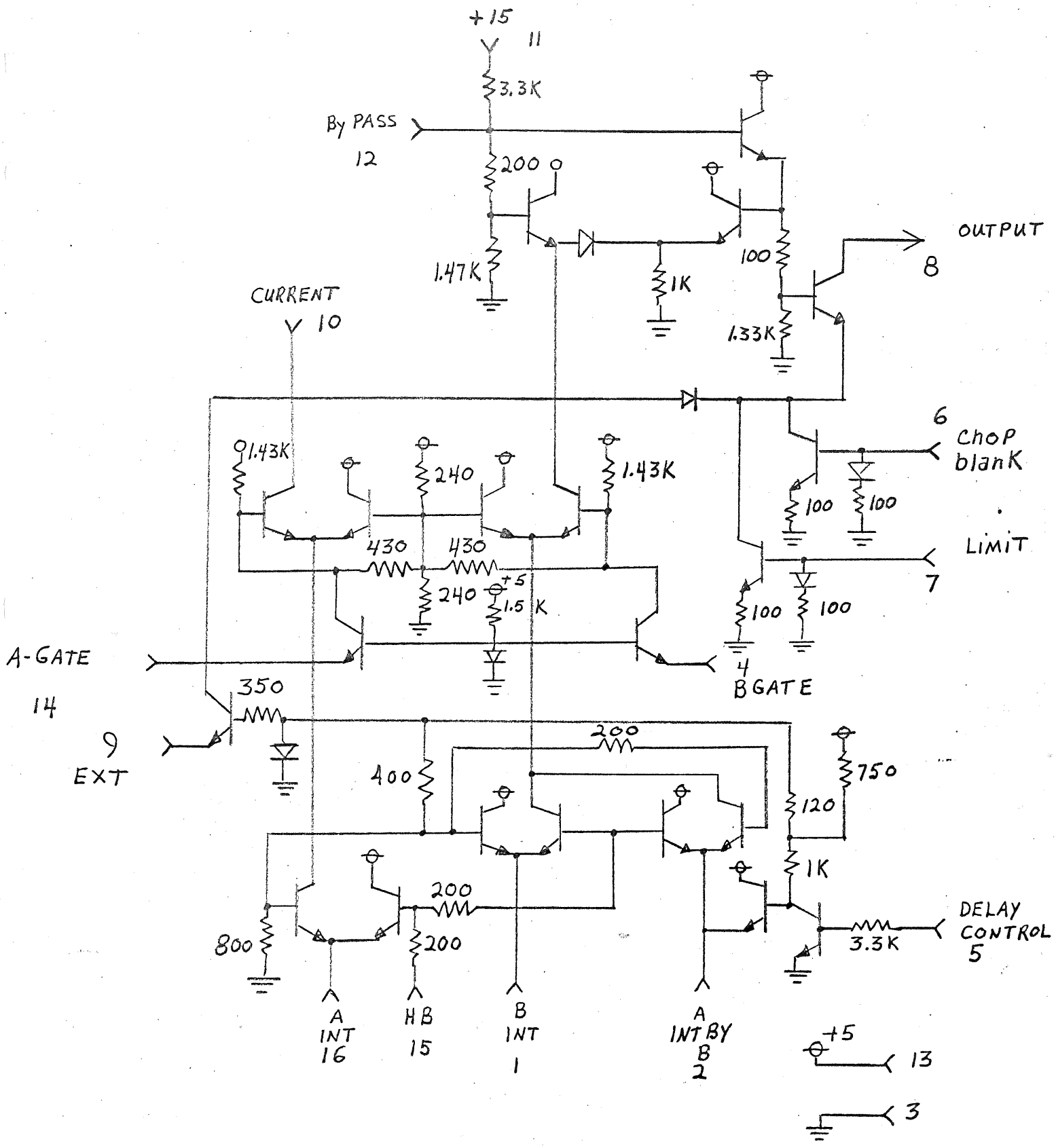
Designer:

Les Larson

IC 5 Z-AXIS LOGIC

M015 B

3-11-69



M022

Horizontal Chop & Alt. Binary (Type 2)

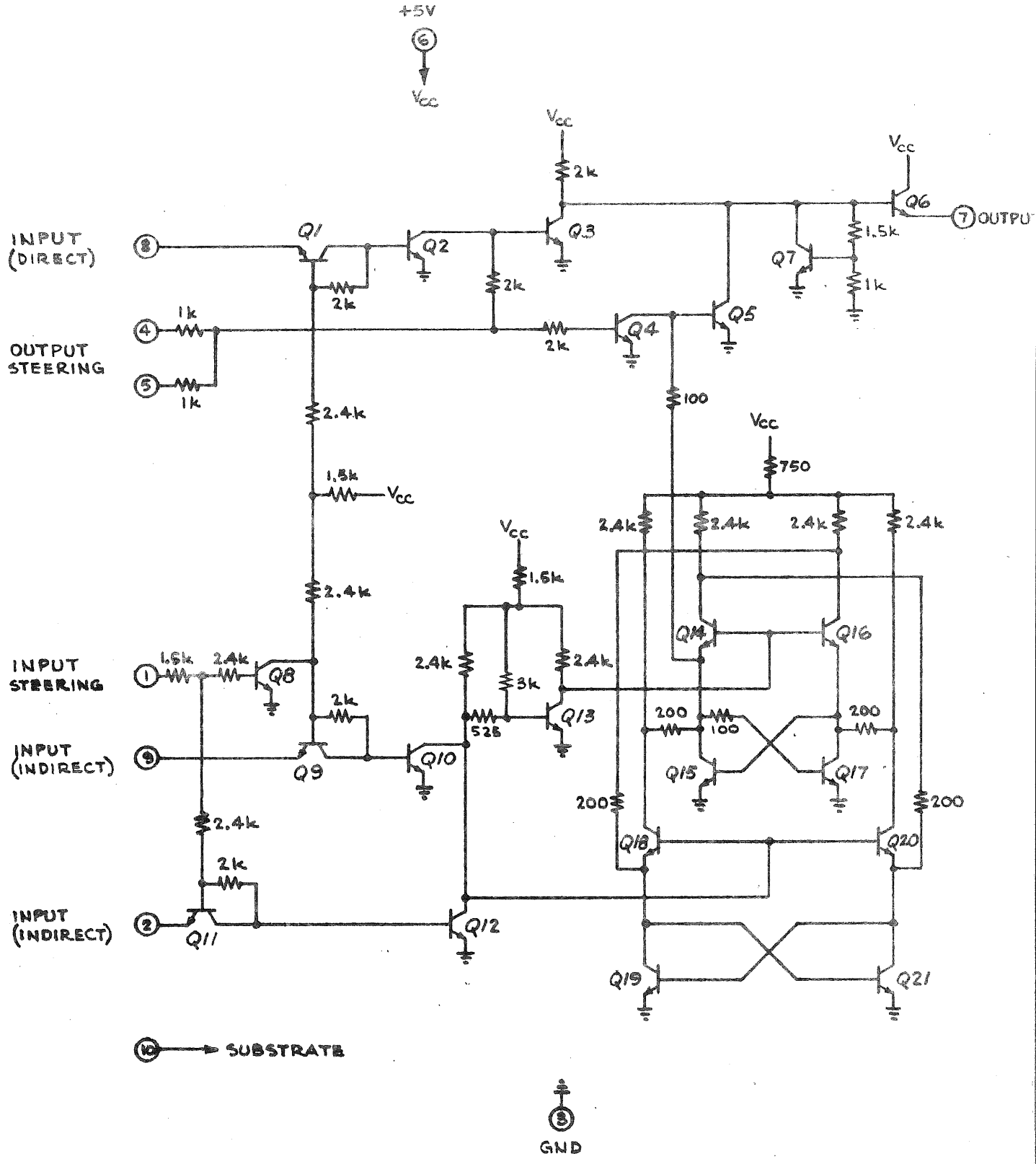
T05-10 pin

Description:

This circuit receives horizontal mode switch information, alternating signals, chopping signals (.5 MHz) and produces an output to the horizontal switch as to which sweep should be received. This same output is used in the horizontal lockout logic and in both vertical alt. binaries.

Deisgner:

Les Larson



M022 DC BINARY

M009

Lamp Logic

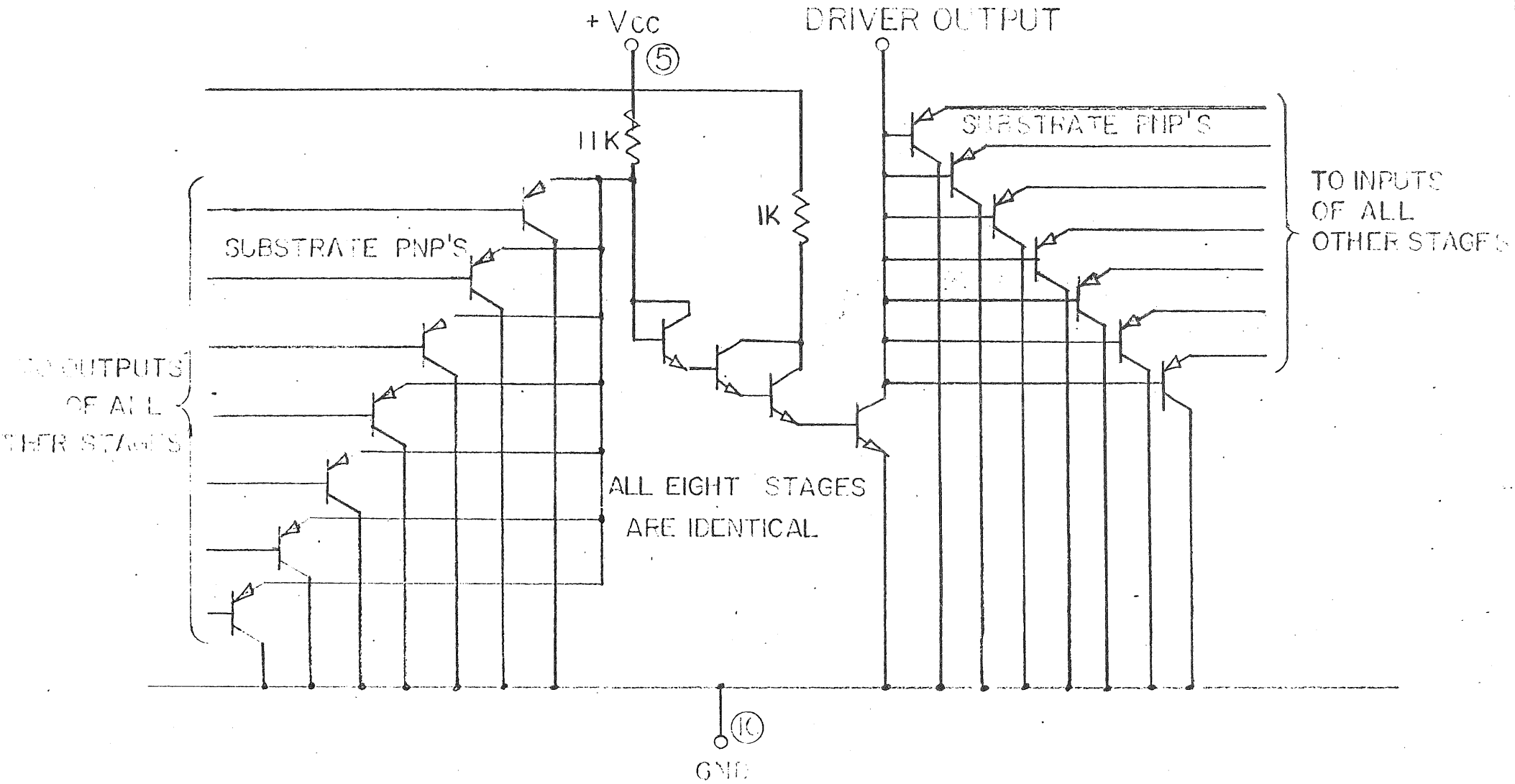
T05-10 pin

Description:

An eight-stable circuit capable of driving any one of eight output transistors. The output devices are capable of delivering 100 mA with less than one volt VCE. The circuit is switched by momentarily grounding the appropriate output collector. The same circuit is also available in a two four-stable version.

Designer:

George Wilson



MOOD LAMP LOGIC

M030

Lamp Logic, 4-Stable

T05-10 pin

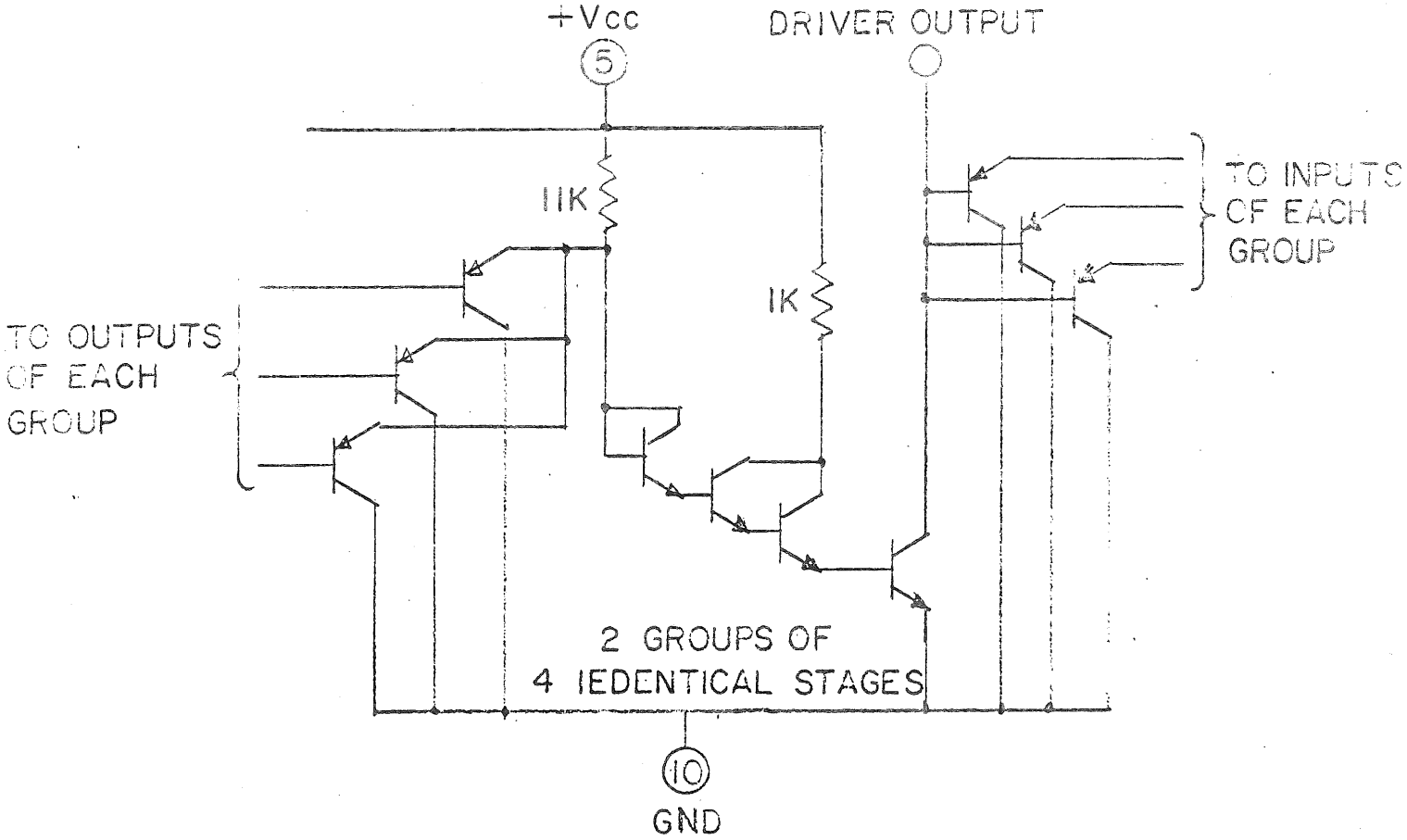
Description:

Two four-stable circuits, each circuit controls four output transistors capable of delivering 100 mA at less than one volt VCE. Maimum supply voltage is 10 V. The circuit is switched by momentarily grounding the output collector to be turned on.

Designer:

George Wilson

MO30
LAMP LOGIC 4 STABLE



GROUP PINS
1-2-3-4
6-7-8-9

M031

Lamp Logic, 2-Stable

T05-10 pin

Description:

Four groups of 2 lamps. First group pins 1-2, second group pins 3-4, third group pins 6-7, fourth group pins 8-9.

Maximum saturation resistance is 6 Ω.

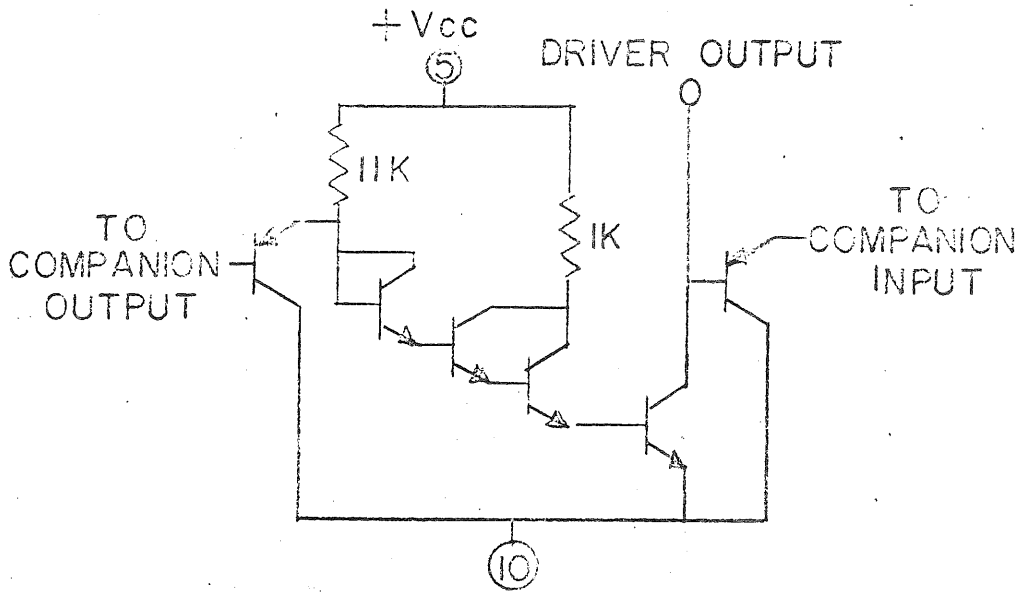
Maximum loads 60 mA.

This chip contains four bistable circuits. Each circuit controls two output transistors capable of delivering 100 mA at less than 1 V VCE. Maximum supply voltage is 10 V. The circuits is switched by momentarily grounding the output collector to be turned on.

Designer:

George Wilson

M031
LAMP LOGIC, 2 STABLE



GND
LAMP GROUPS
PINS
1&2 , 3&4
6&7 , 8&9

M019

Analog to Decimal Converter

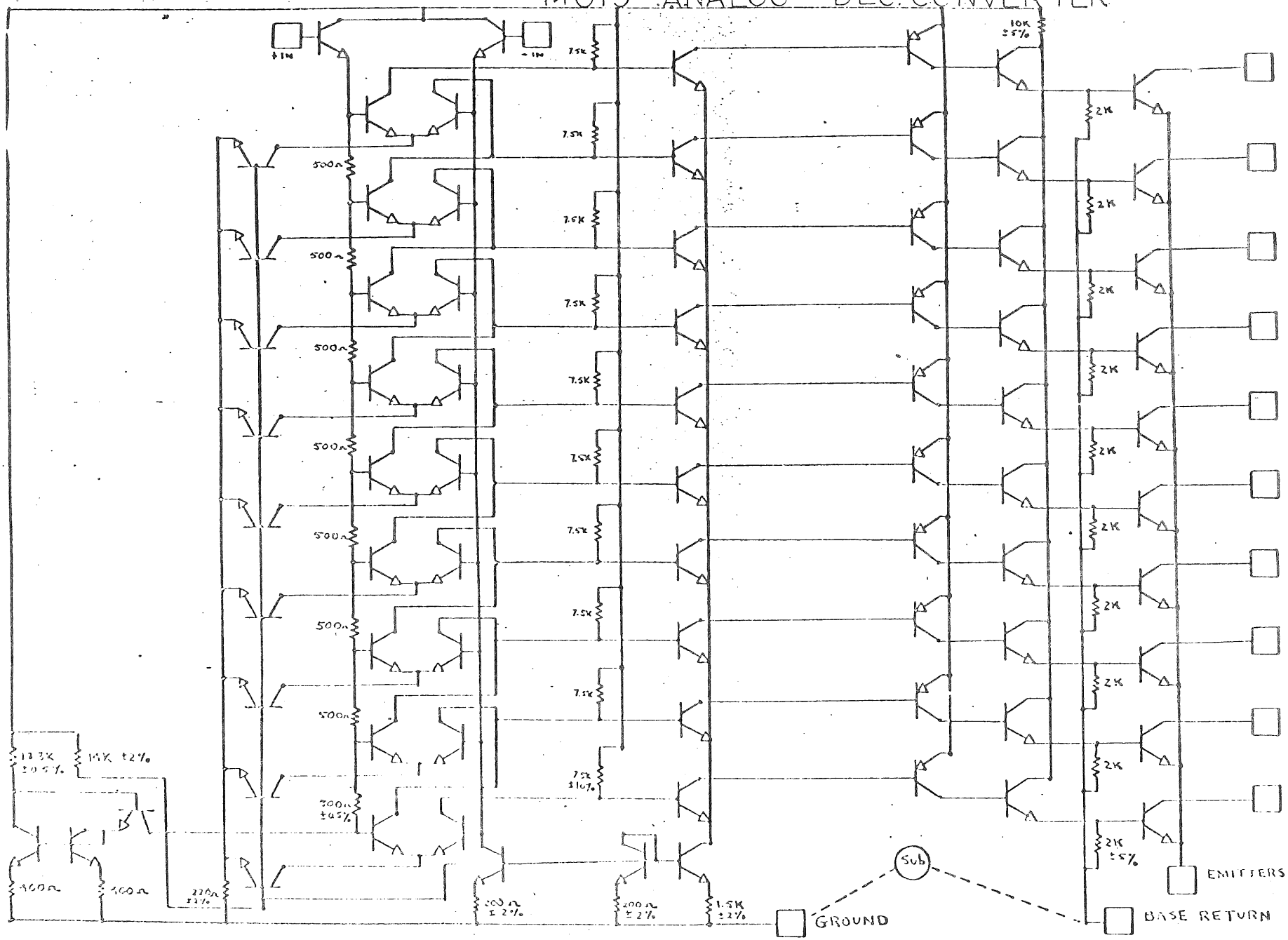
Description:

Operating with a single 15 V supply, the M019 converts differential analog input voltage to one of ten output indications, with a transition spacing of 500 mV ±2% and a transition zone of less than 5 mV. The outputs may be wired as current steering, in which case, one of the circuit terminals accepts the current input, or in the form of saturated transistors. Ratings of the output circuits are presently 15 V and 25 mA.

Designer:

Barrie Gilbert

M019 ANALOG – DEC. CONVERTER



M020

Data Switch

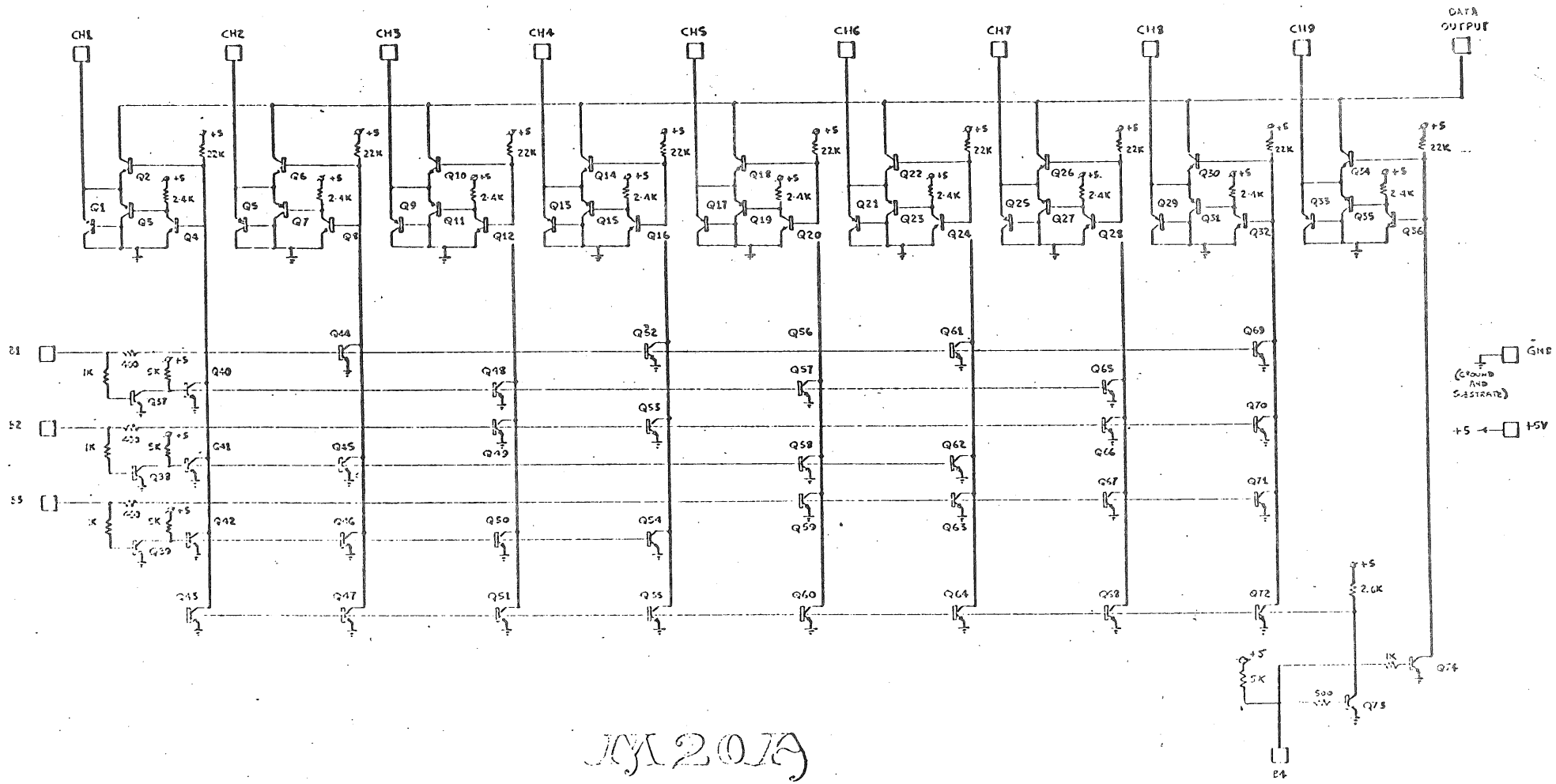
Description:

A current-steering switching circuit designed specifically for the knob-readout system.

Accepts nine inputs @ currents in the range 0 - 1 mA and selects one under the control of a BCD code. The output is from an NPN collector. The inputs are virtual grounds within ± 100 mV of ground potential for input ranges of ± 1 mA.

Designer:

Barrie Gilbert



M20A

DATASWITCH

M024

Character Generator

16 pin dil

Description:

To generate the X- and Y- waveforms corresponding to ten different alphanumeric symbols, under control of an external scanning voltage. There are four different sets of symbols, designated by the suffixes -N (numbers), -L (letters), -S (symbols) and -P (prefixes).

Designer:

Barrie Gilbert

M24B Character Generator (Approx. Circuit)

M025

Decade Counter

Description:

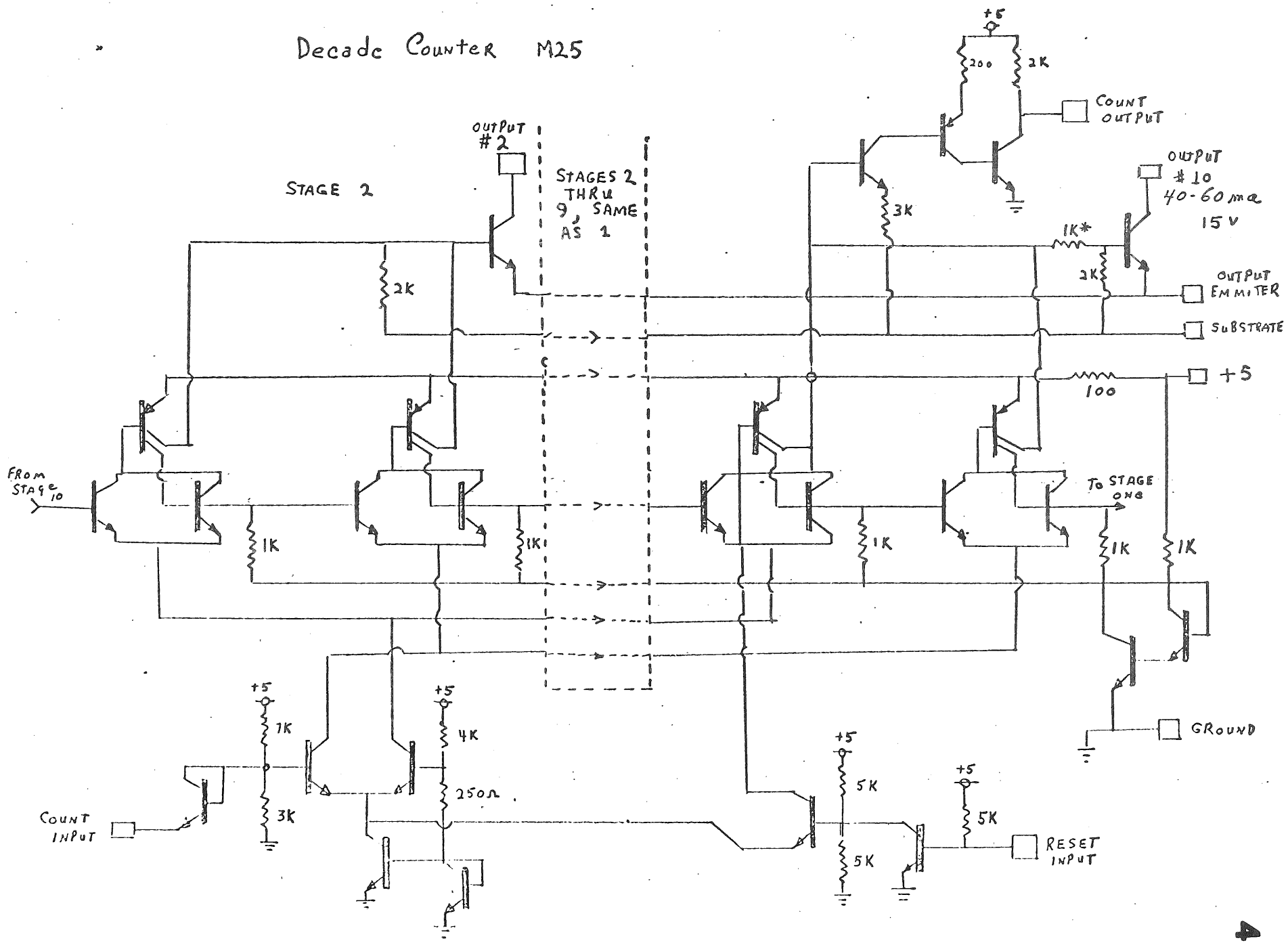
General.

The M025 is a decade counter having power-handling output capabilities, and all ten outputs brought out to pins. It features an auxiliary count output pin, a reset input and versatile operating modes. The nominal supply voltage is 5 V, but operation is stable from 3 V to over 8 V. Count input rates up to 5 MHz are acceptable.

Designer:

Barrie Gilbert

Decade Counter M25



M026

Zero Logic

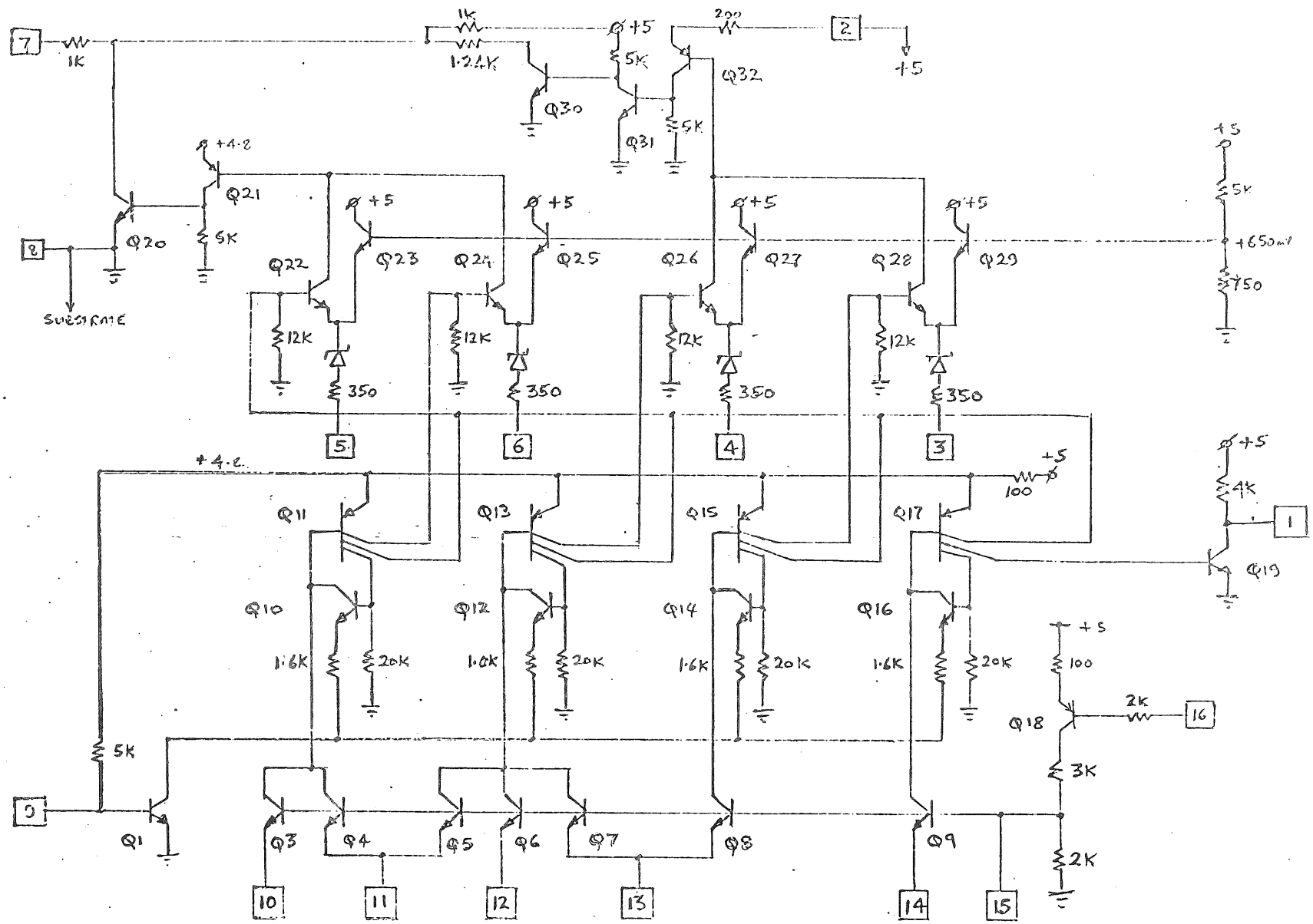
Description:

General

The M026 is a special-purpose circuit for use in the new-generation knob-readout system. It comprises an input logic section, four memory cells, an output logic section and a binary-to-ternary conversion stage. It uses a single +5 supply.

Designer:

Les Larson


7
1K
1K
1.24K
+5
5K
200
2
+5
Q30
Q31
Q32
5K
+4.2
Q21
Q20
5K
8
SUBSTRATE
+5
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
12K
350
5
6
4
3
+5
5K
+650mV
750
+4.2
100
Q11
Q13
Q15
Q17
Q10
Q12
Q14
Q16
1.6K
20K
1.0K
+5
4K
1
Q19
+5
100
Q18
2K
16
3K
2K
5K
9
Q1
Q3
Q4
Q5
Q6
Q7
Q8
Q9
10
11
12
13
14
15

M26

M027

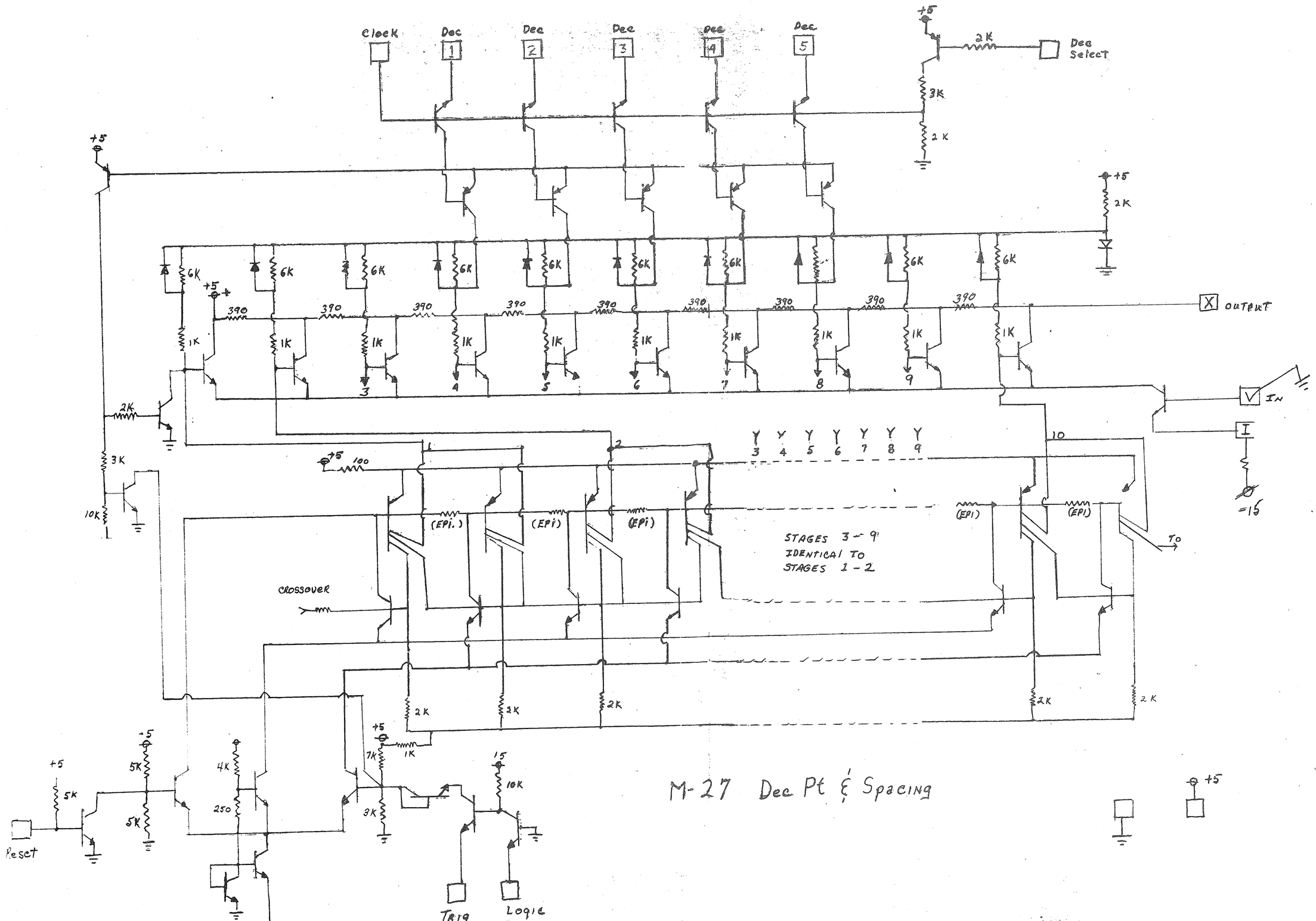
Decimal Point & Spacing

Description:

To produce a positioning signal (10-level staircase) for the new generation readout system, and also position the decimal point. Consists of a decade counter, digital-to-analog converter, input logic.

Designer:

Les Larson



M-27 Dec Pt & Spacing

M028

Output Assembler

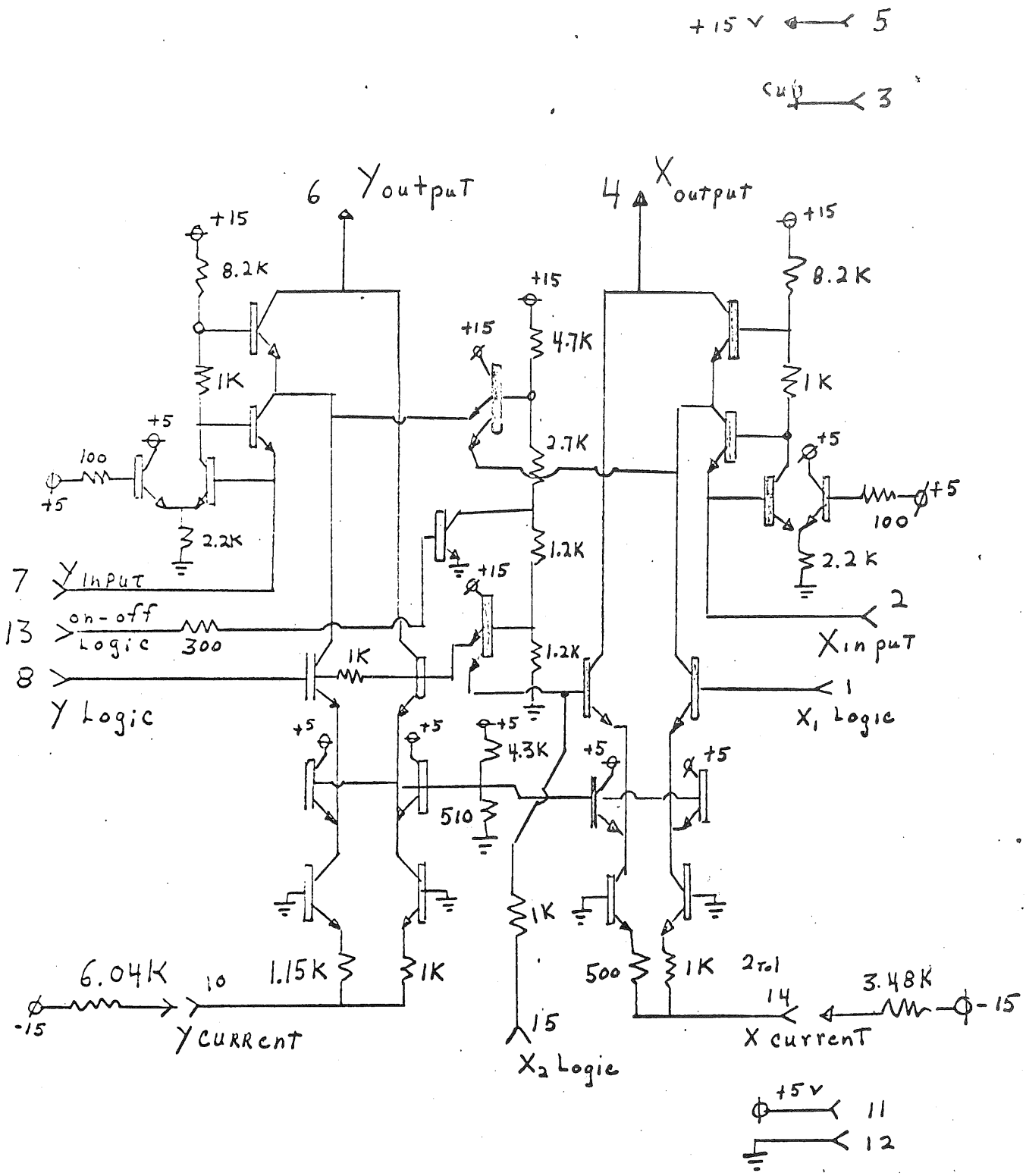
Description:

Produces a display format signal (X- and Y- waveforms) from binary and analog input signals. Part of new generation readout system.

Designer:

Les Larson

Output Assembler M028



M029

Timing Generator

Description:

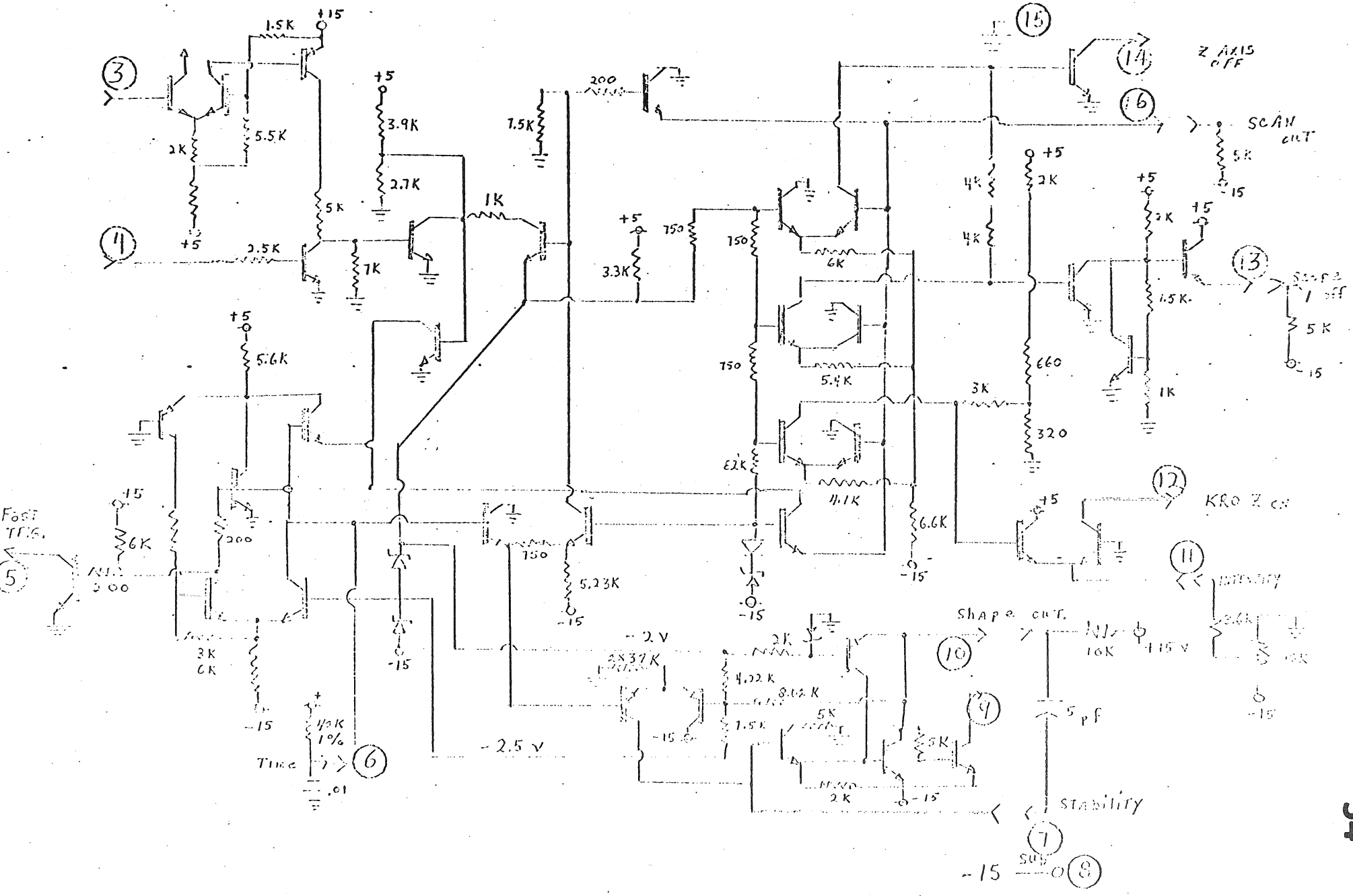
Generates a timing clock, a shaped negative pulse for the M025, a scanning ramp for the M024, the X-Y on off and intensity controls for the Z axis.

Designer:

Les Larson

+5 — (1)
+15 — (2)

TIMING GENERATOR M029



M047

Quad Timing Unit

Description:

Generates four separate and independent timing intervals.

Input Required: Positive voltage greater than 0.9 V at a current greater than 20 μA. Two units have a single input - pin 6 and pin 10. The other two units have OR gates - pin 2 or pin 3 and pin 13 or pin 14.

Output Available: During the timing interval the output is at 5 V through 5 kΩ. During the off period the output will sink 10 mA below 0.9 V.

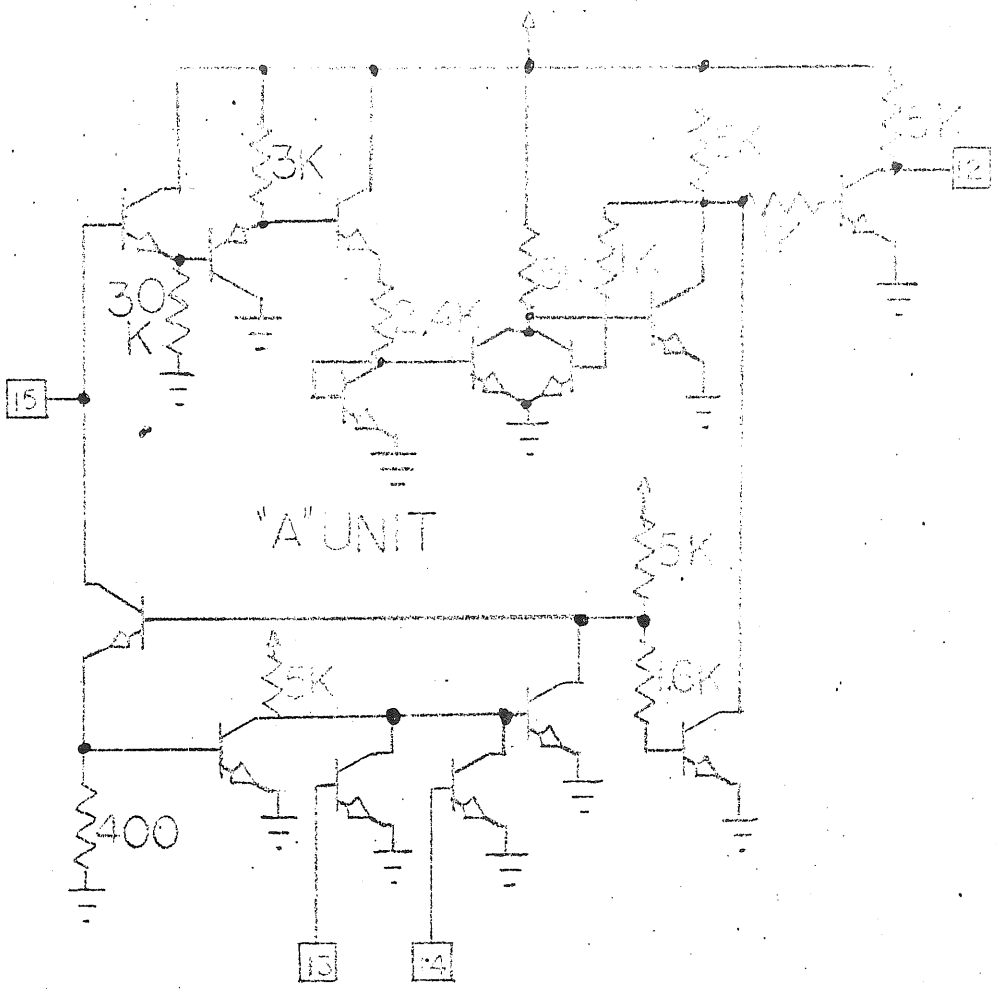
RC Required: Resistor should supply no more than 750 μA. Allow 5 μA for the operation of the IC. For narrow input pulses (less than 0.5 ms per μF of capacitance) the timing ramp will occur from 1 V to 3.6 V. Wider input pulses will change the ramp to 0 V to 3.6 V.

Operation: The circuit is a pulse stretcher in operation. The output will remain positive for a time set by the width of the input pulse plus a timing interval set by an RC.

Designer:

Mike Nash

QUAD TIMING UNIT



PIN CONNECTIOS

4 UNITS	A	B	C	D
INPUT LOGIC	13&14	10	6	2&3
RC	15	9	7	1
OUTPUT LEVEL	12	11	5	4
+5VOLTS	16			
GND	8			

M046

Storage Logic

Description:

Design for HO series storage scopes - contains logic circuits which control the erase of the upper and lower screen. This also includes an auto erase multi which is free running or controlled by the sweep gate.

16 pin inline pack + 5 V DC

Input	--	9 leads (indicated operation occurs when raising the input positive)
Output	--	2 leads
Timing	--	RC for display time C for width of the erase pulse from display multi

The chip is composed of 4 logic groups, one differentiator and one timing multi.

A. The four logic groups are:

1. Upper Erase pulse out

   $5 = (\overline{4}) - (\overline{9}) \cdot \left[(7)(\text{Auto Erase}) + 6\right]$

2. Lower Erase pulse out

   $13 = (\overline{14}) \cdot (\overline{9}) \cdot \left[(11)(\text{Auto Erase}) + 12\right]$

3. Auto Start -- controlled by end of + Gate or internally when pin 10 open

4. Gate for preventing an erase pulse during sweep when operating in the Auto Erase with sweep on.

B. The differentiator produces a pulse out at the end of the display time. The width of the pulse is set by a C from pin 1 to ground. ≃1.5 ms per μF.

M046

Description: (Cont'd.)

C. Display Multi

Time is set by an RC at pin 3. Allow 2 μA for IC timing circuit. Don't exceen 750 μA timing current. End of display time occurs when C reaches 3.6 V of change.

Added Comments

Input Leads

6 & 12) Manual erase occurs when applying 0.6 mA or greater at a potential of 0.9 V. Remote leads may also be used in parallel with the internal manual erase switches. Switch contact bounce will appear at outputs pins 11 and 12.

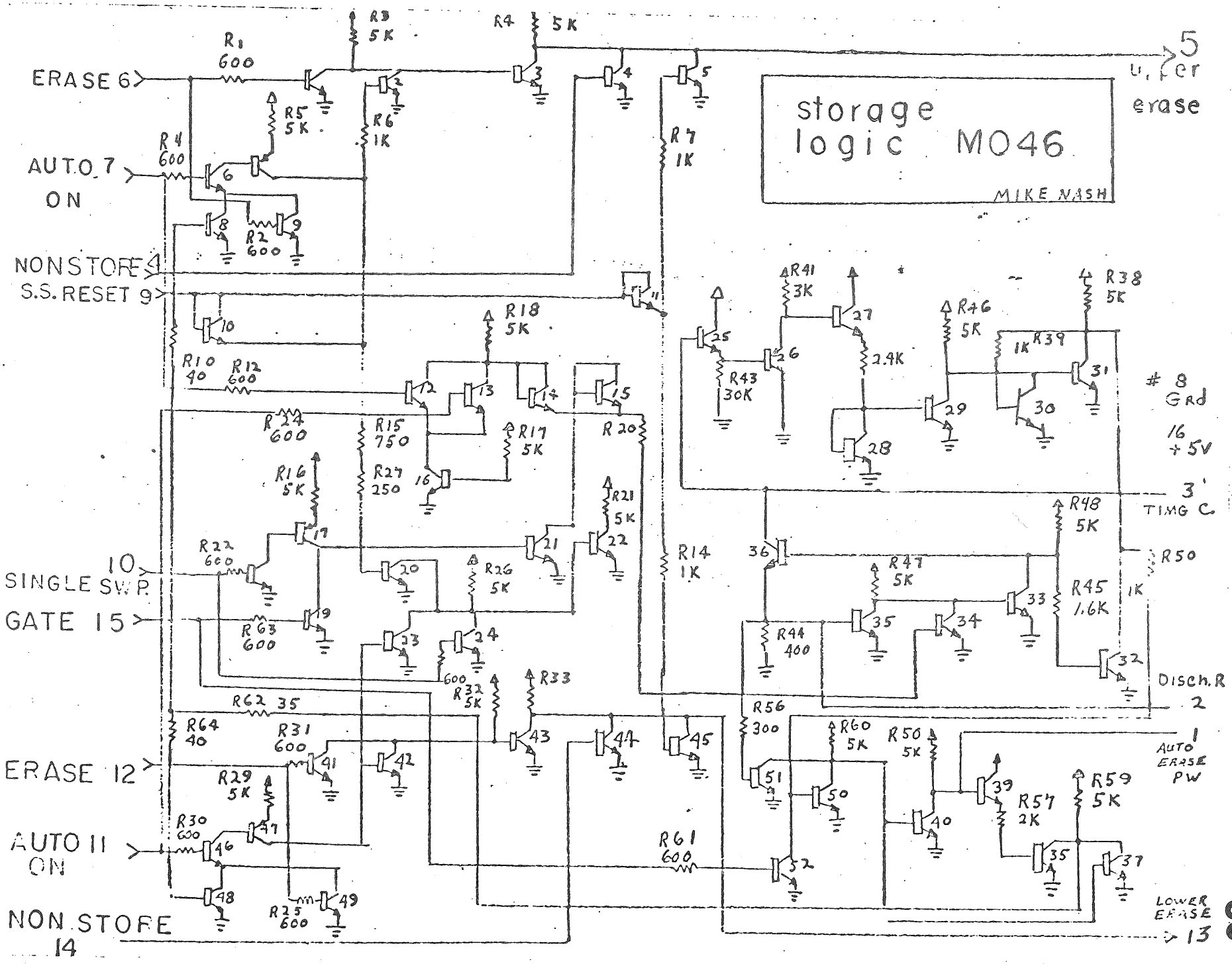
7 & 11) AUTO ON - Display multi becomes operative when applying 0.6 mA or greater at a potential of 1.6 V.

4 & 14) NON STORE - Applying 0.6 mA or greater at a potential of 0.8 V prevents pulses from appearing at the outputs (pin 5 or 13).

9) Single Sweep Reset - Applying 0.6 mA or greater at a potential of 1.6 V will reset display multi without erasing.

Designer:

Mike Nash


storage logic M046
MIKE NASH
ERASE 6
AUTO 7 ON
NON STORE 4
S.S. RESET 9
10 SINGLE SW.P.
GATE 15
ERASE 12
AUTO 11 ON
NON STORE 14
5 u. fer erase
8 Grd
16 +5V
3 TIMG C.
R50
Disch. R 2
1 AUTO ERASE PW
LOWER ERASE 13
R1 600
R2 600
R3 5K
R4 5K
R4 600
R5 5K
R6 1K
R7 1K
R10 40
R12 600
R14 1K
R15 750
R16 5K
R17 5K
R18 5K
R20
R21 5K
R22 600
R24 600
R25 600
R26 5K
R27 250
R29 5K
R30 600
R31 600
R32 5K
R33
R38 5K
R39 1K
R41 3K
R43 30K
R44 400
R45 1.6K
R46 5K
R47 5K
R48 5K
R50 1K
R56 300
R57 2K
R59 5K
R60 5K
R61 600
R62 35
R63 600
R64 40
2.4K
600

M042

Sweep Control

Description:

This single package control system is intended for use in conjunction with the M018 Miller Integrator and Delay Pickoff. Its primary application is for the H series of instruments, and it should be generally useful in other low-to-medium-speed applications.

Functions

Trigger slope selection and pulse forming.

Sawtooth start/stop.

Holdoff and single-sweep lockout.

Bright baseline generation.

Characteristics

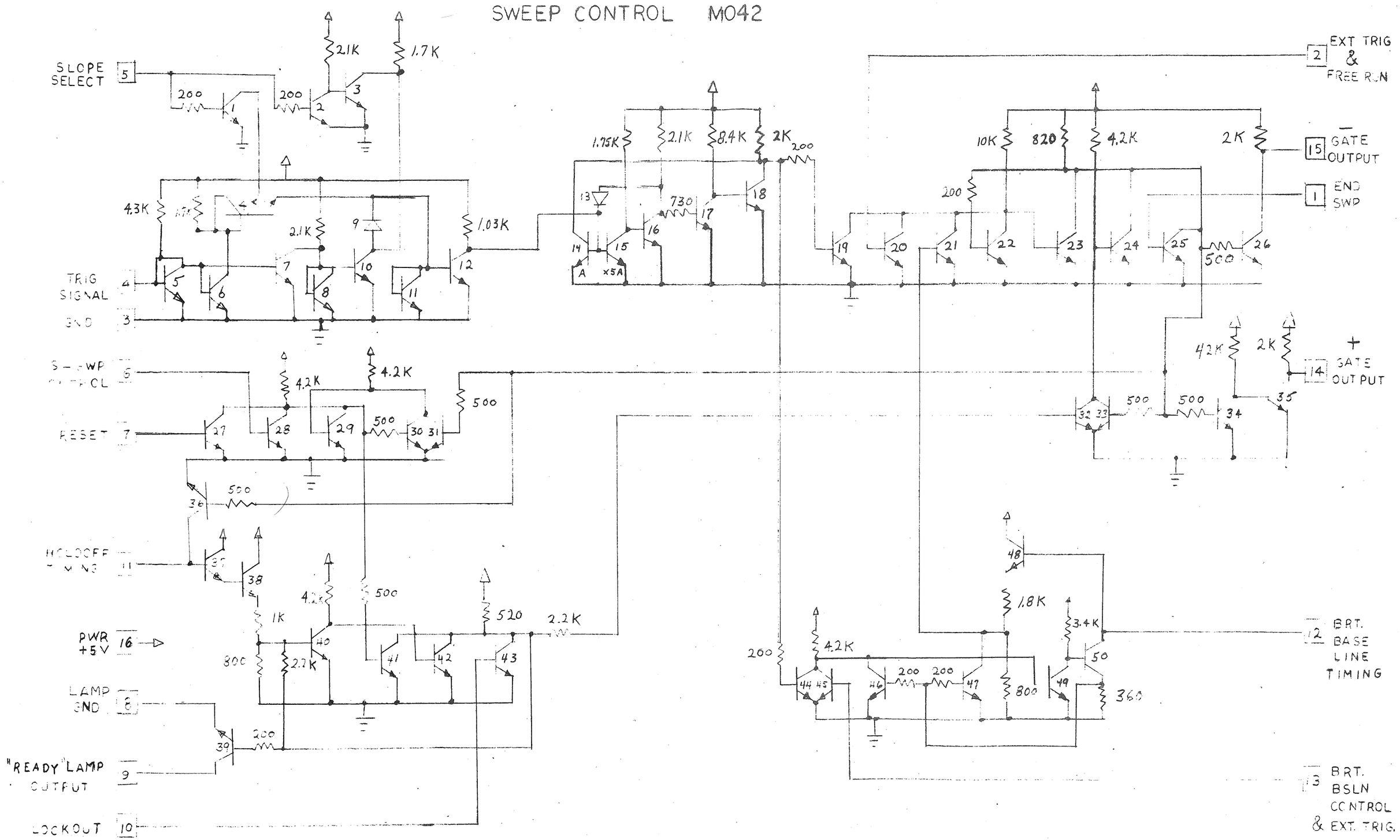
Sweep (with M018):	Amplitude ----------	0 to + 10 V starts at grd.
	Max. output rate -------	10 V/μs
Triggering:	Min. input (<10 MHz) ----	0.2 mA p-p
	Max usable frequency ----	40 MHz
	Triggering delay --------	50 ns

The maximum usable frequency may be increased by connecting external T.D. trigger processing.

Designer:

Val Garuts

SWEEP CONTROL M042



M018

Miller Integrator & Delay Pickoff

Description:

Circuit Performance: (0°C to +70°C)

A. All Input Gating (pins 1 & 5) as follows:

0 .... <0.4 V
1 .... >0.8 V (>0.5 mA to <5 mA)

B. Integrator Out (pin 3):

1. Maximum slewing rate 1 volt/100 ns. This is premised on an Integrating I of 1 mA and a timing C of 100 pF.

   (This slewing rate can possibly be increased by using a smaller timing C (i.e. 50 pF) at the expense of greater abberations at the ramp start (due to Base to Emitter C of the gating element). This will be investigated.

2. Maximum loading: ≤ 2 mA in addition to the integrating I.

3. Timing C: 100 pF to 10 μF (connected between pin 8 & 9).

4. Integrating I: + 1 μA to + 1 mA (injected into pin 9).

5. Quiescent level (pin 1 ... logic 0)

   a. Integrating I 1 μA to 0.2 mA
      Level ± 50 mV

   b. Integrating I > 0.2 mA to 1 mA
      Level ± 75 mV

6. Z Out: ≤ 50 Ω

C. Summing Pt (pin 9): Error I ≤ 1 nA @ 25°C, reducible to ≤ 0.5 nA @ 25°C using Thermalloy #2211B Heat radiator.

D. Delayed Gate Out: (pin 4):

1. Waveform: Ground referenced + 3.5 V step. I limited to 3 mA with + 10 V supply and 5 mA with + 15 V supply.

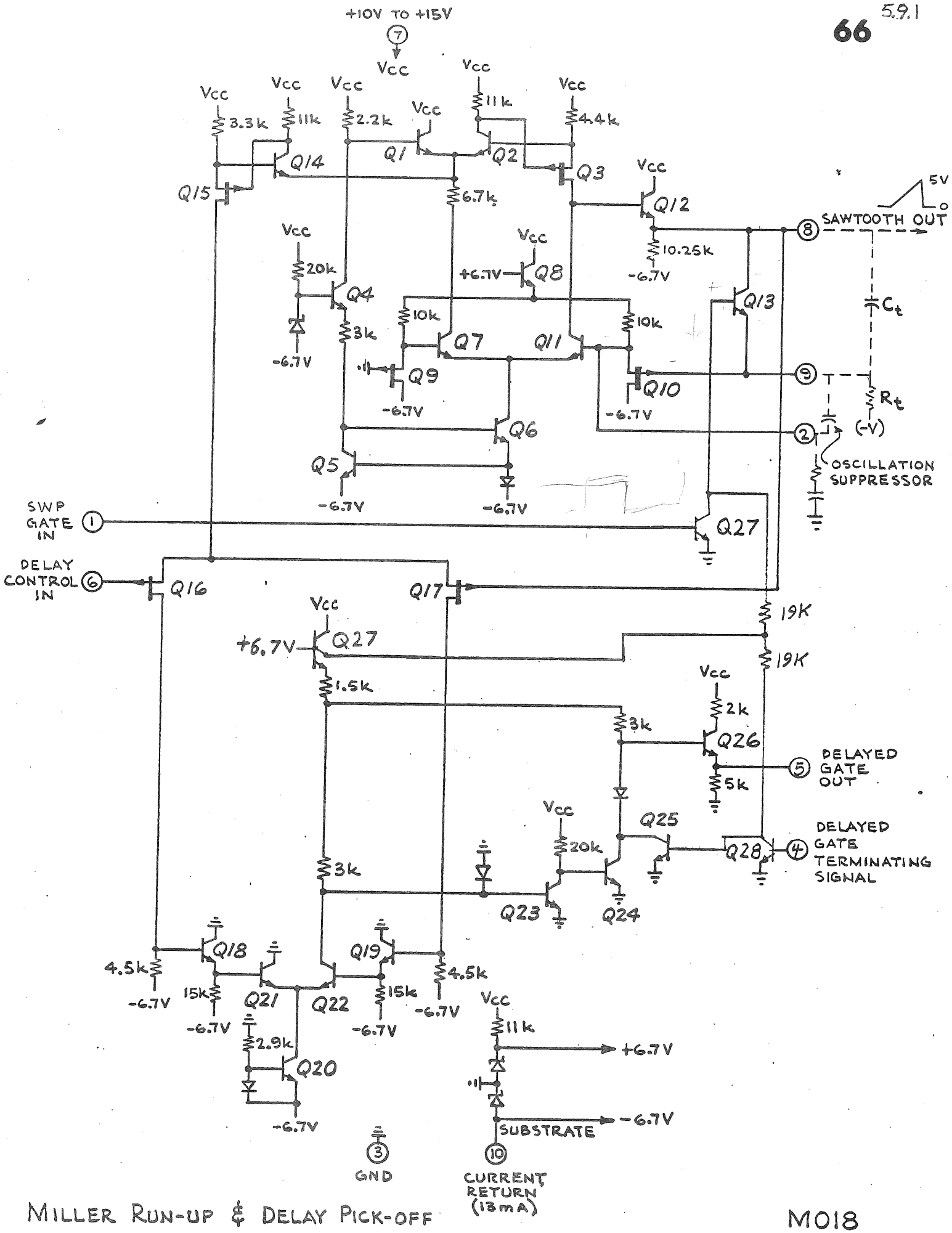
M018

Description: (cont'd.)

2. Output Z: $\leq$ 50 Ω @ + 3.5 V; $\leq$ 5.5 k @ 0 V.
3. Risetime: Dependent on loading. $\leq$ 50 ns with 2 k paralleled by 10 pF.
4. Falltime: Dependent on loading. $\leq$ 50 ns with 2 k paralleled by 10 pF.
5. Jitter: When used as a delaying gate $\leq$ 40 k :1
6. Hysterysis: (i.e. the Integrator out excursion necessary to switch Gate on (+ 3.5 V) then off (0 V) ≃ 10 mV.

Designer:

Joe Burger



MILLER RUN-UP & DELAY PICK-OFF

M018

M052

Trigger & Sweep

Description:

This IC includes all functions for trigger and sweep.

TRIGGER:

Input: FET input, 50 mV to 1 V pp

Level: Single control for level and plus or minus slope

Frequency: DC to 5 MHz

SWEEP:

Ramp Output: Negative slope from + 2 V to) V, ext. adj. ± 0.5 V

Maximum dV/dT: 1 V/μsec

Timing Resistor Voltage: + 2.5 V ± 0.5 V

Holdoff: Ext. C, internal 0.25 mA timing I

Auto Free-Run: External RC

Unblank Output: +2 V during sweep

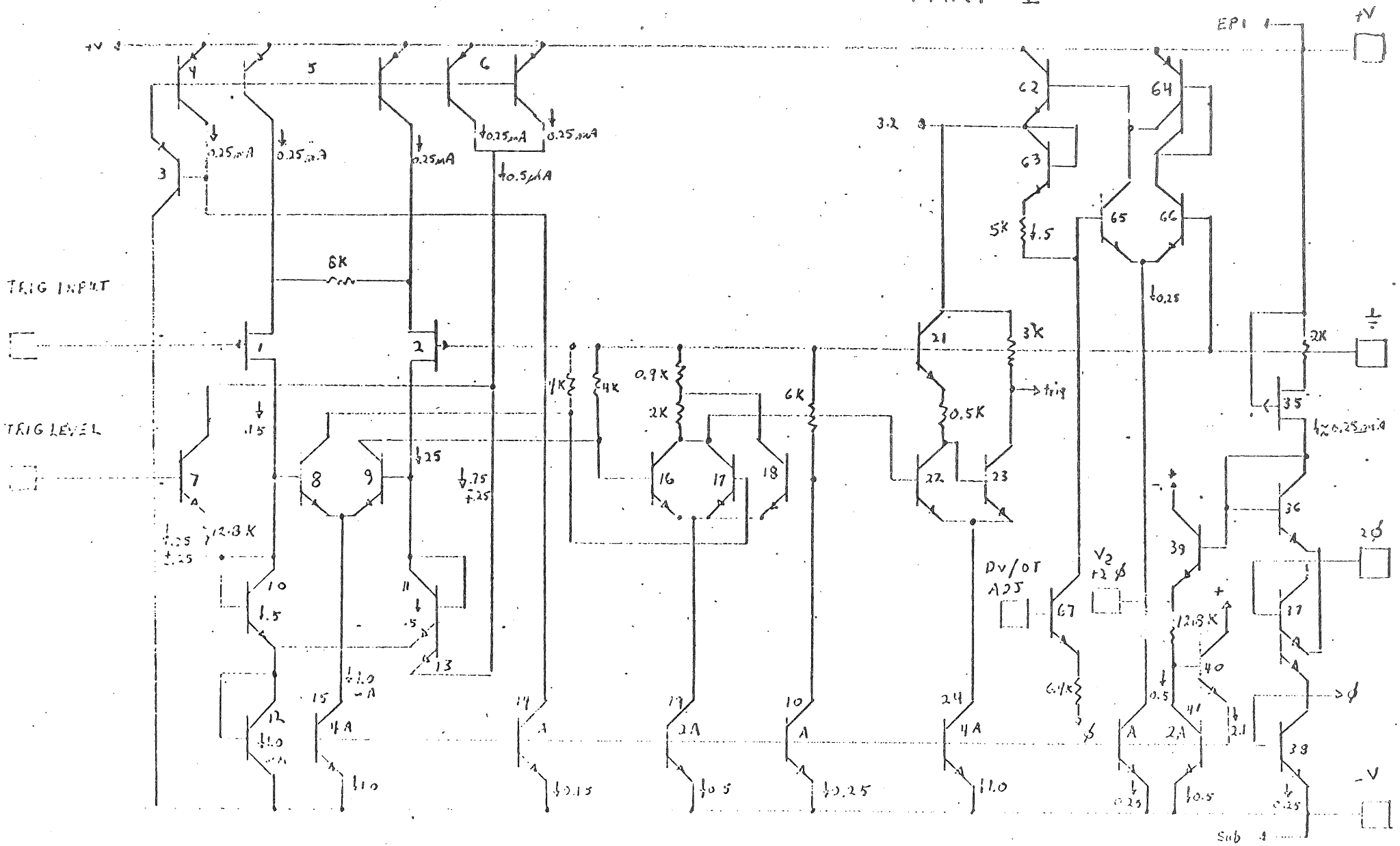
Power Supplies: ± 5 to ± 10 V @ 8 mA

Designer:

Dave Allen

M052 Mini Scope Sweep + Trig. (Trig + Bias Circuit)

PART I



M052 Mini Scope Sweep + trig. . . (Sweep Circuit)

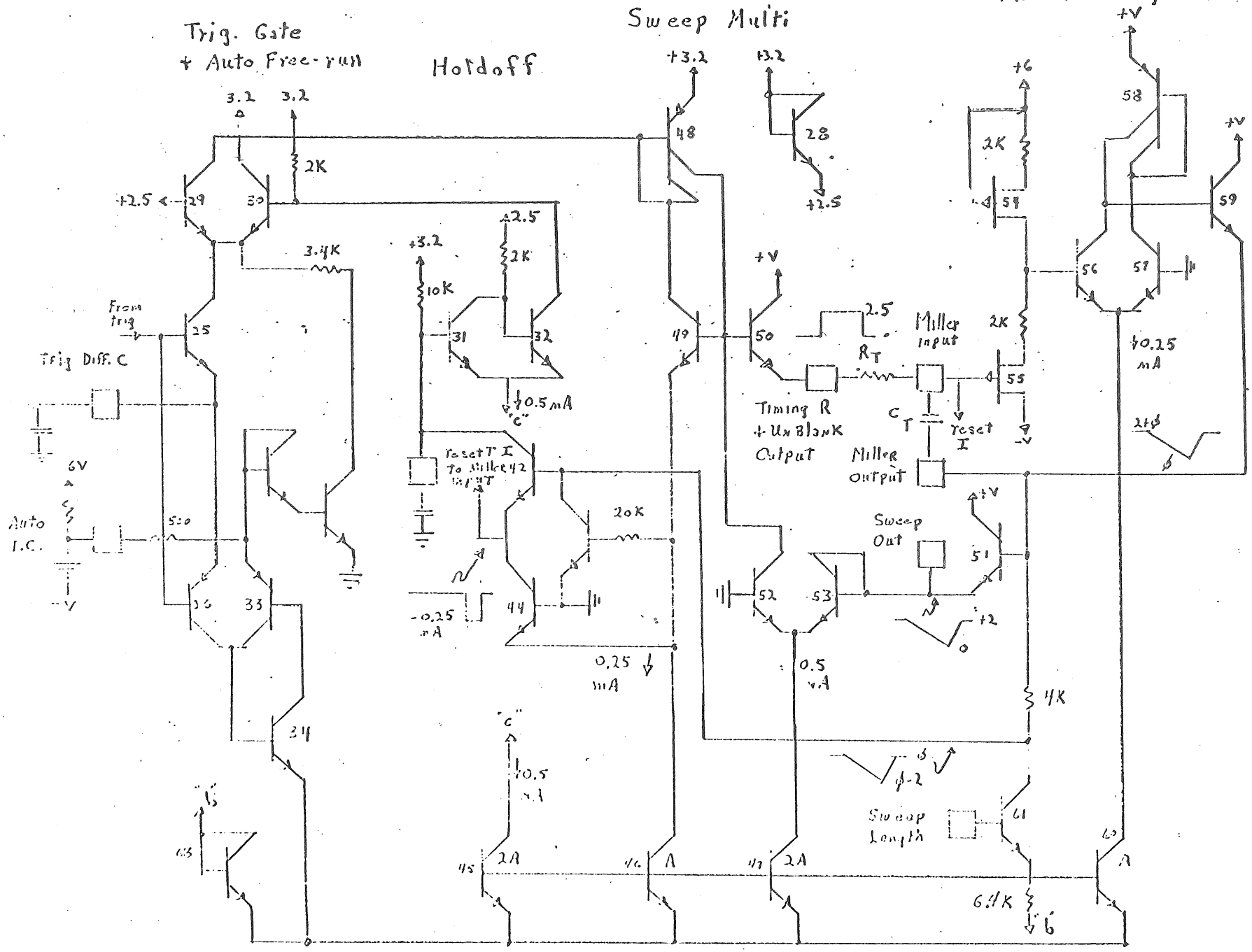
PART 2

Trig. Gate + Auto Free-run

Holdoff

Sweep Multi

Miller Integrator



576 Readout System

M033

M034

M035

M038

M039

Description:

The 576 readout system is comprised of four fiber-optic readout modules. Three of these modules are each driven by a M038 and M039. The fourth module displays the ratio of vertical current/div. to base step/div. This beta/div. readout is driven by M033, M034 and M035. The IC's are programmed from switch closures or external inputs and perform the required logic functions to drive the lamps in the readout.

M038

This circuit drive the 1.2 or 5 and the V or A symbol.

M039

This circuit drives the decade portion of the readout. The input information is in the form of binary coded exponents of 10. There are also binary coded multipliers from the various magnifier switches. The exponential sum of these inputs is then encoded to drive the various lamps required for the readout. Over 100 two input gate functions are performed, using 135 transistors.

576 Readout System (Cont'd.)

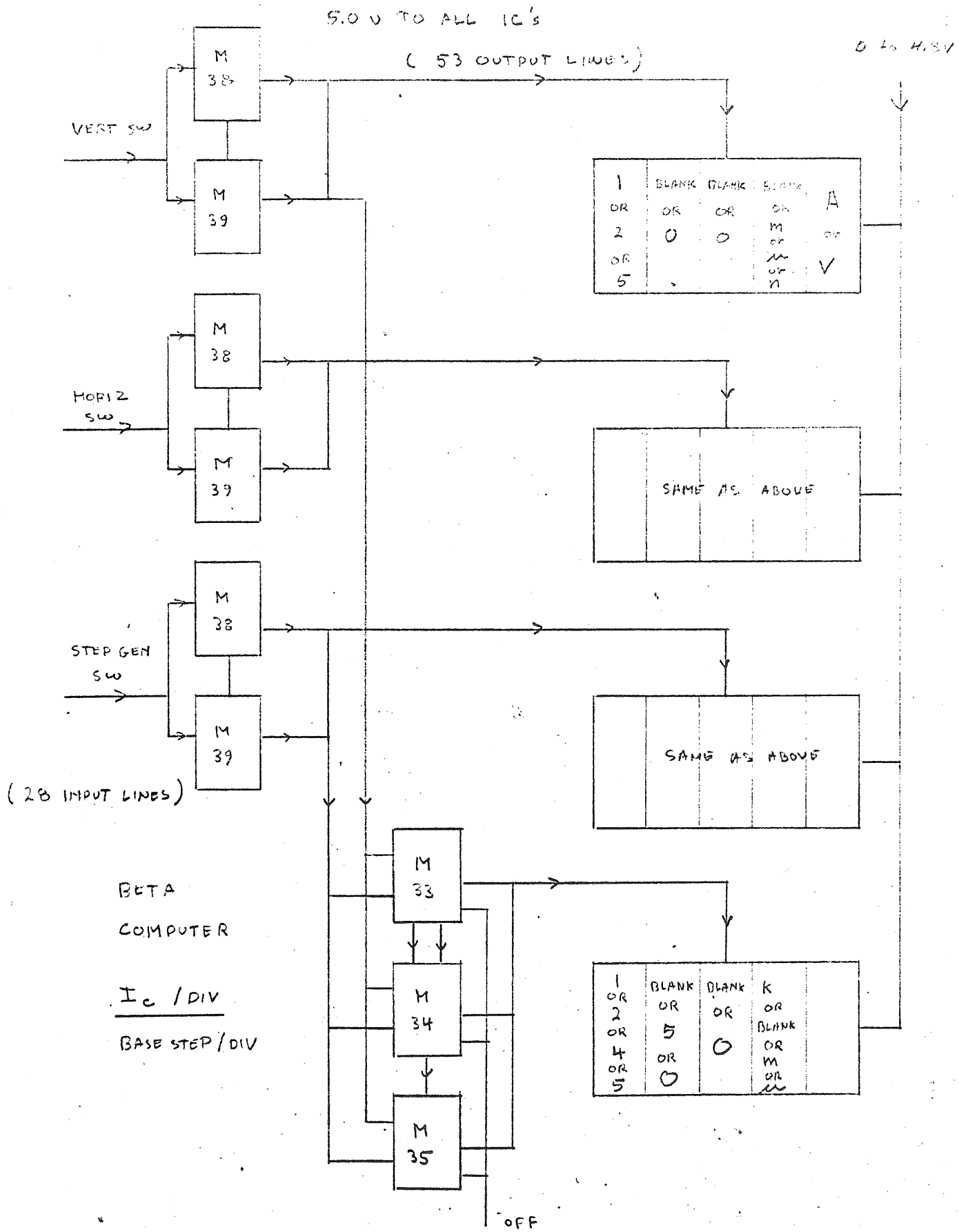
Beta Computer -- M033, M034 and M035

These circuits compute the ratio of vertical current/div. to step gen/div. M033 computes the ratio of the 125 inputs. M034 computes the ratio of the 10^0, 10^1 and 10^2 inputs. M035 computes the ratio of the 10^0, 10^{-3}, 10^{-6} and 10^{-9} inputs. Ratios greater than 10^{+3} or less than 10^{-6} are not displayed.

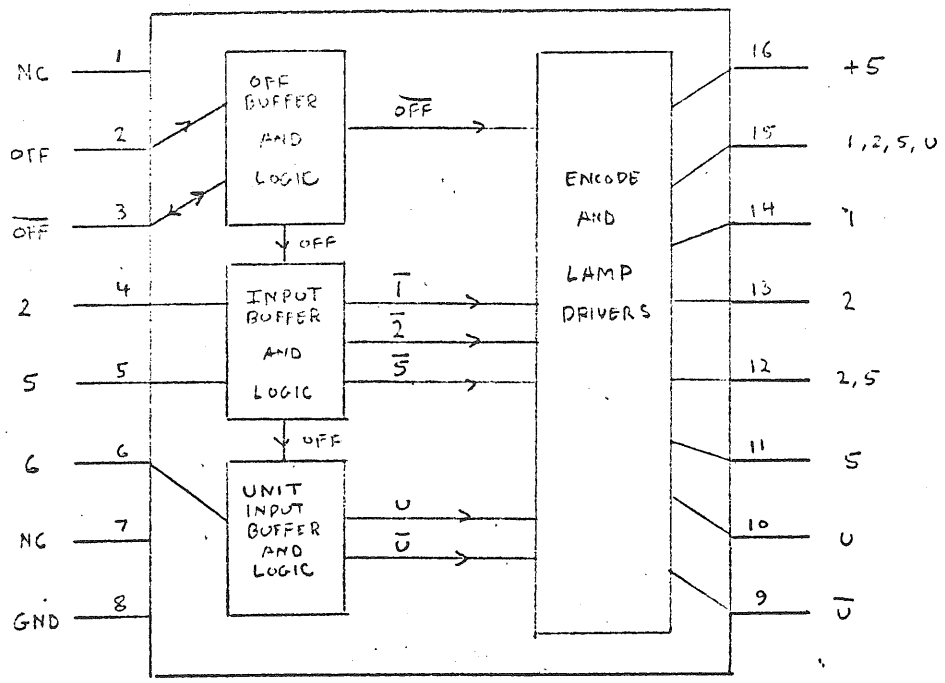
Designer:

Jerry Rogers

576 FIBER OPTICS READOUT SYSTEM



M 038C 155-0007



PIN 15 = $\overline{2} + \overline{3}$

14 = $\overline{4} \cdot \overline{5} \cdot (\overline{2} + \overline{3})$

13 = $4 \cdot (\overline{2} + \overline{3})$

12 = $4 + 5 \cdot (\overline{2} + \overline{3})$

11 = $5 \cdot (\overline{2} + \overline{3})$

10 = $\overline{6} \cdot (\overline{2} + \overline{3})$

9 = $6 \cdot (\overline{2} + \overline{3})$

3 = $\overline{2}$

INPUT LEVELS: FALSE ≥ 5V OR ≤ 0.1μA

TRUE ≤ 2V @ ≤ 1mA

OUTPUT: TRUE ≤ 0.6V @ 60mA

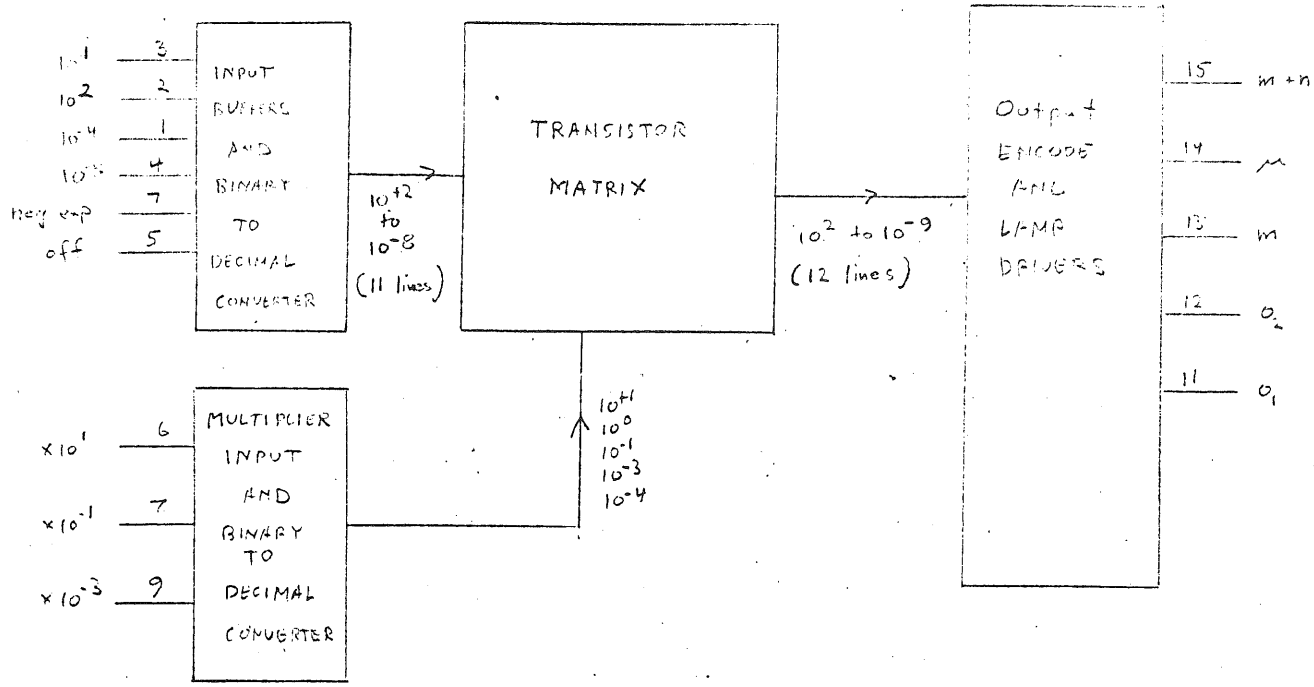
IF PIN 2 IS FALSE THEN PIN 3 = 1V

IF PIN 2 IS TRUE THEN PIN 3 = 4V

PIN 2 AND 3 BOTH TRUE NOT ALLOWED

PIN 4 AND 5 BOTH TRUE NOT ALLOWED

M 33 155-0008



INPUT LOGIC

$10^2 = 2$
$10^1 = 3$
$10^0 = 7 + \overline{7}$
$10^{-1} = 3 \cdot 7$
$10^{-2} = 2 \cdot 7$
10^{-3} $2 \cdot 3 \cdot 7$
10^{-4} $1 \cdot 7$
10^{-5} $1 \cdot 3 \cdot 7$
10^{-6} $1 \cdot 2 \cdot 7$
10^{-7} $1 \cdot 2 \cdot 3 \cdot 7$
10^{-8} $4 \cdot 7$

MULTIPLIER LOGIC

$10^1 = 6$
$10^0 = \overline{6 \cdot 7} + 6 \cdot 7$
$10^{-1} = 7$
$10^{-3} = 9$
10^{-4} $7 \cdot 9$

LOGIC LEVELS

INPUTS AND MULTIPLIERS:
FALSE $\geq 5V$ OR $\leq 0.1\mu A$
TRUE $\leq 2V$ @ $\leq 1mA$

OFF: FALSE 1 to 1.2V
TRUE $\geq 4V$

THE FOLLOWING INPUT COMBINATIONS ARE NOT ALLOWED:
INPUTS $> 10^2$ OR $< 10^{-8}$
INPUT TIMES MULTIPLIER $> 10^2$ OR $< 10^{-10}$

THE OUTPUT OF THE MATRIX IS THE EXPONENTIAL SUM OF THE TWO INPUTS.

OUTPUTS

PIN 15 $= 10^{-1} + 10^{-2} + 10^{-3} + 10^{-7} + 10^{-8} + 10^{-9}$

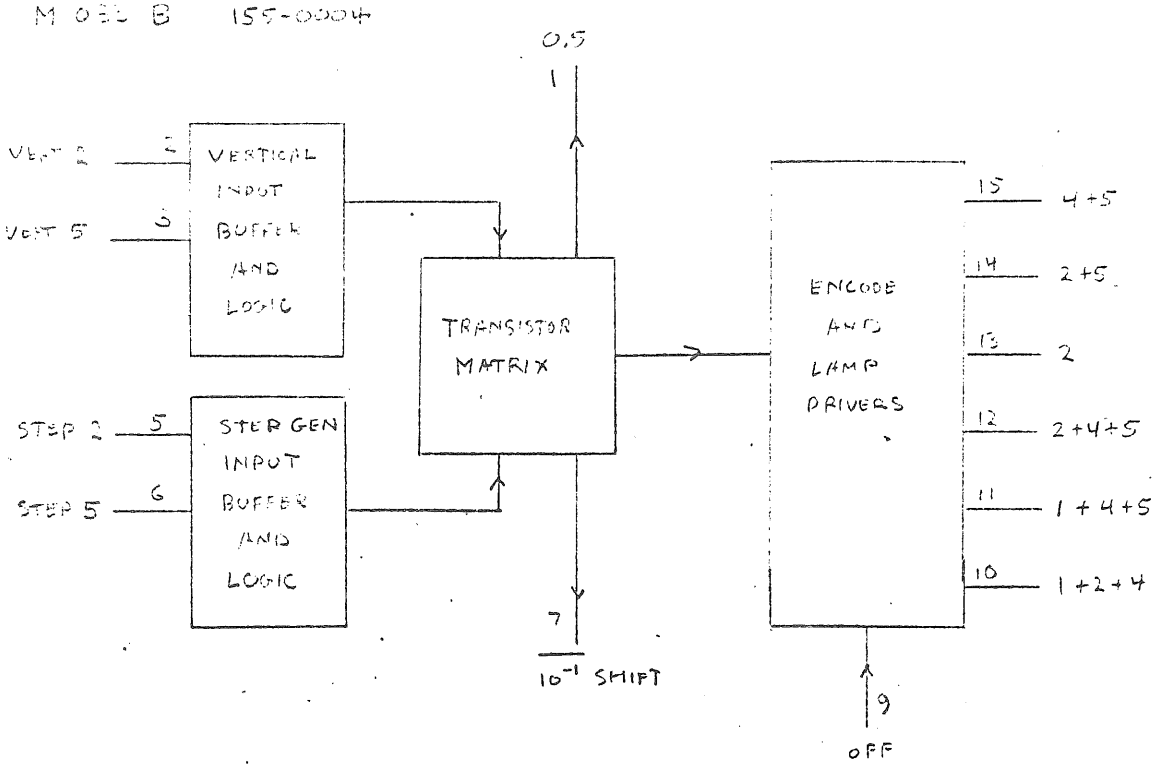
14 $= 10^{-4} + 10^{-5} + 10^{-6}$

13 $= 10^{-1} + 10^{-2} + 10^{-3}$

12 $= 10^2 + 10^1 + 10^{-4} + 10^{-7}$

11 $= 10^2 + 10^1 + 10^{-1} + 10^{-2} + 10^{-4} + 10^{-5} + 10^{-7} + 10^{-8}$
$(\overline{10^0} + \overline{10^{-3}} + \overline{10^{-6}} + \overline{10^{-9}})$

MODEL B 155-0004



VERT INPUT: $1 = \overline{\text{PIN } 2 + \text{PIN } 3}$

$2 = 2$

$5 = 3$

STEP INPUT: $1 = \overline{5+6}$

$2 = 5$

$5 = 6$

TRANSISTOR MATRIX TRUTH TABLE.

STEP \ VERT	1	2	5
1	1	2	5
2	0.5	1	2.5
5	0.2	0.4	1

OUTPUTS:

$5 = 5 + 0.5$

$4 = 0.4$

$2 = 2.5 + 2 + 0.2$

$1 = 1$

$0.5 = 2.5$

$\overline{10^{-1}}$ SHIFT $= 0.5 + 0.4 + 0.2$

LOGIC LEVELS:

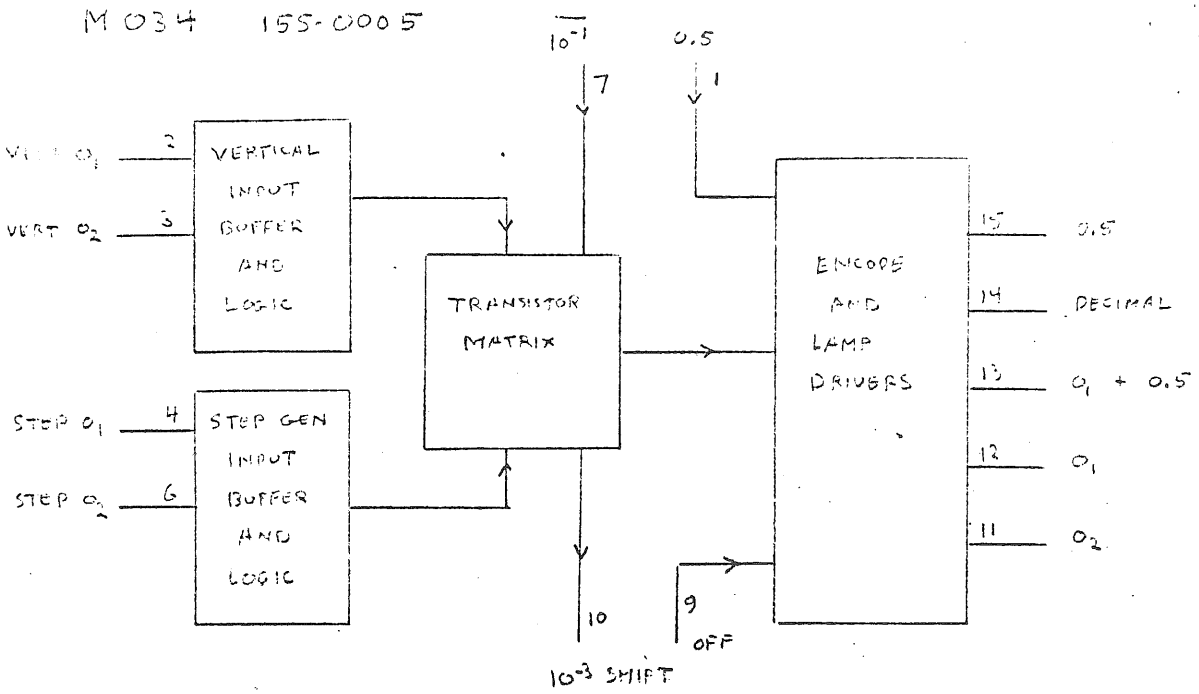
INPUTS: FALSE ≥ 1.2 V.
TRUE ≤ 0.6 V

0.5 OUTPUT: FALSE $\leq 10\mu A$
TRUE $\geq 200\mu A$ @ ≥ 2.5V

$\overline{10^{-1}}$ SHIFT.: FALSE ≤ 0.4V
TRUE ≥ 4V @ ≤ 1mA

LAMP DRIVERS: ≤ 0.6V @ 60mA

M 034 155-0005



VERT INPUT: $10^0 = \overline{2 \cdot 3}$

$10^1 = 2$

$10^2 = 2 \cdot 3$

STEP GEN INPUT: $10^0 = \overline{4.6}$

$10^1 = 4$

$10^2 = 4.6$

MATRIX TRUTH TABLE

STEP GEN. \ VERT	10^0	10^1	10^2
10^0	10^0	10^1	10^2
10^1	10^{-1}	10^0	10^1
10^2	10^{-2}	10^{-1}	10^0

OUTPUTS:

PIN 15 = $0.5 \cdot \overline{OFF}$

14 = = $0.5 \cdot (10^0 + 10^{-3}) \cdot \overline{OFF}$

13 = $\overline{(10^0 + 10^{-3})} + 0.5 \cdot \overline{OFF}$

12 = $\overline{(10^0 + 10^{-3})} \cdot \overline{0.5} \cdot \overline{OFF}$

11 = $10^2 + 10^{-1}$

10 = $10^{-1} + 10^{-2} + 10^{-3}$

LOGIC LEVELS:

INPUTS: FALSE ≥ 1.2 V
TRUE ≤ 0.6 V

0.5: FALSE $\leq 1\mu A$
TRUE $\geq 100\mu A$

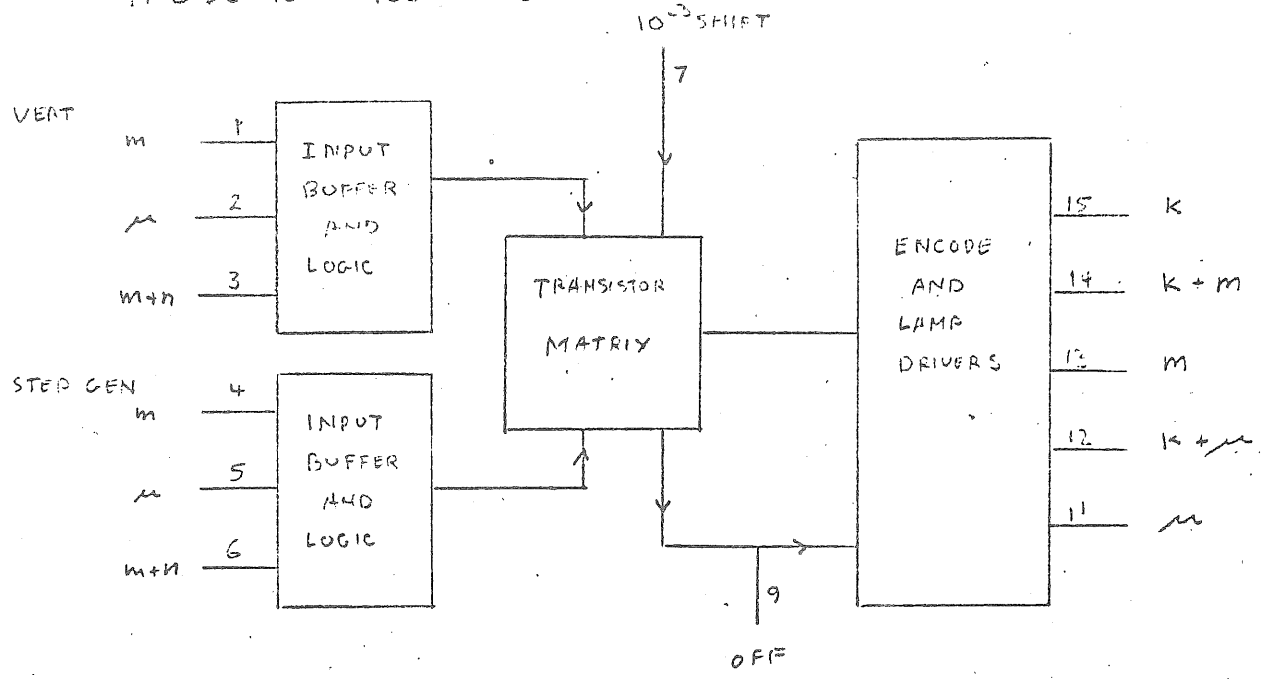
$\overline{10^{-1}}$ SHIFT: FALSE ≤ 0.4 V
TRUE ≥ 2 V

OUTPUTS:

10^{-3} SHIFT: FALSE ≥ 2 V
TRUE ≤ 0.4 V

LAMP DRIVERS: ≤ 0.6 V @ 60mA

M 035 B 155-0006



VERT INPUT: $10^0 = \overline{1 \cdot 2 \cdot 3}$

$10^{-3} = 1 \cdot 3$

$10^{-6} = 2$

$10^{-9} = 3$

STEP GEN. INPUT: $10^0 = \overline{4 \cdot 5 \cdot 6}$

$10^{-3} = 4 \cdot 6$

$10^{-6} = 5$

$10^{-9} = 6$

MATRIX TRUTH TABLE

VERT:

STEP GEN:	10^0	10^{-3}	10^{-6}	10^{-9}
10^0	10^0	10^{-3}	10^{-6}	10^{-9}
10^{-3}	10^3	10^0	10^{-3}	10^{-6}
10^{-6}	10^6	10^3	10^0	10^{-3}
10^{-9}	10^9	10^6	10^3	10^0

OUTPUTS:

PIN 15 = 10^3

14 = $10^3 + 10^{-3}$

13 = 10^{-3}

12 = $10^3 + 10^{-6}$

11 = 10^{-6}

9 = $10^{-12} + 10^{-9} + 10^6 + 10^9$

LOGIC LEVELS

INPUTS: FALSE ≥ 1.2V
TRUE ≤ 0.6V

10^{-3} SHIFT: FALSE ≥ 2 V
TRUE ≤ 0.4 V

OFF FALSE ≥ 2V
TRUE ≤ 0.4 V

OUTPUTS:

OFF FALSE ≥ 2 V
TRUE ≤ 0.4 V

LAMP DRIVERS ≤ 0.6 V
@ 60 mA

Additional circuits are
under development and are
classified confidential.

Refer to latest I.C. product
schedule for latest listings.
See Ed Cole, Extension 6534
Delivery Station 50-332 for
further information.