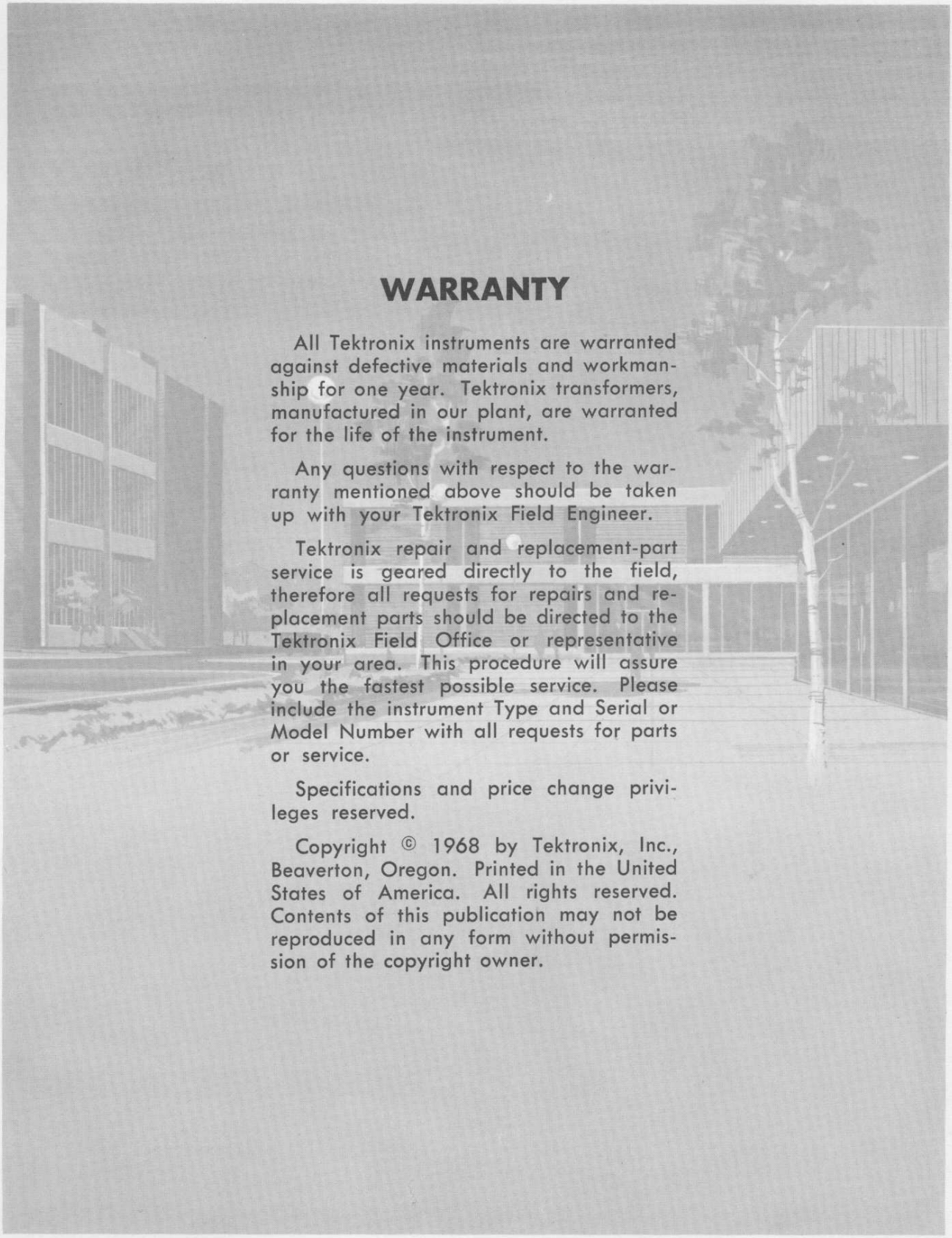
INSTRUCTION MANUAL

Serial Number _____

Tektronix, Inc.
S.W. Millikan Way ● P. O. Box 500 ● Beaverton, Oregon 97005 ● Phone 644-0161 ● Cables: Tektronix

070-0759-00

468



WARRANTY

All Tektronix instruments are warranted against defective materials and workmanship for one year. Tektronix transformers, manufactured in our plant, are warranted for the life of the instrument.

Any questions with respect to the warranty mentioned above should be taken up with your Tektronix Field Engineer.

Tektronix repair and replacement-part service is geared directly to the field, therefore all requests for repairs and replacement parts should be directed to the Tektronix Field Office or representative in your area. This procedure will assure you the fastest possible service. Please include the instrument Type and Serial or Model Number with all requests for parts or service.

Specifications and price change privileges reserved.

CONTENTS

Abbreviations and symbols used in this manual are based on or taken directly from IEEE Standard 260 "Standard Symbols for Units", MIL-STD-12B and other standards of the electronics industry. Change information, if any, is located at the rear of this manual.

Fig. 1-1. Type 3S2 Sampling Unit.

SECTION 1
SPECIFICATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Type 3S2 Sampling Unit is a dual-channel vertical amplifier plug-in unit designed for operation in any one of the Tektronix Type 560-Series Oscilloscopes except the Type 561 (it will operate in the Type 561A). The Type 3S2 accepts "S" Series sampling heads. The sampling heads determine the input characteristics of the sampling unit and the availability of the trigger pickoff.

The Type 3S2 will operate with any Tektronix 3T-series sampling unit. The Type 3T2 Random Sampling Sweep is recommended, because it can display the triggering event without a pretrigger or signal delay line. Conventional or real time 2B- or 3B-series time-base units include the Types 2B67, 3B1, 3B4 and the 3B5 non-digital time bases, and the Type 3B2 Analog/Digital Time Base Unit. The Type 3S2 provides the vertical information needed for voltage measurements by Tektronix digital readout systems, such as the Type 567-Type 6R1A, or the Type 568-Type 230.

One or two "S" Series sampling heads can be plugged into the Type 3S2, or used remotely on an optional extender cable unit. The Type 3S2 provides the power for the sampling heads.

Interconnections to the circuits in the sampling heads are provided by connectors in the sampling head compartments of the Type 3S2.

If a trigger pickoff is provided in the sampling head, the Type 3S2 provides a trigger selection circuit and returns a portion of the input signal to the front panel for externally triggering a sampling sweep unit. An internal reconstructed signal is provided to trigger the real-time time-base.

Sampled signals are presented to both the oscilloscope CRT and to the front panel connectors for external use with auxiliary equipment such as pen recorders. The two Channels may be displayed either individually or in one of three combined modes: DUAL-TRACE, A+B (Algebraic addition), or a VERT/B HORIZ (X-Y). The A VERT/B HORIZ (X-Y) mode does not apply in real time operation.

ELECTRICAL CHARACTERISTICS

Digital Unit Compatibility

The Type 3S2 is compatible for operation with all Type 230 Digital Units and all Type 6R1A Digital Units. It is compatible with all Type 6R1 Digital Units SN 695 and up. The Type 6R1 Digital Units SN 101-694 require the installation of Tektronix Modification Kit 040-0342-00 when operating with a Type 3S2.

The following characteristics apply over an ambient temperature range of 0°C to + 50°C. These characteristics apply only after the Type 3S2 VERT GAIN control has been properly adjusted for the oscilloscope and after a sufficient warm-up time. For particular system warm-up requirements, refer to the main frame oscilloscope instruction manual. A procedure for mating the Type 3S2 to each oscilloscope can be found in the Operating Instructions section.

The Type 3S2 meets the tolerances stated below after a 5-minute warmup.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
Deflection Factors		
Units/Div Switch Range	2 to 200 in 7 steps in a 1-2-5 sequence with Units/Div labeled on the sampling head.	
Accuracy	Within 3%, NORMAL; 6% SMOOTH	Normal sequential sampling with at least 20 samples per cycle of displayed square wave.
Units/Div VARIABLE Range	Reduction in deflection to 0.7 or less when control is turned CCW from CAL position, and 2.5 times or more increase in deflection when control is turned CW from CAL position.	
Interchannel Delay Range	At least +5 ns to −5 ns.	With two same type sampling heads plugged in, using time-coincident signals.
Loop Gain		
NORMAL	Can be set to unity with DOT RESPONSE control.	Range of DOT RESPONSE control is $\leq$0.95 to $\geq$1.05.

ELECTRICAL CHARACTERISTICS *(cont'd)*

Characteristic	Performance Requirement	Supplemental Information
SMOOTH	Loop gain is reduced to be $\leq$0.3.	Random noise in display reduced to approx 1/2.
Dot Slash	Vertical dot drift is $\leq$ 0.1 div when sampling sweep unit is triggered at 20 Hz.	Measure with Units/Div switch at 200 with no signal input to the sampling head.
OFFSET Output Voltage Range	+10 to −10 volts.	
Accuracy	Actual DC OFFSET Voltage is 0.1× OFFSET Output voltage within 2%.	Source Resistance 10 kΩ within 1%.
DC OFFSET Range	+1 to −1 volt[1].	
A Output, B Output Amplitude in Volts (Referred to Input)	Signal input times $\left(\frac{200}{\text{Units/Div Setting}}\right)$	Maximum output voltage ±4 V. Source Resistance 10 kΩ, within 0.5%.
Accuracy (Referred to Input)	Within 2%.	
Accuracy (Referred to CRT)	Within 3%. (200 mV/Div).	
Accuracy of Vertical Signal to Digital Unit	Within 3%.	
TRIG OUT (SN B040250-up) (with Type S-1, S-2) Amplitude (referred to the Type S-1, S-2 input)	Approximately 1× inut signal voltage into 50 Ω for AC. Approximately .1× input signal voltage into 50 Ω for DC. Coupling time constant is 5 μs. Approximately 1× for both AC and DC signals into 1 MΩ.	
Risetime	2 ns or less, 10% to 90%, into 50 Ω using 70 ps risetime input pulse	
Strobe signal in Trig Out Signal	$\leq$50 mV peak into 50 Ω	
TRIG OUT, SN B010101 to SN B030249 (with Type S-1, S-2) Amplitude (Referred to the Type S-1, S-2 input)		Approximately 0.1 × input signal voltage DC coupled into 50 Ω. Approximately 2 1/2× input signal voltage into 1 MΩ.
Risetime	0.6 ns or less, 10% to 50%, into 50 Ω using 70 ps risetime input pulse.	
Strobe signal in Trig Out signal	$\leq$10 mV peak into 50 Ω.	
Position Indicator Lamps	One indicator lamp will be on and the other off when CRT dot is more than 4 divisions away from the graticule centerline.	
POSITION Range	$\geq$ +5 to −5 vertical divisions from the graticule center.	When DC OFFSET is set to deliver 0 V to OFFSET output jack.

[1]**Unless otherwise stated on the sampling head front panel.**

ENVIRONMENTAL CHARACTERISTICS

Storage

Temperature— −40°C to +65°C.

Altitude— To 50,000 feet.

Operating

Operating Temperature— 0°C to +50°C.

Operating Altitude— To 15,000 feet.

MECHANICAL CHARACTERISTICS

Dimensions— Height 6 1/4 inches

Width 4 1/4 inches

Length 14 1/2 inches

Approximate dimensions including knobs and connectors.

Construction— Aluminum alloy chassis with epoxy laminated circuit boards. Front panel is anodized aluminum.

Accessories— An illustrated list of the accessories supplied with the Type 3S2 is at the end of the Mechanical Parts List pullout pages.

SECTION 2
OPERATING INSTRUCTIONS

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

This section discusses installation, first time operation, function of front panel controls and connectors, basic operation and applications of the Type 3S2. If you are unfamiliar with sampling, it may be very helpful to read Section 3, Basic Tektronix Sampling Principles, before proceeding with this section.

The Type 3S2 is a special purpose dual-channel sampling unit designed to operate with the following indicator oscilloscopes: Type 561A, RM561A, Type 567, RM567, Type 568, and R568. The Type 3S2 accepts S-series sampling heads which determine the input characteristics of the sampling system and provide a trigger pickoff. For equivalent time sampling, the sampling system consists of an indicator oscilloscope, Type 3S2 with sampling head (or heads), and a sampling sweep unit. A random sampling sweep unit such as the Type 3T2 is recommended, because it eliminates the necessity of pretriggering or signal delay for viewing a repetitive signal.

The Type 3S2 can be used for real time operation with all real-time time-base units such as Type 2B67, 3B1, 3B2, 3B3, 3B4, and 3B5. An internal trigger source from the display signal is provided for real time operation.

The vertical deflection factors of 2 to 200 are calibrated to the units labeled on the sampling head. Sampling head extender cable units are available to operate the S-series sampling heads remotely up to 6 feet away. Three-foot sampling head extender cable is Tektronix Part No. 012-0124-00. Six-foot sampling head extender cable is Tektronix Part No. 012-0125-00. Contact your local Tektronix Field Engineer or Representative for price and availability of these optional accessories.

Installing the Type 3S2 in the Oscilloscope

The Type 3S2 is designed to drive the vertical deflection plates of the oscilloscope CRT, and therefore is installed in the left-hand compartment of the oscilloscope.

NOTE

The Horiz Plug-in Compatibility switch SW6, located on the upper portion of the internal bulkhead immediately behind the front panel, must be set to agree with the type of time base used.

To insert the Type 3S2 into the oscilloscope compartment, turn the aluminum knob (at the front panel bottom center) counterclockwise several turns until it stops. Then slide the Type 3S2 completely into the compartment. Once the plug-in unit is seated, turn the aluminum knob a few turns clockwise until it is hand-tight.

The Type 3S2 requires at least one sampling head in order to operate. The sampling head (or heads) can be plugged into the Type 3S2 or used remotely by use of an extender cable.

To insert a sampling head into the right or left Channel compartment of the Type 3S2, slide the unit completely into the compartment, leaving the latch at the bottom of the unit free to move. Once the sampling head is seated, push the latch to lock the head in place. To remove, pull the latch knob away from the panel, then pull the unit from the compartment. See Fig. 2-1. The same system of connections applies when using the sampling head extender cable.

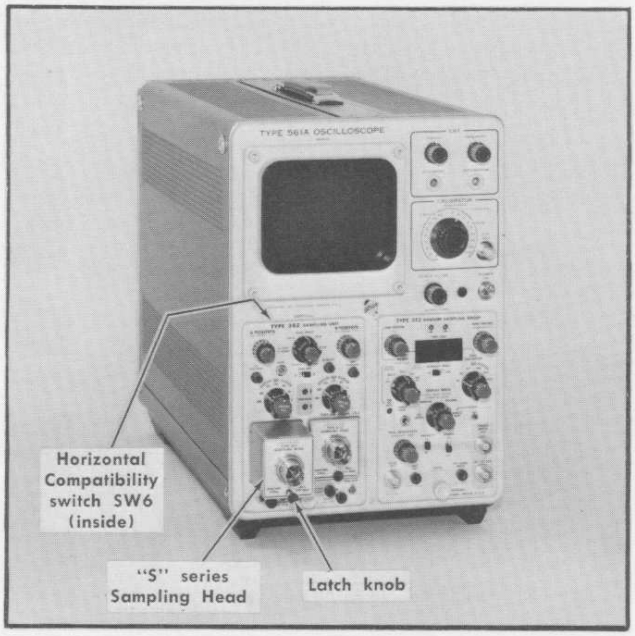


Fig. 2-1. Installation information and location of the Horiz Plug-In Compatibility switch.

Mating

The Type 3S2 Vertical Output Amplifier gain must be matched to the indicator oscilloscope CRT deflection factor for accurate gain measurements. The GAIN control, a screwdriver adjustment on the front panel adjusts the Vertical Output Amplifier gain of the Type 3S2. Adjustment of this GAIN control using the Type 284 Pulse Generator as a signal source is shown under Equivalent-Time Sampling Operation which follows. For further Gain information, refer to the Gain Adjustment instructions later in this section.

FIRST-TIME OPERATION

Equivalent-time Sampling Operation

Equivalent-time sampling operation of the Type 3S2 requires a sampling sweep plug-in unit in the right hand compartment of the indicator oscilloscope. In this First Time Operation procedure, a Type 3T2 Random Sampling sweep is used. The Type 3T2 is recommended for use with the Type 3S2, because random sampling permits viewing the signal in advance of the triggering event. Such trigger lead-time is required by the Type 3S2 to view fast rise pulses while internally triggering the sampling sweep unit from the TRIG OUT connector. The Type 561A Oscilloscope is used, and a Type 284 Pulse Generator is used as a signal source. Any S-Series sampling head can be used. In this First Time Operation, two Type S-1 Sampling Heads are used. If you are not already familiar with the operation of the oscilloscope and sampling sweep unit, read the manuals for these instruments before proceeding.

Single Trace

Make sure that the internally mounted Horiz Plug-in Compatibility switch SW6 is in the Sampling 3T-Series position. See Fig. 2-1 for its location. Also make sure that the Samples/Div switch SW450 on the Type 3T2 bulkhead immediately behind the front panel is set to the Variable (Front Panel) position.

Type 3S2

Horiz Plug-In Compatibility SW6 (behind front panel)	Sampling
Display Mode	CH B
NORMAL-SMOOTH	NORMAL
A and B POSITION	Midrange
DC OFFSET (both Channels)	Midrange (5 turns from one end)
Units/Div (both Channels)	200
VARIABLE (both Channels)	CAL
INVERT	Push in
DOT RESPONSE (both channels)	Midrange
B DELAY	Midrange
TRIG OUT switch	Optional

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep rate	100 ns
Range	1 μs
Diplay Mag	×1
Time Magnifier	×1
Variable	Cal
Time Position	Both fully clockwise
Trig Sensitivity	Fully clockwise
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	Ext

Type 284

Square Wave Amplitude	1.0 V
Period	1 μs
Mode	Square Wave Output
Lead Time	75 ns

Connect the Square Wave Output signal from the Type 284 to the input connector of the Sampling Head installed in the Channel B compartment through a 5 ns coaxial cable. Any applied signal (to Type S-1) should be 1 volt or less. This is the normal signal range for the Type S-1. See the sampling head specification of the Type S-1 or the S-Series sampling head you are using for further information. Connect the Trigger Output signal from the Type 284 to the 50 Ω external Trigger Input connector on the Type 3T2 through a 5 ns signal delay coaxial cable with BNC connectors.

Center the trace on the graticule with the A POSITION control, and if necessary use the DC OFFSET control. Adjust the Trig Sensitivity control on the Type 3T2 counterclockwise, then clockwise for a stable trace. Observe a square wave display. If its amplitude is 5 vertical divisions, the Type 3S2 GAIN adjustment on the front panel is properly set. If the amplitude is not 5 vertical divisions, adjust the GAIN control with a small screwdriver for 5 vertical divisions.

Now check Channel A by applying the input signal to the input connector of the sampling head installed in the Channel A compartment. Change the Display Mode switch to CH A.

NOTE

Operating the sampling head without the input connector terminated by a 50 Ω resistor or coaxial cable will cause a vertical shift to the zero signal baseline by a few millivolts. This occurs because the strobe kickout signal is reflected from the open input connector. The kickout signal arrives back at the sampling bridge during sampling time, while the bridge is still conducting. To avoid this, set the display zero reference point with the input circuit connected, not before connecting it. Also use at least 20 cm of airline between the Type S-1 input and a fast generator or circuit that is sensitive to the fast Strobe kickout signal.

Experiment with the various Channel B front-panel controls, and notice the effect of each. For example, note the effect of the POSITION control in positioning the display above and below the zero reference level at the graticule centerline. Return the Position control back to midrange, and turn the DC OFFSET control counterclockwise to position the upper portion of the square wave to the graticule centerline. This new reference level, set by the DC OFFSET control, can be monitored at the OFFSET ×10 10 kΩ jack.

Now, notice that the POSITION control positions the display above and below the new reference level.

FUNCTION OF FRONT PANEL CONTROLS AND CONNECTORS

A special removeable knob is used on the three controls A DOT RESPONSE, B DOT RESPONSE and B DELAY allowing these controls to be screwdriver adjusted. Knob removal may be an operator convenience in production line applications. Pull the knob away from panel to remove. Observe the internal spring wire orientation before replacing a knob. The spring wire should slide into the control shaft screwdriver slot to prevent knob slippage at the end of control rotation.

Display Mode Switch — Selects one of the five following display modes.

- **CH A** — The Channel A signal is displayed.
- **CH B** — The Channel BB signal is displayed.
- **DUAL-TRACE** — Both channel signals are displayed, but each trace has one-half the normal number of dots per sweep. The display switches from CH A to CH B after each CH A dot, and vice versa. While operating in Dual-Trace, one sweep contains the same number of dots as if only one channel were displayed.
- **A + B** — The algebraic sum (±A±B as selected with the INVERT switches) of the two Channels is displayed.

A VERT B HORIZ — The Channel A signal is displayed vertically and the Channel B signal is displayed horizontally for X-Y operation. Functions only with sampling sweep units.

NORMAL-SMOOTH (Red knob concentric with the Display Mode switch) — Selects unity loop gain at NORMAL, and reduces the loop gain to ≤0.3 at SMOOTH. NORMAL provides the correct loop gain required when measuring risetime. SMOOTH reduces the effect of random noise on the display while requiring high sampling dot density for the correct displayed risetime.

POSITION Controls — Adjust the vertical position of the A and B displays independently. (The B position control becomes the horizontal position control in the A VERT B HORIZ mode.)

DC OFFSET ±1 V Controls — These controls apply internal signal offset voltages of +1 to −1 volt to the sampling head (unless otherwise stated on the sampling head front panel). The input signal zero reference (related to the CRT) is the DC Offset voltage instead of ground. Permits all portions of a maximum +1-volt input signal to be positioned through the CRT vertical "window" even at a deflection factor of 2 units/div (2 mV/Div with a Type S-1 or S-2).

The vertical window is a total of 16 mV when the deflection factor is 2 mV/Div, and 1.6 volts when the deflection factor is 200 mV/Div. The front panel OFFSET monitor jacks allow accurate slide-back voltage measurements to be made of part or all of a signal at 10× the actual offset voltage applied to the head.

Units/Div Switches — Selects calibrated deflection factor for each Channel. The units are selected and named on the adjacent S-Series sampling head. For example, with a Type S-1 sampling head in Channel A and the Channel A Units/Div switch set at 100, each major division of deflection corresponds to 100 millivolts of applied signal at the S-1 input connector when the VARIABLE Control is in the CAL position.

VARIABLE Controls (Same control knob with INVERT Switches) — Provides + and — Uncalibrated variation of the deflection factor between labeled values of the Units/Div switches. Counterclockwise rotation decreases the display size, increasing the deflection factor to at least 2.43 times the Units/Div calibrated value (display is ≤0.7 as large as when VARIABLE is at CAL). Clockwise rotation increases the display size, decreasing the deflection factor to at least 0.4 times the Units/Div calibrated value (display is ≥2.5 as large as when VARIABLE is at CAL).

INVERT Switches — In the Normal (pushed in) position, a positive input signal deflects the CRT beam upward. In the pulled position the displayed signal is inverted. When the Display Mode switch is set to A + B, algebraic addition of Channels A and B is obtained. The position of the INVERT switches determines the polarity of each channel before algebraic addition.

DOT RESPONSE — Allows the loop gain of each Channel to be adjusted to unity when the NORMAL-SMOOTH switch is in the NORMAL position.

GAIN — Matches the vertical output amplifier gain to the oscilloscope CRT deflection factor. (Does not affect the internal Digital Gain accuracy.)

TRIG OUT A or B Switch — When the sampling head contains a trigger pickoff circuit, selects the signal from Channel A or Channel B input circuit. Delivers the signal to the TRIG OUT jack on the front panel. (Such signals are useful for externally triggering a sampling sweep unit). It also selects an internal vertical signal facsimile from channel A or B for use in internal triggering of real-time time-base units.

B DELAY — Varies the time position of CH B display over a range of at least 10 ns. Time coincidence will depend upon the time difference of sampling heads and sampling head extender cable units.

VERT OUTPUTS

A OUTPUT .2 V/DIV, 10 kΩ — The Channel A facsimile signal (the same Memory output signal that drives the Vertical Amplifier) is available at this con-

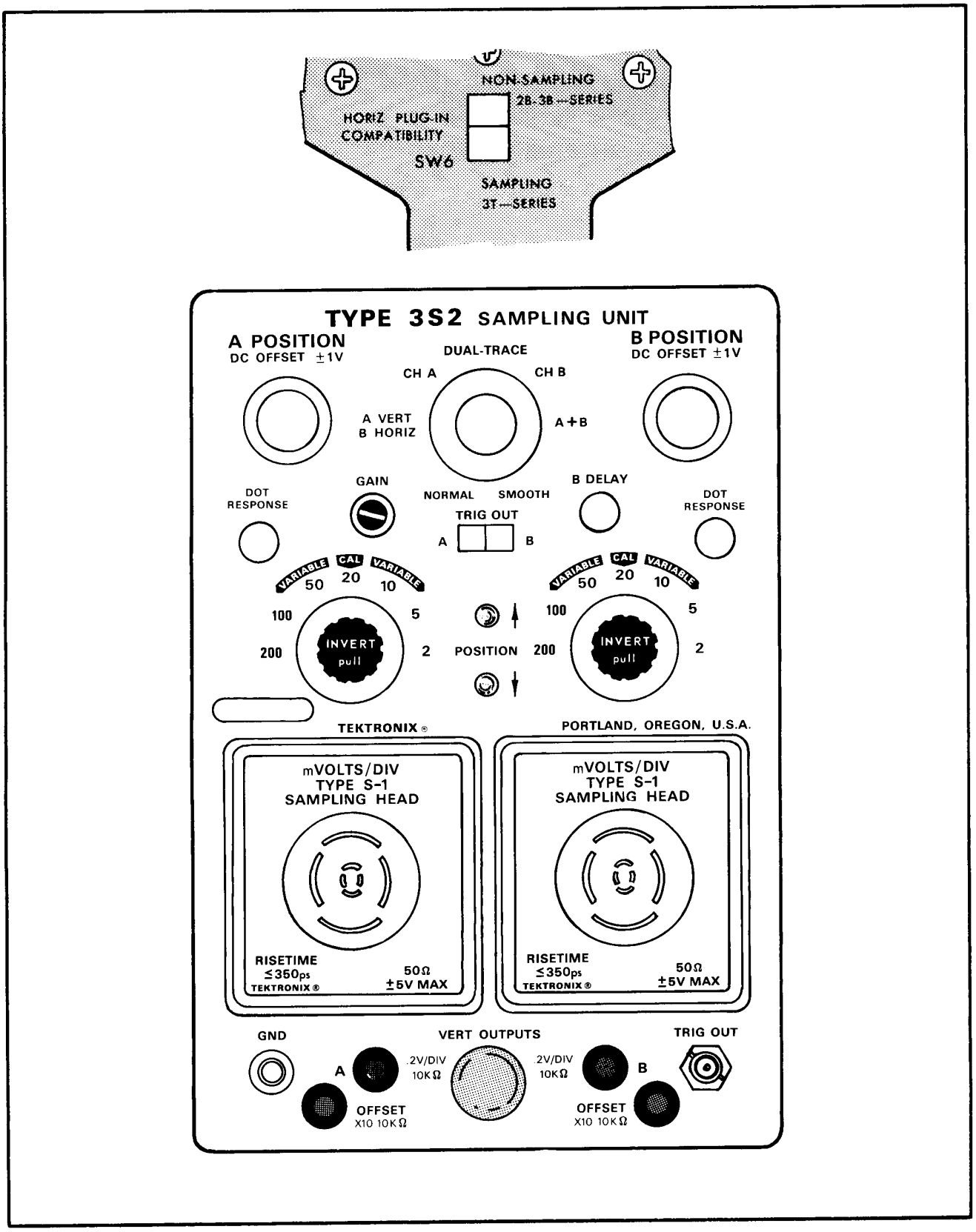


Fig. 2-2. Control Setup Chart.

	nector. The front panel labeled open-circuit deflection factor of 0.2 V per division of CRT deflection applies only when the Units/Div VARIABLE control is at its CAL detent position. (The VARIABLE control alters the CRT deflection factor but does not change the signal amplitude fed to the VERT OUTPUT jacks.) Maximum open-circuit signal amplitude is ±4 volts for all Units/Div switch controlled deflection factors. Output voltage swing is not limited to the magnitude displayed on the CRT. Permits a non-sampling type oscilloscope to monitor the facsimile signal the equivalent of 40 CRT divisions when the Units/Div switch is at 2 (mV/Div). Output resistance is 10 kΩ. Output amplitude is not affected by the Display Mode switch position.
B OUTPUT .2 V/DIV, 10 kΩ	Performs the same function for Channel B.
A OFFSET ×10 10 kΩ	Unless otherwise specified on the sampling head front-panel, the open-circuit voltage at this jack is 10 times the internal DC Offset voltage as set by the Channel A DC OFFSET control. The output resistance is 10 kΩ.
B OFFSET ×10 10 kΩ	Unless otherwise specified on the sampling head front panel, the open-circuit voltage at this jack is ten times the internal DC Offset voltage as set by the Channel B DC OFFSET control. The output resistance is 10 kΩ.
TRIG OUT BNC Connector SN B040250-up	When the sampling head contains a trigger pickoff circuit, this connector presents the input signal (before it is sampled) from either the Channel A or the Channel B head, as selected by the TRIG OUT switch. Signal amplitude into 50 Ω is approximately equal to the signal input to the sampling head.
TRIG OUT BNC Connector SN B010101-B030249	When the sampling head contains a trigger pickoff circuit, this connector presents the input signal (before it is sampled) from either the Channel A or the Channel B head, as selected by the TRIG OUT switch. Signal amplitude into 50 Ω is approximately equal to the signal input to the sampling head; amplitude into 1 MΩ is ≈2.5× the input signal. (See Table 2-1 this section.)

Control Setup Chart

Fig. 2-2 is a chart of the Type 3S2 front panel controls, showing two S-Series sampling heads installed. Also shown, is the internally located Horiz Plug-In Compatibility switch. This figure may be reproduced and used as a test setup record for special applications or procedures, or it may be used as a training aid for familiarization with this instrument.

BASIC OPERATING INFORMATION

Dual Trace

The dual-trace feature of the Type 3S2 permits observing Channels A and B simultaneously. This is useful for comparing amplitude, risetime, waveshape, and time relationship of two signals. The sweep may be triggered on information related to either channel. Be sure to trigger from the channel with the earliest signal event. Use input signal cables with equal delays to preserve the time relationship of the two signals.

The B DELAY control adds a variable to the time coincidence of Channel B in relation to Channel A sampling time. The B DELAY range of 10 ns will accommodate small time differences in cables or sampling heads, so that both signals can be displayed in time coincidence.

For dual trace operation, set the controls as follows:

Type 3S2

Horiz Plug-In Compatibility (behind front panel)	Sampling
Display Mode	DUAL-TRACE
NORMAL-SMOOTH	NORMAL
DC OFFSET (both Channels)	Midrange (5 turns from one end)
POSITION (both channels)	Midrange
Units/Div (both Channels)	100
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Push in
DOT RESPONSE	Midrange
B DELAY	Midrange
TRIG OUT switch	Optional

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep rate	100 ns/Div
Range	1 μs
Display Mag	×1
Time Magnifier	×1
Variable	Cal
Time Position	Both fully clockwise
Trig Sensitivity	For triggered display
Recovery Time	Counterclockwise
Trigger Polarity	+
Trigger Source	Ext

Type 284

Square Wave Amplitude	1.0 V
Period	1 μs
Mode	Square Wave Output
Lead Time	Optional

Connect the Square Wave Ouput signal to Channel A

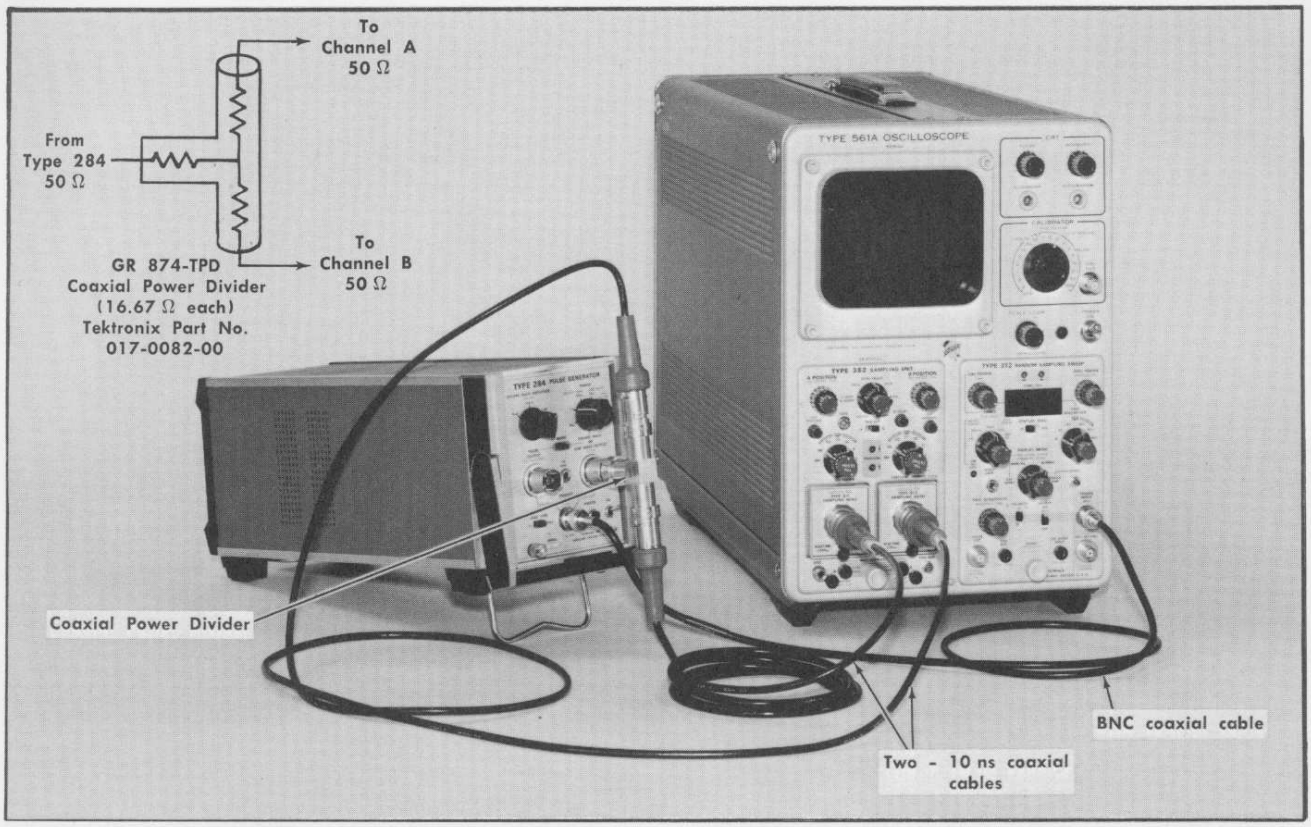


Fig. 2-3. Initial Power divider connections.

and Channel B input connectors through a power divider and two 5 ns coaxial cables. See Fig. 2-3. Connect the Type 284 Trigger Output signal to the Type 3T2 50 Ω external trigger input connector through a 50 Ω coaxial cable.

Adjust the Type 3T2 Trig Sensitivity control for a stable display. Center both traces on the graticule with the POSITION controls, and if necessary use the DC OFFSET controls. One half of the Type 284 signal is applied to each input. This properly triggered dual-trace display will be similar to Fig. 2-4A.

Dot Response. A convenient way to adjust the DOT RESPONSE control so each channel loop gain is unity is to cause double or multiple triggering of the sweep, so that each sample must respond to the full 0.5 volt (full signal amplitude). Turn the Type 3T2 Trig Sensitivity control clockwise into the free-run region, and adjust the Recovery Time control until the display is similar to Fig. 2-4B. In this typical double triggered display, Channel A is at less than unity loop gain, and requires clockwise rotation of its DOT RESPONSE control to obtain a display as shown for Channel B. Adjust the DOT RESPONSE control for the best flat upper or lower portions of the square wave display.

NOTE

The maximum allowable amplitude of the signal into the sampling head input for unity loop gain depends upon the sampling head used. For example, 0.5 V with the Type S-1, and 0.2 V with the Type S-2.

Double or multiple triggering is useful to adjust the DOT RESPONSE control for unity loop gain. However, this type of display should be avoided in normal operation, since it is a false triggered display.

B DELAY. To show B DELAY control operation, change the following controls from the preceding operation:

Type 284

Mode Switch	Pulse Output

Type 3S2

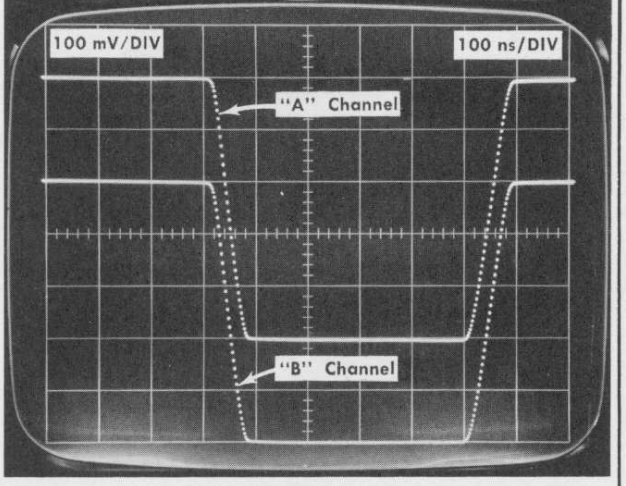
Units/Div (both Channels)	50

Type 3T2

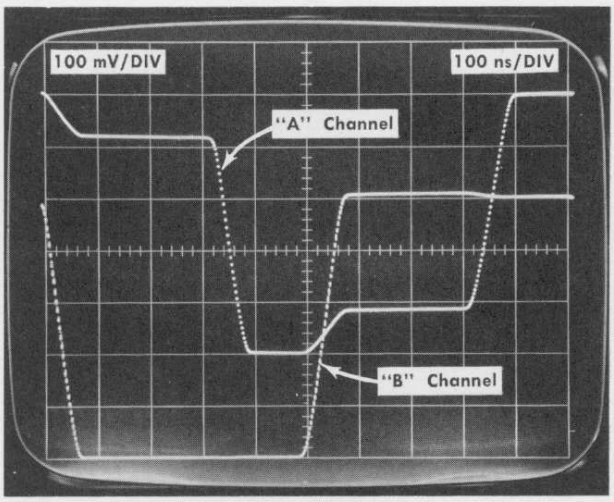
Start Point	Before Trigger
Sweep rate	2 ns
Range	100 ns
Time Magnifier	×5

Connect the Pulse Output signal into the power divider by moving the power divider input to the Pulse Output connector on the Type 284.

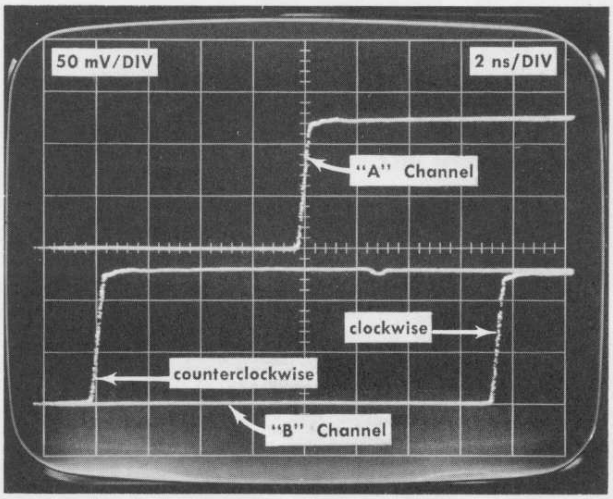
Adjust the Trigger Sensitivity and the Time Position controls on the Type 3T2 to display Channel A step signal at the horizontal center of the graticule (see Fig. 2-4C).



(A) Proper Dual-Trace Triggering

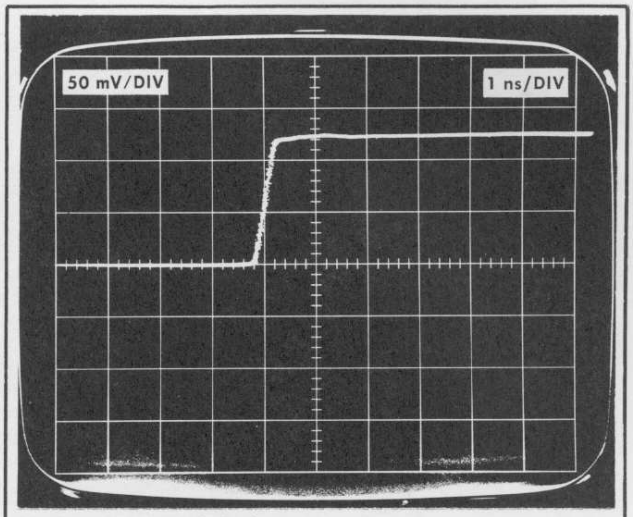


(B) Multiple triggering to check DOT RESPONSE operation

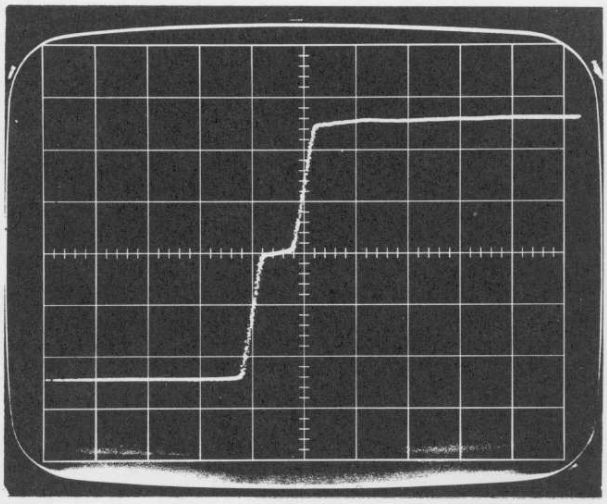


(C) Variable B DELAY operation (double exposure)

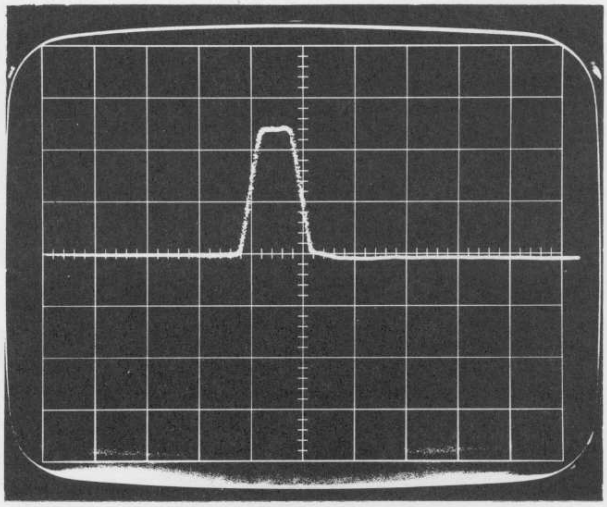
Fig. 2-4. Typical Displays to show dual trace operation.



(A) A or B Channel display



(B) A + B both INVERT switches in the same position



(C) A + B one INVERT switch in the out position

Fig. 2-5. Displays used to show A + B operation.

Operate the B DELAY control to show the variable time relationship between operation of the A and B Channels. Fig. 2-4C is a double exposure display showing the clockwise and counterclockwise positions of the B DELAY control.

Adjust the B DELAY control to move the Channel B step display to the same horizontal position as that of the Channel A step display. This coincidence of the two Channel displays shows that the B Delay circuit has compensated for the small delay differences in the two signal paths.

A + B

The algebraic addition of two signals can be obtained with the Display Mode switch set in the A + B position. The variable B DELAY control can be useful to compensate for small time differences in the setup before making accurate algebraic addition of the two signals. For accurate algebraic addition, the sampling heads for Channel A and B should be the same.

The following example uses a single test signal to both Channels through identical length cables or probes.

For A + B operation, set the controls as follows:

Type 3S2

Horiz Plug-In Compatibility (behind front panel)	Sampling
Display Mode	A + B
NORMAL-SMOOTH	NORMAL
A and B POSITION	Midrange
DC OFFSET (both Channels)	Midrange
Units/Div (both Channels)	50
VARIABLE (both Channels)	CAL
INVERT	Push in
DOT RESPONSE (both channels)	Midrange
B DELAY	As in procedure below
TRIG OUT Switch	Optional

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep rate	1 ns
Range	100 ns
Display Mag	×1
Time Magnifier	×10
Variable	Cal
Time Position	As required
Trig Sensitivity	Fully clockwise
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	Ext

Type 284

Mode	Pulse Output
Lead Time	75 ns. Optional with Type 3T2 Start Point switch at Before Trigger.

Connect the Pulse Output signal from the Type 284 to the Channel A and B input connectors on the sampling heads. Use a power divider and two 5 ns coaxial cables in the arrangement shown in Fig. 2-3.

Connect the Trigger Output signal from the Type 284 to the External Trigger input 50 Ω connector on the sampling sweep unit, through a 5 ns signal delay 50 Ω coaxial cable.

Initially set the Display Mode switch to CH A or B and set the Sampling Sweep Unit for an external-triggered 1 ns/Div stable sweep. Set the time position control as necessary to obtain a display similar to Fig. 2-5A.

Set the Display Mode switch to DUAL-TRACE and adjust the B DELAY control until both displays are in time coincidence. Set the Display Mode switch to A + B. Addition of the two signals will be displayed. Turn the B DELAY control and notice its effect upon the composite display. Fig. 2-5B shows the composite A + B display with the B DELAY control adjusted about 1 ns away from time coincidence of the two signals.

Pull one of the INVERT switches, inverting one of the Channel signals. Now any time difference of the two Channel signals will display a pulse, while those portions of the two signals that are equal and opposite will display a straight line. Adjust the B DELAY control and notice the change in polarity of the pulse as Channel B passes through time coincidence with Channel A. See Fig. 2-5C.

Adjust the B DELAY control for minimum time difference. The display will approach a single trace with no vertical deflection (if the two sampling heads are identical). When the composite A + B display is a straight line, the B DELAY control has adjusted the Channel B display to time coincidence with the Channel A display.

A VERT B HORIZ

A display of Channel A vertically and Channel B horizontally can be obtained with the Display Mode switch in the A VERT B HORIZ position. Use a sampling sweep unit. This unit contains the horizontal amplifier and provides the sampling drive pulse for the Type 3S2. Use any time-related signals to the input connectors of the sampling heads. The signals should not exceed the input signal specifications of the sampling heads.

An initial adjustment is necessary if accurate phase measurements (time relationships) between the two signals are required. Use the variable B DELAY control to compensate for small time differences between the two Channel signal paths. This control acts as a variable phase shift control for Channel B in this A VERT B HORIZ (X-Y) operating mode. Use the same signal on both Channels, through the

same setup cable or probes that will be used when making the phase adjustments. Once the B DELAY is adjusted to the desired position (usually an in-phase display) the phase differences between two signals can be shown.

The initial phase adjustment is made in the DUAL-TRACE position of the Display Mode switch. Use a test pulse-type fast-rise signal to both Channels through identical length cables or probes. Tektronix Type 284 is used in the following initial adjustment.

Set the controls as follows:

Type 3S2

Horiz Plug-In Compatibility	Sampling
Display Mode	DUAL-TRACE
NORMAL-SMOOTH	NORMAL
A and B POSITION	Midrange
DC OFFSET (both Channels)	Midrange (5 turns from one end)
Units/Div (both Channels)	50
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Push in
DOT RESPONSE (both Channels)	Midrange
TRIG OUT Switch	Optional

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep rate	1 ns/Div
Range	100 ns
Display Mag	×1
Time Magnifier	×10
Variable	Cal
Time Position	Both fully clockwise
Trig Sensitivity	Described below
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	Ext

Type 284

Mode	Pulse Output
Lead Time	75 ns

Connect the Pulse output signal from the Type 284 to the Channel A and B input connectors on the sampling heads. Use a power divider and two 5 ns coaxial cables in the arrangement shown in Fig. 2-3. Connect the Trigger Output signal from the Type 284 to the External Trigger input 50 Ω connector on the sampling sweep unit through a 5 ns signal delay 50 Ω coaxial cable.

Adjust the Type 3T2 Trig Sensitivity control for a stable display. Center both traces on the graticule with the Position controls, and if necessary use the DC OFFSET controls. Adjust the Time Position control on the Type 3T2 to display step signals on both Channels. Adjust the B DELAY control to move the Channel B step display to the same position as that of Channel A step display; See Fig. 2-6A. This horizontal time coincidence of the two Channel displays is a preliminary adjustment, preparing the system to measure the phase relationship of two harmonically-related input signals to the two 5 ns cables. Fine adjustment is described below.

Disconnect the Type 284 Pulse signal generator. Change the following controls for A VERT B HORIZ (X - Y) operation.

Type 3S2

Display Mode	A VERT B HORIZ
Units/Div (both Channels)	As desired

Type 3T2

Samples/Div	Midrange
Trig Sensitivity (Leave all other controls as set)	Fully clockwise

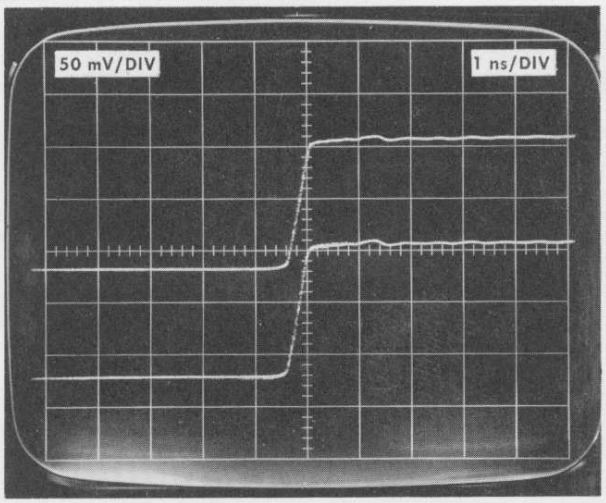
Use a sine wave input signal into the power divider in the same setup as in the initial setting above. The signal should not exceed the specifications of the sampling heads. Center the display with the POSITION controls, and if necessary use the DC OFFSET controls. The A POSITION control on the Type 3S2 will control the vertical position of the display, and the B POSITION will control the horizontal position of the display. The display will be similar to Fig. 2-6B. A fine adjustment of the B Delay control may be required to eliminate phase difference at the inputs of the two 5 ns coaxial cables.

After these adjustments, the system is ready to show accurate phase difference displays over a wide range of frequencies. Connect the signals to the inputs to the two 5 ns coaxial cables. Figure 2-6C shows a method of calculating phase difference of two sine waves.

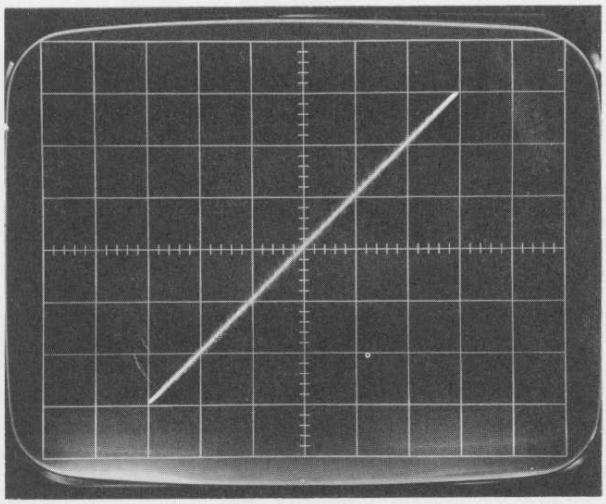
Real Time Sampling

For Real Time Sampling operation use a conventional or real-time time-base unit such as Type 2B67, 3B1, 3B2, 3B3, 3B4 or 3B5. The Type 3S2 provides 100 kHz clock-controlled Strobe Drive pulses to each sampling head, independent of the real-time time-base unit. The repetitive Strobe Drive pulses are turned on when the internal Horiz Plug-in Compatibility switch is set to the Non-Sampling position. A chopped replica trigger signal (the actual input signal, chopped at a 100 kHz rate, amplified after the Memory circuit), is available for internal triggering. The front panel TRIG OUT switch selects which channel chopped replica signal drives the real-time time-base unit, permitting internal triggering from either channel. Real time internal triggering is available even when the sampling head does not contain a trigger pickoff circuit.

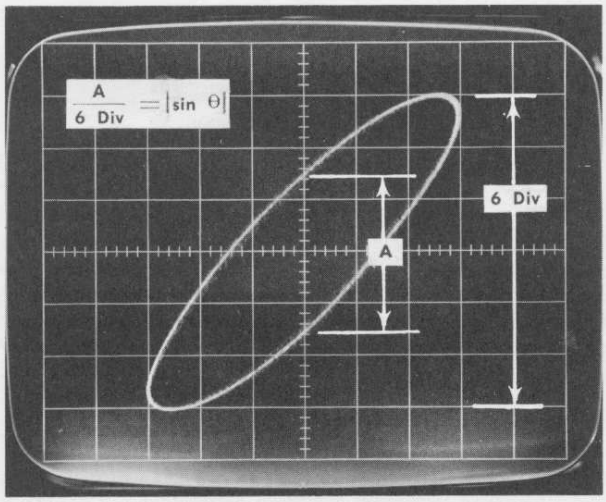
Connect the signals to be observed to the input-connectors of the sampling head (or heads) installed in the Type 3S2.



(A) Initial B DELAY adjustment



(B) In phase



(C) Approx. 30° phase difference. (A is approx. 3 Div)

Fig. 2-6. A VERT B HORIZ operation including (A) initial setup (Dual Trace) (B & C), 500 MHz X-Y display.

Input signals should not exceed the input signal specifications of the sampling head. The following examples use a Tektronix Type 106 Square-Wave Generator at 1 kHz, then at 10 kHz.

For single channel real time operation, set the controls as follows:

Type 3S2

Horiz Plug-In Compatibility	Non Sampling
Display Mode	CH A
NORMAL-SMOOTH	NORMAL
DC OFFSET (Channel A)	Midrange (5 turns from one end)
Units/Div (Channel A)	100
VARIABLE (Channel A)	CAL
INVERT (Channel A)	push in
POSITION	Midrange
DOT RESPONSE (both Channels)	Midrange
B DELAY	Midrange
TRIG OUT switch	A

Type 3B4

Position	Midrange
Time/Div	.2 ms
Magnifier	unmagnified
Trigger Mode	Norm
Triggering Level	as required
Source	Int
Coupling	AC
Slope	+

Connect the Type 106 Fast Rise + output signal through a coaxial cable to the input connector on the sampling head installed in the Channel A compartment of the Type 3S2. Set the Repetition Rate Range switch and Multipliers for 1 kHz. Set the + Transition Amplitude control fully clockwise.

Adjust the Triggering Level control on the Type 3B4 for a stable trace. The display will be similar to that of Fig. 2-7A. Notice that with the constant sampling rate of 100 kHz, the upper and lower portions of the square wave display shows no obvious dots or segments.

Change the Repetition Rate Range switch and the Multiplier on the Type 106 for 10 kHz. Set the Time/Div switch on the Type 3B4 to 20 μs/Div. Observe that the display is segmented. See Fig. 2-7B. This shows the fast sweep rate limitation of real time sampling. The range of sweep rates available for use in real time sampling is from the lowest rate available on the real-time time-base unit to about 0.1 ms/Div. At 0.1 ms/Div about 10 dots per division will be displayed.

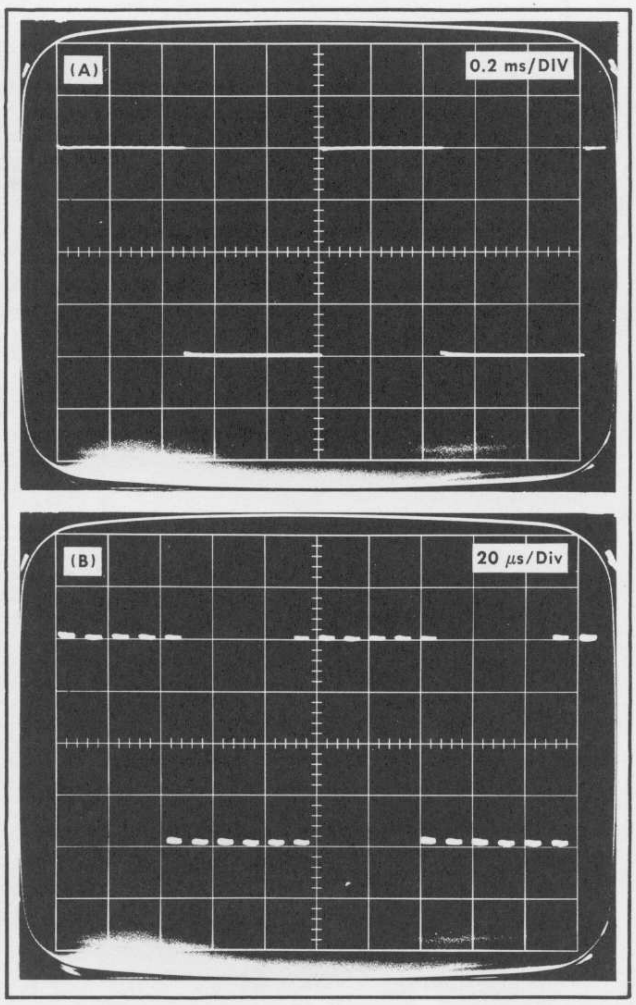


Fig. 2-7. Real Time display of (A) 1 kHz and (B) 10 kHz square wave showing the fast sweep rate limitations.

Real time sampling offers slower sweep rates at the full bandwidth of the sampling head installed in the Type 3S2. Other characteristics are reduction of random noise in the display through smoothing, and DC offset capabilities matched with good overload recovery.

Useful operating modes for Real Time sampling are CH A or CH B, DUAL-TRACE, and A+B. Real Time operation does not permit the A VERT B HORIZ mode. In this mode, only the Channel A signal will be displayed.

Numerical real time voltage measurements can be made with the Type 3S2 when used with a readout system such as Tektronix Type 567 with Type 6R1A and Type 3B2, or Tektronix Type 568 with Type 230 and Type 3B2. Useful modes of operation for these measurements are: CH A (or CH B), and DUAL-TRACE.

Gain Adjustment

The GAIN control (a front-panel screwdriver adjustment) matches the gain of the Type 3S2 vertical output amplifier to the Oscilloscope CRT deflection factor. The gain should be checked and adjusted each time the Type 3S2 is used with a different oscilloscope.

An accurate known voltage source should be used into the input connector of the sampling head. The signal source impedance must be considered when it drives the input of a 50 Ω sampling head.

For 50 Ω input sampling heads, the Tektronix Type 284 or a precision chopped voltage can be used. The calibrator output of the indicator oscilloscope (with possibly decreased accuracy) can be used. Check amplitude specifications of the calibrator and use only the 50 Ω output position (usually 0.1 V into 50 Ω).

Using Type 284

Using the Type 284 as the signal source to check and/or adjust the GAIN control of the Type 3S2 and a 50 Ω sampling head, proceed as follows:

1. Allow the equipment to warm up for a least 5 minutes.
2. Set the controls as follows:

Type 3S2

Horiz Plug-in Compatibility	Sampling
Display Mode	CH B
NORMAL-SMOOTH	NORMAL
A and B POSITION	Midrange
DC OFFSET (both Channels)	Midrange (5 turns from one end)
Unit/Div (both Channels)	200
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Pushed in
DOT RESPONSE (both Channels)	Midrange
B DELAY	Midrange
TRIG OUT Switch	B

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep rate	200 ns/Div
Range	10 μs
Display Mag	×1
Time Magnifier	×5
Variable	Cal
Time Position	Both fully clockwise
Trig Sensitivity	For Triggered Display
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	Ext

Type 284

Square Wave Amplitude	1.0 V
Period	1 μs
Mode	Square Wave Output
Lead Time	Optional

3. Connect the Square Wave Output signal from the Type 284 to the sampling head input connector in the Channel B compartment. Use a coaxial cable. Connect the Trigger Output signal from the Type 284 to the external Trigger Input 50 Ω connector on the Type 3T2 through a coaxial cable.

4. Adjust the Type 3T2 Trig Sensitivity control for a stable display. Center the trace on the graticule with the Channel B POSITION control. Observe a square wave display. If its amplitude is 5 vertical divisions, the Type 3S2 GAIN control is properly set. If the amplitude is not 5 vertical divisions, adjust the GAIN control with a small screwdriver for 5 vertical divisions.

5. Check Channel A by connecting the signal into the Sampling Head 50 Ω input connector installed in the Channel A compartment. Change the Display Mode switch to CH A. If the amplitude is not 5 vertical divisions refer to the Performance and Recalibration section of this Instruction Manual.

Using Oscilloscope Calibrator

NOTE

It is recommended that 60 Hz oscilloscope calibrators be used as a signal source for setting the Type 3S2 GAIN control only when no other source is available, and only after verifying the signal amplitude with accurate measuring equipment. The following procedure uses the Type 567 or Type 568 20 kHz Calibrator (500 mV into 50 Ω, ±2%), producing a Type 3S2 deflection factor accuracy of ±5%.

1. Allow the equipment to warm up for at least 5 minutes.

2. Set the controls as follows:

Type 3S2

Horiz Plug-In Compatibility	Sampling
Display Mode	CH B
NORMAL-SMOOTH	NORMAL
A and B POSITION	Midrange
DC OFFSET (both Channels)	Midrange (5 turns from one end)
Units/Div (both Channels)	100
VARIABLE (both Channels)	CAL
INVERT (both Channels)	Push In
DOT RESPONSE (both Channels)	Midrange
B DELAY	Midrange
TRIG OUT Switch	B

Type 3T2

Horiz Position	Midrange
Samples/Div	9 o'clock position
Display Mode	Normal
Start Point	With Trigger
Sweep Rate	10 μs
Range	100 μs
Time Magnifier	×1
Variable	Cal
Display Mag	×1
Time Position	Optional
Trig Sensitivity	For Triggered display
Recovery Time	Clockwise
Trigger Polarity	+
Trigger Source	Ext

3. Apply the signal from the indicator oscilloscope calibrator 500 mV into 50 Ω connector to the Channel B 50 Ω input connector of the sampling head installed in the Type 3S2. Use a coaxial cable and a BNC to GR adapter at the calibrator connector.

Connect the 18 inch trigger cable from the Type 3S2 TRIG OUT connector to the Type 3T2 external Trigger Input 50 Ω connector. Adjust the Trig Sensitivity control for a stable square wave display.

4. Center the display with the Channel B POSITION control and if necessary use the DC OFFSET control.

5. With the Channel B POSITION and DC OFFSET controls, align the display with the graticule lines and check for exactly 5 divisions of vertical deflection. If the amount of vertical deflection is not 5 divisions, adjust the GAIN control for 5 divisions.

6. Check Channel A by connecting the signal into the Sampling Head 50 Ω input connector installed in the Channel A compartment of the Type 3S2. Set the TRIG OUT switch to A. If the amplitude is not 5 vertical divisions refer to Section 6, Performance Check and Recalibration.

Vertical Outputs

A and B signals. Channel A and Channel B composite signals are available at the Vertical Output jacks. The signals at these jacks are taken after the sampling process, and are, therefore, proportional representations of the display signal rather than the input signals themselves. The output signal voltage follows the 100 kHz chop rate of the input signal in real time sampling. The open circuit voltage at either jack is 200 mV per division of display when the VARIABLE controls are in the CAL position. The maximum output is ±4 volts. The output resistance is 10 kΩ. The signals are taken prior to the Display Mode switch, and are therefore not affected by the mode of operation. They are affected only by the respective Units/Div switches, DC OFFSET controls, and the NORMAL-SMOOTH switch. The signals are not inverted by pulling the INVERT switches, and are not

affected by the POSITION controls. Output voltage swing is not limited to the magnitude displayed on the CRT. This permits a non-sampling type oscilloscope to monitor the facsimile signal the equivalent of 40 CRT divisions when the Units/Div switch is at 2 (2 mV/Div). Since the signals at the Vertical Output jacks are equivalent time signals, they are useful for pen recorder applications when the sampling sweep unit external input is driven by the recorder.

OFFSET Outputs. The two offset monitor jacks permit accurate measurement of the DC voltage set by the DC OFFSET controls. Each monitor jack output voltage has a range of +10 to −10 volts. Unless otherwise specified on the sampling head front panel the monitor jack output voltage is ten times the internal DC Offset voltage. The output resistance is 10 kΩ.

TRIG OUT, SN B040250-Up. The TRIG OUT connector makes available an amplified portion of the input signal when the sampling head contains a trigger pickoff circuit. This signal can be used for external triggering of equivalent time sampling sweep units. The voltage output at the TRIG OUT connector is approximately equal to the input.

Risetime of the trigger pickoff circuit in the sampling heads Types S-1 and S-2, including the Type 3S2 Trigger Amplifier characteristics, is stated in Section 1. No limits are specified when the TRIG OUT connector drives 1 MΩ.

Normal use of this form of internal triggering is to drive the sampling sweep unit external trigger input 50 Ω connector. The TRIG OUT signal is not useful for externally triggering a real-time time-base unit.

The TRIG OUT signal is useful to externally trigger a random sampling sweep plug-in unit such as the Type 3T2. To operate the Type 3T2 in random sampling mode, set the Start Point switch to Before Trigger. Connect the TRIG OUT signal to the external Trigger Input 50 Ω connector with the short coaxial cable provided with the Type 3S2. Proper displays triggered from the TRIG OUT signal are easy to obtain during random sampling when the signal is cyclic square or sine waves.

NOTE

The Lead Time control in the Type 3T2 may require clockwise adjustment if you are unable to see the pulse rise (plus transition) when using the TRIG OUT signal and random sampling. If a pulse display can be obtained when the two Type 3T2 Time Position controls are fully clockwise, the internal Lead Time control is correctly adjusted. Refer to the Calibration section of the Type 3T2 Instruction Manual.

TRIG OUT, SN B010101 - B030249. Table 2-1 shows the output voltage available into 50 Ω and into 1 MΩ, to trigger normal-process (not random process) equivalent time sampling sweep unit.

No trigger signal risetime limits are specified in Section 1 when the TRIG OUT connector drives 1 MΩ, but the increase in gain slows it considerably. Risetime into 1 MΩ is approximately 0.3 μs, 10% to 90%, with considerable rounding during the last 10%. Open-circuit DC output voltage is about −2.5 volts. It can swing positive from ground no more than about +2 volts, but negative from ground to about −12 volts. Thus, when using the TRIG OUT signal into a 1 MΩ load, severe distortion occurs to the signal when the sampling head input signal is greater than about +1.8 volts.

Fig. 2-8 shows two double exposures of random sampling attempts to measure a pulse risetime with a Type S-1 Sampling Head, while triggering the Type 3T2 with the TRIG OUT signal. The left waveform in each photo indicates a false risetime and includes a few holes in the horizontal portions. The right waveform in each photo indicates a correct risetime. All four exposures were made with the Type 3T2 operating in the random sampling mode. Triggering is by an external pretrigger signal for both right waveforms and by the Type 3S2 TRIG OUT signal for both left waveforms. The obvious change in risetime and the increased transition jitter show that the TRIG OUT signal is not always useful for fast risetime displays. Slower sweep rates for displaying cyclic signals produces no such distortions of the CRT display when using the TRIG OUT signal and random sampling.

TABLE 2-1

TRIG OUT Signal Amplitudes SN B010101 - B030249

Signal Input into S-1 or S-2 Sampling Heads	TRIG OUT (front panel)	
	into 50 Ω	into 1 MΩ
±2 V	400 mV	+2 to −7.6 V DC
±1 V	200 mV	0 to −5 V DC
0.5 V	50 mV	1.25 V P-P
0.4 V	40 mV	1 V P-P
0.3 V	30 mV	750 mV P-P
0.2 V	20 mV	500 mV P-P
0.1 V	10 mV	250 mV P-P
50 mV	5 mV	125 mV P-P
20 mV	2 mV	50 mV P-P
10 mV	1 mV	25 mV P-P

BASIC APPLICATIONS

Vertical Deflection Measurements

Vertical displacement of the trace on the CRT is directly proportional to the signal at the input connector of the sampling head installed in the Type 3S2. The amount of displacement for a given signal can be selected with the Units/Div switch. To provide sufficient deflection for best resolution, set the Units/Div switch so the display spans a large portion of the graticule. Also, when measuring between points on the display, be sure to measure consistently from either the bottom, middle, or top of the trace. This prevents the width of the trace from affecting the measurements.

To make a vertical deflection difference measurement between two points on the display, proceed as follows:

1. Note the vertical deflection, in graticule divisions, between the two points on the display. Make sure the VARIABLE control is in the CAL position.

NOTE

The vertical deflection factor is determined by the Units/Div switch and the value of the units of measure as stated on the sampling head front panel. The ratio of the input signal to the resultant

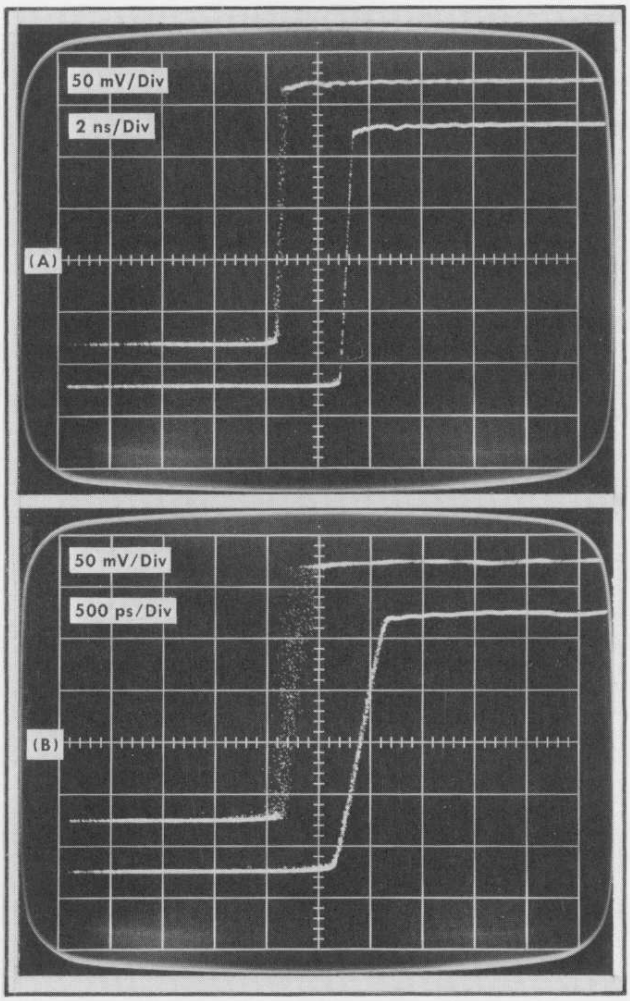


Fig. 2-8. Random sampling operation using TRIG OUT signal for Ext. triggering Type 3T2 (SN B010101-B040249).

deflection is called the deflection factor. For example, with the sampling head unit values stated as mV/Div, and the Units/Div switch set to 20, the vertical deflection factor will be 20 mV/division.

2. Multiply the divisions of vertical deflection by the deflection factor, and the external attenuator or probe attenuation factor (if any). The product is the voltage difference between the two points measured.

For example, suppose you measure 4.4 divisions of deflection between two points on the display and the Units/Div switch is set for 20 mV/Div. Multiply 20 millivolts/division by 4.4 divisions, the product is 88 millivolts. This is the voltage difference at the input connector between the two points on the display. Now assume there is a 10× external attenuator (probe) between the input connector and the signal source. To determine the actual signal voltage at the source, multiply 10 (the attenuation factor of the probe) by 88 millivolts; this product (880 millivolts or 0.88 volts) is the actual voltage at the signal source.

It is also possible to measure an instantaneous (or DC) voltage to ground from the display. This measurement is accomplished in the same manner, except that with no signal applied, you must first establish a ground-reference point on the CRT.

NOTE

To establish the ground reference point be sure the input connector is either terminated by a 50 Ω resistor or coaxial cable connected to the input.

To do this, trigger the sampling sweep unit with the signal source and display a trace. Then, position the trace so it is exactly aligned with one of the gratciule lines. The actual graticule line you select will be largely determined by the polarity and amplitude of the applied signal. After establishing the ground reference, make no further adjustments with the Position or DC OFFSET controls.

Apply the signal and measure the voltage in the manner previously described. Make all measurements from the established ground reference point. Accuracy of this measurement is within ±3%.

If the applied signal has a relatively high DC level, the ground-reference point and the actual signal may be so far apart that neither will appear on the CRT. In this case, refer to the following discussion on "Voltage Measurements Using the DC Offset Control."

Voltage Measurements Using the DC OFFSET Control

Unless otherwise stated on the sampling head front panel, the DC offset voltage cancels the effects of an applied DC voltage of up to ±1 volt at the sampling head input. Also, accurate slideback amplitude measurements of the applied signal can be obtained by positioning the display at various points and measuring the amount of voltage change at the appropriate OFFSET monitor jack (left hand jack monitors Channel A, right hand jack monitors Channel B).

Source resistance for the voltage at the OFFSET monitor jacks is 10 kΩ; therefore, meter loading may be a factor if other than an infinite-impedance meter is used. The accuracy of the DC offset voltage measurement depends on the accuracy and the loading effect of the measuring device. The following measuring devices are recommended, in order of preference, for monitoring voltage at the OFFSET jacks.

(1) Differential, non-loading DC voltmeter with an accuracy of 0.2% or better. This type of device provides 2% accuracy of absolute offset voltage measurements. Measurements of small changes in offset voltage can be made more accurately than 2%.

(2) Vacuum-tube voltmeter with an input impedance of at least 10 megohms. Accuracy of the VTVM should be as high as practical.

(3) Zero-center ±1 mA milliammeter with as high an accuracy as practical. The milliammeter should be connected directly between the appropriate OFFSET monitor jack and ground. When using a milliammeter, 100 microamperes is equivalent to 1 volt open-circuit at the OFFSET monitor jack (0.1 volt of actual offset to the signal).

Slideback Measurement Procedure

To measure the voltage difference between two points on a waveform (such as peak or peak-to-peak volts), proceed as follows:

1. Set the appropriate DC OFFSET control to about mid-range.

2. Apply the signal to be measured to the appropriate input. Adjust for a stable display with about 7 divisions of vertical deflection between the two points of the signal to be measured.

3. With the POSITION and DC OFFSET controls, move one of the points to be measured to the center line of the graticule and measure the voltage at the appropriate OFFSET monitor jack. Use one of the measuring devices mentioned previously. DO NOT MOVE THE POSITION CONTROL AFTER THIS STEP.

4. With the DC OFFSET control, move the display so the other point to be measured is aligned with the centerline of the graticule and again measure the voltage at the OFFSET monitor jack.

5. Find the difference between the voltage measured in step 3 and the voltage measured in step 4, and divide by 10. The result is the voltage difference, in volts, between the two points on the waveform. This voltage tolerance is ±2% of the input signal plus the tolerance and loading effect of the measuring device.

Use of Smoothing

Random process sampling does not permit the use of smoothing. This process requires unity dot response to construct a coherent display from the samples taken at random. When using random process sampling, the random sampling sweep plug-in unit Start Point control will be in the Before Trigger position. In this position, operate the Type 3S2 in the NORMAL position of the NORMAL-SMOOTH switch, and adjust the DOT RESPONSE control to unity dot response.

Normal process sampling does permit the use of smoothing. Time and amplitude noise may sometimes be objectionable when operating at minimum deflection factors or maximum sweep rates. For Smoothing, turn the NORMAL-SMOOTH switch on the Type 3S2 to the SMOOTH position. This will reduce the random noise, about one half by decreasing the gain of the sampling feedback loop. Fig. 2-9 shows the advantage of using smoothing when observing a low-amplitude signal.

Dot Density. Normally the SMOOTH position of the NORMAL-SMOOTH switch will not significantly affect the risetime of the display if the dot density is sufficient. If, however, the display waveform shape is affected when the switch is changed from the NORMAL position to the SMOOTH position, a compromise must be made between smoothing and dot density. Fig. 2-10 illustrates the effect produced by using smoothing when the dot density is low. This effect can be compared to the high dot density of the same input signal as shown in Fig. 2-9B.

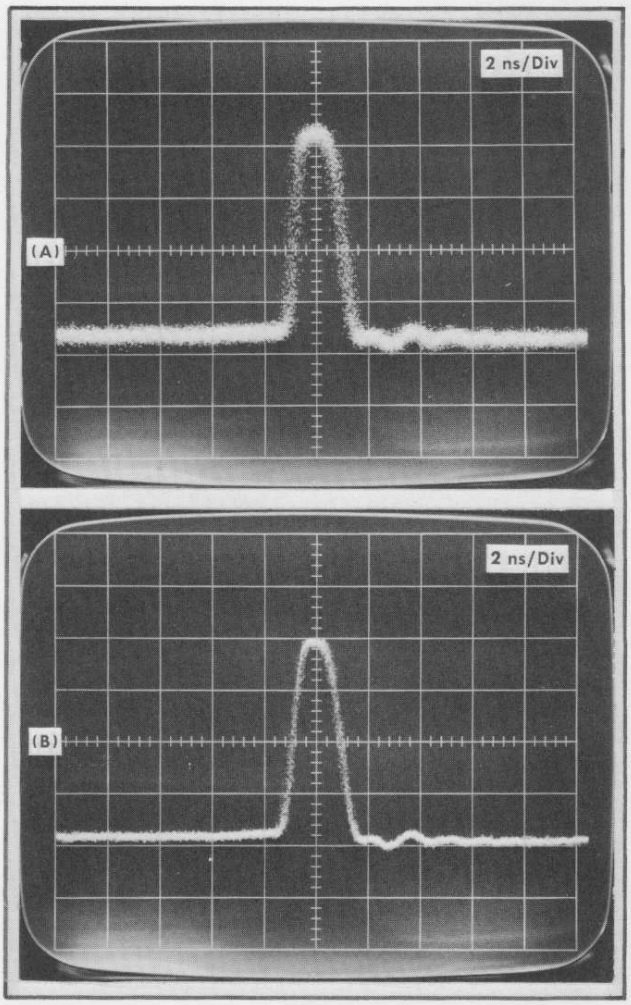


Fig. 2-9. Use of SMOOTH-NORMAL switch in normal process sampling for decreasing display noise when viewing a low-amplitude signal. (A) NORMAL-SMOOTH switch at NORMAL; (B) NORMAL-SMOOTH switch at SMOOTH.

"False" Displays

Because sampling displays only a fraction of any one cycle of a repetitive signal, it is sometimes possible to obtain a false equivalent-time display of the signal. The incorrect equivalent-time display occurs when the sampling rate is an exact multiple of the signal rate. Each sample vertical position represents the correct signal amplitude, but an incorrect number of samples is taken, causing the false equivalent-time display.

False equivalent-time displays can be detected by changing the sampling sweep unit Samples/Div control; i.e., changing the dot density. Occasionally such a false equivalent-time display occurs when the sampling sweep unit triggering circuit is adjusted to free run, and at the same time the triggering signal amplitude synchronizes it falsely. Any time the display equivalent time changes when changing the dot density alter the Time/Div switch to obtain a display with an equivalent time that does not change with dot density change. Usually the sweep rate should be increased (turn the Time/Div

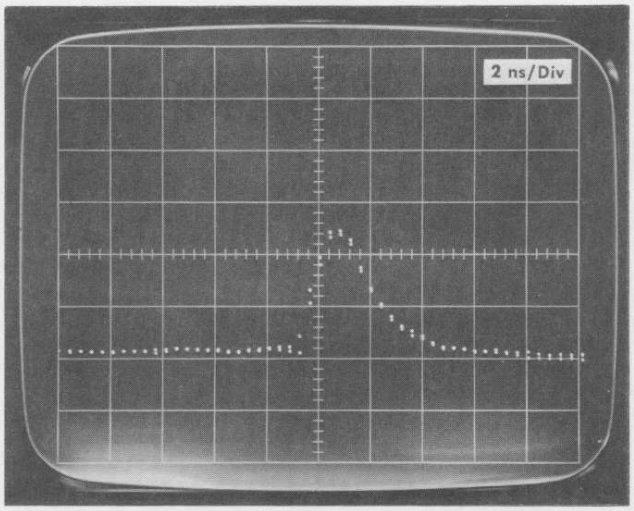


Fig. 2-10. Degraded display of signal shown in Fig. 2-9B, caused by use of smoothing with sampling sweep unit set for low dot density normal process sampling.

control clockwise), but some false displays can be obtained when the signal repetition rate is slower than can be shown by equivalent-time normal process sampling. When that occurs, the display can usually be corrected by changing to real-time sampling. Fig. 2-11 gives an example of a false and a correct display for two sweep rates when the signal is a 500 MHz sine wave.

Fig. 2-12 is a double triggered false display of a 100 ns period square wave. This display is useful to adjust the DOT RESPONSE control to unity dot response.

Digital Readout

The Type 3S2 will provide vertical information for use with several different Tektronix Digital Readout systems, such as those including the Type 567 and 6R1A with Type 262 Programmer, or the Type 568-Type 230 system. With either digital system, a time base plug-in, either sampling or real time is needed along with the Type 3S2.

Time Domain Reflectometry (TDR)

The Type 3S2 with the Type S-1 Sampling Head can be used for Time Domain Reflectometry displays. TDR using the Type 284 Pulse Generator is described in the Type 284 Instruction Manual. Very fast displays, and special TDR analysis of small reactances is possible with the Type S-2 and the Type 284. See the Type 1S2 Instruction Manual for information about such fast displays.

Pen Recorder Operation

The signals available at the A and B Vert Output jacks provide a convenient source for driving the Y axis of a pen recorder. It is common practice to manually scan the CRT (with the sampling sweep plug-in controls) while driving the time axis of the recorder with the sweep output voltage. Another method for pen recording is to couple the scanning voltage of the recorder to the external sweep input connector of the sweep unit. Be sure the sweep voltage from the recorder agrees with the limits of the input to the sampling sweep plug-in. The source resistance of the A and B output jacks is 10 kΩ. This impedance must be considered in the calibration of some types of pen recorder amplifiers.

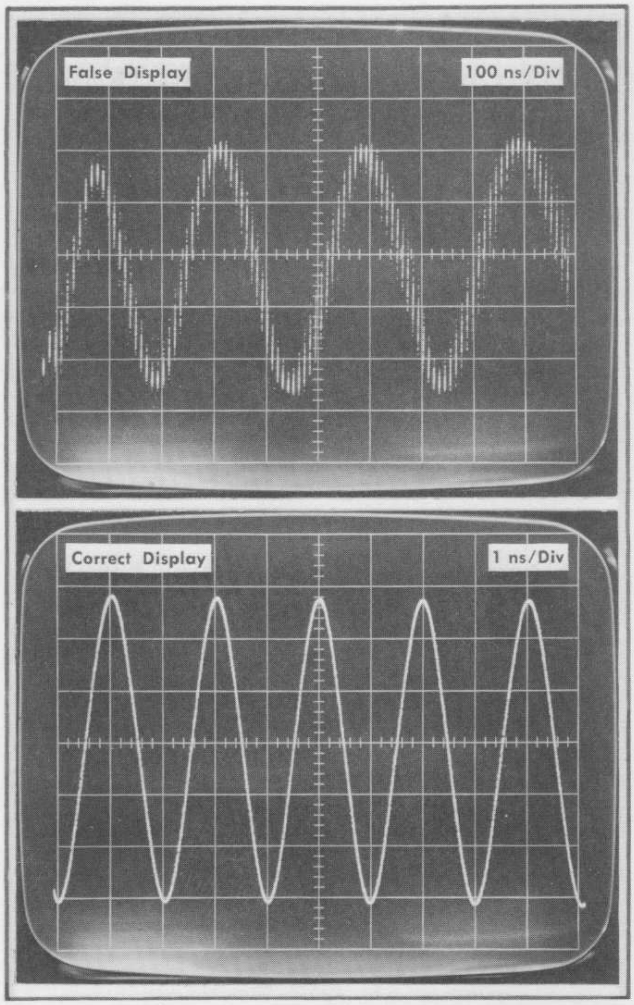


Fig. 2-11. Typical false and correct displays using a 500 MHz signal input.

Use of a Sampling Head Extender Cable

Two different sampling head extender cables are available for operating one or both sampling heads outside the Type 3S2. One is three feet long (Tektronix Part No. 012-0124-00), and the other six feet long (Tektronix Part No. 012-0125-00). Contact your Tektronix Field Engineer or Representative for price and availability information.

Sampling heads can be operated on either length extender cable without compromising system step function response. However, the extender cable signal delay must be considered in allowing proper pretrigger leadtime for normal process sampling. As compared to operating the sampling head inside the Type 3S2, use of a three foot cable adds about 5 ns to the

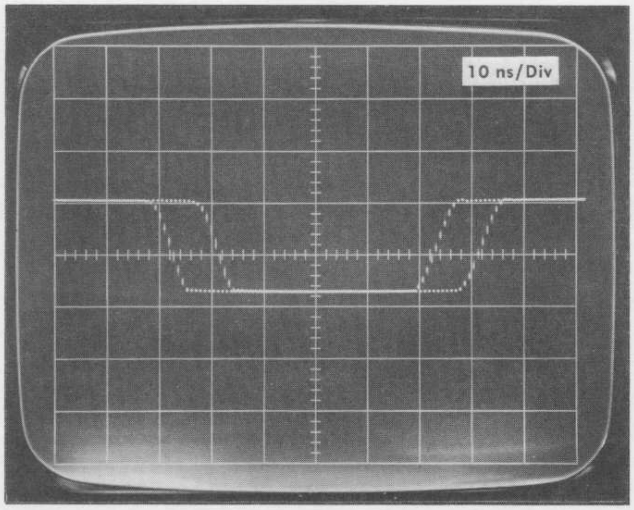


Fig. 2-12. Double triggered false display using a 100 ns period square wave.

required pretrigger leadtime; use of the six foot extender cable adds about 10 ns. To illustrate the above, assume the following conditions: Type 3T2 with Start Point Switch at With Trigger; Type S-1 or S-2 Sampling Head on 3-foot extender cable from Type 3S2 Channel A; external trigger 50 Ω coupling coaxial cable with 5 ns signal delay; and system operating in Type 568 oscilloscope. With these conditions, minimum trigger leadtime for a fast step display is 73 ns. If only 68 or 70 ns trigger leadtime is available, operate the sampling head and extender cable in Type 3S2 Channel B, using the B DELAY control to provide up to 5 ns more leadtime.

The B DELAY control can also restore the time coincidence of two identical sampling heads when one is operating on a three foot extender cable; not, however, when one head is on a six foot cable and the other inside the Type 3S2.

The first time a sampling head is operated on an extender cable, its Bridge Bal control may need adjustment, particularly if DC Offset measurements are to be made accurately referenced to ground. The sampling head instruction manual describes Bridge Bal adjustments. Readjustment of the control may be required when the sampling head is again installed directly into the Type 3S2.

Input Connectors

The type of sampling heads installed in the Type 3S2 determines the input impedance. Types S-1 and S-2 sampling heads are both 50 Ω input. 50 Ω coaxial cables may be used for applying input signals with minimum signal loss or distortion.

NOTE

Operating the sampling head without the input connector terminated by the 50 Ω resistor or coaxial cable will cause a vertical shift of the zero signal baseline by a few millivolts. This is because the strobe kickout signal is reflected from the open input connector. It arrives back at the sampling bridge during sampling time, while the bridge is still conducting. Set the display zero reference point with the input circuit connected, not before connecting it. Also use at least a 20 cm airline between the sampling head input and a fast generator or circuit that is sensitive to the fast strobe kickout signal.

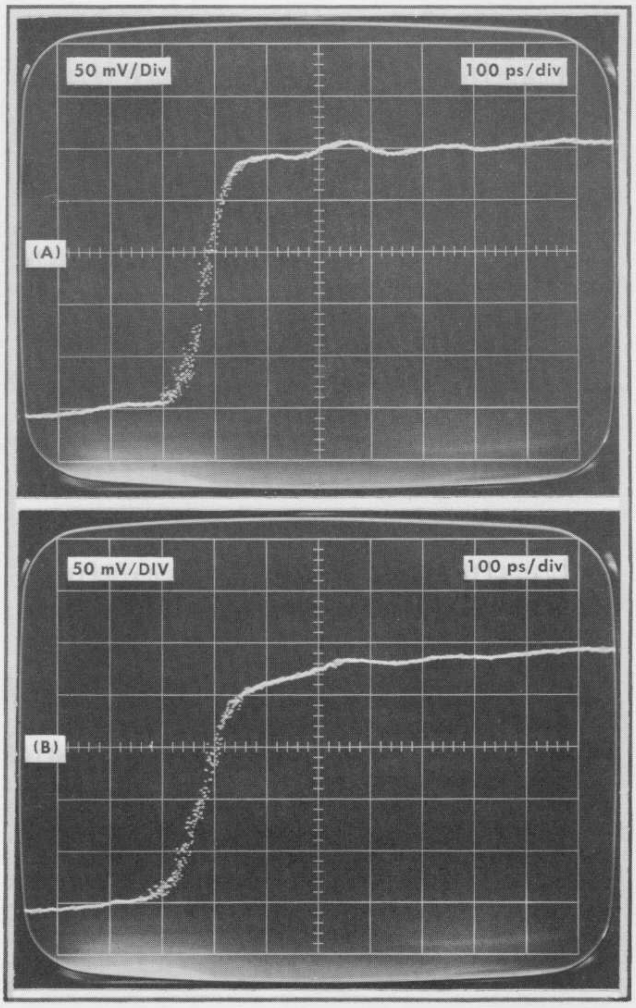


Fig. 2-13. Coaxial cable in a fast-rise system (A) using 5 ns-delay and (B) 15 ns-delay cable.

When connecting a signal to the input, many factors must be taken into consideration, including loading of the source, losses in coaxial cables, time delay, AC or DC coupling, attenuation of large signals and matching impedances at high frequencies.

Coaxial Cables

Signal cables that connect the vertical signal from the source to a 50 Ω input connector should have a characteristic impedance of 50 ohms. Impedance other than 50 ohms will cause reflections that may make it difficult to interpret the display. High-quality low-loss coaxial cables should be used

to ensure that all the information obtained at the source will be delivered to the input. If it is necessary to use cables with characteristic impedance other than 50 ohms, suitable impedance-matching devices will aid in obtaining meaningful displays.

The characteristic impedance, velocity of propagation and nature of signal losses in a coaxial cable are determined by the physical and electrical characteristics of the cable. Common coaxial cables, such as RG-213/U, have losses caused by energy dissipation in the dielectric proportional to the signal frequency. Some small diameter cables (1/8 inch) lose much of the high-frequency information of a fast-rise pulse in a very few feet of cable.

Losses of high frequency information can be shown with a fast rise pulse generator and sampling system. Using a 5-ns-delay RG-58A/U coaxial cable as a connecting cable, a display similar to Fig. 2-13A can be shown. Adding an additional 10 ns-delay RG-58A/U coaxial cable in the signal path results in a display similar to that of Fig. 2-13B. By using larger diameter, higher quality cable such as RG213/U in the same system, less loss is shown with the same length of connecting cable. Tektronix Type 113 Delay Cable is a high quality, low loss cable with 60 ns signal delay.

Attenuating the Input Signal

The maximum signal amplitude that should be applied to the input connector of the sampling head will depend upon the sampling head installed in the Type 3S2. To attenuate the signals to 50 Ω input sampling heads, use an attenuator probe and/or external coaxial attenuators. The attenuators must have good frequency response beyond the frequency response of the sampling head to avoid reducing system performance. High quality coaxial attenuators are available through your Tektronix Field Office or Representative with attenuation factors such as 10×, 5× and 2×. When the attenuators are stacked, their attenuation factors multiply; i.e., two 10× attenuators produce 100× attenuation. The 50 Ω attenuators must be matched to 50 Ω input and output impedances to provide their stated attenuation factor.

To divide a signal into two equal parts, and maintain a good 50 Ω impedance match, use a power divider such as GR 874 TPD Tektronix Part No. 017-0082-00. The loss between any two of the power divider connectors is 6 dB (half voltage) when each connector has a 50 Ω circuit connected.

Passive Probes. The Tektronix P6034 10× Probe and the P6035 100× Probe are moderate-resistance passive probes designed for use with 50-ohm systems. They are small in size permitting measurements to be made in miniaturized circuitry. Power rating is 0.5 watt up to a frequency of 500 MHz. Momentary voltage peaks up to 500 volts can be permitted at low frequencies, but voltage derating is required at higher frequencies. Characteristic data is given in the probe instruction manuals.

The P6034 10× Probe places 500 ohms resistance and less than 0.8 pF capacitance in parallel with the signal source at low frequencies. The probe bandwidth is DC to approximately 3.5 GHz, and risetime is 100 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 300 ohms and the capacitive reactance is about 400 ohms.

The P6035 100× Probe places 5 kΩ resistance and less than 0.7 pF capacitance in parallel with the signal source at low frequencies. Bandwidth of the probe is DC to approximately 1.5 GHz, and risetime is 200 picoseconds or less (10% to 90%). At 1 GHz the input resistance is about 2 kΩ and the capacitive reactance is about 450 ohms.

Built-in Probes. Another satisfactory method of coupling fractional nanosecond signals from within a circuit is to design the circuit with a built-in 50-ohm output terminal. With this built-in probe, the circuit can be monitored without being disturbed. When the circuit is not being tested, a 50-ohm terminating resistor can be substituted for the test cable. If it is not convenient to build in a permanent 50-ohm test point, an external coupling circuit, which may be considered a probe, can be attached to the circuit.

Several factors must be considered when constructing such a built-in signal probe. A probe is designed to transfer en-

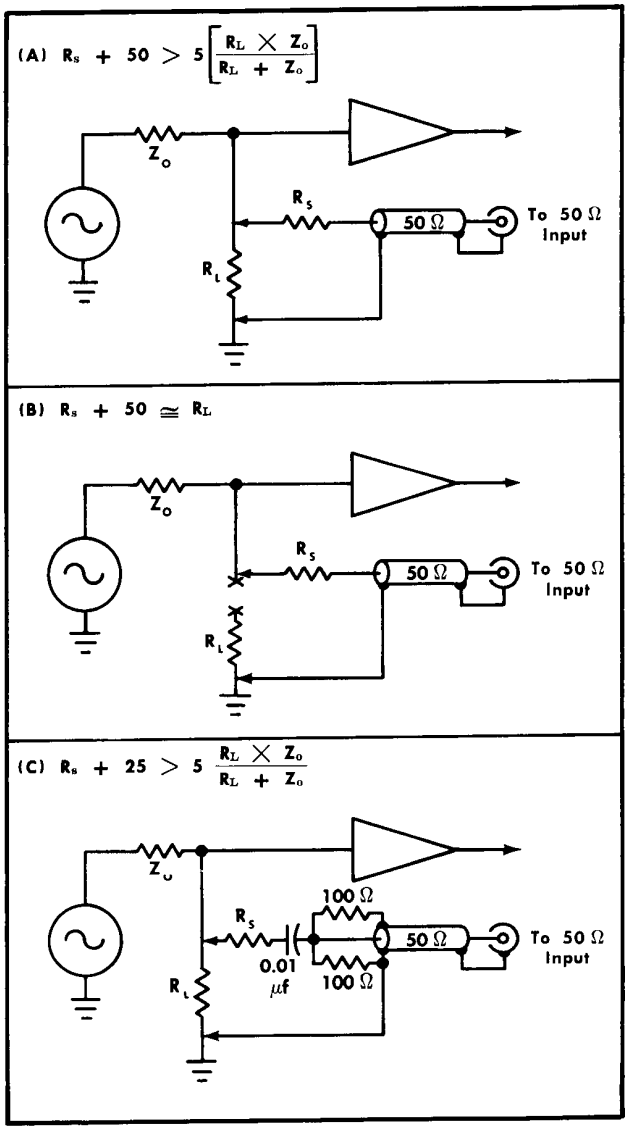


Fig. 2-14. Built-in probes for coupling to a test circuit. (A) Parallel method; (B) series method; (C) reverse-terminated parallel method.

ergy from a source to a load, with controlled fidelity and attenuation. Both internal and external characteristics affect its operation. It must be able to carry a given energy level, be mechanically adaptable to the measured circuit, and be equally responsive to all frequencies within the limits of the system. The probe must not load the circuit significantly or the display may not present a true representation of the circuit operation. Loading may even disrupt the operation of the circuit. When it is necessary to AC-couple the probe, the capacitor should be placed between the series attenuator resistance and the 50-ohm probe cable to minimize differences between the input characteristics with and without the capacitor. In a 50-ohm environment, stray capacitance to ground has a shorter and more uniform time constant than if the capacitor were placed at the signal source where the impedance is usually higher and sometimes of unknown value.

Fig. 2-14A shows the parallel method of coupling to a circuit under test. Resistor R_s is connected in series with the 50-ohm input cable to the sampling unit, placing R_s +50 ohms across the impedance in the circuit. This method usually requires the use of an amplitude correction factor. In order to avoid overloading the circuit, the total resistance of R_s + 50 ohms should not be less than 5 times the impedance of the device (R_L in parallel with Z_O) requiring a 20% correction. The physical position of R_s will affect the fidelity of the coupling.

Fig. 2-14B shows the series method of coupling to a circuit. Resistor R_s plus the 50 ohm Sampling Head input resistance replaces the impedance of the circuit under test. If R_L is 50 ohms, simply substitute the 50-ohm test cable without R_s. It is best to locate R_s in the original position of R_L and to ground the coaxial cable where R_L was grounded.

A variation of the parallel method is the reverse-terminated network shown in Fig. 2-14C. This system may be used across any impedance up to about 200 ohms. At higher source impedances, circuit loading would require more than 20% correction. The two 100-ohm resistors across the cable input serve to reverse-terminate any small reflections due to connectors, attenuators, etc. The series capacitor, which is optional, blocks any DC component and protects the resistors.

NOTES

SECTION 3
TEKTRONIX BASIC SAMPLING PRINCIPLES

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section provides a basic functional description of the vertical channels of sampling oscilloscopes. A discussion of equivalent-time sampling process is included. Operating instructions, including first time operation, are given in Section 2.

BASIC SAMPLING TECHNIQUES

The current state of the electronics art does not permit the direct cathode-ray tube display of fractional-nanosecond risetime low-level signals. Risetimes in the order of 0.35 ns can be displayed on a CRT if the signal is at least several volts in amplitude.

An inherent limitation in linear amplifiers is the compromise necessary between bandpass and gain. A high gain amplifier is a low bandpass amplifier; and conversely, wide-band amplifiers are necessarily low gain amplifiers. For any particular configuration, gain times bandpass is nearly a constant, so anything done to increase the gain will proportionately reduce the bandpass and vice versa. The gain-bandpass product limitation of linear amplifiers restricts the display of millivolt signals on a CRT to the 50 to 200 MHz region.

The sampling technique permits the quantitative display (on a CRT) of a facsimile of fractional-nanosecond risetime low-level signals. In sampling, many cycles of an input signal are translated into one cycle of low-frequency information. The change takes place at the input, or sampling bridge. Since only the sampling bridge is subjected to the input signal high frequencies, and all the amplification takes place at relatively low frequencies, the performance of a sampling system is not dependent on the gain-bandpass limitations of conventional amplifiers.

However, the sampling technique introduces some limitations of its own. The sampling process being described is restricted to repetitive signals of low amplitude (typically 1 or 2 volts peak to peak), from low impedance sources. Fortunately, most fractional-nanosecond risetime signals exist in low impedance environments and are generally low amplitude. Piping the signal from the circuit under test to the input of the sampling oscilloscope vertical channel requires a more sophisticated technique than lower bandpass systems. In spite of its limitations, sampling can measure fast signals that otherwise defy observation.

A sampling system looks at the instantaneous amplitude of a signal during a specific small time period, remembers the amplitude, and displays a single dot on the CRT corresponding to the amplitude. After a dot is displayed for a fixed amount of time, the system again looks at the instantaneous amplitude of a different cycle of the input signal. Each successive look, or sample, is at a slightly later time in relation to a fixed point of each signal cycle. Each sample is displayed as a spot on the CRT. Generally the vertical position of the dot represents the equivalent time when the sample was taken. After many cycles of the input signal, the sampling system has reconstructed and displayed a single facsimile made up of many samples, each sample taken from a different cycle of the input signal.

Fig. 3-1 illustrates the equivalent time reconstruction of a repetitive square wave. The CRT display is a series of dots rather than the conventional oscilloscope continuous presentation. In the illustration, a series of samples is taken of the input signal. After each sample, when memory has been established and stabilized, the CRT is unblanked and a dot appears. A large number of such dots form the display.

The number of dots per horizontal unit of display is called dot density. The dot density of a display is controlled by the operator to provide the best compromise between resolution and repetition rate of the display. Since only one sample is taken from any particular input cycle, the time required to reconstruct a display is a function of the dot density selected and the repetition rate of the signal. The higher the dot density selected (for higher resolution), the longer the time required to construct the equivalent time display. The higher the repetition rate of the signal, the less time required to reconstruct the waveform (limited by a maximum repetition rate of the system).

Sampling requires repetitive input signals, although not necessarily signals with constant repetition rate. The equivalent time between dots is determined by the time delay between the fixed point on the signal at which triggering occurs, and the point at which the sample is taken. Since both time references (triggering-time and sample-time) are taken from the same cycle of the signal, the signal repetitions do not have to be identical in amplitude, time duration, and shape. Any differences in the individual cycles show as noise or jitter in the reconstructed display.

Sampling systems have maximum signal repetition rates at which samples can be taken and accurately displayed. The primary limit is the time required for the preamp and the AC amplifier to stabilize after a sample has been taken.

Signals below 100 kHz may have considerable repetition rate jitter and still the sampling oscilloscope will present a sample of each cycle, without display jitter. For signals with a repetition rate higher than 100 kHz, the timing unit holds off retriggering for a maximum of about 10 μs. This means that a sample will not be taken from every cycle of a high repetition rate signal. Only those cycles are sampled which occur after the end of the holdoff. If the signal is

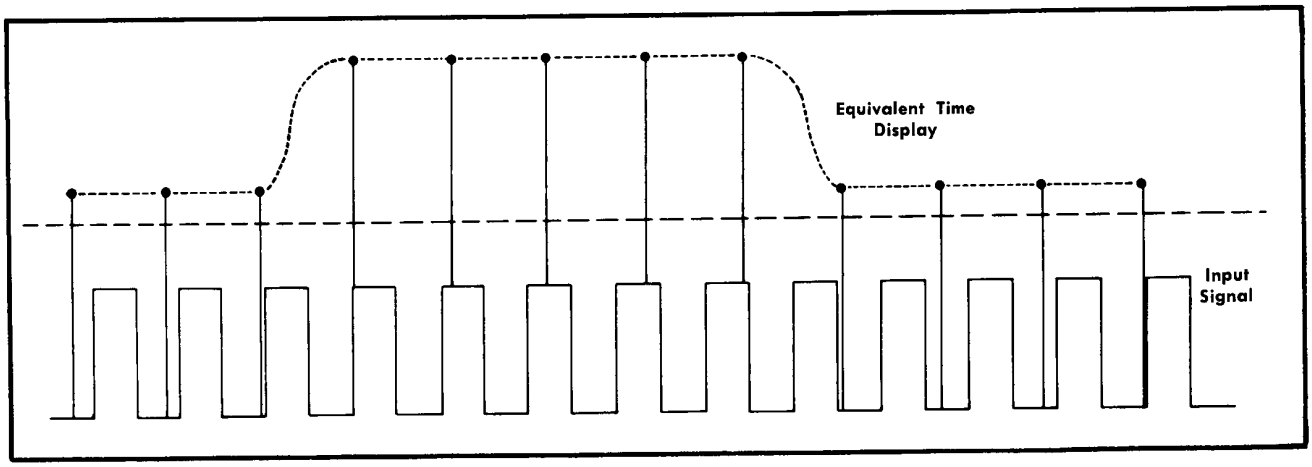


Fig. 3-1. Equivalent time display of repetitive real time signal by means of the sampling technique.

truly repetitive and each cycle is identical, these "missed" cycles are of little significance.

The circuits in the vertical channel of a Tektronix sampling oscilloscope comprise an error-sampled feedback system with ratchet memory. The memory output is not reset to zero after displaying a dot. The memory output remains at the displayed amplitude of each dot in succession until it is corrected by the next sample. The amplitude difference between the two samples is then the error between the memory output and the new sampled amplitude.

Fig. 3-2 shows a simplified block diagram of an error-sampled feedback system with ratchet memory. The output signal from the sampling bridge is the difference, or error, between the instantaneous amplitude of the signal at sample time and the previously memorized amplitude. A change is made to the memory output only when the instantaneous amplitude of the signal at sample time is different from the memory output. The memory output "ratchets" up or down at sample time as a result of the error signal sampled. The transition of memory from one output voltage to another occurs between displayed dots, and is therefore not seen on the CRT.

The error-sampled ratchet-memory technique has the advantage of allowing display noise to be "smoothed". Smoothing is discussed later in this section. The error-sampled approach also minimizes signal kickout into the input cable by the sampling bridge interrogate pulse (hereafter called "strobe" pulse). Since the sample is always the difference between the signal and the memory output, the error signal and kickout are much smaller in amplitude than they would

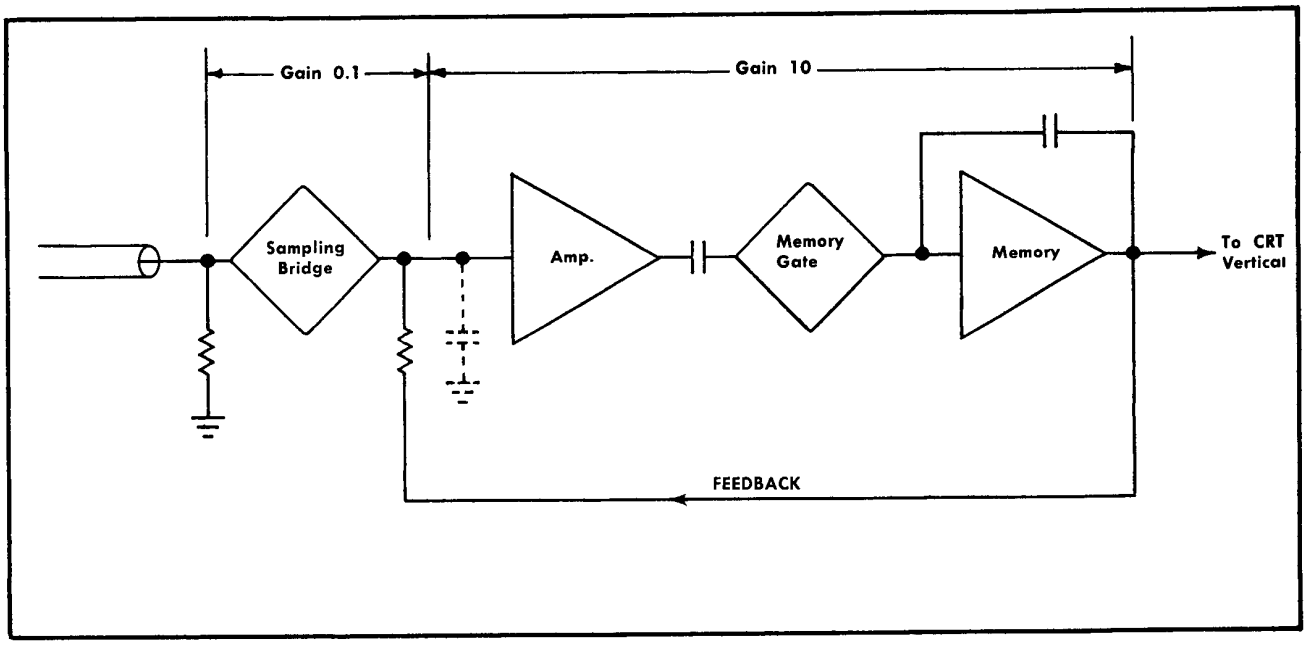


Fig. 3-2. Simplified block diagram of an error-sampled feedback system with a ratchet memory.

be if the memory output reverted to zero and the entire signal was sampled after each dot.

The output from the sampling bridge at sampling time is about 2% of the difference between the signal voltage and the memory output. The 2% signal is the input to the first amplifier. The output of the amplifier is AC-coupled to a memory gate. The memory gate couples the signal to the memory amplifier during the time it is gated on. The memory amplifier changes the memory feedback voltage to equal the signal voltage at the instant of sampling. These changes in memory output occur while the CRT is blanked, and do not show up in the display. The memory output does not revert to zero, but remains at a fixed voltage until corrected by the next error signal. (The signal to the amplifier of a typical sampling system is only about 2% of the error signal sampled by the bridge. The percentage of response, or attenuation through the sampling bridge, is the sampling efficiency.)

At each sample time, the difference between the memory feedback and the 2% signal value is amplified and applied to the memory circuit via the memory gate, to correct the memory output to follow a rising signal in a series of steps as shown in Fig. 3-3. This figure shows the input signal and memory feedback voltages for six samples along the rise of a step waveform.

At the time of sample 1, the input signal and the feedback voltage are equal. There is no error voltage, so the memory output is not changed. The CRT is blanked until the circuit stabilizes after the memory gate pulse ends.

At the time of sample 2, the input signal is (for example) 0.1 volt. The memory output is 0. Assuming a sampling efficiency of 10%, the input of the amplifier receives 10% of the error signal, or 0.01 volt. The 0.01 volt, times the gain of the amplifiers (×10), corrects the memory output and feedback to equal the 0.1 volt signal at sample time. Again, the CRT is blanked during this change until the circuit is stabilized.

At the time of sample 3, the difference between the input signal and the feedback is 0.35 volt. The amplifier input responds to 10% or 0.035 volt. The gain of the amplifier and memory changes the feedback 0.35 volt to the new value of

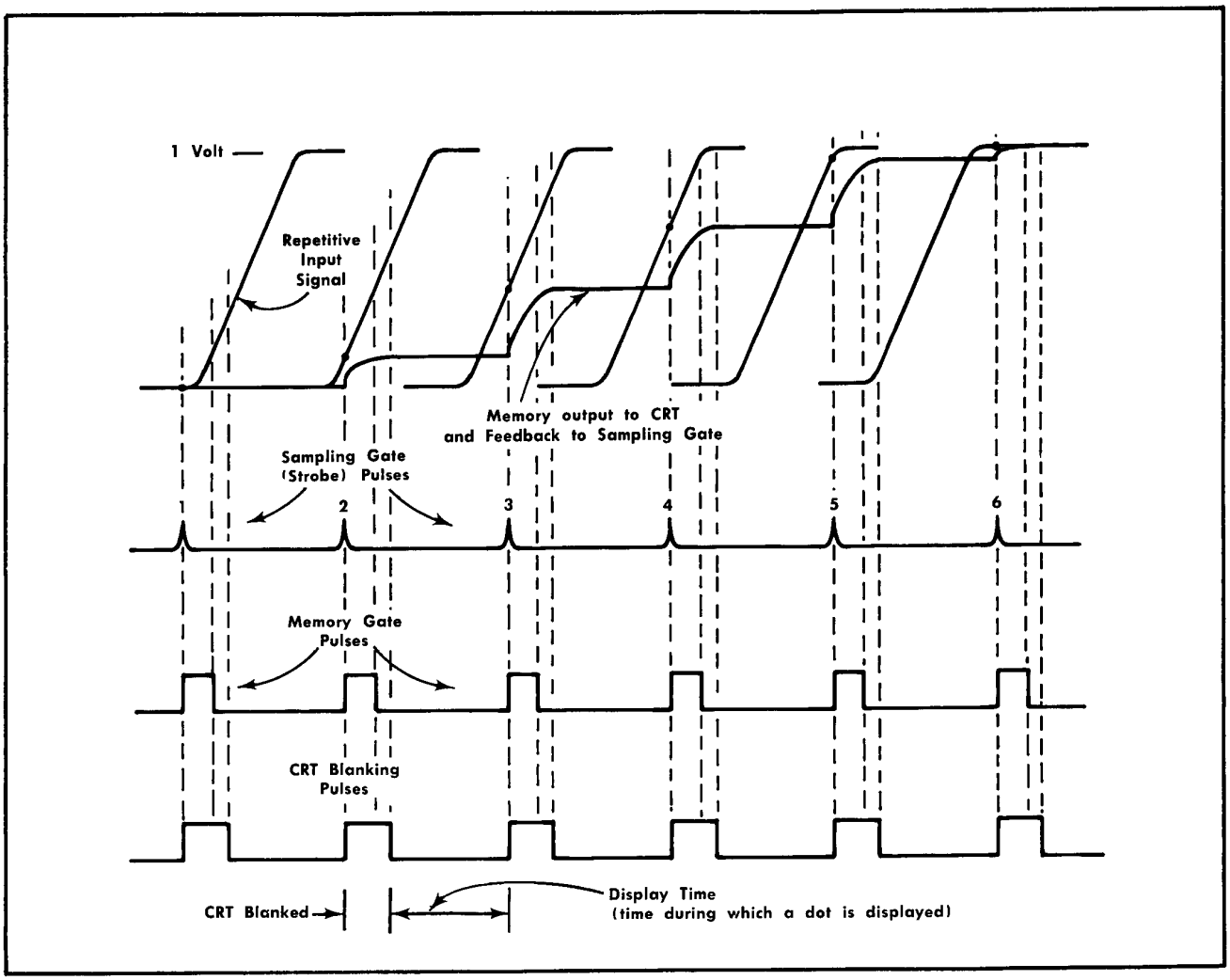


Fig. 3-3. Simplified representation of an error-sampled ratchet-memory waveform.

0.45 volt (equal to the signal at number three sampling time). The CRT is again blanked during this change until the circuit is stabilized.

This process continues until sample 7 (not shown). Here again, there is no difference between the input signal and the feedback. There is no error signal, and the memory output and feedback is not changed. The system will remain at this voltage until the input changes, or until system drift has caused an error in the memory output (if there is a long period of time between successive samples).

Effective Sampling Time

The minimum risetime a sampling system can display is controlled by the time interval during which the strobe pulse applies forward bias to the sampling bridge diodes. The duration of the bridge forward bias is controlled by the time the strobe pulse exceeds a fixed reverse bias. Special circuitry is used to make the strobe duration as short as possible consistent with noise and diode recovery time. The strobe pulse is generated by a snap-off diode and a short section of shorted transmission line called a clipping line. The effective bridge conduction time is adjusted primarily by controlling the amplitude and duration of the strobe pulse, thus controlling the time during which the strobe pulse exceeds the reverse bias. Adjusting the reverse bias is a secondary means of controlling the sampling bridge conduction time. Fig. 3-4 shows how the strobe pulse breaks through the reverse bias on the sampling bridge. The reverse bias is shown by dashed lines through the strobe pulses.

Dot Response (Loop Gain)

Dot response is a visual display of the system's ability to reduce the error voltage to zero after each sample. When the gain of the memory feedback loop is equal to (and compensates for) the attenuation across the sampling bridge, the loop gain is unity or 1. In this case, the memory feedback voltage equals the value of the signal voltage at sampling time.

If the dot response is less than unity, the memory output signal and feedback to the first amplifier is less than necessary to reduce the error voltage to zero. The memory output and the feedback will then approach the signal asymptotically after several samples have been taken. The

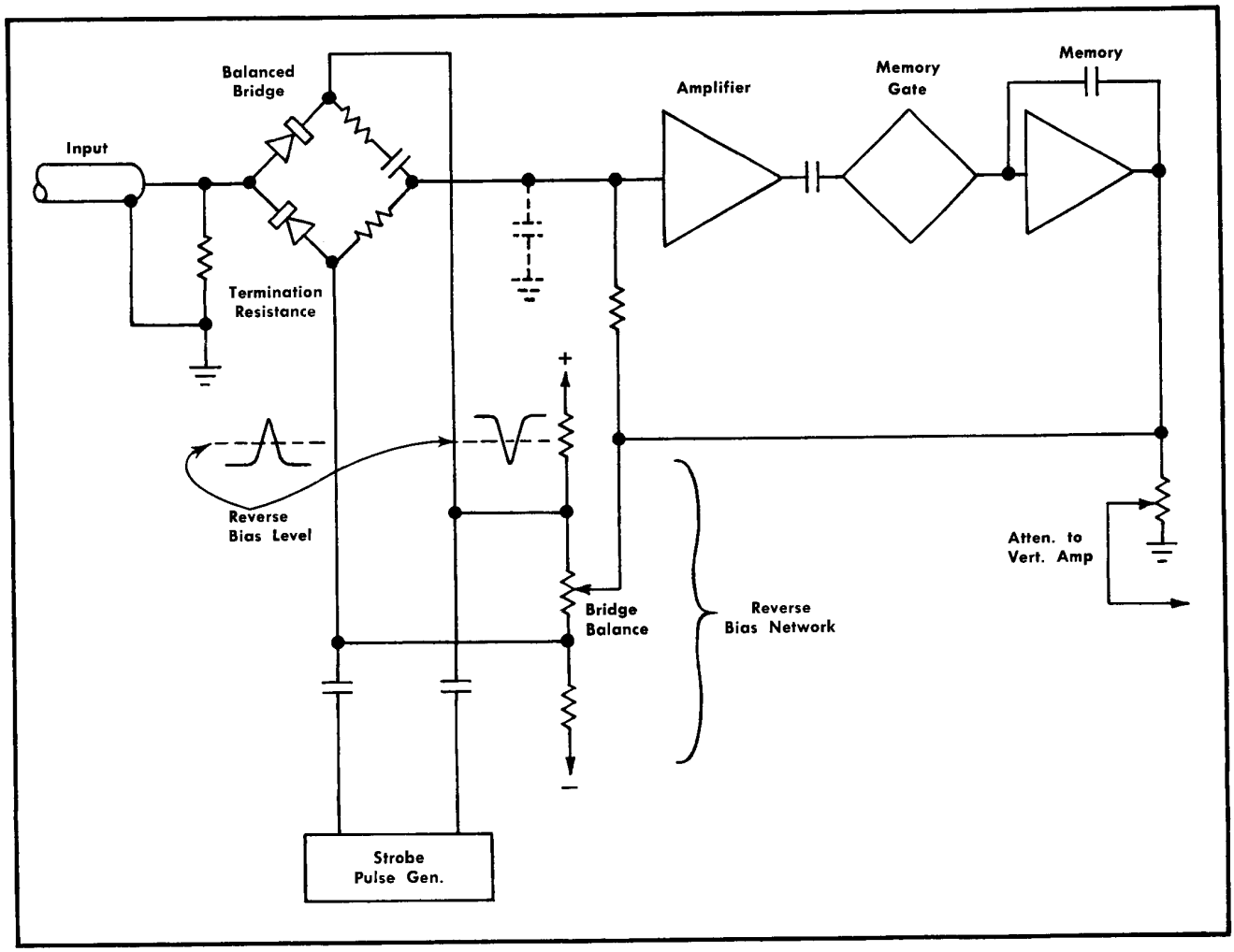


Fig. 3-4. Simplified diagram, showing how the strobe pulse causes the sampling bridge to conduct.

error voltage thus approaches zero (for a steady state signal) after several samples, being reduced by the same factor after each sample. In the case of a loop gain of less than unity, the feedback voltage is effectively a moving average of several preceding samples.

If the loop gain is greater than unity, the feedback voltage will be greater than the error signal after each sample. The displayed dot sequence of a step signal will then alternately overshoot and undershoot for a few samples.

For least displayed waveform distortion the loop gain must be unity, allowing the system to track the input signal as closely as possible.

Smoothing

A loop gain of less than unity can be useful, if the resulting compromise is understood and the system is operated properly. Random noise in the display is reduced when loop gain is less than unity, since several consecutive samples are averaged. The averaging may also slow down the fastest display risetime capability, depending upon the number of dots contained in the step transition and/or the loop gain. By increasing the number of dots in a step transition, the display will follow the actual step transition more closely.

Fig. 3-5 shows the usual effects on a step display when smoothing is used for two different sampling densities (sampling density or dot density is the number of samples or dots per horizontal division). In the Type 3S2 the operational choice of loop gain is either 1.0 (NORMAL) or 0.3 (SMOOTH). In Fig. 3-5A the actual risetime (between the 10% and 90% points) for unity loop gain displays 4 dots. When operating at 0.3 loop gain , 7 dots are shown. There is a significant difference between the 0.3 loop gain (SMOOTH) and the unity loop gain (NORMAL) displays.

In Fig. 3-5B the sampling density is increased, showing a difference of one sample in the SMOOTH and NORMAL positions between the 10% and 90% points of this step transition.

When the smoothed mode has a loop gain of 0.3, as in the Type 3S2, 15 or more samples between the 10% and 90% points of a risetime will result in the smoothed and unsmoothed displays having essentially the same risetime. When the smoothed display contains 12 samples between the 10% and 90% points, the smoothed risetime will be about 6% longer than for the unsmoothed display. As the number of samples contained in the risetime is reduced below 12, the difference between smoothed and unsmoothed display goes up rapidly.

Smoothing of Random Noise

When the loop gain is reduced to 0.3, the displayed dots represent the average of several consecutive samples. Noise of a random nature will be materially reduced in the display at the possible expense of introducing an error in the displayed risetime. Therefore, if random noise is apparent, reducing the loop gain may improve the display. Note that this is only true for random noise. Systematic noise (noise with its repetition rate harmonically related to the signal) is treated as part of the signal.

The Type 3S2 has a loop gain control labeled NORMAL-SMOOTH. In the SMOOTH mode, loop gain is reduced to 0.3. Always check that there is sufficient sampling density to warrant smoothing. This can be done by changing the dots/division (or samples/division) control on the timing unit and observing the effect of sampling density on the displayed risetime.

Smoothing cannot be applied where the full amplitude of each sample is required. When using the random sampling process of a sampling sweep unit like the Type 3T2, each sample requires unity loop gain. The display dots are not presented in time sequence, and therefore cannot be averaged.

Tangential Noise

Traditionally the amplitude of random noise in an amplifier is qualified by stating the equivalent RMS value of the noise referred to the input of the amplifier. In the case of a CRT sampling display, qualifying the noise amplitude by stating its RMS value is somewhat unsatisfactory. The visible effect of the random noise is more nearly 3 times the RMS value of the noise. Peak-to-peak limits of truly random noise would have to be stated as — infinity to + infinity. Obviously these broad limits would reveal nothing about the amount of significant noise to expect in a display. It has been determined empirically that 90% of the dispersion caused by random noise closely approximates the visible widening of the trace. The noise can be described as existing between two horizontal tangents representing the significant upper and lower limits of the trace width. Hence, the term TANGENTIAL NOISE. Tangential noise is defined as an equivalent peak-to-peak voltage at the input of a sampling system that will cause the same trace widening as 90% of the random noise. 5% of the dots can be expected to fall above the trace width and 5% below it. This method of stating the noise figure of a sampling system is considered to be more meaningful than the RMS value, in that it more closely approximates the actual observed trace widening. Measurement of Tangential Noise is described in Section 6.

Display Sensitivity—Deflection Factor

The two terms display sensitivity and deflection factor are often mistakenly interchanged. Deflection factor is defined as the ratio of the input signal amplitude to the resultant displacement of the indicating spot. When the oscilloscope vertical gain control is calibrated in volts per division, it is indicating deflection factor. Deflection sensitivity is the reciprocal of deflection factor. Sensitivity is indicated by a vertical gain control calibrated in divisions per volt.

There is always some point within the oscilloscope vertical amplifier after which the signal remains at a fixed deflection factor. The signal out of the vertical memory amplifier of a sampling oscilloscope is usually the first point at which the standard vertical deflection signal exists. Thus, the memory and feedback voltages previously mentioned always deflect the CRT spot vertically with a fixed deflection factor.

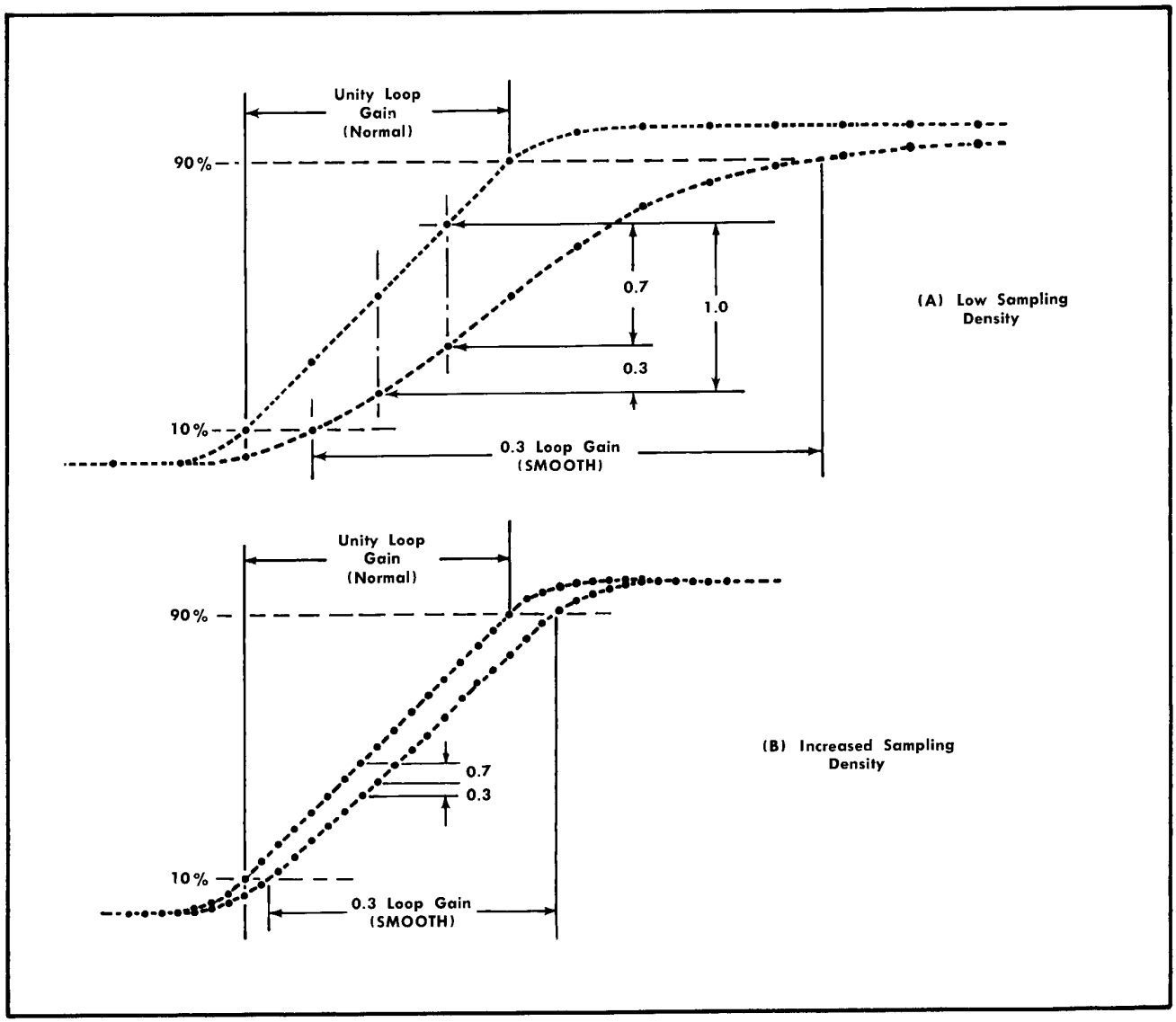


Fig. 3-5. Equivalent-time display with and without smoothing for two different sampling densities.

Fig. 3-6A shows a simplified block diagram of a bridge and amplifier combination where the gain of the amplifier just compensates for the attenuation of the sampling bridge. In Fig. 3-6B the amplifier has twice as much gain as is necessary to compensate for the low sampling efficiency. By introducing a 2:1 attenuator in the feedback path between the memory output and the bridge output, the loop gain is still maintained at unity. Now, only half as much input signal produces the same memory output as in Fig. 3-6A.

Fig. 3-6 shows two fixed attenuators in each sample. The usual method of changing amplifier and memory gain in a sampling unit is to attenuate the signal through (or to) it. The attenuator in series with the amplifier and memory is called the forward attenuator, in contrast to the feedback attenuator.

The attenuators in Fig. 3-6 and Fig. 3-7 show that both the "forward gain" and the "feedback attenuation" are altered when changing a sampling system vertical deflection factor.

The system deflection factor can be altered two ways: 1) by changing both the forward and the feedback attenuation and thereby maintaining the same loop gain, and 2) by changing only the feedback attenuation, at the expense of varying the loop gain. If loop gain is not greater than unity, and many samples are included in a signal transition, the memory feedback to the sampling bridge always approaches the signal amplitude regardless of the forward attenuator attenuation ratio.

Since loop gain is determined by the combined forward and feedback attenuation ratios, the displayed dot response can be altered without altering the deflection factor by changing the forward attenuation only. Increasing the forward attenuation ratio (decreasing the amplifier and memory gain) "smooths" the display by making the loop gain less than unity.

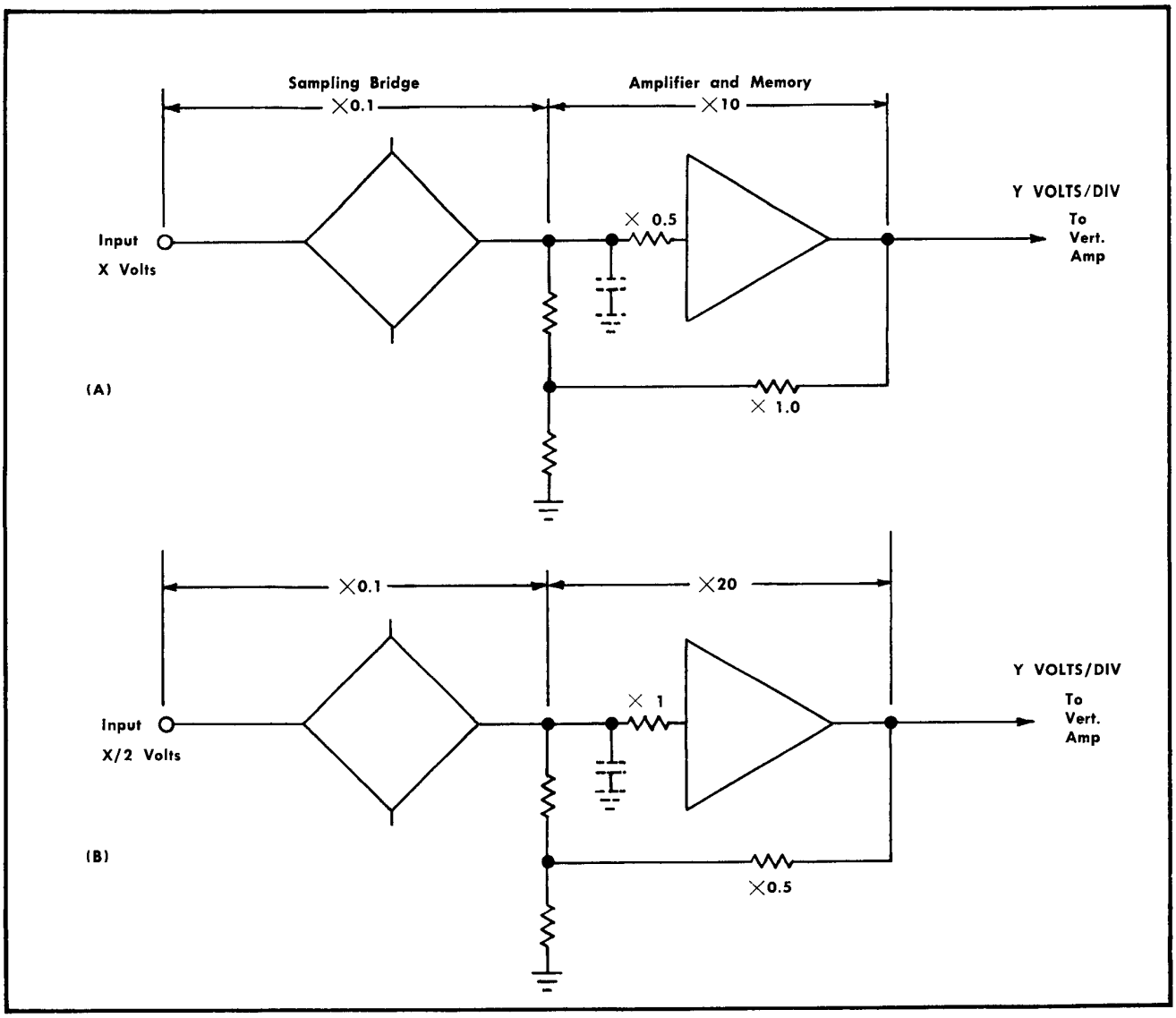


Fig. 3-6. Method of decreasing the vertical deflection factor while maintaining unity loop gain.

DC Offset

Since the sampling bridge can operate over a range of +2 to —2 volts of input signal, and the system has resolution capability of 2 mV/div, it is advantageous to be able to display a small vertical "window" of the input signal. Fig. 3-7 shows the method of adding a DC offset voltage to the memory feedback. The error signal produced at sampling time is no longer referenced to ground. Instead, it is referenced to the DC offset voltage.

A DC Offset voltage is recognized as a signal by the sampling bridge, algebraically adding it to the error signal. Therefore, the memory feedback signal in a system with DC Offset includes a DC value to cancel the DC Offset voltage at the output side of the sampling bridge. The deflection factor of a system with DC Offset is centered around the DC Offset voltage instead of ground. This permits portions of the signal (other than ground) to be positioned to the CRT center, without altering the deflection factor.

Real-Time Sampling

Real-time sampling is a method of operation in which the samples are taken at a constant rate from relatively low frequency signals (DC to 20 kHz approximately) and displayed at a sweep rate determined by the Time/div switch on the real-time time-base. Thus, the samples are taken continually along the input signal rather than one sample from each repetition of the signal. The displayed series of dots follows the actual shape of the input signal waveform.

In real-time sampling operation, the vertical signal provides the trigger to start the sweep. The display, however,

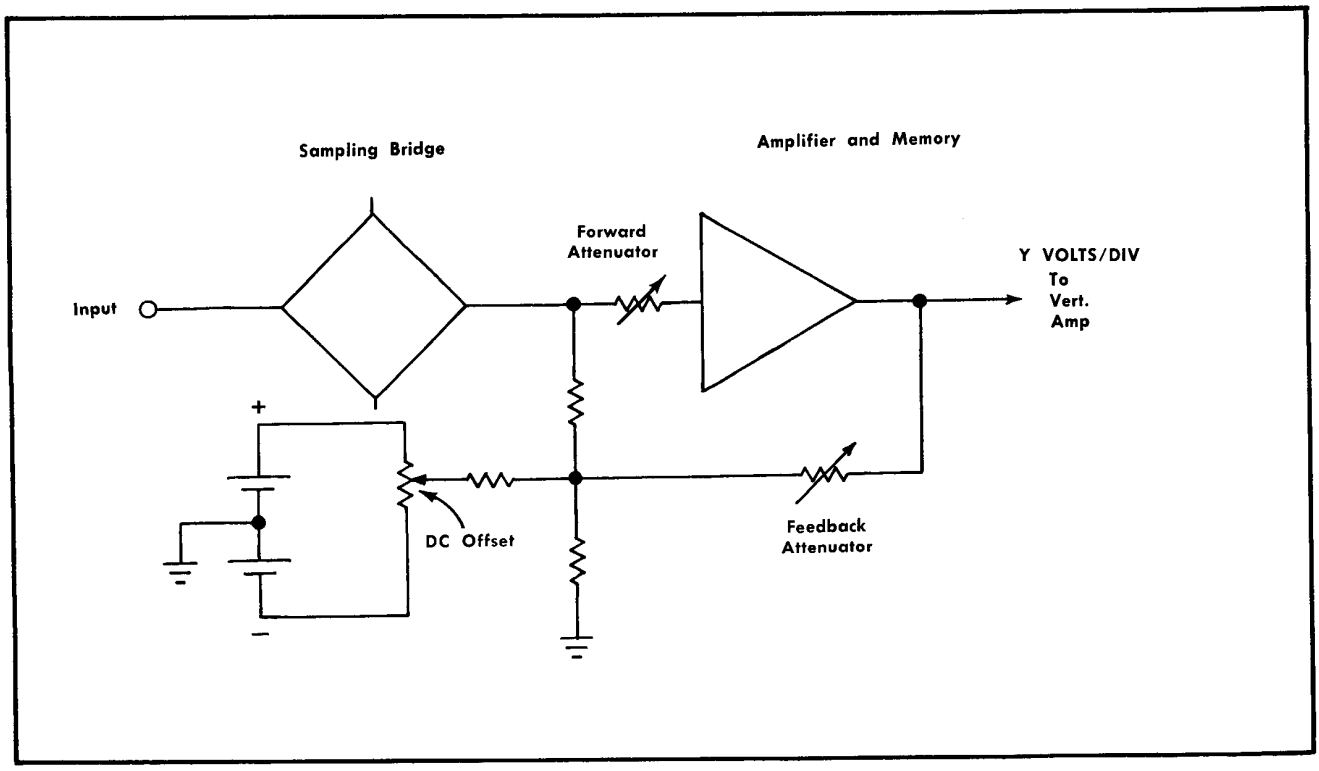


Fig. 3-7. Method of adding a DC Offset voltage to the memory feedback.

is composed of samples at a fixed repetition rate, not necessary related to the input frequency.

Sweep Rates

The range of sweep rates available for use in real-time sampling is from the slowest rate provided by the real-time sweep plug-in to about 0.1 ms/div. At this sweep rate, the usual 100 kHz sampling rate provides about 100 samples/sweep. At faster sweep rates above 0.1 ms/div, the display dots begin to have significant horizontal dimension due to their duration in real time, and interpretation of the display becomes difficult.

The characteristics of real-time sampling, in addition to slow sweeps at full bandwidth, are reduction of random noise in the display through smoothing, and DC offset capability matched with good overload recovery.

SECTION 4
CIRCUIT DESCRIPTION

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains a block diagram description and circuit description of the Type 3S2 Sampling Unit. The block diagram description is an expansion of Section 3, Basic Sampling Principles. The circuit description follows the sequence of diagrams at the back of this manual.

BLOCK DIAGRAM

Refer to Fig. 4-1 and the complete block diagram at the back of this manual during the following description. Since most of Channel A and Channel B are identical, no reference is made to either channel except where they differ. Channel A occupies the top half of the block diagram.

Both Fig. 4-1 and the complete block diagram include a simplified block of a typical sampling head. The Type 3S2 Sampling Unit serves no useful purpose by itself, but functions as part of a sampling system only when a sampling head is installed. Thus, the sampling head simplified blocks are included.

Feedback Loop and Pulse Amplifier Chain

Fig. 4-1 relates to Fig. 3-4 and Fig. 3-7. The reconstructed signal out of the Memory block (Fig. 4-1) is the first point in the Type 3S2 at which the amplitude is always a standard value of 0.5 volt per CRT vertical division. The signal between the sampling head output (TP121) and the Memory input bears no similarity to the signal at the Memory output. Under ideal conditions, there is no signal between those two points whenever the sampling head input signal is at a steady value. The Post Amplifier, AC Amplifier and Memory Gate all are part of a pulse amplifier chain that amplifies the sampling head output signal just after each sample is taken. The pulse chain signals are greatest in amplitude when the sampled signal is at its full amplitude difference from the last sample (as in using the random sampling process in the Type 3T2 Random Sampling Sweep unit).

To complete the association of Fig. 4-1 with Section 3, the following describes the operating cycle:

a. The sampling head bridge applies an error signal to the head preamp whenever there is a voltage difference at the bridge input and output terminals at sampling time. The error-signal voltage amplitude is just a few per cent of the difference (sampling efficiency), and the pulse duration out of the bridge is equal to the bridge conduction time. A small storage capacitance at the head Preamp input time-stretches the pulse so the pulse chain can amplify the error signal pulses at moderate rates of rise.

b. The time-stretched pulse is amplified by the Type 3S2 Post Amplifier and sent forward into the attenuating network made up of the NORMAL-SMOOTH switch, the DOT RESPONSE control and the Forward Attenuator portion of the Units/Div switch.

c. The AC Amplifier again amplifies the pulse and applies it to the Memory circuit during conduction time of the Memory Gate. In effect, the error signal charge applied to the head Preamp is then transferred to the feedback capacitor of the Memory circuit.

d. The Memory circuit applies its error signal-determined output voltage to both the vertical amplifier and to the feedback attenuator and sampling head bridge output terminal. Control of the input deflection factor by the Forward and Feedback Attenuators is described near the end of Section 3. The DOT RESPONSE control is also described in Section 3.

Vertical Channel Following Memory

Blocks between the Memory and the CRT include: the Inverter and the INVERT switch, the Units/Div VARIABLE control and internal Digital Gain control, the Channel Amplifier and the Output Amplifier with its input controlled by the Dual-Trace Multi. The Output Amplifier drives the indicator oscilloscope CRT vertical deflection plates directly.

The Inverter is a $\times 1$ gain inverting amplifier that is normally in the circuit. The inverter is by-passed when the INVERT switch is pulled out to invert the display.

The Channel Amplifier is a $\times 2$ gain inverting amplifier with both the Units/Div VARIABLE and Digital Gain controls in series with the signal input. The Channel Amplifier drives both the Output Amplifier and the real-time time-base unit. The signal to the real-time time-base unit is for internal triggering of a real-time sampling display.

Channel B Channel Amplifier drives the same output line to the sampling sweep unit during A VERT-B HORIZ operation. The signal then drives the horizontal deflection plate amplifier in the sampling sweep unit.

Both of the above functions require that the Horiz Plug-In Compatibility switch be placed at the correct position. See the Operating Instructions.

The Output Amplifier is a high gain inverting amplifier that drives the CRT vertical deflection plates directly. The input is from either Channel A or Channel B, selected by the Dual-Trace Multi. The multi control circuit selects one channel continuously (CH A or CH B), alternates between channels after each sample (DUAL-TRACE), or parallels the two channels and adds their signals algebraically at the summing input circuit.

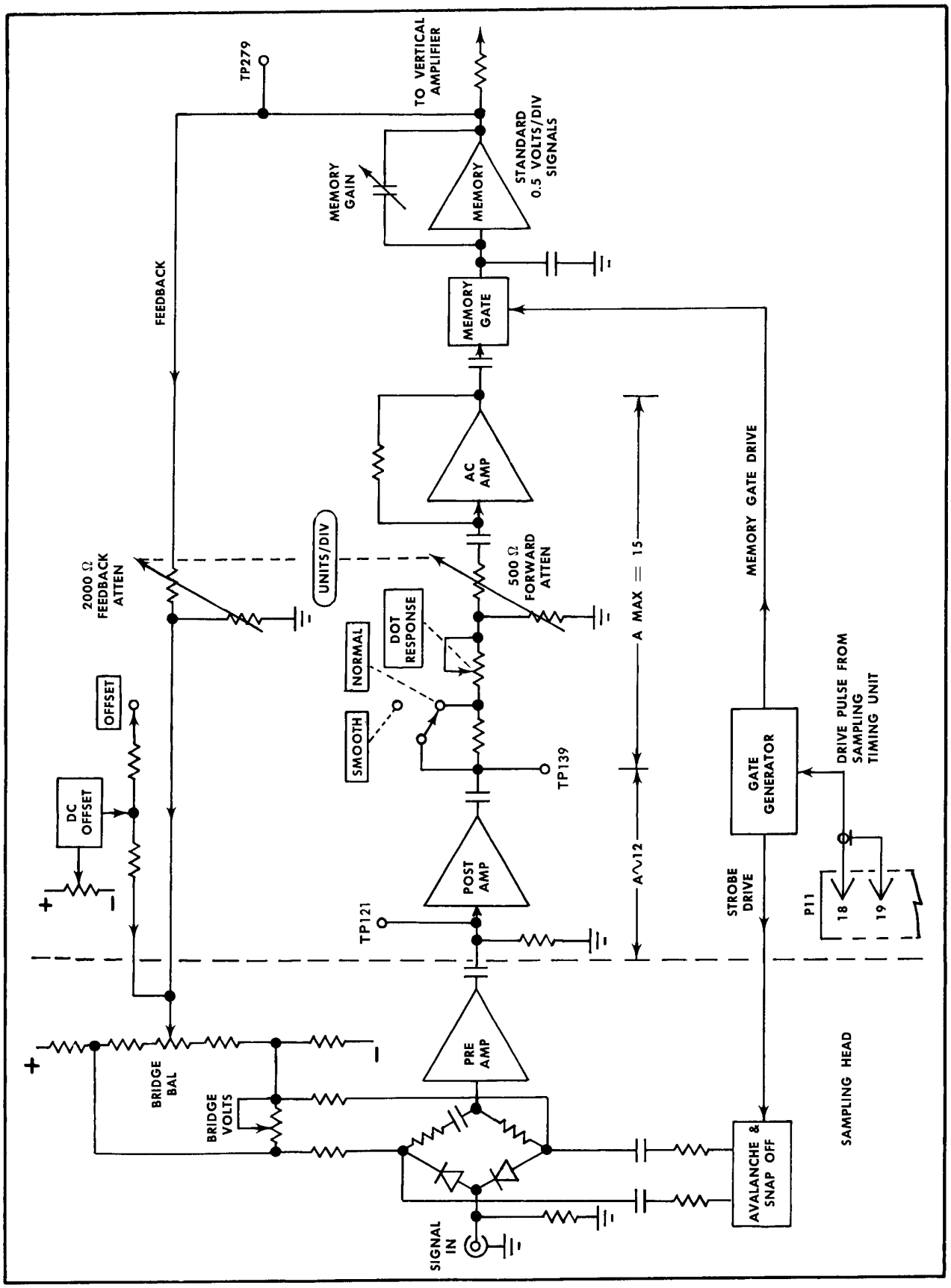


Fig. 4-1. Type 3S2 and sampling head feedback loop block diagram.

The Position Lamp Driver circuit monitors the DC voltage of the Output Amplifier lines and turns on the appropriate neon lamp to indicate whether the deflection voltage has placed the trace above or below the graticule.

Gate Generators

The Type 3S2 Gate Generator blocks function in two different modes: driven by the associated 3T-series sampling sweep unit, or self excited at a 100 kHz rate when the assocated time base is of the 2B- or 3B-series. The function is selected by the internally mounted Horiz Plug-In Compatibility switch, SW6. When SW6 is at the Sampling position, the sampling sweep unit drives the Blocking Oscillator, which then drives the Dual-Trace Driver and both Delay & Strobe Driver blocks. When SW6 is at the Non-Sampling position, the Dual-Trace Driver oscillates and drives the Blocking Oscillator, which again drives both Delay & Strobe Driver blocks.

Sampling; 3T-Series Operation

Since the Type 3S2 will operate with several different sampling sweep units, the Gate Generator is designed to operate from slightly different Sampling Drive pulses. The Blocking Oscillator converts the normal variations in amplitude, risetime and duration of the Sampling Drive pulses to a standardized drive pulse with always the same amplitude, risetime and duration.

The Blocking Oscillator output pulse is converted to an RC ramp signal at both Delay circuits, and the (internal) A Delay and (front-panel) B Delay controls select a point along each ramp at which the Strobe Drive is generated. As the individual channel Strobe Drive is generated, the Memory Gate Driver causes the same channel Memory Gate to conduct. The duration of Memory Gate conduction is controlled by the Memory Gate Width control. Thus, a few nanoseconds after the arrival of a Sampling Drive pulse, a Strobe Drive pulse is sent to the sampling head, and the Memory Gate is driven into conduction. The instrument is calibrated so the B DELAY control alters the time of the Channel B Strobe Drive pulse approximately ± 5 ns with respect to the Channel A Strobe Drive pulse (when both sampling heads are the same type).

The Dual-Trace Driver circuit drives both the CRT blanking circuit (to extinguish the CRT beam while the dot is being moved between samples) and the Dual-Trace Multi. The Dual-Trace Multi mode of operation is not controlled by the Dual-Trace Driver, but by the Vertical Mode Switch, SW730A. If the Vertical Mode switch is at DUAL-TRACE, the Dual-Trace Driver causes the Dual-Trace Multi to change state at the time each sample is taken.

Non-Sampling; 2B, 3B-Series Operation

Non-Sampling real-time time-base units do not provide a Sampling Drive pulse to the Blocking Oscillator. Since the Type 3S2 will operate with linear sawtooth time base units, the Gate Generator must provide its own sampling Strobe Drive control.

The Dual Trace Driver is made to oscillate at 100 kHz and to drive the Blocking Oscillator, the CRT blanking circuit and the Dual-Trace Multi.

The remainder of the Gate Generator circuits function as when operating with a sampling sweep unit. The operational differences between the two types of time bases are explained in the Operating Instructions, Section 2.

Trigger Amplifier

SN B040250-Up. A trigger amplifier block shown at the left of the block diagram near the sampling heads, couples an amplified portion of the sampling head input signal to a front panel connector. The amplifier is not connected to any of the Type 3S2 sampling process circuits. The front panel TRIG OUT switch selects the head from which the trigger pickoff signal is sent to the front panel connector.

The same TRIG OUT switch selects the internal Channel Amplifier signal for internal triggering of real-time time-base units.

SN B010101-B030249. Trigger amplifiers in this serial number range deliver a signal approximately 0.1 times the sampling head input signal.

A trigger amplifier block shown at the left of the block diagram near the sampling heads, couples a portion of the sampling head input signal to a front panel connector. The amplifier is not connected to any of the Type 3S2 sampling process circuits. The front panel TRIG OUT switch selects the head from which the trigger pickoff signal is set to the front panel connector.

The same TRIG OUT switch selects the internal Channel Amplifier signal for internal triggering of real-time time base units.

CIRCUIT DESCRIPTION

The following circuit description sequence follows the order of the diagrams in section 9.

Post Amplifiers & Attenuators

The Post Amplifier and Attenuators diagram includes Post Amplifiers for both channels, as well as Forward and Feedback attenuators, DC Offset and the common Trigger Amplifier. Where the two channels are identical, the operation of only one is described. Differences between the channels are discussed in detail.

The Trigger Amplifier SN B040250-Up, consists of the front panel TRIG OUT switch and TRIG OUT connector, transistors Q103, Q104, Q113 and Q114, and associated components. Q103 and Q113 are connected as common-base, amplifiers, with only one conducting at a time. The TRIG OUT switch selects the conducting transistors, Q103 for Channel A or Q113 for Channel B.

The signal input at J101 and J111 from a sampling head trigger pickoff circuit is approximately 0.1 of the input signal to the sampling head. A total AC gain of about 10 in the trigger amplifier causes the TRIG OUT connector signal to be about equal in amplitude to the sampling head input signal, within the bandpass limitations of the amplifier and when loaded by 50 Ω. Total DC gain into 50 Ω is about 0.075, and into 1 MΩ it is about 1.

Assume the TRIG OUT switch is at A. Then all the current from the channel B sampling head tirgger pickoff circuit

and R113 passes through D113 and R115 to ground; Q113 is cut off because its base voltage is +1.7 V and its emitter voltage is +1.5 V, 0.2 volt reverse biased.

The signal entering at J101 is in phase with the sampling head input signal. Q103 does not invert the signal, but both Q103 and Q114 do invert it (total of two invertions), making the TRIG OUT signal in phase with the sampling head input signal. D103 is reverse biased because C106 charges to a positive value equal to the most positive signal value that enters J101, minus about 0.5 V drop across D103. C106 charge has no leakage path, thus D103 reverse bias effectively disconnects R105, C106 and the lead to the TRIG OUT switch from the trigger amplifier input.

R101 raises Q103 emitter input resistance to provide a nominal 50 Ω termination to the coaxial cable feed line from the sampling head. Q103 collector circuit is DC coupled to Q104 base, with the main current path through R104, L104 and D104 which is bypassed by C104. D104 serves to temperature compensate Q104 so its collector DC voltage does not shift appreciably with temperature changes.

Q104 and Q114 form a stabilized feedback amplifier that has its DC gain set by the potentiometric ratio of R108-R109. The AC gain is higher for high frequencies due to the feedback bypass capacitor C108. (Both C108 and L104 aid to assure the total amplifier high frequency gain-bandwidth product is at high as possible.)

Q114 emitter has two bypass capacitors that aid to keep the gain high. C118 bypasses the very high frequencies and C117 bypasses the lower frequencies.

Q114 collector output is RC coupled to the TRIG OUT connector by R110 and C110. C110 assures that the low AC impedance at Q114 collector is coupled to the output connector. The output RC circuit has a 5 μs time constant. Low AC impedance occurs at Q114 collector due to the feedback path through R109. When Q114 collector moves (due to the signal) a current through R109 limits the gain. However, if some of Q114 collector signal current is required by the TRIG OUT load, that current does not get back through R109 effectively turning the output current on harder. Thus Q104-Q114 feedback amplifier output at Q114 is a very low impedance signal source.

The amplifier contains two power supply decoupling networks. R110-C110 decouple the +15-V supply from current pulses within the amplifier. R119-C119 decouple the —12.2 V supply from current pulses at the amplifier output. R114 isolates the decoupled +15-V supply from the Q104-Q114 feedback amplifier.

The active transistor will be forced to conduct significant base current when the sampling head is removed from the Type 3S2, but no damage occurs. The open circuit output voltage rises from about +0.1 V (no signal value) to about +0.8 V when there is no sampling head connected to the active trigger amplifier.

The Trigger Amplifier, SN B010101-B030249 consists of front panel TRIG OUT switch and TRIG OUT connector, transistors Q103 and Q113, and associated components. The transistors are connected as a common-base amplifier, but only one conducts at a time. The TRIG OUT switch selects the conducting transistor, Q103 for Channel A or Q113 for Channel B.

Fig. 4-2 is a schematic of only the Channel B portion of the Trigger Amplifier. Included is the signal input connection from a sampling head trigger pickoff circuit (Q17), and operating voltages. The supply voltages listed are values at the output side of power supply decoupling circuits located on the Trigger Amplifier circuit board.

Approximately 6 mA of current passes through the active transistor, as selected by the TRIG OUT switch. If the TRIG OUT switch is placed at A, D113 in series with R115 take all the current otherwise taken by Q113. Note the two voltages at Q113 emitter. Note also that when inactive, the transistor is reverse biased 0.2 volt. When the TRIG OUT switch is at B, Q113 is active and delivers an in-phase signal to the TRIG OUT connector through R114.

Fig. 4-2 shows —2.5 volts at the TRIG OUT connector. This is true only when the connector is loaded by 1 MΩ. When loaded by 50 Ω, the output voltage is —0.1 volt, but the static state DC currents within the circuit are not significantly altered.

Total circuit gain includes the characteristics of the associated sampling head. When the head is either a Type S-1

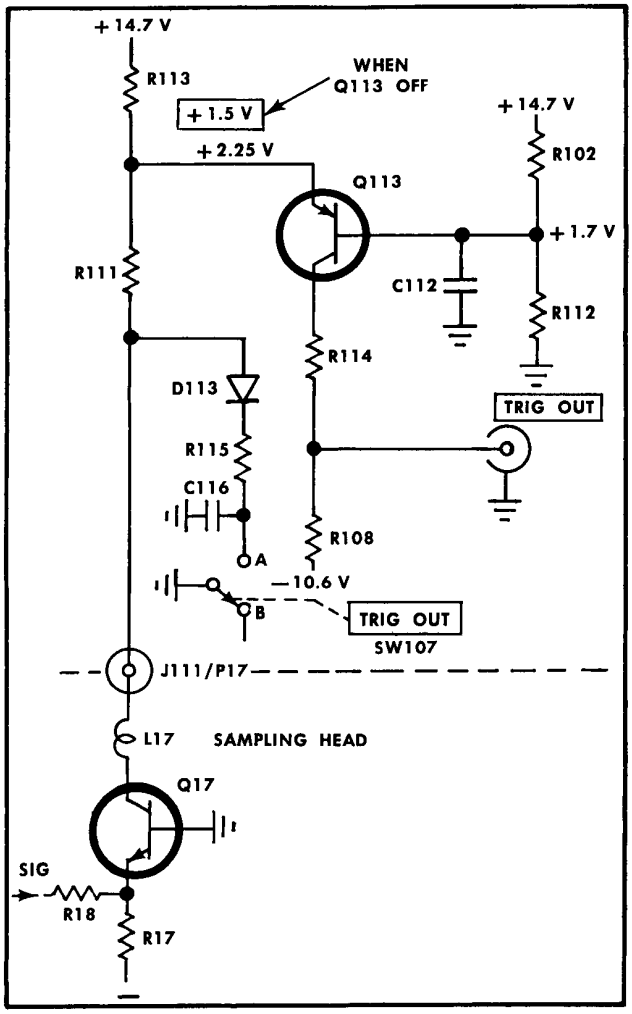


Fig. 4-2. Channnel B Trigger circuit connections.

or Type S-2, and when the TRIG OUT connector is loaded by 50 Ω, the gain is approximately 0.1, so signal output amplitude is 10% of that at the sampling head input connector. When the TRIG OUT connector is loaded by 1 MΩ, the gain is about 2.5 times the signal at the sampling head input connector. The frequency response is related to typical gain-bandwidth product, and the amplifier upper frequency limit is the highest when loaded by 50 Ω.

The active transistor will be forced to conduct significant base current when the sampling head is removed from the Type 3S2, but no damage occurs.

The Post Amplifiers are two-stage non-inverting operational amplifiers with AC coupled complementary emitter followers between the second stage and the output. The input impedance is 90 Ω, which properly terminates the coaxial cable feed from the sampling head. Output impedance is very low to provide signal current to the 50 Ω Forward Attenuator. Total AC gain is approximately 12, producing a 2.4 volt output signal for a 0.2 volt input signal. DC gain is essentially unity and feedback keeps the amplifier within its proper dynamic range.

Q123 and Q128 (channel A) are the amplifier transistors, and Q133 and Q136 are the output emitter followers. Q133 assures low output impedance for positive output signals, and Q136 assures low output impedance for negative output signals. Each emitter follower has a resistor in the collector for parasitic oscillation suppression. C134 permits the output emitters to be at different DC voltages and also assures that the emitter of the non-driving transistor follows the output voltage.

Output of the Post Amplifier is AC coupled to the NORMAL-SMOOTH switch, the DOT RESPONSE control and the Forward Attenuator (part of the Units/Div switch).

The Forward Attenuation Network consists of the NORMAL-SMOOTH switch, the DOT RESPONSE control, and the Forward Attenuator portion of the Units/Div switch.

Changing the NORMAL-SMOOTH switch to SMOOTH introduces R141 in series with the Post Amplifier output signal, reducing the loop gain to 0.3 or less compared to loop gain in the NORMAL Position.

The Forward Attenuator, made up of resistors R145A through R145G, presents a constant 500 Ω load to the driving side. The output resistance to the AC Amplifier changes from 1 kΩ to 100 kΩ in seven steps. Six of the seven resistors are always in parallel connection to ground, with the seventh in series with the signal to the AC Amplifier input. Signal pulse amplitude across the 500 Ω to ground does not change when the Units/Div switch position is changed. No attenuation occurs because the output series resistor is actually the input resistor to the feedback type AC Amplifier. The Forward Attenuator is called an attenuator because it affects the signal amplitude as it passes through the pulse chain from Post Amplifier to Memory input. Fig. 4-3 shows the full forward attenuator network and identifies the AC Amplifier input terminal. Change in signal amplitude at the AC Amplifier output is thus not actually attenuation, but a change in gain. The gain is controlled by the ratio of feedback resistor R215 to the value of the series element of R145. The AC Amplifier gain changes from 15 at 2 units/div to 0.15 at 200 units/div.

The Forward Attenuator portion of the Units/Div switch is ganged with the Feedback Attenuator portion. The result is that changing the Units/Div switch does not change the dot response (or loop gain). Changing either the NORMAL-SMOOTH switch or the DOT RESPONSE control changes only the forward signal, and thus does change the loop gain.

The Feedback Attenuator and DC Offset are connected together within the sampling head where they are combined and applied to the Sampling Bridge output terminals. The Feedback Attenuator receives the Memory circuit output signal from a very low impedance. The attenuator places one of seven resistors in series with the Memory output signal, and the other six resistors paralleled to ground as slightly more than 2000 Ω. Maximum attenuation (at 2 Units/Div) allows 0.42% of the Memory signal to pass to the Sampling Bridge circuit. Mimimum attenuation (at 200 Units/Div) allows 42% of the Memory signal to pass to the Sampling Bridge Circuit. The attenuation of 0.42% and 42% is corrected to exactly 0.40% and 40% by the parallel value of R148, R149 and 53 kΩ to ground inside the sampling head. (The Forward Attenuator ratio or AC Amplifier gain ratio of 100:1, and the feedback attenuator ratio of 1:100 assure that the loop gain is not altered throughout the Units/Div switch range).

Each channel DC Offset circuit is a single transistor emitter follower that converts the fairly high resistance of the DC OFFSET control to a fairly low resistance at the emitter. Q155 emitter voltage follows the voltage of the arm of the DC OFFSET control, offset by —0.6 volt. Q155 drives a 22.4 kΩ resistive load, consisting of Q155 output resistance, R158 19.1 kΩ and 2000 Ω of the Feedback Attenuator. Thus the DC OFFSET voltage at Q155 emitter develops a fixed voltage across the Feedback Attenuator 2000 Ω regardless of the Units/Div switch setting.

Memory Diagram

The Memory diagram applies to both channels of the Type 3S2. The diagram shows the 200-series circuit numbers of Channel A. Corresponding components in Channel B are numbered 500 through 599. Channel B pin connectors are lettered in blue. The diagram includes the AC Amplifier, the Memory Gate, the Memory Amplifier and the Inverter.

The AC Amplifier (whose gain is described above with the Forward Attenuation Network) is an inverting operational amplifier with AC coupled complementary emitter followers at the output. Q203 is the voltage amplifier, Q211 emitter follower adds current gain to Q203 collector signal, and Q223-Q224 provide the very low output resistance.

The amplifier input is AC coupled by C201 to permit the amplifier DC operating voltages to be independent of the changes made in input resistance by the Units/Div switch. Q203 base is the summing input terminal of the operational amplifier. As a signal arrives and changes the base voltage, the collector voltage changes in the opposite direction and Q211 emitter drives current of the opposite polarity through R215 back to the Q203 base. The input and feedback signal currents are equal, keeping the base voltage almost constant. The output signal is coupled to the Memory Gate by Q223, Q224 and R229, C229. R229 limits the signal output current assuring that C229 does not receive a significant charge for output signals of high pulse amplitude.

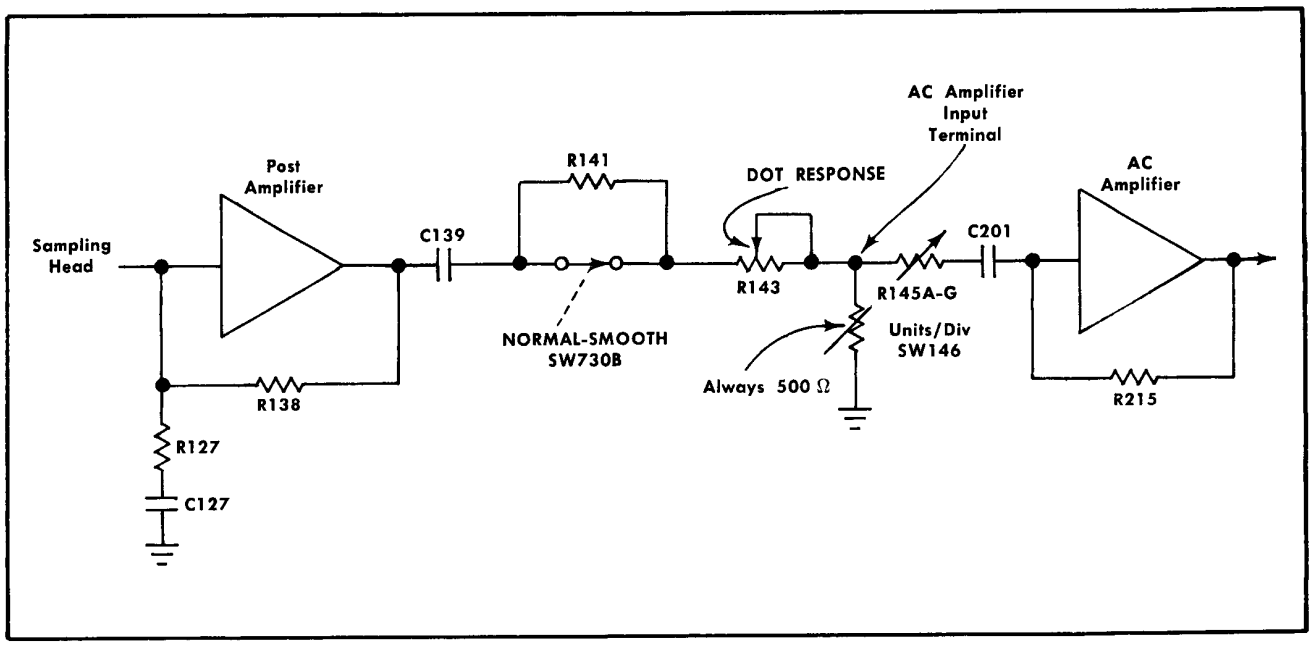


Fig. 4-3. Forward Attenuation network, showing that the output resistor of the Units/Div Forward Attenuator is actually the AC Amplifier input resistor.

The two diodes provide protection when transistors are removed from their sockets. D201 conducts if Q211 is removed, and D209 conducts if Q203 is removed. Parasitic suppressing resistors include R207, R210, R219, R221 and R225.

The Memory Gate is a special pulse driven diode gate that assures a very high input resistance to the Memory Amplifier except for about 0.15 to 0.20 μs at the time of each sample. During the conduction time, the Memory Gate is a low impedance that allows the AC amplifier to introduce a charge into the Memory Amplifier.

Fig. 4-4 is a detailed block diagram of the circuits on the Memory diagram. The Memory Gate is represented by a resistor, a coil and a relay switch. The resistor is the parallel value of the four biasing resistors which assure that the four gating diodes are normally not conducting. This equivalent circuit shows that the Memory Amplifier input is zero volts when there is no error signal at sample time.

Looking from the Memory Gate output toward its input, the four gating diodes are normally reverse biased by the voltage of Zener diode D231. (Two of the four diodes provide very high reverse biased leakage resistance, although they don't turn off very fast. The other two turn off fast at the end of the gating pulse, although they don't provide high resistance when reverse biased). D231 voltage is balanced to ground by R232 and R233 so D236 cathode rests at +2.5 volts and D238 anode rests at —2.5 volts. C231 assures that the AC Amplifier output signal drives both sides of the memory gate diodes.

The gate diodes are forward biased into conduction by T235 at the time of each sample due to the drive pulse from the Memory Gate Driver. T235 is a toroidal transformer specially wound to balance capacitive and inductive coupling to the two secondary windings. The winding with only one end connected provides the capacitive balance. The magnetic toroid core provides the inductive balance. Thus, the drive pulse is converted to identical drive signals to assure that the output junction of the four diodes accurately divides the 5 volts of D231-C231. This places the junction of D237-D239 at ground when no error signal is applied from the AC Amplifier. The Functions of the two limiting diodes D232-D233, and the Memory Gate, are discussed in the Memory Amplifier description next. R236, R238 and D234 are shunt damping loads to T235 which minimize self-inductance ringing when the memory gate drive pulse ends.

The Memory Amplifier is an integrating operational amplifier with special low leakage (high DC resistance) input circuit. The input and feedback components are capacitors, making the AC input impedance very low. The internal high gain assures a very low output resistance; so that as long as there is no change at the input, the output DC voltage remains stable. The input low leakage circuit has no DC connection to ground except during the time the Memory Gate conducts.

The Memory Amplifier is specially decoupled from the power supplies because the output stage (Q261 and Q266) can require a current pulse as great as 30 mA for a 20 volt output change at sample time. The decoupling networks are: R241-C241, R261-C261 and R267-C267. L298, in the output lead to the INVERT switch, presents a high impedance to the Memory output for high frequency (fast change) signals. The inductor assures that the output amplifier does not have to provide high current to the output load. L298 slows the output signal response, but at a time when the CRT is blanked.

A dual junction FET (Q243) is the input stage. It is biased for essentially no leakage at the input gate, and the stage has high voltage gain at the in-phase output drain lead. Any

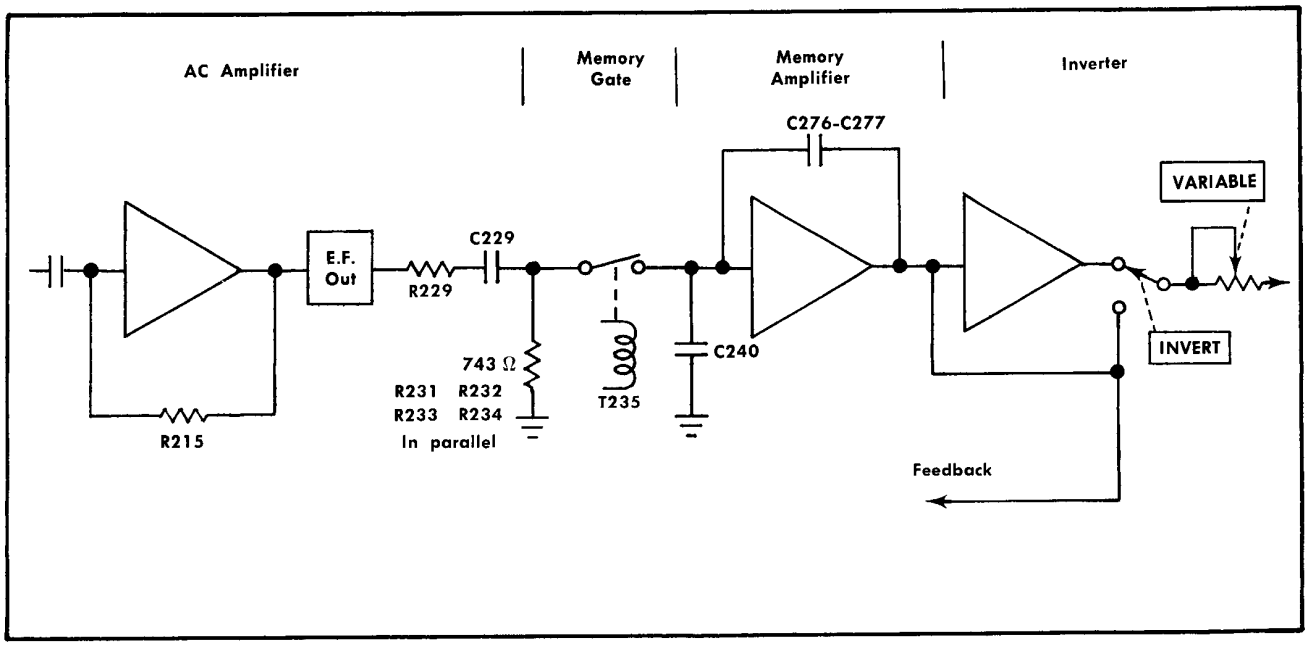


Fig. 4-4. Basic Memory Gate circuit between AC Amplifier and Memory Amplifier. (Detailed block of Memory diagram.)

voltage change at Q243A gate lead is amplified and applied to the inverting amplifier Q252. Q252 collector circuit applies proper bias to both bases of the output complementary emitter follower pair, Q261-Q266 and restores the DC level negatively so a zero input signal (at Q243A) is also a zero output signal. Q252 collector and Q261-Q266 output lead operate linearly through the range of +10 to −10 volts.

Because of the high open-loop gain, the Memory Amplifier does not have the fast risetime that the prior amplifiers have. The AC Amplifier output pulse duration is shorter than the Memory Amplifier risetime. C240 at Q243 input gate lead accepts some of the charge from the AC Amplifier, stores it until the Memory Amplifier can respond, and then loses the charge again due to feedback current.

A cycle of operation at sample time takes the following sequence:

a. The Memory Gate drive pulse arrives at essentially the same time the Sampling Bridge is strobed into conduction. Propagation delay through the three AC coupled amplifiers is quite short. The CRT is blanked at the same time. (The fact that the Memory Amplifier input is always at zero volts, and the Memory Gate is balanced around zero volts, prevents any false changes in C276-C277 charge. Therefore, there is no change in the Memory Amplifier output voltage during the time the Memory Gate conducts ahead of the arrival of the AC Amplifier output signal).

b. The AC Amplifier applies a pulse signal through R229-C229 and the Memory Gate to the Memory Amplifier input. C240 accepts some of the charge until the amplifier begins to respond, driving an equal and opposite current back to the input through the feedback capacitors.

c. Since the AC Amplifier output signal is applied to the Memory Amplifier "virtual signal ground" input, C229 receives about 10% of the total error signal charge before the Memory Gate stops conducting. Thus, as the AC Amplifier output returns to its quiescent voltage, the output side of C229 overshoots. The 743 Ω of the Memory Gate discharges C229 well in advance of the next error signal.

If the Type 3S2 is displaying a single transition step over the full graticule with the display starting at the lower left and ending at the upper right, the error signal is very large during retrace. Such large error signals (even during random process sampling) apply a significant charge to C229. Then the overshoot at the end of the error signal pulse is large enough to cause one side of the Memory Gate to conduct, and remove some of the intended charge in the feedback capacitors. Two normally non-conducting clamp diodes prevent such undesired removal of memory charge. D232 and D233 help to discharge C229 if it receives too great a charge during the Memory Gate conduction time, thus preventing false amplitude displays. These two diodes do not conduct at any other time.

d. As the Memory Gate drive pulse ends, C240 charge is removed by the Memory Amplifier feedback. This causes the Memory output voltage to continue changing toward proper amplitude for a short period of time after the Memory Gate stops conducting. As soon as C240 charge is returned to normal, the output voltage remains fixed until the next sample.

The actual resting voltage at Q243A gate may not be precisely zero, but it is within a few millivolts of zero. Any deviation from zero can be due to several things: slight differences in conduction of the Memory Gating diodes; slight differences in resistance of the four Memory Gate biasing resistors; some small error signal being generated at each sample time even when the sampling head input signal is zero. Q243B gate voltage is adjusted over a small range to allow the above normal variations. Adjustment of Q243B gate voltage is called the Smoothing Balance adjustment, because it is set so there is no change in Memory

Amplifier output when the forward attenuation is changed. The forward attenuation is changed by changing the NORMAL-SMOOTH switch between its two positions. Whatever small zero-input error signal may exist in the system it always has an average value that will not alter the memory stored charge. Changing the forward attenuation changes the peak amplitude of the residual error signal, but not its average voltage zero value. Therefore, Q243 gate voltage is adjusted to equal the average voltage zero value of the residual error signal, and the trace does not move when changing the NORMAL-SMOOTH switch position.

Memory output voltage limits of about +10 and —10 are set by two diodes in parallel with the feedback capacitors. The diodes, D276 and D277 are reverse biased by 9 volts each. If the output tries to go more positive than about +10 volts, D277 conducts (9 + 0.6 = 9.6 volts) reducing the amplifier gain to much less than 1. If the output tries to go more negative than about —10 volts D276 conducts, reducing the amplifier gain to much less than 1. The clamping diodes prevent the amplifier transistors from saturating at the time of an overdrive signal, and thus assure fast response away from the clamped voltage at the next sample.

The amplifier contains two protective diodes that conduct only when a transistor is removed from its socket. D243 prevents Q243 source leads from having to withstand —100 volts when it is plugged into its socket while the power is on. D252 protects Q252 base-emitter junction in the event Q243 is removed from its socket while the power is on.

Temperature compensation of the amplifier is accomplished effectively by the source-coupled FET input amplifier and D254 and D256. The two identical halves of Q243 compensate each other so their total current does not change with temperature change. D254 and D256 have junction-drop temperature coefficients similar to Q261 and Q266 base-emitter junctions, and thus stabilize the output circuit.

The Memory Amplifier drives the front panel vertical output jack through a resistive attenuator that delivers 40% of the memory signal through 10 kΩ. The jack is labeled A or B VERT OUTPUT, 0.2 V/DIV, 10 kΩ. The memory output signal is the standard deflection signal mentioned in Section 3, and is 0.5 volt/CRT division. The memory also drives an ×1 gain inverting amplifier, the Inverter, because the rest of the vertical amplifier stages (Channel Amplifier and Output Amplifier) invert the signal to the CRT.

NOTE

The Memory output limits of ±10 volts at 0.5 V/div equals 40 CRT divisions of display area, required when operating at high sensitivity and many divisions of DC OFFSET. The whole pulse amplifier chain is designed for full response and fast recovery so that on-screen displays have accurate deflection factors and DC offset reference. Such operation provides accurate signals at the front panel Vert Output jacks, even through much of the signal is not displayed on the 8 division CRT.

The Inverter Amplifier is a temperature compensated DC coupled operational amplifier with a gain of 1. R280 and R288 (0.1% tolerance resistors) set the gain. Q282 and Q284 emitter-coupled stage provides both the temperature compensation and high internal gain. Q287 provides the inversion and negative signal offset so the input and output can both be at zero volts at the same time. Q287 collector has the same ±10 volt operating range as the Memory output. L287 raises the load resistance during fast changes at sample time to limit the pulse current amplitude required of the — 12.2-volt supply at Q287 emitter.

Protective components are D282 which conducts when Q287 is removed from its socket and protects Q282 base-emitter junction from excessive reverse bias; D287 which conducts when Q284 is removed from its socket and protects Q287 base-emitter junction from excessive reverse bias; and C286-R286 which stabilize the amplifier against self-oscillation.

The Inverter drives the Channel Amplifier through the INVERT switch and the VARIABLE and Digital Gain controls.

A & B Channel Amps

The two Channel Amplifiers are approximately 2× gain inverting operational amplifiers. The gain is adjusted by the Digital Gain control (while the Units/Div switch VARIABLE control is at its CAL position) so the output to the Digital Unit is the required 1 V/Div. A center-screen zero signal input produces an output of +10 volts when the POSITION control is centered in its range. The output voltage can swing through approximately a 20 volt range, thus limiting the Memory output to 20 divisions of CRT display. The input current summing point is referenced approximately 0.6 volt above ground at the base of Q307 (Q607).

Q307 is the inverting amplifier and Q312 is the current gain emitter follower output. When a positive signal overdrives the amplifier, both Q307 and Q312 turn on hard, and both transistors may saturate. When a negative drive signal overdrives the amplifier, Zener diode D317 and D316 limit Q312 emitter voltage to about +21.8 volts, stopping any increase in feedback current. Once the feedback current stops following the input current, the summing input point becomes a higher impedance and starts negative. Q307 is completely cut off. D310 catches its collector at +22.4 volts, and D306 catches its base at —0.6 volt. The amplifier remains in this condition until the negative overdrive ceases.

D316 is in series with D317 to isolate D317 junction capacitance from the output terminal. C307, C315 and R315 all serve to stabilize the amplifier against self-oscillation. L313 presents a high impedance to Q312 emitter during fast signal changes so all the circuit current can be used for feedback; then, the inductor connects the load when the output voltage has stabilized. This reduces the amplitude of pulse currents required of the power supply during high amplitude fast changes.

The Channel Amplifiers always drive both the Output Amplifier and the Digital Unit. Either one may also drive the real-time time-base unit, depending upon the position of the TRIG OUT switch and the Horiz Plug-in Compatibility switch. Channel B Channel Amplifier can also drive a sampling sweep unit for the A VERT-B HORIZ mode of operation. R641 is in the circuit to simplify the construction of the Vertical Mode switch, and ground Q612 emitter at all other switch positions except A VERT-B HORIZ.

The circuit associated with the TRIG OUT switch offsets the +10-volt center-screen Channel Amplifier output signal to

zero at the junction of R332 and R334. This allows proper operation of the Non-Sampling time base DC coupled internal triggering circuit. D331 is a catching diode to stop the trigger output from going to —100 volts between positions of the TRIG OUT switch.

Output Amplifier

The Output Amplifier diagram contains circuits for three blocks of the complete block diagram: the Dual-Trace Multi, the Output Amp and the Position Lamp Driver.

The Dual Trace Multi programs the selection of the Channel Amplifier which drives the Output Amplifier, and the Dual Trace Multi operation is programmed by the Vertical Mode switch on the front panel. The Dual Trace Multi is actually a multivibrator only when the Vertical Mode switch is placed in the DUAL-TRACE position. At the other modes of operation, the Dual Trace Driver drive signal is diode-disconnected, and only one of the two transistors may conduct. A conducting transistor takes the signal current of the channel not displayed, and a non-conducting transistor permits its associated channel to be displayed. Multi transistor Q714 controls Channel B, and Q724 controls Channel A.

The signals of both Channel Amplifiers enter the Output Amplifier diagram into the emitter circuits of two common base amplifiers. These amplifiers share the collector load resistance of R753 in parallel with R762. With the exception of A + B operation, only one of the common base amplifiers (Q749 or Q759) is connected to the collector load resistance. The Output Amplifier diagram lists DC voltages for displaying Channel A. Q714 conduction (controlled by the Vertical Mode switch) forward-biases D750 so that Q749 collector voltage reverse-biases D751. This disconnects the Channel B signal from the Output Amplifier. Q724 non-conduction permits R725 to reverse bias D760, so that Q759 collector current passes through D761 and the Channel A signal reaches the Output Amplifier input. There is essentially no current in R753, but D782-C782 assure that the resistor is in parallel with R762 so far as signals are concerned.

A + B operation turns off both Q714 and Q724, permitting both Q749 and Q759 to be connected to R753-R762. Both channel signals are thus added algebraically. R753 is now connected to +15 volts. This doubles the DC current in the collector load resistance, so the current of both common base stages added together does not alter the DC level into the Output Amplifier. There will probably be a vertical shift in the display when changing the vertical mode switch from CH B to A + B, the amount of shift depending upon the voltage tolerance of Zener diode D782.

Dual-Trace operation forward biases D701 so the —50 V to 0 V Dual-Trace Driver signal can reach the Dual-Trace Multi and switch it at each sample time. Each time a sample is taken, the Dual-Trace Multi changes states on the positive portion of the drive pulse. Each time the multi changes states the Output Amplifier is driven by the other channel. The multi divides the sampling rate by two and delivers a Digital Intensified Zone Enable signal (up = logical 0 at about +1 volt = CH A; down = logical 1 at about —1 volt = CH B) to the digital unit from Q714 collector.

The Output Amplifier consists of the high gain stage Q771 and Q775, and a ×1 inverting amplifier Q781 and Q785. The high gain stage drives the inverter. Both circuits are DC coupled operational amplifiers with a common negative point at Zener diode D782.

Signals arrive from the common-base stages Q749 and/or Q759, and pass through the front panel GAIN control to the summing input at the base of Q771. The internal Vertical Centering control also applies a DC signal to the same summing point, permitting adjustment for differences in the center-screen voltage that appears at the common-base switching stages, and the tolerance range of D782. Signals are amplified by Q771 and given current gain by emitter follower Q775. (All four Output Amplifier transistors have BV_{CBO} ratings of 300 volts). D774 connects Q771 collector to the output if Q775 base falls faster than its emitter for fast full screen positive-going changes. Q775 emitter also drives the ×1 inverter input.

The inverter amplifier is identical to that just described, except that the gain is 1. D784 connects Q781 collector to the output if Q785 base falls faster than its emitter for fast full screen negative-going changes. Both sides of the Output Amplifier drive the Position Lamp Driver stage.

The position Lamp Driver is a floating current switch that operates the two position-indicating neons on the front panel.

The average voltage at the CRT deflection plates is about +180 volts, which sets the total emitter current of Q793 and Q795 at 0.3 mA. When the two deflection plate voltages are equal, the two transistors share the 0.3 mA and both neons are lighted. If either side neon goes more positive than the other, the transistor on that side takes all the 0.3 mA and the other transistor cuts off. Each transistor has a BV_{CBO} rating of 85 volts, so R797 prevents the turned off-transistor collector from going all the way to +300 volts. The dark neon has some voltage across it, but not enough to cause it to glow. D791 and D792 assure that the two transistor base voltages are never more than 0.6 volts apart.

Gate Generators

The Gate Generators diagram contains circuits for the Blocking Oscillator, Dual-Trace Driver, both Delay & Strobe Drivers and both Memory Gate Drivers. The Blocking oscillator starts the sampling process when driven by the Sampling sweep unit with the Horiz Plug-In Compatibility switch at Sampling 3T-Series. When the Horiz Plug-In Compatibility switch is at Non-Sampling 2B, 3B-Series, the Dual-Trace Driver oscillates at 100 kHz and drives the Blocking Oscillator. The Blocking Oscillator always drives the two Delay & Strobe Driver circuits. The Dual-Trace Driver always drives the Dual-Trace Multivibrator and CRT cathode for interdot blanking of the display.

The Blocking Oscillator can be thought of as a risetime improving circuit. If the sampling sweep unit drive pulse risetime changes from one type of time base to another, the Blocking Oscillator cancels the difference. Q3 always delivers a signal of the same amplitude and same risetime at its output. The stage is a simple amplifier until T3 builds up enough positive feedback for regeneration. After regeneration, the circuit ignores the drive pulse shape, amplitude and energy content. Q3 is normally biased to cutoff, causing the output signal to go from +15 volts to ground each time it is driven. D2 disconnects T3 backswing pulse from Q3 base and also makes certain T3 does not load the drive pulse.

The Dual-Trace Driver is a monostable multivibrator during Sampling 3T-Series operation, and a free running 100 kHz Colpitts oscillator during Non-Sampling 2B, 3B-Series operation.

As a monostable multivibrator, neither transistor conducts until driven. — 12.2 volts is applied to R10 and R19, placing Q17 at zero bias. Q24 is reverse biased by the junction drop of D24 and current in R21.

A negative drive pulse from the Blocking oscillator is coupled through C15 and C23 to Q24 base. (D15 is reverse-biased 15 volts while Q17 is off, so it doesn't stop the drive pulse from reaching Q24.) Q24 turns on hard and D25-C25 couples drive to Q17 base. Q17 turns on and applies more drive to Q24, limited at ground by D15. Thus a heavy regeneration causes a 50 volt output pulse to drive both the Dual-Trace Multi and the CRT cathode circuit. C23 charges rapidly, but C22 does not. C22 holds base drive current applied to Q24 for a longer period. When C22 is charged, Q24 cuts off and its falling collector signal is AC coupled by C25 alone to Q17 base turning it off. The turn-off is also regenerative, with D24 limiting the reverse bias on Q24 and helping to recharge C23 for the next cycle. (R22 in series with C22 causes the positive portion of the output signal to be stable at essentially ground. The time of conduction is independent of drive because Q17 keeps D15 conducting until the regenerative turn-off starts.)

Placing the Horiz Plug-In Compatibility switch to Non-Sampling 2B, 3B-Series converts Q17 to a Colpitts oscillator. Now the Blocking Oscillator receives no signal from the real-time time-base unit. Instead, it is driven by the oscillator through C4. The Dual Trace Multi still produces a 50 volt output pulse because D25 is reverse biased most of the time. The oscillator frequency is controlled by L8, C9 and C10.

The Delay & Strobe Driver and Memory Gate Width circuits are actually one circuit. The A and B channel circuits are identical except for R32, located between +15 volts and the B DELAY control. R32 is a power supply isolation resistor. The Channel B circuit is explained below.

The complete circuit, from Blocking Oscillator output to the two pulse outputs, consists of: A two-diode comparator that compares a negative-going ramp with a fixed DC voltage variable by the Delay control; a very low-current amplifier that follows the Delay control voltage without affecting its output to the next stage; and a monostable multivibrator with two output terminals.

Quiescent circuit conditions are: Q36 base voltage rests between +15 and +11 volts, as set by the B DELAY control. Q36 current is limited to about 1 mA by R36, which does not pull the collector up to —12.2 volts. Instead, D38 clamps the collector at —12.8 volts assuring that there is no change in output voltage when the Delay control position is changed. Q41 is reverse biased 0.6 volt by D38, and Q54 is reverse biased 0.6 volt by current in D54, D52, R51 and the Memory Gate Width control. Q54 collector voltage is —12.2 volts.

As the Blocking Oscillator fires, R34-C34 form a negative-going ramp that soon causes D34 to conduct. When D34 conducts, the ramp turns Q36 on. C36 contains enough charge for Q36 collector to clear D38 of carriers, and to forward-bias Q41. As Q41 conducts, the negative signal is coupled through C41 and C33 back to Q36 base in a regenerative turn-on. The feedback signal also reverse-biases D31 and D34 so as not to disturb the other channel Delay circuit.

The —27 volt signal from Q41 collector drives Q54 through C45. C45 signal current reverse-biases D52, allowing R53 to turn on just into saturation. Q54 collector signal couples through R48 back to Q41 base and holds Q41 in steady conduction. R59 applies a steady 50 mA current to the Memory Gate transformer primary (T535) for the pulse duration of about 180 ns.

C33 regenerative turn-on to Q36 does not last as long as Q54 turn-on to Q41, but since Q41 base voltage cannot go more positive than about —11.6 volts, Q36 collector is not disturbed. The duration of Q54 conduction is therefore controlled only by the position of the Memory Gate Width control which adjusts C45 charge rate. The smaller the resistance, the shorter the gate duration. As C45 charges toward +15 volts, D52 again conducts and turns Q54 off, stopping the Memory Gate pulse and the drive to Q41 base. However, Q41 was in saturation, so it does not stop conducting immediately. Q41 collector signal rises positive about 350 ns after it is driven negative. This RC rise is slow and does not couple much energy through either C41 or C33. Q41 total negative step is coupled by C41 as a Strobe Drive pulse to the sampling head.

The sampling drive pulse from the sampling sweep unit is slewed in time from the initial trigger event of each sweep. An additional time positioning is accomplished in the two Delay (ramp comparator) circuits. The additional time slewing of the strobe drive pulses requires an identical time slewing of the Memory Gate drive pulses in order to maintain proper processing of the error signals into the Memory Amplifier. Therefore, the Memory Gate Driver is driven by the Delay & Strobe Driver.

Power Distribution & Connectors

The Power Distribution & Connectors diagram contains many power supply decoupling networks and the internal power supplies. Power from the indicator oscilloscope enters through P11 at the left edge of the diagram. P11 also shows pin connections of other circuits within the Type 3S2.

Decoupling networks are drawn within outlined areas that represent particular diagrams already described. At the page right are the decoupling networks that are located on the left side Vertical Board.

One section of the Vertical Mode switch shows the biasing voltage change sent to the sampling sweep unit horizontal amplifier during A VERT B HORIZ operations. Function of the bias change is discussed in the sweep unit instruction manual.

Internal Power Supplies obtain power from the indicator oscilloscope at 6.3 VAC, and from the +125-volt and —100-volt supplies.

The +15-Volt Supply is fed 6.3 VAC at T821. T821 secondary voltage of approximately 51 VAC is rectified by D823-D825, filtered by C824, and regulated by D827, Q828, Q830, Q836 and Q839. The regulator circuit is of the series type, with Q839 the series pass (variable resistance) transistor. Q828 and Q830 form a temperature compensated comparator circuit, and Q836 inverts and amplifies the compar-

ator output which controls Q839. The output voltage is compared with the reference Zener diode D827.

Assume a positive change in the output voltage. The correcting action that follows causes Q839 series resistance to increase, restoring the output voltage to its correct value. The positive change at the output is directly coupled to Q828 base, and attenuator-coupled to Q830 base. Q830 emitter is driven by Q828 emitter and follows the change all the way. Q830 base does not follow the change 100% and therefore the transistor receives a forward bias signal. Q830 increases its current and applies a positive signal to Q836 base, causing Q836 to reduce its collector current. (In normal operation all Q836 collector current is Q839 base current, and none passes through R837-D837). Current reduction in Q836 causes Q839 base and emitter to go more negative. Or more properly stated, Q839 increases its series resistance so the load current increases the voltage across it, restoring the output to its proper value. R837-D837 take all Q836 collector current if the +15 volts output is shorted, permitting Q839 emitter to go positive with respect to the base, and thus become a very high series resistance. Such high resistance of Q839 protects the transformer and rectifiers from damage.

The —50 Volt Supply consists of the comparator, Q842-Q844, and shunt regulator Q848. (The —50-Volt supply is one of two voltage references for the +50 V supply).

The supply changes the resistance of Q848 to take more current when the load current reduces, and to take less current when the load current increases. D848 protects Q848 from damage in the event the output is shorted to a voltage more positive than —12.2 volts.

Comparator transistors Q842-Q844 compare a voltage near ground at the junction of R845-R846 with zero volts at ground. If the output load current increases (output voltage goes positive), Q844 base and emitter follow the change. Q844 emitter drives Q842 emitter positively, which is an increase in forward bias and turns Q842 on harder. Q842 collector voltage change decreases Q848 turn-on-bias, increasing Q848 resistance and permitting a negative return in voltage at the supply output.

The +50-Volt Supply uses one transistor as an emitter follower and the other transistor as both a comparator and as the shunt regulating element. R857-R858 presents a voltage near +15 volts to the base of emitter follower Q856. Q856 provides current gain to the signal and applies it to the base of comparator-regulator transistor Q853.

If the output load current increases (voltage goes negative), Q856 emitter takes Q853 base negative, reducing Q853 current. As Q853 current reduces, the output voltage rises back to its proper value.

A short circuit that places the +50-Volt line less positive than +15 volts will reverse-bias Q853 and protect Q853 from damage. The large resistance value of R857 and R858 protects Q856 from damage.

A short circuit on the —50-Volt line will cause the +50-Volt output to be a few volts low. Again, no transistors will be damaged.

Digital Switching

The Digital Switching diagram contains information on the Units/Div and VARIABLE CAL switches, and their connections out to the Digital Unit. The Units/Div switch selects the Digital Unit decimal neon and units nixie operation for both Channels when the VARIABLE controls are at CAL. Diodes in some of the lines prevent logic interactions when the associated digital unit is externally programmed.

NOTES

SECTION 5
MAINTENANCE

Change information, if any, affecting this section will be found at the rear of the manual.

Introduction

This section of the manual contains maintenance information for use in preventive maintenance, corrective maintenance or troubleshooting of the Type 3S2.

PREVENTIVE MAINTENANCE

General

Preventive maintenance consists of cleaning, visual inspection, lubrication, etc. Preventive maintenance performed on a regular basis will help prevent instrument failure and will improve reliability of this instrument. The severity of the environment to which the Type 3S2 is subjected will determine the frequency of maintenance.

Cleaning

The Type 3S2 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path.

The top and bottom covers of the 560-series instruments into which the Type 3S2 fits, provide protection against dust in the interior of the instrument. Operating without the covers in place will require more frequent cleaning.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastic used in this instrument. Some chemicals to avoid are benzene, toluene, xylene, acetone or similar solvents.

Exterior. Loose dust accumulated on the outside of the Type 3S2 can be removed with a soft cloth or small paint brush. The paint brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild solution of water and detergent. Abrasive cleaners should not be used.

Interior. Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high-humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air. Remove any dirt which remains with a soft paint brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces on circuit boards.

Lubrication

The reliability of potentiometers, rotary switches and other moving parts can be increased if they are kept properly lubricated. Use a cleaning-type lubricant (such as Tektronix Part No. 006-0218-00) on switch contacts. Lubricate switch detents with a heavier grease (such as Tektronix Part No. 006-0219-00). Potentiometers should be lubricated with a lubricant which will not affect electrical characteristics (such as Tektronix Part No. 006-0220-00). Do not over-lubricate. A lubrication kit containing the necessary lubricants and instructions is available from Tektronix. Order Tektronix Part No. 003-0342-00.

Visual Inspection

The Type 3S2 should be inspected occasionally for such defects as broken connections, improperly seated transistors, damaged circuit boards and heat-damaged parts.

The remedy for most visible defects is obvious; however, care must be taken if heat-damaged parts are located. Overheating is usually only a symptom of trouble. For this reason, it is essential to determine the actual cause of overheating before the heat-damaged parts are replaced; otherwise, the damage may be repeated.

Recalibration

To assure accurate measurements, check the calibration of this instrument after each 500 hours of operation or once every six months.

Parts Identification

Identification of Switch Wafers. Wafers of switches shown on the circuit diagram are numbered from the first wafer located behind the detent section of the switch to the last wafer. The letters F and R indicate whether the front or the rear of the wafer is used to perform the particular switching function. For example, the designation 2R printed by a switch section on a schematic identifies the switch section as being on the rear side of the second wafer when counting back from the front panel.

Wire Color Code. The wiring in the Type 3S2 is color coded to facilitate circuit tracing. In the case of power-supply leads, the color code indicates the voltage carried, with the widest stripe denoting the first significant figure. Table 5-1 lists the color combinations and the voltages indicated by the colors.

All leads that clip to the circuit boards are color coded. The color code of each lead and the pin lettering is shown in parts location figures later on in this section.

Resistor Coding. The Type 3S2 uses a number of very stable metal film resistors identified by their gray background color and color coding.

If the resistor has three significant figures with a multiplier, the resistor will be EIA color coded. If it has four significant figures with a multiplier, the value will be printed on the resistor. For example, a 333 kΩ resistor will be color coded, but a 333.5 kΩ resistor will have its value printed on the resistor body.

The color-coding sequence is shown in Fig. 5-1.

TABLE 5-1

Power Supplies Wire Color Coding

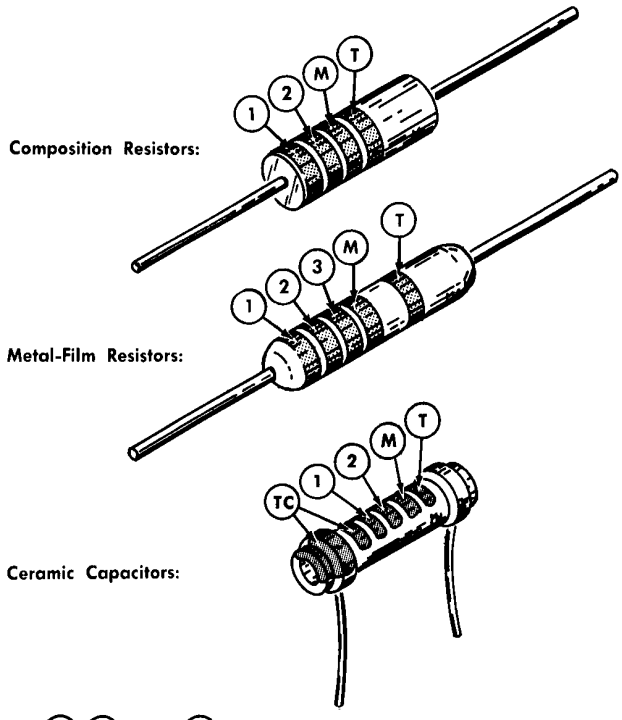
Supply	Color Code
−12.2 V	Brown Red Black on Tan
−100 V	Brown Black Brown on Tan
+15 V	Brown Green Black on White
+125 V	Brown Red Brown on White
+300 V	Orange Black Brown on White

Capacitor Marking. The capacitance values of common disc capacitors and small electrolytics are marked in microfarads on the side of the component body. The white ceramic capacitors used in the Type 3S2 are color coded in picofarads using a modified EIA code (Fig. 5-1).

Diode Color Code. The cathode end of each glass enclosed diode is indicated by a stripe, a dot or a series of stripes. For normal silicon or germanium diodes the stripes also indicate the type of diode, using the resistor color-code system (e.g., 6185 indicates the type of diode with Tektronix Part No. 152-0185-00). The cathode and anode ends of metal-enclosed diodes can be distinguished by the diode symbol marked on the body or by the flared end of the anode.

Parts Replacement

All parts used in the Type 3S2 can be purchased directly through your Tektronix Field Office or Representative. However, replacements for standard electronic items can generally be obtained locally in less time than is required to obtain them from Tektronix. Replacements for the special parts used in the assembly of the Type 3S2 should be ordered from Tektronix since these parts are either manufactured or selected by Tektronix to satisfy a particular requirement. Before purchasing or ordering, consult the Electrical Parts List to determine the value, tolerance and rating required.



(1) (2) and (3) —1st, 2nd and 3rd significant figures;
(M) —multiplier; (T) —tolerance;
(TC) —temperature coefficient.

Resistor and Capacitor Color Code

Color	Significant Figures	Multiplier		Tolerance	
		Resistors	Capacitors	Resistors	Capacitors
Silver	---	10^{-2}	---	±10%	---
Gold	---	10^{-1}	---	±5%	---
Black	0	1	1	---	±20% or 2 pF*
Brown	1	10	10	±1%	±1% or 0.1 pF*
Red	2	10^{2}	10^{2}	±2%	±2%
Orange	3	10^{3}	10^{3}	±3%	±3%
Yellow	4	10^{4}	10^{4}	±4%	+100% −0%
Green	5	10^{5}	10^{5}	±0.5%	±5% or 0.5 pF*
Blue	6	10^{6}	10^{6}	---	---
Violet	7	---	---	---	---
Gray	8	---	10^{-2}	---	+80% −20% or 0.25 pF*
White	9	---	10^{-1}	---	±10% or 1 pF*
(none)	---	---	---	±20%	±10% or 1 pF*

*For capacitance of 10 pF or less.

NOTE: (T) and/or (TC) color code for capacitors depends upon manufacturer and capacitor type. May not be present in some cases.

Fig. 5-1. Resistor and ceramic capacitor color-code.

NOTE

When selecting the replacement parts, it is important to remember that the physical size and shape of a component may affect its performance at high frequencies. Parts orientation and lead dress should duplicate those of the original part since many of the components are mounted in a particular way to reduce or control stray capacitance and inductance. After repair, portions of the instrument may require recalibration.

Power Supply Filter Capacitor C824. Unsolder the capacitor leads and push the capacitor from the clamp towards the left side of the unit. Install the replacement capacitor and solder the leads.

Transformer T821. The transformer is mounted by two screws, located on each side of the soldered connections. Be sure that leads from the circuit boards do not touch the transformer and that the transformer leads do not short.

Rotary Switches. Individual wafers or mechanical parts of rotary switches are normally not replaced. The availability of replacement switches, either wired or unwired, is detailed in the Electrical Parts List.

Circuit Boards. Use ordinary 60/40 solder and a 35- to 40-watt pencil type soldering iron on the circuit boards. The tip of the iron should be clean and properly tinned for best heat transfer to the solder joint. A higher wattage soldering iron may separate the etched wiring from the base material.

All of the components mounted on the Vertical and Control circuit boards can be replaced without removing the boards from the instrument. Observe soldering precautions given under Soldering Techniques in this section.

Replacement of soldered-in diodes. Grasp the diode lead between the body of the diode and the circuit board with a small pair of tweezers.

Touch the tip of the soldering iron to the lead where it enters the circuit board. Do not lay the iron tip directly on the circuit board. Gently but firmly pull the diode lead from the hole in the circuit board. If removal of the lead does not leave a clean hole, apply a sharp object such as a toothpick or pointed tool while reheating the solder. Avoid using too much heat.

NOTE

Cleaning of the circuit board hole while the board is mounted in the instrument is not recommended. Solder pushed through the hole toward the back side cannot always be cleared away unless the back side is accessible. Thus, clear the mounting holes only when the board is out of the instrument.

To place the new diode, bend the leads and trim to fit just through the board. Tin each lead while using the tweezers as a heat sink. Place the diode leads in the holes. Apply a small amount of solder, if necessary, to assure a good bond. Use the tweezers as a heat sink and use only enough heat for a good connection.

Replacement of other soldered-in components. Grip the component lead with long-nose pliers. Touch the soldering iron to the lead at the solder connection. Do not lay the iron directly on the board, as it may damage the board. Refer to Fig. 5-2.

When the solder begins to melt, pull the lead out gently. This should leave a clean hole in the board. If not, the hole can be cleaned by reheating the solder and placing a sharp object such as a toothpick or pointed tool into the hole to clean it out.

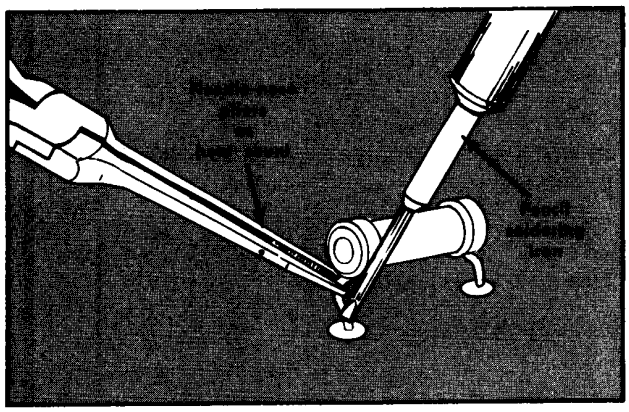


Fig. 5-2. Apply the soldering iron to the heat-shunted lead when removing a component from a circuit card.

Bend the leads of the new component to fit the holes in the board. If the component is replaced while the board is mounted in the instrument, cut the leads so they will just protrude through the board.

Pre-tin the leads of the component by appling the soldering iron and a small amount of solder to each (heat-shunted) lead. Insert the leads into the board until the component is firmly seated against the board. If it does not seat properly, heat the solder and gently press the component into place.

Apply the iron and a small amount of solder to the connection to make a firm solder joint. To protect heat-sensitive components, hold the lead between the component body and the solder joint with a pair of long-nose pliers or other heat sink.

Clean the area around the soldered connection with a flux-remover solvent to maintain good environmental characteristics. Be careful not to remove information printed on the board.

Metal Terminals. When soldering metal terminals (e.g., switch terminals, potentiometers, etc.), ordinary 60/40 solder can be used. The soldering iron should have a 40- to 75-watt rating with a $\frac{1}{8}$ inch wide chisel-shaped tip.

Observe the following precautions when soldering metal terminals:

1. Apply only enough heat to make the solder flow freely.

2. Apply only enough solder to form a solid connection. Excess solder may impair the function of the part.

3. If a wire extends beyond the solder joint, clip off the excess.

4. Clean the flux from the solder joint with a flux-remover solvent to maintain good environmental characteristics.

Circuit Board Replacement. If a circuit board is damaged and cannot be repaired, the entire assembly including all soldered-on components should be replaced. The part number given in the Mechanical Parts List is for the completely wired board.

Procedure for replacing circuit boards follows:

For the Vertical and Control circuits boards,

1. Disconnect all square pin and coaxial connectors by pulling straight out from the board.

2. Remove the board mounting screws.

3. Install the replacement board and replace the mounting screws.

4. Replace the square pin and coaxial connectors, referring to the wire color coding and pin identification information at the end of this section.

For the Trigger circuit board,

1. Remove the board by applying slight pressure outward at the plastic clips.

2. Disconnect all square pin and coaxial connectors by pulling straight out from the board.

3. Reconnect the square pin and coaxial connectors to the replacement board, referring to the wire color coding and pin identification information at the end of this section.

4. Install the replacement board in the plastic clips.

TROUBLESHOOTING

Introduction

The following information is provided to facilitate troubleshooting of the Type 3S2 if trouble develops. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component.

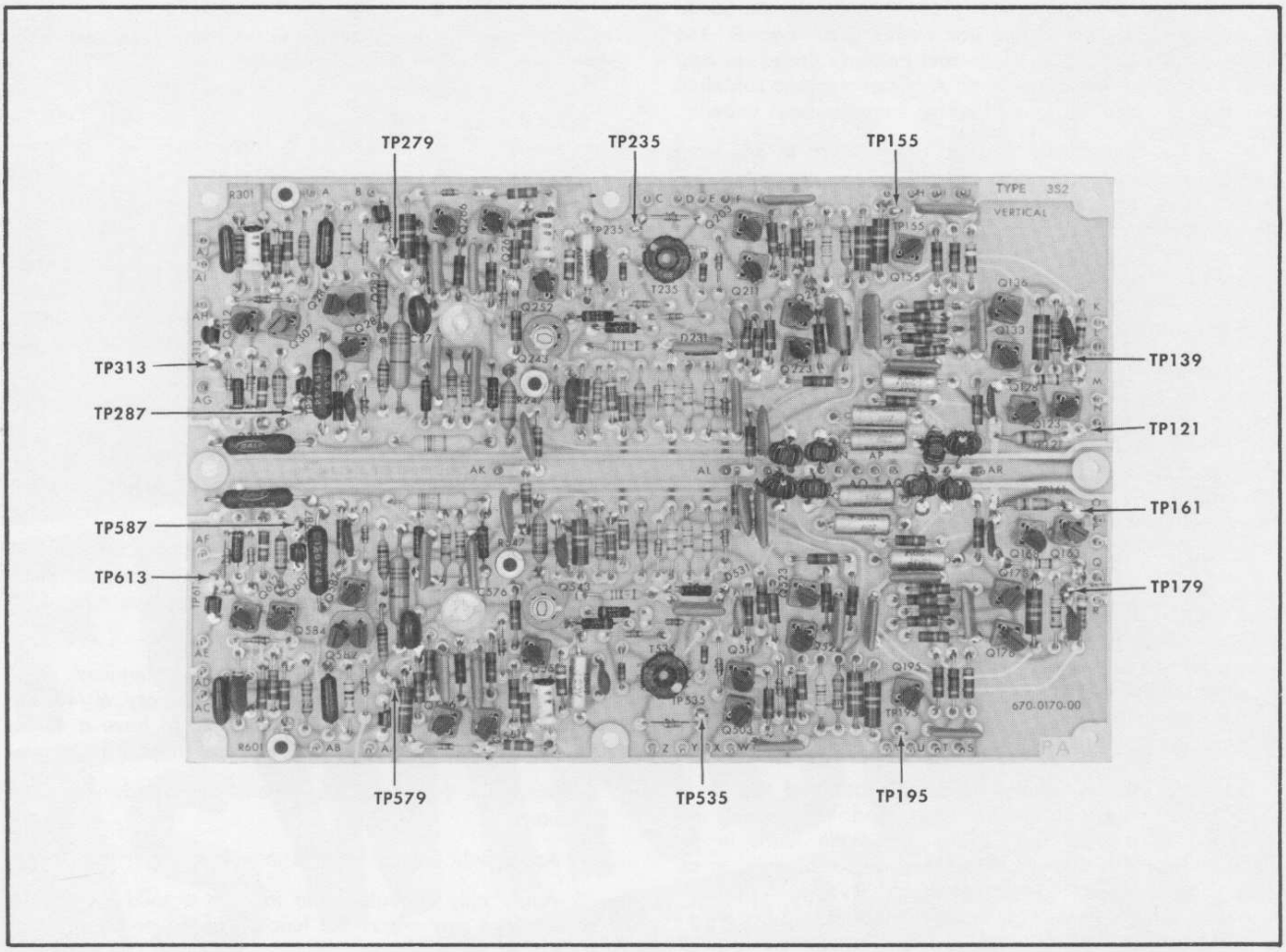


Fig. 5-3. Test point locations, Vertical circuit board.

Troubleshooting Aids

Diagrams. Circuit diagrams are given on foldout pages in Section 11. The circuit number and electrical value of each component in this instrument are shown on the diagram.

Component Numbering. The circuit number of each electrical part is shown on the circuit diagram. Each main circuit is assigned a series of circuit numbers. Table 5-2 lists the main circuit in the Type 3S2 and the series of circuit numbers assigned to each. For example, using Table 5-2, a resistor numbered R615 is identified as being located in the Channel B Channel Amplifier.

TABLE 5-2

Circuit Numbers on Schematics	Circuit
1-100	Gate Generators
100-199	Post Amplifier & Attenuators
200-299	Channel A Memory
300-399	Channel A Channel Amplifier
500-599	Channel B Memory
600-699	Channel B Channel Amplifier
700-799	Output Amplifier
800-889	Power Distribution and Connectors
890-899	Digital Switching

Troubleshooting Techniques

This troubleshooting procedure is arranged in an order which checks the simple trouble possibilites before proceding with extensive troubleshooting. The first few checks assure proper connections, operation and calibration. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located it should be replaced following the replacement procedures given in this section.

1. Check Associated Equipment. Before proceeding with troubleshooting of the Type 3S2 check that the equipment used with the Type 3S2 is operating correctly. Check that the signal is properly connected and that the interconnecting cables are not defective. Also, check the power source.

2. Check Control Settings. Incorrect control settings can indicate a trouble that does not exist. For example, incorrect setting of the Vertical Units/Div VARIABLE control appears as incorrect gain, etc. If there is any question about the correct function or operation of any control, see the Operating Instructions section of this manual.

3. Check Instrument Calibration. Check the calibration of the instrument, or the affected circuit if the trouble exists in one circuit. The indicated trouble may only be a result of misadjustment or may be corrected by calibration. Complete instructions are given in the Calibration section of this manual.

4. Isolate the Trouble to a Circuit. If the trouble has not been corrected or isolated to a particular circuit with the preceding steps, make the following checks if possible.

a. Check for the correct resistance readings at the interconnecting plug terminals, as indicated in Table 5-3.

If the resistance values at the interconnecting plug are equal to or higher than stated in Table 5-3, proceed with the next step.

b. Install any sampling head and correct the Type 3S2 to the oscilloscope in which it will normally operate. Use the flexible cable extension, Tektronix Part No. 012-0006-00.

TABLE 5-3

Interconnecting Plug Resistance Checks

Sampling Heads removed and the Type 3S2 disconnected from Oscilloscope (pin numbers omitted are unconnected)

Pin Number	Resistance to Ground	Meter Leads Reversed
1	infinite	infinite
2	infinite	infinite
9	0	0
10	38 kΩ	13 kΩ
11	0	0
12	46 kΩ	48 kΩ
15	4.4 kΩ	4.6 kΩ
16	1 kΩ	1 kΩ
17	40 kΩ	15 kΩ
18	320 kΩ	300 Ω
19	0	0
20	5.8 kΩ	6 kΩ
21	32 kΩ	15 kΩ
22	0	0
23	5 kΩ	4 kΩ
24	5 kΩ	10 kΩ

Turn on the instrument and allow at least 5 minutes warm-up time.

Incorrect operation of all circuits often indicates trouble in the power supplies. Check first for correct adjustment of the individual supplies. However, a defective component elsewhere in the instrument can appear as a power-supply trouble and may also affect the operation of other circuits.

Table 5-4 shows the tolerance of the internal supply voltages and the normal voltages supplied by the oscilloscope. If a power supply voltage is within the listed tolerances, the supply can be assumed to be working correctly. If outside the tolerances, the +15 volt adjustment may be incorrect, or a component may be defective. All power supply test points are located on the Control Board.

Power Supply voltage checks may be made at the points indicated in Table 5-4 or Fig. 5-4.

Table 5-5 shows typical voltage readings at the various test points, with the front-panel controls set as follows:

A and B DC OFFSET controls	Adjusted for 0 volts at OFFSET OUT jacks
A and B POSITION controls	Centered

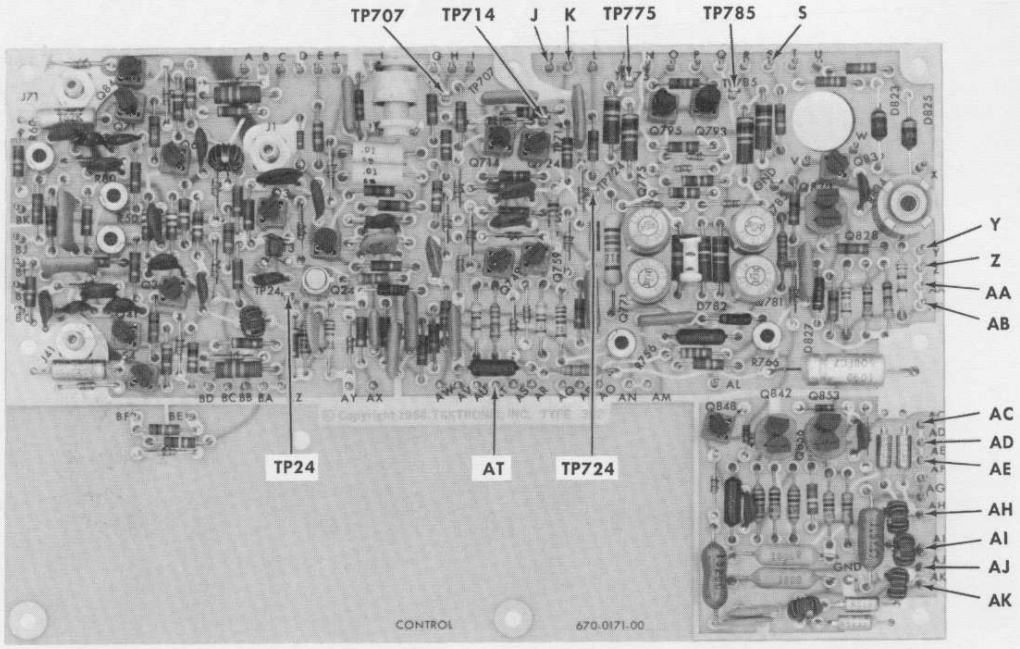


Fig. 5-4. Test point locations, Control circuit board.

Mode Switch	CH A
A and B Vertical Units/Div	200
NORMAL/SMOOTH	NORMAL
Horiz Plug-In Compatibility	Sampling

TABLE 5-4

Power Supply	Tolerance	Test Point
+15 V[1]	±0.15 V	Pin Y, Z, AA or AB
+50 V	±1 V	Pin AJ or AK
+125 V		Pin K or J
+300 V		Pin S
−12.2 V		Pin AT
−50 V	±0.5 V	Pin AH or AI
−100 V		Pin AD, AC or AE

[1]Adjusted by R834.

Transistor Checks

Transistors should not be replaced unless they are actually defective. Transistor defects usually take the form of the transistor opening, shorting or developing excessive leakage. To check a transistor for these and other defects, use a transistor curve display instrument such as a Tektronix Type 575. However, if a good transistor checker is not readily available, a defective transistor can be found by signal-tracing, by making in-circuit voltage checks, by measuring the transistor forward-to-back resistance ranges, or by using the substitution method. The location of all transistors is shown in the parts location figures later in this section.

To check transistor using a voltmeter, measure the emitter to-base and emitter-to-collector voltages and determine whether the voltages are constant with the normal resistances and currents in the circuit (see Fig. 5-5). Note the electrode configuration in Fig. 5-6.

To check a transistor using an ohmmeter, know your ohmmeter ranges, the currents they deliver and the internal battery voltage(s). If your ohmmeter does not have sufficient resistance in series with its internal voltage source, excessive

TABLE 5-5

TEST POINT VOLTAGE READINGS

Vertical Board Test Point	Voltage Reading	Vertical Board Test Point	Voltage Reading	Control Board Test Point	Voltage Reading
121	0	279	+0.08	24	—44
139	0	287	—0.15	707	+1.2
155	—0.02	313	+8.7	714	+12.7
161	0	535	—12.2	724	—1.4
179	0	579	+9.7	775	+180
195	—0.005	587	—9.7	785	+175
235	—12.2	613	+21		

current will flow through the transistor under test. Excessive current and/or high internal source voltage may permanently damage the transistor.

NOTE

As a general rule, use the R X 1K range where current is usually limited to less than 2 mA and the internal voltage is usually 1½ volts. You can quickly check the current and voltage by inserting a multimeter between the ohmmeter leads and measuring the current and voltage for the range you intend to use.

When you know which ohmmeter ranges will not harm the transistor, use those ranges to measure the resistance with the ohmmeter connected both ways as given in Table 5-6.

If there is doubt whether the transistor is good, substitute a new transistor; but first, be certain the circuit voltages applied to the transistor are correct before making the substitution.

Two transistors, Q103 and Q311, have soldered leads only. Q839 is mounted with two bolts that can be removed only after the Control board has been removed. Use a 5/16 inch socket wrench to remove the nuts while holding the bolt heads with the other hand. All other transistors have sockets or are mounted to the board without solder.

When checking transistors by substitution, be sure that the voltages on the transistor are normal before making the substitution. If a transistor is substituted without first checking

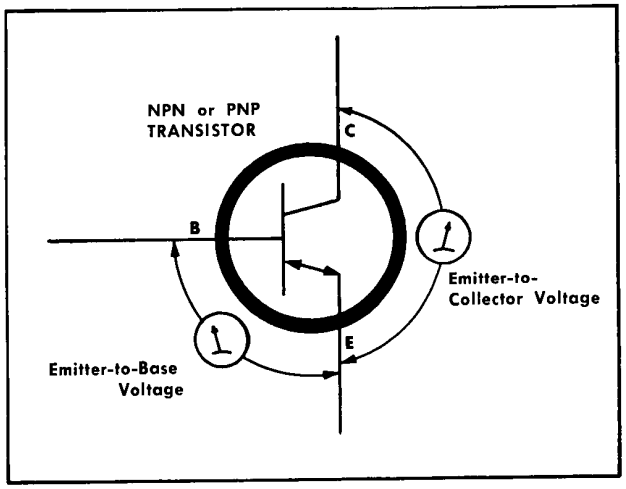


Fig. 5-5. In-circuit checks NPN or PNP transistors.

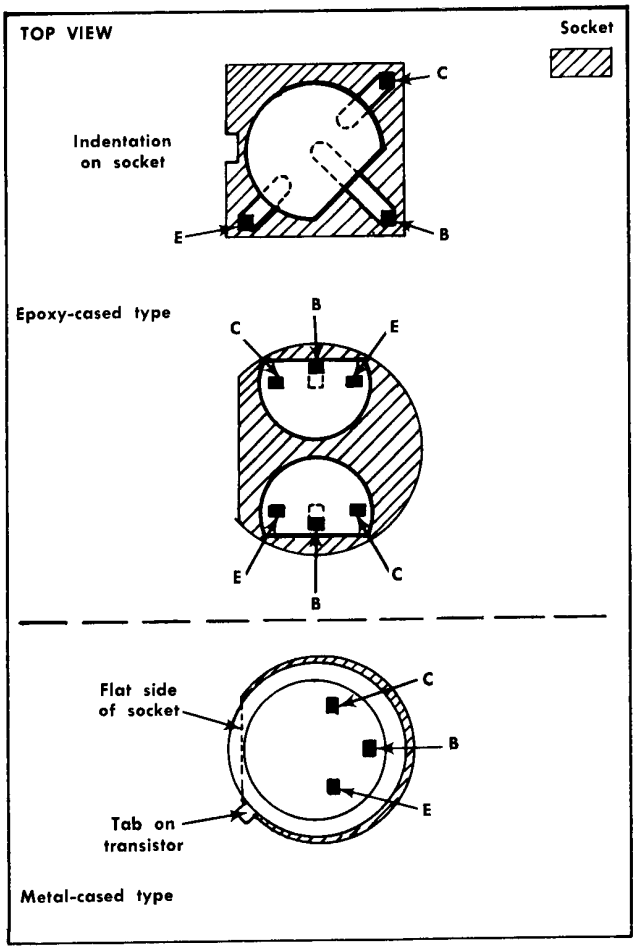


Fig. 5-6. Electrode configuration for socket-mounted transistors as viewed from the top of the transistor.

TABLE 5-6

Transistor Resistance Checks

Ohmmeter Connections[2]	Resistance Readings That Can Be Expected Using the R X 1 k Range
Emitter-Collector	High readings both ways (about 60 kΩ to around 500 kΩ).
Emitter-Base	High reading one way (about 200 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).
Base-Collector	High reading one way (about 500 kΩ or more). Low reading the other way (about 400 Ω to 2.5 kΩ).

[2]Test prods from the ohmmeter are first connected one way to the transistor leads and then the test prods are reversed (connected the other way). Thus, the effects of the polarity reversal of the voltage applied from the ohmmeter to the transistor can be observed.

out the circuit, the new transistor may immediately be damaged by some defect in the circuit.

CAUTION

Be careful when making measurements on live circuits. The small size and high density of components used in this instrument result in close spacing. An inadvertent movement of the test probes, or the use of oversized probes, may short between circuits.

Diode Checks

A diode can be checked for an open or shorted condition by measuring the resistance between terminals. With an ohmmeter scale having an internal source of about 1.5 volts, the resistance should be very high in one direction and very low when the leads are reversed.

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diode. Do not measure tunnel diodes with an ohmmeter; use a dynamic tester (such as Tektronix Type 575 Transistor-Curve Tracer).

Field Effect Transistors (FET)

Field effect transistors in the Type 3S2 should not be tested with an ohmmeter. Rather, if you suspect a dual FET (Q243A or Q243B, both in the same enclosure on the Vertical circuit board or Q543 on the Vertical circuit board), pull the unit out of the socket, rotate it 180° and re-insert it. Q243 can be installed with the guide pin pointing either up or down. Q543 can be installed with the guide pin pointing either front or back. If there is no change in circuit operation, both sections of the dual FET are probably good. Q243 and Q543 should be replaced if during a calibration procedure, the Smoothing Balance control cannot be properly adjusted.

Actual condition of either half of an FET can be checked using a Tektronix Type 575 Transistor Curve Tracer. Follow the lead identification of Fig. 5-7 when making connections at the curve trace sockets.

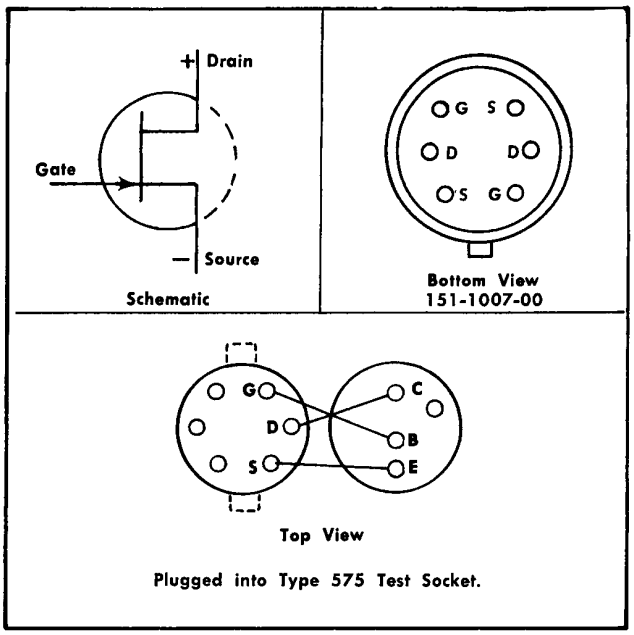


Fig. 5-7. Pin arrangements on FET's used in Type 3S2.

Set the curve tracer controls:

COLLECTOR SWEEP Controls	
PEAK VOLTS RANGE	20.0
POLARITY	+ (NPN)
PEAK VOLTS	Fully counterclockwise
DISSIPATION LIMITING RESISTOR	2 K
VERTICAL Controls	
CURRENT OR VOLTAGE	1 COLLECTOR MA
POSITION	Spot at lower left corner of graticule
HORIZONTAL Controls	
VOLTS/DIV	10 COLLECTOR VOLTS
POSITION	Spot at lower left corner of graticule
BASE STEP GENERATOR Controls	
REPETITIVE/OFF/SINGLE FAMILY	REPETITIVE
STEPS/FAMILY	Fully counterclockwise
POLARITY	—
STEPS/SEC	120 (up)
SERIES RESISTOR	Optional
STEP SELECTOR	.2 MA PER STEP

Slope Panel Controls

Center rotary switch	EMITTER GROUNDED

Connect a 1000 Ω (1% or 5%) ½ watt resistor between the B and E binding posts on the side of the sloping panel on which you plan to test the FET. This resistor develops a voltage bias for the Gate lead at 1 volt per mA base step current.

Since the leads of the FET are short, you can avoid bending them (with a chance of breakage) by building an adapter out of a spare transistor socket and wire leads to the sloping panel binding posts. Follow Fig. 5-7 when making connections.

151-1007-00

Zero-bias channel (Idss) is a minimum of 1.5 mA at 10 volts. Minimum Gm is 1000 μmhos at a drain current of 1 mA.

Major Circuit and Parts Locations

The remainder of this section includes photographs of sections of the Type 3S2. Major circuit areas are identified. All components mounted on circuit boards are identified by circuit numbers. All circuit board connections are identified by pin number or color code.

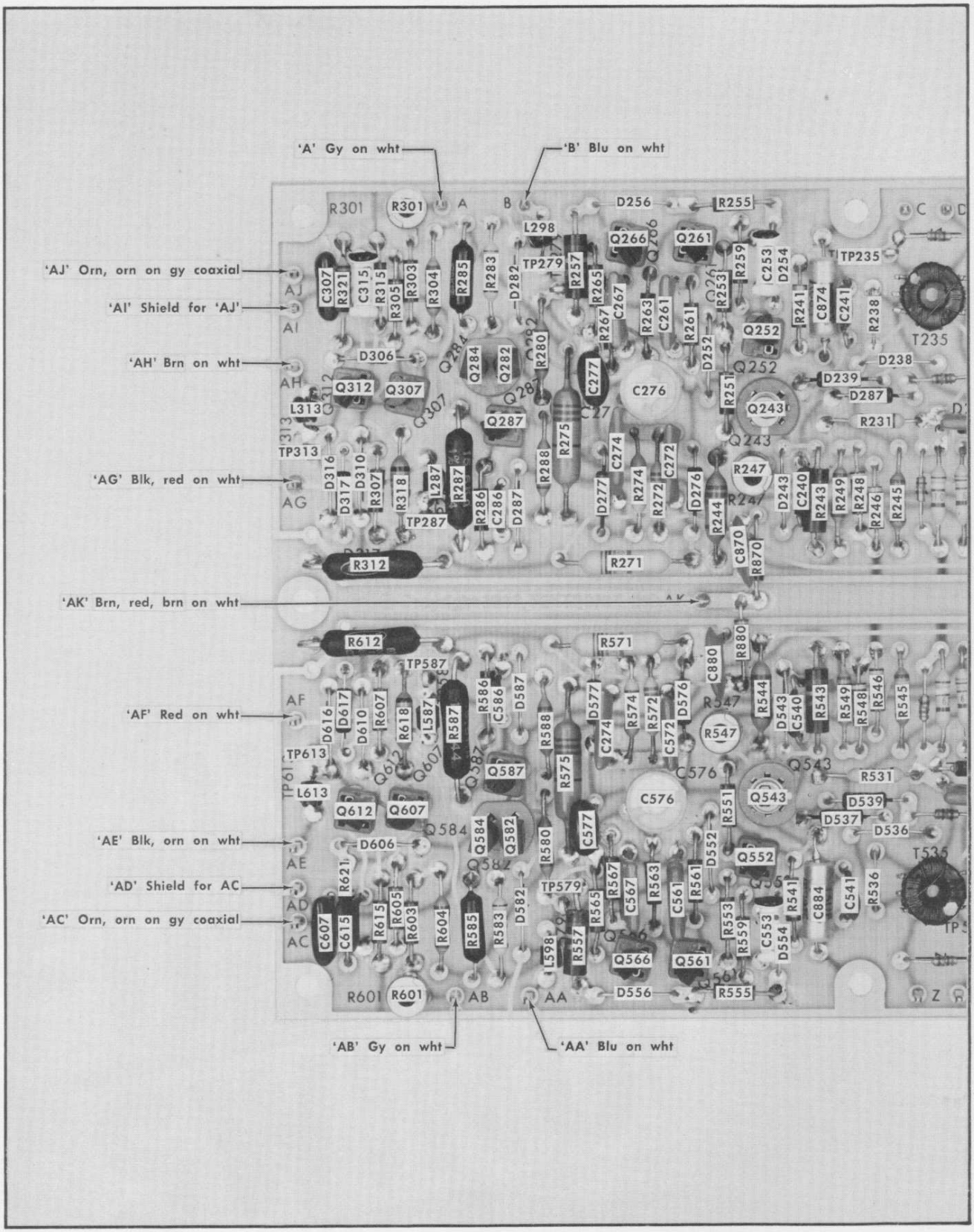


Fig. 5-8A. Vertical circuit board assembly, left.

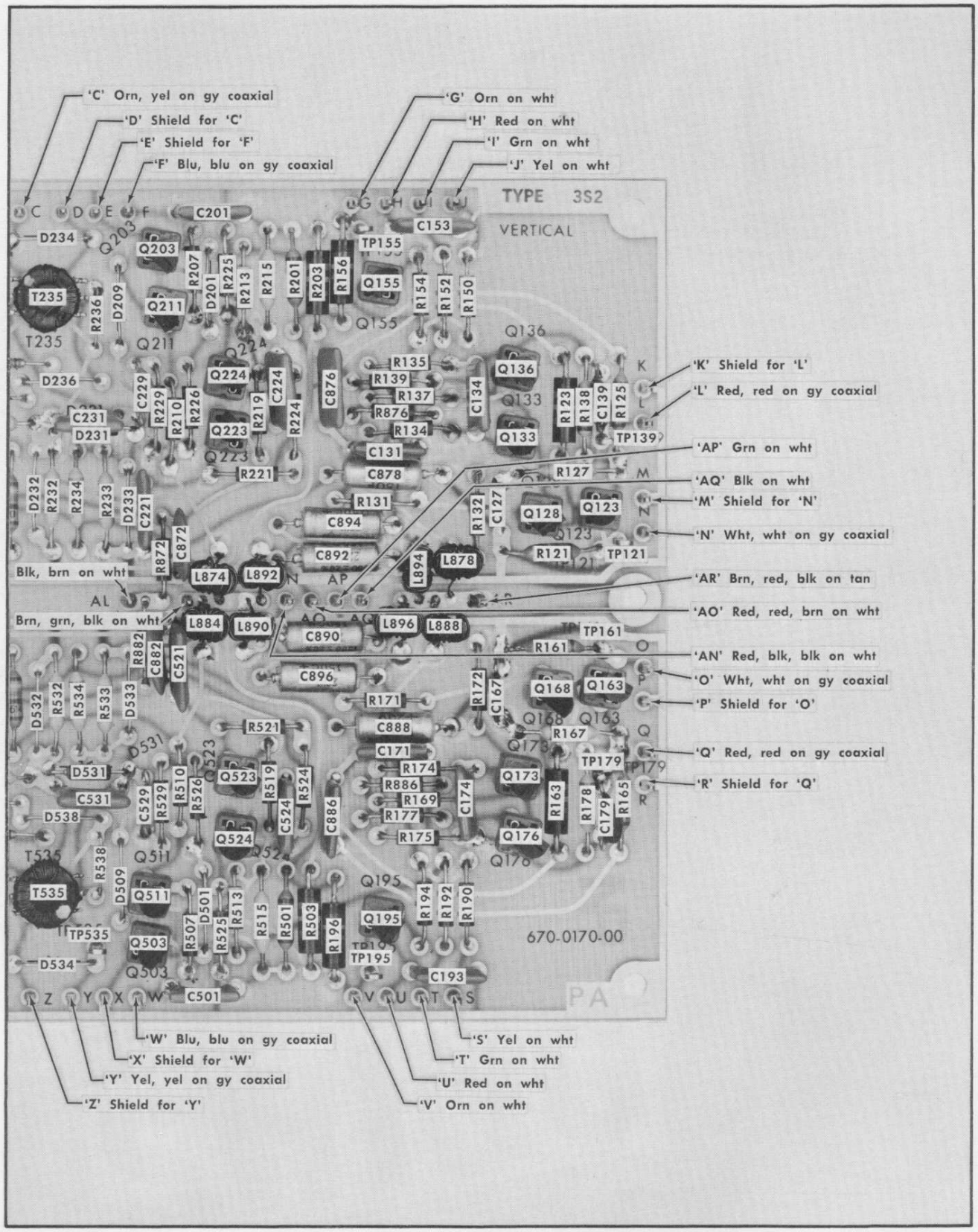


Fig. 5-8B. Vertical circuit board assembly, right.

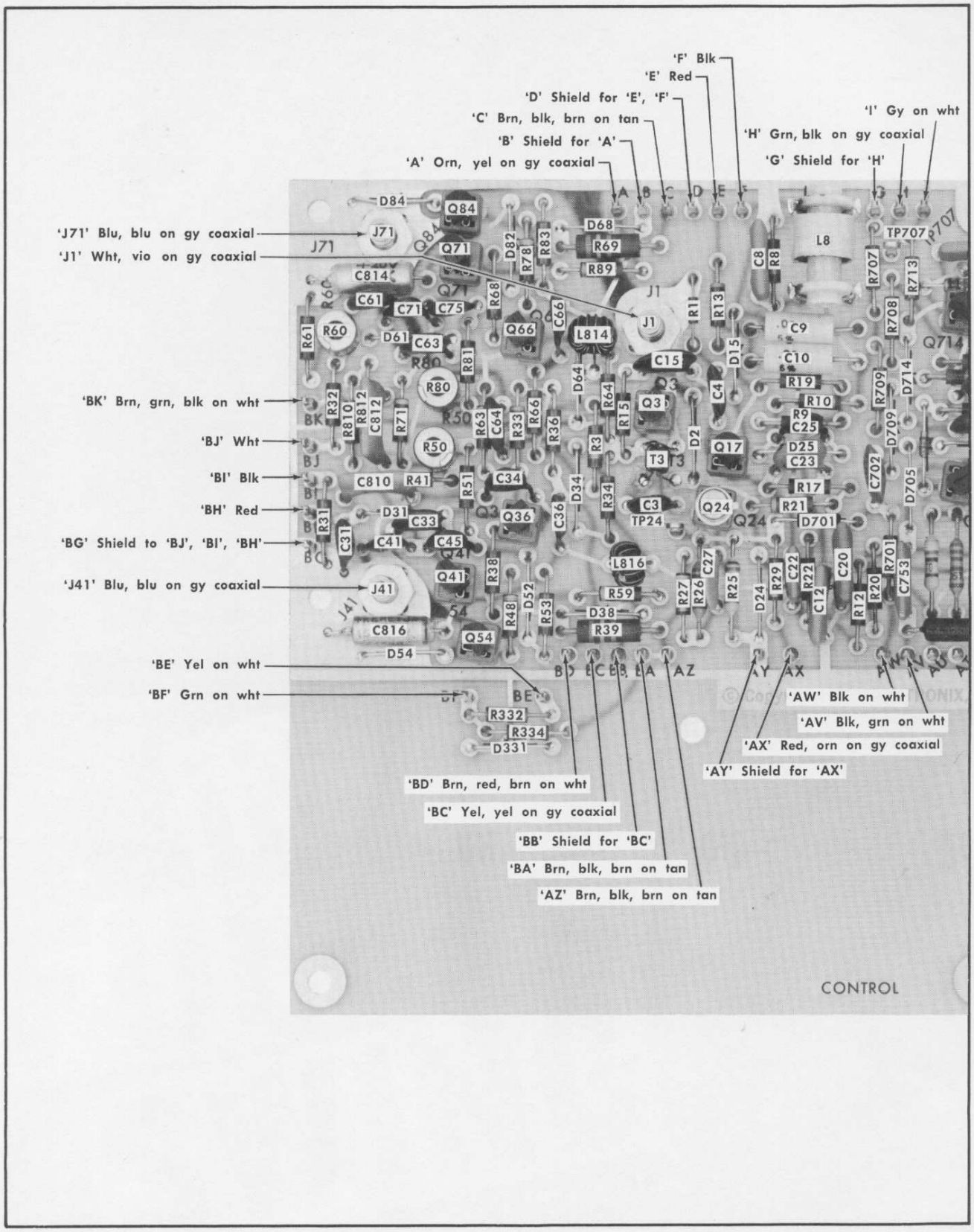


Fig. 5-9A. Control circuit board assembly, left.

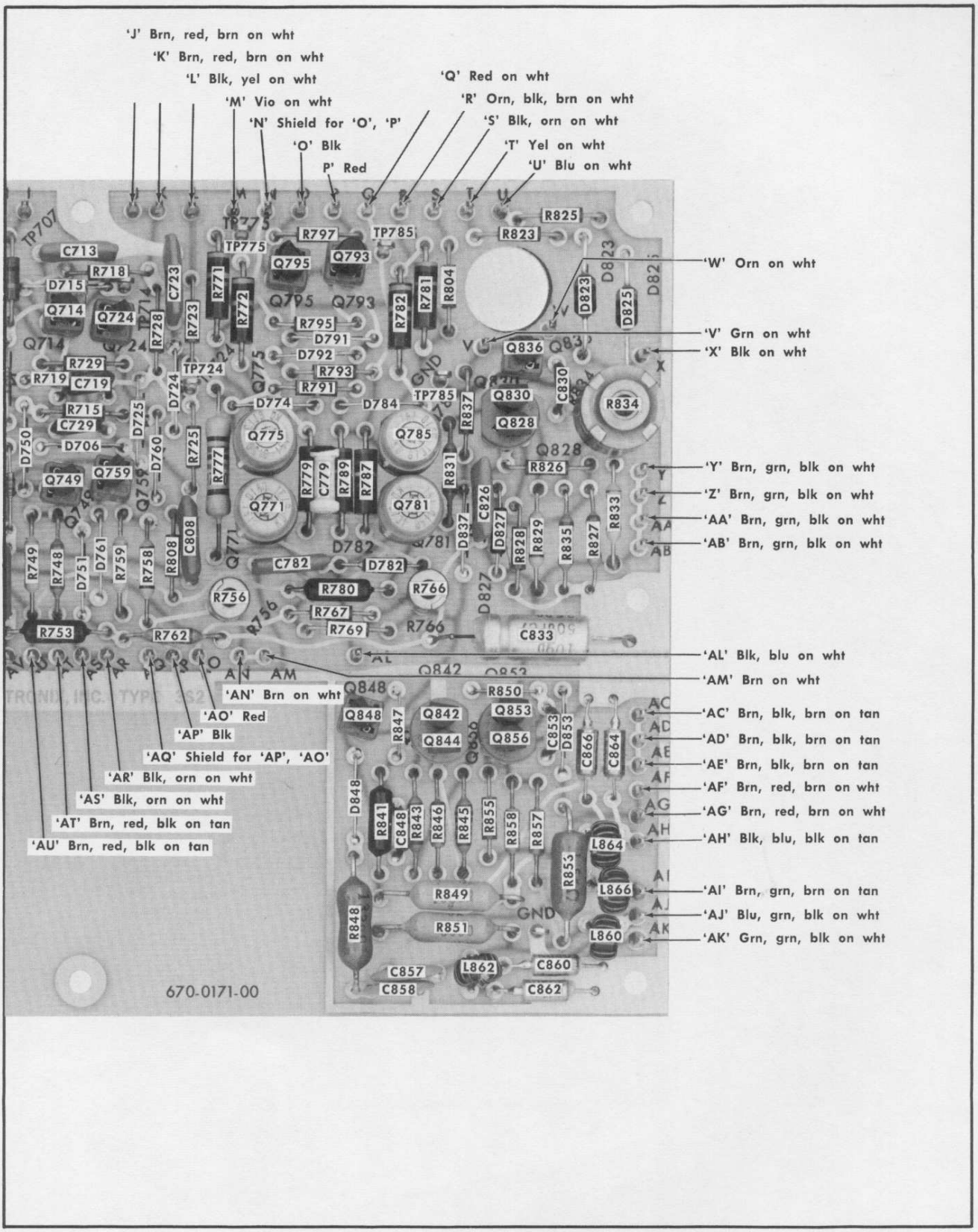


Fig. 5-9B. Control circuit board assembly, right.

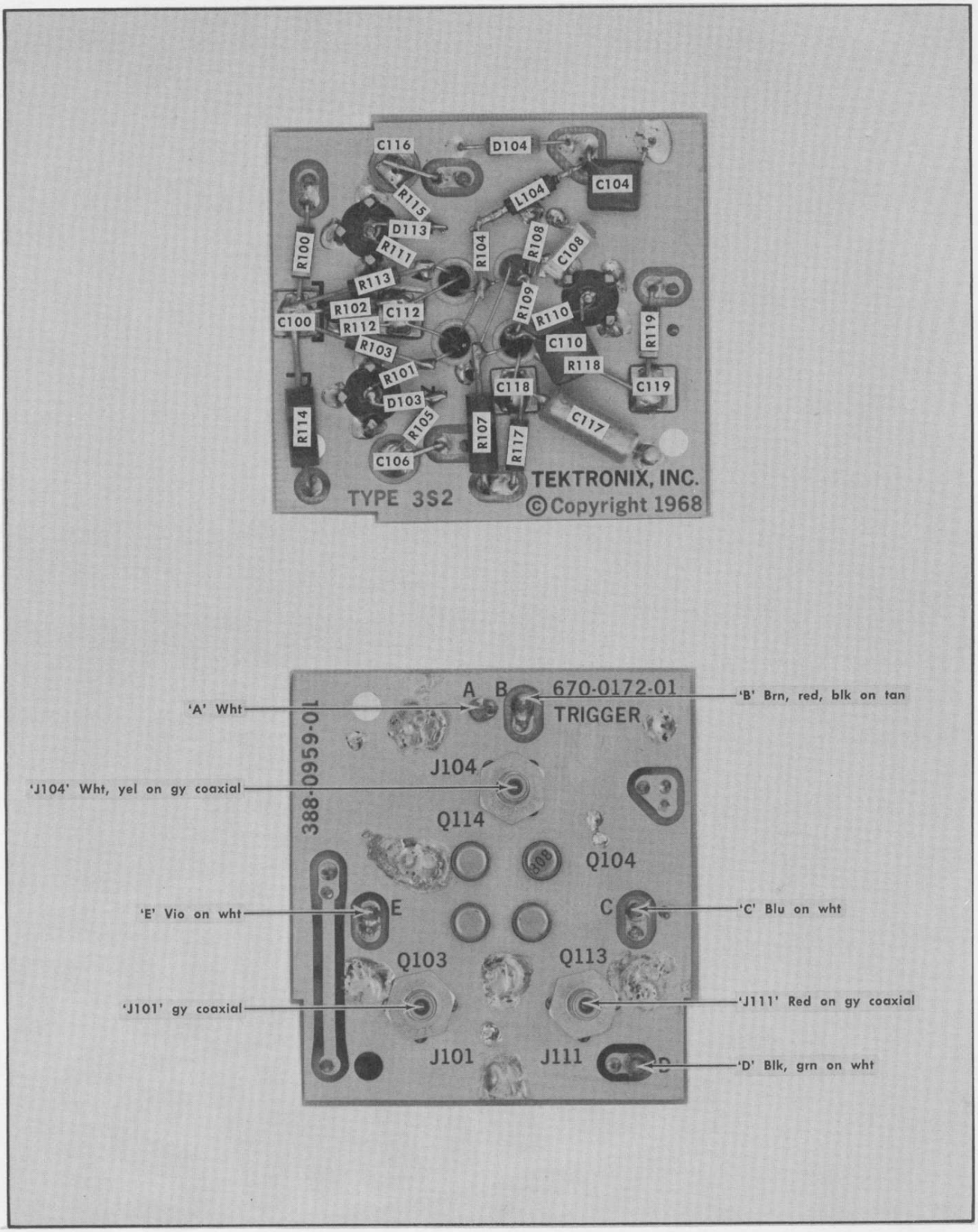
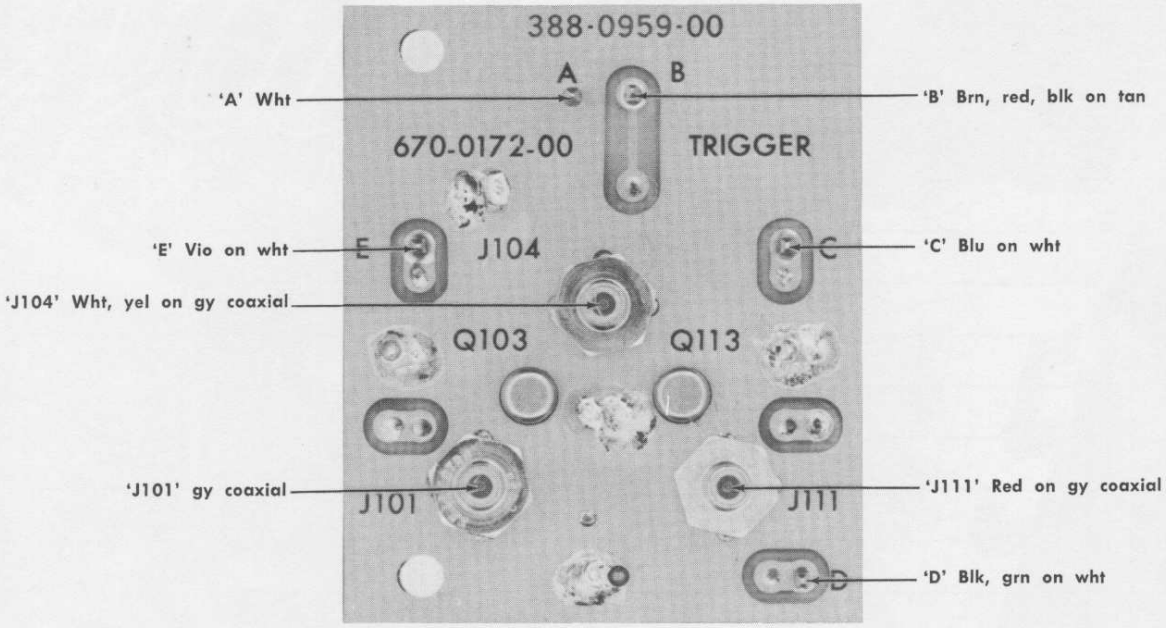


Fig. 5-10. Trigger circuit card assembly, SN B040250-up.



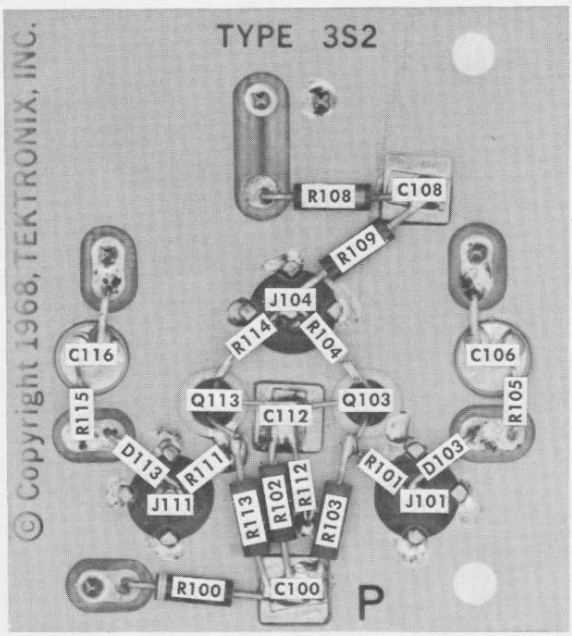


Fig. 5-11. Trigger circuit card assembly, SN B010101 - SN B030249.

NOTES

SECTION 6
PERFORMANCE CHECK / CALIBRATION

Change information, if any, affecting this section will be found at the rear of the manual.

General Information

The Performance Check is a method of rapidly checking the instrument's performance without internal adjustments. Failure to meet the requirements given in any check indicates the need for recalibration. Performance Check steps are those identified in the type style used in the sub-heading for this paragraph. Recalibration Steps are headlined in the style of the next sub-heading.

Any needed maintenance should be performed before proceeding with recalibration. The Recalibration steps restore the instrument to original performance standards stated in Section 1.

Completing the recalibration steps of this procedure matches the performance of one channel to the other, and enables both channels to operate with any S-series sampling head. It assures that the DOT RESPONSE controls and B DELAY control have sufficient electrical range for all heads. Either a Type S-1 or Type S-2 is used, with the Type S-1 recommended.

Equipment Required

The equipment listed following, or its equivalent, is required for recalibrating or checking the performance of the Type 3S2. To assure accuracy, all test equipment must be calibrated. If other equipment is substituted, it must meet or exceed the limits stated in the description. The first group of items includes those used in both the Performance Check and Calibration procedures. Following are additional items used only for one or the other of the two procedures.

1. Indicator oscilloscope such as Type 561A in which to operate the Type 3S2.

2. Type S-1 or S-2 Sampling Head.

3. 3T-Series sampling sweep unit, Type 3T2 recommended.

4. Test oscilloscope with vertical risetime of 20 ns or less and minimum deflection factor of 10 mV/div or less. For example, Tektronix Type 545B with Type W plug-in unit, or Type 585A with Type 82 plug-in.

5. 1× Probe, P6011. Tektronix Part No. 010-0193-00.

6. Square wave and pulse generator that produces 1 μs period square waves with 1.0 volt peak amplitude into 50 ohms or 0.5 volt peak amplitude into Type S-1 or 0.2 volt peak amplitude into Type S-2. Also required is a pulse of approximately 0.25 volt with $\leq$70 ps risetime. The Tektronix Type 284 will meet the above requirements, with attenuators, items 7 and 8.

7. 50 Ω 2× attenuator with GR 874 connectors, such as GR 874-G6. Tektronix Part No. 017-0080-00.

8. 50 Ω 5× attenuator with GR 874 connectors, such as GR 874-G14. Tektronix Part No. 017-0079-00.

9. 50 Ω coaxial cable with GR 874 connectors, such as 5 ns signal delay RG 58C/U cable, Tektronix Part No. 017-0512-00.

10. 50 Ω cable, approximately 4 feet long with BNC connectors. For example, RG 58C/U, Tektronix Part No. 012-0057-01. (This cable is supplied with the Type 284).

Recalibration Aids

Items in the list below are required for complete recalibration, but not for the Performance Check.

11. Flexible plug-in extension cable to operate the Type 3S2 outside the indicator oscilloscope. Tektronix Part No. 012-0066-00.

12. 10× probe, P6010. Tektronix Part No. 010-0188-00.

13. If a Type W Plug-In Unit is not available, a precision voltmeter is needed that can measure up to +50 or −50 volts with an accuracy of ±0.25%. John Fluke Model 801B meets the requirements.

14. Bench multimeter such as Simpson Model 262 or Triplett Model 630 NA.

15. Small-bit screwdriver for making adjustments.

16. Plastic tool for adjusting ferrite slug of L8, $^5/_{64}$ inch inside diameter hex core. Tektronix Part No. 003-0310-00, and 003-0307-00 for the handle.

17. Normalizer Head, optional for Unity Dot Response adjustment. Tektronix Calibration Fixture 067-0572-00. See step 14.

Performance Check Equipment

The items listed below are needed to complete the Performance Check, but are not required for recalibration.

18. 50 Ω 5× attenuator with BNC connectors. Tektronix Part No. 011-0060-00.

19. BNC female to GR adapter, Tektronix Part No. 017-0063-00.

20. 50 Ω Amplitude Calibrator. Output impedance 50 Ω; voltage range 0.012 to 1.2 volts square wave; accuracy within ±0.3%. Tektronix Calibration Fixture 067-0508-00.

21. Square wave generator, frequency 200 kHz and 20 Hz, to check Memory Slash. Tektronix Type 106 Square-Wave Generator.

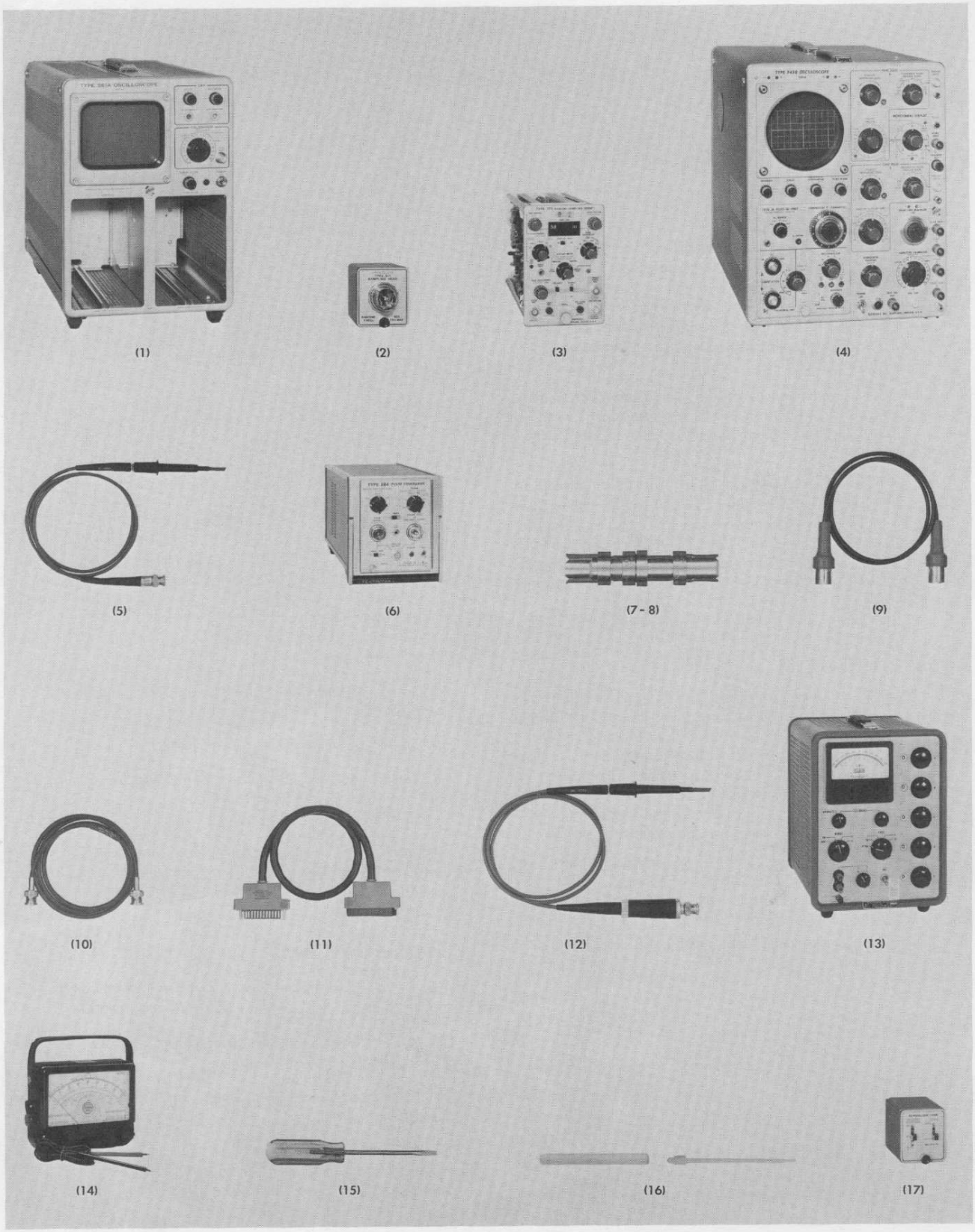


Fig. 6-1. Equipment required for Recalibration.

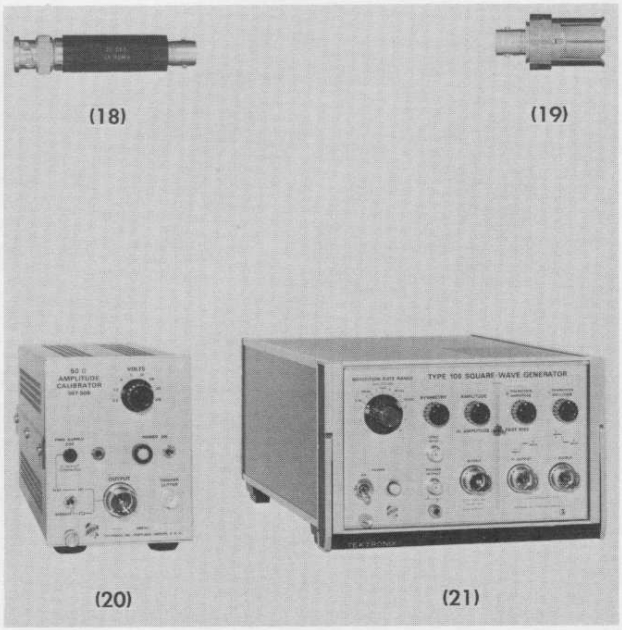


Fig. 6-2. Equipment required for Performance Check, not included in Fig. 6-1.

PERFORMANCE CHECK AND RECALIBRATION RECORD INDEX

The following abridged procedure may be used as a performance check or recalibration procedure guide by the experienced calibrator, or it may be used as a record. (Tektronix, Inc. authorizes reproduction of the abridged procedure by any user of the equipment). The step numbers and titles are identical to those used in the complete procedure. When the instrument meets the requirements in the Performance Check steps, the Type 3S2 will meet all Characteristics listed in Section 1.

Type 3S2 Serial No._____

Performance/Recalibration Date_____

Performed By_____

☐ 1. Check and Adjust Power Supplies — Page 6-6

+15 Volt value_____

+50 Volt value_____

−50 Volt value_____

☐ 2. Check Gate Generator and Sampling Head Avalanche Operation — Page 6-6

Blanking pulse width at 50% amplitude points _____ (2 μs to 4 μs)

☐ 3. Check Dot Response and Smoothing — Page 6-6

DOT RESPONSE control can be set for a unity loop gain display. Change of NORMAL-SMOOTH switch from NORMAL to SMOOTH changes loop gain from unity to $\leq$0.3.

☐ 4. Adjust Memory Gate Width Controls — Page 6-8

Maximum loop gain

☐ 5. Adjust Sampling Head Snap Off and Avalanche Volts Controls — Page 6-9

Near Maximum loop gain

☐ 6. Adjust Sampling Head Bridge Balance — Page 6-10

No trace movement with Units/Div switch change

☐ 7. Adjust Smoothing Balance Controls — Page 6-10

No trace shift as NORMAL-SMOOTH switch is changed.

☐ 8. Check Vertical Digital Accuracy (with Readout System) — Page 6-10

Accuracy within 3%

☐ 9. Adjust Digital Gain Controls — Page 6-10

Correct Digital Unit reading

☐ 10. Check Deflection Factor Accuracies Over Range of Units/Div Switch and Variable Control — Page 6-10

Variable control reduces deflection to 0.7 or less when control is turned CCW from CAL position, and 2.5 times or more increase in deflection when control is turned CW from CAL position.

☐ 11. Check Vertical Gain Change in SMOOTH — Page 6-11

Amplitude change must be 3% or less.

☐ 12. Adjust Vertical Centering, GAIN, and A-B Bal Controls — Page 6-11

Correct operation

☐ 13. Check Position Indicators and Position Control Range — Page 6-12

Position control will move trace +4 div and −4 div from graticule center; indicator neon will light showing direction trace is off graticule.

☐ 14. Adjust Both Channels for Unity Dot Response (Normalizer Head) — Page 6-12

2.5 volt peak to peak amplitude of signal at TP279 with mid-range (electrical center) setting of DOT RESPONSE control.

☐ 15. Adjust Both Channels for Unity Dot Response — Page 6-12

Correct balance between sampling head Gain control and Type 3S2 Memory Gain controls.

☐ 16. Check Interchannel Delay Range — Page 6-13

B DELAY control range is 10 ns and can match the B display to the A display.

☐ 17. Adjust A Delay Control Page 6-14

B DELAY control range is within +5 ns and —5 ns of A display.

☐ 18. Adjust Sampling Mode Repetition Rate Page 6-14

Non-Sampling 2B-, 3B- Series free-run rate is 95 kHz to 105 kHz.

☐ 19. Check Memory Slash Page 6-14

Vertical dot drift is ≤0.1 div when timing unit is triggered at 20 Hz.

☐ 20. Check Offset Out (Range and Accuracy) Page 6-14

Offset Out jack is 10 times the DC offset referred to the input ±2%.

☐ 21. Check A and B Vert Outputs Voltage Page 6-15

Output is 200 mV per displayed division ±3%.

☐ 22. Check Trig Out (Into 50 Ω) SN B040250-Up Page 6-16

Amplitude is approximately equal to the input signal and risetime is ≤2 ns (10% to 90%) with a 70 ps risetime pulse as the input signal. (These limits include performance of the sampling head trigger pickoff circuit.)

☐ 23. Check Trig Out (Into 50 Ω) SN B010101-SN B030249. Page 6-16

Amplitude is approximately 0.10 times the input signal and risetime of 0.6 ns or less (10% to 50%) with a 70 ps pulse as the input signal. (These limits include performance of the sampling head trigger pickoff circuit.)

PRELIMINARY PROCEDURE

Performance Check

Install the Type 3S2 (with a calibrated sampling head installed in Channel A) in the left side compartment and install the sampling sweep unit in the right side compartment of the indicator Oscilloscope.

Recalibration Procedure

a. Remove the indicator oscilloscope left side panel and connect the flexible interconnecting cable between the oscilloscope horizontally mounted connector, J11, and the Type 3S2.

b. Install the Type 3T2 (or other sampling sweep unit) into the indicator oscilloscope right side compartment.

c. Remove the case from the sampling head that is to be used in this procedure. Install the head (without case) into the Type 3S2 left side (Channel A) compartment. Make certain that both the coaxial (trigger) connector and the Sampler Board multi-terminal contacts are properly mated. Leave the Type 3S2 right side compartment vacant.

CAUTION

When the sampling head cover is off, turn off the oscilloscope power before installing the head. It is possible to blow out one of the blow-by compensating transistors by irregular contact sequence when installing a sampling head that has no case on.

Both Procedures

Make all power connections. Turn on the power to all equipment. Allow five minutes warmup time before proceeding. Set the controls as listed following Fig. 6-3.

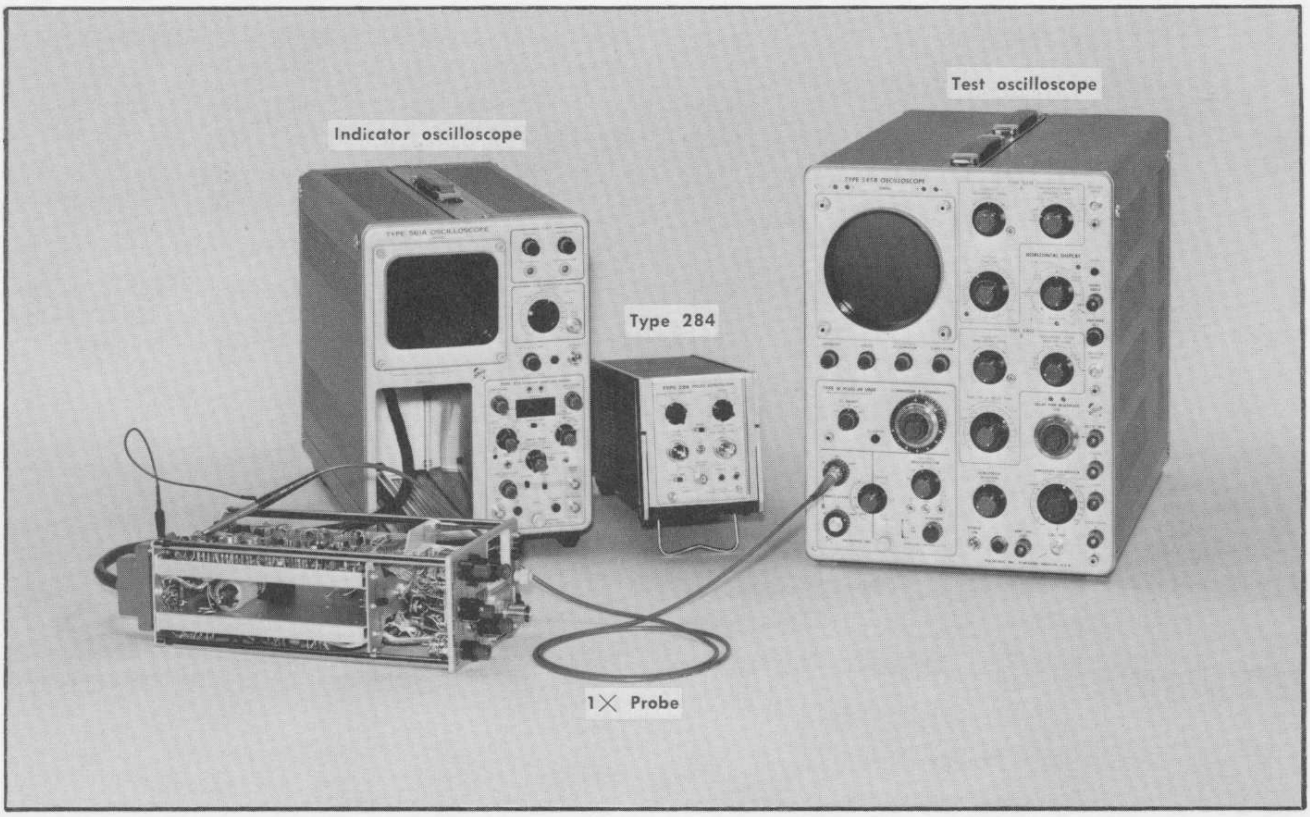


Fig. 6-3. Initial test equipment setup for steps 1 and 2.

Control Settings

Type 3S2 (Both channels)

Mode Switch	CH A
DOT RESPONSE	Midrange
Units/Div	100
VARIABLE	CAL
INVERT	Pushed in
A POSITION	Midrange, trace centered
B POSITION	Midrange
DC OFFSET	Midrange, Adjust to bring display onto screen in step 1
Internal Horiz Plug-In Compatibility	Sampling

Type 3T2

Display Mode	Normal
Start Point	With Trigger
Sweep Rate	500 ns/div
Range	10 μs
Time Magnifier	×2
Variable	Cal
Display Mag	×1
Time Position controls	Fully clockwise
Horiz Position	Midrange
Trig Sensitivity	10° clockwise into free run region
Recovery Time	Optional
Trigger Polarity	+
Trigger Source	Ext
Samples/Div	White dot 90° CCW from top center 1000 samples/sweep

Type 284

Mode	Square Wave
Period	1 μs
Square Wave Amplitude	1.0 V
Lead Time	75 ns

Test Oscilloscope

Sweep Rate	5 ms/div
Vertical	
With 1× Probe	10 mV/div, AC coupled
Triggering	+ Line

NOTE

If the Sampling Head being used is known to operate correctly, do not adjust any control at this time. If the sampling head is being recalibrated at the same time the Type 3S2 is being recalibrated, preset the Bridge Volts control fully clockwise; see Fig. 6-10. (The control will probably remain full clockwise in a Type S-1, and might be readjusted slightly in a Type S-2.)

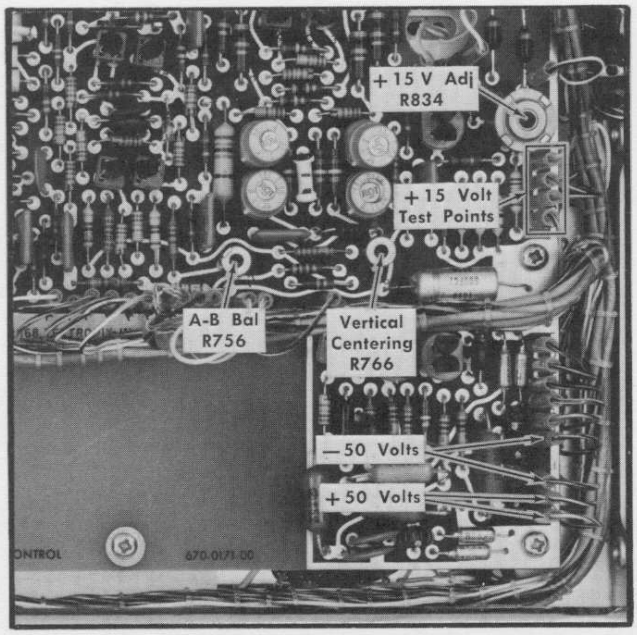


Fig. 6-4. Power supply test points and adjustment locations on right rear of Type 3S2.

1. Check and Adjust Power Supplies

a. Refer to Fig. 6-4 to locate the power supply test points and the +15-Volt adjustment. Location is on the instrument right rear side.

b. Use the Type W Unit with a 1× probe or a precision voltmeter. Connect the probe to the test points in succession.

c. CHECK—Power supplies within tolerance listed as follows:

Tolerance

Voltage	%	Volts
+15 V	±1%	±0.15 V
+50 V	±2%	±1 V
—50 V	±1%	±0.5 V

d. ADJUST—+15 Volts control, R834, for +15 volts.

2. Check Gate Generator and Sampling Head Avalanche Operation

a. Change the test oscilloscope probe from 1× to 10×, and reset the controls for:

Sweep rate	20 μs/div
Vertical With 10× Probe	20 V/div, AC Coupled
Triggering	+ Internal

b. Connect the test oscilloscope 10× Probe ground clip to the Type 3S2 frame so the tip can reach (Test Point) TP 24 on the instrument right side; see Fig. 6-5A. The blanking pulse signal at TP24 should be similar to that shown in Fig. 6-5C.

c. Center the test oscilloscope display vertically and increase the sweep rate to 1 μs.

d. Check that the blanking pulse duration at the 50% amplitude points is between 2 μs and 4 μs (2 to 4 divisions).

e. Reset the test oscilloscope sweep rate to 20 μs.

f. Connect the probe ground clip so the tip can be connected to Q69 emitter (Sampling Head); see Fig. 6-5B. The signal should be similar to that shown in Fig. 6-5D.

NOTE

The test points checked in step 2 are of particular value if you cannot obtain a free-run trace. If there is no signal at TP24, check that the sampling sweep unit is actually free running.

3. Check Dot Response and Smoothing

Requirement—NORMAL: DOT RESPONSE control can be set for a unity dot response display when the NORMAL-SMOOTH switch is at NORMAL.

SMOOTH: Dot response is $\leq$0.3 when the sampling sweep unit operates in a normal sequential dot sampling process (Type 3T2 Start Point switch at With Trigger).

a. Set the Units/Div switch to 100 with S-1; to 50 with S-2. Set the Type 284 to deliver 1 μs square waves at 1.0 volt. Install the appropriate 50 Ω attenuator listed in Table 6-1 between the signal cable and the Type 284 output connector.

b. Set the sampling sweep unit for 500 ns/div (0.5 μs/div). Obtain a double triggered display on the indicator oscilloscope by free running the time base and adjusting the Recovery Time control. The display should be similar to any one in Fig. 6-7.

c. Set the DOT RESPONSE control to unity loop gain as in Fig. 6-7A.

d. Change the NORMAL-SMOOTH switch from NORMAL to SMOOTH.

e. Check that the display is less than 1.7 divisions with the Type S-1 or less than 1.3 division with the Type S-2.

f. Reset the switch to NORMAL.

TABLE 6-1

Attenuator To Be Used With Type 284

Sampling Head	Attenuator	P-P Signal Desired at Input	Type 284 Square Wave Amplitude
S-1	2×	0.5 V	1.0 V
S-2	5×	0.2 V	1.0 V

4. Adjust Memory Gate Width Controls ◐

a. Leave the 10× Probe on the test oscilloscope vertical input. Connect the 1× Probe to the test oscilloscope External Trigger input connector. Reset the controls for:

Sweep Rate	0.1 μs/div
Vertical	
With 10× Probe	0.1 V/div
Triggering	+ External

b. Install a 50 Ω attenuator onto the Type 284 Square Wave or Sine Wave Output connector (see Table 6-1). Place a coaxial cable (with GR-874 connectors) between the attenuator and the sampling head input connector.

c. Place a coaxial cable (with BNC connectors) between the Type 284 Trigger Out connector and the sampling sweep unit External Trigger input connector (on the Type 3T2 this refers to the 50 Ω input).

d. Refer to Fig. 6-6 for Type 3S2 test points and controls located on the instrument left side. Connect the test oscilloscope external trigger 1× probe tip to TP235. Connect the vertical 10× probe tip to TP121.

e. Adjust the Type 3S2 Trigger Sensitivity and Recovery Time controls for a double-triggered indicator oscilloscope display similar to any in Fig. 6-7. The test oscilloscope display should be like one of the waveforms shown in Fig. 6-8 when the sampling head is a Type S-1 and like Fig. 6-9A if the sampling head is a Type S-2. (It is recommended that a Type S-1 be used if available.)

f. Locate R80, the Channel A Memory Gate Width Control (see Fig. 6-5) and adjust it for an indicator oscilloscope display of maximum loop gain. The test scope display is at maximum amplitude for maximum loop gain.

g. Turn off the oscilloscope power and move the sampling head into the Type 3S2 Channel B compartment. Turn the oscilloscope power back on. Move the test scope 10× probe tip to TP161. Change the Type 3S2 Mode switch to CH B and obtain a display. Locate R50, the channel B Memory Gate Width control (see Fig. 6-5) and adjust it for maxi-6-5) and adjust it for maximum loop gain.

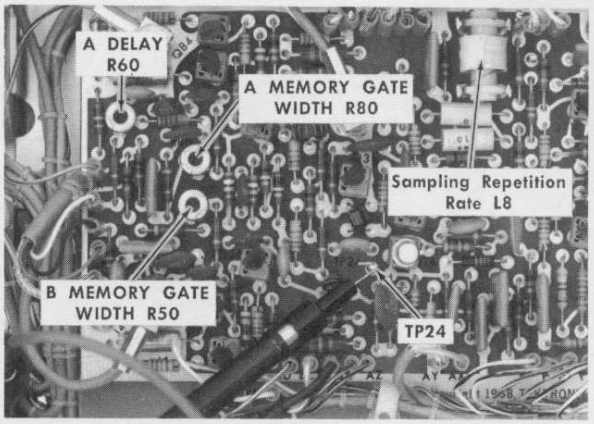
5. Adjust Sampling Head Snap Off and Avalanche Volts Controls ◐

NOTE

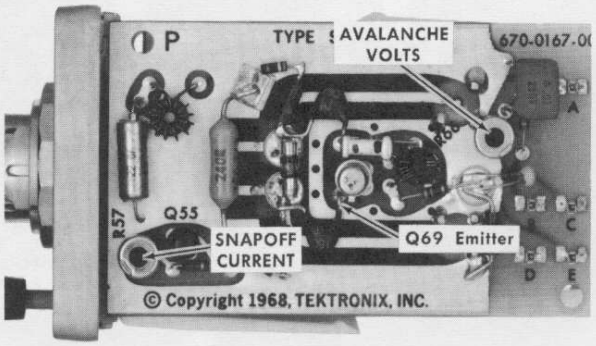
If the sampling head used in this procedure is operating properly, and there is no intent to recalibrate the head, disregard this step. This step is to be used only when the sampling head also needs calibration.

a. Continue with the double-triggered display obtained in step 4, and leave the test oscilloscope probe on TP161.

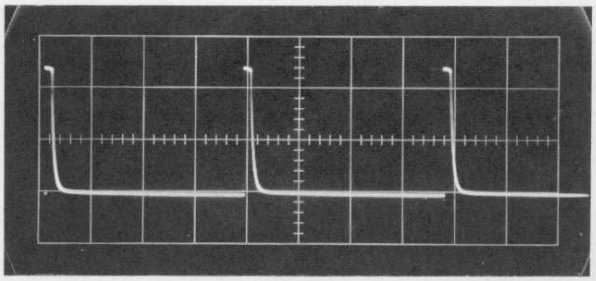
b. Refer to Fig. 6-5B for control locations. Adjust the Snap Off Current control, R57. The test oscilloscope display amplitude will change. Adjust R57 for a test oscilloscope display near the maximum amplitude obtainable (near maximum loop gain). The final position of R57 is decided thus; Note that the Type 3S2 display moves up and down when



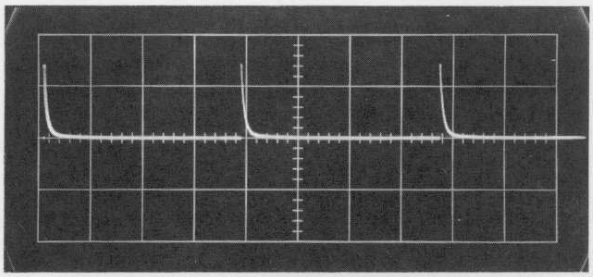
(A) 10× Probe connected to TP24.



(B) Sampling Head controls, on right side.



(C) TP24 signal. 20 μs/div. 20 V/div.



(D) Q69 emitter signal 20 μs/div. 20 V/div.

Fig. 6-5. Step 2 checks.

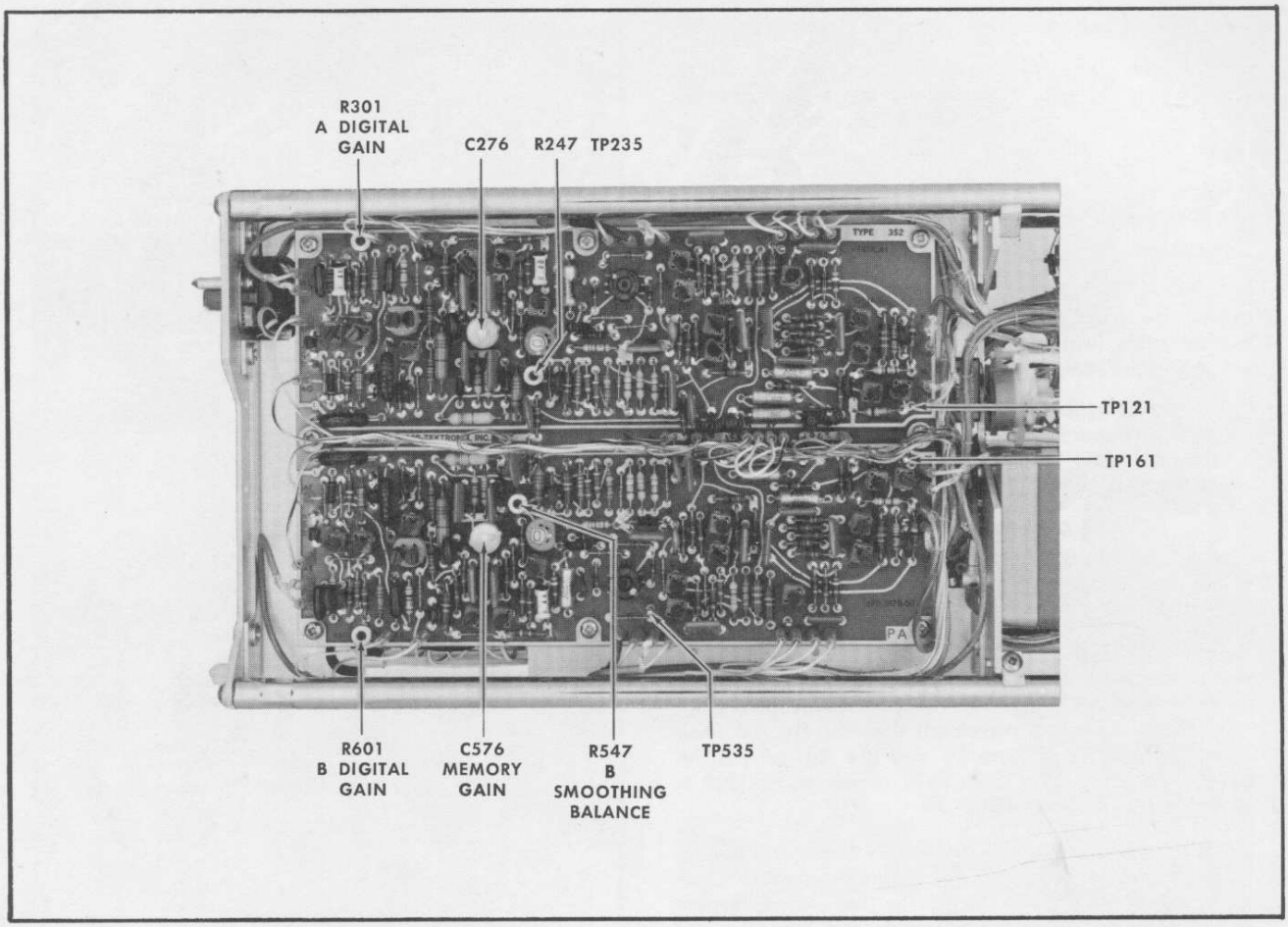


Fig. 6-6. Type 3S2 Left side test points and adjustments.

turning R57; if a maximum vertical up or down excursion occurs near a point where the test oscilloscope display amplitude is maximum, leave R57 at that Type 3S2 maximum excursion point.

c. Move the test oscilloscope probe to the emitter of the sampling head avalanche transistor, Q69 (shown in Fig. 6-5B). Adjust the Avalanche Volts control, R66, slightly clockwise and note that the avalanche circuit operation becomes unstable. Return R66 about $\frac{1}{8}$ turn counterclockwise from the point of instability.

d. Interaction between the two controls may require that the above two adjustments be repeated.

NOTE

Step 5 adjustments do not assure proper sampling noise and risetime calibration. Those adjustments are described in the sampling head instruction manual recalibration procedure.

6. Adjust Sampling Head Bridge Balance Controls

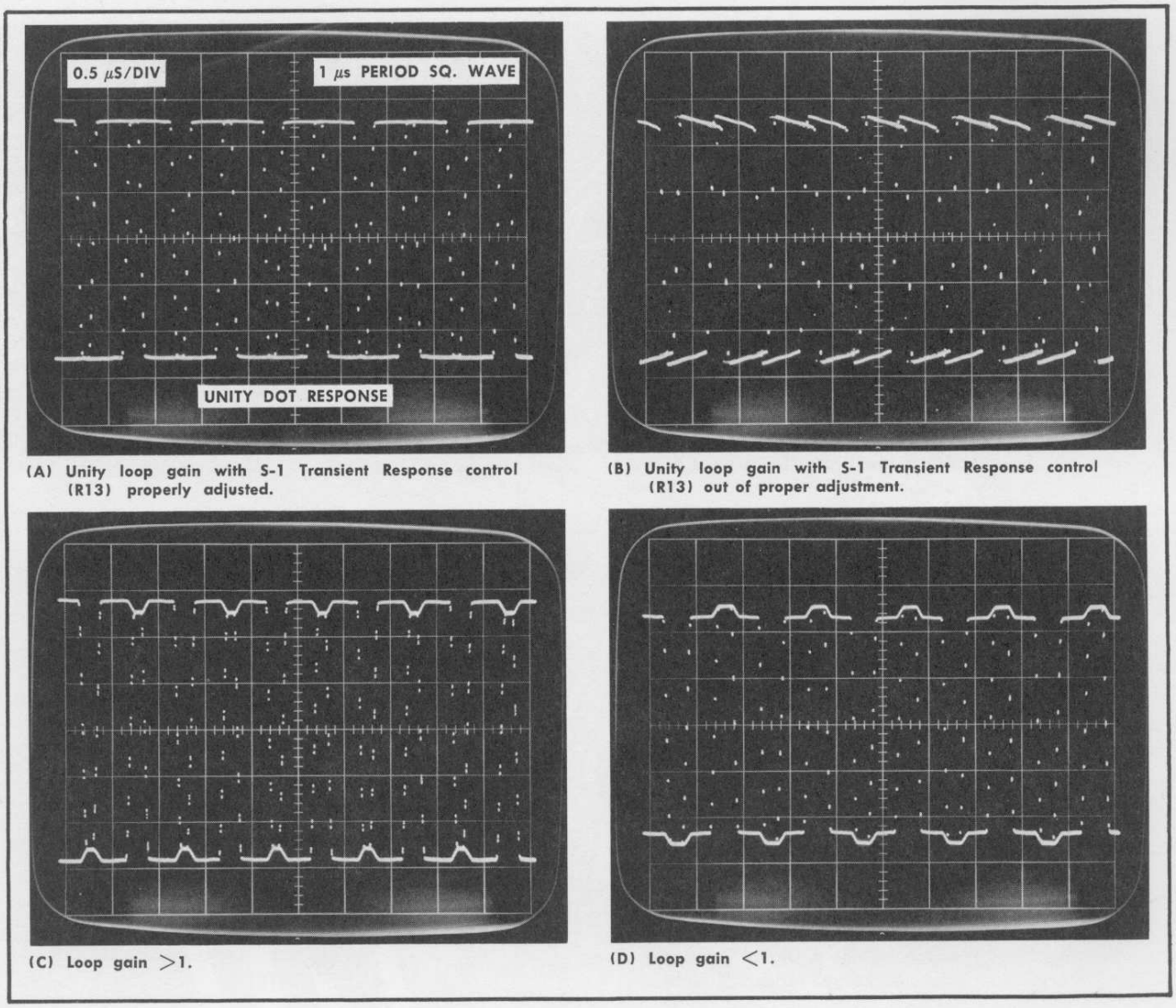
a. Disconect the signal cable from the Type 284. Leave the cable connected to the sampling head. Leave the sampling sweep unit triggered from the Type 284 for a displayed no-signal trace.

b. Adjust both DC OFFSET controls so they deliver zero volts to the front panel OFFSET OUT jacks.

c. Change the Units/Div switch from 200 to 2 and adjust Bridge Bal R22, (shown in Fig. 6-10) for no more than one division of trace movement as the switch is changed from 200 to 2.

7. Adjust Smoothing Balance Controls

a. Disconnect the cable from the Type 284. Leave the cable connected to the sampling head. Leave the sampling sweep unit triggered from the Type 284 for a displayed no-signal trace.



(A) Unity loop gain with S-1 Transient Response control (R13) properly adjusted.

(B) Unity loop gain with S-1 Transient Response control (R13) out of proper adjustment.

(C) Loop gain >1.

(D) Loop gain <1.

Fig. 6-7. Type 3S2/S-1 waveforms when signal is 1 μs period square wave. Timebase was double triggered to show dot response.

b. Adjust both Type 3S2 DC OFFSET controls so they deliver zero volts to the front panel OFFSET OUT jacks.

c. Turn the NORMAL-SMOOTH control to SMOOTH and note the trace shift. If the trace moves vertically, readjust the Channel B SMOOTHING BALANCE control R547, (shown in Fig. 6-6) until there is no trace movement as the NORMAL-SMOOTH control is switched between its two positions.

d. Turn off the oscilloscope power and move the sampling head back to Channel A; turn the oscilloscope power back on. Readjust the Channel A SMOOTHING BALANCE control R247, shown in Fig. 6-6, until there is no trace shift as the NORMAL-SMOOTH control is switched between its two positions.

NOTE

The Type 3S2 Smoothing Balance control cannot be correctly adjusted if the sampling head Bridge Bal control has not been adjusted first. It is best to repeat both steps 6 and 7 to assure that the Type 3S2 Smoothing Balance control is correctly adjusted.

8. Check Vertical Digital Accuracy (with Readout System)

Requirement—The Type 3S2 will permit a Tektronix digital readout system to make voltage measurements with an accuracy of ±3%.

a. Connect the Type 284 Square Wave Output to the sampling head input through a 50 Ω coaxial cable. Set the Type 3S2 Units/Div switches to 200 and check that the VARIABLE controls are at CAL. The square wave amplitude is now 1.0 volt, ±0.5% when the sampling head input resistance is 50 Ω.

b. Set the Type 284 Period switch for 10 μs square waves. Set the sampling unit sweep rate to 2 μs/div.

c. Set the digital unit controls to measure voltage from Channel A, along a rising slope waveform.

d. CHECK—Digital readout is between 0.965 V and 1.035 V.

e. Change the sampling head to Channel B and the Mode switch to CH B. Set the digital unit to read voltage from Channel B.

f. CHECK—Digital readout is between 0.965 V and 1.035 V.

9. Adjust Digital Gain Controls ◐

NOTE

This step applies only if the Type 3S2 is used with a Type 567/6R1A or Type 568/230 Digital System and if R301 or R601 have been replaced or otherwise misadjusted. If this step does not apply, then DO NOT adjust R301 or R601 from the factory adjustment positions.

a. Turn off indicator oscilloscope power, remove the flexible extension cable, and install the Type 3S2 in the compartment, (or use 2 flexible extensions). Turn the instrument power on.

b. Remove any attenuator that is in the signal cable between the Type 284 and the sampling head input. The square wave amplitude is now 1.0 volt, ±0.5% when the sampling head input resistance is 50 Ω. Set the Type 284 Period switch to deliver 10 μs square waves. Set both Type 3S2 units/div switches to 200 and obtain a display similar to Fig. 6-8. Check that both VARIABLE controls are at CAL. Set the digital unit controls to measure voltage from Channel A, along a rising slope waveform.

c. Refer to Fig. 6-6 and locate the A Digital Gain control, R301. Adjust R301 until the digital unit reads 1.00 volts.

d. Move the Sampling Head to Channel B. Set the Type 3S2 Mode switch to CH B.

e. Locate the B Digital Gain control, R601. Change the digital unit to read voltage from Channel B. Adjust R601 until the digital unit reads 1.00 volts.

NOTE

Changing either Digital Gain control requires that the front panel GAIN control and the A-B Bal control be adjusted as described in step 12.

f. Turn the power off, reinstall the Type 3S2 on the extension and turn the power on.

10. Check Deflection Factor Accuracies Over Range of Units/Div Switch and Variable Control Range

Requirement—All calibrated deflection factors will produce displays with amplitude accuracy of ±3% (when the VARIABLE control is at CAL). VARIABLE control fully counterclockwise reduces display amplitude to 70% or less of calibrated amplitude. VARIABLE control fully clockwise increases display amplitude to 250% or more of calibrated amplitude.

a. Set the Type 3S2 Units/Div switch to 200 and apply 1.2 volts from the 50 Ω Amplitude Calibrator (item 20, equipment required) to the Channel B Input through a 50 Ω coaxial cable and connect a coaxial cable from the Amplitude Calibrator Trigger Output connector to the sampling sweep unit external Trigger Input 50 Ω connector.

b. Set the sampling sweep unit for a sweep rate of 10 μs/div, and obtain a stable triggered display.

c. Adjust the front panel GAIN control for a display amplitude of 6 divisions.

d. Check all positions of the attenuator switch as listed in Table 6-2 for a 6 division display amplitude within a tolerance of ±0.18 div.

TABLE 6-6

Units/Div	50 Ω Amplitude Calibrator
200	1.2 V
100	.6 V
50	.3 V
20	.12 V
10	.06 V
5	.03 V
2	.012 V

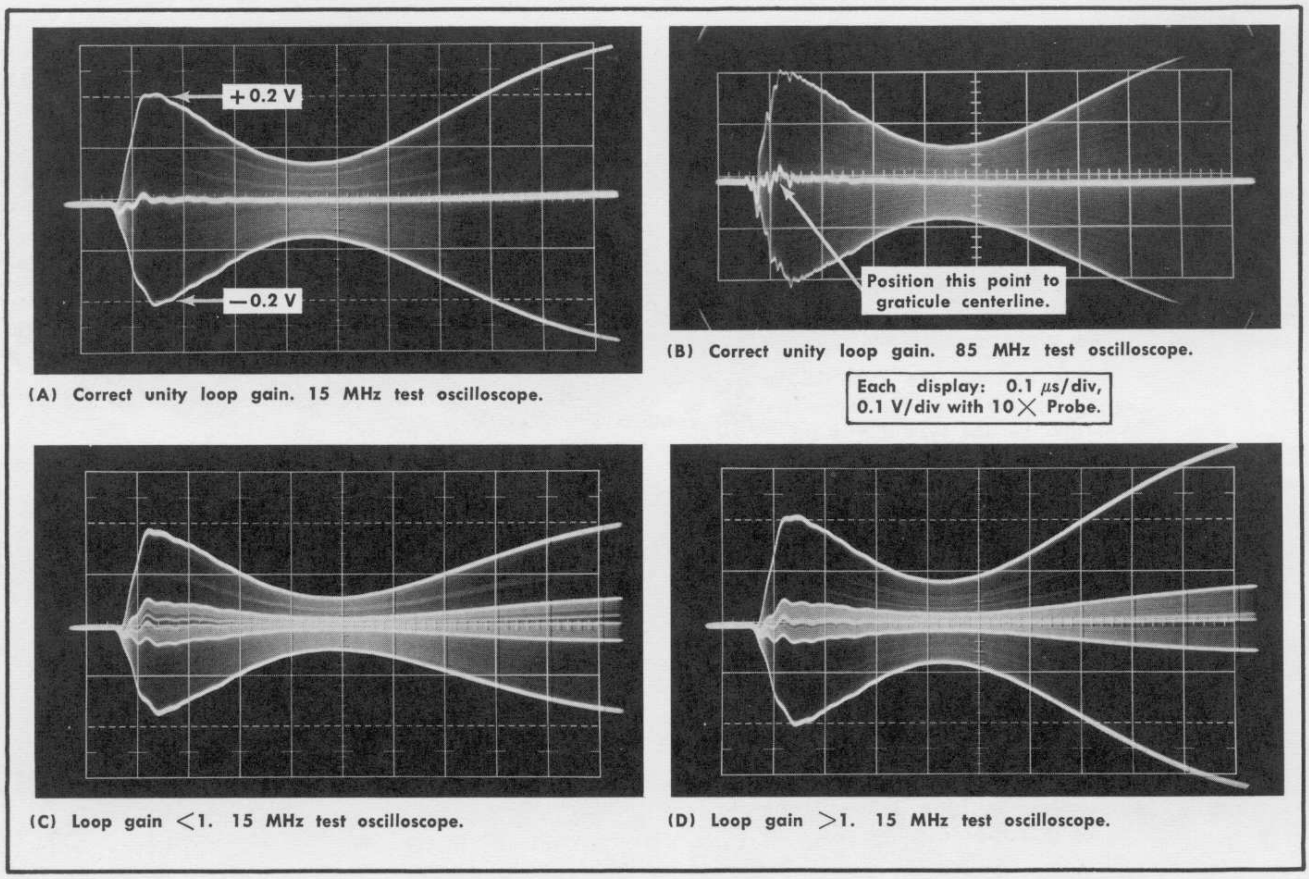
NOTE

Record deflections in each case. If one range is above tolerance, GAIN can be reduced to bring all ranges within tolerance without need for checking Forward and Feedback attenuator resistor values.

e. Set the Units/Div switch to 200 and the 50 Ω Amplitude Calibrator to .06 volts. Display amplitude is 3 divisions.

f. Turn the VARIABLE control fully counterclockwise from the detent setting and check the display amplitude for 2.1 divisions or less.

g. Turn the VARIABLE control fully clockwise from the detent setting and check the display amplitude for 7.5 divisions or more.



(A) Correct unity loop gain. 15 MHz test oscilloscope.

(B) Correct unity loop gain. 85 MHz test oscilloscope.

(C) Loop gain <1. 15 MHz test oscilloscope.

(D) Loop gain >1. 15 MHz test oscilloscope.

Fig. 6-8. Test oscilloscope displays of Type S-1 output signal (at TP121 or TP161) when externally triggered by Memory Gate signal. Timebase unit was double triggering on 1 μs period square wave.

h. Return the VARIABLE control to the detent (CAL) position.

i. Change the sampling head to A Channel and the Mode switch to CH A. Repeat the check for the A Channel.

11. Check Vertical Gain Change in SMOOTH

Requirement—Pulse amplitude change must not be more than —3% when NORMAL-SMOOTH switch is changed from NORMAL to SMOOTH while Units/Div switch is at 200. (This check cannot be made at any other setting of the Units/Div switch, because the gain change will not show between Units/Div switch positions of 50 to 2.)

a. Connect the Type 106 Trigger Output to the sampling sweep unit 50 Ω Trigger Input through a 50 Ω coaxial cable and 5× attenuator.

b. Set both Units/Div switches to 200 and set the Type 106 for a 200 kHz Repetition Rate. Connect the Type 106 Hi Amplitude Output to the Channel A sampling head input connector through a 50 Ω coaxial cable and 5× attenuator and adjust the amplitude control for a display amplitude of 5 divisions.

c. Set the sampling sweep unit sweep rate to 1 μs/div and the Samples/Div control to the 9 or 10 o'clock position (at least 20 dots per division). Obtain a stable triggered display.

d. Change the NORMAL-SMOOTH switch to the SMOOTH position.

e. Check that the peak amplitude does not decrease more than 3% (0.15 division of the 5 division display). Ignore any rolloff at the leading portion of the display.

f. Repeat the check for the B Channel.

If either channel display amplitude changes more than —3% the Memory Amplifier internal gain (open loop gain) is lower than it should be. Change Q243 and/or Q252. If the gain is still low, check the value of R244 and/or R257.

12. Adjust Vertical Centering Control, R766; GAIN Control, R764; and A-B Control, R756

a. Leave the sampling head in Channel B. Disconnect the signal cable at the source (not at the sampling head).

b. With no signal to the sampling head, obtain a trace.

c. Use the bench multimeter between the chassis and Channel B front panel Vertical Output jack. Set the meter to read volts, and adjust the Channel B DC OFFSET control for a reading of zero volts. This sets the B Channel Memory circuit output voltage to zero.

d. Set the multimeter to read at least +10 volts. Connect the meter negative lead to the chassis and the positive lead to the arm terminal of the B POSITION control. Set the B POSITION control for a multimeter reading of +7.5 volts.

e. Refer to Fig. 6-4 for the location of the Vertical Centering control R766; and adjust R766 until the indicator oscilloscope trace is at the graticule centerline.

f. Connect the cable between the Type 284 and the sampling head input. Set the sampling sweep unit for a sweep rate of 0.5 μs/div. Set the Type 284 to deliver 10 μs square waves at 1.0 volt. Obtain a display similar to Fig. 6-11, normally triggered (not double triggered).

g. Adjust the front panel GAIN control for a 5 division display. If the control is turned very far, recheck the Vertical Centering adjustment.

h. Move the sampling head to Channel A, and set the Type 3S2 Mode switch to CH A.

Refer to Fig. 6-4 for location of the A-B Bal control, R756. Adjust R756 for a 5 division display.

NOTE

This step assures that the Type 3S2 will operate in any 560 series indicator oscilloscope.

13. Check Position Indicators and Position Control Range

Requirement—Up POSITION indicator neon lights, and down POSITION indicator neon is dark, when CRT beam is above the graticule. Down POSITION indicator lights and up POSITION indicator is dark when CRT beam is below the graticule.

POSITION control will position a free run trace at least +5 div and −5 div from its midrange setting.

a. Set the sampling sweep unit triggering controls for a free-running trace and the Type 3S2 POSITION control to place the trace above the top graticule line.

b. Check that the up indicator is on and the down indicator is off.

c. Position the trace below the bottom graticule line.

d. Check that the down indicator is on and the up indicator is off.

e. Set the POSITION control to midrange (dot at top center and use the DC OFFSET control to set the trace at the bottom graticule line.

f. Turn the POSITION control clockwise and check that the trace moves up 5 divisions or more.

g. Reset the POSITION control to the midrange and set the trace to the top graticule line with the DC OFFSET control.

h. Turn the POSITION control counterclockwise and check that the trace moves down 5 divisions or more.

i. Change the sampling head to the other channel and repeat steps e through h of the above procedure.

If either channel does not operate as stated above in steps b and d, check the Position Indicator neon control circuit. If either channel POSITION control range is less than ±5 divisions, check the Channel Amplifier circuits for transistors with low β, or feedback resistor that have changed value.

14. Adjust Memory Gain Capacitors (Channel A C276, Channel B C576) Using Normalizer Head Calibration Fixture ◐

NOTE

Steps 14 and 15 accomplish the same goal of obtaining proper Memory Gain capacitor adjustment. Step 14 uses a special Tektronix calibration fixture (item 17 of equipment required), and Step 15 uses either a Type S-1 or S-2 Sampling Head. Both steps are included in this procedure to allow the Type 3S2 to be adjusted when a Normalizer Head is not available. Time is saved if a Normalizer is used, and step 15 can then be disregarded.

a. Install the Normalizer Head in the Channel B opening and set the Units/Div switch to 100.

b. Free run the sampling sweep unit. If using a Type 3T2, any sweep rate that produces a continuous double trace display is satisfactory. If using a Type 3T4 or Type 3T77A, the Time/Div control must be at .5 μs or some other sweep rate counterclockwise from the .5 μs position.

Set the Type 3S2 NORMAL-SMOOTH switch to NORMAL. Use the DC OFFSET control so the sampling display is two traces, several divisions apart.

c. Connect the test oscilloscope 10× probe to TP579 (or TP279 for Channel A); see Fig. 6-6. Free run the test oscilloscope, using a sweep rate of 1 ms/div and vertical deflection factor of 1 V/div (including the probe 10× attenuation). The test oscilloscope display will be two straight line traces when the sampling sweep unit is a Type 3T2. The display will be a square wave when the sampling sweep unit is a Type 3T4 or Type 3T77A.

d. Set the DOT RESPONSE control fully clockwise, and note either the indicator or test oscilloscope display. Record the number of divisions of trace separation. Set the DOT RESPONSE control fully counterclockwise. Record the number of divisions of trace separation. Calculate the number of divisions by which the two traces should be separated when the DOT RESPONSE control is at its electrical midrange setting. Set the DOT RESPONSE control to its electrical midpoint.

e. Adjust the Memory Gain capacitor (see Fig. 6-6 for location) until the two indicator oscilloscope traces are exactly 5 major divisions apart. The test oscilloscope display should indicate exactly 2.5 volts difference between the two traces (or the square wave signal peak to peak value). The ±3% tolerance of both of these displays may show that

they differ. This is of no consequence to the Type 3S2 calibration, because of the range of the DOT RESPONSE control. The real value of this adjustment is that if more than one Type 3S2 is calibrated in the same lab, then they will all permit unity loop gain operation of any calibrated sampling head in any Type 3S2. This step or step 15 should be performed before attempting a sampling head recalibration, particularly when adjusting the sampling head Preamplifier Gain control.

f. Repeat the above procedure for the other Type 3S2 channel.

15. Adjust Both Channels For Unity Dot Response

NOTE

This step establishes the correct balance between the sampling head Preamplifier Gain control (R46, see Fig. 6-10) and the Type 3S2 Memory Gain controls C276 and C576. The procedure includes, both the indicator oscilloscope and test oscilloscope displays.

a. Input signal amplitude to the sampling head must be the values stated earlier in Table 6-1. The test oscilloscope display of the sampling head output signals (Fig. 6-8 and Fig. 6-9) are to be adjusted for ±0.2 volt when using a Type S-1, and for ±0.08 volt when using a Type S-2.

Set the Type 284 to deliver 1 μs square waves at 1.0 volt. Install the correct 50 Ω attenuator in the signal cable at the Type 284 output connector. Set the sampling sweep rate to 500 ns/div (0.5 μs/div). Set both Type 3S2 units/div controls to 100.

b. Obtain a double-triggered display on the indicator oscilloscope by free running the sampling sweep unit and adjusting the Recovery Time control. The display should be similar to any one in Fig. 6-7.

Turn the Type 3S2 DOT RESPONSE control through its range. The double-triggered display amplitude should change over the control range in a manner similar to the triple exposure of Fig. 6-12. Set the DOT RESPONSE control to its electrical midpoint; not necessarily to unity loop gain.

c. Connect the test oscilloscope 10× probe to TP121 (or TP161 for Channel B). Externally trigger the test oscilloscope from TP235, using a sweep rate of 0.1 μs/div and vertical deflection factor of 0.1 V/div (including the probe 10× attenuation).

d. Decide whether the sampling display dot response indicates a loop gain greater or less than unity. Also note carefully the test oscilloscope display amplitude.

If the sampling head output signal is greater than that stated in part a at the beginning of this step, and at the same time the sampling display shows greater than unity loop gain, adjust the Type 3S2 Memory Gain capacitor for unity loop gain. (Channel A Memory Gain capacitor is C276; see Fig. 6-6 for control locations).

If the sampling head output signal (on the test scope) is still greater than required, reduce the sampling head preamplifier gain (R46 shown in Fig. 6-10) a small amount, but not all the way to unity loop gain. Return the loop to unity dot response with the Memory Gain capacitor.

Or, if the Sampling Head output signal is less than required when the indicator oscilloscope displays unity loop gain, increase the sampling head preamplifier gain a small

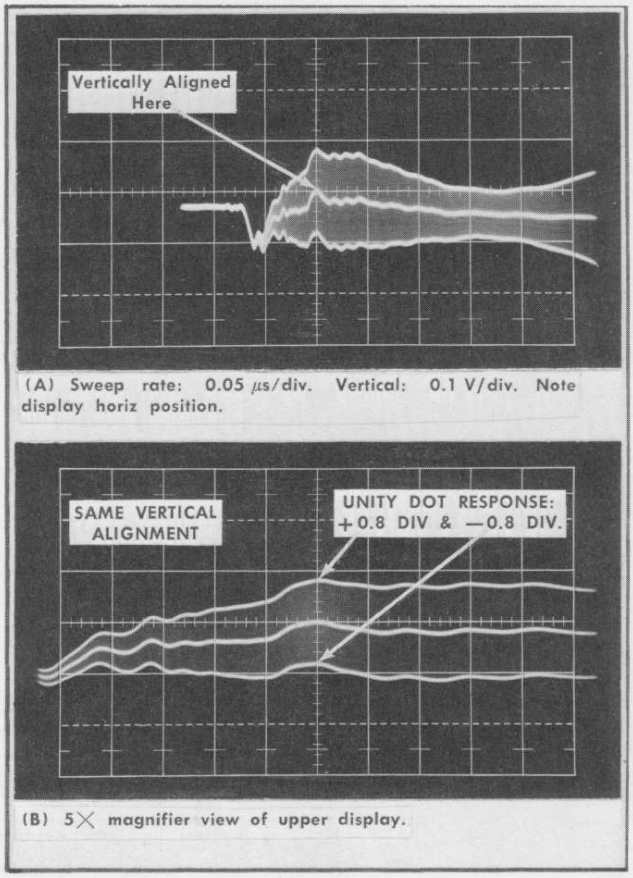


Fig. 6-9. 85 MHz test oscilloscope displays of Type S-2 double triggered output signal showing unity loop gain. TP121 or TP161, step 4.

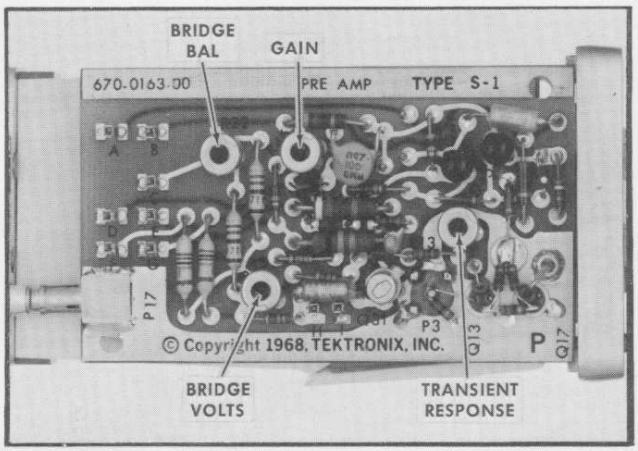


Fig. 6-10. Sampling Head adjustments, left side.

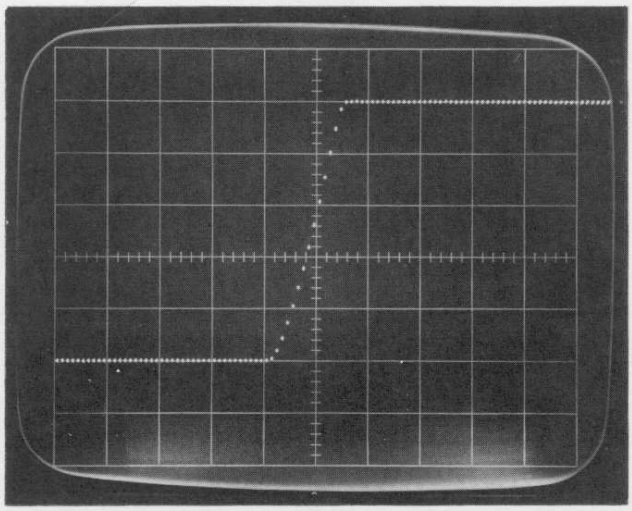


Fig. 6-11. Typical 5 div display of step 12f.

amount. Return the loop to unity gain with the Memory Gain capacitor.

Through such interacting adjustments, set the system loop gain to unity while the test osciloscope reveals that the sampling head output signal is the correct amplitude listed in part a of this step.

e. Repeat the above procedure for the other channel.

16. Check Interchannel Delay Range

Requirement—B DELAY control range is at least 10 ns.

a. It is desirable, but not necessary to use two sampling heads of the same type, either S-1 or S-2. One sampling head may be used, changing it from one channel to the other as necessary.

b. Connect the Type 284 fast pulse output to the Channel A sampling head input connector. Externally trigger the sampling sweep unit from the Type 284 Trigger Output connector. Set the sampling sweep rate to 2 ns/div with the Display Mag switch at ×1. Set the Type 3S2 Mode switch to CH A.

c. Obtain a step display of the signal fed to Channel A. Adjust the sampling sweep unit Time Position controls so the center of the rise passes through the center of the graticule.

d. Change the Mode switch to CH B and apply the Type 284 fast pulse to the Channel B input connector.

e. Set the Type 3S2 B DELAY control fully counterclockwise and note the position of the step 50% amplitude point. It should be 2.5 divisions or more to the left of the graticule center (at least 5 ns to the left of center).

f. Turn the B DELAY control fully clockwise and check that the Channel B 50% amplitude point is to the right of the center graticule line, for a total range of at least 10 ns.

17. Adjust Type 3S2 A Delay Control ❶

a. Install two identical sampling heads, either Type S-1 or Type S-2.

b. Connect the Type 284 fast pulse output to the Channel B Sampling Head input connector. Set the Type 3T2 sweep rate to 2 ns/div with the Mag switch at ×1. Set the Type 3S2 mode switch to DUAL-TRACE.

c. Obtain a step display of the signal fed to Channel B. Set the B DELAY control fully counterclockwise and use the sampling sweep unit Time Position controls to move the step so the center of its rise passes to the left of the graticule 2.5 div point; see point no. 1, Fig. 6-13.

d. Turn the B DELAY control fully clockwise. The step display should now be to the right of the graticule 7.5 div point; see point no. 2, Fig. 6-13. Adjust the sampling sweep Time Position controls so the two points (No. 1 and No. 2 of Fig. 6-13) fall equal distances on the left and right of the graticule centerline.

e. Move the signal cable to Channel A input. The step display should now be at the graticule centerline: see Fig. 6-13, point No. 3. If not, adjust the A Delay control, R60 shown in Fig. 6-7, so that the step display half-amplitude point does cross at the graticule centerline.

NOTE

In the event that two identical sampling heads are not to be used in the Type 3S2, it is proper to make the above adjustments with the two heads that will normally be used in your instrument.

18. Adjust Sampling Mode Repetition Rate ❶

a. Set the sampling sweep unit Trig Sensitivity control fully counterclockwise and the Type 3S2 Horiz Plug-In Compatibility switch SW6 (located on internal bulkhead), to the Non-Sampling 2B, 3B-Series position.

b. Set the test oscilloscope sweep rate to 10 μs/div and the vertical deflection factor to 20 V/div (including 10× probe). Connect the test oscilloscope 10× probe to TP24, Fig. 6-5A.

c. Check that the test oscilloscope display is between 9.5 and 10.5 cycles in 10 divisions (95 kHz to 105 kHz). Adjust L8, located on the right side, Fig. 6-5A, for 10 cycles if the repetition rate is not correct.

d. Reset the Horiz Plug-In compatibility switch SW6, to the Sampling 3T-Series position and remove the 10× probe.

19. Check Memory Slash

Requirement—Vertical dot drift is ≤0.1 division when timing unit is triggered at 20 Hz.

a. Connect the Type 106 Trigger Output to the sampling sweep unit 50 Ω Trigger Input through a 50 Ω coaxial cable and 5× attenuator.

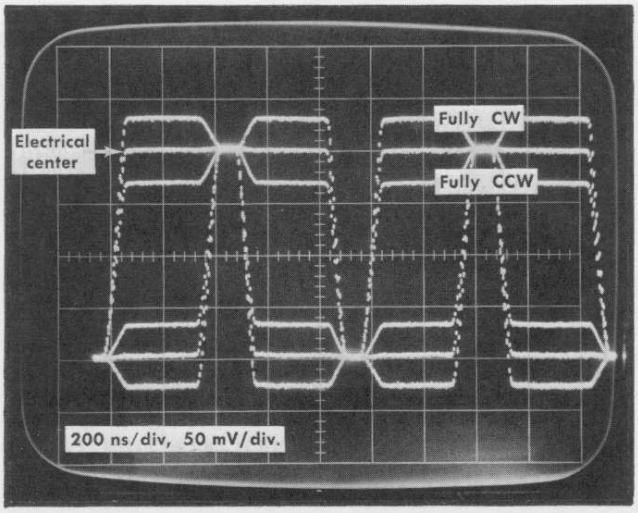


Fig. 6-12. Finding electrical center of Type 3S2 DOT RESPONSE control. Triple exposure; double triggered; 1 μs square wave.

b. Set both Type 3S2 Units/Div switches to 200 and set the Type 106 for a 20 Hz Repetition Rate. Set the sampling sweep unit Trig Sensitivity control so the sweep is triggered.

c. Check that the vertical amplitude of slash (dot drift) is 0.1 division or less.

d. Change the Mode switch to CH A and check that the vertical amplitude of slash is 0.1 division or less.

20. Check Offset Out (Range and Accuracy)

Requirement—Each channel OFFSET OUT jack voltage is 10 times the internal DC Offset referred to the input, ±2%.

a. Set the test oscilloscope and Type W controls as follows:

Triggering Mode	Auto
Time/cm	5 ms

Type W Plug-In Unit

Display	A — Vc
Input Atten	R ≈ ∞
Millivolts/cm	20
Variable	Cal
Comparison Voltage	0.00
Vc Range	—11
A Input Selector	DC
Position	Midrange

b. Connect a 1× probe to the Type W Input A connector, connect the probe tip to the Channel A OFFSET OUT jack of the Type 3S2 and adjust the Channel A DC OFFSET control for zero volts out as indicated by the test oscilloscope CRT.

c. Set the 50 Ω Amplitude Calibrator Volts switch to .6 and connect this output through a 50 Ω coaxial cable to the Channel A sampling head input connector. Connect the Trigger Output connector to the sampling sweep unit Trigger Input 50 Ω connector and set the sweep rate for 10 μs.

d. Set the Trig Sensitivity of the sampling sweep unit for a stable trace and set the Type 3S2 A POSITION control to move the top of the displayed signal to the center of the graticule.

e. Set the A Channel Units/Div switch to 5 and use the A POSITION control to again set the top of the displayed signal to the center of the graticule.

f. Turn the A Channel DC OFFSET control clockwise until the bottom of the signal is displayed at the centerline of the graticule, and measure the offset voltage with the test oscilloscope. Set the Type W Comparison Voltage control (Vc) to measure 6 volts. Then make a final measurement with the Comparison Voltage variable. The Type 3S2 Offset Out voltage must be 6 volts, ±2%, 5.88 to 6.12 volts.

g. Set the Comparison Voltage (Vc) of the Type W to 10 Volts, turn the A Channel DC OFFSET control fully clockwise, and check for ≥ —10 Volts.

h. Set the Vc Range switch to +11, turn the A Channel DC OFFSET counterclockwise, and check for ≥ +10 Volts.

i. Change the signal input to the Channel B Sampling Head Input, set the Mode switch to CH B and connect the test oscilloscope, probe to the B OFFSET OUT jack. Repeat the above procedure for the B Channel.

21. Check A and B Vert Outputs Voltage

Requirement—Output voltage of each channel, A or B, is 200 mV per displayed division ±3%.

a. Set both Units/Div switches to 100 and set the 50 Ω Amplitude Calibrator Volts switch to .6.

b. Set the Type W Comparison Voltage to 0.00 and the Vc Range switch to —11.

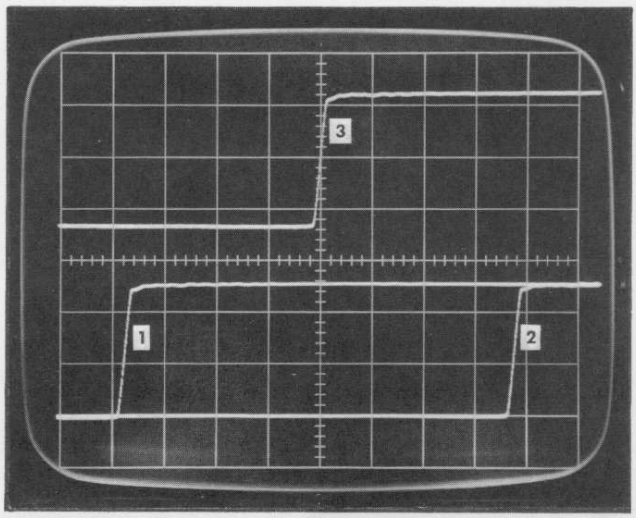


Fig. 6-13. Waveforms for step 17. Sweep rate: 2 ns/div, with Display mag switch at X1.

c. Connect the signal from the Type 3S2 B VERT OUTPUT jack through a 1× probe to the Type W Input A.

d. Adjust the Position control of the Type W so the positive portion of the square wave (top of the display) is at the center of the graticule. Some adjustment of the B Channel DC OFFSET control of the Type 3S2 may be necesary.

e. Set the Comparison Voltage of the Type W so the negative portion of the square wave (bottom of the display) is at the center of the graticule.

f. Check that the Comparison Voltage is 1.2 volts ±3% (1.164 to 1.236 volts) which is 200 mV per division of display amplitude.

g. Move the signal to Channel A Sampling Head Input connector, set the Mode switch to CH A and move the 1× probe to the A VERT OUTPUT jack of the Type 3S2. Repeat the measurement procedure for the A VERT OUTPUT.

h. Disconnect the test oscilloscope probe.

22. Check Trig Out (Into 50 Ω) SN B040250-up

Requirement—Trig Out signal amplitude is approximately equal to the input signal voltage into 50 Ω load (at least 0.9 times the input voltage); risetime is 2 ns or less, 10% to 90%, with ≤70 ps risetime pulse as the input signal.

a. With the same Channel A 6 division display as at the end of step 21, connect the TRIG OUT cable to the sampling head input in Channel B through a GR to BNC female adapter. Set the B Units/Div switch to 100 and the Mode switch to CH B. Set the TRIG OUT switch to A.

b. Check that the display amplitude is approximately 6 divisions, or at least 5.4 divisions, 540 millivolts.

c. Reverse the signal connections to the two sampling head input connectors.

d. Set the Mode switch to CH A and the TRIG OUT switch to B.

e. Check that the display amplitude is approximately 6 divisions or at least 5.4 divisions, 540 millivolts.

f. Disconnect the cables from the 50 Ω Amplitude Calibrator.

g. Connect the Type 284 Trigger Output connector to the sampling sweep unit external Trigger Input 50 Ω connector. Use a 5 ns delay coaxial cable with BNC connectors.

Connect the Type 284 Pulse Output connector to the Channel B sampling head input connector. Use a 5 ns signal delay coaxial cable with GR connectors (either RG-58 or RG-213 Cable). Connect the TRIG OUT signal cable to the Channel A sampling head input connector. Set the Type 3S2 Mode switch to CH B and the TRIG OUT switch to B.

h. Set both Units/Div switches to 50. Set the sampling sweep rate to 2 ns/div and adjust the Triggering and Time Position controls for a stable display. The display is that of the fast pulse input signal to Channel B.

i. Set the Type 3S2 Mode switch to CH A and measure the risetime of the TRIG OUT signal between the 10% and 90% amplitude points.

j. Reverse the position of the input cable to the sampling heads. Set the Type 3S2 Mode switch to CH B and the TRIG OUT switch to A. Measure the TRIG OUT signal risetime between the 10% and 90% amplitude points. Use the Variable control to set the amplitude to a convenient display size, such as 5 divisions. Check that the risetime takes not longer than 2 ns.

If difficulty is encountered, check the sampling head trigger circuit components first, then check the Type 3S2 Trigger circuit components.

23. Check Trig Out (Into 50 Ω) SN B010101-SN B030249

Requirement—Trig Out signal amplitude is approximately 0.010 times input signal voltage into 50 Ω load (at least 0.09 times the input voltage); risetime is 0.6 ns or less, 10% to 50%, with ≤ 70 ps risetime pulse as the input signal.

a. With the same Channel A 6 division display as at the end of step 21, connect the TRIG OUT cable to the sampling head input in Channel B through a GR to BNC female adapter. Set the B Units/Div switch to 20 and the Mode switch to CH B. Set the TRIG OUT switch to A.

b. Check that the display amplitude is approximately 3 divisions, or at least 2.7 divisions (54 millivolts).

c. Reverse the signal connections to the two sampling head input connectors. Set the Channel A Units/Div switch to 20 and the Channel B Units/Div switch to 100.

d. Set the Mode switch to CH A and the TRIG OUT switch to B.

e. Check that the display amplitude is approximately 3 divisions or at least 2.7 divisions (54 millivolts).

f. Disconnect the cables from the 50 Ω Amplitude Calibrator.

g. Connect the Type 284 Trigger Output connector to the sampling sweep unit external Trigger Input 50 Ω connector. Use a 5 ns delay coaxial cable with BNC connectors.

Connect the Type 284 Pulse Output connector to the Channel B sampling head input connector. Use a 5 ns signal delay coaxial cable with GR connectors (either RG-58 or RG-213 cable). Connect the TRIG OUT signal cable to the Channel A sampling head input connector. Set the Type 3S2 mode switch to CH B, and the TRIG OUT switch to B.

h. Set the Channel A Units/Div switch to 5 and the Channel B Units/Div switch to 50. Set the sampling sweep rate to 1 ns/div and adjust the Triggering and Time Position controls for a stable display. The display is that of the fast pulse input signal to Channel B.

i. Set the Type 3S2 Mode switch to CH A and measure the risetime of the TRIG OUT signal between the 10% and 50% amplitude points.

j. Reverse the position of the input cable to the sampling heads. Change the Units/Div switches to Channel A, 50; Channel B, 5; the TRIG OUT switch to A, and the Mode switch to B. Measure the TRIG OUT signal risetime between the 10% and 50% amplitude points. Use the Variable control to set amplitude to a convenient display size, such as 5 divisions. Check that the risetime takes not longer than 0.6 ns.

If difficulty is encountered, check the sampling head trigger circuit components first, then check the Type 3S2 Trigger circuit components.

PARTS LIST ABBREVIATIONS

BHB	binding head brass
BHS	binding head steel
cap.	capacitor
cer	ceramic
comp	composition
conn	connector
CRT	cathode-ray tube
csk	countersunk
DE	double end
dia	diameter
div	division
elect.	electrolytic
EMC	electrolytic, metal cased
EMT	electrolytic, metal tubular
ext	external
F & I	focus and intensity
FHB	flat head brass
FHS	flat head steel
Fil HB	fillister head brass
Fil HS	fillister head steel
h	height or high
hex.	hexagonal
HHB	hex head brass
HHS	hex head steel
HSB	hex socket brass
HSS	hex socket steel
ID	inside diameter
incd	incandescent
int	internal
lg	length or long
met.	metal
mtg hdw	mounting hardware
OD	outside diameter
OHB	oval head brass
OHS	oval head steel
PHB	pan head brass
PHS	pan head steel
plstc	plastic
PMC	paper, metal cased
poly	polystyrene
prec	precision
PT	paper, tubular
PTM	paper or plastic, tubular, molded
RHB	round head brass
RHS	round head steel
SE	single end
SN or S/N	serial number
SW	switch
TC	temperature compensated
THB	truss head brass
thk	thick
THS	truss head steel
tub.	tubular
var	variable
w	wide or width
WW	wire-wound

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number
*000-0000-00	Asterisk preceding Tektronix Part Number indicates manufactured by or for Tektronix, Inc., or reworked or checked components.
Use 000-0000-00	Part number indicated is direct replacement.
	Screwdriver adjustment.
	Control, adjustment or connector.

SECTION 7
ELECTRICAL PARTS LIST

Values are fixed unless marked Variable.

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
				Bulbs			
B798	150-0035-00			Neon A1D T2			
B799	150-0035-00			Neon A1D T2			
				Capacitors			
Tolerance ±20% unless otherwise indicated.							
C3	283-0032-00			470 pF	Cer	500 V	5%
C4	283-0115-00			47 pF	Cer	200 V	5%
C6	290-0134-00			22 μF	Elect.	15 V	
C8	283-0059-00			1 μF	Cer	25 V	+80%—20%
C9	285-0598-00			0.01 μF	PTM	100 V	5%
C10	285-0598-00			0.01 μF	PTM	100 V	5%
C12	283-0059-00			1 μF	Cer	25 V	+80%—20%
C15	283-0113-00			56 pF	Cer	500 V	1%
C20	283-0059-00			1 μF	Cer	25 V	+80%—20%
C22	283-0108-00			220 pF	Cer	200 V	10%
C23	283-0084-00			270 pF	Cer	1000 V	5%
C25	283-0094-00			27 pF	Cer	200 V	10%
C27	283-0003-00			0.01 μF	Cer	150 V	
C31	283-0032-00			470 pF	Cer	500 V	5%
C33	283-0115-00			47 pF	Cer	200 V	5%
C34	283-0094-00			27 pF	Cer	200 V	10%
C36	283-0032-00			470 pF	Cer	500 V	5%
C41	283-0103-00			180 pF	Cer	500 V	5%
C45	283-0094-00			27 pF	Cer	200 V	10%
C61	283-0032-00			470 pF	Cer	500 V	5%
C63	283-0115-00			47 pF	Cer	200 V	5%
C64	283-0094-00			27 pF	Cer	200 V	10%
C66	283-0032-00			470 pF	Cer	500 V	5%
C71	283-0103-00			180 pF	Cer	500 V	5%
C75	283-0094-00			27 pF	Cer	200 V	10%
C100	283-0072-01			0.01 μF	Cer		
C104	283-0167-00	XB040000		0.1 μF	Cer	100 V	10%
C106	283-0121-00			0.001 μF	Cer	200 V	
C108	283-0072-01	B010100	B039999	0.01 μF	Cer		
C108	281-0645-00	B040000		8.2 pF	Cer	500 V	±0.25 pF
C110	283-0167-00	XB040000		0.1 μF	Cer	100 V	10%
C112	283-0072-01			0.01 μF	Cer		
C116	283-0121-00			0.001 μF	Cer	200 V	
C117	290-0187-00	XB040000		4.7 μF	Elect.	35 V	
C118	283-0072-01	XB040000		0.01 μF	Cer		
C119	283-0072-01	XB040000		0.01 μF	Cer		

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
C127	283-0051-00			0.0033 μF	Cer	100 V 5%
C131	283-0026-00			0.2 μF	Cer	25 V
C134	283-0059-00			1 μF	Cer	25 V +80%—20%
C139	283-0065-00			0.001 μF	Cer	100 V 5%
C149	283-0103-00			180 pF	Cer	500 V 5%
C153	283-0026-00			0.2 μF	Cer	25 V
C159	283-0067-00			0.001 μF	Cer	200 V 10%
C167	283-0051-00			0.0033 μF	Cer	100 V 5%
C171	283-0026-00			0.2 μF	Cer	25 V
C174	283-0059-00			1 μF	Cer	25 V +80%—20%
C179	283-0065-00			0.001 μF	Cer	100 V 5%
C189	283-0103-00			180 pF	Cer	500 V 5%
C193	283-0026-00			0.2 μF	Cer	25 V
C199	283-0067-00			0.001 μF	Cer	200 V 10%
C201	283-0059-00			1 μF	Cer	25 V +80%—20%
C221	283-0026-00			0.2 μF	Cer	25 V
C224	283-0059-00			1 μF	Cer	25 V +80%—20%
C229	283-0032-00			470 pF	Cer	500 V 5%
C231	283-0059-00			1 μF	Cer	25 V +80%—20%
C240	283-0594-00			0.001 μF	Mica	100 V 1%
C241	283-0000-00			0.001 μF	Cer	500 V
C253	281-0611-00			2.7 pF	Cer	200 V ±0.25 pF
C261	283-0059-00			1 μF	Cer	25 V +80%—20%
C267	283-0059-00			1 μF	Cer	25 V +80%—20%
C272	283-0026-00			0.2 μF	Cer	25 V
C274	283-0026-00			0.2 μF	Cer	25 V
C276	281-0092-00			9-35 pF, Var	Cer	
C277	283-0600-00			43 pF	Mica	500 V 5%
C286	283-0076-00			27 pF	Cer	500 V 10%
C299	283-0103-00			180 pF	Cer	500 V 5%
C307	283-0615-00			33 pF	Mica	500 V 5%
C315	283-0076-00			27 pF	Cer	500 V 10%
C501	283-0059-00			1 μF	Cer	25 V +80%—20%
C521	283-0026-00			0.2 μF	Cer	25 V
C524	283-0059-00			1 μF	Cer	25 V +80%—20%
C529	283-0032-00			470 pF	Cer	500 V 5%
C531	283-0059-00			1 μF	Cer	25 V +80%—20%
C540	283-0594-00			0.001 μF	Mica	100 V 1%
C541	283-0000-00			0.001 μF	Cer	500 V
C553	281-0611-00			2.7 pF	Cer	200 V ±0.25 pF
C561	283-0059-00			1 μF	Cer	25 V +80%—20%
C567	283-0059-00			1 μF	Cer	25 V +80%—20%
C572	283-0026-00			0.2 μF	Cer	25 V
C574	283-0026-00			0.2 μF	Cer	25 V
C576	281-0092-00			9-35 pF, Var	Cer	

Capacitors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
C577	283-0600-00		43 pF	Mica	500 V	5%
C586	283-0076-00		27 pF	Cer	500 V	10%
C599	283-0103-00		180 pF	Cer	500 V	5%
C607	283-0615-00		33 pF	Mica	500 V	5%
C615	283-0076-00		27 pF	Cer	500 V	10%
C702	283-0060-00		100 pF	Cer	200 V	5%
C713	283-0059-00		1 μF	Cer	25 V	+80%—20%
C719	283-0144-00		33 pF	Cer	500 V	1%
C723	283-0059-00		1 μF	Cer	25 V	+80%—20%
C729	283-0144-00		33 pF	Cer	500 V	1%
C753	283-0026-00		0.2 μF	Cer	25 V	
C782	283-0026-00		0.2 μF	Cer	25 V	
C779	281-0592-00		4.7 pF	Cer		±0.5 pF
C808	283-0059-00		1 μF	Cer	25 V	+80%—20%
C810	283-0059-00		1 μF	Cer	25 V	+80%—20%
C812	283-0059-00		1 μF	Cer	25 V	+80%—20%
C814	290-0135-00		15 μF	Elect.	20 V	
C816	290-0135-00		15 μF	Elect.	20 V	
C824	290-0317-00		1000 μF	Elect.	40 V	+100%—10%
C826	283-0059-00		1 μF	Cer	25 V	+80%—20%
C830	283-0094-00		27 pF	Cer	200 V	10%
C833	290-0158-00		50 μF	Elect.	25 V	+75%—15%
C848	283-0067-00		0.001 μF	Cer	200 V	10%
C853	283-0067-00		0.001 μF	Cer	200 V	10%
C857	283-0004-00		0.02 μF	Cer	150 V	
C858	283-0004-00		0.02 μF	Cer	150 V	
C860	290-0327-00		0.56 μF	Elect.	100 V	
C862	290-0327-00		0.56 μF	Elect.	100 V	
C864	290-0327-00		0.56 μF	Elect.	100 V	
C866	290-0327-00		0.56 μF	Elect.	100 V	
C870	283-0004-00		0.02 μF	Cer	150 V	
C872	283-0004-00		0.02 μF	Cer	150 V	
C874	290-0135-00		15 μF	Elect.	20 V	
C876	283-0026-00		0.2 μF	Cer	25 V	
C878	290-0135-00		15 μF	Elect.	20 V	
C880	283-0004-00		0.02 μF	Cer	150 V	
C882	283-0004-00		0.02 μF	Cer	150 V	
C884	290-0135-00		15 μF	Elect.	20 V	
C886	283-0026-00		0.2 μF	Cer	25 V	
C888	290-0135-00		15 μF	Elect.	20 V	
C890	290-0134-00		22 μF	Elect.	15 V	
C892	290-0134-00		22 μF	Elect.	15 V	
C894	290-0134-00		22 μF	Elect.	15 V	
C896	290-0134-00		22 μF	Elect.	15 V	

Semiconductor Device, Diodes

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D2	*152-0185-00			Silicon Replaceable by 1N4152
D15	*152-0185-00			Silicon Replaceable by 1N4152
D24	*152-0185-00			Silicon Replaceable by 1N4152
D25	*152-0233-00			Silicon Tek Spec
D31	*152-0185-00			Silicon Replaceable by 1N4152
D34	*152-0185-00			Silicon Replaceable by 1N4152
D38	*152-0185-00			Silicon Replaceable by 1N4152
D52	*152-0185-00			Silicon Replaceable by 1N4152
D54	*152-0185-00			Silicon Replaceable by 1N4152
D61	*152-0185-00			Silicon Replaceable by 1N4152
D64	*152-0185-00			Silicon Replaceable by 1N4152
D68	*152-0185-00			Silicon Replaceable by 1N4152
D82	*152-0185-00			Silicon Replaceable by 1N4152
D84	*152-0185-00			Silicon Replaceable by 1N4152
D103	*152-0185-01	B010100	B039999	Silicon Replaceable by 1N4152
D103	*152-0185-00	B040000		Silicon Replaceable by 1N4152
D104	*152-0075-00	XB040000		Germanium Tek Spec
D113	*152-0185-01	B010100	B039999	Silicon Replaceable by 1N4152
D113	*152-0185-00	B040000		Silicon Replaceable by 1N4152
D201	*152-0185-00			Silicon Replaceable by 1N4152
D209	*152-0185-00			Silicon Replaceable by 1N4152
D231	152-0195-00			Zener 1N751A 0.4 W 5.1 V 5%
D232	*152-0185-00			Silicon Replaceable by 1N4152
D233	*152-0185-00			Silicon Replaceable by 1N4152
D234	*152-0185-00			Silicon Replaceable by 1N4152
D236	*152-0185-00			Silicon Replaceable by 1N4152
D237	*152-0323-00			Silicon Tek Spec
D238	*152-0185-00			Silicon Replaceable by 1N4152
D239	*152-0323-00			Silicon Tek Spec
D243	*152-0185-00			Silicon Replaceable by 1N4152
D252	*152-0185-00			Silicon Replaceable by 1N4152
D254	*152-0185-00			Silicon Replaceable by 1N4152
D256	*152-0185-00			Silicon Replaceable by 1N4152
D276	*152-0323-00			Silicon Tek Spec
D277	*152-0323-00			Silicon Tek Spec
D282	*152-0185-00			Silicon Replaceable by 1N4152
D287	*152-0185-00			Silicon Replaceable by 1N4152
D306	*152-0185-00			Silicon Replaceable by 1N4152
D310	*152-0185-00			Silicon Replaceable by 1N4152
D316	*152-0185-00			Silicon Replaceable by 1N4152
D317	152-0280-00			Zener 1N753A 0.4 W 6.2 V 5%
D331	*152-0185-00			Silicon Replaceable by 1N4152
D501	*152-0185-00			Silicon Replaceable by 1N4152
D509	*152-0185-00			Silicon Replaceable by 1N4152
D531	152-0195-00			Zener 1N751A 0.4 W 5.1 V 5%
D532	*152-0185-00			Silicon Replaceable by 1N4152
D533	*152-0185-00			Silicon Replaceable by 1N4152
D534	*152-0185-00			Silicon Replaceable by 1N4152

Semiconductor Device, Diodes *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
D536	*152-0185-00			Silicon Replaceable by 1N4152
D537	*152-0323-00			Silicon Tek Spec
D538	*152-0185-00			Silicon Replaceable by 1N4152
D539	*152-0323-00			Silicon Tek Spec
D543	*152-0185-00			Silicon Replaceable by 1N4152
D552	*152-0185-00			Silicon Replaceable by 1N4152
D554	*152-0185-00			Silicon Replaceable by 1N4152
D556	*152-0185-00			Silicon Replaceable by 1N4152
D576	*152-0323-00			Silicon Tek Spec
D577	*152-0323-00			Silicon Tek Spec
D582	*152-0185-00			Silicon Replaceable by 1N4152
D587	*152-0185-00			Silicon Replaceable by 1N4152
D606	*152-0185-00			Silicon Replaceable by 1N4152
D610	*152-0185-00			Silicon Replaceable by 1N4152
D616	*152-0185-00			Silicon Replaceable by 1N4152
D617	152-0280-00			Zener 1N753A 0.4 W 6.2 V 5%
D701	*152-0233-00			Silicon Tek Spec
D705	*152-0185-00			Silicon Replaceable by 1N4152
D706	*152-0185-00			Silicon Replaceable by 1N4152
D709	*152-0185-00			Silicon Replaceable by 1N4152
D714	*152-0185-00			Silicon Replaceable by 1N4152
D715	152-0008-00			Germanium
D724	*152-0185-00			Silicon Replaceable by 1N4152
D726	152-0008-00			Germanium
D750	*152-0185-00			Silicon Replaceable by 1N4152
D751	*152-0185-00			Silicon Replaceable by 1N4152
D760	*152-0185-00			Silicon Replaceable by 1N4152
D761	*152-0185-00			Silicon Replaceable by 1N4152
D774	*152-0185-00			Silicon Replaceable by 1N4152
D782	152-0227-00			Zener 1N753A 0.4 W 6.2 V 5%
D784	*152-0185-00			Silicon Replaceable by 1N4152
D791	*152-0185-00			Silicon Replaceable by 1N4152
D792	*152-0185-00			Silicon Replaceable by 1N4152
D823	152-0066-00			Silicon 1N3194
D825	152-0066-00			Silicon 1N3194
D827	152-0212-00			Zener 1N936 9 V 5% 0.005%/°C TC
D837	*152-0185-00			Silicon Replaceable by 1N4152
D848	*152-0185-00			Silicon Replaceable by 1N4152
D853	*152-0185-00			Silicon Replaceable by 1N4152
D891	*152-0107-00			Silicon Replaceable by 1N647
D892	*152-0107-00			Silicon Replaceable by 1N647
D894	*152-0107-00			Silicon Replaceable by 1N647
D895	*152-0107-00			Silicon Replaceable by 1N647
D897	*152-0107-00			Silicon Replaceable by 1N647
D898	*152-0107-00			Silicon Replaceable by 1N647

Connectors

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
J1	131-0391-00			Coax, 50 Ω male
P11	131-0149-00			24 contact, male
P12	131-0149-00			24 contact, male
J41	131-0391-00			Coax, 50 Ω male
J71	131-0391-00			Coax, 50 Ω male
J101	131-0391-00			Coax, 50 Ω male
J104	131-0391-00			Coax, 50 Ω male
J111	131-0391-00			Coax, 50 Ω male
J120	131-0581-00			Receptacle, 12 contact, female
J160	131-0581-00			Receptacle, 12 contact, female

Inductors

L6	*120-0382-00		Toroid, 14 turns single
L8	*114-0179-00		500-800 μH, Var Core not replaceable
L104	*108-0373-00	XB040000	56 nH
L287	*120-0402-00		Toroid, 3 turns single
L298	*120-0402-00		Toroid, 3 turns single
L313	*120-0402-00		Toroid, 3 turns single
L587	*120-0402-00		Toroid, 3 turns single
L598	*120-0402-00		Toroid, 3 turns single
L613	*120-0402-00		Toroid, 3 turns single
L814	*120-0382-00		Toroid, 14 turns single
L816	*120-0382-00		Toroid, 14 turns single
L860	*120-0382-00		Toroid, 14 turns single
L862	*120-0382-00		Toroid, 14 turns single
L864	*120-0382-00		Toroid, 14 turns single
L866	*120-0382-00		Toroid, 14 turns single
L874	*120-0382-00		Toroid, 14 turns single
L878	*120-0382-00		Toroid, 14 turns single
L884	*120-0382-00		Toroid, 14 turns single
L888	*120-0382-00		Toroid, 14 turns single
L890	*120-0382-00		Toroid, 14 turns single
L892	*120-0382-00		Toroid, 14 turns single
L894	*120-0382-00		Toroid, 14 turns single
L896	*120-0382-00		Toroid, 14 turns single

Transistors

Q3	151-0190-00		Silicon	2N3904
Q17	151-0190-00		Silicon	2N3904
Q24	*151-0133-00		Silicon	Selected from 2N3251
Q36	151-0188-00		Silicon	2N3906
Q41	151-0190-00		Silicon	2N3904
Q54	151-0188-00		Silicon	2N3906
Q66	151-0188-00		Silicon	2N3906
Q71	151-0190-00		Silicon	2N3904
Q84	151-0188-00		Silicon	2N3906
Q103	151-0202-00		Silicon	2N4261
Q104	*151-0212-00	XB040000	Silicon	Tek Spec

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q113	151-0202-00		Silicon	2N4261
Q114	151-0202-00	XB040000	Silicon	2N4261
Q123	*151-0192-00		Silicon	Replaceable by MPS - 6521
Q128	151-0188-00		Silicon	2N3906
Q133	151-0190-00		Silicon	2N3904
Q136	151-0188-00		Silicon	2N3906
Q155	151-0190-00		Silicon	2N3904
Q163	*151-0192-00		Silicon	Replaceable by MPS - 6521
Q168	151-0188-00		Silicon	2N3906
Q173	151-0190-00		Silicon	2N3904
Q176	151-0188-00		Silicon	2N3906
Q195	151-0190-00		Silicon	2N3904
Q203	151-0190-00		Silicon	2N3904
Q211	151-0190-00		Silicon	2N3904
Q223	151-0190-00		Silicon	2N3904
Q224	151-0188-00		Silicon	2N3906
Q243	151-1007-00		FET	Dual
Q252	151-0188-00		Silicon	2N3906
Q261	151-0190-00		Silicon	2N3904
Q266	151-0188-00		Silicon	2N3906
Q282	151-0188-00		Silicon	2N3906
Q284	151-0188-00		Silicon	2N3906
Q287	151-0190-00		Silicon	2N3904
Q307	151-0190-00		Silicon	2N3904
Q312	151-0188-00		Silicon	2N3906
Q503	151-0190-00		Silicon	2N3904
Q511	151-0190-00		Silicon	2N3904
Q523	151-0190-00		Silicon	2N3904
Q524	151-0188-00		Silicon	2N3906
Q543	151-1007-00		FET	Dual
Q552	151-0188-00		Silicon	2N3906
Q561	151-0190-00		Silicon	2N3904
Q566	151-0188-00		Silicon	2N3906
Q582	151-0188-00		Silicon	2N3906
Q584	151-0188-00		Silicon	2N3906
Q587	151-0190-00		Silicon	2N3904
Q607	151-0190-00		Silicon	2N3904
Q612	151-0188-00		Silicon	2N3906
Q714	151-0188-00		Silicon	2N3906
Q724	151-0188-00		Silicon	2N3906
Q749	151-0190-00		Silicon	2N3904
Q759	151-0190-00		Silicon	2N3904
Q771	151-0150-00		Silicon	2N3440
Q775	151-0150-00		Silicon	2N3440
Q781	151-0150-00		Silicon	2N3440
Q785	151-0150-00		Silicon	2N3440

Transistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
Q793	151-0179-00			Silicon 2N3877 A
Q795	151-0179-00			Silicon 2N3877 A
Q828	151-0188-00			Silicon 2N3906
Q830	151-0188-00			Silicon 2N3906
Q836	151-0188-00			Silicon 2N3906
Q839	*151-0148-00			Silicon Selected from 40250 (RCA)
Q842	151-0188-00			Silicon 2N3906
Q844	151-0188-00			Silicon 2N3906
Q848	151-0188-00			Silicon 2N3906
Q853	151-0190-00			Silicon 2N3904
Q856	151-0188-00			Silicon 2N3906

Resistors

Resistors are fixed, composition, ±10% unless otherwise indicated.

R1	317-0511-00	510 Ω	1/8 W		5%
R3	315-0102-00	1 kΩ	1/4 W		5%
R8	315-0103-00	10 kΩ	1/4 W		5%
R9	315-0512-00	5.1 kΩ	1/4 W		5%
R10	315-0102-00	1 kΩ	1/4 W		5%
R12	315-0101-00	100 Ω	1/4 W		5%
R13	315-0331-00	330 Ω	1/4 W		5%
R15	315-0512-00	5.1 kΩ	1/4 W		5%
R17	315-0222-00	2.2 kΩ	1/4 W		5%
R19	315-0102-00	1 kΩ	1/4 W		5%
R20	315-0101-00	100 Ω	1/4 W		5%
R21	315-0363-00	36 kΩ	1/4 W		5%
R22	315-0512-00	5.1 kΩ	1/4 W		5%
R25	321-0684-00	15 kΩ	1/8 W	Prec	1/2%
R26	321-0684-00	15 kΩ	1/8 W	Prec	1/2%
R27	315-0471-00	470 Ω	1/4 W		5%
R29	315-0122-00	1.2 kΩ	1/4 W		5%
R30	311-0310-00	5 kΩ, Var			
R31	315-0123-00	12 kΩ	1/4 W		5%
R32	315-0511-00	510 Ω	1/4 W		5%
R33	315-0394-00	390 kΩ	1/4 W		5%
R34	315-0122-00	1.2 kΩ	1/4 W		5%
R36	315-0104-00	100 kΩ	1/4 W		5%
R38	315-0101-00	100 Ω	1/4 W		5%
R39	301-0563-00	56 kΩ	1/2 W		5%
R41	315-0472-00	4.7 kΩ	1/4 W		5%
R48	315-0432-00	4.3 kΩ	1/4 W		5%
R50	311-0607-00	10 kΩ, Var			
R51	315-0272-00	2.7 kΩ	1/4 W		5%
R53	315-0103-00	10 kΩ	1/4 W		5%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R59	315-0301-00			300 Ω	1/4 W		5%
R60	311-0633-00			5 kΩ, Var			
R61	315-0123-00			12 kΩ	1/4 W		5%
R63	315-0394-00			390 kΩ	1/4 W		5%
R64	315-0122-00			1.2 kΩ	1/4 W		5%
R66	315-0104-00			100 kΩ	1/4 W		5%
R68	315-0101-00			100 Ω	1/4 W		5%
R69	301-0563-00			56 kΩ	1/2 W		5%
R71	315-0472-00			4.7 kΩ	1/4 W		5%
R78	315-0432-00			4.3 kΩ	1/4 W		5%
R80	311-0607-00			10 kΩ, Var			
R81	315-0272-00			2.7 kΩ	1/4 W		5%
R83	315-0103-00			10 kΩ	1/4 W		5%
R89	315-0301-00			300 Ω	1/4 W		5%
R100	315-0910-00			91 Ω	1/4 W		5%
R101	317-0390-00			39 Ω	1/8 W		5%
R102	315-0682-00	B010100	B039999	6.8 kΩ	1/4 W		5%
R102	315-0622-00	B040000		6.2 kΩ	1/4 W		5%
R103	315-0821-00	B010100	B039999	820 Ω	1/4 W		5%
R103	315-0751-00	B040000		750 Ω	1/4 W		5%
R104	317-0510-00	B010100	B039999	51 Ω	1/8 W		5%
R104	317-0151-00	B040000		150 Ω	1/8 W		5%
R105	317-0390-00			39 Ω	1/8 W		5%
R107	301-0152-00	XB040000		1.5 kΩ	1/2 W		5%
R108	315-0122-00	B010100	B039999	1.2 kΩ	1/4 W		5%
R108	317-0151-00	B040000		150 Ω	1/8 W		5%
R109	315-0201-00	B010100	B039999	200 Ω	1/4 W		5%
R109	317-0331-00	B040000		330 Ω	1/8 W		5%
R110	317-0471-00	XB40000		470 Ω	1/8 W		5%
R111	317-0390-00			39 Ω	1/8 W		5%
R112	317-0102-00			1 kΩ	1/8 W		5%
R113	315-0821-00	B010100	B039999	820 Ω	1/4 W		5%
R113	315-0751-00	B040000		750 Ω	1/4 W		5%
R114	317-0510-00	B010100	B039999	51 Ω	1/8 W		5%
R114	301-0101-00	B040000		100 Ω	1/2 W		5%
R115	317-0390-00			39 Ω	1/8 W		5%
R117	315-0511-00	XB040000		510 Ω	1/4 W		5%
R118	315-0821-00	XB040000		820 Ω	1/4 W		5%
R119	315-0910-00	XB040000		91 Ω	1/4 W		
R121	321-0093-00			90.9 kΩ	1/8 W	Prec	1%
R123	301-0563-00			56 kΩ	1/2 W		5%
R125	321-0267-00			5.9 kΩ	1/8 W	Prec	1%
R127	321-0154-00			392 Ω	1/8 W	Prec	1%
R129	315-0512-00			5.1 kΩ	1/4 W		5%
R131	315-0101-00			100 Ω	1/4 W		5%
R132	315-0101-00			100 Ω	1/4 W		5%
R134	315-0123-00			12 kΩ	1/4 W		5%
R135	315-0153-00			15 kΩ	1/4 W		5%
R137	315-0101-00			100 Ω	1/4 W		5%
R138	321-0263-00			5.36 kΩ	1/8 W	Prec	1%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description			
R141	315-0222-00			2.2 kΩ	1/4 W		5%
R143	311-0702-00	B010100	B029999	250 Ω, Var			
R143	311-0095-00	B030000		500 Ω, Var			
R145A	321-0193-00			1 kΩ	1/8 W	Prec	1%
R145B	321-0231-00			2.49 kΩ	1/8 W	Prec	1%
R145C	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R145D	321-0289-00			10 kΩ	1/8 W	Prec	1%
R145E	321-0327-00			24.9 kΩ	1/8 W	Prec	1%
R145F	321-0356-00			49.9 kΩ	1/8 W	Prec	1%
R145G	321-0385-00			100 kΩ	1/8 W	Prec	1%
R147A	321-0450-01			475 kΩ	1/8 W	Prec	1/2%
R147B	321-0760-01			189.9 kΩ	1/8 W	Prec	1/2%
R147C	321-0759-01			95 kΩ	1/8 W	Prec	1/2%
R147D	321-0354-01			47.5 kΩ	1/8 W	Prec	1/2%
R147E	321-0757-01			18.99 kΩ	1/8 W	Prec	1/2%
R147F	321-0758-01			9.5 kΩ	1/8 W	Prec	1/2%
R147G	321-0258-01			4.75 kΩ	1/8 W	Prec	1/2%
R149	321-0354-01			47.5 kΩ	1/8 W	Prec	1/2%
R150	315-0392-00			3.9 kΩ	1/4 W		5%
R151[1]	311-0529-00			2.5 kΩ, Var			
R152	315-0202-00			2 kΩ	1/4 W		5%
R154	315-0101-00			100 Ω	1/4 W		5%
R156	301-0513-00			51 kΩ	1/2 W		5%
R158	321-0316-00			19.1 kΩ	1/8 W	Prec	1%
R159	321-0289-00			10 kΩ	1/8 W	Prec	1%
R161	321-0093-00			90.9 kΩ	1/8 W	Prec	1%
R163	301-0563-00			56 kΩ	1/2 W		5%
R165	321-0267-00			5.9 kΩ	1/8 W	Prec	1%
R167	321-0154-00			392 Ω	1/8 W	Prec	1%
R169	315-0512-00			5.1 kΩ	1/4 W		5%
R171	315-0101-00			100 Ω	1/4 W		5%
R172	315-0101-00			100 Ω	1/4 W		5%
R174	315-0123-00			12 kΩ	1/4 W		5%
R175	315-0153-00			15 kΩ	1/4 W		5%
R177	315-0101-00			100 Ω	1/4 W		5%
R178	321-0263-00			5.36 kΩ	1/8 W	Prec	1%
R181	315-0222-00			2.2 kΩ	1/4 W		5%
R183	311-0702-00	B010100	B029999	250 Ω, Var			
R183	311-0095-00	B030000		500 Ω, Var			
R185A	321-0193-00			1 kΩ	1/8 W	Prec	1%
R185B	321-0231-00			2.49 kΩ	1/8 W	Prec	1%
R185C	321-0260-00			4.99 kΩ	1/8 W	Prec	1%
R185D	321-0289-00			10 kΩ	1/8 W	Prec	1%
R185E	321-0327-00			24.9 kΩ	1/8 W	Prec	1%
R185F	321-0356-00			49.9 kΩ	1/8 W	Prec	1%
R185G	321-0385-00			100 kΩ	1/8 W	Prec	1%
R187A	321-0450-01			475 kΩ	1/8 W	Prec	1/2%
R187B	321-0760-01			189.9 kΩ	1/8 W	Prec	1/2%
R187C	321-0759-01			95 kΩ	1/8 W	Prec	1/2%
R187D	321-0354-01			47.5 kΩ	1/8 W	Prec	1/2%

[1]Furnished as a unit with R323.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R187E	321-0757-01			18.99 kΩ	1/8 W	Prec 1/2 %
R187F	321-0758-01			9.5 kΩ	1/8 W	Prec 1/2 %
R187G	321-0258-01			4.75 kΩ	1/8 W	Prec 1/2 %
R189	321-0354-01			47.5 kΩ	1/8 W	Prec 1/2 %
R190	315-0392-00			3.9 kΩ	1/4 W	5%
R191[2]	311-0529-00			2.5 kΩ, Var		
R192	315-0202-00			2 kΩ	1/4 W	5%
R194	315-0101-00			100 Ω	1/4 W	5%
R196	301-0513-00			51 kΩ	1/2 W	5%
R198	321-0316-00			19.1 kΩ	1/8 W	Prec 1%
R199	321-0289-00			10 kΩ	1/8 W	Prec 1%
R201	321-0420-00			232 kΩ	1/8 W	Prec 1%
R203	301-0563-00			56 kΩ	1/2 W	5%
R207	315-0122-00			1.2 kΩ	1/4 W	5%
R210	315-0101-00			100 Ω	1/4 W	5%
R213	315-0472-00			4.7 kΩ	1/4 W	1%
R215	321-0306-00			15 kΩ	1/8 W	Prec 1%
R219	315-0101-00			100 Ω	1/4 W	5%
R221	315-0101-00			100 Ω	1/4 W	5%
R224	315-0752-00			7.5 kΩ	1/4 W	5%
R225	315-0220-00			22 Ω	1/4 W	5%
R226	315-0752-00			7.5 kΩ	1/4 W	5%
R229	315-0101-00			100 Ω	1/4 W	5%
R231	321-0254-00			4.32 kΩ	1/8 W	Prec 1%
R232	321-0231-00			2.49 kΩ	1/8 W	Prec 1%
R233	321-0231-00			2.49 kΩ	1/8 W	Prec 1%
R234	321-0242-00			3.24 kΩ	1/8 W	Prec 1%
R236	317-0102-00			1 kΩ	1/8 W	5%
R238	317-0102-00			1 kΩ	1/8 W	5%
R241	315-0392-00			3.9 kΩ	1/4 W	5%
R243	301-0513-00			51 kΩ	1/2 W	5%
R244	321-1389-01			111 kΩ	1/8 W	Prec 1/2 %
R245	321-0304-00			14.3 kΩ	1/8 W	Prec 1%
R246	315-0471-00			470 Ω	1/4 W	5%
R247	311-0635-00			1 kΩ, Var		
R248	315-0471-00			470 Ω	1/4 W	5%
R249	321-0296-00			11.8 kΩ	1/8 W	Prec 1%
R251	315-0101-00			100 Ω	1/4 W	5%
R253	315-0102-00			1 kΩ	1/4 W	5%
R255	315-0241-00			240 Ω	1/4 W	5%
R257	301-0513-00			51 kΩ	1/2 W	5%
R259	315-0241-00			240 Ω	1/4 W	5%
R261	315-0101-00			100 Ω	1/4 W	5%
R263	315-0101-00			100 Ω	1/4 W	5%
R265	315-0101-00			100 Ω	1/4 W	5%
R267	315-0101-00			100 Ω	1/4 W	5%
R271	322-1389-01			111 kΩ	1/4 W	Prec 1/2 %
R272	321-0283-00			8.66 kΩ	1/8 W	Prec 1%
R274	321-0292-00			10.7 kΩ	1/8 W	Prec 1%

[2]Furnished as a unit with R623.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R275	323-1389-01			111 kΩ	½ W	Prec ½%
R280	321-1289-07			10.1 kΩ	⅛ W	Prec 1/10%
R283	321-0303-00			14 kΩ	⅛ W	Prec 1%
R285	321-0409-00			178 kΩ	⅛ W	Prec 1%
R286	315-0222-00			2.2 kΩ	¼ W	5%
R287	308-0320-00			15.6 kΩ	3 W	WW 1%
R288	321-1289-07			10.1 kΩ	⅛ W	Prec 1/10%
R293[3]	*311-0693-00			10 kΩ, Var		
R298	321-0745-03			25.05 kΩ	⅛ W	Prec ¼%
R299	321-1310-03			16.7 kΩ	⅛ W	Prec ¼%
R301	311-0609-00			2 kΩ, Var		
R303	315-0132-00			1.3 kΩ	¼ W	5%
R304	321-1389-01			111 kΩ	⅛ W	Prec ½%
R305	315-0681-00			680 Ω	¼ W	5%
R307	315-0124-00			120 kΩ	¼ W	5%
R312	308-0320-00			15.6 kΩ	3 W	WW 1%
R315	315-0101-00			100 Ω	¼ W	5%
R318	321-0309-00			16.2 kΩ	⅛ W	Prec 1%
R321	321-0319-00			20.5 kΩ	⅛ W	Prec 1%
R323[4]	311-0529-00			2.5 kΩ, Var		
R332	315-0203-00			20 kΩ	¼ W	5%
R334	315-0204-00			200 kΩ	¼ W	5%
R501	321-0420-00			232 kΩ	⅛ W	Prec 1%
R503	301-0563-00			56 kΩ	½ W	5%
R507	315-0122-00			1.2 kΩ	¼ W	5%
R510	315-0101-00			100 Ω	¼ W	5%
R513	315-0472-00			4.7 kΩ	¼ W	5%
R515	321-0306-00			15 kΩ	⅛ W	Prec 1%
R519	315-0101-00			100 Ω	¼ W	5%
R521	315-0101-00			100 Ω	¼ W	5%
R524	315-0752-00			7.5 kΩ	¼ W	5%
R525	315-0220-00			22 Ω	¼ W	5%
R526	315-0752-00			7.5 kΩ	¼ W	5%
R529	315-0101-00			100 Ω	¼ W	5%
R531	321-0254-00			4.32 kΩ	⅛ W	Prec 1%
R532	321-0231-00			2.49 kΩ	⅛ W	Prec 1%
R533	321-0231-00			2.49 kΩ	⅛ W	Prec 1%
R534	321-0242-00			3.24 kΩ	⅛ W	Prec 1%
R536	317-0102-00			1 kΩ	⅛ W	5%
R538	317-0102-00			1 kΩ	⅛ W	5%

[3]Furnished as a unit with SW293.

[4]Furnished as a unit with R151.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R541	315-0392-00			3.9 kΩ	1/4 W	5%
R543	301-0513-00			51 kΩ	1/2 W	5%
R544	321-1389-01			111 kΩ	1/8 W Prec	1/2%
R545	321-0304-00			14.3 kΩ	1/8 W Prec	1%
R546	315-0471-00			470 Ω	1/4 W	5%
R547	311-0635-00			1 kΩ, Var		
R548	315-0471-00			470 Ω	1/4 W	5%
R549	321-0296-00			11.8 kΩ	1/8 W Prec	1%
R551	315-0101-00			100 Ω	1/4 W	5%
R553	315-0102-00			1 kΩ	1/4 W	5%
R555	315-0241-00			240 Ω	1/4 W	5%
R557	301-0513-00			51 kΩ	1/2 W	5%
R559	315-0241-00			240 Ω	1/4 W	5%
R561	315-0101-00			100 Ω	1/4 W	5%
R563	315-0101-00			100 Ω	1/4 W	5%
R565	315-0101-00			100 Ω	1/4 W	5%
R567	315-0101-00			100 Ω	1/4 W	5%
R571	322-1389-01			111 kΩ	1/4 W Prec	1/2%
R572	321-0283-00			8.66 kΩ	1/8 W Prec	1%
R574	321-0292-00			10.7 kΩ	1/8 W Prec	1%
R575	323-1389-01			111 kΩ	1/2 W Prec	1/2%
R580	321-1289-07			10.1 kΩ	1/8 W Prec	1/10%
R583	321-0303-00			14 kΩ	1/8 W Prec	1%
R585	321-0409-00			178 kΩ	1/8 W Prec	1%
R586	315-0222-00			2.2 kΩ	1/4 W	5%
R587	308-0320-00			15.6 kΩ	3 W WW	1%
R588	321-1289-07			10.1 kΩ	1/8 W Prec	1/10%
R593[5]	*311-0693-00			10 kΩ, Var		
R598	321-0745-03			25.05 kΩ	1/8 W Prec	1/4%
R599	321-1310-03			16.7 kΩ	1/8 W Prec	1/4%
R601	311-0609-00			2 kΩ, Var		
R603	315-0132-00			1.3 kΩ	1/4 W	5%
R604	321-1389-01			111 kΩ	1/8 W Prec	1/2%
R605	315-0681-00			680 Ω	1/4 W	5%
R607	315-0124-00			120 kΩ	1/4 W	5%
R612	308-0320-00			15.6 kΩ	3 W WW	1%
R615	315-0101-00			100 Ω	1/4 W	5%
R618	321-0309-00			16.2 kΩ	1/8 W Prec	1%
R621	321-0319-00			20.5 kΩ	1/8 W Prec	1%
R623[6]	311-0529-00			2.5 kΩ, Var		
R641	321-0289-00			10 kΩ	1/8 W Prec	1%
R701	315-0203-00			20 kΩ	1/4 W	5%
R703	315-0100-00			10 Ω	1/4 W	5%
R707	315-0222-00			2.2 kΩ	1/4 W	5%
R708	315-0223-00			22 kΩ	1/4 W	5%

[5]Furnished as a unit with SW593.

[6]Furnished as a unit with R191.

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R709	315-0103-00			10 kΩ	1/4 W	5%
R711	315-0101-00			100 Ω	1/4 W	5%
R713	315-0101-00			100 Ω	1/4 W	5%
R715	315-0562-00			5.6 kΩ	1/4 W	5%
R718	315-0244-00			240 kΩ	1/4 W	5%
R719	315-0153-00			15 kΩ	1/4 W	5%
R723	315-0101-00			100 Ω	1/4 W	5%
R725	315-0562-00			5.6 kΩ	1/4 W	5%
R728	315-0244-00			240 kΩ	1/4 W	5%
R729	315-0153-00			15 kΩ	1/4 W	5%
R748	321-0295-00			11.5 kΩ	1/8 W Prec	1%
R749	321-0250-00			3.92 kΩ	1/8 W Prec	1%
R753	321-0254-00			4.32 kΩ	1/8 W Prec	1%
R756	311-0635-00			1 kΩ, Var		
R758	321-0293-00			11 kΩ	1/8 W Prec	1%
R759	321-0250-00			3.92 kΩ	1/8 W Prec	1%
R762	321-0249-00			3.83 kΩ	1/8 W Prec	1%
R764	311-0608-00			2 kΩ, Var		
R766	311-0607-00			10 kΩ, Var		
R767	315-0333-00			33 kΩ	1/4 W	5%
R769	315-0223-00			22 kΩ	1/4 W	5%
R771	301-0303-00			30 kΩ	1/2 W	5%
R772	301-0303-00			30 kΩ	1/2 W	5%
R777	323-0409-00			178 kΩ	1/2 W Prec	1%
R779	301-0164-00			160 kΩ	1/2 W	5%
R780	321-0284-00			8.87 kΩ	1/8 W Prec	1%
R781	301-0303-00			30 kΩ	1/2 W	5%
R782	301-0303-00			30 kΩ	1/2 W	5%
R787	301-0164-00			160 kΩ	1/2 W	5%
R789	301-0164-00			160 kΩ	1/2 W	5%
R791	315-0304-00			300 kΩ	1/4 W	5%
R793	315-0304-00			300 kΩ	1/4 W	5%
R795	315-0624-00			620 kΩ	1/4 W	5%
R797	315-0106-00			10 MΩ	1/4 W	5%
R801	301-0473-00			47 kΩ	1/2 W	5%
R802	315-0102-00			1 kΩ	1/4 W	5%
R804	315-0101-00			100 Ω	1/4 W	5%
R808	315-0101-00			100 Ω	1/4 W	5%
R810	315-0100-00			10 Ω	1/4 W	5%
R812	315-0100-00			10 Ω	1/4 W	5%
R820	308-0406-00			1.2 kΩ	3 W WW	1%
R823	307-0103-00			2.7 Ω	1/4 W	5%
R825	307-0103-00			2.7 Ω	1/4 W	5%
R826	315-0101-00			100 Ω	1/4 W	5%
R827	321-0184-00			806 Ω	1/8 W Prec	1%

Resistors *(cont)*

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description		
R828	315-0101-00			100 Ω	¼ W	5%
R829	321-0253-00			4.22 kΩ	⅛ W Prec	1%
R831	321-0296-00			11.8 kΩ	⅛ W Prec	1%
R833	321-0203-00			1.27 kΩ	⅛ W Prec	1%
R834	311-0442-00			250 Ω, Var		
R835	321-0184-00			806 Ω	⅛ W Prec	1%
R837	315-0102-00			1 kΩ	¼ W	5%
R841	321-0408-00			174 kΩ	⅛ W Prec	1%
R843	321-0684-00			15 kΩ	⅛ W Prec	½%
R845	321-0684-00			15 kΩ	⅛ W Prec	½%
R846	321-0756-03			50 kΩ	⅛ W Prec	¼%
R847	317-0102-00			1 kΩ	⅛ W	5%
R848	308-0253-00			1.32 kΩ	3 W WW	5%
R849	308-0393-00			1.6 kΩ	3 W WW	5%
R850	317-0102-00			1 kΩ	⅛ W	5%
R851	308-0421-00			3 kΩ	3 W WW	5%
R853	308-0304-00			1.5 kΩ	3 W WW	1%
R855	315-0114-00			110 kΩ	¼ W	5%
R857	321-0761-03			35 kΩ	⅛ W Prec	¼%
R858	321-0755-03			65 kΩ	⅛ W Prec	¼%
R870	315-0330-00			33 Ω	¼ W	5%
R872	315-0101-00			100 Ω	¼ W	5%
R876	315-0101-00			100 Ω	¼ W	5%
R880	315-0330-00			33 Ω	¼ W	5%
R882	315-0101-00			100 Ω	¼ W	5%
R886	315-0101-00			100 Ω	¼ W	5%

Switches

	Unwired or Wired	Tektronix Part No.		
SW6		260-0878-00	Slide	SAMPLING MODE
SW107		260-0816-00	Slide	TRIG OUT
SW146[7]	Wired	*262-0827-00	Rotary	ATTENUATOR A
SW146		260-0914-00	Rotary	ATTENUATOR A
SW186[8]	Wired	*262-0827-00	Rotary	ATTENUATOR B
SW186		260-0914-00	Rotary	ATTENUATOR B
SW290		260-0516-00	Micro	SPDT
SW293[9]		*311-0693-00		
SW590		260-0516-00	Micro	SPDT
SW593[10]		*311-0693-00		
SW730A,B	Wired	*262-0828-00	Rotary	DUAL TRACE
SW730A,B		260-0913-00	Rotary	DUAL TRACE

[7]Furnished as a unit with SW293 and R293.

[8]Furnished as a unit with SW593 and R593.

[9]Furnished as a unit with R293.

[10]Furnished as a unit with R593.

Test Points

Ckt. No.	Tektronix Part No.	Serial/Model No. Eff	Disc	Description
TP24	*214-0579-00			Pin, Test Point
TP121	*214-0579-00			Pin, Test Point
TP139	*214-0579-00			Pin, Test Point
TP155	*214-0579-00			Pin, Test Point
TP161	*214-0579-00			Pin, Test Point
TP179	*214-0579-00			Pin, Test Point
TP195	*214-0579-00			Pin, Test Point
TP235	*214-0579-00			Pin, Test Point
TP279	*214-0579-00			Pin, Test Point
TP287	*214-0579-00			Pin, Test Point
TP313	*214-0579-00			Pin, Test Point
TP535	*214-0579-00			Pin, Test Point
TP579	*214-0579-00			Pin, Test Point
TP587	*214-0579-00			Pin, Test Point
TP613	*214-0579-00			Pin, Test Point
TP707	*214-0579-00			Pin, Test Point
TP714	*214-0579-00			Pin, Test Point
TP724	*214-0579-00			Pin, Test Point
TP775	*214-0579-00			Pin, Test Point
TP785	*214-0579-00			Pin, Test Point

Transformers

T3	*120-0546-00	Toroid, 4 turns, bifilar
T235	*120-0547-00	Toroid, (4) 15 turn windings
T535	*120-0547-00	Toroid, (4) 15 turn windings
T821	*120-0545-00	Power

Cable Assemblies

W101	*175-0480-00	8½ inch
W104	*179-1243-00	Trigger Out
W111	*175-0482-00	4 inch

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations which appear either on the back of the diagrams or on pullout pages immediately following the diagrams of the instruction manual.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the Description column.

Assembly and/or Component
Detail Part of Assembly and/or Component
mounting hardware for Detail Part
Parts of Detail Part
mounting hardware for Parts of Detail Part
mounting hardware for Assembly and/or Component

Mounting hardware always appears in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

Mounting hardware must be purchased separately, unless otherwise specificed.

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial or model number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ABBREVIATIONS AND SYMBOLS

For an explanation of the abbreviations and symbols used in this section, please refer to the page immediately preceding the Electrical Parts List in this instruction manual.

INDEX OF MECHANICAL PARTS LIST ILLUSTRATIONS

(Located behind diagrams)

SECTION 8
MECHANICAL PARTS LIST

FIG. 1 EXPLODED

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	Description
1-1	333-1032-01			1	PANEL, front
-2	386-1334-00			1	PLATE, sub-panel front
-3	366-0109-00			1	KNOB, aluminum securing
	- - - - - -			-	knob includes:
	213-0005-00			1	SCREW, set, 8-32 x 1/8 inch, HSS
-4	214-0052-00			1	FASTENER, pawl right, w/stop
	- - - - - -			-	mounting hardware: (not included w/fastener)
	210-0004-00			2	LOCKWASHER, internal, #4
	210-0406-00			2	NUT, hex., 4-40 x 3/16 inch
-5	136-0140-00			4	SOCKET, banana jack
	- - - - - -			-	mounting hardware for each: (not included w/socket)
-6	210-0895-00			1	BUSHING, banana jack socket
	210-0940-00			1	WASHER, flat, 1/4 ID x 3/8 inch OD
	210-0583-00			2	NUT, hex., 1/4-32 x 5/16 inch
-7	210-0269-00			1	LUG, solder, 0.257 ID non-locking
	129-0035-00			1	ASSEMBLY, ground post
	- - - - - -			-	assembly includes:
-8	200-0103-00			1	CAP, knurled, 1/4-28 x 3/8 ID x 11/32 inch long
	210-0046-00			1	LOCKWASHER, internal, 0.261 ID x 0.400 inch OD
	210-0455-00			1	NUT, hex., 1/4-28 x 3/8 inch
-9	355-0507-00			1	STEM, 1/4-28 x 13/16 inch long
	- - - - - -			-	mounting hardware: (not included w/assembly)
-10	210-0269-00			1	LUG, solder, 0.257 inch ID, non-locking
-11	352-0084-00			2	HOLDER, plastic, neon
-12	200-0609-00			2	COVER, neon holder
-13	378-0541-00			2	FILTER, lens, neon
-14	366-0365-00			1	KNOB, red—INVERT FULL
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-15	366-0322-00			1	KNOB, gray—ATTENUATOR
	- - - - - -			-	knob includes:
	213-0004-00			1	SCREW, set, 6-32 x 3/16 inch, HSS
-16	262-0827-00			1	SWITCH, wired—ATTENUATOR
	- - - - - -			-	switch includes:
	260-0914-00			1	SWITCH, unwired
-17	384-0688-00			1	SHAFT, 3.97 inches long
-18	351-0107-00			1	GUIDE, plastic, variable resistor
	- - - - - -			-	mounting hardware: (not included w/guide)
	210-0001-00			2	LOCKWASHER, internal, #2
-19	210-0405-00			2	NUT, hex., 2-56 x 3/16 inch
-20	214-0749-00			1	SPRING, detent

FIG. 1 EXPLODED *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
	210-0255-00			1		LUG, solder, 3/8 ID x 0.500 inch OD, SE
	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
-21	366-0319-00			1		KNOB, red—DC OFFSET ±1 V
	- - - - - -			-		knob includes:
	213-0020-00			1		SCREW, set, 6-32 x 1/8 inch, HSS
-22	366-0408-00			1		KNOB, gray—B POSITION
	- - - - - -			-		knob includes:
	213-0048-00			1		SCREW, set, 4-40 x 1/8 inch, HSS
-23	- - - - - -			1		RESISTOR, variable
	- - - - - -			-		mounting hardware: (not included w/resistor)
-24	210-0207-00			1		LUG, solder, 3/8 ID x 5/8 inch OD, SE
-25	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
-26	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
	200-0263-00	XB030240		1		COVER, dust, variable resistor (not shown)
-27	366-0189-00			1		KNOB, red—NORMAL SMOOTH
	- - - - - -			-		knob includes:
	213-0020-00			1		SCREW, set, 6-32 x 1/8 inch, HSS
-28	366-0322-00			1		KNOB, gray—DUAL TRACE
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, 6-32 x 3/16 inch, HSS
-29	262-0828-00			1		SWITCH, wired—DUAL TRACE
	- - - - - -			-		switch includes:
	260-0913-00			1		SWITCH, unwired
	- - - - - -			-		mounting hardware: (not included w/switch)
-30	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
-31	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
-32	366-0319-00			1		KNOB, red—DC OFFSET ±1 V
	- - - - - -			-		knob includes:
	213-0020-00			1		SCREW, set, 6-32 x 1/8 inch, HSS
-33	366-0408-00			1		KNOB, gray—A POSITION
	- - - - - -			-		knob includes:
	213-0408-00			1		SCREW, 4-40 x 1/8 inch, HSS
-34	- - - - - -			1		RESISTOR, variable
	- - - - - -			-		mounting hardware: (not included w/resistor)
-35	210-0207-00			1		LUG, solder, 3/8 ID x 5/8 inch OD, SE
-36	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
-37	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
	200-0263-00	XB030240		1		COVER, dust, variable resistor (not shown)

FIG. 1 EXPLODED *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-38	366-0365-00			1		KNOB, red—INVERT PULL
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-39	366-0322-00			1		KNOB, gray—ATTENUATOR
	- - - - - -			-		knob includes:
	213-0004-00			1		SCREW, set, 6-32 x 3/16 inch, HSS
-40	262-0827-00			1		SWITCH, wired—ATTENUATOR
	- - - - - -			-		switch includes:
	260-0914-00			1		SWITCH, unwired
-41	384-0688-00			1		SHAFT, 3.97 inches long
-42	351-0107-00			1		GUIDE, plastic, variable resistor
	- - - - - -			-		mounting hardware: (not included w/guide)
	210-0001-00			2		LOCKWASHER, internal, #2
-43	210-0405-00			2		NUT, hex., 2-56 x 3/16 inch
-44	214-0749-00			1		SPRING, detent
	- - - - - -			-		mounting hardware: (not included w/switch)
	210-0012-00			1		LOCKWASHER, internal, 3/8 ID x 1/2 inch OD
	210-0978-00			1		WASHER, flat, 3/8 ID x 1/2 inch OD
	210-0255-00			1		LUG, solder, 3/8 ID x 0.500 inch OD, SE
	210-0590-00			1		NUT, hex., 3/8-32 x 7/16 inch
-45	366-0283-00			1		KNOB, gray—DOT RESPONSE
-46	366-0283-00			1		KNOB, gray—B DELAY
-47	366-0283-00			1		KNOB, gray—DOT RESPONSE
-48	- - - - - -			3		RESISTOR, variable
	- - - - - -			-		mounting hardware for each: (not included w/resistor)
	213-0020-00			1		SCREW, set, 6-32 x 1/8 inch, HSS
-49	- - - - - -			1		RESISTOR, variable
	- - - - - -			-		mounting hardware: (not included w/resistor)
-50	210-0471-00			1		NUT, hex., 1/4-32 x 5/16 x 19/32 inch long
-51	210-0046-00			1		LOCKWASHER, internal, 0.261 ID x 0.400 inch OD
-52	358-0054-00			1		BUSHING, variable resistor mounting
-53	260-0816-00			1		SWITCH, slide—TRIG OUT
	- - - - - -			-		mounting hardware: (not included w/switch)
-54	210-0405-00			2		NUT, hex., 2-56 x 3/16 inch
-55	351-0132-00			2		GUIDE, plastic, circuit board
-56	131-0581-00			2		CONNECTOR, 12 pin
	- - - - - -			-		mounting hardware for each: (not included w/connector)
-57	211-0082-00			2		SCREW, thread forming, 4-40 x 1/2 inch PHS
	210-0201-00			1		LUG, solder, SE #4
-58	386-1333-00			1		PLATE, chassis support
-59	343-0088-00			2		CLAMP, cable, small snap-in
-60	348-0115-00			2		GROMMET, plastic, "U" shaped

FIG. 1 EXPLODED *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-61	260-0878-00			1		SWITCH, slide—SAMPLING MODE
	- - - - - -			-		mounting hardware: (not included w/switch)
-62	211-0101-00			2		SCREW, 4-40 x 1/4 inch, 100° csk, FHS
	210-0406-00			2		NUT, hex., 4-40 x 3/16 inch
-63	384-0615-00			4		ROD, spacer, plug-in
-64	179-1242-00			1		CABLE HARNESS, switch w/connectors
-65	179-1243-00			1		CABLE HARNESS, trigger out w/connectors
-66	670-0170-00			1		ASSEMBLY, circuit board—VERTICAL
	- - - - - -			-		assembly includes:
	388-0925-00			1		BOARD, circuit
	214-0506-00			44		PIN, connector, straight, male
-67	214-0579-00			15		PIN, test point
-68	136-0220-00			30		SOCKET, transistor, 3 pin
-69	136-0235-00			4		SOCKET, transistor, 6 pin
	- - - - - -			-		mounting hardware: (not included w/assembly)
-70	211-0116-00			8		SCREW, sems, 4-40 x 5/16 inch, PHB
-71	441-0765-00			1		CHASSIS, vertical
	- - - - - -			-		mounting hardware: (not included w/chassis)
-72	211-0504-00			5		SCREW, 6-32 x 1/4 inch, PHS
-73	358-0215-00			2		BUSHING, plastic, horseshoe
-74	260-0516-00			2		SWITCH, micro
	- - - - - -			-		mounting hardware for each: (not included w/switch)
-75	213-0181-00			2		SCREW, thread forming, #2 x 3/8 inch, PHS
-76	- - - - - -			1		TRANSFORMER
	- - - - - -			-		mounting hardware: (not included w/transformer)
-77	211-0131-00			2		SCREW, 4-40 x 7/8 inch, PHS
-78	214-0843-00			1		BAR, mounting, tapped, 4-40
-79	- - - - - -			1		TRANSISTOR
	- - - - - -			-		mounting hardware: (not included w/transistor)
-80	211-0504-00			2		SCREW, 6-32 x 1/4 inch, PHS
-81	210-0457-00			2		NUT, keps, 6-32 x 5/16 inch
-82	344-0118-00			1		CLIP, capacitor mounting
	- - - - - -			-		mounting hardware: (not included w/clip)
-83	213-0044-00			1		SCREW, thread forming, 5-32 x 3/16 inch, PHS

FIG. 1 EXPLODED *(cont)*

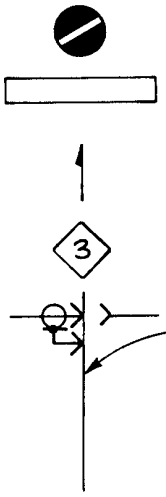
Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-84	670-0172-00	B010100	B039999	1		ASSEMBLY, circuit board—TRIGGER
	670-0172-01	B040000		1		ASSEMBLY, circuit board—TRIGGER
	- - - - - -			-		assembly includes:
	388-0959-00	B010100	B039999	1		BOARD, circuit
	388-0959-01	B040000		1		BOARD, circuit
-85	131-0391-00			3		CONNECTOR, stand-off, male
	214-0506-00			5		PIN, connector, straight, male
	- - - - - -			-		mounting hardware: (not included w/assembly)
-86	344-0131-00			3		CLIP, plastic, mounting
-87	213-0088-00			3		SCREW, thread forming, 5-32 x 1/4 inch, PHS
-88	175-0480-00			1		CABLE ASSEMBLY, RF, 8 1/2 inches long w/connectors
	- - - - - -			-		mounting hardware: (not included w/cable assembly)
	354-0331-00	XB030250		1		SNAP, ring (not shown)
	343-0190-00	XB030250		1		RETAINER, connector (not shown)
-89	175-0482-00			1		CABLE ASSEMBLY, RF, 4 inches long w/connectors
	- - - - - -			-		mounting hardware: (not included w/cable assembly)
	354-0331-00			1		SNAP, ring (not shown)
	343-0190-00			1		RETAINER, connector (not shown)
-90	348-0063-00			1		GROMMET, plastic, 1/2 inch diameter
-91	441-0764-00			1		CHASSIS, control
	- - - - - -			-		mounting hardware: (not included w/chassis)
-92	211-0504-00			5		SCREW, 6-32 x 1/4 inch, PHS
-93	670-0171-00			1		ASSEMBLY, circuit board—CONTROL
	- - - - - -			-		assembly includes:
	388-0926-00			1		BOARD, circuit
-94	131-0391-00			3		CONNECTOR, stand-off, male
-95	136-0183-00			4		SOCKET, transistor, 3 pin
-96	136-0220-00			17		SOCKET, transistor, 3 pin
-97	136-0235-00			3		SOCKET, transistor, 6 pin
-98	214-0506-00			63		PIN, connector, straight, male
-99	214-0579-00			8		PIN, test point
	200-0116-00			4		COVER, transistor, shrink-on (not shown)
	- - - - - -			-		mounting hardware: (not included w/assembly)
-100	211-0116-00			8		SCREW, sems, 4-40 x 5/16 inch, PHB
-101	179-1241-00			1		CABLE HARNESS, digital power, w/connectors
-102	351-0037-00			1		GUIDE, plastic, plug-in
	- - - - - -			-		mounting hardware: (not included w/guide)
-103	211-0013-00			1		SCREW, 4-40 x 3/8 inch, RHS
-104	210-0586-00			1		NUT, keps, 4-40 x 1/4 inch
-105	387-0595-00			1		PLATE, rear
	- - - - - -			-		mounting hardware: (not included w/plate)
-106	212-0044-00			4		SCREW, 8-32 x 1/2 inch, RHS

FIG. 1 EXPLODED *(cont)*

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
1-107	131-0149-00			1		CONNECTOR, 24 pin
	- - - - - -			-		mounting hardware: (not included w/connector)
-108	211-0016-00			2		SCREW, 4-40 x 5/8 inch, RHS
-109	166-0032-00			2		SPACER, 1/4 OD x 5/16 inch long
-110	210-0586-00			2		NUT, keps, 4-40 x 1/4 inch
-111	131-0149-00			1		CONNECTOR, 24 pin
	- - - - - -			-		mounting hardware: (not included w/connector)
-112	211-0008-00			2		SCREW, 4-40 x 3/16 inch, RHS
-113	210-0586-00			2		NUT, keps, 4-40 x 1/4 inch
-114	210-0202-00			1		LUG, solder, SE #6
	- - - - - -			-		mounting hardware: (not included w/lug)
-115	211-0504-00			1		SCREW, 6-32 x 1/4 inch, PHS
-116	210-0407-00			1		NUT, hex., 6-32 x 1/4 inch
-117	200-0256-00			1		COVER, capacitor, 1 inch diameter x 2 1/32 inch long
-118	200-0820-00			1		BEZEL, dual sampling head
	- - - - - -			-		mounting hardware: (not included w/bezel)
-119	343-0153-00			6		CLAMP, rim clenching
	210-0004-00			6		LOCKWASHER, internal, #4
	210-0406-00			6		NUT, hex., 4-40 x 3/16 inch
-120	343-0154-00			1		CLAMP, bezel

SECTION 9
DIAGRAMS

The following symbols are used on the diagrams:



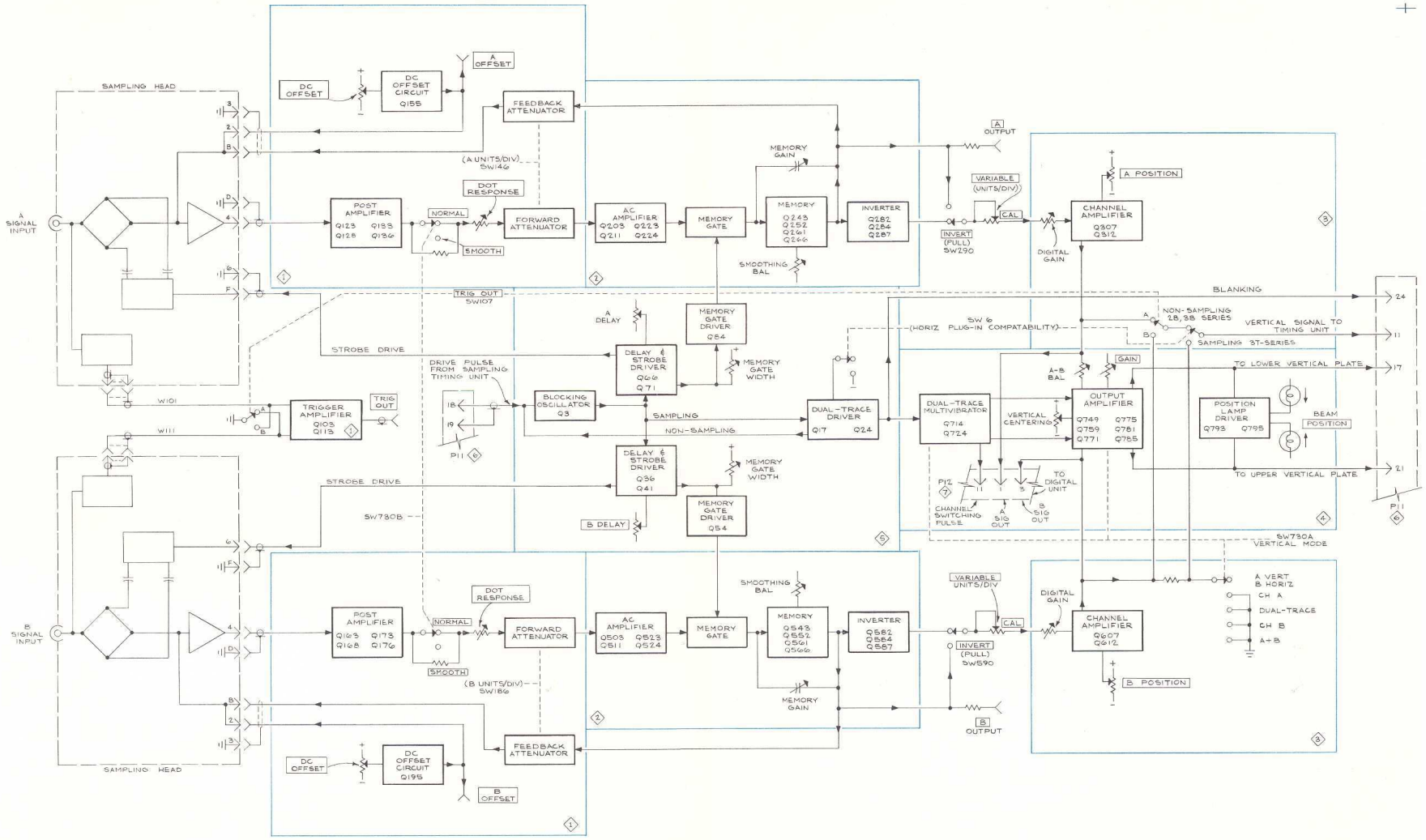
Screwdriver adjustment

Front panel control or connector

Clockwise control rotation in direction of arrow

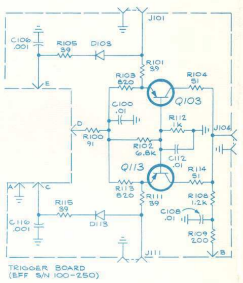
Refer to indicated diagram

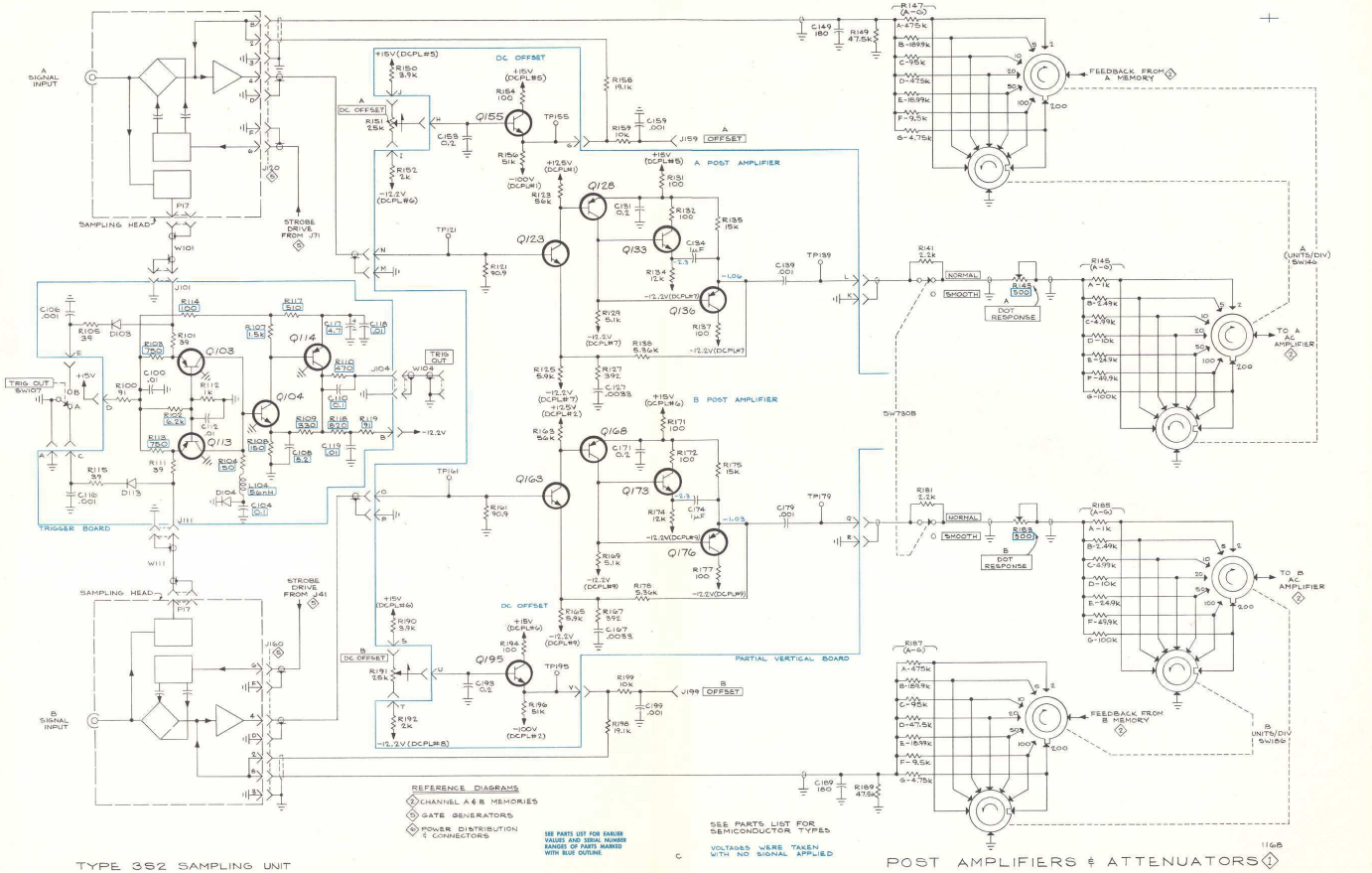
Blue line encloses components located on circuit board



TYPE 3S2 SAMPLING UNIT

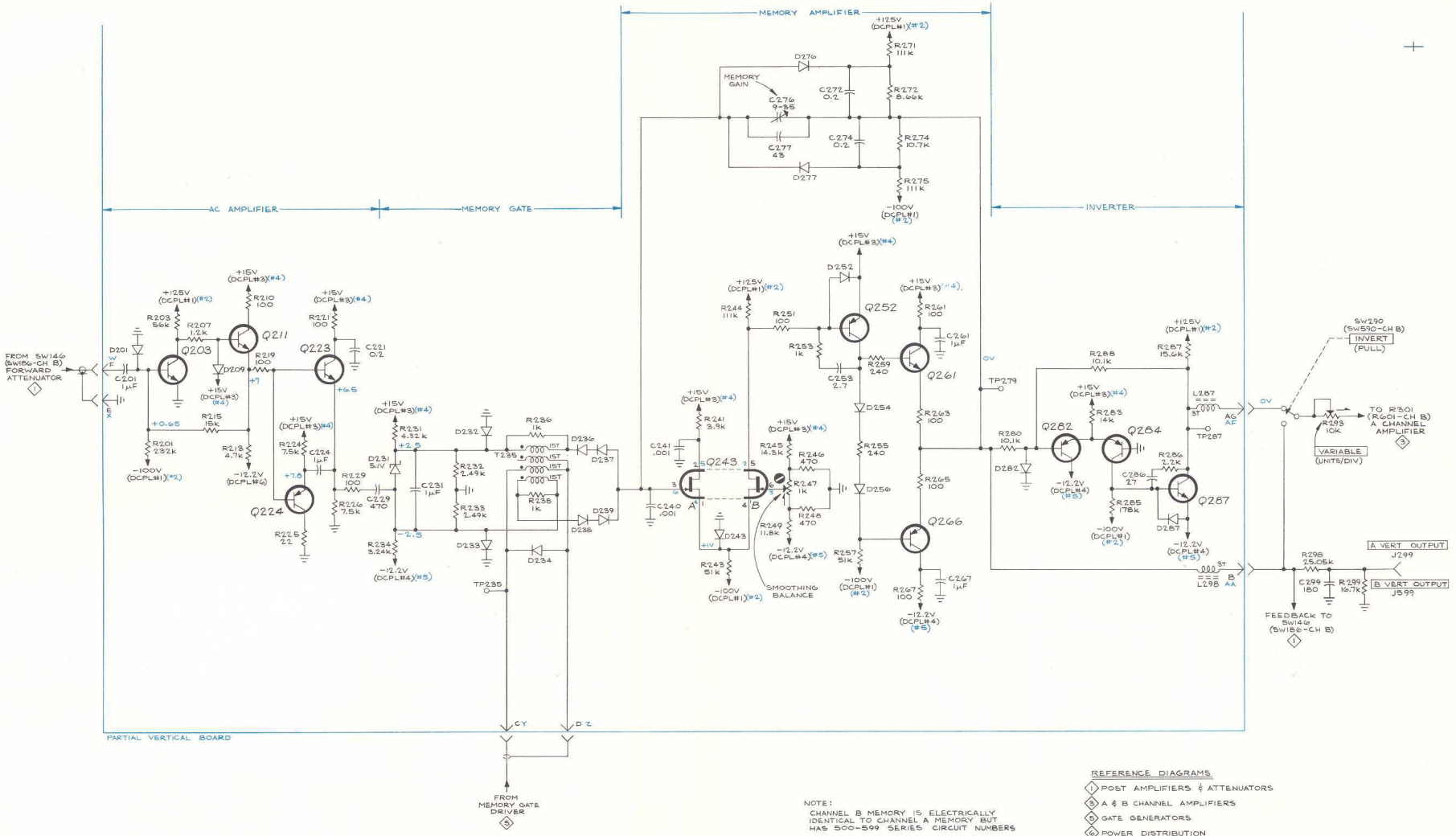
BLOCK DIAGRAM





TYPE 352 SAMPLING UNIT

POST AMPLIFIERS & ATTENUATORS



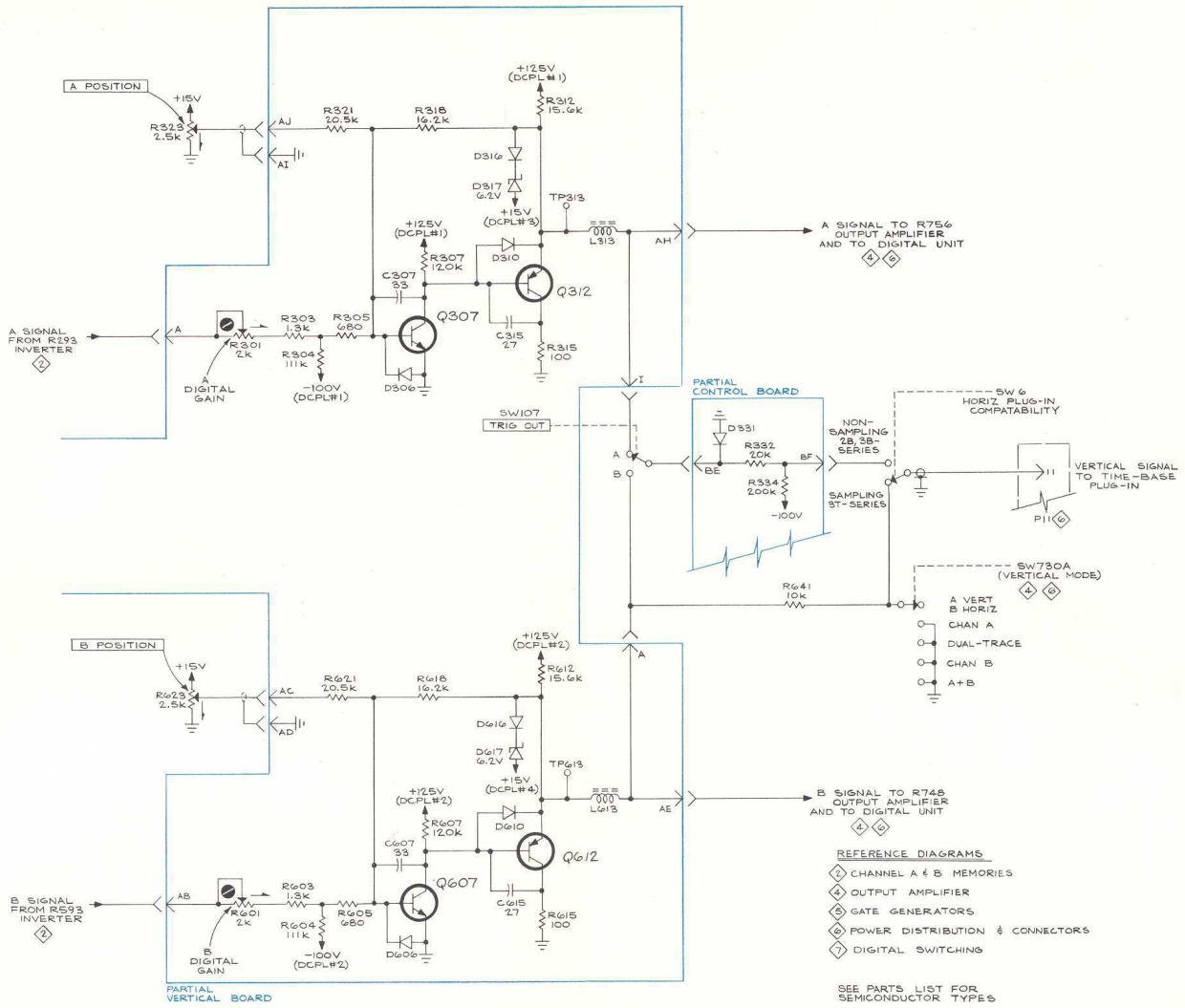
NOTE:
CHANNEL B MEMORY IS ELECTRICALLY IDENTICAL TO CHANNEL A MEMORY BUT HAS 500-599 SERIES CIRCUIT NUMBERS

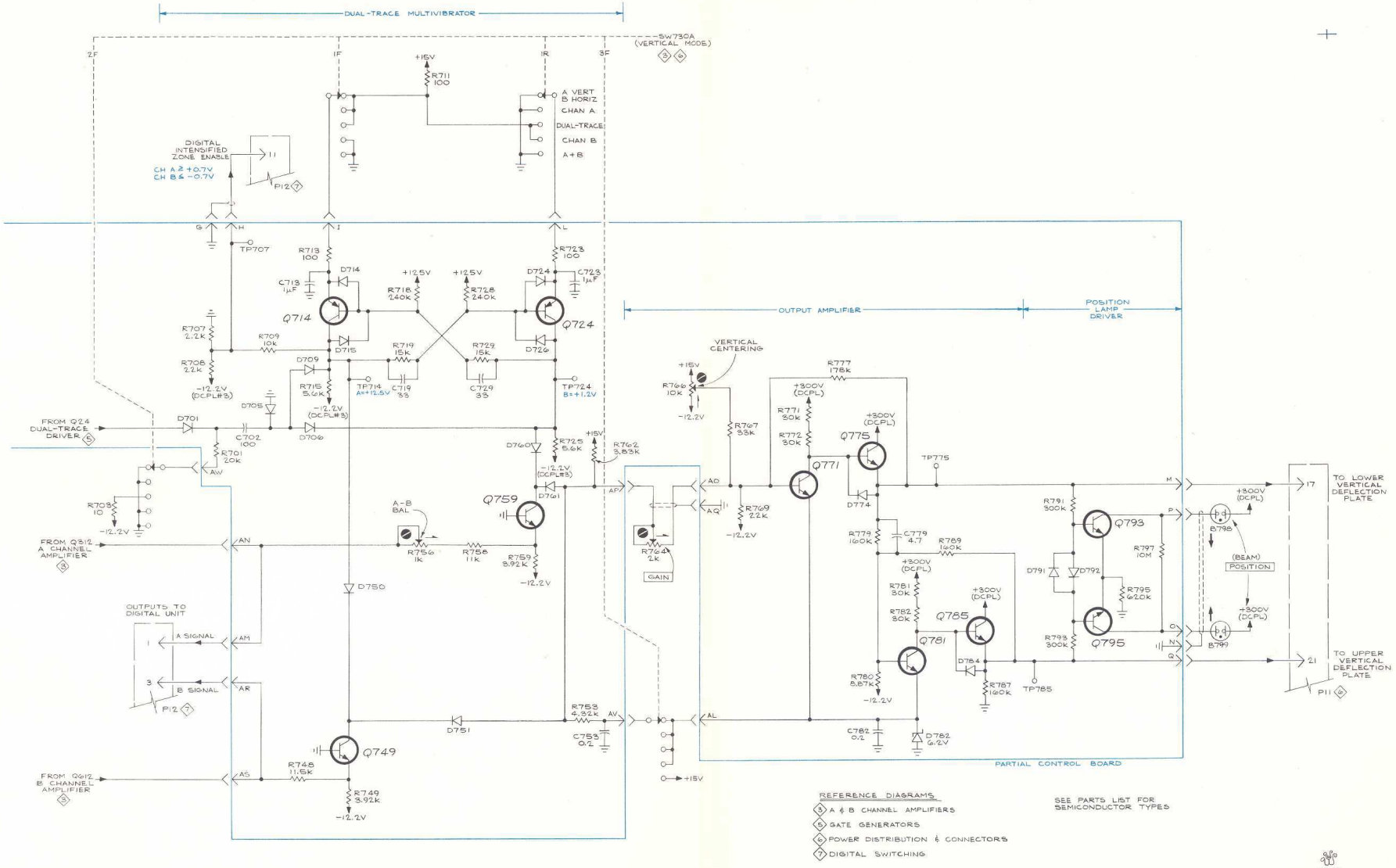
CHANNEL B PIN CONNECTORS & SUPPLY VOLTAGES ARE LETTERED IN BLUE

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

OPERATING VOLTAGES APPLY AFTER DC OFFSET CONTROL IS SET FOR ZERO VOLTS AT OFFSET JACK.

REFERENCE DIAGRAMS
1. POST AMPLIFIERS & ATTENUATORS
3. A & B CHANNEL AMPLIFIERS
5. GATE GENERATORS
6. POWER DISTRIBUTION & CONNECTORS


A POSITION
+15V
R323 2.5k
AJ
AI
R321 20.5k
R318 16.2k
+125V (DCPL#1)
R312 15.6k
D316
D317 6.2V
+15V (DCPL#3)
TP313
L313
AH
A SIGNAL TO R756 OUTPUT AMPLIFIER AND TO DIGITAL UNIT
4 6
+125V (DCPL#1)
R307 12.0k
D310
C307 33
Q312
Q307
A SIGNAL FROM R293 INVERTER
2
A
R301 2k
A DIGITAL GAIN
R303 1.3k
R304 111k
R305 680
-100V (DCPL#1)
D306
C315 27
R315 100
I
PARTIAL CONTROL BOARD
SW107
TRIG OUT
A
B
D331
R332 20k
R334 200k
-100V
BE
BF
NON-SAMPLING 28,38-SERIES
SAMPLING 3T-SERIES
SW 6 HORIZ PLUG-IN COMPATABILITY
VERTICAL SIGNAL TO TIME-BASE PLUG-IN
P11 6
SW730A (VERTICAL MODE)
4 6
R641 10k
A VERT
B HORIZ
CHAN A
DUAL-TRACE
CHAN B
A+B
A
B POSITION
+15V
R623 2.5k
AC
AD
R621 20.5k
R618 16.2k
+125V (DCPL#2)
R612 15.6k
D616
D617 6.2V
+15V (DCPL#4)
TP613
L613
AE
B SIGNAL TO R748 OUTPUT AMPLIFIER AND TO DIGITAL UNIT
4 6
+125V (DCPL#2)
R607 12.0k
D610
C607 33
Q612
Q607
B SIGNAL FROM R593 INVERTER
2
AB
R601 2k
B DIGITAL GAIN
R603 1.3k
R604 111k
R605 680
-100V (DCPL#2)
D606
C615 27
R615 100
PARTIAL VERTICAL BOARD
REFERENCE DIAGRAMS
2 CHANNEL A & B MEMORIES
4 OUTPUT AMPLIFIER
5 GATE GENERATORS
6 POWER DISTRIBUTION & CONNECTORS
7 DIGITAL SWITCHING
SEE PARTS LIST FOR SEMICONDUCTOR TYPES

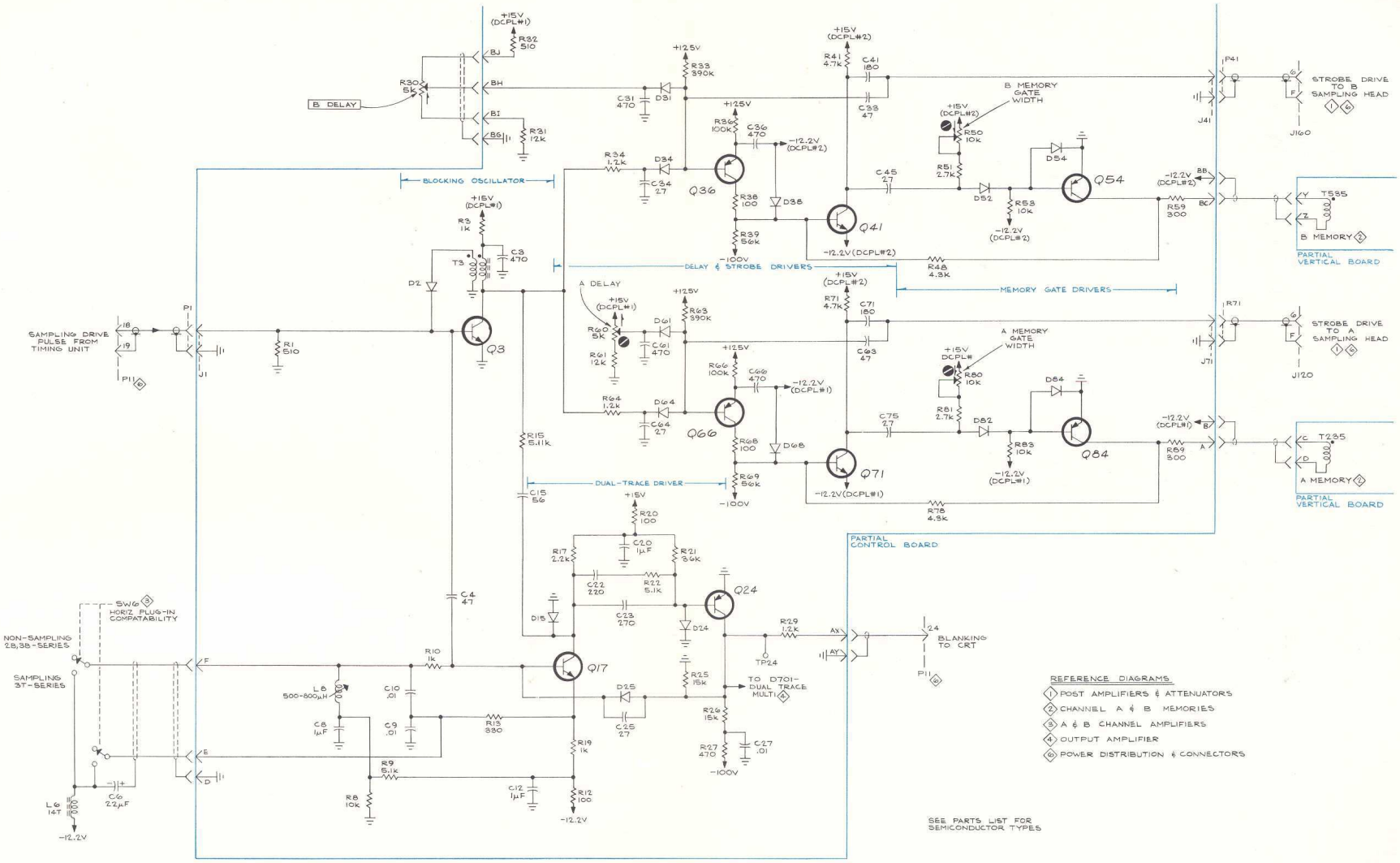


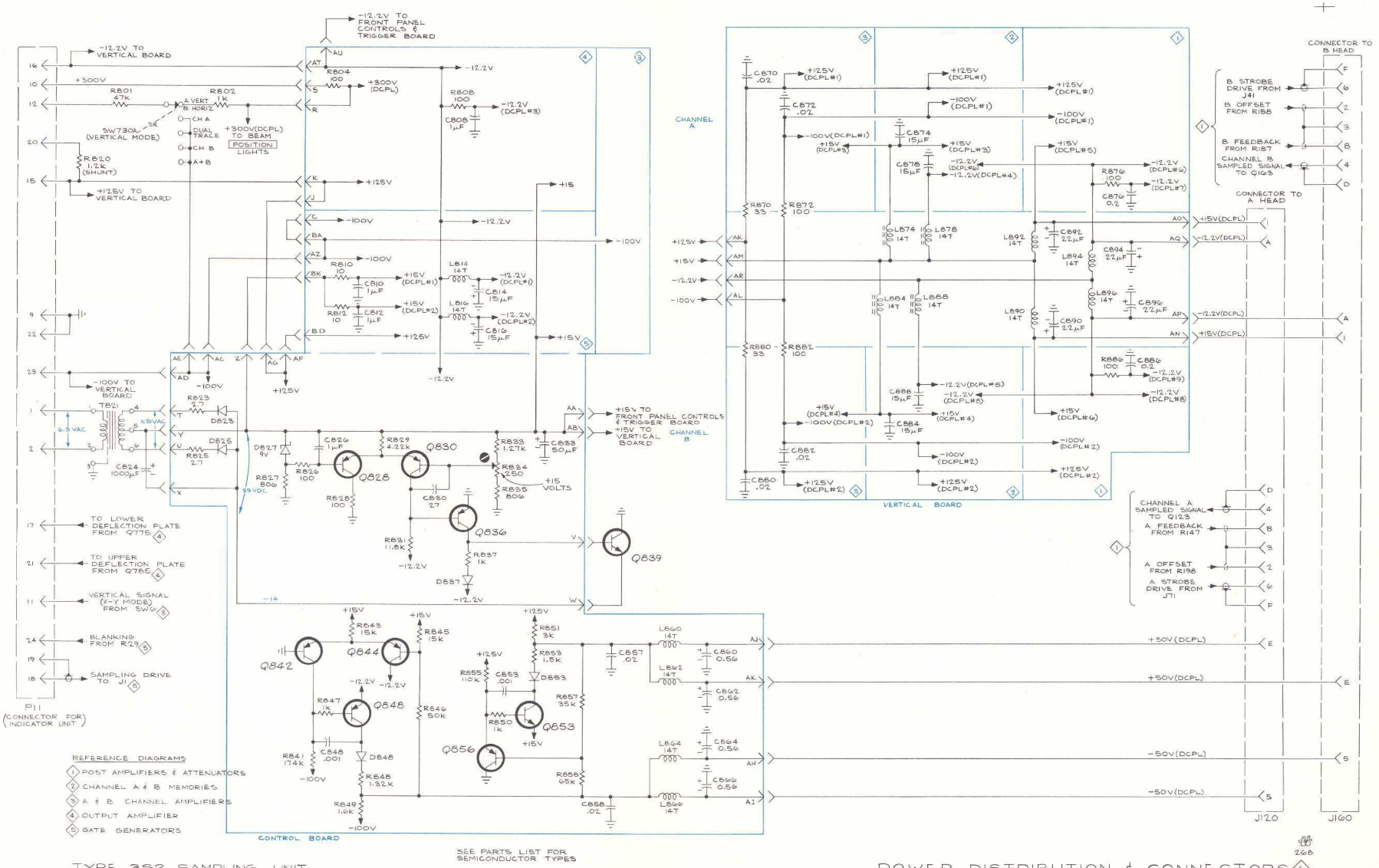
TYPE 352 SAMPLING UNIT

A

OUTPUT AMPLIFIER 4

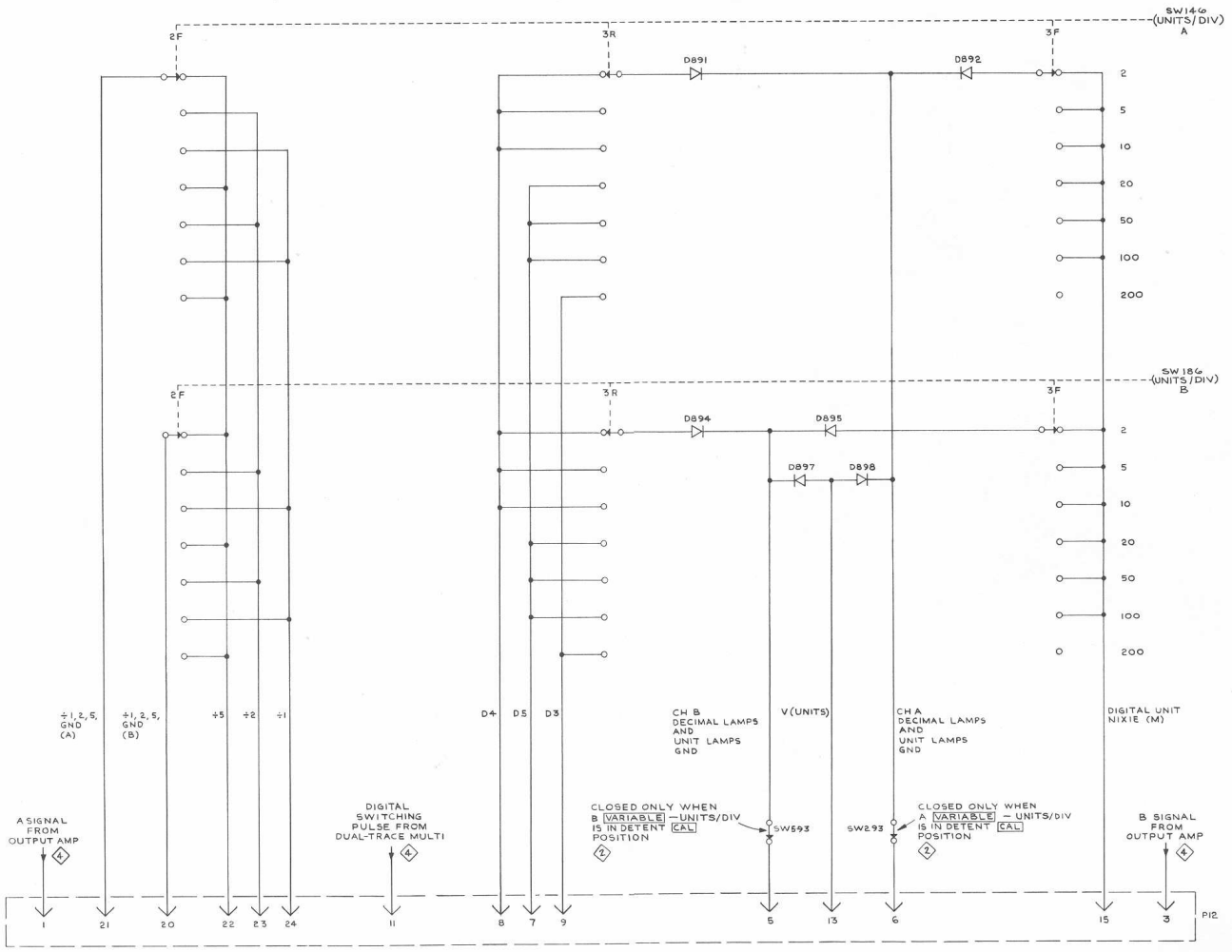
268


B DELAY
BLOCKING OSCILLATOR
DELAY & STROBE DRIVERS
MEMORY GATE DRIVERS
DUAL-TRACE DRIVER
A DELAY
B MEMORY GATE WIDTH
A MEMORY GATE WIDTH
SAMPLING DRIVE PULSE FROM TIMING UNIT
STROBE DRIVE TO B SAMPLING HEAD
STROBE DRIVE TO A SAMPLING HEAD
B MEMORY
A MEMORY
PARTIAL VERTICAL BOARD
PARTIAL CONTROL BOARD
BLANKING TO CRT
TO D701- DUAL TRACE MULTI
NON-SAMPLING 28,38-SERIES
SAMPLING 3T-SERIES
HORIZ PLUG-IN COMPATABILITY
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
REFERENCE DIAGRAMS
1 POST AMPLIFIERS & ATTENUATORS
2 CHANNEL A & B MEMORIES
3 A & B CHANNEL AMPLIFIERS
4 OUTPUT AMPLIFIER
6 POWER DISTRIBUTION & CONNECTORS



TYPE 3S2 SAMPLING UNIT

POWER DISTRIBUTION & CONNECTORS 6



REFERENCE DIAGRAMS

2 CHANNEL A & B MEMORIES

4 OUTPUT AMPLIFIER

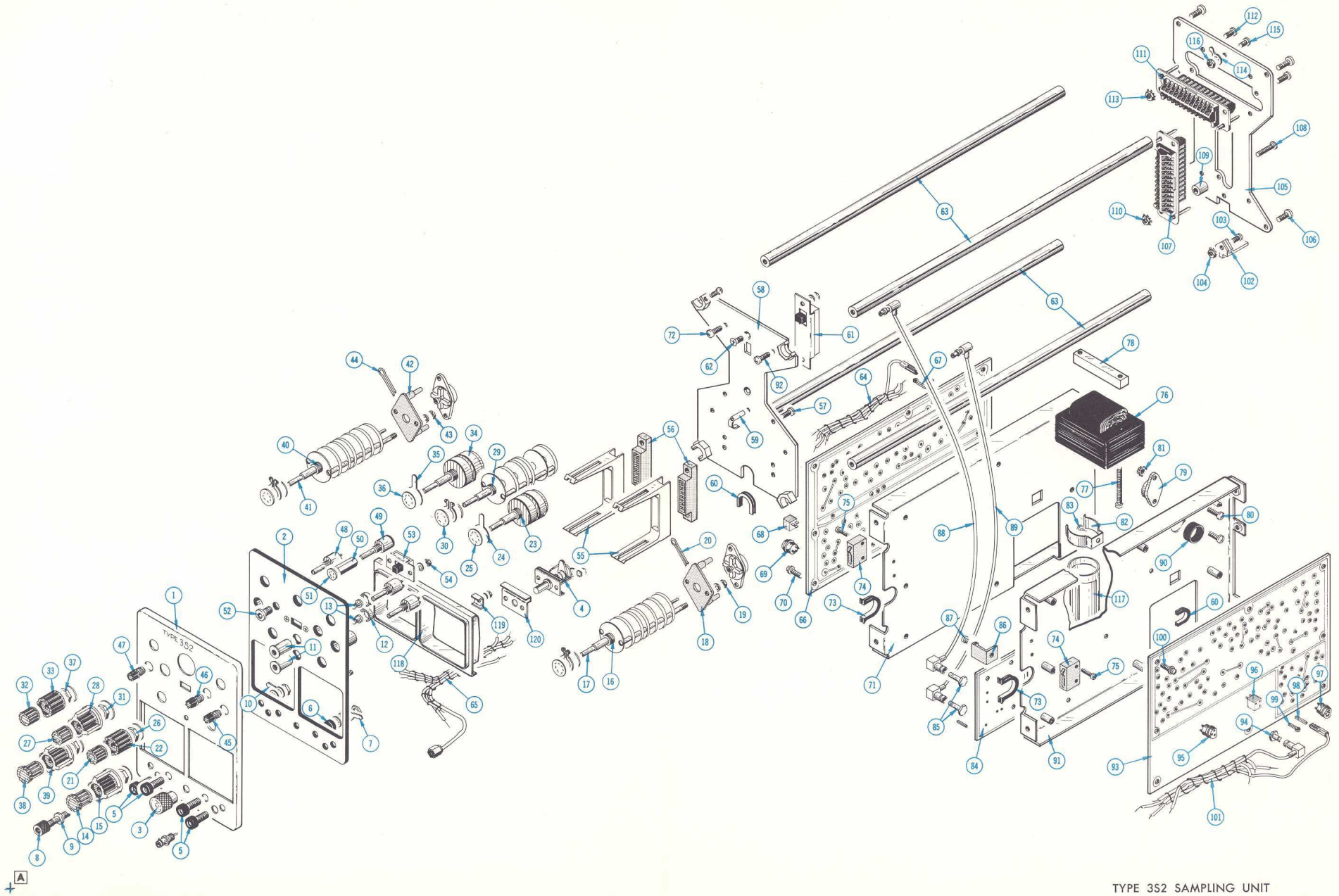
TYPE 3S2 SAMPLING UNIT

DIGITAL SWITCHING 7

2-68

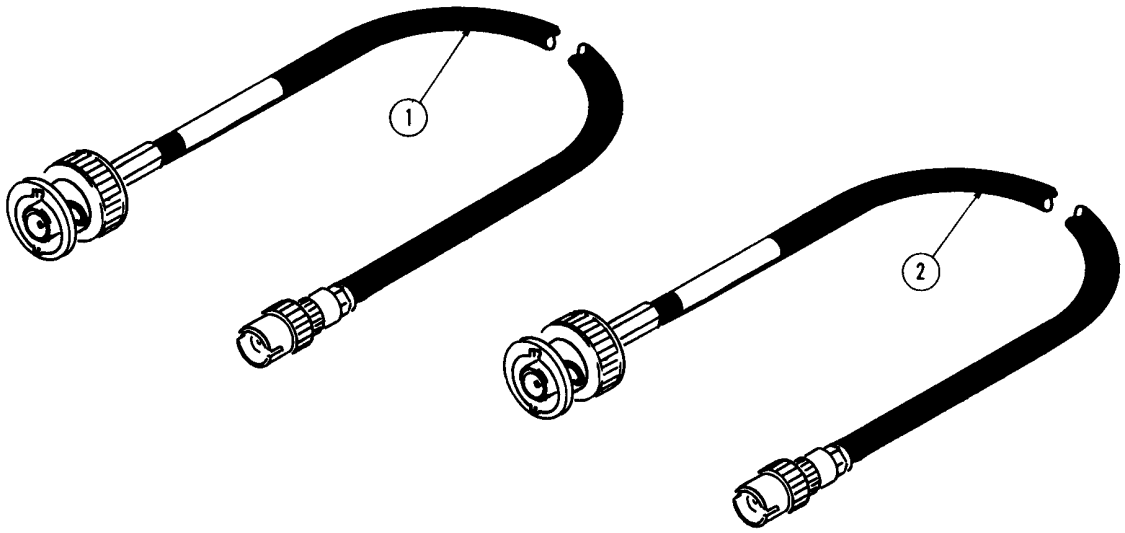
A

FIG. 1 EXPLODED



TYPE 3S2 SAMPLING UNIT

FIG. 2 STANDARD ACCESSORIES



[A]

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Serial/Model No. Disc	Qty	1 2 3 4 5	Description
2-1	012-0127-00			1		CABLE ASSEMBLY, RF, 18.5 inches long
-2	012-0128-00			1		CABLE ASSEMBLY, RF, 10 inches long
	070-0759-00			2		MANUAL, instruction (not shown)

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

SAMPLING HEADS

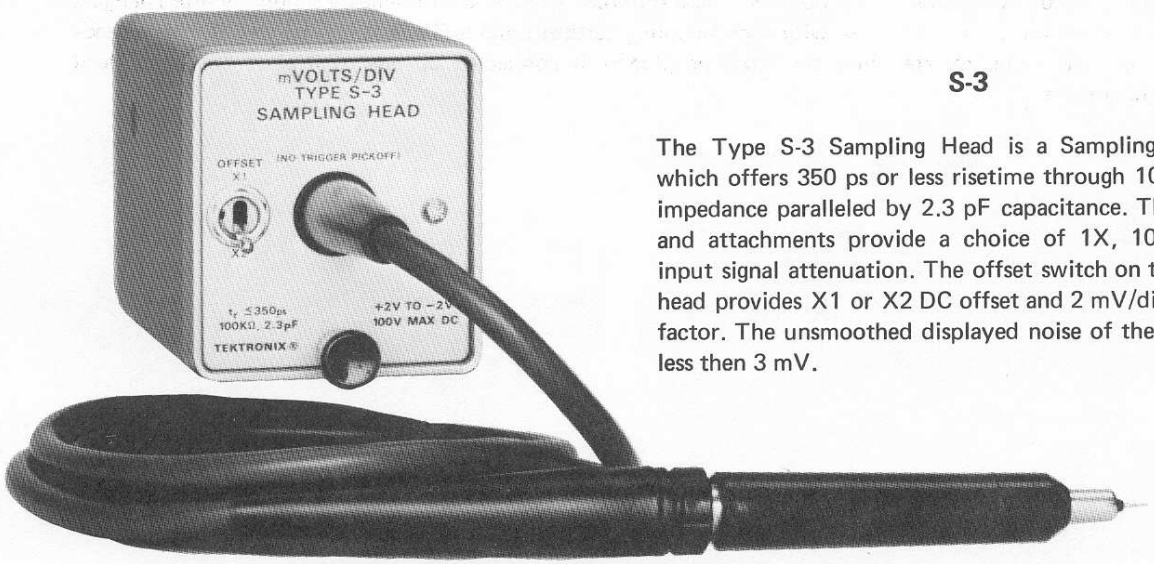
Tektronix sampling systems utilizing sampling heads offer a wide variety of performance features. Among these are several different risetimes, special low-noise display features, various attenuations, pulse generators and trigger countdown options. These different features are obtainable simply by interchanging heads. Heads are designed for use with such sampling vertical units as Types 3S2, 3S5 and 3S6. The heads can be used either inserted into the sampling plug-in or connected outside of it via a Sampling Head extender cable.

S-1

The S-1 Sampling Head has a risetime of 50 ps or less with unsmoothed random noise less than 2 mV at an input impedance of 50 Ω. The head is equipped with an internal trigger pickoff to provide a trigger signal output from the plug-in unit. When the Type S-1 is used in conjunction with a Random Sampling Sweep unit, the system will display a triggering event without use of a delay line or a pretrigger.

S-2

The S-2 Sampling Head has a risetime of 50 ps or less, unsmoothed random noise less than 6 mV through an input impedance of 50 Ω. The Type S-2 is equipped with an internal trigger pickoff to provide a trigger signal output from the plug-in unit. When the Type S-2 is used with a Random Sampling Sweep unit, the sampling system will display a triggering event without use of either delay lines or a pretrigger.



S-3

The Type S-3 Sampling Head is a Sampling-probe unit which offers 350 ps or less risetime through 100 kΩ input impedance paralleled by 2.3 pF capacitance. The probe tip and attachments provide a choice of 1X, 10X or 100X input signal attenuation. The offset switch on the sampling head provides X1 or X2 DC offset and 2 mV/div deflection factor. The unsmoothed displayed noise of the Type S-3 is less then 3 mV.

S-4

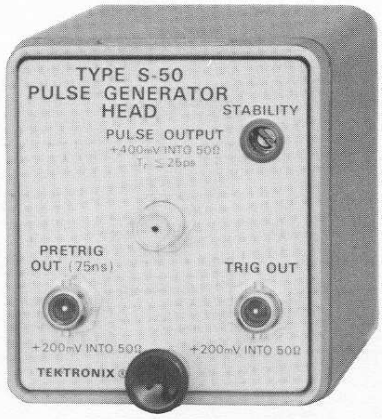
The Type S-4 Sampling Head has a risetime of 25 ps or less through 50 Ω input impedance. The unsmoothed displayed random noise is less than 5 mV. The unit is equipped with an internal trigger pickoff to provide trigger signal output from the plug-in unit. When the Type S-4 is used with a Random Sampling Sweep unit, the sampling system will display a triggering event without use of either delay lines or a pretrigger.

S-5

The Type S-5 Sampling Head may be used where extremely low noise high impedance applications are needed. Using the Type S-5, displayed random noise is 500 μV or less. The risetime of the sampling head is 1 ns or less with an input resistance of 1 MΩ paralleled by 15 pF capacitance. The unit is shipped with a Tektronix P6010 Probe and offers both AC and DC input coupling.

S-50

The Type S-50 is a pulse generator head which produces a positive-going pulse having risetime of 25 ps or less. The pulse amplitude is at least 400 mV into 50 Ω impedance, having a duration of 100 ns with a repetition rate of 25 kHz. The unit has both a pretrigger out jack and a trigger out jack. The pretrigger output risetime is 400 ps or less. The positive-going pretrigger pulse has an amplitude of at least 180 mV into 50 Ω. The trigger output is a positive-going pulse having a risetime of 200 ps or less with an amplitude of at least 200 mV into 50 Ω.



S-51

The Type S-51 is a trigger countdown head designed to provide stable sampling displays of signals from 1 GHz to 18 GHz. The Trigger Countdown output is available on both front and rear panels of the unit. The output signal is a direct countdown of the input and permits triggering by a standard sampling sweep unit.