## TEKTRONIX

## 100 MHz COUNTER

 DC 501INSTRUETION MANUAL

## INSTRUCTION <br> MANUAL

## 100 MHz COUNTER DC 501

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## OPERATING INSTRUCTIONS

## DC 501 General Description

The DC 501100 MHz Counter measures frequency from 10 Hz to 100 MHz , and totalizes (counts number of events) from 0 to $10^{7}$ at a maximum rate of 100 MHz . Seven 7 -segment light-emitting diodes (LED's) provide a visual numerical display. The decimal point is automatically positioned and leading zeros (to the left of the most significant digit or decimal point) are blanked. Digit overflow is indicated by a front-panel LED. Signals to be counted can be applied via a front-panel BNC connector into an impedance of $1 \mathrm{M} \Omega$ and 20 pF or via the rear connector into an impedance of about $50 \Omega$ and 20 pF . The DC 501 is designed to operate in a TM 500 -Series Power Module only.

## Preparation

The DC 501 is ready for use as it is received. To install, align the upper and lower rails of the DC 501 with the plug-in compartment tracks of the power module, and insert it fully. To remove, pull the release latch to disengage the DC 501 from the power module. Connect the power module cord to a suitable line-voltage source.

## Basic Operation

## NOTE

Refer to the Controls and Connectors pullout page. Also, additional information is given later in this section.

Display Check. Press the RESET button to check the 7 character segments of each digit; the numerical display should be a row of eights. To check the decimal point position and the units indicators, set the MEASUREMENT INTERVAL switch as follows:

| Switch Position | Numerical Display | Units |
| :---: | :---: | :---: |
| .01 SEC | .0000 | MHz |
| .1 SEC | .00000 | MHz |
| 1 SEC | .000 | kHz |
| 10 SEC | .0000 | kHz |
| MANUAL | 000 |  |

In the MANUAL position, no decimal point will be displayed. Press the START button and check that the GATE indicator lights, then release the button (STOP) and
check that the GATE light goes out. To check the OVERFLOW indicator, set the MEASUREMENT INTERVAL switch to 10 s , the INPUT switch to EXT, and apply a $15-$ or $20-\mathrm{MHz}$ signal to the INPUT connector. The length of time a display can be held is determined by the DISPLAY TIME control, and will be discussed in the next few paragraphs.

Frequency Measurements. The DC 501 provides direct measurement of the average frequency of signals from about 10 Hz to 100 MHz . The input sensitivity is 300 mV peak to peak, so select the proper attenuation (X1, X5, $X 10$, or $X 50$ ) for the given signal. Other input characteristics are given on page 1-3.


The input signal must not exceed 500 volts.

Set the INPUT switch to EXT and apply a signal to the INPUT connector. Set the MEASUREMENT INTERVAL switch to the .01 SEC position and observe the numerical readout display. Adjust the TRIGGER LEVEL control for a stable reading. The zeroes leading the most significant digit in the display should be blanked. Then turn the MEASUREMENT INTERVAL switch to the position that gives the desired reading. Generally, use the shorter measurement intervals for high-frequency, low-resolution measurements and longer intervals for measurements requiring a high resolution. For instruments having the Automatic Gate option, the measurement interval is selected automatically when the MEASUREMENT INTERVAL switch is set to the AUTO position.

## NOTE

The OVERFLOW indicator can be lit for highresolution measurements, allowing the frequency to be indicated to 0.1 Hz . Refer to the Electrical Characteristics at the end of this section for resolution and accuracy at each position of the MEASUREMENT INTERVAL switch.

The display is updated at a rate determined by the DISPLAY TIME control. Each time a sample of the input signal is taken, the GATE light will flash and the new
reading will be displayed. To change the display time, which is continuously variable from about 0.1 second to 10 seconds, or to hold a display indefinitely, turn the DISPLAY TIME control.

Totalizing (Counting Number of Events). The DC 501 will display the accumulated number of pulses applied to the External or Internal input circuit up to $9,999,999$ pulses. Input signal rate should not exceed 100 MHz . Before applying the signal, set the MEASUREMENT INTERVAL switch to MANUAL. Apply the signal and push the START button. The GATE indicator will light and the progressing count will be displayed. Adjust the ATTEN and TRIGGER LEVEL controls as necessary to obtain a steady count. To stop the counting, release the START button. The GATE light will go out and the displayed count will be held. The displayed count will continue by pressing the START button again. The counter can be reset to zero at any time by pushing the RESET button.

## Signal Connection

Coaxial cables and probes offer very convenient means of connecting the signals to the front-panel INPUT BNC connector. These devices are shielded to prevent pickup of electrostatic interference. A 10X attenuation probe not only reduces the size of the input signal, but is also presents a high input impedance to allow the circuit under test to perform very close to normal operating conditions:

Input and output data access to the DC 501 is made via the plug-in connector contacts at the rear of the main circuit board. Fig. 1-1 identifies the contacts and their associated input/output assignments. An optional multi-pin connector, to which these data can be hard-wired to provide external access, is available to install on the rear panel of the power module.

## Input Attenuation and Trigger Level Adjustment

Signals to be counted may have a wide variety of shapes and amplitudes, many of which are unsuitable to drive the counting circuits. Because of this, the signal is first passed through an attenuator, then applied to a signal-shaping circuit which converts it to rectangular pulses of uniform amplitude. This circuit includes a reference level adjustable between + and -2 volts to which the incoming signal is compared, allowing the 300 -millivolt sensitivity window of the signal-shaping circuit to be adjusted to a convenient amplitude on the incoming waveform (see Fig. 1-2). Obtaining a steady, reliable reading is dependent upon the proper selection of input attenuation and proper adjustment of the TRIGGER LEVEL control.

Generally, the best point on a waveform for triggering the counter is where the slope is steep and therefore usually free of noise. On a sine-wave signal, for example, the
steepest slope occurs at the zero-crossing point. Noise pulses or other signal components of sufficient amplitude to produce unwanted trigger pulses will cause an erratic or incorrect count. Fig. 1-2 shows the TRIGGER LEVEL control adjusted to avoid error. In critical measurement applications, monitor the incoming signal with a test oscilloscope.

## Measurement Interval and Display Time Controls

The MEASUREMENT INTERVAL switch selects the time interval (also called gate time) during which the DC 501 counts. The internal time-base circuit derives gate times from an accurate $1-\mathrm{MHz}$ reference signal to make frequency measurements. These gate times are $0.01 \mathrm{~s}, 0.1 \mathrm{~s}$, 1 s , or 10 s . The measurement interval selected determines the measurement range and resolution. Also, the displayed decimal point is positioned correctly and the correct measurement units ( MHz or kHz ) are indicated for the corresponding switch position.


Fig. 1-1. Input/Output assignments of plug-in connector contacts.


Fig. 1-2. Two examples of triggering circuit output showing how proper adjustment of TRIGGERING LEVEL control can avoid an erroneous count.

The DISPLAY TIME control sets the length of time a measurement can be held in the counter and displayed. The HOLD detent position allows a measurement to be held indefinitely, or until the counter is reset to zero by the front-panel RESET button.

## Optional Features

Option 1-0.5 P/M 5 MHz Crystal Oscillator. The DC 501 can be ordered with a temperature-compensated crystal oscillator to provide a highly stable and precise internal time base $1-\mathrm{MHz}$ clock. This option includes a divide-by-five IC counter to provide the proper output.

Option 2-Automatic Gate Control and Readout Scaling Circuit. This circuit automatically selects the 0.1 -, 1 -, or 10 -second measurement interval to display the largest number of digits without overflow, and provides the appropriate scaling of decimal-point and units lights to produce the correct display. If overflow indication occurs, the input signal is $\geqslant 100 \mathrm{MHz}$ and the overflow digit is a " 1 "

## Electrical Characteristics

## MEASUREMENT RANGES AND ACCURACY

Frequency: 10 Hz to 100 MHz ; 0.1 -s to 10 -s counting gate tirie; displays kHz or MHz units with positioned decimal point. Accuracy, $\pm 1$ count $\pm$ time-base accuracy.

Count: Register capacity, $10^{7}$; totalizes events accumulated between start/stop commands from front-panel button.

## INPUT

Frequency, 10 Hz to 100 MHz ; sensitivity, 300 mV peak to peak; triggering level, adjustable $\pm 2 \mathrm{~V}$; attenuator, X 1 , $\mathrm{X} 5, \mathrm{X} 10$, or X 50 ; maximum input voltage, 500 V (DC + peak $A C$, or peak to peak $A C$ ) at 1 kHz or less; impedance, (EXT input), approx $1 \mathrm{M} \Omega$ paralleled by about 20 pF (INT input) approx $50 \Omega$ paralleled by about 20 pF ; coupling, AC.

## INTERNAL TIME BASE

|  | Standard | Option 1 |
| :--- | :--- | :--- |
| Crystal Frequency | 1 MHz | 5 MHz |
| Stability $\quad\left(0^{\circ} \mathrm{C}\right.$ to <br> $\left.+50^{\circ} \mathrm{C}\right), ~ a f t e r ~ 1 / 2$ <br> hour warm-up | Within 1 part in <br> $10^{5}$ | Within 5 parts <br> in $10^{7}$. |
| Long-term Drift | 1 part or less in <br> $10^{5}$ per month | 1 part or less in <br> $10^{7}$ per month |
| Accuracy | Adjustable to <br> within 1 part in <br> $10^{7}$ | Adjustable to <br> within 5 parts <br> in $10^{9}$. |

INTERNAL MEASUREMENT INTERVAL.
Selectable in decade steps.

| Measurement <br> Interval | Display | Units | Resolution |
| :---: | :---: | :---: | :---: |
| 10 ms | 000.0000 | MHz | 100 Hz |
| 100 ms | 00.00000 | MHz | 10 Hz |
| 1 s | 0000.000 | kHz | 1 Hz |
| 10 s | 000.0000 | kHz | 0.1 Hz |
| Mat | 0000000 | (ads to |  |

Accuracy, with in $\pm \frac{1}{\text { total count }} \pm$ time-base accuracy.

## DATA PRESENTATION

$V$ isual numerical readout, seven 7 -segment LED with automatically positioned decimal point; units, LED indicates kHz or MHz ; overflow. LED indicates that readout is exceeded; gate, LED indicates open gate.

## DATA INPUTS and OUTPUTS

Available via plug-in connector to 50 -pin connector at rear of Power Module. Input lines are available for signal input, and internal and external scan clock control. Output lines are available for BCD output (serial-by-digit), and to indicate status of timing, data good, reset, scale, decimal point and overflow.


Fig. 2-1. DC 501 Block Diagram.

## THEORY OF OPERATION

## Introduction

This section of the manual contains an electrical description of the circuits in the DC 501100 MHz Counter. A block diagram is shown in Fig. 2-1, and complete schematics are given on pullout pages in the Servicing Information section.

## BLOCK DIAGRAM DESCRIPTION

Signals to be counted are applied via the EXT INPUT connector or via pin 16A at the rear interface, attenuators, and a coupling capacitor to the signal-shaping circuit. This circuit conditions the input signal and produces an output suitable to drive the first decade counter.

The time-base circuit generates the signals which determine when the counter is allowed to count (GATE), when the readout display is updated (LATCH), and when the counter is cleared or reset (CLEAR, CLEAR , or $\overline{R E S E T}$ ). The generation and the time relationship between these signals are determined by the front-panel MEASUREMENT INTERVAL, DISPLAY TIME, Manual Gate START/STOP, and RESET controls.

The decade counter units receive the shaped input signal when the gate is "open". Each DCU corresponds to one of the display LED's. Immediately upon closure of the GATE, the LATCH locks the sample taken into the storage register. If the sample taken exceeds the seven available display digits, the excessive count spills over and is indicated by the OVERFLOW LED on the front panel. Before a new sample of the input signal is taken, the time-base circuit sends in a CLEAR pulse to reset all the DCU's to zero.

The multiplexing circuit scans the latches of the storage register at a 2 -kilohertz rate, enabling each latch and its corresponding display LED sequentially on a time-shared basis. The BCD output of the storage register is decoded and the correct combination of LED segments is lighted to display any digit between 0 and 9 . Also, the decoder and display-multiplexing circuit provides leading-zero suppression if the display is within the display-register capacity. Decimal point location is a function of the MEASUREMENT INTERVAL switch.

## CIRCUIT DESCRIPTION

## Input Circuit

Signals to be counted are applied via front-panel INPUT connector J100, or via the internal input at pin 16A at the rear interface, to the attenuators. The attenuators are frequency-compensated voltage dividers consisting of resistors R102-R107 and capacitors C102-C107. Switches S100A and S100B allow front-panel selection of X1, X5, X 10 , or X 50 attenuation of the input signal. C1 10 provides $A C$ coupling.

FET source follower Q115 and emitter follower Q122 present a high impedance to the input signal. The diodes in the base circuit of E. F. Q128 form a series-limiter and clamping network, which reduces the input signal to limits suitable for driving the shaping circuits. The clamping diodes limit the voltage at the emitter of Q128 to a dynam ic range of about 1.2 volts.

U150B, an OR gate integrated circuit with push-pull outputs, is connected as a Schmitt trigger. It shapes the input signal into a square wave. Its "hysteresis window" is a width of about 200 mV . The output changes states when the signal voltage passes through the upper threshold, then reverts to its original state when the signal voltage passes through the lower threshold. For this reason, an input signal smaller in amplitude than the width of the hysteresis window cannot activate the counting circuits.

The quiescent level at the input of $\cup 150 B$ can be adjusted to overcome some of the triggering difficulties arising from various input-signal shapes and frequencies. Integrated-circuit operational amplifier U135 and its associated discrete components are connected as a voltage follower. TRIGGER LEVEL potentiometer R135 selects a voltage between ground and about -2 volts and applies it to pin 3 of $\cup 135$. This level is then established at pin 2, and hence, the input of $U 150 B$, through the action of the operational amplifier.

The output of $U 150 B$ is applied to U150A, whose push-pull outputs drive Q160 and Q162, which are connected as a differential pair. This circuit provides a level shift to TTL level, and further shapes the signal to be counted. A waveform with fast rising and falling edges is produced at the collector of Q160. CR165 limits the amplitude of the count signal to 5 volts, clamping the

## Theory of Operation-DC 501

negative-going portion of the signal to ground. The signal is then passed through emitter follower Q170 to U160B, where it receives a final phase inversion (to correspond with the input signal) and becomes the decade input.

## Time Base and Control Circuit

General. The time base and control circuit generates the following control signals:

1. GATE. The GATE output determines when the counter is allowed to count. When this output level is HI, the gate is "open" and the counter counts the input signal. While the gate is open, the front-panel GATE indicator is lit. The time during which the gate is open is determined by the MEASUREMENT INTERVAL switch setting.
2. LATCH. This output determines when the measurement made by the decade counter units is transferred to the storage register latches, permitting the readout display to be updated. In the normal gate mode (one of four selectable gate intervals), or in the optional AUTO gate mode, the LATCH goes HI for $1 \mu \mathrm{sec}$ immediately upon closure of the GATE. In the manual gate mode, the LATCH is held HI to allow continuous updating. Also, the LATCH is activated by the RESET signal.
3. CLEAR and CLEAR. These outputs determine when the counter is to be reset to zero. Just before the GATE opens, CLEAR and $\overline{\text { CLEAR }}$ are activated for a short duration (less than $2 \mu \mathrm{sec}$ ), resetting the DCU's to zero before a new count is taken. Also, CLEAR and CLEAR are activated by the $\overline{\mathrm{RESET}}$ signal.
4. $\overline{\mathrm{RESET}}$. This output is used to reset all of the counting and dividing circuits in the DC 501, and to enable all of the LED-readout character segments for a segment check. The active level is LO, produced by a switch closure to ground (front-panel RESET switch, or between the detent positions of the MEASUREMENT INTERVAL switch).

1 MHz Clock. A precise one-megahertz clock provides the reference for operation of the gate-generating circuits. The output of crystal oscillator Y200 is adjustable by C201 to exactly one megahertz. The four parts of U200 form a shaper-buffer stage to produce square-wave clock pulses and to isolate the oscillator from the $1-\mathrm{MHz}$ output line.

## NOTE

An optional 1 MHz clock is available, using a very stable 5 MHz crystal oscillator and a divide-by-five counter. This combination is shown on the schematic as Y201 and U201.

Time Base Decade Dividers (DDU's). The DDU's consist of seven cascaded divide-by-ten counters, U209 through U215. They produce four gate times, $0.01 \mathrm{sec}, 0.1 \mathrm{sec}, 1 \mathrm{sec}$ and 10 sec , which are made available via the MEASUREMENT INTERVAL switch to the gate generator to establish the precise time interval the GATE is open. The 1 MHz clock signal is applied to pin 14 of U209, whose output is connected to the input of the subsequent decade. Each decade is clocked with a negative-going transition. The DDU's are reset by a CLEAR pulse, which places a 0 count in U209 and a 9 count in each subsequent decade.

Gate Generator. The gate generator produces the GATE control signal and initiates the CLEAR, $\overline{C L E A R}$, and LATCH pulses. The generating portion consists of U220A, U222A, U220B, and U222B. The display time control portion consists of Q230, Q238, and Q240. The circuit will be described first in the normal gate mode (MEASUREMENT INTERVAL switch in one of the four gate time positions).

Assume that the $T_{0}$ conditions are as given in Fig. 2-2. The Q outputs of U220A, U222A, U220B, and U222B are all LO. Q230 is off and the emitter of Q238 rises as C235 charges. At $\mathrm{T}_{1}, \mathrm{Q} 238$ reaches its firing potential and discharges the capacitor. This results in a short-duration LO pulse on the direct-set input (pin 2) of U220A, forcing its $Q$ output HI and its $\overline{\mathrm{Q}}$ output LO. With two HI inputs on NAND gate U230A, its output goes LO and the output of NOR gate U230C goes HI, producing the CLEAR and $\overline{\text { CLEAR }}$ control signals. The next HI -to-LO transition from the $1-\mathrm{MHz}$ clock $\left(\mathrm{T}_{2}\right)$ toggles U222A, causing its Q output to go HI and its $\overline{\mathrm{Q}}$ to go LO. With a LO applied to one of its inputs, U230A reverts to its original condition, terminating the CLEAR and CLEAR pulses. The DDU's then start counting from their 0999999 reset condition.

At the end of a 10 -microsecond delay (time for the DDU's to count the first digit, plus a propagation delay), a negative transition from the DDU's via the MEASUREMENT INTERVAL switch toggles U220B. This corresponds to $T_{3}$ in Fig. 2-2. U220B's Q output goes HI and its $\overline{\mathrm{Q}}$ output goes LO. The next negative transition from the $1-\mathrm{MHz}$ clock $\left(\mathrm{T}_{4}\right)$ toggles U 222 B , causing its Q output to go HI (GATE open) and its $\overline{\mathrm{Q}}$ output to go LO (supplying current to the front-panel GATE indicator LED, CR225). The GATE signal is also applied to the base of Q230, saturating the transistor and preventing C235 from charging.

The GATE remains open ( HI ) for the time duration selected by the MEASUREMENT INTERVAL switch. At the end of this time, which corresponds to $T_{5}$ in Fig. 2-2, another negative transition from the DDU's toggles U220B. U220B's Q output goes LO and its $\overline{\mathrm{Q}}$ output goes HI. The next negative transition from the $1-\mathrm{MHz}$ clock $\left(T_{6}\right)$ toggles


Fig. 2-2. Time Base generator normal gating mode ladder diagram.

U222B, causing its Q output to go LO, closing the GATE. Simultaneously, the $\overline{\mathrm{Q}}$ output goes HI , removing current from the GATE indicator LED.

When the GATE output goes LO, the negative transition toggles U220A, switching Q LO and $\overline{\mathrm{Q}} \mathrm{HI}$. Now NAND gate U230D has two HI inputs, placing a LO at the input of OR gate U230B and activating the LATCH control signal (HI state). One microsecond later ( $T_{7}$ ), a negative edge from the $1-\mathrm{MHz}$ clock toggles U222A, switching its outputs and placing a LO on the input of NAND gate U230D. U230D reverts to its original condition, terminating the LATCH signal.

The display time begins when the GATE signal ends ( $\mathrm{T}_{6}$ ). When O 230 turns off, C235 begins to charge through R232-R235 toward the Vcc supply. R235, DISPLAY TIME, provides an adjustable time constant to vary the display time from about 0.1 second to about 10 seconds. When the DISPLAY TIME control is fully clockwise (HOLD detent position), S235 opens, and C235 stops charging. When S 235 is closed and C235 charges sufficiently to bring O 238 to its firing potential $\left(\mathrm{T}_{1}\right)$, the display time ends and the next GATE-opening sequence begins.

Manual Gate. The manual mode of operation is selected by placing the MEASUREMENT INTERVAL switch in the MANUAL position. The switch closure to ground (cam 5 of the switch) places a LO on the set inputs of U220B and U222A, and a LO on the clear input of U220A. This forces the Q outputs of U222A and U220B HI, and the Q output of U220A LO. With both inputs of U230D held HI, the LATCH output is held HI , allowing the counter to update the display continuously. The GATE is opened when the front-panel START button is pushed in, opening S2 10 and applying a HI to the clear input of U222B. As before, the GATE-open condition is HI at the Q output of U222B. The GATE is then closed when S210 is set to STOP (button out). To reset the counters in the manual mode, the RESET button must be pushed to activate the CLEAR , $\overline{\text { CLEAR }}$, and $\overline{\text { RESET }}$ control signals.

Automatic Gate (For Instruments Having Option 2). The automatic gate mode is selected by placing the MEASUREMENT INTERVAL switch in the AUTO position. The output of the automatic time base circuit is connected to the gate generator via contact 1 of the switch. Contact 2 opens to enable the readout-scaling circuit. The automatic gating cycle begins with the CLEAR pulse, which occurs when Q238 reaches its firing potential, as discussed for the

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normal gate mode (gate generator). The CLEAR pulse resets the time-base DDU's and the counter circuit DCU's, resulting in a LO applied to the toggle inputs of U180A, U180B, U181A, and U181B. This establishes the following initial conditions: LO at both inputs of U183A, LO at both inputs of U183D, HI at both inputs of U185C, a LO and a HI at the inputs of U 185 B , and HI at both inputs of U185A. The resulting LO at the output of U185A is applied to the toggle input of U220B in the gate generator. The next HI -to-LO transition from the $1-\mathrm{MHz}$ clock will toggle U222B and open the GATE. Just before the GATE opens, however, U183B has two HI inputs, producing a LO to clear U180A, U180B, U181A, and U181B. The U183B output then returns to the HI state less than a microsecond later when the GATE opens.

The GATE closes at the end of a 0.1 -second or a 1 -second interval if the display register is approaching its capacity, or at the end of a 10 -second interval. The toggle input to U181A is also the toggle input to the $10^{6} \mathrm{DCU}$, which corresponds to the most significant digit of the display. The gate-closure sequence is as follows:

After about 80 milliseconds, a HI is applied from the . 1 -sec DDU to U183A, which results in a HI applied via U185C to NAND gate U185B for about 20 milliseconds. If during that period U181A is toggled by the MSD (most significant digit), its Q output goes HI , causing U185A output to go HI . At the end of precisely .1 second, a HI -to-LO transition is input from the $.1-\mathrm{sec}$ DDU, which results in the U185A output going LO, toggling U220B in the gate generator. Then on the next HI-to-LO transition from the $1-\mathrm{MHz}$ clock, U222B is toggled, ending the GATE interval.

If no MSD input is received during the .1 -second interval, the process is repeated through the 1 -second interval, with U180B and U183D the active devices. The . 1 -second logic cannot interfere with this process because of the LO input at pin 1 of U183A, which was established when U180A was toggled at the end of .1 second. If no MSD input is received during the 1 -second interval, then the negative transition received by $U 183 C$ at the end of precisely 10 seconds causes the U185A output to go LO, initiating GATE closure.

When the GATE closes, the LATCH pulse toggles storage registers $\cup 190 A$ and $\cup 190 B$, transferring the 1 -second and 10 -second timing logic to the inputs of NAND-gate decoders U191A, U191B, and U191C. These devices provide the proper readout scaling. If the GATE time was 0.1 second, CR1 192 and CR 193 are turned on; 1 second, CR 191 and CR 195; 10 seconds, CR 190 and CR 194.

## Counter Circuit

Decade Counter Units (DCU's). The $10^{\circ}$ through $10^{6}$ DCU's are seven cascaded divide-by-ten counters. The first decade counter is made up of four individual J-K flip-flops to accept the high-speed decade input (up to 100 MHz ), and each subsequent DCU is a single IC. U165A, U165B, U167, and U169 comprise the first ( $10^{\circ}$ ) decade counter, and U235 through U240 make up the remaining six DCU's.

When the $J$ and $K$ inputs of U165B are HI (GATE open), the counter is enabled. The input signal is applied to the toggle input of U165B. On every tenth clock input counted by the first decade counter, the output of $\cup 169$ goes LO, providing a carry signal which becomes the clock input for the second decade counter. Each subsequent decade divides by ten in a similar manner. Four BCD output lines are connected from each DCU to its associated storage-register latch. When the CLEAR (HI) and CLEAR (LO) signals are activated, all of the decade counters are reset to the zero-count state.

Storage Register. The seven IC latches (U250 through U256) comprise a storage register which stores the corresponding decade counter BCD output. The BCD output is applied to the data inputs at pins $1,5,7$, and $3\left(2^{0}, 2^{1}, 2^{2}\right.$, and $2^{3}$ bits respectively). The LATCH pulse is applied to the data-strobe input at pin 2 of each latch immediately upon closure of the GATE or when the MEASUREMENT INTERVAL switch is placed in the MANUAL position, as described in the time base and control circuit. While the LATCH input is HI , the logic levels at the data inputs are transferred to the associated BCD bit output to be scanned by the multiplexing circuit.

Overflow Register. When the decade counters have counted to $9,999,999$, the counters are full. At the next count, the $2^{3}$ output of U 240 goes LO, providing a toggle input to U241B. When this occurs, a LO is transferred from pin 10 to pin 8 of U241B, then when the LATCH pulse ends (goes LO), U241A is toggled and the LO is transferred to pin 13. When pin 13 of U241A goes LO, CR241 and CR242 conduct. CR242 is an LED, and in its conduction state gives a front-paneI OVERFLOW indication.

In the Manual counting mode, OVERFLOW indication is achieved via Q242 and CR244. The emitter of Q242 is grounded by a switch closure, then when pin 9 of U241B goes HI on the first overflow count, Q242, CR244, and CR242 turn on.

U241 is reset by the $\overline{\text { CLEAR }}$ pulse. To prevent leadingzero suppression during the overflow condition, the displaycontrolling circuits are notified via U245A that the count is in excess of that displayed by the LED readout.

## Decode and Display Multiplex

Scan Clock. The scan rate of the multiplexing circuit is determined by the scan clock. The scan clock is composed of U260B and U260D, which operate as a free-running multivibrator at an approximate 2 -kilohertz rate. The scan-clock output is passed through NOR gate U260A, which can also accept an externally applied scan clock signal. Other input/output lines provide internal scan-clock disable and internal scan clock output. The scan clock drives an eight-state counter and a storage register for zero suppression.
$\div 8$ Counter and Time-Slot Decoder. The divide-by eight counter is made up of U262B, U263A, and U262A, which are three halves of SN7474 type D flip-flops. The output of this counter drives U265, and SN74145 BCD-to-decimal decoder. U265 provides eight output lines (designated TS $_{\varnothing}$ through $\mathrm{TS}_{7}$ in the schematics and in Fig. 2-3) to simultaneously enable the output of each counter latch and its corresponding display LED sequentially. For example, when the $\mathrm{TS}_{1}$ line goes LO, Q280 is turned on to supply anode voltage to CR280 at the same time inverter U267C applies a HI to pin 6 of latch U256, enabling its output. Operation in a time sequence allows the latches to share a common set of output lines.

Seven-Segment Decoder and Display LED's. U270 is a BCD-to-seven-segment decoder. It accepts the BCD output of the latches, then supplies current to the appropriate cathodes of the enabled LED to display the correct number. The display LED's are CR280 through CR286. When looking at the front panel of the DC 501, CR280 controls the numerical digit displayed at the far left $\left(10^{6}\right)$, CR281 controls the second ( $10^{5}$ ), etc. Each LED has seven segments, arranged so that a combination of lighted segments forms a number. When all of the segments are lighted, an " 8 " is formed.

Leading Zero Suppression. Decoder driver U270 also has a zero-blanking feature which allows suppression of the zeroes leading the most significant digit (MSD) in the display. At $\mathrm{TS}_{\phi}$, a LO is applied to the direct-clear input of U263B, the zero-suppression storage register. This sets U263B to the zero-suppress state ( HI at pin 8), allowing the Ripple-Blanking Input (RBI, pin 5) of U270 to be LO. When the output of U265 advances to the next time slot ( $\mathrm{TS}_{1}$ ), the RBI of U 270 remains LO for a few nanoseconds due to propagation delays, which allows the first digit to arrive from the latches while RBI is LO. If this first digit being decoded is a zero, the output to the display LED will be inhibited and the Ripple Blanking Output (pin 4) will be LO. If the digit is not a zero, the outputs are enabled and


Fig. 2-3. Multplexing circuit ladder diagram showing timing with an all-zero display.

RBO goes HI. The RBO is applied to the D input (pin 12) of U263B and is transferred to the output when the next scan-clock HI -to-LO transition occurs. Thus if the first digit is a zero, pin 5 of U 270 is held LO, inhibiting the output until the first non-zero digit comes through the decoder. When the first non-zero digit arrives, the outputs of U270 are enabled and the digit is displayed. Also, the RBO output at pin 4 is set HI , removing the RBI from pin 5 and allowing all succeeding digits to be displayed through the $\mathrm{TS}_{7}$ sequence.

When the scan gets past the decimal point in the display, or if the display overflows, any zeroes arriving at the decoder should be displayed. This is achieved as follows: $\mathrm{TS}_{5}$ is inverted by U267E and applied through OR gate U245B as a LO at the direct-set input of U263B. This holds pin 5 of U 270 HI , preventing zero-blanking during the $\mathrm{TS}_{5}$, $\mathrm{TS}_{6}$, and $\mathrm{TS}_{7}$ time slots. The location of the decimal point in the display is determined by the MEASUREMENT INTERVAL switch. The proper information is applied via the closed contacts of the switch to either NAND gate U 246 A or U246B. Then either $\mathrm{TS}_{3}$ or $\mathrm{TS}_{4}$ is enabled to the input of OR gate U245B via these NAND gates, setting U263B to the non-blank state at the appropriate time. In the case where the counter overflows, the HI output from U245A is applied to U245B, setting U263B to the non-blank state.

When the front-panel RESET button is pushed, RESET goes LO, overriding the output of U263B, applying the non-blank and lamp-test functions to the decoder. This causes all seven segments in the display LED to be turned on.

Input and Output Data. The following inputs and outputs are available via the plug-in connector to external equipment. See Fig. 1-1.

INT SCAN DISABLE: A LO applied to this line disables the internal scan clock.

EXT SCAN: Provides input for an external scan clock.

INT SCAN CLOCK OUT: Provides output for the internal scan clock.
$\mathrm{TS}_{\varnothing}$ : A LO is present on this output line in the $\mathrm{TS}_{\varnothing}$ state

DATA GOOD: A HI is present on this output line when a new reading is being transferred into the storage-register latches.

OVERFLOW: This output is HI when the count overflows.

RESET: This is a dual-function input/output line. It provides a LO output during reset, or can be used as an external reset input.

Data Lines: 1, 2, 4, 8 provide BCD output, serial by digit, from the currently enabled storage-register latch. Other data lines include a LO when the MHz light is on, and a LO when the second decimal point is lit.

## Regulated Power Supplies

The DC 501 operating power is obtained from the power module mainframe and then electronically regulated to provide stable supplies of +15 volts, +5 volts, -5.2 volts, and -10 volts. The +15 -volt supply, whose active device is $\cup 300$, provides the reference for the remaining supplies. Its output is set to exactly +15 V by adjustment of R305.

Integrated circuit U320 regulates the +5 -volt supply, and transistors Q 330 and Q 340 regulate the -5.2 -volt and -10 -volt supplies respectively. The series-pass transistors for these supplies are located in the mainframe, where they can provide the proper heat dissipation.

## SERVICING INFORMATION

## Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

$$
\begin{aligned}
\text { Capacitors }= & \text { Values one or greater are in picofarads. }(\mathrm{pF}) . \\
& \text { Values less than one are in microfarads }(\mu \mathrm{F}) . \\
\text { Resistors }= & \text { Ohms }(\Omega)
\end{aligned}
$$

Symbols used on the diagrams are based on ANSI-Y32.2-1970.
Logic symbology is based on MIL-STD-806B in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The following special symbols are used on the diagrams:


External Screwdriver adjustment.

External control or connector.

Clockwise control rotation in direction of arrow.


## POO circult board

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

| A | Assembly, separable or repairable (circuit board, etc.) | LR | Inductor/resistor combination |
| :--- | :--- | :--- | :--- |
| AT | Attenuator, fixed or variable | M | Meter |
| B | Motor | Q | Transistor or silicon-controlled rectifier |
| BT | Battery | P | Connector, movable portion |
| C | Capacitor, fixed or variable | R | Resistor, fixed or variable |
| CR | Diode, signal or rectifier | RT | Thermistor |
| DL | Delay line | S | Switch |
| DS | Indicating device (lamp) | T | Transformer |
| F | Fuse | TP | Test point |
| FL | Filter | U | Assembly, inseparable or non-repairable (integrated |
| H | Heat dissipating device (heat sink, heat radiator, etc.) |  | circuit, etc.) |
| HR | Heater | V | Electron tube |
| J | Connector, stationary portion | VR | Voltage regulator (zener diode, etc.) |
| K | Relay | Y | Crystal |

L Inductor, fixed or variable

## Services Available

Tektronix, Inc. provides complete instrument repair and adjustment at local Field Service Centers and at the Factory Service Center. Contact your local TEKTRONIX Field Office or representative for further information.

## Test Equipment

For measurement of the power supply voltages, a 20,000 ohms/volt VOM will give satisfactory measurements. For example, Triplett 630 NA multimeter.

For $1-\mathrm{MHz}$ frequency measurement, a secondary frequency standard or other frequency source having a stability of at least 5 parts on $10^{7}$ ( 5 parts in $10^{8}$ if measuring optional 5 MHz crystal output) is recommended for accuracy. Also recommended is a test oscilloscope with a bandwidth of at least 1 MHz and a stable triggering circuit for frequency-comparison measurement.

## Procedure

## NOTE

The performance of this instrument can be check at any temperature within the $0^{\circ} \mathrm{C}$ to $+50^{\circ} \mathrm{C}$ range. Make any adjustment at a temperature between $+20^{\circ} \mathrm{C}$ and $+30^{\circ} \mathrm{C}\left(+68^{\circ} \mathrm{F}\right.$ and $\left.+86^{\circ} \mathrm{F}\right)$.

The DC 501 can be operated either fully installed in a TM 500 Series Power Module or connected to a plug-in extender (TEKTRONIX Part No. 067-0645-01).

Power Supply Checks and Adjustment. Connect the voltmeter between the +15 -volt test point and ground. Adjust R305 for a reading of +15 volts. Then check the +5 -volt, -5.2 -volt, and -10 -volt supplies to be within $5 \%$.


## TMENT OF INTERNAL CONTROLS

## NOTE

If the instrument is operated on the plug-in extender, the +5 -volt supply may not regulate.

## an be check at

 $+50^{\circ} \mathrm{C}$ range. ature between ).fully installed in a ected to a plug-in 45-01).
ent. Connect the ooint and ground. s. Then check the s to be within $5 \%$.


Time-Base Frequency Check and Adjustment. Connect the DC 501 1-MHz time base reference and the secondary standard to the oscilloscope as shown. Adjust the oscilloscope to display several complete cycles.

To determine oscillator error, observe the rate of horizontal drift of the displayed waveform. Waveform moving to the right indicates that the time-base frequency is $<1 \mathrm{MHz}$; to the left, $>1 \mathrm{MHz}$. The period in seconds for the waveform to move the width of one cycle is equal to the frequency difference in parts in $10^{6}$. For example, if the waveform drifts to the right at a rate of one cycle's width every 10 seconds, the time-base frequency is 0.1 part in $10^{6}$ low. Maximum allowable frequency difference is 1 part in $10^{5}$ ( 5 parts in $10^{7}$ for the optional 5 MHz crystal). Adjust C201 for no drift.

## FRONT-PANEL CONTROLS AND CONNECTORS





note, Components shown with dashed lines are located on back side of board.

## ELECTRICAL PARTS LIST

Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts ar service.
abbreviations and reference designators

| A | Assembly, separable or repairable | $\begin{aligned} & \mathrm{FL} \\ & \mathrm{H} \end{aligned}$ | Filter Heat dissipating | PTM | paper or plastic, tubular molded |
| :---: | :---: | :---: | :---: | :---: | :---: |
| AT | Attenuator, fixed or variable |  | (heat sink, etc.) | R | Resistor, fixed or variable |
| B | Motor | HR | Heater | RT | Thermistor |
| BT | Battery | J | Connector, stationary portion | S | Switch |
| C | Capacitor, fixed or variable | K | Relay | T | Transformer |
| Cer | Ceramic | L | Inductor, fixed or variable | $T P$ | Test point |
| CR | Diode, signal or rectifier | LR | Inductor/resistor combination | U | Assembly, inseparable or |
| CRT | cathode-ray tube | $M$ | Meter |  | non-repairable |
| DL | Delay line | Q | Transistor or silicon- | V | Electron tube |
| DS | Indicating device (lamp) |  | controlled rectifier | Var | Variable |
| Elect. | Electrolytic | P | Connector, movable portion | VR | Voltage regulator (zener diode, |
| EMC | electrolytic, metal cased | PMC | Paper, metal cased |  | etc.) |
| EMT | electrolytic, metal tubular | PT | paper, tubular | WW | wire-wound |
| F | Fuse |  |  | $Y$ | Crystal |

COUNTER TIME BASE AND CONTROL

| Ckt. No. | Grid Loc | Tektronix Part No. | Serial/Model No. Eff Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| ASSEMBLY |  |  |  |  |
| A1 ${ }_{1}^{1}$ |  | 670-2102-00 | B010100. B039999 | MAIN Circuit Board Assembly (part of) |
| $\mathrm{Al}^{1}$ |  | 670-2102-01 | B040000 | MAIN Circuit Board Assembly (part of) |
| $\mathrm{Al}^{2}$ |  | 670-3406-00 |  | MAIN Circuit Board Assembly (part of) |
| $\mathrm{Al}^{3}$ |  | 670-3407-00 |  | MAIN Circuit Board Assembly (part of) |
| ${ }_{\text {A2 }} 3$ |  | 670-2103-00 |  | DISPLAY Circuit Board Assembly (part of) |
| $A 3^{3}$ |  | 670-2249-00 |  | AUTO-GATE Circuit Board Assembly |
| CAPACITORS |  |  |  |  |
| C102 | M5 | 281-0510-00 |  | $22 \mathrm{pF}, \mathrm{Cer}, 500 \mathrm{v}, 20 \%$ |
| C103 | M4 | 281-0605-00 |  | 200 pF , Cer, 500 V , |
| C106 | L4 | 281-0509-00 |  | 15 pF, Cer, $500 \mathrm{~V}, 10 \%$ |
| C107 | L5 | 281-0540-00 |  | 51 pF , Cer, $500 \mathrm{~V}, 5 \%$ |
| C110 | L5 | 283-0068-00 |  | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| C112 | L5 | 281-0571-00 |  | $82 \mathrm{pF}, \mathrm{Cer}, 500 \mathrm{~V}, 20 \%$ |
| C113 | L6 | 283-0003-00 |  | $0.01 \mu \mathrm{~F}$, Cer, $150 \mathrm{~V},+80 \%-20 \%$ |
| C122 | K5 | 283-0000-00 |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| C127 | K5 | 283-0000-00 |  | $0.001 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| C139 | M5 | 283-0003-00 |  | $0.01 \mu \mathrm{~F}, \mathrm{Cer}, 150 \mathrm{~V},+80 \%-20 \%$ |
| C140 | M5 | 283-0177-00 |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C141 | M5 | 283-0000-00 |  | $0.001 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| C152 | J6 | 281-0589-00 |  | 170 pF, Cer, $500 \mathrm{~V}, 5 \%$ |
| C200 | G5 | 281-0504-00 |  | $10 \mathrm{pF}, \mathrm{Cer}, 500 \mathrm{~V}, 10 \%$ |
| ${ }_{2}$ Standard only. |  |  |  |  |
| ${ }_{3}^{2}$ Option 1 only. |  |  |  |  |
| ${ }^{3} \mathrm{Optio}$ | 2 on |  |  |  |

Grid Tektronix Serial/Model No.

| Ckt. No. | Grid Loc | Tektronix Part No. | Serial/Model No. Eff Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| CAPACITORS (cont) |  |  |  |  |
| C201 | G5 | 281-0166-00 |  | 1.9-15.7 pF, Var, Air |
| C202 | G5 | 281-0739-00 |  | $18 \mathrm{pF}, \mathrm{Cer}, 500 \mathrm{~V}$ |
| C235 | M4 | 290-0536-00 |  | $10 \mu \mathrm{~F}$, Elect., $25 \mathrm{~V}, 20 \%$ |
| DIODES |  |  |  |  |
| CR115 | K5 | 152-0141-02 |  | Silicon, replaceable by 1 N 4152 |
| CR122 | K5 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR124 | J5 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| CR125 | J5 | 152-0141-02 |  | Silicon, replaceable by $1 \times 4152$ |
| CR127 | J5 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| CR128 | J5 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR165 | H6 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR190 ${ }_{1}^{1}$ | Q2 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| CR191 | Q2 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| CR152 | R2 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR1931 | R2 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR194 ${ }^{1}$ | R2 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| CR195 ${ }^{\text { }}$ | Q2 | 152-0141-02 |  | Silicon, replaceable by 1 N4152 |
| CR240 | L4 | 152-0141-02 |  | Silicon, replaceable by 1N4152 |
| INDICATOR |  |  |  |  |
| DS 225 | 06 | 150-1001-01 |  | Light, emitting diode |
| CONNECTOR |  |  |  |  |
| J100 Ch | assis | 131-0955-00 |  | Receptacle, electrical BNC |
| TRANSISTORS |  |  |  |  |
| Q115 | K5 | 151-1022-00 |  | Silicon, FET, selected from 2N4392 |
| Q122 | K4 | 151-0325-00 |  | Silicon, PNP, replaceable by 2N4258 |
| Q128 | J6 | 151-0259-00 |  | Silicon, NPN, selected from 2N3563 |
| Q160 | 16 | 151-0190-00 |  | Silicon, NPN, replaceable by 2 N 3904 or TE3904 |
| Q162 | 16 | 151-0190-00 |  | Silicon, NPN, replaceable by 2 N 3904 or TE3904 |
| Q170 | H6 | 151-0325-00 |  | Silicon, PNP, replaceable by 2 N 4258 |
| Q230 | M4 | 151-0341-00 |  | Silicon, NPN, replaceable by 2 N 3565 |
| Q238 | L4 | 151-0504-00 |  | Silicon, Unijunction, replaceable by 2N4851 |
| Q240 | L4 | 151-0341-00 |  | Silicon, NPN, replaceable by 2 N 3565 |
| RESISTORS |  |  |  |  |
| R101 |  | 315-0510-00 |  | 51 ת, 1/4 W, 5\% |
| R102 | M5 | 323-0611-00 |  | $900 \mathrm{k} \Omega, 1 / 2 \mathrm{~W}, 1 \%$ |
| R103 | M4 | 321-0617-00 |  | $111 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R106 | L4 | 323-0620-00 |  | $800 \mathrm{k} \Omega, 1 / 2 \mathrm{~W}, 1 \%$ |
| R107 | L5 | 321-0423-00 |  | $249 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R112 | L5 | 321-0356-00 |  | $49.9 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R113 | L6 | 315-0103-00 |  | $10 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R115 | L6 | 315-0470-00 |  | $47 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R117 | J6 | 315-0101-00 |  | $100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R118 | K5 | 315-0182-00 |  | $1.8 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |

[^0]COUNTER TIME BASE AND CONTROL (1) (cont)

| Ckt. No. | Grid Loc | Tektronix Part No. | Serial/Model No. Eff Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| RESISTORS | (cont) |  |  |  |
| R120 | K5 | 315-0101-00 |  | $100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R121 | K5 | 315-0561-00 |  | $560 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R122 | J5 | 315-0332-00 |  | $3.3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R123 | K5 | 315-0223-00 |  | $22 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R126 | J5 | 315-0470-00 |  | $47 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R127 | J5 | 315-0202-00 |  | $2 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R130 | J5 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R132 | K6 | 315-0103-00 |  | $10 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R135 |  | 311-1220-00 |  | $20 \mathrm{k} \Omega$, Var |
| R137 | M6 | 315-0513-00 | B010100 B039999 | $51 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R137 | M6 | 315-0513-00 | B040000 | $51 \mathrm{k} \Omega$, (nominal value), selected |
| R139 | M6 | 315-0103-00 |  | $10 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R140 | L5 | 323-0612-00 |  | $950 \mathrm{k} \Omega, 1 / 2 \mathrm{~W}, 1 \%$ |
| R152 | J6 | 315-0101-00 |  | 100 ת, $1 / 4 \mathrm{~W}, 5 \%$ |
| R153 | J5 | 315-0101-00 |  | $100 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R155 | I5 | 315-0331-00 |  | 330 ת, $1 / 4 \mathrm{~W}, 5 \%$ |
| R158 | I5 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R159 | I5 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R162 | 16 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R163 | I6 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R165 | I5 | 315-0561-00 |  | $560 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R167 | I6 | 315-0621-00 |  | $620 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R169 | I5 | 315-0561-00 |  | 560 ת, 1/4 W, 5\% |
| R172 | H5 | 315-0152-00 |  | $1.5 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R173 | H6 | 315-0470-00 |  | $47 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R175 | H5 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R177 | K6 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R191 ${ }^{1}$ | R2 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W} ; 5 \%$ |
| R200 | G5 | 315-0181-00 |  | $180 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R203 | H6 | 315-0242-00 |  | $2.4 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R205 | G6 | 315-0271-00 |  | 270 ת, 1/4 W, 5\% |
| R209 | G6 | 315-0301-00 |  | 300 ת, 1/4 W, 5\% |
| R220 | L3 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R222 | L2 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R224 | M2 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R226 | L3 | 315-0301-00 |  | 300 ת, $1 / 4 \mathrm{~W}, 5 \%$ |
| R230 | L3 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R232 ${ }_{2}$ | L4 | 315-0202-00 |  | $2 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| $\mathrm{R} 235{ }^{2}$ | C3 | 311-1342-00 |  | $500 \mathrm{k} \Omega$, Var |
| R238 | L4 | 315-0100-00 |  | $10 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R240 | L4 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |

[^1]Grid Tektronix Serial/Model No.
Ckt No Eff Disc

| SWITCHES |  |  |
| :---: | :---: | :---: |
| S100A | M5 | $260-1353-01$ |
| S100B | M4 | $260-0583-00$ |
| S101 |  | 260 |
| S200 $^{1}$ | K3 | $105-0354-00$ |
| S201 $^{1}$ | I3 | $105-0356-00$ |
| S210 | M3 | $260-1425-00$ |
| S220 | M3 |  |
| S235 | C4 |  |


| INTEGRATED | CIRCUITS |  |
| :---: | :---: | :---: |
| U135 | M6 | $156-0067-00$ |
| U150 | I5 | $156-0182-00$ |
| U160 $^{1}$ | H5 | $156-0180-00$ |
| U180 $^{1}$ | P3 | $156-0039-00$ |
| U181 $^{1}$ | P3 | $156-0039-00$ |
| U183 $^{1}$ | 03 | $156-0030-00$ |
| U185 $^{1}$ | 33 | $156-0030-00$ |
| U190 $^{1}$ | Q3 | $156-0041-00$ |
| U191 $^{1}$ | R3 | $156-0047-00$ |
| U200 $^{1}$ | F5 | $156-0030-00$ |
| U201 $^{3}$ | E6 | $156-0079-00$ |

CRYSTALS

| Y 200 | F5 | $158-0079-00$ |
| :--- | :--- | :--- |
| $\because 201{ }^{3}$ | F 6 | $119-0262-00$ |

${ }_{2}$ Option 2 only.
${ }_{3}$ R235 \& S235 furnished as a unit.
Option 1 only.

Operational amplifier, replaceable by UA741C
Type 2-3-2 input gate, replaceable by MC10105
Quad 2-input nand gate, replaceable by SN74500N
Dual 15 MHz master-slave flip-flop, replaceable by SN7473N
Dual 15 MHz J-K master-slave flip-flop, replaceable by SN7473N
Quad 2-input positive nand gate, replaceable by SN7400N
Quad 2-input positive nand gate, replaceable by SN7400N
Dual 15 MHz D-type pos-edg-trig flip-flop, replaceable by SN7474N
Triple 3-input positive $n=n d$ gate, replaceable by SN7410N
Quad 2..input positive nand gate, replaceable by SN7400N
Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter,
replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\alpha-5$ ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2- $\delta-5$ ripple counter,
zeplaceable by SN7490N
Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N
Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N
Dual 15 MHz J-K msster-slave flip-flop, replaceable by SN7476N
Dual 20 MHz J-K master-slave flip-flop, replaceable by SN74111N
Quad 2-input positive nand buffer, replaceable by SN7473N

Pushbutton, ATTENUATOR<br>Slide, DPDT<br>Actuator assembly, MEASUREMENT INTERVAL<br>Actuator assembly, MEASUREMENT INTERVAL<br>Push, RESET

[^2]


Counter time base and control (1) iem $\begin{aligned} & \text { den } \\ & 0272\end{aligned}$

| Ckt. No. | Grid Loc | Tektronix Part No. | Serial/Mode Eff | No. Disc | Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ASSEMBLIES |  |  |  |  |  |
| $\mathrm{Al}_{1}^{1}$ |  | 670-2102-00 | B010100 | B039999 | MAIN Circuit Board Assembly (rart of) |
| $\mathrm{Al}_{2}$ |  | 670-2102-01 | B040000 |  | MAIN Circuit Board Assembly (part of) |
| $\mathrm{Al}_{3}$ |  | 670-3406-00 |  |  | MAIN Circuit Board Assembly (part of) |
| A1 |  | 670-3407-00 |  |  | MAIN Circuit Board Assembly (part of) |
| A2 |  | 670-2103-00 |  |  | DISPLAY Circuit Board Assembly (part of) |
| A4 |  | 670-2708-00 | XB010283 |  | PROTECTION Circuit Board Assembly |
| A5 |  | 670-3300-00 | YB040000 |  | $\div 5$ Circuit Board Assembly |
| CAPACITORS |  |  |  |  |  |
| C260 | L1 | 283-0111-00 |  |  | $0.1 \mu \mathrm{~F}, \mathrm{Cer}, 50 \mathrm{~V}$ |
| C265 | L1 | 283-0111-00 |  |  | $0.1 \mu \mathrm{~F}, \mathrm{Cer}, 50 \mathrm{~V}$ |
| C267 |  | 283-0000-00 | XB010283 |  | $0.001 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V},+100 \%-0 \%$ |
| C302 | E6 | 290-0529-00 |  |  | $47 \mu \mathrm{~F}$, Elect., $20 \mathrm{~V}, 20 \%$ |
| C305 | D6 | 283-0060-00 |  |  | 100 pF , Cer, $200 \mathrm{~V}, 5 \%$ |
| C322 | B5 | 290-0531-00 |  |  | $100 \mu \mathrm{~F}$, Elect., $10 \mathrm{~V}, 20 \%$ |
| C325 | B6 | 283-0150-00 |  |  | $650 \mathrm{pF}, \mathrm{Cer}, 200 \mathrm{~V}, 5 \%$ |
| C334 | H6 | 283-0000-00 |  |  | $0.001 \mu \mathrm{~F}, \mathrm{Cer}, 500 \mathrm{~V},+100 \%-0 \%$ |
| C335 | H6 | 283-0177-00 |  |  | $1 \mu \mathrm{~F}, \mathrm{Cer}, 25 \mathrm{~V},+80 \%-20 \%$ |
| C340 | E6 | 290-0529-00 |  |  | $47 \mu \mathrm{~F}$, Elect., $20 \mathrm{~V}, 20 \%$ |
| DIODES |  |  |  |  |  |
| CR241 | 11 | 152-0141-02 |  |  | Silicon, replaceable by 1 N 4152 |
| CR244 | 12 | 152-0141-02 |  |  | Silicon, replaceable by 1 N 4152 |
| INDICATORS |  |  |  |  |  |
| DS242 | P6 | 150-1001-01 |  |  | Light emitting diode |
| DS280 | N5 | 150-1002-00 |  |  | Numerical display diode |
| DS281 | 05 | 150-1002-00 |  |  | Numerical display diode |
| DS282 | 05 | 150-1002-00 |  |  | Numerical display diode |
| DS283 | 05 | 150-1002-00 |  |  | Numerical display diode |
| DS284 | P5 | 150-1002-00 |  |  | Numerical display diode |
| DS285 | P5 | 150-1002-00 |  |  | Numerical display diode |
| DS286 | Q5 | 150-1002-00 |  |  | Numerical display diode |
| DS290 | P6 | 150-1001-01 |  |  | Light emitting diode |
| DS292 | 06 | 150-1001-01 |  |  | Light emitting diode |
| VR320 | R6 | 152-0166-00 | XB010283 |  | Zener, selected from 1N753A, $0.4 \mathrm{~W}, 6.2 \mathrm{~V}, 5 \%$ |
| FUSE |  |  |  |  |  |
| F320 | R5 | 159-0021-00 | XB010283 |  | Cartridge, 2A, 3AG, fast-blo |
| TRANSISTORS |  |  |  |  |  |
| Q242 | J1 | 151-0341-00 |  |  | Silicon, NPN, replaceable by 2 N 3565 |
| Q280 | F2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 2907 |
| Q281 | F2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 2907 |
| Q282 | G2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 3907 |
| Q283 | G2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 3907 |
| Q284 | G2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 3907 |
| Q285 | G2 | 151-0301-00 |  |  | Silicon, PNP, replaceable by 2 N 3907 |
| ${ }_{2}$ Standa <br> ${ }_{3}^{2}$ Option <br> Option | rd ond 1 2 only 2 | y. |  |  |  |


| Ckt. No. | Grid Loc | Tektronix <br> Part No. | Serial/Model No. Eff <br> Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| TRANSISTORS (cont) |  |  |  |  |
| Q286 | G2 | 151-0301-00 |  | Silicon, PNP, replaceable by 2N3907 |
| Q320 | R4 | 151-0515-01 | XB010283 | Thyristor, $50 \mathrm{~V}, 8 \mathrm{~A}$, replaceable by 2N4441 |
| Q330 | D6 | 151-0342-00 |  | Silicon, PNP, replaceable by 2N4249 |
| Q340 | B4 | 151-0342-00 |  | Silicon, PNP, replaceable by 2N4249 |
| RESISTORS |  |  |  |  |
| R242 | I2 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R244 | I2 | 315-0301-00 |  | $300 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R260 | M3 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R261 | M2 | 315-0242-00 |  | $2.4 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R264 | M2 | 315-0562-00 |  | $5.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R265 | M2 | 315-0242-00 |  | $2.4 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R267 | M2 | 315-0102-00 |  | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R271 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R272 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R273 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R274 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R275 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R276 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R277 | H2 | 315-0750-00 |  | $75 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R280A | F1 |  |  | $300 \Omega$, |
| R280B | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R280C | F1 |  |  | $300 \Omega$, |
| R280D | F1 | 307-0357-00 |  | $1 \mathrm{k} \Omega$, Thick film, 7 section divider |
| R280E | F1 |  |  | $300 \Omega$, |
| R280F | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R280\% | F1 |  |  | $300 \Omega$, |
| R 280 H | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R280J | F1 |  |  | $300 \Omega$, |
| ${\mathrm{R} 280 \mathrm{~K}_{1}}$ | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R280L ${ }^{-1}$ | F1 | 307-0357-00 |  | $300 \Omega$, Thick $\because i l m, 7$ section divider |
| R280M | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R280N | F1 |  |  | $300 \Omega$, |
| R280P | F1 |  |  | $1 \mathrm{k} \Omega$, |
| R282 | I2 | 315-0151-00 |  | $150 \Omega, 1 / 4 W, 5 \%$ |
| R283 | I2 | 315-0151-00 |  | $150 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R284 | I2 | 315-0151-00 |  | $150 \Omega, 1 / 4 W, 5 \%$ |
| R290 | M2 | 315-0301-00 |  | $300 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R292 | M2 | 315-0301-00 |  | 300 ת, 1/4 W, 5\% |
| R302 | C5 | 307-0107-00 |  | $5.6 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R303 |  | 303-0132-00 | XB040000 | $1.3 \mathrm{k} \Omega, 1 \mathrm{~W}, 5 \%$ |
| R304 | C5 | 315-0332-00 |  | $3.3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R305 | D5 | 311-1408-00 |  | $1 \mathrm{k} \Omega$, Var |
| R306 | D5 | 315-0302-00 |  | $3 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |

$1_{\text {R280A-R280P }}$ furnished as a unit.

| Ckt. No. | Grid Loc | Tektronix Part No. | Serial/Model No. Eff Disc | Description |
| :---: | :---: | :---: | :---: | :---: |
| RESISTORS (cont) |  |  |  |  |
| R308 | C5 | 315-0152-00 |  | $1.5 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R310 | B5 | 306-0560-00 | B010100 B039999 | $56 \Omega, 2 \mathrm{~W}, 10 \%$ |
| R310 | B5 | 306-0121-00 | B040000 | $120 \Omega, 2 \mathrm{~W}, 10 \%$ |
| R320 | R6 | 316-0102-00 | XB010283 | $1 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 10 \%$ |
| R322 | B5 | 308-0463-00 |  | $0.2 \Omega, 3 \mathrm{~W}, \mathrm{WW}, 1 \%$ |
| R325 | B5 | 315-0162-00 |  | $1.6 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R327 | C5 | 321-0260-00 |  | $4.99 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R328 | B5 | 321-0231-00 |  | $2.49 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R330 | C5 | 315-0161-00 |  | $160 \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R334 | D5 | 321-0256-00 |  | $4.53 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R335 | D5 | 321-0308-00 |  | $15.8 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R340 | B5 | 315-0202-00 |  | $2 \mathrm{k} \Omega, 1 / 4 \mathrm{~W}, 5 \%$ |
| R344 | D5 | 321-0286-00 |  | $9.31 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R345 | C5 | 321-0308-00 |  | $15.8 \mathrm{k} \Omega, 1 / 8 \mathrm{~W}, 1 \%$ |
| R350 | A5 | 305-0101-00 |  | $100 \Omega, 2 \mathrm{~W}, 5 \%$ |
| SWITCHESS200S201 |  |  |  |  |
| INTEGRATED CIRCUITS |  |  |  |  |
| U1 |  | 156-0118-00 | XB040000 | Dual 100 MHz J-K master-slave flip-flop, replaceable by SN74S112 |
| U2 |  | 156-0180-00 | XB040000 | Quad 2-input nand gate, replaceable by SN74500N |
| U165 | H4 | 156-0118-00 |  | Dual 100 MHz J-K master-slave flip-flop, replaceable by SN74S112 |
| U167 | G4 | 156-0100-00 | B010100 B039999X | Single 40 MHz J-K edge-triggered flip-flop, replaceabl by SN74H102 |
| U169 | F4 | 156-0100-00 | B010100 B0399999X | Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceabl by SN74H102 |
| U235 | D3 | 156-0079-00 |  | Single 10 MHz divide-by-2-\&-5 rinple counter, replaceable by SN7490N |
| U236 | C3 | 156-0079-00 |  | Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N |
| U237 | B3 | 156-0079-00 |  | Single 10 MHz divide-by-2- $\&-5$ ripple counter, replaceable by SN7490N |
| U238 | B1 | 156-0079-00 |  | Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N |
| U239 | C1 | 156-0079-00 |  | Single 10 MHz divide-by-2-\&-5 ripple counter, replaceable by SN7490N |
| U240 | D1 | 156-0079-00 |  | Single 10 MHz divide-by-2- $\delta-5$ ripple counter, replaceable by SN7490N |
| U241 | G3 | 156-0039-00 |  | Dual 15 MHz J -K master-slave flip-flop, replaceable by SN7473N |
| U245 | J2 | 156-0165-00 |  | Dual 4 -input positive nor gate, replaceable by SN7425N |

COUNTERS AND DISPLAY 〈 2$\rangle$ (CONT)
Grid Tektronix Serial/Model No.
Ckt. No. Loc Part No. Eff Disc

## Description

| INTEGRATED | CIRC | ITS (cont) |  |
| :---: | :---: | :---: | :---: |
| U246 | F3 | 156-0043-00 | Quad 2-input positive nor gate, replaceable by SN7402N |
| U250 | E3 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U251 | D 4 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U252 | C4 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U253 | B3 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U254 | B2 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U255 | C2 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U256 | D2 | 156-0198-00 | Quad latch, replaceable by MC4035P |
| U260 | M1 | 156-0030-00 | Quad 2-input nand gate, replaceable by SN7400N |
| U262 | K2 | 156-0041-00 | Dual 15 MHz D-type pos-edge-trig flip-flop, replaceable by SN7474N |
| U263 | L2 | 156-0041-00 | Dual 15 MHz D-type nos-edge-trig flip-flop, replaceable by SN7474N |
| U265 | E2 | 156-0111-00 | Single BCD-to-decimal decoder/driver, replaceable by SN7415N |
| U267 | E2 | 156-0058-00 | Hex. inverter, replaceable by SN7404N |
| U270 | H3 | 156-0128-00 | Single BCD-to-seven-segment decoder/driver, replaceable by SN7447N |
| U300 | C6 | 156-0071-00 | Voltage, regulator, replaceable by UA723C |
| U320 | B6. | 156-0071-00 | Voltage, regulator, replaceable by UA723C |




## MECHANICAL PARTS LIST

> Replacement parts should be ordered from the Tektronix Field Office or Representative in your area. Changes to Tektronix products give you the benefit of improved circuits and components. Please include the instrument type number and serial number with each order for parts or service.

ABBREVIATIONS

| BHB | binding head brass | h | height or high | OHB | oval head brass |
| :--- | :--- | :--- | :--- | :--- | :--- |
| BHS | binding head steel | hex. | hexagonal | OHS | oval head steel |
| CRT | cathode-ray tube | HHB | hex head brass | PHB | pan head brass |
| Csk | countersunk | HHS | hex head steel | PHS | pan head steel |
| DE | double end | HSB | hex socket brass | RHS | round head steel |
| FHB | flat head brass | HSS | hex socket steel | SE | single end |
| FHS | flat head steel | ID | inside diameter | THB | truss head brass |
| Fil HB | fillister head brass | lil | length or long | THS | truss head steel |
| Fil HS | fillister head steel | OD | outside diameter |  | w |

FIGURE 1 EXPLODED \& OPTION NO. 2

| Fig. \& Index No. | Tektronix Part No. | Serial/Model No. Eff Disc |  | $\begin{aligned} & \mathbf{Q} \\ & \mathbf{t} \\ & \mathbf{y} \end{aligned}$ | $12345 \quad$ Description |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1-1 | 366-1031-00 |  |  | 1 | KNOB, red--DISPLAY TIME |
|  | - - |  |  | - | knob includes: |
|  | 213-0153-00 |  |  | 1 | SETSCREW, 5-40 x 0.125 inch, HSS |
| -2 | 366-1165-00 |  |  | 1 | KNOB, gray--MEASUREMENT INTERVAL |
|  | - - |  |  | - | knob includes: |
|  | 213-0153-00 |  |  | 2 | SETSCREW, 5-40 $\times 0.125$ inch, HSS |
| -3 | 366-0494-00 |  |  | 1 | KNOB, gray--TRIGGER |
|  | - - - - - |  |  | - | knob includes: |
|  | 213-0153-00 |  |  | 1 | SETSCREW, 5-40 x 0.125 inch, HSS |
| -4 | 366-1257-30 |  |  | 1 | PUSHBUTTON--RESET |
| -5 | 366-1402-01 |  |  | 1 | PUSHBUTTON--START |
| -6 | 366-1402-00 |  |  | 1 | PUSHBUTTON--X5 |
| -7 | 366-1257-87 |  |  | 1 | PUSHBUTTON--X10 |
| -8 | 366-1422-00 | B010100 | B019999 | 1 | KNOB, latch |
|  | 366-1422-01 | B020000 |  | 1 | KNOB, latch |
|  | 214-1840-00 | XB020000 |  | 1 | PIN, knob securing |
| -9 | 131-0955-00 |  |  | 1 | CONNECTOR, receptacle, BNC, w/hardware |
|  | - - - |  |  | 1 | mounting hardware: (not included w/connector) |
| -10 | 210-0255-00 |  |  | 1 | TERMINAL, lug, solder, 0.391 inch, diameter, SE |
| -11 | - - - - - |  |  | 1 | RESISTOR, variable <br> mounting hardware: (not included w/resistor) |
| -12 | 210-0583-00 |  |  | 1 | NUT, hex., 0.25-32 x 0.312 inch |
| $\begin{array}{r} -13 \\ -14 \end{array}$ | 210-0940-00 |  |  | 1 | WASHER, flat, 0.25 ID $\times 0.375$ inch OD |
|  | 210-0046-00 |  |  | 1 | WASHER, lock, internal, 0.261 ID x 0.40 inch OD |
| -15 | 426-0916-00 |  |  | 1 | FRAME, readout window |
| -16 | 331-0314-00 |  |  | 1 | WINDOW, readout |
| -17 | 426-0681-00 |  |  | 4 | FRAME, pushbutton |
| -18 | 333-1584-00 | B010100 | B039999 | 1 | PANEL, front |
|  | 333-1584-01 | B040000 |  | 1 | PANEL, front |
|  | ------ |  |  | 2 | mounting hardware: (not included w/panel) |
| -19 | 211-0159-00 |  |  | 2 | SCREW, 2-56 x 0.375 inch, PHS |
| -20 | 210-0405-00 |  |  | 2 | NUT, hex., 2-56 x 0.188 inch |

FIGURE 1 EXPLODED \& OPTION NO. 2 (cont)


Fig. \&


| -59 | 333-1620-00 | 1 | PANEL, front |
| :---: | :---: | :---: | :---: |
| -60 |  | 1 | CIRCUIT BOARD ASSEMBLY--AUTO-GATE (See A3 electrical list) |
|  | - - - - - - | - | mounting hardware: (not included w/circuit board assembly) |
| -61 | 211-0001-00 | 2 | SCREW, 2-56 x 0.25 inch, PHS |
| -62 | 179-1851-00 | 1 | WIRING HARNESS |
|  | 105-0356-00 | 1 | ACTUATOR ASSEMBLY |
|  | - - - - - | - | actuator assembly includes: |
| -63 | 200-1391-00 | 1 | COVER |
|  | - | - | mounting hardware: (not included w/cover) |
|  | 211-0022-00 | 2 | SCREW, (discard \& use ref. \#61) |
| -64 | 210-0001-00 | 2 | WASHER, lock, internal, 0.092 ID x 0.18 inch OD |
| -65 | 210-0405-00 | 2 | NUT, hex., 2-56 x 0.188 inch |
| -66 | 354-0219-00 | 1 | RING, retaining |
| -67 | 401-0057-00 ${ }_{1}$ | 1 | BEARING, front, w/bushing |
| -68 | 214-1139-00 | - | SPRING, flat, gold |
|  | 214-1139-021 | - | SPRING, flat, green |
|  | 214-1139-03 | - | SPRING, flat, red |
| -69 | 214-1127-00 | 1 | ROLLER, detent |
| -70 | 105-0355-00 | 1 | DRUM ASSEMBLY |
| -71 | 401-0056-00 | 1 | BEARING, rear |
| -72 | 210-0406-00 | 4 | NUT, hex., 4-40 x 0.188 inch |

$1_{\text {Replace }}$ only with part bearing the same color code as the original part in your instrument.


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## STANDARD ACCESSORIES

| Fig． 8 Index | Tektronix | Serial／Model No． |  | 0 |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | t | 1 | 2 | 3 | 4 | 5 | Description |
|  | Part No． | Eff | Disc |  |  |  |  |  |  |  |
| 2. | 070－1339－00 |  |  | 1 |  | AN | U |  | in | t shown） |



## MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.
A single change may affect several sections. Sections of the manual are often printed at different times, so some of the information on the change pages may already be in your manual. Since the change information sheets are carried in the manual until ALL changes are permanently entered, some duplication may occur. If no such change pages appear in this section, your manual is correct as printed.

DC501, DC502

## TEXT CORRECTION

The upper limit frequency response specifications has been changed to 110 MHz . Any reference to a 100 MHz should be changed to read: 110 MHz .

DC 502 EFF SN B040000-up

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES
REMOVE:

U167

U169

A1 670-2102-01
ADD :

U1
156-0118-00

156-0180-00
CHANGE TO:

> 670-3300-00

U2

156-0100-00
156-0100-00

Sing1e $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102

Single $40 \mathrm{MHz} \mathrm{J}-\mathrm{K}$ edge-triggered flip-flop, replaceable by SN74H102

MAIN Circuit Board Assembly

DIVIDE BY 5, Circuit Board Assembly
Dual 100 MHz J-K master-slave flip-flop, replaceable by SN74S112

Quad 2-input nand gate, replaceable by SN74S00N


DC 501 EFF SN B050000-up

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES

## CHANGE TO:

R310 306-0121-00 $120 \Omega, 2 \mathrm{~W}, 10 \%$

ADD :
R303 303-0132-00
$1.3 \mathrm{k} \Omega, 1 \mathrm{~W}, 5 \%$


DC501 EFF SN B050501
DC501-950A EFF SN B040492
DC501-950B EFF SN B050508
DC501-950D EFF SN B040500

## ELECTRICAL PARTS LIST CORRECTION

## CHANGE TO:

C110 283-0267-00
$0.01 \mu \mathrm{~F}$, Cer, $500 \mathrm{~V}, \pm 20 \%$

DC 501 EFF SN B060000-up
DC 502 EFF SN BO70000-up

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGE
Change to:
R137 311-1554-00 $200 \mathrm{k} \Omega$, Var
ADD:
C121 283-0111-00 $0.1 \mu \mathrm{~F}$, Cer, 50 V
(R137 and C121 are located on Diagram 1$\rangle$ COUNTER TIME BASE \& CONTROL)



DC 501, DC501-950A, DC501-950B, DC501-950D EFF SN B070000-up

DC 502, DC502-950A EFF SN B080000-up

ELECTRICAL PARTS LIST AND SCHEMATIC CHANGES
ADD:

| C252 | $281-0523-00$ | 100 pF, Cer $, 350 \mathrm{~V}, 20 \%$ |
| :--- | :--- | :--- |
| C 254 | $281-0523-00$ | $100 \mathrm{pF}, \mathrm{Cer}, 350 \mathrm{~V}, 20 \%$ |
| C 256 | $281-0523-00$ | $100 \mathrm{pF}, \mathrm{Cer}, 350 \mathrm{~V}, 20 \%$ |
| C 258 | $281-0523-00$ | $100 \mathrm{pF}, \mathrm{Cer}, 350 \mathrm{~V}, 20 \%$ |




[^0]:    $1_{\text {Option }} 2$ only.

[^1]:    ${ }_{2}$ Option 2 only.
    ${ }^{2}$ R235 \& S235 furnished as a unit

[^2]:    Crystal, 1 MHz
    Oscillator, RF, 5 MHz

