Tektronix®

PM 110
PERSONALITY MODULE FOR Z8001 MICROPROCESSOR

INSTRUCTION MANUAL

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PM 110
PERSONALITY MODULE FOR Z8001 MICROPROCESSOR

INSTRUCTION MANUAL

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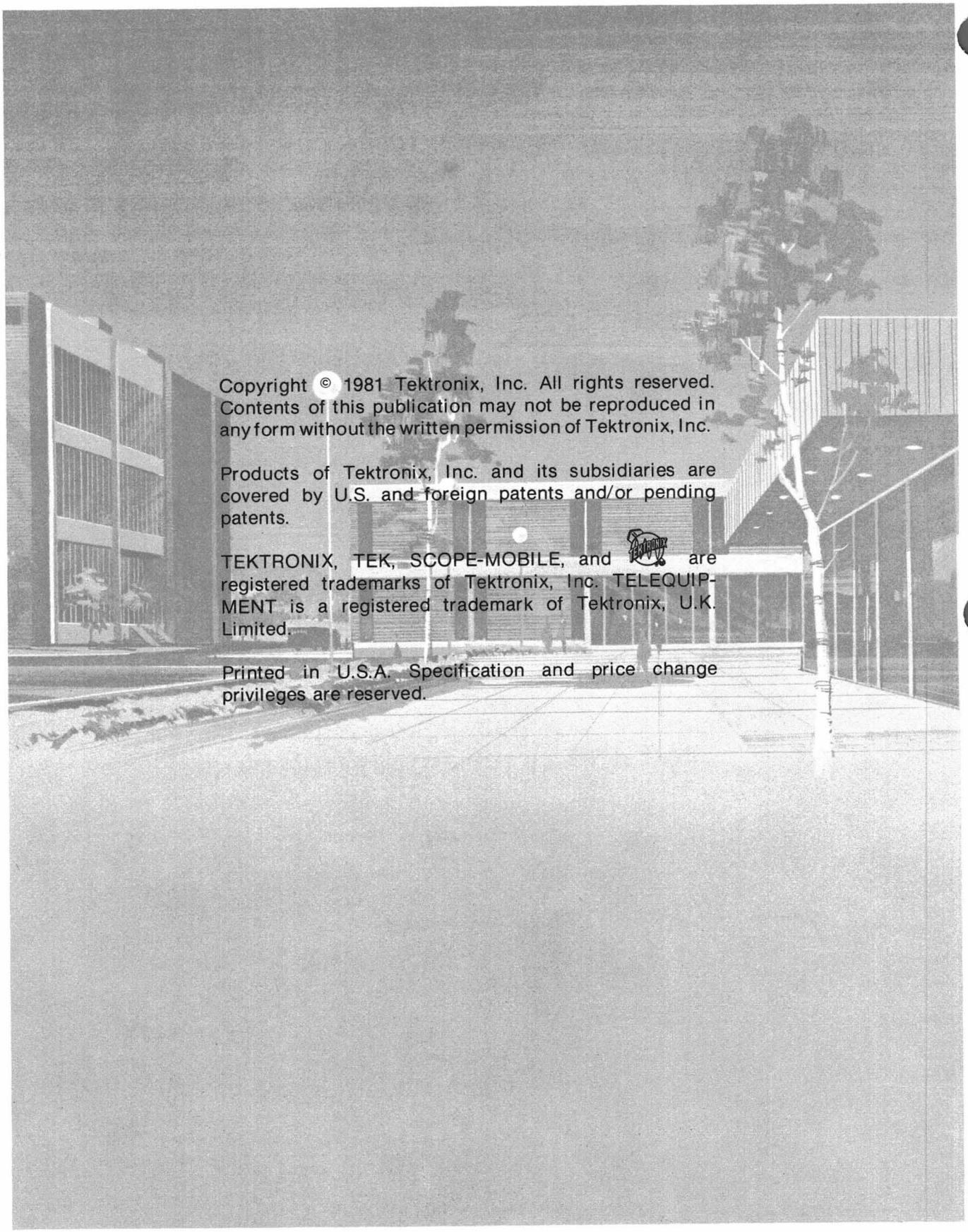

ABOUT THIS MANUAL

This manual describes operation and service of the PM 110 Personality Module. The operator's part of the manual describes connection of the personality module to the logic analyzer, connection of the personality module to the system under test (SUT), and other information necessary for operation. The service part of this manual is found after the colored divider page, and is intended for use by qualified personnel in servicing the personality module. It contains circuit descriptions, diagnostic techniques, schematic diagrams, and parts lists. Refer to the Table of Contents for the location of specific information.

The PM 110 supports the Z8001 microprocessor. The only logic analyzer currently supported by the PM 110 is the 7D02. The reader will require the following documentation:

7D02 Logic Analyzer Operator's Manual (P/N 070-2918-00)

7D02 Logic Analyzer Service Manual (P/N 070-2919-00)

Z8001 Manual.

Throughout this manual, references are made to signals. The reader should keep the following conventions in mind.

1. The overscore ($\overline{\ }$) over a signal name indicates that the signal is active or asserted in the low state. For example, $\overline{AS}$ is an active low signal. The default value is to the high state, so if no overscore appears over the signal name, the signal is an active high. Some lines are active high or low. For example, the R/$\overline{W}$ line is active high in the READ state, and active low in the WRITE state.

2. The text refers to the components on the schematic with an assembly, or board, number first, and then the component number. For example, A1U3XXX is a component on Board 1, the top board in the personality module pod. On the A1 schematic, the component is shown without the assembly number, e.g., U3XXX.

3. 'Zilog' and 'Z8001' are trademarks of Zilog, Inc., with whom Tektronix, Inc., is not associated.

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WARNING

The following servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

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LIST OF ILLUSTRATIONS

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OPERATOR'S SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and service personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or to other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accesible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found.

Symbols As Marked on Equipment

Attention - refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accesible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Do Not Operate in Explosive Atmosperes

To avoid explosion, do not operate this product in an explosive atmospere unless it has been certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

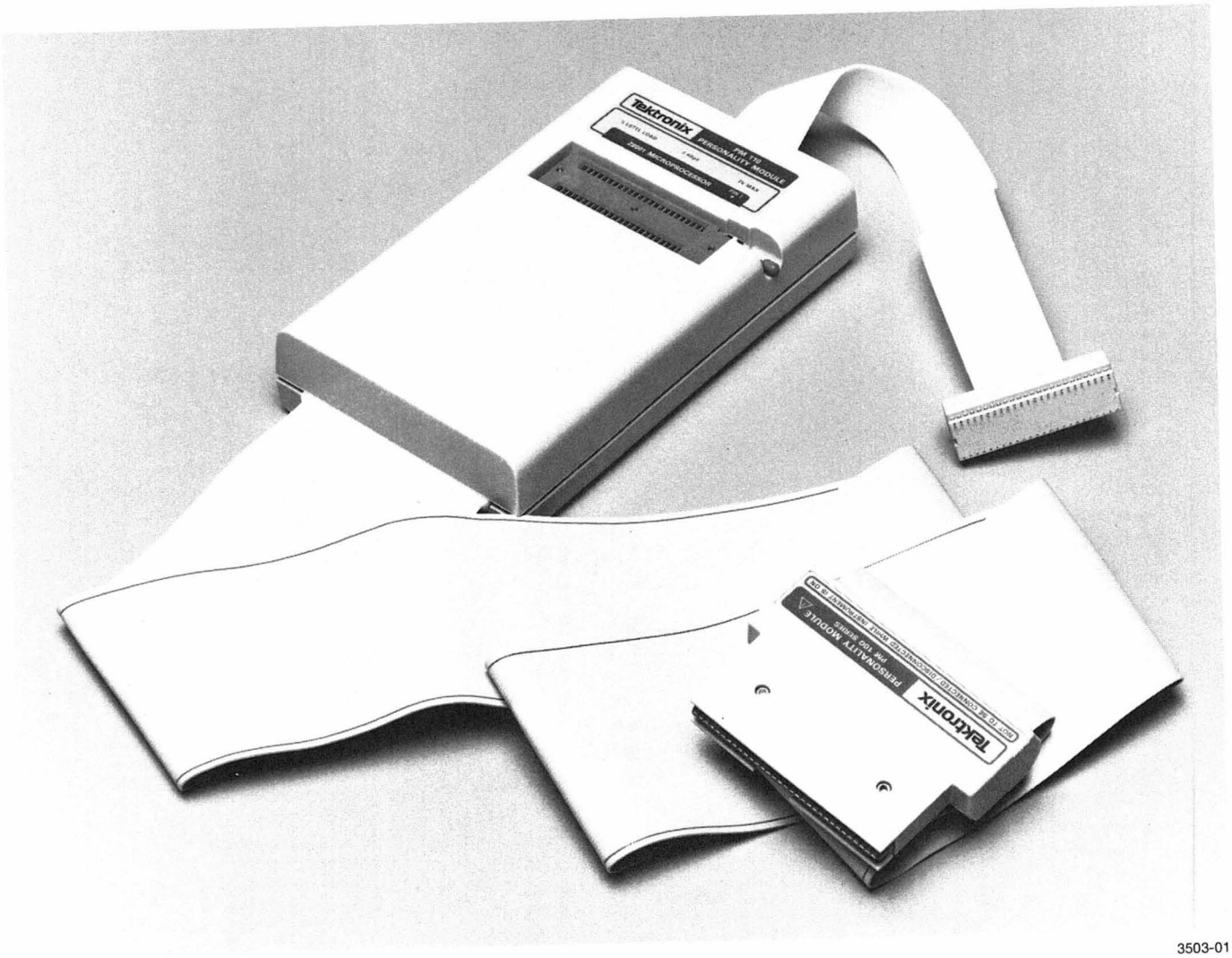
Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

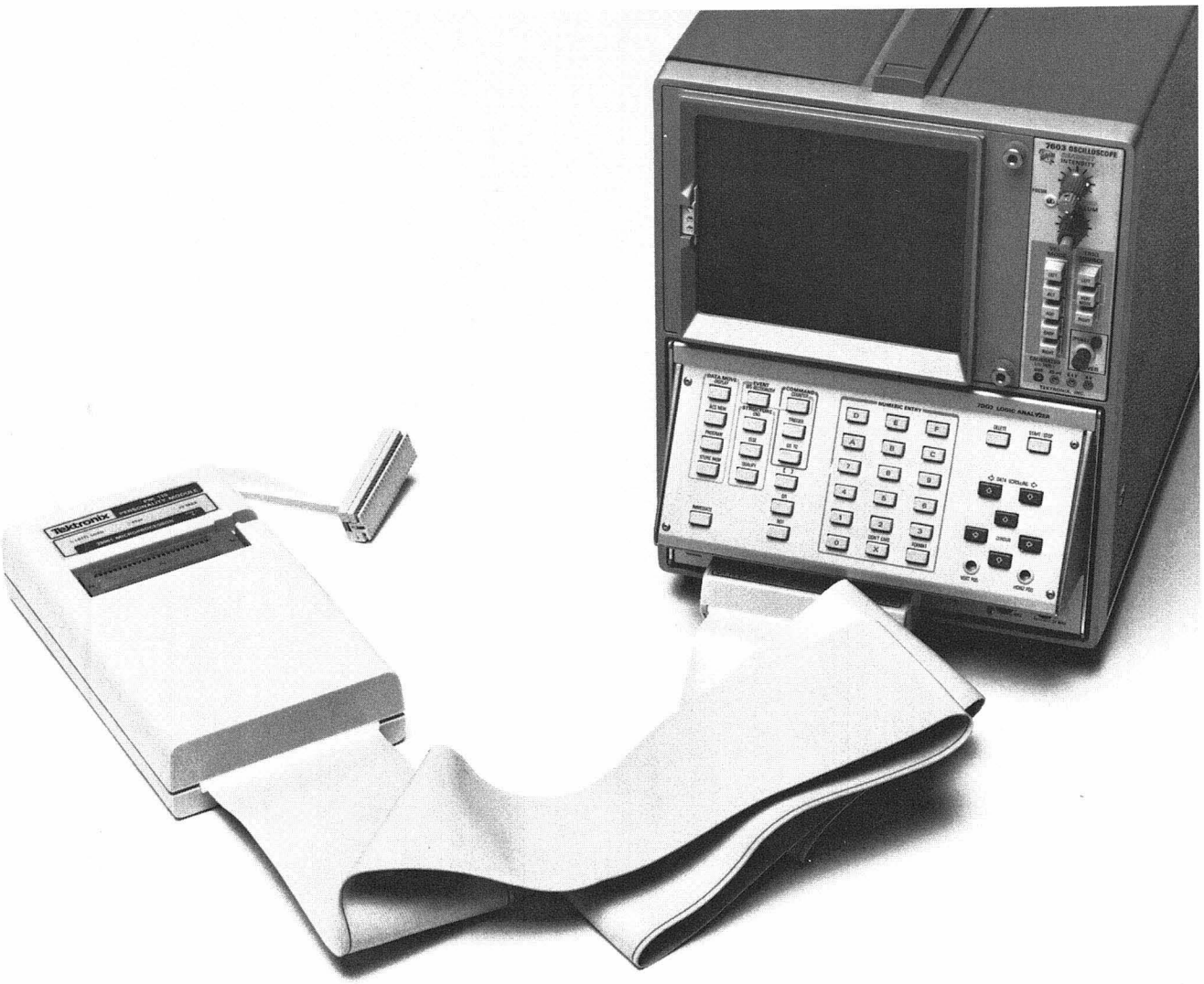
Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



3503-01

The PM 110 Personality Module



3503-02

Figure 1-1. The PM 110 Personality Module, connected to a 7D02 Logic Analyzer.

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Section 1

INTRODUCTION TO THE PM 110

The PM 110 Personality Module collects data from a Z8001-based system under test (SUT) and transfers it to a Tektronix logic analyzer in a format the logic analyzer can interpret.

Physically, the PM 110 personality module consists of a circuitry pod with a ribbon cable and logic analyzer plug on one end, and a flat ribbon cable with a microprocessor plug on the other end.

The microprocessor in the SUT is removed and plugged into the ZIF socket in the personality module. The personality module microprocessor plug is then inserted into the SUT, replacing the Z8001.

The Z8001 then drives the SUT as before, through the personality module. This allows the logic analyzer to monitor all communication between the Z8001 and the SUT.

The personality module performs the following separate functions:

1) Allows the logic analyzer to receive address, segment, data, and control information from the SUT.

2) Before data acquisition, the personality module sets up the acquisition hardware and personalizes the logic analyzer program display into a format for Z8001-based systems.

After data acquisition, the personality module allows the logic analyzer to disassemble and/or display the acquired data.

3) The personality module generates additional control signals, needed by the logic analyzer.

4) In self-test mode, the personality module outputs a predictable set of test signals designed to simulate a subset of Z8001 instructions and special modes. The self-test signals are used to test the personality module and logic analyzer.

To operate with the PM 110, the 7D02 Logic Analyzer requires the expansion option.

Section 2

OPERATING INSTRUCTIONS FOR THE PM 110 PERSONALITY MODULE

STORAGE AND INSTALLATION OF PERSONALITY MODULE

Storing the Personality Module

When storing the Personality Module, protect the microprocessor plug with anti-static foam. This prevents damage to the pins during storage and protects the Personality Module from static electricity.

NOTE

No plastic protector for the microprocessor plug is available for the PM 110.

Connecting Personality Module to Logic Analyzer

CAUTION

Always turn the mainframe power switch OFF before connecting the Personality Module to the logic analyzer mainframe. Before removing the microprocessor from your system under test and installing the microprocessor plug, turn off your system power switch. Failure to take this precaution may cause permanent damage to the logic analyzer, the personality module, and the system under test.

1. Turn mainframe power switch to the OFF position.

2. Insert the PM 110 logic analyzer plug, label side up, into the socket on the front of the Logic Analyzer.

Connecting Personality Module to the System Under Test (SUT)

1. Turn OFF the power to your SUT and the logic analyzer.

2. Ground yourself to drain static electricity.

3. Remove the microprocessor from your SUT and insert it into the ZIF socket in the Personality Module Pod. Be sure to insert

it correctly, with pin 1 of your microprocessor next to the lever on the ZIF socket.

4. Plug the PM microprocessor plug into the empty microprocessor socket on your SUT Again, make sure to insert the plug correctly. Pin 1 of the microprocessor plug is marked with a notch and an arrow.

5. Turn on the logic analyzer mainframe power switch and power up your SUT.

NOTE

To save wear to the microprocessor socket on your SUT, you may insert another socket into your SUT socket.

A socket appropriate for this purpose is available through your Tektronix Field Office. You may use two 24-pin socket instead of a 48-pin socket.

USING THE PERSONALITY MODULE

This sub-section describes how to operate the PM 110 Personality Module with a 7D02 Logic Analyzer. It does not contain general information on 7D02 operation. Consult a 7D02 Operator's Manual for that information.

The PM 110 firmware consists of (1) data used by the 7D02 for diagnostic parameters and powerup defaults, and (2) code interpreted by the 7D02 to format displays of data from the 7D02 acquisition memory. For information about diagnostic parameters, see the sections on Performance Check and Diagnostics.

7D02 Displays

The following 7D02 screen displays contain PM 110-specific elements. For information about signal lines, consult the Theory of Operation, and the Signal Glossary sections.

WD RECOGNIZER Event Format -- When the PM 110 is attached to the 7D02, the 7D02 WD RECOGNIZER key produces the following display. The radices of the data bus and address bus may be changed with the 7D02 FORMAT key.

```
DATA=XXXX
SEGMENT=XX
ADDRESS=XXXX
000=MEM W 001=MEM R   STATUS=X
010=I/O W 011=I/O R 100=RFSH X
101=FCH 1 110=ACK  111=FCH N X
N/S=X IRQ=X
R/W=X uOUT,EPU=X EXT TRIG=X
```

The following is an explanation of each field, and its use.

DATA --
Definition: The 16-bit data bus.
Generated by: The system under test (SUT) and the processor under test (PUT) in the ZIF socket.
Default radix: hexadecimal
Other radices available (7D02 FORMAT key): octal and binary
Stored in acquisition memory: Yes.

SEGMENT --
Definition: The 8 bits of the segment lines.
Generated by: The SUT and the PUT
Default radix: hexadecimal
Other radices available (7D02 FORMAT key): octal and binary
Stored in acquisition memory: Yes

ADDRESS --
Definition: The 16-bit address bus.
Generated by: The SUT and the PUT
Default radix: hexadecimal
Other radices available (7D02 FORMAT key): octal and binary
Stored in acquisition memory: Yes

STATUS=X
X
X

Definition: The status code of the Z8001 machine cycle. The user may select any one of the following:

Memory Write	000
Memory Read	001
I/O Write	010
I/O Read	011
Refresh	100
Fetch 1 (the first Z8001 cycle of an instruction)	101

@

Acknowledge (Interrupt or Segment Trap) 110

Fetch N (any Z8001 cycle but the first) 111

For example, if you selected Memory Read cycles, the display would look like this:

```
STATUS=0
       0
       1
```

N/$\overline{S}$ -- The buffered, encoded, Normal/$\overline{System}$ bit. In normal mode, this line reflects the N/$\overline{S}$ line of the Z8001. On I/O cycles, this line defines a Normal or Special I/O. This bit is stored in acquisition memory.

IRQ -- The buffered, encoded Interrupt Request line. Insert a 1 on this bit to check for any interrupt request from the SUT to the Z8001. This bit is stored in acquisition memory.

R/$\overline{W}$ -- The true buffered Read/$\overline{Write}$ signal from the Z8001. Insert a 1 for this status bit to detect any Read states. Insert a 0 to detect Write states.

μOUT,EPU -- The shared resource status bit. Insert a 0 to detect any shared resource transactions.

TRIGGER Command Format -- When the TRIGGER command key is pressed on the 7D02, the following display appears:

```
1 TRIGGER 0-MAIN
     0-BEFORE DATA
     0-SYSTEM UNDER TEST CONT.
     0-STANDARD CLOCK QUAL.
```

The PM 110 affects this display only in the CLOCK QUAL. field.

When the cursor is placed on this element, this display appears:

```
0-STANDARD CLOCK QUAL.
  0 STANDARD CLOCK QUAL.
  1 USER CLOCK QUAL.
```

If 1-USER CLOCK QUAL. is selected on the 7D02 screen, the following display will show:

```
1    1-FALLING EDGE OF CLOCK
       0 RISING EDGE OF CLOCK
       1 FALLING EDGE OF CLOCK
     C9-C4 (ANDED CLOCKS)=1X11XX
```

Clock qualification allows the user to select the edge of the SUT master clock on which data is considered to be valid and should be sampled. This qualified SUT clock is used by the logic analyzer to generate the State Clock. As shown in Figure 2-1, the default clock qualification state is 'Falling edge of SUT Master Clock, C9, C7, and C6 in high state.'

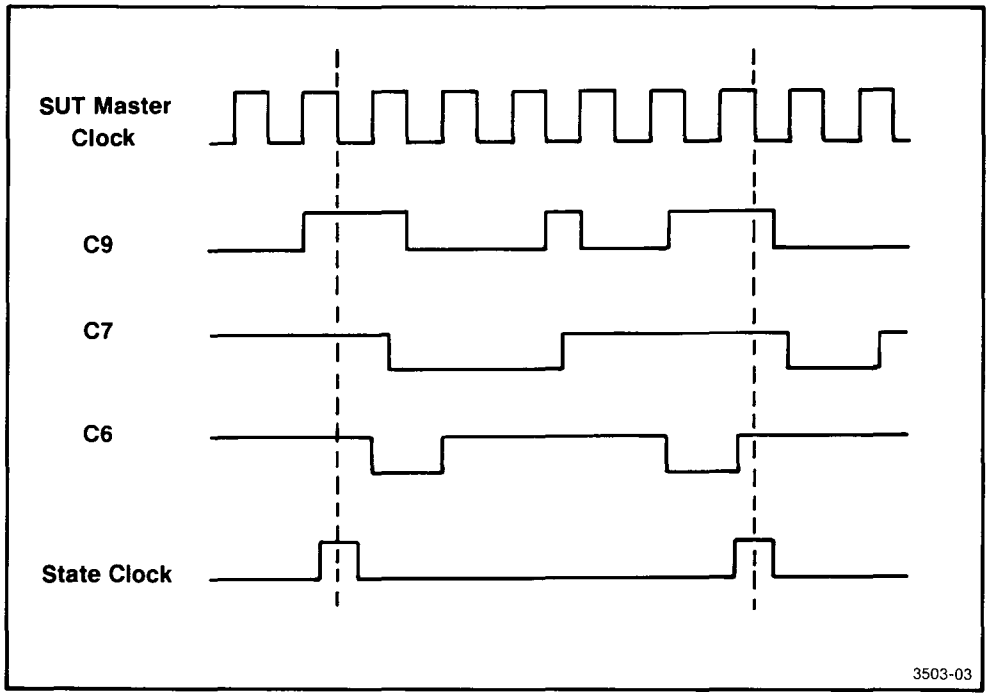

Figure 2-1. PM 110 master clock synthesis in default state: falling edge of SUT master clock; C9, C7, and C6 in positive state.

The control lines are as follows:

C9 -- The QUAL signal from the PM 110, normally used for clock qualification. This qualification bit defaults to a 1.

C8 -- The buffered $\overline{\text{WAIT}}$ request line to the Z8001. Used to qualify out Wait states when the normally used qualifier, C9, is not used. This qualification bit defaults to an X, or "don't care".

C7 -- The active low $\overline{\text{SUT}}$ $\overline{\text{HALTED}}$ line from the PM 110. The default value of this bit is always high, but if the user wants

to qualify on Halt states, he can enter an X or a 0 for this line (X is recommended).

NOTE

When single-stepping through a program (7D02 'SYSTEM UNDER TEST HALT' mode) put an X in C7. This will allow the logic analyzer to recognize an instruction regardless of the halt state.

C6 -- A PM 110-generated line used to qualify out bus cycles carrying no useful information. This line is active low on Internal Operation, Refresh, and Bus Acknowledge cycles. The default state of the qualification bit is high to prevent triggering on, or acquisition of, these cycles.

C5 -- The buffered Z8001 R/$\overline{W}$ signal. Default value is X.

C4 -- The "shared resource" qualification bit, active low. Default value is X.

NOTE

Redefining the state clock is not a normally recommended procedure, and may produce unpredictable results. If the TRIGGER-MAIN command is deleted from the 7D02 program, the values last entered in the USER CLOCK QUAL. are retained. The default state of STANDARD CLOCK QUAL. is restored after logic analyzer power-up or reselection of 0-STANDARD CLOCK QUAL.

FORMAT Mode Display -- The only field specific to the PM 110 is the

SEGMENTED=0, ELSE NONSEGMENTED

field.

The Z8001 operates in either segmented, or non-segmented mode. To correctly disassemble segmented mode operations, enter a 0. To disassemble non-segmented operations, enter a 1.

Mnemonic Disassembly Data Display -- The address, segment, data, and status information stored in the acquisition memory is formatted and displayed as follows:

```
LOC SEG ADDR    OPERATION      NI
ddd hh hhhh ttt*ttttttt?ttt    Nb
ddd hh hhhh     hhhh  sssss    Sb
```

```
ddd ** hhhh     hhhh  sssss    Nb
ddd hh hhhh ***    (hhhh)      Nb
dddThh-hhhh-----hhhh--sssss----Nb
ddd hh hhhh     hhhh  sssss    Nb
```

d -- a decimal digit indicating location in 7D02 memory

b -- a binary digit indicating interrupts

s -- The Status (see Status Definitions, below)

T -- the place where the 7D02 was triggered

h -- a hex digit

t -- an opcode

N or S -- Normal or System

*** -- Indicates an illegal opcode or non-supported instruction

* -- (in ttt*ttt) indicates missing data

? -- Indicates questionable opcode value or mnemonic

** -- in the segment field indicates possible invalid segment data output at this location.

@ -- Indirect addressing mode is being used.

NI -- The two stored control lines. The value under the 'N' indicates Normal or System mode. The value under the 'I' indicates an interrupt request to the Z8001. (A 1 indicates an interrupt was requested.)

Absolute Data Display --
Unless changed with the FORMAT key, the Absolute Data Display will have the following format:

```
LOC   SEG  ADDR   DATA  STATUS NI
ddd    nn  nnnn   nnnn  ssssss Nb
dddT---nn--nnnn---nnnn--ssssss-Sb
```

d -- a decimal digit indicating location in 7D02 memory

n -- an ASCII, hex, or octal digit

s -- the status word (see Status Definitions below)

T -- the place where the 7D02 triggered

N or S -- the NORMAL or SYSTEM mode

@

b -- a binary digit

Table 2-1

STATUS DEFINITIONS

FETCH1	Instruction Fetch, First Word
FETCHN	Instruction Space
MEMR	Data Memory Read Request
MEMW	Data Memory Write Request
VI ACK	Vectored Interrupt Acknowledge
NVI AK	Non-vectored Interrupt Acknowledge
NMI AK	Non-maskable Interrupt Acknowledge
SEG AK	Segment Trap Acknowledge
I/O W	Write I/O Reference
SI/O W	Write Special I/O Reference
I/O R	Read I/O Reference
SI/O R	Read Special I/O Reference
REFRSH	Memory Refresh

PM 110/Z8001 Irregularities

The following table shows assembly listing differences between Zilog, AMD, and the PM 110 in segmented and non-segmented mode.

Table 2-2

Z8001 LISTING DIFFERENCES

Addressing Mode	Zilog	AMD	PM 110 Non-Seg.	PM 110 Seg.
Immediate Data (IM)	#%FF2D	#FF2D	#FF2D	#FF2D
Indirect Register (IR)	@R11	R11^	@R11	@RR11?
Direct Address (DA)	%1234	#1234^	1234	561234
Indexed Address (X)	%1234(R7)	1234(R7)	1234(R7)	561234(R7)
Relative Address (RA)	#+12	label(12)	absolute address	
Based Address (BA)	R8(#%1234)	R8^(1234)	R8(#1234)	RR8(#1234)
Based Indexed Address (BX)	R8(R4)	R8^(R4)	R8(R4)	RR8(R4)

1. Zilog used the percent sign only to indicate that the following number will be in hex. The PM 110 will display data and addresses always in hex in mnemonic mode so a base indicator is not used in the display.

2. A HALT message from the 7D02 or the system under test will not be detected until the next FETCH1 cycle. This may cause some confusion while using the 'SYSTEM UNDER TEST HALT' mode. The use may want to do one of the following:

a) Change the program to USER CLOCK QUAL, and enter C9-C4=1XX1XX. This will qualify out halt states, and allow the logic analyzer to acquire data for display.

b) Change the program to USER CLOCK QUAL, and enter C9-C4=1XXXXX. This will allow the logic analyzer to trigger on the desired data, and display it, and its Read/Writes. The rest of the acquisition memory space will be filled with refresh cycles.

3. An $\overline{\text{NMI}}$ request may not be seen immediately following an Interrupt Acknowledge cycle, if the $\overline{\text{NMI}}$ request occurred during the cycle.

SUPPORTED INSTRUCTIONS

The following Z8001 instructions are supported by PM 110 firmware. Note that 'B' following an instruction indicates 'Byte'.

ADC	Add with Carry
ADCB	Add with Carry
ADD	Add
ADDB	Add
ADDL	Add
AND	And
ANDB	And
BIT	Bit Test
BITB	Bit Test
CALL	Call Procedure
CALR	Call Procedure Relative
CLR	Clear
CLRB	Clear
COM	Complement
COMB	Complement
COMFLG	Complement Flag
CP	Compare (Immediate or Register)
CPB	Compare (Immediate or Register)
CPL	Compare (Register)
CPD	Compare and Decrement
CPDB	Compare and Decrement
CPDR	Compare, Decrement, and Repeat
CPDRB	Compare, Decrement, and Repeat
CPI	Compare and Increment
CPIB	Compare and Increment
CPIR	Compare, Increment, and Repeat
CPIRB	Compare, Increment, and Repeat
CPSD	Compare String and Decrement
CPSDB	Compare String and Decrement
CPSDR	Compare String, Decrement, and Repeat
CPSDR	Compare String, Decrement, and Repeat
CPSI	Compare String and Increment
CPSIB	Compare String and Increment
CPSIR	Compare String, Increment, and Repeat
CPSIRB	Compare String, Increment, and Repeat
DAB	Decimal Adjust Bit
DEC	Decrement
DECB	Decrement
DI	Disable Interrupt
DIV	Divide
DIVL	Divide
DJNZ	Decrement, Jump if Not Zero
DBJNZ	Decrement, Jump if Not Zero
EI	Enable Interrupt
EX	Exchange
EXB	Exchange

EXTS	Extend Sign
EXTSB	Extend Sign
EXTSL	Extend Sign
HALT	Halt
IN	Input
INB	Input
INC	Increment
INCB	Increment
IND	Input and Decrement
INDB	Input and Decrement
INDR	Input, Decrement, and Repeat
INDRB	Input, Decrement, and Repeat
INI	Input and Increment
INIB	Input and Increment
INIR	Input, Increment, and Repeat
INIRB	Input, Increment, and Repeat
IRET	Interrupt Return
JP	Jump
JR	Jump Relative
LD	Load into Register, Memory, or Load Immediate into Memory
LDB	Load into Register, Memory, or Load Immediate into Memory
LDL	Load into Register or Memory
LDA	Load Address
LDAR	Load Address Relative
LDCTL	Load to or from Control Register
LDCTLB	Load into or from Flag Byte Register
LDD	Load and Decrement
LDDB	Load and Decrement
LDDR	Load, Decrement, and Repeat
LDDRB	Load, Decrement, and Repeat
LDI	Load and Increment
LDIB	Load and Increment
LDIR	Load, Increment, and Repeat
LDIRB	Load, Increment, and Repeat
LDK	Load Constant
LDM	Load Multiple
LDPS	Load Program Status
LDR	Load (Store) Relative
LDRB	Load (Store) Relative
LDRL	Load (Store) Relative
MBIT	Multi-Bit Test
MREQ	Multi-Micro Request
MRES	Multi-Micro Reset
MSET	Multi-Micro Set
MULT	Multiply
MULTL	Multiply
NEG	Negate
NEGB	Negate
NOP	No Operation
OR	Or
ORB	Or
OTDR	Output, Decrement, and Repeat
OTDRB	Output, Decrement, and Repeat

OTIR	Output, Increment, and Repeat
OTIRB	Output, Increment, and Repeat
OUT	Output
OUTB	Output
OUTDB	Output and Decrement
OUTI	Output and Increment
OUTIB	Output and Increment
POP	Pop
POPL	Pop
PUSH	Push
PUSHL	Push
RES	Bit Reset, Static or Dynamic
RESB	Bit Reset, Static or Dynamic
RESFLG	Reset Flag
RET	Return from Procedure
RL	Rotate Left
RLB	Rotate Left
RLC	Rotate Left Through Carry
RLCB	Rotate Left Through Carry
RLDB	Rotate Left Digit
RR	Rotate Right
RRB	Rotate Right
RRC	Rotate Right Through Carry
RRCB	Rotate Right Through Carry
RRDB	Rotate Right Digit
SBC	Subtract with Carry
SBCB	Subtract with Carry
SC	System Call
SDA	Shift Dynamic Arithmetic
SDAB	Shift Dynamic Arithmetic
SDAL	Shift Dynamic Arithmetic
SDL	Shift Dynamic Logical
SDLB	Shift Dynamic Logical
SDLL	Shift Dynamic Logical
SET	Bit Set (Dynamic or Static)
SETB	Bit Set (Dynamic or Static)
SETFLG	Set Flag
(S)IN	Input
(S)INB	Input
(S)IND	Input and Decrement
(S)INDB	Input and Decrement
(S)INDR	Input, Decrement, and Repeat
SINDRB	Input, Decrement, and Repeat
(S)INI	Input and Increment
(S)INIB	Input and Increment
(S)INIR	Input, Increment, and Repeat
SINIRB	Input, Increment, and Repeat
SLA	Shift Left Arithmetic
SLAB	Shift Left Arithmetic
SLAL	Shift Left Arithmetic
SLL	Shift Left Logical
SLLB	Shift Left Logical
SLLL	Shift Left Logical

@

SOTDR	Special Output, Decrement, and Repeat
SOTDRB	Special Output, Decrement, and Repeat
SOTIR	Special Output, Increment, and Repeat
SOTIRB	Special Output, Increment, and Repeat
(S)OUT	Output
(S)OUTB	Output
(S)OUTD	Output and Decrement
SOUTDB	Output and Decrement
(S)OUTI	Output and Increment
SOUTIB	Output and Increment
SRA	Shift Right Arithmetic
SRAB	Shift Right Arithmetic
SRAL	Shift Right Arithmetic
SRL	Shift Right Logical
SRLB	Shift Right Logical
SRLL	Shift Right Logical
SUB	Subtract
SUBB	Subtract
SUBL	Subtract
TCC	Test Condition Code
TCCB	Test Condition Code
TEST	Test
TESTB	Test
TRDB	Translate and Decrement
TRDRB	Translate, Decrement, and Repeat
TRIB	Translate and Increment
TRIRB	Translate, Increment, and Repeat
TRTDB	Translate, Test, and Decrement
TRTDRB	Translate, Test, Decrement, and Repeat
TRTIB	Translate, Test, and Increment
TRTIRB	Translate, Test, Increment, and Repeat
TSET	Bit Test and Set
TSETB	Bit Test and Set
XOR	Exclusive OR
XORB	Exclusive OR

Section 3

SPECIFICATIONS

This section of the manual lists the electrical, mechanical, and environmental characteristics of the PM 110 Personality Module. Since the PM 110 operates only as part of a logic analyzer system, all operating voltages and currents are furnished by the logic analyzer to which the PM 110 is connected.

If verification of these listed electrical characteristics is required for customer incoming inspection or other purposes, the Performance Check section lists the necessary test equipment and procedures.

Items listed in the Supplemental Information column are either explanatory notes or performance characteristics for which no limits are specified. They may not be verified.

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFO.
TTL Input Levels		0 V - 7 V Signal Swing
Input Impedance		1/2 LSTTL load with 40 pF nominal
Voltage in low limits (operating)		0.0 V min., 0.5 V max.
Voltage in high limits (operating)		2.0V min., 7.0V max.
Current in low limits (VIL=0.4V)		-0.2 mA max.
Current in high limits (VIH=2.7V)		0.02 mA max.
Maximum Voltage in, non-operating, non-destructive		-7V to +7V continuous
Threshold Voltage		+1.4V nominal (TTL Compatible)
Hysteresis		0.2V minimum
$\overline{\text{STOP}}$ output drive		

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VOH		2.4V, IOH=0.5 mA
VOL		0.5V, IOL=1 mA
Clock Input		
Resistance		50 kilohms nominal
Capacitance		40 pF nominal
Clock Period	165 ns min.	
Clock Pulse Width (min.)		70 ns high, 70 ns low
Threshold Voltage		Fixed 1.4V nominal (TTL compatible)
Hysteresis		.4 V nominal
Voltage in high limits (operating)		Min. 2.0V, max. 7.0V
Voltage in low limits (operating)		Min. 0.0 V max. 0.6 V
Maximum voltage in, non-operating non-destructive		-15V to +15V
Delay through ECL clock		10.5 ns min., 14.5 ns max.
Delay added to STOP (from microprocessor plug to ZIF)		63 ns max.
Data channel delay DI0-15		35 ns max.
Address channel delay AI0-15		65 ns max.
Address channel		

delay from SN0-6 to AI16-AI23		75 ns max.
Address channel delay from ST0-1 to AI16-17		60 ns max.
Control channel delay C5, C8		38 ns max.
Self Test Clock		
Clock Period		148 ns +/-17 ns
Clock Pulse Width (High and Low)		55 ns min.
Data Line		
Setup	32 ns min.	
Hold	3 ns min.	Relative to SUT clock T3 falling edge
Address AD0-15		Setup 15 ns min., Hold 23 ns min. relative to $\overline{AS}$ rising edge
SN0-SN6		Setup 25 ns min. Hold 25 ns min Relative to $\overline{AS}$ rising edge
N/$\overline{S}$		Setup 86 ns min., Hold 0 ns min., Relative to falling edge of T3
$\overline{AS}$		Setup 78 ns min., Pulse Width 42 ns min., relative to rising edge of T2
R/$\overline{W}$		Setup 65 ns min., Hold 0 ns min., Relative to rising edge of T2
ST0-3		Setup 65 ns min. Hold 0 ns min. Relative to rising edge of T2

$\overline{\text{WAIT}}$	Setup 55 ns min., Hold 24 ns min. For Memory or I/O cycles, relative to trailing edge of T2 or TWA. For Acknowledge cycles, TWA3 or TWA5.
$\overline{\text{MO}}$, $\overline{\text{BUSAK}}$	Setup 85 ns min., Hold 0 ns min. relative to trailing edge of T3
$\overline{\text{VI}}$, $\overline{\text{NVI}}$	Setup 110 ns min. hold 0 ns min. relative to trailing edge of T3
$\overline{\text{SEGT}}$	Setup 85 ns min., Hold 0 ns min. relative to trailing edge of T3
$\overline{\text{NMI}}$	Setup 110 ns min., Pulse Width 28 ns min. Relative to trailing edge of T3
Size	4.7 x 8 x 1.7 inches (12 x 20.3 x 4.3 cm)
Weight	2.15 lbs. (1 kg approx.)
Cable Length (logic analyzer to pod)	4 ft. +/- 1 inch (122 cm. +/- 2.5 cm)
Cable Length (microprocessor plug to personality module conductor in module pod)	13 inches +/- 1/2 inch (33 cm. +/- 1.2 cm.)
Operating Temperature	-15 degrees C to

	+55 degrees C
Non-operating Temperature	-62 degrees C to +85 degrees C
Relative humidity	95 to 97% 5 24-hour cycles @ 30 degrees C to 60 degrees C
Operating Altitude	4.5 km (15,000 feet)
Non-operating Altitude	15 km (50,000 feet)

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

Section 4

THEORY OF OPERATION

OVERVIEW

The primary function of a Personality Module is to collect data from a system under test (SUT) and transfer it to the logic analyzer in a format that the logic analyzer can interpret. With the Z8001 in the PM 110 ZIF socket and the PM 110 microprocessor plug replacing the Z8001 in its SUT socket, the SUT operates through the PM 110. This allows the logic analyzer to monitor almost all communication between the Z8001 and the rest of the system.

The PM 110 Personality Module performs the following separate tasks:

1. The PM 110 allows the logic analyzer to acquire data from the system as the system operates.

2. Before the logic analyzer acquires data, the personality module PROM

   a. sets up the acquisition hardware
   b. personalizes the logic analyzer program display into a format for Z8001-based systems.

After the logic analyzer acquires data, the personality module allows the logic analyzer to

   a. display the acquired data in a usable format.
   b. disassemble the acquired data into Z8001 mnemonics, if desired.

3. The personality module generates additional control signals needed by the logic analyzer, which are not provided by the SUT. This includes correctly timing the data acquisition during Z8001 Wait states, and specifying interrupt types.

4. The personality module provides the logic analyzer with an ECL clock. The Z8001 SUT clock is buffered and sent to the logic analyzer. The personality module also converts the ECL clock to TTL levels for internal use in the personality module.

5. The personality module allows SUT execution to be halted by either the SUT or the logic analyzer. When the system is halted, the personality module outputs a "Z8001 HALTED" message to the logic analyzer.

6. In self-test mode, the personality module outputs a predictable set of test signals, designed to simulate a subset of Z8001

instructions and special modes. The signals may be used to test the personality module and the logic analyzer.

Refer to Figure 4-1, the Block Diagram, and the schematics in DIAGRAMS AND BOARD ILLUSTRATIONS.

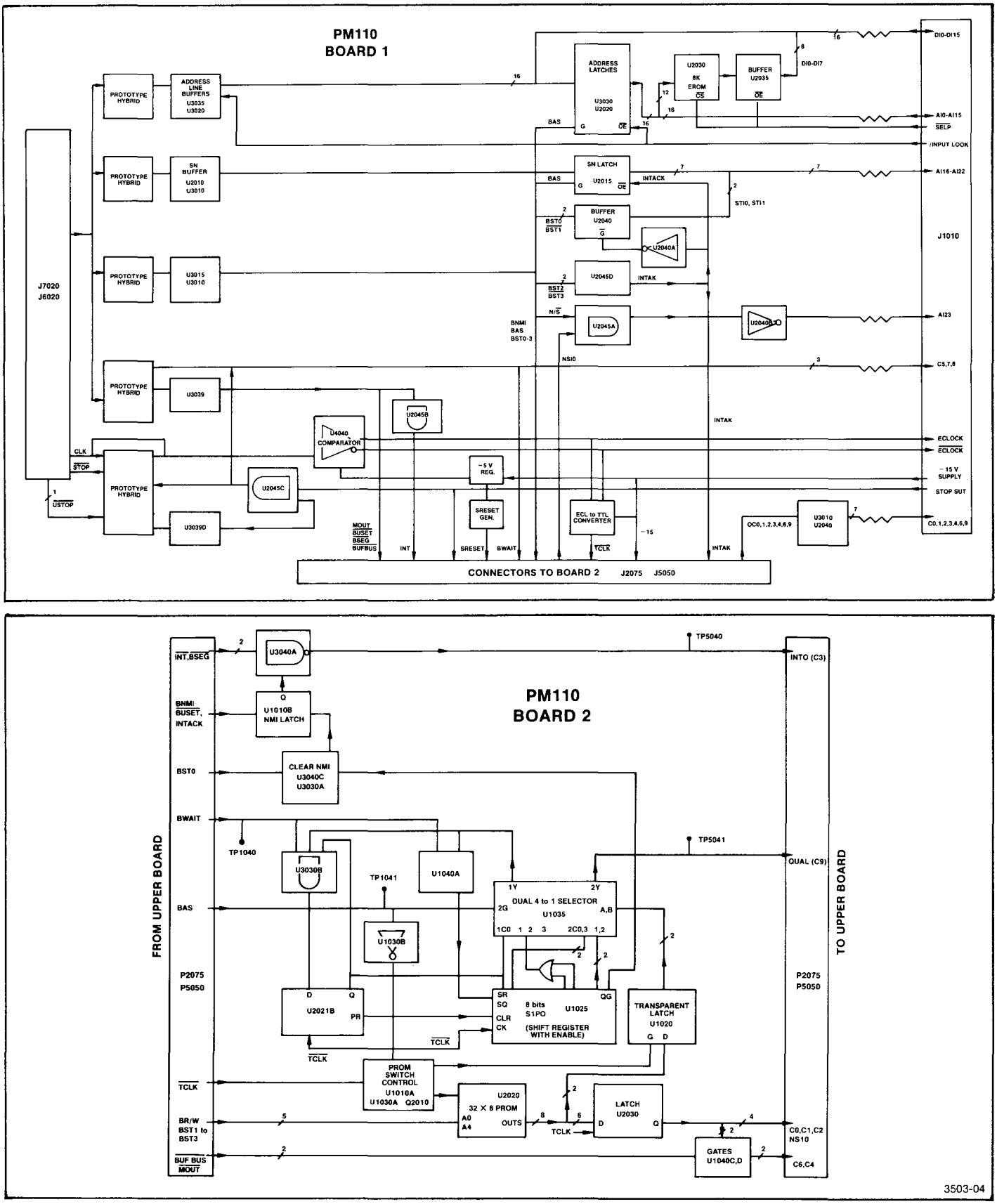


Figure 4-1. The PM 110 Block Diagram.

System Description

The PM 110 Personality Module provides the logic analyzer with 16 Data/Address lines, 7 Segment lines and an N/$\overline{S}$ bit. It also provides the ECL-level clock, and 10 control lines.

The logic analyzer provides the PM 110 with power and the following three control lines.

$\overline{\text{INPUT LOOK}}$ -- This signal disables the PM 110 address/data input circuitry, halting the data flow from the SUT to the logic analyzer.

$\overline{\text{SEL P}}$ -- This signal enables the PROM in the personality module. The PROM then sends information to disassemble the acquired data in the logic analyzer.

$\overline{\text{STOP SUT}}$ -- This signal allows the user to halt the SUT after any point in the logic analyzer program.

All signals to and from the logic analyzer except the clock are TTL-compatible.

Some of the 10 control lines to the logic analyzer are generated by the Z8001 SUT. Others are encoded by the PM 110.

The first 4 control lines are stored by the logic analyzer and used as primary events for word recognition:

C0 -- buffered, encoded R/$\overline{W}$. Active low on Memory or I/O Writes, low on refresh and Interrupt Acknowledge cycles.

C1 -- encoded signal. High on I/O, Interrupt Acknowledge, and FetchN. (FetchN = any logic analyzer data fetch cycle but the first, Fetch1.) Low on Memory, Fetch1, EPA transfer (Extra Processor Application, where another microprocessor is being used in parallel), Reserved, Internal Operation, and Refresh cycles.

C2 -- Encoded signal. Active high on Fetch, Interrupt Acknowledge, and Refresh cycles.

C3 -- Interrupt Request encoded signal. Combined $\overline{\text{NMI}}$, $\overline{\text{VI}}$, $\overline{\text{NVI}}$ and $\overline{\text{SEGT}}$. C3 is active high on these interrupt cycles.

The next two control lines are not stored by the logic analyzer, but are used as primary events for word recognition and used as clock qualifiers.

C4 -- Active low indicates a shared resource transaction (another microprocessor sharing the system, EPU, EPA and $\overline{\text{MO}}$ Read or Write cycles).

C5 -- The Z8001 R/$\overline{W}$ signal.

The last four control lines are not stored by the logic analyzer and are used as clock qualifiers only.

C6 -- An encoded signal used to qualify out bus cycles with no useful information. Active low on Internal Operation, Refresh, and Bus Acknowledge cycles.

C7 -- encoded $\overline{\text{SUT HALTED}}$ line from the PM 110 to the logic analyzer. Active low indicates either the SUT or the logic analyzer has halted the Z8001.

C8 -- buffered, inverted Wait request signal. C8 is used to qualify out WAIT states.

C9 -- encoded general clock qualifier. Active high.

CIRCUIT DESCRIPTION

T States

Reference will be made to "T States" throughout this section. This refers to the clock cycles of the SUT clock, which drives the Z8001, logic analyzer, and personality module. Each clock cycle at pin 35 of the Z8001 is described as a "T State". The first cycle being T1, the second, T2, etc.

Clock

The logic analyzer requires ECL-level clocking. The CLOCK signal from the SUT is input to the Clock Comparator, A1U4040. The ECL output is sent to the logic analyzer on ECLOCK and $\overline{\text{ECLOCK}}$. ECLOCK may be checked at A1TP3045.

The personality module requires TTL-level clocking. The negative-going output from the ECL Clock Comparator is input to the ECL-to-TTL Converter. The Converter, consisting of transistors A1Q3045, A1Q3040, A1Q3041, and A1Q3042, sends its TTL output, $\overline{\text{T CLK}}$, to the personality module lower board. $\overline{\text{T CLK}}$ may be checked at A1TP1015 on Board 1, and A2TP1042 on Board 2.

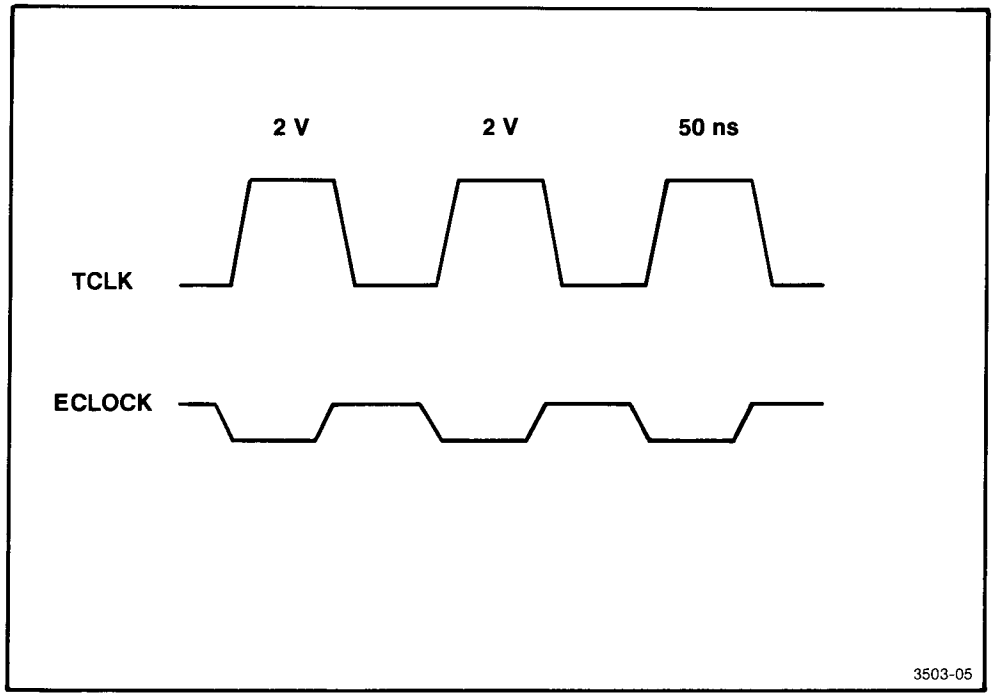


Figure 4-2. Clock circuitry timing relationships.

Address Strobe

The BAS is used to strobe data, address, and control information into the logic analyzer. This line is the buffered, inverted, Z8001 $\overline{AS}$ line. Check this line on A1TP4020 on Board 1, and A2TP1041 on Board 2.

Data Acquisition

Sixteen address and data (multiplexed) lines are taken from the Z8001 in the ZIF socket (J6010) and applied to buffers and latches in the personality module.

Data is buffered by input buffers A1U3035 and A1U3020 directly to the logic analyzer on DI0-DI15.

Addresses are buffered by input buffers A1U3035 and A1U3020, and then latched by A1U3030 and A1U2020. Addresses are available at the beginning of any CPU cycle. See the timing diagram in Figure 4-5. Note that the address latches are driven by the BAS line.

The logic analyzer receives address information on AI0-AI15.

The seven segment lines, SN0-SN6, are latched by A1U2015. A1U2015 is driven by BAS, just like the address latches. This means that the segment information goes to the logic analyzer at the same time as the addresses -- at the beginning of the CPU cycle. See the timing diagram in Figure 4-5.

Two of the segment lines to the logic analyzer, AI16 and AI17, and multiplexed -- used for two purposes. During interrupts, AI16 and AI17 send interrupt decode information to the logic analyzer. See "Interrupts".

Reading The Personality Module PROM

After data acquisition, the logic analyzer disables the input buffers and address latches by pulling the $\overline{\text{INPUT LOOK}}$ line high. The logic analyzer then enables the PROM (A1U2030) by pulling the $\overline{\text{SEL P}}$ line low. The PROM then sends disassembly information on the acquired data to the logic analyzer on DI0-DI7.

AI23

Line AI23 to the logic analyzer is multiplexed. In normal mode, it carries the N/$\overline{\text{S}}$ status bit of the Z8001. On I/O cycles, it defines a Normal or Special I/O. This is possible since all I/O are known to be on System status. The signal on AI23 comes from an AND gate, A1U2045. One input is the N/$\overline{\text{S}}$ line from the Z8001. The other input, NSIO, is produced by the PM 110 status decode circuitry on the lower board. NSIO is only low for Special I/O.

Interrupts

The Z8001 is capable of four different interrupt states: $\overline{\text{SEGT}}$, $\overline{\text{NMI}}$, $\overline{\text{NVI}}$, and $\overline{\text{VI}}$. When one of these interrupt states occurs, the Z8001 status lines, ST3-ST0, output the following codes:

@

Table 4-1

STATUS PIN STATES

Status Pin	ST3	2	1	0
$\overline{\text{SEGT}}$	0	1	0	0
$\overline{\text{NMI}}$	0	1	0	1
$\overline{\text{NVI}}$	0	1	1	0
$\overline{\text{VI}}$	0	1	1	1

Status pins ST0 and ST1 contain enough information to determine which one of the four interrupt states exist. ST0 and ST1 are buffered into lines STI0 and STI1, respectively, and sent to the logic analyzer on AI16 and AI17 (after A1U2015 is tri-stated by the INTACK line).

The INTACK line is produced by the PM 110 by ANDing together the buffered ST2 line, BST2, and the inverted ST3 line. As shown in table 4-1, these two lines ANDed together (with ST3 inverted) would produce a high signal on the INTACK line.

The high signal on the INTACK line serves two purposes: 1) it tri-states A1U2015, clearing AI16 and AI17 of segment address information, making these lines available for STI0 and STI1. 2) It serves as input to the NMI Latch on the lower board. The NMI Latch on the lower board is part of the circuitry that generates C3, or IRQ to the logic analyzer.

C3 goes to its active high state whenever $\overline{\text{VI}}$, $\overline{\text{NVI}}$, $\overline{\text{SEGT}}$, or $\overline{\text{NMI}}$ are activated. The first three are level-sensitive, and $\overline{\text{NMI}}$ is edge-sensitive. The Z8001 samples all interrupts at the rising edge of the last clock cycle. $\overline{\text{VI}}$ and $\overline{\text{NVI}}$ are ANDed together on A1U2045B. The resulting signal, INT, is sent to the lower board, where it is NANDed with the buffered $\overline{\text{SEGT}}$, BSEG, and the latched $\overline{\text{NMI}}$ line on A2U3040A. A2U3040A outputs a high whenever one of the level sensitive interrupt requests goes active low, or whenever the edge-sensitive $\overline{\text{NMI}}$ line is latched by A2U1010B. A2U3040A output, named INTO, may be tested on A2TP5040. It goes back to board 1, is buffered, and sent to the logic analyzer on the C3 control line.

The NMI latch is cleared only when an active INT is detected during T7 of an Interrupt Acknowledge.

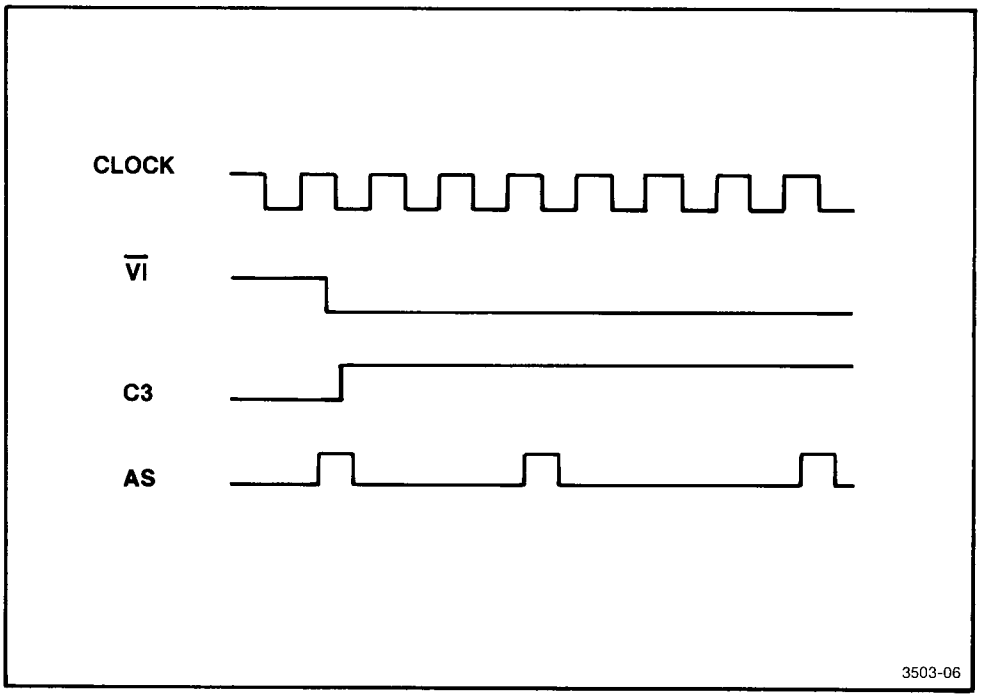


Figure 4-3. Interrupt timing relationships.

Control Line Encoder

The Control Line Encoder on board 2 receives input from the BAS, $\overline{TCLK}$, BWAIT, BR/$\overline{W}$, and the four buffered status lines, BST0-3.

The BAS line marks the T1 cycle. It may be tested on board 2 on A2TP1041. BAS clears A2U1025 and presets A2U2021B and A2U1010A. At the same time, it turns on A2U2020, which is kept on by A2U1010A until the leading edge of the clock after BAS returns low. Check the output of A2U1010A (inverted to active low) on A2TP1020. See Figure 4-4.

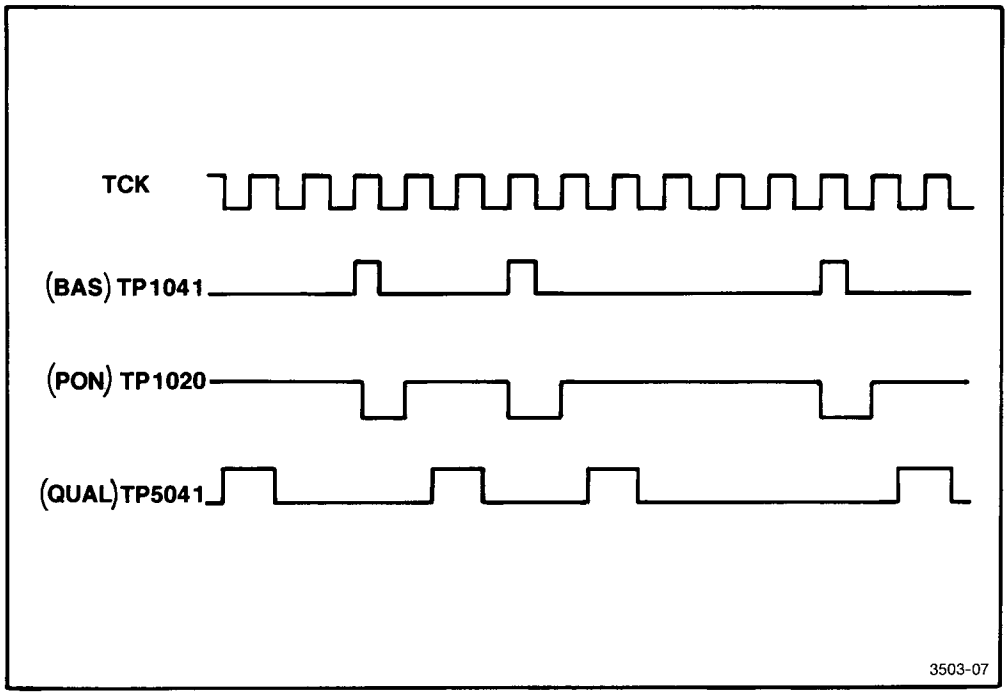


Figure 4-4. Timing relationship of BAS on A2TP1041 to A2TP1020.

While BAS is high, BR/$\overline{W}$, and BST0-3 are valid inputs to the Control Line Decoder PROM A2U2020. These five lines define the type of Z8001 cycle. From these five inputs, A2U2020 is programmed to generate control lines and also input a signal to the C9 Generator.

Table 4-2
C9 GENERATOR INPUT

Z8001 CPU Cycle	A2U2020 Output to C9 Generator	
	D07	D06
Internal Operation, Refresh	0	0
Interrupts and Segments Trap	0	1
EPA Transfer, Standard I/O, Special I/O	1	0
Data Address Space, EPU Transfer; Stack Address Space, EPU Transfer; Data Address Space; Stack Address Space; Reserved; Program Address Space; Program Address Space, First Word of Instruction	1	1

C9 Generator

The function of the C9 Generator is the generation of the C9 (QUAL) signal at the right time.

Multiplexer A2U1035 works with the shift register A2U1025 and flip-flop A2U2021B to generate the QUAL line (which is later buffered and sent to the logic analyzer on C9). When BAS goes active high, at the beginning of the CPU cycle, the shift register is cleared and the flip-flop is set, causing A2U1035 to output a signal on the QUAL line. If there are no Wait states, a high pulse will propagate from A2U2021B through the shift register on every trailing edge of the clock.

Wait states are detected by the Z8001 on the falling edge of the clock. Wait states can be detected only if A2P2030 and A2P1020 are jumpered across pins 2-3.

If Wait states occur, the C9 Generator waits for the correct number of clock cycles before putting a high signal on the QUAL line.

There are four different types of Z8001 CPU cycles, and the following four C9 Generator states to accommodate them.

1. For 3-T-State cycles, (memory cycles, for example), $\overline{\text{WAIT}}$ is

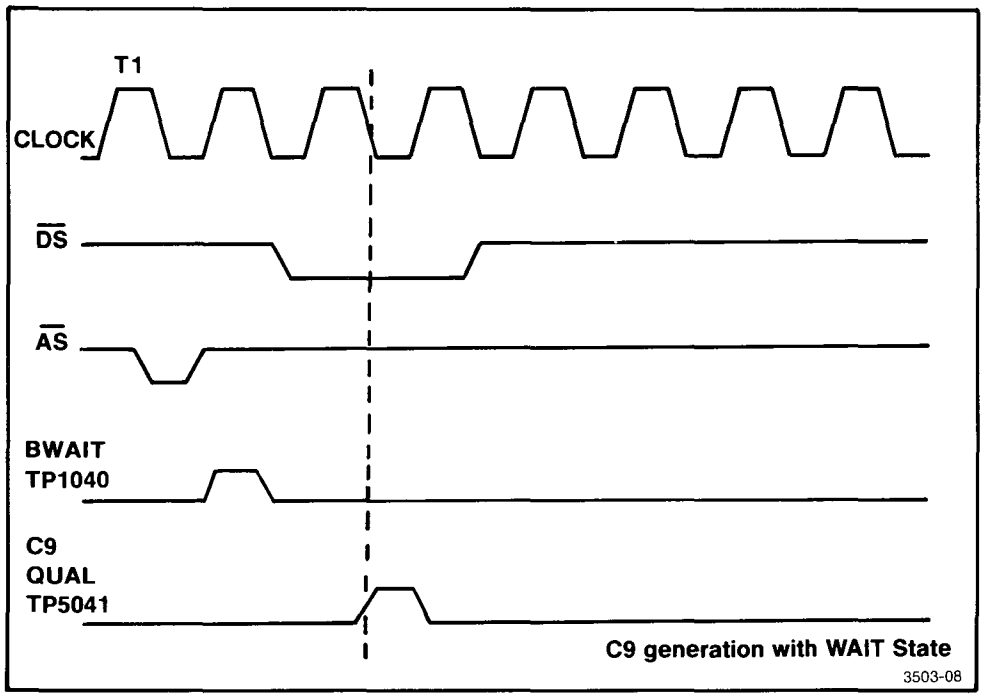
sampled on the T2 falling edge, and C9 is generated on T3.

2. For 4-T-State cycles, (I/O cycles, for example), $\overline{\text{WAIT}}$ is sampled on the T3 falling edge, and C9 is generated on T4.

3. For Interrupt Acknowledge cycles, $\overline{\text{WAIT}}$ is sampled on T5 and T7. C9 is generated on T8.

4. For 3-T-State cycles where $\overline{\text{WAIT}}$ is disabled, (Refresh and Internal Operation cycles), C9 is generated on T3.

See Figure 4-5.



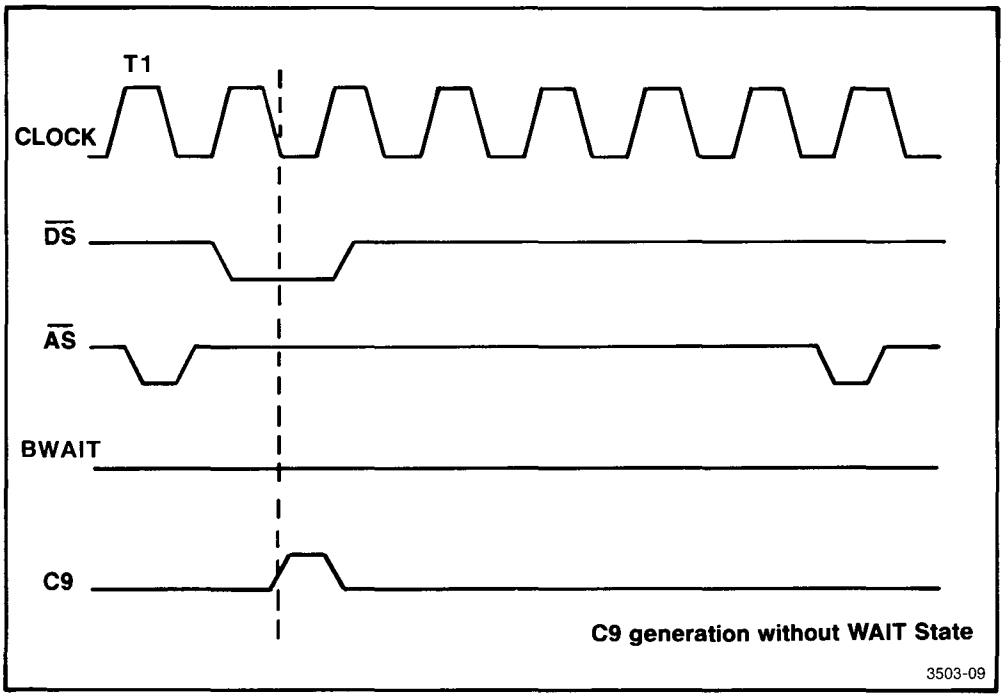


Figure 4-5. Timing relationships during QUAL state, with and without **WAIT** states.

Halt

Either the logic analyzer or the SUT can halt the microprocessor. A low signal on either the $\overline{\text{STOP SUT}}$ (from the logic analyzer), or the $\overline{\text{USTOP}}$ (from the SUT) will input the $\overline{\text{STOP}}$ signal to the Z8001 in the ZIF socket. Control line C7, $\overline{\text{SUT HALTED}}$, to the logic analyzer will also be reset back to low.

Z8001 Lines Ignored

Because of lack of control lines or redundancy of information, the following Z8001 signals are ignored: B/$\overline{\text{W}}$, $\overline{\text{MI}}$, $\overline{\text{BUSRQ}}$, and RESERVED. In addition, $\overline{\text{MREQ}}$ and $\overline{\text{DS}}$ are buffered by the personality module, but not used by the logic analyzer. The buffered $\overline{\text{DS}}$ line may be checked on A1TP3020.

Self Test Circuitry

Jumper A2P6010 enables the Self-Test circuitry when in the ON position.

A2Q8020 and the related components form a modified Colpitts oscillator at approximately 12.5 MHz. The signal is divided by 2 in A2U3010A to form CLOCK (available at A2TP7020) and $\overline{\text{CLOCK}}$. CLOCK goes to the Self-Test socket, and $\overline{\text{CLOCK}}$ goes to the Self-Test circuitry.

A2U4040 divides the $\overline{\text{CLOCK}}$ by 11 and A2U5010, A2U5020, A2U4030 and A2U5030 continue the clock division, by 16 for each, respectively.

While $\overline{\text{AS}}$ is being generated, these ICs stop the countdown chain for one clock cycle by the following procedure: A2U3010B pin 8 goes low, which disables the counters, causing A2U4040 to repeatedly output 0000, (for a divide by 11). A2U6010, A2U6020, and A2U6030 buffer the countdown chain to form address, data, and segment information. Status lines are formed from the inversion of the lower address nibble by A2U4020.

Jumpers A2P7010 and A2P6041 enable and disable address lines AD7 and AD9, respectively. When A2P7010 (shown on the board as B) and A2P6041 (shown on the board as A) are in the 1-2 position, Address 7 and Address 9 are zero. This is useful for diagnostics. The 2-3 position allows testing for stuck bits.

The Self-Test Circuitry resets itself at power up. When the RCO pin of A2U4040 and the Q output of A2U3010 go high, the high signals on SYNCA and SYNCB are NANDed together on $\overline{\text{SRESET}}$, which clears A2U4040.

CAUTION

The Self Test circuitry should not be enabled during normal operation. To do so may cause SUT failure and/or excessive power consumption.

Section 5

PERFORMANCE CHECK

The following procedures are designed to confirm that a PM 110 is operating within specified levels of performance.

EQUIPMENT

1. 7D02 Logic Analyzer mounted in 7000 Series Mainframe.

2. PM 110 Personality Module.

3. Tektronix PG502 Pulse Generator with 50 ohm terminator and female BNC to EZ-Ball adapter.

4. Tektronix PG508 50 MHz Pulse Generator with 50 ohm terminator and female BNC to EZ-Ball adapter.

5. Oscilloscope with dual channel, 200 MHz bandwidth (for example, the Tektronix 475).

6. 2 matched (delay must be equal, plus or minus 0.5 ns) 10X oscilloscope probes, 200 MHz bandwidth.

7. Connector pins for insertion into the ZIF socket.

8. Coaxial cable.

9. A 48-pin wire-wrap DIP socket (or two 24-pin sockets) to protect PM 110 ZIF socket.

TEST PROCEDURES

NOTE

To ensure correct test results, apply power to 7D02 and test equipment for a minimum of 20 minutes before proceeding with tests.

Test 1 -- Clock Period

(Specification calls for 165 ns min. clock period.)

1. Connect the PM 110 to the logic analyzer, with the microprocessor plug in the Self-Test socket, and the Self-Test circuitry enabled. (See ´How to Use Self-Test Circuitry´.)

2. Connect a DC505A Frequency Counter to TP7040, (shown on the board as 'C').

3. Connect the Ground to GND on the PM 110.

4. Set the counter to measure period TTL levels, averaged (AVGD) over 100 cycles with CLOCK RATE set to 10 ns.

5. Power up the 7D02 and hold down any 7D02 key to enter diagnostics mode.

6. Run the '9 -- PER. MOD SYSTEM' diagnostic test, while reading the period. The period should read less than or equal to 165 ns.

ABOUT SETUP AND HOLD TIME MEASUREMENT

1) The PG502 triggers the PG508. Connect a coaxial cable from the PG502 + TRIG OUT to the PG508 TRIGGER/GATE/IN.

2) the PG502 generates the clock signal and the PG508 generates the test signal.

3) It will be necessary to insert connector pins into the ZIF socket to conduct the tests. You may want to protect your ZIF socket by inserting a 48-pin wire-wrap DIP socket, and then inserting the pins into it.

4) Before the Setup and Hold Time test, the output of the PG502 and PG508 must be measured on the oscilloscope. To ensure that the pulse generator settings stay the same, keep the oscilloscope probes connected to the PG502 and PG508 adapters during the test.

5) Always ground the PG502 and PG508 adapters before the tests. Grounds points on the PM 110 are A1TP1010, A1TP3050,A1TP3051, and A1TP6020.

Test 2 -- Data Setup and Hold Time

(Specification calls for setup -- 32 ns min., hold -- 3 ns min.)

Background -- Data signals are stored in the logic analyzer on the trailing edge of the clock.

Procedure -- Using the oscilloscope, set the PG502 for 10 MHz square wave, variable period adjustment to 300 ns.

1. Set the PG508 for EXT TRIG, 6 ns Transition Time, .1 microsecond duration.

2. Connect the Channel 1 scope probe to the PG502 adapter.

3. Connect the Channel 2 scope probe to the PG508 adapter.

4. Obtain a display of both the PG502 and PG508 pulses on the oscilloscope screen. The displays should look like this:

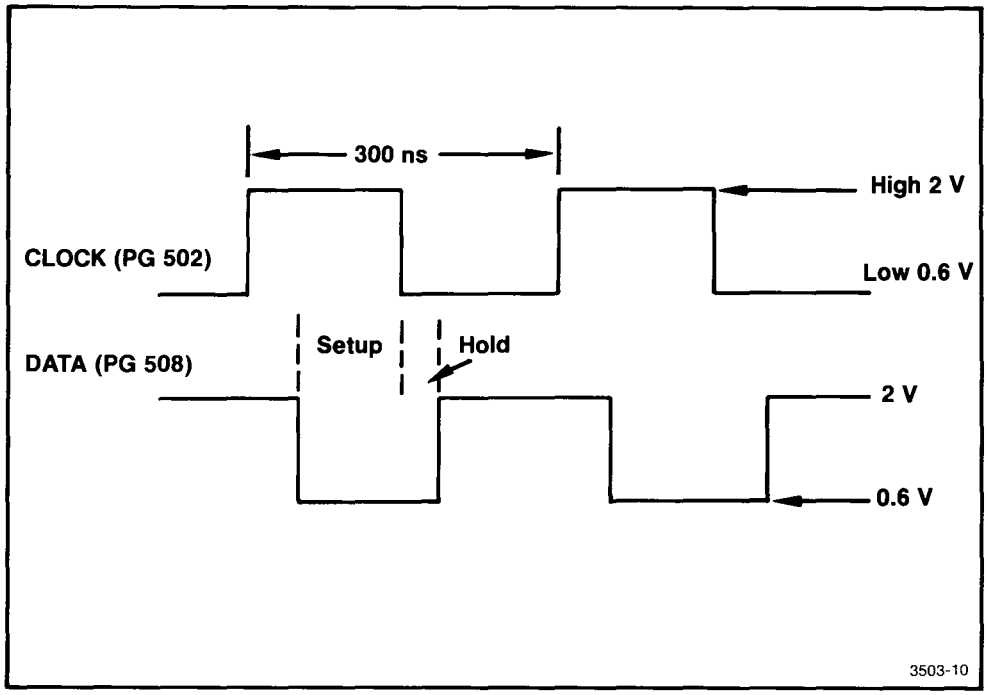


Figure 5-1. PG502 and PG508 waveforms for data line setup and hold performance check.

5. Connect PG502 adapter to pin 35 of the PM 110 ZIF socket. Ground the PG502 adapter at A1TP1010, A1TP3050, A1TP3051, or A1TP6020. See Figure 5-2 for ZIF socket pin diagram.

AD0	1	48	AD8
AD9	2	47	SN6
AD10	3	46	SN5
AD11	4	45	AD7
AD12	5	44	AD6
AD13	6	43	AD4
$\overline{\text{STOP}}$	7	42	SN4
$\overline{\text{u1}}$	8	41	AD5
AD15	9	40	AD3
AD14	10	39	AD2
Vcc	11	38	AD1
$\overline{\text{VI}}$	12	37	SN2
$\overline{\text{NVI}}$	13	36	GND
$\overline{\text{SEGT}}$	14	35	CLOCK
$\overline{\text{NMI}}$	15	34	$\overline{\text{AS}}$
$\overline{\text{RESET}}$	16	33	RESERVED
$\overline{\text{u0}}$	17	32	B/$\overline{\text{W}}$
$\overline{\text{MREQ}}$	18	31	N/$\overline{\text{S}}$
$\overline{\text{DS}}$	19	30	R/$\overline{\text{W}}$
ST3	20	29	$\overline{\text{BUSAK}}$
ST2	21	28	$\overline{\text{WAIT}}$
ST1	22	27	$\overline{\text{BUSRQ}}$
ST0	23	26	SN0
SN3	24	25	SN1

3503-12

Figure 5-2. PM 110 ZIF socket pin diagram.

6. Connect the PG508 adapter to pin 1 (AD0) of the PM 110 ZIF socket.

7. Connect the adapter grounds to pin 36 of PM 110 ZIF, or to test points A1TP1010, A1TP3050, A1TP3051, or A1TP6010.

8. Enter the following program on the 7D02:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXXXXXXXXXXXXX0
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

9. Press the 7D02 START key to run the program. The test passes if no data is acquired.

10. Invert the data pulse by complementing the PG508 and setting the data bit to 1. The 7D02 program should now look like this:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXXXXXXXXXXXXX1
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
```

```
1     0-SYSTEM UNDER TEST CONT.
1     1-USER CLOCK QUAL.
1     1-FALLING EDGE OF CLOCK
1     C9-C4 (ANDED CLOCKS)=XXXXXX
```

The oscilloscope display should now look like this:

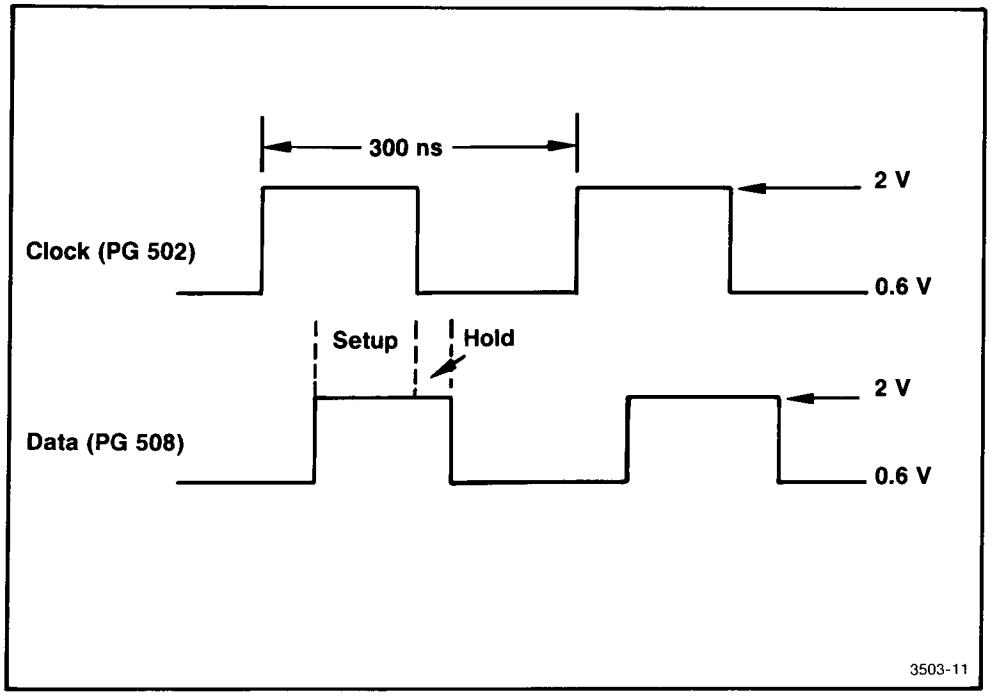


Figure 5-3. PG502 and PG508 waveforms for data line setup and hold performance check (data line inverted).

11. Repeat this test for each data bit, remembering to complement the PG508 each time a data bit changes from 0 to 1 and back.

Section 6

MAINTENANCE AND TROUBLESHOOTING

MAINTENANCE AND CLEANING

Repair

Tektronix, Inc., provides complete instrument service at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field office or representative for further information.

Obtaining Replacement Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts List, Section 7, and the Replaceable Mechanical Parts List, Section 9, for the proper value, rating, tolerance, and description.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include component and number from the Electrical Parts List.)

4. The Tektronix part number.

Cleaning Instructions

This instrument should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation, which can cause overheating and component breakdown.

Exterior -- Loose dust on the personality module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

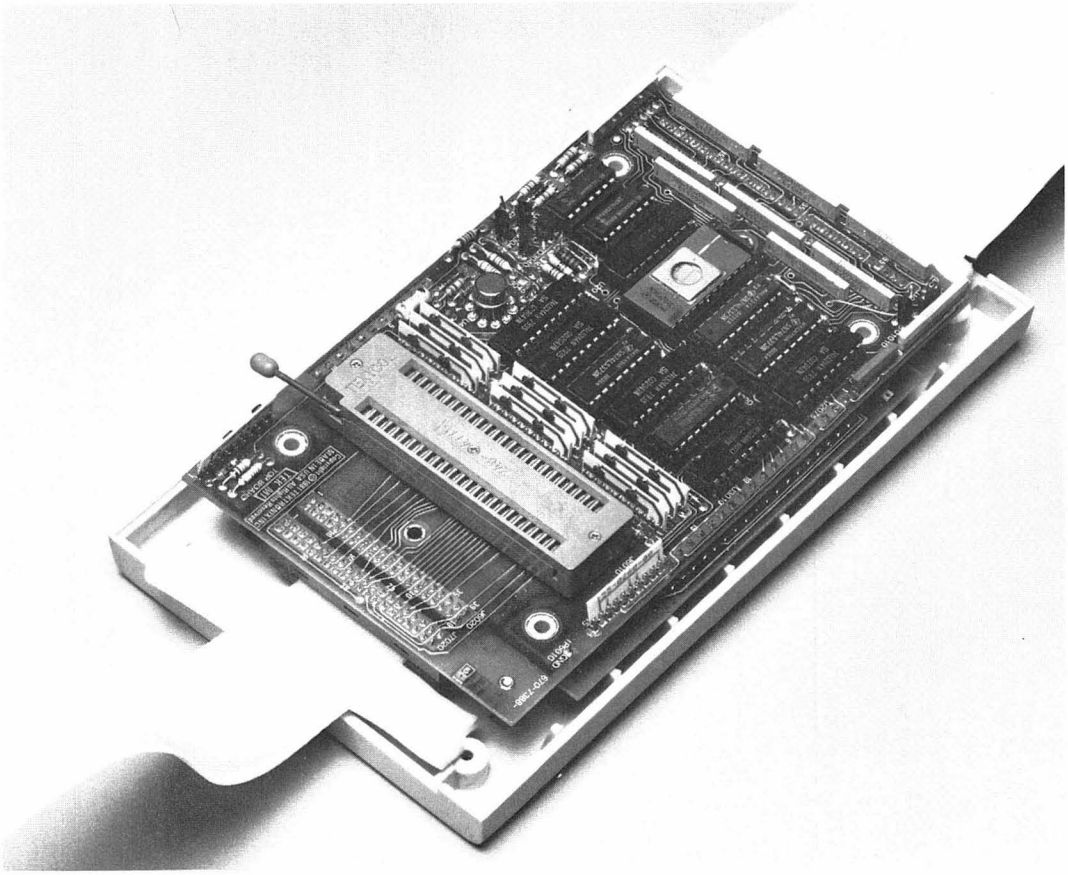
Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Don't get the microprocessor plug or logic analyzer plug wet. DO NOT use chemical cleaning agents. They may damage the plastics used in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone or similar solvents.

Interior -- Dust in the interior should be removed with a jet of dry, low pressure air and a soft brush.

After major repairs flush the board well with clean isopropyl alcohol. Make certain soldering resin and dirt are removed from the board.

How to Disassemble Personality Module Pod

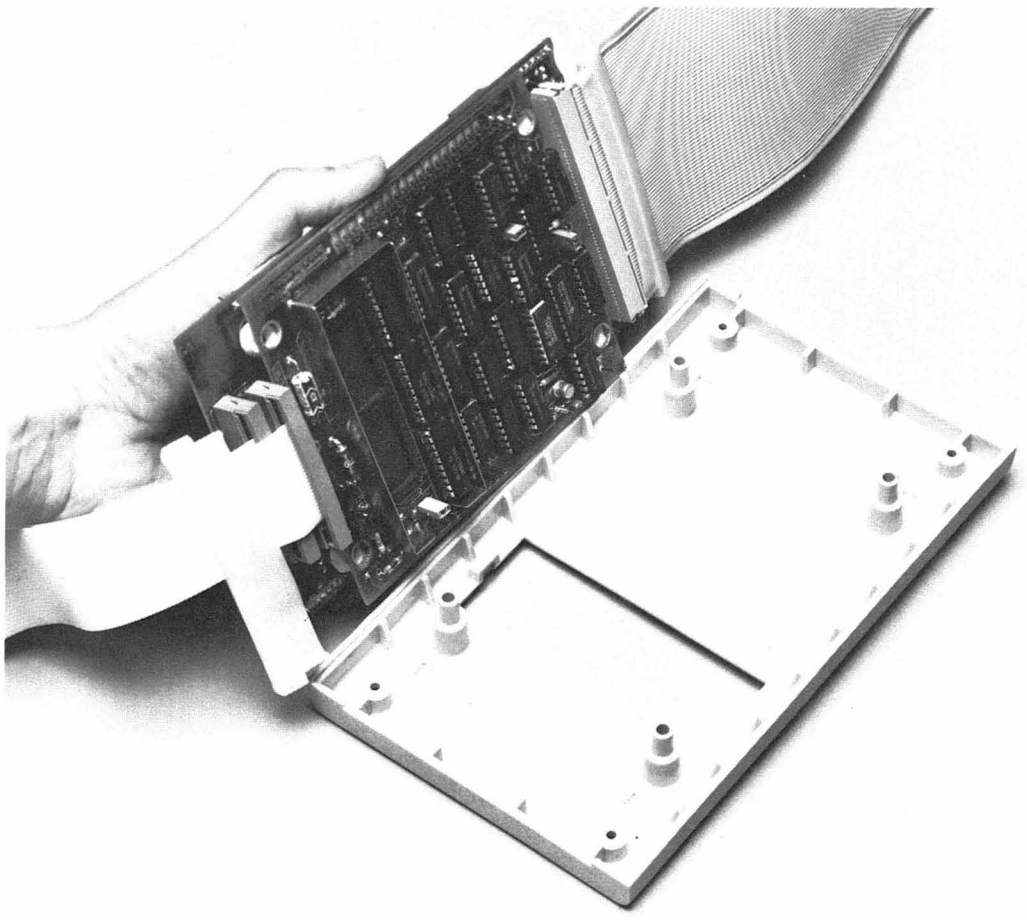
To remove the top cover, unscrew the four middle screws on the bottom of the Personality Module. Lift the top cover off. The top board, A1, is now accessible. See Figure 6-1.



3503-13

Figure 6-1. PM 110 with top cover removed, allowing access to top board, A1.

To reach components on the bottom board, A2, unscrew the four outer screws on the bottom of the Personality Module. Both boards, still connected to each other, may now be lifted out of the case. See Figure 6-2.



3503-14

Figure 6-2. PM 110 removed from case, boards A1 and A2 accessible.

The Personality Module may now be operated, with both boards available for signature analysis.

To reassemble the Personality Module, reverse the above procedure.

CAUTION

The Personality Module case protects the boards from moisture, dirt, and breakage. Keep the case on unless performing troubleshooting or repair.

How to Disassemble and Clean Microprocessor Plug

The microprocessor plug is an extremely sensitive device. It should be cleaned regularly, but only by qualified service personnel.

1. To disassemble, remove the two screws on the top of the plug housing, and open the housing.

2. Use magnification to inspect the top of the plug housing (wire side) for wire alignment and cleanliness.

3. Clean the top of the plug housing (wire side) by spraying with freon spray. Do not spray longer than 10 seconds.

4. To remove the hybrid, use a fiber alignment tool or your fingernails. Gently pry up along the long sides of the hybrid. Be careful not to bend any of the pins.

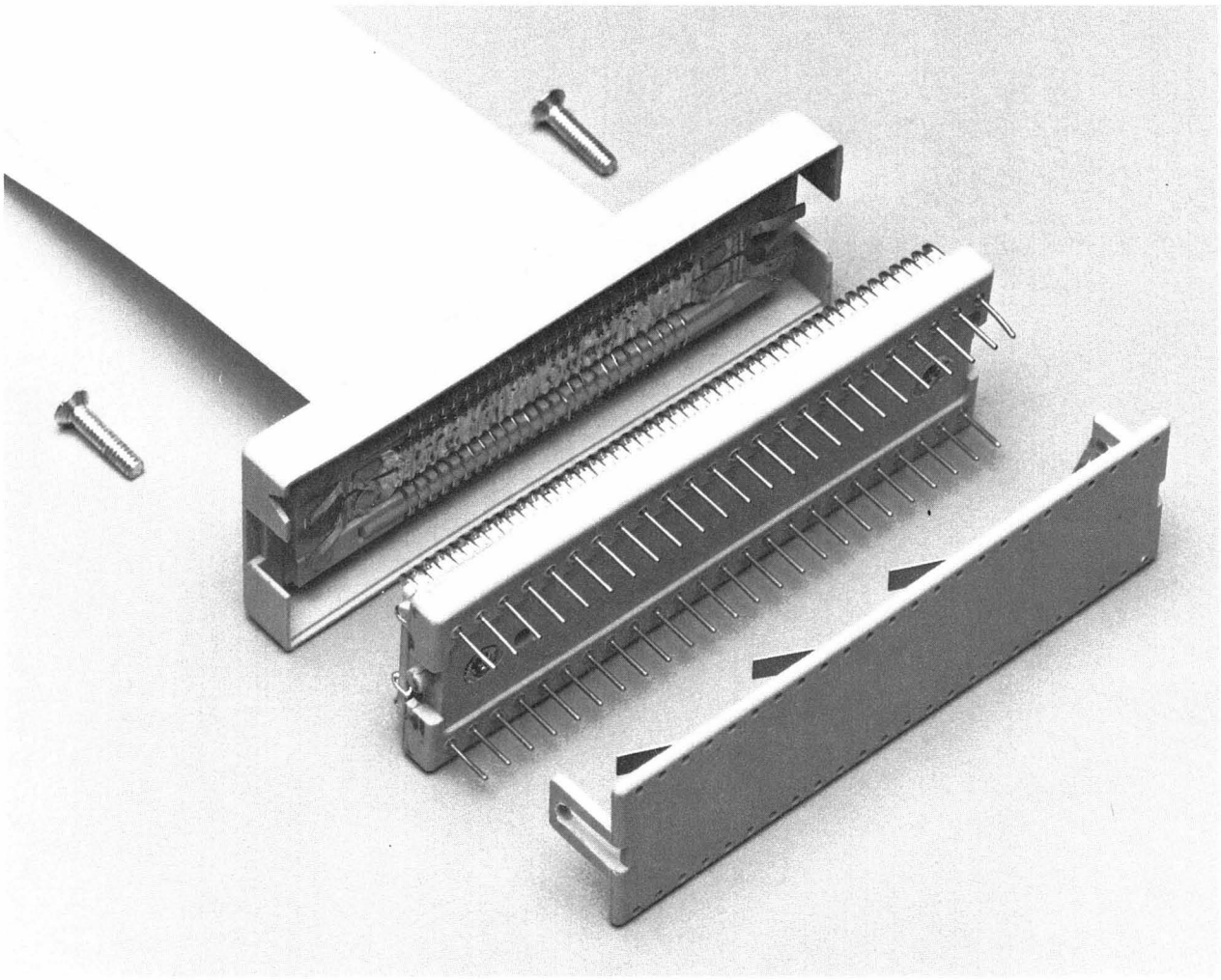
CAUTION

Do not use metal tools on the hybrid.

5. Clean the hybrid with freon spray. Do not spray longer than 10 seconds.

6. Insert the hybrid into the plug housing. Pin 1 of the hybrid is marked with a "1" on both sides of the hybrid. Pin 1 of the plug housing is marked with a notch. Gently press the hybrid into the plug housing.

7. Re-assemble the plug housing and insert the two screws. Do not over-tighten the screws.



3503-15

Figure 6-3. PM 110 microprocessor plug disassembly.

TROUBLESHOOTING

Where to Find:

Performance Check for Specs -- Section 5

Specs -- Section 3

Diagnostics and Troubleshooting Procedures -- Section 6

Circuit Descriptions -- Section 4

Schematics -- Section 8

Signature Analysis Tables -- Section 6

Signal Glossary -- Section 10

How to Use the Self-Test Circuitry

On the bottom side of the PM 110 Personality Module is a plastic door covering the self-test stimulus generator outputs. Some 7D02 diagnostics will run only if the self-test plug is inserted into the test socket. The 7D02 indicates when this is necessary with the message 'PLEASE CONNECT SELF TEST STIMULUS.'

Before starting this procedure, the mainframe power switch is turned off, and the PM 110 is plugged into the 7D02.

Connect the P6451 Timing Option plug to P6040, next to the self-test plug. Be sure to connect the white P6451 ground wire to an appropriate ground pin on the PM 110 (A1TP1010, A1TP3050, A1TP3051, or A1TP6020). The black P6451 zero wire goes on P6040 pin 1, marked with an arrow. P6451 wire 1 goes on P6040 pin 2, and so forth. The self test should only be used in a service situation. For better understanding of the self-test circuitry, see the Theory of Operation section.

1. If a microprocessor is in the Personality Module ZIF socket, remove it.

CAUTION

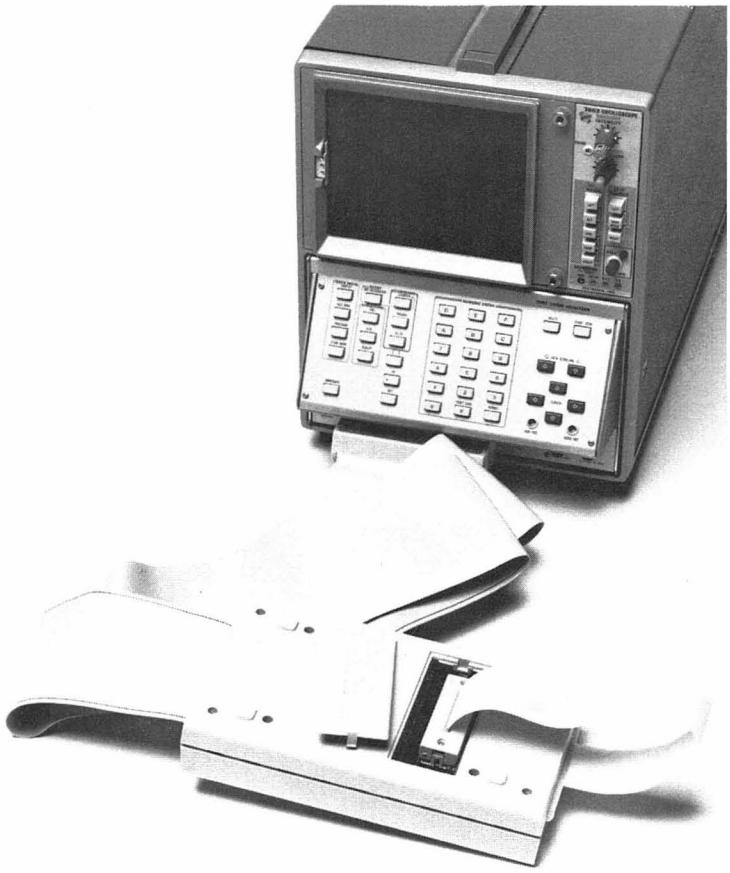
Never operate the self-test circuitry with a microprocessor in the PM 110 ZIF socket.

2. Open the plastic cover on the bottom of the Personality Module by inserting a small screw driver into the latch slot and gently prying up the cover. Put the cover in a safe place, and don't lose it.

@

3. Switch jumper A2P6010 to pins 1-2, the 'ON' position.

4. Insert the Personality Module microprocessor plug into the self-test socket A2J6021. Make sure the plug is inserted correctly, with pin 1 in the proper position. The cable should not be twisted. See Figure 6-4.



3503-16

Figure 6-4. PM 110 with microprocessor plug inserted in self-test socket.

NOTE

To prevent wear and tear on the self-test socket, insert a replaceable 48-pin socket into the self-test socket. (Two 24-pin sockets may be used instead of a 48-pin socket.)

5. Power up the logic analyzer and execute the desired diagnostic tests. See the Diagnostic Tests sub-section.

6. When testing is complete, turn off the mainframe power

switch.

7. Remove the microprocessor plug from the self-test socket.

8. Return jumper A2P6010 to pins 2-3, the 'OFF' position.

9. Replace the plastic cover.

CAUTION

The Self Test circuitry should be disabled and covered with the plastic cover when not in use. If the Self Test circuitry is enabled during normal personality module operation, it will consume excess power and may cause SUT failure.

DIAGNOSTIC TESTS

Acquisition Memory Contents Produced by Self-Test

While the PM 110 is set up for self-testing, you may check the self-test data acquired in acquisition memory. Enter the following PM 110 Word Recognizer and Trigger program:

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=0080
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1THEN DO
1TRIGGER 0-MAIN
1   0-BEFORE DATA
1   0-SYSTEM UNDER TEST CONT.
1   0-STANDARD CLOCK QUAL.
 END TEST 1
```

Press the START key to run the program. The acquisition memory should be filled with the following contents:

```
LOC  SEG  ADDR  DATA  STATUS    NI
000   7D  FD6D  FFED  SEG AK    N0
```

```
001    70  FD70  FDF0  MEM  R    N0
002    70  FD71  FDF1  MEM  R    N0
003    70  FD72  FDF2  MEM  R    N0
004    70  FD73  FDF3  MEM  R    N0
005    70  FD74  FDF4  FETCH1    N0
006    70  FD75  FDF5  FETCH1    N0
007    70  FD76  FDF6  MEM  R    N0
008    70  FD77  FDF7  MEM  R    N0
009    7E  FD78  FFF8  VI ACK    N0
010    7F  FD79  FFF9  NVI AK    N0
011    70  FD7A  FDFA  SI/O R    N0
012    70  FD7B  FDFB  SI/O R    N0
013    7C  FD7C  FFFC  NMI AK    N0
014    7D  FD7D  FFFD  SEG AK    N0
015T--00--0000--0080--MEM  W----S1
016    00  0001  0081  MEM  W    S1
017    00  0002  0082  MEM  W    S1
018    00  0003  0083  MEM  W    S1
019    00  0004  0084  FETCH1    S1
020    00  0005  0085  MEM  W    S1
021    00  0006  0086  MEM  W    S1
022    00  0007  0087  MEM  W    S1
023    7E  0008  0288  VI ACK    S1
024    7F  0009  0289  NVI AK    S0
025    00  000A  008A  SI/O W    N0
026    00  000B  008B  I/O  W    S0
027    7C  000C  028C  NMI AK    S0
028    7D  000D  028D  SEG AK    S0
029    00  0010  0090  MEM  R    S0
030    00  0011  0091  MEM  R    S0
031    00  0012  0092  MEM  R    S0
032    00  0013  0093  MEM  R    S0
033    00  0014  0094  FETCH1    S0
034    00  0015  0095  FETCHN    S0
035    00  0016  0096  MEM  R    S0
036    00  0017  0097  MEM  R    S0
037    7E  0018  0298  VI ACK    S0
038    7F  0019  0299  NVI AK    S0
039    00  001A  009A  SI/O R    N0
040    00  001B  009B  I/O  R    S0
041    7C  001C  029C  NMI AK    S0
042    7D  001D  029D  SEG AK    S0
043    10  0020  00A0  MEM  W    S0
044    10  0021  00A1  MEM  W    S0
045    10  0022  00A2  MEM  W    S0
046    10  0023  00A3  MEM  W    S0
047    10  0024  00A4  FETCH1    S0
048    10  0025  00A5  MEM  W    S0
049    10  0026  00A6  MEM  W    S0
050    10  0027  00A7  MEM  W    S0
051    7E  0028  02A8  VI ACK    S0
052    7F  0029  02A9  NVI AK    S0
053    10  002A  00AA  SI/O W    N0
```

054	10	002B	00AB	I/O W	S0
055	7C	002C	02AC	NMI AK	S0
056	7D	002D	02AD	SEG AK	S0
057	10	0030	00B0	MEM R	S0
058	10	0031	00B1	MEM R	S0
059	10	0032	00B2	MEM R	S0
060	10	0033	00B3	MEM R	S0
061	10	0034	00B4	FETCH1	S0
062	10	0035	00B5	FETCHN	S0
063	10	0036	00B6	MEM R	S0
064	10	0037	00B7	MEM R	S0
065	7E	0038	02B8	VI ACK	S0
066	7F	0039	02B9	NVI AK	S0
067	10	003A	00BA	SI/O R	N0
068	10	003B	00BB	I/O R	S0
069	7C	003C	02BC	NMI AK	S0
070	7D	003D	02BD	SEG AK	S0
071	00	0040	00C0	MEM W	N0
072	00	0041	00C1	MEM W	N0
073	00	0042	00C2	MEM W	N0
074	00	0043	00C3	MEM W	N0
075	00	0044	00C4	FETCH1	N0
076	00	0045	00C5	MEM W	N0
077	00	0046	00C6	MEM W	N0
078	00	0047	00C7	MEM W	N0
079	7E	0048	02C8	VI ACK	N0
080	7F	0049	02C9	NVI AK	N0
081	00	004A	00CA	SI/O W	N0
082	00	004B	00CB	SI/O W	N0
083	7C	004C	02CC	NMI AK	N0
084	7D	004D	02CD	SEG AK	N0
085	00	0050	00D0	MEM R	N0
086	00	0051	00D1	MEM R	N0
087	00	0052	00D2	MEM R	N0
088	00	0053	00D3	MEM R	N0
089	00	0054	00D4	FETCH1	N0
090	00	0055	00D5	FETCHN	N0
091	00	0056	00D6	MEM R	N0
092	00	0057	00D7	MEM R	N0
093	7E	0058	02D8	VI ACK	N0
094	7F	0059	02D9	NVI AK	N0
095	00	005A	00DA	SI/O R	N0
096	00	005B	00DB	SI/O R	N0
097	7C	005C	02DC	NMI AK	N0
098	7D	005D	02DD	SEG AK	N0
099	10	0060	00E0	MEM W	N0
100	10	0061	00E1	MEM W	N0
101	10	0062	00E2	MEM W	N0
102	10	0063	00E3	MEM W	N0
103	10	0064	00E4	FETCH1	N0
104	10	0065	00E5	MEM W	N0
105	10	0066	00E6	MEM W	N0
106	10	0067	00E7	MEM W	N0

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107	7E	0068	02E8	VI ACK	N0
108	7F	0069	02E9	NVI AK	N0
109	10	006A	00EA	SI/O W	N0
110	10	006B	00EB	SI/O W	N0
111	7C	006C	02EC	NMI AK	N0
112	7D	006D	02ED	SEG AK	N0
113	10	0070	00F0	MEM R	N0
114	10	0071	00F1	MEM R	N0
115	10	0072	00F2	MEM R	N0
116	10	0073	00F3	MEM R	N0
117	10	0074	00F4	FETCH1	N0
118	10	0075	00F5	FETCHN	N0
119	10	0076	00F6	MEM R	N0
120	10	0077	00F7	MEM R	N0
121	7E	0078	02F8	VI ACK	N0
122	7F	0079	02F9	NVI AK	N0
123	10	007A	00FA	SI/O R	N0
124	10	007B	00FB	SI/O R	N0
125	7C	007C	02FC	NMI AK	N0
126	7D	007D	02FD	SEG AK	N0
127	20	0000	0080	MEM W	S0
128	20	0001	0081	MEM W	S0
129	20	0002	0082	MEM W	S0
130	20	0003	0083	MEM W	S0
131	20	0004	0084	FETCH1	S0
132	20	0005	0085	MEM W	S0
133	20	0006	0086	MEM W	S0
134	20	0007	0087	MEM W	S0
135	7E	0008	0288	VI ACK	S0
136	7F	0009	0289	NVI AK	S0
137	20	000A	008A	SI/O W	N0
138	20	000B	008B	I/O W	S0
139	7C	000C	028C	NMI AK	S0
140	7D	000D	028D	SEG AK	S0
141	20	0010	0090	MEM R	S0
142	20	0011	0091	MEM R	S0
143	20	0012	0092	MEM R	S0
144	20	0013	0093	MEM R	S0
145	20	0014	0094	FETCH1	S0
146	20	0015	0095	FETCHN	S0
147	20	0016	0096	MEM R	S0
148	20	0017	0097	MEM R	S0
149	7E	0018	0298	VI ACK	S0
150	7F	0019	0299	NVI AK	S0
151	20	001A	009A	SI/O R	N0
152	20	001B	009B	I/O R	S0
153	7C	001C	029C	NMI AK	S0
154	7D	001D	029D	SEG AK	S0
155	30	0020	00A0	MEM W	S0
156	30	0021	00A1	MEM W	S0
157	30	0022	00A2	MEM W	S0
158	30	0023	00A3	MEM W	S0
159	30	0024	00A4	FETCH1	S0

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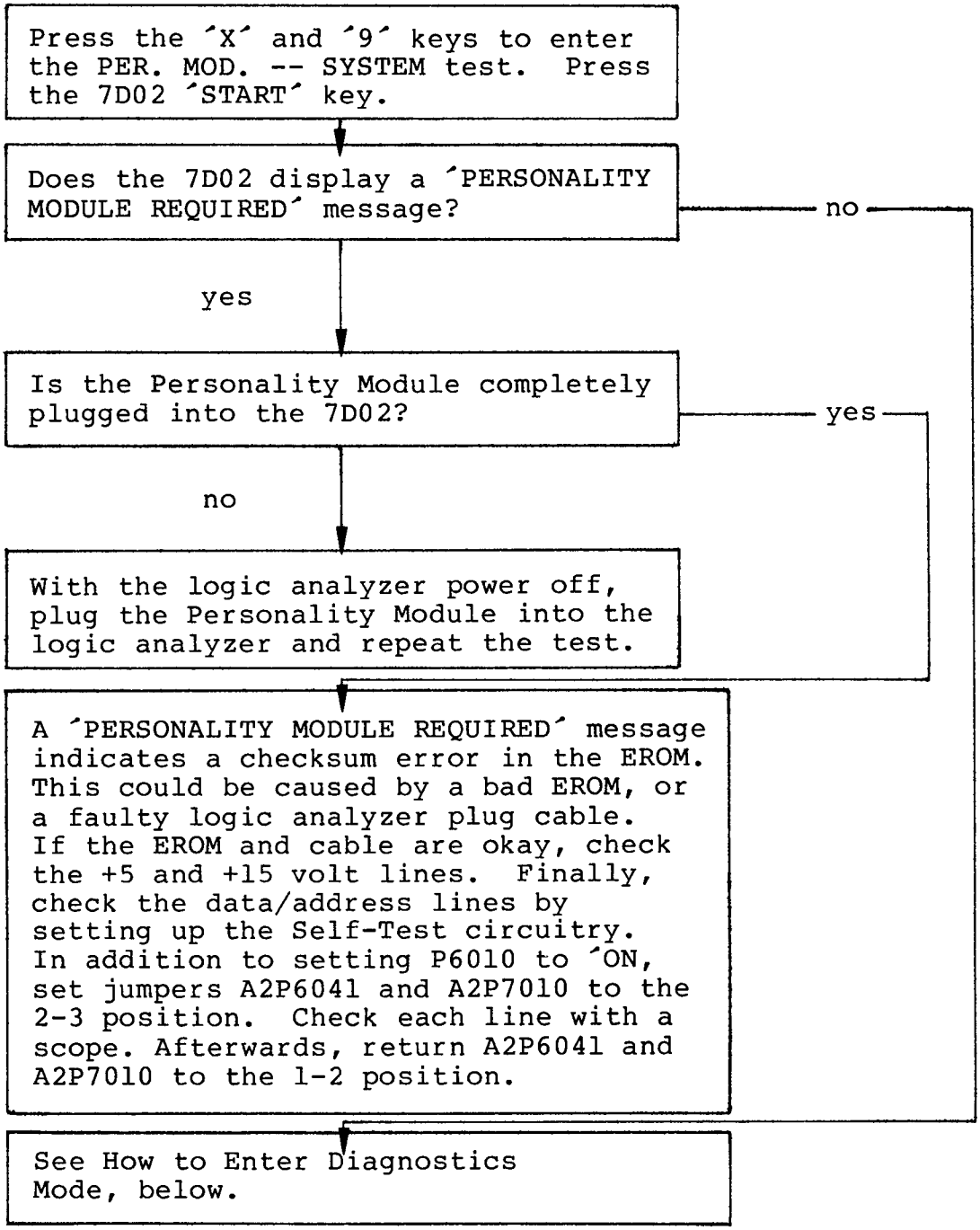
160	30	0025	00A5	MEM W	S0
161	30	0026	00A6	MEM W	S0
162	30	0027	00A7	MEM W	S0
163	7E	0028	02A8	VI ACK	S0
164	7F	0029	02A9	NVI AK	S0
165	30	002A	00AA	SI/O W	N0
166	30	002B	00AB	I/O W	S0
167	7C	002C	02AC	NMI AK	S0
168	7D	002D	02AD	SEG AK	S0
169	30	0030	00B0	MEM R	S0
170	30	0031	00B1	MEM R	S0
171	30	0032	00B2	MEM R	S0
172	30	0033	00B3	MEM R	S0
173	30	0034	00B4	FETCH1	S0
174	30	0035	00B5	FETCHN	S0
175	30	0036	00B6	MEM R	S0
176	30	0037	00B7	MEM R	S0
177	7E	0038	02B8	VI ACK	S0
178	7F	0039	02B9	NVI AK	S0
179	30	003A	00BA	SI/O R	N0
180	30	003B	00BB	I/O R	S0
181	7C	003C	02BC	NMI AK	S0
182	7D	003D	02BD	SEG AK	S0
183	20	0040	00C0	MEM W	N0
184	20	0041	00C1	MEM W	N0
185	20	0042	00C2	MEM W	N0
186	20	0043	00C3	MEM W	N0
187	20	0044	00C4	FETCH1	N0
188	20	0045	00C5	MEM W	N0
189	20	0046	00C6	MEM W	N0
190	20	0047	00C7	MEM W	N0
191	7E	0048	02C8	VI ACK	N0
192	7F	0049	02C9	NVI AK	N0
193	20	004A	00CA	SI/O W	N0
194	20	004B	00CB	SI/O W	N0
195	7C	004C	02CC	NMI AK	N0
196	7D	004D	02CD	SEG AK	N0
197	20	0050	00D0	MEM R	N0
198	20	0051	00D1	MEM R	N0
199	20	0052	00D2	MEM R	N0
200	20	0053	00D3	MEM R	N0
201	20	0054	00D4	FETCH1	N0
202	20	0055	00D5	FETCHN	N0
203	20	0056	00D6	MEM R	N0
204	20	0057	00D7	MEM R	N0
205	7E	0058	02D8	VI ACK	N0
206	7F	0059	02D9	NVI AK	N0
207	20	005A	00DA	SI/O R	N0
208	20	005B	00DB	SI/O R	N0
209	7C	005C	02DC	NMI AK	N0
210	7D	005D	02DD	SEG AK	N0
211	30	0060	00E0	MEM W	N0
212	30	0061	00E1	MEM W	N0

213	30	0062	00E2	MEM W	N0
214	30	0063	00E3	MEM W	N0
215	30	0064	00E4	FETCH1	N0
216	30	0065	00E5	MEM W	N0
217	30	0066	00E6	MEM W	N0
218	30	0067	00E7	MEM W	N0
219	7E	0068	02E8	VI ACK	N0
220	7F	0069	02E9	NVI AK	N0
221	30	006A	00EA	SI/O W	N0
222	30	006B	00EB	SI/O W	N0
223	7C	006C	02EC	NMI AK	N0
224	7D	006D	02ED	SEG AK	N0
225	30	0070	00F0	MEM R	N0
226	30	0071	00F1	MEM R	N0
227	30	0072	00F2	MEM R	N0
228	30	0073	00F3	MEM R	N0
229	30	0074	00F4	FETCH1	N0
230	30	0075	00F5	FETCHN	N0
231	30	0076	00F6	MEM R	N0
232	30	0077	00F7	MEM R	N0
233	7E	0078	02F8	VI ACK	N0
234	7F	0079	02F9	NVI AK	N0
235	30	007A	00FA	SI/O R	N0
236	30	007B	00FB	SI/O R	N0
237	7C	007C	02FC	NMI AK	N0
238	7D	007D	02FD	SEG AK	N0
239	40	0100	0180	MEM W	S0
240	40	0101	0181	MEM W	S0
241	40	0102	0182	MEM W	S0
242	40	0103	0183	MEM W	S0
243	40	0104	0184	FETCH1	S0
244	40	0105	0185	MEM W	S0
245	40	0106	0186	MEM W	S0
246	40	0107	0187	MEM W	S0
247	7E	0108	0388	VI ACK	S0
248	7F	0109	0389	NVI AK	S0
249	40	010A	018A	SI/O W	N0
250	40	010B	018B	I/O W	S0
251	7C	010C	038C	NMI AK	S0
252	7D	010D	038D	SEG AK	S0
253	40	0110	0190	MEM R	S0
254	40	0111	0191	MEM R	S0
255	40	0112	0192	MEM R	S0

Personality Module Diagnostic Failure During Power-up

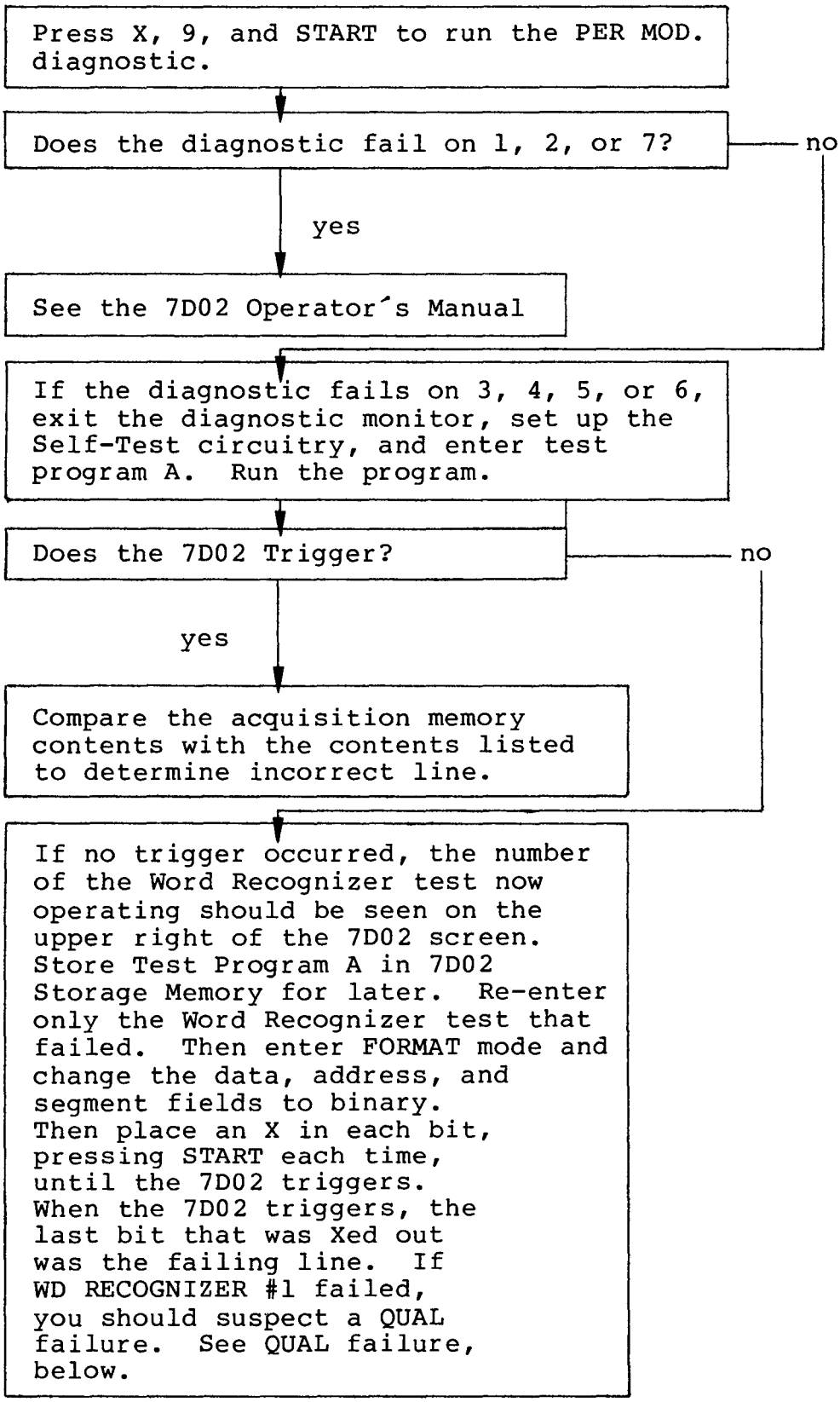
If a FAIL message appears on the PER. MOD. -- SYSTEM test during 7D02 power-up diagnostics, you should go through the following troubleshooting steps, in this order, to locate the problem.



How to Enter Diagnostic Mode

If there was no failure at power-up, but you still want to enter diagnostic mode, turn off the 7D02 power switch, and turn it back on while pressing any key on the 7D02 keypad for at least 5 seconds. This will cause the Keyboard diagnostic to fail. All diagnostics will then be available for selection.

The only diagnostic discussed here is number 9 -- PER MOD. -- SYSTEM.



Test Program A

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=0084
1 SEGMENT=00
1 ADDRESS=0004
1 000=MEM W 001=MEM R   STATUS=1
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 1
1 N/S=0 IRQ=1
1 R/W=0 uOUT,EPU=0 EXT TRIG=X
1 TIMING WR=X
1THEN DO
1---------
1 COUNTER # 1 0-EVENTS
1    1-RESET
1 COUNTER # 2 0-EVENTS
1    1-RESET
1 GOTO 2
1---------
 END TEST 1
 TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=55D5
2 SEGMENT=40
2 ADDRESS=5555
2 000=MEM W 001=MEM R   STATUS=1
2 010=I/O W 011=I/O R 100=RFSH 1
2 101=FCH 1 110=ACK  111=FCH N 1
2 N/S=1 IRQ=0
2 R/W=1 uOUT,EPU=0 EXT TRIG=X
2 TIMING WR=X
2THEN DO
2 GOTO 3
2ELSE DO
2 COUNTER # 1 0 -EVENTS
2    0-INCREMENT
 END TEST 2
 TEST 3
3IF
3 WORD RECOGNIZER # 3
3 DATA=A8AA
3 SEGMENT=10
3 ADDRESS=A82A
3 000=MEM W 001=MEM R   STATUS=0
3 010=I/O W 011=I/O R 100=RFSH 1
3 101=FCH 1 110=ACK  111=FCH N 0
3 N/S=1 IRQ=0
3 R/W=0 uOUT,EPU=0 EXT TRIG=X
```

```
3 TIMING WR=X
3THEN DO
3 GOTO 4
3ELSE DO
3 COUNTER # 2 0-EVENTS
3    0-INCREMENT
 END TEST 3
 TEST 4
4IF
4 WORD RECOGNIZER # 4
4 DATA=FFFD
4 SEGMENT=7D
4 ADDRESS=FD7D
4 000=MEM W 001=MEM R   STATUS=1
4 010=I/O W 011=I/O R 100=RFSH 1
4 101=FCH 1 110=ACK  111=FCH N 0
4 N/S=1 IRQ=0
4 R/W=1 uOUT,EPU=0 EXT TRIG=X
4 TIMING WR=X
4THEN DO
4 TRIGGER 0-MAIN
4    0-BEFORE DATA
4    0-SYSTEM UNDER TEST CONT.
4    0-STANDARD CLOCK QUAL.
 END TEST 4
```

Acquisition Memory Contents After Test Program A

LOC	SEG	ADDR	DATA	STATUS	NI
015T	7D	FD7D	FFFD	SEG AK	N0
016	60	FD00	FD80	MEM W	S0
017	60	FD01	FD81	MEM W	S0
018	60	FD02	FD82	MEM W	S0
019	60	FD03	FD83	MEM W	S0
020	60	FD04	FD84	FETCH1	S0
021	60	FD05	FD85	MEM W	S0
022	60	FD06	FD86	MEM W	S0
023	60	FD07	FD87	MEM W	S0
024	7E	FD08	FF88	VI ACK	S0
025	7F	FD09	FF89	NVI AK	S0
026	60	FD0A	FD8A	SI/O W	N0
027	60	FD0B	FD8B	I/O W	S0
028	7C	FD0C	FF8C	NMI AK	S0
029	7D	FD0D	FF8D	SEG AK	S0
030	60	FD10	FD90	MEM R	S0
031	60	FD11	FD91	MEM R	S0
032	60	FD12	FD92	MEM R	S0
033	60	FD13	FD93	MEM R	S0

QUAL Failure

A QUAL failure should be suspected if erroneous data is stored, or if there is a failure to trigger.

Troubleshoot as follows:

1. Set up the PM 110 Self-Test circuitry, and enter Test Program A.

2. Temporarily ground A2TP1020, $\overline{\text{PON}}$.

3. Start the program. If the program triggers correctly, Check A2U1030 and A2Q2010 for correct signatures. (See Signature Analysis, later in this section.

4. Check signatures of A2U1035 to isolate erroneous input (or QUAL output), and successively through A2U1025, A2U1030, A2U1010, A2U1020, A2U2021, A2U1040, A2U3030, or A2U3040, as required.

5. Remove the ground from $\overline{\text{PON}}$ after locating the problem.

How to Use 7D02 Diagnostic Module B -- TIMING OPTION

Make sure the P6451 plug is properly grounded. Check signature on A2P6040.

SLOW CLOCK or NO CLOCK Failure

If a SLOW CLOCK or NO CLOCK message appears during the running of a program, stop the program. Change the clock to user-defined, and enter all Xs in C9-C4.

Press START. If the SLOW CLOCK or NO CLOCK message persists, suspect a problem in the SUT clock.

If the program triggers, check C9, C7, and C6, and their related components.

Interrupt Line Troubleshooting Procedures

The power-up diagnostics do not automatically check the interrupt lines. To check these lines, follow this procedure:

1. Connect the PM 110 to a 7D02 logic analyzer and install a 48-pin wire-wrap socket (or two 24-pin sockets) to the PM 110 microprocessor plug.

2. Connect a PG502 or PG508 to wire-wrap pin 35, with ground connected to pin 36. Set the pulse generator for 5 volts, 0 to +5 signal -- 6 MHz square wave.

3. Power up the 7D02.

4. Enter the following 7D02 program (with a 1 in IRQ):

```
1IF
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=1
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
```

5. Press the 7D02 START key. Program should continue to run and not acquire data.

6. Ground the following wire-wrap pins, one at a time: 12, 13, 14, 15, and re-start the program each time.

7. The 7D02, searching for activity on the IRQ line, should trigger each time one of these pins are grounded.

SETUP AND HOLD TIME TROUBLESHOOTING TESTS

The following setup and hold tests should be used for troubleshooting the PM 110 components. The equipment used is the same as in the Setup and Hold Time tests in the Performance Check section. Please re-read the equipment list, and the sub-section titled: 'About Setup and Hold Time Measurement'.

Address Line Setup and Hold --

(Specification calls for 15 ns min. setup, 23 ns min. hold)

Address lines are first stored on the PM 110 on the rising edge of the Address Strobe, $\overline{AS}$, by transparent latches.

Using the same basic procedure as the Data Line Setup and Hold Test in the Performance Check section, connect the PG502 to both $\overline{AS}$ on ZIF pin 34 AND Clock on ZIF pin 35.

Connect the PG508 to AD0 on ZIF pin 1.

Enter the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXXXXXXXXXXXXX0
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

With the oscilloscope, check the pulses from the PG502 and PG508 into the PM 110 ZIF. They should resemble this display:

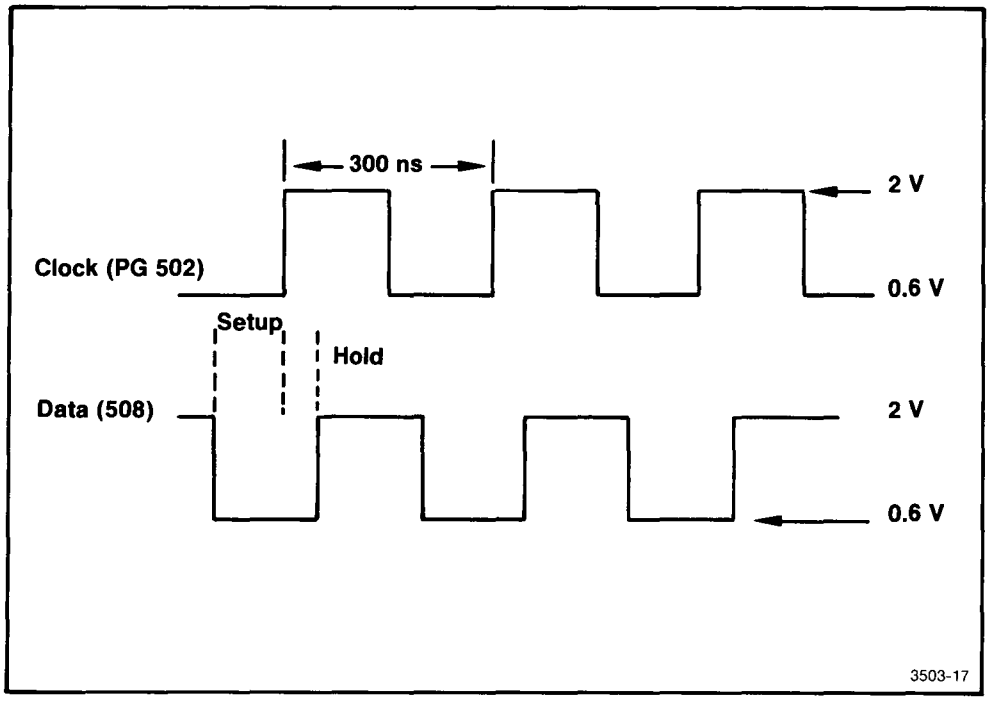


Figure 6-5. Address line setup and hold time clock and data pulses.

Complement the PG508 to invert the pulse, and change AD0 to 1 in the 7D02 display. The pulses should now resemble this display:

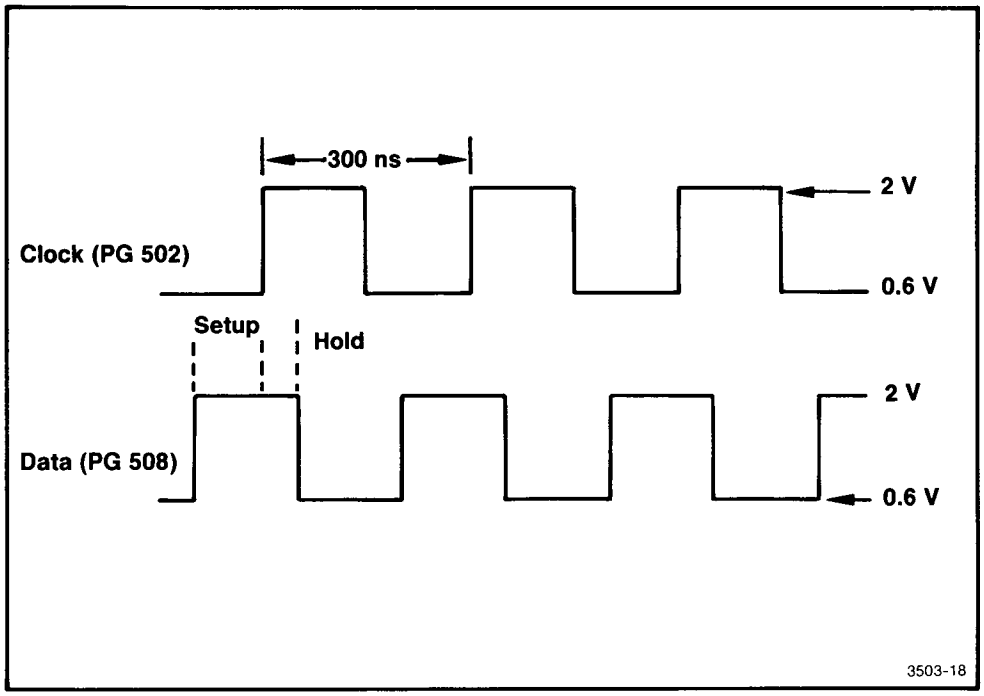


Figure 6-6. Address line setup and hold time clock and data pulses with data pulse inverted.

Repeat for each Address pin in the PM 110 ZIF socket. Remember to complement the PG508 every time you change an address bit.

If data is acquired, the test has failed, and you should suspect trouble in A1U2020 or A1U3030, if the the trouble is confined to the upper, or lower 8 bits, respectively. There could also be a problem with A1U3015 or A1U4015.

Segment Line Setup and Hold --

(Specification calls for 25 ns Setup min., and 25 ns Hold min.)

Segment number lines SN0 to SN7 are latched on the PM 110 by $\overline{AS}$ just like the address lines. However, the segment latch can be tristated depending on the state of the control lines.

Procedure is the same as the Address Line Setup and Hold, except ST2, ZIF pin 21, should be grounded. Apply the PG508 pulse shown in Figure 6-5 to ZIF pin 26, SN0.

Enter the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XXXXXXX0
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

Run the 7D02 program. Test passes if no data is acquired. Invert the PG508 pulse, as shown in Figure 6-6, and change the 7D02 program to

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
a SEGMENT=XXXXXXX1
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

Repeat the test for ZIF pins SN1-SN6.

If this test fails, check A1U2015, A1U2010, A1U3010, A1U2040,

A1U2045, A1U3039, A1U3015, and the input protection components.

N/$\overline{S}$ Setup and Hold --

(Specification calls for 86 ns min. Setup and 0 ns min. Hold.)

The N/$\overline{S}$ line is multiplexed with the I/O type flag depending on the NSIO line from Board 2.

a. Connect PG502 to ZIF pin 35.

b. Connect PG508 to ZIF pin 31.

c. Obtain a display like Figure 6-7.

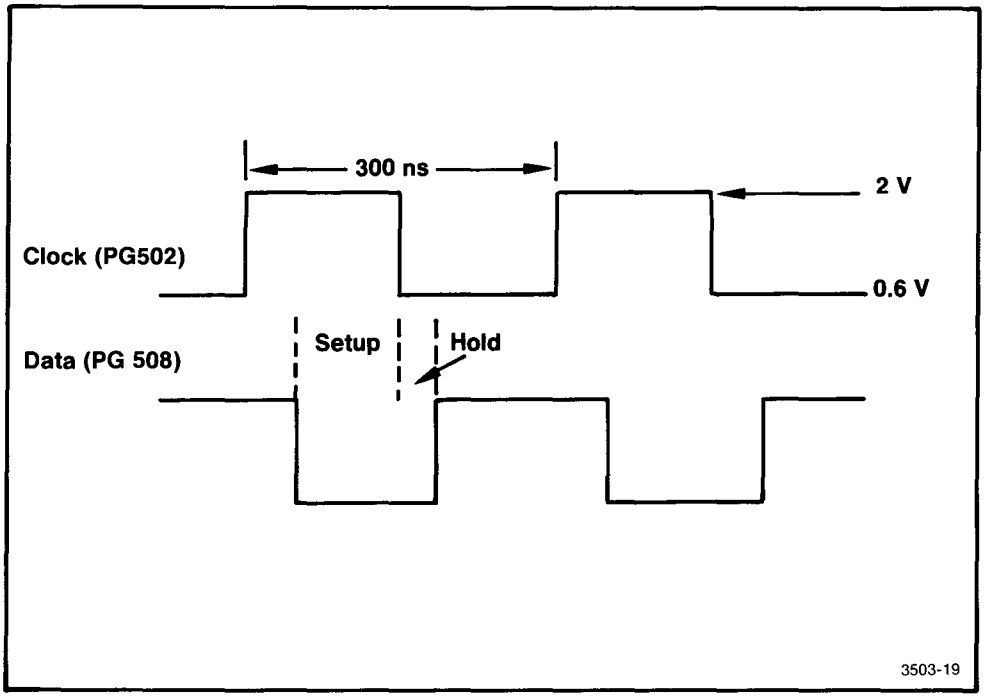


Figure 6-7. N/$\overline{S}$ setup and hold time clock and data pulses.

d. Connect grounds to ZIF pin 36, or test points TP1010, TP3050, TP3051, or TP6020.

e. Enter the following program on the 7D02:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=0 IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

The test passes if no data is acquired. Complement the PG508 to invert the pulse (see Figure 6-8) and repeat the test with $N/\overline{S}=1$.

If the test fails, check A1U3015, A1U2045, and A1U2040.

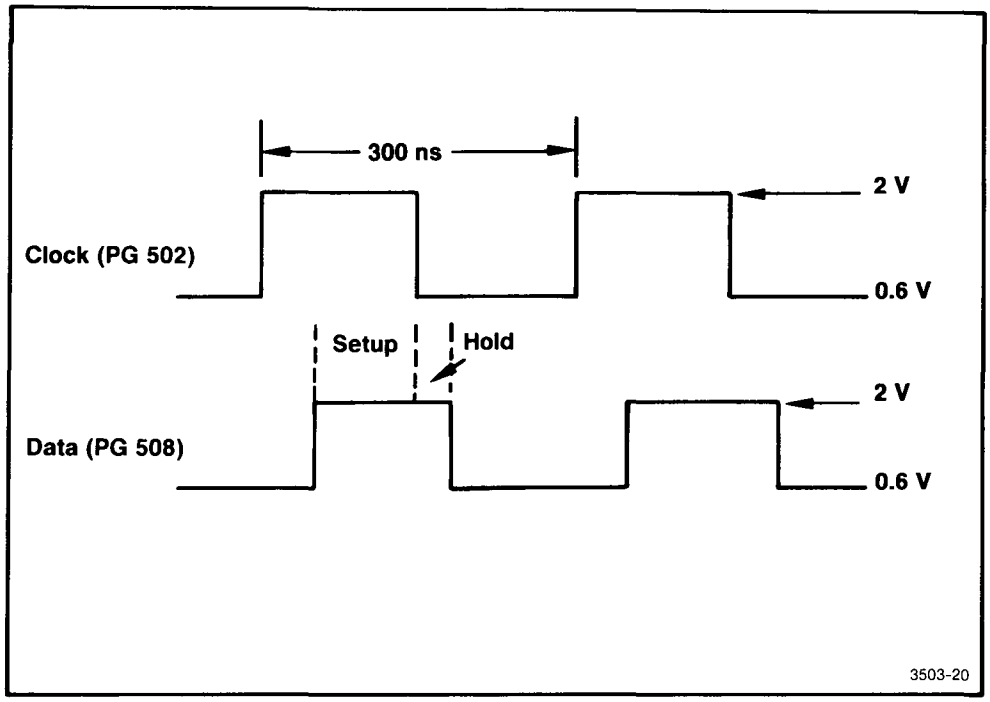


Figure 6-8. N/$\overline{S}$ line setup and hold time with PG508 data pulse inverted.

$\overline{AS}$ Line Setup and Pulse Width --

(Spec calls for 78 ns Setup and 42 ns Pulse Width)

The $\overline{AS}$ signal in its active low state marks the beginning of a CPU cycle. The PM 110 is level sensitive to this line. $\overline{AS}$

turns on the Control Line Encoder PROM on Board 2. Data on this PROM is latched on the leading edge of T2. A setup time is required for the $\overline{AS}$ relative to this leading edge.

a. Set the PG502 and PG508 to output pulses appearing on the oscilloscope screen line the ones in Figure 6-9.

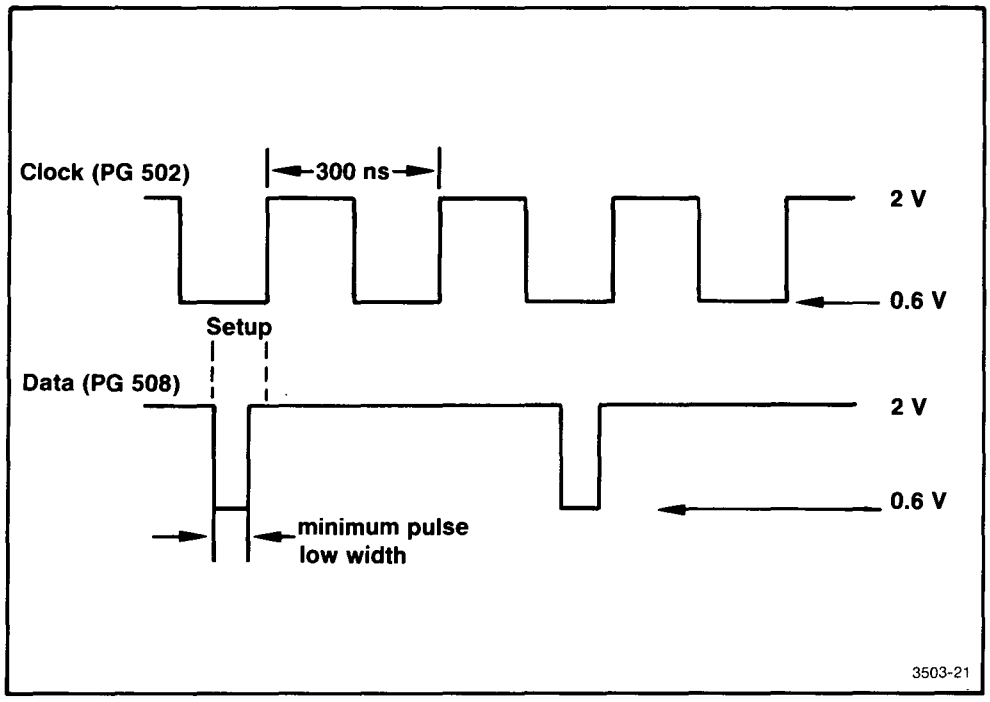


Figure 6-9. $\overline{AS}$ setup and hold time clock and data pulses.

Note that there must be a minimum of 2 PG502 (clock) pulses between every PG508 (data) pulse.

b. Connect ST1, 2, and 3 (ZIF pins 20, 21, 22) to ground.

c. Connect the PG508 to $\overline{AS}$ (ZIF pin 34).

d. Connect the PG502 to CLOCK (ZIF pin 35).

e. Enter the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
```

```
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=1
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 0
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

If no data is acquired by the 7D02, the test passes.

If the test fails, check A1U3015 and A1U4015.

$\overline{MO}$ and $\overline{BUSACK}$ Setup and Hold

(Spec calls for 85 ns min. Setup, 0 ns min. Hold)

The $\overline{MO}$ and $\overline{BUSACK}$ lines are ANDED with data from the Control Line Encoder PROM on Board 2 to generate C4 and C6. For this to occur, data in the PROM latch must be high to enable these two signals to pass through. The 7D02 samples C4 and C6 on trailing edge of the clock.

a. Connect ST0-ST3 (ZIF pins 20-23) to +5. (Use pin 11 of the enabled Self Test socket for +5.)

b. Connect $\overline{AS}$ (ZIF pin 34) to ground (ZIF pin 36, or TP1010, TP3050, TP3051, or TP6020).

c. Use the same PG502 and PG508 settings as for the $\overline{AS}$ Setup and Hold. See Figure 6-9.

d. Connect the PG502 probe to CLOCK (ZIF pin 35).

e. Connect the PG508 probe to $\overline{MO}$ (ZIF pin 17).

f. Enter the following 7D02 program.

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
```

```
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXX1
```

g. Press the 7D02 START key to run the test. The Test passes if no data is acquired and a SLOW CLOCK message is displayed.

h. Repeat the test with the PG508 pulse inverted, and the following program on the 7D02:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=X
1 010=I/O W 011=I/O R 100=RFSH X
1 101=FCH 1 110=ACK  111=FCH N X
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXX0
```

Repeat the test for the $\overline{\text{BUSACK}}$. Apply the PG508 probe to ZIF pin 29. Change the 7D02 program to

```
C9-C4 (ANDED CLOCKS)=XXX1XX.
```

If the test fails, check A1U3039, A1U3010, A2U1040, and A1U2040.

R/$\overline{W}$ Setup and Hold

(Spec calls for 65 ns min. Setup and 0 ns min. Hold)

The R/$\overline{W}$ line is one of the address lines to the Control Line Encoder PROM. R/$\overline{W}$ must meet a setup time relative to the leading edge of the clock, so that the PROM can generate correct data.

a. Connect ST0-ST3 (ZIF pins 20-23) to +5 (pin 11 of the enabled Self-Test socket).

b. Connect $\overline{AS}$ (ZIF pin 34) to GND (ZIF pin 36).

c. Generate PG502 and PG508 pulses like those in Figure 6-5.

d. Apply PG508 to R/$\overline{W}$ (ZIF pin 30).

e. Apply PG502 to CLOCK (ZIF pin 35).

f. Enter the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000-MEM W 001-MEM R   STATUS=0
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 0
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

g. Press the 7D02 START button the run the test. Test passes if no data is acquired.

h. Repeat the test with the PG508 pulse inverted and the following 7D02 program:

```
1IF
1
```

```
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=0
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 1
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

If the test fails, check A1U3039.

ST0-ST3 Setup and Hold

(Spec calls for 65 ns Setup and 0 ns Hold)

ST0-ST3 address the Control Line Encoder PROM on Board 2.

a. Connect ST3 (ZIF pin 20) to GND (ZIF pin 36).

b. Connect $\overline{AS}$ (ZIF pin 34) to GND (ZIF pin 36).

c. Set up PG502 and PG508 waveforms like those in Figure 6-5.

d. Connect PG502 probe to CLOCK (ZIF pin 35).

e. Connect PG508 probe to ST0 to ST2 (ZIF pins 21-23).

f. Enter the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=1
1 010=I/O W 011=I/O R 100=RFSH 1
1 101=FCH 1 110=ACK  111=FCH N 0
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
```

```
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

Press the 7D02 START key to run the test. Test passes if no data is acquired.

Invert the PG508 pulse and repeat the test, with the following 7D02 program:

```
1IF
1
1 NOT
1 WORD RECOGNIZER # 1
1 DATA=XXXX
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=0
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 1
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
```

If the test fails, check A1U3010, A1U3015, A1U2045, and A1U2040.

$\overline{\text{WAIT}}$ Line Setup and Hold

(Spec calls for 55 ns min. Setup, 24 ns min. Hold)

The $\overline{\text{WAIT}}$ signal extends the CPU cycle. When the PM 110 detects a $\overline{\text{WAIT}}$, it delays the generation of the C9 qualifier. The signal must meet the Setup and Hold time requirements relative to the trailing edge of the clock.

a. Turn on the Self Test circuitry.

b. Connect A2TP7020 (CLOCK) to pin 35 of the ZIF socket.

c. Connect A2TP7010 ($\overline{\text{AS}}$) to pin 35 of the ZIF socket.

d. Connect pins 1-4 on A2P6040 to ZIF pins 1, 38, 39, and 40.

e. Connect ST0-ST3 (ZIF pins 20-23) to +5 (Self Test pin 11).

f. Set PG508 to external trigger, high impedance, and trigger it from $\overline{AS}$.

g. Generate a pulse low on the trailing edge of T2 clock (see Figure 6-10 below. Connect the PG508 to $\overline{WAIT}$ (ZIF pin 28).

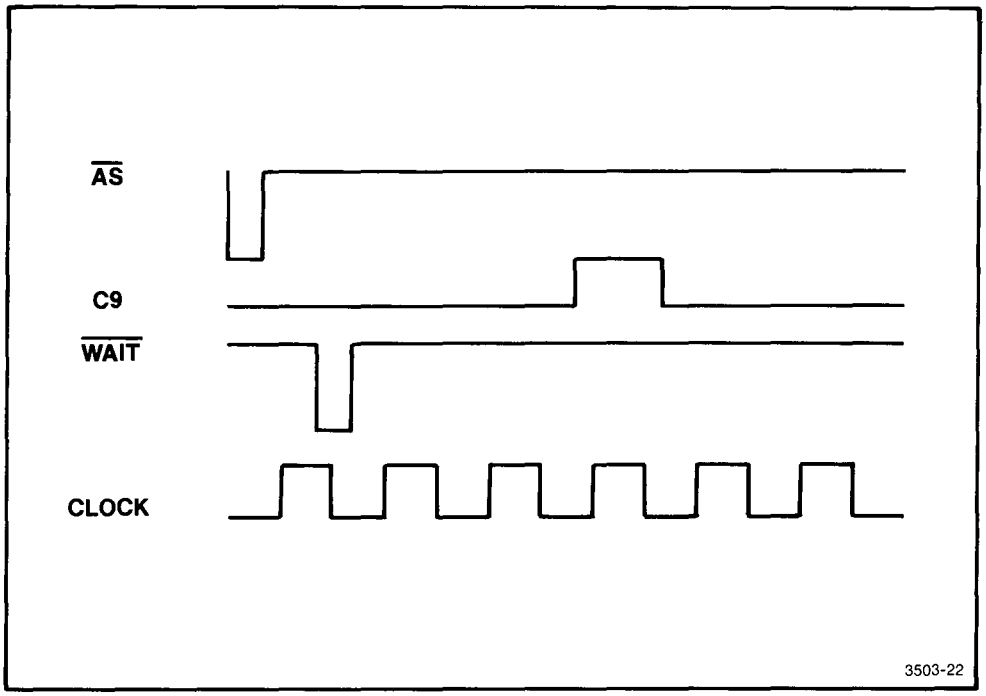


Figure 6-10. $\overline{WAIT}$ line setup and hold clock and data pulses.

h. C9 is A2TP5041.

i. Enter the following 7D02 program:

```
1IF
1
1 NOT
```


@

```
1 WORD RECOGNIZER # 1
1 DATA=XXX2
1 SEGMENT=XX
1 ADDRESS=XXXX
1 000=MEM W 001=MEM R   STATUS=0
1 010=I/O W 011=I/O R 100=RFSH 0
1 101=FCH 1 110=ACK  111=FCH N 1
1 N/S=X IRQ=X
1 T R/W=X uOUT,EPU=X EXT TRIG=X
1 TIMING WR=X
1
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=1XXXXX
```

j. Press the 7D02 START key to run the program.

k. Test passes if no data is acquired, and no SLOW CLOCK flag appears.

l. Repeat the test with the PG508 pulse inverted and the 7D02 program changed to DATA=XXX1.

If this test fails, check A1U3030, A1U1040, A1U2021, A1U1010, A1U1025, A1U1030, A1U1035, and A1U1020.

$\overline{\text{VI}}$, $\overline{\text{NVI}}$, $\overline{\text{SEGT}}$, and $\overline{\text{NMI}}$ Line Setup and Hold -- (Spec calls for $\overline{\text{VI}}$, $\overline{\text{NVI}}$, 110 ns min. Setup, 0 ns min. Hold; $\overline{\text{SEGT}}$ 85 ns min. Setup, 0 ns min. Hold; $\overline{\text{NMI}}$ 110 ns min. Setup, 28 ns min. Hold.)

All interrupt lines are ANDed and sampled by the 7D02 on the trailing edge of the clock, except for $\overline{\text{NMI}}$, which is internally latched first, and cleared late on the Interrupt Acknowledge cycle.

a. Turn on the Self Test circuit.

b. Connect A2TP7020 to CLOCK (ZIF pin 35).

c. Connect A2TP7010 to $\overline{\text{AS}}$ (ZIF pin 34).

d. Connect ST3 (ZIF pin 20) to GND (ZIF pin 36).

e. Trigger the PG508 from $\overline{\text{AS}}$ and generate a low pulse as in Figure 6-11.

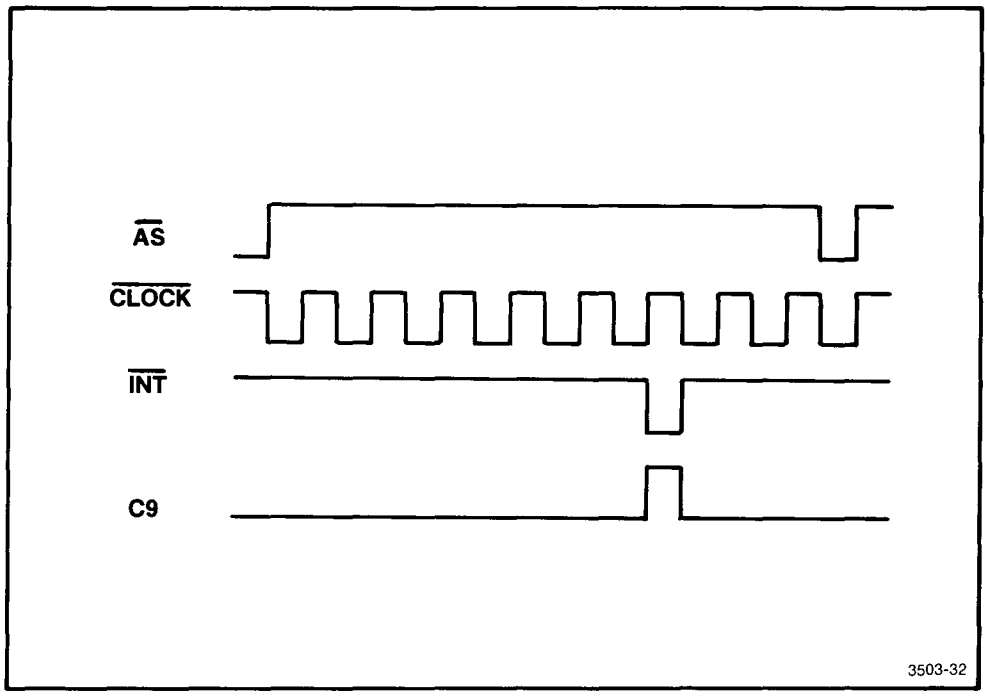


Figure 6-11. Interrupt setup and hold time clock and data pulses.

f. Connect PG508 probe to $\overline{VI}$ (ZIF pin 12).

g. Enter the following 7D02 program:

```
lIF
l
l NOT
l WORD RECOGNIZER # l
l DATA=XXXX
l SEGMENT=XX
l ADDRESS=XXXX
l 000=MEM W 001=MEM R   STATUS=X
l 010=I/O W 011=I/O R 100=RFSH X
l 101=FCH l 110=ACK  111=FCH N X
l N/S=X IRQ=l
l T R/W=X uOUT,EPU=X EXT TRIG=X
l TIMING WR=X
l
lTHEN DO
l TRIGGER 0-MAIN
```

```
1     0-BEFORE DATA
1     0-SYSTEM UNDER TEST CONT.
1     1-USER CLOCK QUAL.
1     1-FALLING EDGE OF CLOCK
1     C9-C4 (ANDED CLOCKS)=1X11XX
```

h. Press the 7D02 START key to run the test. Test passes if no data is acquired. The VECTORED INTERRUPT flag may show on the screen.

i. Repeat the test with the PG508 pulse inverted, and the 7D02 program changed to IRQ=0.

j. Repeat for $\overline{\text{NVI}}$ (ZIF pin 13) and $\overline{\text{SEGT}}$ (ZIF pin 14).

k. To test $\overline{\text{NMI}}$, apply a low pulse of 28 ns on ZIF pin 15. Set the IRQ bit on the 7D02 program to 1. $\overline{\text{NMI}}$ is edge-sensitive, so do not attempt to repeat the test with the pulse inverted.

If the test fails, check A1U3039, A1U2045, A1U3015, A2U1010, and A2U3040.

SIGNATURE ANALYSIS

Introduction

A 'signature' is a four-digit alphanumeric number representing time-dependent logic activity during a specified measurement interval for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probable malfunction in the circuit.

The signal that causes the node to produce a signature is the "stimulus". In signature analysis. The stimulus is supplied by the personality module itself. This way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation. The personality module supplies this predictable stimulus when the microprocessor plug is inserted into the Self Test Socket.

Signature Analysis Procedure

Disassemble and lay out the personality module boards as described in Figure 6-1 and Fig. 6-2.

Set up the PM 110 Self Test circuitry (see 'How to Use Self Test Circuitry') but leave the logic analyzer power switch off until ready to start.

Use a Sony/Tektronix 308 with a signature probe and a P6451 probe. Attach lines 0 and 1 of the P6451 probe to ST and SP on Board A2, the bottom board. Connect the P6451 Ground wire to

ground, and the P6451 Clock wire to C, both on Board A2.

Connect the ground wire of the signature probe to ground on the bottom board.

Set the signature analyzer as follows:

1. Press the 'C' key for signature.
2. Press the '6' key three times for falling edges.
3. Press the 'REPEAT' key.

Power up the logic analyzer. Press WD RECOGNIZER and put a 1 in EXT TRIG. Press TRIG, END, and START. The 7D02 should not trigger. Begin testing the PM 110 components. Compare the signatures of the components with the Signature Tables.

Table 6-1

SIGNATURES

NOTE

Table entries with '----' indicate a normally unstable signature on certain lines. An asterisk (*) means this pin is jumpered to another pin.

A1 (Upper) Board

NOTE

Some pins have an additional signature in parentheses. The parentheses signature is obtained when A2TP1020 (shown as $\overline{\text{PON}}$ on the board) is grounded.

Vcc 07U3

A1J2075

1	0000	
2	07U3	
3	U80F	
4	06A4	
5	040A	
6	0000	
7	3A4A	(681P)
8	AF0A	
9	07U2	
10	F8U2	(99U0)
11	HU9A	(CU35)
12	AP81	(5H02)
13	551A	
14	209U	(2CU7)
15	06A4	
16	07U3	
17	6P9F	
18	0000	

A1J5050

1	1AC3	(3H72)
2	56H3	
3	63F5	

4	----
5	P17P
6	07U3
7	06A4
8	07U2
9	6CPH
10	07U3
11	0000

A1U2010

1	0000
2	9288
3	0157
4	634F
5	00FH
6	07U3
7	0003
8	07U2
9	6P9F
10	0000
11	6P9F
12	07U2
13	0003
14	07U3
15	----
16	634F
17	0157
18	9288
19	0000
20	07U3

A1U2015

1	56H3
2	----
3	9288
4	634F
5	----
6	07U3
7	07U3
8	970F
9	----
10	0000
11	040A
12	----
13	0003
14	003F
15	----
16	7C6F
17	00FH

18	0157
19	30FF
20	07U3

A1U2020

1	0000
2	55U5
3	55U5
4	85FA
5	85FA
6	0000
7	003F
8	ACU9
9	ACU9
10	0000
11	040A
12	9288
13	9288
14	582F
15	582F
16	37A6
17	37A6
18	3UAP
19	3UAP
20	07U3

A1U2030

1	0000
2	PACU
3	970F
4	6CPH
5	P17P
6	63F5
7	CC08
8	UUUU
9	----
10	----
11	----
12	0000
13	----
14	----
15	----
16	----
17	----
18	37A6
19	55U5
20	07U3
21	85FA
22	0000

23	9288
24	07U3

A1U2035

1	07U3
2	----
3	UUUU
4	----
5	CC08
6	----
7	63F5
8	----
9	P17P
10	0000
11	6CPH
12	----
13	970F
14	----
15	PACU
16	----
17	00FH
18	----
19	07U3
20	07U3

A1U2040

1	0000
2	56H3
3	5120
4	84CP
5	834H
6	209U
7	276F
8	0000
9	3HC9
10	3A4A
11	30FF
12	U80F
13	7C6F
14	63F5
15	5120
16	07U3

A1U2045

1	PH4F
2	1AC3
3	84CP

@

4	06A4
5	06A4
6	06A4
7	0000
8	07U2
9	07U3
10	07U2
11	56H3
12	CFUC
13	P17P
14	07U3

A1U3010

1	0000
2	003F
3	07U2
4	970F
5	F8U2
6	HU9A
7	551A
8	AP81
9	U80F
10	0000
11	U80F
12	AP81
13	551A
14	HU9A
15	F8U2
16	970F
17	07U2
18	003F
19	0000
20	07U3

A1U3015

1	0000
2	03U9
3	AF0A
4	PACU
5	P17P
6	0157
7	63F5
8	00FH
9	073P
10	0000
11	00FH
12	073P
13	----
14	----

15	P68H
16	----
17	ACU9
18	040A
19	0000
20	07U3

A1U3020

1	0000
2	582F
3	003F
4	ACU9
5	05FA
6	9288
7	3UAP
8	37A6
9	55U5
10	0000
11	55U5
12	37A6
13	3UAP
14	9288
15	85FA
16	ACU9
17	----
18	582F
19	0000
20	07U3

A1U3030

1	0000
2	CC08
3	CC08
4	PACU
5	PACU
6	6CPH
7	6CPH
8	00FH
9	0000
10	0000
11	040A
12	63F5
13	63F5
14	UUUU
15	UUUU
16	P17P
17	P17P
18	970F
19	970F

20	07U3

A1U3035

1	0000
2	UUUU
3	970F
4	00FH
5	P17P
6	PACU
7	63F5
8	6CPH
9	CC08
10	0000
11	CC08
12	6CPH
13	63F5
14	PACU
15	P17P
16	00FH
17	970F
18	UUUU
19	0000
20	07U3

A1U3039

1	0000
2	07U2
3	07U3
4	CFUC
5	06A4
6	6CPH
7	06A4
8	07U2
9	06A4
10	0000
11	06A4
12	07U2
13	06A4
14	6CPH
15	06A4
16	----
17	07U3
18	07U2
19	0000
20	07U3

ZIF Socket (A1J6010)

1	UUUU
2	003F
3	55U5
4	37A6
5	85FA
6	3UAP
7	07U2
8	ACU9
9	ACU9
10	582F
11	07U3
12	06A4
13	06A4
14	06A4
15	ACU9
16	07U3
17	07U2
18	00FH
19	00FH
20	P68H
21	CFUC
22	6436
23	U80F
24	0003
25	00FH
26	0157
27	0157
28	0157
29	07U2
30	6CPH
31	PACU
32	00FH
33	0000
34	03U9
35	07U3
36	0000
37	003F
38	CC08
39	63F5
40	P17P
41	970F
42	970F
43	6CPH
44	PACU
45	00FH
46	634F
47	9288
48	9288

A2 (Lower) Board

NOTE

On all lower board signatures, the $\overline{\text{PON}}$ is attached to GND.

A2U1020

1	07U3
2	0000
3	07U3
4	07U3
5	07U3
6	0000
7	07U3
8	0000
9	P219
10	69P4
11	98U7
12	040A
13	5PCC
14	32C8
15	354C
16	07U3

A2U1030

1	----
2	040A
3	040A
4	03U9
5	040A
6	0000
7	0000
8	4FHP
9	3379
10	7854
11	7854
12	0000
13	7UA7
14	07U3

A2U1010

1	07U3
2	0000
3	07U3
4	03U9
5	040A

6	03U9
7	0000
8	----
9	----
10	07U3
11	AF0A
12	07U3
13	----
14	07U3

A2U1025

1	HAF2
2	0000
3	0000
4	5337
5	4FHP
6	3379
7	FHP5
8	FHP5
9	03U9
10	0000
11	714A
12	0000
13	66U2
14	99CF
15	A66U
16	A99C
17	A99C
18	07U3
19	0000
20	07U3

A2U1035

1	0000
2	32C8
3	0000
4	7UA7
5	FHP5
6	714A
7	----
8	0000
9	6P9F
10	FHP5
11	66U2
12	A66U
13	FHP5
14	P5PA
15	040A
16	07U3

A2U1040

1	----
2	06A4
3	HAF2
4	040A
5	0001
6	07U3
7	0000
8	681P
9	07U2
10	6398
11	2CU7
12	07U2
13	U5CF
14	07U3

A2U2021

1	07U3
2	07U3
3	07U3
4	----
5	07U3
6	0000
7	0000
8	----
9	----
10	----
11	0000
12	----
13	07U3
14	07U3

A2U2030

1	0000
2	----
3	CU35
4	6398
5	----
6	----
7	----
8	0000
9	07U3
10	----
11	----
12	----
13	99U0
14	3H72
15	3H72

16	07U3

A2U3010

1	07U3
2	07U3
3	07U3
4	07U3
5	0000
6	07U3
7	0000
8	03U9
9	040A
10	07U3
11	07U3
12	0001
13	07U3
14	07U3

A2U3020

1	0000
2	07U3
3	0000
4	0000
5	07U3
6	0000
7	----
8	0000
9	040A
10	07U3
11	040A
12	----
13	07U3
14	07U3
15	07U3
16	07U3

A2U3030

1	07U3
2	07U3
3	06A4
4	----
5	714A
6	HH31
7	0000
8	03U9
9	07U3
10	07U3

11	03U9
12	488U
13	488U
14	07U3

A2U3040

1	HC95
2	06A4
3	0000
4	07U3
5	07U3
6	07U3
7	0000
8	488U
9	56H3
10	U80F
11	5337
12	551A
13	06A4
14	07U3

A2U4010

1	07U3
2	07U3
3	07U3
4	0157
5	0003
6	07U2
7	0000
8	03U9
9	040A
10	040A
11	07U3
12	0000
13	07U3
14	07U3

A2U4020

1	0157
2	06A4
3	0000
4	07U3
5	63F5
6	6436
7	0000
8	U80F
9	UUUU

10	CFUC
11	CC08
12	P68H
13	P17P
14	07U3

A2U4030

1	07U3
2	07U3
3	07U3
4	07U3
5	07U3
6	07U3
7	03U9
8	0000
9	07U3
10	C799
11	37A6
12	55U5
13	0A34
14	9288
15	8P5U
16	07U3

A2U4040

1	07U3
2	07U3
3	07U3
4	07U3
5	07U3
6	07U3
7	03U9
8	0000
9	07U3
10	07U3
11	0003
12	003F
13	00FH
14	0157
15	0001
17	07U3

A2U5010

1	07U3
2	07U3
3	07U3
4	07U3

@

5	07U3
6	07U3
7	03U9
8	0000
9	07U3
10	0001
11	P17P
12	63F5
13	CC08
14	UUUU
15	CF36
16	07U3

A2U5020

1	07U3
2	07U3
3	07U3
4	07U3
5	07U3
6	07U3
7	03U9
8	0000
9	07U3
10	CF36
11	634F
12	PACU
13	970F
14	6CPH
15	C799
16	07U3

A2U5030

1	07U3
2	07U3
3	07U3
4	07U3
5	07U3
6	07U3
7	03U9
8	0000
9	07U3
10	8P5U
11	ACU9
12	582F
13	3UAP
14	85FA
15	0001
16	07U3

A2U6010

1	0000
2	970F
3	970F
4	P17P
5	P17P
6	63F5
7	63F5
8	CC08
9	CC08
10	0000
11	6CPH
12	6CPH
13	PACU
14	PACU
15	UUUU
16	UUUU
17	634F
18	634F
19	0000
20	07U3

A2U6020

1	0000
2	9288
3	9288
4	003F
5	003F
6	55U5
7	55U5
8	37A6
9	37A6
10	0000
11	582F
12	582F
13	ACU9
14	ACU9
15	3UAP
16	3UAP
17	85FA
18	85FA
19	0000
20	07U3

A2U6030

1	0000
2	003F
3	003F

```
4   ACU9
5   ACU9
6   0157
7   0157
8   0003
9   0003
10  0000
11  00FH
12  00FH
13  07U3
14  ----
15  0157
16  0157
17  00FH
18  00FH
19  0000
20  07U3


A2P6040

1   0157
2   00FH
3   003F
4   0003
5   UUUU
6   CC08
7   63F5
8   P17P


BAS  ----

QUAL  6P9F

INTO  551A


A2P1020

1   07U3
2   HAF2*
3   HAF2*


A2P2030

1   0000
2   HH31*
3   HH31*


A
```

1 003F*
2 003F*
3 0A34

B

1 00FH*
2 00FH*
3 634F

A2P6010

1 07U3*
2 07U3*
3 07U3

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

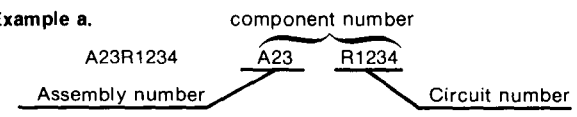
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

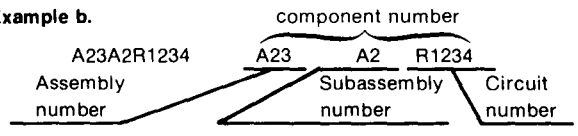
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-7388-00			CKT BOARD ASSY:UPPER	80009	670-7388-00
A2	670-7389-00			CKT BOARD ASSY:LOWER	80009	670-7389-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A1	----- -----			CKT BOARD ASSY:UPPER		
A1C1010	283-0203-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N075E474M
A1C2015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3044	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	72982	8101B210C0G0100J
A1C3045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3046	283-0260-00			CAP.,FXD,CER DI:5.6PF,5%,200V	72982	8111B200C0G569C
A1C3047	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710100X5P101J
A1C4010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4045	283-0175-00			CAP.,FXD,CER DI:10PF,5%,200V	72982	8101B210C0G0100J
A1C4070	281-0541-00			CAP.,FXD,CER DI:6.8PF,10%,500V	72982	301-000C0H0689D
A1C5010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C7045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1CR2050	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR3040	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR3045	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR4090	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1J6020	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A1Q2040	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A1Q2042	151-0712-00			TRANSISTOR:SILICON,NPN	04713	SPS8223
A1Q3040	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A1Q3045	151-0711-00			TRANSISTOR:SILICON,NPN	04713	SPS8224
A1R1010	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1020	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1027	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1029	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1030	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1037	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1040	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1047	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1049	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1050	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R2010	307-0651-00			RES NTWK,FXD,FI:5,3.3K OH,5%,0.150W	01121	206A332
A1R2042	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R2050	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R3040	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A1R3041	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A1R3042	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A1R3043	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R3045	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R3047	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R3049	321-0281-00			RES.,FXD,FILM:8.25K OHM,1%,0.125W	91637	MFF1816G82500F
A1R4040	321-0342-00			RES.,FXD,FILM:35.7K OHM,1%,0.125W	91637	MFF1816G35701F
A1R5035	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R5050	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1R6010	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R7040	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R7045	321-0288-00			RES.,FXD,FILM:9.76K OHM,1%,0.125W	91637	MFF1816G97600F
A1U1010	156-1150-01			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-1150-01
A1U2010	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U2015	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U2020	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A1U2030	160-1509-00			MICROCIRCUIT,DI:8192 X 8 EPROM	80009	160-1509-00
A1U2035	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A1U2040	156-0720-01			MICROCIRCUIT,DI:HEX BUS DR W/3 STATE INPUT	80009	156-0720-01
A1U2045	156-0460-00			MICROCIRCUIT,DI:QUAD 2-INP AND GATE	80009	156-0460-00
A1U3010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244N
A1U3015	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	18324	N74LS240N
A1U3020	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244N
A1U3030	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244N
A1U3035	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244N
A1U3039	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	18324	N74LS244N
A1U4010	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4015	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4020	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4025	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4030	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4035	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U4040	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A1U5010	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U5015	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U5020	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U5030	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U7050	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	----- -----			CKT BOARD ASSY:LOWER		
A2C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2010	283-0256-00			CAP.,FXD,CER DI:130PF,5%,100V	51642	200-100N1500131J
A2C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C5020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C5030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C5040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C7030	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A2C7040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C8010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C8020	283-0769-00			CAP.,FXD MICA D:278PF,1%,500V	00853	D15-5F2780F0
A2C8021	283-0687-00			CAP.,FXD,MICA D:560PF,2%,300V	00853	D153E561G0
A2L8020	108-0719-00			COIL,RF:805NH	80009	108-0719-00
A2Q2010	151-0301-01			TRANSISTOR:SILICON,PNP,PRESTRESSED	80009	151-0301-01
A2Q8020	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2R2020	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A2R3010	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A2R7010	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A2R7040	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R7041	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A2R8010	315-0912-00			RES.,FXD,CMPSN:9.1K OHM,5%,0.25W	01121	CB9125
A2U1010	156-0388-02			MICROCIRCUIT,DI:DL D FLIP-FLOP,CHK	80009	156-0388-02
A2U1020	156-1318-00			MICROCIRCUIT,DI:4 BIT BISTABLE LATCH	01295	SN74LS375
A2U1025	156-0975-02			MICROCIRCUIT,DI:UNIV SHIFT/STORAGE RGTR	01295	SN74LS299N3/J4
A2U1030	156-0383-01			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	80009	156-0383-01
A2U1035	156-0798-01			MICROCIRCUIT,DI:DUAL 14-LINE TO 1-LINE	80009	156-0798-01
A2U1040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U2020	160-1205-00			MICROCIRCUIT,DI:32 X 8 PROM	80009	160-1205-00
A2U2021	156-0388-02			MICROCIRCUIT,DI:DL D FLIP-FLOP,CHK	80009	156-0388-02
A2U2030	156-1221-00			MICROCIRCUIT,DI:HEX D-TYPE FF	01295	SN74LS378
A2U3010	156-0388-02			MICROCIRCUIT,DI:DL D FLIP-FLOP,CHK	80009	156-0388-02
A2U3020	156-1258-00			MICROCIRCUIT,DI:DUAL J-K NEG-EDGE TRIG FF	01295	SN74LS112
A2U3030	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A2U3040	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A2U4010	156-0466-01			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR	80009	156-0466-01
A2U4020	156-0645-01			MICROCIRCUIT,DI:SCHMITT-TRIG,POS-NAND GATE	80009	156-0645-01
A2U4030	156-0844-01			MICROCIRCUIT,DI:SYN 4-BIT BINCNTR,FT	80009	156-0844-01
A2U4040	156-0788-00			MICROCIRCUIT,DI:SYN 4-BIT CNTR W/SYN CLEAR	34335	SN74LS162A
A2U5010	156-0844-01			MICROCIRCUIT,DI:SYN 4-BIT BINCNTR,FT	80009	156-0844-01
A2U5020	156-0844-01			MICROCIRCUIT,DI:SYN 4-BIT BINCNTR,FT	80009	156-0844-01
A2U5030	156-0844-01			MICROCIRCUIT,DI:SYN 4-BIT BINCNTR,FT	80009	156-0844-01
A2U6010	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A2U6020	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97
A2U6030	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

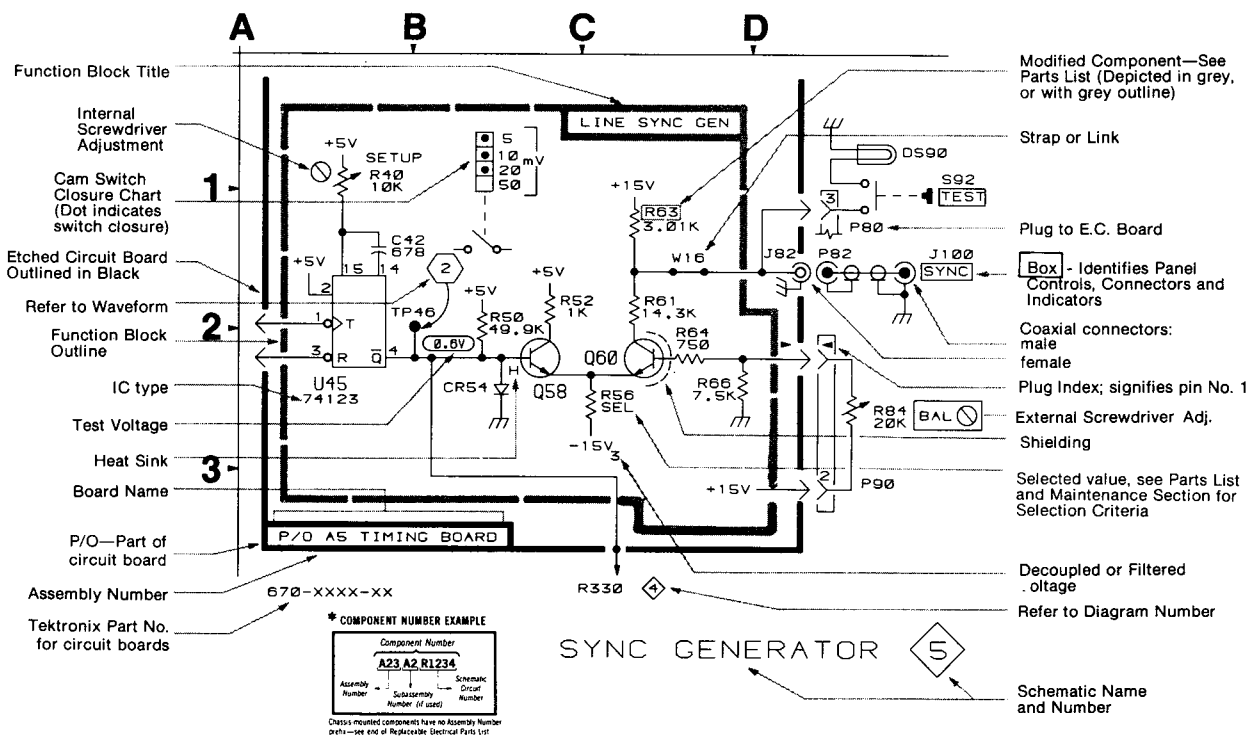
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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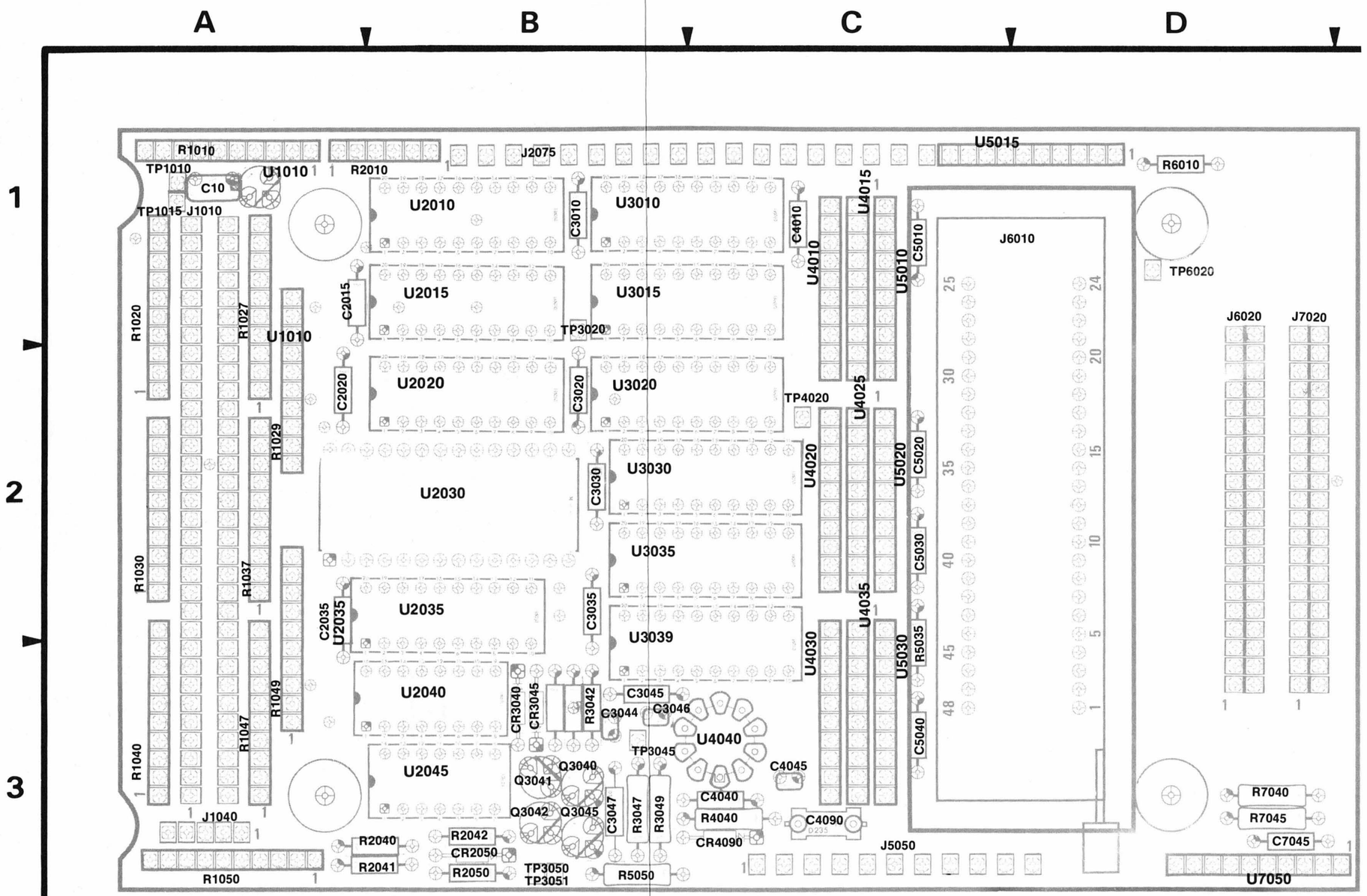


3503-24

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Figure 8-1. A1 Upper Board Component Locations.

@

TABLE 8-1

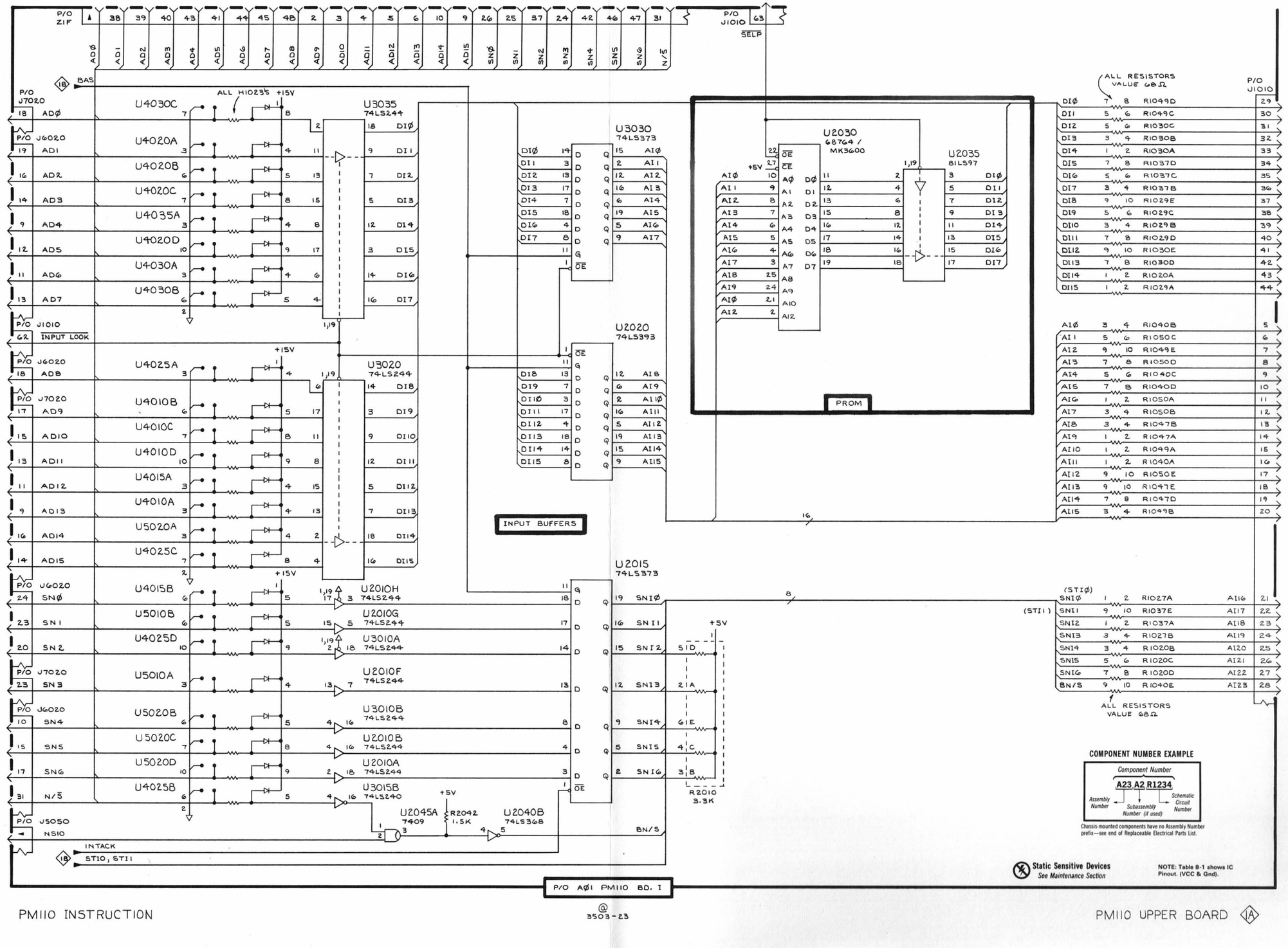
IC Pin Information

PM 110	VCC	GND
7409	14	7
74LS00	14	7
74LS02	14	7
74LS10	14	7
74LS11	14	7
74LS14	14	7
74LS37	14	7
74LS74	7	14
74LS112	16	8
74LS153	16	8
74LS161	16	8
74LS162	16	8
74LS240	20	10
74LS244	20	10
74LS288	16	8
74LS299	20	10
74LS368	16	8
74LS373	20	10
74LS375	16	8
74LS378	16	8
74LS393	14	7
81LS97	20	10
H1023	1	2
SP9685	2	1,16

UPPERBOARD 1A

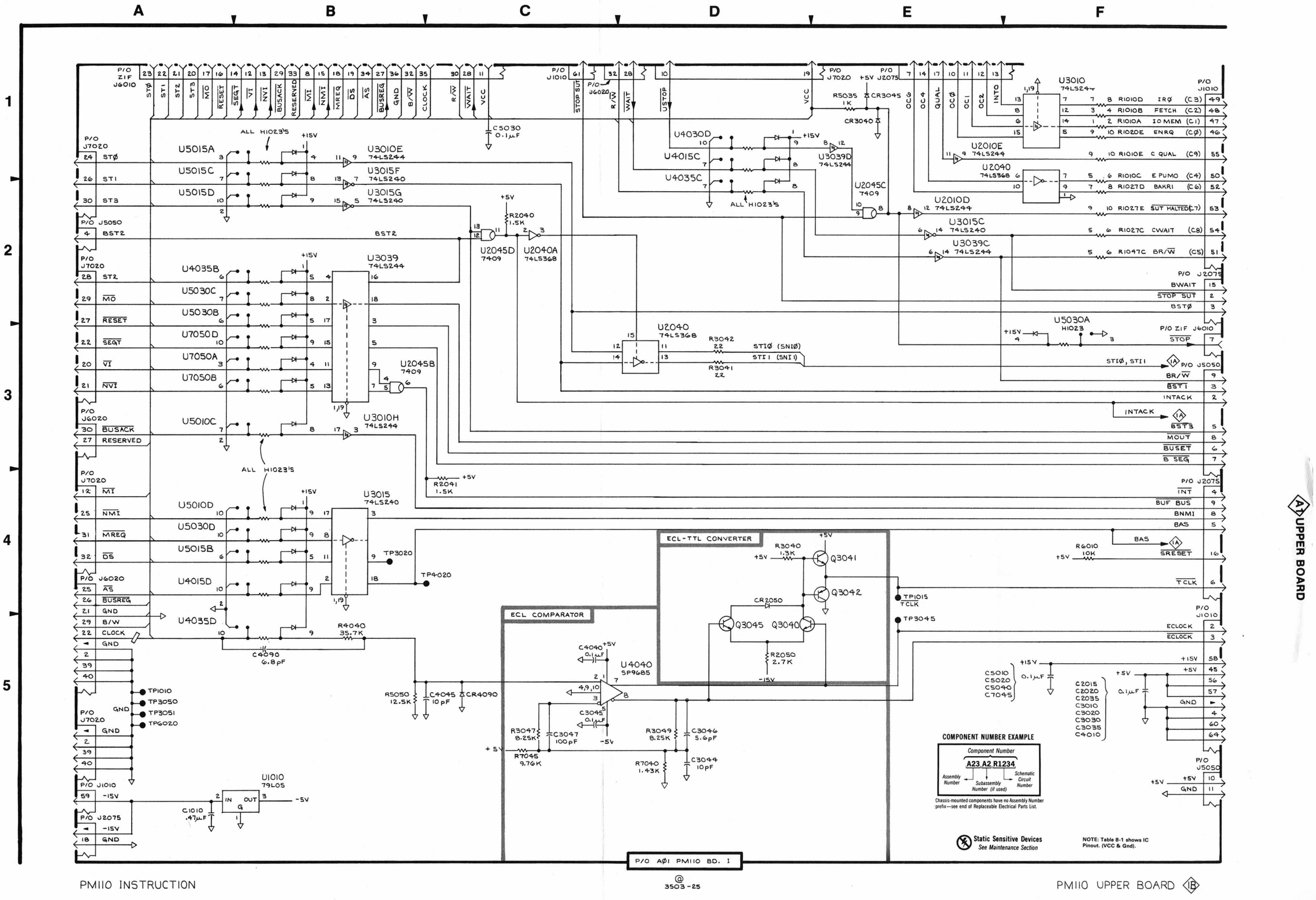
ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1010	A3	A1	R1049D	F1	A3
J1010	D1	A1	R1049E	F3	A3
J1010	F1	A1	R1050A	F3	A3
J5050	A5	C3	R1050B	F3	A3
J6010	A1	C1	R1050C	F3	A3
J6020	A5	D1	R1050D	F3	A3
J6020	A1	D1	R1050E	F3	A3
J6020	A3	D1	R2010	D5	B1
J6020	A4	D1	R2042	C5	B3
J7020	A3	D1	U2010A	B5	B1
J7020	A5	D1	U2010B	B5	B1
J7020	A1	D1	U2010F	B5	B1
R1020A	F2	A1	U2010G	B4	B1
R1020B	F5	A1	U2010H	B4	B1
R1020C	F5	A1	U2015	C4	B1
R1020D	F5	A1	U2020	C3	B2
R1020E	F5	A1	U2030	D2	B2
R1027A	F4	A1	U2035	E2	B2
R1027B	F4	A1	U2040B	C5	B3
R1029A	F2	A2	U2045A	B5	B3
R1029B	F2	A2	U3010A	B5	B1
R1029C	F2	A2	U3010B	B5	B1
R1029E	F2	A2	U3015B	B5	B1
R1030A	F2	A2	U3020	B3	B2
R1030B	F1	A2	U3030	C2	B2
R1030C	F1	A2	U3035	B2	B2
R1030D	F2	A2	U4020A	A1	C2
R1030E	F2	A2	U4020B	A2	C2
R1037A	F4	A2	U4020C	A2	C2
R1037B	F2	A2	U4020D	A2	C2
R1037C	F2	A2	U4025A	A3	C2
R1037D	F2	A2	U4025B	A5	C2
R1037E	F4	A2	U4025C	A4	C2
R1040A	F3	A3	U4025D	A4	C2
R1040B	F3	A3	U4030A	A2	C3
R1040C	F3	A3	U4030B	A2	C3
R1040D	F3	A3	U4030C	A1	C3
R1047A	F3	A3	U4035A	A2	C2
R1047B	F3	A3	U5010A	A5	C1
R1047D	F4	A3	U5010B	A4	C1
R1047E	F4	A3	U5020A	A4	C2
R1049A	F3	A3	U5020B	A5	C2
R1049B	F4	A3	U5020C	A5	C2
R1049C	F1	A3	U5020D	A5	C2



ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	A5	A1	R2040	C2	B3
C2015	F5	A1	R2041	C4	B3
C2020	F5	A2	R2050	D5	B3
C2035	F5	A2	R3040	D4	B3
C3010	F5	B1	R3041	D3	B3
C3020	F5	B2	R3042	D3	B3
C3030	F5	B2	R3047	C5	B3
C3035	F5	B2	R3049	D5	B3
C3044	D5	B3	R4040	B5	C3
C3045	C5	B3	R5035	E1	C3
C3046	D5	B3	R5050	B5	B3
C3047	C5	B3	R6010	F4	D1
C4010	F5	C2	R7040	D5	D3
C4040	C5	C3	R7045	C5	D3
C4045	C5	C3	TP1010	A5	A1
C4090	B5	C3	TP1015	E4	A1
C5010	F5	C2	TP3020	B4	B1
C5020	F5	C2	TP3045	E5	B3
C5030	C1	C2	TP3050	A5	B3
C5040	F5	C3	TP3051	A5	B3
C7045	F5	D3	TP4020	C4	C2
CR2050	D4	B3	TP6020	A5	D1
CR3040	E1	B3	U1010	B5	A1
CR3045	E1	B3	U2010D	E2	B1
CR4090	C5	C3	U2010E	E1	B1
J1010	A5	A1	U2040	F2	B3
J1010	F5	A1	U2040	D3	B3
J1010	C1	A1	U2040A	C2	B3
J2075	F4	B1	U2045B	B3	B3
J2075	A5	B1	U2045C	E2	B3
J2075	F2	B1	U2045D	C2	B3
J2075	E1	B1	U3010	F1	B1
J5050	A2	C3	U3010E	B1	B1
J5050	F5	C3	U3010H	B3	B1
J5050	F3	C3	U3015	B4	B1
J6010	A1	C1	U3015C	E2	B1
J6010	F3	C1	U3015F	B2	B1
J6020	A4	D1	U3015G	B2	B1
J6020	A3	D1	U3039	B2	B3
J6020	A3	D1	U3039C	E2	B3
J7020	A2	D1	U3039D	E1	B3
J7020	E1	D1	U4030D	D1	C3
J7020	A1	D1	U4035B	A2	C2
J7020	A5	D1	U4035C	D2	C2
J7020	A4	D1	U4035D	A5	C2
Q3040	D5	B3	U4035D	A5	C2
Q3041	E4	B3	U4040	C5	C3
Q3042	E4	B3	U5010D	A4	C1
Q3045	D5	B3	U5015A	A1	C1
R1010A	F1	A1	U5015B	A4	C1
R1010B	F1	A1	U5015C	A1	C1
R1010C	F1	A1	U5015D	A2	C1
R1010D	F1	A1	U5030A	F3	C3
R1010E	F1	A1	U5030B	A2	C3
R1020E	F1	A1	U5030C	A2	C3
R1027C	F2	A1	U5030D	A4	C3
R1027D	F2	A1	U7050A	A3	D3
R1027E	F2	A1	U7050B	A3	D3
R1047C	F2	A3	U7050D	A3	D3



A2 LOWER BOARD

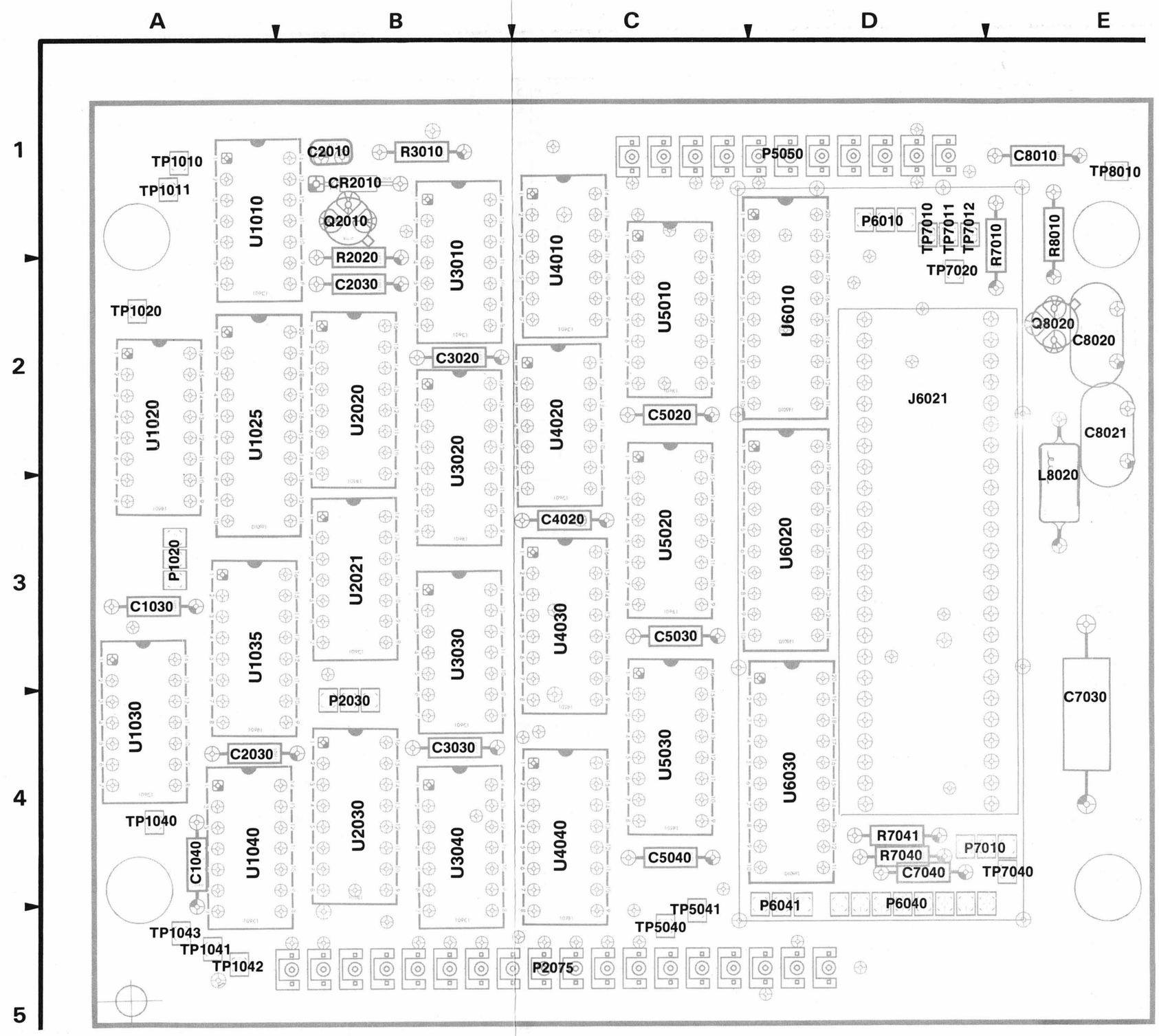
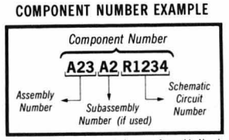


Figure 8-2. A2 Lower Board Component Locations.

3503-26

Static Sensitive Devices
See Maintenance Section

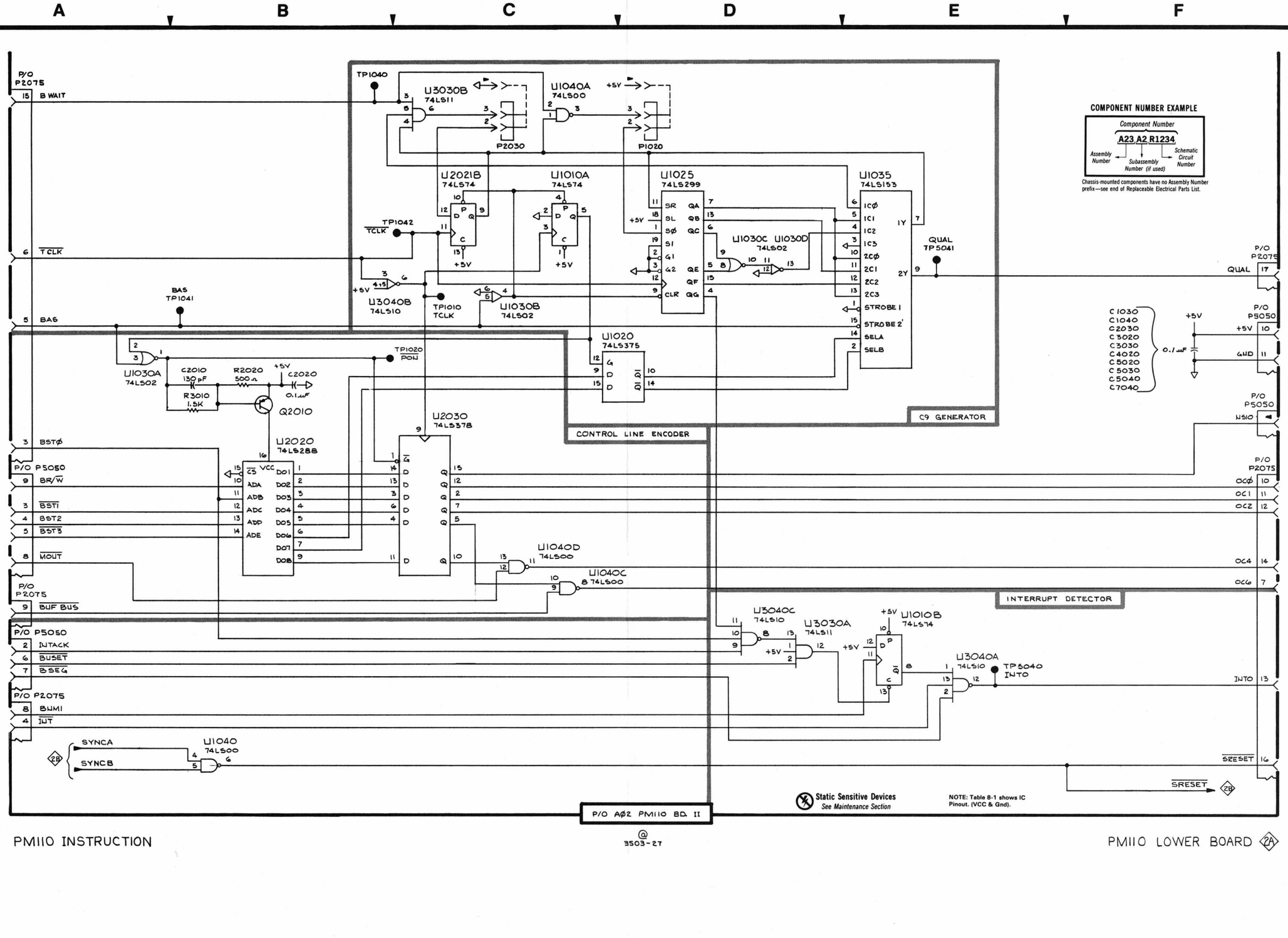
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

ASSEMBLY A02

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1030	F2	A3
C1040	F2	A4
C2010	B3	B1
C2020	B3	B2
C2030	F2	A4
C3020	F2	B2
C3030	F2	B4
C4020	F2	C3
C5020	F2	C2
C5030	F2	C3
C5040	F2	C4
C7040	F2	D4
P1020	D1	A3
P2030	C1	B4
P2075	A4	B5
P2075	F2	B5
P2075	A1	B5
P2075	F3	B5
P5050	A3	C1
P5050	A4	C1
P5050	F2	C1
P5050	F3	C1
Q2010	B3	B1
R2020	B3	B1
R3010	B3	B1
TP1010	C2	A1
TP1020	B2	A2
TP1040	B1	A4
TP1041	B2	A5
TP1042	C2	A5
TP5040	E4	C5
TP5041	E2	C5
U1010B	E4	A1
U1020	C2	A2
U1025	D2	A2
U1030A	A2	A4
U1030B	C2	A4
U1030C	D2	A4
U1030D	D2	A4
U1035	E2	A3
U1040	B5	A4
U1040A	C1	A4
U1040C	C4	A4
U1040D	C4	A4
U2020	B3	B2
U2021B	C2	B3
U2030	C3	B4
U3030A	D4	B3
U3030B	C1	B3
U3040A	E4	B4
U3040B	B2	B4
U3040C	D4	B4



COMPONENT NUMBER EXAMPLE

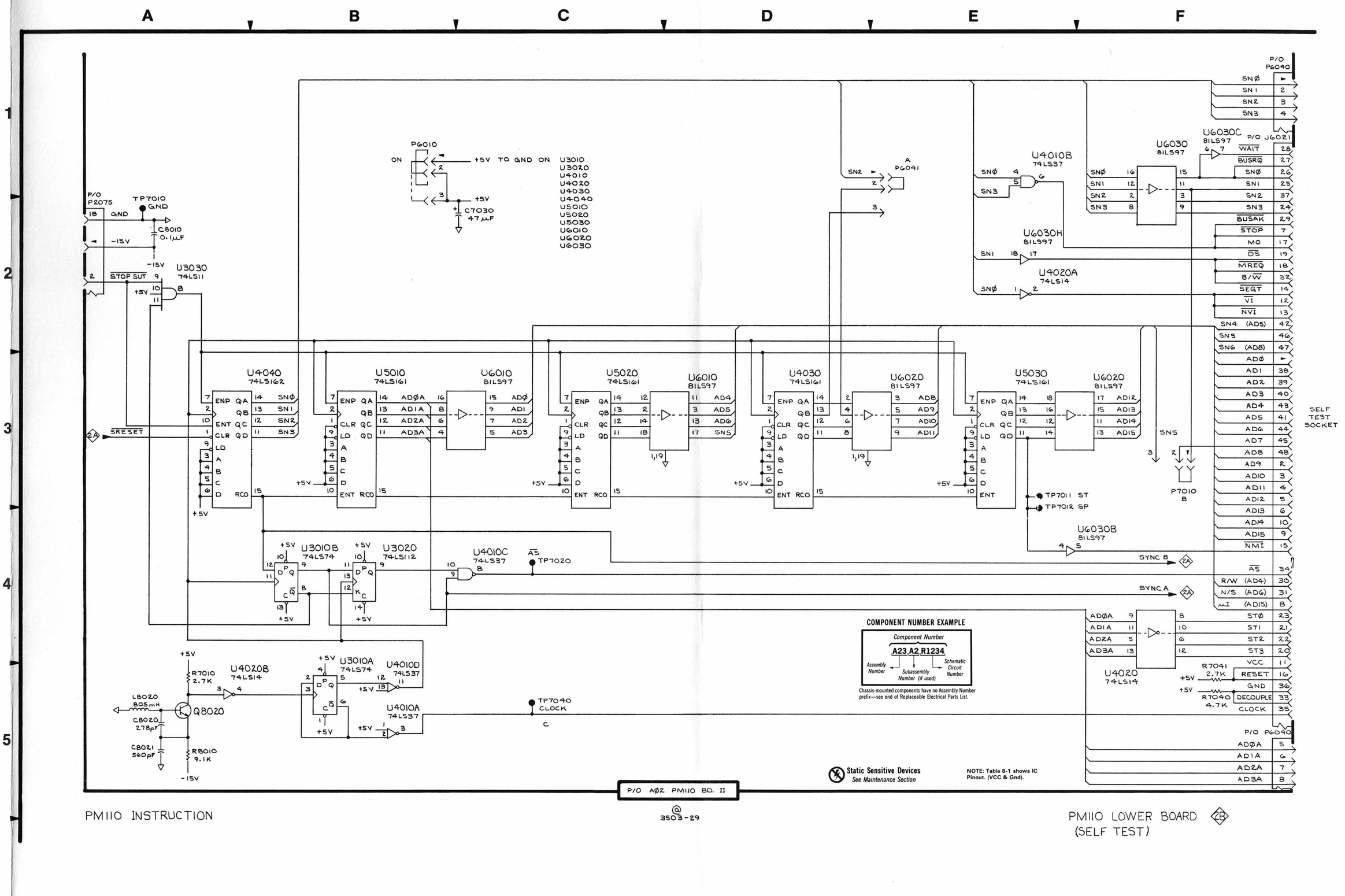
Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

LOWERBOARD 2B

ASSEMBLY A02

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C7030	C2	E3
C8010	A2	E1
C8020	A5	E2
C8021	A5	E2
J6021	F1	D2
L8020	A5	E2
P2075	A2	B5
P6010	B1	D1
P6040	F1	D4
P6040	F5	D4
P6041	E1	D4
P7010	F3	E4
Q8020	A5	E2
R7010	A5	E1
R7040	F5	D4
R7041	F5	D4
R8010	A5	E1
TP7010	A2	D1
TP7011	E3	D1
TP7012	E3	D1
TP7020	B4	D2
TP7040	C5	E4
U3010A	B5	B2
U3010B	B4	B2
U3020	B4	B3
U3030	A2	B3
U4010A	B5	C2
U4010B	E1	C2
U4010C	B4	C2
U4010D	B5	C2
U4020	F4	C2
U4020A	E2	C2
U4020B	A5	C2
U4030	D3	C3
U4040	A3	C4
U5010	B3	C2
U5020	C3	C3
U5030	E3	C4
U6010	D3	D2
U6010	C3	D2
U6020	E3	D3
U6020	F3	D3
U6030	F1	D4
U6030B	F4	D4
U6030C	F1	D4
U6030H	E2	D4



PM110 INSTRUCTION

PM110 LOWER BOARD (2B)
(SELF TEST)

P/O J1010		P/O P7020
5	UDS (AIØ)	5
6	AI1	◄
7	AI2	7
8	AI3	4
9	AI4	9
10	AI5	6
11	AI6	8
12	AI7	11
13	AI8	12
14	AI9	13
15	AI10	15
16	AI11	14
17	AI12	17
18	AI13	16
19	AI14	19
20	AI15	18
21	AI16	21
22	AI17	22
23	AI18	23
24	AI19	24
25	AI20	26
26	AI21	25
27	AI22	28
28	AI23	27
58	+15V$_D$	58
56	+5V	45
57		57
45		10
◄	GND	20
4		30
60		40
64		50
59	-15V$_D$	59

AØ3 PM110 LOGIC ANALYZER PLUG BD.

P/O J1010		P/O P7020
29	DIØ	32
30	DI1	29
31	DI12	34
32	DI3	31
33	DI4	33
34	DI5	36
35	DI6	35
36	DI7	38
37	DI8	42
38	DI9	37
39	DI10	39
40	DI11	44
41	DI12	41
42	DI13	46
43	DI14	43
44	DI15	48
46	CØ (ENRQ)	47
47	C1 (IOMEM)	52
48	C2 (FETCH)	49
49	C3 (IRQ)	54
50	C4 (E PUMO)	56
51	C5 (BR/$\overline{W}$)	51
52	C6 (BAKRI)	60
53	C7 (SUT HALTED)	53
54	C8 (CWAIT)	62
55	C9 (C QUAL)	55
63	$\overline{SELP}$	63
61	$\overline{HALT}$ (STOP SUT)	61
2	CLOCK (ECLOCK)	2
3	$\overline{CLOCK}$ ($\overline{ECLOCK}$)	3
62	LOOK (INPUT LOOK)	64

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
- A23: Assembly Number
- A2: Subassembly Number (if used)
- R1234: Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

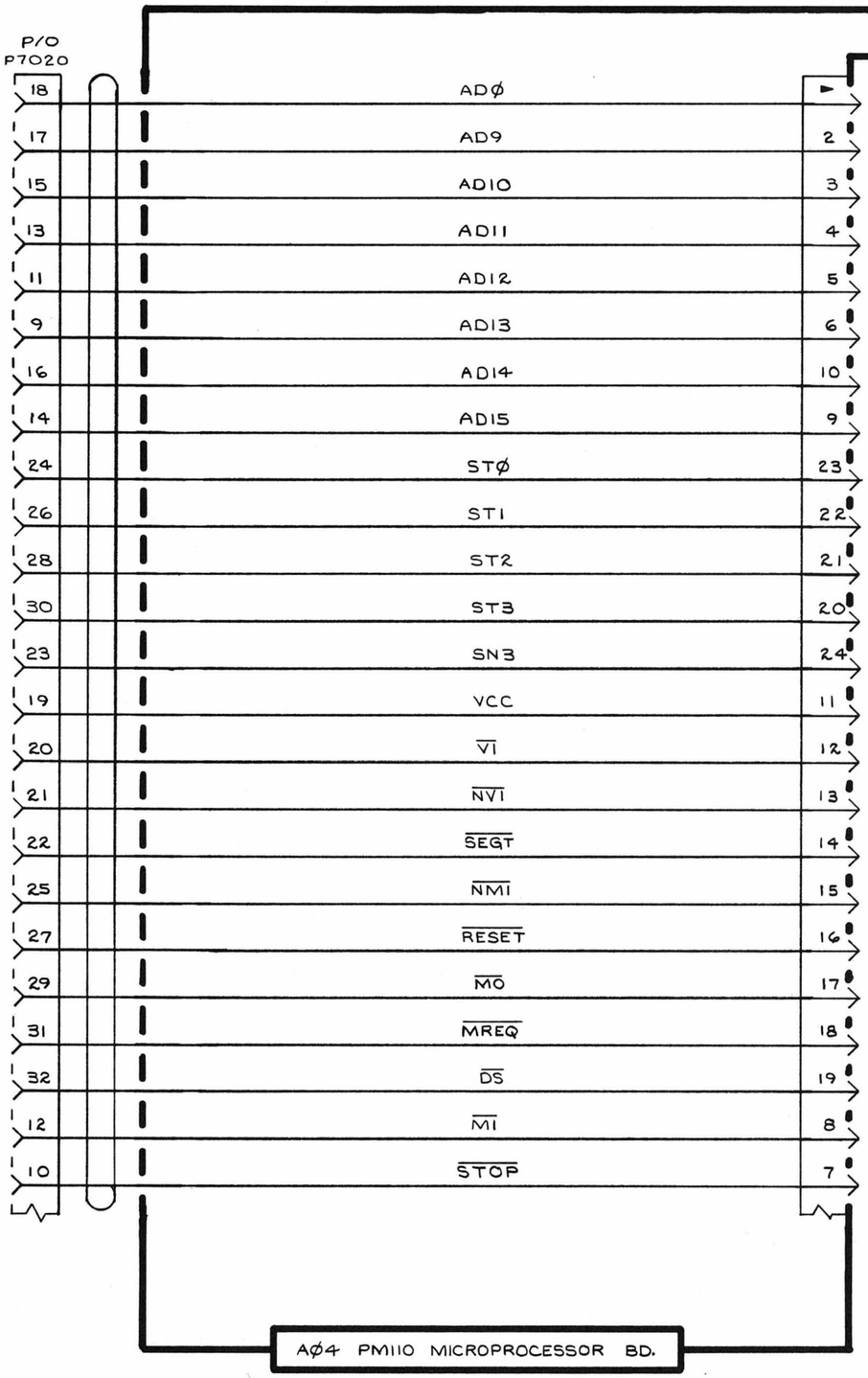
Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

A3 L A PLUG

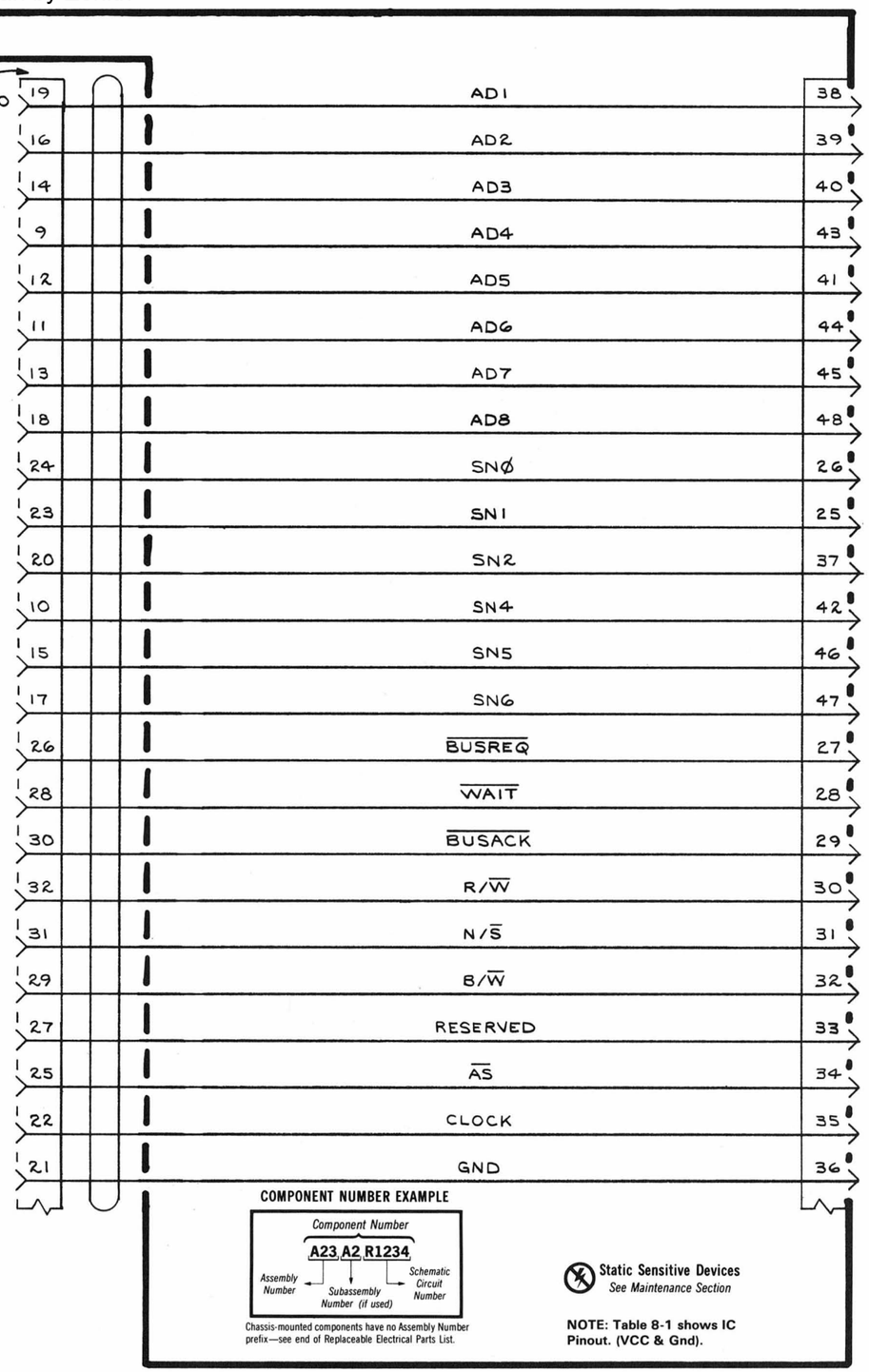
PM110 INSTRUCTION @ 3503-30

PM110 LOGIC ANALYZER PLUG 3



@ 3503-31

PM110 INSTRUCTION



COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

PM110 MICROPROCESSOR PLUG ④

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-4433-00			1		MARKER,IDENT:MKD Z8001	80009	334-4433-00
-2	380-0658-00			1		HSG HALF,CKT BD:TOP	80009	380-0658-00
						(ATTACHING PARTS)		
-3	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-4	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
						(ATTACHING PARTS)		
-5	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-6	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-7	200-2412-01			1		CABLE,NIP ELEC:3.45 L X 0.05 INS DIM	80009	200-2412-01
	175-4600-00			1		CA ASSY,SP,ELEC:48 PIN,21.0 L	80009	175-4600-00
-8	386-4684-00			1		. PLATE,PIN PROT:48 PIN,NYLON	80009	386-4684-00
-9	204-0909-00			1		. BODY HALF,PROBE:BOTTOM,48 PIN,NYLON	80009	204-0909-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
						(ATTACHING PARTS)		
-10	211-0112-00			2		. SCREW,MACHINE:2-56 X 0.375,FLH,100 DEG	83385	OBD
						- - - * - - -		
-11	307-1153-00			1		. PASSIVE NETWORK:INTERCONNECT	80009	307-1153-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-12	175-4601-00			1		. CA ASSY,SP,ELEC:132,33 AWG,19.6 L,RIBBON	80009	175-4601-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-13	334-3753-00			1		. . MARKER,IDENT:MKD P6020	80009	334-3753-00
-14	334-3754-00			1		. . MARKER,IDENT:MKD P7020	80009	334-3754-00
	131-2749-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2749-00
-15	334-3722-00			1		. PLATE,IDENT:P6460 MICROPROCESSOR	80009	334-3722-00
-16	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-17	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-18	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-19	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
						- - - * - - -		
-20	380-0590-01			1		. HSG HALF,CKT BD:	80009	380-0590-01
-21	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-22	200-2412-00			2		. CABLE NIP,ELEC:	80009	200-2412-00
-23	175-4741-01			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L,RIBBON	80009	175-4741-01
-24	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-25	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A3 REPL)		
-26	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	----- -----			1		CKT BOARD ASSY:UPPER(SEE A1 REPL)		
-28	136-0784-00			1		. SKT,PL-IN ELEK:MICROCIRCUIT,48 PIN,ZIF	19613	248-4775520602
-29	210-1133-00			4		. WASHER,FLAT:0.142 ID X 0.058 THK,FBR	80009	210-1133-00
-30	131-0608-00			112		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-31	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-32	131-0787-00			40		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-33	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-34	131-0590-00			28		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-35	361-0998-00			4		SPACER,CKT BD:0.245 ID X 0.38 OD X 0.23 H	80009	361-0998-00
-36	----- -----			1		CKT BOARD ASSY:LOWER(SEE A2 REPL)		
-37	337-2722-00			1		. SHIELD,ELEC:ACCESS DOOR,BRASS	80009	337-2722-00
-38	131-0608-00			38		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-39	131-0993-03			1		. LINK,TERM.CONNE:2 WIRE ORANGE	00779	530153-3
	131-0993-07			4		. LINK,TERM.CONNE:2 WIRE VIOLET	00779	530153-7
-40	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-41	136-0578-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-42	136-0263-04			29		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-43	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
-44	380-0594-01			1		HSG HALF,CKT BD:BOTTOM	80009	380-0594-01

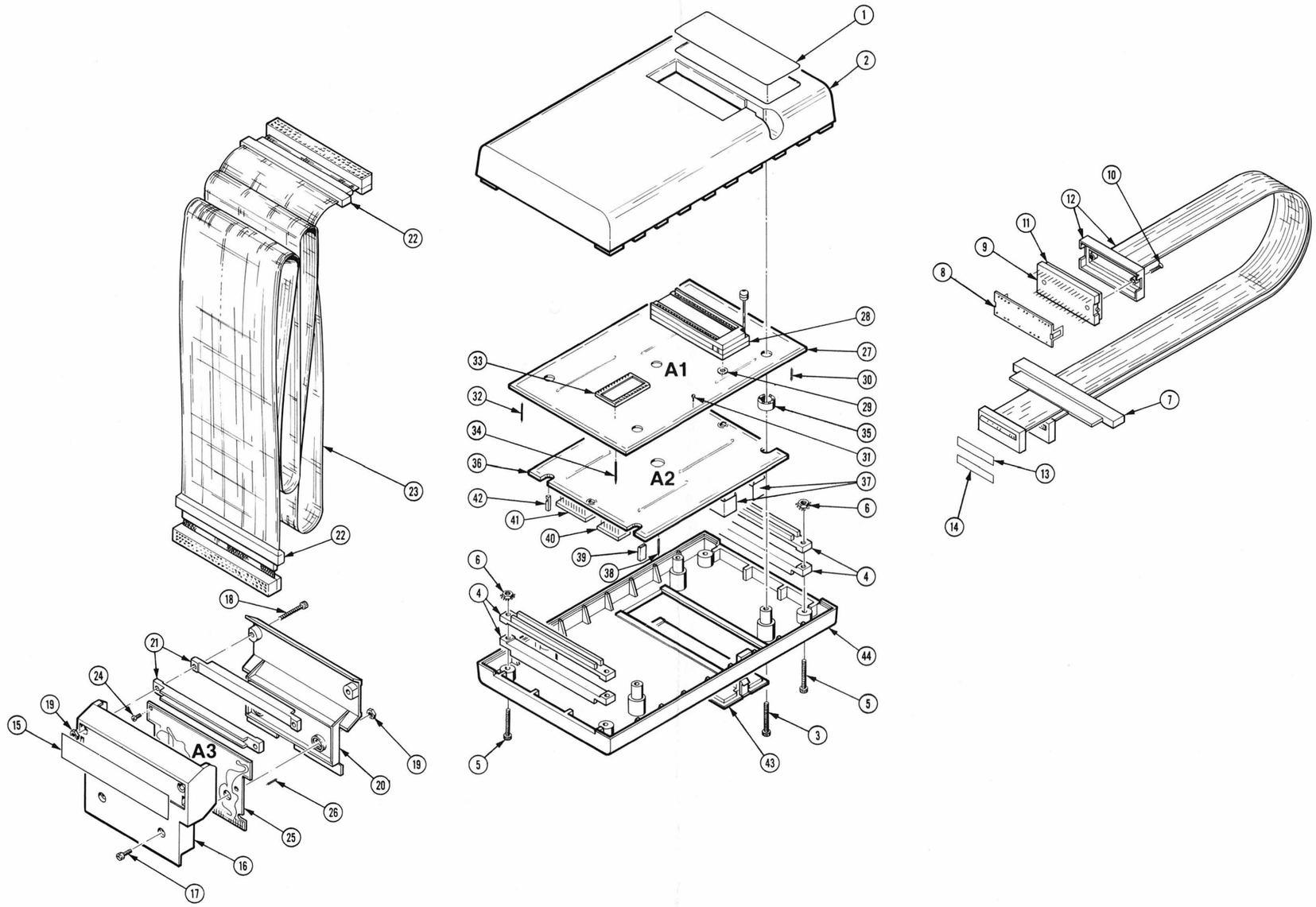


FIGURE 1 EXPLODED

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-3503-00			1		MANUAL,TECH:INSTRUCTION	80009	070-3503-00

Section 10

SIGNAL GLOSSARY

The listings which follow describe each signal line within the PM 110, including the Z8001 signal lines. For additional information, refer to the Theory of Operation section, and the Schematics and Diagrams section.

A -- Jumper A2P6041 in the Self-Test Circuitry. When this jumper is in the 1-2 position, Address 7 and Address 9 are zero.

AD0-AD15 -- Z8001 Address/Data input/output lines. These multiplexed lines are used for I/O.

AI0-AI15 -- PM 110 Address Input lines to the logic analyzer. These lines are also used to address the PROM.

$\overline{AS}$ -- Z8001 Address Strobe. The rising edge of $\overline{AS}$ indicates addresses are valid. $\overline{AS}$ occurs at the beginning of every machine cycle.

B -- Jumper A2P7010 in the Self-Test Circuitry. When this jumper is in the 1-2 position, Address 7 and Address 9 are zero.

BAS -- The buffered, inverted $\overline{AS}$ line.

BNMI -- The buffered, inverted $\overline{NMI}$ line.

BN/$\overline{S}$ -- In normal mode, this line carries the buffered Z8001 N/$\overline{S}$ bit. In I/O mode, this line defines a normal or special I/O.

BR/$\overline{W}$ -- The buffered R/$\overline{W}$ line.

$\overline{BSEG}$ -- The buffered $\overline{SEGT}$ line.

BST0 -- The buffered ST0 line.

$\overline{BST1}$ -- The buffered, inverted ST1 line.

BST2 -- The buffered ST2 line.

$\overline{BST3}$ -- The buffered, inverted ST3 line.

$\overline{BUFBUS}$ -- The buffered $\overline{BUSACK}$ line.

$\overline{BUSACK}$ -- The Z8001 Bus Acknowledge. A low on this line indicates that the CPU has relinquished control of the bus.

$\overline{BUSET}$ -- The buffered $\overline{RESET}$ line.

$\overline{BUSREQ}$ -- The Z8001 Bus Request. A low on this line indicates a

request for the bus from the CPU.

B/$\overline{W}$ -- The Z8001 Byte/$\overline{Word}$. A high on this line indicates a byte; a low indicates a word.

BWAIT -- The buffered, inverted $\overline{WAIT}$ line.

C -- The Self-Test circuit Clock testpoint A2TP7040.

CLOCK -- The Z8001 Clock Input line.

C0, ENRQ -- The buffered, encoded R/$\overline{W}$. This line is active low on Memory or I/O Writes, and low on Refresh and Interrupt Acknowledge cycles.

C1, IOMEM -- Encoded signal. High on I/O, Interrupt Acknowledge, and FETCHN. Low on Memory, FETCH1, EPA transfer.

C2, FETCH -- Encoded signal. High on Fetch and Interrupt Acknowledge, and Refresh cycles.

C3, IRQ -- Encoded Interrupt Request. High on any of the four interrupt requests.

C4, E PUMO -- The shared resource control line.

C5, BR/$\overline{W}$ -- The buffered Z8001 R/$\overline{W}$ line.

C6, BAKRI -- An encoded signal, low on Internal Operation, Refresh, and Bus Acknowledge cycles.

C7, $\overline{SUT}$ $\overline{HALTED}$ -- Encoded signal. A low indicates either the logic analyzer or the SUT has halted the Z8001.

C8, CWAIT -- The buffered, inverted $\overline{WAIT}$ request signal.

C9, CQUAL -- The encoded, active high, clock qualifier.

DI0-DI15 -- PM 110 Data Disassembly lines from the PROM to the logic analyzer.

$\overline{DS}$ -- Z8001 Data Strobe. This line is active low when valid data enters or leaves the CPU.

ECLOCK -- The ECL-level clock produced by the PM 110 for the logic analyzer.

GND -- Ground

INPUT LOOK -- The 7D02-generated line to disable the input buffers, halting the data flow from the SUT to the logic analyzer.

Signal Glossary -- PM 110 Instruction

$\overline{INT}$ -- The ANDed result of $\overline{VI}$ and $\overline{NVI}$.

INTACK -- The ANDed result of ST2 and $\overline{ST3}$, indicating an interrupt.

INTO -- The encoded interrupt acknowledge line before being buffered into C3.

$\overline{MI}$ -- The Z8001 Multi-Micro In pin, not used by the PM 110.

$\overline{MO}$ -- The Z8001 Multi-Micro Out pin.

$\overline{MOUT}$ -- The buffered $\overline{MO}$ line.

$\overline{MREQ}$ -- The Z8001 Memory Request pin. A low indicates that the address/data bus holds a memory address.

N/$\overline{S}$ -- The Z8001 Normal/$\overline{System}$ Mode pin. A high indicates Normal mode, a low indicates System mode.

$\overline{NMI}$ -- The Z8001 Non-Maskable Interrupt. A falling edge on this line requests a non-maskable interrupt.

NSIO -- The encoded output of the PM 110 Status Decoder. A low on this line indicates Special I/O.

$\overline{NVI}$ -- The Z8001 Non-vectored Interrupt. A low on this line requests a non-vectored interrupt.

QUAL -- The encoded instruction fetch signal, prior to being buffered into C9.

RESERVED -- The Z8001 Decouple pin, currently not used.

$\overline{RESET}$ -- The Z8001 Reset line. A low on this line resets the Z8001.

R/$\overline{W}$ -- The Z8001 Read/$\overline{Write}$. A high indicates that the Z8001 CPU is reading from memory or I/O. A low indicates the Z8001 CPU is writing to memory or I/O.

$\overline{SEGT}$ -- The Z8001 Segment Trap. A low indicates a segment trap request.

$\overline{SELP}$ -- The 7D02-generated PROM-enable line.

SN0-SN6 -- The Z8001 Segment outputs. This lines indicate the segment number portion of the memory address.

SNI0-SNI6 -- The buffered segment number input lines to the logic analyzer.

$\overline{\text{SRESET}}$ -- The NANDed output of SYNCA and SYNCB, which clears A2U4040.

ST0-ST3 -- The Z8001 Status active high outputs. These lines specify the Z8001 CPU status. See the table below.

Table 10-1

STATUS LINE DEFINITIONS

ST3-ST0	Definition
0000	Internal operation
0001	Memory refresh
0010	I/O reference
0011	Special I/O reference
0100	Segment trap acknowledge
0101	Non-maskable interrupt acknowledge
0110	Non-vectored interrupt acknowledge
0111	Vectored interrupt acknowledge
1000	Data memory request
1001	Stack memory request
1010	Data memory request (EPU)
1011	Stack memory request (EPU)
1100	Instruction space access
1101	Instruction fetch, first word
1110	EPU Transfer
1111	Reserved

$\overline{\text{STOP}}$ -- The Z8001 active low Stop input line.

$\overline{\text{STOP}}$ $\overline{\text{SUT}}$ -- The logic analyzer stop request line, which enables the logic analyzer to halt Z8001 operation.

STI0, STI1 -- The buffered status lines carrying interrupt decode information to the logic analyzer on AI16 and AI17.

SYNCA, SYNCB -- Part of the Self-Test reset circuitry. SYNCA and SYNCB are NANDed together to produce the $\overline{\text{SRESET}}$ line.

$\overline{\text{TCLK}}$ -- The TTL-level clock used by the PM 110.

$\overline{\text{USTOP}}$ -- The SUT stop request line to the Z8001.

$\overline{\text{VI}}$ -- The Z8001 Vectored Interrupt active low request line.

$\overline{\text{WAIT}}$ -- The Z8001 Wait request line from the SUT to the Z8001.