Tektronix
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1220/1225/1230
LOGIC ANALYZER

PM402

Z80 Microprocessor Probe

Operator's Manual

The PM402 has a software version number of 2.51. For use with the PM402, the 1220 and 1225 Logic Analyzers require software versions of 2.5 or above; the 1230 Logic Analyzer requires a software version of 3.03 or above.

Please check for change information at the back of this manual

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OVERVIEW

The PM402 Z80 Microprocessor Probe Personality Module consists of a Z80 disassembly probe (with ribbon cable) and this user's manual. This manual shows you how to connect and use the PM402 Z80 disassembly probe with the 1220/1225/1230 Logic Analyzers. This manual does not teach you how to use analyzer keypads or menus. For information on using analyzers refer to your logic analyzer operator's manual. For more information about the Z80 microprocessor, refer to your Z80 microprocessor data book.

The PM402 Version 2.51 works with 1220/1225 Logic Analyzers having software version numbers 2.5 or higher and 1230 Logic Analyzers with software version numbers 3.03 or higher. If you're using a 1220/1225 version 2.5 or higher or a 1230 version 3.03 or higher, you must use the version 2.51 PM402.

The PM402 gives you an interface from the 1220/1225/1230 Logic Analyzer to Z80-based systems under test (SUT). Along with regular analyzer features, the PM402 interface lets you sample data synchronously, use the Z80 clock, and display disassembly data in hardware and software formats.

Conventions. This manual uses these conventions:

- The term analyzer refers to the 1220, 1225, and 1230 Logic Analyzers unless otherwise specified.
- The term SUT refers to the Z80 system under test.
- Active low signals are identified by a bar over the signal name, for example, $\overline{\text{NMI}}$.

ANALYZER CONFIGURATION

You must have at least 32 channels in the 1220/1225/1230 to use the Z80 disassembly probe. This is because the probe uses 32 channels to acquire synchronous data from the Z80-based SUT. You must also use a version 2.51 PM402 if you're using a 1220/1225 version 2.5 or higher or a 1230 version 3.03 or higher. Figure 1 shows the analyzer and expansion card configuration.

CONNECTING AND POWERING UP

The Z80 disassembly probe has two probe cables that connect to the analyzer. Follow these steps to connect the Z80 probe to the analyzer. Figures 1 and 2 show how the analyzer connects to your SUT.

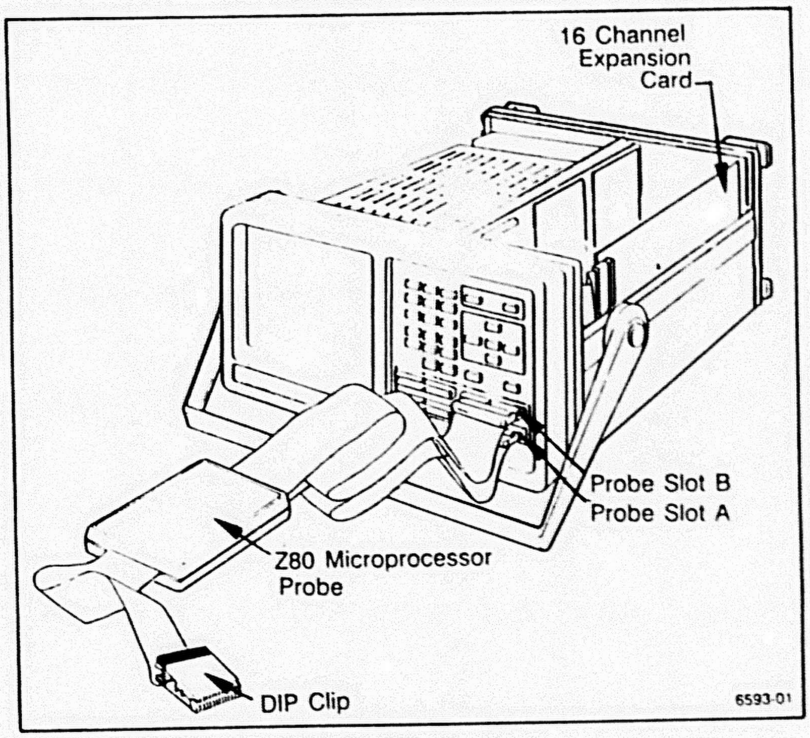

Figure 1. Analyzer configuration with probe.

1. Make sure that the power to the analyzer and SUT is off.

CAUTION

Do not connect the Z80 disassembly probe to the analyzer unless power to analyzer is off. Do not connect the Z80 disassembly probe to the SUT unless power to the SUT is off. If you connect the disassembly probe to the SUT when power to the SUT is on and power to the analyzer is off, too much power can flow through the probe's inputs and damage the probe.

2. Connect the bottom cable from the probe to input A on the front of the analyzer.
3. Connect the top cable from the probe to input B on the front of the analyzer.

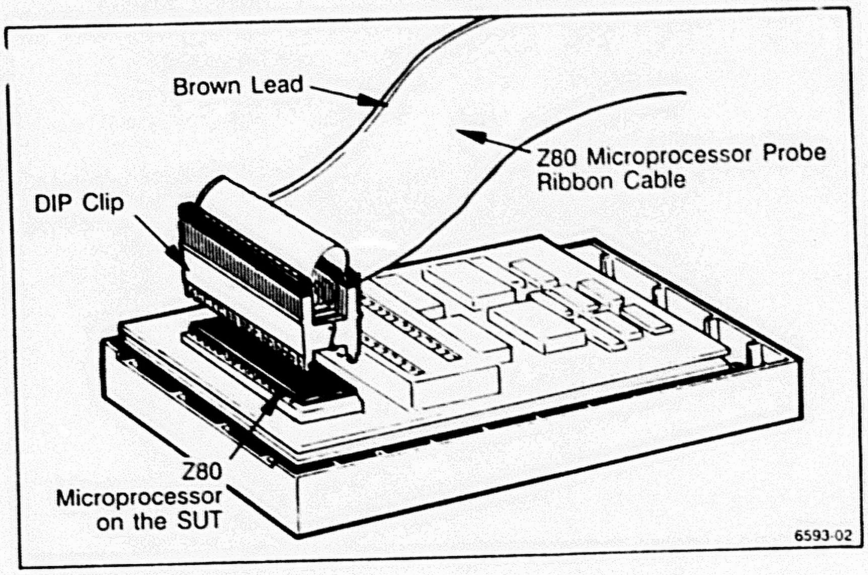

Figure 2. Connecting the DIP clip and SUT.

4. Connect the Z80 probe clip to the SUT as shown in Figure 2 (power to the SUT should be off). The brown lead goes to pin 1 on the Z80 microprocessor. Figure 3 shows the Z80 pinout, and Table 1 lists analzyer-to-Z80 signal line connections. Figure 3 and Table 1 are shown after this procedure.
5. Turn on the analyzer which also supplies power to the probe. The analyzer screen now displays the Initialization menu (Figure 4, shown after this procedure).
6. Press ENTER to upload the Z80 disassembly setup into the analyzer. Pressing ENTER overwrites the existing setup and changes probe links, channel groups, and defined conditions for Z80 disassembly. If you press MENU, the PM402 setup is not uploaded and you cannot display disassembled data; instead, the current setup is saved.
7. Turn on power to the SUT.

You can now press MENU to call up the Main menu (Figure 5), which lists setup, data, and utility features. Since the default disassembly setup defines the setup parameters for you (probe links, sampling rate and format, conditions, and so on), you can press START at any time to acquire data from your SUT. Example 1, later in this manual, shows a data acquisition with the default setup.

Signal Name	Z80 Pin Numbers		Signal Name
A11	1	40	A10
A12	2	39	A9
A13	3	38	A8
A14	4	37	A7
A15	5	36	A6
0	6	35	A5
D4	7	34	A4
D3	8	33	A3
D5	9	32	A2
D6	10	31	A1
+5V	11	30	A0
D2	12	29	GND
D7	13	28	/RFSH
D0	14	27	/M1
D1	15	26	/RESET
/INT	16	25	/BUSRQ
/NMI	17	24	/WAIT
/HALT	18	23	/BUSAK
/MREQ	19	22	/WR
/IORQ	20	21	/RD

6593-03

Figure 3. Z80 pinout.

Table 1
Z80 Signals and Analyzer Channels

Z80 Signals	122x/1230 Channels	Channel Groups	Description
A15-A00	B15-B00	ADD	Address bus
D07-D00	A15-A08	DAT	Data bus
$\overline{MREQ}$	A04	STB	Strobes
$\overline{IOREQ}$	A03		
$\overline{M1}$	A02		
$\overline{RD}$	A01		
$\overline{WR}$	A00		
$\overline{NMI}$	A07	INT	Interrupts
$\overline{INT}$	A06		
$\overline{HALT}$	A05		

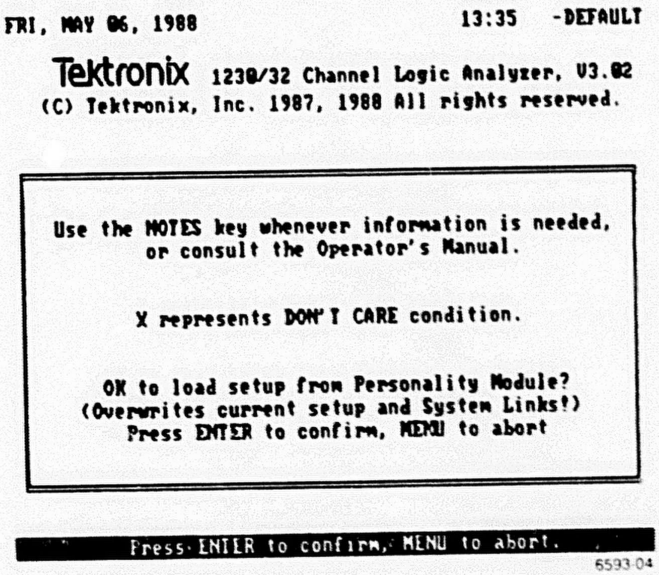

Figure 4. Initialization menu. When you turn the analyzer on with the PM402 plugged in, the Intialization menu includes a message telling you that you can now upload the disassembly setup by pressing ENTER.

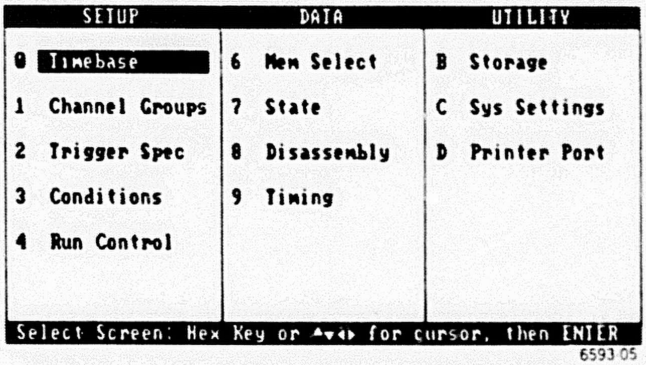

Figure 5. Main menu. The Main menu always shows disassembly as a menu selection. However, you can display acquired data in disassembly format only when the PM402 is plugged in. As long as the channel groups are in the default definitions and the acquisition memory is valid, you can display valid disassembly data.

Loading Disassembly Setups. You don't have to upload the disassembly setup when you see the Initialization menu. However, if you don't, you must enter the disassembly setup manually or reset the analyzer so that the PM402 can upload the disassembly setup for you. You can reset the analyzer by pressing NOTES and ENTER firmly at the same time.

Using Probes

The Z80 disassembly probe must always be plugged into slots A and B on the analyzer front panel. If you have a 1225 or 1230 Logic Analyzer, you can use slots C and D for acquisition probes.

You don't have to unplug an acquisition probe to use the disassembly probe. If you want to use an acquisition probe but not the disassembly probe, you don't have to unplug the disassembly probe. You can always run the trigger specification on either timebase.

The probe in slot A must always be connected to the clock in your SUT. If the probe in slot A is not connected to your SUT clock, the analyzer won't trigger when you press START. If you're using more than one probe and the probes are linked synchronously, each probe must be connected to the same clock point in your SUT.

Using the Menus and Cursor

The PM402 is controlled by selections you make in the analyzer's menus. You can always call up the Main menu by pressing MENU.

You don't have to specify the Z80 when you select disassembly information from the Main menu. The analyzer looks at the probe inputs to find out that the Z80 probe is connected. For more information about using the menus and cursor, refer to your logic analyzer operator's manual.

Online Help

At the bottom of the disassembly screen, a one-line help message tells you which keys to press for disassembly functions. If you need more help, press NOTES. The analyzer then displays in-depth information about Z80 disassembly, including the disassembler's software version number. You can press MENU at any time to exit the help and return to the previous display.

SETTING UP TO ACQUIRE DATA

This discussion shows you how the PM402 sets up the analyzer for Z80 disassembly. The setups shown here are for an analyzer with 32 channels. Example 1, later in this manual, shows a data acquisition using this 32-channel default setup.

A setup is a set of parameters that describes the current analyzer configuration for data acquisition and storage. For example, the setup includes information about probe links, acquisition rates, glitch capture, threshold voltage, and Z80 trigger conditions.

Timebase

The acquisition timebase, probe links, glitch capture, and threshold voltage for Z80 disassembly are shown in Figure 6. If you're using a 1230, the PM402 uses the synchronous clock rate of your SUT. If you're using a 1220 or 1225, the PM402 is set up for synchronous acquisition at 100 ns.

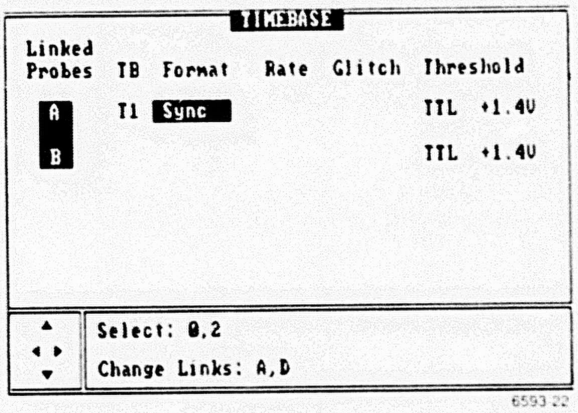

Figure 6. Timebase menu.

Probe Links. The Z80 probe is a 32-channel disassembly probe which uses probe slots A and B. For Z80 disassembly, probes A and B are linked together in the same timebase so that all disassembly is done with the same acquisition format and rate. If you're also using one or more acquisition probes, the acquisition probes are linked asynchronously in T2.

Clocking. The default disassembly clock format is synchronous so that you use the clock rate in your SUT as the data sampling rate. The Z80 disassembly probe automatically qualifies your SUT clock with software internal to the probe. There are no external clock qualifiers for the Z80 disassembly probe.

For the 1230, the clock rate is set by your SUT. For the 1220/1225, the clock rate is set to $\leq$100 ns by default. For Z80 disassembly, you must use a clock rate of $\leq$100 ns if you're using a 1220/1225.

Glitch Capture. The Z80 disassembly probe does not acquire glitches. When you turn glitch capture on, the upper eight channels are deleted from each channel group. Because the Z80 probe is a 32-channel probe, if you turned glitch capture on for disassembly, the analyzer would wait for data to appear on the missing channels. The analyzer would not be able to complete an acquisition.

Channel Grouping

The PM402 sets up the analyzer's channel groups as shown in Figure 7. The Channel Grouping menu shows how the channel groups are named; for example, ADD for the address bus. The control lines are separated into two channel groups: strobe lines and interrupt lines.

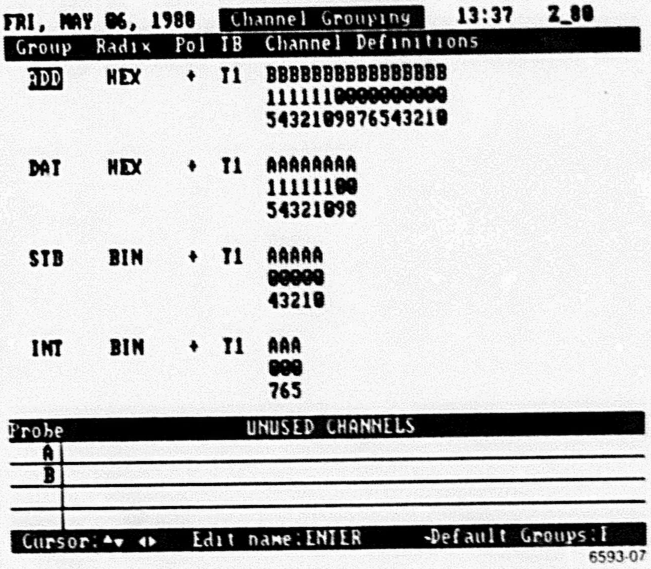

Figure 7. Channel Grouping menu.

Trigger Conditions

The Conditions menu lets you define data conditions which the analyzer can recognize and trigger on. When you upload the Z80 setup, the Z80 input signals are grouped to correspond to the analyzer channels as listed earlier in Table 1. The conditions listed in Table 2 show the logic states corresponding to Z80 operations.

Table 2
Z80 Cycle Types and Analyzer Conditions

Signal Line	ADD hex	DAT hex	STB bin	INT bin
OPC FET	X X X X	X X	0 1 0 0 1	X X 1
MEM READ	X X X X	X X	0 1 1 0 1	X X 1
MEM WRIT	X X X X	X X	0 1 1 1 0	X X 1
I/O READ	X X X X	X X	1 0 1 0 1	X X 1
I/O WRIT	X X X X	X X	1 0 1 1 0	X X 1
INT ACK	X X X X	X X	1 0 0 0 1	X X 1
RESET	0 0 0 0	X X	X X X X X	X X X
NMI	X X X X	X X	X X X X X	0 X X
IRQ	X X X X	X X	X X X X X	X 0 X
HALT	X X X X	X X	X X X X X	X X 0

All signals are sampled synchronously with a Z80 machine cycle, except for $\overline{\text{NMI}}$ (nonmaskable interrupt). An $\overline{\text{NMI}}$ can occur anytime. If an active $\overline{\text{NMI}}$ occurs for at least 70 ns, the $\overline{\text{NMI}}$ signal is stored in memory. When you display disassembly information in hardware mode, the $\overline{\text{NMI}}$ condition is then included in the listing on the screen. For example, Figure 12 shows an $\overline{\text{NMI}}$ condition.

Figure 8 shows the Conditions and Trigger Spec menus. The trigger statement shown in the figure is for a 1230. If you're using a 1220/1225, the default trigger action is START instead of TRIG.

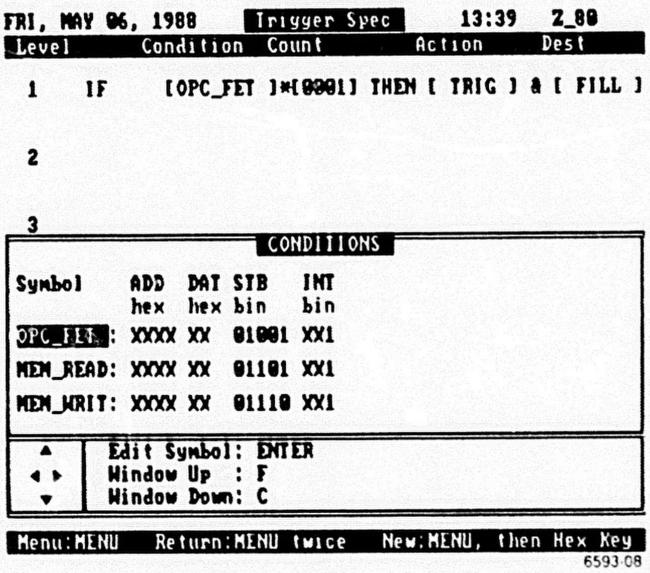

Figure 8. Conditions and Trigger Spec menus. The default condition window is large enough to show three of the defined conditions. Table 2 lists all signals/conditions defined for the Z80 probe. The default trigger statement is an if-then statement with the first condition, OPC FET, as the trigger condition. For the 1230, the trigger action is TRIG. For the 1220/1225, the trigger action is START.

Trigger Specification

The default trigger statement is an if-then statement. At initialization, the analyzer is set to trigger and fill when the condition OPC FET occurs. Figure 8 shows the Trigger Spec menu along with the Conditions menu.

Run Control

When you initialize the analyzer the Run Control menu is set up as shown in Figure 9. The default display for acquired data is a disassembly display. The trigger position is set at memory location 1024, and the analyzer looks for the trigger after the pretrigger memory is full.

The Run Control menu also sets the memory-compare mode to Manual and tells you that the default channel mask for comparing memories is OPC FET, which is also the default trigger condition. A window (or viewport) at the bottom of the screen lists the value for OPC FET. Remember that channels set to X (don't care) are masked, or not compared, during a memory comparison.

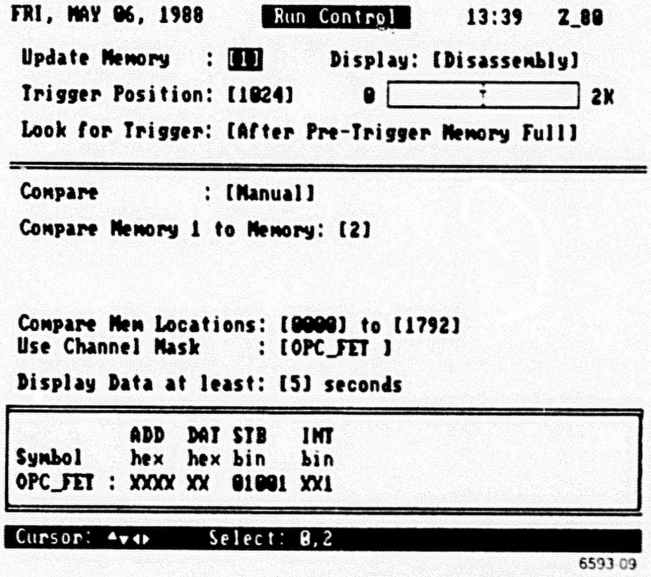

Figure 9. Run Control menu.

SETTING UP TO DISASSEMBLE CODE

Once you've set up the analyzer for disassembly, you can start to acquire and display data from your SUT. Your logic analyzer operator's manual tells how to display data in state and timing formats. This discussion shows you how to display disassembled Z80 data, which you can do only when the PM402 is connected to the analyzer.

Regardless of how you set up timebases and channel groups, the Z80 disassembly probe will display disassembly data for your SUT. As long as the acquisition memory is valid and the channel groups are set to the default Z80 setup definitions, the disassembly display is also valid.

Disassembly Mnemonics. The PM402 lets you display acquired data in disassembly mnemonics. Disassembly mnemonics are assembly-language instructions that have been disassembled from a machine language program. For example, Z80 disassembly mnemonics include RET, OR, NOP, CALL, JP, and DEC. An actual disassembly line might read DEC DE, which means 'decrement the DE register pair.' Figure 10 shows an example of disassembly mnemonics.

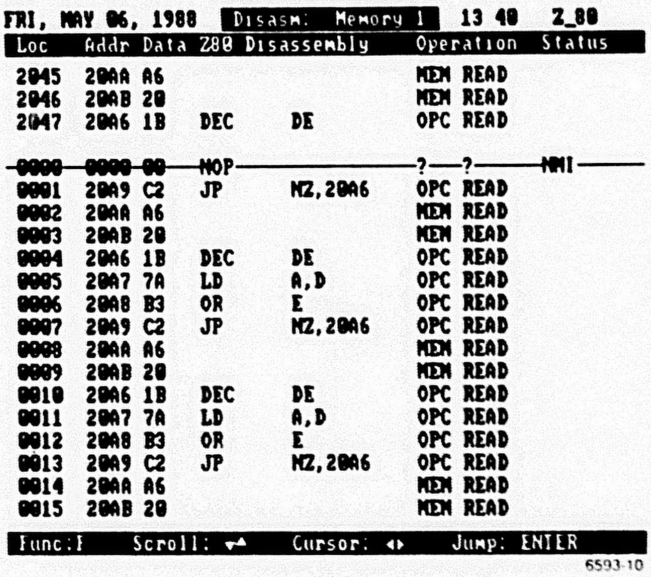

Figure 10. Disassembly mnemonics in hardware mode. In this hardware disassembly display, the cursor marks the beginning of memory. The blank line separates the beginning and end of memory. The question marks indicate an invalid opcode. Figure 11, later in this manual, shows a software display that corresponds to this figure.

Invalid Opcodes. If the analyzer finds an invalid opcode, the analyzer puts a question mark in the operation column. An invalid opcode occurs when the analyzer doesn't have enough information to completely disassemble the instruction. Figure 10 shows an invalid opcode occurring at the beginning of memory.

Searching for Events. Searching for events in the Disassembly menu works the same as searching for events in the State Table. Press 0 or 2 to cycle through the available conditions (including the beginning and end of acquisition and the trigger event). Press 1 to do the search.

When the analyzer finds the search event, it redraws the disassembly screen so that the cursor is in the middle of the screen on the search event. If you searched for an event that did not occur, the analyzer displays the message Not Found. One of the menu bars at the bottom of the screen lists the current search event. For more information about searching, refer to your logic analyzer operator's manual.

The analyzer can display and search for opcode fetches in software mode. However, since memory reads and writes are suppressed in software mode, the analyzer cannot display those instructions if you try to search for them. If you're using software mode and search for an event that is not an opcode fetch, the analyzer displays the instruction where the previous search event occurred instead.

Displaying in Hardware or Software Mode. With the Z80 disassembly probe attached, you can display disassembled data in hardware or software mode. In hardware display mode, the analyzer shows all bus operations and displays every acquired cycle. In software display mode, the analyzer shows only instructions; reads and writes are suppressed so that the display looks like an assembly listing. You can toggle between display modes by pressing DON'T CARE.

Using the Hardware Display Mode

For disassembly displays in hardware mode, the analyzer displays each sample location with address and data from the Z80 bus cycle. Disassembled instructions are displayed at the beginning of each valid machine cycle. Figure 10, earlier in this discussion, shows a hardware disassembly display.

In the displays, the Loc column shows memory locations. The Addr column shows the address, while the Data column displays acquired data. When the PM402 recognizes the beginning of an instruction, the analyzer disassembles that instruction and displays it in the middle column.

The Operation column displays the decoded cycle types $\overline{MREQ}$, $\overline{IORQ}$, and $\overline{M1}$ as bus operations OPC, MEM, INT, and I/O. This column also displays valid $\overline{RD}$ and $\overline{WR}$ cycles. Applicable bus operations are displayed in the order they occur; for example, an OPC READ and then a MEM WRITE.

The last column displays the status of interrupt lines. In the Status and Operation columns, the interrupt with the highest priority is listed. For example, if an $\overline{NMI}$ and $\overline{HALT}$ occur at the same time, the $\overline{NMI}$ signal is listed in the display. Table 3 lists interrupt priorities.

Table 3
Active Interrupt Priorities

Active Line	Description
NMI	Nonmaskable interrupt
INT	Interrupt
HALT	Halt

Pressing DON'T CARE while in the hardware display mode toggles the disassembly screen to the software display mode, and vice versa.

Using the Software Display Mode

The software display mode is useful because it displays only instructions – memory reads and writes are suppressed. The display resembles an assembly or program listing because it shows only one opcode fetch per line and each line must be the start of an instruction sequence. Because of this, the locations displayed are not contiguous. Figure 11 shows a software disassembly display.

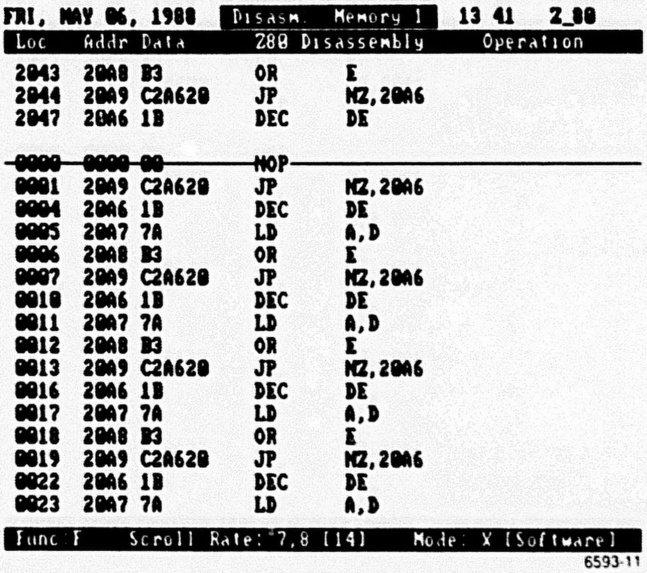

Figure 11. Software disassembly display. This display corresponds to the hardware disassembly shown in Figure 10. Press DON'T CARE to toggle from software to hardware display mode.

The Data column displays bytes that make up the opcode and also displays any data fetches for the instruction. The Operation column lists the bus operations for the instruction sequence. For each instruction cycle, the analyzer uses the Operation column to tell you the memory address and I/O activity for that cycle. In this column, the address is displayed on the left of the equals sign; data is displayed on the right. Figure 13 under *Examples* shows address and data information.

Searching for Events. You can search for events in the software disassembly display the same as you search for events in the State Table. However, because memory reads and writes are suppressed, if you search for an event that occurs on a memory read or write cycle, the analyzer searches instead for the previous fetch, displaying that instruction on the screen. To search for a memory read or write, press DON'T CARE to toggle to hardware mode, select the search event, and then press 1 to search.

When you press DON'T CARE to switch display modes, the analyzer goes through memory to find the opcode fetch closest to the cursor position. When it finds the opcode fetch, the analyzer displays the disassembly in software mode with the cursor in the middle of the screen. If it can't find an opcode fetch, the analyzer returns to hardware mode:

EXAMPLES

These three examples show you how to acquire data for disassembly, display the data in hardware and software mode, and cross-trigger the disassembly probe from a different timebase (using an acquisition probe).

The first example uses the default setup for a simple acquisition. In the second example, you define specific conditions on which you want to trigger. The third example uses 48 channels to cross-trigger the Z80 disassembly probe from the timebase used by an acquistion probe.

Example 1. A Simple Acquisition

This example uses the default Z80 setup uploaded when you connected the analyzer to an SUT and initialized the analyzer. This example shows you how to:

- acquire and disassemble data
- jump to a specific location
- search for a particular event
- toggle between display modes.

Follow these steps to make a simple acquisition and begin manipulating data.

1. Make sure the analyzer is connected to your SUT and the analyzer is initialized with the default disassembly setup.
2. Press START to acquire data. The Acquisition Process screen is displayed, telling you the status of the acquisition. When the acquisition is complete, the analyzer stops and displays the data in a timing diagram since that is the default data format.

3. Press MENU, then 8 to call up the Disassembly menu and display the acquired data in disassembly format. Figure 12 shows the hardware display mode for the disassembly data.

4. Press DON'T CARE to toggle to software display mode. When you switch disassembly modes, the analyzer goes through memory to find the opcode fetch closest to the cursor. If it can't find an opcode fetch, it will return to hardware mode. Figure 13 shows the corresponding software display mode.

5. Press ENTER to tell the analyzer you want to enter a new location to be displayed, then enter 0000 to jump to the beginning of memory. As you finish entering the digits, the analyzer jumps to the selected memory address and displays the new information.

6. Press 0 or 2 to cycle through available search functions till you choose the trigger for the search event.

7. Press 1 to search for the trigger. Figures 12 and 13 show the trigger event in hardware and software modes.

The scroll rate, jump, and search features for disassembly displays work the same as they do in the State Table. For more information about these features, refer to your logic analyzer operator's manual.

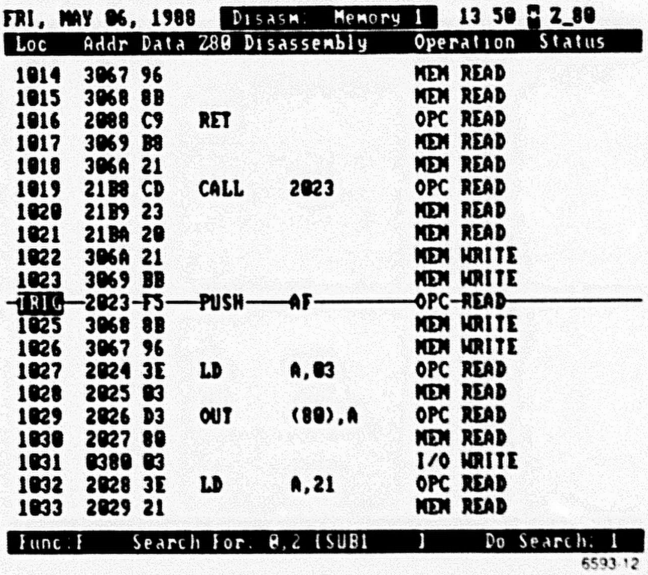

Figure 12. Hardware disassembly display. The search event in this example is the trigger event, which occurred at memory location 1024 as specified in the Run Control menu.

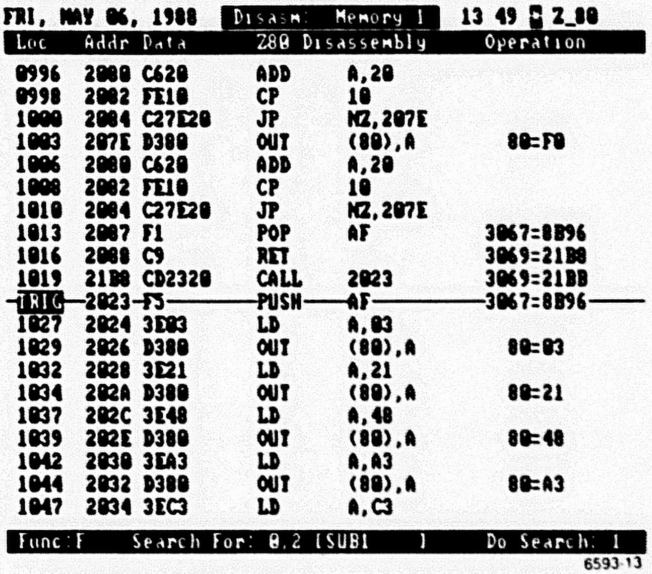

Figure 13. Corresponding Software disassembly. Because the search event was not a memory read or write, the software disassembly display (corresponding to the hardware display shown in Figure 12) shows the trigger event at the cursor. The Operation column shows the address (left side of equals sign) and data information for the instructions that occurred.

Example 2: Trigger on a Subroutine

This example shows you how to acquire specific data. In this example, a subroutine is generating an $\overline{\text{NMI}}$ signal at address 0066. You want to acquire the subroutine, then look at what happens after the subroutine to find out why it's generating the $\overline{\text{NMI}}$. You need to define three conditions: the beginning of the subroutine (address 2023), the end of the subroutine (address 2050), and the $\overline{\text{NMI}}$ condition (address 0066 and Z80 interrupt value 0XX).

This example uses the default setup except for defined conditions and trigger statements. You don't need to change the timebase, channel grouping, or run-control information from

the default 32-channel setup for this example. Follow these steps to trace a subroutine and trigger on a resulting $\overline{NMI}$ signal.

1. In the Conditions menu, change the NMI condition word so that the analyzer triggers on an $\overline{NMI}$ only if it occurs at the address 0066. Figure 14 shows the new NMI condition word definition: 0066 XXXX XXXXX 0XX.
2. Add two new conditions: SUBBEG and SUBEND.
3. Define SUBBEG to have a hexadecimal address of 2023 (the beginning of the subroutine)and SUBEND to have a hexadecimal address of 2050 (the end of the subroutine)Figure 14 shows the new condition words, and also shows that the values for the data and control buses of both condition words are don't cares.
4. In the Trigger Spec menu, define three levels of if-then trigger statements as shown in Figure 14.
5. Press START. The analyzer acquires occurrences of the subroutine, filling memory when the $\overline{NMI}$ occurs. Figures 15 and 16 show the hardware and software disassembly for this example.

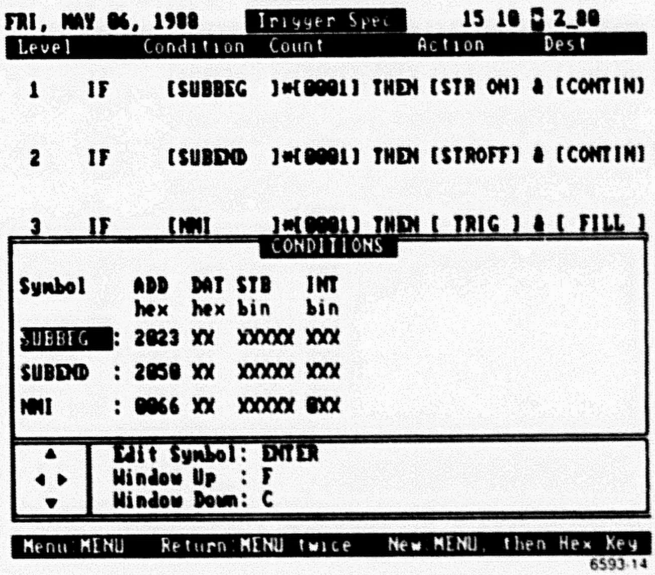

Figure 14. Subroutine and NMI setup. The two new conditions define the beginning and end of the subroutine you're tracing. The $\overline{\text{NMI}}$ condition is changed so that the analyzer will trigger on $\overline{\text{NMI}}$ only if $\overline{\text{NMI}}$ occurs at address 0066. The three-levels of trigger statements tell the analyzer to store everything between the beginning and end of the subroutine, and trigger on the $\overline{\text{NMI}}$.

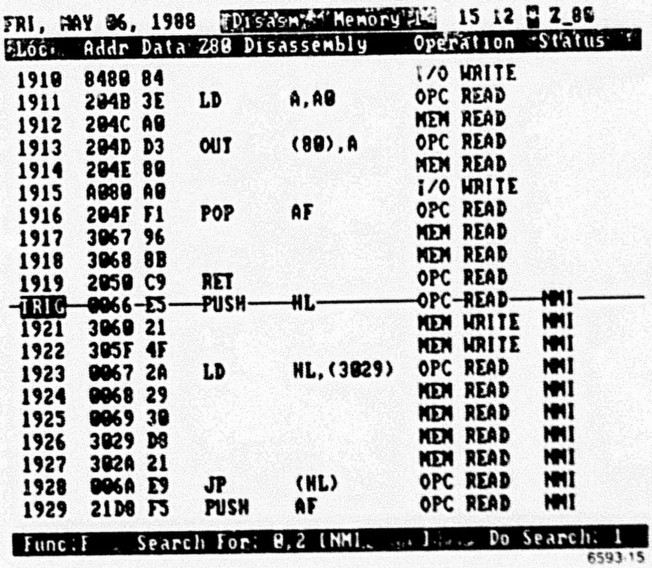

Figure 15. Hardware display with NMI condition. The cursor marks the search event, NMI, which occurred at address 0066 after the subroutine finished (address 2050 at analyzer memory location 1919). The hardware display mode shows each memory read and write that occurred during the subroutine.

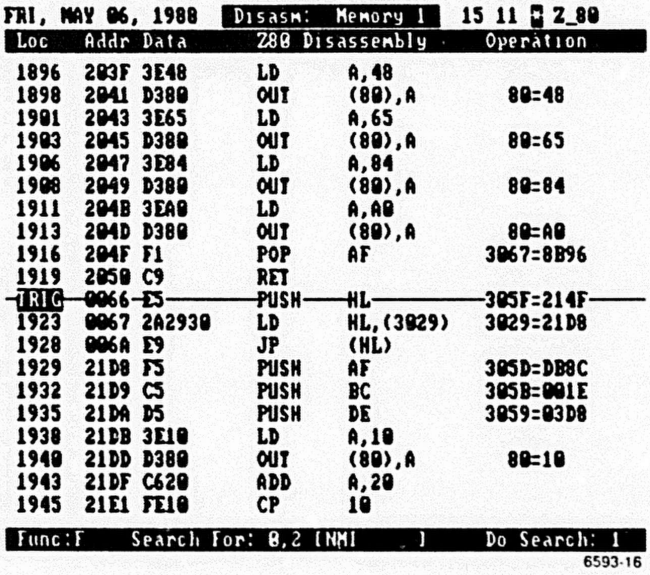

Figure 16. Software display with NMI condition. You can show the search event, NMI, in software mode by pressing DON'T CARE. You can see the subroutine sequence in a more compact form in software mode since only one instruction is displayed for each bus operation.

Example 3: Cross-Triggering

If you're using a 1225 or 1230 Logic Analyzer, you can acquire data on 16-channel acquisition probes at the same time you use the Z80 disassembly probe. You can also set the Z80 probe to trigger off the acquisition probe, or vice versa. This example shows you how to set up the Z80 probe to trigger off the acquisition probe.

Configuration. This example uses a 1225/1230 with 48 channels. The Z80 disassembly probe is still plugged into probe slots A and B. The 16-channel acquisition probe (P6443 or P6444) is plugged into probe slot C.

What This Example Shows. This example shows how to set up an acquisition probe to trigger on a condition, then set up the disassembly probe to automatically cross-trigger and show the acquired information in disassembly display. In this example, you want to know what will happen to your code if a particular I/O port receives a write signal from an external

device. You trigger the acquisition probe on a write from an external device to the I/O port. The analyzer then automatically cross-triggers the disassembly probe so that you can display the disassembly data for that acquisition.

Figures 17 through 20 show the setup menus for this example. The menus show how to set up the 1225/1230 with these parameters:

- Probes A and B are in T1; probe C is in T2.
- Channel group GPE is renamed to EXT and contains (for simplicity) all 16 channels from probe C.
- The trigger condition EXT I/O is defined for the external write to the I/O port.
- The trigger timebase is T2 (the acquisition probe) so that the 1225/1230 recognizes the trigger condition EXT I/O and automatically cross-triggers the disassembly probe when EXT I/O occurs.

The Steps for Cross-Triggering. Follow these steps to cross-trigger the Z80 probe off the acquisition probe and search for the trigger event in the resulting disassembly display.

1. In the Timebase menu, link probes A and B in timebase T1 (separately from probe C, which should be in T2). Refer to Figure 17.
2. In the Channel Grouping menu, scroll to channel group GPE and change the channel group name to EXT. Refer to Figure 18.
3. In the Conditions menu, define a condition EXT I/O to the value of the WRITE signal, in this case, 15FF. Figure 17 shows the Trigger Spec menu and the value of the trigger condition EXT I/O.
4. In the Trigger Spec menu, set the trigger condition to EXT I/O. Figure 19 shows the Trigger Spec menu.
5. Look at the menu bar at the bottom of the Trigger Spec menu, and press D to toggle the trigger timebase to T2. Refer to Figure 19.

6. In the Run Control menu, make sure the 1225/1230 looks for the trigger EXT I/O after the pretrigger memory is full. The default data display format should still be set to Disassembly. Refer to Figure 20.
7. Press START. The 1225/1230 acquires data in both timebases, fills memory, and stops. The disassembly screen is displayed. Figure 21 shows a sample disassembly display.
8. Press 0 or 2 to cycle through available search events until you select Trigger, then press 1 to locate the trigger. Figure 21 shows the trigger event in a hardware disassembly display.

Once you've made the acquisition, you can call up state, disassembly, and timing displays for the acquired data. Since you used two timebases to make the acquisition, you can toggle each display to see what happened in T2 on the acquisition probe, then what happened in T1 on the disassembly probe.

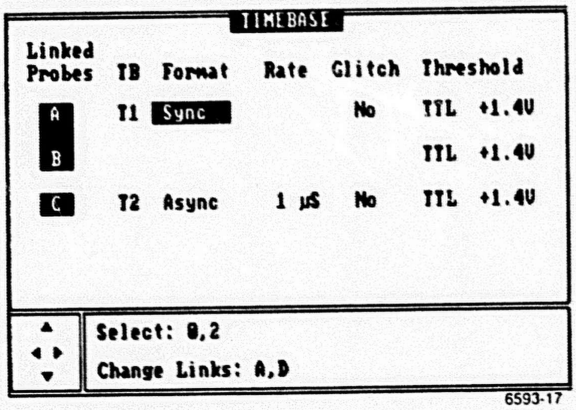

Figure 17. Timebase for cross-trigger. Probes A and B (the Z80 disassembly probe) are linked in T1, and probe C (the acquisition probe) is in T2. This lets you cross-trigger the disassembly probe on the data acquired in T2.

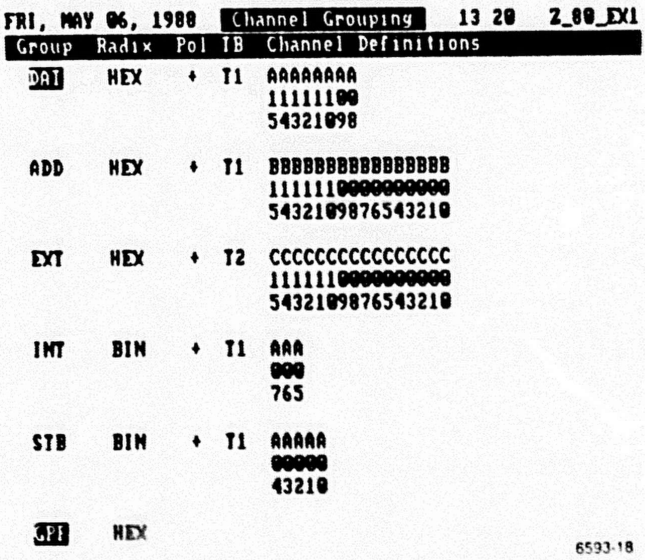

Figure 18. Channel Grouping for cross-trigger. The analyzer screen shows only four channel groups at a time. This figure is two combined screens so you can see all six channel group definitions. The channel group shows that the fifth channel group is renamed to EXT and contains all 16 channels for the acquisition probe (timebase T2).

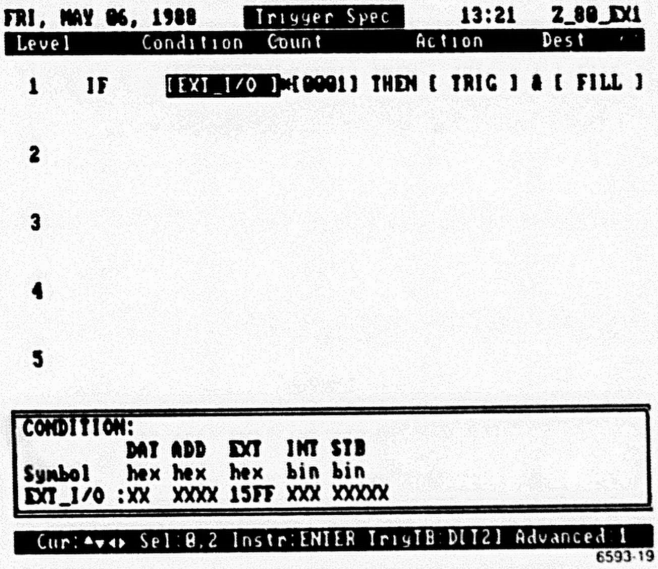

Figure 19. Conditions and Trigger Spec for cross-trigger. The trigger condition EXT I/O is defined as the value of the external WRITE signal to the I/O port. The menu bar at the bottom of the Trigger Spec screen shows that the trigger timebase is T2.

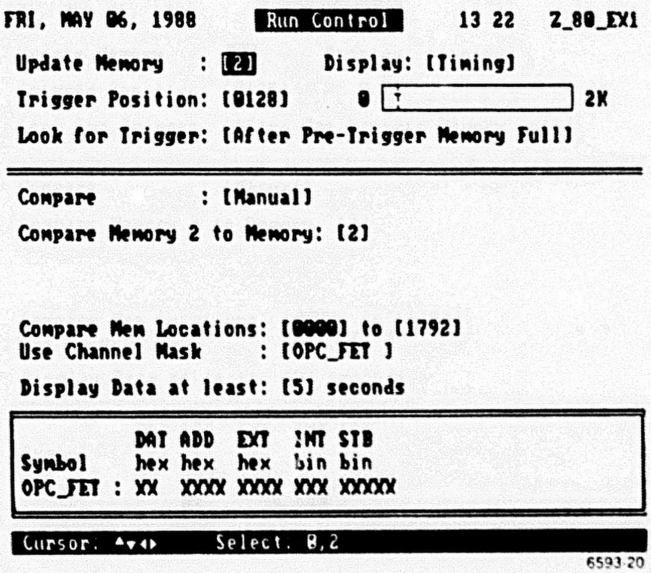

Figure 20. Run Control for cross-trigger. The 1225/1230 looks for the trigger after the pretrigger memory is full. When the pretrigger memory is full, the analyzer cross-triggers the disassembly probe (A and B) and fills the rest of memory. When the trigger condition EXT I/O is found, the analyzer stops and displays the acquired data in disassembly format.

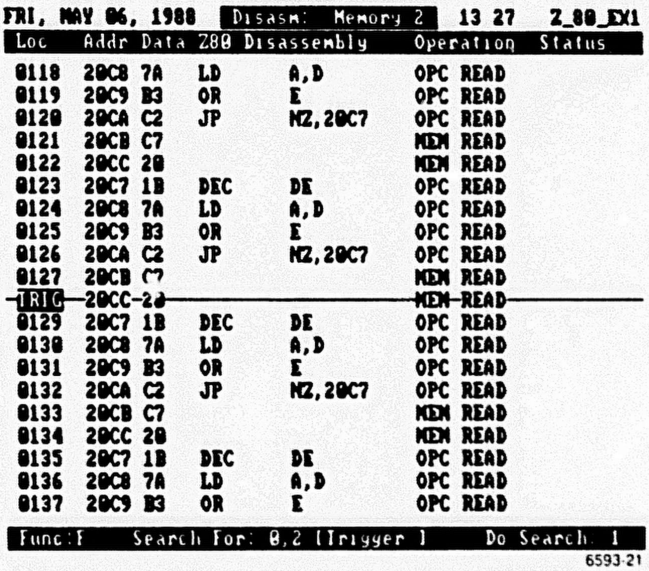

Figure 21. Hardware disassembly display. The cursor marks the location of the trigger event EXT I/O.