NUCLEAR INSTRUMENTS AND METHODS 66 (1968) 246–252; © NORTH-HOLLAND PUBLISHING CO.

INDUCTANCE EFFECTS ON CAPACITIVE LOADING OF A TUNNEL DIODE

J. E. MORRIS

Department of Electrical Engineering, University of Saskatchewan, Saskatoon, Canada

and

Z. C. TAN and J. B. EARNSHAW

Department of Physics, University of Auckland, Auckland, New Zealand

Received 10 September 1968

The switching analysis of a tunnel diode with a parallel capacitive load is extended to include the cases of stray tunnel diode and lead inductance. Computed and experimental waveforms are presented and these are discussed using simple analytical models. Some applications of the capacitively loaded tunnel diode are briefly described.

1. Introduction

The uses of tunnel diodes (td) in modern electronics as memory elements, pulse shapers, discriminators, scalers, etc. have been extensively described in the literature of the last ten years. Scant consideration has been given, however, to the uses of a td with a capacitive load.

This paper will briefly describe the switching of a capacitively loaded td and some practical applications of capacitive loading. The effects of parasitic inductances are described with the aid of computed and practical waveforms[1]). It is shown that there are two distinct oscillation modes which the circuit designer must consider.

The equivalent circuit of the tunnel diode[2]) used in the analysis is shown in fig. 1. The following differential equations which describe the behaviour of the circuit of fig. 1 are solved by the Runge-Kutta method[3]) of solution using an IBM 1620 digital computer:

$$dv_j/dt = (i_T - i_j)/C_j,$$
$$di_T/dt = (v_1 - v_j)/L_T,$$
$$dv_L/dt = i_L/C_L + (v_T - v_L)R_L/L_L,$$
$$di_L/dt = (v_T - v_L)/L_L,$$
$$v_T = \{(L_L L_T dI_{in}/dt) + L_L v_j + L_T v_L\}/(L_L + L_T).$$

The static characteristic curve $(i_j - v_j)$ of the td is shown in fig. 2 and this curve is approximated by 65 linear segments for the computation. The junction capacitance C_j at the junction voltage v_j was calculated from the standard equation

$$C_j = C_v(V_d - V_v)^{\frac{1}{2}}/(V_d - v_j)^{\frac{1}{2}},$$

where V_d is the diffusion voltage and C_v is the junction capacitance at the valley voltage V_v. For all theoretical results presented C_v is 20 pF.

Experimentally, td and load currents were displayed on the Tektronix 661 oscilloscope by means of the CT-1/P6040 current probe, and voltages with the 500 Ω P6034. The input waveform has a 5 ns rise time, (cf the td switching time about 2 ns).

2. Simple capacitive loading (R_L=0 Ω, L_L=L_T=0 nH)

Fig. 3a shows calculated switching waveforms demonstrating the wellknown increase in rise time and delay time with load. Assuming $C_j \approx C_v$, it is clear that the simple case is equivalent to unloaded switching with junction capacitance $(C_v + C_L)$. Switching times, then, are proportional to $(C_v + C_L)$. The load pulse height/half width ratio is thus approximately proportional to $C_L/(C_v + C_L)^2$ and is a maximum for $C_L = C_v$ (fig. 3b). The switching trajectories, $(i_T - v_T)$, in the $i_j - v_j$ plane, are shown in fig. 3c.

An immediate application of capacitive loading is an approximate method of measuring td valley capacitance. A slow ramp trigger current is used and the td voltage rise time is plotted against load capacitance, C_L. If the rise time without load is t_{r0}, the rise time is $2t_{r0}$ when $C_L = C_v$.

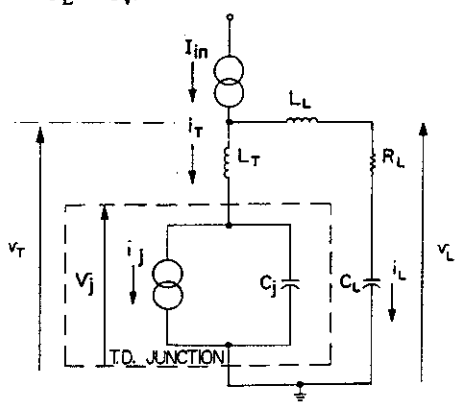

Fig. 1. General circuit for computations.

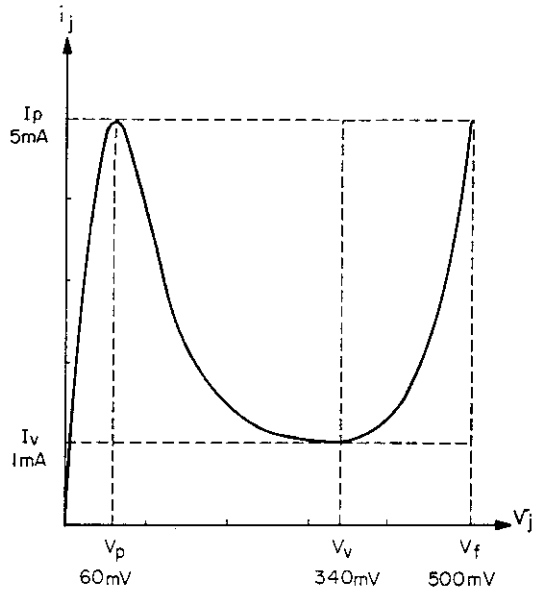

Fig. 2. Static characteristic of tunnel diode junction.

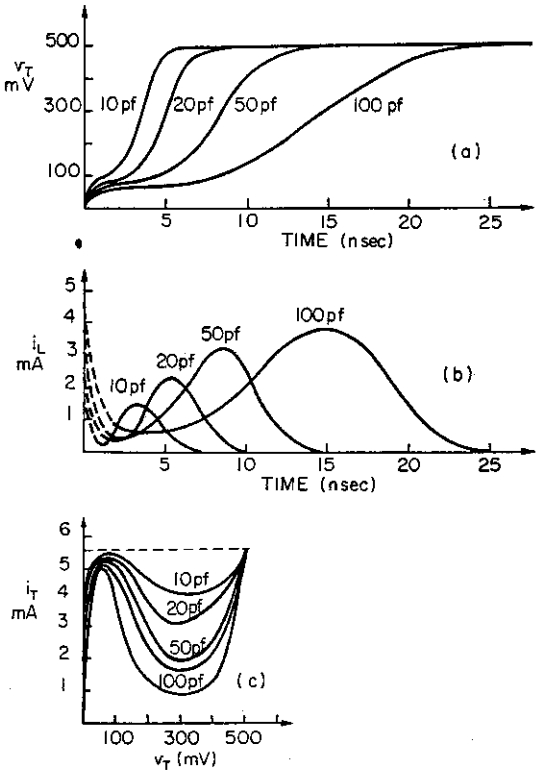

Fig. 3. Simple capacitive loading ($L_L = L_T = 0$ nH, $R_L = 0\,\Omega$, $I_{in} = 5.5$ mA step, $C_L = 10, 20, 50\ 100$ pF).
(a) voltage transients; (b) load currents; (c) switching trajectories.

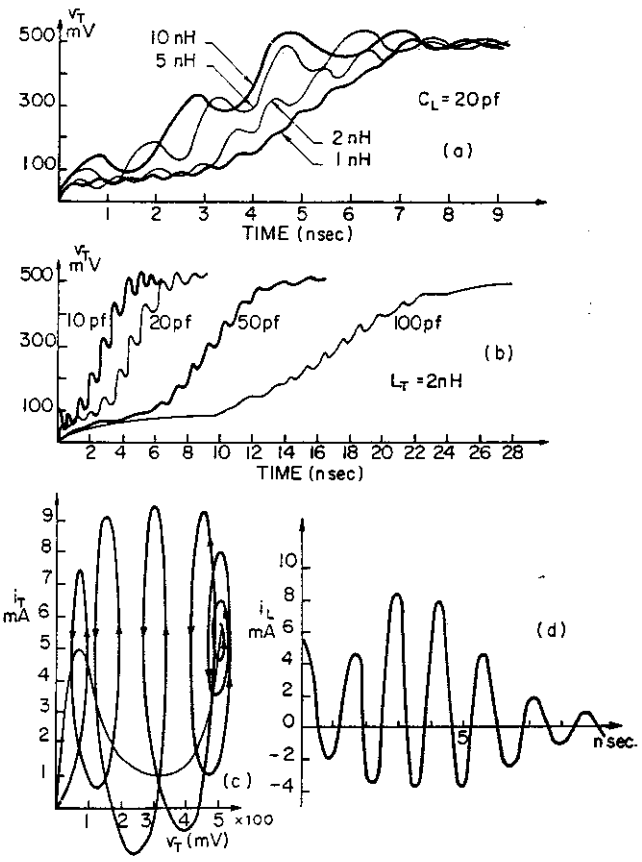

Fig. 4. Switching with finite tunnel diode inductance.
($L_L = 0$ nH, $R_L = 0\,\Omega$, $I_{in} = 5.5$ mA step).
(a) voltage transients ($C_L = 20$ pF, $L_T = 1, 2, 5, 10$ nH);
(b) voltage transients ($L_T = 2$ nH, $C_L = 10, 20, 50, 100$ pF);
(c) switching trajectory ($L_T = 5$ nH, $C_L = 20$ pF);
(d) load current ($L_T = 5$ nH, $C_L = 20$ pF).

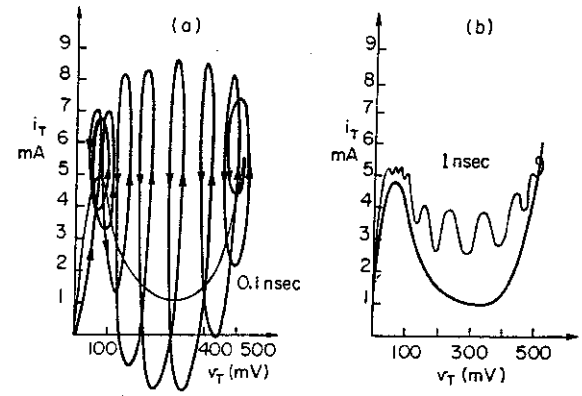

Fig. 5. Switching trajectories for inputs with finite rise times ($L_T = 2$ nH, $C_L = 20$ pF). Rise time = 0.1 ns (a); 1.0 ns (b).

The second use of capacitive loading, with which this paper is primarily concerned, is to conduct part of the capacitive current generated by switching, from the circuit via a low impedance path i.e. to form a generator of narrow Gaussian shaped current pulses. Any stray circuit inductance will clearly generate oscillations under the effect of switching transients and any practical circuit will have to take such oscillation into account. In fact, preliminary investigations of the pulse generator described later were discouraging due to oscillation in the output pulse.

3. Stray tunnel diode inductance ($R_L=0\ \Omega$, $L_L=0$ nH)

Typical switching waveforms for a step input are shown in fig. 4. A simplified circuit is proposed as a model for an approximate analysis. The resistive part of the td junction is neglected and only C_L, L_T and $C_j(\approx C_v)$ are considered. A step input, I_{in}, initiates a voltage oscillation,

$$(I_{in}/C_L)(C_s/C_L)(1/\omega_0)\sin(\omega_0 t),$$

where

$$C_s = C_v C_L/(C_v+C_L) \text{ and } \omega_0 = (L_T C_s)^{-\frac{1}{2}}.$$

Analytically predicted and computed oscillation frequencies are within the limits of frequency estimation from computed results, at the valley point. Amplitudes compare less favourably due to the ignored negative resistance, (e.g. 20 mV analytical, 25 mV computed at the valley). It is, however, evident that the oscillation produced by stray tunnel diode inductance is initiated by the input waveform. The effect of increasing the input rise time is shown in fig. 5. Analytically, the voltage oscillation is predicted as

$$(I_{in}/C_L)(C_s/C_L)\{1/(\omega_0^2 T)\}\sin(\omega_0 t),$$

for a ramp input rising at a rate I_{in}/T, i.e. an input I_{in} is effectively a step if rise time $T \leqq (L_T C_s)^{\frac{1}{2}}$, (typically about 0.3 ns). If input rise times are of the order of a few ns, a few nH of stray inductance will not initiate this particular oscillation mode. Some experimental waveforms are shown in fig. 6. The large values of inductance (lengths of straight wire were used) are required by the 5 ns input rise time before any oscillation is apparent.

4. Stray load inductance ($R_L=0\ \Omega$, $L_T=0$ nH)

Once again, some selected transients are shown in figs. 7 and 8. A simple analytical model, similar to that in the previous case is considered by assuming a ramp voltage rise (td switching) across the L_L-C_L load. The resulting load current is

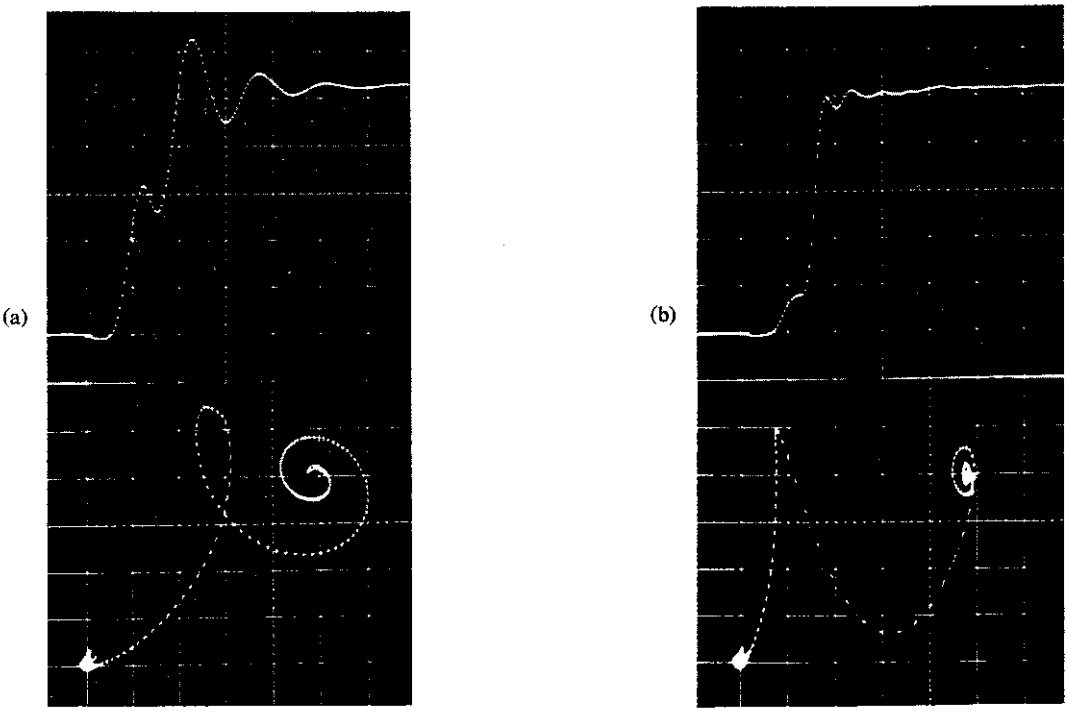

Fig. 6. Voltage transients and switching trajectories for finite tunnel diode inductance (T.D. 1N3716, $I_p=4.50$ mA, $I_v=0.61$ mA, $C_v=19$ pF, $I_{in}=5.0$ mA, input rise time $=5$ ns, $C_L=18$ pF). Voltage transients: vert. 100 mV/div, hor. 10 ns/div; Trajectories: vert. 1 mA/div, hor. 100 mV/div; $L_T=240$ nH (a), 60 nH (b).

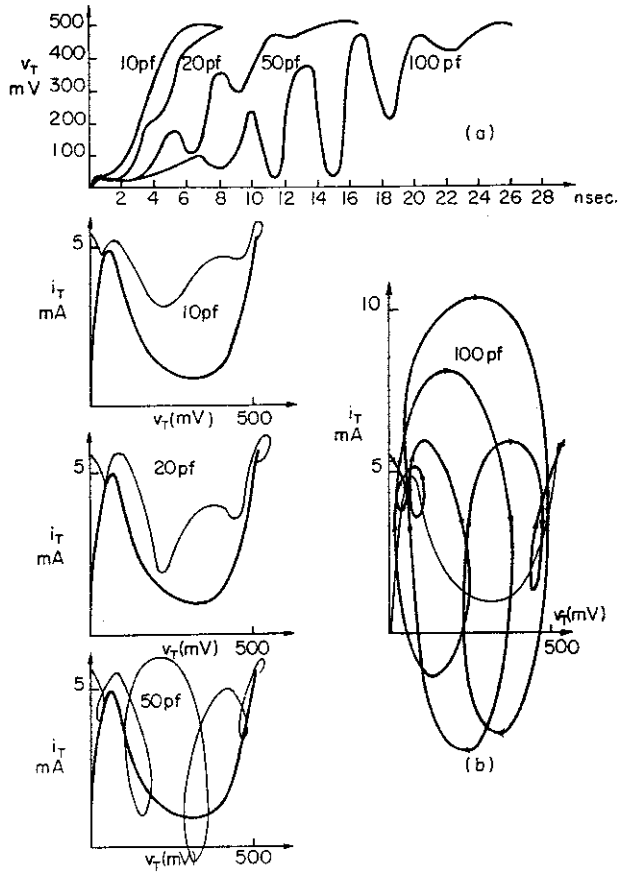

Fig. 7. Switching with finite load inductance ($L_T=0$ nH, $R_L=0\,\Omega$, $I_{in}=5.5$ mA step, $L_L=20$ nH, $C_L=10, 20, 50, 100$ pF).
(a) voltage transients; (b) switching trajectories; (c) load currents.

$$C_L(V/T)\{1-\cos(\omega_0 t)\},$$

where $\omega_0=(L_LC_L)^{-\frac{1}{2}}$ and V/T is the rate of td switching. However, because the junction voltage is itself affected by the oscillation, the estimated analytical results are not expected to compare favourably with the more detailed computer calculations. Fig. 9 shows computed load currents for three input current ramp step rise times. The basic pulse shape is not greatly dependent on the output waveform except where this affects the delay and rise times of the junction switching. Practical waveforms are shown in fig. 10 for direct comparison with the theoretical results.

The effect of L_T has been shown to be negligible for practical purposes, (more correctly the oscillation mode previously discussed is negligible), and L_L (i.e. the present oscillation mode), dominates the oscillation observed in practice. As far as the present oscillation mode is concerned, the switching source looks into a $(L_T+L_L)-C_L$ series combination and it is therefore the total series loop inductance which is important.

In fig. 11, the step input delay and rise time variations are shown with stray inductance and load capacitance. Delay and rise times are defined, respectively, as the times the td voltage takes to reach $V_p+\frac{1}{10}(V_f-V_p)$ and to go from that to $V_f-\frac{1}{10}(V_f-V_p)$. Clearly, the definition breaks down when there is a superimposed oscillation. The values shown are for an estimated hypothetical smooth voltage rise over which the oscillation is superimposed. The use of rise time variation for valley capacitance measurement evidently gives a lower than true value and the error is more sensitive to td inductance (about 15% for $L_T=2$ nH).

5. Resistive damping

A logical course of action to reduce load oscillation is to include a series damping resistance. The effect of 5 Ω and 50 Ω resistances is shown in fig. 12.

6. Current pulse generators

Clearly, the line output of the simple pulse generator shown in fig. 13 will be a close approximation of the idealised Gaussian pulse for moderate stray inductances and input rise times. Typical observed waveforms are shown in fig. 15a. Note that the pulse

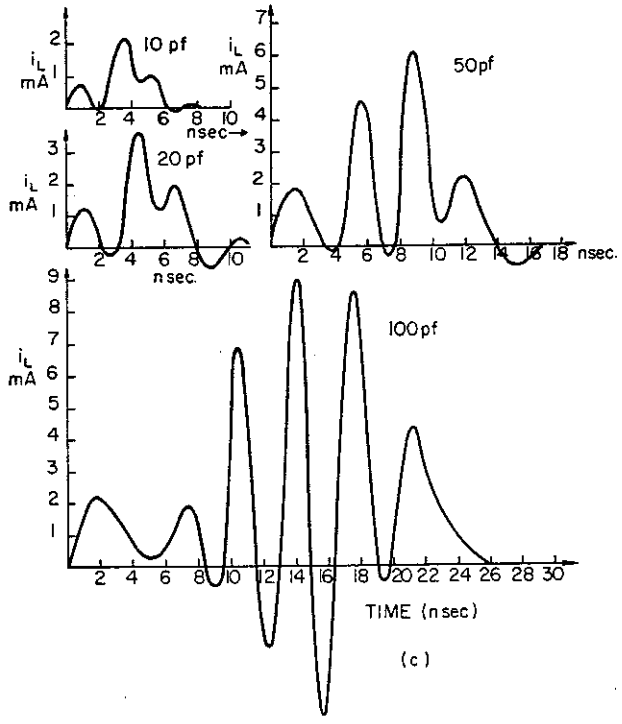

Fig. 7. (c).

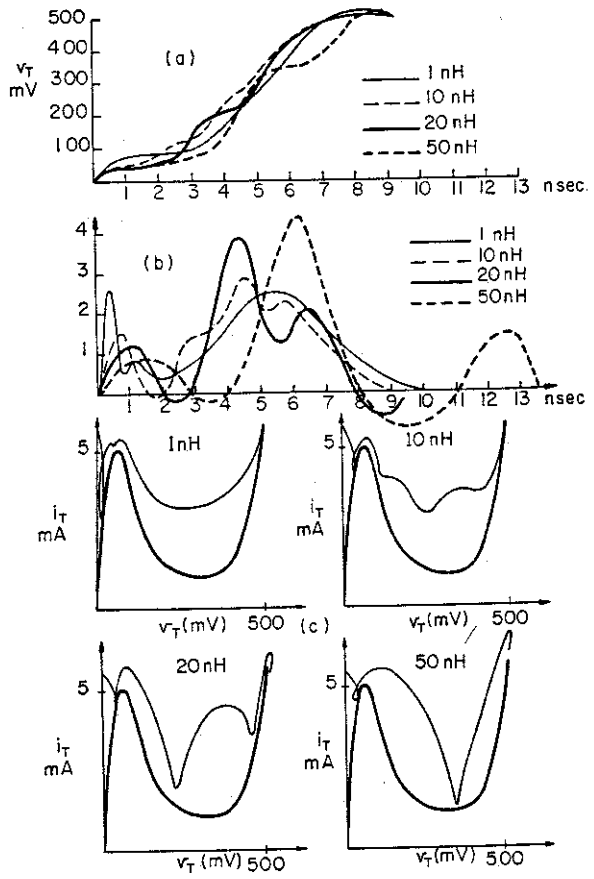

Fig. 8. Switching with finite load inductance ($L_T = 0$ nH, $R_L = 0\,\Omega$, $I_{in} = 5$ mA step, $C_L = 20$ pF, $L_L = 1, 10, 20, 50$ nH).
(a) voltage transients; (b) switching trajectories; (c) load currents.

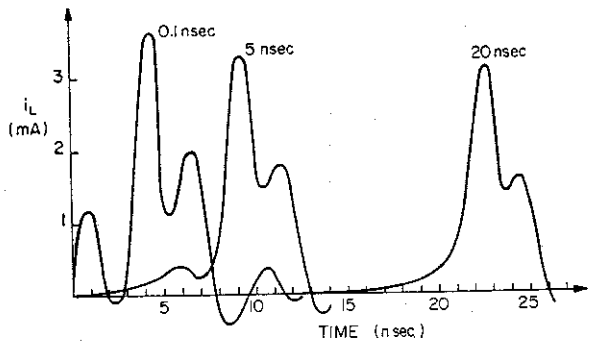

Fig. 9. Effect of input rise time on load pulse ($L_T = 0$ nH, $L_L = 20$ nH, $R_L = 0\,\Omega$, $C_L = C_v = 20$ pF, $I_{in} = 5.5$ mA ramp step, input rise times = 0.1, 5.0, 20 ns).

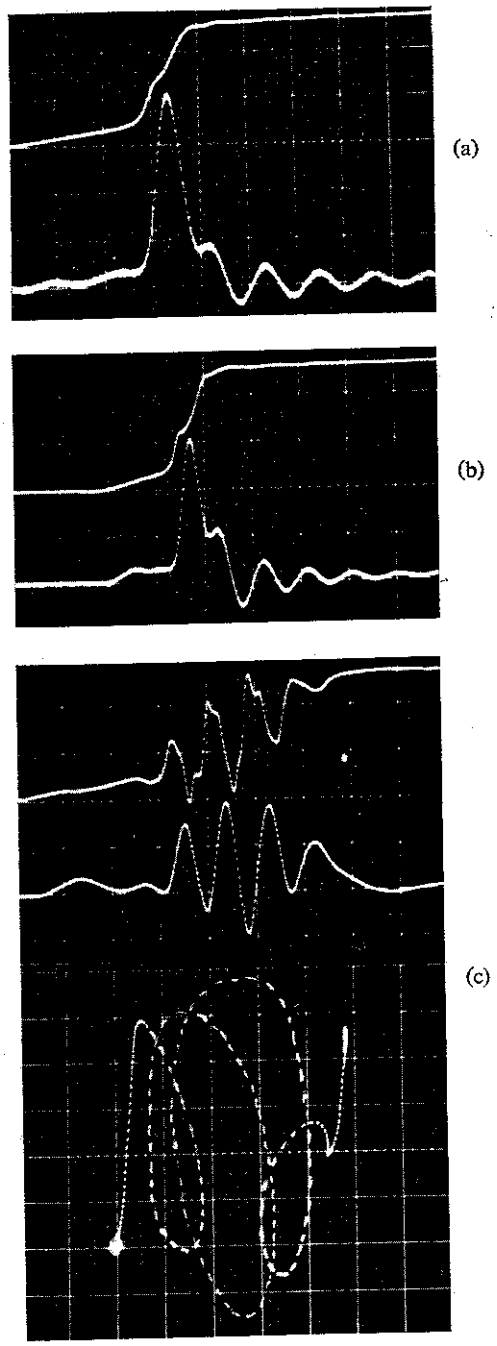

Fig. 10. Switching with finite load inductance (T.D. 1N3716, $I_p = 4.50$ mA, $I_v = 0.61$ mA, $C_v = 19$ pF, $I_{in} = 5.0$ mA, input rise time = 5 ns, $L_L = 20$–25 nH).
(a) voltage transient and load current ($C_L = 6$ pF, vert. 200 mV/div and 0.4 mA/div, hor. 2.5 ns/div);
(b) voltage transient and load current ($C_L = 18$ pF, vert. 200 mV/div and 1 mA/div, hor. 5 ns/div);
(c) voltage transient, load current and switching trajectory ($C_L = 100$ pF, vert. 200 mV/div. 4 mA/div and 1 mA/div, hor. 5 ns/div and 100 mV/div).

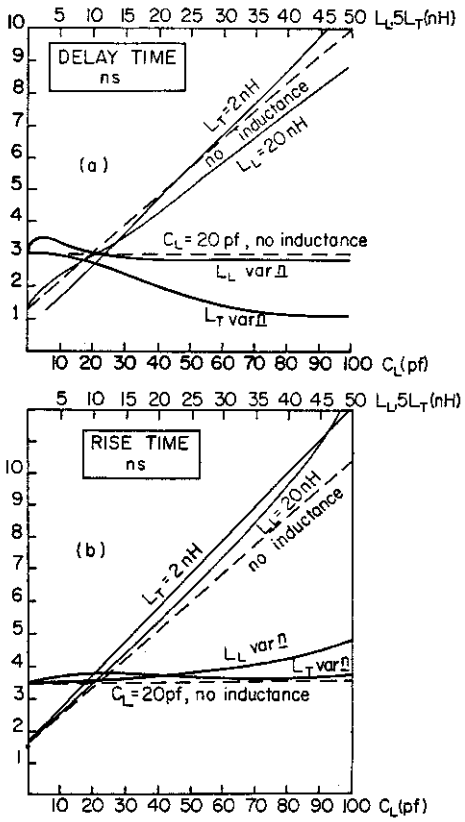

Fig. 11. Delay time and rise time variation ($R_L = 0\,\Omega$, $I_{in} = 5.5$ mA step), with C_L($L_T = 0$ nH, $L_T = 2$ nH; $L_L = 0$ nH, $L_T = 0$ nH; $L_L = 20$ nH, $L_T = 0$ nH); with L_L($C_L = 20$ pF, $L_T = 0$ nH); with L_T($C_L = 20$ pF, $L_L = 0$ nH).

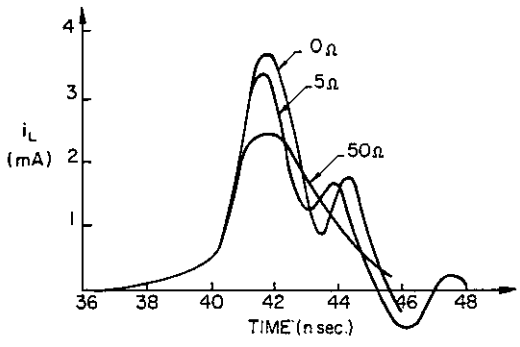

Fig. 12. Effect of resistive damping ($L_L = 20$ nH, $L_T = 0$ nH, $C_L = C_v = 20$ pF, $I_{in} = 5.5$ mA ramp step, rise time = 40 ns, $R_L = 0, 5, 50\,\Omega$).

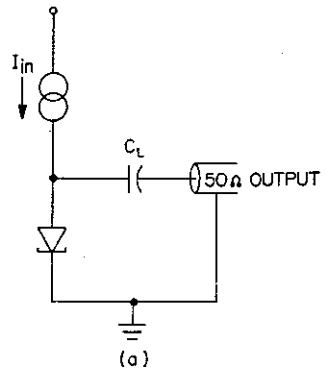

Fig. 13. Simple pulse generator.

height/half width ratio is no longer a maximum for $C_L = C_v$. Pulse height is, of course, reduced and half width increased by the series resistance, but these effects are offset, more or less, by residual circuit oscillation which may also cause some overshoot.

Such a circuit has extremely limited application by virtue of the td inherent bi-directionality and lack of isolation of output from input. Isolation is provided by the circuit shown in fig. 14 with the necessary damping resistance included. The emitter input impedance, which the td sees, is low, but the collector impedance,

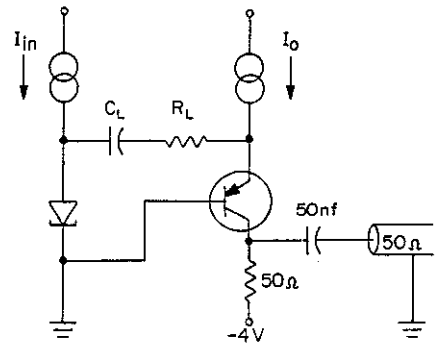

Fig. 14. Tunnel diode – transistor pulse generator.

looking back from the output, is high, providing good isolation. Note that the transistor is turned on at all times and the bias current I_b has to be greater than

$$(I_p - I_v)C_L/(C_L + C_v),$$

in order to maintain this condition when the td resets. Ideally, the 3.5 V across the collector-base junction keeps the transistor out of saturation and the base current low so the entire load pulse is transmitted to the output circuit. This is only true for transistors with cut-off frequencies much higher than the pulse frequency. When the td switching time is of the same

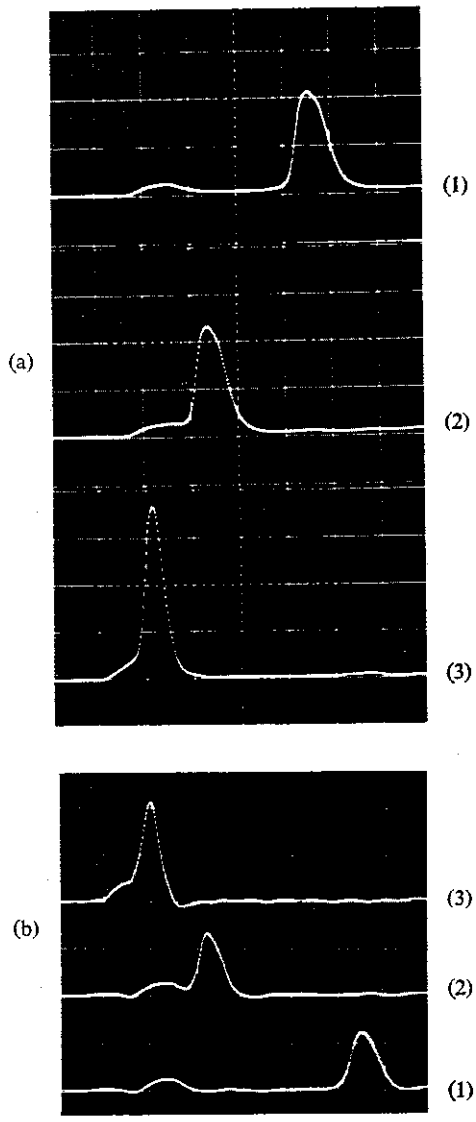

Fig. 15. Pulse generator output waveforms [T.D. 1N3716, $I_p = 4.8$ mA, $I_v = 0.8$ mA, $C_v = 23$ pF, $C_L = 22$ pF, $R_L = 47\ \Omega$, input rise time = 5 ns, input amplitude (1) 5.0 mA, (2) 5.5 mA, (3) 10.0 mA, vert. 1 mA/div, hor. 5 ns/div].
(a) simple pulse generator; (b) tunnel diode-transistor pulse generator.

order or less than the transistor base charging time then there is significant pulse amplitude loss and, (considering the high frequency grounded base equivalent circuit of the transistor) pulse spread in the effectively inductive collector. So the speed limitations on the circuit are provided by the transistor cut-off frequency. Typical waveforms shown in fig. 15b are for the 1N3716 td (switching time about 2 ns) with a 2N976 transistor (f_T about 900 MHz). The circuit has operated successfully with monostable (univibrator) biassing of the td. Faster td's (1N3857, 1N3858) requiring larger damping resistances to offset the effective inductance of the transistor, tend to spread the pulse.

7. Conclusions

Oscillation effects in capacitively loaded td circuits fall into two categories. Provided trigger currents are not too fast, only one mode is observed and may be minimised by reducing the total series loop inductance and by the inclusion of damping resistance. These precautions are included in the construction of a simple generator of narrow current pulses.

The limitations of the present treatment require some comment. The immediate object is to illustrate the type of effects encountered in capacitively loaded td circuits and to demonstrate the feasibility of such simple circuits as generators of narrow current pulses. In the same way that consideration of inductive effects on resistive loading led to the development of the separatrix concept and stability criteria, so a more detailed examination of inductive effects or capacitive loading may necessitate modification of triggering requirements, bias point stability, transient responses to short trigger pulses, etc. Development of the pulse generator similarly requires detailed consideration of the transient response due to the transistor equivalent circuit and effects of transistor cut-off frequency and propagation time. The negative output pulse produced when the tunnel diode resets may be undesirable in some applications and its elimination or suppression has to be considered.

The work described above was carried out in the Department of Physics, University of Auckland with financial support from the N.Z. Universities Research Grants Committee. The authors gratefully acknowledge the assistance of Mr. P. M. Fenwick with the computer programming.

References

[1] J. E. Morris, M.Sc. Thesis (University of Auckland, 1967).
[2] J. B. Earnshaw, Ph.D. Thesis (University of Auckland, 1966).
[3] J. Singer, *Elements of numerical analysis* (Academic Press, 1964).