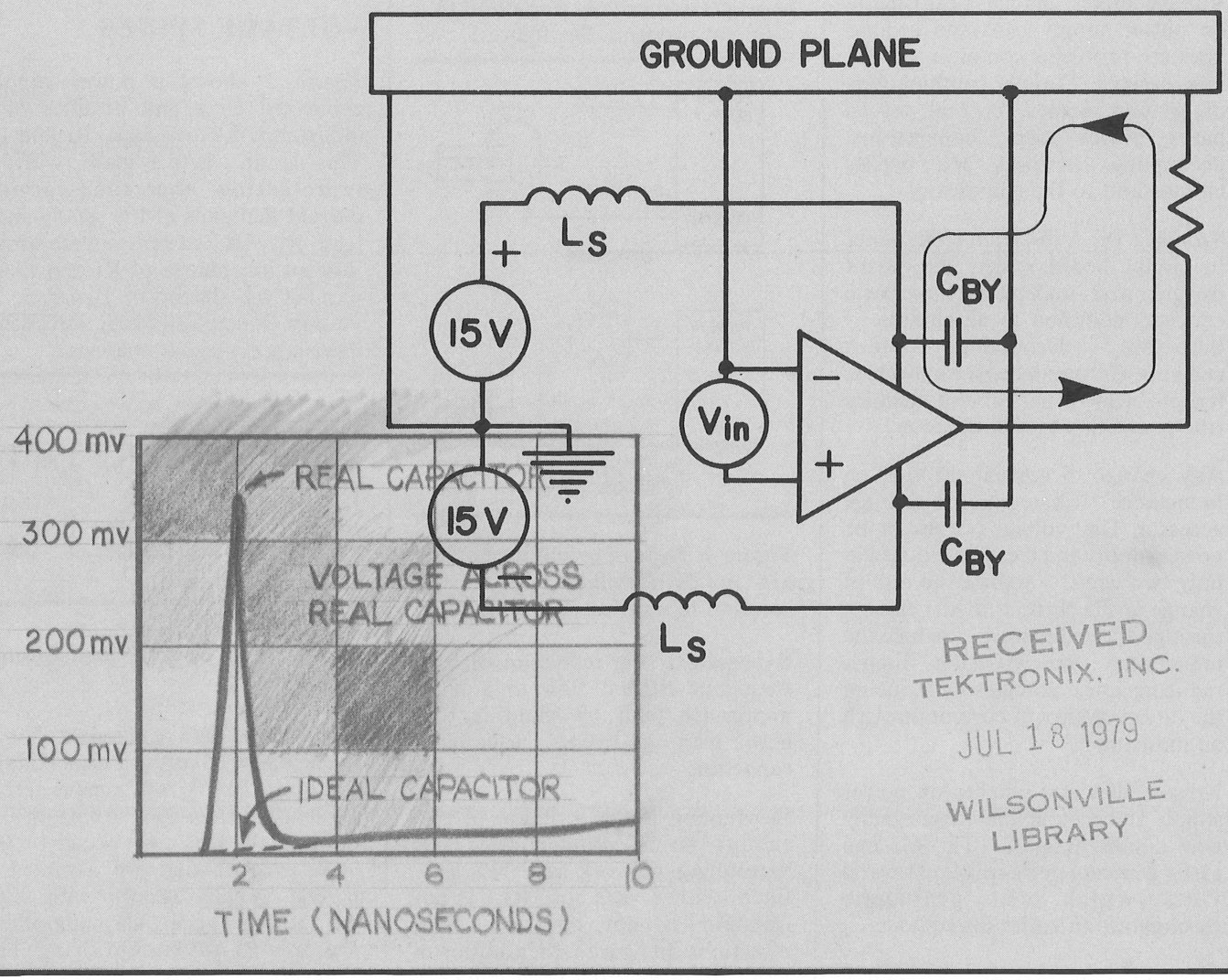
ENGINEERING NEWS

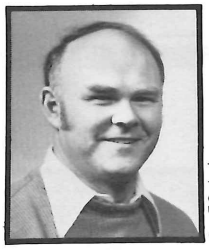
Company Confidential

April 1978

From Paper to Circuit Board: Bypassing



From Paper to Circuit Board: Bypassing



Laudie Doubrava, SPS Engineering, ext. 1119.

Laudie has more information than is shown here, so give him a call if you have any questions.

Many problems occur in transforming a new design into operating circuitry. Circuits that have zero-resistance and zero-inductance runs on paper become much more complex when implemented on a circuit board.

Voltage spikes, glitches and ringing on power supply runs and ground lines are problems common to most new designs. Various combinations of ground planes, current return paths, power supply connections, decoupling networks and bypass circuits add to the complexity.

To make the translation from paper to circuit board easier, the circuit designer must understand three basic concepts common to all circuits: - bypassing. - decoupling. - return currents. Common to each concept is the problem of parasitic inductance (the pencil line turned inductor).

Any change of current through an inductance will create a voltage across it. That voltage is noise in the power supply and it can be reduced in only two ways: - reduce the rate of change in the current (di/dt) passing through the inductance. - reduce the inductance. We will first discuss reducing noise voltages by reducing the rate of change of current through an inductance.

Noise spikes and glitches on power supply and ground lines plague many new circuit designs. TTL IC's can easily generate noise spikes of several volts which can propagate throughout an entire instrument.

Standard bypassing and decoupling techniques often fail to suppress these spikes and, worse, can create other problems.

DEFINITIONS

Bypassing and decoupling techniques are often poorly understood and improperly applied. Many designers believe bypassing and decoupling are synonymous. They are not; they are distinct concepts and each is a solution to a different problem. See figure 1.

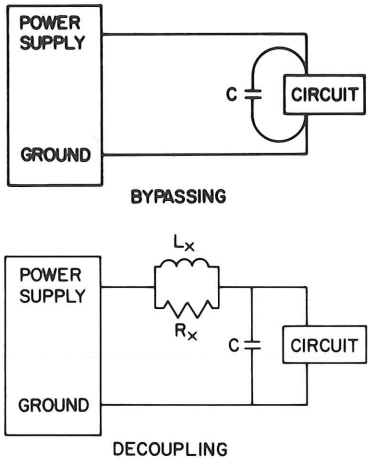


Figure 1. Bypassing and decoupling are not synonymous. Each is a solution to a different problem.

Bypassing is the reduction of high frequency current flow in a high-impedance path by shunting that path with a bypass, usually a capacitor.

Decoupling is the isolation of two circuits on a common line. The decoupling network is a low pass filter (either RC or RLC) but isolation is not equal in both directions. In figure 1, the addition of impedances R_x and/or L_x produces a decoupling network.

Most circuits require bypassing, not decoupling. Using decoupling techniques to accomplish bypassing will give disappointing if not disastrous results. Complete understanding of both concepts is vital. We will begin by looking at bypassing.

VOLTAGE SPIKES

Figure 2 shows a power supply connected by a pair of lines with inductance L_S to a load, R_I and I_L. This is an "active load" with I_I representing the time-varying current demands of the steady-state load R_I. The current source looks into an impedance of R_I and L_S in parallel as shown in *figure 3*. A voltage change will occur across this impedance when I_I changes.

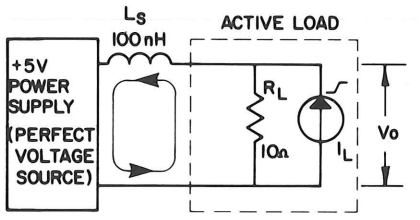


Figure 2. An "active" load without bypassing.

If the active load demands a change in current of 35 mA in 1 ns, a voltage spike of 330 mV will appear across the load (as shown in the bottom half of figure 3). This noise occurs on the load even though we assumed a perfect power supply with zero output impedance. (Throughout this article, a 35 mA current change in 1 ns will be used as a standard load transient test; the test is typical of the current demands of a single 7400

series TTL gate during a low-to-high output transistion.)

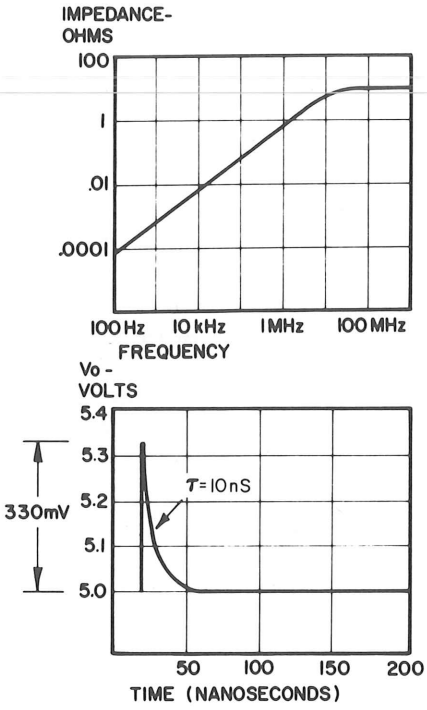


Figure 3. At the top is a plot of the impedance seen by an "active" load current source without bypassing. At the bottom is a plot of the spike generated across the unbypassed load with the load current demand of 35 mA/ns.

To reduce the noise generated by the varying current demands of the load, the impedance seen by I_L must be reduced. This can be done by adding a low impedance "bypass," usually a capacitor, near the current source as shown in *figure 4*. Since high-frequency currents now see a low impedance, noise generation is greatly reduced.

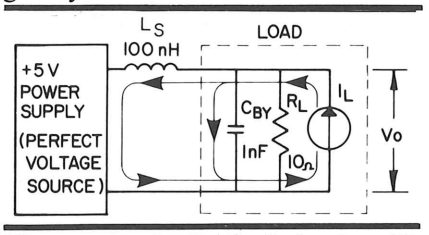


Figure 4. A "active" load with bypassing.

From what we have seen so far, adding an impedance in series with L_S (a decoupling network, for instance) will not decrease the noise produced by I_L but most likely will increase it.

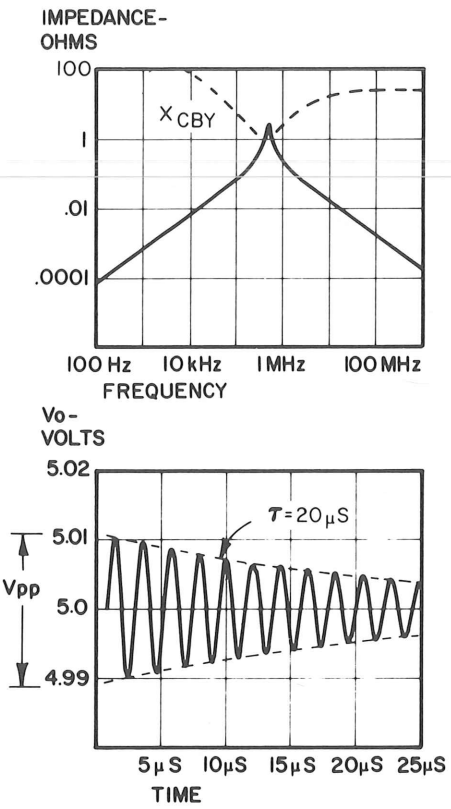


Figure 5. At the top is a plot of the impedance seen by an "active" load current source (I_L), with bypassing added. At the bottom is a plot of the response of the bypassed load to a step current demand of 35 mA.

For the bypassed load, the impedance seen by I_L is greatly reduced at high frequencies. However, a sharp resonant peak now exists which causes the output to ring (see *figure 5*). This peak is caused by the parallel resonant circuit formed by the bypass capacitor and L_S. If the bypass capacitor is one microfarad, the maximum V_{PP} is less than 24 mV, a substantial decrease from the 330 mV spike produced without bypassing. However, the decay time constant, τ_C is 20 microseconds which is 20,000 times longer than the unbypassed case. Bypassing reduces the amplitude of the disturbance but spreads its effects over a longer time. The same energy must be supplied by the power supply with or without bypassing. Bypassing just averages the demand over a longer period of time. The high frequency oscillations may cause some problems to sensitive circuits, but most applications will tolerate the low amplitude oscillations. A later article on mid-frequency bypassing will deal with simple techniques to eliminate "ringing" while retaining all the other desirable bypassing characteristics.

For the bypassed load in *figure 4*, maximum

$$V_{pp} = 2\Delta I_L \sqrt{L_S / C_{BY}}$$

and decay time (τ) equals $2R_L C_{BY}$

Increasing C_{BY} to 10 microfarads will decrease V_{PP} to 7 mv, but τ will increase to 200 microseconds.

If you now apply bypassing to an actual circuit, you will find it will not work as we've described. Noise voltages will stubbornly refuse to disappear and there will still be spikes on the supply lines. The mistake too often made at this point is to abandon bypassing and insert a decoupling network. This will almost guarantee even more noise.

Let's look at bypassing again to find the additional problems. The previous example assumed that an ideal capacitor is used as a bypass. In reality, capacitors have a small parasitic series inductance L_C and resistance R_C. This parasitic inductance is responsible for most bypassing failures.

REAL CAPACITOR

A good quality one microfarad ceramic bypass capacitor has about 10 nH of inductance and 50 milliohms of resistance. A look at a real capacitor in the frequency domain (*figure 6*) reveals that it has a resonant frequency of 1.6 MHz and is effectively an inductor above that frequency. This capacitor functions as a capacitor only below a frequency of 1.6 MHz. This is typical of real capacitors used for bypassing. They are capacitors only over a limited frequency.

Even though the parasitic values are small, they have a drastic effect on the capacitor's performance as a bypass element. For example, a 35 mA/ns current step applied to the capacitor will generate a a 350 millivolt spike across the capacitor (as shown in *figure 7*). This is much

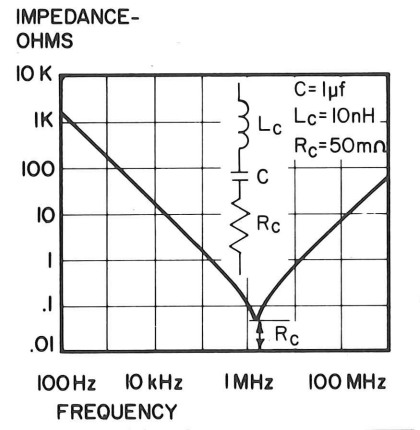


Figure 6. A close look at an example real capacitor reveals that it has a resonant frequency of 1.6 MHz and is effectively an inductor above that frequency. It functions as a capacitor only below a frequency of 1.6 MHz.

more noise than the previous bypassing example indicated.

How can we convert the real capacitor into an effective bypass element? One solution is to use ten 0.1 μF capacitors in parallel. This gives us a 1 microfarad capacitor with a series inductance of 1 nH, instead of 10 nH, if they can be effectively paralleled.

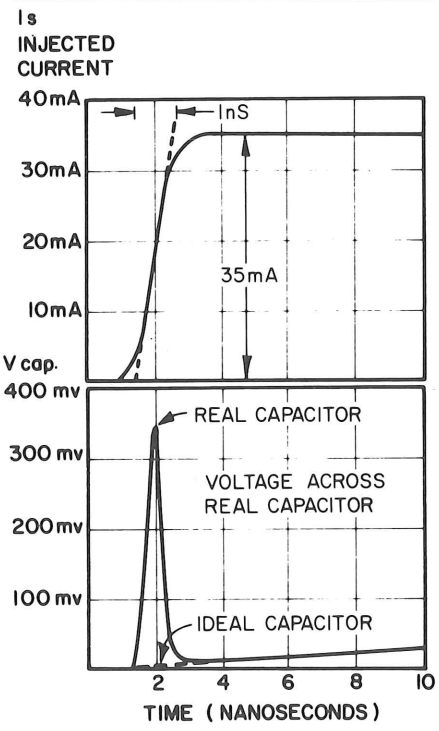


Figure 7. At the bottom are plotted the real and ideal capacitor responses to the 35 mA/ns current input (Is) shown above.

This capacitor, driven with the current source in our previous example (a di/dt of 35 mA/1 ns), will generate only 35 mV across the capacitor instead of 350 mV. However, this is not a practical solution because of the number of capacitors necessary to support just one gate's demand. A better answer is available and almost for free: use the ciruit board. The etched circuit board provides a nearly ideal bypass component to complement our real capacitor. It is particularly effective in suppressing the voltage spike appearing across the inductance of the real capacitor.

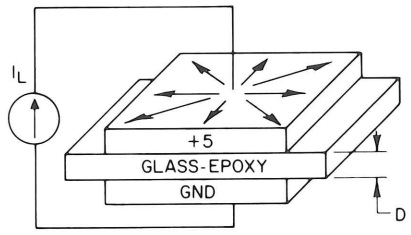


Figure 8. A close look at an etched circuit board as a bypass element shows two conducting layers sandwiching an insulating layer, essentially a huge parallel plate capacitor. Electrically, this construction is in parallel with the bypass capacitor.

USE THE CIRCUIT BOARD

Let's look a little closer at this new bypass component (see *figure 8*). It has two conducting layers with a layer of insulation in between. It is essentially a huge parallel-plate capacitor. Electrically, this component is in parallel with the bypass capacitor which is inserted into the etched circuit board.

The two-plate structure is more than a large capacitor because it forms a transmission line to any signal impressed upon it. With current source I_L as an input, the wavefront of the injected signal immediately begins to propogate in all directions and encompasses a larger and larger area. Consequently, a larger and larger capacitance, increasing as the radius squared, is seen by the signal.

Similarly, inductance is also increasing but at a slower rate proportional to the log of the radius. Because of this, the instantaneous characteristic impedance Z_0 presented to the propagating signal is rapidly decreasing.[1]

$$Z_0 = \sqrt{L/C}$$

For a typical EC board, the impedance seen at the signal source will decrease to less than 1 ohm within 125 ps. (See *figure 9*). This impedance shunts the bypass capacitor thereby suppressing the inductive voltage spike.

Figure 10 is a graph of the voltage across the current source I_L for current input of 35 mA/1 ns. Note that the potential levels off at about 5 mV during the entire current rise time, which is a sharp contrast to the 350 mV voltage spike seen across a real capacitor with the same input current.

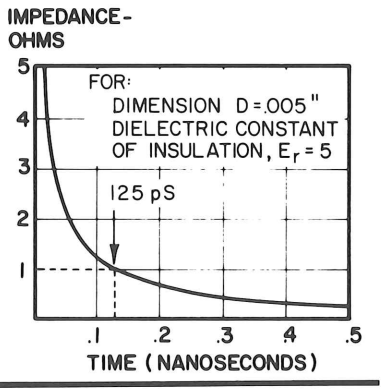


Figure 9. For a typical etched circuit board, the impedance seen at the signal source will decrease to less than one ohm within 125 ns. This impedance shunts the bypass capacitor thereby suppressing the inductive voltage spike.

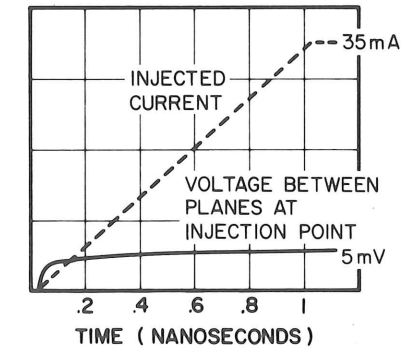


Figure 10. Plotted here is the voltage difference between supply plane and ground plane for an injected current of 35 mA/ns.

Figure 11 is a practical implementation of a multilayer etched circuit board to be used for proper bypassing. The ground and voltage supply layers are placed to provide the closest spacing to each other (in this case, 5 mils).

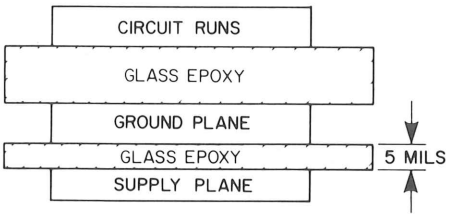


Figure 11. An etched circuit board layout for effective high-frequency bypassing.

PLACEMENT

The circuit runs are placed on the outer layers, with the continuous ground plane directly beneath acting as a return current path. All that is now needed is to properly place bypass capacitors onto the board. In most applications, placement of bypass capacitors is simple.

To be effective, the bypass must be at the point that gives the shortest, closest-coupled return-current path. This path often is not obvious but it is imperative that it be identified correctly.

LOGIC CIRCUITS

In TTL logic, the capacitor should be placed near the gate between supply and ground (*figure 12*).

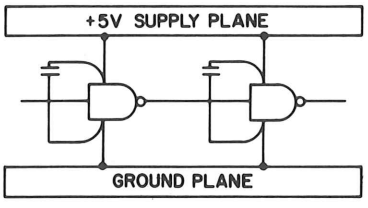


Figure 12. This diagram shows correct bypassing for TTL logic. Any inductance between capacitor and the active source will increase noise.

For ECL logic, however, the correct placement is not immediately obvious. Bypassing of -5.2 V to ground is not critical since these currents are essentially constant. Bypassing should be applied at the load resistor between -2 V and ground (*figure 13*). A bypass at this point insures the shortest path for return current to ground.

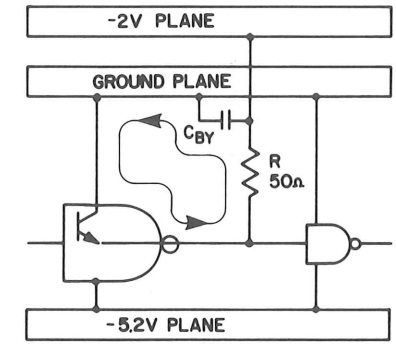


Figure 13. This diagram shows correct ECL bypassing.

ANALOG CIRCUITS

Bypassing in analog circuits is more complicated. The paths where supply currents are flowing are more difficult to determine. *Figure 14* shows an op amp circuit operating from dual supplies without bypassing. For a positive transition at the output, current will be demanded from the positive supply. A drop in the positive supply voltage at the op amp will occur because of the inductance of the supply line.

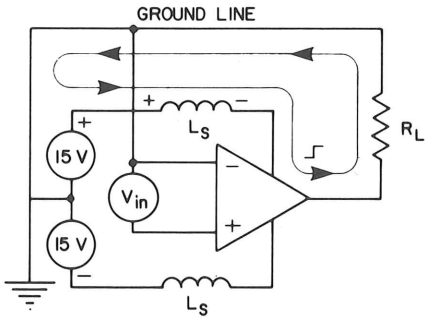


Figure 14. Shown here is an op amp circuit without bypassing.

For a negative transition in the output, a similar problem occurs. Current demand from the negative supply causes a voltage drop at the opamp negative supply terminal.

Power supply rejection of opamps decreases with frequency. High frequency noise will actually be amplified and may create feedback instability if correct bypassing is not used.[2]

Proper bypassing is shown in *figure 15*. Both positive and negative supply lines are bypassed to the ground return path for the load. The signal currents flow through the signal paths, but are restricted from flowing in the power supply lines. All high frequency current demands are supplied locally by the bypass. The inductance of the signal path and the ground return may still affect the output signal. This is a problem that will be covered in a later article.

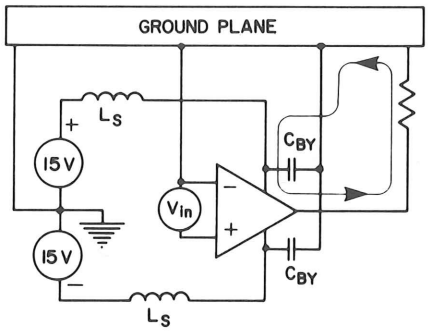


Figure 15. Here, proper bypassing has been added to the opamp circuit shown in figure 14.

Later articles will describe: (1) decoupling (what it can do for you and to you), (2) "real" power supply characteristics (output impedance, stability and ringing, (3) midfrequency bypassing, and and interaction with "real" power supplies, and (4) signal current return paths and their effect on loop inductance.

REFERENCES

1. S. Ramo and J. R. Whinnery. **Fields and Waves in Modern Radio** (second edition). New York: Wiley and Sons, 1953, 395.

2. Paul Brokaw. "An IC Amplifier User's Guide to Decoupling and Grounding." **Electronic Products**. (December 1977), 45-53.

Tom Woody, Large Screen DVST Engineering, ext.7147 .

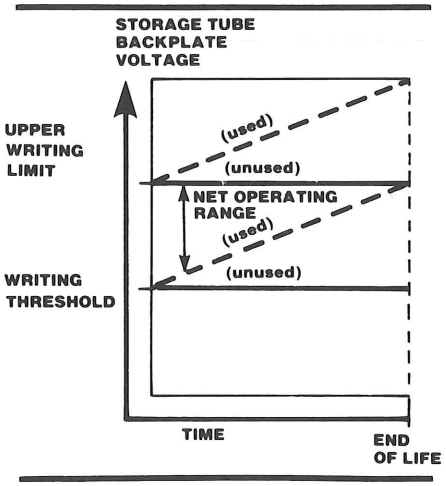
IMPROVED PHOSPHOR LIFE IN DVST'S

Tom presented a version of this article at the April Society for Information Display conference in San Francisco.

PHOSPHOR AGING

Scopes and computer displays are used in very different ways. Scopes usually display nonrepetitive asynchronous signals but computer displays heavily use both alphanumerics and graphics. Scopes tend to age the phosphor uniformly and display crt's tend to age a few areas repeatedly.

In display crt's, written areas are subject to higher flood gun current density than those of unwritten areas. This changes the surface characteristics of the phosphor [3, 4] and the operating points of the written areas. The net operating range is gradually reduced to zero in a length of time determined by how the display is used. **Differential aging**, the varying times in which net operating range is reduced to zero as determined by differing uses, is shown below.



LIFE TESTING OF PHOSPHORS

Development of experimental phosphors requires a way to test them in a reasonable time period. We developed a test which writes high density graphic information on the phosphor. We chose this kind of test for rapid aging of the phosphor because many users store graphic information for long periods of time. If the information is displayed repetitively in the same area for several hours, it produces a condition most viewers call "phosphor burn." Actually, it is a combination of differential aging and loss of luminance efficiency. This luminance loss correlates with electron current density effects.[3] On the other hand, some customers use their terminals only for alphanumeric information which ages the crt less intensively as you proceed from the upper left to the lower right quadrant.

These two modes of use led us to two types of phosphor evaluation. The first test of high density graphics gives us fast feedback on phosphor stability because current densities are higher. The high density graphics test takes only four to eight weeks for results.

If phosphor materials under test show substantial improvements compared to P-1 phosphor controls, then the tested materials advance to the next stage of testing with alphanumerics. This test ages one-fourth of the crt area with alphanumerics that continuously cycle for several months.

Our phosphor aging program required several years of testing before we found satisfactory materials for our display crt's.

SOLUTION TO AGING

Tektronix has used P-1 phosphor in all of its phosphor storage crt's since the Model 564 oscilloscope was released in the early 1960's. When differential aging was recognized in display applications, Tektronix began to look at other phosphors as substitutes, especially the rare earth phosphors such as Yttrium oxysulfide (Y_2O_2S:Tb) and Lanthanum oxysulfide (La_2O_2S:Tb) because of their high luminance efficiencies. Less efficient phosphors were also examined for their life stability.

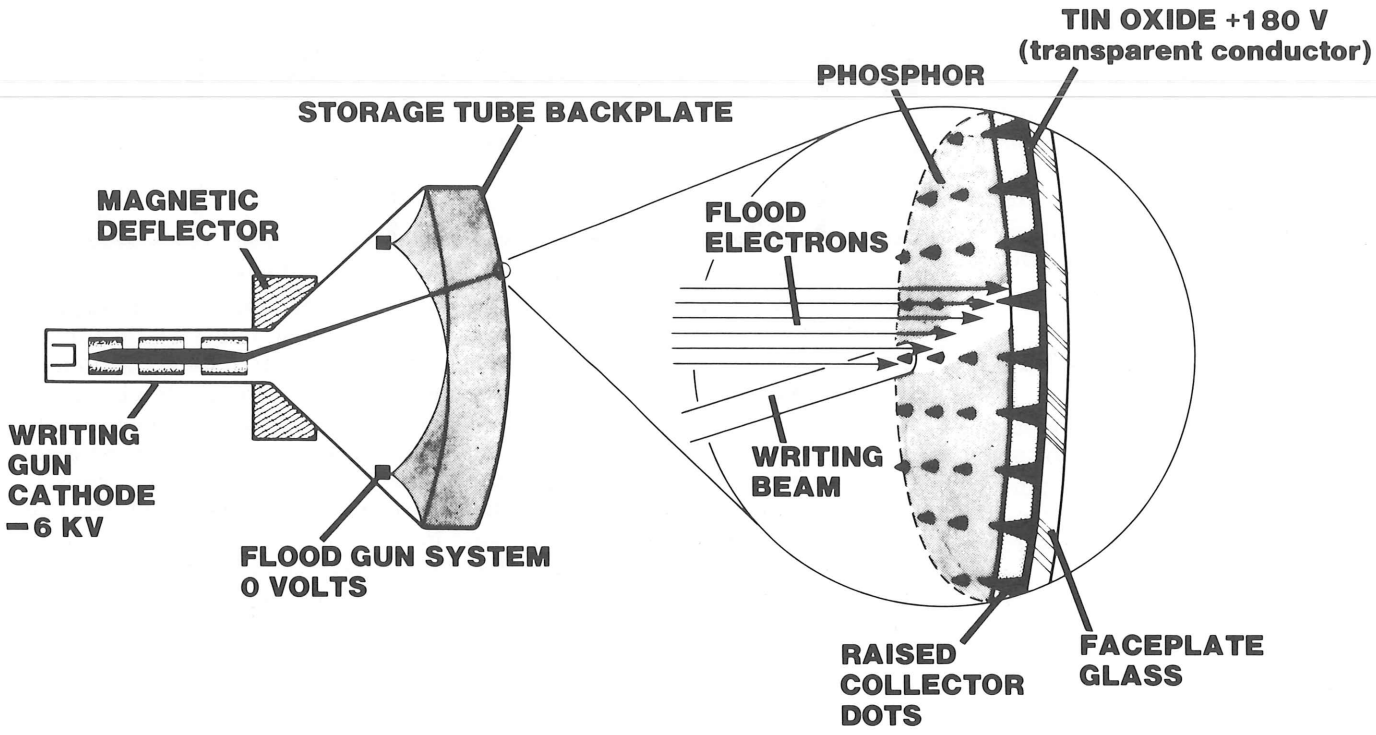
We found that oxysulfide phosphors are difficult to process with adequate yields, and that oxide phosphors such as Y_2O_3:Tb are compatible with our present P-1 processing. Though less efficient than oxysulfides, the oxide phosphors have very good life stability. We also found that a mixture of P-1 and rare earth oxides forms a very stable phosphor combination. We now use this phosphor combination in terminals and monitors that use 19-inch crt's.

Low voltage electron aging has not received as much attention as higher voltage aging. For this reason, we examined the intrinsic properties of P-1 phosphor in parallel with our empirical studies.

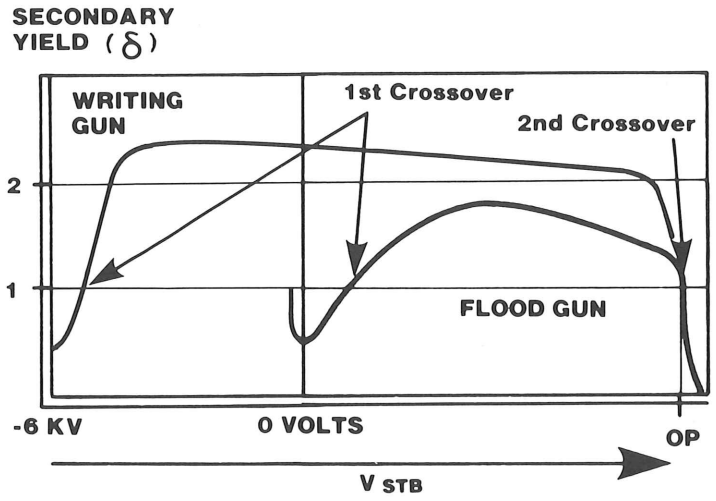
We found that P-1 aging is a result of electron-enhanced phase transformations [4] which means that the P-1 phosphor crystal lattice changes shape when bombarded by electrons. This has been confirmed by electron diffraction studies. These changes are a result of thermodynamic instability of the P-1 crystal lattice. [5]

continued on page 8

DVST OPERATION



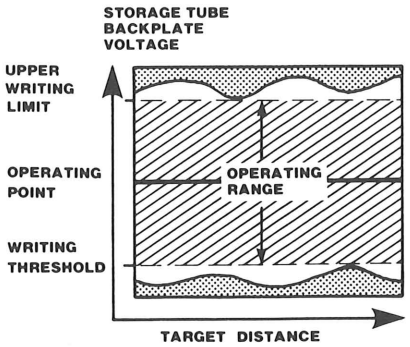
A crt contains a writing gun, a flood gun system and a phosphor/ collector target. The flood electrons land continuously on the phosphor and, in the absence of writing gun electrons, maintain the phosphor at the flood gun cathode voltage of 0 volts. When the writing gun electrons strike the phosphor, the target charges rapidly towards the collector potential which is defined as the operating point (OP) of the phosphor. This charges the phosphor past the first crossover of the flood gun system and the flood gun electrons then maintain the written areas at the second crossover or operating point.



DVST DEFINITIONS [1]

Writing threshold (WT) is the largest potential at which the writing gun will charge the phosphor to first crossover and maintain a stored charge image. **Upper Writing limit** (UWL) is the highest potential at which the charge image will meet resolution specifications (so that adjacent traces don't bleed together). The **operating point** (OP) is chosen to satisfy system performance requirements such as luminance and writing speed. Writing threshold and upper writing limit vary continuously over the target. The **operating range** (OR) is a measure of the latitude over which the target may be operated in the storage mode.

Parameters UWL, OP, OR and WT are shown schematically at the right. In general, small areas of the phosphor may have very large operating ranges, but when taken collectively over the entire target-face, they are reduced. This, of course, depends on the uniformity of the target and the phosphor type used.



Next, we began work to stabilize P-1 phosphor by substituting other materials into the P-1 lattice. Theoretically, these other materials will increase the strength of the bonds between elements in the crystal lattice and minimize electron bombardment damage. As a result of earlier studies, we found that some combinations of MgO and P-1 yield a phosphor with a five-fold increase in the usable life of the crt. This phosphor material will be introduced in the 19-inch crts this year.

ACKNOWLEDGEMENTS

I wish to thank the following people for their aid in our phosphor aging studies. For materials development: Ralph Mosman, Paul Chang and and Bob Vreeland. For materials analysis and evaluation: Bill Mason, Dave Gutzler and June Pimental.

BIBLIOGRAPHY

1. Anderson, R.H., "A Simplified DVBST", **IEEE Transactions on Electron Devices**, Vol. ED-14 No. 12, Dec. 1967, pp. 838-844.

2. Winningstad, C.N., "The Simplified DVBST in Computer-Output Application", **SID Digest**, May 1967, pp. 129.

3. Hurd, Jim, "Electron Induced Description of Oxygen from the $ZnSiO_4$:Mn Surface", **The Electrochem Society**, May 12-17, 1974.

4. Dash, J.; Fossum, J., "Electron Microscope Study of P-1 Phosphor Aging", **The Electrochem Society**, Washington, D.C., May 2-7, 1976.

5. Chang, Paul C.; Dash, John, "Electron Diffraction Study of Tek P-1 Aging Mechanism", Report #043, Tektronix, Jan. 27, 1976.

6. Gutzler, D., "The Efficiency of Y_2O_2S:Tb under Low Energy Electron Bombardment", **Electrochem Society**, May 8-13, 1977.

CRT	PHOSPHOR	ACCELERATED HOURS	LUMINANCE	INTRODUCED
11″	P-1	3000	8 fl.	1967
	Y_2O_2S:Tb	9000	24 fl.	1977
19″	P-1	700	8 fl.	1974
	P-1 + Y_2O_3:Tb	2000	8 fl.	1976
	P-1 + MgO	4000	8 fl.	1978

Table 1. This table summarizes the use of the new phosphor materials. Presently there are two crt sizes used in display products: the 11-inch and 19-inch diagonal crt's. Column three lists the average accelerated test hours as previously described. This test is based on aging the top left quadrant of the crt 24 hours a day, 7 days a week. As indicated in the table, the 19-inch display life is increased at no expense to luminance but the 11-inch rare earth display not only increases life by a factor of three but also luminance by a factor of three. [5] This increases the viewability of the display significantly over that of P-1. We have found by analyzing instrument use in the field that the user can expect, on the average, two to three times the accelerated hour usage for instrument on time. In the case of the 19-inch display with P-1 MgO phosphor, the user can expect 8000 to 12,000 instrument hours of crt use or 4 to 6 years use at 40 hours per week. This is a five-fold improvement over the earlier P-1 phosphor.

IN PRINT

CLIFF MORGAN

Cliff Morgan (SPS Engineering) is the author of "Digital Signal Processing", an article in the November 1977 issue of **Laser Focus Magazine**. The article discusses how software aids researchers in extracting and analyzing laser signals. Two applications are discussed: fluorescence-decay research and laser-fusion research.

For reprints, call Cliff Morgan on ext. 1154.

HALE FARLEY

"High Speed Waveform Measurements in Laser Fusion Research" is the title of an article authored by Hale Farley (Santa Clara field office) for the January 1978 issue of **Research/Development**. Farley discussed such topics as the areas of laser fusion in which electronic instruments are used, instrument selection, fast storage oscilloscopes, waveform digitizers, streak cameras and displaying particle pulses.

For reprints, call Don Boldea on ext. 5556.

BLAZO, HAWKEN AND PERKINS

Peter Perkins (Product Safety Engineering), Kenneth Hawken (Display Device Engineering) and Stephen Blazo (now with Watkins-Johnson Company) presented a paper entitled "A Crt That Stores 400 MHz Transients" at the December 1977 International Electron Devices Meeting in Washington, D.C.

The paper describes the design of the high-speed storage crt for the Tektronix 7834 Oscillscope. The crt can store single events at 400 MHz and uses an electron gun with quadrupole lenses to achieve scan expansion and beam focus. A more uniform display of the stored signals was achieved using an improved collimation system (a system for aligning the electron beam in the tube).

For a reprint, call Ken on ext. 5544, or Pete on ext. 7374.

BERG, STRANDE AND WHITE

Bill Berg (now with Control Data Corporation), Ed Strande (High Frequency Components) and Bob G. White (Switch and Relay Engineering) were coauthors of "Elastomers Solve Tough Problems in High-Frequency Systems" in the January 5, 1978 issue of **EDN**. The article describes three new devices that use metallized elastomer contacts: an improved high-frequency microstripline connector, a cam switch and a relay.

For a copy of the article, call the library on ext. 5388.

HOUSING NEEDED FOR SUMMER STUDENTS

Tektronix will again be hiring technical students for summer employment. They represent electronic engineering, computer science and the physical sciences.

Since they will be here for only a few months, arranging housing is a major problem. If you would like to make a housing arrangement with a student, call Nancy Andrews (College Relations) on ext. 5633.

WRITING TECHNICAL ARTICLES...for fun and (sometimes) profit

Bill Furlow, T & M Publicity, ext. 6601.

That idea you just talked about at lunch might make a good magazine article. Technical articles give you a chance to communicate with engineers who share your interests and problems. If your ideas are formulated well enough that you can convey them to one or two people in an hour or less, you could probably write a technical article in just a few hours more. Let's look at some of the reasons for writing technical articles before we get into the "how to" part.

COMMUNICATE WITH OTHER DESIGNERS...

That's what you do at coffee or lunch or at professional society conferences. That's what you do every day at Tektronix. But how many people do you reach? One, ten, a hundred? A technical article can reach a thousand times as many!

And a very surprising fact for new authors is that articles open up a valuable avenue of information exchange. Your article doesn't end the discussion; it begins the discussion. You will receive mail and phone calls from designers who need more information or have some to pass along. And some of the greatest nit-pickers in the world will carefully examine your design criteria and formulas. If you make a mistake, you'll learn about it quickly, and that can be the most valuable thing of all—even if it is hard on the ego.

Everybody knows that we're living in an information explosion, that the sum total of man's knowledge is doubling every half decade and all that. Perhaps such stunning statistics make you feel that anything you know could not make much of a dent in things. Many engineers have much the same attitude because they are so familiar with their work that they assume everyone else is too. But most worthwhile design articles are written by "ordinary"—but competent—design engineers. The crisis is not so much the gathering of new knowledge, but the effective dissemination of that knowledge. The information you have is significant, and chances are good that at least one magazine (there are more than 4000 in the U.S.) will be interested in what you have to say.

Perhaps your writings won't be remembered as long as Tolstoy's, but to a harried and hurried designer who's looking for the answers you have, your article can be a lot more important.

ENHANCE YOUR PROFESSIONAL STATUS

A designer shouldn't be penalized for not writing articles, but on the other hand, most authors do feel that writing has helped their careers. A well-written and well-researched article carries a definite air of authority, and many times, the research that's required to back up your article will improve your knowledge in that specific field. It all adds up to technical competence that is made more visible by your articles.

Technical articles can be a logical extension of your daily work that will help you meet other engineers in your own field. They will also make you more visible to the management of your own company, and if you stand up to that visibility, your career will be enhanced.

TEK'S IMAGE

Hand in hand with your status is that of Tektronix. Improve one and you're almost certain to improve the other. The value of the trade press as a method of improving the corporate image is well recognized by most corporate management. That's why the IDG and T & M Publicity departments spend so much time chasing down technical articles and sending out press releases.

If you have any doubts about the value of technical articles carrying your name and that of your company, just call the Publicity Department (ext. 6601) and ask us what we think about publishing your article. You should check with us anyway, for several good reasons. First of all, the Publicity Department will give you any assistance we can. We can help you write, edit and illustrate your article. We will also help you get corporate approvals required to release your article for publication and give you advice on which magazine might be most receptive.

EARN EXTRA MONEY

Some society journals don't pay anything, and, in fact, some even charge for the editing and art department time that is required in preparing your article. On the other extreme, some large-circulation, general-interest magazines pay extremely well. Trade publications (**Computer Design**, **EDN** and **Electronics** are examples) tend to pay at the lower end of the scale (usually $25 to $35 per magazine page.

Once you've selected one or two magazines that interest you, contact us and ask about their payment schedule. They'll probably quote an average, but flexible, price per printed page. Editors tend to pay less for articles that require a lot of work on their part, and more for well-prepared material covering a topic of particular interest.

No matter how good your article is, you can see you're not going to get rich by writing for the trade press, but it can be worth your time. A half-page circuit design shouldn't take more than a few minutes of your time since you've probably done the groundwork on the job already. A six-page article will take a lot longer, but if the basic work has been done on the job, you'll be surprised how little effort is required. And don't forget that your Publicity Department can take a lot of the pain out of the job. Next month we'll discuss some more specific details about publishing technical articles.

RENTAL INSTRUMENTS

Instrument Control recently added several instruments to the Instrument Rental Pool. The Hewlett-Packard 5940A Bus System Analyzer is useful in both design and service work, simplifying the diagnosis of software and hardware problems. Also out of the "Brand X" factory are the HP 9815A, 9825A and 9830A desk-top calculators.

Among the Tek terminals and associated equipment are the 4010, 4012, 4013 and 4051 terminals, 4932 modem and 4601 hardcopy unit. Most recently added to the Rental Pool is a Comodore PET terminal with 8k RAM. Specifications and operating manuals for these instruments are available from Instrument Control's files (at no charge).

For more information, call Joe Rowland or Mary Wilhelm (ext. 7141) or drop by 58-188.

PROFILE

CHEMICAL MACHINING

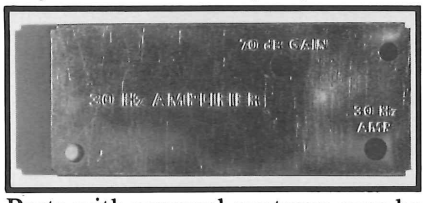
This is the second of a series of profiles of departments of interest to the Tektronix engineering and scientific community. The information is abstracted from the recently published Engineering Sourcebook (Who/What/Where/When). For a copy of the sourcebook call Jacquie Calame on ext. 6867.

Kay Geis and Henry Bahrs, Chemical Machining department. They are standing behind a coordinatograph, a device used to cut artwork for chemical milling patterns. The readout on the left indicates the coordinatograph's position in the pattern.

WHAT

Chemical Machining provides thin metal parts chemically machined to any contour.

Chemical machining is especially useful in thin metals (0.001 to 0.025 inch thick). Parts may be permanently marked with titles or part numbers by etching on one side. The part shown below was etched for easy and certain identification by production workers. Bend-lines were etched into the design so that the part may be bent into shape by hand.



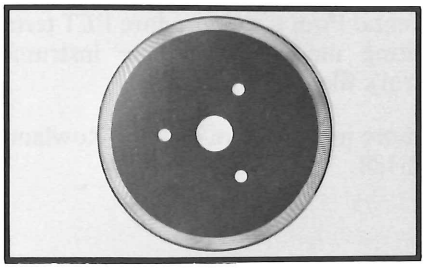
Parts with unusual contours may be etched for prototype devices. When design changes have settled down and large quantities are needed for production, the parts can be made with punch and die. For the small quantities used in engineering prototypes, the cost of chemical machining is low compared with the cost of mechanical tooling.

WHEN

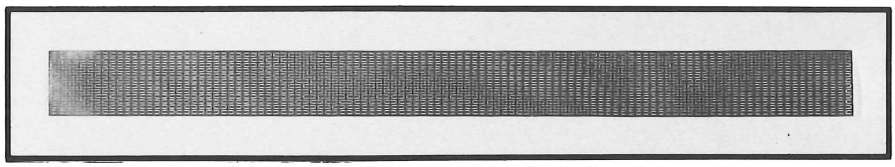
Contact Chemical Machining during the design phase of product development for consultation and before the prototype phase for parts. The lead time for producing the parts varies with the workload, but it is usually one to three weeks. Bring a job request and a dimensioned sketch or drawing.

WHO and WHERE

Chemical Machining (part of Engineering Support) is located at 50-354. Call Henry Bahrs or Kay Geis on ext. 7988 for information.



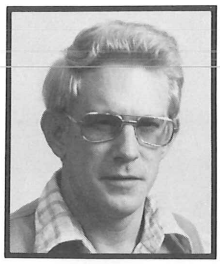
A chemically-machined rotor interruptor, with 360 1-degree slots. This disk is set between a light-emitting diode and a photosensitive transistor that counts the slots as the disk is rotated. The interruptor is used in the 4631 Hard Copy unit and 4632 Video Hard Copy unit.



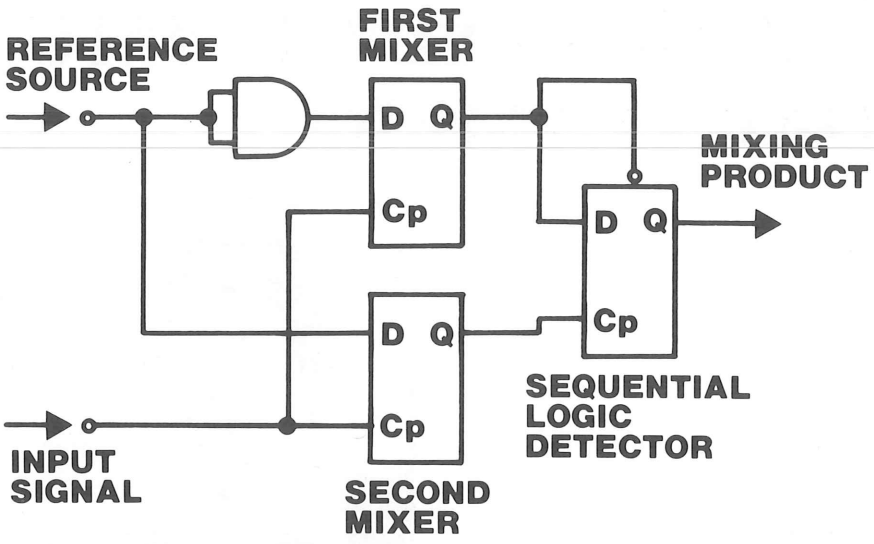
A chemically-machined ground plane for etched circuit boards.

PATENTS RECEIVED

SIDEBAND DETECTOR



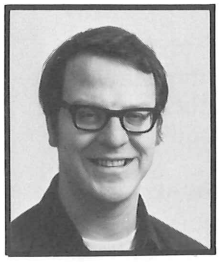
Fendall Winston, Frequency Domain Instrumentation, ext. 7193.



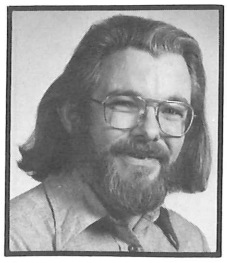
In this sideband detector circuit there are two channels with one sequential logic mixer in each channel. The output of a reference source is fed to the first mixer through a delay and to the second mixer in phase. An input signal is simultaneously fed to both mixers. The mixer outputs then feed to a sequential logic circuit where the desired sideband is detected.

This invention is an improvement over other sideband detectors because mixing requires only conventional combination and sequential logic and the detection requires only conventional sequential logic. Thus, there is no need to use precision components such as phase networks, filters and attenuators.

PHASE-LOCKED DEMODULATOR



Larry Nelson, T.V. Products Eng., ext. 7940.

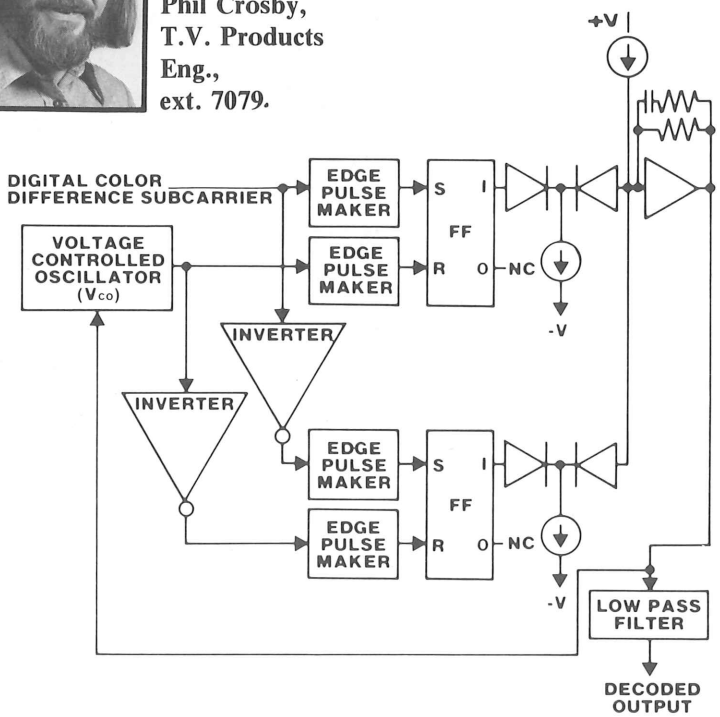


Phil Crosby, T.V. Products Eng., ext. 7079.

This patent is for a phase detector that provides a voltage output which is determined by the phase difference between a limited input signal and a reference signal. The phase detector increases the dynamic range of the resultant phase-locked loop.

The phase difference $\triangle\Phi$ between the reference and the voltage controlled oscillator is nominally 180°. The AC component in the phase detector output is proportional to 180° - $\triangle\Phi$. This means that the design of the loop filter and the low pass filter is simplified in cases where

$$\triangle f/f \geq .1$$



TECHNICAL COMMUNICATIONS DEPARTMENT

The following article is abstracted from the Engineering Sourcebook (Who/What/Where/When). For a copy, call Jacquie Calame (Technical Communications) on ext. 6867.

WHAT

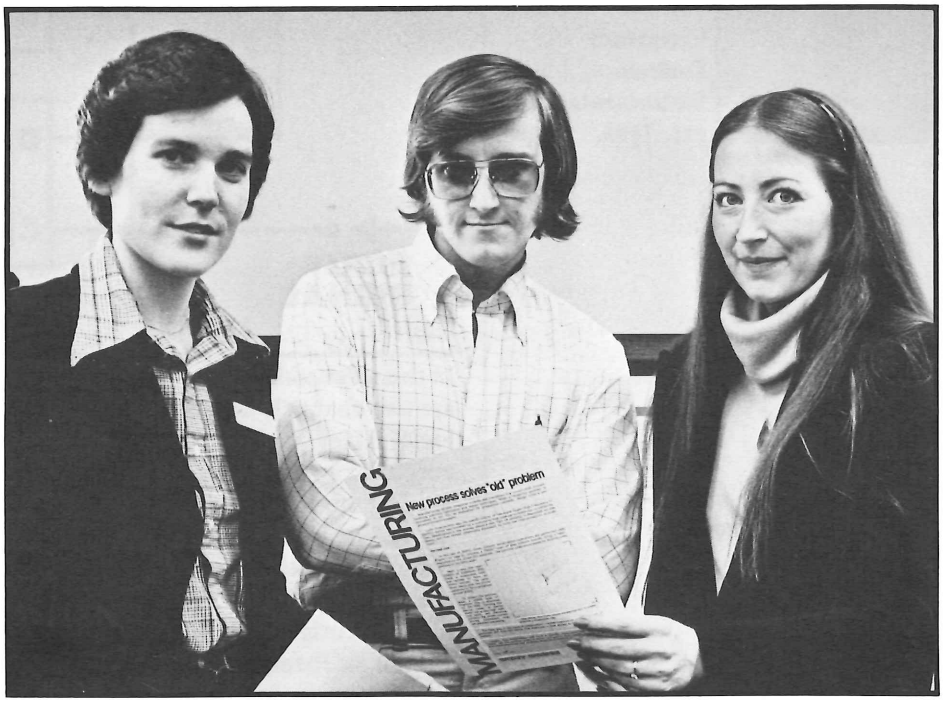
Technical Communications distributes vendor data books, prepares application notes and publishes two newspapers: **Component News** and **ManuFACTuring**.

Component News contains technical articles on purchased and Tektronix-made components and includes application, availability, cost, quality, product safety and reliablity information. **Component News**, published twice monthly, is distributed to design and staff engineers, manufacturing line managers and others.

ManuFACTuring, published monthly, facilitates communication among Tektronix manufacturing areas. The newspaper is also an informal liaison between engineering and manufacturing groups.

In addition to the newspapers, Technical Communications publishes application notes, designer's guides and user's handbooks. Examples include: **Device Derating Guidelines, Designer's Guide to Variable Resistors, VENTBOX—A Computerized Thermal Analysis Program** and the **Engineering Sourcebook**.

Technical Communications also provides data books from outside vendors and will special-order publications not in stock.



Technical Communications department members are Carolyn Schloetel (left), Frank Dufay (center) and Jacquie Calame (right).

WHEN

Component News requires a two-week lead time to publish articles. Allow two to three weeks to have articles published in **ManuFACTuring**. Special seminar announcements require a one-week lead time.

WHO

Carolyn Schloetel (ext. 6867) manages Technical Communications (located at 58-299). Other people in the group are: Jacquie Calame (associate editor, graphics production) and Frank Dufay (technical writer). Jacquie and Frank are also on ext. 6867. Call that number for mailing list changes and data book distributions.

SURVEY

We are always interested in feedback from our readers. Feel free at any time to call ext. 5674 or drop by 50-462 to tell us what you would like to see in Engineering News. We have provided a questionnaire for those who prefer writing their comments.

Overall, have we met your needs for engineering news? Rate us on a scale of 1 (bottom) to 10 (top rating). _____

What article in the last year was most interesting to you? (Title or subject) _____

Which cover was the most pleasing to you? (Subject or issue number). _____

Would you rather see Engineering News go into greater depth than it does now? Or cover more topics? Or both?
deeper coverage ☐ wider coverage ☐ both ☐ OK as is ☐

Do you like the Engineering News format (readability and overall appearance)?
Rate us on a scale of 1 (bottom) to 10 (top rating). _____

Which of these features are valuable to you?	very valuable	so-so	little or no value
New technology at Tektronix.			
New Tektronix products.			
Announcements of classes and seminars.			
Digests of papers presented by Tektronix engineers.			
Patents received.			
Special design file (a running catalogue of designs, to avoid reinventing the wheel).			
IEEE legal and educational program news.			
News about GPIB technology.			
Organization charts of engineering and support groups.			
New technical standards.			
Product safety engineering requirements and services.			
In-prints (notice of Tektronix authors who have been published).			
Metric conversion at Tektronix.			
Calls for papers.			

What field do you work in?
Electronic engineering? ___ Mechanical engineering? ___ Chemistry? ___ Physics? ___ Software? ___ Marketing? ___

Do you also subscribe to Component News? ___ Software News? ___

Additional comments? _____

Please mail to EN 50-462

Vol. 5, No. 4, April 1978. Editor: Burgess Laughlin , ext. 5468. Art director: Scott Sakamoto. Technical illustrator: Joe Yoder. Published by the T&M Publicity Dept. (part of Test and Measurement Marketing) for the benefit of the Tektronix engineering and scientific community in Beaverton, Grass Valley and Wilsonville areas.

Why EN?

Engineering News serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community).

Contributing to EN

Do you have an article or paper to contribute or an announcement to make? Contact the editor on ext. 5468.

How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle and the timeliness of the content). But the *minimum* is five weeks for simple announcements and about eight weeks for major articles.

The most important step for the contributor is to put his message on paper so that the editor will have something to work with. Don't worry about organization, spelling and grammar. The editor will take care of those when he puts the article into shape for you.