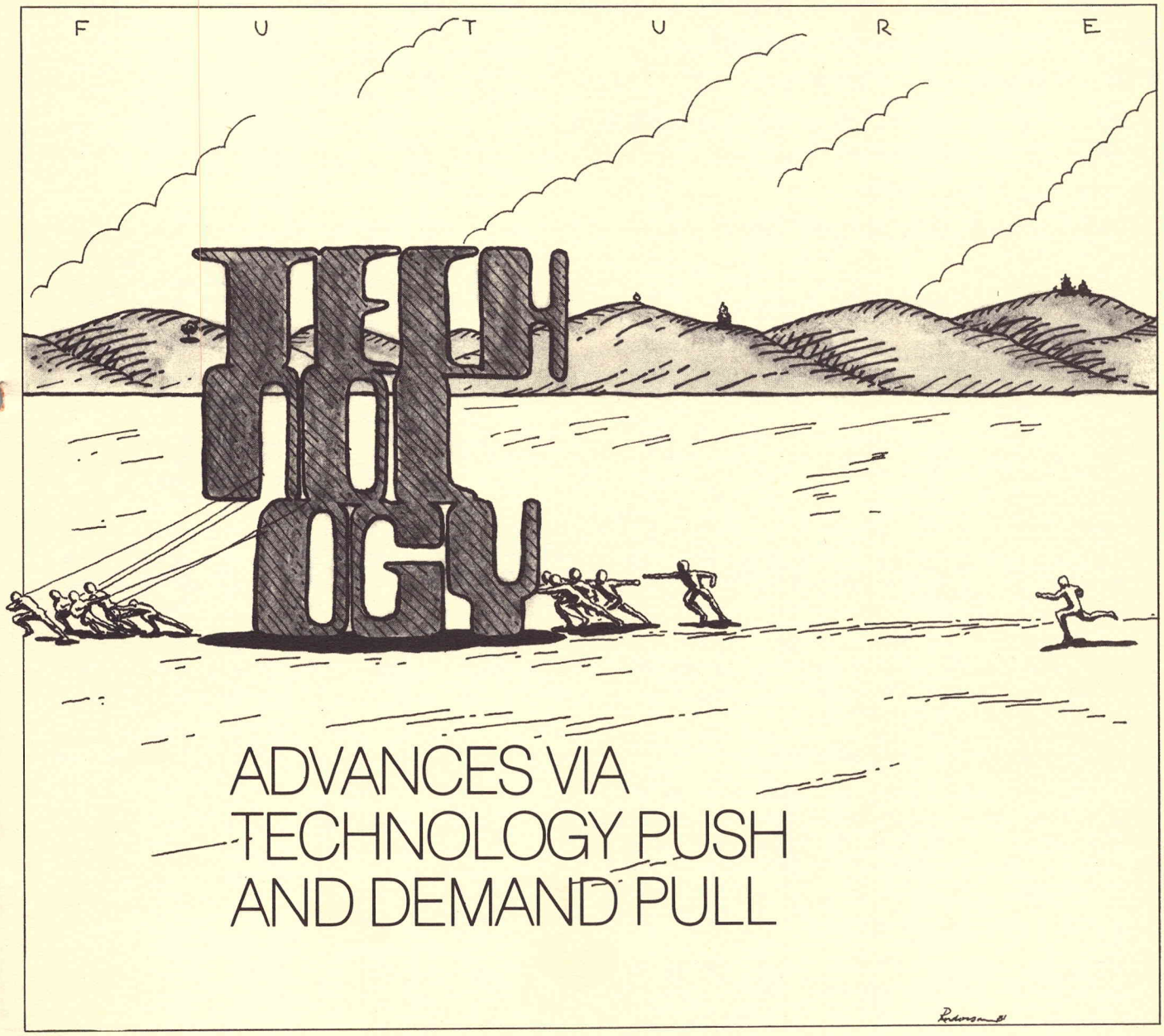
TEK INFORMATION FOR TECHNOLOGISTS

JULY 1981

TECHNOLOGY report

COMPANY CONFIDENTIAL



ADVANCES VIA TECHNOLOGY PUSH AND DEMAND PULL

Tektronix®
COMMITTED TO EXCELLENCE

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Why TR?

Technology Report serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community).

Contributing to TR

Do you have an article or paper to contribute or an announcement to make? Contact the editors on ext. MR-8934 or write to d.s. 53-077.

How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle, and the timeliness of the content). But the *minimum* is six weeks for simple announcements and as much as 14 weeks for major technical articles.

The most important step for the contributor is to put the message on paper so that the editor will have something with which to work. Don't worry about organization, spelling, and grammar. The editors will take care of those when they put the article into shape for you. □

COMPUTER SCIENCE INSTRUCTORS WANTED

Oregon State University is looking for adjunct professors to teach graduate-level computer science in the Tektronix MS Program. Instructors are needed for the following courses. Classes begin September 29, 1981.

CS 411G Assemblers and Compilers

CS 411G is the first quarter of a three-quarter sequence in language processor techniques. Topics include one-pass and two-pass assembly, symbol table, mnemonic tables, regular expression scanners, conditional and macro assembly, and code generation.

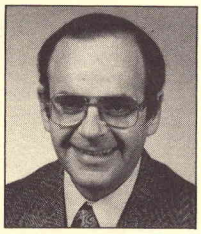
CS 511 SOFTWARE SYSTEMS

CS 511G is the first quarter of a three-quarter sequence in software systems design. A broad area of software engineering is covered. Topics are software lifecycle estimating, specification and design techniques, coding and maintenance techniques, testing and, at the instructor's option, proof-of-correctness and program complexity analysis.

Candidates should have a PhD in computer science or a related field. Exceptional applicants with a masters will also be considered.

If you are interested in teaching these courses—or similar courses—to industrial students, contact Laura Allen, Education and Training, ext. B-2381. □

FUTURE INSTRUMENTS: THE DRIVING FORCES



Arnie Frisch is an Engineer V in the Electronic Systems Laboratory. Arnie first joined Tektronix in 1964 and for seven years was program manager for spectrum analyzers. He left Tek in 1971 and rejoined full time in 1979. Electron microscopes and communication aids for the severely handicapped were his primary interests while he was away.

This article is based on Arnie's presentation at *Engineering Forum 21, IC Technology — Impact on Tektronix.* The Engineering Activities Council sponsors forums to promote the communication of engineers' views of technology to Tektronix management.

Technology Push and Demand Pull

There are two major factors that affect what semiconductor technologies will be used in our future instruments: *technology push* and *demand pull*. These factors are often difficult to separate. When technology enables the customer to do something faster, more accurately, or more conveniently . . . we in turn have to develop products to measure or function faster or more accurately or more conveniently — so that the customer can develop things that do things faster or more accurately — and so on.

Successful instruments usually result from a combination of both push and pull. All pull is not good because it results from a very competitive situation, one in which everyone recognizes the demand and can build the product. All push is not good because few customers will pay the premium required for the extra performance that is now possible, but for which the customer probably has little need. Figure 1 represents the range, from the highly competitive situation, where you have a 100% pull, to the very low competition situation that exists with a 100% push — optimum sales and profits occur with a combination of the two.

To produce a credible scenario for the future of instrumentation, we first must understand where we are and what we have been doing. To do that, let's look at the characteristics of the instruments introduced by Tek during the last four years.

Figure 2 shows us that the composition of these instruments is largely digital, or conversely, less analog; but we probably didn't need the figure to remind us of that.

Figure 3 compares our newer products on the basis of whether they incorporate a CRT or use one in a peripheral device. It shows that we are becoming less and less of a scope company.

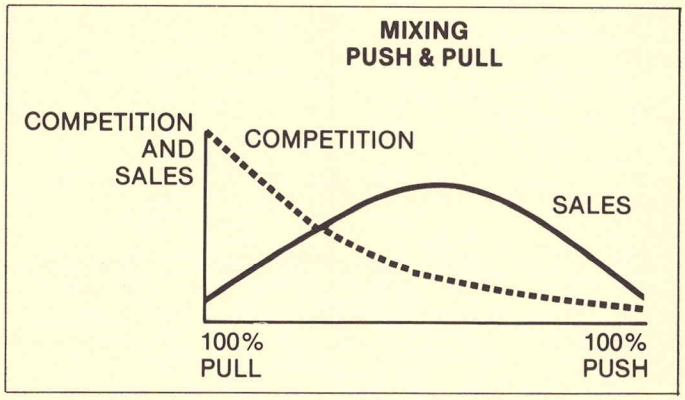


Figure 1. When technology makes something possible, customer demand is initially low. This is the all *push* point. At this point, sales are typically low. On the other hand, when the customer *demand pull* is high and competition is fierce, sales tend to be low for an individual vendor. At midpoint, neither all push nor all pull, the most opportunities exist.

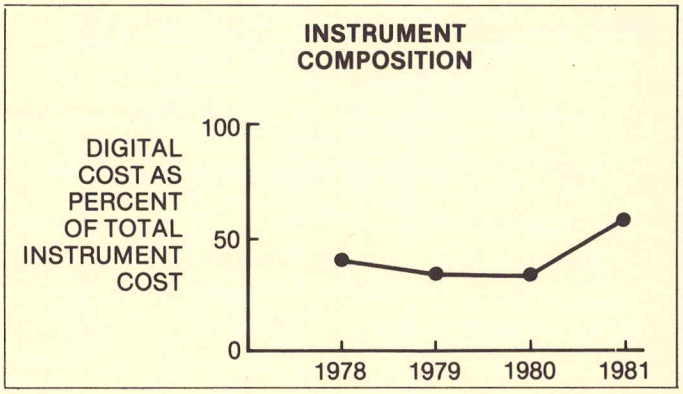


Figure 2. The percentage of cost represented by digital circuits has become significant.

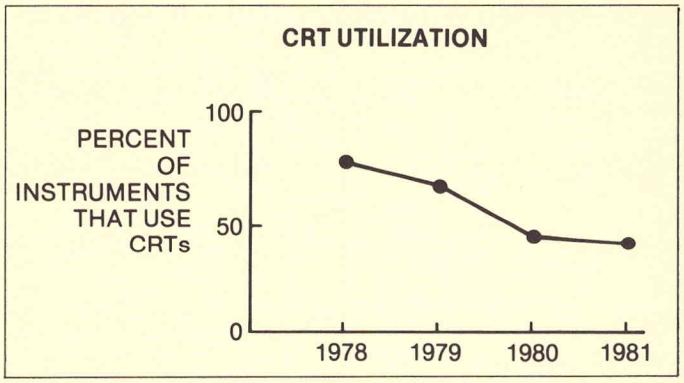


Figure 3. Today, fewer new Tek instruments employ CRTs.

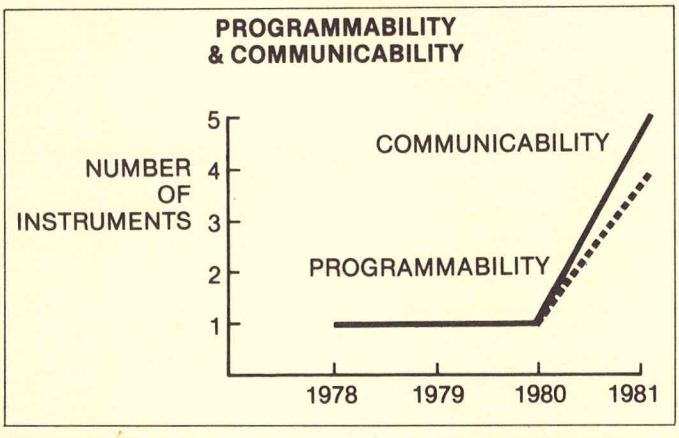


Figure 4. The changes represented in figure 3 have been gradual. In contrast, the increase of instruments featuring programmability and communicability has been dramatic.

Most of these trends are gradual; the factors involved have changed slowly from year to year. Figure 4 however, shows the remarkable increase of instruments having functional programability and the ability to communicate using machine intelligence. These instruments are a response to demand pull, of our trying to catch up with the market demands and competition. Just a few years ago, instrument programmability and communications were technology push factors.

However, the underlying market pull is not for programmability and communicability as such, these features are means to an end. The demand pull, today, is really for *low-cost-per-function*. We will see shortly why the market created this pull. But first, let's extrapolate from what we have just reviewed and predict future instrument characteristics.

Programmable Functionality

It is safe to say that products will continue to become more digital and programmable. These characteristics enable instruments to resolve the problems of functional and measurement complexity.

The push from technology will allow some major departures in instrument architectures and capabilities. Programmability will not merely change front-panel settings. Programmability will change the fundamental function of the instrument: I call this *programmable functionality.*

Figure 5 shows a simplified block diagram of an instrument. What is it? Well, its function is not defined. It might be a digital oscilloscope, but then it might very well be a spectrum analyzer, or something else. Its function depends on what is done with the input signal after it is digitized. This is a simple example of an instrument that has programmable functionality, but it is also an example of emulation of an analog system. Emulation may not be the best way to achieve programmable functionality.

The designer of a system, such as represented in figure 5, can emulate the performance of an analog instrument by cleverly selecting the parameters of the digital hardware and developing the right algorithms to make the digital aspect of the instrument *transparent* to the user. Unfortunately, the result of such a design approach can easily be an expensive digital equivalent of an instrument such as an analog storage scope — not a real advance in measurement capability or ease.

Because of push and pull, it is probable that future instrumentation will consist of a number of moderately complex modules that do not have an obvious generic-instrument function (such as spectrum analysis). The complex aggregate of such modules will be programmable to perform a widely varied set of stimulus-response tests. These stimulus/response testers will operate in both the frequency and time domain. They will solve a broad spectrum of test and measurement problems. The concept of such a system is diagrammed in figure 6.

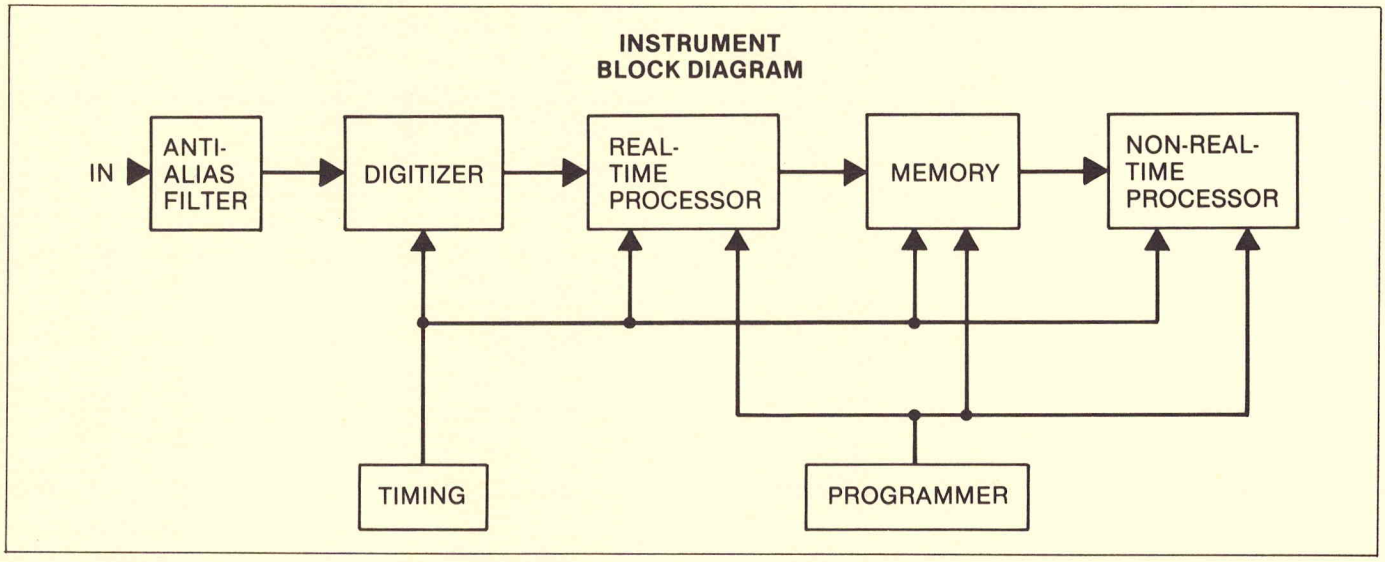


Figure 5. What is it? It could be a scope or a spectrum analyzer depending on how it's programmed. This, however, is not the instrument of the future; it does not have programmable functionality.

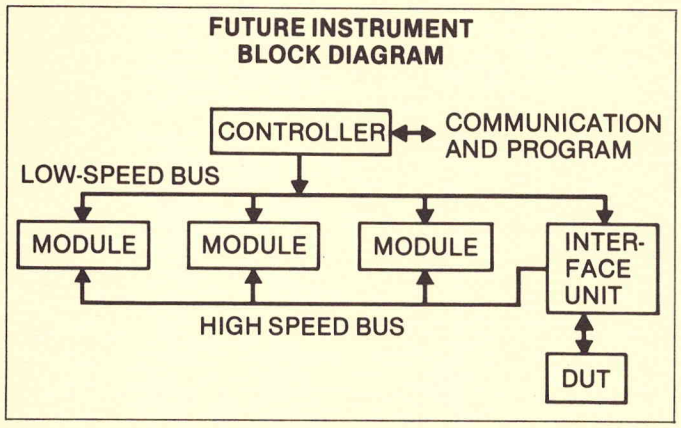


Figure 6. The instrument of the future? Perhaps. A system of relative complex modules, following the concepts in this block diagram, could be programmed to function as a stimulus-response tester, or a spectrum analyzer, a scope, or something else.

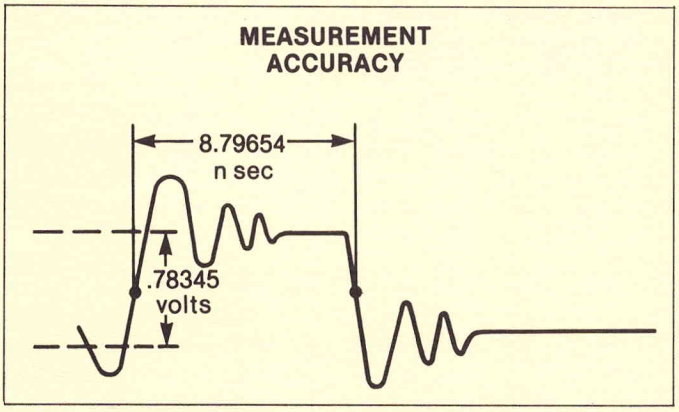


Figure 7. More customers are demanding precision and high resolution that conventional instruments cannot easily achieve. How do you make these measurements? How do you make large numbers of these measurements economically?

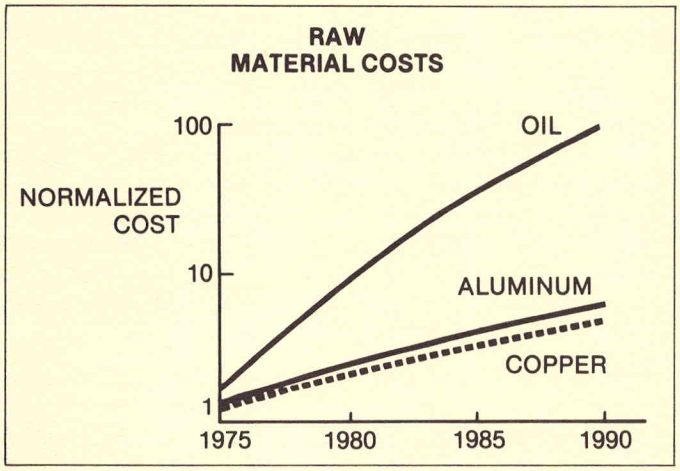


Figure 8. While the price of almost all other materials has increased, the price of silicon has remained relatively constant until recent years.

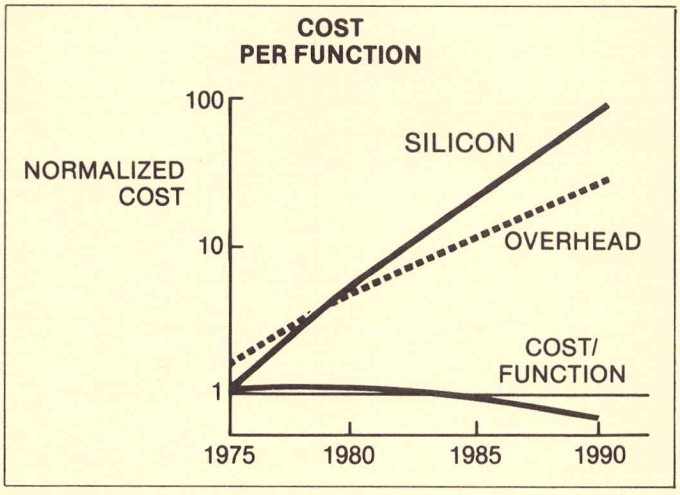


Figure 9. Even though the cost of silicon and overhead is now doubling about every four to five years, the increase of silicon functionality compared to silicon used has been even faster, doubling every two to three years. Thus, cost-per-function goes down with time, a trend made possible by increased programmability and communicability in silicon-based devices.

The Forces Pushing Programmable Functionality

Programmable functionality has the potential for creating instruments with significantly advanced measurement capability. Let's examine some of the forces that are pushing future instrumentation towards programmable functionality.

The requirements of our customers are becoming more exacting in such areas as precision and resolution of voltage and timing measurements. But our ability to achieve more precise measurements with conventional test equipment is limited. How do we make the measurements shown in figure 7? Simply digitizing an oscilloscope, or other instrument, does not solve this problem, especially when the converter is marginal on bits or its clock rate is marginal in relation to the Nyquist rate.

Because customer demand for test performance is expanding beyond the capability of conventional test equipment, some customers assemble large conglomerations of equipment, filling benches and racks and spilling over to the nooks and crannies.

The cost of making more accurate, more numerous measurements by conventional means is increasing rapidly. The availability of adequately trained personnel is falling, and salaries are rising. The cost of every part of the measurement device is rising and will continue to do so — *with the exception of silicon* (see figure 9).

More use of silicon-based devices reduces the cost of increasing measurement functionality. We can reduce the cost-per-function by giving instruments communicability and programmability, our machines can then reduce the drudgery of making many tests and measurements and, at the same time, improve throughput.

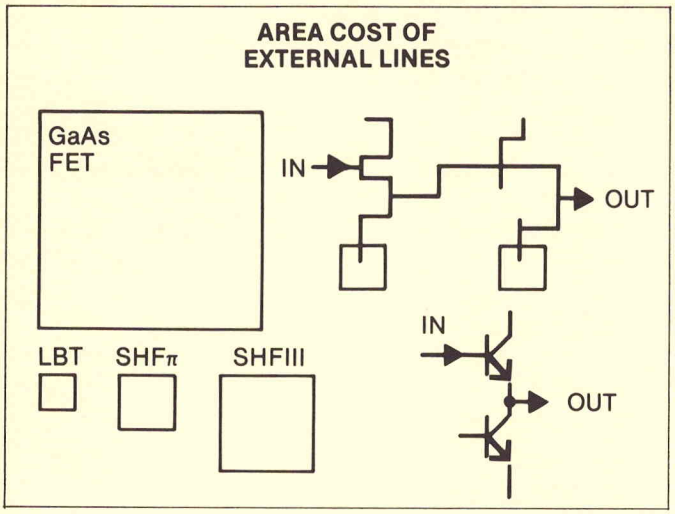


Figure 10. The relative areas required for various processes used in devices that drive external 50-ohm lines are shown here. Galium Arsenide is least efficient.

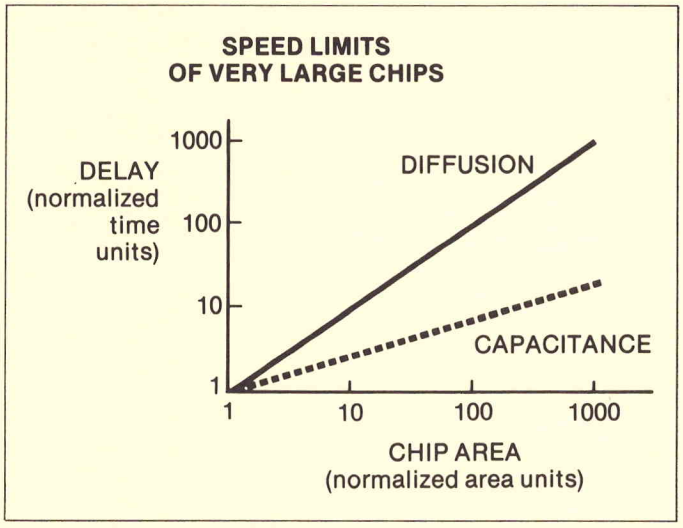


Figure 11. Dense circuits on very large chips are currently limited by diffusion delays. These delays can be overcome by using multilevel metal interconnects of fine lines such as employed in the Hewlett Packard 32-bit microprocessor (not shown).

What Semiconductors Will We Need?

Now that we have some background, we can reliably predict what semiconductor technologies we will need.

We are going to need a very high-speed interface technology to make programmable, transparent connections to analog and digital circuits. Part of this requirement can be met by any scaled process with adequate speed: bipolar or FET, Silicon or Galium Arsenide . . . or even Germanium.

But for a high-speed programmable, multiline analog interface, it is likely that we will need to develop an integrated mechanical-switch technology. In addition, analog-signal processing is likely to lean towards bipolar processes because they are better able to drive high-speed outputs.

In figure 10, we can see the area requirements of various processes if they are to drive external 50-ohm lines. You can see that the Galium Arsenide field-effect transistor (FET) is relatively inefficient with respect to area required, whereas the bipolar processes are much more efficient.

High-speed analog-to-digital converters will need a combination of accurately matchable analog comparators and fast, small-area digital devices. An example might be SHF III or SHFπ combined with "little bitty transistors" (LBT) or MESFETs. It is possible that some MESFET processes might be laser trimmable for very accurate matching, and thus allowing very small, fast 8-bit flash converters having about 5,000 FETs.

Digital devices of several classes will be needed. Very large chips are inherently speed limited by interconnect delay, while smaller chips are inefficient because of excessive I/O overhead. It is likely that several classes of gate arrays will be used to overcome these limitations.

Since very large tasks will be accomplished by these future ICs, there is very little need for them to use processes that are compatible since interfacing between ICs will be limited to a few lines. Therefore, we will see processes optimized to the size of the chip and even to the architecture. Gallium Arsenide will be useful for moderate-sized gate arrays, but will become capacitance limited in speed at larger sizes. However, more complex pipelined architectures will allow larger chips to achieve some speed advantage over silicon.

Current technology can be used to make large, low-density silicon-FET gate arrays. But dense circuits, which are currently speed limited by the diffusion delays in polysilicon (see figure 11), will have to use multilevel metal interconnects of fine lines as used in Hewlett-Packard's 32-bit microprocessor.

Conclusions

Finally, my view of the future of semiconductor technology is — pardon a pun — integrated. As complexities increase, technologies are becoming increasingly dependent on computers. Without significant computer resources, designing for anything of value is almost unmanageable. These computer resources will be needed most intensively at the early stages of IC design to estimate the performance obtainable from a given architecture and to devise and incorporate test capability and fault tolerance. Traditional test methods may not be of much value in the future because they don't assure proper functioning in the presence of transient faults, which become more likely as chips become scaled in size. Finally, these computers will be used to aid in the layout of chips, and to generate a data base for use in manufacturing and in maintenance.

All this implies an even higher level of technical operation and, again, integration of our traditional capabilities to successfully make the transition to the instrumentation of the future.

For More Information

For more information, call Arnie Frisch, ext. DR-5497. □

UNIVERSITY RELATIONS TEAMS FORMED

In an effort to build strong, highly interactive relationships with key technical universities, Tektronix has formed six University Relations Teams. Focusing on the top schools in the nation, the teams' objectives are:

- to build Tektronix' image as a high technology company,
- to influence university curricula and teaching research programs in a manner helpful to Tektronix, and
- to attract the top graduates to Tektronix.

The teams are organized around the major disciplines that are of primary interest to Tek: computer-aided design and computer-aided manufacturing (CAD/CAM), computer science, electrical engineering, manufacturing engineering and management, materials/physics/chemistry, and mechanical engineering. Each team has a leader and approximately five members; all product operations and manufacturing divisions, the Technology Group, and Central Manufacturing have team representatives.

The team leaders will manage the interface between the key universities and Tektronix for their respective disciplines.

The major elements of the program are to:

- establish liaison with key professors whose research is of interest to Tek,
- give technical presentations on-campus,
- fund research that can prove valuable to Tek through technological advancement,
- award equipment grants, and
- recommend funding for scholarships and affiliate programs.

Supporting the University Relations teams as liaison and coordinator is Jane Stayer. For more information, she can be reached at ext. B-5118. □

UNIVERSITY RELATIONS TEAMS

TEAM	LEADER
CAD/CAM	Jerry Sullivan, Manager, Computer Science Center, Technology Group
Computer Science	Dick Lemke, Manager, Logic Analyzer/ DCA Engineering, DAD
Electrical Engineering	R. Michael Johnson, Manager, TM 500 Engineering, ID
Manufacturing Engineering and Management	Don Blem, MRP Corporate Program Manager, Production and Materials Management
	John Eckholt, Manager, Industrial and Systems Engineering, Manufacturing
Materials/Physics/ Chemistry	Aris Silzars, Manager, Solid State Technology Group
Mechanical Engineering	Ed Strande, Manager, Mechanical Components, Lab Scopes, ID

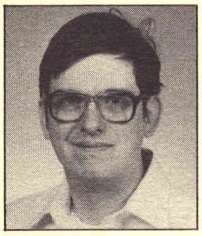
UNIVERSITY RELATIONS TEAMS CALL FOR PAPERS

The University Relations Teams are seeking engineers to give technical presentations at MIT, Stanford, and other well-known universities during the '81-'82 academic year.

The paper's subject matter should be of current technological interest in the areas of CAD/CAM, computer science, electrical engineering, materials/physics/chemistry, or mechanical engineering.

Contact Jane Stayer at ext. B-5118 for further information. □

A NEW DIGITAL IC DESIGN METHODOLOGY: THE INTEGRATED SYSTEMS APPROACH



Thomas Almy is a senior research engineer in the Computer Research Labratory, part of Applied Research. Tom joined Tektronix eight years ago after receiving his BS from Cornell and his MSEE from Stanford.

This article is based on Tom's presentation at *Engineering Forum 21, IC Technology — Impact on Tektronix.* The Engineering Activities Council sponsors forums to promote the communication of engineers' views of new technology to Tektronix management.

The Integrated Systems Approach is a new digital IC design methodology, sometimes called the Carver Mead Approach. We, in the Computer Research Laboratory, are now investigating this methodology through Stanford University's Center for Integrated Systems and the University of Washington's Northwest Regional VLSI Consortium.

I will talk about three aspects of the methodology:

- First, the purpose of this methodology: to enable digital system designers to design their own LSI and VLSI.
- Second, the techniques I used, as part of our investigation of the methodology, to design an IC.
- Third, I will conclude with what I view is the future of the Integrated Systems Approach. Today, this methodology is mainly experimental.

The Tall, Thin System Designer Can Design ICs

Why should you, the system designer, want to design ICs? First, it's faster to do it yourself because you do not have to wait for an IC designer to learn your design. And second, you are sure that the IC is exactly what you want every step of the way because you completely control the design process.

The digital-system designer can design integrated circuits by being "tall" — knowing a little bit about every step in the design and fabrication process — and by being "thin" — the designer doesn't have to know very much about any one step. This is the "Tall Thin Man" concept that is part of the Carver Mead Methodology.

The key concept in the methodology is that only the essentials be taught. This means that design rules are simplified, at the expense of IC performance and density and the signal aspects of the design are simplified to lumped resistance/capacitance (RC) networks.

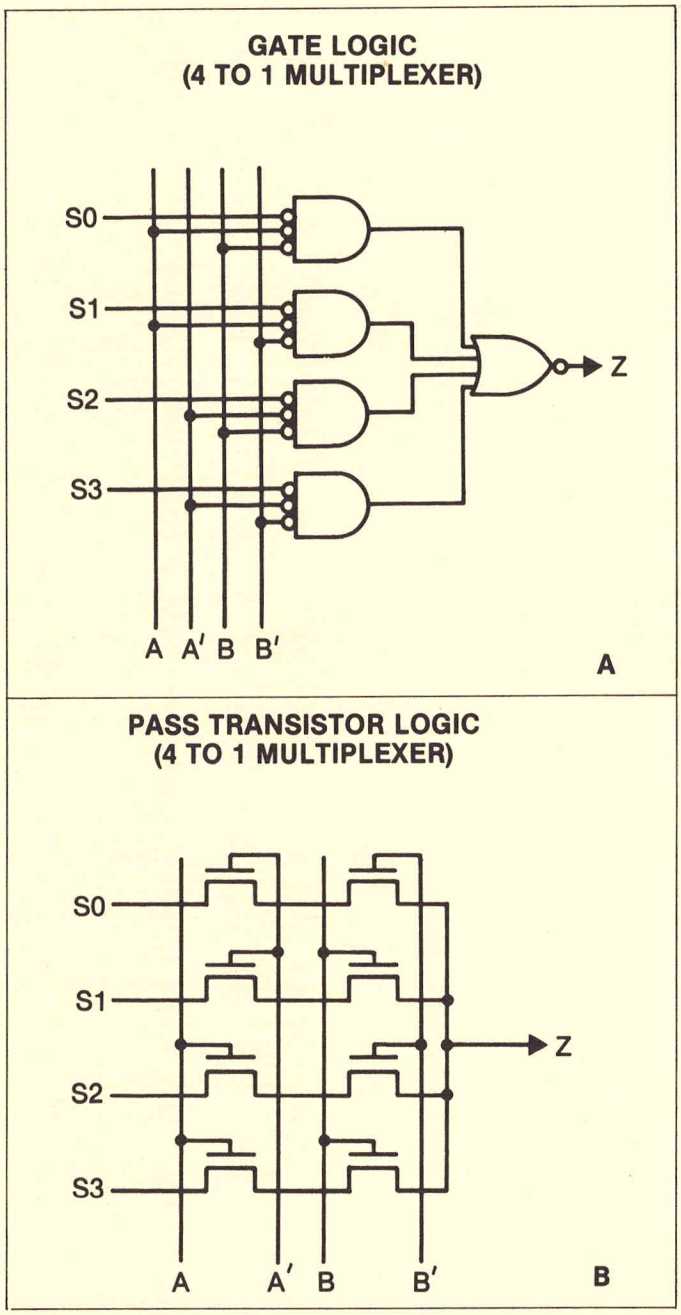


Figure 1. The Integrated Systems Approach stresses the employment of reliable, proven circuitry at the bottom design level: gate logic (A), which is much like TTL and pass-transistor logic (B), which is much like relay logic.

To insure design portability, Carver Mead stresses three things:

- Use design rules based on multiples of minimal resolution length (lambda). This allows straight forward scaling of the design. (There are some IC elements, such as pads, that are not scaled.)
- Employ a standard for design file interchange , such as CIF, to allow easy porting of cell libraries as well as the generation of multiproject chips.
- Control the processing within the margins set up in the design rules to ensure that chips will function.

Carver Mead stresses top-down design. That is, starting with a decision as to what high-level function the chip is to perform. This function is then divided into lower-level functions, such as programmable logic arrays, RAMs, arithmetic logic units, multiplexers, or busses. These functions may then be subdivided until a bottom level — simple cells of just a few transistors — is reached. This structured design approach is fast, less prone to errors, and easy to modify. However, to gain maximum benefit the project should also be well structured.

The approach also stresses using only reliable, proven circuitry at the bottom level. For that reason, only two logic implementation designs are allowed: gate logic (much like simple TTL) and pass transistor logic, which is similar to relay logic. (See figure 1.)

To improve throughput in the mask-making and fabrication steps and reduce overall cost, IC prototypes are placed on multiproject chips. Each chip has several designers' projects on it (as many as will fit), with only the pads from a single project bonded out on any one packaged chip (figure 2). Additionally, several multiproject chips are placed on each wafer. In this way, one wafer and several mask sets can provide dozens of projects with a couple of prototype parts apiece. The multiproject chip also reduced the processing cost per project substantially.

Designing An IC

Last summer at Stanford University, I used the Carver Mead Methodology to design a content addressable memory IC. It took me eight weeks, including the course work and learning the ropes. My design was roughly 3100 by 3700 microns, with five-micron features and 3000 transistors.

My first step, after conceptualization and the external specifications were settled — they were before going to Stanford — was to make a block diagram of the design and then convert it to a floor plan for the chip. The floor plan shows the major-function blocks in roughly the same positions and dimensions that they will have in the chip.

Next, I divided the major-function blocks into smaller and smaller pieces until the bottom-level cells were reached. At this point, I needed approximately 36 cell types, 14 of which were in the University's cell library.

Cell design is a bottom-up process. To demonstrate this process, let's follow the design of the two-input NAND gate in

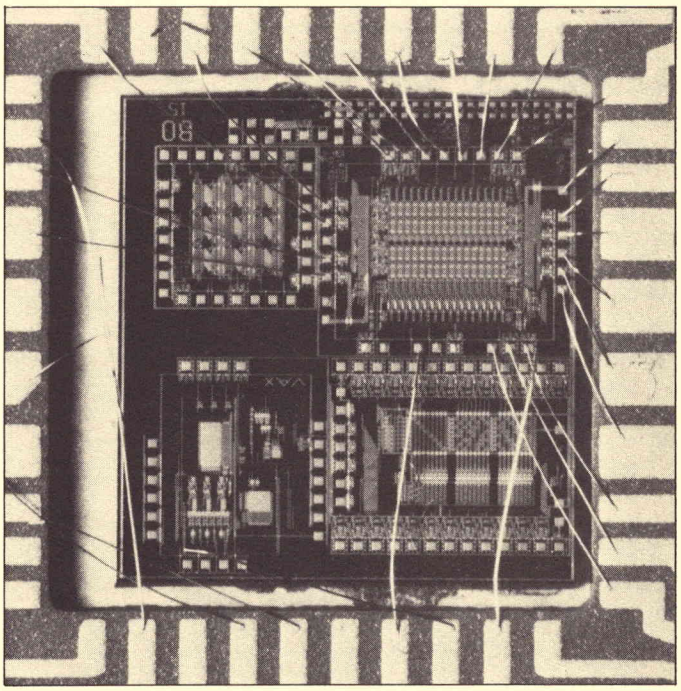


Figure 2. This multiproject chip contains four designs. My design is bonded out. Three other designers shared this chip, thus reducing individual project IC cost substantially.

figure 3. The schematic (figure 3A) is converted into a stick diagram (figure 3B). The stick diagram uses colors to represent the different layers of the integrated circuit. At this point, there is no concern with design-rules because the lines have no width. Designing this way is very simple; the only component is a transistor, which occurs wherever a red polysilicon line crosses a green diffusion line.

In figure 3B there are three transistors — because red lines cross green lines at three places. The black dot represents a connection cut (butt joint) between the red and green layers. The yellow area represents ion implantation which effectively converts one of the transistors into a pull-up resistor. There is a single metal interconnect layer, represented by blue, which is used to supply V_{DD} and ground.

After stick diagramming, the next step is to prepare design data for digitizing. For this step, data can be entered by graphic entry or by hand. In hand digitizing, colored pencils and quadrille paper are used to plot a two-dimensional *realization* of the design (figure 4).

Next, the cell is digitized by writing a procedure in one of several layout languages. Direct graphic digitalizing is done with a graphic-entry terminal or computer, which is what I did, using a Xerox Alto computer. (This was roughly four to five times faster than the few cells I laid out with colored pencils.)

After digitizing, all the cells were composed into arrays and the cells were interconnected using the computer, by writing program procedures to specify the design or using the interactive graphics computer.

After the complete design was entered, a set of programs were run to do design-rule checking and simulation. At Stanford, these programs ran on a Digital Equipment VAX 11/780. I used roughly 2.5 hours of CPU time, including the extra passes I made after finding errors.

Fabrication and Testing

At this stage, I released the design to have masks made and to be fabricated on a multiproject chip. These steps were coordinated by the Information Sciences Institute (ISI) of the University of Southern California. The fabrication was done by American Microsystems, Inc. (AMI). Such fabrication companies are called silicon foundries — foundries don't design, they just turn out chips. Because this was ISI's first attempt as a coordinator, turnaround was roughly three months. In the future, it should be one to two months.

With my chips completed, the hard part began — testing. Universities, where most of the integrated systems research takes place, have largely ignored testing. However, I made my chip testable.

After returning to Tek, I tested my content addressable chips with a custom test fixture. Of the seven delivered to me by AMI, two did not function. The remainder were completely functional — except for a single error, a logic error that only affects applications where the chips are cascaded. This error will be easy to fix.

I am now redesigning my chip for greater capacity. My goal is to complete a Carver Mead design process here at Tek.

The Future Of The Integrated Systems Approach

In a sense, what I did at Stanford represents the future. Although their facilities are crude and limited, that type of facility will evolve to be tomorrow's efficient and reliable IC-design facility. Tomorrow, the system designer will routinely design ICs and thus be free of the constraints of depending on an IC designer.

It was fun to design that chip last summer, but I wouldn't want to do another design at the same level. Instead of designing at the transistor level, it would be more efficient and more error-free to design with higher level functional blocks such as programmable-logic arrays, RAMs, arithmetic-logic units, busses, and multiplexers. And the ability to build up systems from high-level parts — much as today's designers use TTL dual in-line packages on an etched circuit board, but with more flexibility — would be a major improvement over the process I followed at Stanford.

I envision design systems that have high-level entry facilities. Designing at the transistor-level design can be best performed by professional IC designers.

We mustn't ignore simulation, even in the ideal quick-turnaround environment. Universities are making some efforts here, even though they have been ignoring testing of the final part.

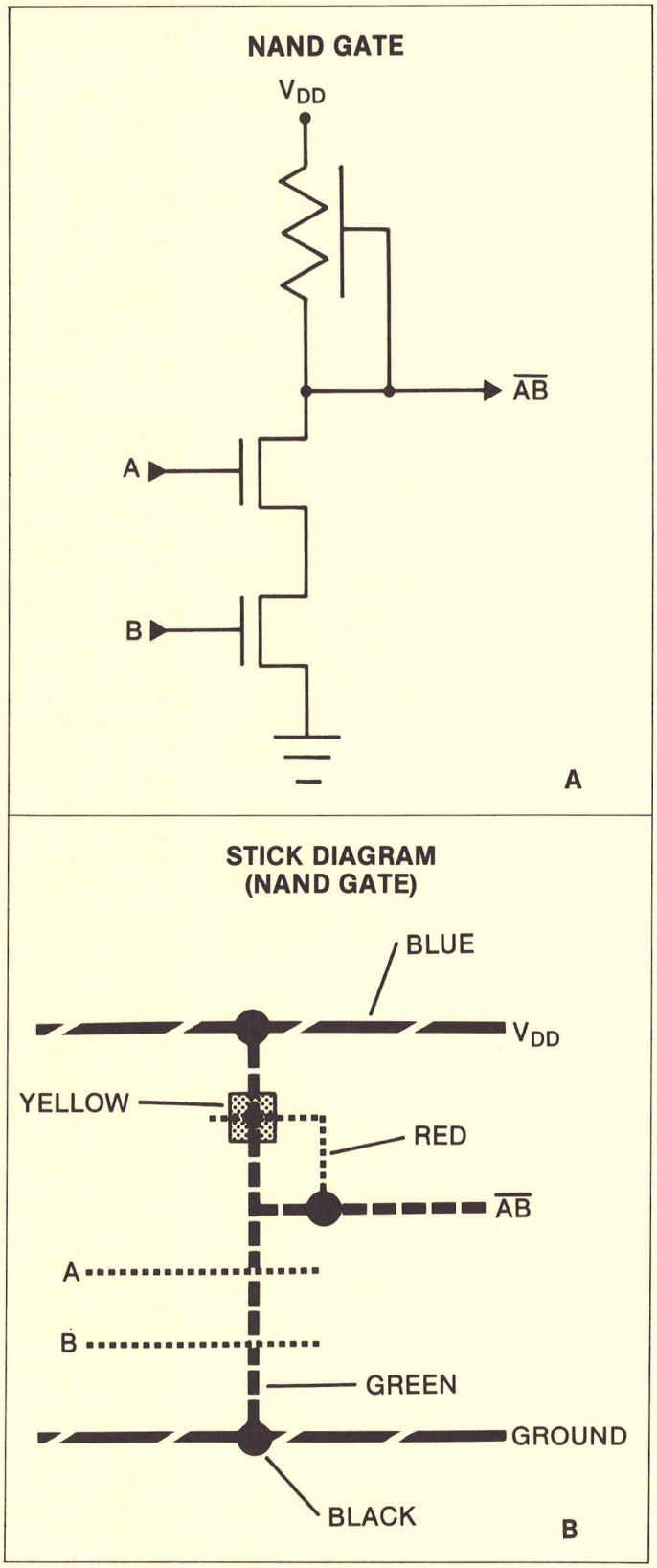


Figure 3. In the bottom-up design process, the schematic for a two-input NAND gate (A) is redrawn as a stick diagram (B), which uses colors to represent the different IC layers. The next step, digitizing, can be made with a graphic entry terminal, or by hand as shown in figure 4.

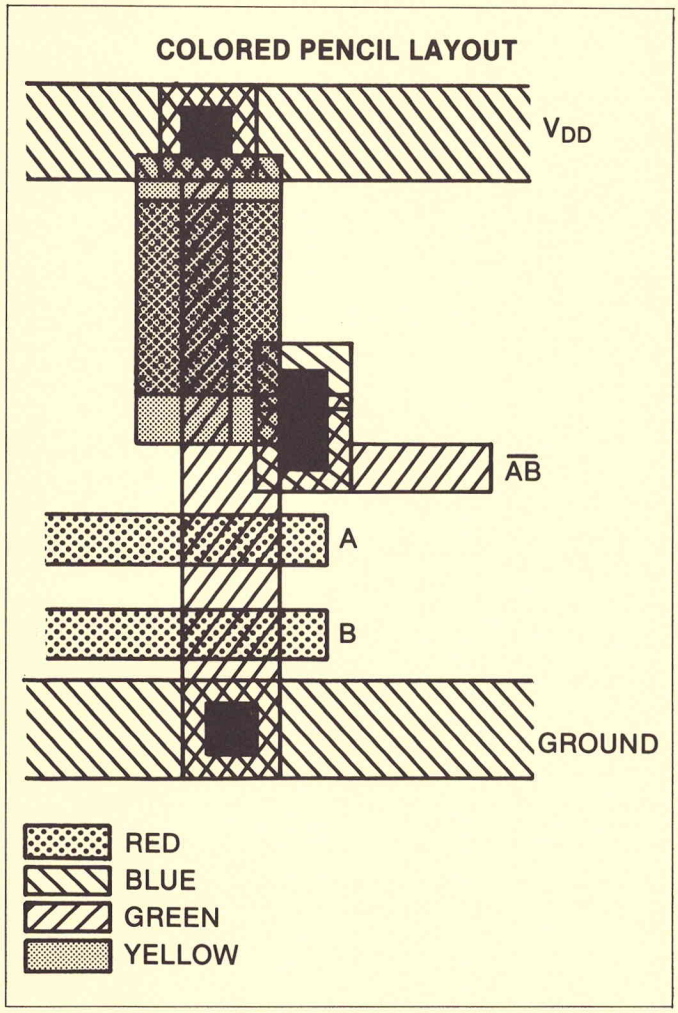


Figure 4. This figure is the result of defining the location and dimensions of IC elements on quadrille paper with colored pencils. This step is an alternative to using a graphic entry terminal for digitizing.

There is a need for design systems that are independent of technologies or processes. The system designer wants to design an IC without having to consider whether it is going to be fabricated in NMOS or I^2L or ECL — or worrying about having the design rules optimized for individual processes. When only the logic design needs to be considered, the design program itself can generate the circuits appropriate for the selected technologies and follow the appropriate design rules. Not only does such a program remove a burden from the designer, but it also allows quick changes to other technologies or processes after the design cycle is completed.

Design systems of the future will provide, invisible to the designer, testability features. Race conditions will be checked for and eliminated and the internal state will be loadable and observable. Redundancy may be built into ICs for high reliability. Test vectors will be automatically generated. The goal of the Carver Mead Method is to have reliable, testable chips without interfering with the flow of system designer's ideas.

I feel that the Integrated Systems Approach will prove to be a boon for system designers, allowing them to quickly and efficiently bring their designs to fruition.

For More Information

For more information call Tom Almy, ext. B-6188. □

ASCII & GPIB CODE CHART

B7 B6 B5 / BITS / B4 B3 B2 B1	ø ø ø	ø ø 1	ø 1 ø	ø 1 1	1 ø ø	1 ø 1	1 1 ø	1 1 1
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ø ø ø ø	0 **NUL** 0 0	20 **DLE** 10 16	40 0 **SP** 20 32	60 16 **0** 30 48	100 0 **@** 40 64	120 16 **P** 50 80	140 0 **`** 60 96	160 16 **p** 70 112
ø ø ø 1	1 GTL **SOH** 1 1	21 LLO **DC1** 11 17	41 1 **!** 21 33	61 17 **1** 31 49	101 1 **A** 41 65	121 17 **Q** 51 81	141 1 **a** 61 97	161 17 **q** 71 113
ø ø 1 ø	2 **STX** 2 2	22 **DC2** 12 18	42 2 **"** 22 34	62 18 **2** 32 50	102 2 **B** 42 66	122 18 **R** 52 82	142 2 **b** 62 98	162 18 **r** 72 114
ø ø 1 1	3 **ETX** 3 3	23 **DC3** 13 19	43 3 **#** 23 35	63 19 **3** 33 51	103 3 **C** 43 67	123 19 **S** 53 83	143 3 **c** 63 99	163 19 **s** 73 115
ø 1 ø ø	4 SDC **EOT** 4 4	24 DCL **DC4** 14 20	44 4 **$** 24 36	64 20 **4** 34 52	104 4 **D** 44 68	124 20 **T** 54 84	144 4 **d** 64 100	164 20 **t** 74 116
ø 1 ø 1	5 PPC **ENQ** 5 5	25 PPU **NAK** 15 21	45 5 **%** 25 37	65 21 **5** 35 53	105 5 **E** 45 69	125 21 **U** 55 85	145 5 **e** 65 101	165 21 **u** 75 117
ø 1 1 ø	6 **ACK** 6 6	26 **SYN** 16 22	46 6 **&** 26 38	66 22 **6** 36 54	106 6 **F** 46 70	126 22 **V** 56 86	146 6 **f** 66 102	166 22 **v** 76 118
ø 1 1 1	7 **BEL** 7 7	27 **ETB** 17 23	47 7 **'** 27 39	67 23 **7** 37 55	107 7 **G** 47 71	127 23 **W** 57 87	147 7 **g** 67 103	167 23 **w** 77 119

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1 1 ø 1	15 D CR 13	35 1D GS 29	55 13 2D − 45	75 29 3D = 61	115 13 4D M 77	135 29 5D] 93	155 13 6D m 109	175 29 7D } 125
1 1 1 ø	16 E SO 14	36 1E RS 30	56 14 2E . 46	76 30 3E > 62	116 14 4E N 78	136 30 5E ^ 94	156 14 6E n 110	176 ~ 30 7E 126
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KEY

octal 25 PPU
NAK
hex 15 21

GPIB code
ASCII character
decimal

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IEEE STD 488-1978
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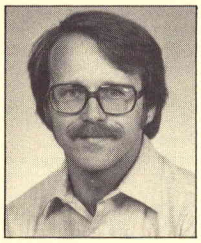
MAKING CUSTOM MOS AN ACCESSIBLE TECHNOLOGY



Don Larson has been a MOS/LSI Designer in Monolithic Circuits Engineering (MCE), part of the Technology Group, for five years. Previously he was a bipolar designer in MCE. He joined Tektronix eight years ago. Don has an MSEE and a BSEE from the University of California at Berkeley.

This article is based on Don Larson's presentation at *Engineering Forum 21, IC Technology — Impact on Tektronix.* The Engineering Activities Council promotes forums as a means for engineers to communicate their views of technology to Tektronix management.

Few MOS custom integrated circuits have been used in Tektronix instruments. This article will point out those barriers that have prevented custom MOS from being designed into Tek instruments, indicate how that situation is changing, and show how the goal of the IC Design group is to give the instrument designers easier access to silicon technology.

Why We Haven't Used MOS

I believe widespread use of MOS ICs is essential if Tek is to stay competitive. Until recently there were many reasons why MOS circuits were not used in TEK instruments:

- First, there was just no need for an MOS circuit in many instruments. Those instruments contained many analog parts, but few digital components. And where an MOS circuit could be used, suitable standard products were available to implement the required function.
- The long development time prevented or discouraged many designers from placing a custom IC in their product. It often took a year or more before the first parts were available for evaluation.
- The design project leader found the custom IC process to be difficult to control and schedule. Schedules were long and there were so many variables that maintaining the schedule seemed impossible.
- To the designer, the availability of MOS wafers has appeared unreliable. It has taken a long time to get an in-house MOS process on-line and there have been problems maintaining a stable process.
- And finally, chip performance has been inadequate. The first MOS processes implemented had difficulty achieving TTL speeds — and that level of performance is essential if there is to be widespread use of MOS parts.

MOS ICs — A Good Choice Now

So what has changed? Why should a designer now include an MOS IC in his product?

The nature of our instruments is changing. More products are being designed with a digital architecture. This creates more opportunities for using custom MOS ICs. In fact, many new instruments will be impossible to implement without custom MOS circuits. And more than ever, there is a need to lower manufacturing cost, something custom ICs can do — especially in systems that contain many digital components.

A microprocessor today can require 10 to 20 TTL support ICs — some of which implement medium-scale-integration functions. This number of TTL gates can be done economically with a custom IC. So, even when a microprocessor is to be used in an instrument, a custom IC might make an appropriate peripheral or support chip.

We must also consider the competitive advantages gained by designing with custom MOS. Designing with off-the-shelf components does not provide a technology barrier. We have the technology available, let's use it to uniquely enhance our products to gain a competitive edge.

Reducing Chip-Design Time

I believe chip-design times have been the main barrier to the increased use of MOS at Tek. We in the IC group must provide new techniques and tools to enable the business-unit designers to drastically reduce design times. This is why we are now developing more structured design methods as well as increasing our computer-aided design (CAD) efforts to reduce turnaround time for IC prototypes.

Figure 1 shows the basic steps in the IC design process. It can take anywhere from 2 to 4 months for design and simulation. Another 3 to 8 months can be spent in layout. And it can take 1 to 2 months for fabrication and packaging. So once the chip is defined, the designer in the business unit will see prototype parts in from 6 to 14 months.

Gate Arrays

A design methodology that can reduce turnaround time is gate arrays, which are fixed structures of transistors personalized to the designers' needs by the interconnections selected — all other steps in the process are the same for all circuits. Gate arrays can reduce turn-around times in all phases of the design process once the chip has been defined.

Turnaround time is reduced because the gate array restricts the designer's options. Because there are only a fixed number of identical gates in a gate array, the designer can only choose how they are to be interconnected. This is done by developing a logic diagram using only the number and type

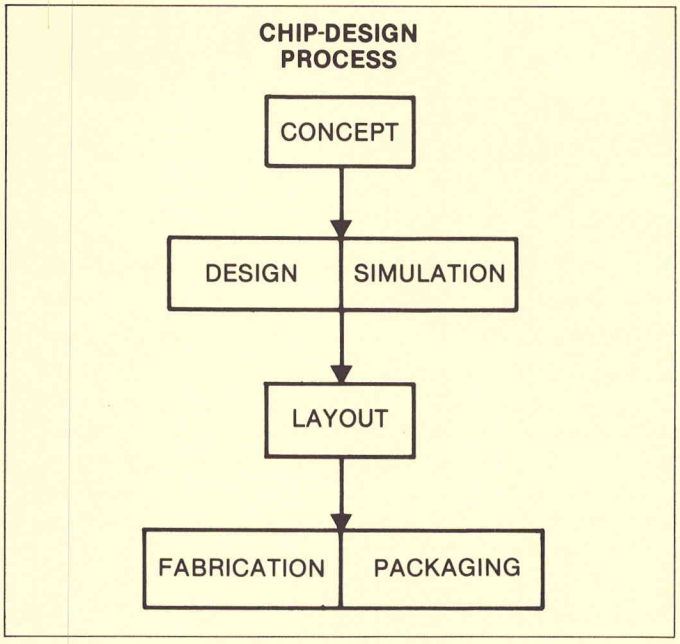


Figure 1. The basic steps in the MOS IC design process take 6 to 14 months.

of gates available in the array. In addition, the performance of the gates in the array can be precharacterized, thus reducing the time required to simulate the circuit.

The regular structure of the gate array enables CAD tools to interconnect gates automatically. But even without CAD, manual layout is simple and quite fast. Layout times are often just weeks or even days. With CAD, layout can be a matter of hours. Because only the interconnect is customized for each circuit, metallized wafers can be stocked, making very rapid prototype turnaround possible.

Gate arrays provide a value-engineered approach. That is, we can trade increased chip area — and therefore increased parts cost — for reduced development time and cost. For the relatively small number of parts required over the life of many instruments, this is a good tradeoff.

Standard Cells Also Reduce Design Time

Standard cells also can reduce design and layout time. Standard cells are arrays of predefined cells arranged and interconnected on a predefined grid. The predefined cells are stored in a user library. The circuit designer selects the needed cells. Typical cell functions include single gates, latches, and registers. New cells can be defined and added to the library as required.

Although standard cells reduce turnaround time, fabrication time is not reduced because all mask layers are unique for each circuit. Therefore, it is not possible to stock wafers at any step in the process.

Standard cells have several advantages over gate arrays. First, they have higher density, and therefore lower cost, this is achieved by placing only the required gates and cells on the silicon. Second, standard cell circuits can be designed to run as fast or as slow as required.

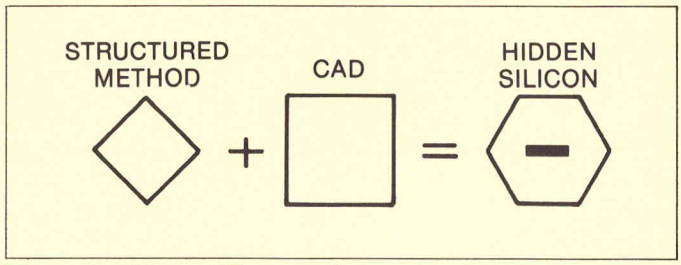


Figure 2. Hiding Silicon — A structured design method, such as gate arrays, used with computer aided design removes silicon processing from circuit design consideration.

On the negative side, the standard cell is harder to design than the gate array. There are more variables for the instrument designer to deal with — more decisions to be made. Which cells to use? How are the cells to be placed on the circuit? And since wafers cannot be stocked, obtaining prototype parts employing standard cells is slower than with gate arrays.

MOS, An Available Technology

In the past year, the Tek MOS Lab has demonstrated that it can reliably supply MOS wafers. At this time there are no MOS parts on shortage status and all prototype circuits have been fabricated promptly. In addition, all production processes have a second source readily available for back-up processing.

Our goal, in the MOS Design group, is to make access to a custom IC as close as the nearest computer terminal. New computer aids and new design methods will enable the designer to design an IC with familiar tools and produce results quickly. No longer will the designer be confused, intimidated, or frustrated by the technology.

When the correct design methodology is used, we can "hide" the silicon from the designer. That is, the instrument designer does not have to deal with silicon; the circuit is the only concern. If a structured methodology coupled with CAD is used, the designer need only generate accurate, testable logic. The designer does not have to worry about the details of layout and fabrication and can be confident that these portions of the chip design process will be carried out quickly.

As for performance, processes available today, such as scaled NMOS and iso-CMOS, can beat TTL performance. For many applications, speed is no longer a barrier to using MOS.

MOS Must Succeed At Tektronix — And It Can.

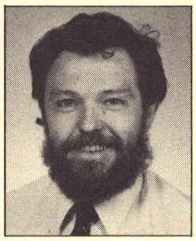
With CAD and structured design methods, design turnaround times can be acceptable. MOS processes now available in the MOS Lab have the performance to meet the needs of the business units and delivery is reliable. But most important, the business units will demand access to the technology. It is the responsibility of the IC Design group to provide that access. And it is the responsibility of the business unit to help and support us.

For More Information

For more information, call Don Larson, ext. DR-4078. □

PHYSICIST IV

JERRY MURCH



Jerry M. Murch, Terminals and Displays, part of IDD, ext. W1-3858.

Engineer/Scientists IVs and Vs serve as technical resources both inside and outside the company. To increase their visibility to the Tektronix technical community, *Technology Report* is publishing a series of profiles of these individuals.

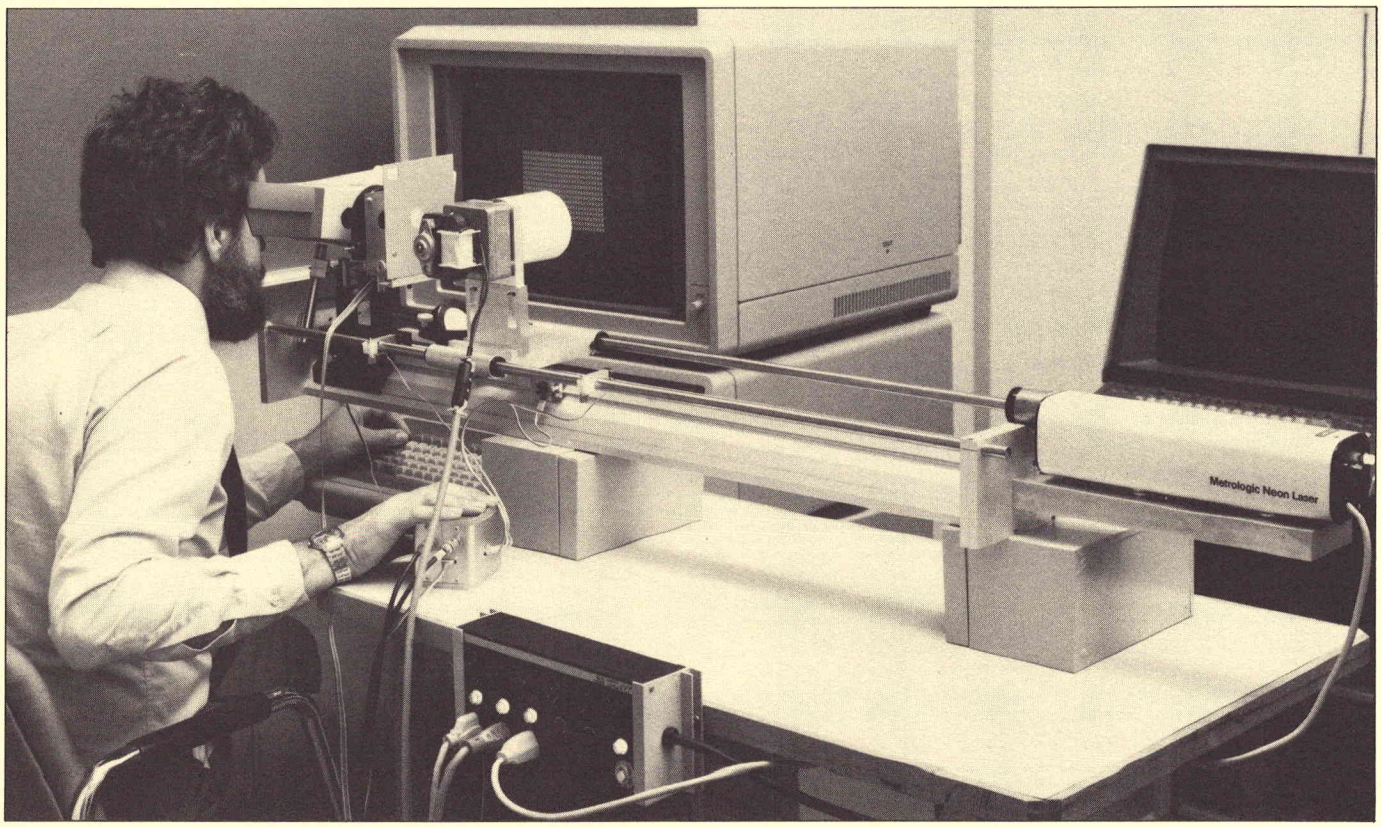
The first person to use a wheel did not worry about rolling resistance. The user of the first cathode-ray tube didn't worry about viewing fatigue or efficient data display. But, today, after millions have used CRTs and data displays have become pervasive, companies such as Tek are concerned about those factors. That is why Jerry Murch is here.

Jerry Murch is a *perceptual physicist* specializing in color vision. He employs his knowledge of human factors, the physics of light, the physiology of vision, and the psychology of perception to better understand the complexities of data display.

Jerry is analyzing the "rolling resistance" of data display — viewer fatigue. Are people fatigued by viewing data displays? If they are, what causes that fatigue? What relieves that fatigue?

Jerry Murch is one of a worldwide group of people trying to answer those questions — and more. Is there an insidious eye hazard from raster displays? How can we communicate better via the CRT? Again, facts and measurements are needed, as well as our understanding of how people see the patterns of light that constitute a CRT display. How does a CRT display 'conflict" with the physiology of vision that evolved in response to a sunlit, outdoor environment — a "friendly" environment, no flourescents on the ceiling, no flourescing screens on the console?

Tektronix builds information display systems which must be matched to the visual capabilities and capacities of the users of those systems. We know that such matching needs to be an integral part of the design and development process. But how can we match without learning more? We don't have the required knowledge.



Now that color data displays are common, the industry is finding that it does not know enough about the process of color vision. Questions that scientists never anticipated are being asked.

For example, we really don't know much about light. Theories about electromagnetic waves and quantum mechanics "work" to some extent, but not well enough for many purposes. Much about the nature of light still eludes modern physics. And we don't know enough about the physiology of vision, particularly as it applies to data display.

In the physical (real) world, the receptors in the eye seem to react to an object's edge with a Gaussian response. In a display, the CRT beam sweeping through a data point also produces a Gaussian-shaped pulse of light, which may confuse the human system of vision. If the sharp edges of the real world are processed as Gaussian edges, what happens when what we see already has a Gaussian edge? Perhaps part of the answer is in the psychology of perception.

Perception is how the brain interprets the electrical signals that are, in turn, a response to light by the transducers (receptors) of the eye.

Jerry's task is to piece together information from three disciplines — physics, physiology, and psychology — in order to improve display systems.

In his investigations, Jerry is seeking objective measurements of user reactions by using measuring tools such as the optometer. The optometer, with a human subject's help, determines where the subject's eye is trying to focus. Perhaps the human visual system can't lock focus on a data point of light with Gaussian shapes — eye muscles that are continuously trying to focus will soon tire. (Incidently, there seems to be positive value to middle-age vision. The lack of focusing abilities in stiff older lenses apparently eliminates the fatigue caused by continuously trying to focus.)

In his work, Jerry intends to evaluate the viewability of current display technologies as well as to simulate an "ideal" CRT display by projecting an image onto a CRT screen from a transparency. This image can be varied to assess how well the visual system deals with a specific display characteristic. A theoretically ideal display can thus be determined. The next step is a challenge to engineering technology: *how close can we come to building the ideal display?*

Jerry came to Tek last Fall from Portland State University, where he was a professor of psychology. He holds a doctorate of natural sciences (physics, physiology and psychology) as well as a masters of science. Much of his work in the past twenty years has been in color vision. He is a veteran in his field, having studied and taught in various German and American universities and has presented or published extensively here and abroad.

Technology Report asked Jerry to comment on the differences between the academic world and Tek. His response: "It's not all that different . . . but response to your work tends to be faster. Academic research gets published and then the researcher waits — the feedback is slow and low key. If the work is well received, it is cited in other papers. Then, after a year or more, the researcher counts citations. In contrast, results from industrial research are regularly evaluated for potential use. If all goes well, your work is usually incorporated in a product. You can touch it and show it to others."

For more information or to participate in the viewability project as an observer, call Jerry, ext. W1-3858. □

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If you have questions other than equipment requests, call Ray Barrett, manager of Central Pool Administration, ext. B-1787 or John Lasswell, manager of Metrology/Equipment Management, ext. B-1774. □

A BRIGHT AND COLORFUL FUTURE FOR DVST

Jon Reed is the vice-president and general manager of the Information Display Division. Jon spent six years in CRT Engineering, the last year as manager. In addition, his three years as IDD Manufacturing manager, three years managing the OEM effort and serving for the past year-and-a-half as Director of Corporate Marketing has given Jon many views of the subject of his article.

Jon Reed, in a talk given at the annual Frost-Sullivan Conference, whose subject was the Assessment and Forecasting of Computer Graphics, predicted "another dimension to DVST Technology." This article, based on Jon's talk, details the features and enhancements that make the future for Tek DVST products " bright and colorful."

Direct-view storage tube technology has a bright and colorful future in the 80's.

I base that prediction on recent enhancements as well as on the development of altogether new features — features that I believe will add another dimension to DVST technology.

In the past the DVST's strong points have been:

- very high resolution,
- low cost compared to competing display technologies, and
- flicker-free display.

Its disadvantages were:

- low interactivity,
- short tube life,
- dimness, and
- low contrast.

In the future, we will maintain the DVST's high resolution and continue to meet the challenge that inexpensive memory is presenting to the traditional cost advantage of the DVST. Even better, emerging technology will continue to advance interactivity, life, brightness, and contrast.

Reviewing DVST Fundamentals

Before we look more closely at the future of the DVST, let's review basic DVST technology.

The major elements of the DVST are the writing gun, flood guns, and phosphor target (figure 1). The target includes a transparent conductive layer that provides a foundation for an array of collectors. The writing gun — in the neck of the CRT — is negative relative to the target. The flood guns sit on the back wall of the CRT funnel.

The DVST is normally used to display information stored on the screen. In that mode, the writing-gun's beam scans — that is, writes on — the target, creating a stored charge that is positive, thereby attracting the flood gun electrons, which cause the phosphor to luminesce. The unwritten areas of the target remain at a much lower potential than the written areas.

Once the information has been stored, there's no need to refresh it — it continues to luminesce. But if that's the case, then how do we display new information to replace what is already stored on the screen? We have to erase.

We erase by applying a two-level erase pulse to the target. The first part of the pulse makes the whole target more positive, thereby attracting flood gun electrons, effectively writing the whole screen. The second part of the pulse lowers the target potential — thus erasing the screen.

Write-Through

What if we want to change only a small part of the information on the screen? We would have to erase the whole screen — which takes about a second — and then rewrite the old as well as the new information. At low data-transmission rates, rewriting the whole screen with information can take several seconds.

A technique called *write-through* was developed to avoid much of the delay in erasing and rewriting. In this technique, the beam writes the new information, with just enough current to make the phosphor luminesce but not with enough current to store the information. Continuously rewriting the new information — a process called *refresh* — maintains its luminance.

Refreshing is similar to the principal action of raster scan except that the high-resolution of the DVST display is retained. Because the target is a continuous and not a discrete dot or stripe target, the resolution is limited only by the writing-beam spot size. The DVST application of write-through is typically known as *directed-beam refresh.* The discrete nature of a raster-scan or the shadow-mask type of target structure is not a limiting factor in DVST. Therefore, diagonal vectors, for example, do not show irregularities (jaggies) as they would on a raster-scan display.

The resolution of a DVST is equivalent to that of a 1000-line raster display on a 19-inch CRT. There are high-resolution color raster displays on the market that approach DVSTs for number of lines per display. But, that is in one direction only — vertically. These raster displays still show jaggies, and more prominently than the DVST because the raster-scan display is on a discrete dot target.

Advances In The 70s

Now, let's take a look at other advances in DVST technology. In the 70's, we increased screen size from 11 inches to 25 inches — a more than two-fold increase that allows the user to display five times more alphanumeric characters and vectors.

Also during the 70's, we increased the life of the phosphor more than five-fold. That means most users can now use their CRTs 40 hours a week for four to six years. Other advances were: minimizing the flash that occurred during each screen erase, and the addition of circuitry that allows the user to copy parts of the screen rather than the whole screen. This feature is important if the screen is densely packed with information.

Recent Advances

Enhanced Interactivity

Historically, DVSTs have been looked at as noninteractive display devices — you put information on the screen; it's stored there; and then, if you're through using the information, you erase the screen and rewrite it with new information.

In the last five years, we have been exploring and enhancing the write-through feature. As we saw earlier, write-through is functionally the same as the refresh mode in raster technology; therefore, it's easy to change. With write-through, you can put information on the screen and it's viewable, but it's not stored. Write-through, then, has greatly enhanced the DVST's interactivity.

Another factor enhancing interactivity is the use of faster data links. DVSTs have typically been used in 300- to 1200-baud applications because most users thought of DVSTs as low-cost devices that should be connected to low-cost data transmission lines. Well, those low-cost lines are slow.

Now, however, DVSTs are being used at 19.2 kilobaud, which is fairly fast. The DVST's calculated limit is about 0.5 megabaud in point-plot mode and 1 megabaud in vector mode. At those rates, the electronic hardware would be the limitation in writing a DVST display. It would take some direct coupling and high-speed hardware to get up to those rates. So we still have a long way to go to take full advantage of the speed potential of DVST technology.

To further enhance interactivity, new products will have a *repaint* feature that, in effect, provides selective erase. In this technique, fast data transmission combined with local memory allows you to rewrite part of the information on the screen in less than a second rather than 20 or 30 seconds.

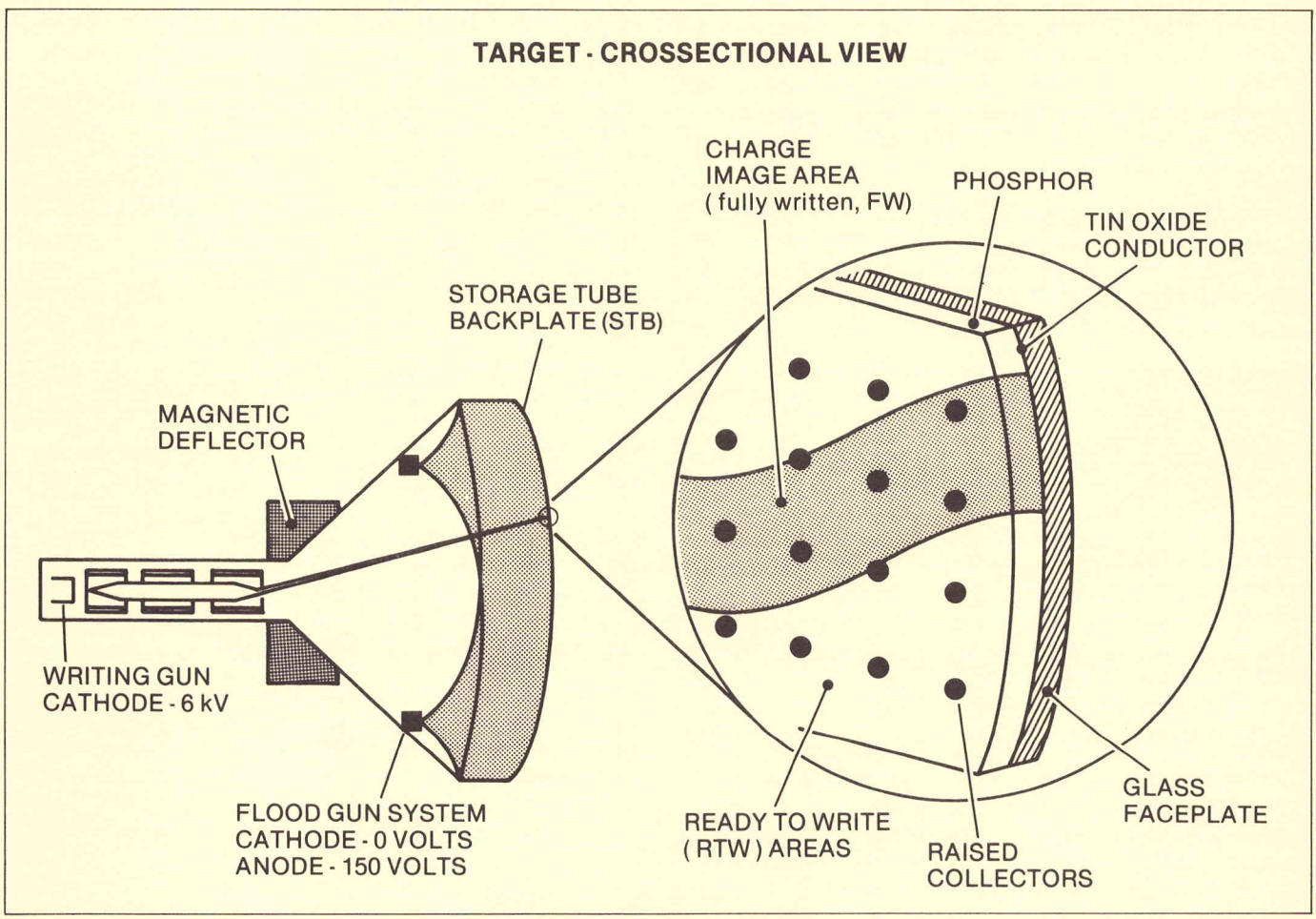


Figure 1. The basic parts of a direct view storage tube.

When a host computer sends graphic data to a DVST terminal for display, it can command the terminal to store the data in local random-access memory (RAM) as a numbered segment. Then, if the screen is erased, the segment can be quickly repainted — redisplayed — from local memory. All the host has to do is tell the terminal to display that segment. The host doesn't have to retransmit the entire sequence of graphics data.

The result is a sharp increase in repaint speed and less traffic between the host and the terminal. We can, for example, store in RAM an integrated-circuit mask containing 26,000 short vectors, and redraw it on the screen in less than half a second. Repaint is so fast, it makes the erase look slow by comparison.

Color Write-Through

Beyond utilizing faster data transmission, there have been other advances in DVST technology. The biggest by far is *color write-through.* Write-through, as we have seen, greatly increases the interactivity of the display. Adding color enhances the viewability of that display. By viewability I mean the user's ability to understand the information displayed, as well as the user's ability to look at the screen without strain.

One drawback to the original write-through was that the refreshed information was displayed at about the same brightness as the stored information, and it was in the same color. So, it was difficult for the user to distinguish between the two. The display was confusing, especially in a complex application like that of displaying a diagram of a multilayer circuit board. One solution was to make the refresh dimmer than the stored information. The two were then definitely different, but not very viewable.

A better solution was to write-through in another color. The write-through color we chose was a greenish-yellow, a color compatible with but different from the green used for stored information. To obtain the new color, we used a mixture of red phosphor and green phosphor.

You might ask, won't the stored as well as the write-through information appear in the new color? No, because the red phosphor doesn't luminesce until its electrical potential reaches about 400 volts; that's about 100 volts higher than the potential required to make the green phosphor luminesce. This technique is similar to that of a penetration-type display — where the beam penetrates phosphor layers to produce other colors. The penetration, and therefore the color, is controlled by switching the accelerating potential applied. But, there is no voltage switching in color write-through because we use two independent electron sources at different potentials in the CRT. The flood gun electrons maintain the stored image, and the writing gun electrons provide the refresh image.

Besides the basic green and the new greenish-yellow, we can now also produce a third color by employing a technique we call *over-write.* Using the new phosphor mixture, if we store information on the screen and then refresh the same image over the stored image, we get a color that's halfway between basic green and the greenish-yellow of write-through.

We haven't decided to fully develop this third-color technique. We're not sure how much use there will be for it. And users having red-green color blindness may not be able to use it effectively.

Better Contrast Ratio

DVSTs have typically had a contrast ratio — that is, the ratio between the lightest and the darkest parts of the screen — of about 10 to 1 initially. DVSTs, however, improve with usage, so that after 300 to 500 hours of operation, they have a contrast ratio of 30 to 40 to 1. What happens is that stray microscopic particles of phosphor in the target produce undesired background luminescence, but this situation improves with age. The utility of high contrast, of course, is that it enables the viewer to more easily distinguish items on the screen.

One way we have chosen to increase the effective contrast is to use color, in addition to luminance, as a factor that affects perceived contrast. We are going to use a color filter to set-off stored information. With the filter we've chosen, the background color is magenta, and the stored information is still green. Using the filter lowers luminance somewhat, but increases the total effective contrast.

The color write-through and the over-write features are suitable for many applications like multilayer circuit-board design and automobile-body design. In such applications, with local memory — or host memory if the data links are fast enough — you can change the DVST display the same way you can with a raster or directed-beam system. You can use a menu area to manipulate objects or characters on the screen. Then when you're satisfied with the display, you can press a key and store it on the screen, and also in computer memory. You can redisplay it later and work on a selected area.

So, you still have the DVST's inherent advantages of high resolution, low cost, and flicker-free display with storage. But now you also have greater interactivity and viewability.

Greater Stored Luminance

DVSTs have been criticized as dim. We have taken several steps toward increasing the luminance of displayed information.

First, we raised the target phosphor's operating-point voltage — the voltage at which it will luminesce — thereby increasing the power and, thus, the luminance at the screen.

Second, we changed the shape of the CRT funnel to get more current to the screen. We went from a 90-degree to a 100-degree deflection-angle CRT. Thus we shortened the tube and got more flood-gun electrons to the screen. That too increased the luminance.

Improved Phosphor Life

Sometimes advances in one area of a technology cause problems in other areas.

When we increased the stored luminance by increasing the current to the display, we created a problem: greater current reduces the life of the target phosphor. However, using new phosphors and processing techniques — developed as part of a continuing phosphor-improvement program — overcame this problem even at the increased current density, and gave the tube 50 percent longer phosphor life.

Write-through information is also a different color from the filter color. In this regard, we now call the write-through *color-enhanced refresh* to distinguish it from the earlier monochrome DVST write-through.

Improved Hardcopy Performance

Improved hardcopy performance is another feature of today's DVST technology. In particular, our goal has been to minimize noise in the hardcopy. To do that, we spent two years studying those parameters that effect the hardcopy ability of the CRT. As a result, we redesigned the CRT funnel and the floodgun structure to improve the hardcopy. These changes minimize the necessity to adjust hardcopy circuitry as the DVST ages.

Other improvements in the area of hardcopy are shorter setup time, easier use, more stability, and higher reliability.

In The Future

A logical extension of the 19-inch color-enhanced refresh tube will be a 25-inch version, which we expect will have enhancements that will make the display even more viewable. Specifically, we expect to increase the write-through luminance on the 25-inch tube. With this tube there will be an increased capacity for displaying information, but at an even higher brightness level.

I think we will continue to see advances in all the features we've examined here: 25-inch color-enhanced tubes, faster data links, lower costs, and higher luminance.

Besides those advances, there may well be a major new feature: color storage. The technologies needed to provide color storage exist today. We are investigating those technologies now. Implementing color storage will be a marketing decision — not an engineering problem. We are looking at the preformance/price trade-offs.

Nevertheless, for some applications, color storage — combined with color write-through — could offer a powerful and marketable combination of technologies.

Into the 90s — A Bright And Colorful Future

Speaking of markets, I expect that we won't see a major downturn in the use of DVST technology until the 1990's. Replacing DVST technology is inevitable at some point, but if you look at business surveys, you will see that the world-wide marketplace for displays is increasing dramatically. So, even if DVST's relative share of the display market should decline somewhat, total unit volume will still be very high.

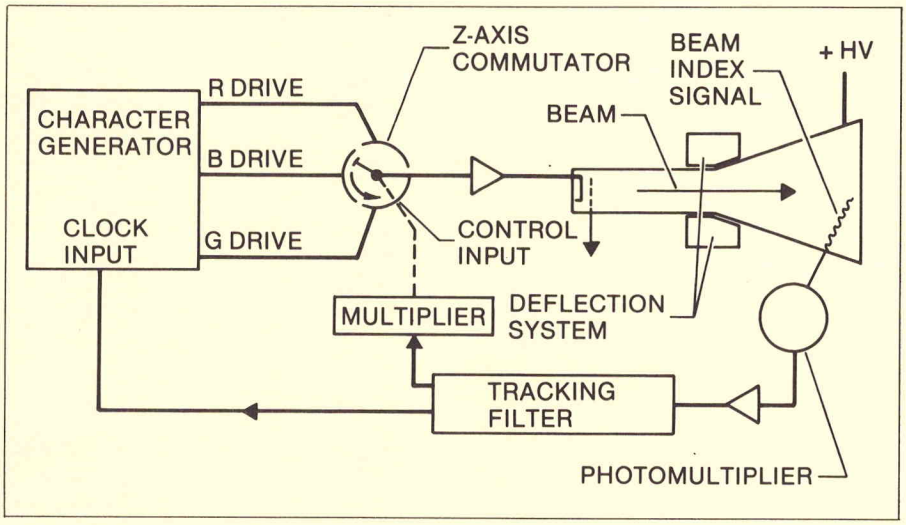
All in all, then, I do believe that DVST technology has a bright and colorful future. □

PATENT RECEIVED: No. 4,247,869

IMPROVED RESOLUTION AND LINEARITY IN A BEAM-INDEX DISPLAY SYSTEM

Robert Culter, CPI Plotters Electrical Engineering, ext. W1-2723.

Charles Osborne, former employee.



Robert Culter and Charles Osborne have received a patent for an improvement on the beam-indexing technique for color CRT systems. Beam indexing is a technique that creates a signal which represents the beam's position on the display. Such a signal is employed to turn on the beam in a video display CRT during an interval in which a specific phosphor color is desired.

Because data generation was not synchronized, previous systems produced low-resolution displays not suitable for precise data display. Essentially, this invention synchronizes both the data generation and the beam drive to overcome the timing problems found in earlier techniques. The result: much higher resolution data displays.

The key element in this invention is that the output of the tracking filter is applied to both the control input of the Z-Axis commutator and the clock input of the character generator.

For More Information

For more information, call Bob Culter at ext. W1-3723. □

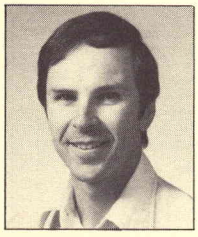
PAPERS AND PRESENTATIONS

MARCH PAPERS AND PRESENTATIONS

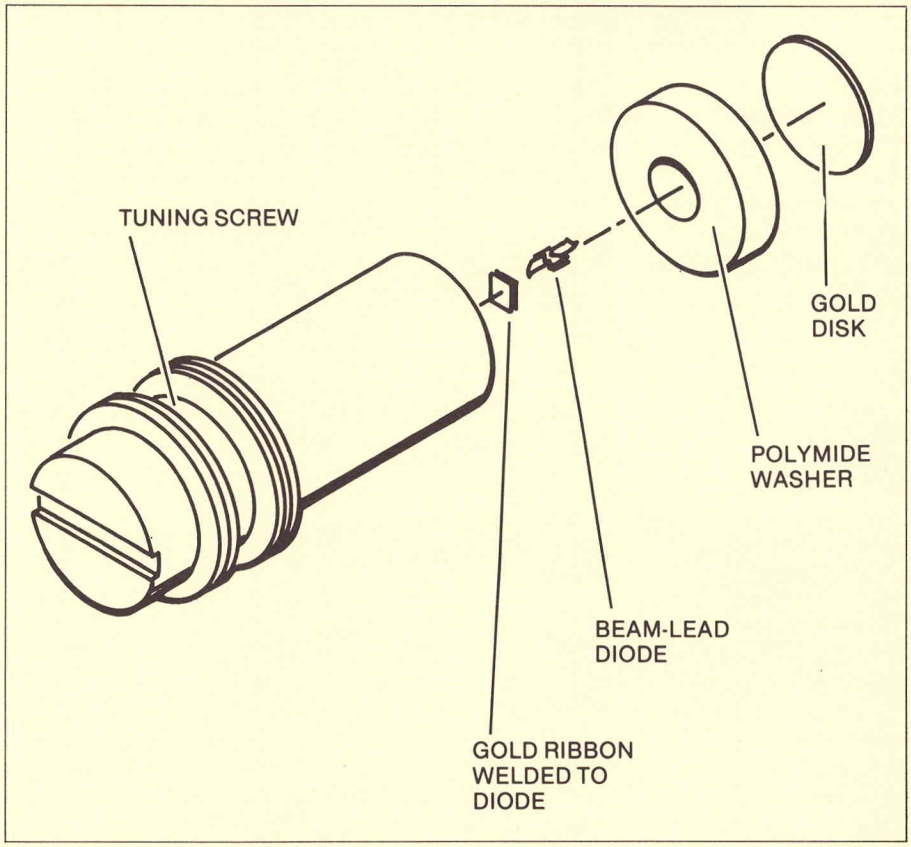
TITLE	AUTHOR	PUBLISHED	PRESENTED
Debugging a Hardware/Software System: An Application in Systems Integration	Dennis Glasby, WR 1868 Paul Dittman, WR 1869 Chris Bennett	**Computer Design**	—
Deconvolution as a feasible Alternative to the Root-Sum-Squares Rule for Non-Gaussian Transition-Duration Analysis	Bob Cram, ext. B-4806	**IEEE Transactions on Instrumentation and Measurement**	—
Measurement of Losses in Noise-Matching Networks	Eric Strid, ext. B-4713	**IEEE Transactions on Microwave Theory and Techniques**	—
In-House Standards Fill Gaps in Instrument-Computer Interface	Maris Graube, ext. B-6234	**Electronics**	—
Automatic Spectrum Analysis	Gary Mott, ext. B-7956	**RF Design**	—

PATENT RECEIVED: 4,246,556

LOW PARASITIC SHUNT DIODE PACKAGE



Phil Snow, Microwave Technology Group, part of Frequency Domain Instruments, ext. DR-1462.



Phil Snow has received a patent for a diode packaging scheme in which a low-dielectric polyimide insulating washer reduces the parasitic shunt capacity normally associated with microwave diode packages from 0.25 pf to 0.1 pf. The tuning screw and beam-leaded Schottky diode, used in the package, provide a consistent series inductance of 0.1 nanohenry, compared with an inconsistent 0.5 nanohenry inductance for conventional chip and wire schemes. The conventional method required expensive tooling, exacting adjustment, and waiting a week to see if the adjustment held.

This new package is used in the 18-to-26.5-Ghz and 26.5-to-40-Ghz high-performance waveguide mixer accessories sold with the 492 Spectrum Analyzer. The use of a tuning screw as a mounting media provides a solid ground and convenient means to allow the diode to be easily replaced in the field. The $6.00 beam-leaded Schottky diode used in the package is cheaper and less labor intensive than the $60.00 multijunction diode previously used; a diode that was not field replaceable. The new diode's frequency response is equal to, or better than, the prior chip and probe method which provided a ±5 dB maximum unflatness from 18 to 40 Ghz.

For More Information

For more information, call Phil Snow, ext. DR-1462. □

Technology Report

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