TEK INSTRUCTION MANUAL

070-7752-00
Product Group 46

067-0557-00 CALIBRATION FIXTURE

INSTRUCTION

Tektronix®
COMMITTED TO EXCELLENCE

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Please Check for CHANGE INFORMATION at the Rear of This Manual

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THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

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OPERATORS SAFETY SUMMARY

The general safety information in this summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Power Source

Use only the power transformer supplied with your instrument. The transformer is for indoor use only, and may be plugged into a specified power source. The transformer supplies 18 Vac to the calibration fixture.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of correct type and rating as specified in the parts list for your product. Refer fuse replacement to qualified service personnel.

Do Not Operate in an Explosive Atmosphere

To avoid explosion, do not operate this instrument in an explosive atmosphere.

Do Not Operate Without Cabinet in Place

Do not remove the product covers or cabinet. Do not operate the instrument without the cabinet properly in place.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

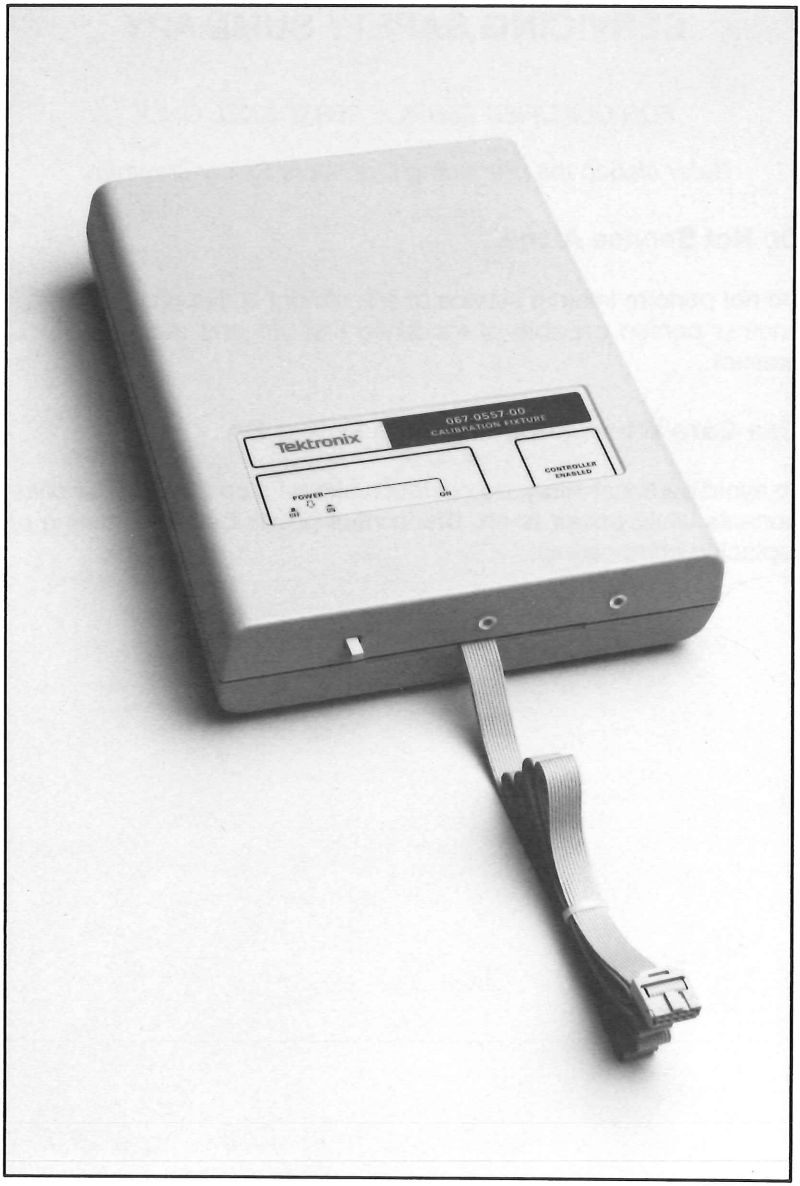
Refer also to the preceding Operators Safety Summary

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

To avoid personal injury, do not touch exposed connections or components while power is on. Disconnect power before soldering or replacing components.



7752-10

The 067-0557-00 Calibration Fixture.

SECTION 1

General Information

INTRODUCTION

Description

The TEKTRONIX 067-0557-00 Calibration Fixture is a GPIB-hardware controlled calibration fixture for the TEKTRONIX 2246 Option 1Y (serial number B100100 and up) and the TEKTRONIX 2246 Mod A (serial number B100100 and up) oscilloscopes.

NOTE

In this instruction manual, the nomenclature "2246 Option 1Y (B100100 and up) and 2246 Mod A (B100100 and up)" oscilloscope will usually be shortened to simply "2246" oscilloscope; so that references to the 2246 oscilloscope in this manual refer to the Option 1Y (B100100 and up) and Mod A (B100100 and up) instruments.

This self-contained calibration fixture allows control of the front-panel contact closures and switch matrix on the 2246 oscilloscope.

The 067-0557-00 is configured as a GPIB talk-only device with relation to the 2246 oscilloscope; and the fixture is configured as a talk-listen device in relation to the controller, reporting syntax errors only. The device number (address) and message terminator (LF/EOI) is user selectable via the hardware switch accessible through a window in the rear of the cabinet.

Two status lights are provided on the front of the cabinet to indicate when the fixture's power is on, and when the controller is enabled.

IEEE 488 (GPIB) Function Capability

The IEEE Standard 488-1978 identifies the interface function repertoire of a programmable instrument on the digital interface in terms of interface function subsets. The subsets are defined in the standard. The subsets that apply to the 067-0557-00 interface system are listed in Table 1-1.

Table 1-1
IEEE 488 Interface Function Subsets[a]

Function	Subset	Capability
Source Handshake	SH1	Complete.
Accepter Hand-shake	AH1	Complete.
Basic Talker	T6	Responds to Serial Poll. Untalked if My Listen Address (MLA) is received.
Basic Listener	L4	Unlistened if My Talk Address (MTA) is received.
Service Request	SR1	Complete.
Remote Local	RL0	No "local" capability (remote only).
Parallel Poll	PP0	Does not respond to Parallel Poll.
Device Clear	DC1	Complete.
Controller	C0	No Controller function.

[a] Refer to IEEE Standard 488-1978 for more detailed information. The standard is published by The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017.

Accessories

Standard accessories shipped with the 067-0557-00 include a wall-plug power transformer, an instruction manual, and an extra connector-saver cable. Refer to the Accessories page at the back of this manual for accessory information and part numbers.

SPECIFICATION

Electrical characteristics are given in Table 1–2, environmental characteristics in Table 1–3, and mechanical characteristics in Table 1–4.

Table 1–2
Electrical Characteristics

Characteristic	Performance Requirement[a]
GPIB Requirements	Complies with ANSI/IEEE Standard 488–1978.
AC Power Source	90 volts to 132 volts.
Source Frequency	58 Hz to 62 Hz.
Fuse Rating	2 ampere, fast blow.
Maximum Power Consumption	8 watts.

[a] **Performance Requirements not checked in this manual.**

Table 1-3
Environmental Characteristics

Characteristic	Description
Environmental Requirements	Instrument meets or exceeds the environmental requirements of MIL-T-28800D for Type III, Class 5 equipment as described below.
Temperature	
Operating	0°C to 50°C (32°F to 122°F).
Nonoperating	-40°C to 71°C (-40°F to 160°F). Tested to MIL-T-28800D paragraphs 4.5.5.1.3 and 4.5.5.1.4 except in 4.5.5.1.3, steps 4 and 5 (0°C operating test) are performed ahead of step 2 (-40°C nonoperating test). Equipment shall remain off upon return to room ambient during step 6. Excessive condensation shall be removed before operating during step 7.
Humidity (operating and nonoperating)	Five cycles (120 hours) referenced to MIL-T-28800D paragraph 4.5.5.1.2.2, for Type III, Class 5 instruments. Nonoperating and operating at 95% -5% to +0% relative humidity. Operating at 30°C and 50°C for all modes of operation. Nonoperating at 30°C to 60°C.

Table 1-3 (cont)

Characteristic	Description
Vibration (operating)	15 minutes along each of 3 major axes at a total displacement of 0.015 inch p-p (2.4 g at 55 Hz) with frequency varied from 10 Hz to 55 Hz to 10 Hz in one-minute sweeps. Hold for 10 minutes at 55 Hz in each of the three major axes. All major resonances must be above 55 Hz. Meets requirements of MIL-T-28800D, paragraph 4.5.5.3.1.
Bench Handling Test (cabinet on)	Each edge lifted four inches and allowed to free fall onto a solid wooden bench surface. Meets requirements of MIL-T-28800D, paragraph 4.5.5.4.3.
Shock (operating and nonoperating)	30 g, half-sine, 11 ms duration, 3 shocks per axis each direction, for a total of 18 shocks. Meets requirements of MIL-T-28800D, paragraph 4.5.5.4.1, except limited to 30 g.
Transportation	
Packaged Vibration	Meets the limits of the National Safe Transit Association test procedure 1A-B-1, excursion of 1 inch p-p at 4.63 Hz (1.1 g) for 30 minutes on the bottom and 30 minutes on the side (for a total of 60 minutes).
Package Drop Test	Meets the limits of the National Safe Transit Association test procedure 1A-B-2; 10 drops of 36 inches.

Table 1-4
Mechanical Characteristics

Characteristic	Description
Weight (with power transformer)	1.46 kg (3.23 lb).
Domestic Shipping Weight	2.6 kg (5.75 lb).
Height	58.4 mm (2.3 in).
Width	184 mm (7.25 in).
Depth	235 mm (9.25 in).

SECTION 2

Preparation For Use

CONNECTORS, SWITCHES, AND INDICATORS

Rear-Cabinet Connectors and Switch

Power Connector—is located at the rear of the 067-0557-00 and can be accessed through the round opening in the back of the fixture. Eighteen volts RMS can be supplied to the fixture by connecting the wall-plug power transformer to this connector.

GPIB Hardware Connector—is located at the rear of the upper cabinet. Through this connector, the calibration fixture accepts and addresses instructions for the 2246 instrument. The connector pin assignments are as follows:

Pin	Line Name	Description
1	DI01	IEEE-488 Data I/O
2	DI02	IEEE-488 Data I/O
3	DI03	IEEE-488 Data I/O
4	DI04	IEEE-488 Data I/O
5	EOI	IEEE-488 Data I/O
6	DAV	IEEE-488 Handshake
7	NRFD	IEEE-488 Handshake
8	NDAC	IEEE-488 Handshake
9	IFC	IEEE-488 Input
10	SRQ	IEEE-488 Output
11	ATN	IEEE-488 Input
12	GND	Ground
13	DI05	IEEE-488 Data I/O
14	DI06	IEEE-488 Data I/O
15	DI07	IEEE-488 Data I/O
16	DI08	IEEE-488 Data I/O
17	REN	IEEE-488 Input
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground

Address and Message-Terminator Switch – is located at the rear of the 067-0557-00 and can be accessed through the rectangular opening in the back of the upper cabinet. When you refer to the following switch description and to Figure 2-1, place the 067-0557-00 with its feet on a flat surface and the back (rear) of the fixture facing you.

NOTE

The address and message-terminator switch is read upon power-up of the instrument. To change the state of the address or message terminator after turn-on, you must power the instrument down and then up again before the changed switch settings are acknowledged.

The address and message-terminator switch is a six-wide DIP (dual in-line package) switch. The first five switches (starting from the left side) are the address switches. These are binary switches with a decimal equivalent of 1, 2, 4, 8, and 16 (left to right). The sixth switch is the LF/EOI, message terminator switch. A binary low (0) state is invoked by placing a switch in the up position, a high (1) state by placing a switch in the down position.

As an example, Figure 2-1 shows the first five switches set to decimal address 23 and the sixth switch set to the EOI message-terminator position.

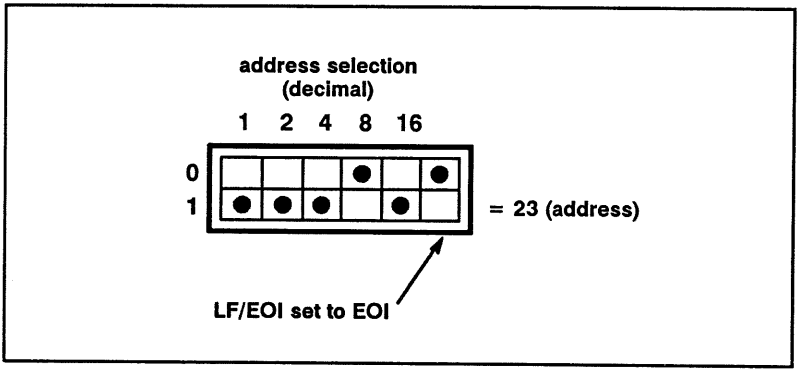


Figure 2-1. Setting the Address and Message-Terminator switch.

THE DECIMAL ADDRESS. Valid addresses are from 1 to 30. Address 0 is reserved for maintenance and servicing the instrument. Address 31 is the IEEE 488 UNT (Untalk) and UNL (Unlisten) interface address message; setting address 31 prevents the calibration fixture from communicating over the GPIB interface.

Do not set the 067-0557-00 address to the same address as the controller being used. When shipped, the calibration fixture is set to address 23.

MESSAGE TERMINATOR. The sixth switch sets the message terminator so that the operating system can respond to one of two possible message terminators that a controller could send on the GPIB interface. These are:

EOI position — Input message terminator—only the EOI line on IEEE 488 digital interface asserted with last data byte as the message terminator. Output message terminator—<;> with EOI asserted.

LF/EOI position — Input message terminator—<CR> <LF and EOI> are added to the end of the message being sent (EOI is asserted with the <LF> character). If the <LF> character without EOI, EOI with <LF>, or EOI asserted with any data byte is sent anywhere in the message string, the 067-0557-00 recognizes it as a message terminator. Output message terminator—<;><CR> then <LF> with EOI asserted.

When shipped, the 067-0557-00 message terminator is set to EOI.

Front-Cabinet Cable, Indicators, and Switch

Front-Panel Connector Cable – is accessible at the center-front of the calibration fixture. This cable is used to connect the 067-0557-00 to the 2246 oscilloscope during scope calibration. The 067-0557-00 is shipped with a short, easily replaceable "connector-saver" cable that may be used between the front-panel connector cable and the 2246 cable receptacle. The 2246 cable receptacle is located under the access cover on the top of its cabinet.

The front-panel cable provides the load, six column strobes, and shift clock to the calibration fixture and is the serial data line to the 2246. The connector pin assignment is as follows:

Pin	Line Name	Description
1	AS5	Column strobe 05
2	AS4	Column strobe 04
3	AS3	Column strobe 03
4	AS2	Column strobe 02
5	AS1	Column strobe 01
6	AS0	Column strobe 00
7	GND	Ground
8	SR SHIFT	Serial shift clock
9	SR LOAD	Serial load
10	SR DATA	Serial data

POWER Switch – is located on the front of the upper cabinet. Press the switch in for ON and press again for OFF (button out).

POWER ON Indicator – is located on the front of the upper cabinet. This green LED is illuminated while the instrument is powered up and operating.

CONTROLLER ENABLED Indicator – is located on the front of the upper cabinet. This green LED is illuminated while the 067-0557-00 has control of the state of the 2246 front-panel (contact closures and switch matrix). The oscilloscope front panel is disabled when the controller is enabled.

OPERATING CONSIDERATIONS

Power-Up Self Test

Connect the 067-0557-00 to an IEEE 488 GPIB controller by connecting a standard GPIB cable from the 067-0557-00 GPIB Hardware Connector to the controller. Connect the calibration fixture's Front-Panel Connector cable to the 2246 cable receptacle (located under the access cover on the 2246 cabinet top). Use of the "connector saver" cable between the Front-Panel Connector cable and the 2246 cable receptacle will reduce wear to the front-panel connector cable.

NOTE

Refer to the manuals for your controller and the 2246 for detailed safety and operating information on those instruments.

Before turning on the 067-0557-00, make sure that the Address and Message-Terminator (DIP) switch on the rear of the fixture is correctly set for the fixture address and the message terminator. The switch settings are read and acknowledged only at power-up. Refer to the address and message-terminator information in the Connectors, Switches, and Indicators part of this section for switch setting information.

NOTE

Do not set the 067-0557-00 address to the same address as the controller being used.

When shipped, the 067-0557-00 is set for EOI message terminator and a decimal address of 23.

When power is first turned on, the calibration fixture enters a power-up self-test mode. If the controller program you are using services an SRQ, the following responses will be received. The response to an ERRor? (the ? must be included in the command) will be **401**, which indicates a normal system event. If the serial poll status byte is

reported, the response will be **65** which also indicates a normal system event. In the event that the controller program you are using does not service SRQs, you will need to turn RQS off by issuing the RQS OFF command. This must be performed prior to issuing ERRor? commands.

Status and Error Reporting

Programmable interrupts are provided in the calibration fixture to inform the controller of asynchronous events, such as command errors. If the calibration fixture is set to report such events (by the **RQS ON** command), it asserts SRQ and sets its status byte and error code appropriately. The status byte returned in response to a serial poll and the error code returned in response to an error query (**ERR?**) are listed in Table 2-1.

Table 2-1
Error Responses

Error or Event	ERR? Response	Serial Poll Response (STB)
Command Error		
No errors or events	0	0
Active, no errors to report	0	-128
Command header error	101	97
Header delimiter error	102	97
Command argument error	103	97
Argument delimiter error	104	97
Missing argument	106	97
Invalid message unit delimiter	107	97
System Event		
Power on	401	65

With RQS OFF the controller may find out about events without first performing a serial poll. The error query (ERR?) may be sent at any time and the instrument returns an error code waiting to be reported. The controller can clear all errors by sending the error query (ERR?) until a zero (0) code is returned or send the DCL message.

With RQS OFF the controller may perform a serial poll, but the status byte only contains device-dependent status information. With RQS ON, the status byte contains the class of the event and a subsequent error query returns additional information about the previous event reported by the status byte. Status byte and error code responses are listed in Table 2-1.

Because the status byte conveys limited information about an event, the events are divided into classes; the status byte reports the class of event. The classes of events are defined as follows:

Command Error – indicates the instrument has received a command that is invalid or it cannot understand.

System Events – are events that are common to instruments in a system (Power On, User Request, etc.).

REPACKAGING INFORMATION

Save the original carton and packing material for reuse if the instrument should have to be reshipped on a commercial transport carrier. If the calibration fixture is to be shipped to a Tektronix Service Center for service or repair, enclose the following information: the owner's address, name and phone number of a contact person, type of instrument, and a description of the service required.

If the original packing materials are not available, repackage the instrument as follows:

Use a corrugated cardboard shipping carton with a test strength of at least 200 pounds and with an inside dimension at least six inches greater than the instrument dimensions. Wrap the instrument with

polyethylene sheeting or equivalent to protect the outside finish and prevent entry of foreign materials into the instrument. Cushion the instrument on all sides with three inches of padding material or urethane foam between the carton and the instrument. Seal the carton with an industrial stapler or strapping tape.

SECTION 3

Programming Information

MESSAGE FORMATS

The information in this section assumes that the user has some understanding of the communication process between instruments on the IEEE 488 digital interface (GPIB) and some experience with controller programs.

Each command begins with a header—a word that describes the function to be implemented. Many commands require an argument value following the header—a word or number that specifies the desired state of the implemented function.

Query commands have no arguments; the header contains the question mark character (?) to identify the header as a query command.

NOTE

Command headers and arguments must contain, as a minimum, the exact characters and minimum number of characters that are shown in upper case in the command lists in this manual.

Commands

The command words were chosen to be as understandable as possible, and still allow a familiar user to shorten them as much as necessary—as long as the results are not ambiguous. Syntax is also standardized to make the commands easier to learn.

In the command lists, headers and arguments are listed in a combination of upper-case and lower-case characters. The instrument accepts any abbreviated header or argument containing at least the characters shown in upper case. Any characters added to the abbreviated (upper-case) version must be those shown in lower case.

Headers

A command consists of at least a header. Each command has a unique header, which may be all that is needed to invoke a command; for example:

FACtory
BWIm

Arguments

Some commands require the addition of arguments to the headers to describe exactly what is to be done. If there is more to the command than just the header, then the header must be followed by at least one space. The argument can be a single word or a numeric value; for example:

SECs 50Ms

Command Separator

Multiple commands may be put into one message by separating the individual commands with a semicolon; for example:

SECs 50Ms; MOde ALt

Message Terminator

Messages may be terminated with either EOI or LF. A complete message may be terminated with EOI or the ASCII line feed character (LF). Some controllers assert the EOI line concurrently with the last data byte in the message; others use only the LF character as a terminator. The 067-0557-00 interface can be set to accept either terminator. With EOI ONLY selected as the terminator, the 067-0557-00 interprets a data byte received with the EOI line asserted as the end of an input message. The calibration fixture also asserts the EOI line concurrently with the last data byte of an output message.

If LF/EOI is selected as the message terminator, the 067-0557-00 interprets the LF character without EOI asserted, or any data byte received with EOI asserted, as the end of an input message. At the end of an output message, the calibration fixture transmits carriage return <CR>, followed by line feed <LF> with EOI asserted.

FRONT-PANEL INITIALIZATION

Many of the 067-0557-00 commands toggle 2246 front-panel settings, rather than setting them to a specific state. For example, the **CHV3** command sets Channel 3 Volts/Div to 0.5 V if it had been set to 0.1 V, but the same command sets Channel 3 Volts/Div to 0.1 V if it had been set to 0.5 V. Because of this, it is necessary to establish a defined state for front-panel controls from which a sequence of commands can be sent to achieve a desired setup.

The **FACtory** command provides a predefined state by setting the front-panel controls to their factory settings. The **FACtory** command should be issued immediately after the **LOck** command in any program to control the 2246. Then, commands can be sent to change the settings of the front panel from the factory settings to the desired setup. The 2246 Operators manual and Table 3-2 in this section contain a description of the factory settings.

Although it is possible to keep track of the state of the front-panel settings as commands are issued (after sending one **FACtory** command), it is advisable to issue the **FACtory** command at the beginning of each portion of the program that establishes a desired setup. This is particularly important if portions of the program may be run independently or out of sequence.

COMMAND LIST

Table 3-1 describes all of the available 067-0557-00 commands. The first column lists the name (or header) of the command. The capitalized letters must be present to identify the command, and the lower-case letters are optional. The second column lists arguments

that can be associated with the command, and command descriptions are given in the third column.

The commands in Table 3–1 are 2246 commands only, except where noted.

NOTE

The LOck command must be sent before any 2246 commands will be acted upon.

The FACtory command must be used to establish predetermined front-panel settings, because the instrument setup cannot be read back via the GPIB interface. From predetermined front-panel settings, a sequence of commands can be executed to perform a given function. Upon completion of the execution of the given commands, the FACtory command must be executed again to establish a predetermined front-panel setup. Factory settings are listed in the 2246 Operators manual and are also given in Table 3–2 (following the 067–0557–00 command list).

NOTE

Established front-panel settings may change when the UNlock command is issued. Consequently, UNlock should not be used in programs except as the last command, when control is returned to the user and it is not necessary to have a defined front-panel setup. If program control resumes after an UNlock is issued, the LOck and FACtory commands must be issued again to return to known front-panel settings. Settings affected by UNlock are VOLTS/DIV and SEC/DIV.

Table 3-1
Command List for the 067-0557-00

Header	Argument	Description
LOck		Locks out the 2246 front panel. This enables the 067-0557-00, allowing commands to be sent to the 2246 oscilloscope. It also disables the 2246 front-panel buttons and switches.
UNlock		Unlocks the 2246 front panel. This disables the calibration fixture. The oscilloscope front-panel buttons and switches will be functional. Established front-panel settings (VOLTS/DIV and SEC/DIV) may change when the UNlock command is issued.
FACtory		Returns the front-panel controls to their factory setting. (See Table 3-2 or the 2246 Operators manual.)
CHA1		Toggles CH 1 on/off, the same as pressing the Channel 1 Mode button.
CHA2		Toggles CH 2 on/off, the same as pressing the Channel 2 Mode button.
CHA3		Toggles CH 3 on/off, the same as pressing the Channel 3 Mode button.
CHA4		Toggles CH 4 on/off, the same as pressing the Channel 4 Mode button.
CHADd		Toggles CH1-CH2-ADD on/off, the same as pressing the ADD Mode button.
CHOp		Toggles Vertical Mode to CHOP or ALT, the same as pressing the CHOP/ALT Mode button.
CHC1	Ac Dc Gnd	Sets Channel 1 Vertical Coupling to the selected mode.
CHC2	Ac Dc Gnd	Sets Channel 2 Vertical Coupling to the selected mode.

Table 3-1

Header	Argument	Description
CHV1	<n>[a]	Sets Channel 1 Volts/Div gain to the value of <n>, the argument. The effects of probe coding are independent of CHV1.
CHV2	<n>[a]	Sets Channel 2 Volts/Div gain to the value of <n>, the argument. The effects of probe coding are independent of CHV2.
INV2		Toggles Channel 2 inversion on or off. The number 2 is optional.
CHV3		Toggles Channel 3 Volts/Div gain to 0.5 V or 0.1 V.
CHV4		Toggles Channel 4 Volts/Div gain to 0.5 V or 0.1 V.
BWlm		Toggles bandwidth limit (20 MHz SCOPE BW) on/off.
MOde		Selects Horizontal display mode from the list under the argument column. Choices are mutually exclusive.
	AOnly	Selects only the A sweep for display.
	ALt	Selects both normal and delayed sweeps for display.
	Bonly	Selects only the B sweep for display.
	Xy	Selects X-Y mode.

[a] **The valid values of <n> for CHV1 and CHV2 are:**

5V	**.5v**	**50mv**	**5Mv**
2V	**.2v**	**20mv**	**2Mv**
1V	**.1v**	**10mv**	

Table 3-1 (cont)

Header	Argument	Description
SECs	<n>[b]	Selects the Horizontal sweep speed in seconds per division for the active sweep mode. When Horizontal mode is A, changing the sweep speed will cause both the A and B sweep speeds to change. If the sweep speed is changed to 5Ms or faster, the B sweep speed will be set equal to the A sweep speed. If the sweep speed is changed to 10Ms or slower, the B sweep speed will be set to 5Ms. When Horizontal mode is ALT or B, if the resulting speed of B sweep is slower than the current A sweep speed, the A sweep speed will be set equal to the B sweep speed.
HMAG		Toggles X10 Horizontal magnification on/off.
ABsel		Selects A Trigger/B Trigger as the active trigger for the Mode, Source, and Coupling.
TMOde		Selects the Trigger Mode from the list of arguments.
	ALvl	Selects Auto Level as the Trigger Mode.
	AUto	Selects Auto as the A Trigger Mode. When A/B Select is set to B, selects Runs After as the B Trigger Mode.
	Norm	Selects Norm as the Trigger Mode.
	TVln	Selects TV Line as the Trigger Mode.

[b]The valid values of <n> for SECs are:

.5S	50Ms	5Ms	.5Ms	50Us	5Us	.5Us	50Ns
.2S	20Ms	2Ms	.2Ms	20Us	2Us	.2Us	20Ns
.1S	10Ms	1Ms	.1Ms	10Us	1Us	.1Us	

(When Horizontal Mode is ALT or B, values of <n> from .5S to 10Ms will produce sweep speeds of 5Ms.)

Table 3-1 (cont)

Header	Argument	Description
TMOde (cont)		
	TFId	Selects TV Field as the A Trigger Mode. When A/B Select is set to B, selects TV Line as the B Trigger Mode.
	SgIs	Selects Single Sequence as the A Trigger Mode. When A/B Select is set to B, selects TV Line as the B Trigger Mode.
TSRc		Selects Trigger Source from the list of arguments.
	Vert	Selects the Vertical Mode as the Trigger Source. When multiple vertical mode channels are selected, the channel with the lowest numerical value is selected as the Tirgger Source.
	CH1	Selects Channel 1 as the Trigger Source.
	CH2	Selects Channel 2 as the Trigger Source.
	CH3	Selects Channel 3 as the Trigger Source.
	CH4	Selects Channel 4 as the Trigger Source.
	Line	Selects Line signal as the Trigger Source.
TSLpneg		Toggles the Trigger Slope negative/ positive.
TCOupling		Selects Trigger Coupling from the list of arguments.
	Dc	Selects DC as the Trigger Coupling.
	Noise	Selects Noise Reject as the Trigger Coupling.

Table 3-1 (cont)

Header	Argument	Description
TCOupling (cont)		
	Hf	Selects High-Frequency Reject as the Trigger Coupling.
	Lf	Selects Low-Frequency Reject as the Trigger Coupling.
	Ac	Selects AC as the Trigger Coupling.
CLrdsp		Selects the Clear Display function.
LAstmeas		Selects the Last Measurement function.
CURsorvolts		Selects the Cursors menu.
SEL1		Selects VOLTS function.
SEL2		Selects ground reference VOLTS function.
SEL6		Selects AUTO TRACKING MENU.
(AUTO TRACKING MENU)		
SEL1		Selects TRACK MEASUREMENT (on/off).
SEL2		Selects TRACK TRIGGER LEVEL function.
SEL3		Selects TRACK ground function.
SEL5		Selects BACK TO PREVIOUS MENU.
SEL6		Selects MENU OFF function.

Table 3-1 (cont)

Header	Argument	Description
VOltmeter		Selects the Voltmeter menu.
SEL1		Selects DC function.
SEL2		Selects +PEAK function.
SEL3		Selects -PEAK function.
SEL4		Selects PEAK-PEAK function.
SEL5		Selects SELF CALIBRATION function.
SEL6		Selects GATED MEASUREMENT MENU.
(GATED MEASUREMENT MENU)		
SEL1		Selects GATED +PEAK function.
SEL2		Selects GATED -PEAK function.
SEL3		Selects GATED PEAK-PEAK function.
SEL5		Selects BACK TO PREVIOUS MENU.
TIMemenu		Selects the Time menu.
SEL1		Selects SEC (seconds) function.
SEL2		Selects 1/SEC (1/seconds) function.
SEL3		Selects PHASE function.
SEL5		Selects SELF CALIBRATION function.
SETMeas		Selects the Measurement Channel.
SERvmenu		Selects the Service menu.
SEL1		Selects menu item one.
SEL2		Selects menu item two.
SEL3		Selects menu item three.
SEL4		Selects menu item four.
SEL5		Selects menu item five.
SEL6		Selects menu item six.

Table 3-1 (cont)

Header	Argument	Description
		NOTE *The following commands relate to the calibration fixture only. They do not effect the 2246, with the exception that the front panel will be unlocked with the execution of the INITialize command.*
IDentify?		The ID? query returns the name of the instrument and the firmware version of the ROM on the lower board. The **?** must be included in the command.
NAme?		The NA? query returns the name of the instrument and the firmware version of the ROM on the upper board. The **?** must be included in the command.
ERRor?		With RQS ON, the error query returns the error code for the most recent SRQ generated. With RQS OFF, the highest priority error code is returned. Returns error code **0** if no errors. The **?** must be included in the command.
INITialize		The INIT command returns the complete operation system to the power-up default values. This command does not cause a power-up SRQ nor cause the operation system to go to a "local" mode.
RQS	<n>	Where <n>, the argument, is either ON, OFF, or ?. The RQS command controls the generation of SRQs. With RQS OFF, no SRQs (except the power-on SRQ) will be generated. Any pending SRQs will be generated with RQS ON. The state of the RQS argument is returned when queried (?).

Table 3-2
2246 Factory Settings

Control	Setting
VERTICAL MODE	CH 1 and CH 2
CH 1, CH 2 INPUT COUPLING	DC
CH 1, 2, 3, 4 VOLTS/DIV	0.1 V
CH 2 INVERT	OFF
SCOPE BW (bandwidth limit)	OFF
HORIZONTAL MODE	A
X10 MAG	OFF
A SEC/DIV	0.1 ms
B SEC/DIV	1 μs
A, B SLOPE	⌐
A/B SELECT	A
A TRIGGER MODE	AUTO LEVEL
B TRIGGER MODE	RUNS AFTER
A and B TRIGGER SOURCE	CH 1
A and B TRIGGER COUPLING	DC
TRIGGER HOLDOFF	As selected
MEASUREMENTS	OFF
TRACKING CURSORS	TRACK MEASMT
MENU Displays	OFF
CONFIGURE Selections	NO
A INTEN, B INTEN, READOUT	As selected

PROGRAMMING EXAMPLE

The programs used for scope calibration will depend upon your system and the type of controller you will use. The following example does not include programming information specific to any particular type of controller, but instead lists the 067-0557-00 commands that would be included in the program.

The example shown will configure the front panel to allow the CALIBRATOR output to be checked. The program should send each of the commands listed below to the 067-0557-00 in the order shown. Where the program addresses the 067-0557-00, the decimal 23 address should be used.

Command	Response
LOCK	Locks out the 2246 front panel and allows commands to be sent to the 2246.
FACTORY	Sets the front-panel controls to their factory settings.
CHA2	Turns off CH 2 Vertical Mode. Both CH 1 and CH 2 are on in the factory settings state. The CHA2 command toggles CH 2 off, leaving only CH 1 on.
CHV1 10MV	Sets the CH 1 Volts/Div to 10 mV.
SEC .2MS	Sets the Sec/Div to 0.2 ms.
BWLM	Turns on 20 MHz bandwidth limit. Bandwidth limit is off in the factory settings state, and the BWLM command toggles it on.

After the program has sent these commands to the 067-0557-00, the 2246 front panel will be set to perform a check of the CALIBRATOR output. Connecting a 10X probe from the CH 1 input to the CALIBRATOR output allows the signal to be observed, although this is not necessary to check that the proper setup has been performed.

Before you run a program created from this example, make these preliminary preparations:

1. Connect the calibration fixture to an IEEE 488 (GPIB) controller using a GPIB cable.

NOTE

Be certain that the calibration fixture's address switches are set to decimal 23 and its message terminator switch is set for EOI before turning on power to the fixture.

2. Connect the calibration fixture to the 2246 by plugging the front-panel connector cable into the receptacle located under the access cover on the top of the 2246 cabinet.

3. Power up the GPIB controller, the 2246 oscilloscope, and the 067-0557-00 calibration fixture.

4. Run the program created from this example.

This completes the sample program.

SECTION 4

Performance Check

SOFTWARE CHECKOUT PROCEDURE

This procedure checks the ability of the microprocessor in the calibration fixture to communicate with a controller on the IEEE 488 interface (GPIB).

The 067-0557-00 has no internal adjustments for calibration purposes; therefore, it is not necessary to check its performance at any regular intervals. If the instrument fails the performance check, circuit troubleshooting by a qualified service person is indicated.

The only equipment required for this procedure is a GPIB-compatible controller, a GPIB cable, and a 2246 oscilloscope.

Procedure

1. Connect the calibration fixture to an IEEE 488 (GPIB) controller, using a GPIB cable.

NOTE

Be certain that the calibration fixture's address switches are set to decimal 23 and its message terminator switch is set for EOI before turning on power to the fixture.

2. Connect the calibration fixture to the 2246 oscilloscope by plugging the front-panel connector cable into the receptacle located under the access cover on the top of the 2246 cabinet.

3. Power up the GPIB controller. Load an appropriate Talker-Listener program into the controller's memory. The program must be capable of sending the 067-0557-00 commands to the calibration fixture and displaying returned messages. Where the program addresses the 067-0557-00, use the decimal 23 address.

4. Start the Talker-Listener program and power up the 2246 oscilloscope and the 067-0557-00 calibration fixture.

5. Send the following messages in the order listed and note the responses. Responses to queries (commands that have a question mark (?) as the last character) are messages returned to the controller; otherwise, the response refers to an action to be observed on the 2246.

Message	Response
ID?	ID TEK/MIL067,V79.1,F03;
NA?	NAME MIL067,V79.1,F00;
LOCK	Check that the 2246 front-panel buttons no longer respond when pressed.
FACTORY	Check that the 2246 front-panel controls are set to their factory settings.
UNLOCK	Check that the 2246 front-panel buttons respond normally when pressed.

6. This completes the software checkout procedure.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

SECTION 5

Theory of Operation

MICROPROCESSOR (Diagram 1)

Microprocessor (U1214)

NOTE

For more detailed information on the internal action of the microprocessor, refer to the manufacturer's data sheet.

Integrated circuit U1214 is an 8-bit microprocessor containing an internal 1 MHz clock, a divide-by-four clock input circuit, and 128 bytes of internal random-access memory (RAM). The microprocessor's internal RAM is located at hexadecimal addresses 0000 to 007F.

The internal, single-phase, 1 MHz TTL clock output on pin 37 is derived from a 4 MHz crystal-controlled oscillator, Y1200 and associated components.

The crystal oscillator circuit operates in the series resonant mode with inductor L1200 ensuring that the crystal starts oscillating at 4 MHz. Capacitor C1202 and resistor R1214 are used to shock the circuit into oscillation. Resistor R1214 effectively disconnects C1202 from the ac circuit after startup, thereby preventing frequency pulling.

The RESET signal starts the microprocessor from a power-down condition (power failure or initial start up). When a high level is detected on pin 40, the microprocessor begins the restart sequence. See Power Supply and Reset Circuit descriptions (diagram 4).

Pin 3 of U1214 and pin 2 of U1203 (diagram 3) are tied high via logic gate U1210C. This causes the clock output of U1214 to operate normally (not stretched) and locks out the direct memory access request feature of the GPIB control chip, U1203. The high-level output from U1210C is also used to set high levels on pin 9 of U1216C and pin 12 of U1219C (diagram 2).

Pin 36 of U1214 controls the microprocessor's internal RAM (addresses 0000 to 007F). Pin 36 is pulled high by R1217 (diagram 2) to enable the RAM and remains high unless the microprocessor board is configured for the forced instruction mode. The microprocessor's internal RAM is disabled for this mode by grounding pin 36 via J1210 (diagram 2). This has the effect of disabling the microprocessor's output data buffer. The Non-Maskable Interrupt (NMI, pin 6) is held high by R1212.

Normal low-level TTL interrupt request signals to U1214 occur on pin 4, /IRQ, and can originate from any one of the four labeled sources connected to the wired-OR junction. All four of these interrupts are maskable. The microprocessor may or may not recognize these interrupts, depending on the operating conditions when the signal occurs. When recognized, the microprocessor completes its current instruction before servicing the current interrupt condition. A memory map for interrupt vectors is listed in Table 5-1.

The /HALT function for U1214 (pin 2) is tied high via R1211.

Two other output control lines, VMA (pin 5) and R-/W (pin 34), are used by the microprocessor to read data from and write data to peripheral devices. The R-/W signal goes low to write data to or goes high to read data from the data buses.

Table 5-1

Memory Map for Interrupt Vectors (Hexadecimal Addresses)

Vector		Description
MS	**LS**	
FFFE	FFFF	RESET (restart)
FFFC	FFFD	Non-Maskable Interrupt (NMI)
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request (IRQ)

The VMA line goes low to indicate that the 16-bit code on the address bus is not a valid memory address. VMA does not go low between machine instructions unless the microprocessor is using the address register for some operation other than accessing a valid location in memory or input/output peripherals. VMA is not gated by or necessarily related to the 02 clock in any way. An operational flow chart for U1214 is shown in Figure 5-1.

Address Buses

There are three separate address buses: the microprocessor address bus (A0-A15), the internal address bus (IBA0-IBA15), and the external address bus (EBA0-EBA15). None of these buses are tied directly to another.

Integrated circuits U1200, U1204, U1208, and U1215 operate as unidirectional buffers from the microprocessor address bus to the internal and external address buses. Buffer U1200 carries the low-order address bits, and U1204 carries the high-order address bits to the internal address bus. The address bits to the external address bus (via U1208 and U1215) are not connected in a low- and high-order fashion. Under normal operating conditions these buffers are always enabled. All four of these address buffers are disabled when pin 19 on U1200 and pin 1 on U1204, U1208, and U1215 go high.

The external address bus is used by the microprocessor to address the memory and peripheral devices located on the lower board. The internal address bus is used to address the memory and peripheral devices on the upper board.

Data Buses

There are four data buses on the microprocessor: the microprocessor data bus (D0-D7), the internal data bus (IBD0-IBD7), the external data bus (EBD0-EBD7), and the GPIB data bus (DIO1-DIO8).

Both integrated circuits, U1205 and U1213, operate as unidirectional data buffers; U1205 is used by the microprocessor to read data from the internal bus and U1213 is used to write data to the internal data bus.

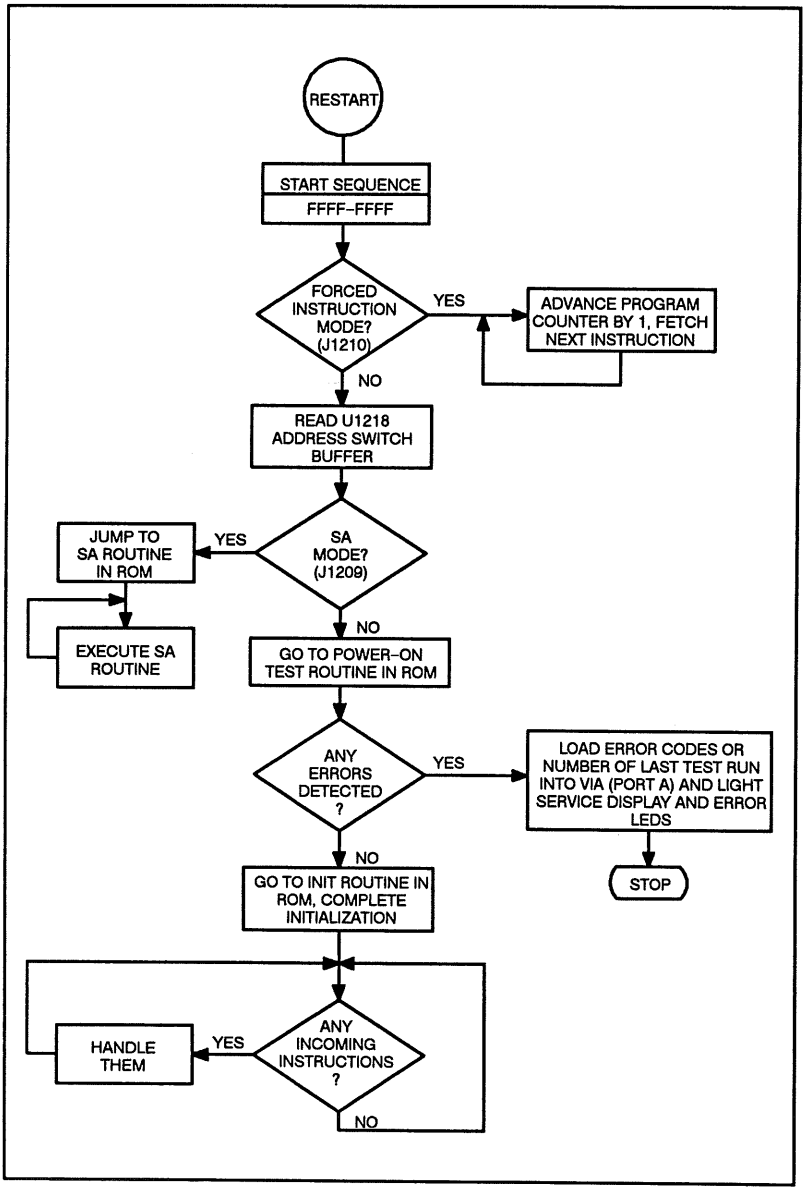


Figure 5–1. Microprocessor operational flow chart.

The write data buffer, U1213, is an octal D-type transparent latch. As long as pin 11 is held high by the system clock signal (B02), the outputs (1Q-8Q) follow the data inputs (D0-D7). When the clock signal goes low, the output is latched at the level of the data that was set up. This latch allows interfacing with slow memory devices because data can be held on the internal data bus for a finite amount of time longer than the microprocessor is capable of holding data on its data bus. Old data can be retained in or new data entered into U1213 even while the Q outputs are off. The Q outputs ore off when pin 1 is high, and data is written onto the internal data bus when pin 1 is set low via U1216C.

When pin 34 of U1214 is set high to read data from the internal data bus via U1205, pin 5 of U1210B is set high. In order to read data from the internal data bus, pins 1 and 19 of U1205 must both be low. This condition will exist when the system clock on pin 4 of U1210B is high and the /INT_DATA_ENBL signal on pin 19 of U1205 is low. The system clock is high for the last half of any given cycle.

Pin 19 of U1205 is low any time there is a read or write operation from or to hexadecimal addresses 0000 through 3FFF or addresses E000 through FFFF. Pin 1 is set high for a write operation, disabling U1205. The internal and external data buses are never active at the same time.

Data communication to and from a selected function circuit is via U1206, an octal bus transceiver with tri-state outputs. The IBR/W signal on pin 1 controls the direction of data flow over the external bus, a high state for a read operation or a low state for a write operation. The external bus is selected for read or write operations that require hexadecimal addresses in the 4000-DFFF range.

ADDRESS AND BUS DECODERS (Diagram 2)

Page 0 Decoder

Table 5–2 lists the hexadecimal address ranges for the memory and peripheral devices.

The Page 0 Decoder includes integrated circuits U1211, U1220A, U1223C, U1220B, U1223D, U1220C, and U1223F. These circuits decode the addresses for the devices in the 0000–00C7 range (see Table 5–2).

Integrated circuit U1211 operates to allow the microprocessor to communicate with its own internal RAM, the VIA IC (U1226), and the GPIB control IC (U1203).

Table 5–2

Memory Address Ranges

Device Selected	Hexadecimal Addresses
Microprocessor RAM U1214	0000–007F
Versatile Interface Adapter VIA U1226	0080–008F
GPIB Control U1203	00C0–00C7
System RAM U1222	2000–27FF (2K x 8 bits)
Address Switch Register SW1100, U1218	3000 (Read Only)
Circuit Select Latch U1207	3000 (Write Only)
Bank Region ROM U1107	4000–DFFF
System ROM U1231	E000–FFFF

The write data buffer, U1213, is an octal D-type transparent latch. As long as pin 11 is held high by the system clock signal (B02), the outputs (1Q-8Q) follow the data inputs (D0-D7). When the clock signal goes low, the output is latched at the level of the data that was set up. This latch allows interfacing with slow memory devices because data can be held on the internal data bus for a finite amount of time longer than the microprocessor is capable of holding data on its data bus. Old data can be retained in or new data entered into U1213 even while the Q outputs are off. The Q outputs ore off when pin 1 is high, and data is written onto the internal data bus when pin 1 is set low via U1216C.

When pin 34 of U1214 is set high to read data from the internal data bus via U1205, pin 5 of U1210B is set high. In order to read data from the internal data bus, pins 1 and 19 of U1205 must both be low. This condition will exist when the system clock on pin 4 of U1210B is high and the /INT_DATA_ENBL signal on pin 19 of U1205 is low. The system clock is high for the last half of any given cycle.

Pin 19 of U1205 is low any time there is a read or write operation from or to hexadecimal addresses 0000 through 3FFF or addresses E000 through FFFF. Pin 1 is set high for a write operation, disabling U1205. The internal and external data buses are never active at the same time.

Data communication to and from a selected function circuit is via U1206, an octal bus transceiver with tri-state outputs. The IBR/W signal on pin 1 controls the direction of data flow over the external bus, a high state for a read operation or a low state for a write operation. The external bus is selected for read or write operations that require hexadecimal addresses in the 4000-DFFF range.

ADDRESS AND BUS DECODERS (Diagram 2)

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The Page 0 Decoder includes integrated circuits U1211, U1220A, U1223C, U1220B, U1223D, U1220C, and U1223F. These circuits decode the addresses for the devices in the 0000–00C7 range (see Table 5–2).

Integrated circuit U1211 operates to allow the microprocessor to communicate with its own internal RAM, the VIA IC (U1226), and the GPIB control IC (U1203).

Table 5–2

Memory Address Ranges

Device Selected	Hexadecimal Addresses
Microprocessor RAM U1214	0000–007F
Versatile Interface Adapter VIA U1226	0080–008F
GPIB Control U1203	00C0–00C7
System RAM U1222	2000–27FF (2K x 8 bits)
Address Switch Register SW1100, U1218	3000 (Read Only)
Circuit Select Latch U1207	3000 (Write Only)
Bank Region ROM U1107	4000–DFFF
System ROM U1231	E000–FFFF

Pin 6 of U1211 remains high as long as none of the address bits IBA11 through IBA15 go high. Pin 5 remains high as long as none of the address bits IBA8 through IBA10 go high. Pins 5 and 6, when both are high, enable logic gates U1220A and U1220C. Whether U1220A or U1220C are addressed depends on the state of the IBA7 bit; if IBA7 is high pin 12 of U1220A goes low, if IBA7 is low the inversion on pin 14 of U1223F causes pin 8 of U1220C to go low. During the time that the microprocessor is communicating with its internal RAM, pin 8 of U1220C is held low, disabling the internal data bus (IBD0–IBD7) via pins 3 and 6 of U1217B.

Pin 12 of U1220A will be low for hexadecimal addresses in the 0080–00FF range. This 128 byte region is divided into two parts, the upper half dedicated to the GPIB Control IC and the lower half dedicated to the VIA IC. The VIA IC has two input select lines, /CS2 (U1220A, pin 12) and CS1 (U1223B, pin 16). The /CS2 signal must be low for the microprocessor to access either the GPIB or the VIA. The high level CS2 signal on pin 14 of U1223C enables logic gate U1220B at pin 5. With U1220B enabled and assuming a high level also on pin 4, the logical state of address bit IBA6 determines which of the two ICs are being addressed by the microprocessor. When IBA6 is high, the GPIB Control IC is being selected by the high-level CS1 signal on pin 12 of U1223D.

The GPIB Control and VIA ICs are accessed in different ways, due to different access and setup times. The GPIB is selected only during the time that the buffered clock (B02) and the buffered valid memory address (IBVMA) signals on pins 5 and 4 of U1219B are both high. The VIA IC, due to its very long access time, must be directly clocked by B02 from pin 14 of U1210D.

Primary and Secondary Decoders

Integrated circuits U1224 and U1225 are the Primary and Secondary Decoders, respectively. Address bits IBA13, IBA14, and IBA15 divide the 65-Kbyte memory into eight 8-Kbyte blocks (decimal) or eight 2-Kbyte blocks (hexadecimal). For example, the hexadecimal range at pin 15 of U1224 is from 0000 through 1FFF, while the range at pin 7 is

E000 through FFFF. The binary code on pins 3, 2, and 1 of U1224 is 000 through 111, selecting outputs Y0 through Y7. Five of the addressed outputs, Y2 through Y6, are not connected to any other devices because those addresses are dedicated to the 40-Kbyte bank region on the external bus (see Table 5-2). BVMA is the only enable line for U1224. Pin 7 of U1224, when low, enables the ROM IC.

The Secondary Decoder, U1225, is a dual one-of-four decoder, one-half of which is enabled with a low level on pin 1 for all addresses in the 2000-3FFF range. Address bit IBA12 and IBA11 are decoded on pins 3 and 2, respectively. The binary code for these address bits (00 through 11) selects outputs U1225A Y0 through Y3. The logical states of the signal lines on pin 13 and 14 are decoded by U1225 during the low-level clock period on pin 15 to select outputs U1225B Y0 or Y1.

When hexadecimal address 3000 appears on the address lines, the AY2 output (pin 6) goes low and sets a low on pin 13 of U1225. When the read/write signal on pin 14 goes low for a write operation, the binary code (00) on pins 13 and 14 selects the BY0 output to go low. A low on pin 12 enables the inputs of the Circuit Select Latch, U1207, during the negative half of the clock period on pin 15 of U1225. The microprocessor never reads the Circuit Select Latch; a copy of the latch's data is stored in RAM. When pin 14 of U1225 goes high for a read operation, the binary code for pins 13 and 14 is 01. This code selects the BY1 output (pin 11) to go low and disables logic gate U1216B at pin 3. This, in turn, sets a low on pin 16 of U1223B and disables the external and internal buses via pins 1, 12, 4, and 6 of U1217A and U1217B, respectively. With these two buses disabled, the microprocessor can then proceed to use its data bus (D0-D7) to read the contents of the Address Switch Register in U1218. The Address Switch Register is enabled by the low-level ASE signal on pin 19.

The System RAM, U1222, is selected when pin 4 of U1225A goes low. Pin 7 of U1225A goes low when the microprocessor enters the signature analysis mode.

Signature Analysis

The signal at test point TP1207 (pin 4 of U1236A) has two possible uses; troubleshooting the instrument using signature analysis methods, or using the signal to trigger a logic analyzer at the beginning and end of data transfer over the digital interface. The device can be configured for the signature analysis (SA) mode by physically relocating the position of J1209.

Integrated circuit U1236A is a latched SR flip-flop with the output on pin 4 normally high. When the microprocessor places hexadecimal address 3800 on the internal bus, pin 7 of U1225A and pin 1 of U1236A go low. Pins 2 and 3 of U1236A must also be high (indicating a write operation with a valid memory address) to toggle U1236A from a high state to a low state. Pin 4 remains in the low state as long as the address remains on the internal bus. When the address is removed, pin 4 returns to its normally high state. Pin 1 of U1236A goes low for any hexadecimal address in the 3800-3FFF range.

Bus Select Decoder

Integrated circuit U1217, along with U1216B, U1223B, and U1223G, operates as the Bus Select Decoder.

Both of the external and internal buses can be disabled via U1216B, U1223B, and U1217 at the same time under three conditions: (1) when the microprocessor's internal RAM is disabled and a low is set on pin 5 of U1216B; (2) when the Address Switch Register, U1218, is selected to be read and a low is set on pin 3 of U1216B; and (3) when pin 4 of U1216B is set low. Whenever both external and internal buses are disabled, the microprocessor is limited to reading the contents of the Address Switch Register via the D0-D7 data lines. The internal and external buses will never be enabled at the same time; if one is on, the other is off.

Pins 9, 10, and 11 of U1217 are connected to the decoded 0000, 2000, and E000 addressed outputs from U1224. The external bus (U1217A, pin 12) is enabled via a high level on pin 5 of U1223G as long as these three inputs to U1217C (pins 9, 10, 11) remain high. If any pin (9, 10,

11) goes low, the external bus is disabled by a low level on pin 5 of U1223G and the internal bus is enabled by the high level on pin 5 of U1217B. The external bus can also be disabled by a low level signal on pin 13 of U1217A.

The external bus can be mechanically disabled, even when pin 12 of U1217A is low, by relocating J1204 from pins 1 and 2 to pins 2 and 3. The low-level output from U1209C is then changed to a high level, which disables the external data bus transceiver, U1206. The low-level external bus signal on pin 9 of U1209C is gated with the low-level clock signal on pin 10. The gating of these two signals ensures that the external data bus is not enabled until the address and control lines have had time to settle.

The internal bus (U1217B, pin 6) is enabled via a high level on pin 5 of U1217B as long as pins 3 and 4 remain high. If any pin (3, 4, 5) goes low, the internal bus is disabled. Note that the external and internal buses are both disabled when the microprocessor's internal RAM is active; pin 8 of U1220C and pins 3 and 2 of U1217B and U1217A will all be low. Pin 2 of U1217A will be low because pin 9 (0000) will be low. The complete Bus Select Decoder circuit operates to ensure that only one of the three data buses or the microprocessor's internal RAM is operating at any given time. See Table 5-3.

Control Line Buffers

The control line buffer circuit is composed of U1228, U1209A, U1209D, U1210D, and U1219C. The valid memory address and read/write signals are first buffered by U1209A (pin 2) and U1209D (pin 12), respectively.

The outputs of the first buffers are then divided into four separate control signals at the output of U1228, two for the external bus areas of memory and two for the internal areas of memory. In normal operation, the input signals to U1209A, U1209D, and U1228 pass through without inversion.

Table 5-3

Bus Selection

Mode	Internal Bus	External Bus	Address Switch	Comment
Internal access	On	Off	Off	0000–3FFF E000–FFFF
External access	Off	On	Off	4000–DFFF
Forced instruction	Off	Off	On	Cycle through all 65K memory continuously.
Address switch access	Off	Off	On	3000 (read only)
Micro-processor internal RAM access	Off	Off	Off	0000–007F
Jumper inhibit of external bus	X	Off	X	External bus shut off via J1204.

The microprocessor clock output is buffered by U1210D with complementary outputs on pins 14 and 13. The buffered clock signal on pin 14 of U1210D is used by both the external and internal areas of memory; this signal is terminated by the parallel combination of R1203 and R1204. The voltage level at the junction of these two resistors biases the high-level state of the clock to about 3.6 volts.

Integrated circuit U1219C is always enabled at pin 12 and gates the internal bus read/write signal on pin 11 through to toggle the SA test point TP1207 on a write operation.

INTERNAL MEMORY and I/O CONTROL (Diagram 3)

System RAM

The System RAM, U1222, provides the microprocessor with a random access memory space (2K x 8). The microprocessor uses hexadecimal addresses in the 2000–27FF range to address the System RAM.

The most significant bit (IBD7) is tied high via R1219. This resistor allows the operating system to determine how much RAM space is available. For example, the microprocessor writes 0s to the bottom half of each 1K–byte block from locations 2000 through 2FFF (2000, 2400, 2800, and 2C00). If it then reads back, for example, 0 for 2000, 0 for 2400, F for 2800 and 2C00, it knows that a total of 2K–bytes of RAM space is available and where it is located. The microprocessor looks at data bit IBD7, which will always be high if there is no memory at a given address to pull it low when read back.

System ROM

The hexadecimal address range for the System ROM U1231 is E000 through FFFF.

When address E000 appears on the internal address bus, pin 1 of U1216A goes high. This action enables (selects) U1231 to respond to all addresses in the E000–FFFF range. The read operation on the output data port of U1231 begins when the clock signal on pin 2 of U1216 goes high and sets a low on pin 22 of U1231.

Circuit Select Latch

Integrated circuit U1207, with eight internal D–type flip–flops and single rail outputs, operates as the Circuit Select Latch. Output CSEL_1 is used to select the Front Panel Interface (FPI) memory and decoder circuit.

When the microprocessor enables the data inputs of U1207 with a low level on pin 1 (3000), it performs a write operation to select the FPI circuit. Data is presented at the 1D through 8D inputs and this data is latched on the output port (1Q through 8Q) about 30 ns after the inverted clock signal on pin 11 goes high. After the FPI circuit is selected, pin 1 of U1207 goes high and the circuit select data remains on the output port until pin 1 goes low again to enable U1207 for another circuit select operation. A read operation is not performed on U1207; circuit select information is stored in RAM.

Service Display DS1202

The Service Display circuit consists of DS1202, U1236C, U1236B, and associated components. The BCD decoder, clocked latch, and current limited LED are all contained within DS1202.

The readout is in hexadecimal format with one of sixteen characters (0...9, A...F) displayed. The display is blanked for every half-cycle of the buffered clock signal on pin 8 (pin 8 goes high). BCD data corresponding to error codes is stored in the peripheral data output registers for the PA port of U1226. This data is transferred from U1226 to the internal latches of DS1202 each time the clock signal on DS1202 pin 5 goes high.

If the microprocessor board is properly initialized and no errors are detected, the digit 0 will be displayed. If initialization is incomplete, all of the BCD inputs will be high and the letter F will be displayed. Errors detected during the power-up self-test routine are displayed as one digit or alpha character.

Two decimal points, one left-hand and one right-hand, are used to indicate the condition of the inverted buffered clock signal on pin 6 of U1236B. When pin 6 goes low, pin 7 goes high, turning off the left-hand decimal point. The low-to-high transition on U1236B pin 7 and U1236C pin 12 also causes U1236C pin 9 to go low, turning on the right-hand decimal point. With the right-hand decimal point on, if the RESET line (U1236C, pin 11) goes low pin 9 will go high, turning off the right-hand decimal point.

At power-on the RESET line goes low for about 2-3 seconds, blanking the right-hand decimal point for that period of time. It then goes high and remains high unless a momentary power failure occurs.

Since the outputs of U1236B (pin 7) and U1236C (pin 9) are complementary, the only way for both decimal points to appear to be on is for the clock signal to be running. If the clock signal is locked high or low, one or the other of the decimal points will be completely turned off. If the clock duty cycle is very far off from the normal 50% value, one or the other decimal point will appear brighter, due to intensity modulation. Observing the decimal points yields information about the clock and the RESET line.

NOTE

Refer to Service Display Codes in the Maintenance section of this manual for diagnostic codes associated with DS1202.

Versatile Interface Adapter (VIA)

The Versatile Interface Adapter, U1226, operates as an input/output control device. Control of peripheral devices is handled primarily through two 8-bit bidirectional ports, PA0-PA7 and PB0-PB7. Each PA and PB line can be programmed as either an input or an output.

NOTE

For more detailed information on the internal operation of U1226, refer to the manufacturer's data sheet.

Four register select inputs, RS0, RS1, RS2, and RS3, permit the microprocessor to address U1226 and select any one of 16 internal registers. Register select coding is with address bits IBA0 through IBA3 on pins 38, 37, 36, and 35, respectively. The address coding to select an internal register is shown in Table 5-4.

Table 5-4

U1226 Internal Registers

Register Number	Register Select Codes				Description	
	RS3	RS2	RS1	RS0	Write	Read
0	0	0	0	0	Output Reg. B	Input Reg. A
1	0	0	0	1	Output Reg. A	Input Reg. A
2	0	0	1	0	Data Direction Register B	
3	0	0	1	1	Data Direction Register A	
4	0	1	0	0	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1 High-Order Counter & Latch	T1 High-Order Counter
6	0	1	1	0	T1 Low-Order Latches	
7	0	1	1	1	T1 High-Order Latches	
8	1	0	0	0	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2 High-Order Counter	
10	1	0	1	0	Shift Register	
11	1	0	1	1	Auxiliary Control Register	
12	1	1	0	0	Peripheral Control Register	
13	1	1	0	1	Interrupt Flag Register	
14	1	1	1	0	Interrupt Enable Register	
15	1	1	1	1	Same as Reg 1 Except No Handshake	

Two IC select inputs, CS2 and CS1 (pins 23 and 24), are used to enable U1226 and allow access to an internal register. The selected (addressed) register is accessed when pin 24 is high and pin 23 is low. Refer to the discussion under Page 0 Decoder and Table 5-2 for address decoding (IC select) information. At power up, the reset signal on pin 34 goes low to clear all of the internal registers to logical 0 (except the internal timers at pins 16 and 17 and the internal shift register). Clearing the internal registers places all of the peripheral interface lines in an input state, disables the timers, shift register, and the interrupt output on pin 21. After the reset signal goes high, the microprocessor can then communicate with U1226.

Assuming that U1226 has been enabled on pins 23 and 24, communication is over the data lines on the internal bus, IBD0-IBD7 (pins 26 through 33). The direction of data transfers between U1226 and the microprocessor is controlled by the read/write signal on pin 22. When pin 22 is low, data will be transferred into a selected internal register; when pin 22 is high, data will be transferred out of a selected internal register. Data transfer in either direction occurs during the high-level clock period on pin 25. When U1226 is not selected, the internal data bus goes to the high-impedance state.

The internal timers (TMR 1 and TMR 2, pins 17 and 16) are used for the WAIT INTERVAL command. Timer 2 generates a 10 ms period pulse string to Timer 1. Timer 1 contains the number of 10 ms periods that the microprocessor must wait before it executes the commands in the program storage buffer. This number of periods can be the equivalent of 0 seconds up to 655.35 seconds.

The LED indicators, DS1200 and DS1201, are illuminated whenever the microprocessor sets a high level on either U1226, pin 14 or pin 15. Both indicators are not normally illuminated at the same time.

Pin 21 of U1226 goes low to notify the microprocessor when an enabled interrupt occurs within U1226. Interrupts may be caused by the active edge of a signal applied to inputs CA1 (pin 40), CA2 (pin 39), CB1 (pin 18), CB2 (pin 19), and time out events of Timer 1 and Timer 2. The logical 0 state of pin 21 can only be cleared by clearing all enabled interrupts.

Address/Service Switch Register

The Address/Service Switch Register is composed of SW1100, U1218, and associated components. Five internal contacts of SW1100 are labeled as to their binary weight with the top switch (TC, pins 1 and 12) being the message terminator switch. An open switch equals a logical 1 (high) set on the inputs to U1218, A1 through A6; a closed switch equals a logical 0 (low). At power-up, the microprocessor reads the address switch via buffer U1218 and stores it in an address register located in the GPIB Control IC, U1203. A read-only operation is performed on U1218 by enabling U1218 with a low on pin 19 during the time that pin 1 is also low.

Pin 8 of U1218 is used for placing the operating system in the signature analysis (SA) mode. The CAL mode (pin 6) is not used. Pin 8 of U1218 is normally high; it is pulled low by relocating J1208.

The microprocessor can be placed in a forced instruction mode by relocating J1208, J1209, and J1210 so that pins 3 of J1210 and J1208, and pin 1 of J1209 are all grounded. This action disables the internal data bus, the external data bus, and the microprocessor's internal RAM.

After J1208, J1209, and J1210 have been repositioned for the forced instruction mode, it is necessary to set SW1100 so that the TC (message terminator) switch is open (high = 1) and all others closed (low = 0). This places hexadecimal code 01 on the microprocessor data bus (D0–D7). With the internal data bus, external data bus, and the microprocessor's internal RAM disabled, the microprocessor will always read hexadecimal code 01 on its data port. This is a NOP (no operation) code that tells the microprocessor to advance its internal program counter by one count. This causes the microprocessor to address all locations in the total memory space indefinitely, in a sequential manner. The internal address buffers and the control line buffers are enabled during this operation. As a result, all of the address select lines to the memory devices (except pin 1 of U1207) are exercised when that device's address appears on the address bus. The microprocessor never performs a write operation on any memory device while in the forced instruction mode.

GPIB Control

NOTE

For more detailed information on the internal operation of the GPIB Control IC (U1203), refer to the manufacturer's data sheet.

Integrated circuit U1203 performs the interface function between the microprocessor and the digital interface specified in IEEE Standard 488-1978. The handshake process for the DAV, NRFD, and NDAC lines on the digital interface is handled automatically within U1203. The IC is selected by a low level on pin 3 for all addresses in the 00C0-00C7 range. See Table 5-2.

Communication between U1203 and the microprocessor is via the internal data bus (IBD0-IBD7) and fourteen internal memory-mapped registers. The logical state of the three least significant bits (IBA0, IBA1, and IBA2; pins 6, 7, and 8) determine which internal register is selected. A read operation clocks data out of an internal register back to the microprocessor, and a write operation clocks data into an internal register. For a read operation on U1203, pins 4 and 5 will be high; for a write operation, pins 4 and 5 will be low. Data is transferred in both directions on the positive edge of the clock signal on pin 18. Reading and writing to the same address will not access the same register within U1203 because they are "read only" or "write only" registers. Internal register select coding is shown in Table 5-5.

When U1203 detects the IEEE 488 talk or listen address for the GPIB controller, it responds by entering the required addressed state and generates a low-true interrupt signal on pin 9. Interrupts to the microprocessor are generated by the following basic events:

- A data byte has been received.
- Ready to accept the next (or first) data byte.
- The Group Execute Trigger (GET) message has occurred.

- Device Clear Active State (DCAS) has occurred.
- My talk or listen address has been received.
- A Serial Poll Active State (SPAS) has occurred with bit 7 set in the serial poll register.

The buffered trigger signal on pin 14 of U1227D and pin 39 of U1203 can be generated in one of two ways, either by the GET message over the IEEE 488 digital interface or by a forced GET command from the microprocessor.

The talk enable (TE) output on pin 21 of U1203 controls the direction of data byte transfer through bidirectional bus transceiver U1201 and direction of signal flow through line transceiver U1202. When pin 21 is high, data byte transfer is output to the IEEE 488 digital interface; when low, data byte transfer is input to U1203. None of the /CE, /TE, or /SYS signal outputs are connected to the IEEE 488 digital interface.

Table 5-5

U1203 Internal Registers

Register Select Code			Description	
RS0	**RS1**	**RS2**	**Read Only**	**Write Only**
0	0	0	Interrupt Status 0	Interrupt Enable 0
0	0	1	Interrupt Status 1	Interrupt Enable 1
0	1	0	Address Status	Auxiliary Command
0	1	1	Bus Status	Address Register
1	0	0	Address Switch 1	Serial Poll
1	1	0	Command Pass Through	Parallel Poll (not used)
1	1	1	Data Input	Data Output

Integrated circuit U1201 contains active pull-up components for fast recovery of the changing data lines. The normal operating mode for U1201 is with pin 11 at a high level. However, the IEEE 488 standard requires that the data lines go to an open-collector state for a parallel poll. When both EOI and ATN lines on the digital interface are asserted low true, pin 11 of U1201 goes high, disabling the internal active pull-up components. Pin 11 returns to the high state at the end of a parallel poll. The GPIB Controller does not respond to parallel poll messages from the IEEE 488 digital interface.

RESET, MEMORY, AND DECODERS (Diagram 4)

Power Supply

The purpose of the power supply is to provide a five-volt digital supply for the 067-0557-00 calibration fixture, using 18 Vac from a plug-in wall transformer.

The input voltage from the plug-in wall transformer is full-wave rectified by CR1103 and filtered by C1118, C1119, and the inductance of the transformer. In line with CR1103 is fuse F1101, which limits the input current. F1101 is paralleled by DS1103 (a visual indicator of an open fuse) and R1118. Following the fuse is power switch SW1101, POWER ON indicator DS1104, and R1119.

U1121 is a pulse-width modulator regulator which is configured in the positive buck converter mode. U1121 operates in the current-control mode rather than the normal voltage-control mode. This means that the switch duty cycle is controlled by the switched current rather than by output voltage. U1121 (VSW pin 4 to GND pin 2) and CR1102 conduct alternately so that the voltage applied to L1100 is either the dc input voltage or zero. If T1 is the time U1121 is conducting, and T2 is the time U1121 is not conducting or CR1102 is conducting, Vout is equal to Vin $\times$ [T1/(T1 + T2)] or Vin $\times$ duty cycle where duty cycle = T1/(T1 + T2). The output voltage is sensed and applied to the FB input which is the negative input of an error amplifier. The output of

the error amplifier sets a trip level for the current through VSW to GND. This trip level for the current through VSW to GND then determines the duty cycle of T1 (the time U1121 is conduction charging L1100) and T2 (the time U1121 is not conducting and L1100 discharging). The GND pin (pin 3) of U1121 is the driving point for the positive buck converter inductor L1100. U1121 pin 3 (GND) must therefore switch back and forth between the input voltage and converter ground. Therefore the bootstrapped supply voltage for U1121 pin 5 must be provided by using a peak detector composed of CR1100, C1130, and C1120. While U1121 is operating (switching), C1130 and C1120 will maintain an input-to-ground pin voltage at a voltage equal to the input supply voltage. Feedback pin 2 is referenced to GND pin 3, and therefore is switching along with U1121 GND. The feedback circuit must float on the switching ground pin and at the same time be proportional to the dc value of the output voltage. This is accomplished by peak detecting the output voltage with CR1101 during the off time of U1121. At the same time, the voltage on the ground pin of U1121 is one diode drop (CR1102) negative with respect to system ground. This is true because CR1102 is forward biased by load current flowing through L1100. C1122 will maintain the feedback voltage during the on-time of U1121.

CR1102 is a unidirectional switch which is closed when U1121 (VSW pin 4 to GND pin 3) is open and not conducting. This provides a return path for the energy-storage inductor L1100 to discharge its stored energy. R1131 and C1121 form a frequency-compensation network for the error amplifier to provide acceptable loop stability. C1123 acts as an energy-storage element and filter for the output. L1101, C1124, and C1125 form a two-pole filter for further reduction of the output voltage ripple.

Reset Circuit

The Reset Circuit operates as follows: As the 5-volt power supply turns on, its output voltage rises to 5 volts. The reference voltage on pin 4 of U1122A will initially be higher than the voltage on pin 5, causing the output on pin 2 to be low. As the output voltage from the power supply nears 5 volts, pin 5 will become higher in potential than pin 4, driving the output of U1122A high. This allows C1128 to start

charging through R1128. As soon as the potential on pin 7 of U1122B is greater than the potential on pin 6 of U1122B (the 3-volt reference voltage), the output of U1122B (RESET) will go high. If, for some reason, the supply voltage dips below 4.15 volts, the output of U1122A will go low and begin to dump the capacitor. If the power supply stays low, the potential at pin 7 will become less than the reference voltage and RESET will be asserted.

Memory and Decoders

The microprocessor in the GPIB Controller selects the Front Panel Interface for data transfers (EBD0-EBD7) by setting pins 4 and 5 of U1106B high. The low level on pin 6 of U1106B enables the address decoder (U1108) on pin 5 and enables the bidirectional data buffer (U1100) on pin 19. Pins 4 and 5 of U1106B must be low and pin 6 must be high to enable the address decoder when a valid memory address (EBVMA) for the FPI appears on the external address bus (EBA0-EBA15).

The five control lines to the FPI are buffered by seven non-inverting buffers contained in U1101.

The Circuit Select and EBVMA lines are set high each time the microprocessor selects the FPI for a read or write operation on an addressed memory device. The read/write control signal on pin 5 of U1101 goes high for a read operation and goes low for a write operation. A write operation is never performed on the read-only-memory device (ROM, U1107).

The memory devices for the FPI consist of an 8K $\times$ 8 bit ROM (U1107) and two peripheral interface adapters (PIA), U1105 and U1109.

The 16 address bits (EBA0-EBA15) are buffered by unidirectional, noninverting buffers U1102 and U1103. The hexadecimal addresses for the FPI operating system are in the 4000-DFFF range.

Integrated circuit U1108 decodes buffered address bits BA13, BA14, and BA15 to select the ROM or both PIAs for addressing. The ROM (U1107) is selected when the microprocessor places hexadecimal address 4000 on the external address bus, setting pin 20 of U1107 to a

low state. An instruction word is placed on the BD0–BD7 data bus when the read/write and clock signals on pins 1 and 2 of U1106A both go high.

Both peripheral interface adapters, U1105 and U1109, are selected for addressing when hexadecimal address 8000 sets pin 23 on each device to a low state. Buffered address bit BA3 is inverted by U1104C. The inversion of BA3 allows the microprocessor to select either U1105 or U1109 for data transfer. Communication with the internal registers of U1105 and U1109 is via address bits BA0 and BA1. For either PIA, pin 23 must be low and pin 24 must be high to select the proper data channel. Buffered data is clocked into (a write operation) or out of (a read operation) an internal register on the rising edge of the clock signal on pin 25 of either PIA.

NOTE

For more detailed information related to internal register selection for U1105 or U1109 refer to the manufacturer's data sheet.

At power-up the RESET control line (U1101, pin 14) goes low. This resets all of the internal registers of the PIAs to zero. The microprocessor then configures all of the CA1, CA2, CB1, CB2 ports of the PIAs as inputs. The CA2 port (U1105, pin 39) is held high by R1101. This causes the ERROR light, DS1100, to be illuminated with a low level on pin 4 of U1104B until the completion of the self-test routine. Upon successful completion of the self-test routine, the CA2 port (U1105) is programmed to a low state, turning off the ERROR light. If an FPI related error occurs, the CA2 port (U1105) is programmed to a high state, keeping DS1100 illuminated.

Interrupt signals to the microprocessor in the GPIB Controller are via the IRQ lines (pins 37 and 38 on the PIAs). An interrupt from either PIA causes pin 8 of U1106C to go low and remain low until the microprocessor clears the interrupt condition.

The BFR TRIG (Buffered Trigger) signal on pin 18 of U1101 is generated via the GPIB Control chip in response to the GET (Group Execute Trigger) interface message sent over the IEEE 488 digital interface.

The CA1 port for U1105 (pin 40) operates as a feedback interrupt flag path that allows the microprocessor to know that the FPI circuit has received the BFR TRIG signal.

FRONT PANEL INTERFACE (FPI) (Diagram 5)

The Front Panel Interface Circuit (FPI) is designed to mimic the 2246 1Y and 2246 Mod A (SN B100100 and up) oscilloscope front panel. The circuit provides to the 2246 oscilloscope 16 correctly timed data bits which are interpreted by the 2246 as front panel data. All data and signals between the GPIB Controller and the 2246 are contained on a 10-pin connector, J1103.

NOTE

For more information on the operation of the 2246 front panel, refer to the Tektronix 2246 1Y and Mod A oscilloscope manuals.

The FPI generates 16 data bits through two 3-to-8 decoders, U1110 and U1111. The select and enable lines (G1, pin 6) of these decoders are sourced from U1105 and U1109 (diagram 4), making these signals controllable by the microprocessor. A qualifying signal, /DTACK is common to all six NAND gates, U1112A, B, and C; and U1113A, B, and C. To select a specific column, the microprocessor selects one of the six data lines, ENCOL0-ENCOL5. If the selected data line is high and /DTACK is high, the 3-to-8 decoders will be enabled during the time the appropriate column strobe is high, thus insuring the correct timing of the data bits.

The 16 data bits are then loaded into two parallel-in, serial-out shift registers (U1119 and U1120) by a load signal, SH-/LD, from the 2246. Another signal, CLK, from the 2246 then shifts the bits out serially through pin 9 of U1120. The signals pass through a tri-state buffer, U1115; a pull-up buffer composed of Q1102 and Q1103, and out of the GPIB Controller to the 2246 oscilloscope.

An enable/disable front panel signal line, /ENDATOUT, controls the output of the tri-state buffers. With the tri-state buffers enabled, data from the GPIB Controller will override existing front panel data from the scope, thereby effectively locking the front panel. With the tri-state buffers disabled, the 2246's own front panel data is used. LED DS1102 indicates the state of the /ENDATOUT line; if the front panel of the 2246 is disabled, the LED will be on.

There is one special case that needs to be taken care of separately: the diagnostic menu. In this case, two buttons (MENU1 and MENU6) need to be pressed at the same time. This means that two bits, not the normal one bit, need to be high for a complete front-panel scan. U1114A, U1114B, U1115C, and U1115D accomplish this. If the control line DIAG is high, the tri-state buffers will be disabled during COLSTRB5 and COLSTRB3. The outputs of the tri-state buffers are tied high by R1114 and R1115, and therefore high bits will be clocked into the shift registers on COLSTRB5 and COLSTRB3. The data, as scanned from COLSTRB3 to COLSTRB5, will look like this:

0100000000000000 0000000000000000 0010000000000000

When the 2246 accepts data, it will do two load pulses on its SH-/LD line. U1114C, U1116A and B, U1117A and B, and U1118A and B detect this condition. These six flip-flops and the 3-input AND gate form a state machine which operates as follows: /DTACK, the output from the state machine, is normally low, disabling the ability of the FPI to write data. To initiate a write, the W signal must pulse, which sets the /DTACK signal false (high). If the write is successful, the 2246 will do two load pulses on the SH-/LD line, which will set /DTACK low again. For the special case of the diagnostic menu, the circuitry looks for two sets of two SH-/LD pulses.

SECTION 6

Maintenance

GENERAL AND CORRECTIVE MAINTENANCE

Static-Sensitive Components

The following precautions apply when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Keep anything capable of generating or holding a static charge off the work station surface.

Table 6-1

Relative Susceptibility to Static-Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFET	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a] **Voltage equivalent for levels (voltage discharged from a 100-pF capacitor through resistance of 100 Ω):**

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V (est)
8 = 900 V
9 = 1200 V

5. Keep the component leads shorted together whenever possible.
6. Pick up components by their bodies, never by their leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

Cleaning

Do not allow moisture to get inside the instrument during external cleaning. Use only enough liquid to dampen the cloth or applicator.

This instrument should be cleaned as often as operating conditions require. Loose dust accumulated on the outside of the instrument can be removed with a soft cloth or small brush. Remove dirt that remains with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

To clean or inspect the inside of the instrument, first refer to the Removal and Replacement Instructions in this section. The best way to clean the interior is to blow off the accumulated dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water.

If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 1% mild detergent and 99% water. Use clean water to rinse.

Circuit boards and components must be dry before applying power to the instrument.

Dry all parts with low-pressure air. Components and assemblies may be dried in an oven or drying compartment using low-temperature (125°F to 150°F) circulating air.

Obtaining Replacement Parts

Electrical and mechanical replacement parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components may be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., check the Replaceable Electrical Parts list for the proper value, rating, tolerance, and description.

NOTE

The physical size and shape of a component may affect instrument performance. Always use direct-replacement components, unless it is known that a substitute will not degrade performance.

Some parts are manufactured or selected by Tektronix to satisfy particular requirements. To determine the manufacturer, refer to Cross Index—Mfr. Code Number to Manufacturer at the beginning of the replaceable parts lists.

When ordering replacement parts from Tektronix, include the instrument type, a description of the part (if electrical, include the complete component number), and the Tektronix part number.

Soldering Techniques

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts. General soldering techniques that apply to maintenance of any precision electronic equipment should be used when working on this instrument.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base

material and melt the insulation on small wires. Always keep the soldering iron tip properly tinned to ensure the best heat transfer from the tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

CAUTION

Only a maintenance person experienced in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

Transistors and Integrated Circuits

Transistors and integrated circuits should not be replaced unless they are actually defective. If one is removed from its socket or unsoldered from the circuit board during routine maintenance, return it to its original board location. Any replacement component should be of the original type or a direct replacement.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the IC from the socket before the other. To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

Removal and Replacement Instructions

Cabinet Separation

To access the interior of the fixture, separate the cabinet top from the cabinet bottom as follows:

Be sure the calibration fixture is disconnected from the power source.

Turn the fixture upside down and remove the four screws from the corners of the cabinet. Use a number 15 torx screwdriver tip to remove the screws.

A20—Upper Board Removal

To remove A20—Upper board, do the following:

Unplug the ribbon cables from J1103, J1101 and J1100 on the Upper board.

Use the torx number 15 tip to remove the six screws at the edges of the board that attach the Upper board to the cabinet top.

The POWER ON and CONTROLLER ENABLED LEDs are mounted on the front of the cabinet top, and the LED wires are attached to the Upper board. When removing the Upper board, unsolder and remove the wires at their board connection, noting the board location of the wires for reassembly. Leave the LEDs mounted on the cabinet front.

Raise the rear of the circuit board until it just clears the back of the cabinet top and continue backing the board from the cabinet until the power-switch button clears its cabinet slot. Continue removal.

A10—Lower Board Removal

Separate the top cabinet from the bottom cabinet as described in Cabinet Separation.

Unplug the ribbon cables from J1200 and J1201.

Remove six screws from the edges of the Lower circuit board, using the number 15 torx screwdriver tip. Lift out the Lower board.

Reassembly

To reassemble the calibration fixture, reverse the removal procedures.

DIAGNOSTICS AND TROUBLESHOOTING

Troubleshooting Aids

Schematic diagrams are located in Section 8, Diagrams and Circuit Board Illustrations. The diagrams include the assembly number and name of the circuit board near the bottom edge of the diagram. Functional blocks on the schematic diagram are outlined with wide gray lines. Components within the outlined area perform the function named by the block label. The Theory of Operation uses these functional block names when describing circuit operation. Component numbers and electrical values of components in the instrument are shown on the schematic diagrams.

Circuit board illustrations in the Diagrams section show the physical location of components and instrument test points.

The schematic diagrams and circuit board illustrations have grid borders along their left and top edges. The grid coordinates for the components are given in an accompanying table.

Any signal name preceded by a slash (in the Theory of Operation or the schematic diagrams) indicates that the signal performs its intended function when it is in the Low state; for example, /ADDR.

DS1202 Service Display Codes

Table 6–2 is a summary of the digits that may be displayed on DS1202 and the problems associated with the each digit.

Table 6-2
DS1202 Service Display Codes

Displayed Digit	Associated Problem
0	No errors, self-test completed
1	EO ROM (U1231)
2	FO ROM (U1231)
3	ROM (U1231)
4	System RAM (U1222)
5	Internal RAM (U1214)
6	GPIB IC (U1202)
7	VIA (U1226)
F	Self-test not completed, or in Forced Instruction mode.

Upon power-up, the 067-0557-00 goes through a self-test routine. If the self-test routine is completed with no errors, a **.0.** appears in the DS1202 display. The relative brightness of the two decimal points indicates the duty cycle of the clock waveform. Both decimal points should be approximately the same brightness to indicate that the clock waveform is approximately at a 50% duty cycle. The right-most decimal point will be illuminated when the RESET line is high.

During the self-test routine, if the microprocessor (U1214) internal RAM is defective, a **5** is displayed on DS1202. At this point, the calibration fixture halts operation. The ERROR (DS1201) and ADDRESSED (DS1200) indicator lights should remain on.

The next check performed is system RAM, U1222. If this test fails, a **4** is displayed by DS1202. Execution is halted and the ERROR and ADDRESSED LEDs are illuminated.

The next step is a ROM check (U1231). The ROM is divided into two sections, EO and FO. If the EO ROM section fails the test, a **1** is displayed; if the FO ROM section fails, a **2** is displayed. If both sections

fail the test, a **3** is displayed. At this point, the execution halts in a loop accessing each section. The ERROR and ADDRESSED lights will be on.

The peripheral registers are checked next. If the GPIB IC U1202 is not operating, a **6** is displayed. If the VIA (Versatile Interface Adapter) U1226 is not operating, a **7** is displayed. If these ICs are not operating, execution halts. An **F** is displayed if the power-up routine is not completed and the error is not determined as above, or if the unit is in the forced instruction mode.

If all tests are passed, the kernel is verified, the GPIB IC is initialized, and power-on SRQ is asserted.

Signature Analysis

Test Equipment

A signature analyzer, such as the Hewlett Packard HP 5006A, is required test equipment for signature analysis troubleshooting.

SA Mode Limits

The major areas where the SA (signature analysis) mode is of little value are:

- Where the SA mode depends on a circuit or device to run the SA routine; for example, certain ROM, microprocessor, or buffer faults.
- Where the fault is directly or indirectly related to the microprocessor phase two (02) clock, which provides the clock for the signature analyzer (test equipment).
- Where the signature analyzer test point flip-flop (U1236) fails to generate the Start/Stop pulse for the signature analyzer.

Test Mode Setups

Power up the signature analyzer. After it has powered up, set the Start, Stop, and Clock for negative slope (all three buttons in). Check that the Hold and Self Test buttons are out.

Connect the test pod to the signature analyzer, the Clock lead to U1214-37 (02), the Start and Stop leads to TP1207 (SA), and the GND lead to Ground. Now connect the data probe to the signature analyzer. This probe will be used to acquire the actual signature data.

To enter the SA mode, power down the calibration fixture, place J1209 on pins 1 and 2, and power the calibration fixture back up. If this mode is entered properly, ERROR (DS1201) and ADDRESSED (DS1200) LEDs will be illuminated at one-half brightness. **.0.** will be displayed on Service Display DS1202.

Use the signature analyzer and Table 6-3 to troubleshoot the Lower circuit board. Probe the circuits (signals) at the locations given in the table and compare the signature analyzer display to the correct signature supplied in Table 6-3. Signal names in the table are in alphabetical (or alphanumeric) order and match signal names on the schematic diagrams.

Troubleshooting Hints

Use the following procedure for troubleshooting with the signature analyzer:

1. The observable symptoms should give you an indication of the area (block) that is causing the trouble. If so, follow steps 2 through 4 for that area. If not, follow steps 2 through 5 for the entire instrument.

2. Check for correct signatures at the important output points of the block or the device. (See Table 6-3.)

3. If the signatures are good at the given outputs, it is not necessary to check for correct signatures at the inputs. If the signature is incorrect at an output, then check all inputs to that block. Ignore

signal paths to an input that checks good. Trace back only from the point that had the incorrect signature.

4. Check the source point for a given signal path having the incorrect signature. If the source point signature is correct, the trouble must be between the source point and the last incorrect signature point. Try to find a common point with a number of inputs. If the common point signature is correct, all of the inputs and circuitry along those input paths are good.

5. Repeat steps 3 and 4 until you reach a block (device) where all inputs are good and the output is bad; the trouble must be in, or related to, that block.

All of the test point locations in the following signature list are located on A10—Lower board.

Table 6-3
SA Mode Signature List

Signal	Location	Pin	Signature
+5V	U1214	35	7023
A0	U1214	9	01CU
A1	U1214	10	566H
A2	U1214	11	12H7
A3	U1214	12	0AHP
A4	U1214	13	09UP
A5	U1214	14	A8UA
A6	U1214	15	210P
A7	U1214	16	P31H
A8	U1214	17	6A33
A9	U1214	18	H3A7
A10	U1214	19	1C1U
A11	U1214	20	8UC7
A12	U1214	22	HFHA
A13	U1214	23	8536
A14	U1214	24	A8AF
A15	U1214	25	3HUH
/ADDR	U1206	3	8911
ASE	U1206	11	F29U
/ASE[3000(R)]	U1218	19	C2CF
BA	U1214	7	0000
BANK	U1217	2	782C
/BANK	U1217	8	0808
BR/W	U1209	3	U60U
CARD SEL EN	U1207	1	37C4

Table 6-3 (cont)

Signal	Location	Pin	Signature
CSEL0	U1207	2	U58U
CSEL1	U1207	5	9CA8
CSEL2	U1207	6	UH73
CSEL3	U1207	9	PU1U
CSEL4	U1207	12	271H
CSEL5	U1207	15	8F44
CSEL6	U1207	16	H6UU
CSELEXP	U1207	19	050F
D0	U1214	33	A40U
D1	U1214	32	2PP2
D2	U1214	31	2U95
D3	U1214	30	A1C3
D4	U1214	29	2532
D5	U1214	28	4FP5
D6	U1214	27	FUUU
D7	U1214	26	AU09
DIO1	U1203	38	0AAP
DIO8	U1203	31	7023
/E000	U1224	7	F521
/E000H	U1216	13	C502
EBR/W	U1228	8	U60U
EBVMA	U1228	11	6P2A
EOI	U1203	27	AFA6
/EXTBUS	U1217	12	U36F

Table 6-3 (cont)

Signal	Location	Pin	Signature
/EXTBUS + 02	U1206	19	7226 or 7023 or U36F
GPIB CHIP EN	U1203	3	0H2F
/HALT	U1214	2	7023
/IBA7	U1220	9	933P
IBA12	U1231	18	HFHA
IBA13	U1204	9	8536
IBA14	U1204	13	A8AF
IBA15	U1204	7	3HUH
IBD0	U1205	2	4H85
IBD1	U1205	18	AU88
IBD2	U1205	4	AP05
IBD3	U1205	16	F023
IBD4	U1205	6	44A2
IBD5	U1205	14	2H75
IBD6	U1205	8	6FU0
IBD7	U1205	12	P96C
/INTDATAEN	U1205	19	5F18
/IRQ	U1214	4	3U93
LOW 2K	U1211	6	6044
LOW 256	U1220	1	H2A8
/MR	U1214	3	7023
NC	U1227	7	1P09
/NMI	U1214	6	7023
PA(/N)	U1226	2 through 9	3U93

Table 6-3 (cont)

Signal	Location	Pin	Signature
PB(/N)	U1226	10 through 17	U932
/RAM ENBL	U1214	36	7023
/RST	U1214	40	7023
W/R	U1210	9	862F
R/W	U1214	34	U60U
SA STRT/STP	TP1207		C811
SRQ	U1203	29	6113
SYS RAM CE	U1222	18	9716
SYS ROM CE	U1231	22	F521
TE	U1203	21	0C8H
VIA CE	U1226	23	3C92
VIACS2	U1220	5	4CC1
VMA	U1214	5	6P2A
/WE	U1227	9	U60U
/WRITEENBL	U1213	1	U60U
UP RAM ACT	U1220	8	5CH6
/0000	U1224	15	501U
/2000	U1224	14	PH15
/2000H	U1225	4	9716
/2800H	U1225	5	471A
/3000H(W)	U1225	12	37C4
/3800H	U1225	7	C811
/3800H	U1225	13	U52C
/4000	U1224	13	PUC8
/8000	U1224	11	899A
$0000H	U1220	8	5CH6

Table 6-3 (cont)

Signal	Location	Pin	Signature
$0080H	U1226	23	3C92
$0080N	U1226	24	512H
$00C0H	U1220	6	0H2F

SECTION 7

Replaceable Electrical Parts

Parts Ordering Information

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

List of Assemblies

A list of assemblies can be found at the beginning of the electrical parts list. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

Cross Index–Mfr. Code Number to Manufacturer

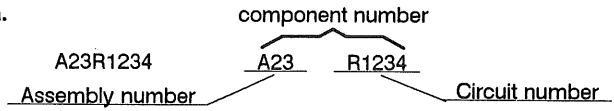
The Mfg. Code Number to Manufacturer cross index for the electrical parts list is located immediately after this page. The cross index provides codes, names, and addresses of manufacturers of components listed in the electrical parts list.

Abbreviations

Abbreviations conform to American National Standard Y1.1.

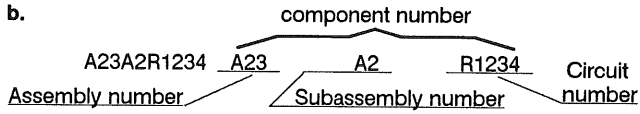
Component Number (column one of the parts list)

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

The component's circuit number appears on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the mechanical parts list. The component number is obtained by adding the assembly number prefix to the circuit number.

The electrical parts list is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the electrical parts list.

Tektronix Part No. (column two of the parts list)

Indicates part number to be used when ordering replacement part from Tektronix.

Serial No. (columns three and four of the parts list)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

Name & Description (column five of the parts list)

In the parts list, an item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. For further item name identification, the U.S. Federal Catalog handbook H6-1 can be utilized where possible.

Mfr. Code (column six of the parts list)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

Mfr. Part No. (column seven of the parts list)

Indicates actual manufacturer's part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	W GENESEE ST	AUBURN NY 13021
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
09922	BURNDY CORP	RICHARDS AVE	NORWALK CT 06852
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
14936	GENERAL INSTRUMENT CORP DISCRETE SEMI CONDUCTOR DIV	600 W JOHN ST	HICKSVILLE NY 11802
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
32159	WEST-CAP ARIZONA SUB OF SFE TECHNOLOGIES	2201 E ELVIRA ROAD	TUCSON AZ 85706-7026
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
34576	ROCKWELL INTERNATIONAL CORP SEMICONDUCTOR PRODUCTS DIV	4311 JAMBOREE RD PO BOX C	NEWPORT BEACH CA 92660-3007
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769-2963
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY PO BOX 1501	SECAUCUS NJ 07094-2917
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195-4526
56845	DALE ELECTRONICS INC	2300 RIVERSIDE BLVD PO BOX 74	NORFOLK NE 68701-2242
57668	ROHM CORP	8 WHATNEY PO BOX 19515	IRVINE CA 92713
59492	K AND L QUARTZTEK DIV OF K AND L MICROWAVE INC SUB OF DOVER CORP	20 S 48TH AVE	PHOENIX AZ 85043-3820
65786	CYPRESS SEMICONDUCTOR CORP	3901 N 1ST ST	SAN JOSE CA 95134-1506
75915	LITTELFUSE INC SUB TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016-3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
81073	GRAYHILL INC	561 HILLGROVE AVE PO BOX 10373	LA GRANGE IL 60525-5914
TK1345	ZMAN AND ASSOCIATES	7633 S 180TH	KENT WA 98032
TK2098	MINNESOTA MINING & MFG CO BRANCH OFFICE	100 ANDOVER PARK W	SEATTLE WA 98188-2801

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	671-1499-00			CIRCUIT BOARD:MGPIB,LOWER	80009	671-1499-00
A20	671-1288-00			CIRCUIT BD ASSY:MGPIB UPPER	80009	671-1288-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	671-1499-00			CIRCUIT BOARD:MGPIB,LOWER	80009	671-1499-00
A10C1200	281-0762-00			CAP,FXD,CER DI:27PF,20%,100V	04222	MA101A270MAA
A10C1201	281-0762-00			CAP,FXD,CER DI:27PF,20%,100V	04222	MA101A270MAA
A10C1202	281-0861-00			CAP,FXD,CER DI:270PF,5%,50V	04222	SA101A271JAA
A10C1203	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1204	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1205	290-0963-00			CAP,FXD,ELCTLT:220UF,+50-20%,25WVDC	80009	290-0963-00
A10C1206	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1207	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1208	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1210	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1211	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1213	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1216	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1218	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1219	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1220	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1222	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1223	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1224	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1225	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1228	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10C1230	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A10DS1200	150-1160-00			LT EMITTING DIO:GREEN	50434	QLMP 1587
A10DS1201	150-1160-00			LT EMITTING DIO:GREEN	50434	QLMP 1587
A10DS1202	150-1013-00			LAMP,LED RDOUT:RED,HEXADECIMAL W/LOGIC	01295	TIL 311

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10J1200	131-3147-00			CONN,RCPT,ELEC:HEADER,2 X 25,0.1 SPACING	53387	3596-6002
A10J1201	131-4114-00			CONN,RCPT,ELEC:HEADER,2 X 12,0.1 CTR	TK2098	3589-6002
A10J1204	131-0589-00			TERM,PIN:0.46 L X 0.025 SQ PH BRZ GLD PL	22526	48283-029
A10J1208	131-0589-00			TERM,PIN:0.46 L X 0.025 SQ PH BRZ GLD PL	22526	48283-029
A10J1209	131-0589-00			TERM,PIN:0.46 L X 0.025 SQ PH BRZ GLD PL	22526	48283-029
A10J1210	131-0589-00			TERM,PIN:0.46 L X 0.025 SQ PH BRZ GLD PL	22526	48283-029
A10L1200	108-0317-00			COIL,RF:FIXED,15 UH	32159	71501M+10PERCENT
A10P1204	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10P1208	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10P1209	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10P1210	131-0993-00			BUS,CONDUCTOR:SHUNT ASSEMBLY,BLACK	22526	65474-005
A10R1200	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A10R1201	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E
A10R1202	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E
A10R1203	322-3249-00			RES,FXD,FILM:3.83K OHM,1%,0.2W,TC=T0	56845	ORDER BY DESCR
A10R1204	322-3281-00			RES,FXD,FILM:8.25K OHM,1%,0.2W,TC=T0	57668	CRB20 FXE 8K25
A10R1208	313-1272-00			RES,FXD,FILM:2.7K OHM,5%,0.2W	57668	TR20JE 02K7
A10R1210	313-1302-00			RES,FXD,FILM:3K OHM,5%,0.2W	57668	TR20JE 03K0
A10R1211	313-1302-00			RES,FXD,FILM:3K OHM,5%,0.2W	57668	TR20JE 03K0
A10R1212	313-1302-00			RES,FXD,FILM:3K OHM,5%,0.2W	57668	TR20JE 03K0
A10R1213	313-1302-00			RES,FXD,FILM:3K OHM,5%,0.2W	57668	TR20JE 03K0
A10R1214	313-1105-00			RES,FXD,FILM:1M OHM,5%,0.2W	57668	TR20JE1M
A10R1215	313-1102-00			RES,FXD,FILM:1K OHM,5%,0.2W	57668	TR20JE01K0
A10R1216	313-1102-00			RES,FXD,FILM:1K OHM,5%,0.2W	57668	TR20JE01K0
A10R1217	313-1102-00			RES,FXD,FILM:1K OHM,5%,0.2W	57668	TR20JE01K0
A10R1218	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R1219	313-1103-00			RES,FXD,FILM:10K OHM,5%,0.2W	57668	TR20JE10K0
A10R1220	313-1821-00			RES,FXD,FILM:820 OHM,5%,0.2W	57668	TR20JE 820E
A10R1221	313-1821-00			RES,FXD,FILM:820 OHM,5%,0.2W	57668	TR20JE 820E
A10R1227	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E
A10R1228	313-1221-00			RES,FXD,FILM:220 OHM,5%,0.2W	57668	TR20JE220E
A10R1229	313-1221-00			RES,FXD,FILM:220 OHM,5%,0.2W	57668	TR20JE220E
A10U1200	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1201	156-1414-00			MICROCKT,DGTL:TTL,OCTAL GPIB XCVR DATA BUS	01295	SN75160 (N OR J)
A10U1202	156-1415-00			MICROCKT,DGTL:TTL,OCTAL GPIB XCVR MGT BUS	80009	156-1415-00
A10U1203	156-1444-01			MICROCKT,DGTL:NMOS,GPIB INTFC CONTROLLER	01295	TMS9914A (NL
A10U1204	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1205	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1206	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A10U1207	156-0913-00			MICROCKT,DGTL:OCTAL D FF W/ENABLE	01295	SN74LS377N
A10U1208	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1209	156-0479-00			MICROCKT,DGTL:QUAD 2-INP OR GATE	80009	156-0479-00
A10U1210	156-0696-00			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND	01295	SN4265N
A10U1211	156-0985-00			MICROCKT,DGTL:DUAL 5-INPUT NOR GATE	04713	SN74LS260(NORJ)
A10U1213	156-1065-00			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N
A10U1214	156-1342-00			MICROCKT,DGTL:NMOS,8 BIT W/CLOCK & RAM	04713	MC6802P
A10U1215	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1216	156-0386-00			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	01295	SN74LS10(N OR J)
A10U1217	156-0386-00			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	01295	SN74LS10(N OR J)
A10U1218	156-1277-00			MICROCKT,DGTL:LSTTL,3-STATE OCTAL BFR,SCRN	27014	DM81LS95ANA+
A10U1219	156-0696-00			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND	01295	SN4265N
A10U1220	156-0386-00			MICROCKT,DGTL:TRIPLE 3-INP NAND GATE	01295	SN74LS10(N OR J)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10U1222	156-1594-00			IC,MEMORY:NMOS,SRAM;2K X 8,150NS;,DIP24.6	65786	CY6116-55PC
A10U1223	156-1058-00			MICROCKT,DGTL:STTL,OCTAL SCHMITT TRIGGER	80009	156-1058-00
A10U1224	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A10U1225	156-0541-00			MICROCKT,DGTL:DUAL 2 TO 4 LINE DCDR/DEMUX	80009	156-0541-00
A10U1226	156-1539-00			MICROCKT,DGTL:NMOS,6522,I/D PORT W/TIMER	34576	R6522AP
A10U1227	156-0696-00			MICROCKT,DGTL:QUAD CMPLM-OUTPUT & NAND	01295	SN4265N
A10U1228	156-0396-00			MICROCKT,DGTL:TTL,QUAD 3-STATE BFR74126	18324	N74126(N OR F)
A10U1231	136-0755-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
A10U1231	160-7043-00			IC,MEMORY:CMOS,EPROM;8K X 8,PRGM 156-2858-00,GPIB CONTROL LOWER BOARD;27V64,DIP28.6	80009	160-7043-00
A10U1236	156-0804-00			MICROCKT,DGTL:QUADRUPLE S-R LATCH	04713	74LS279(N OR J)
A10Y1200	158-0256-00			XTAL UNIT,QTZ:4.000MHZ 0.0025% SER	59492	150-6070

A10U1231

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20	671-1288-00			CIRCUIT BD ASSY:MGPIB UPPER	80009	671-1288-00
A20C1100	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1101	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1102	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1103	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1104	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1105	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1107	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1108	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1109	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1110	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1111	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1112	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1113	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1114	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1115	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1116	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1117	281-0798-00			CAP,FXD,CER DI:51PF,1%,100V	04222	MA101A510GAA
A20C1118	290-0845-00			CAP,FXD,ELCTLT:330UF,+50-10%,25V	54473	ECE-A25V330L
A20C1119	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1120	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A20C1121	290-0283-00			CAP,FXD,ELCTLT:0.47UF,10%,35V	05397	T320A474K035AS
A20C1122	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A20C1123	290-0963-00			CAP,FXD,ELCTLT:220UF,+50-20%,25WVDC	80009	290-0963-00
A20C1124	290-0963-00			CAP,FXD,ELCTLT:220UF,+50-20%,25WVDC	80009	290-0963-00
A20C1125	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20C1126	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1127	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	SA105E104ZAA
A20C1128	290-0943-02			CAP,FXD,ELCTLT:47UF,20%,25V	55680	UVX1E470MAA1TD
A20C1130	290-0267-00			CAP,FXD,ELCTLT:1UF,20%,35V	05397	T320A105M035AS
A20CR1100	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1101	152-0141-02			SEMICOND DVC,DI:SW,SI,30V,150MA,30V,DO-35	03508	DA2527 (1N4152)
A20CR1102	152-0581-04			SEMICOND DVC,DI:RECT,SI,20V,1A,A59	04713	1N5817RL
A20CR1103	152-0585-00			SEMICOND DVC,DI:RECT,SI,200V,1A	14936	W02M-30
A20DS1100	150-1160-00			LT EMITTING DIO:GREEN	50434	QLMP 1587
A20DS1102	150-1244-00			LT EMMITING DIO:GREEN,3.0 L,W/STRAIN RELIEF	80009	150-1244-00
A20DS1103	150-1160-00			LT EMITTING DIO:GREEN	50434	QLMP 1587
A20DS1104	150-1244-00			LT EMMITING DIO:GREEN,3.0 L,W/STRAIN RELIEF	80009	150-1244-00
A20F1101	159-0208-00			FUSE,WIRE LEAD:2A,125V,5 SEC	75915	255002
A20J1100	131-3147-00			CONN,RCPT,ELEC:HEADER,2 X 25,0.1 SPACING	53387	3596-6002
A20J1101	131-4114-00			CONN,RCPT,ELEC:HEADER,2 X 12,0.1 CTR	TK2098	3589-6002
A20J1102	131-3985-00			CONN,RCPT,ELEC:PNL,2 X 12,STR,0.085 SPACING	80009	131-3985-00
A20J1103	131-4529-00			CONN,RCPT,ELEC:HEADER,10 PIN	80009	131-4529-00
A20J1104	131-4368-00			JACK,POWER:CKT BD MOUNT,RT ANG	80009	131-4368-00
A20L1100	108-0975-00			COIL,RF:FIXED,520UH	80009	108-0975-00
A20L1101	108-0554-00			COIL,RF:FIXED,5UH,+/-20%	TK1345	108-0554-00
A20Q1102	151-0188-05			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-05
A20Q1103	151-0188-05			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-05
A20R1100	313-1331-00			RES,FXD,FILM:330 OHM,5%,0.2W	57668	TR20JE 330E
A20R1101	307-0595-00			RES NTWK,FXD,FI:7,5.6K OHM,2%,1.0W	11236	750-81-5.6K
A20R1102	313-1202-00			RES,FXD,FILM:2K OHM,5%,0.2W	57668	TR20JE02K0
A20R1103	313-1512-00			RES,FXD,FILM:5.1K OHM,5%,0.2W	57668	TR20JE 5K1

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20R1104	313-1202-00			RES,FXD,FILM:2K OHM,5%,0.2W	57668	TR20JE02K0
A20R1111	313-1202-00			RES,FXD,FILM:2K OHM,5%,0.2W	57668	TR20JE02K0
A20R1112	307-0541-00			RES NTWK,FXD,FI:(7)1K OHM,10%,1W	01121	108A102
A20R1113	313-1102-00			RES,FXD,FILM:1K OHM,5%,0.2W	57668	TR20JE01K0
A20R1114	313-1202-00			RES,FXD,FILM:2K OHM,5%,0.2W	57668	TR20JE02K0
A20R1115	313-1202-00			RES,FXD,FILM:2K OHM,5%,0.2W	57668	TR20JE02K0
A20R1116	313-1471-00			RES,FXD,FILM:470 OHM,5%,0.2W	57668	TR20JE 470E
A20R1117	313-1151-00			RES,FXD,FILM:150 OHM,5%,0.2W	57668	TR20JE150E
A20R1118	313-1102-00			RES,FXD,FILM:1K OHM,5%,0.2W	57668	TR20JE01K0
A20R1119	313-1151-00			RES,FXD,FILM:150 OHM,5%,0.2W	57668	TR20JE150E
A20R1120	313-1153-00			RES,FXD,FILM:15K,5%,0.2W	57668	TR20JE15K0
A20R1121	313-1393-00			RES,FXD,FILM:39K OHM,5%,0.2W	57668	TR20JE 39K
A20R1122	313-1331-00			RES,FXD,FILM:330 OHM,5%,0.2W	57668	TR20JE 330E
A20R1123	313-1105-00			RES,FXD,FILM:1M OHM,5%,0.2W	57668	TR20JE1M
A20R1124	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E
A20R1125	313-1104-00			RES,FXD,FILM:100K OHM,5%,0.2W	57668	TR20JE100K
A20R1126	313-1105-00			RES,FXD,FILM:1M OHM,5%,0.2W	57668	TR20JE1M
A20R1127	313-1103-00			RES,FXD,FILM:10K OHM,5%,0.2W	57668	TR20JE10K0
A20R1128	313-1203-00			RES,FXD,FILM:20K OHM,5%,0.2W	57668	TR20JE20K
A20R1131	313-1101-00			RES,FXD,FILM:100 OHM,5%,0.2W	57668	TR20JE100E
A20R1132	322-3193-00			RES,FXD,FILM:1K OHM,1%,0.2W,TC=T0	57668	CRB20 FXE 1K00
A20R1133	322-3237-00			RES,FXD,FILM:2.87K OHM,1%,0.2W,TC=T0	80009	322-3237-00
A20R1134	313-1100-00			RES,FXD,FILM:10 OHM,5%,0.2W	57668	TR20JE10E0
A20R1135	313-1270-00			RES,FXD,FILM:27 OHM 5%,0.2W	57668	TR20JT68 27E
A20R1136	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A20SW1100	260-2064-00			SWITCH,ROCKER:(6)SPST,125MA,30VDC	81073	76YYXXXS

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20SW1101	260-2443-00			SWITCH,PUSH:POWER,DPST,6A,250VAC	80009	260-2443-00
A20U1100	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A20U1101	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	80009	156-0956-00
A20U1102	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	80009	156-0956-00
A20U1103	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	80009	156-0956-00
A20U1104	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A20U1105	156-1205-00			MICROCKT,DGTL:NMOS,PERIPHERAL INTFC ADPTR	04713	MC68B21P OR L
A20U1106	156-0384-00			MICROCKT,DGTL:QUAD 2-INP NAND GATE	01295	SN74LS03 N OR J
A20U1107	160-7044-00			IC,MEMORY:CMOS,EPROM;8K X 8,PRGM 156-2858-0 0,GPIB CONTROL UPPER BOARD;27V64,DIP28.6	80009	160-7044-00
A20U1108	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A20U1109	156-1205-00			MICROCKT,DGTL:NMOS,PERIPHERAL INTFC ADPTR	04713	MC68B21P OR L
A20U1110	156-3592-00			MICROCKT,DGTL:HCMOS,3-LINE TO 8-LINE	80009	156-3592-00
A20U1111	156-3592-00			MICROCKT,DGTL:HCMOS,3-LINE TO 8-LINE	80009	156-3592-00
A20U1112	156-0144-00			MICROCKT,DGTL:3-INPUT NAND GATE	80009	156-0144-00
A20U1113	156-0144-00			MICROCKT,DGTL:3-INPUT NAND GATE	80009	156-0144-00
A20U1114	156-0481-00			MICROCKT,DGTL:TRIPLE 3-INP AND GATE	80009	156-0481-00
A20U1115	156-1373-00			MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A20U1116	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A20U1117	156-0387-00			MICROCKT,DGTL:DUAL J-K FLIP-FLOP	01295	SN74LS73 N OR J
A20U1118	156-0387-00			MICROCKT,DGTL:DUAL J-K FLIP-FLOP	01295	SN74LS73 N OR J
A20U1119	156-0789-00			MICROCKT,DGTL:8-BIT SR,PRL LOAD	01295	SN74LS165N
A20U1120	156-0789-00			MICROCKT,DGTL:8-BIT SR,PRL LOAD	01295	SN74LS165N
A20U1121	156-3213-00			MICROCKT,LINEAR:SWITCHING REGULATOR,5 PIN	80009	156-3213-00
A20U1122	156-0411-00			MICROCKT,LINEAR:SGL SPLY COMPARATOR	04713	LM339N
A20VR1100	152-0667-00			SEMICOND DVC,DI:ZEN,SI,3.0 V # 2% AT 2MA	04713	SZG30025RL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A20VR1100	156-0411-00			MICROCKT,LINEAR:SGL SPLY COMPARATOR	04713	LM339N

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A40	174-2257-00			CA ASSY,SP,ELEC:5,28 AWG,2.0 L	80009	174-2257-00
A55	120-1807-00			TRANSFORMER,PWR:16VA,WALL,WPWR PLUG	80009	120-1807-00
A55	174-2257-00			CA ASSY,SP,ELEC:5,28 AWG,2.0 L	80009	174-2257-00
W110	174-2000-00					
W101	174-2001-00					
W103	174-2002-00					

SECTION 8

Diagrams and Circuit Board Illustrations

Symbols

Graphics symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI/IEEE 91-1984. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

A slash before a signal name indicates that the signal performs its intended function when it is in the low state; for example, /IRQ.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc., are:

Y14.15-1966	Drafting Practices.
Y14.2M-1979	Line Conventions and Lettering.
ANSI/IEEE 280-1985	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standards Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical Components shown on the diagrams are in the following units unless noted otherwise:

Capacitors	Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors	Ohms (Ω).

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number.

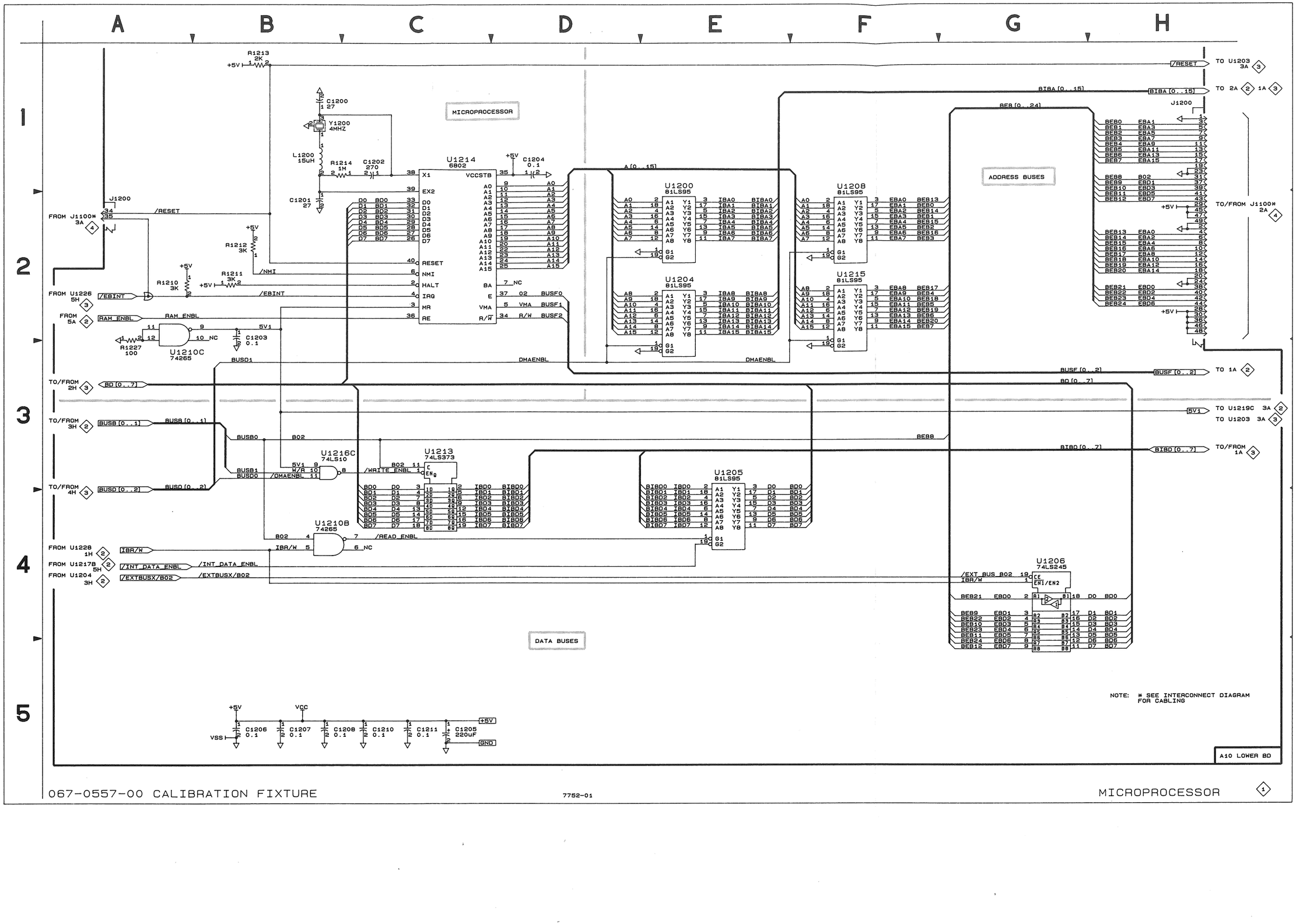
The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear near the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.

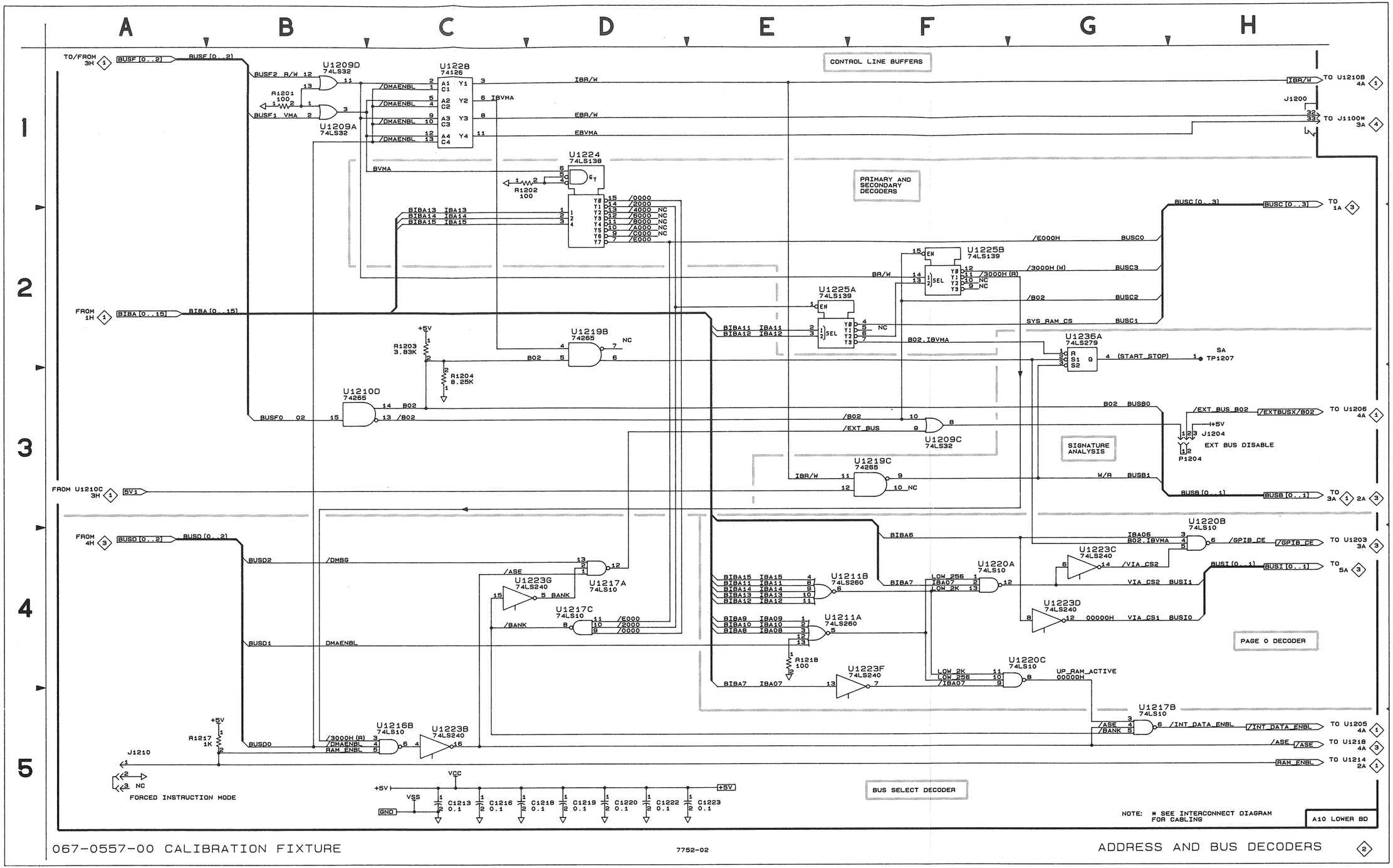
MICROPROCESSOR DIAGRAM 1

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1200	1B	3D	J1200B	2H	4D	U1200	2D	5B
C1201	2B	4D	J1200C	2H	4D	U1204	2D	5B
C1202	2C	4D	J1200D	2H	4D	U1205	3E	1A
C1203	3B	4B	J1200E	2A	4D	U1206	4G	3D
C1204	2D	3C				U1208	2F	4C
C1205	5C	1C	L1200	1B	3D	U1210B	4B	1F
C1206	5B	4F				U1210C	2A	1F
C1207	5B	2G	R1210	2B	4B	U1213	3C	3A
C1208	5B	4G	R1211	2B	4B	U1214	2C	4C
C1210	5C	1F	R1212	2B	4B	U1215	2F	4D
C1211	5C	4A	R1213	1B	4C	U1216C	3B	1A
			R1214	2C	4D			
J1200A	1H	4D	R1227	3A	4B	Y1200	1B	3D

Partial A10 also shown on diagrams D2 and D3.


MICROPROCESSOR
ADDRESS BUSES
DATA BUSES
U1214 6802
U1200 81LS95
U1204 81LS95
U1208 81LS95
U1215 81LS95
U1205 81LS95
U1206 74LS245
U1213 74LS373
U1216C 74LS10
U1210B 74265
U1210C 74265
Y1200 4MHZ
L1200 15uH
R1213 2K
R1214 1M
C1200 27
C1201 27
C1202 270
C1204 0.1
R1212 3K
R1211 3K
R1210 3K
R1227 100
C1203 0.1
C1206 0.1
C1207 0.1
C1208 0.1
C1210 0.1
C1211 0.1
C1205 220uF
J1200
/RESET
/NMI
/EBINT
RAM_ENBL
BUSD1
DMAENBL
BUSB0
BUSB1
B02
/WRITE_ENBL
/DMAENBL
/READ_ENBL
IBA/W
/INT_DATA_ENBL
/EXTBUSX/B02
/EXT BUS B02
BIBA [0..15]
BIBD [0..7]
BUSF [0..2]
BD [0..7]
BUSB [0..1]
BUSD [0..2]
A [0..15]
BEB [0..24]
FROM J1100* 3A
FROM U1226 5H
FROM 5A
TO/FROM 2H
TO/FROM 3H
TO/FROM 4H
FROM U1228 1H
FROM U1217B 5H
FROM U1204 3H
TO U1203 3A
TO 2A
TO 1A
TO U1219C 3A
TO/FROM 1A
TO/FROM J1100* 2A
+5V
VCC
VSS
GND
NOTE: * SEE INTERCONNECT DIAGRAM FOR CABLING
A10 LOWER BD



067-0557-00 CALIBRATION FIXTURE

7752-02

ADDRESS AND BUS DECODERS

ADDRESS AND BUS DECODERS DIAGRAM 2

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1213	5C	2A	R1203	3C	1E	U1217C	4D	1B
C1216	5C	1A	R1204	3C	1E	U1219B	3D	2E
C1218	5C	4E	R1217	5B	1E	U1219C	3E	2E
C1219	5D	1E	R1218	4E	5B	U1220A	4F	3A
C1220	5D	3A				U1220B	3G	3A
C1222	5D	3E	TP1207	3G	1D	U1220C	4F	3A
C1223	5D	1D				U1223B	5C	1D
			U1209A	1B	2B	U1223C	4F	1D
J1200D	1H	4D	U1209C	3F	2B	U1223D	4F	1D
J1204	3G	2B	U1209D	1B	2B	U1223F	4E	1D
J1210	5A	1F	U1210D	3B	1F	U1223G	4C	1D
			U1211A	4E	5A	U1224	1D	4A
P1204	3G	2B	U1211B	4E	5A	U1225A	2E	2E
P1210	5A	1F	U1216B	5C	1A	U1225B	2F	2E
			U1217A	4D	1B	U1228	1C	5A
R1201	1B	2B	U1217B	5G	1B	U1236A	3F	2C
R1202	1C	4A						

Partial A10 also shown on diagrams D1 and D3.

INTERNAL MEMORY AND I/O CONTROL DIAGRAM 3

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1224	2F	3A	P1208	3F	4G	U1209B	3D	2B
C1225	2F	2D	P1209	3F	4E	U1216A	2C	1A
C1228	2F	5A				U1218	3G	4E
C1230	2G	2D	R1200	2F	4E	U1219D	2B	2E
			R1208	4D	1C	U1222	1C	3E
DS1200	4F	1D	R1215	2B	2A	U1223A	4E	1D
DS1201	5F	1D	R1216	4A	2B	U1223E	5E	1D
DS1202	3G	1B	R1219	1C	4F	U1226	4D	2C
			R1220	4G	1C	U1227A	4C	2B
J1200A	1H	4D	R1221	4G	1C	U1227B	2C	2B
J1200B	3H	4D	R1228	4F	2E	U1227C	1G	2B
J1200C	4A	4D	R1229	5F	2D	U1227D	3G	2B
J1201A	2H	5E				U1231	1D	3B
J1201B	2H	5E	U1201	2E	4F	U1236B	4D	2C
J1208	3F	4G	U1202	3E	4F	U1236C	4G	2C
J1209	3F	4E	U1203	2D	3F	U1236D	1F	2C
			U1207	1E	2E			

Partial A10 also shown on diagrams D1 and D2.

A B C D E F G H

1 2 3 4 5

SYSTEM RAM

SYSTEM ROM

CIRCUIT SELECT LATCH

GPIB CONTROL

VERSATILE INTERFACE ADAPTER

SERVICE DISPLAY

ADDRESS/ SERVICE SWITCH REGISTER

A10 LOWER BD

U1222 6116

U1231 2764

U1207 74LS377

U1236D 74LS279

U1227C 74265

U1219D 74265

U1216A 74LS10

U1227B 74265

U1203 9914

U1201 75160A

U1209B 74LS32

U1202 75161A

U1218 81LS95

U1227D 74265

DS1202 TIL311

U1236B 74LS279

U1227A 74265

U1226 SY6522

U1223A 74LS240

U1223E 74LS240

U1236C 74LS279

DS1200 ADDRESSED

DS1201 ERROR

R1200 9x4.7K

R1219 10K

R1215 1K

R1216 1K

R1208 2.7K

R1220 820

R1221 820

R1228 220

R1229 220

C1224 0.1

C1225 0.1

C1228 0.1

C1230 0.1

J1200

J1201

J1208

J1209

P1208

P1209

TO/FROM 1H BIBA[0..15]

TO/FROM 3H BIBD[0..7]

TO/FROM 2H BUSC[0..3]

FROM 3H BUSB[0..1]

FROM U1220B 4H /GPIB CE

FROM U1228 1H IBR/W

FROM U1210C 3H 5V1

FROM A1213 1H /RESET

FROM U1223B 5H /ASE

FROM J1100M 3A

FROM 4H BUSI[0..1]

BUSC1 SYS RAM CS

BUSC2 /B02

BUSC3 /3000H (W)

BUSC0 /E000H

/ROMDIS

BUSB1

BUSB0

W/R

/WE

B02

/GPIB CE

IBR/W

5V1

/RESET

/ASE

/DMAENBL

BUSI1 VIA CS2

BUSI0 VIA CS1

CSEL 1

BFR TRIG

/GPIB INT

/VIA INT

/EBINT

DMAENBL BUSD1

/DMBG BUSD2

BUSD0

PA[0..3]

BGPIB[0..21]

BD[0..7]

BUSD[0..2]

TO J1100M 2A

TO/FROM J1101M 5A

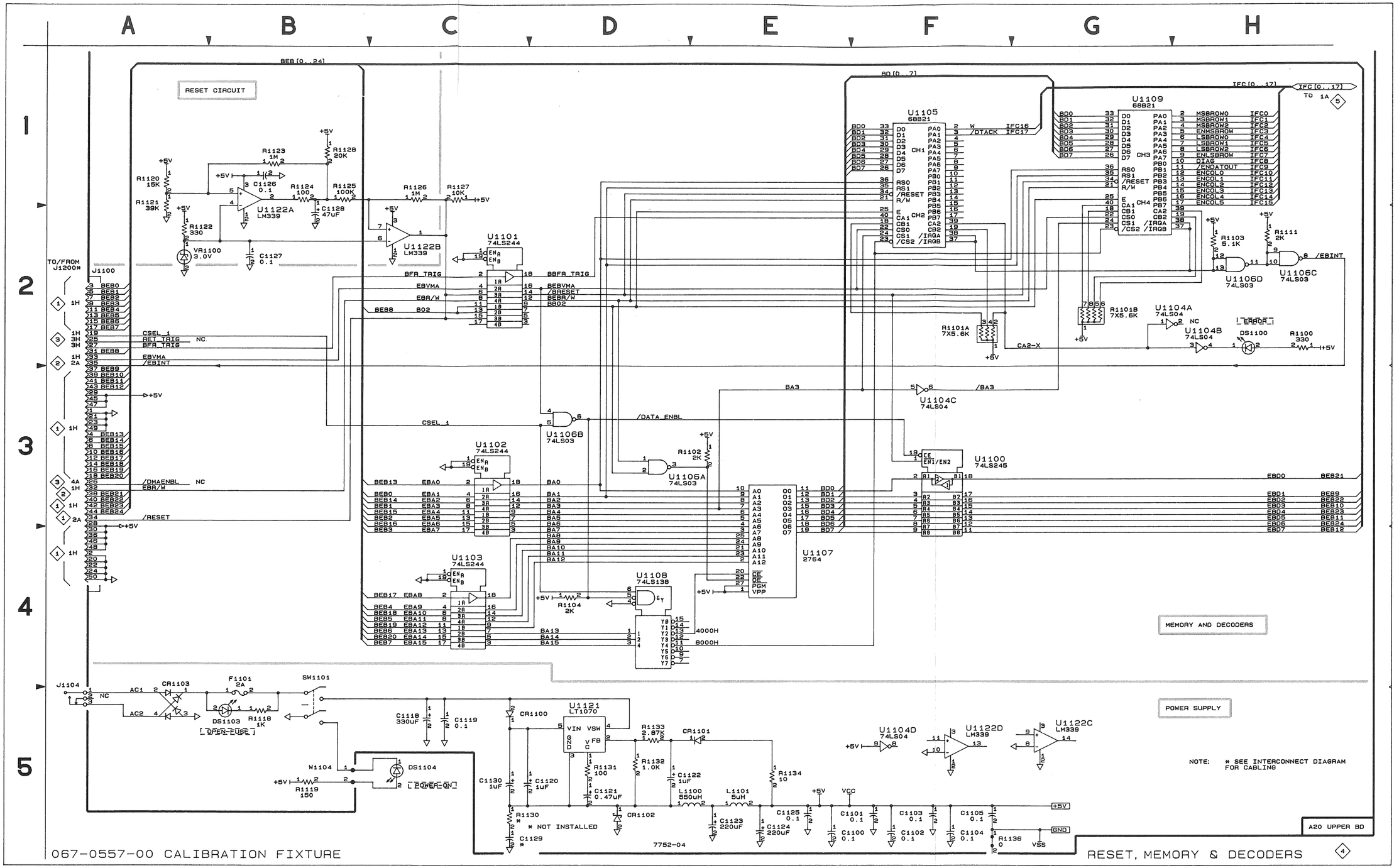
TO 3A

TO U1214 2A

067-0557-00 CALIBRATION FIXTURE

7752-03

INTERNAL MEMORY AND I/O CONTROL


RESET CIRCUIT
MEMORY AND DECODERS
POWER SUPPLY
A20 UPPER BD
RESET, MEMORY & DECODERS
067-0557-00 CALIBRATION FIXTURE
NOTE: * SEE INTERCONNECT DIAGRAM FOR CABLING
* NOT INSTALLED
7752-04
U1122A LM339
U1122B LM339
U1101 74LS244
U1102 74LS244
U1103 74LS244
U1105 68B21
U1109 68B21
U1100 74LS245
U1106A 74LS03
U1106B 74LS03
U1106C 74LS03
U1106D 74LS03
U1104A 74LS04
U1104B 74LS04
U1104C 74LS04
U1104D 74LS04
U1107 2764
U1108 74LS138
U1121 LT1070
U1122C LM339
U1122D LM339
4000H
8000H
[OPEN-FUSE]
[POWER-ON]
[ERROR]

RESET, MEMORY, & DECODERS DIAGRAM 4

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1100	5E	3F	J1100A	2A	3G	R1133	5D	3C
C1101	5F	2E	J1100B	3A	3G	R1134	5E	3C
C1102	5F	1E	J1104	4A	5G	R1136	5G	1G
C1103	5F	2F						
C1104	5F	3D	L1100	5D	5B	SW1101	4B	5A
C1105	5G	3E	L1101	5E	4F			
C1118	4C	4C				U1100	3F	3F
C1119	5C	3B	R1100	2H	3C	U1101	2C	3E
C1120	5C	4B	R1101A	2F	5D	U1102	3C	1E
C1121	5D	5D	R1101B	2G	5D	U1103	4C	2F
C1122	5D	4D	R1102	3D	5F	U1104A	2G	4D
C1123	5D	5E	R1103	2G	4F	U1104B	2G	4D
C1124	5E	5E	R1104	4D	5F	U1104C	3F	4D
C1125	5E	4C	R1111	2H	5F	U1104D	5E	4D
C1126	1B	3A	R1118	4B	4B	U1105	1E	4E
C1127	2B	2A	R1119	5B	3B	U1106A	3D	5F
C1128	2B	3A	R1120	1A	3A	U1106B	3D	5F
C1129	5C	3B	R1121	2A	3A	U1106C	2H	5F
C1130	5C	5D	R1122	2A	3A	U1106D	2G	5F
			R1123	1B	4A	U1107	3E	1E
CR1100	4C	4A	R1124	2B	4A	U1108	4D	4G
CR1101	5D	4C	R1125	2B	4A	U1109	1G	2D
CR1102	5D	4A	R1126	2C	4A	U1121	5D	4C
CR1103	4A	4G	R1127	2C	4A	U1122A	2B	2A
			R1128	1B	4A	U1122B	2C	2A
DS1100	2G	3D	R1130	5C	3A	U1122C	5F	2A
DS1103	4B	4B	R1131	5D	4C	U1122D	5F	2A
DS1104	5C	3B	R1132	5D	3C			
						VR1100	2A	3A
F1101	4B	4B						

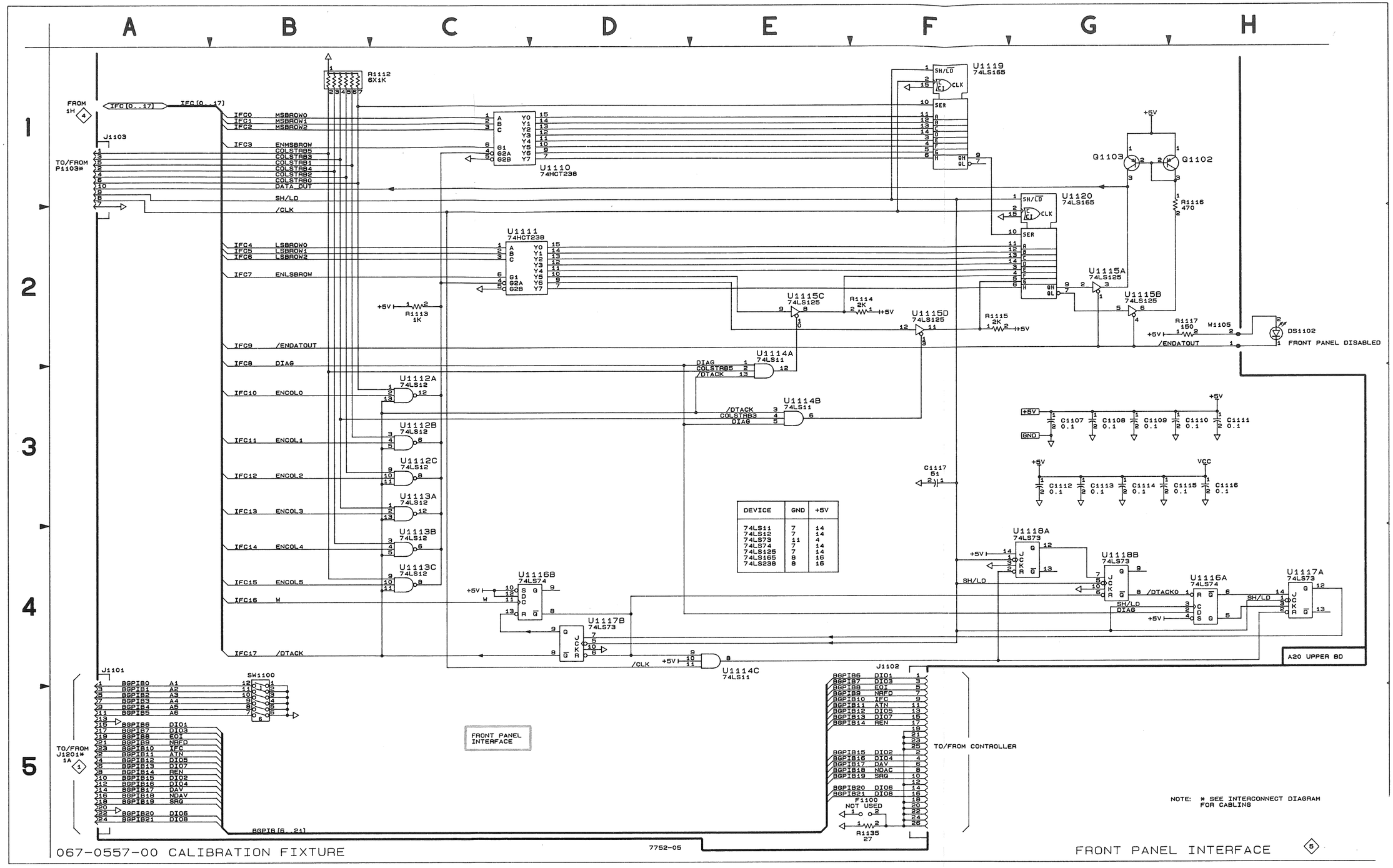
Partial A20 also shown on diagram D5.

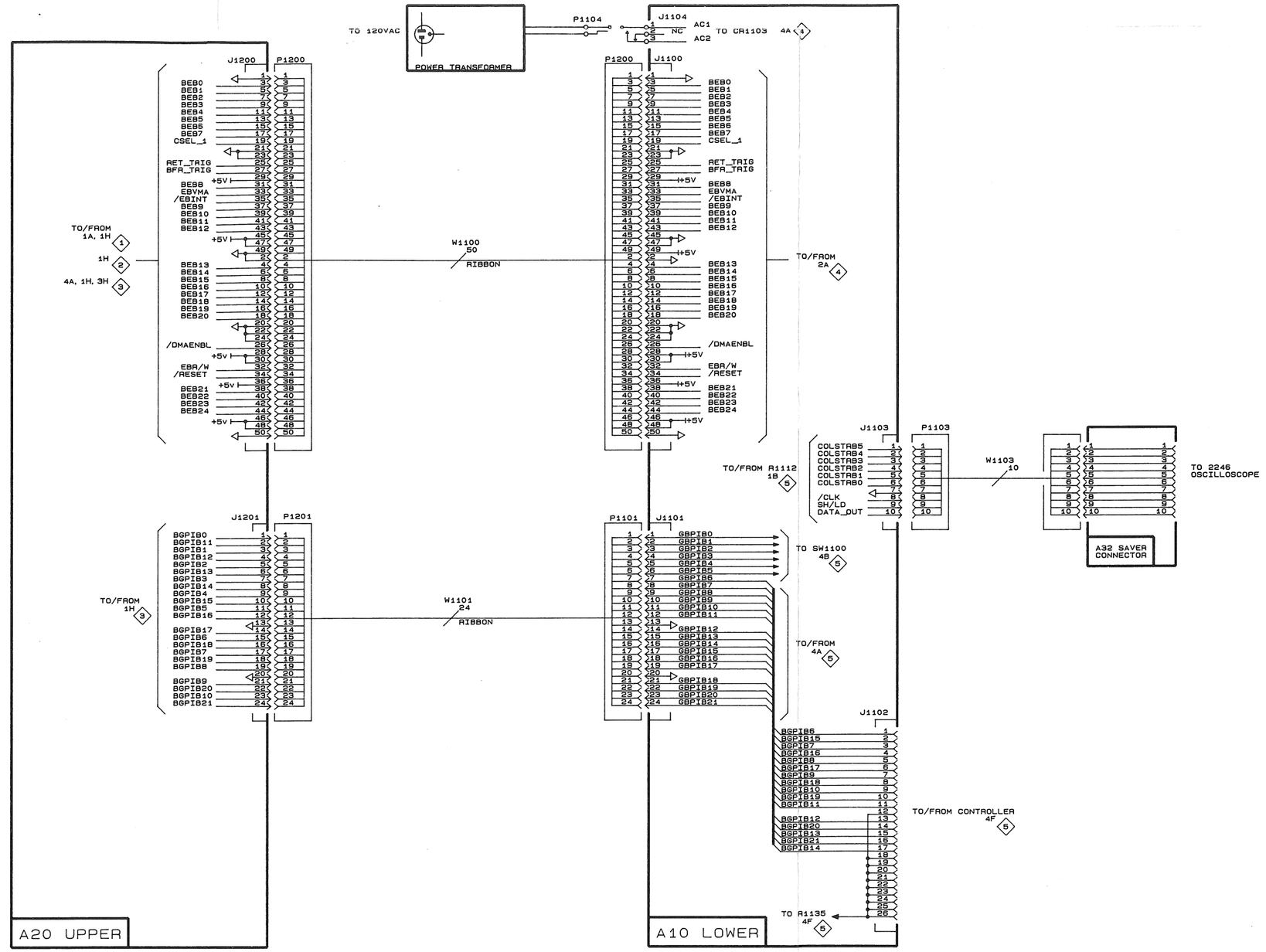
FRONT PANEL INTERFACE DIAGRAM 5

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1107	3F	1E	J1103	1A	1C	U1112C	3C	2D
C1108	3G	4F				U1113A	3C	4D
C1109	3G	1D	Q1102	1G	1A	U1113B	4C	4D
C1110	3G	1C	Q1103	1G	1A	U1113C	4C	4D
C1111	3G	1B				U1114A	3E	2A
C1112	3F	2C	R1112	1B	1C	U1114B	3E	2A
C1113	3G	3D	R1113	2C	1C	U1114C	4D	2A
C1114	3G	2A	R1114	2E	3A	U1115A	2G	2B
C1115	3G	2B	R1115	2F	2B	U1115B	2G	2B
C1116	3G	2C	R1116	2G	1A	U1115C	2E	2B
C1117	3F	2C	R1117	2G	2B	U1115D	2F	2B
			R1135	5E	4G	U1116A	4G	3C
DS1102	2H	1B				U1116B	4C	3C
			SW1100	4B	1H	U1117A	4H	3C
F1100	5E	2G				U1117B	4D	3C
			U1110	1C	2C	U1118A	4F	3B
J1101A	4A	3G	U1111	2C	2B	U1118B	4G	3B
J1101B	5A	3G	U1112A	3C	2D	U1119	1F	1D
J1102A	4F	3H	U1112B	3C	2D	U1120	2F	2C
J1102B	5F	3H						

Partial A20 also shown on diagram D4.

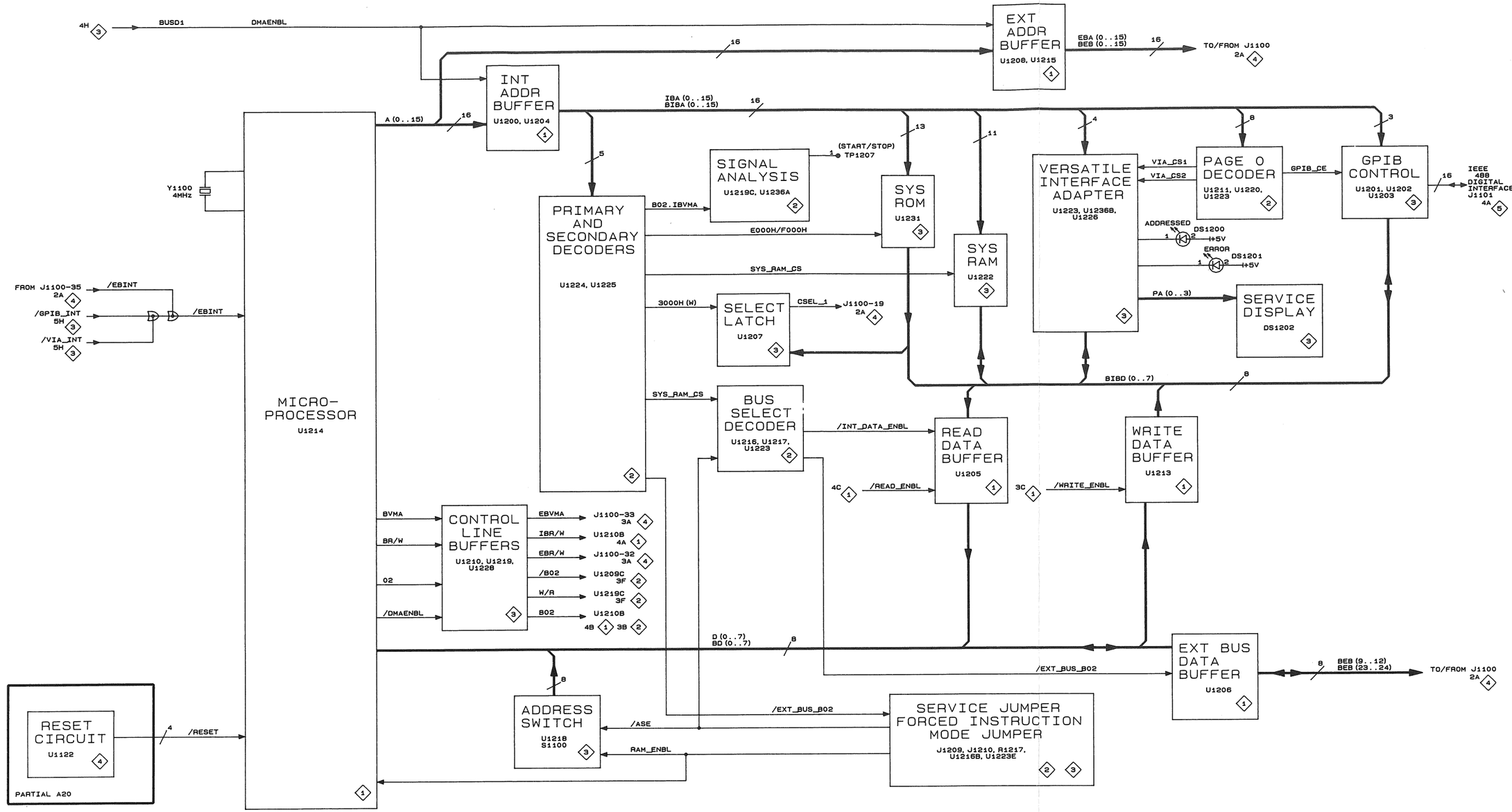

FROM 1H 4
IFC(0..17)
J1103
TO/FROM P1103*
IFC0 MSBROW0
IFC1 MSBROW1
IFC2 MSBROW2
IFC3 ENMSBROW
COLSTRB5
COLSTRB3
COLSTRB1
COLSTRB4
COLSTRB2
COLSTRB0
DATA_OUT
SH/LD
/CLK
IFC4 LSBROW0
IFC5 LSBROW1
IFC6 LSBROW2
IFC7 ENLSBROW
IFC9 /ENDATOUT
IFC8 DIAG
IFC10 ENCOL0
IFC11 ENCOL1
IFC12 ENCOL2
IFC13 ENCOL3
IFC14 ENCOL4
IFC15 ENCOL5
IFC16 W
IFC17 /DTACK
R1112 6X1K
U1110 74HCT238
U1111 74HCT238
R1113 1K
U1112A 74LS12
U1112B 74LS12
U1112C 74LS12
U1113A 74LS12
U1113B 74LS12
U1113C 74LS12
U1114A 74LS11
U1114B 74LS11
U1114C 74LS11
U1115C 74LS125
U1115D 74LS125
U1115A 74LS125
U1115B 74LS125
R1114 2K
R1115 2K
U1116B 74LS74
U1117B 74LS73
U1118A 74LS73
U1118B 74LS73
U1116A 74LS74
U1117A 74LS73
U1119 74LS165
U1120 74LS165
Q1103
Q1102
R1116 470
R1117 150
W1105
DS1102
FRONT PANEL DISABLED
/ENDATOUT
DIAG
COLSTRB5
/DTACK
/DTACK0
SH/LD
C1107 0.1
C1108 0.1
C1109 0.1
C1110 0.1
C1111 0.1
C1112 0.1
C1113 0.1
C1114 0.1
C1115 0.1
C1116 0.1
C1117 51
VCC
+5V
GND
A20 UPPER BD
J1101
SW1100
BGPIB0 A1
BGPIB1 A2
BGPIB2 A3
BGPIB3 A4
BGPIB4 A5
BGPIB5 A6
BGPIB6 DIO1
BGPIB7 DIO3
BGPIB8 EOI
BGPIB9 NRFD
BGPIB10 IFC
BGPIB11 ATN
BGPIB12 DIO5
BGPIB13 DIO7
BGPIB14 REN
BGPIB15 DIO2
BGPIB16 DIO4
BGPIB17 DAV
BGPIB18 NDAC
BGPIB19 SRQ
BGPIB20 DIO6
BGPIB21 DIO8
BGPIB(6..21)
TO/FROM J1201* 1A 1
FRONT PANEL INTERFACE
J1102
TO/FROM CONTROLLER
F1100 NOT USED
R1135 27
DEVICE | GND | +5V
74LS11 | 7 | 14
74LS12 | 7 | 14
74LS73 | 11 | 4
74LS74 | 7 | 14
74LS125 | 7 | 14
74LS165 | 8 | 16
74LS238 | 8 | 16
NOTE: * SEE INTERCONNECT DIAGRAM FOR CABLING
7752-05
067-0557-00 CALIBRATION FIXTURE
FRONT PANEL INTERFACE 5



067-0557-00 CALIBRATION FIXTURE

7752-06

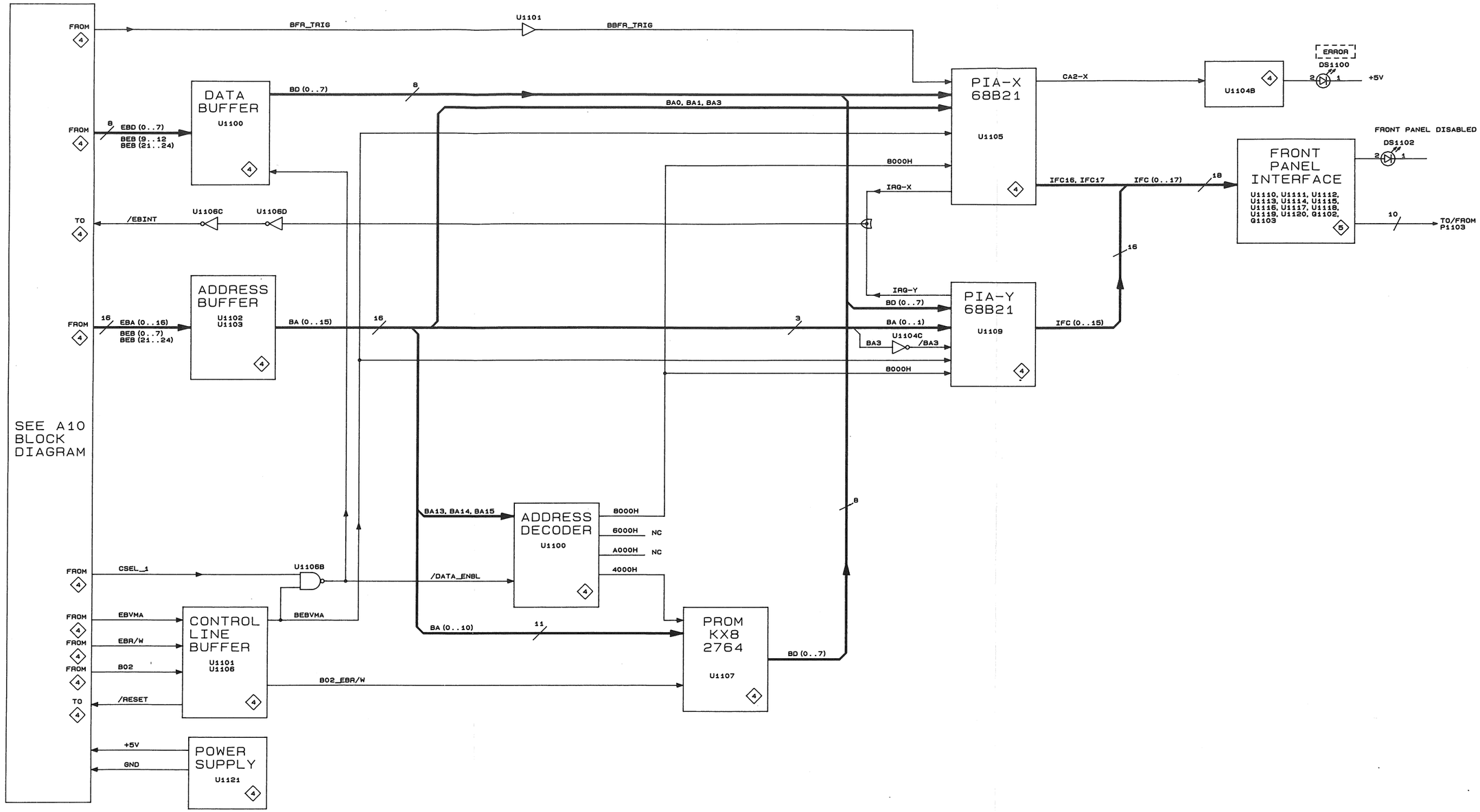
INTERCONNECT DIAGRAM 6



067-0557-00 CALIBRATION FIXTURE

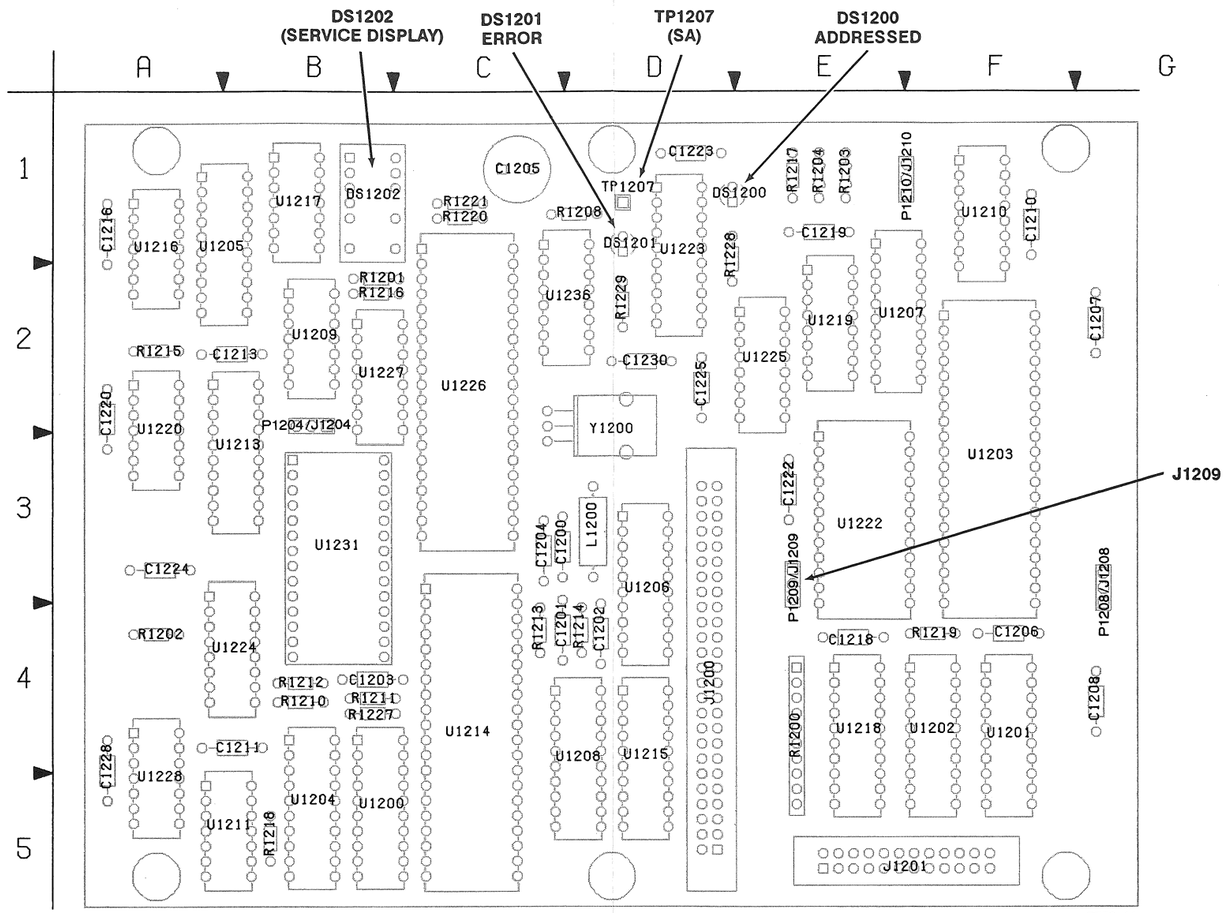
7752-08

A10 BLOCK DIAGRAM


SEE A10 BLOCK DIAGRAM
FROM 4
BFR_TRIG
U1101
BBFR_TRIG
DATA BUFFER U1100
BD (0..7)
8
BA0, BA1, BA3
EBD (0..7)
BEB (9..12 BEB (21..24)
PIA-X 68B21 U1105
CA2-X
U1104B
ERROR
DS1100
+5V
B000H
IRQ-X
IFC16, IFC17
IFC (0..17)
18
FRONT PANEL INTERFACE
U1110, U1111, U1112, U1113, U1114, U1115, U1116, U1117, U1118, U1119, U1120, G1102, G1103
FRONT PANEL DISABLED
DS1102
TO 4
/EBINT
U1106C
U1106D
10
TO/FROM P1103
16
IRQ-Y
BD (0..7)
PIA-Y 68B21 U1109
IFC (0..15)
ADDRESS BUFFER U1102 U1103
EBA (0..16)
BEB (0..7) BEB (21..24)
BA (0..15)
BA (0..1)
BA3
U1104C
/BA3
3
B000H
BA13, BA14, BA15
ADDRESS DECODER U1100
B000H
6000H NC
A000H NC
4000H
CSEL_1
U1106B
/DATA_ENBL
EBVMA
EBR/W
B02
/RESET
CONTROL LINE BUFFER U1101 U1106
BEBVMA
B02_EBR/W
BA (0..10)
11
PROM KX8 2764 U1107
BD (0..7)
+5V
GND
POWER SUPPLY U1121

A10—LOWER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1200	1			U1203	3
C1201	1	L1200	1	U1204	1
C1202	1			U1205	1
C1203	1	P1204	2	U1206	1
C1204	1	P1208	3	U1207	3
C1205	1	P1209	3	U1208	1
C1206	1	P1210	2	U1209	2
C1207	1			U1209	3
C1208	1	R1200	3	U1210	1
C1210	1	R1201	2	U1210	2
C1211	1	R1202	2	U1211	2
C1213	2	R1203	2	U1213	1
C1216	2	R1204	2	U1214	1
C1218	2	R1208	3	U1215	1
C1219	2	R1210	1	U1216	1
C1220	2	R1211	1	U1216	2
C1222	2	R1212	1	U1216	3
C1223	2	R1213	1	U1217	2
C1224	3	R1214	1	U1218	3
C1225	3	R1215	3	U1219	2
C1228	3	R1216	3	U1219	3
C1230	3	R1217	2	U1220	2
		R1218	2	U1222	3
DS1200	3	R1219	3	U1223	2
DS1201	3	R1220	3	U1223	3
DS1202	3	R1221	3	U1224	2
		R1227	1	U1225	2
J1200	1	R1228	3	U1226	3
J1200	2	R1229	3	U1227	3
J1200	3			U1228	2
J1201	3	TP1207	2	U1231	3
J1204	2			U1236	2
J1208	3	U1200	1	U1236	3
J1209	3	U1201	3		
J1210	2	U1202	3	Y1200	1



7752-11

Figure 8-1. A10—Lower board.

A20—UPPER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1100	4	DS1104	4	R1128	4
C1101	4			R1130	4
C1102	4	F1100	5	R1131	4
C1103	4	F1101	4	R1132	4
C1104	4			R1133	4
C1105	4	J1100	4	R1134	4
C1107	5	J1101	5	R1135	5
C1108	5	J1102	5	R1136	4
C1109	5	J1103	5		
C1110	5	J1104	4	SW1100	5
C1111	5			SW1101	4
C1112	5	L1100	4		
C1113	5	L1101	4	U1100	4
C1114	5			U1101	4
C1115	5	Q1102	5	U1102	4
C1116	5	Q1103	5	U1103	4
C1117	5			U1104	4
C1118	4	R1100	4	U1105	4
C1119	4	R1101	4	U1106	4
C1120	4	R1102	4	U1107	4
C1121	4	R1103	4	U1108	4
C1122	4	R1104	4	U1109	4
C1123	4	R1111	4	U1110	5
C1124	4	R1112	5	U1111	5
C1125	4	R1113	5	U1112	5
C1126	4	R1114	5	U1113	5
C1127	4	R1115	5	U1114	5
C1128	4	R1116	5	U1115	5
C1129	4	R1117	5	U1116	5
C1130	4	R1118	4	U1117	5
		R1119	4	U1118	5
CR1100	4	R1120	4	U1119	5
CR1101	4	R1121	4	U1120	5
CR1102	4	R1122	4	U1121	4
CR1103	4	R1123	4	U1122	4
		R1124	4		
DS1100	4	R1125	4	VR1100	4
DS1102	5	R1126	4		
DS1103	4	R1127	4		

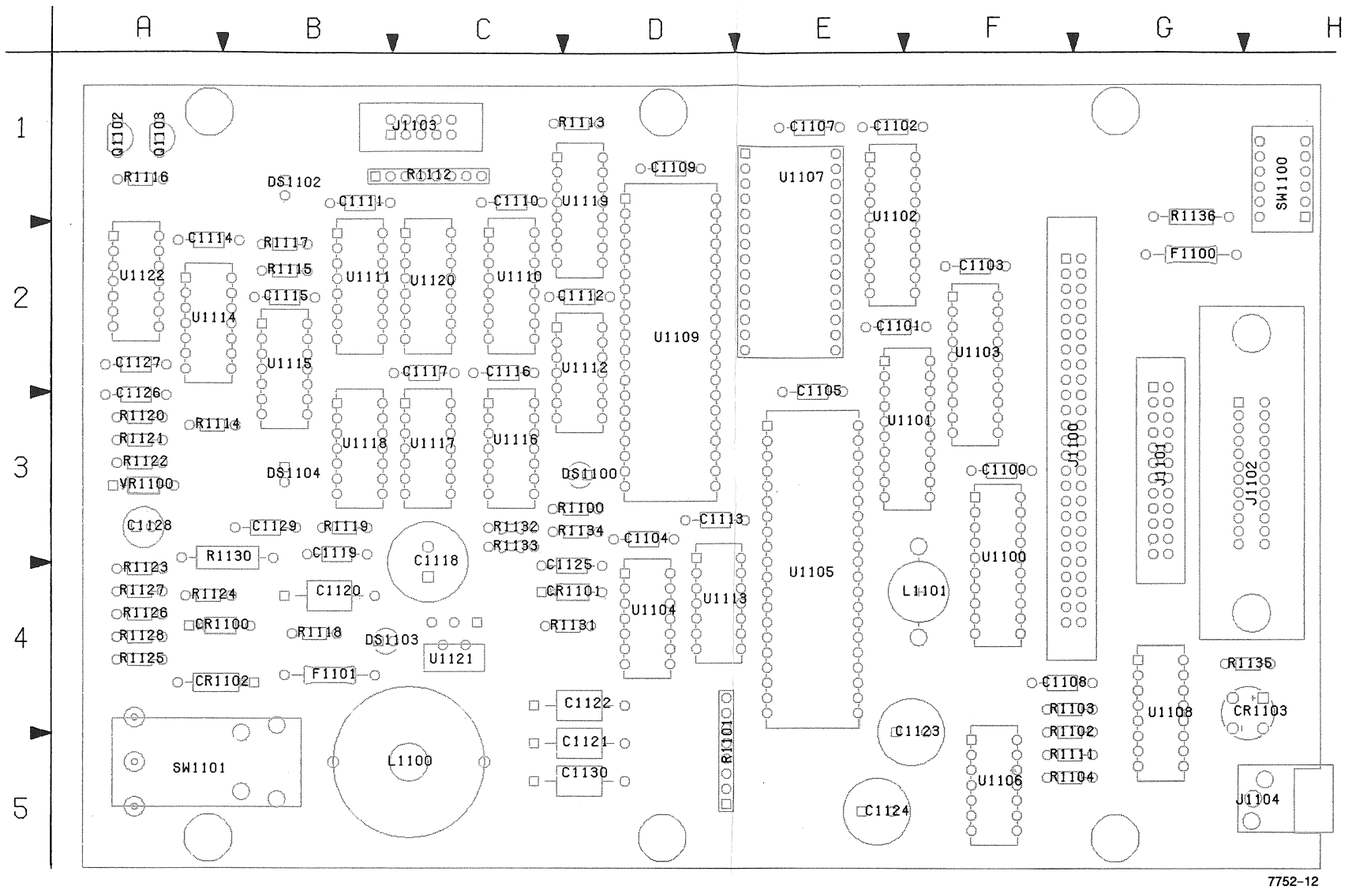


Figure 8-2. A20—Upper board.

SECTION 9

Replaceable Mechanical Parts

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

When ordering parts, include the following information in your order: part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Item Name

In the parts list, an item name is separated from the description by a colon(:). Because of space limitations, an item name may sometimes appear as incomplete. For further item name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

Figure and Index Numbers

Items in this section are referenced by figure and index numbers to the illustrations.

Indentation System

The mechanical parts list is indented to indicate item relationships. Following is an example of the indentations system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or component
Attaching parts for assembly and/or component

END ATTACHING PARTS

Detail part of assembly and/or component
Attaching parts for detail part

END ATTACHING PARTS

Parts of detail part
Attaching parts for parts of detail part

END ATTACHING PARTS

Attaching parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation.

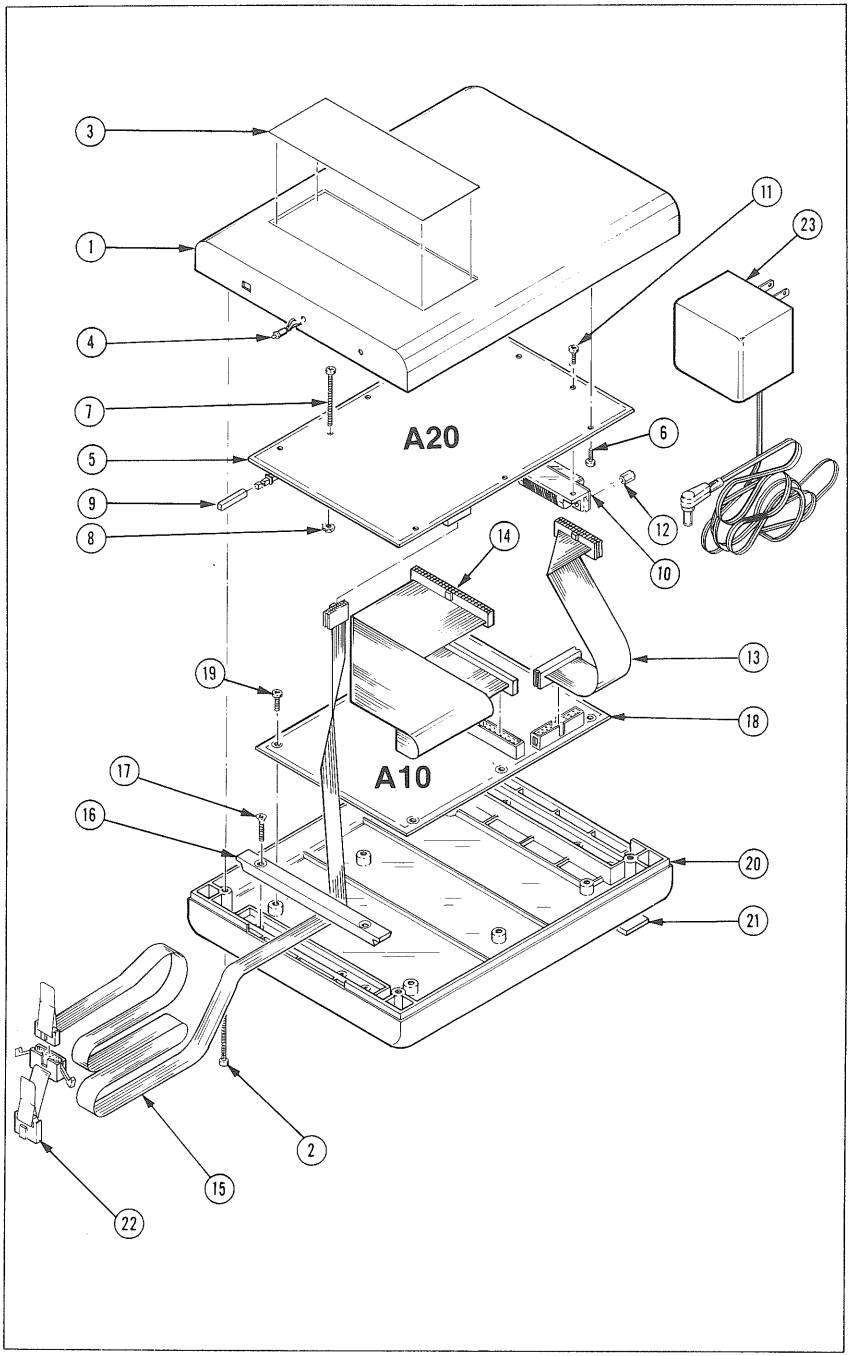
Attaching parts must be purchased separately, unless otherwise specified.

Abbreviations

Abbreviations conform to American National Standard Y1.1.

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	380-0687-08			1	HOUSING HALF:TOP	80009	380-0687-08
					ATTACHING PARTS		
-2	211-0712-00			4	SCR,ASSEM WSHR:6-32 X 1.25,PNH,STL,TORX	01536	ORDER BY DESCR
					END ATTACHING PARTS		
-3	334-7803-00			1	MARKER,IDENT:MKD CALIBRATION FIXTURE	80009	334-7803-00
-4	----- -----			1	LED,GREEN;(SEE DS1102 REPL)		
-5	----- -----			1	CKT BD ASSY;MGPIB,UPPER(SEE A20 REPL)		
					ATTACHING PARTS		
-6	211-0722-00			6	SCREW,MACHINE:6-32 X 0.25,PNH,STL	80009	211-0722-00
					END ATTACHING PARTS		
					CKT BD ASSY INCLUDES		
-7	211-0333-00			1	.SCR,ASSEM WSHR:4-40 X 1.0,PNH,STL,TORX T9	TK0858	ORDER BY DESCR
-8	210-0586-00			1	.NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-9	366-1512-04			1	.PUSH BUTTON:IVORY GY,0.18 X SQ X 0.83	80009	366-1512-04
-10	----- -----			1	CONNECTOR:(SEE J1102 REPL)		
					ATTACHING PARTS		
-11	211-0378-00			2	.SCR,ASSEM WSHR:4-40 X 0.375.PNH,STL,CD PL	80009	211-0378-00
-12	211-0722-00			6	.SCREW,MACHINE:6-32 X 0.25,PNH,STL	80009	211-0722-00
					END ATTACHING PARTS		
-13	----- -----			1	CABLE ASSY:(SEE P1101 REPL)		
-14	----- -----			1	CABLE ASSY:(SEE P1100 REPL)		
-15	----- -----			1	CABLE ASSY:(SEE P1103 REPL)		
-16	343-1006-00			1	CLAMP,CABLE:4.9 L,ALUMINUM	80009	343-1006-00
					ATTACHING PARTS		
-17	211-0522-00			2	SCREW,MACHINE:6-32 X 0.625,FLH,100 DEG,STL	93907	ORDER BY DESCR
					END ATTACHING PARTS		
-18	----- -----			1	CKT BD ASSY;MGPIB,LOWER(SEE A10 REPL)		
-19	211-0722-00			6	SCREW,MACHINE:6-32 X 0.25,PNH,STL	80009	211-0722-00
					END ATTACHING PARTS		
-20	380-0688-00			1	CABINET,BOTTOM:	80009	380-0688-00
-21	348-0596-00			4	PAD,CAB.FOOT:0.69 X 0.255 X 0.06,PU	80009	348-0596-00

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-22	----- -----			1	CABLE ASSY;(SEE A40 REPL)		
					STANDARD ACCESSORIES		
	----- -----			1	CABLE ASSY;(SEE A55 REPL)		
-23	----- -----			1	TRANSFORMER;(SEE A55 REPL)		
	070-7752-00			1	MANUAL,TECH:INSTR,067-0557-00	80009	070-7752-00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MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 01-11-90 Change Reference: C1/1190

Product: 067-0557-00 Calibration Fixture Manual Part Number: 070-7752-00

DESCRIPTION Product Group

EFFECTIVE ALL INSTRUMENTS

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A20DS1102	150-1054-00	LED GREEN, 6"L, striped 0.5", 30mA, 120mW
A20DS1104	150-1054-00	LED GREEN, 6"L, striped 0.5", 30mA, 120mW