Tektronix®

PM111

PERSONALITY MODULE FOR 6809 MICROPROCESSOR

INSTRUCTION MANUAL

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PM111

PERSONALITY MODULE FOR 6809 MICROPROCESSOR

INSTRUCTION MANUAL

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SERVICE INFORMATION

WARNING

The following servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in operating instructions unless you are qualified to do so.

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OPERATOR'S SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and service personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or to other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found.

Symbols As Marked on Equipment

Attention - refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

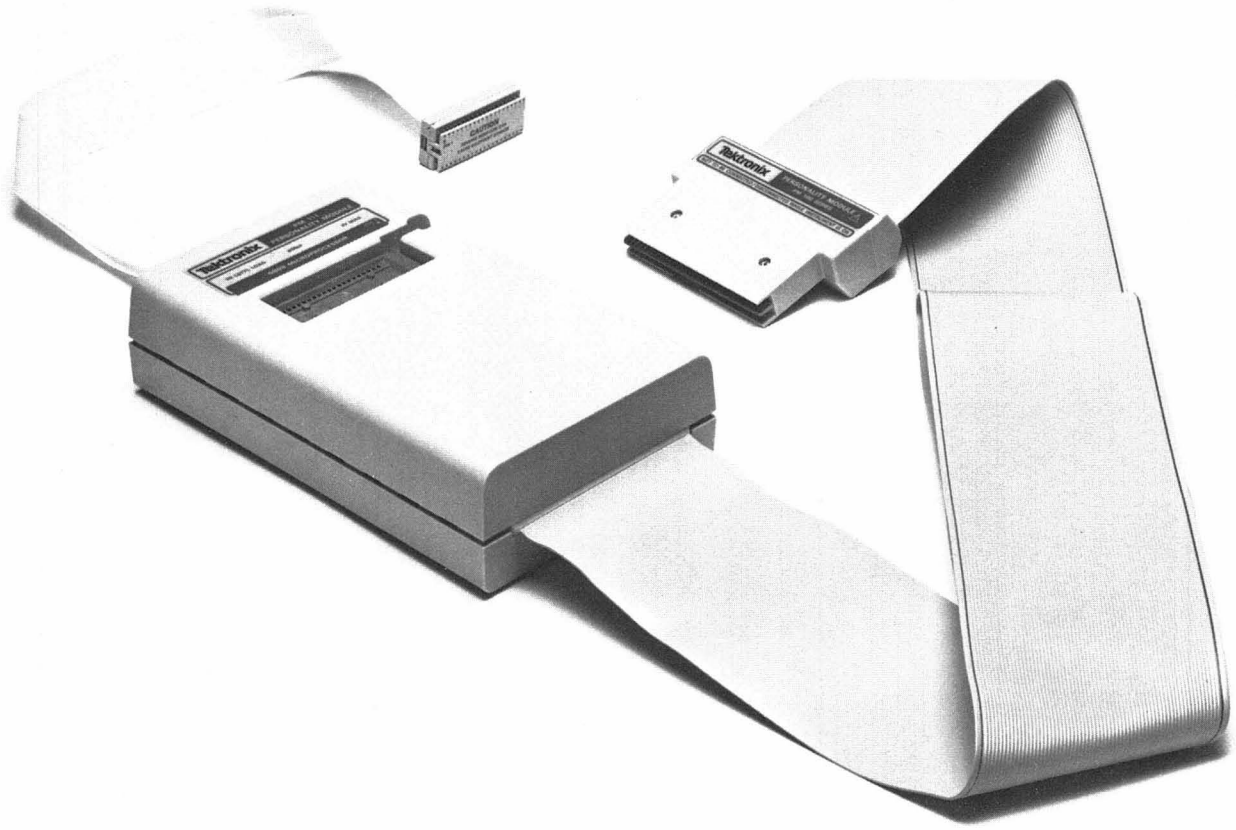
Upon loss of the protective-ground connection, all accesible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Do Not Operate in Explosive Atmosperes

To avoid explosion, do not operate this product in an explosive atmospere unless it has been certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.



4155-01

The PM 111 Personality Module for 6809/6809E microprocessors.

INTRODUCTION

OVERVIEW

The PM 111 Personality Module personalizes the logic analyzer for use with MC6809/MC6809E microprocessors. The personality module contains firmware which modifies the display and diagnostics of the logic analyzer for use with the microprocessor. This firmware also allows the logic analyzer to disassemble the information it receives into the mnemonics of that microprocessor.

The microprocessor is removed from the system under test (SUT) and installed in the zero insertion force (ZIF) socket of the PM 111. The microprocessor plug from the PM 111 is then plugged into the socket of the SUT. As the personality module passively monitors the system under test, it does not interfere with the normal operation of the microprocessor. It does, however, collect and transfer data to the logic analyzer in a standard format that the logic analyzer can interpret.

Physically, the PM 111 Personality Module consists of a pod containing three circuit boards. A four foot ribbon cable with a 64-pin connector serves as the interface to the logic analyzer, while a pair of 26 line ribbon cables with a 40-pin plug interfaces the PM 111 to the system under test. A ZIF socket, located on the top side of the module, receives the microprocessor itself. A 40-pin test socket, located on the bottom of the module, receives the PM 111 40-pin plug during the self-test mode of operation.

ABOUT THIS MANUAL

This manual describes the operation and servicing of the PM 111 Personality Module. The operator's portion of this manual provides an overview of the personality module, connection and operating instructions, and specifications associated with the personality module. The service portion of the manual is found after the colored divider page. It contains detailed circuit descriptions, schematics, performance check procedures, maintenance and troubleshooting information, electrical and mechanical replaceable parts lists, and a signal glossary. Refer to the Table of Contents for the specific locations of information.

To better understand the operation of the PM 111 Personality Module, the operator should be familiar with the operation of the Motorola MC6809 or MC6809E series of microprocessors. The reader should be familiar with the following reference material.

"MC6809 Advance Information", Motorola Inc., 1980

"MC6809E Advance Information", Motorola Inc., 1980

"MC6809-MC6809E Programming Manual", Motorola Inc., 1981

7D02 Logic Analyzer Service Manual, Tektronix Inc., P/N 070-2919-00

7D02 Logic Analyzer Operator's Manual, Tektronix Inc., P/N 070-2918-00

The PM 111 Personality Module supports the following microprocessors:

MC6809 (1.0 MHz)

MC68A09 (1.5 MHz)

MC68B09 (2.0 MHz)

With minimal configuration changes, the PM 111 will also support the following microprocessors:

MC6809E (1.0 MHz)

MC68A09E (1.5 MHz)

MC68B09E (2.0 MHz)

CONVENTIONS USED IN THIS MANUAL

The following provides a list of the conventions used throughout this manual.

- Whenever a reference is made to the PM 111, the information should be considered true for all versions of the MC6809 and MC6809E microprocessors, unless otherwise noted. Special considerations of the 6809E series of microprocessors are referenced in the Table of Contents, located at the front of this manual.

- A bar ($\overline{\ }$) over a signal name, or a portion of a signal name in the schematics, indicates that the signal is active when in the low state. For example, $\overline{\text{HALT}}$ indicates that HALT is an active low signal. R/$\overline{\text{W}}$ indicates that 1=Read, 0=Write.

- An (H) or (L) following a signal name indicates that the signal is active in the high or low state. For example, LOOK(H) indicates that LOOK is an active high signal. SELP(L) indicates that SELP is an active low signal. The absence of an (L) after a signal name implies active high (H).

- A slash (/) before a signal name or portion of a signal name in the simulated screen displays, indicates that the signal name appears that way on the 7D02 screen. For example, R/W is the same as R/$\overline{\text{W}}$ for schematics and R/W(L) for the text.

- Component numbers are composed of an assembly number and a schematic circuit number. For example, A1U1031 indicates that component U1031 is located on assembly A1 (board 1) of the personality module.

- A convention of minimizing lengthy parts references is used in this this manual. For example, the reference A1U3045, A1U4045, and A1U5045 representing components on assembly A1 (board 1) may be referenced as A1U's 3045, 4045, and 5045.

- The following board-related terms should be considered synonymous:

  upper - top - Buffer Board - Assembly A1
  middle - Fetch Predictor Board - Assembly A2
  lower - bottom - Self-Test Board - Assembly A3

OPERATING THE PM 111 PERSONALITY MODULE

OVERVIEW

This section of the manual provides information concerning the operation of the PM 111 Personality Module.

MODES OF OPERATION

The PM 111 has two basic modes of operation. The first is the normal mode of operation where the personality module acts as a passive bus monitor, collecting data and then transferring it to the logic analyzer. The second is a self-test mode that is used to verify the correct operation of the personality module. Refer to the Theory of Operation and the Maintenance and Troubleshooting sections for more information.

CONNECTION INSTRUCTIONS

CONNECTING THE PM 111 TO THE LOGIC ANALYZER

CAUTION

Always be certain to turn OFF the mainframe (logic analyzer) power before connecting or disconnecting any personality module. Failure to take this precaution may result in permanent damage to the logic analyzer, the personality module, or the system under test.

Turn off the mainframe power and insert the ribbon cable connector labeled PERSONALITY MODULE - PM 100 SERIES into the receptacle on the logic analyzer labeled with the same name.

CONNECTING THE PM 111 TO THE 6809 SYSTEM UNDER TEST (SUT)

1. Turn off the power to the logic analyzer and the SUT.
2. Ground yourself to drain static electricity.

CAUTION

Always be certain to turn off the power to any instrument before removing the microprocessor and installing it in the zero insertion force (ZIF) socket of the personality module.

Static input protection has been provided on all zero insertion force (ZIF) socket pins except pin 7. This same protection exists on the 40-pin test socket except for pins 7, 38, and 39.

3. Remove the 6809 microprocessor from the SUT and install it in the ZIF socket of the personality module. If using the 6809E microprocessor, the microprocessor remains in the SUT (refer to the PM 111 connection to the 6809E system under test). Be sure to install it properly, keeping pin 1 of the microprocessor toward the lever of the ZIF socket.

4. Plug the personality module 40-pin plug into the SUT socket where the microprocessor was removed. Make certain that pin 1 of the 40-pin plug goes to pin 1 of the SUT socket. Pin 1 of the 40-pin plug is marked with a notch and an arrow.

5. Turn on the power to the logic analyzer and the SUT, and reset the SUT.

CONNECTING THE PM 111 TO THE 6809E SYSTEM UNDER TEST

Six pins on the 6809E series differ from the 6809. In order to accomodate these changes, pins 38 and 39 of the microprocessor must be disconnected from the PM 111. The recommended procedure is as follows:

1. Clip pins 38 and 39 off a 40-pin dip socket (Tektronix P/N 136-0623-00).

2. Insert this socket into a female adapter (Tektronix P/N 380-0647-00).

3. Connect the female adapter to the 10 cm 40-pin low profile dip clip adapter (Tektronix P/N 015-0339-00).

4. Clip the low profile dip clip over the 6809E (the 6809E remains installed in the system under test). Check to ensure that pin 1 of the dip clip is matched to pin 1 of the SUT.

POWER SOURCE

Since the PM 111 operates only as a part of the logic analyzer system, all operating voltages and currents are furnished by the logic analyzer to which the PM 111 is connected.

STORING THE PM 111 PERSONALITY MODULE

Keep the personality module in a clean area where the temperature remains between -62 and +85 degrees C. Care should be taken when flexing the PM 111 cables between -62 and -15 degrees C. Humidity should not exceed 95%, non-condensing. The personality module should not be taken above 50,000 feet.

PROGRAMMING THE 7D02

The following 7D02 screen displays contain elements inherent to only the PM 111 Personality Module. For additional information about signal lines, refer to the Theory of Operation section, the Signal Glossary section, and the Additional Information found at the end of this section.

THE WORD RECOGNIZER

When the PM 111 is attached to the logic analyzer, the 7D02 WD RECOGNIZER key will produce the following display. The address and data buses have their default radices of hex. The radices of these fields may be changed to octal or binary by use of the 7D02 FORMAT key. All other fields are permanently set to binary.

```
TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 FETCH1=X FETCH1+2=X R/W=X BA=X
1 INT=X INVAL.OP=X EXT.TRIG.IN=X
1 TIMING WR=X
1THEN DO
1
```

DATA Field

The 8-bit data bus, which defaults to hexadecimal radix values, may also be displayed in octal or binary. When the START key is pressed, the logic analyzer stores the information from the data bus. It is possible to setup the Word Recognizer to recognize a specified data bus value by entering a value in the DATA field and setting all other fields to "don't care" conditions.

ADDRESS Field

The 16-bit address bus, which defaults to hexadecimal values, may also be displayed in octal or binary. When the START key is pressed, the logic analyzer stores the information from the address bus. It is possible to set up the Word Recognizer to recognize a specified address bus value by entering a value in the ADDRESS field and setting all other fields to "don't care" conditions.

FETCH1 Field

The FETCH1 field uses a binary radix. FETCH1=1 only on Fetch-1 cycles. A Fetch-1 cycle is a cycle on which the first byte (opcode) of an instruction is read from memory for execution.

The FETCH1 line is the C1 control line IFC(L). The FETCH1 information is stored in the logic analyzer acquisition memory.

FETCH1+2 Field

The FETCH1+2 field uses a binary radix. FETCH1+2=1 on either a Fetch-1 cycle (see FETCH1) or a Fetch-2 cycle. When FETCH1=1, then FETCH1+2=1. On a "Page 2" or a "Page 3" instruction (i.e., one whose first byte is 10H or 11H, respectively) two bytes are required to uniquely identify the opcode. A Fetch-2 cycle is a cycle on which the second byte of a 2-byte opcode is read from memory for execution. A Fetch-2 cycle is also any cycle on which the postbyte of one of the following instructions is read: TFR, EXG, PSHS, PSHU, PULS, PULU, or any indexed instruction. An indexed Page 2 or Page 3 instruction will have two Fetch-2 cycles.

The FETCH1+2 line is the C2 control line IFC+IFC2(L). The FETCH2 information is stored in the logic analyzer acquisition memory.

R/W Field

The R/W (Read/Write) field uses the binary radix. R/W(L)=1 on memory reads and R/W(L)=0 on memory writes. The R/W(L) line will appear high (a Read) on any fetch cycle.

The R/W(L) line is the C0 control line. This is the 6809 R/W(L) line that is stored in the logic analyzer acquistion memory.

The following Table 2-1 describes the relationship between the C0, C1, and C2 control lines.

Table 2-1
CONTROL LINES C0, C1, AND C2

C2 FETCH1+2	C1 FETCH1	C0 R/W	CYCLE TYPE
0	0	0	MEMORY WRITE
0	0	1	MEMORY READ
0	1	X	ILLEGAL STATE
1	X	0	ILLEGAL STATE
1	0	1	FETCH-2
1	1	1	FETCH-1

BA Field

The BA (Bus Available) field uses the binary radix. BA=1 on Halt, Bus Grant, and SYNC Acknowledge cycles, as well as the "Dead" cycle preceding a bus exchange. BA=0 on all other cycles such as Normal (running), Interrupt Acknowledge, and Reset Acknowledge cycles.

NOTE

Under default clock qualification, BA will always be low (BA=0). A user wishing to see all values of BA will have to turn off the clock qualifier C8 (i.e., set C8=X).

The BA line is the C4 control line. This is the 6809 BA line. It is not stored in the logic analyzer acquisition memory.

INT Field

The INT (Interrupt Request) field uses the binary radix. The INT signal equals 1 whenever one or more of the 6809 interrupt lines NMI(L), IRQ(L), or FIRQ(L) is asserted.

The INT line is the C3 control line. This line is generated by the PM 111 hardware and is stored in the logic analyzer acquisition memory.

INVAL.OP Field

The INVAL.OP (Invalid Opcode) field uses the binary radix. An invalid opcode is defined as one of the following:

- A Fetch-1 on which the data bus does not contain a valid opcode.
- A Fetch-2 for a Page-2 or Page-3 instruction on which the data bus does not contain a valid second opcode byte.
- An invalid postbyte (Fetch-2) for an indexed instruction.

NOTE

An illegal opcode will unsynchronize the fetch predictor. Any acquisition done after an illegal opcode may contain mislabeled cycles. An Interrupt Acknowledge cycle will re-synchronize the fetch predictor.

The INVAL.OP line, IOCO(L), is the C5 control line. The C5 control line is not stored by the logic analyzer acquisition memory.

EXT.TRIG.IN Field

The EXT.TRIG.IN (External Trigger In) field uses the binary radix. This is the External Trigger In signal from the logic analyzer front panel BNC connector. The EXT.TRIG.IN signal is not stored by the logic analyzer acquisition memory.

TIMING WR Field

The TIMING WR field will only be found in the Word Recognizer if the Timing Option (Option 02) is installed in the 7D02.

CLOCK QUALIFICATION

When the TRIGGER key is pressed, the logic analyzer provides the user with the following screen display format.

```
1 TRIGGER  0-MAIN
1            0-MAIN
1            1-TIMING
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
```

The last menu is of specific interest to the PM 111 user. When the cursor is placed on the 0-STANDARD CLOCK QUAL. box, the following display appears:

```
1     0-STANDARD CLOCK QUAL.
1       0 STANDARD CLOCK QUAL.
1       1 USER CLOCK QUAL.
```

If the 1 USER CLOCK QUAL. element is selected, the following display will appear:

```
1     1-USER CLOCK QUAL.
1     1-FALLING EDGE OF CLOCK
1       0 RISING EDGE OF CLOCK
1       1 FALLING EDGE OF CLOCK
1     C9-C4 (ANDED CLOCKS)=X0X0XX
```

Notice the default values of 0 given to C8 and C6 in the ANDED CLOCKS field. This is the default clock qualification setup used by the PM 111. If all of the control lines are set to X's ("don't cares"), the 7D02 will use all E clock cycles but with the default clock qualification setup, the 7D02 clocks only when:

- Clock E (pin 34) is on the falling edge, and
- C8 (much like BA) is in the low state indicating the 6809 has control of the bus and is not in a DMA or Dead cycle, and
- C6 (VMA)(L) is in the low state indicating a valid address is present on the bus.

Refer to Figure 2-1 for an example of default state clock generation.

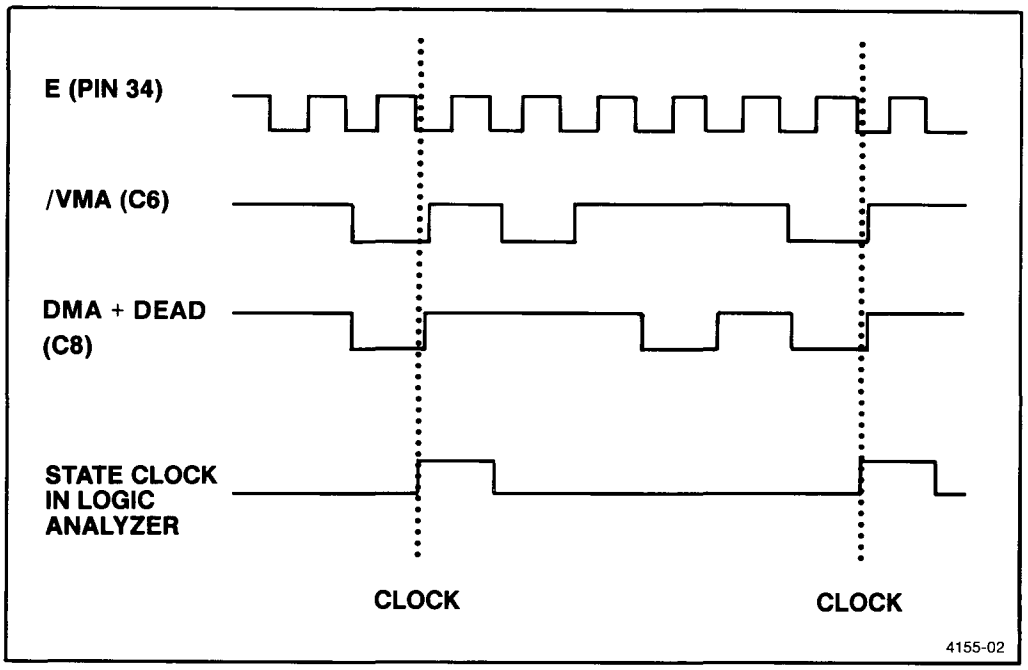


Figure 2-1. Default state clock generation.

The control lines C9-C4 are PM 111 control lines that may be used to re-define the state clock. The selected state is ANDED with the selected state of the clock E. If both states are true, a clock is generated.

The following example shows a redefined state clock:

```
1       C9-C4 (ANDED CLOCKS)=XXX0XX
```

where C8 has been changed to X (don't care). In this example, the clock qualifier has been set to qualify on all 6809 cycles, except invalid memory address cycles.

Another example shows further redefining:

```
1       C9-C4 (ANDED CLOCKS)=X1X0XX
```

where C8 has been changed to 1. In this example, the clock qualifier has been set to qualify only on valid DMA, Dead, Halt or Sync Acknowledge cycles.

NOTE

In most cases, the operator will not need to redefine the state clock. This procedure may produce unpredictable results.

If the TRIGGER-MAIN command is deleted from the program, the values last entered in the USER CLOCK QUAL. field will be retained. All fields will return to their power-up conditions when the logic analyzer is powered down, then powered back up again.

The following is a description of the clock qualification control lines:

C9

This qualifier is not used by the PM 111. C9 is always high and the user should never qualify on C9=0 (no clocks will be generated and the 7D02 will be effectively disabled).

C8

This line is essetially the same as the C4 control line (discussed later), except that (when C8=1) it qualifies all Dead cycles, not just the ones on which BA=1. The Dead cycles of the 6809/6809E usually come in pairs, one before and one after every bus exchange. The former comes when BA goes from 0 to 1, and the latter on the cycle after BA goes from 1 to 0. Refer to the MC6809 Advance Information for more explanation.

C7

C7=0 will qualify all cycles on which either the 6809 HALT(L) or DMA/BREQ(L) is asserted. Both these lines indicate requests from external sources; however, since the DMA/BREQ(L) line must be asserted throughout DMA operations, this line can qualify DMA cycles. The 7D02 monitors the value of this line during data acquisition and displays the message "HALT/DMA" on the top right line of the 7D02 screen whenever C7=0.

NOTE

The 6809E does not have a DMA/BREQ(L) line. When the PM 111 is used with a 6809E, C7=HALT(L).

C6

This line is the Valid Memory Address line generated by the PM 111 hardware. C6=1 whenever the 6809 address bus=FFFF, BS=0, and R/W(L)=1 simultaneously. This indicates a cycle on which internal operations are taking place and no valid information is on the 6809 buses. The user will normally want to qualify on C6=0, when valid bus transactions are (usually) taking place. Refer to the "MC6809 Advance Information" and the "MC6809 - MC6809E Microprocessor Programming Manual" for more information.

C5

This is the Invalid Opcode line generated by the PM 111 hardware. Because this line is asserted the cycle after an invalid opcode is detected, it is useful for triggering but not for clock qualification.

C4

This is the Bus Available line from the 6809. C4=1 qualifies Halt, Bus Grant, and SYNC Acknowledge cycles. It also qualifies the "Dead" cycle preceding a bus exchange. C4=0 qualifies all other cycles, i.e., Normal (running), Interrupt Acknowledge, and Reset Acknowledge cycles. Refer to the "MC6809 Advance Information" for more information.

THE FORMAT MODE DISPLAY

When the PM 111 is connected to the logic analyzer and the Timing Option is installed in the 7D02, the 7D02 FORMAT key produces the following display:

```
TIMING OPTION WORD RECOGNIZER
   0-BINARY
WORD RECOGNIZER ADDRESS FIELD
   2-HEX
WORD RECOGNIZER DATA FIELD
   2-HEX
TIMING OPTION DATA DISPLAY
   0-BINARY
ADDRESS FIELD DISPLAY
   2-HEX
DATA FIELD DISPLAY
   2-HEX
HIGHLIGHT MEMORY DIFFERENCES?
   1-NO
DISPLAY GLITCHES?
   0-YES
TIMING OPTION DATA INVERSION
   DATA=00000000
```

The PM 111-specific menus are:

The WORD RECOGNIZER ADDRESS FIELD menu sets the radix for the ADDRESS field in the WD RECOGNIZER display. It does not affect the acquired data display.

The WORD RECOGNIZER DATA FIELD menu sets the radix for the DATA field in the WD RECOGNIZER display. It does not affect the acquired data display.

The ADDRESS FIELD DISPLAY sets the radix for the acquired address bus values when displayed in the Absolute display mode.

The DATA FIELD DISPLAY sets the radix for the acquired data bus values when displayed in the Absolute display mode.

The following Table 2-2 lists the possible radix selections for the preceding Format display fields.

Table 2-2
RADIX SELECTION

FIELD	RADICES			
	BINARY	OCTAL	HEX	ASCII
TIMING OPTION WORD RECOGNIZER	*	X	X	
WORD RECOGNIZER ADDRESS FIELD	X	X	*	
WORD RECOGNIZER DATA FIELD	X	X	*	
TIMING OPTION DATA DISPLAY	*	X	X	X
ADDRESS FIELD DISPLAY	X	X	*	X
DATA FIELD DISPLAY	X	X	*	X

X = Possible Selection Choice
* = Power-up Default Radix

MNEMONIC DISPLAY OF ACQUIRED DATA

The PM 111 - 7D02 Logic Analyzer produces a mnemonic disassembly display like the following:

```
LOC ADDR  OPERATION          INT
001 4047  FF    FETCH 2       0
---T494A  BF    READ          0
003 494B  6C    READ          0
004 494C  5D    READ          0
005 4048 TFR  A,B             0
```

All numeric data, in the mnemonic display, is displayed in the hex radix and the radices may not be changed with the 7D02 FORMAT key. On most Fetch-1 cycles, the data and status fields (under the OPERATION column) are replaced with the disassembled instruction.

Correct disassembly by the firmware is guaranteed when default clock qualification is used. If data qualification is used, it must be such that all fetch cycles are stored (i.e., store on Word Recognizer FETCH1+2=1) for correct disassembly.

THE HEADER

The first line of the mnemonic display will be the following header:

LOC ADDR OPERATION INT

The meanings of the column headers are as follows:

LOC — is the column that contains a decimal number, 0-255, indicating the location in the logic analyzer acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest acquired data.

ADDR — is the column that contains the value that was on the 6809 address bus when this word of data was acquired.

OPERATION — is the column that contains the disassembled 6809 instruction (on Fetch-1 cycles), or the value that was on the data bus together with a label identifying the cycle type (on non-Fetch-1 cycles).

INT — is the column that contains the value of the interrupt that was on control line C3 (INT) when this word of data was acquired.

DISPLAY OF NON-FETCH-1 CYCLES

On non-Fetch-1 cycles, a word of data will be displayed as:

111 aaaa dd cccccccc i

where

111 — is the acquisition memory location (000-255) of the word of data displayed in this line. The oldest word of data is in location 000, the newest in 255.

aaa — is the address bus value.

dd	is the data bus value.
ccccccc	is the cycle type (i.e., one of the following):
	"FETCH 2" (Fetch-2 cycle)
	"READ " (memory read cycle)
	"WRITE " (memory write cycle)
	"????? " (invalid cycle: a combination of control lines that should not occur).
	Refer to Table 2-1 for the relationship between these cycle types and the control lines C2-C0.
i	is the value that was on control line C3 when this word of data that acquired. The value will be 1 if an interrupt request was pending, and 0 if there was no interrupt request.

The trigger word will be emphasized by displaying the letter "T" in column 4 and by replacing the memory location under the LOC header column with a horizontal bar.

```
   ---Taaaa  dd    ccccccc       i
```

DISPLAY OF FETCH-1 CYCLES

On the first opcode fetch cycle of an instruction, the disassembled mnemonics for the instruction will appear instead of the normal data and status display. The instruction will be displayed in two blank-separated fields: the opcode mnemonic, and the instruction operand(s), if any.

Under default clock qualification, there is one exception. At the beginning of its interrupt processing sequence, the 6809 does a fetch of the first byte of what would have been the next instruction. It then discards this fetch and goes into its register stacking and vectoring. Such discarded Fetch-1 cycles are displayed in the same format as non-Fetch-1 cycles, except that the cycle label is FETCH.

If the user modifies the clock qualifiers so that DMA cycles are stored, a similar situation will arise whenever a Fetch-1 precedes a DMA sequence. In this case, the instruction actually was executed, but its individual cycles may be strung out through and interleaved with DMA cycles. Correct disassembly is not guaranteed if default clock qualification is not used.

MC6809 instructions consist of one or two opcode bytes and 0-3 additional bytes that describe the operands of the instruction. In case of multiple-byte instructions, the firmware will search ahead in acquisition memory for the additional bytes in order to provide operands for the disassembled instructions. If the needed word is in memory, it will be used to disassemble the instruction and will also appear on its own display line (as hex data) at its location in acquisition memory.

The format of a Fetch-1 display line will be as follows:

```
lll aaaa mmmm oooooooooooooo i
```

where "lll", "aaaa", and "i" are previously described and

mmmm	is the opcode mnemonic.
oooooooooooooo	represents the disassembled operand(s), if any.

The trigger word will be emphasized by displaying the letter "T" in column 4 and by replacing the space under the LOC header column with a horizontal bar.

```
---Taaaa mmmm oooooooooooooo i
```

Instruction Opcodes

The following opcode mnemonics will be supported:

ABX	BHI	CMPA	EXG	LBPL	LSL	PULU	STX
ADCA	BITA	CMPB	INC	LBRA	LSLA	ROL	STY
ADCB	BITB	CMPD	INCA	LBRN	LSLB	ROLA	SUBA
ADDA	BLE	CMPS	INCB	LBSR	LSR	ROLB	SUBB
ADDB	BLS	CMPU	JMP	LBVC	LSRA	ROR	SUBD
ADDD	BLT	CMPX	JSR	LBVS	LSRB	RORA	SWI
ANDA	BMI	CMPY	LBCC	LDA	MUL	RORB	SWI2
ANDB	BNE	COM	LBCS	LDB	NEG	RTI	SWI3
ANDCC	BPL	COMA	LBEQ	LDD	NEGA	RTS	SYNC
ASR	BRA	COMB	LBGE	LDS	NEGB	SBCA	TFR
ASRA	BRN	CWAI	LBGT	LDU	NOP	SBCB	TST
ASRB	BSR	DAA	LBHI	LDX	ORA	SEX	TSTA
BCC	BVC	DEC	LBLE	LDY	ORB	STA	TSTB
BCS	BVS	DECA	LBLS	LEAS	ORCC	STB	
BEQ	CLR	DECB	LBLT	LEAU	PSHS	STD	
BGE	CLRA	EORA	LBMI	LEAX	PSHU	STS	
BGT	CLRB	EORB	LBNE	LEAY	PULS	STU	

The opcode set is essentially that described in the reference material listed in the Introduction section of this manual. However, since the ASL, ASLA, ASLB, BHS, BLO, LBHS, and LBLO mnemonics are redundant to those listed below, they have not been included. The following mnemonics are synonymous with the those just mentioned, and are used instead: LSL, LSLA, LSLB, BCC, BCS, LBCC, and LBCS respectively.

On each Fetch-1 cycle, the 6809 does a prefetch of the next byte of the instruction. Normally the prefetch will be either a Read or a Fetch-2 cycle. If the instruction is only one byte long (e.g., the SYNC instruction), this prefetched byte is discarded by the processor. The PM 111 labels and displays such discarded prefetches as READ cycles. Note that if there is no change in the flow of control, the discarded byte will be refetched and executed on the next Fetch-1 cycle. This time the PM 111 will label it a FETCH1 and it will be disassembled in mnemonic displays.

An illegal opcode during disassembly will be displayed as "****" and the hex value of the opcode (the value on the data bus) will be displayed in parenthesis in the operand field.

EXAMPLE:

```
LOC ADDR  OPERATION       INT
133 1700  ****  (1B)       0
```

It takes two bytes to determine the opcode mnemonic for a Page-2 or Page-3 instruction; the first byte (10H or 11H, respectively) will be displayed as an illegal opcode if the second byte (the Fetch-2 cycle) is either invalid or not stored in acqusition memory.

Instruction Operands

The manner in which an operand is displayed will depend on the addressing mode used, as follows:

Immediate:	#xx or #xxxx
Direct:	@xx
Extended:	xxxx
Extended Indirect:	[xxxx]
Register (TFR,EXG):	r,r
Relative/Long Relative:	xxxx
Push/Pull Instructions:	r,r,...,r (up to 7 registers)
	ALL (if all 8 registers)
Indexed:	[,i]
	[?xx,i]
	[?xxxx,i]
	[a,i]
	,i+
	[,i++]
	,-i
	[,--i]
	[?xx,PCR]
	[?xxxx,PCR]

where
x = hex digit
a = A, B, D (any accumulator register)
r = A, B, D, X, Y, S, U, PC, DP, CC (any register [not D on Push/Pull])
i = X, Y, S, U (any index register)
? = optional "-"
[] = are optional on indexed operands (presence indicates indirection)

Asterisks. The asterisks displayed in the operand field indicate one of the following conditions:

- missing operands (operands that cannot be disassembled because a needed cycle was not stored in the acquisition memory). In general, one "*" will be displayed for each hex digit or register name that is missing.
- an invalid postbyte for an Indexed instruction. The operand display in this case will always be "*,*", as if the post-byte were not in memory at all.

- an invalid register number in the postbyte of a TFR or EXG instruction. Such a postbyte consists of two 4-bit fields (one for each register number), but only 10 of the 16 possible register numbers are meaningful. One "*" will be displayed for each invalid register number.

NOTE

A TFR or EXG instruction must specify two registers of equal length (8-bit or 16-bit). The PM 111 will display an instruction such as "TFR A,X" even though it is not valid.

MNEMONIC DISPLAY EXAMPLE

The following is a portion of a hypothetical display:

```
LOC ADDR  OPERATION          INT
001 2662 TFR  A,B             0
002 2623  89    FETCH 2       0
---T2624 BEQ  269E            0
004 2625  78    READ          0
005 269E PSHS A               0
006 269F  02    FETCH 2       0
007 3007  77    WRITE         0
008 26A0 ORB  #**             0
```

Lines 001-002 display the two cycles of a TFR instruction. Line 002 is the postbyte containing the 2 register numbers used to disassemble the "A,B" operands in line 001.

Line 003 is the trigger word. Lines 003-004 display the 2 cycles of a BEQ. Note that the 8-bit displacement (line 004) is used to produce a 16-bit absolute address in the disassembly (line 003).

Lines 005-007 show a PSHS of the 8-bit register A. Line 006 is the register mask from which the operand "A" was disassembled. Line 007 is the actual write of the contents of A to the stack.

Line 008 is the last word in acquisition memory. The instruction is an OR immediate to register B. The operand cannot be disassembled because the cycle on which the immediate data was read was not stored in memory.

ABSOLUTE DISPLAY OF ACQUIRED DATA

The PM 111-7D02 Logic Analyzer produces an absolute display like the following:

LOC	ADDRESS	DATA	I
001	4047	FF	F0
---T	494A	BF	R0
003	494B	6C	R0
004	494C	5D	R0

In absolute data display mode, the radices in which the data and address buses are displayed are individually selectable as binary, octal, hex, or ASCII. The default for each is hex.

THE HEADER

The first line of the absolute display will be the following header:

LOC ADDRESS DATA I

The meanings of the column headers are as follows:

LOC — is the column that contains a decimal number, 0-255, indicating the location in the logic analyzer acquisition memory. In order of acquisition, 000 is the oldest acquired data, and 255 is the newest acquired data.

ADDRESS — is the column that contains the value that was on the 6809 address bus when this word of data was acquired.

DATA — is the column that contains the value that was on the 6809 data bus when this word of data was acquired.

I — is the column that contains the value of the interrupt that was on the C3 (INT) control line when this word of data was acquired.

DATA DISPLAY

A single word of data will be displayed in the following format:

```
111 aaaaaaaaaaaaaaaa dddddddd ci
```

where

111	is the acquisition memory location (0-255) of the word of data displayed on this line. The oldest word of data is in location 000, the newest in 255.
aaaaaaaaaaaaaaaa	is the address bus value. It will be 4-16 digits long (radix-dependent) and centered in the field.
dddddddd	is the data bus value. It will be 2-8 digits long (radix-dependent) and centered in the field.
c	is the cycle type, i.e., one of the following: "F" (opcode fetch) "R" (memory read) "W" (memory write) "?" (invalid cycle: a combination that should not occur) Refer to Table 2-1 for the relationship between the previous cycle types and the control lines C2-C0.
i	is the value that was on control line C3 when this word of data was acquired. The value will be 1 if an interrupt request was pending, and 0 if there was no interrupt request.

The trigger word will be emphasized by displaying the letter "T" in column 4 and by replacing the space under the LOC header column with a horizontal bar.

ABSOLUTE DISPLAY EXAMPLE

The following is a portion of a hypothetical display. Note that in actual use:

- The radix of the address or data bus will not change from line to line.
- The address and data buses need not be displayed in the same radix.

```
LOC      ADDRESS          DATA     I
000        1654            22     F0
---T     177765            116    W0
002        R <E>           T      R1
003 1111000010100011 11001011 R0
```

Line 000 demonstrates hex radices for both the data and address buses.

Line 001 is a trigger line with octal radices for both buses.

Line 002 is an example of ASCII radices.

Line 003 is an example of binary radices.

ADDITIONAL INFORMATION

CONTROL LINES

The following table summarizes information concerning the control lines and their relationship to the PM 111 Personality Module.

Table 2-3
PM 111 CONTROL LINES

LINE	DERIVED FROM	ACTIVE	STORED	WORD RECOGNIZER	CLOCK QUALIFIER (DEFAULT)	COMMENTS
R/W(L) (C0)	6809 R/W(L) LINE	(H)/(L)	YES	YES		1
FETCH1 (C1)	PM 111 HARDWARE	(H)*	YES	YES		1
FETCH1+2 (C2)	PM 111 HARDWARE	(H)*	YES	YES		1
INT (C3)	6809 NMI(L), IRQ(L),FIRQ(L)	(H)	YES	YES		2
BA (C4)	6809 BA LINE	(H)		YES	X	3
INVAL.OP (C5)	PM 111 HARDWARE	(H)		YES	X	4
VMA(L) (C6)	6809 address bus,BS,R/W(L)	(L)			0	5
HALT. (DMA/ BREQ) (C7)	6809 HALT(L), DMA/BREQ	(H)			X	6
DMA+DEAD (C8)	PM 111 hardware, BA line	(H)			0	7
(C9)	tied high	(H)			X	8

*= Asserted low in the hardware, but inverted by firmware to appear asserted high to user.

COMMENT FIELD NUMBERS

1= Refer to Table 2-1.

2= Interrupts sampled on the falling edge of clock E. Minimum pulse width of 1 E cycle required on NMI(L).

3= Related to C8. Always low under default clock qualification.

4= Asserted 1 cycle after an illegal opcode; not useful as clock qualifier.

5= Similar to the 6800 VMA line, except asserted low.

6= C7 is asserted low when HALT(L) or when DMA/BREQ(L) is low. HALT(L) line (only) when used with the 6809E microprocessor.

7= Asserted high when BA is high, and for one cycle after BA goes low.

8= Always high (H); do not use.

6809E OPERATING CONSIDERATIONS

The following information pertains to the operation of the 6809E series of microprocessors.

- The 6809E may not be halted under control of the 7D02-PM 111 system.
- The 6809E does not have a DMA/BREQ(L) line. When the PM 111 is used with the 6809E series of microproceesors, the control line C7= HALT(L).
- The real time message DMA/HALT will flicker in the upper right hand corner of the screen while the 7D02 is waiting for a trigger. This message appears when the busy line is low. This may be remedied, if desired, by changing the PM 111 internal jumper strap A2J7013 to the 6809E position.

SPECIAL INSTRUCTION OPCODES

Both the CWAI and the SYNC opcodes can give a slow clock indication. This occurrence is normal when executing these instructions.

HALTING THE 6809 MICROPROCESSOR

The PM 111 Personality Module is a passive bus monitor, with the exception of the HALT(L) line. The PM 111 hardware permits the microprocessor in the zero insertion force (ZIF) socket to be halted by the user's system under test (SUT), and/or the 7D02 Logic Analyzer. To halt the processor from the SUT, assert the SUT's HALT(L) line low. To halt the processor from the 7D02, change the trigger menu from SYSTEM UNDER TEST CONT. to SYSTEM UNDER TEST HALT. Using the CURSOR control key, move the cursor to the field and enter a 1. Upon triggering, the 7D02 will halt the processor. It will remain halted until the 7D02 returns to acquiring data and has not yet triggered. This applies only to the 6809 microprocessor in the PM 111 ZIF socket, and not the 6809E microprocessor, which must remain in the user's system.

PM 111 SPECIFICATIONS

OVERVIEW

This section of the manual lists the following PM 111 specifications:

TABLE TYPE	TABLE NUMBER
CHARACTERISTICS	3-1
QUALIFIERS	3-2
ELECTRICAL	3-3
MECHANICAL	3-4
ENVIRONMENTAL	3-5
PM 111 LOGIC ANALYZER CABLE	3-6
MICROPROCESSOR PLUG	3-7

Items listed in the Performance Requirements column are specifications of the instrument that can be verified as described in the Performance Check section of this manual.

If verification of these listed electrical specifications is necessary for customer incoming inspection or other purposes, the Performance Check section lists the necessary test equipment and procedures for doing so.

Items listed in the Supplemental Information column are either explanatory notes or performance characteristics for which no limits are specified. They are not tested in the Performance Check section of this manual.

The PM 111 Personality Module supports the following microprocessors:

MC6809
MC68A09
MC68B09
MC6809E
MC68A09E
MC68B09E

SYSTEM DESCRIPTION

HALT PUT(L) is an output from the logic analyzer. The PM 111 generates HALT(L) from the HALT PUT(L) and P HALT(L) signals.

LOOK is a control line generated by the 7D02 that disables the AI0-AI15 and DI0-DI7 buffers in the personality module.

SELP(L) is a control line generated by the 7D02 that is used to read the PROM in the personality module.

SAFETY GOALS

The personality module complies with the requirements of U.L. 1244, IEC 348, and CSA 556B.

Table 3-1
PM 111 CHARACTERISTICS

CHARACTERISTIC	DESCRIPTION
Signal Inputs	
Max. Number of Channels	33
Data Lines	8
Address Lines	16
Control Lines	9
Clock (E)	
Maximium Frequency	2 MHz (68B09/68B09E)
Minimum Frequency	100 kHz
Display	
Max. No. of Channels	28
Data Lines	8
Address Lines	16
Control Lines	4

Table 3-2
PM 111 QUALIFIERS

LINE	STORED		WORD RECOGNIZER	CLOCK QUALIFIER
R/W(L)	C0	X	X	
IFC(L)	C1	X	X	
(IFC+IFC2)(L)	C2	X	X	
INT	C3	X	X	
BA	C4		X	X
IOCO(L)	C5		X	X*
VMA(L)	C6			X
(HALT).(DMA/BREQ)	C7			X
DMA+DEAD	C8			X

* NOTE: Not useful for clock qualification.

Table 3-3

ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Data Input Channels		
TTL Input Levels		0 V to +7 V signal swing 1/2 LSTTL load, except PHALT(L) =1 LSTTL load
Input Capacitance		45 pF nominal
Voltage in low limits (operating)	+0.6 V max.	+0.0 V min.
Voltage in high limits (operating)	+2.0 V min.	+7.0 V max.
Current in low limits (V in low =+0.4 V)		-0.2 mA max. (-0.4 mA max. for PHALT)(L)
Current in high limits (V in high =+7.0 V)		+0.1 mA max.
Current in high limits (V in high =+2.7 V)		+0.02 mA max. (+0.04 mA max. for PHALT)(L)
Maximum voltage in, non-operating, non-destructive (all except clock)		-7 V to +15 V continuous on any two inputs simultaneously
Threshold Voltage		Fixed +1.4 V nom. TTL compatible
Hysteresis		+0.4 V nom. +0.2 V min.

Table 3-3 (cont)
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Delay from logic analyzer HALT PUT(L) to HALT(L) out		
Maximum		50 ns
HALT(L) output drive		
V out high		+2.4 V, I out=1mA
V out low		+0.5 V, I out=-1mA
Clock (E), pin 34 of microprocessor		
Input Impedance		50 kilohms nominal
Input Capacitance		35 pF nominal
Clock Period	500 ns min.	10,000 ns max.
Clock Pulse Width (min.)		220 ns high, 210 ns low
Voltage in low limits (operating)		+0.0 V min., +0.5 V max.
Voltage in high limits (operating)		+2.4 V min., +5.6 V max.
Threshold Voltage		Fixed, +1.4 V nom.
Hysteresis		+0.4 V nominal
Maximum Voltage in non-operating, non-destructive		-15 V to +15 V
Crystal Loading (MC6809)		
C in, pin 38		Typ. 15 pF
C out, pin 39		Typ. 9 pF

Table 3-3 (cont)
ELECTRICAL SPECIFICATIONS

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
Propagation Delays through personality module		
Delay through ECL clock		+10.5 ns min., +15 ns max.
Delay added to PHALT(L) line (from 40-pin plug to microprocessor)	55 ns max.	
Channel Delay		
DMA+DEAD		145 ns max.
(HALT).(DMA/BREQ)		125 ns max.
VMA(L)		170 ns max.
IOCO(L) (clocked)		450 ns max.
INT		155 ns max.
IFC(L) (clocked)		210 ns max.
(IFC+IFC2)(L) (clocked)		485 ns max.
Delay, Data Channels DI0-DI7		15 ns min., 45 ns max.
Delay, all other channels		10 ns min., 50 ns max.
Test Clock		
Clock Period	450 ns min., 500 ns max.	
Oscillator Pulse Width (high or low)	75 ns min.	Test Clock Osc. runs at 2X E Clock

Table 3-3 (cont)
ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL INFORMATION
System Specifications with logic analyzer		
Control		
Setup Time		
R/W(L)		140 ns*
BA		190 ns*
BS		160 ns*
(DMA/BREQ)(L)		120 ns*
NMI(L)		155 ns**
IRQ(L)		95 ns**
FIRQ(L)		95 ns**
Hold Time		
R/W(L)		0 ns
BA		0 ns
BS		0 ns
(DMA/BREQ)(L)		0 ns
NMI(L)		0 ns
IRQ(L)		0 ns
FIRQ(L)		0 ns
Address		
Setup Time		220 ns max.
Hold Time		0 ns max.
Data DI0-DI7		
Setup Time	40 ns max.	
Hold Time	10 ns max.	
Data Acquisition Period	500 ns min.	
Timing Option Data		
Setup Time	20 ns max.	
Hold Time	5 ns max.	
Power Dissipation in pod		3.0 W max.

*= Sampled on the falling edge of clock E.
**= All PM 111 interrupt lines are sampled on the falling edge of clock E, as opposed to the Motorola specification of sampling on the falling edge of Q. This is no problem so long as the interrupts are not cleared by the falling edge of Q. On NMI (L), there is a requirement for a minimum pulse width of 1 E cycle.

Table 3-4
MECHANICAL SPECIFICATIONS

CHARACTERISTIC	SUPPLEMENTAL INFORMATION
Size	4.7" x 8" x 1.9" (12 x 20.3 x 4.8 cm)
Weight	Approx. 2.5 lbs. (1.2 kg) with cables
Cable Length (logic analyzer to module)	4 ft. +/- 1.0 in. (122 cm +/- 2.5 cm)
Cable Length (SUT plug to personality module pod)	18.5 in. +/- .5 in. (47 cm +/- 1.3 cm)

Table 3-5
ENVIRONMENTAL SPECIFICATIONS

CHARACTERISTIC	SUPPLEMENTAL INFORMATION
Temperature	
Operating	-15 deg. C to +55 deg. C
Non-operating (in module pod)	-62 deg. C to +85 deg. C
Relative Humidity	95 to 97%, non-condensing
Altitude	
Operating	15,000 ft. (4.5 km)
Non-operating	50,000 ft. (15 km)

Table 3-6
PM 111 LOGIC ANALYZER CABLE

PM 111 J1048 PIN	SIGNAL	DESCRIPTION
1	GND	GROUND
2	CLK	Differential ECL level; high=-0.8 V,low=-1.7 V
3	CLK(L)	Differentially terminated into 124 ohms; ECL level
4	GND	GROUND
5	AI0	*
6	AI1	*
7	AI2	*
8	AI3	*
9	AI4	*
10	AI5	*
11	AI6	*
12	AI7	*
13	AI8	*
14	AI9	*
15	AI10	*
16	AI11	*
17	AI12	*
18	AI13	*
19	AI14	*
20	AI15	*
21	+5 V	+5 V

*= STTL output back terminated into 68 ohms.

Table 3-6 (cont)
PM 111 LOGIC ANALYZER CABLE

PM 111 J1048 PIN	SIGNAL	DESCRIPTION
22	+5 V	+5 V
23	+5 V	+5 V
24	+5 V	+5 V
25	+5 V	+5 V
26	+5 V	+5 V
27	+5 V	+5 V
28	+5 V	+5 V
29	DI0	*
30	DI1	*
31	DI2	*
32	DI3	*
33	DI4	*
34	DI5	*
35	DI6	*
36	DI7	*
37	+5 V	+5 V
38	+5 V	+5 V
39	+5 V	+5 V
40	+5 V	+5 V
41	+5 V	+5 V
42	+5 V	+5 V
43	+5 V	+5 V

*= STTL output back terminated into 68 ohms.

Table 3-6 (cont)
PM 111 LOGIC ANALYZER CABLE

PM 111 J1048 PIN	SIGNAL	DESCRIPTION
44	+5 V	+5 V
45	+5 V	+5 V supply
46	R/W(L)	C0, *
47	IFC(L)	C1, *
48	IFC+IFC2(L)	C2, *
49	INT	C3, *
50	BA	C4, *
51	IOCO(L)	C5, *
52	VMA(L)	C6, *
53	(HALT).(DMA/BREQ)	C7, *
54	DMA+DEAD	C8, *
55	+5 V	C9, +5 V
56	+5 V	+5 V supply
57	+5 V	+5 V supply
58	+15 V	+15 V supply
59	-15 V	-15 V supply
60	GND	GROUND
61	HALT PUT(L)	1 LSTTL Input Load
62	LOOK	3 LSTTL Input Loads
63	SELP(L)	2 LSTTL Input Loads
64	GND	GROUND

*= STTL output back terminated into 68 ohms.

Table 3-7
MICROPROCESSOR PLUG

TO POD CONNECTION	ZIF	SIGNAL NAME 6809(E)	EXTRA SIGNALS (PM 111)	STATIC PROTECTION 6809/6809E
J3002-				
1			GND	NO
2			GND	NO
3	5	BS		YES
4	6	BA		YES
5	4	FIRQ(L)		YES
6	3	IRQ(L)		YES
7	2	NMI(L)		YES
8	7	VCC		YES*
9	8	A0		YES
10			NC	NO
11	9	A1		YES
12	10	A2		YES
13	1	VSS		NO
14	11	A3		YES
15			-9.5V	NO
16	12	A4		YES

* = Etched spark gap only.

All lines from the microprocessor plug connect to the microprocessor in the ZIF socket, except pin 40, and pins 38 and 39, which connect to a hybrid clock oscillator in the plug.

Table 3-7 (cont)
MICROPROCESSOR PLUG

TO POD CONNECTION	ZIF	SIGNAL NAME 6809(E)	EXTRA SIGNALS (PM 111)	STATIC PROTECTION 6809/6809E
17	13	A5		YES
18	14	A6		YES
19	20	A12		YES
20	19	A11		YES
21	18	A10		YES
22	17	A9		YES
23	15	A7		YES
24	16	A8		YES
25			GND	NO
26			GND	NO
J3004-				
1			GND	NO
2			GND	NO
3	36	MRDY (AVMA)		YES*
4	37	RESET(L)		YES*
5	38	EXTAL		YES
6	39	XTAL		YES*
7		HALT(L)		YES

* = Etched spark gap only.

All lines from the microprocessor plug connect to the microprocessor in the ZIF socket, except pin 40, and pins 38 and 39, which connect to a hybrid clock oscillator in the plug.

Table 3-7 (cont)
MICROPROCESSOR PLUG

TO POD CONNECTION	ZIF	SIGNAL NAME 6809(E)	EXTRA SIGNALS (PM 111)	STATIC PROTECTION 6809/6809E
8	35	Q OUT (Q IN)		YES*
9	34	E OUT (E IN)		YES
10	33	DMA/BREQ(L)	(BUSY)	YES
11	32	R/W(L)		YES
12	31	D0		YES
13			VSS	NO
14	30	D1		YES
15			INV OUT	NO
16	29	D2		YES
17	28	D3		YES
18	27	D4		YES
19	21	A13		YES
20	22	A14		YES
21	23	A15		YES
22	24	D7		YES
23	26	D5		YES
24	25	D6		YES
25			GND	NO
26			GND	NO

* = Etched spark gap only.

All lines from the microprocessor plug connect to the microprocessor in the ZIF socket, except pin 40, and pins 38 and 39 which connect to a hybrid clock oscillator in the plug.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

SERVICING SAFETY SUMMARY

For Qualified Service Personnel Only

Refer also to the Operator's Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid is present.

Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connectors and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is designed to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

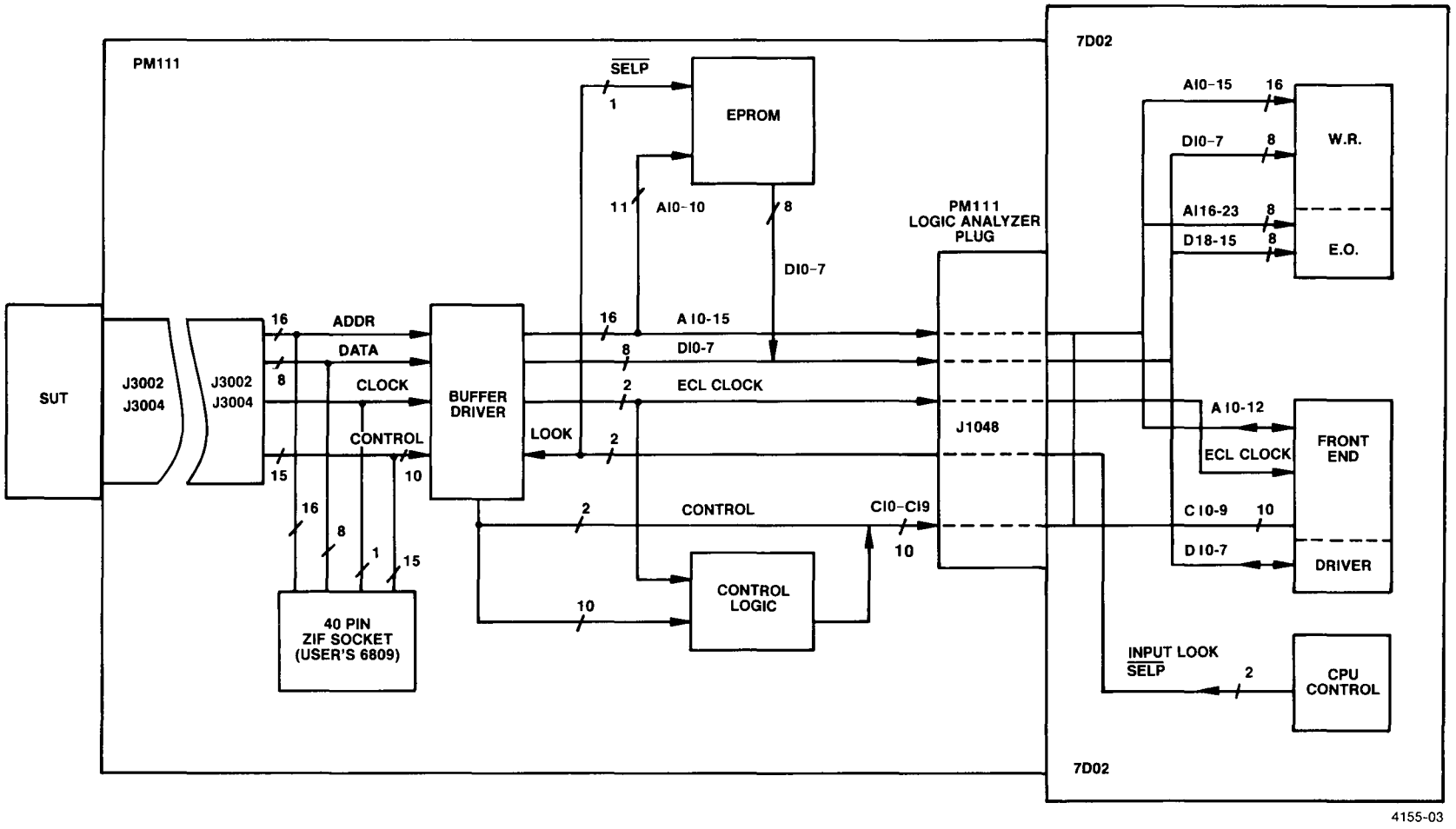


Figure 4-1. Overview block diagram.

GENERAL THEORY OF OPERATION

OVERVIEW

The PM 111 Personality Module acts as a passive bus monitor over the 6809/6809E bus in real time. The personality module generates information according to conditions present on the bus for 7D02 data qualification and triggering.

FUNCTIONS

The PM 111 Personality Module performs two basic functions. First, the PM 111 acts as a hardware interface between the microprocessor system and the logic analyzer. The PM 111 allows the selected microprocessor to operate as if it were in the system under test (SUT) with the address, data, control, and clock lines available to the logic analyzer. The second function of the PM 111 is to provide personalized interpretation and setup information, which is specific to the 6809/6809E microprocessors, in a standard format for the logic analyzer. This information aids in mnemonic disassembly of acquired information, customizing of displays, and in providing default word recognition.

BLOCK DIAGRAMS AND SCHEMATICS

Figure 4-1 is an Overview block diagram illustrating the overall interaction between the system under test (SUT), the personality module, and the logic analyzer.

Figures 4-2, 4-3, and 4-7 are detailed block diagrams of boards A1, A2, and A3 respectively. These block diagrams, showing individual function blocks, should be useful when troubleshooting certain problems.

Schematic diagrams are provided in the Diagrams section of this manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

CONVENTIONS USED IN THIS MANUAL

A bar (—) over a signal name or portion of a signal name in the schematics, indicates that the signal is active when in the low state. For example, $\overline{\text{HALT}}$ indicates that HALT is an active low signal. R/$\overline{\text{W}}$ indicates that 1=read, 0=write.

An (H) or (L) following a signal name indicates that the signal is active in the high or low state. For example, LOOK(H) indicates that LOOK is an active high signal. SELP(L) indicates that SELP is an active low signal. The absence of an (L) after a signal name implies active high (H).

A slash (/) before a signal name or portion of a signal name in the simulated screen displays, indicates that the signal name appears that way on the 7D02 screen. For example, R/W is the same as $R/\overline{W}$ for the schematics and R/W(L) for the text.

Component numbers in this manual are composed of an assembly number and a schematic circuit number. For example, A1U3025 indicates that component U3025 is located on assembly A1 (board 1) of the personality module.

The following board-related terms should be considered synonymous:

upper - top - Buffer Board - Assembly A1
middle - Fetch Predictor Board - Assembly A2
lower - bottom - Self-Test Board - Assembly A3

THE FETCH PREDICTOR

The Fetch Predictor, located on boards A1 and A2, is a State Machine which predicts fetches of opcodes in a sequence of 6809 instructions. A fetch is defined as the first or subsequent byte(s) of data defining an opcode of an instruction. The instruction fetch must be distinguished from operand reads in order to (1) facilitate proper disassembly into opcode mnemonics and (2) make possible data qualification of fetches prior to execution. Since the fetch predictor anticipates the fetch in time for the clock edge that latches it into the 7D02's memory, the corresponding memory read can be labeled as a fetch in acquisition memory.

SELF-TEST CIRCUITRY

The Self-Test Circuitry, located on the bottom board (A3), supplies stimulus on both the 40-pin test socket and the timing option pins, A3J2042. The stimulus at the 40-pin test socket emulates a user's SUT executing a sequence of instructions, and receiving external stimuli, such as interrupts, HALT, and DMA/BREQ. These instructions are representative of each major type of 6809 opcode, and thoroughly exercise the fetch predictor, buffer, and clock hardware. There is no particular significance to the sequence of the instructions. They are listed in the Performance Check section, which is used as reference in the self-test mode of operation. The output at the timing option pins,

also a known pattern, is used as a reference during the Power-Up Verification sequence. Refer to the Performance Checks for more information concerning these outputs.

6809E HARDWARE CONSIDERATIONS

The following information pertains to the operation of the 6809E series of microprocessors.

- The 6809E may not be halted under control of the 7D02-PM 111 system.
- When the PM 111 is used with the 6809E series of microprocessors, the control line C7=HALT(L).
- When using the 6809E microprocessor, which has a BUSY line in place of the 6809 DMA/BREQ(L) line, the message HALT/DMA in the upper right corner of the 7D02 screen may flash during data acquisition. If desired, the message may be disabled by moving the jumper A1J7013 to pins 2 and 3.

BOARD 1 DETAILED CIRCUIT DESCRIPTIONS

OVERVIEW

The block diagram of Figure 4-2 shows this circuitry in functional blocks. Refer to Figure 4-2 for an overview of assembly 1 (board A1) and to aid in understanding the flow of signals to and from this board.

Schematic diagrams are provided in the Diagrams section of this manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

All components in the following board 1 descriptions are located on board A1. As components are referenced, the board number will be omitted from the reference (e.g., A1U1031 will be U1031). Components located on other boards will be referenced including their respective board numbers.

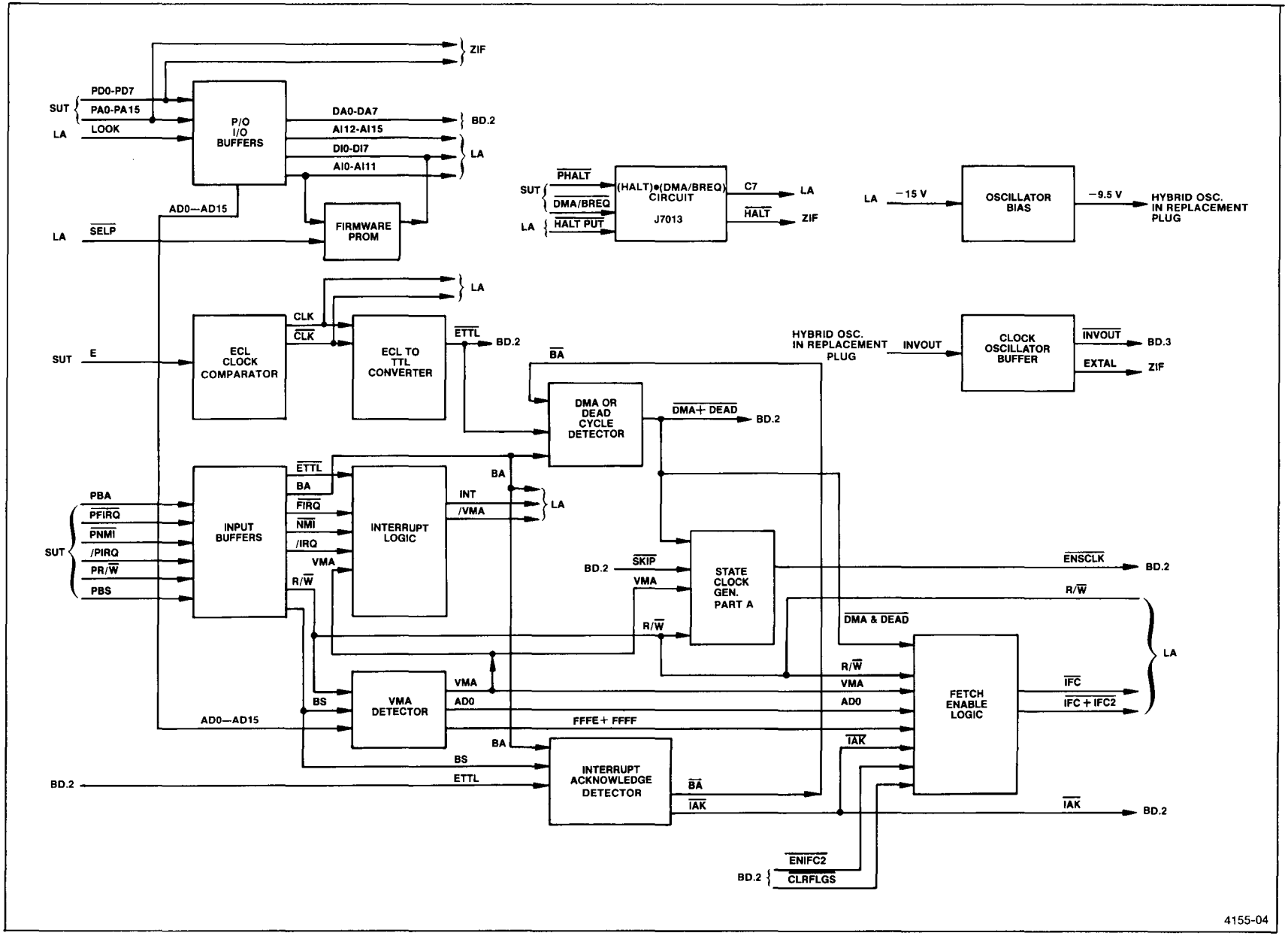


Figure 4-2. Board A1 block diagram.

I/O BUFFERS

The I/O Buffers circuitry accepts the address and data inputs for the personality module from the zero insertion force (ZIF) socket and the 40-pin microprocessor plug. This circuitry contains static input-protection hybrids and two sets of octal buffer-drivers with 3-state outputs.

The first set of buffer-drivers (U4025, U2025, and U6025) are protected by spark gaps against static discharge that could damage the personality module. The buffered data lines DA0-DA7 from U4025 connect to U5025 and the Data Latch A2U3060. The address lines AD0-AD15 from buffers U2025 and U6025 connect to U2035, U6035, and the VMA Detector circuitry.

The second set of buffer-drivers U5025, U2035, and U6035 are tri-stated by the LOOK line (from the logic analyzer) when the logic analyzer is reading the contents of the EPROM. Outputs from these buffers connect to the Firmware EPROM and the logic analyzer.

FIRMWARE EPROM

The Firmware EPROM function block consists of a 2Kx8 EPROM (U4035) and an 8-bit tri-state buffer driver (U5035). The EPROM, addressed by AI0-AI11, contains information used by the 7D02 to modify the 7D02 screen displays and the diagnostics for use with that microprocessor. The SELP(L) signal allows the EPROM and buffer to gate this information onto the data bus.

INPUT BUFFERS

The Input Buffer U1018 accepts the following signals from the 40-pin microprocessor plug and buffers them for use by the board-1 circuitry.

PR/W(L)
PBS
PBA
PNMI(L)
PIRQ(L)
PFIRQ(L)

@

ECL CLOCK COMPARATOR

The ECL Clock Comparator, U1031, is a hysteresis-controlled high speed comparator that generates two ECL level signals CLK and CLK(L) from the E clock signal. The two outputs connect to the ECL To TTL Converter circuit and to the logic analyzer.

The 50 kilohm, 4X attenuator input accepts the E clock signal from the 40-pin microprocessor plug. The output from the ECL comparator, U1031, is differential at ECL levels. These outputs, CLK and CLK(L), are used by the logic analyzer to generate a master state clock.

ECL-TO-TTL CLOCK CONVERTER

The ECL-to-TTL converter circuit changes the ECL differential input signals, CLK and CLK(L), to an inverted TTL level signal ETTL(L). The ETTL(L) signal is used by the State Clock Generator and is inverted for use by the Interrupt Acknowledge Detector.

DMA+DEAD CYCLE DETECTOR

The DMA+DEAD Cycle Detector produces the DMA+DEAD(L) signal for use by the State Clock Generator Part A and the logic analyzer (after being inverted). This line is useful in signalling that dead cycles exist or the bus is in use by other controllers.

The DMA+DEAD(L) line is defined as being asserted low whenever BA is high, and for one E clock cycle following BA's transition from high to low. The latter is the trailing dead cycle following the termination of DMA transfers and Sync Acknowledge cycles.

U3045 latches the state of BA from the previous E cycle. The output of U2045 is low if either BA(L) is low (BA is high), or if BA(L) is high (BA is low), and BA, latched in U3045 from the previous cycle, is high.

INTERRUPT ACKNOWLEDGE DETECTOR

The Interrupt Acknowledge Detector, NAND gate U6045B, generates the IAK(L) signal for the Fetch Enable Logic and the Present State Latch. According to Table 4-1, when BS is high (1) and BA is low (BA=0), an Interrupt or Reset Acknowledge state exists within the processor. These two levels, combined with a high ETTL signal, will produce the active low IAK(L) signal. Refer to Figure 4-6.

Table 4-1
PROCESSOR STATE INDICATOR TABLE

BA	BS	Processor State
0	0	Normal (Running)
0	1	Interrupt or Reset Acknowledge
1	0	Sync Acknowledge
1	1	Halt/Bus Grant

INTERRUPT LOGIC

The Interrupt Logic produces a composite interrupt signal, INT, by ORing the NMI(L), IRQ(L), and FIRQ(L) signals. The INT signal to the logic analyzer indicates an interrupt request from any one of these ORed signals, which originate at the SUT.

Since NMI(L) is an edge triggered signal, U3045A must be used to latch the signal in its active low state until the interrupt goes away and a valid memory address on the bus is detected. When NMI(L) goes low, U3045A sends the pin 7 output low. This is the active LNMI(L) signal. When NMI(L) returns high and VMA(L) goes low, ETTL(L) will clock a high onto pin 7 to deactivate the LNMI(L) signal. The INT signal is generated via U6045A.

VMA DETECTOR

The VMA Detector circuitry decodes and supplies the VMA signal to the Fetch Enable Logic, the State Clock Generator Part A, and the inverted VMA(L) signal to the Interrupt Logic function block. An invalid memory address (VMA low or VMA(L) high), exists when the following conditions within the PM 111 are present.

- FFFF is on the address bus
- BS=0
- R/W(L)=1 (READ)

When AD1-AD13 and AD14-AD15 are all high (indicating FFFE or FFFF on the address bus), the outputs at U3025-9 and U5045C-8

(respectively) go low. If BS (U4045C-10) also goes low, the requirements of the first NAND gate are met and the output pin 8 goes high. This output, as well as AD0 and R/W(L), are the inputs to the second NAND gate U6045C. If AD0 and R/W(L) are both high, the requirements for U6045C are met and the low-going VMA signal is generated.

FETCH ENABLE LOGIC

The Fetch Enable Logic circuitry supplies the logic analyzer with the IFC(L) and IFC+IFC2(L) signals on control lines C1 and C2, respectively. The IFC(L) signal, asserted low by the hardware but inverted in the firmware for the screen display, indicates that an Instruction Fetch Cycle (Fetch-1) occurred. The IFC+IFC2 (L) signal, asserted low in the hardware but inverted in the firmware for the screen display, indicates an Instruction Fetch Cycle in which the first or subsequent byte(s) of an instruction were fetched.

The IFC(L) signal, decoded by U4045A, occurs when CLRFLGS(L) and ENIFC(L) are asserted, and FFFE is not. The first line, CLRFLGS(L), is from the Fetch Predictor. This line indicates the end of one completer sequence through the fetch predictor state machine, and that the following cycle will be a fetch. The flags are cleared in preparation for the next cycle through the state machine. FFFE is decoded to exclude the extraneous prediction of fetches during 6809 Reset sequences. U7025B decodes the third signal line, ENIFC(L). When asserted low, this line indicates that the microprocessor is doing a valid read. The following lines are in the high state when this occurs.

- VMA
- R/W(L)
- IAK(L)
- DMA+DEAD(L)

The processor is indicating a valid memory cycle, is reading memory, and is not in an Interrupt Acknowledge or DMA+Dead cycle. The IFC+IFC2(L) line indicates a Fetch-1 or a Fetch-2 is taking place. This occurs when predicted by ENIFC2(L) and when the processor is not doing any of the following transfers: a write, an invalid memory cycle, an Interrupt Acknowledge, a DMA, a Dead cycle, nor an access from FFFE. ENIFC2(L), indicating a Fetch-1 or Fetch-2 cycle, is generated by the Fetch Predictor.

STATE CLOCK GENERATOR PART A

The State Clock Generator Part A enables state clocks only during certain cycles. Gate U7025 is used to qualify state clocks which are valid memory reads, which are not DMA+DEAD cycles, and which are not skipped by the Skip State Clock Circuitry (discussed later).

(HALT).(DMA/BREQ) CIRCUIT

The (HALT).(DMA/BREQ) Circuit has two functions. First, the circuit detects the presence of a halt from either the system under test PHALT(L) or the logic analyzer HALT PUT(L). This halt request is output to the microprocessor installed in the zero insertion force (ZIF) socket on the HALT(L) line, and to the logic analyzer on the (HALT).(DMA/BREQ) line. Secondly the circuitry detects a DMA/BREQ(L) signal from the system under test (SUT) and transmits it to the logic analyzer on the (HALT).(DMA/BREQ) line. The (HALT).(DMA/BREQ) line (the C7 control line), when asserted low, causes the HALT/DMA message to appear on the 7D02 screen.

When the logic analyzer issues a HALT PUT(L) or the SUT issues a PHALT(L), the low signal is inverted twice by passing through U5045A and U7035G. The ORed signal now has two destinations. First the signal is inverted in the NAND gate U5045B and reinverted in U7035C for output on the (HALT).(DMA/BREQ) line. Secondly, the signal connects to pin 40 HALT(L) of the ZIF socket. Regardless of which source issued the halt, both the logic analyzer and the microprocessor are both signalled of the event.

When the SUT sends the DMA/BREQ(L) line low, a request for use of the bus by another controller is signalled. The request has two possible destinations. First, the microprocessor is informed of the request on pin 33, DMA/BREQ(L). Secondly, the request is buffered in U1018G and arrives at J7013. If the jumper is positioned to pass the signal (pins 1 and 2 shorted), U5045B and U7035C pass the signal to the logic analyzer on control line C7. The request for use of the bus has now been indicated to the microprocessor, as well as the logic analyzer. When using the 6809E microprocessor, which has a BUSY line in place of the DMA/BREQ line, the message HALT/DMA in the upper right corner of the 7D02 screen may flash during data acquisition. If desired, the flashing message may be disabled by moving the jumper plug A1J7013 to pins 2 and 3.

CLOCK OSCILLATOR BUFFER

The Clock Oscillator Buffer circuitry accepts the INVOUT signal from the clock oscillator hybrid (in the end of the 40-pin plug)

and inverts it for the Clock Divider circuit on the Self-Test board, and the EXTAL input pin of the 6809 in the zero insertion force (ZIF) socket.

OSCILLATOR BIAS

The Oscillator Bias circuitry provides the clock oscillator hybrid with the necessary -9.5 V for operation. It accomplishes this task by using the -15 V supply and a -5.6 V zener diode.

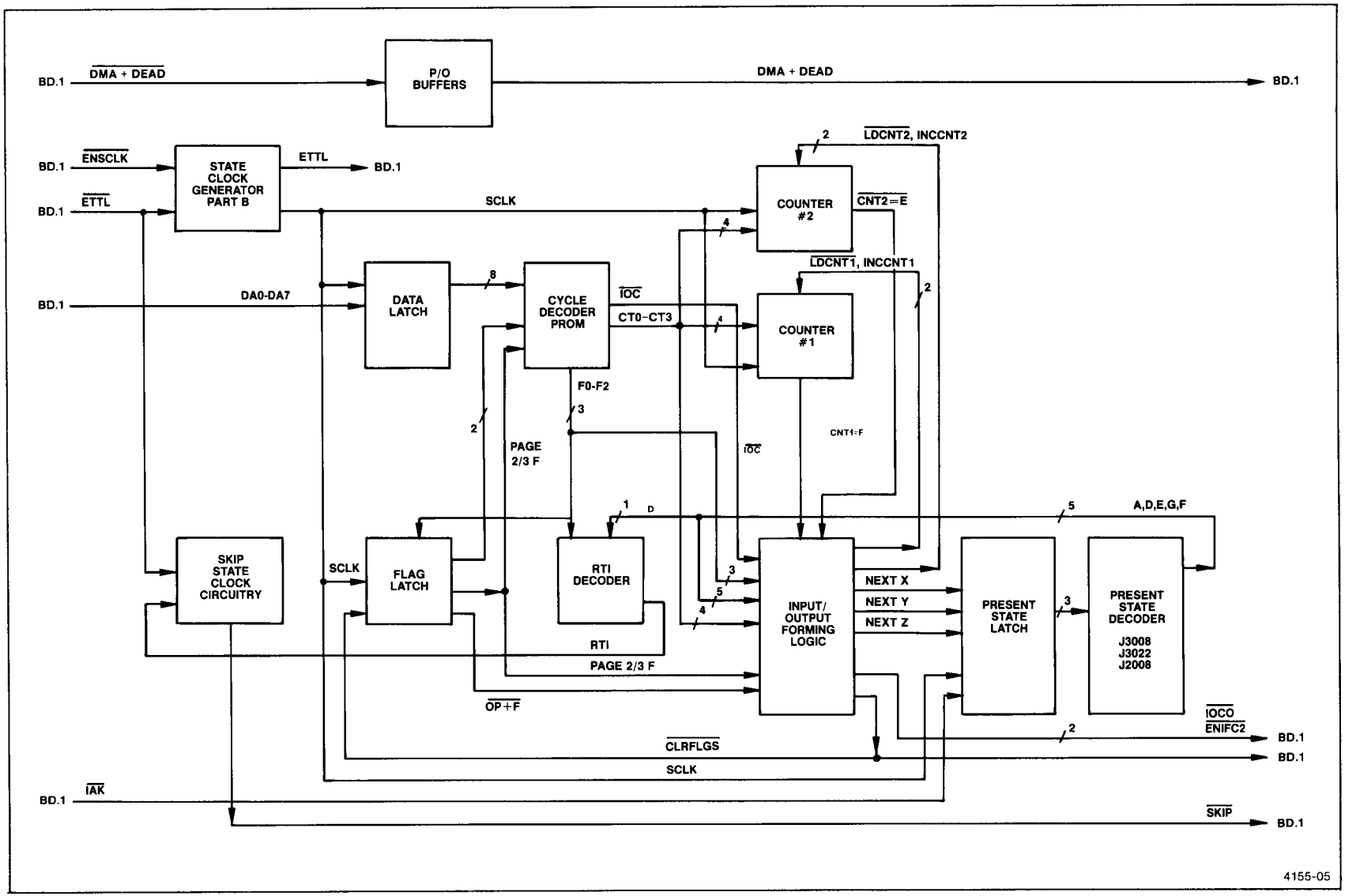


Figure 4-3. Board A2 block diagram.

BOARD 2 DETAILED CIRCUIT DESCRIPTIONS

OVERVIEW

The block diagram of Figure 4-3 shows this circuitry in functional blocks. Refer to Figure 4-3 for an overview of assembly 2 (board A2) and to aid in understanding the flow of signals to and from this board.

Schematic diagrams are provided in the Diagrams section of this manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

All components in the following board 2 descriptions are located on board A2. As components are referenced, the board number will be omitted from the reference (e.g., A2U3025 will be U3025). Components located on other boards will be referenced including their respective board numbers.

FETCH PREDICTOR OPERATION

On the basis that all 6809 microprocessor instructions require a known number of clock cycles in which to execute, the number of clock cycles until the next opcode fetch may be determined from the current instruction.

The 6809 Fetch Predictor can decode up to three consecutive bytes to determine the number of clock cycles required to execute an instruction, in order to determine how long to wait before labeling the next data bus read as an opcode fetch.

When the 6809 encounters a 1 byte instruction, it does a pre-fetch of the next byte as normal. If the 6809 was executing a 1 byte instruction, the pre-fetched byte will be discarded. These discarded pre-fetches will appear as READ cycles on the acquisition memory display (Absolute or Mnemonic).

Instruction types have been categorized, according to the number of bytes to be decoded, so the total number of clock cycles per instruction may be defined. Refer to Table 4-2. The type of instruction decoded combined with various input variables, determines the correct path through the fetch predictor state machine.

Table 4-2
NUMBER OF BYTES DECODED PER OPCODE

INSTRUCTION TYPE	NUMBER OF BYTES REQUIRED TO DETERMINE # OF CLOCKS FOR INSTRUCTION
Regular	1
Regular+	2
RTI	1*
PUL	2
Page 2	2
Page 3	2
Page 2+	3
Page 3+	3

*=Plus E bit of the Condition Code Register pulled from the stack.

Decoding of the first byte of an opcode determines whether or not subsequent bytes need to be decoded. It determines the instruction type , and for regular type instructions, defines the total number of clock cycles per instruction. For multiple byte instructions, the first byte defines some minimum number of clock cycles which must be added to a variable number of clock cycles (determined by decoding subsequent bytes). Storage of the number of cycles is afforded by two presettable counters (U1050 and U1060), whose primary job is to internally track the number of clock cycles required by the 6809 to execute any given instruction. Once each counter has in turn incremented to 15, the state machine predicts a fetch. The following clock cycle should be a 6809 fetch. Since the fetch predictor anticipates the fetch in time for the clock edge which latches it into the 7D02, the corresponding memory read can duly be labeled as a fetch in the aquisition memory. This information may also be used for triggering and data qualification.

Fetch Predictor Flow Chart

The 6809 Fetch Predictor Flow Chart should aid in understanding the 6809 Fetch Predictor. As shown in the flow chart, IAK(L) (Interrupt Acknowledge) provides a convenient method of synchronizing the fetch predictor to the 6809 microprocessor. IAK(L), provided by the 6809, is generated in response to a Reset, an NMI(L), SWI, SWI2, SWI3, and, if their corresponding mask bits are not set, an IRQ(L) or FIRQ(L). Since the fetch of the first instruction of an interrupt service routine always follows 3 cycles after the detection of IAK(L), the state machine always jumps to state A. Refer to Figure 4-4. A reset and its corresponding IAK(L) can occur when the state machine is in any

state; therefore, IAK(L) is tested for in all states. Note that although it is only necessary to latch the data bus in states D or F, depending upon certain input variables, it is latched in every state as a matter of convenient implementation. If an Illegal Opcode (IOC) is decoded in states D or F, the state machine returns to state D and attempts to re-synchronize.

The following describes the cases in which the state machine does not clock.

- Writes. By not clocking on writes, the number of cycles to time-out is reduced, particularly for stack write operations. In addition, it is no longer necessary to distinguish between IRQ(L) and FIRQ(L) for example, since from the standpoint of the number of cycles for their execution, they differ only in the number of stack writes.

- VMA. By not clocking on invalid memory address cycles, the number of cycles to time-out is reduced, and secondly, it is no longer necessary to know whether or not the branch, depicted by the ADDRESS BUS CYCLE-BY-CYCLE PERFORMANCE figure in the MC6809 Advance Information (Motorola,1980), was taken.

- Dead, DMA, or Sync Acknowledge cycles. By not clocking the state machine on Dead, DMA, or Sync Acknowledge cycles, the number of those cycles becomes transparent to the state machine. Consequently, the fetch that would have been predicted for the next cycle following the completion of the current instruction is inhibited until immediately following the completion of any number of Dead, DMA, or Sync Acknowledge cycles.

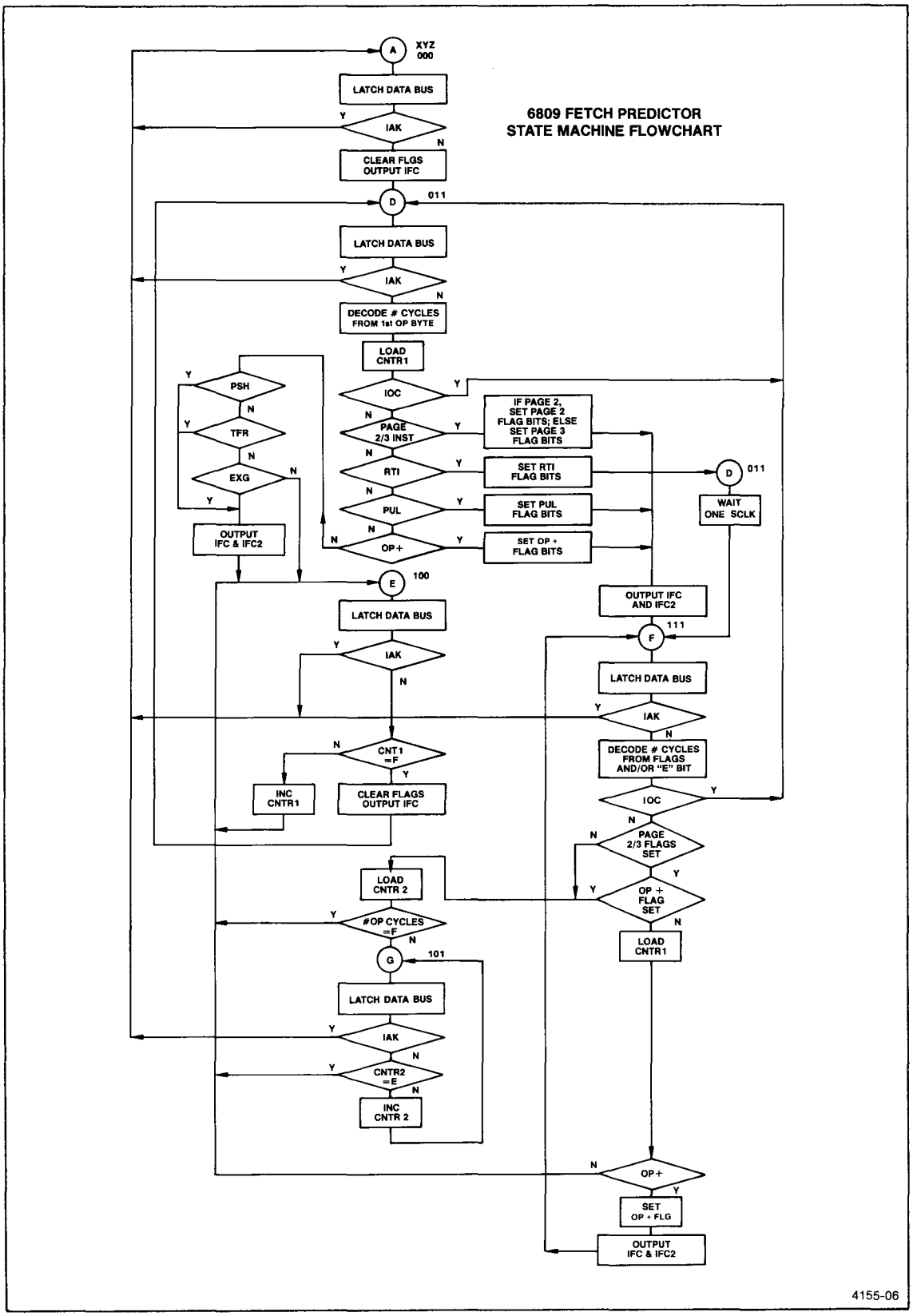


Figure 4-4. 6809 fetch predictor state machine flow chart.

Regular Instructions

For a Regular single byte opcode, the number of cycles is decoded in state D and loaded into counter 1. If the instruction is a two cycle instruction (the shortest there is), an F is loaded into counter 1; otherwise the complement of the number of cycles to time-out, minus 2, is loaded into counter 1. Assuming the opcode detected was not illegal, the next state becomes E. If counter 1 equals F, the Instruction Fetch Cycle IFC(L) line will be asserted and the next state will be D. Otherwise, counter 1 will be incremented to F, taking as many cycles as is necessary to time-out prior to issuing the IFC(L).

Regular+ Instructions

A Regular+ instruction has two bytes to be decoded. In state D , the first byte is decoded and loaded into counter 1. Then the Opcode Plus flag is set, and IFC(L) and IFC+IFC2(L) (subsequent fetch bytes) are asserted prior to progressing to state F. Since the Opcode Plus flag bits are fed back into the higher order address lines of the Cycle Decoder PROM, a new decoding table is addressed for decoding the second byte. Because the Opcode Plus flag is already set, the state machine branches to load counter 2 and then progresses to state G, if the number of opcode cycles is not equal to F. The reason for testing if the number of opcode cycles is equal to F is to minimize the time overhead of the state machine so as to not exceed the number of cycles of the shortest 2 byte instruction. In state G, counter 2 is incremented for as many cycles as is necessary to reach E, whereupon the state machine proceeds to state E. Again, counter 1 is incremented to F and IFC(L) is asserted prior to returning to state D.

Page 2 Or Page 3 Instructions

For these types of instructions, the first byte serves primarily to indicate that a second byte needs to be decoded. Although counter 1 is loaded in state D, this value is ignored. The Page 2 or Page 3 flag bits are set while IFC(L) and IFC+IFC2(L) are asserted prior to state F. Again a new table is addressed due to the set flag bits. Since these flag bits are set, and the Opcode Plus flag bit is not, counter 1 is reloaded with a value from the second table. Because this is not an Opcode Plus (Regular+) instruction, the state machine progresses to state E and increments counter 1 to F as before.

Page 2+ Or Page 3+ Instructions

These types of instructions require decoding of 3 bytes. The first byte indicates only that it is a Page 2 or Page 3 instruction and correspondingly sets the Page 2 or Page 3 flag bits. Again counter 1 is set and ignored in state D. The cycle decoder table, addressed by the Page 2 or Page 3 flag bits in state F, is loaded into counter 1 since the Opcode Plus flag is not set. The second byte decoded, however, indicates that this instruction is also an Opcode Plus type and consequently sets the Opcode Plus flag prior to returning to state F. A third cycle decoder table is now addressed, and its output value is loaded into counter 2 since the Opcode Plus flag bit is now set in addition to the Page 2 or Page 3 flag bits. Again, counter 2 is incremented to E in state G, following which counter 1 is incremented to F in state E. IFC(L) is asserted as before.

RTI Instruction

The number of cycles required for an RTI instruction is totally dependent on whether or not the E bit of the stacked condition code register is set. In state D, counter 1 will be loaded with the number of cycles corresponding to the E bit not set, and the RTI flag bits will be set prior to progressing to state F. In state F, a new cycle decoder table is addressed as a function of the RTI flag bits, and the condition code is pulled off the stack and input on the eight lower address lines of the decoder PROM. Consequently, the E bit of the condition code register addresses that portion of the decoder table containing the correct number of additional cycles required when the E bit is set. This number is loaded into counter 2 because the Page 2 and Page 3 flag bits are not set. In states G and E, counters 2 and 1 are incremented to their terminal values as before, prior to outputting IFC(L).

PUL Instruction

PUL type instructions load counter 1 and set the Pul flag bits in state D. In state F, the Pul operand in combination with the Pul flag bits, address the proper value to be loaded into counter 2. States G and E follow as before. A Pul Nothing instruction is a valid opcode requiring 3 cycles.

STATE CLOCK GENERATOR PART B

The State Clock Generator Part B produces the SCLK signal used throughout the Fetch Predictor circuitry.

When the State Clock Generator Part A sends ENSCLK(L) low, and the rising edge of ETTL(L) clocks U3030A, the SCLK signal goes active high. This high at U3050A-2 remains until ETTL(L) returns

low, causing a high on pins 1 and 2 of U3050A. U3050A pin 3 goes low, setting the flip-flop and returning SCLK to the low state. The SCLK signal remains low unless the ENSCLK(L) signal is still asserted at the next rising edge of ETTL(L). SCLK pulses will be output until ENSCLK(L) returns high.

DATA LATCH

The Data Latch accepts 8-bit opcodes from the microprocessor data bus and latches them for use by the Cycle Decoder PROM. The inputs, DA0-DA7, are latched on the rising edge of the SCLK signal. Note that the latched data bus values have been inverted by A1U4025.

CYCLE DECODER PROM

The Cycle Decoder PROM is a 2Kx8 EPROM containing seven decoder tables. The tables indicate the number of clock cycles each 6809 instruction takes for execution.

Signal lines from the Data Latch U3060 carry the latched 8-bit opcode to be decoded by the PROM. The decoded information on the outputs CT0-CT3 tells Counter 1 and Counter 2 what their increment values will be. The counters are loaded with the complement of the number of cycles to delay, and incremented to E or F.

The F0-F2 lines carry the conditions of various flag bits to the Flag Latch. Once latched, the information is fed back into the Cycle Decoder PROM. This information points to one of several decoder tables used to decode subsequent bytes of the current instruction. Refer to Table 4-3.

The IOC(L) (Illegal Opcode) signal line is an output from the Cycle Decoder PROM that indicates the last opcode decoded was an illegal opcode. This signal is asserted low as the IOCO(L) line to the logic analyzer, but inverted high in the firmware for the screen display.

FLAG LATCH

The Flag Latch, U2070, latches the conditions on lines F0-F2 from the Cycle Decoder PROM. These conditions are clocked to the outputs of the latch on the rising edge of SCLK. The outputs connect to the Input/Output Forming Logic and serve as input addresses for the Cycle Decoder PROM. The PROM uses these addressing inputs to point to 1 of several different decoder tables within the PROM. These tables aid in decoding subsequent bytes of the current instruction. Refer to Table 4-3.

Table 4-3
CYCLE DECODER PROM FLAG DEFINITIONS

TABLE	M.S.NIBBLE	IOC(L) F3	OP+ A10 F2	PAGE 2/3 A9 F1	A8 F0	OPCODE TYPE
	0	0	0	0	0	IOC (L)
	1	0	0	0	1	IOC (L)
	2	0	0	1	0	IOC (L)
	3	0	0	1	1	IOC (L)
	4	0	1	0	0	IOC (L)
	5	0	1	0	1	IOC (L)
	6	0	1	1	0	IOC (L)
	7	0	1	1	1	IOC (L)
0	8	1	0	0	0	REG
1	9	1	0	0	1	RTI
2	A	1	0	1	0	PAGE 2
3	B	1	0	1	1	PAGE 3
4	C	1	1	0	0	PUL
5	D	1	1	0	1	OP+
6	E	1	1	1	0	NOT USED
7	F	1	1	1	1	PSH

COUNTER 1 AND COUNTER 2

Counters 1 and 2 track the number of cycles to wait before indicating that the next instruction cycle is a fetch. To signal this event, counter 1 generates CNT1=F and counter 2 generates CNT2=E(L). These active low signals are used by the Input/Output Forming Logic.

Signal lines CT0-CT3 from the Cycle Decoder PROM carry information indicating the number of cycles the current instruction will take before the next instruction is executed. The LDCNT1(L) and LDCNT2(L) (load counters 1 and 2) signals latch the CT0-CT3 information. SCLK increments the counters until the terminal count is reached when CNT1=F and CNT2=E(L) go low.

SKIP STATE CLOCK CIRCUITRY

The Skip State Clock Circuitry generates the SKIP(L) signal for the State Clock Generator Part A, which disables the generation of the SCLK signal for 1 cycle. The cycle following the skipped cycle corresponds to the condition code being pulled off the stack and placed on the data bus.

When RTI is unasserted (low), the inputs to U3050B-4 and 5 are low and high (respectively). If a Return from Interrupt occurs,

the RTI Decoder sends the RTI line high. This momentary high at U3050B-4 sends SKIP(L) active low. This low exists until the rising edge of ETTL(L) clocks the high RTI signal through the flip-flop. The pin 8 output goes low, causing U3050B to send SKIP(L) inactive high. Refer to Figure 4-5.

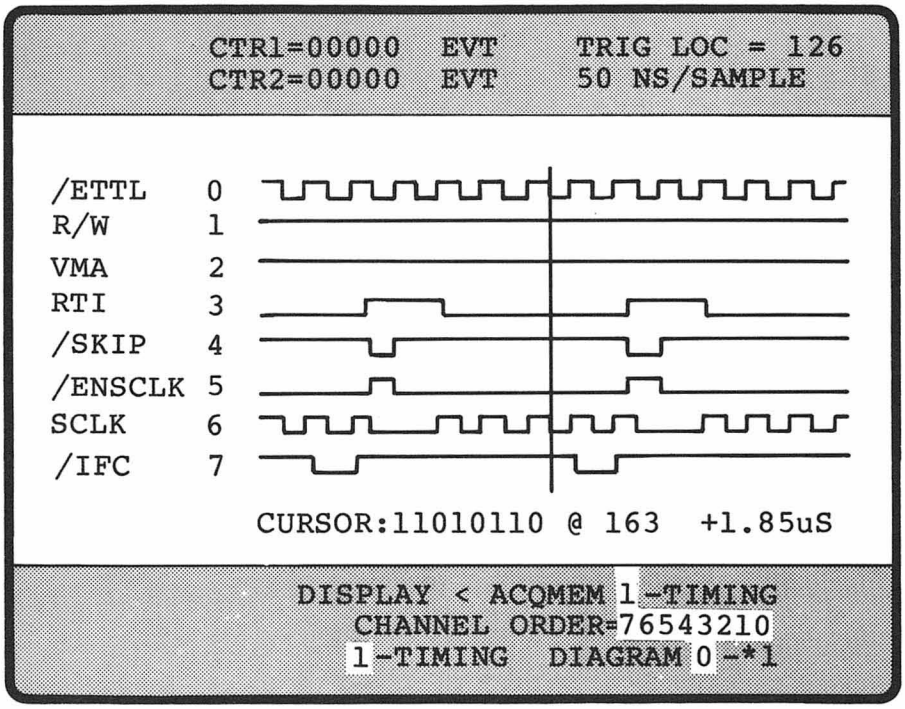


Figure 4-5. Skip SCLK on RTI.

RTI DECODER

The RTI Decoder circuitry supplies the RTI signal to the Skip State Clock Circuitry. This signal indicates when a Return from Interrupt (RTI) instruction occurs.

When the inputs to U3050C (D and F0) are high, the output pin 8 goes low. This low, NORed with the low F1 and F2 signals, sends the output U2040B-6 high. This is the active state of the RTI signal.

PRESENT STATE LATCH

The Q outputs of the Present State Latch (U3010) hold the current state of the Fetch Predictor State Machine. With the rising edge of SCLK, the NEXT X, NEXT Y, and NEXT Z values get loaded in and become the new present state. When IAK(L) (Interrupt Acknowledge) goes low, the latched values are cleared, forcing the

state machine back to state A. Since IAK(L) can be asserted while the state machine is in any of its states, this provides a method of re-synchronizing the Fetch Predictor (a fetch will always follow two cycles after an IAK(L)). Refer to Figure 4-6.

PRESENT STATE DECODER

The Present State Decoder (U3020) is a 3 line to 8 line decoder which provides individual output lines corresponding to each state of the state machine. These outputs simplify the Input/ Output Forming Logic. Jumpers J3008, J3022, and J2008 provide a way to interrupt the state machine loop in order to facilitate signature analysis. The jumpers also serve as convenient test points.

INPUT/OUTPUT FORMING LOGIC

The Input Forming Logic generates the Next State from a logical combination of the Present State and input variables such as CNT1=F, CNT2=E(L), PAGE 2/3 Flag, OP+ Flag(L), OP+, IOC(L), and # OP CYCLES=F(L).

The Output Forming Logic generates outputs from the state machine by using a logical combination of the Present State and the input variables previously listed. The outputs include LD CNT1(L), INC CNT1, LD CNT2(L), INC CNT2, IOCO(L), ENIFC2(L), and CLRFLGS(L).

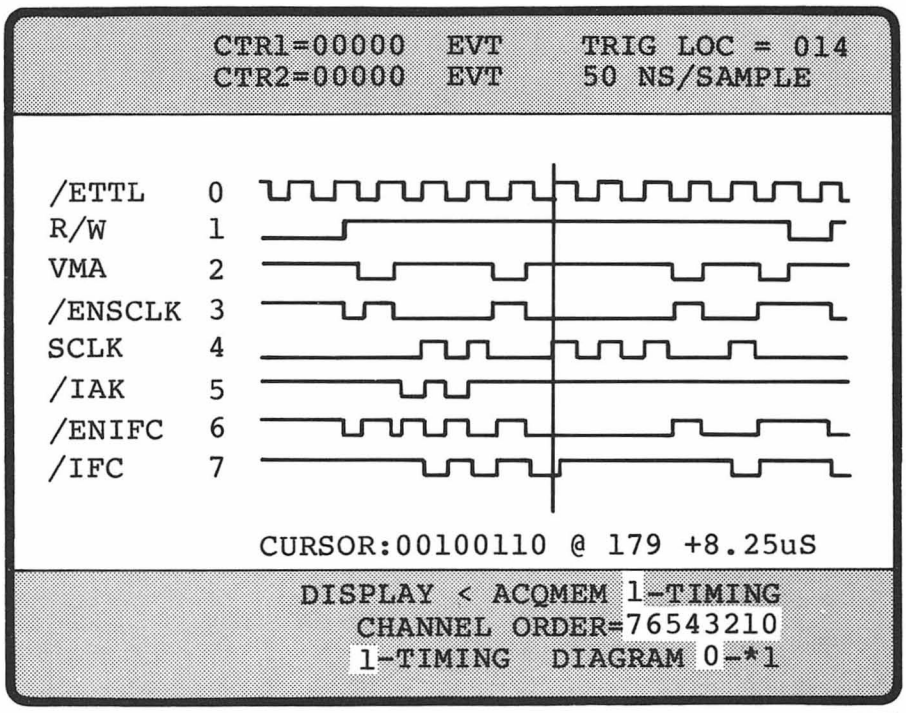


Figure 4-6. End of SWI instruction; showing synchronizing on IAK and generating a fetch.

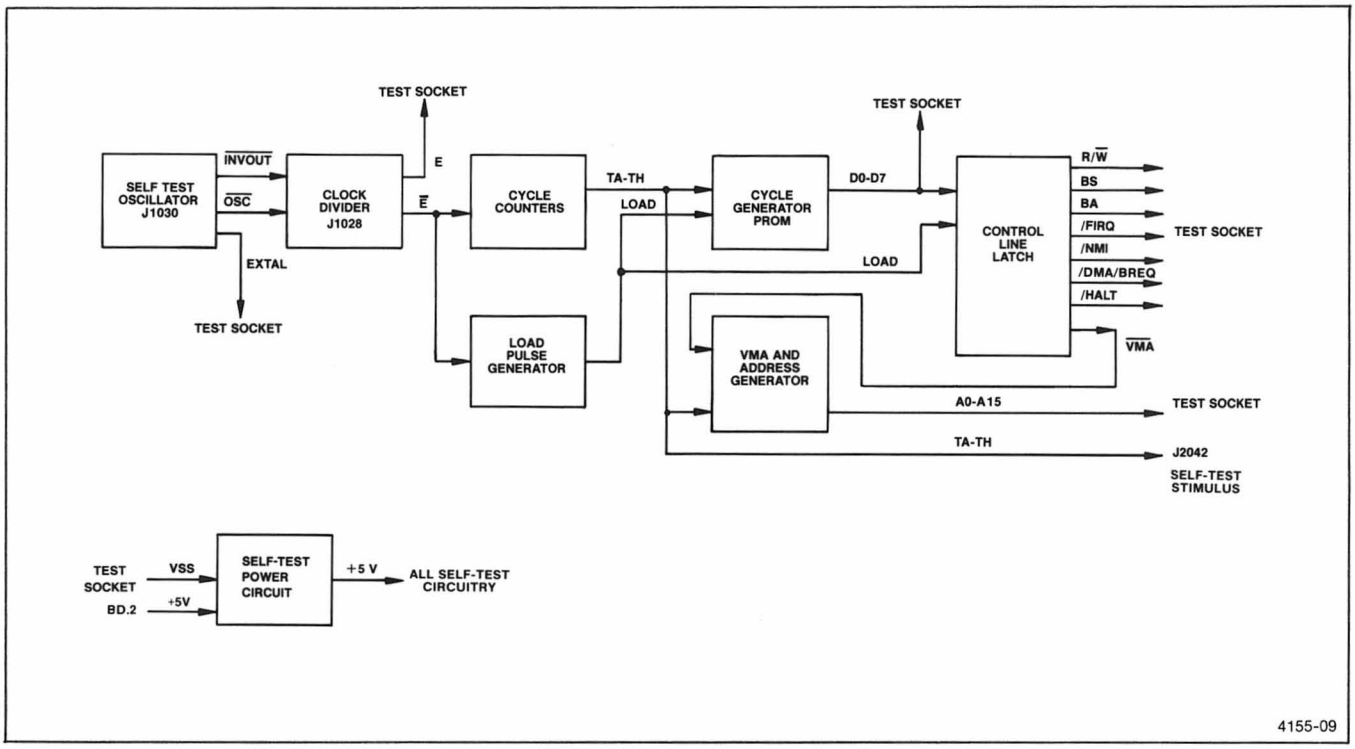


Figure 4-7. Board A3 block diagram.

BOARD 3 DETAILED CIRCUIT DESCRIPTIONS

OVERVIEW

The block diagram of Figure 4-7 shows this circuitry in functional blocks. Refer to Figure 4-7 for an overview of board 3 (assembly A3) and to aid in understanding the flow of signals to and from this board.

Schematic diagrams are provided in the Diagrams section of this manual and are keyed to their respective circuit descriptions by numbered diamond symbols. For increased understanding of the detailed circuit descriptions, refer to both the appropriate schematic diagram and functional block diagram.

All components in the following descriptions are located on board A3. As components are referenced, the board numbers will be omitted from the reference (e.g., A3U1031 will be U1031). Components located on other boards will be referenced including their respective board numbers.

SELF-TEST OSCILLATOR

The Self-Test Oscillator circuitry produces the oscillator signal (at approximately 4.25 MHz), which is inverted by U1029D and becomes the OSC signal. The OSC signal is selected for output in either mode of operation (NORM or TEST) by the jumper J1030.

In the NORM mode of operation (shorting pins 1 and 2 of J1030), the OSC signal passes through the 40-pin test socket to the 40-pin microprocessor plug. Within the 40-pin plug hybrid, the signal becomes INVOUT(L). This signal serves as an input to the Clock Divider circuitry.

In the TEST mode of operation (shorting pins 2 and 3 of J1030), the OSC signal is fed directly to the Clock Divider circuitry. This bypass of the clock oscillator circuitry (in the 40-pin plug hybrid) is useful for troubleshooting purposes. Refer to the Maintenance and Troubleshooting section for more information.

NOTE

The jumper J1030 should only be used in conjunction with jumper J1028.

CLOCK DIVIDER CIRCUITRY

The Clock Divider Circuitry supplies the E(L) clock signal for use by the Cycle Counters circuitry and the Load Pulse Generator.

This circuitry also generates the E clock signal which serves as an output at pin 34 of the 40-pin microprocessor plug. These two signals, E and E(L), are derived from either of the two inputs INVOUT(L) or OSC.

The two inputs, INVOUT(L) and OSC, are selectable by the jumper J1028. The INVOUT(L) signal is used in the NORM position for operation as normal. The OSC signal is used in the TEST position when a bypass of the circuitry in the 40-pin microprocessor plug is desired. For more information, refer to the Maintenance and Troubleshooting section.

The first input signal, INVOUT(L), comes from the clock oscillator circuitry found in the end of the 40-pin microprocessor plug. The INVOUT(L) signal, inverted in A1U7035H and re-inverted in U1029A, is available at pin 1 (labeled NORM) of J1028.

The second input signal, OSC, comes from the Self-Test Oscillator circuitry. This signal is available at pin 3 (labeled TEST) of J1028.

The rising edge of the selected signal clocks the flip-flop U1025B. The pin 8 output of this divide-by 2 circuit is the E clock signal. This signal is inverted in U1029C for the E(L) clock output. The output of the Clock Divider has a 50% duty cycle.

NOTE

The jumper J1028 should be used in conjunction with jumper J1030.

SELF-TEST POWER CIRCUIT

The Self-Test Power Circuit supplies the necessary +5V to the self-test circuitry, but only when the 40-pin plug is installed in the 40-pin test socket. The circuit, designed to reduce power consumption while the self-test circuitry is not being used, is activated when the ground (GND) at pin 1 of the test socket is connected to pin 1 of the 40-pin plug.

CYCLE COUNTERS

The Cycle Counters circuitry supplies the Cycle Generator PROM with a sequential count pattern on lines TA-TH. The count pattern is generated by a pair of synchronous 4-bit counters.

On the first rising edge of E(L) clock, U3025 will send pin 14, TA, high. On each successive rising edge of E(L), the next binary combination will be output from U3025 on TB-TD. When the

terminal count (15) is reached, the ripple carry output will enable the second 4-bit counter. U2029 will output, on the next rising edge of E(L), a high on the LSB output, TE. For each terminal count that U3025 reaches, U2029 will be incremented by 1. The overall effect is that the Cycle Counters circuitry steps through a 256 cycle count on lines TA-TH.

The count lines TA-TH also connect to the VMA and Address Generator and the timing option pins, J2042, located under the plastic door on the bottom of the personality module case.

CYCLE GENERATOR PROM

The Cycle Generator PROM generates the control line values and the data values D0-D7 for the PM 111 40-pin test socket. These data values are used in the PM 111 self-test mode of operation as simulated processor input data.

The inputs to the PROM, U3029, are TA-TH from the Cycle Counters circuitry. On the positive transition of the LOAD pulse, the data (according to the TA-TH inputs) is latched on the D0-D7 outputs.

CONTROL LINE LATCH

The Control Line Latch stores the control line signals from the Cycle Generator PROM and makes them available to the 40-pin test socket. The control lines R/W(L), BS, BA, FIRQ(L), NMI(L), DMA/BREQ(L), and HALT(L) are used in the PM 111 self-test mode of operation. A separate output from this circuit, VMA(L), is an input to the VMA and Address Generator circuitry.

The data lines D0-D7 serve as inputs to the Control Line Latch. On the positive transition of the LOAD signal, the data latched becomes the control line output signals.

LOAD PULSE GENERATOR

The LOAD Pulse Generator supplies a LOAD pulse to the Cycle Generator PROM and the Control Line Latch. The LOAD pulse is low for approximately the first 115 ns of the E clock signal, in order to provide adequate PROM access time. During this low time, the even bytes of the PROM are addressed. When the LOAD pulse goes high, the even byte data is latched and the odd byte in the PROM is addressed. With this type of addressing, both even and odd bytes can be addressed within 1 E clock cycle.

This technique effectively converts the 512x8 PROM into 256x16, providing 16 simultaneous channels of stimulus plus address lines required to emulate a 6809 SUT.

The even bytes in the PROM contain information defining the processor status and control lines. The odd bytes contain data bus values, i.e., opcodes and operands.

For explanation purposes, consider that U1029B-5 is low. The resulting high at the output pin 6 (connected to U1025A-1), the high at U1025A-4, and the rising edge of the E(L) clock signal will send U1025A output pin 6 low. This low on pin 1 of the Cycle Generator PROM will cause the PROM to address even bytes. The high on the Q output charges the capacitor at a calculated RC time constant. When U1029B-5 is high and pin 4 is still high, the output of the NAND gate goes low. This low signal resets the flip-flop, sending the LOAD pulse high. The LOAD pulse will remain high until the next rising edge of E(L) occurs.

VMA AND ADDRESS GENERATOR

The VMA and Address Generator circuitry supplies the address values for pins 8-23 (A0-A15 respectively) of the PM 111 40-pin test socket. These address values are used in the PM 111 self-test mode as input addresses. This circuitry is also capable of outputting the address FFFF on the address bus when an invalid (not VMA) cycle is indicated.

When the VMA(L) line to U3035 is low, the inputs TA-TH are buffered and output as A0-A15. Note that address line A3 also connects to A8 and A11; A4 to A12; A5 to A9, A10, and A13; A6 to A14; and A7 to A15. When the VMA(L) is high, U3035 tri-states the TA-TH outputs and the pull-up resistor network pulls the output lines high. All address lines high (the address FFFF in combination with R/W(L)=1 and BS=0) indicates that an invalid memory cycle is present.

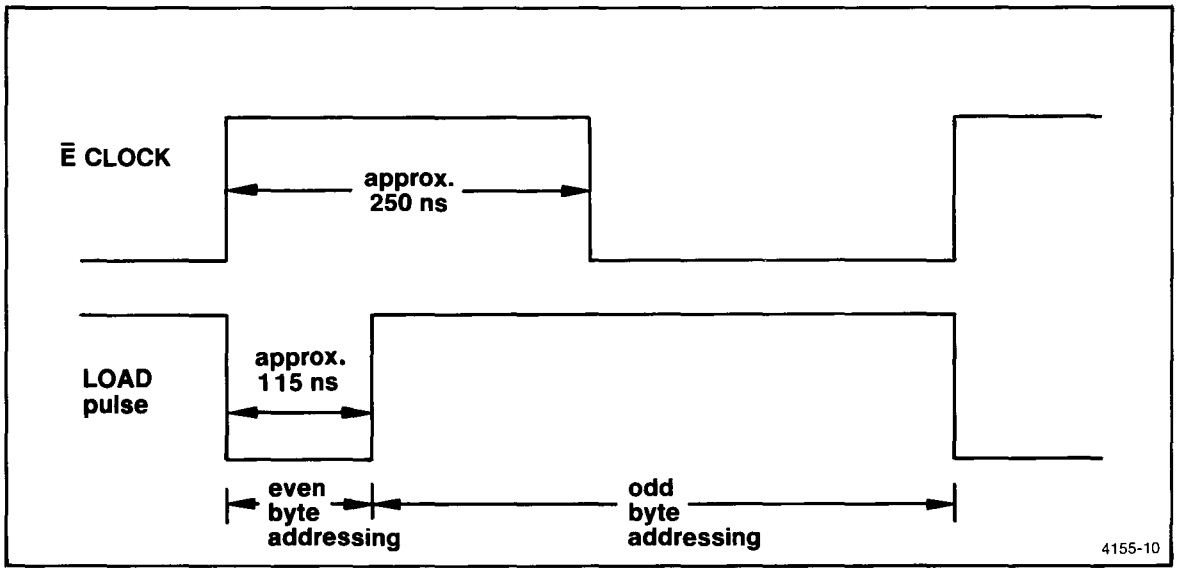


Figure 4-8. Load Pulse Generator.

PERFORMANCE CHECK

OVERVIEW

The procedures which follow provide a method of checking the operation and performance requirements of the PM 111 Personality Module. It is assumed that the 7D02 Logic Analyzer has already passed its performance check according to the 7D02 Service Manual Performance Check section. The Performance Check test procedures should be performed in sequence.

If verification of only the listed Performance Requirements in the Specification section is necessary, complete the Performance Checks, Part 3, located in this section. If the personality module is suspected of being faulty, complete both the Diagnostic Monitor, Part 1 and 2, and the Performance Checks, Part 3.

EQUIPMENT LIST

The test equipment listed in Table 5-1 is required for the performance check of the PM 111 Personality Module. Detailed operating instructions for use of some of the equipment are included in the appropriate test equipment manuals.

Table 5-1
REQUIRED TEST EQUIPMENT

DESCRIPTION	ITEM (W/Tektronix No.)
Logic Analyzer	TEKTRONIX 7D02 Logic Analyzer w/Option 02 (Timing Option)
Timing Option Probe	TEKTRONIX P6451 Data Acquisition Probe
Mainframe	TEKTRONIX 7603 Oscilloscope; 100 MHz (or equivalent 7000 series mainframe)
Test Oscilloscope	TEKTRONIX 7603 Oscilloscope; 100 MHz (or equivalent 100 MHz oscilloscope)
Timebase Plug-in	TEKTRONIX 7B53A; 5 ns/div (required with 7000 series test oscilloscope)
Vertical Plug-in	TEKTRONIX 7A18; 75 MHz (required with 7000 series test oscilloscope)

Table 5-1 (cont)
REQUIRED TEST EQUIPMENT

Oscilloscope Probes (2 required)	TEKTRONIX P6105; 100 MHz
TM 500 Mainframe	TEKTRONIX TM 503 Mainframe
Pulse Generator	TEKTRONIX PG 502 Pulse Generator
Pulse Generator	TEKTRONIX PG 508 Pulse Generator
Coaxial Cable (10 in.)	50 ohm Coaxial Cable; TEKTRONIX P/N 012-0208-00
40 Pin Wire Wrap Socket	Socket; TEKTRONIX P/N 136-0622-00
BNC to Dual Lead Adapter	BNC Female to EZ ball; TEKTRONIX P/N 013-0076-01
BNC male to BNC male Adapters (2 required)	Adapter; TEKTRONIX P/N 103-0029-00
Flat Blade Screwdriver	Slot Screwdriver; Tektronix P/N 003-0199-00
Allen Wrench	3/32" Allen Wrench; Tektronix P/N 003-0108-00

Table 5-2
OPTIONAL TEST EQUIPMENT

DESCRIPTION	ITEM (W/Tektronix No.)
40-pin DIP Socket	Socket; Tektronix P/N 136-0623-00
Female Adapter	Adapter; Tektronix P/N 380-0647-00
Low Profile DIP Clip Adapter	DIP Clip; Tektronix P/N 015-0339-00
Harmonica Cable	Cable Set; Tektronix P/N 012-0800-00
Square Pin Row	Square Pin Row; Tektronix P/N 131-1614-00

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PRELIMINARY SETUP

CAUTION

Always be certain to turn off the mainframe power before connecting or disconnecting the personality module to avoid damage to any of the instruments.

1. Turn off the mainframe power to the logic analyzer at the oscilloscope mainframe.

2. Insert the PM 111 logic analyzer cable plug labeled PERSONALITY MODULE-PM 100 SERIES into the receptacle labeled the same on the front of the 7D02.

3. Remove the plastic door on the bottom of the personality module by inserting a screwdriver into the slot provided and gently prying up the cover.

4. Insert the personality module 40-pin plug into the test socket located under the door. Ensure the plug is inserted correctly, with pin 1 of the plug at pin 1 of the test socket. Refer to Figure 5-1 for correct connection.

4155-11

Figure 5-1. PM 111 in the self-test configuration.

5. Using Table 5-3, connect the P6451 Timing Option Probe to the row of pins (J2042) located under the door on the bottom of the module case.

NOTE

If the optional harmonica cable (Tektronix P/N 012-0800-00) is used with the P6451 Timing Option Probe, the wires from the P6451 should be connected to the harmonica cable with the proper sized square pins (Tektronix P/N 131-1614-00). The harmonica cable can then be used as a convenient method of connection to the timing option pins at A3J2042.

Table 5-3
P6451 TIMING OPTION CONNECTION

COLOR CODE	WIRE #	J2042 PIN
White	GND	GND
Black	0	TA
Brown	1	TB
Red	2	TC
Orange	3	TD
Yellow	4	TE
Green	5	TF
Blue	6	TG
Violet	7	TH

DIAGNOSTIC MONITOR, PART 1

OVERVIEW

The following describes the procedures needed to perform the 7D02 Diagnostic Module tests for the personality module and timing option. These tests confirm the 7D02's ability to do the following:

- Read and recognize pre-programmed word recognizers.
- Compare the data in the personality module EPROM to the logic information in the 7D02.
- Fill the acquisition memory upon recognition of the appropriate word recognizers.
- Compare acquisition memory checksums to checksum stored in the personality module EPROM.
- Display error codes.

DIAGNOSTIC MODULE 9 (PER. MOD.-SYS)

To run the subtests of diagnostic module 9, use the following procedure.

1. Turn on the mainframe power and depress any 7D02 front panel key (except X or START) within two seconds. Keep the key depressed for at least five seconds to simulate a keyboard failure. Simulating a keyboard failure allows entry into the DIAGNOSTIC MONITOR.
2. Press the X key to get the DIAGNOSTIC MONITOR menu.
3. Press the 9 key to test the PER. MOD.- SYSTEM (personality module system).
4. Press the E key to select ENABLE LOOPING.
5. Press the START key to run Test 1.
6. A number such as 1351-XX (the part number of the personality EPROM), is associated with Test 1 and is normal.
7. Wait at least 5 seconds and press the START key to run the next test.
8. Repeat part 7 until all of the tests have been completed.
9. A number associated with any test other than Test 1 is a failure. A number associated with any PASS message indicates a transient failure. A number associated with a FAIL message indicates a solid failure. Write down all numbers associated with any PASS or FAIL messages. Refer to Diagnostic Module 9 PER. MOD.-SYSTEM, in the Maintenance and Troubleshooting section, and Troubleshooting Error List #1, if any failures are noted.
10. Press the START key, then X key to return to the menu.

DIAGNOSTIC MODULE B (TIMING OPTION)

To run the subtests of diagnostic module B, use the following procedure.

1. If the 7D02 Diagnostic Module 9 PER. MOD.-SYSTEM was previously run, continue to part 2. If not, perform parts 1 and 2 of the PER. MOD.-SYSTEM test.

2. Press the B key to run the TIMING OPTION module.

3. Press the E key to ENABLE LOOPING.

4. Press the START key.

5. Wait for five seconds in between all tests. Using the START key, run the remaining two tests.

6. A number associated with any test is a failure. A number associated with a PASS message indicates a transient failure. A number associated with a FAIL message indicates a solid failure. Write down all numbers associated with any PASS or FAIL messages. Refer to 7D02 Diagnostic Module B TIMING OPTION, in the Maintenance and Troubleshooting section, and Troubleshooting Error List #2 if any failures are noted.

DIAGNOSTIC MONITOR, PART 2

The following checks are not part of the Diagnostic Monitor menu and should be considered extended diagnostic checks.

SELF TEST ACQUISITION CHECK

The following check allows you to acquire a listing of the self-test program and compare it to Figure 5-2.

Enter the following program into the 7D02, making sure default clock qualification is changed to all X's (don't cares).

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=0000
1 FETCH1=X FETCH1+2=X R/W=X BA=X
1 INT=X INVAL.OP=X EXT.TRIG.IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
 END TEST 1
```

1. Press the 7D02 START key. The 7D02 should trigger on address 0000.

2. Using the DATA SCROLLING keys, compare the screen display (0-255) to the following Figure 5-2.

LOC	ADDR	OPERATION	INT	*CYCLE TYPE	*OPCODE (HEX)
000	F6F1	AA READ	0	HALT REQ	
001	FFFF	00 READ	0	HALT REQ, not VMA	
002	F6F3	FF READ	0	HALT REQ	
003	F6F4	FF READ	0	HALT REQ, DEAD	
004	F6F5	01 READ	0	HALT REQ, HALTED	
005	F6F6	23 READ	0	HALT REQ, HALTED	
006	F6F7	45 READ	0	HALTED	
007	FFF8	67 READ	0	DEAD	
008	FFF9	LDS ,U	0	PAGE 2+	10
009	FFFA	EE FETCH 2	0	OP+	
010	FFFB	C4 FETCH 2	0	INDEX	
011	FFFC	3C READ	0		
012	FFFD	3F READ	0		
013	FFFE	6C READ	0		
014	FFFF	FF READ	0	not VMA	
---	T0000	NEG @03	0		00
016	0001	03 READ	0		
017	FFFF	00 READ	0	not VMA	
018	0003	FF READ	0		
019	FFFF	00 READ	0	not VMA	
020	0005	01 WRITE	0		
021	0006	TST @09	0		0D
022	0007	09 READ	0		
023	FFFF	00 READ	0	not VMA	
024	0909	FF READ	0		
025	FFFF	00 READ	0	not VMA	
026	FFFF	00 READ	0	not VMA	
027	090C	JMP @0D	0		0E
028	090D	0D READ	0		
029	FFFF	00 READ	0	not VMA	
030	090F	LBRA 1014	0		16
031	1010	07 READ	0		
032	1011	02 READ	0		
033	FFFF	00 READ	0	not VMA	
034	FFFF	00 READ	0	not VMA	
035	1014	LBSR 191D	0		17
036	1015	09 READ	0		

*= These columns do not appear on the 7D02 screen.

LOC	ADDR	OPERATION		INT	*CYCLE TYPE	*OPCODE (HEX)
037	1016	06	READ	0		
038	FFFF	00	READ	0	not VMA	
039	FFFF	00	READ	0	not VMA	
040	1919	00	READ	0		
041	FFFF	00	READ	0	not VMA	
042	191B	19	WRITE	0		
043	191C	19	WRITE	0		
044	191D	DAA		0		19
045	191E	1A	READ	0		
046	191F	ORCC #03		0		1A
047	2620	03	READ	0		
048	2621	1F	READ	0		
049	2622	TFR A,B		0		1F
050	2623	89	FETCH 2	0		
051	FFFF	00	READ	0	not VMA	
052	FFFF	00	READ	0	not VMA	
053	FFFF	00	READ	0	not VMA	
054	FFFF	00	READ	0	not VMA	
055	2F28	BEQ 2F2B		0		27
056	2F29	01	READ	0		
057	FFFF	00	READ	0	not VMA	
058	2F2B	LEAX A,X		0	OP+	30
059	2F2C	86	FETCH 2	0	INDEX	
060	2F2D	00	READ	0		
061	FFFF	00	READ	0	not VMA	
062	FFFF	00	READ	0	not VMA	
063	3630	LEAX ,X		0	OP+	30
064	3631	84	FETCH 2	0	INDEX	
065	3632	00	READ	0		
066	FFFF	00	READ	0	not VMA	
067	3634	PSHS A		0		34
068	3635	02	FETCH 2	0		
069	FFFF	00	READ	0	not VMA	
070	FFFF	00	READ	0	not VMA	
071	3F38	C5	READ	0		
072	3F39	C3	WRITE	0		
073	3F3A	PULS Y		0		35
074	3F3B	20	FETCH 2	0		
075	FFFF	00	READ	0	not VMA	
076	FFFF	00	READ	0	not VMA	
077	3F3E	C5	READ	0		
078	3F3F	00	READ	0		
079	4040	00	READ	0		
080	4041	PULU		0	PULL NOTHING	37
081	4042	00	FETCH 2	0		
082	FFFF	00	READ	0	not VMA	
083	FFFF	00	READ	0	not VMA	
084	4045	BF	READ	0		

*=These columns do not appear on the 7D02 screen.

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LOC	ADDR	OPERATION		INT	*CYCLE TYPE	*OPCODE (HEX)
085	4046	PULU ALL		0		37
086	4047	FF	FETCH 2	0		
087	FFFF	00	READ	0	not VMA	
088	FFFF	00	READ	0	not VMA	
089	494A	BF	READ	0		
090	494B	6C	READ	0		
091	494C	5D	READ	0		
092	494D	26	READ	0		
093	494E	CF	READ	0		
094	494F	CF	READ	0		
095	5050	5F	READ	0		
096	5051	2A	READ	0		
097	5052	3D	READ	0		
098	5053	76	READ	0		
099	5054	CF	READ	0		
100	5055	47	READ	0		
101	5056	53	READ	0		
102	5057	RTI		0	SHORT RTI	3B
103	5958	00	READ	0		
104	5959	5F	READ	0	E BIT CLEAR IN CCR	
105	595A	84	READ	0		
106	595B	0D	READ	0		
107	595C	00	READ	0		
108	595D	RTI		0	LONG RTI	3B
109	595E	00	READ	0		
110	595F	80	READ	0	E BIT SET IN CCR	
111	6660	84	READ	0		
112	6661	0D	READ	0		
113	6662	00	READ	0		
114	6663	3B	READ	0		
115	6664	0A	READ	0		
116	6665	81	READ	0		
117	6666	F9	READ	0		
118	6667	7F	READ	0		
119	6F68	00	READ	0		
120	6F69	25	READ	0		
121	6F6A	44	READ	0		
122	6F6B	FD	READ	0		
123	6F6C	SWI		0		3F
124	6F6D	00	READ	0		
125	FFFF	00	READ	0	not VMA	
126	6F6F	06	WRITE	0		
127	7670	C0	WRITE	0		
128	7671	80	WRITE	0		
129	7672	CF	WRITE	0		
130	7673	F2	WRITE	0		
131	7674	F9	WRITE	0		
132	7675	00	WRITE	0		
133	7676	CF	WRITE	0		

*=These columns do not appear on the 7D02 screen.

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LOC	ADDR	OPERATION	INT	*CYCLE TYPE	*OPCODE (HEX)
134	7677	00 WRITE	0		
135	7F78	00 WRITE	0		
136	7F79	C3 WRITE	0		
137	7F7A	D9 WRITE	0		
138	FFFF	00 READ	0	not VMA	
139	7F7C	CF READ	0	INTERRUPT ACK. (IAK)	
140	7F7D	00 READ	0	INTERRUPT ACK. (IAK)	
141	FFFF	00 READ	0	not VMA	
142	7F7F	LSR 8083	0		74
143	8080	80 READ	0		
144	8081	83 READ	0		
145	FFFF	00 READ	0	not VMA	
146	8083	FF READ	0		
147	FFFF	00 READ	0	not VMA	
148	8085	7F WRITE	0		
149	8086	LDA #AA	0		86
150	8087	AA READ	0		
151	8988	CMPD #3C3C	0	PAGE 2	10
152	8989	83 FETCH 2	0		
153	898A	3C READ	0		
154	898B	3C READ	0		
155	FFFF	00 READ	0	not VMA	
156	898D	LDY B,X	0	PAGE 2+	10
157	898E	AE FETCH 2	0	OP+	
158	898F	85 FETCH 2	0	INDEX	
159	9090	3C READ	0		
160	FFFF	00 READ	0	not VMA	
161	9092	35 READ	0		
162	9093	20 READ	0		
163	9094	CMPU #853C	0	PAGE 3	11
164	9095	83 FETCH 2	0		
165	9096	85 READ	0		
166	9097	3C READ	0		
167	FFFF	00 READ	0	not VMA	11
168	9999	CMPS ,X+	0	PAGE 3+	11
169	999A	AC FETCH 2	0	OP+	
170	999B	80 FETCH 2	0	INDEX	
171	999C	3C READ	0		
172	FFFF	00 READ	0	not VMA	
173	FFFF	00 READ	0	not VMA	
174	999F	3C READ	0		
175	A6A0	35 READ	0		
176	FFFF	00 READ	0	not VMA	
177	A6A2	CWAI	0		3C
178	A6A3	AF READ	0		
179	A6A4	B0 READ	0		
180	FFFF	00 READ	0	not VMA	
181	A6A6	08 WRITE	0		
182	A6A7	C0 WRITE	0		

*=These columns do not appear on the 7D02 screen.

@

LOC	ADDR	OPERATION		INT	*CYCLE TYPE	*OPCODE (HEX)
183	AFA8	80	WRITE	0		
184	AFA9	CF	WRITE	0		
185	AFAA	F2	WRITE	0		
186	AFAB	F9	WRITE	0		
187	AFAC	07	WRITE	0		
188	AFAD	C0	WRITE	0		
189	AFAE	00	WRITE	0		
190	AFAF	00	WRITE	0		
191	B6B0	CA	WRITE	0		
192	B6B1	89	WRITE	0		
193	FFFF	00	READ	0	not VMA	
194	FFFF	00	READ	0	not VMA	
195	FFFF	00	READ	0	not VMA	
196	FFFF	00	READ	0	not VMA	
197	FFFF	00	READ	0	not VMA	
198	FFFF	00	READ	1	not VMA, FIRQ	
199	FFFF	00	READ	1	not VMA, FIRQ	
200	FFFF	00	READ	1	not VMA, FIRQ	
201	FFFF	00	READ	1	not VMA, FIRQ	
202	FFFF	00	READ	1	not VMA, FIRQ	
203	BFBC	BF	READ	1	IAK, FIRQ	
204	BFBD	BF	READ	1	IAK, FIRQ	
205	FFFF	00	READ	1	not VMA, FIRQ	
206	BFBF	NOP		1	FIRQ	12
207	C0C0	C0	READ	1	FIRQ	
208	C0C1	SUBB	#AA	1	FIRQ	C0
209	C0C2	AA	READ	0		
210	C0C3	SYNC		0		13
211	C0C4	CB	READ	0	PRE-FETCH	
212	C0C5	AA	READ	0	DEAD	
213	C0C6	55	WRITE	0	SYNC ACK	
214	C0C7	AA	READ	1	SYNC ACK, NMI	
215	C9C8	55	READ	1	SYNC ACK, NMI	
216	C9C9	AA	WRITE	1	SYNC ACK, NMI	
217	C9CA	55	WRITE	1	DEAD, NMI	
218	C9CB	ADDB	#CB	1	NMI	CB
219	C9CC	CB	READ	1	NMI	
220	FFFF	00	READ	1	not VMA, NMI	
221	C9CE	12	WRITE	1	NMI	
222	C9CF	34	WRITE	1	NMI	
223	D0D0	56	WRITE	1	NMI	
224	D0D1	78	WRITE	1	NMI	
225	D0D2	9A	WRITE	1	NMI	
226	D0D3	BC	WRITE	1	NMI	
227	D0D4	DE	WRITE	1	NMI	
228	D0D5	F0	WRITE	1	NMI	
229	D0D6	12	WRITE	1	NMI	
230	D0D7	34	WRITE	1	NMI	

*= These columns do not appear on the 7D02 screen.

@

LOC	ADDR	OPERATION	INT	*CYCLE TYPE	*OPCODE (HEX)
231	D9D8	56 WRITE	1	NMI	
232	D9D9	78 WRITE	1	NMI	
233	FFFF	00 READ	1	not VMA, NMI	
234	D9DB	D9 READ	1	IAK, NMI	
235	D9DC	DE READ	1	IAK, NMI	
236	FFFF	00 READ	1	not VMA, NMI	
237	D9DE	LDB #12	1	NMI	C6
238	D9DF	12 READ	1		
239	E6E0	**** (87)	0	INVAL.OP CODE	87
240	E6E1	12 READ	0		
241	FFFF	00 READ	0	not VMA	
242	E6E3	E6 READ	0	IAK (re-synchronize)	
243	E6E4	E6 READ	0	IAK (re-synchronize)	
244	FFFF	00 READ	0	not VMA	
245	E6E6	TSTA	0	DMA REQ	4D
246	E6E7	4D READ	0	DMA REQ, DEAD	
247	EFE8	A5 READ	0	DMA REQ, DMA	
248	EFE9	01 WRITE	0	DMA REQ, DMA	
249	EFEA	23 READ	0	DMA REQ, DMA	
250	EFEB	45 WRITE	0	DMA	
251	EFEC	45 READ	0	DEAD	
252	EFED	53 READ	0	PRE-FETCH	
253	EFEE	COMB	0		53
254	EFEF	D8 READ	0	PRE-FETCH	
255	F6F0	EORB @**	0		D8

*= These columns do not appear on the 7D02 screen.

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Figure 5-2. Self test acquisition.

Refer to the Troubleshooting Error List #3, for any failures.

CONTROL LINE CHECK

This test verifies the correct operation of PM 111 control lines.

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.
2. Make the following changes in Word Recognizer # 1.

   1 ADDRESS=XXXX
   and
   1 C9-C4 (ANDED CLOCKS)=X0X0XX

3. Leaving all of the remaining fields in the X (don't care) state, make the following changes listed in Table 5-4, while comparing the results on the screen before pressing the START key to continue.

Table 5-4
TEST TABLE

FIELD CHANGE	VALUE THE TRIGGER SHOULD OCCUR ON
INT=0	INT=0
INT=1	INT=1
ADDRESS=C0C5, BA=1	ADDRESS=C0C5
ADDRESS=C0C5, BA=0	NO TRIGGER
INVAL.OP=1	CYCLE AFTER ****

Refer to the Troubleshooting Error List #4, for any failures.

CLOCK QUALIFICATION CHECK

The following check verifies the correct operation of the PM 111 clock qualification circuitry.

1. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

2. Using the CURSOR control keys, enter the following program:

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=F6F1
1 FETCH1=X FETCH1+2=X R/W=X BA=X
1 INT=X INVAL.OP=X EXT.TRIG.IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=X010XX
END TEST 1
```

3. Press the START key. Trigger should not occur and program should continue to run.

4. Stop the program by pressing the STOP key.

Refer to the Troubleshooting Error List #5, for any failures.

5. Press the IMMEDIATE, DISPLAY, and PROGRAM keys in sequence.

6. Change the basic program to the following:

```
1      C9-C4 (ANDED CLOCKS)=X000XX
```

7. Press the START key.

8. Compare the screen display to the following information.

```
---T   F6F1
       F6F3
       E6E6
      (REPEAT)
```

Refer to the Troubleshooting Error List #6, for any failures.

PERFORMANCE CHECKS, PART 3

OVERVIEW

The following tests should be performed in order (unless otherwise specified), if verification of the listed performance requirements in the Specification section is to be performed.

TEST 1. SETUP and HOLD TIMES (DI0-DI7)

This test confirms the ability of the PM 111 to meet the required specifications for setup and hold times on lines DI0-DI7. Since this test uses input levels matching the Voltage in High and Low Limits specifications, the test also confirms the ability of the PM 111 to operate within those limits.

1. Insert the PM 111 logic analyzer plug into the 7D02.

2. Protect the PM 111 microprocessor plug with a 40-pin wire-wrap socket.

3. Turn on the mainframe power.

4. Set the PG 502 period adjustment to 1 microsecond. Turn variable period knob to the X1 position.

5. Connect the coaxial cable from the + TRIGGER OUT of the PG 502 to the TRIGGER/GATE IN of the PG 508. The PG 502 will trigger the PG 508. Refer to Figure 5-3.

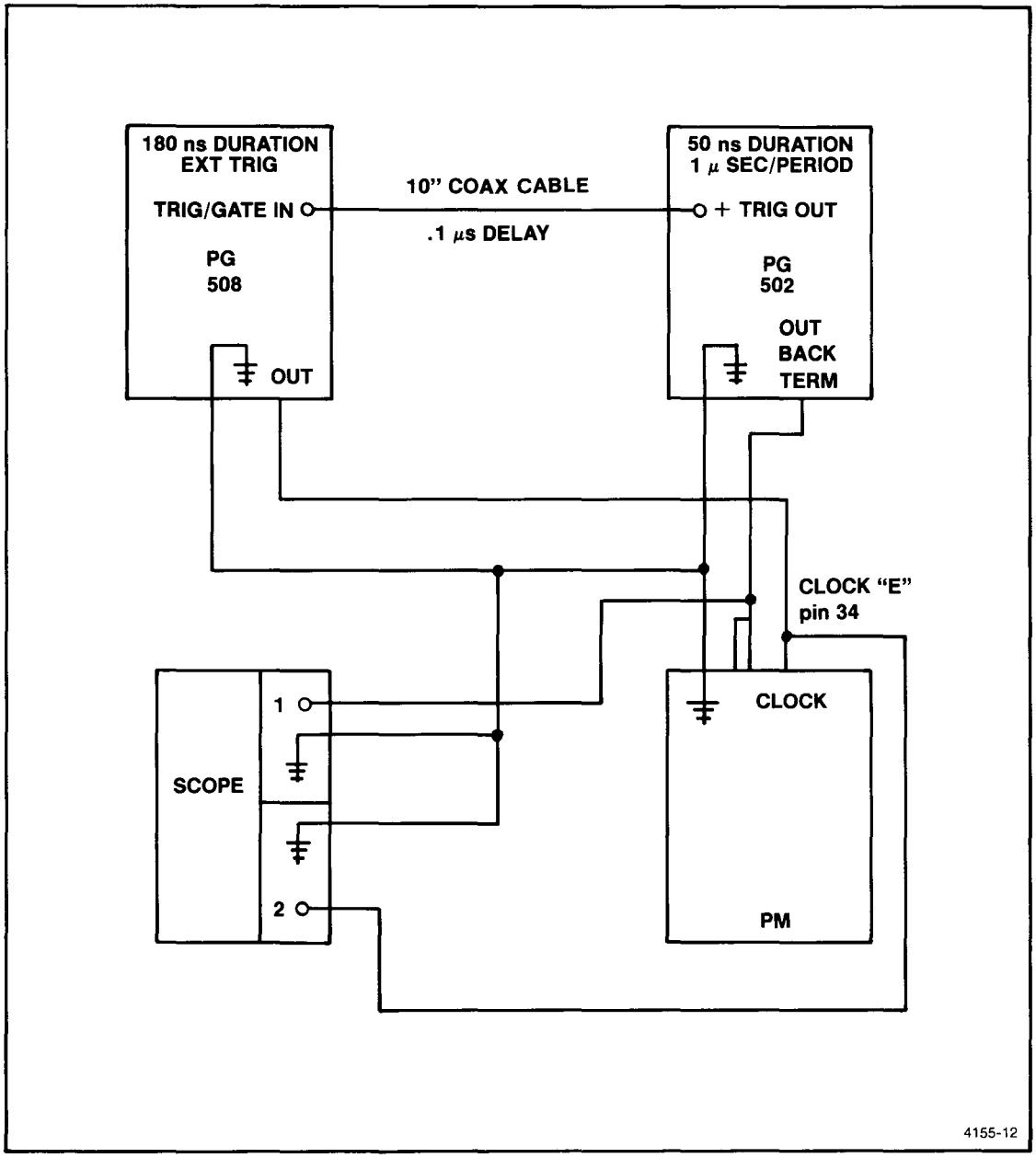

Figure 5-3. Setup and hold time test setup.

6. Set the PG 508 period knob to external trigger. Adjust the tigger/gate level knob until the green triggered/gated indicator is blinking, indicating the PG 508 recognizes trigger/gate impulse and is triggering on it.

7. Set trigger slope to - (out), FREE RUN switch (out), and mode switch to DELAY (in).

8. Set the PG 502 to reverse termination by pulling out the BACK TERMINATION knob.

9. Set the oscilloscope to channel 1. Connect the channel 1 scope probe to the PG 502 output. Switch the input coupling switch to ground and position the trace 1.4 V below the center graticule line. Switch the input coupling to DC and adjust the PG 502 output pulse for a low level of +0.6 V and a high level of +2.0 V.

10. Set the PG 502 NORMAL/COMPLEMENT button to the NORMAL (out) position.

11. Disconnect the oscilloscope probe from the PG 502 output, and connect the PG 502 output across ground (pin 1) and A15 (pin 23) on the PM 111 microprocessor plug.

12. Connect the channel 1 oscilloscope probe to the same pins as the PG 502.

13. Switch the PG 502 pulse duration knob to 5 ns. Adjust the PG 502 variable pulse duration knob so that a 50 ns pulse appears on the oscilloscope screen.

14. Check that the voltage levels of the pulse are +0.6 V to +2.0 V.

15. Switch the oscilloscope to channel 2. Using the channel 2 input, test the PG 508 output pulse voltage levels for +0.6 V to +2.0 V. After adjusting the PG 508 for the desired output, connect the PG 508 outputs across ground (pin 1) and clock E (pin 34) on the PM 111 microprocessor plug.

16. Connect the channel 2 scope probe to ground (pin 1) and clock E (pin 34) on the PM 111 microprocessor plug.

17. Adjust the oscilloscope time base to 20 ns/div. Switch the PG 508 pulse duration knob to 0.1 microseconds. Adjust the variable duration for a 180 ns pulse.

18. Obtain both displays, channel 1 and 2 on the oscilloscope. Set the scope to trigger on channel 2.

19. Adjust the PG 508 delay adjustment to 0.1 microsecond. Adjust the variable position knob until the trailing edge

of the data pulse (PG 502) is 10 ns beyond the trailing edge of the clock pulse (PG 508 output). Refer to Figure 5-4A.

20. The data pulse should be 50 ns wide. The clock pulse should be 180 ns wide.

21. Enter the following program into the 7D02:

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 FETCH1=X FETCH1+2=X R/W=X BA=X
1 INT=X INVAL.OP=X EXT.TRIG.IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    0-BEFORE DATA
1    0-SYSTEM UNDER TEST CONT.
1    1-USER CLOCK QUAL.
1    1-FALLING EDGE OF CLOCK
1    C9-C4 (ANDED CLOCKS)=XXXXXX
1OR IF
1
```

22. Enter the format mode by pressing the FORMAT key on the 7D02.

23. Change the Word Recognizer Address and Data fields to binary radix using the CURSOR control keys. Exit the format mode by pressing the FORMAT key.

24. Compare the changed base program to the following.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XXXXXXXX
1 ADDRESS=XXXXXXXXXXXXXXXX
```

25. Change A15, the far left address bit in the 7D02 program, to 0. All other elements should be in the X (don't care) state.

26. Run the program by pressing the START key.

27. The program should run without triggering or indicating a slow clock. This indicates the 7D02 is seeing the minimum clock pulse width, and making the 40 ns max. setup time and 10 ns max. hold time.

28. Stop the program by pressing the 7D02 STOP key.

    Refer to the Troubleshooting Error List #7, for any failures.

29. Place the PG 502 Complement to the COMPLEMENT position and adjust the oscilloscope so the pulses are on the screen. Verify the pulse out of the PG 502 is 40 ns before and 10 ns after the trailing edges of the clock pulse (PG 508). Refer to Figure 5-4B.

30. Change A15, the far left address bit in the base program, to 1. Press the START key.

31. No slow clock indication should be present, and no trigger should be received. Press the STOP key.

32. Repeat the test for A14 on the microprocessor plug. Move the PG 502 and scope probes from A15 (pin 23) to A14 (pin 22).

33. Change the 7D02 base program. The leftmost address bit should be changed to X, and the next address bit right should be changed to 0.

34. After testing for 0, test for 1 in the address bit. Repeat the previous procedure for the remaining address, then data lines, and remember:

WORD RECOGNIZER ADDRESS OR DATA BIT	PG 502 COMPLEMENT BUTTON
0	NORMAL
1	COMPLEMENTED

35. Refer to Figure 5-4B.

    Refer to the Troubleshooting Error List #7, for any failures.

36. Disconnect all oscilloscope probes.

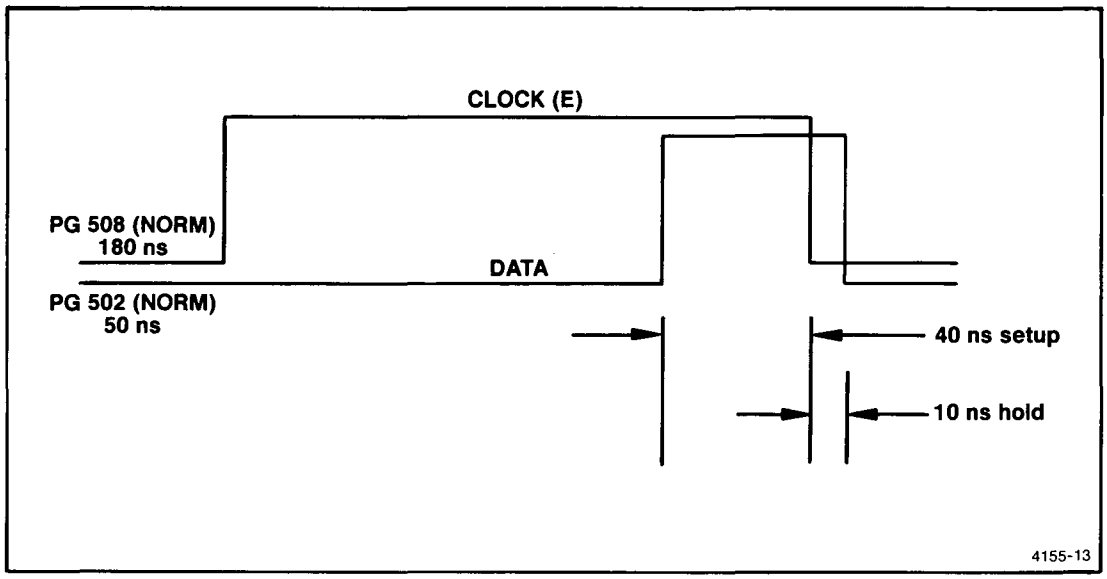

Figure 5-4A. Data lines DI0-DI7 setup and hold (normal).

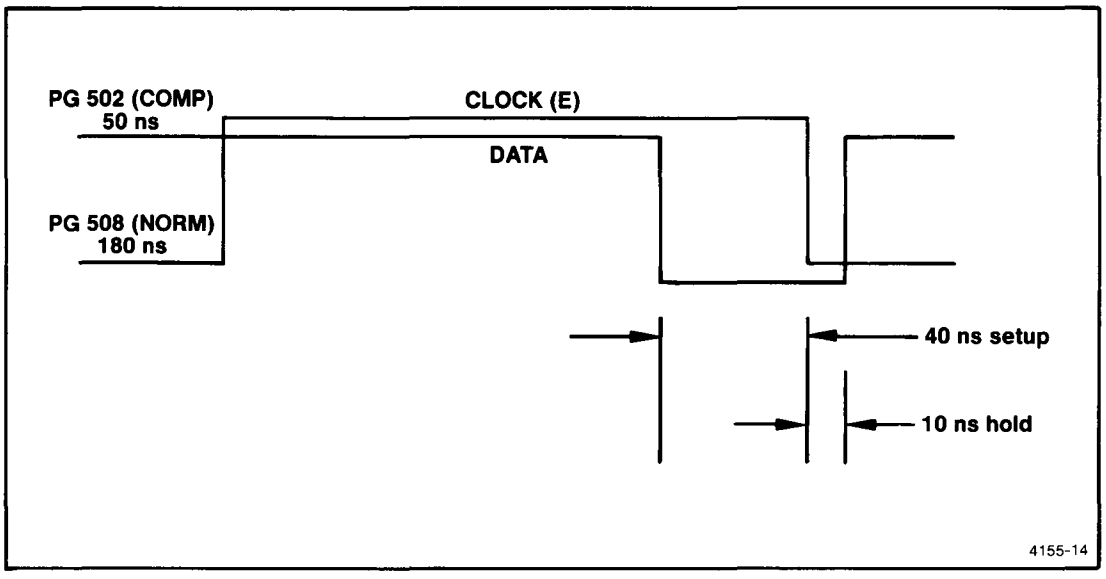

Figure 5-4B. Data lines DI0-DI7 setup and hold (complemented).

TEST 2. TIMING OPTION SETUP and HOLD TIMES

The following test confirms the ability of the timing option to meet the required specifications for setup and hold times. The user may decide to omit this test, in which case the next test in the sequence should be performed.

1. Set the PG 502 period adjustment to 1 microsecond. Turn the variable period knob to the X1 position.

2. The PG 502 will trigger the PG 508. Connect the coaxial cable from the + TRIGGER OUT of the PG 502 to the TRIGGER/GATE IN of the PG 508. Refer to Figure 5-3.

3. Set the PG 508 period knob to external trigger. Adjust the trigger/gate level knob until the green triggered/gated indicator is blinking, indicating the PG 508 recognizes the trigger/gate impulse and is triggering on it.

4. Set the trigger slope to - (out), FREE RUN switch (out), and MODE switch to DELAY (in).

5. Set the PG 502 to reverse termination by pulling out the BACK TERMINATION knob.

6. Set the oscilloscope to display channel 1. Connect the channel 1 scope probe to the PG 502 output. Switch the input coupling to ground. Position the trace 1.4 V below the center graticule line. Switch the input coupling to DC and adjust the PG 502 output pulse for a low level of +0.6 V and a high level of +2.0 V.

7. Set the PG 502 NORMAL/COMPLEMENT button to the NORMAL (out) position.

8. Disconnect the scope probe from the PG 502 output and connect the PG 502 output across the P6451 ground lead (white wire) and the P6451 MSB bit lead (violet wire).

9. Connect the channel 1 oscilloscope probe to the same points as the PG 502 outputs.

10. Switch the PG 502 pulse duration knob to 5 ns and adjust the PG 502 variable pulse duration knob so that a 25 ns pulse appears on the oscilloscope screen. Check that the voltage levels of the pulses are +0.6 V to +2.0 V.

11. Switch the oscilloscope to channel 2. Using the channel 2 input, test the PG 508 output pulse voltage levels for +0.6 V to +2.0 V. After adjusting the PG 508 output for the desired output, connect the PG 508 outputs across ground (pin 1) and pin 34 (E) of the PM 111 40-pin microprocessor plug.

12. Connect the channel 2 oscilloscope probe to ground (pin 1) and pin 34 (E) of the PM 111 40-pin microprocessor plug.

13. Adjust the oscilloscope time base to 20 ns/div. Switch the PG 508 pulse duration to 0.1 microsecond. Adjust the variable knob duration for a 180 ns pulse.

14. Obtain both displays, channel 1 and 2, on the oscilloscope. Set the oscilloscope to trigger on channel 2.

15. Adjust the PG 508 delay adjustment to 0.1 microsecond. Adjust the variable position knob until the trailing edge of the data pulse is 5 ns beyond the trailing edge of the clock pulse (PG 508 output). Refer to Figure 5-5A.

16. The data pulse should be 25 ns wide. The clock pulse should be 180 ns wide.

17. Turn the mainframe power off, then on again to delete any previous programs.

18. Press the WD RECOGNIZER and TRIGGER keys in sequence.

19. Using the CURSOR control keys, move the cursor to the TIMING WR box and enter a 1. The program is now set to recognize and trigger if the requirements of the Word Recognizer and the Trigger sections are met.

20. Move the cursor to the WORD RECOGNIZER field MSB box (far left box), and enter a 0.

21. Run the program by pressing the 7D02 START key.

22. The program should run wihout triggering or indicating a slow clock. This indicates the 7D02 is seeing the minimum clock pulse width, and making the 20 ns setup and 5 ns hold time requirements.

23. Stop the program by pressing the 7D02 STOP key.

    Refer to the Troubleshooting Error List #8, for any failures.

24. Place the PG 502 COMPLEMENT button in the complement position. Adjust the oscilloscope so the pulses are on the screen. Verify the pulse out of the PG 502 is 20 ns before and 5 ns after the clock pulse (PG 508). Refer to Figure 5-5B.

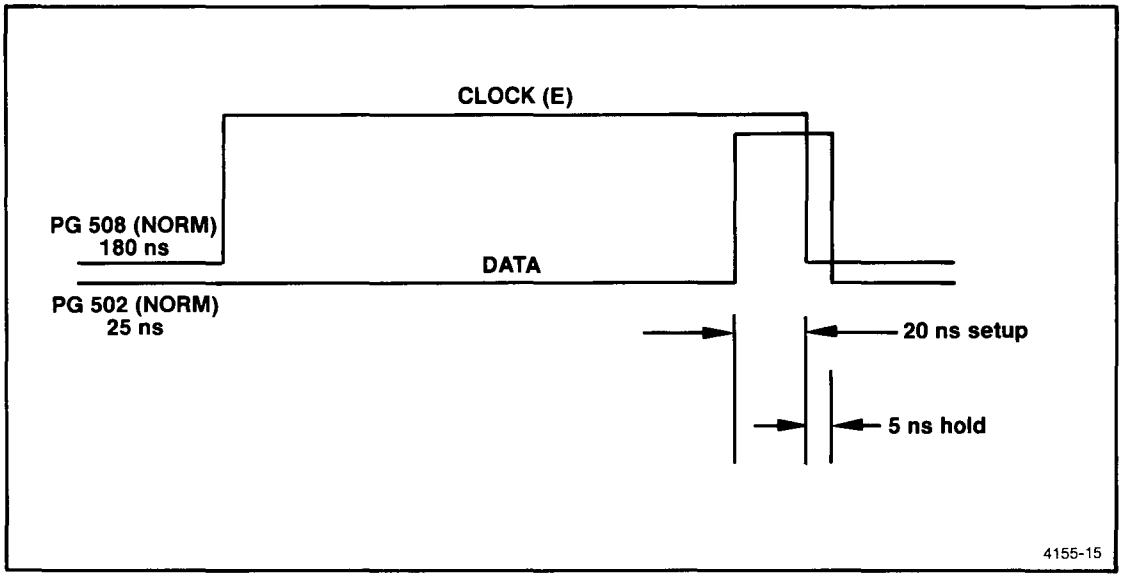

Figure 5-5A. Timing option data setup and hold (normal).

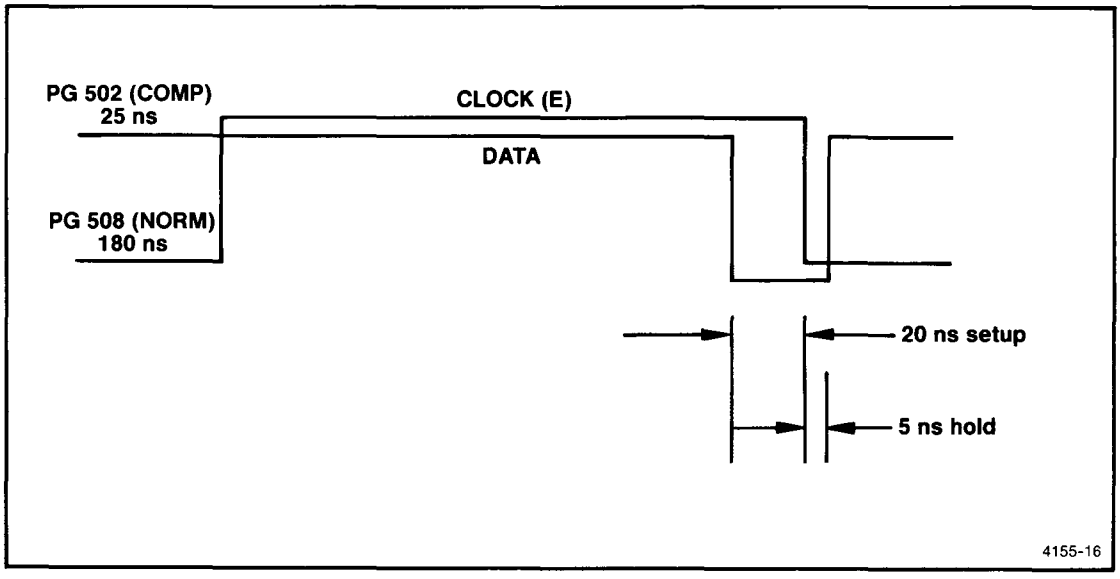

Figure 5-5B. Timing option data setup and hold (complemented).

25. Change the MSB bit in the WORD RECOGNIZER field to 1. Press the START key.

26. Again there should be no trigger and no indication of a slow clock.

27. Stop the 7D02 program.

28. Repeat the test for the next bit right of the MSB. Connect the PG 502 output and scope probes from the violet wire to the blue wire.

29. Change the 7D02 program. The leftmost (MSB) bit should be returned to X, and the next bit right should be change to 0, and then 1.

30. Repeat the above procedure for all of the leads shown in Table 5-5.

Table 5-5
P6451 TIMING OPTION WIRES

COLOR CODE	WIRE #
VIOLET	7 (MSB)
BLUE	6
GREEN	5
YELLOW	4
ORANGE	3
RED	2
BROWN	1
BLACK	0 (LSB)
WHITE	GROUND

31. Use the following guide for the remaining tests.

WORD RECOGNIZER	PG 502 COMPLEMENT BUTTON
0	NORMAL
1	COMPLEMENTED

Refer to the Troubleshooting Error List #8, for any failures.

32. Disconnect all test equipment.

TEST 3. TEST CLOCK PERIOD

This test confirms the ability of the test clock circuitry to operate within the 450 ns to 500 ns max. period specifiation.

1. Connect the channel 1 test oscilloscope probe to pin 34 (clock E) of the 40-pin plug, while it is plugged into the self-test socket.
2. Obtain a screen display of the clock E signal.
3. Measure that the signal period is between 450 and 500 ns, at the +1.4 V threshold level.

   Refer to the Troubleshooting Error List #9, for any failures.

4. Disconnect all test equipment.

TEST 4. TEST CLOCK PULSE WIDTH

This test confirms that the test clock pulse width is 75 ns min.

1. Connect the channel 1 test oscilloscope probe to pin 38 (EXTAL) of the 40-pin plug, while it is plugged into the self-test socket.

2. Obtain a display of the EXTAL signal. Note that the frequency of the EXTAL signal is twice that of the clock E signal.

3. Check that the pulse width (high or low) at the +1.4 V threshold level, is 75 ns min.

   Refer to the Troubleshooting Error List #10, for any failures.

4. Disconnect all test equipment.

TEST 5. CLOCK E PERIOD

This test confirms that the period of the clock E signal is 500 ns min.

Since the diagnostic modules 9 (PER. MOD.-SYSTEM) and B (TIMING OPTION) use stimulus from the test circuitry, and the test circuitry runs at a frequency slightly faster than clock E, the implication is that the 500 ns min. specification has been confirmed by the passing of the diagnostic tests. If the diagnostic tests have not been run, perform the Preliminary Setup and DIAGNOSTIC MONITOR, PART 1 located in this section.

Refer to the Troubleshooting Error List #11, for any failures.

TEST 6. DATA ACQUISITION PERIOD

Since the diagnostic modules 9 (PER. MOD.-SYSTEM) and B (TIMING OPTION) use stimulus from the test circuitry, and the test circuitry runs at a frequency slightly faster than clock E, the implication is that the 500 ns min. specification has been confirmed by the passing of the diagnostic tests. If the diagnostic tests have not been run, perform the Preliminary Setup and DIAGNOSTIC MONITOR, PART 1 located in this section.

Refer to the Troubleshooting Error List #12, for any failures.

TEST 7. PHALT (L) DELAY (from 40-pin plug to microprocessor).

1. Turn the mainframe power off, then on again to delete any previous programs.
2. Set the PG 502 output pulse voltage levels to +0.4 V (low) and +2.4 V (high).
3. Connect the PG 502 output across ground (pin 1) and HALT (L) (pin 40) of the 40-pin wire-wrap socket.
4. Connect the channel 1 oscilloscope probe across the same two pins.
5. Insert square pins in the personality module zero insertion force (ZIF) socket at pins 1 and 40.
6. Connect the channel 2 oscilloscope probe across pins 1 and 40 of the ZIF socket (pin 1 is ground).
7. Set the scope time base for 10 ns/div, and position the trace 1.4 V divisions below the center graticule line. Switch the vertical input attenuator to 1 V/div. The rising edge of the PG 502 output pulse should be positioned on the left graticule line at the point where the leading pulse edge passes through the center horizontal graticule.
8. Obtain both displays on the oscilloscope screen.
9. Set the PG 502 variable pulse duration at 50 ns. Turn the variable duration and variable period knobs to X1.
10. Measure the time delay of the rising edge of the pulse going into the plug to the rising edge of the pulse coming out of the ZIF socket. Rising edge to rising edge should be less than or equal to 55 ns apart.
11. Repeat the test with the falling edge.
12. The falling edges should be less than or equal to 55 ns apart.
13. Refer to Figure 5-6.

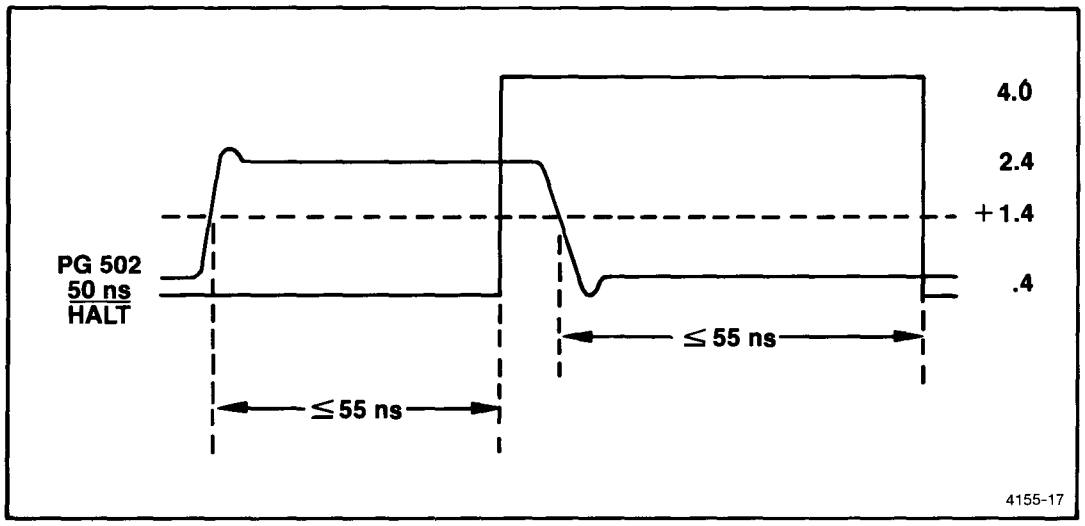

Figure 5-6. HALT (L) delay from 40-pin plug to microprocessor.

Refer to the Troubleshooting Error List #13, for any failures.

MAINTENANCE

REPAIR

The PM 111 requires no periodic maintenance. Properly handled and cared for, your personality module will give dependable service for many years. However, should repair service be needed at any time, Tektronix, Inc., provides complete instrument repair at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field Office or representative for further information.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. Many of the standard electronic components may also be available from a local source in your area. However, before you purchase or order a part from a source other than Tektronix Inc., please check the Replaceable Electrical and the Replaceble Mechanical Parts List(s) for the proper value, rating, tolerance, and description.

ORDERING PARTS

When ordering replacement parts from Tektronix Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include component number from the Replaceable Electrical Parts List).
4. The Tektronix part number.
5. The quantity of each part desired.

CLEANING INSTRUCTIONS

This instrument should be cleaned as often as the operating environment requires. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation. This condition can cause overheating and component breakdown within the instrument.

Exterior

Loose dust on the personality module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Do not get the microprocessor 40-pin plug or the logic analyzer plug wet. Do not use chemical agents as they may damage the plastic. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or other organic solvents.

Interior

Use a jet of dry, low pressure air and a soft brush to remove dust from the interior of the pod and circuit boards. After soldering or when otherwise required, use isopropyl alchohol with a soft cloth or cotton swab to remove flux, resin, or dirt. As the board is cleaned, make certain that the square pins are not contaminated with residual flux to ensure good electrical contact.

PERSONALITY MODULE DISASSEMBLY

Access to interior features can only be gained by disassembling the personality module case. If it becomes necessary to do so, find a clean open space on a table and be sure that screws and other small parts are placed where they will not be lost.

CAUTION

Always turn off the mainframe power before connecting or disconnecting any personality module. Static precautions should be observed at all times when disassembly or repair of the module is performed.

The disassembly procedure is described in the following.

1. To remove the top cover, unscrew the four middle screws on the bottom of the personality module case with a 3/32" Allen wrench.
2. Lift the top cover off. The top board, A1, is now accessible.
3. To access the middle board, A2, and the bottom board, A3, remove the four remaining screws of the personality module case .
4. Lift up gently on the three boards, removing them as a unit by raising them off the mounting posts.
5. Place the eight board spacers, and cable screws and nuts in a container for storage.
6. Separate boards A1 and A2, leaving boards A2 and A3 connected together with a ribbon cable.
7. Spread out the three boards on a non-conductive surface with the component sides up.
8. Plug A1P7017 into A2J4030, as per Figure 6-1.
9. The pod may now be operated with all three boards accessible for signature analysis or other testing.
10. To reassemble the instrument, reverse the above procedure.

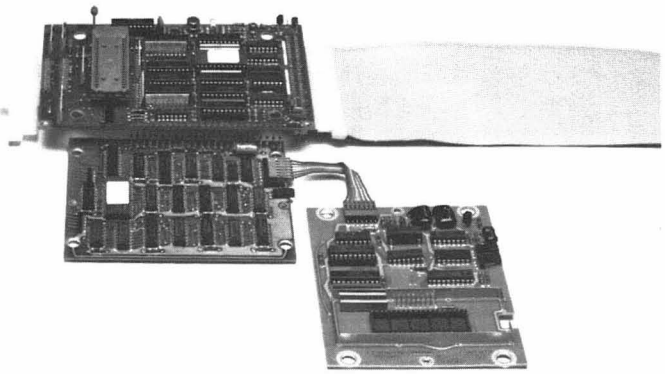

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Figure 6-1. Board layout of disassembled PM 111 Personality Module.

LOGIC ANALYER PLUG DISASSEMBLY

When it becomes necessary to disassemble the logic analyzer plug, use the following procedure:

1. Remove the four screws holding the logic analyzer plug together with a 3/32" Allen wrench.
2. Pull the halves of the plug apart and remove the cable hold-down clamp.
3. Remove the circuit board by lifting up on the cable end and sliding the board out of the plastic hold-down flanges.
4. Reverse the above procedure for reassembly of the logic analyzer plug.

MICROPROCESSOR PLUG DISASSEMBLY

The pins on the microprocessor plug are delicate and may become bent or broken. If this occurs, the pins can be replaced as a unit with the assembly unit listed in the Replaceable Electrical

Parts list. Refer to the exploded drawing for reference to the parts list and a view of a disassembled plug.

The procedure for disassembly is described below.

1. Remove the two Phillips head screws holding the protective face on the plug.

2. Lift off the protective face and inspect the top of the plug housing for wire alignment and cleanliness.

3. If necessary, clean the top of the plug housing (wire side) by briefly spraying with freon spray. No part of the plug housing or hybrid should be sprayed for longer than 10 seconds.

4. If the hybrid must be removed, proceed to part 5; if not, proceed to part 8.

5. Using a plastic alignment tool or your fingernails, gently pry up along the ends of the hybrid. Take care that you don't bend any of the pins or crack the ceramic hybrid substrate.

CAUTION

Do not use any metal tools to remove the hybrid from the housing. The hybrid is extremely susceptible to physical damage.

6. Clean the pin side of the hybrid with freon spray, if necessary.

7. To replace the hybrid, first align the hybrid's pins with the socket in the bottom of the plug housing, while noting pin 1 orientation. Press down on the hybrid with your fingers, distributing pressure evenly on the hybrid.

8. Clean the exposed part of the hybrid with freon spray.

9. In fitting the protective face over the pins, be sure that all of the pins and their respective holes are properly aligned and that none of the pins are bent over.

10. When all parts have been properly fitted back together, reinsert the two screws and tighten equally (do not overtighten).

TROUBLESHOOTING

OVERVIEW

When trouble occurs in the PM 111, several methods are available to the service technician for localizing and identifying the faulty circuit. Always repeat that section of the check that deals with any repaired line to verify repair work.

SUBSTITUTION METHOD

If other logic analyzers or personality modules are available, try substituting them and running the diagnostics again.

CAUTION

Exercise caution when you suspect power supply problems, since a supply that is seriously out of tolerance could cause secondary damage in more than one unit.

DIAGNOSTIC MONITOR

Power-up diagnostic routines are built in and automatically run each time the 7D02 Logic Analyzer-PM 111 Personality Module system is powered on. If a failure is detected, the POWER-UP VERIFICATION test results display this failure. The display offers the operator the choice between beginning operation or displaying the DIAGNOSTIC MONITOR MENU. Depressing any keyboard button (except X or START) within approximately 2 seconds of the power-up and holding the button for approximately 5 seconds will simulate a keyboard failure and allow the operator to access the DIAGNOSTIC MONITOR. The menu offers the choice of running any or all of the module tests, or of exiting the diagnostic monitor. Refer to the Diagnostic Monitor, Part 1 in the Performance Check section for failures. Refer to the 7D02 Service manual for more diagnostics information.

DIAGNOSTIC MODULE 9 PER. MOD.-SYSTEM

Diagnostic Module 9 contains 7 subtests. Subtests 1, 2, 3, 4, and 7 are personality module specific and are discussed in the following. Subtests 5 and 6 are the same for all personality modules. Refer to the 7D02 Service Manual for more information. Subtests 1, 2, 3, 4, and 7 require that the PM 111 be configured in the self-test mode. Refer to the Preliminary Setup in the Performance Check section for connection instructions.

Subtest 1

This test reads a byte at address 3:E010 in the personality module EPROM to determine the EPROM length. This tells the location (EFFC) of the EPROM trailer. The value at EFFC is compared with the value in the next byte, EFFD, which should be its complement. If the two bytes are not complementary, a failure message is printed as follows:

```
1    FAIL    3EFFD-X  (incorrect value @ 3:E010)
```

where X is the first non-complementary bit after the two bytes are compared on a bit-by-bit basis.

If the part number is correct, the following message is printed:

```
1    PASS    1351-00
```

Subtest 2

This test calculates a 16 bit checksum on the EPROM. If the checksum does not match the expected value, the calculated value is reported as the following failure:

```
2    FAIL    XXXX
```

where XXXX= the calculated value.

Subtest 3

The following program is assigned to the 7D02 State Machine:

```
IF WR1= TRUE
THEN TRIGGER TIMING AND MAIN
```

The 7D02 Acquisition Memory board is set for zero delay. All clock qualifiers are disabled, and the state clock is defined as the falling edge of the signal on pin 34 of the microprocessor, according to the data stored in the personality module EPROM. After all setups are complete, a DISPLAY command is sent and the 7D02 slow clock detector is checked. A slow clock indication will result in the following failure:

```
3    FAIL    0FF60-1  (slow or no clock)
```

This can be caused by an erratic or missing clock from the personality module. Anything that generates or transfers the test clock to the 7D02 should be checked.

If the clock appears to be running, the personality module EPROM is read to determine how long to wait for a trigger to occur. Then, a STORE command is sent. After waiting the specified amount of time (2 ms), the activity monitor on the Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If the Main Section is still in STORE mode, the following failure is generated:

```
3    FAIL    2E803-7  (Main Section failed to trigger)
```

Failure to trigger can be caused by failure of the personality module to generate and/or acquire the Word Recognizer 1 (WR1) value.

Subtest 4

This test involves all four of the 7D02 Word Recogniers, the two 7D02 Counters, the 7D02 State Machine, and the 7D02 Acquisition Memory.

The 7D02 Word Recognizers are programmed the same as for subtest 3. The 7D02 State Machine is also programmed with the following program.

```
1IF WR1 THEN GO TO 2, AND RESET CTR 1 AND 2

2IF WR2 THEN GO TO 3
2   ELSE INC. CTR 1

3IF WR3 THEN GO TO 4
3   ELSE INC. CTR 2

4IF WR4 THEN TRIGGER MAIN
```

In the previous example, all cycles are qualified except the trigger, therefore, all cycles are stored except the trigger cycle. The clock qualifiers are the same as for subtest 3 in that all clock qualifiers are disabled, and the state clock is defined as the falling edge of the signal on pin 34 of the microprocessor.

After all steps are complete, a DISPLAY command is sent and the slow clock detector is checked. A slow clock indication results in the following failure.

```
4    FAIL    0FF60-1  (slow or no clock)
```

This can be caused by an erratic or missing clock from the personality module. Anything in the personality module that generates or transfers the test clock should be checked.

If the clock appears to be running, the personality module EPROM is read to determine how long to wait for a trigger. Then, a STORE command is sent. After waiting 2 ms, the Activity Monitor on the 7D02 Acquisition Memory board is examined to see if the Main Section has triggered and returned to DISPLAY mode. If it is still in the STORE mode, the following failure is generated.

```
4    FAIL    2E803-7  (Main Section failed to trigger)
```

Failure to trigger can be caused by failure of the personality module to generate and/or acquire any one of the four Word Recognizer values.

Next, all bytes in the 7D02 Acquisition Memory between 2:E000 and 2:E3FF are summed and the result of the checksum is compared with the expected data stored in the personality module EPROM. Failure to compare results in the following failure message.

```
4    FAIL    3E035-X  (Main Acq. Mem. fails checksum)
```

Failure of the checksum to match is likely due to either an intermittent channel, or the fetch predictor circuitry operating erratically.

Subtest 7

This test checks the clock qualifier lines C9-C4 on the 7D02 Front End board.

The 7D02 State Machine is programmed with the following test sequence.

```
1IF WR1 THEN TRIGGER MAIN
1   ELSE GO TO 1
```

C9-C4 are set equal to 010101, respectively.

Word Recognizer 1 was programmed in an earlier subtest to a value specifed by the personality module EPROM. This test uses each of the control lines in turn to qualify out the value to which Word Recognizer 1 has been programmed.

If the control line works correctly, the State Clock that occurs with Word recognizer 1 will be inhibited and the State Machine will not see the Word Recognizer output. A PASS condition, then, is indicated by the failure of the Main Section to trigger. The processor waits 2 ms to trigger.

Six bytes in the personality module EPROM specify the value to be sent to the 7D02 Front End to inhibit State Clocks when Word Recognizer 1 occurs for each of the six control lines. The following sequence is repeated six times, once for each control line or until a failure occurs.

- Read value from personality module EPROM.
- Write value to Front End latch.
- Send STORE command.
- Wait specified length of time.
- Check Activity Monitor on Acquisition Memory board.
- If in DISPLAY mode, print FAIL and stop.

If subtests 3 and 4 pass, it is safe to assume C9-C4 are operating correctly.

The test results are interpreted as follows:

7	FAIL	3E039	(C4 didn't inhibit trigger)
7	FAIL	3E03A	(C5 didn't inhibit trigger)
7	FAIL	3E03B	(C6 didn't inhibit trigger)
7	FAIL	3E03C	(C7 didn't inhibit trigger)
7	FAIL	3E03D	(C8 didn't inhibit trigger)
7	FAIL	3E03E	(C9 didn't inhibit trigger)

DIAGNOSTIC MODULE B
TIMING OPTION

This module consists of 3 subtests. Subtests 1 and 2 are the same for every personality module. Test 3 is personality module specific. Refer to the 7D02 Service Manual for more information.

This test requires that the stimulus from the self-test circuitry, via the P6451 Timing Option Probe, is connected. Subtest 3 is not run during the POWER-UP VERIFICATION.

The timing option word recognizer is set to trigger on the occurrence of 55H.

Subtest 3

The 7D02 State Machine is programmed similar to the following:

```
1IF TIMING OPTION WR=55
1THEN GO TO 4

4IF TIMING OPTION WR=55
4THEN TRIGGER TIMING AND MAIN
```

The timing option memory address counter is set to 0. All word recognizers, except the timing option, are set to X (don't care).

The slow clock indicator is checked for the presence of a clock. If none is detected, the following failure is printed.

```
3    FAIL    0FF60-1  (slow or no clock detected)
```

If the clock appears to be running, a byte is read from the personality module EPROM that specifies how long to wait for the trigger. Then a STORE command is sent. After waiting the specified amount of time (2 ms), the 7D02 Acquisition Memory Activity Monitor is examined to see if the Main Section has triggered. If it hasn't, the following failure is reported.

```
3   FAIL    2E803-7  (Main Section failed to trigger)
```

This can be caused by the self-test circuitry not generating the 55H value or the P6451 not transferring data properly.

If the trigger occurred, the timing option memory address counter is examined to determine the last data location and the trigger location is calculated. The value saved in the trigger location is then compared with the value in the personality module EPROM that was used to program the timing option word recognizer. If the two are not complementary (data inverted), the following failure is reported.

3 FAIL 3E03F-X (trigger value incorrect)

where X is the first offending bit.

This can be caused by a bad timing relationship between the clock and the data.

If the trigger test passes, the timing option acquisition memory at address 2:F000 - 2:F0FF is checksummed (with the exception of one data byte which is Xs), and the result compared with the expected value stored in the personality module EPROM. If the values are not the same, the following failure is reported.

3 FAIL 3E040-X (checksum error 2:F000 - 2:F0FF)

where X is the first bit that didn't match.

This can be caused by the PM 111 self-test circuitry not generating the correct pattern all the time, or an intermittent failure in the P6451.

PERFORMANCE CHECKS

Testing of specific parameters in the Performance Requirements column of the Specification section is provided through use of listed test equipment, the 7D02 word recognizers, and test programs. To perform the tests, refer to the Performance Check, Part 3 in the Performance Check section. For the corresponding Troubleshooting Error List, refer to the Troubleshooting Error List in this section.

HOW TO USE THE SELF-TEST CIRCUITRY

On the bottom side of the PM 111 Personality Module is a plastic door covering the self-test stimulus generator outputs (a 40-pin test socket). Some 7D02 diagnostic tests will run only if the self-test plug (40-pin microprocessor plug) is installed in the test socket. The 7D02 indicates this, when necessary, by displaying the message PLEASE CONNECT SELF TEST STIMULUS.

The self-test feature is useful in troubleshooting the PM 111 and in verifying the correct operation of the PM 111 via the Diagnostic Monitor of the power up verification sequence. Refer to the Theory Of Operation section for a better understanding of the self-test circuitry.

CAUTION

Always turn off the mainframe power before connecting or disconnecting any personality module.

1. Perform the Preliminary Setup found at the beginning of the Performance Check section of this manual.

2. After connections have been made, turn on the mainframe power while holding down any keyboard button (except X and START) to simulate a keyboard failure. The 7D02 is now in the diagnostic mode.

3. Select and execute the desired 7D02 diagnostic tests. The only tests that require the 40-pin microprocessor plug to be installed in the test socket are 0-TEST ALL, 9-PER. MOD.-SYSTEM, and B-TIMING OPTION.

4. When testing is completed, turn off the mainframe power.

5. Remove the 40-pin plug from the test socket and the P6451 Timing Option Probe from the timing pins.

6. Replace the plastic door on the bottom of the personality module case.

JUMPER PLUGS AND TEST POINTS

The following Table 6-1 provides the name, number, and location of the jumper plugs and test points located in the PM 111 Personality Module.

Table 6-1
PM 111 JUMPER PLUGS AND TEST POINTS

Jumper Plug or Test Point	Board Location	Common Name
TP 1042	A1	ETTL(L)
TP 1043	A1	FFFE
TP 1044	A1	DMA+DEAD(L)
TP 1046	A1	CLK
TP 1047	A1	CLK(L)
TP 1048	A1	GND
J 7013	A1	DMA/BREQ(L)
TP 7022	A1	VMA
TP 7031	A1	ENIFC(L)
TP 7032	A1	IAK(L)
TP 7033	A1	ENSCLK(L)
TP 1070	A2	GND
TP 1071	A2	CT0
TP 2070	A2	CT1
TP 2071	A2	CT2
TP 2072	A2	CT3
J 2008	A2	PRESENT Z
J 3008	A2	PRESENT X
J 3022	A2	PRESENT Y
TP 3070	A2	F0
TP 3071	A2	F1
TP 3072	A2	F2
TP 3073	A2	IOC(L)
TP 3074	A2	SCLK
J 1028	A3	NORM/TEST
J 1030	A3	NORM/TEST

TROUBLESHOOTING ERROR LIST and PROCEDURES

When performance checks or troubleshooting detect a failure, reference notes will direct the service technician to a specific error number listing. This list may in turn direct the technician to a specific procedure to isolate the problem.

The following error list pertains to errors found when performing the Performance Checks, Part 3.

This error list assumes the 7D02 is known to be operating correctly, the personality module has been properly connected, and all power supplies are within their specified tolerances.

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Table 6-2
PM 111 TROUBLESHOOTING ERROR LIST

ERROR NO.	SYMPTOM	POSSIBLE CAUSES
1.	Diagnostic Module 9 "FAIL"	(See Troubleshooting Procedure 1, START)
2.	Diagnostic Module B "FAIL"	(See Troubleshooting Procedure 3)
3.	Self Test Acquisition wrong	(See Troubleshooting Procedure 1, ENTRY POINT 2)
4.	Control Line C3, C4 and C5 check (no trigger)	C3 (INT) circuitry: A1U's 1018, 6045, 3045, 7035, 1004 and all VMA circuitry. C4 (BA) circuitry: U1018, U1002 C5 (I0C0(L)) circuitry: A2U3040, A2U2020, A2U2060, A2U3060, A1U4025, A1U2018, A1U5018.
5.	Clock Qualification (triggered)	C7 (HALT).(DMA/BREQ) circuitry: A1U7035, A1U5045, A1U1018 and A1U1002.
6.	Clock Qual. (X000XX gives wrong display)	C7 circuitry (above), plus VMA circuitry: A1U7035, A1U6045, A1U4045, A1U5045, A1U3025, A1U1018, A1U1002, A1U2025, A1U6025, A1U3008, A1U3024, A1U6004, A1U7024; DMA + Dead circuitry: A2U3040, A1U2045, A1U5045, A1U7035, A1U3045, A1U1018, A1U1002 and ETTL(L).
7.	Setup and Hold problem. Voltage in High and Low limits. (DIO-7)	Data Channel delay out of spec: check A1U4025, A1U5025, A1U2018, A1U5018. Address Channel delay out of spec: check A1U's 2035, 6035, 2025, 6025, 3008, 3024, 6004, 7024. Clock delay out of spec: check A1U1031 and associated circuitry.
8.	Timing Option Setup and Hold	Clock delay out of spec: check A1U1031 and associated circuitry.
9.	Test Clock Period	Check A3U1025B, A3U1029, A3Q1017, A3C1015 and A3C2015.

PM 111 TROUBLESHOOTING ERROR LIST (con't)

ERROR NO.	SYMPTOM	POSSIBLE CAUSES
10.	Test Clock Pulse Width	Check A3U1029D, A3Q1017, A3C1015, A3C2015, and -15 V.
11.	Clock E Period	(See possible causes for ERROR #9)
12.	Data Acquisition Period	(See possible causes for ERRORS #7 and #9)
13.	PHACT(L) DELAY	Check A1U7035, A1U5045, A1CR2018, A1CR2019, A1CR2007 and A1CR2008.

Clock Oscillator Hybrid Troubleshooting Procedure

When the clock oscillator hybrid circuitry located inside the 40-pin microprocessor plug is suspected of being faulty, the following test may be performed to verify correct operation.

1. Plug the wire-wrap socket, Tektronix P/N 136-0622-00, into the optional 40-pin dip socket, Tektronix P/N 136-0623-00 (installed in the PM 111 test socket).

2. Plug the 40-pin microprocessor plug into the wire wrap socket.

3. Connect a test oscilloscope probe to pin 34 (clock E) of the wire wrap socket.

4. With the jumpers A2J1028 and A2J1030 in the NORM position (pins 1 and 2 shorted), the oscillator hybrid is included in the clock circuitry loop. Obtain a display on the test oscilloscope and ensure it is present and correct (refer to the Specifications section).

5. If the E clock signal is present and correct, the oscillator hybrid circuitry is operating properly. If the signal is not present or correct, proceed to part 6.

6. Move the jumpers A2J1028 and A2J1030 into the TEST position (pins 2 and 3 shorted). The oscillator hybrid is now bypassed (out of the clock circuitry loop).

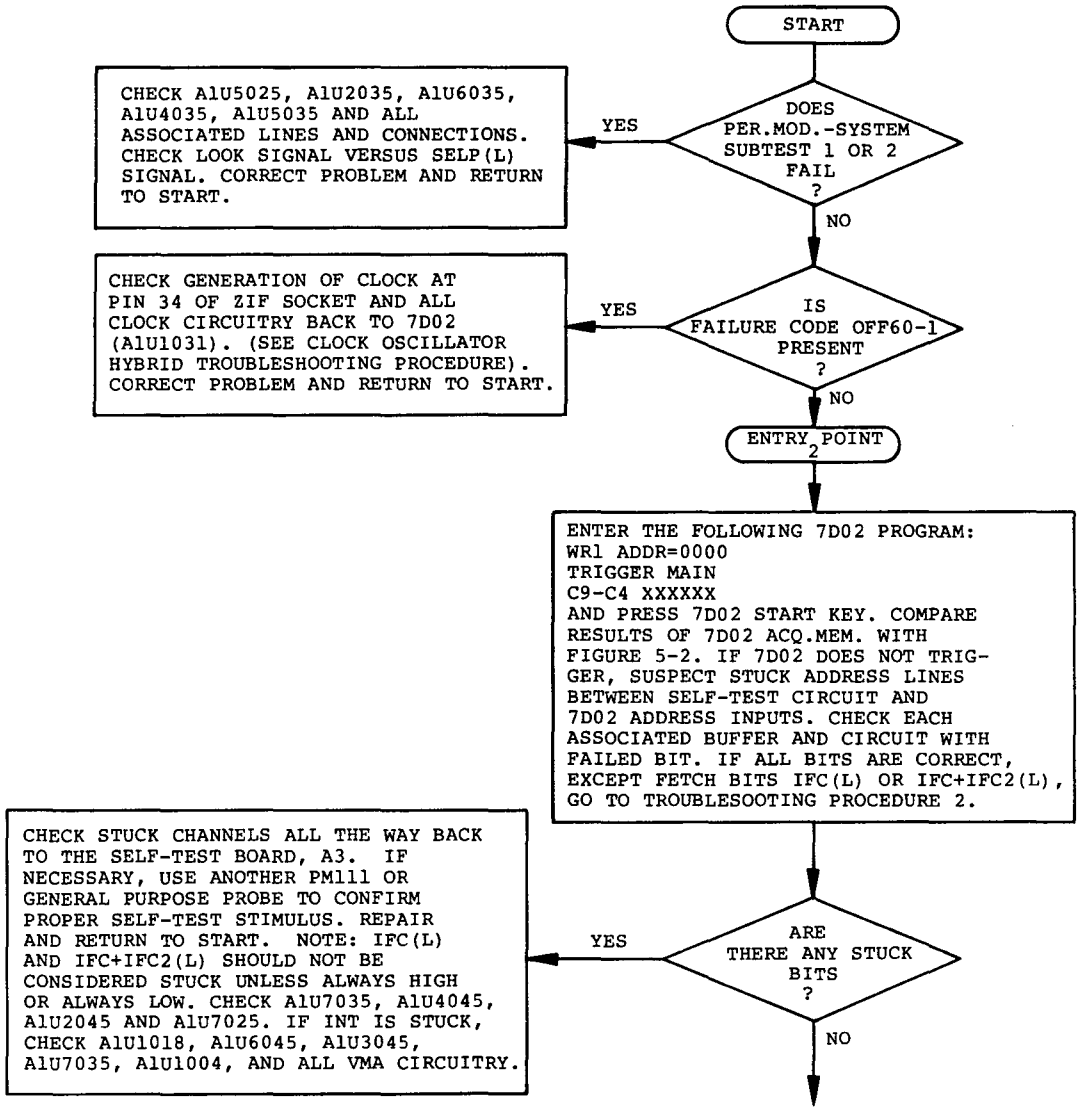
7. Obtain a display on the test oscilloscope and ensure it is present and correct.

8. If the E clock signal is present and correct, the bypass has isolated the fault to either the oscillator hybrid or the 40-pin plug cable. If the E clock signal is not present and correct, check the Clock Divider circuitry or the Self-Test Oscillator circuitry.

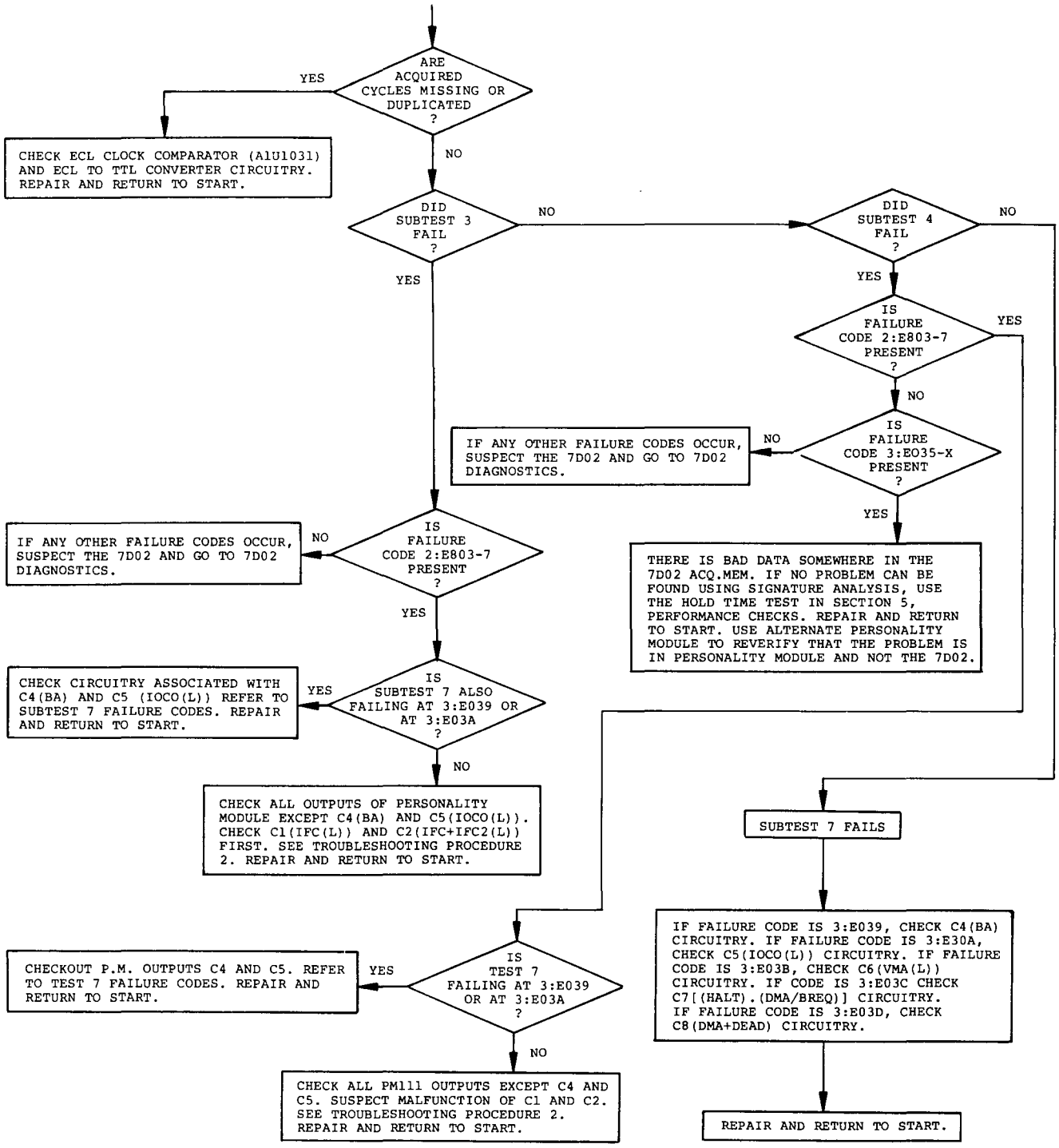
9. Repair the faulty circuitry and verify correct operation by checking for correct waveforms in both NORM and TEST jumper positions.

10. Restore the jumpers A2J1028 and A2J1030 to the NORM position.

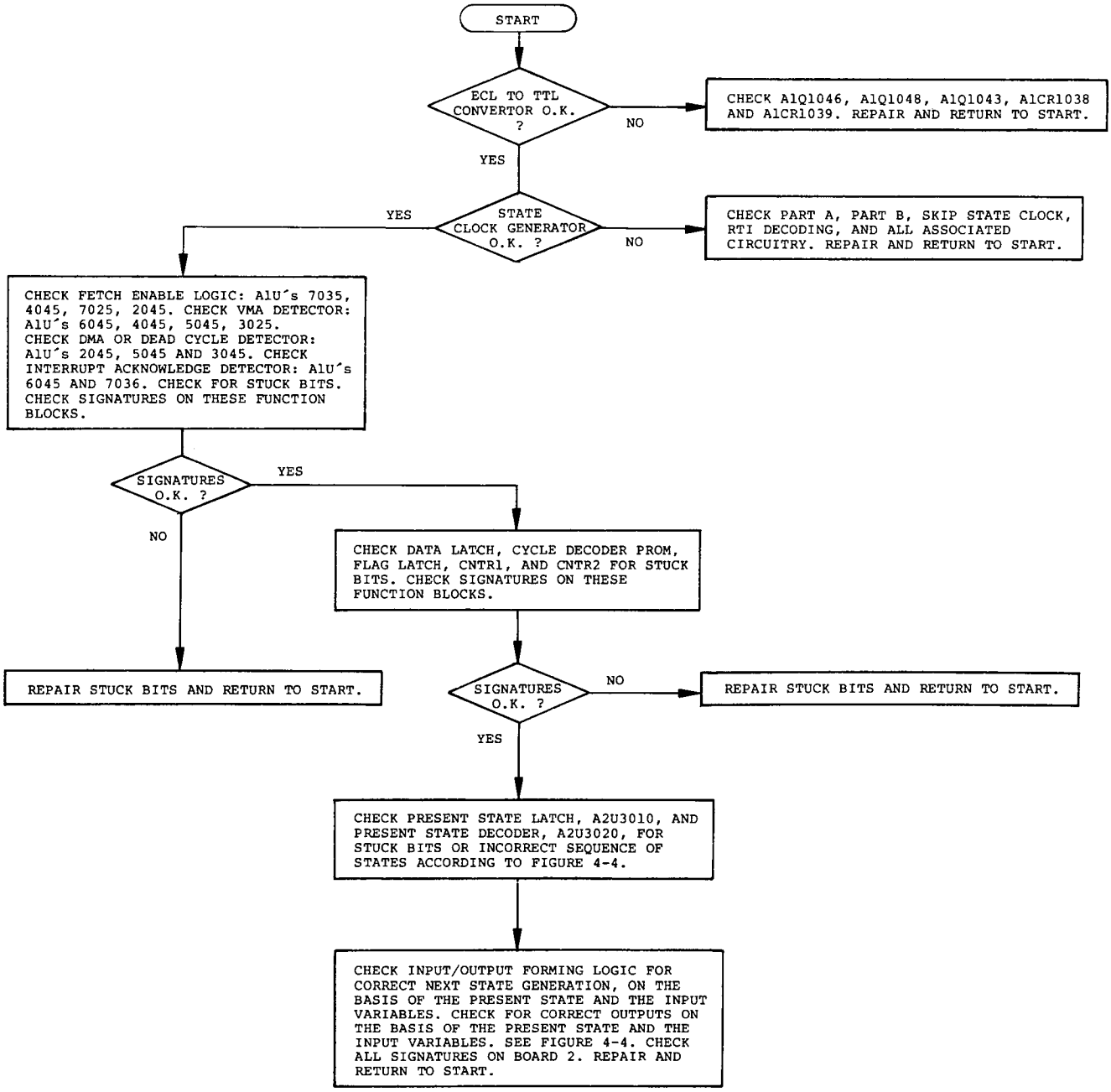
Table 6-3
TROUBLESHOOTING PROCEDURES



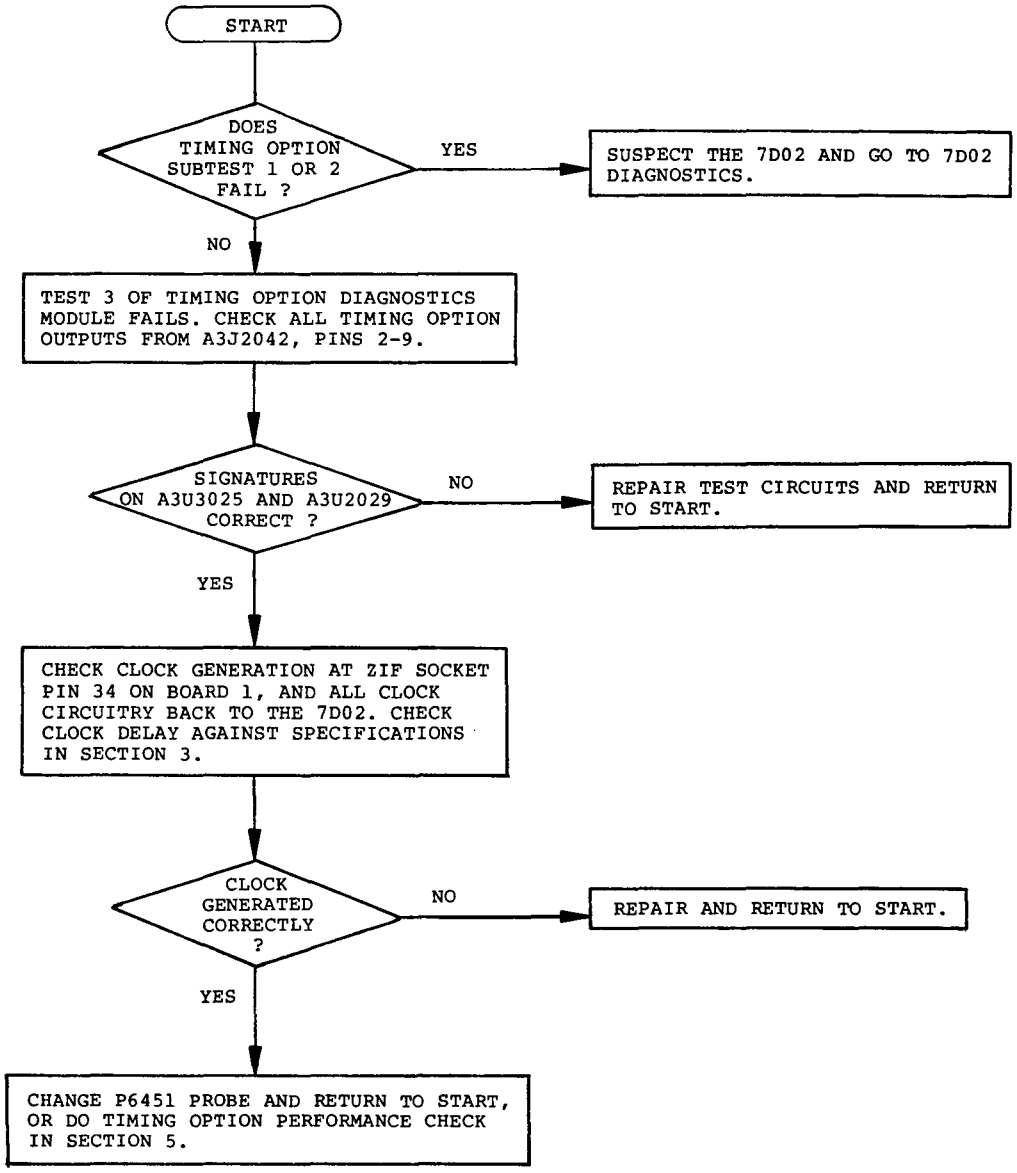
TROUBLESHOOTING PROCEDURE 1



TROUBLESHOOTING PROCEDURE 1 (cont'd)



TROUBLESHOOTING PROCEDURE 2
(FETCH PREDICTOR)



TROUBLESHOOTING PROCEDURE 3

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SIGNATURE ANALYSIS

The Signature Analysis Procedure allows the service technician to check the condition of a logic circuit node in the PM 111 with respect to a specific operating time window.

Troubleshooting With Signature Analysis Procedure

A signature is a four-digit hexadecimal number representing time-dependent logic activity during a specified measurement interval (referred to as a window) for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probable malfunction in the circuit.

The signal that causes the node to produce a signature is the stimulus. In signature analysis, the stimulus is supplied by the personality module itself when configured in the self-test position. This way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation.

Preliminary Setup

1. Use the Sony/Tektronix Type 308 with the P6451 probe.
2. Leave the mainframe power off. Insert the personality module logic analyzer plug into the logic analyzer.
3. Disassemble the personality module and lay out the boards according to the procedure listed in the Personality Module Disassembly section.
4. Insert the personality module 40-pin plug into the 40-pin test socket, located under the door on the bottom of the module case. Ensure that pin 1 orientation is observed. This is the self-test position.
5. Connect the signature analyzer probe clock lead to board A1, test point 1042.
6. Connect the signature analyzer start/stop leads to board A3, J2042-9 (TH).
7. Set the start and stop triggering to rising edge.
8. Set the clock to rising edge.
9. Turn the logic analyzer power switch on while holding down any 7D02 key (except X and STARR). This will force the 7D02 into diagnostic mode.

10. Press the 7D02 X key to obtain a display of the diagnostic menu.

11. Press the F key to select SIGNATURE EXERCISER MENU.

12. Press the 7 key to select PER.MOD.-SYSTEM.

13. The following signature table lists the PM 111 signatures.

NOTE

The signature for +5 V = CC34, and the signature for GND = 0000.

Table 6-4
PM 111 SIGNATURE TABLE

BUFFER BOARD	WITHOUT A2J3008
A1U1018	
2	7449
3	UP44
4	9HC1
5	7719
6	F880
7	CC34
8	0532
9	476C
11	476C
12	0532
13	CC34
14	F880
15	7719
16	9HC1
17	UP44
18	7449
A1U2025	
2	8P34
3	4046
4	02U2
5	H5HH
6	3H97
7	A6PF
8	6UA2
9	3612
11	3612
12	6UA2
13	A6PF
14	3H97
15	H5HH
16	02U2
17	4046
18	8P34
A1U2035	
1	0000
2	3612
3	6UA2

BUFFER BOARD	WITHOUT A2J3008
A1U2035 (con't)	
4	A6PF
5	3H97
6	H5HH
7	02U2
8	4046
9	8P34
11	8P34
12	4046
13	02U2
14	H5HH
15	3H97
16	A6PF
17	6UA2
18	3612
19	0000
A1U2045	
1	UC72
2	C2AP
3	6785
4	H0F2
5	73C4
6	1842
A1U3025	
1	8P34
2	8P34
3	3612
4	02U2
5	02U2
6	02U2
7	3612
9	099A
10	3612
11	6UA2
12	A6PF
13	3H97
14	H5HH
15	02U2

BUFFER BOARD	WITHOUT A2J3008
A1U3045	
2	H8F1
3	H52C
4	0000
5	0532
6	H8F1
7	63U5
9	5U74
10	P440
12	0000
13	F880
14	F880
A1U4025	
2	H8F3
3	AU99
4	10CF
5	6C32
6	435U
7	C83U
8	0724
9	PC01
11	5035
12	CF10
13	030C
14	U86C
15	H006
16	AC88
17	14AH
18	63U7
A1U4035	
1	6UA2
2	3H97
3	02U2
4	8P34
5	3612
6	A6PF
7	H5HH
8	4046

BUFFER BOARD	WITHOUT A2J3008
A1U4035 (con't)	
18 CC34	
19 02U2	
21 3612	
22 02U2	
23 3612	
A1U4045	
1 48C8	7082
2 6785	
3 573C	7082
4 5A35	
5 6785	
6 P5U4	C618
8 C2AP	
9 58F0	
10 7449	
11 099A	
12 UA77	C618
13 5A35	
A1U5025	
1 0000	
2 63U7	
3 14AH	
4 AC88	
5 H006	
6 U86C	
7 030C	
8 CF10	
9 5035	
11 PC01	
12 0724	
13 C83U	
14 435U	
15 6C32	
16 10CF	
17 AU99	
18 H8F3	
19 0000	

BUFFER BOARD	WITHOUT A2J3008
A1U5035	
1 CC34	
2 CC34	
3 5035	
5 030C	
7 H006	
9 14AH	
11 CC34	
12 H8F3	
13 CC34	
14 10CF	
15 CC34	
16 435U	
18 0724	
19 CC34	
A1U5045	
1 PC1C	
2 CC34	
3 502U	
4 PC1C	
5 7719	
6 9F02	
8 58F0	
9 3H97	
10 6UA2	
11 H0F2	
12 73C4	
13 P440	
A1U6025	
2 8P34	
3 3612	
4 02U2	
5 02U2	
6 3H97	
7 02U2	
8 6UA2	
9 3612	
11 3612	
12 6UA2	

BUFFER BOARD	WITHOUT A2J3008
A1U6025 (con't)	
13 02U2	
14 3H97	
15 02U2	
16 02U2	
17 3612	
18 8P34	
19 0000	
A1U6035	
1 0000	
2 3612	
3 6UA2	
4 02U2	
5 3H97	
6 02U2	
7 02U2	
8 3612	
9 8P34	
11 8P34	
12 3612	
13 02U2	
14 02U2	
15 3H97	
16 02U2	
17 6UA2	
18 3612	
19 0000	
A1U6045	
1 UP44	
2 63U5	
3 CC34	
4 7449	
5 73C4	
6 72A1	
8 6P1U	
9 C2AP	
10 476C	
11 4046	
12 9HC1	
13 CC34	

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BUFFER BOARD		WITHOUT A2J3008
A1U7025		
1	476C	
2	6P1U	
3	0000	
4	H526	CC34
5	1842	
6	UHC2	93A0
8	5A35	
9	72A1	
10	1842	
11	0000	
12	6P1U	
13	476C	
A1U7035		
1	0000	
2	4046	
3	0000	
4	6P1U	
5	PC1C	
6	9F02	
7	73C4	
8	P5U4	C618
9	4143	0H2F
11	UA77	C618
12	5PF0	0H2F
13	F880	
14	2736	
15	502U	
16	H52C	
17	CC34	
18	UC72	
19	0000	

FETCH PREDICTOR		WITHOUT A2J3008
A2U1010		
1	1PA4	A1F7
2	4AF2	3F17
3	7F21	1372
4	1P72	0000
5	1FCF	UP32
6	A5U3	CC34
11	F189	2823
12	FP3A	9317
13	C0P7	738F
A2U1020		
1	00H6	A1F7
2	P9F7	H81F
3	1P72	0000
4	PCP0	5U67
5	8519	C8U8
6	4561	CC34
8	9109	7903
9	30PA	6A71
10	66U6	CC34
11	7F21	1372
12	CA70	CC34
13	7ACH	9317
A2U1030		
1	55CP	FCC6
2	1FPC	CC34
3	3348	7082
4	55CP	FCC6
5	A7HU	0000
6	66U6	CC34
8	17U7	1AU3
9	00H6	A17F
10	F189	2823
11	U38F	FCC6
12	3348	7082
13	F0F4	CC34
A2U1040		
1	P9F7	H81F
2	A5AU	F27H
8	C02F	UA24
9	F189	2823

FETCH PREDICTOR		WITHOUT A2J3008
A2U1040 (con't)		
10	1700	F1UF
11	00H6	A1F7
12	PCP0	5U67
13	PP53	3HFU
A2U1050		
1	CC37	
2	0000	0000
3	A623	C440
4	67AU	A9F4
5	526F	5AU9
6	HAC9	97A0
7	HHF2	0000
9	0953	CC34
10	CC34	
11	F4A5	
12	F4A5	
13	PHC8	
14	H35A	
15	1FPC	CC34
A2U1060		
1	CC34	
2	0000	0000
3	A623	C440
4	67AU	A9F4
5	526F	5AU9
6	HAC9	97A0
9	17U7	1AU3
10	3HH3	9820
11	2H86	596H
12	H88F	5870
13	H0F6	9FAA
14	2143	2222
A2U1070		
1	A623	C440
2	67AU	A9F4
4	526F	5AU9

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FETCH PREDICTOR		WITHOUT A2J3008
A2U1070 (con't)		
5	HAC9	97A0
6	1700	F1UF
8	72AF	1849
9	9A77	9916
10	2H86	596H
12	H88F	5870
13	H0F6	9FAA
A2U2010		
1	CA70	CC34
2	3348	7082
4	4561	CC34
5	1975	C2C5
6	H52F	F237
8	P3P7	1286
9	1975	C2C5
10	73AA	6204
12	3348	7082
13	CA70	CC34
A2U2020		
1	A590	1AU3
2	1P72	0000
3	00H6	A1F7
4	1975	C2C5
5	H9C1	0981
6	7CU0	0000
8	A590	1AU3
9	4AF2	3F17
10	H9C1	0981
11	AF15	0000
12	1P72	0000
13	0953	CC34
A2U2030		
1	CA70	CC34
2	A5U3	CC34
3	C02F	UA24
4	4561	CC34
5	86P7	2314

FETCH PREDICTOR		WITHOUT A2J3008
A2U2030 (con't)		
6	73AA	6204
8	AF15	0000
9	00H6	A1F7
10	7ACH	9317
12	573C	7082
13	48C8	7082
A2U2040		
1	A5AU	F27H
2	P9F7	H81F
3	16F9	CC34
4	P9F7	H81F
5	A5AU	F27H
6	H91C	0000
8	3P2H	03FF
9	PP53	3HFU
10	A5AU	F27H
11	P9F7	H81F
12	A788	4506
A2U2050		
1	66U6	CC34
2	HHF2	0000
3	2143	2222
4	9A77	9916
5	7CU0	0000
6	F0F4	CC34
8	3HH3	9820
9	86P7	2314
10	30PA	6A71
11	8CHP	H145
12	A7HU	0000
13	1FPC	CC34
A2U2060		
1	66P4	66P4
2	3350	3350
3	1848	AU41
4	9AHA	2HH3
5	63F1	H4F8

FETCH PREDICTOR		WITHOUT A2J3008
A2U2060 (con't)		
6	8H34	8H34
7	5631	P138
8	CPP9	09P0
9	A623	C440
10	67AU	A9F4
11	526F	5AU9
13	HAC9	97A0
14	PP53	3HFU
15	A5AU	F27H
16	P9F7	H81F
17	4AF2	3F17
19	0CH3	F8C8
22	FP3A	9317
23	81P3	8766
A2U2070		
1	48C8	7082
2	0CH3	F8C8
3	C0P7	738F
4	P9F7	H81F
5	A5AU	F27H
6	7500	
7	FP3A	9317
9	0000	0000
10	81P3	8766
11	3AH7	
12	PP53	3HFU
14	0126	
15	CA12	
A2U3010		
1	72A1	72A1
2	HPC6	6103
3	6582	
4	9109	7903
5	H52F	F237
6	A590	
7	1PA4	A1F7
9	0000	0000
10	957A	7082
11	2P4P	
12	P3P7	1286

FETCH PREDICTOR		WITHOUT A2J3008
A2U3010 (con't)		
14	7CU0	
15	F0F4	
A2U3020		
1	957A	7082
2	1PA4	A1F7
3	HPC6	
4	7CU0	0000
7	1P72	0000
9	55CP	FCC6
10	8CHP	H145
12	00H6	A1F7
A2U3030		
2	UHC2	93A0
3	0000	0000
4	CC34	CC34
6	0000	0000
8	H7C9	CC34
9	6F8H	
10	CC34	CC34
11	0000	0000
12	H91C	0000
A2U3040		
2	0000	0000
3	48C8	7082
4	F189	2823
5	8519	C8U8
6	H9C1	0981
7	1FCF	UP32
8	1842	1842
9	1PA4	A1F7
11	A590	1AU3
12	A376	A376
13	A788	4506
14	6285	C2C5
15	3P2H	03FF
16	7ACH	9317
17	U38F	FCC6

FETCH PREDICTOR		WITHOUT A2J3008
A2U3040 (con't)		
18	CC34	CC34
A2U3050		
1	CC34	CC34
2	0000	0000
3	CC34	CC34
4	H91C	0000
5	H7C9	CC34
6	H526	CC34
8	16F9	CC34
9	1P72	0000
10	PP53	3HFU
11	86P7	2314
12	72AF	1849
13	8CHP	H145
A2U3060		
2	CPP9	09P0
3	6C32	6C32
4	AU99	AU99
5	5631	P138
6	8H34	8H34
7	C83U	C83U
8	PC01	PC01
9	63F1	H4F8
11	0000	0000
12	9AHA	2HH3
13	63U7	63U7
14	AC88	AC88
15	1848	AU41
16	3350	3350
17	U86C	U86C
18	CF10	CF10
19	66P4	66P4
SELF-TEST BOARD		
A3U1025		
1	CC34	

SELF-TEST BOARD	
A3U1025 (con't)	
3	0000
5	0000
6	CC34
11	CC34
A3U1029	
2	0000
3	CC34
4	0000
5	0000
6	CC34
8	0000
11	0000
12	CC34
A3U1035	
2	476C
3	H006
4	14AH
5	66P9
6	7449
7	030C
8	5035
9	F880
11	CC34
12	UP44
13	H8F3
14	10CF
15	0532
16	7719
17	435U
18	0724
19	PC1C
A3U2029	
2	0000
10	826P
11	H58A
12	77F7
13	85PA

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SELF-TEST BOARD	
A3U2029 (con't)	
14	7P25
15	C3F2
A3U3025	
2	0000
11	5CP0
12	P5PH
13	725C
14	96PF
15	826P
A3U3029	
1	CC34
2	96PF
3	725C
4	P5PH
5	5CP0
6	H006
7	14AH
8	030C
9	5035
11	H8F3
12	10CF
13	435U
14	0724
16	7P25
17	85PA
18	77F7
19	H58A
A3U3035	
1	66P9
2	96PF
3	6UA2
4	725C
5	3H97
6	P5PH
7	02U2
8	5CP0
9	8P34

SELF-TEST BOARD	
A3U3035 (con't)	
11	7P25
12	3612
13	85PA
14	A6PF
15	77F7
16	H5HH
17	H58A
18	4046
19	66P9

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

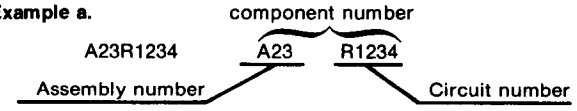
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

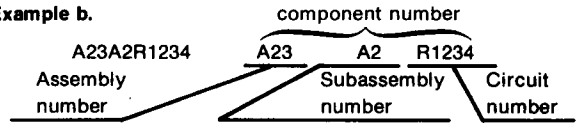
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
15238	ITT SEMICONDUCTORS, A DIVISION OF INTER NATIONAL TELEPHONE AND TELEGRAPH CORP.	P.O. BOX 168, 500 BROADWAY	LAWRENCE, MA 01841
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91418	RADIO MATERIALS COMPANY, DIV. OF P.R. MALLORY AND COMPANY, INC.	4242 W BRYN MAWR	CHICAGO, IL 60646
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
95348	GORDOS CORPORATION	250 GLENWOOD AVENUE	BLOOMFIELD, NJ 07003

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-7368-00			CKT BOARD ASSY:BUFFER	80009	670-7368-00
A2	670-7369-00			CKT BOARD ASSY:FETCH PREDICTOR	80009	670-7369-00
A3	670-7370-00			CKT BOARD ASSY:SELF TEST	80009	670-7370-00
A4	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
A4	----- -----			(NO ELECTRICAL PARTS)		
A1	----- -----			CKT BOARD ASSY:BUFFER		
A1C1015	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C1023	283-0168-00			CAP.,FXD,CER DI:12PF,5%,100V	72982	8101B121C0G0120J
A1C1024	283-0342-00			CAP.,FXD,CER DI:6.5PF,0.5%,2000V	91418	HV6R5D2024R0
A1C1029	283-0330-00			CAP.,FXD,CER DI:100PF,5%,50V	51642	150-050-NP0-101J
A1C1032	283-0157-00			CAP.,FXD,CER DI:7PF,5%,500V	72982	8111B064C0H0709J
A1C1034	281-0700-00			CAP.,FXD,CER DI:3.3PF,10%,200V	59660	374005S3B0339K
A1C1038	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C3009	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C5041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6031	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C6041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C7041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C7046	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C7047	283-0177-00			CAP.,FXD,CER DI:1UF,+80-20%,25V	56289	273C5
A1C7048	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1CR1027	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1028	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR1037	152-0071-00			SEMICOND DEVICE:GERMANIUM,15V,40MA	15238	G865
A1CR1038	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR1039	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR2007	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR2008	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR2018	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR2019	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR7018	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1CR7019	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A1Q1043	151-0282-00			TRANSISTOR:SILICON,NPN	80009	151-0282-00
A1Q1046	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1Q1048	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1R1015	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A1R1025	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A1R1026	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1R1028	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R1033	321-0274-00			RES.,FXD,FILM:6.98K OHM,1%,0.125W	91637	MFF1816G69800F
A1R1035	321-0286-00			RES.,FXD,FILM:9.31K OHM,1%,0.125W	91637	MFF1816G93100F
A1R1036	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R1038	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R1039	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R1045	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A1R2005	301-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.50W	01121	EB4315
A1R2017	315-0301-02			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A1R2035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R3035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R3046	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R4007	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A1R4035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R5046	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R6045	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A1R7018	315-0470-03			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A1R7035	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R7042	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A1U1002	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U1004	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U1018	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A1U1031	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A1U2018	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U2025	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A1U2035	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A1U2045	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A1U3008	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U3024	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U3025	156-0866-02			MICROCIRCUIT,DI:13 INP NAND GATES,SCRN	80009	156-0866-02
A1U3045	156-1059-01			MICROCIRCUIT,DI:DUAL J-K EDGETRIGGERED	01295	SN74LS109A
A1U4025	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 ST OUT	27014	N74LS240N
A1U4035	160-1351-00			MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-1351-00
A1U4045	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A1U5018	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U5025	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 ST OUT	27014	N74LS240N
A1U5035	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A1U5045	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A1U6004	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U6025	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A1U6035	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-04
A1U6045	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A1U7024	155-0260-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0260-00
A1U7025	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A1U7035	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 ST OUT	27014	N74LS240N
A1VR1045	152-0611-00			SEMICOND DEVICE:ZENER,0.4W,9V,2%	80009	152-0611-00
A1VR6003	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	04713	SZG35008

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	----- -----			CKT BOARD ASSY:FETCH PREDICTOR		
A2C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1070	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2070	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4012	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10 V	54473	ECE-B1AV470S
A2C4060	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2R4028	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R4038	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A2R4040	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A2U1010	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U1020	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A2U1030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U1040	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74LS10NP3
A2U1050	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A2U1060	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A2U1070	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A2U2010	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A2U2020	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A2U2030	156-0481-02			MICROCIRCUIT,DI:TRIPLE 3 INP & GATE	27014	DM74LS11NA+
A2U2040	156-0718-03			MICROCIRCUIT,DI:TRIPLE 3-INP NOR GATE	01295	SN74LS27
A2U2050	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A2U2060	160-1352-00			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGM	80009	160-1352-00
A2U2070	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A2U3010	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A2U3020	156-0874-02			MICROCIRCUIT,DI:8 BIT ADDRESSABLE LCH	80009	156-0874-02
A2U3030	156-0331-03			MICROCIRCUIT,DI:DUAL D TYPE POSITIVE EDGE	80009	156-0331-03
A2U3040	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 ST OUT	18324	N74LS240N
A2U3050	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U3060	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	----- -----			CKT BOARD ASSY:SELF TEST		
A3C1015	283-0711-00			CAP.,FXD,MICA D:2700PF,2%,500V	00853	D195E272G0
A3C1025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C1024	283-0649-00			CAP.,FXD,MICA D:105PF,1%,300V	00853	D153F1050F0
A3C1035	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C1043	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C1045	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C2015	283-0711-00			CAP.,FXD,MICA D:2700PF,2%,500V	00853	D195E272G0
A3C2016	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C2017	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C3019	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C3025	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C3029	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C3032	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3C3036	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A3CR2016	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3K2025	148-0076-00			RELAY,REED:1 FORM A,5V,0.25A,100V	95348	F81-1447
A3L2015	108-0683-00			COIL,RF:900MH	80009	108-0683-00
A3Q1017	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3R1017	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A3R1023	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A3R1035	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A3R2015	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R3037	307-0650-00			RES NTWK,FXD,FI:9,2.7K OHM,5%,0.150W	32997	4310R-101-272
A3R3041	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A3R3043	307-0721-00			RES NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A3U1025	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A3U1029	156-0721-02			MICROCIRCUIT,DI:QUAD 2-IN NAND SCHMITT TRI	04713	SN74LS132NDS
A3U1035	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	07263	74LS374
A3U2029	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A3U3025	156-0784-02			MICROCIRCUIT,DI:SYNC 4 BIT BINARY COUNTER	27014	DM74LS163ANA+
A3U3029	160-1346-00			MICROCIRCUIT,DI:512 X 8 EPROM	80009	160-1346-00
A3U3035	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

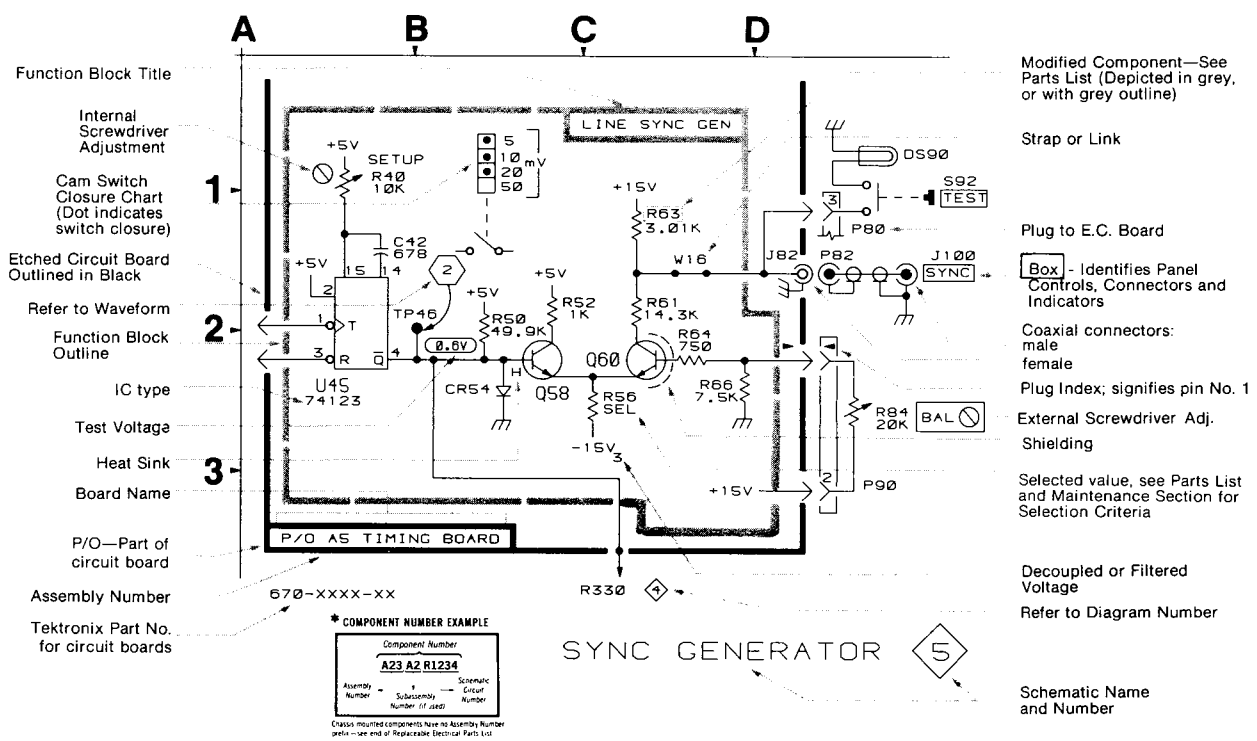
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



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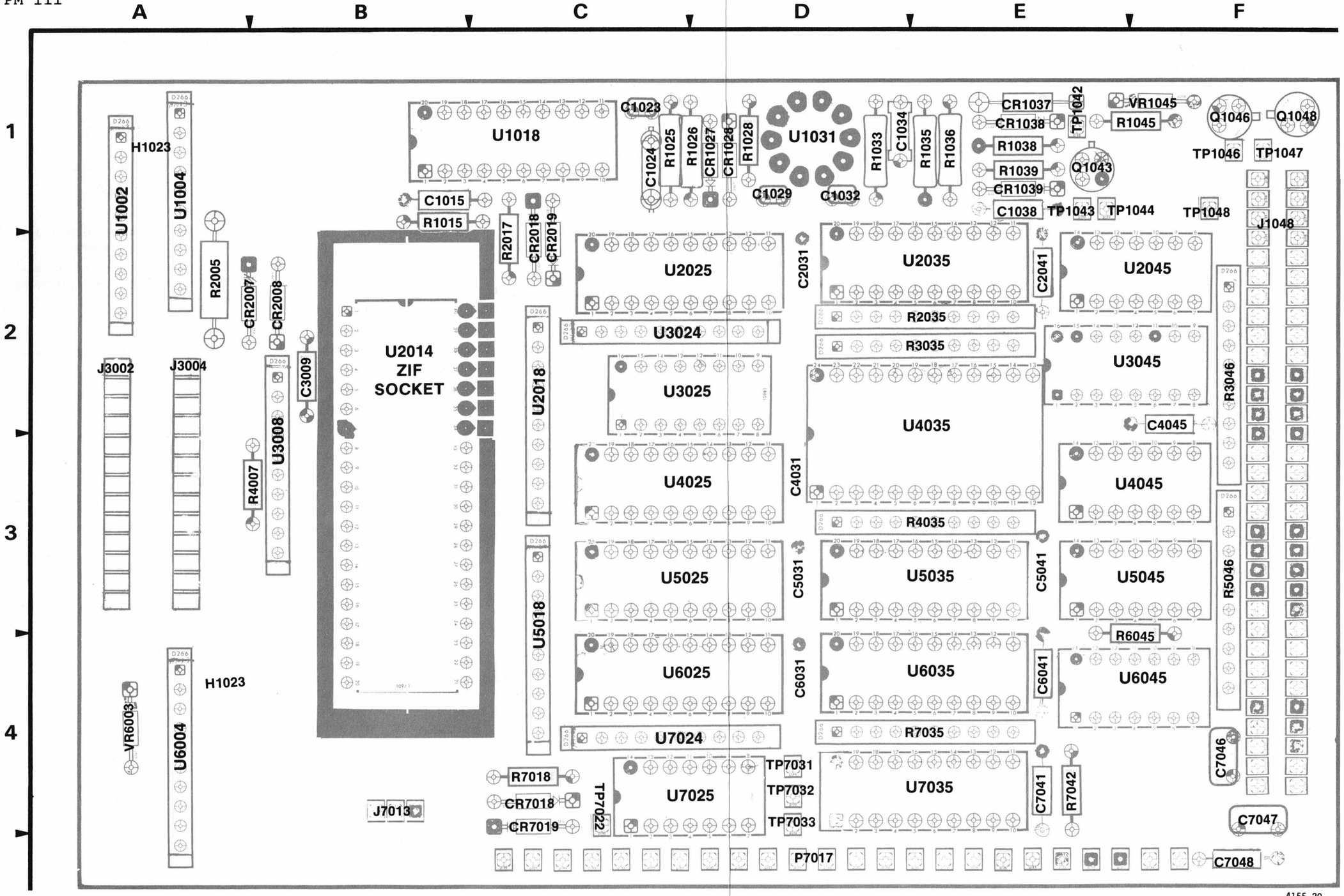


Figure 8-1. A1 - Upper board component locations.

Table 8-1
IC PIN INFORMATION

DEVICE TYPE	VCC	GND
2716	24	12
74LS00	14	7
74LS02	14	7
74LS04	14	7
74LS08	14	7
74LS10	14	7
74LS11	14	7
74LS20	14	7
74LS27	14	7
74S74(LS)	14	7
74LS109	16	8
74LS132	14	7
74LS133	16	8
74LS163	16	8
74LS175	16	8
74LS240	20	10
74LS244	20	10
74LS259	16	8
74LS374	20	10
74LS472	20	10
H1023	10	1

nsitive Devices
ıtenance Section

IUMBER EXAMPLE

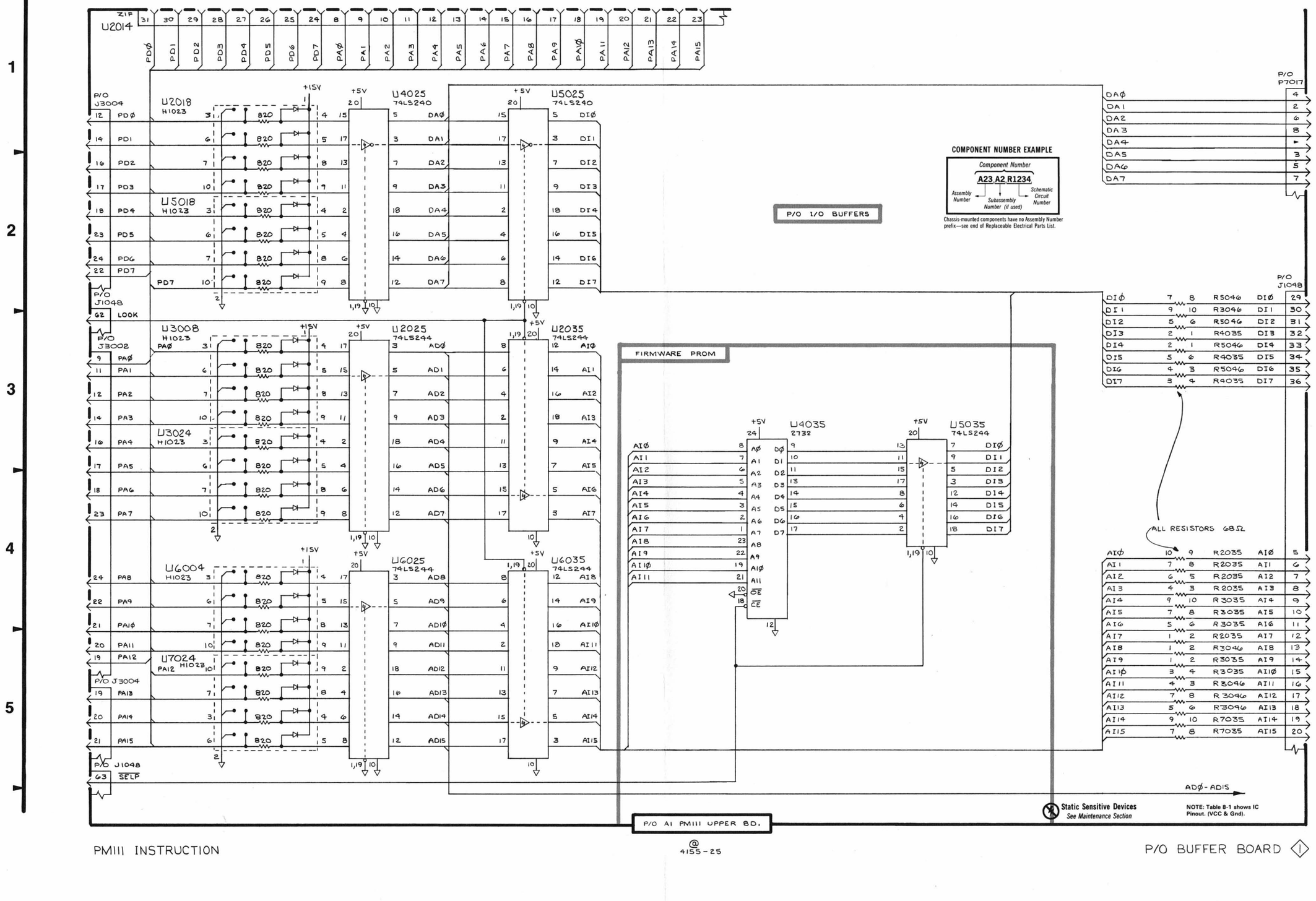
ınent Number
A2,R1234
Schematic Circuit Number
assembly ıer (if used)

ıents have no Assembly Number
ıceable Electrical Parts List.

BUFFER BOARD ◇1

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1048	F2	F1
J1048	A5	F1
J1048	F3	F1
J1048	F4	F1
J1048	A2	F1
J1048	F5	F1
J3002	A3	A3
J3002	A4	A3
J3002	A5	A3
J3004	A2	A3
J3004	A5	A3
J3004	A1	A3
P7017	F1	E5
P7017	F2	E5
R2035	F5	E2
R2035	F4	E2
R3035	F5	E2
R3035	F4	E2
R3046	F5	F2
R3046	F2	F2
R4035	F3	E3
R5046	F2	F3
R5046	F3	F3
R7035	F5	E4
U2014	D1	B2
U2014	B1	B2
U2014	A1	B2
U2014	C1	B2
U2018	A1	C2
U2025	B3	C2
U2035	C3	E2
U3008	A3	B2
U3024	A3	C2
U4025	B1	C3
U4035	D3	E2
U5018	A2	C3
U5025	C1	C3
U5035	E3	E3
U6004	A4	A4
U6025	B4	C4
U6035	C4	E4
U7024	A5	C4



A1—UPPER BOARD ⟨1⟩

PM111 INSTRUCTION

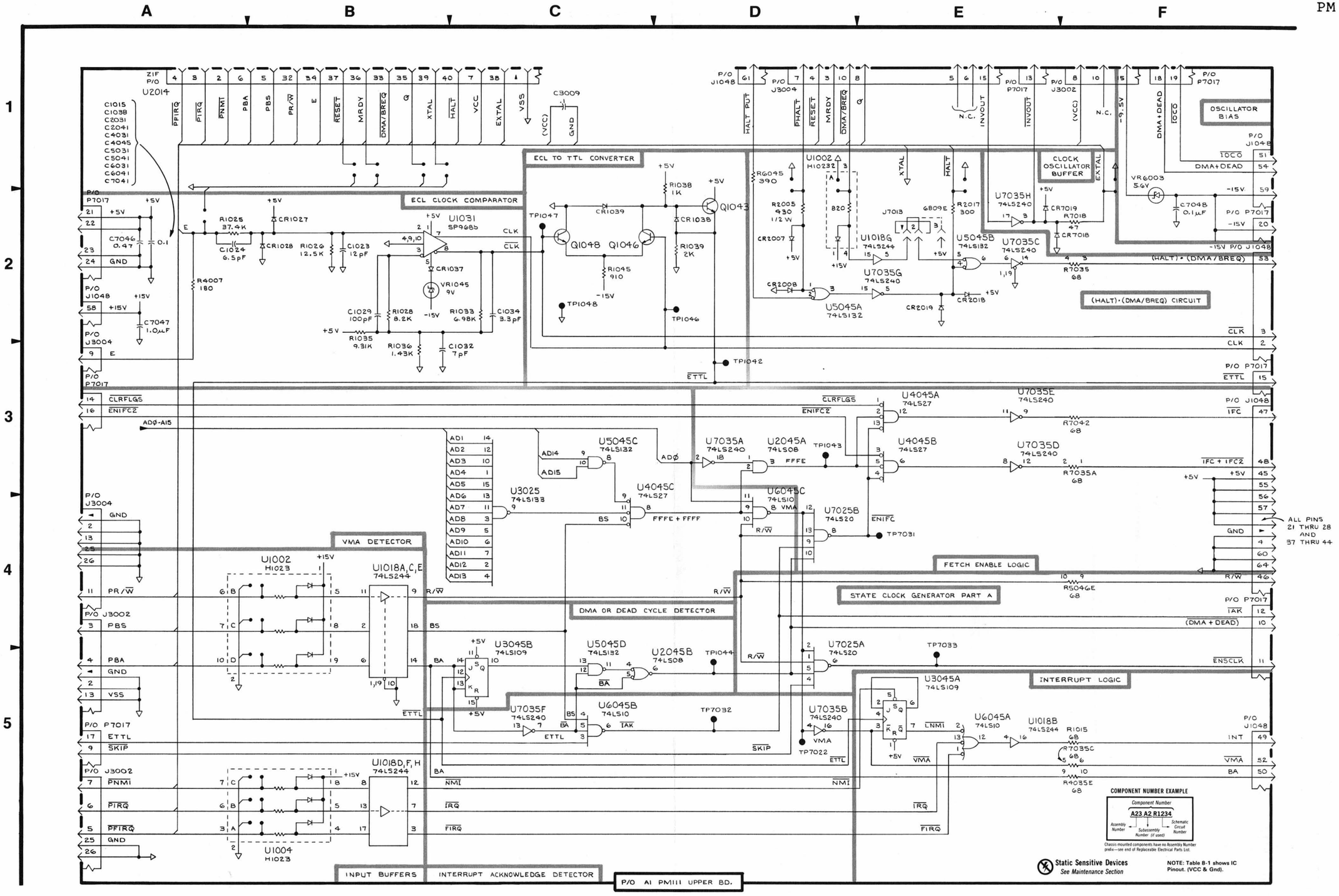
@ 4155-25

P/O BUFFER BOARD ⟨1⟩

BUFFER BOARD

ASSEMBLY A01

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1015	A2	B1	R1033	C2	D1
C1023	B2	C1	R1035	B2	E1
C1024	A2	C1	R1036	B3	E1
C1029	B2	D1	R1038	D1	E1
C1032	B3	D1	R1039	D2	E1
C1034	C2	D1	R1045	C2	F1
C1038	A2	E1	R2005	D2	A2
C2031	A2	D2	R2017	E2	C2
C2041	A2	E2	R4007	A2	B3
C3009	C1	B2	R4035	F5	E3
C4031	A2	D3	R5046	F4	F3
C4045	A2	F2	R6045	D1	F4
C5031	A2	D3	R7018	F2	C4
C5041	A2	E3	R7035	F3	E4
C6031	A2	D4	R7035	F5	E4
C6041	A2	E4	R7035	F2	E4
C7041	A2	E4	R7042	F3	E4
C7046	A2	F4	TP1042	D3	E1
C7047	A2	F4	TP1043	D3	E1
C7048	F2	F5	TP1044	D5	E1
CR1027	B2	D1	TP1046	D2	F1
CR1028	B2	D1	TP1047	C2	F1
CR1037	B2	E1	TP1048	C2	F1
CR1038	D2	E1	TP7022	D5	C4
CR1039	C2	E1	TP7031	E4	D4
CR2007	D2	A2	TP7032	D5	D4
CR2008	D2	B2	TP7033	E5	D4
CR2018	E2	C2	U1002	D1	A1
CR2019	E2	C2	U1002	B4	A1
CR7018	E2	C4	U1004	B5	A1
CR7019	E2	C4	U1018	B4	C1
J1048	F4	F1	U1018	B5	C1
J1048	F1	F1	U1018	E5	C1
J1048	D1	F1	U1018	E2	C1
J1048	F2	F1	U1031	B2	D1
J1048	A2	F1	U2014	B1	B2
J1048	F5	F1	U2014	C1	B2
J1048	F3	F1	U2014	A1	B2
J1048	F3	F1	U2045	C5	F2
J3002	F1	A3	U2045	D3	F2
J3002	A4	A3	U3025	C4	C2
J3002	A5	A3	U3045	C5	F2
J3004	A3	A3	U3045	E5	F2
J3004	A4	A3	U4045	C4	F3
J3004	D1	A3	U4045	E3	F3
J3004	E1	A3	U5045	E2	F3
J7013	E2	B4	U5045	C3	F3
P7017	F4	E5	U5045	D2	F3
P7017	F2	E5	U5045	C5	F3
P7017	F1	E5	U6045	C5	F4
P7017	E1	E5	U6045	D4	F4
P7017	A5	E5	U6045	E5	F4
P7017	A3	E5	U7025	D4	C4
P7017	A2	E5	U7025	D5	C4
P7017	F3	E5	U7035	C5	E4
Q1043	D2	E1	U7035	E2	E4
Q1046	C2	F1	U7035	E3	E4
Q1048	C2	F1	U7035	E2	E4
R1015	F5	B2	U7035	E2	E4
R1025	A2	C1	U7035	D5	E4
R1026	B2	D1	U7035	D3	E4
R1028	B2	D1	VR1045	B2	F1
			VR6003	F1	A4

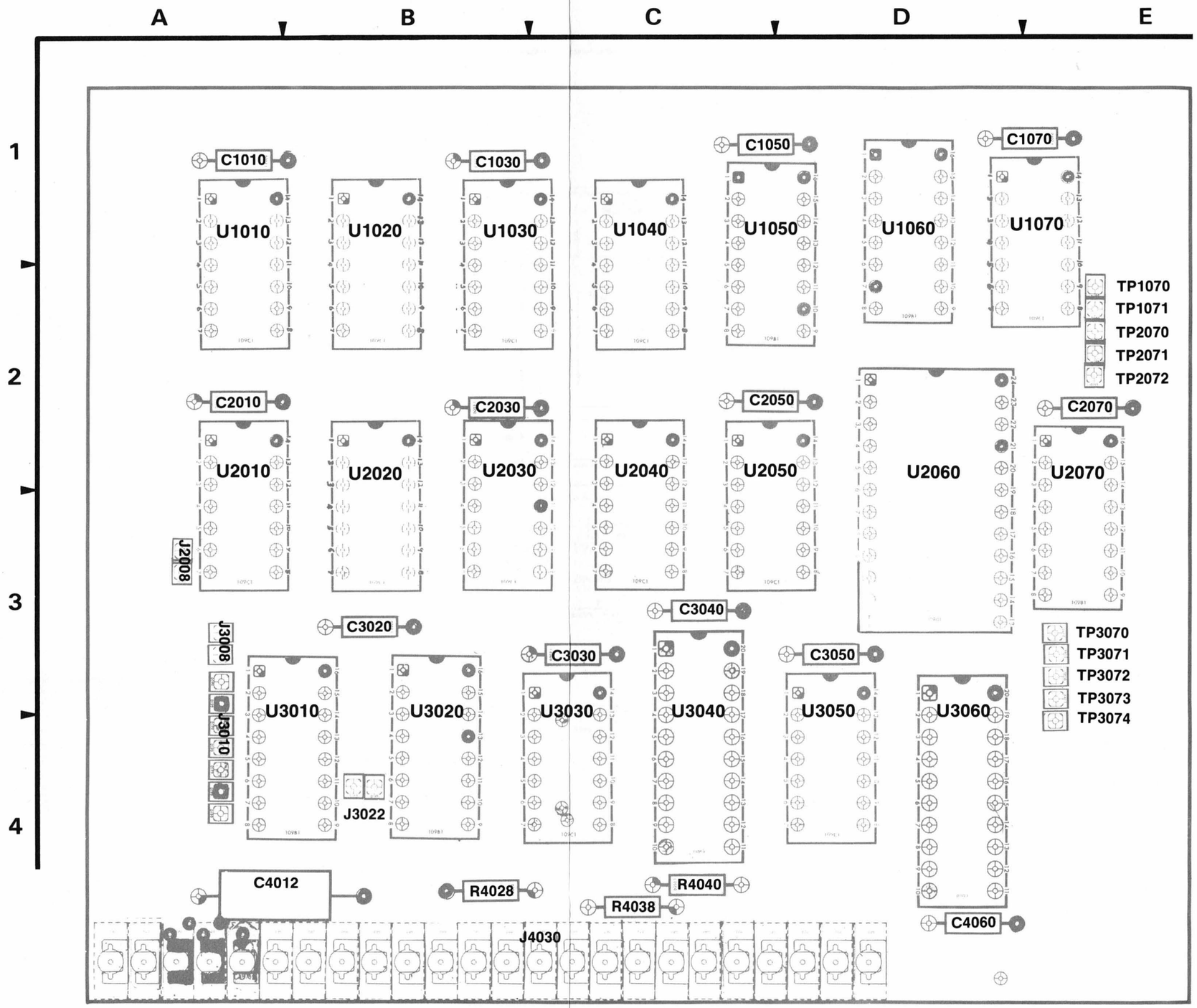


PMIII INSTRUCTION

@ 4155-26

P/O BUFFER BOARD ◇2

A1—UPPER BOARD ◇2



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

4155-19

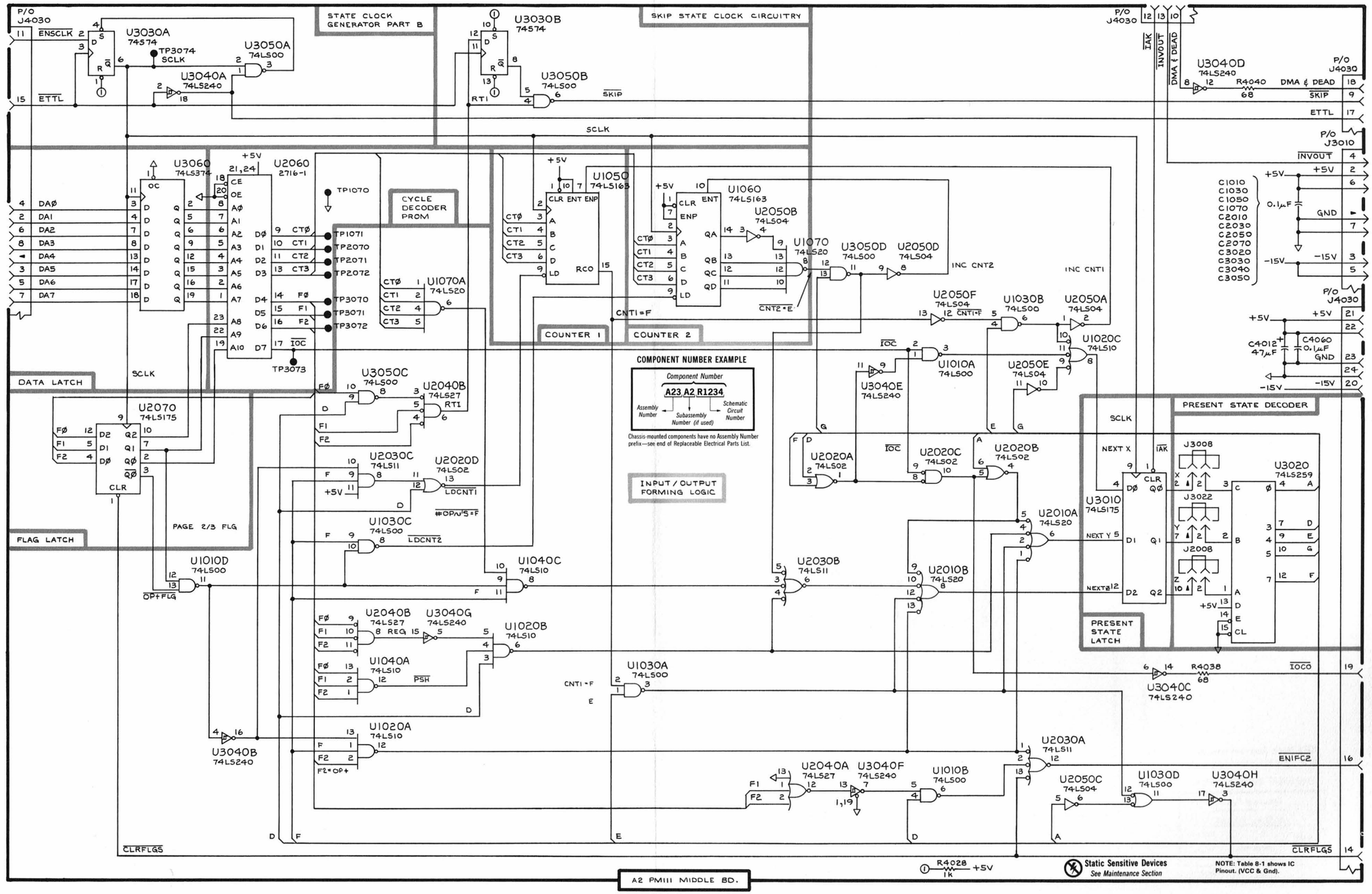
Figure 8-2. A2 - Middle board component locations.

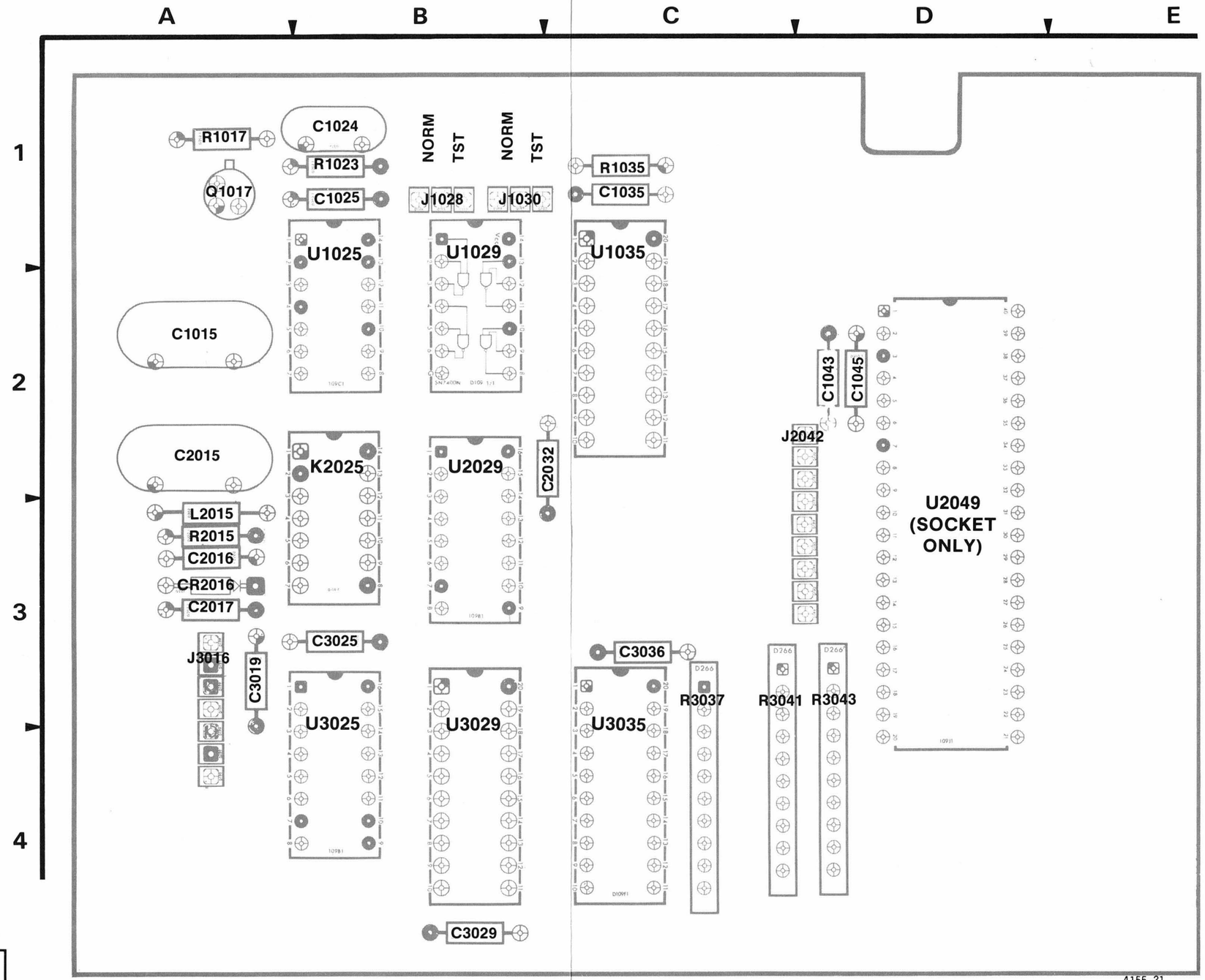
@

FETCH PREDICTOR ◈3

ASSEMBLY A02

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	F2	A1	U1030	C5	B1
C1030	F2	B1	U1030	F5	B1
C1050	F2	C1	U1040	B5	C1
C1070	F2	E1	U1040	C4	C1
C2010	F2	A2	U1050	C2	C1
C2030	F2	B2	U1060	D2	D1
C2050	F2	C2	U1070	D2	E1
C2070	F2	E2	U1070	C2	E1
C3020	F2	B3	U2010	E4	A2
C3030	F2	C3	U2010	E4	A2
C3040	F2	C3	U2020	D3	B2
C3050	F2	D3	U2020	E3	B2
C4012	F3	A4	U2020	E3	B2
C4060	F3	D4	U2020	C3	B2
J2008	F4	A3	U2030	D4	B2
J3008	F3	A3	U2030	B3	B2
J3010	F2	A3	U2030	E5	B2
J3022	F4	B4	U2040	B4	C2
J4030	A2	C5	U2040	D5	C2
J4030	A1	C5	U2040	C3	C2
J4030	F5	C5	U2050	E2	C2
J4030	F3	C5	U2050	D2	C2
J4030	F2	C5	U2050	E2	C2
J4030	F1	C5	U2050	E3	C2
R4028	A1	B4	U2050	E2	C2
R4028	C1	B4	U2050	E5	C2
R4028	E5	B4	U2060	B2	D2
R4038	F5	C4	U2070	A3	E2
R4040	F1	C4	U3010	F4	B3
TP1071	B2	E2	U3020	F4	B3
TP2070	B2	E2	U3030	A1	C3
TP2071	B2	E2	U3030	C1	C3
TP2072	B2	E2	U3040	D3	C3
TP3070	B2	E3	U3040	F5	C3
TP3071	B2	E3	U3040	F5	C3
TP3072	B2	E3	U3040	A1	C3
TP3073	B3	E3	U3040	D5	C3
TP3074	A1	E4	U3040	F1	C3
U1010	E3	A1	U3040	B5	C3
U1010	A4	A1	U3040	C4	C3
U1010	E5	A1	U3050	D2	D4
U1020	B5	B1	U3050	B1	D4
U1020	E3	B1	U3050	B3	D4
U1020	C4	B1	U3050	C1	D4
U1030	E2	B1	U3060	A2	D4
U1030	B4	B1			





Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List-

A3—LOWER BOARD

@

Figure 8-3. A3 - Lower board component locations.

SELF-TEST BOARD ◇4

ASSEMBLY A03		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1015	B3	A2
C1024	C3	B1
C1025	B4	B1
C1035	B4	C1
C1043	E4	D2
C1045	B4	D2
C2015	A3	A2
C2016	B4	A3
C2017	A3	A3
C3019	A3	A3
C3025	B4	B3
C3029	B4	B4
C2032	B4	C2
C3036	B4	C3
CR2016	A4	A3
J1028	A2	B1
J1030	B4	B1
J2042	D4	D2
J2042	C4	D2
J3016	A2	A3
J3016	A3	A3
K2025	B4	A3
L2015	A4	A3
Q1017	B4	A1
R1017	C3	A1
R1023	B4	B1
R1035	E1	C1
R2015	B3	A3
R3037	D3	C3
R3041	E3	C3
R3043	E3	D3
U1025	C3	B1
U1025	B2	B1
U1029	B4	B1
U1029	B2	B1
U1029	A2	B1
U1029	B2	B1
U1035	E1	C1
U2029	C1	B2
U2049	E4	D2
U2049	E1	D2
U2049	B4	D2
U2049	E3	D2
U2049	A4	D2
U2049	E2	D2
U3025	B1	B3
U3029	D1	B3
U3035	D3	C3

A B C D E F

1 2 3 4

CLOCK DIVIDER

CYCLE COUNTERS

CYCLE GENERATOR PROM

CONTROL LINE LATCH

P/O U2049

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
(Assembly Number / Subassembly Number (if used) / Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

U3025 74LS163 — ENT, ENP, LD, CLR, RCO, QA, QB, QC, QD, TA, TB, TC, TD

U2029 74LS163 — ENT, ENP, LD, CLR, QA, QB, QC, QD, TE, TF, TG, TH

U3029 74S472 — A, B, C, D, E, F, G, H, I, S, TA–TH, Q0–Q7, D0–D7

U1035 74LS374 — D1–D8, Q1–Q8, EN, R/W, VMA, BS, BA, FIRQ, NMI, DMA/BREQ, HALT

R1035 68

U1025B 74LS74

U1029A 74LS132

U1029C 74LS132

U1029B 74LS132

U1025A 74LS74

J3016 — INVOUT

NORM J1028

TEST

LOAD PULSE GENERATOR

tpw ≈ 115 ns

LOAD VMA

R1017 1.5K 1%

C1024 105 pF

SELF TEST OSCILLATOR

+5V IN

GND

C2017 .1µF

C3019 .1µF

-15V

R2015 10K

C1015 2700 pF

C2015 2700 pF

L2015 900 nH

Q1017

U1029D 74LS132 OSC

R1023 3K

C1025 .1µF

TEST J1030

NORM

R3037 2.7K

U3035 74LS244 — TA, TB, TC, TD, TE, TF, TG, TH

R3041 68Ω

R3043 68Ω

A0–A15

VMA AND ADDRESS GENERATOR

K2025

CR2016

C2016 .1µF

C1045 .1µF

VSS

EXTAL

P/O U2049

C2032, C1035, C3025, C3029, C3036 .1µF

SELF TEST POWER CIRCUIT

A3 PMIII LOWER BD.

U2042

Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

C1043 .1µF

IRQ, VCC, Q, MRDY, RESET, XTAL

SELF TEST STIMULUS OUTPUT

PMIII INSTRUCTION

@ 4155-28

SELF-TEST BOARD ◇4

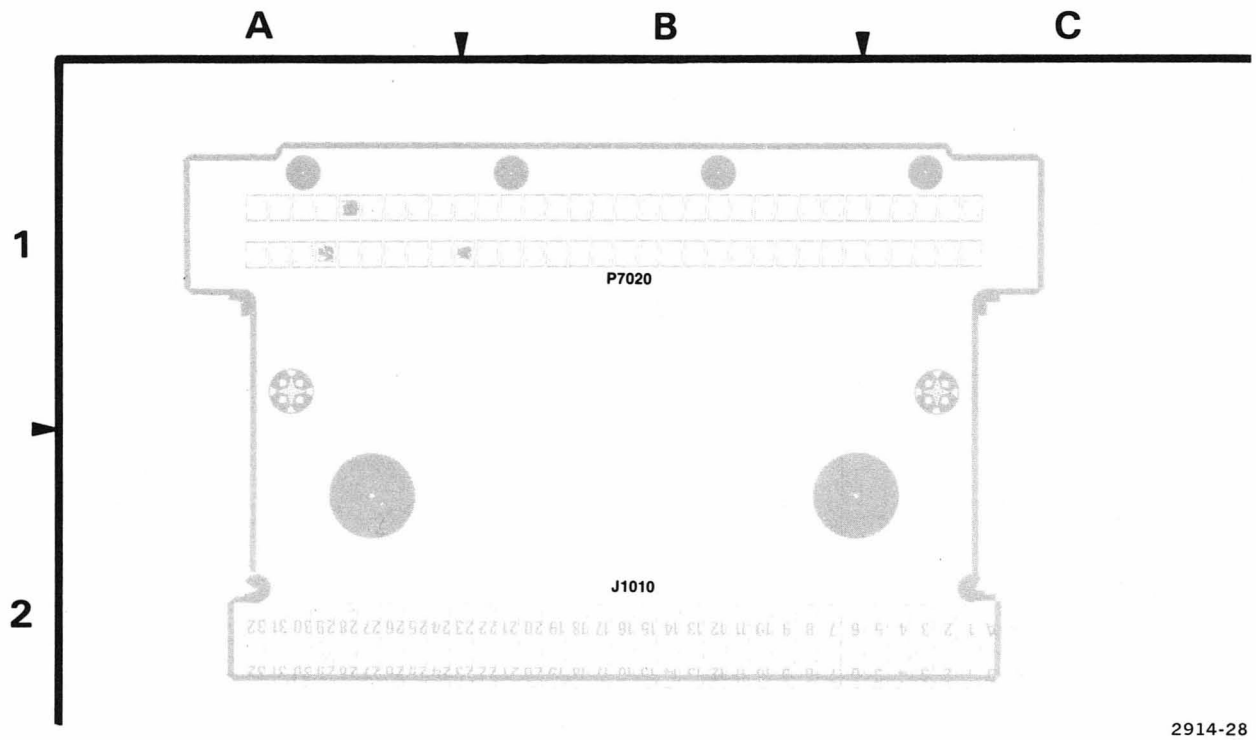


Figure 8-4. Logic analyzer plug board.

P/O J1010		P/O P7020
5	UDS (AIØ)	5
6	AI1	►
7	AI2	7
8	AI3	4
9	AI4	9
10	AI5	6
11	AI6	8
12	AI7	11
13	AI8	12
14	AI9	13
15	AI10	15
16	AI11	14
17	AI12	17
18	AI13	16
19	AI14	19
20	AI15	18
21	AI16 (+5V)	21
22	AI17 (+5V)	22
23	AI18 (+5V)	23
24	AI19 (+5V)	24
25	AI20 (+5V)	26
26	AI21 (+5V)	25
27	AI22 (+5V)	28
28	AI23 (+5V)	27
58	$+15V_D$	58
56	+5V	45
57		57
45		10
◄	GND	20
4		30
60		40
64		50
59	$-15V_D$	59

A4 PM111 LOGIC ANALYZER PLUG BD.

@ 4155-29

PM111 INSTRUCTION

P/O J1010		P/O P7020
29	DIØ	32
30	DI1	29
31	DI12	34
32	DI3	31
33	DI4	33
34	DI5	36
35	DI6	35
36	DI7	38
37	DI8 (+5V)	42
38	DI9 (+5V)	37
39	DI10 (+5V)	39
40	DI11 (+5V)	44
41	DI12 (+5V)	41
42	DI13 (+5V)	46
43	DI14 (+5V)	43
44	DI15 (+5V)	48
46	CØ (R/$\overline{W}$)	47
47	C1 ($\overline{IFC}$)	52
48	C2 ($\overline{IFC+IFC2}$)	49
49	C3 (INT)	54
50	C4 (BA)	56
51	C5 ($\overline{IOCO}$)	51
52	C6 ($\overline{VMA}$)	60
53	C7 (DMA/BREQ)·(HALT)	53
54	C8 (DMA+DEAD)	62
55	C9 (+5V)	55
63	$\overline{SELP}$	63
61	$\overline{HALT}$ ($\overline{HALT\ PUT}$)	61
2	CLOCK (CLK)	2
3	$\overline{CLOCK}$ (CLK)	3
62	LOOK	64

COMPONENT NUMBER EXAMPLE

Component Number

A23 A2 R1234

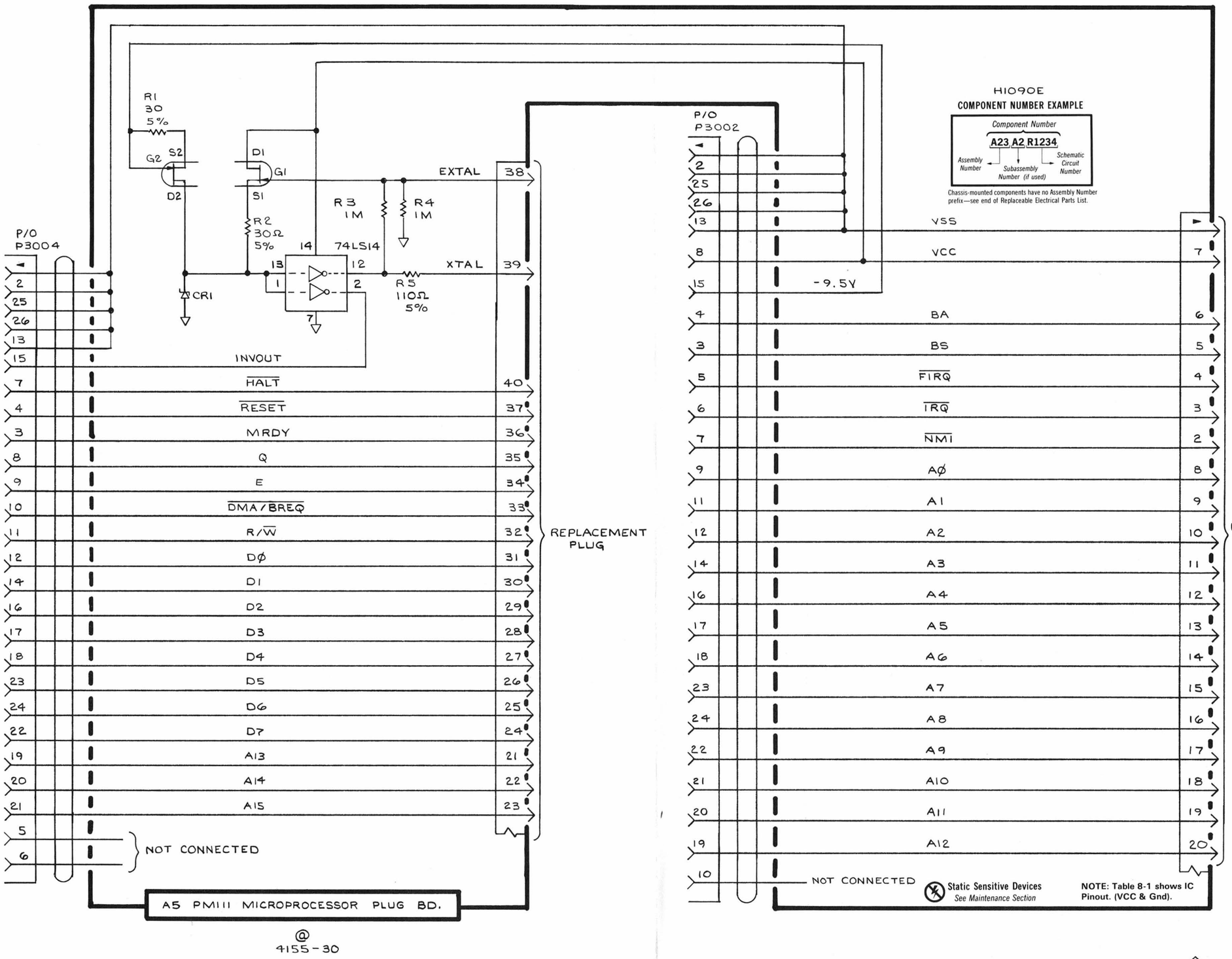
Assembly Number — *Subassembly Number (if used)* — *Schematic Circuit Number*

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & Gnd).

LOGIC ANALYZER PLUG 5



PMIII INSTRUCTION

MICROPROCESSOR PLUG ⑥

H1090E
COMPONENT NUMBER EXAMPLE

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83294	ARROW FASTENER CO., INC.	271 MAYHILL ST.	SADDLE BROOK, NJ 07662
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-4421-00			1		MARKER,IDENT:6809 POD LABEL	80009	334-4421-00
-2	380-0593-04			1		HSG HALF,CKT BD:TOP	80009	380-0593-04
						(ATTACHING PARTS)		
-3	211-0306-00			4		SCREW,CAP:4-40 X 1.125,HEX,SKT HD	83294	OBD
						- - - * - - -		
-4	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
						(ATTACHING PARTS)		
-5	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-6	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-7	200-2429-00			1		CABLE NIP,ELEC:0.69 L X 3.6 W,PLASTIC	80009	200-2429-00
	175-6184-00			1		CA ASSY,SP,ELEC:132,33 AWG,6809 PROBE	80009	175-6184-00
-8	386-4683-00			1		. PLATE,PIN PROT:40 PIN,NYLON	80009	386-4683-00
-8.1	200-2445-00			1		. COVER,PROBE:PIN PROTECTOR,PLASTIC	80009	200-2445-00
-9	204-0907-00			1		. BODY HALF,PROBE:BOTTOM,40 PIN,NYLON	80009	204-0907-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
						(ATTACHING PARTS)		
-10	211-0112-00			2		. SCREW,MACHINE:2-56 X 0.375,FLH,100 DEG	83385	OBD
						- - - * - - -		
-11	155-0254-00			1		. MICROCIRCUIT,LI:6809 EMULATOR PROBE	80009	155-0254-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-12	175-6272-00			1		. CA ASSY,SP,ELEC:66,33 AWG,18.5 L,RIBBON	80009	175-6272-00
	----- -----			-		. (REFER TO MAINTENANCE SECTION)		
-13	334-3281-00		B010100X	1		. . MARKER,IDENT:MARKED DRIVER/RECEIVER	80009	334-3281-00
-14	334-3280-00		B010100X	1		. . MARKER,IDENT:MARKED DRIVER/RECEIVER	80009	334-3280-00
	131-2749-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2749-00
-15	334-3722-00			1		. PLATE,IDENT:P6460 MICROPROC PROBE	80009	334-3722-00
-16	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-17	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-18	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-19	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	OBD
						- - - * - - -		
-20	380-0590-01			1		. HSG,HALF:	80009	380-0590-01
-21	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-22	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05ID,PLASTIC	80009	200-2412-00
-23	175-4741-01			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L,RIBBON	80009	175-4741-01
-24	213-0055-00			4		. SCR,TPG,THD FOR:2-32 X 0.188 INCH,PNH STL	93907	OBD
-25	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A4 REPL)		
-26	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-27	----- -----			1		CKT BOARD ASSY:BUFFER(SEE A1 REPL)		
-28	136-0537-00			1		. SOCKET,PLUG-IN:40 PIN,W/LOCKING LEVER	19613	240-0333-00-0602
-29	131-0608-00			103		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-30	131-0787-00			26		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-31	131-0590-00			24		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-32	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-33	136-0269-00			1		. SOCKET,PLUG-IN:14 CONTACT,LOW CLEARANCE	73803	CS9002-14
-34	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-35	136-0634-00			9		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-36	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-37	361-0998-00			8		SPACER,CKT BD:0.245 ID X 0.380 OD X 0.23 H	80009	361-0998-00
-38	175-4667-00			1		CA ASSY,SP,ELEC:7,26 AWG,4.0 L,RIBBON	80009	175-4667-00
-39	----- -----			1		CKT BOARD ASSY:FETCH PREDICTOR(SEE A2 REPL)		
-40	131-1425-00			1		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-41	131-0993-00			3		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-42	136-0263-04			24		. SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-43	----- -----			1		CKT BOARD ASSY:SELF TEST(SEE A3 REPL)		
-44	337-2975-00			1		. SHIELD,ELEC:ACCESS DOOR	80009	337-2975-00
-45	131-0608-00			9		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-46	131-0993-00			2		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-47	131-1425-00			1		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-48	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-49	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
-50	380-0652-01			1		HSG HALF,CKT BD:BOTTOM	80009	380-0652-01

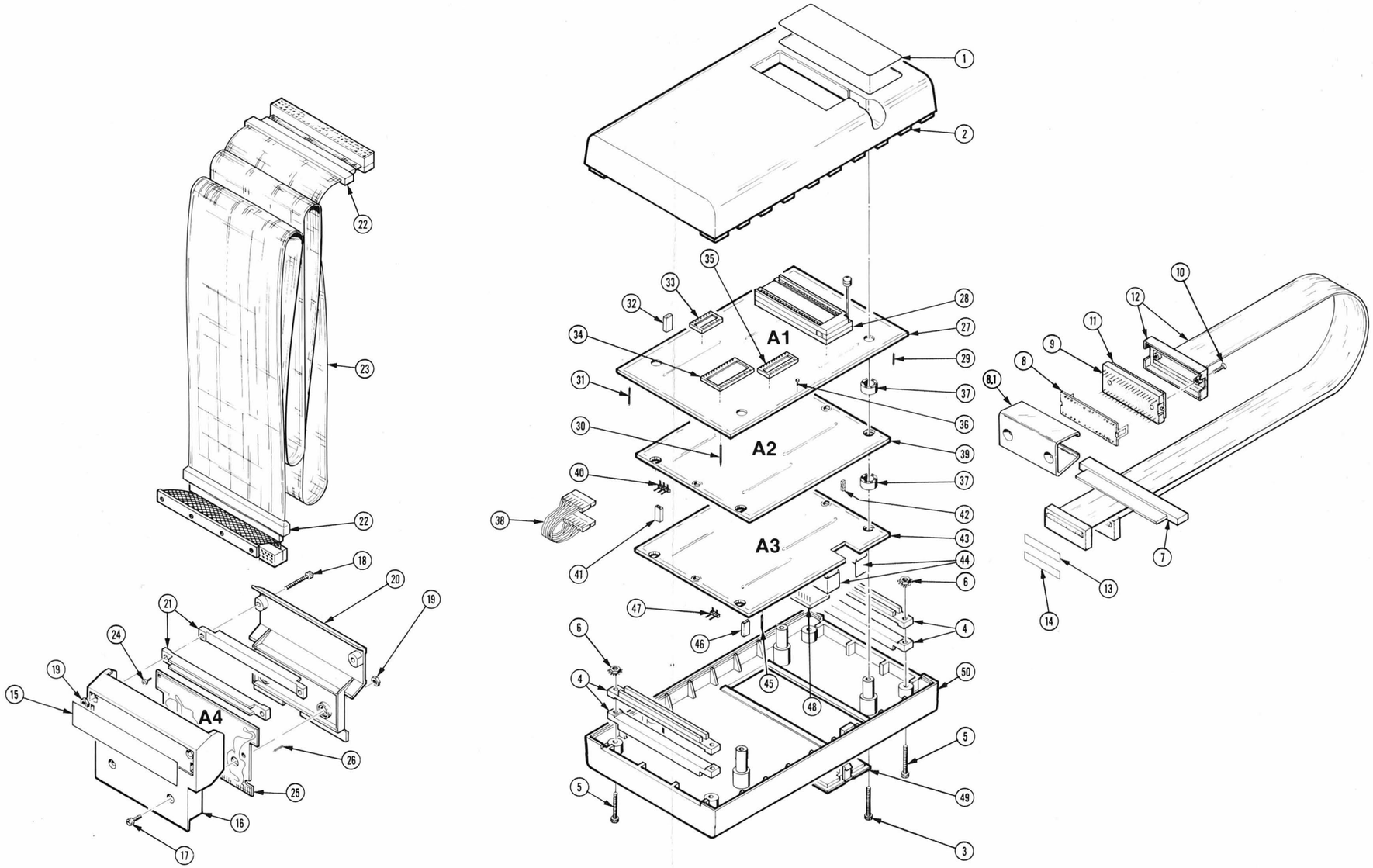


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	070-4155-00			1		MANUAL,TECH:INSTRUCTION	80009	070-4155-00

@

SIGNAL GLOSSARY

This section contains an alphabetical listing of the signals which go to or from the PM 111 Personality Module, as well as a brief description of each signal.

SIGNAL	DESCRIPTION
AI0-AI15	The buffered, bidirectional, 16-bit address bus from the personality module to the logic analyer.
BA	The Bus Available (BA) line from the system under test to the personality module; buffered from the processor, becoming control line C4 from the personality module to the logic analyzer. The signal indicates that the address and data buses, as well as the Read/Write line, are in the high impedance state. The signal can be used to indicate to bus-sharing or DMA systems that buses are available. Appears as BA in the Word Recognizer.
CLK	The ECL level clock signal from the personality module to the logic analyer.
CLK(L)	The inverted ECL level clock signal from the personality module to the logic analyer.
DI0-DI7	The buffered, bidirectional, 8-bit data bus from the personality module to the logic analyer.
DMA/BREQ(L)	The Direct Memory Access (DMA) and Bus Request (BREQ) line from the system under test (SUT) to the personality module; used to suspend program execution and make the buses available for use by a different controller.
DMA+DEAD	The Direct Memory Access (DMA) OR Dead (cycle) line from the personality module to the logic analyer; used to indicate a DMA bus grant or a Dead cycle.
E	The Enable (E) clock from the system under test (SUT) to the personality module; falling edge indicates to memory and peripherals that the data on the bus is stable.
(HALT).(DMA/ BREQ)	The HALT AND DMA Bus Request line is the C7 control line to the logic analyzer. HALT(L) is a combination of PHALT(L) and HALT PUT(L). C7 is asserted low when a Halt request or DMA bus request occurs and causes the HALT/DMA message in the upper right corner of the 7D02 screen.

SIGNAL	DESCRIPTION
HALT PUT(L)	The HALT Processor Under Test (PUT) line from the logic analyer to the personality module; halts the processor approximately 2 cycles after the trigger, if so selected in the trigger menu. PM 111 generates HALT(L) from HALT PUT(L) ORed with PHALT(L).
IFC(L)	The instruction fetch signal line from the personality module to the logic analyzer; used to indicate the occurrence of an Instruction Fetch Cycle (IFC). Appears as FETCH1 in the Word Recognizer.
IFC+IFC2(L)	The instruction fetch signal line from the personality module to the logic analyzer; used to indicate a fetch of the first or subsequent byte(s) of an instruction opcode (IC+IFC2). Appears as FETCH1+2 in the Word Recognizer.
INT	Composite Interrupt (INT) signal from the personality module to the logic analyzer; formed by ORing IRQ(L), FIRQ(L), and latched NMI(L). Appears in the Word Recognizer.
INVOUT	Buffered clock signal from the FET clock oscillator in the hybrid cable assembly (40-pin plug) to the personality module.
IOCO(L)	The Invalid Opcode (IOCO) signal line from the personality module to the logic analyzer; used to indicate an illegal opcode. Appears as INVAL.OP in the Word Recognizer.
LOOK	The input Look signal from the logic analyer to the personality module; controls address and data transmission by disabling AI0-AI15 and DI0-DI7.
PA0-PA15	The address lines from the system under test (SUT) and the zero insertion force (ZIF) socket to the personality module.
PBA	The Processor Bus Available (PBA) signal from the zero insertion force (ZIF) socket and the system under test (SUT) to the personality module. See description of BA.
PBS	The Processor Bus Status (PBS) signal from the zero insertion force (ZIF) socket and the system under test (SUT) to the personality module. When decoded with BA, represents the microprocessor states.

SIGNAL	DESCRIPTION
PD0-PD7	The data lines from the system under test (SUT) to the personality module.
PFIRQ(L)	The Processor Fast Interrupt Request (PFIRQ) signal from the zero insertion force (ZIF) socket and the system under test (SUT) to the personality module. This signal has priority over PIRQ(L) and if not masked, stores only the program counter and the condition code register on the stack.
PHALT(L)	Processor Halt (PHALT) signal from the system under test (SUT) to the personality module; causes the microprocessor to stop running at the end of the present instruction.
PIRQ(L)	Processor Interrupt Request (PIRQ) signal from the zero insertion force (ZIF) socket and the system under test to the personality module; has the lowest interrupt priority of all interrupts. When asserted but not masked, causes the entire machine state to be stored on the stack.
PNMI(L)	Processor Non-Maskable Interrupt (PNMI) signal from the zero insertion force (ZIF) socket and the system under test (SUT) to the personality module; has the highest priority of all interrupts. When asserted, causes the entire machine state to be stored on the stack.
PR/W(L)	Processor Read/Write (PR/W) signal from the zero insertion force (ZIF) socket and the system under test (SUT) to the personality module. See the description of R/W(L).
R/W(L)	The Read/Write (R/W) line from the personality module to the logic analyzer. The signal (buffered from the processor) indicates the direction of data transfer on the data bus. Appears in the Word Recognizer.
SELP(L)	The Select Prom (SELP) signal from the logic analyer to the personality module; selects the contents of the personality module EPROM to be read by the 7D02.
VMA(L)	The Valid Memory Address (VMA) line from the personality module to the logic analyer; when asserted low, indicates a valid memory address cycle. When high, usually signifies internal processor operations.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 11-16-81 Change Reference: C1/1181

Product: PM111 PERSONALITY MODULE Manual Part No.: 070-4155-00

DESCRIPTION

PICN #3

TEXT CHANGES

SECTION 2 OPERATING THE PM 111 PERSONALITY MODULE

page 2-2 under CONNECTING THE PM 111 TO THE 6809E SYSTEM UNDER TEST item 4

ADD:

In addition; a hardware modification must be made. See CHANGING 6809 TO THE 6809E CONFIGURATION in the THEORY OF OPERATION section.

under that

ADD:

5. Plug the PM 111 microprocessor plug into the 40-pin dip socket, carefully aligning pin 1's on both the plug and socket.

page 2-23 under 6809E OPERATING CONSIDERATIONS

ADD:

NOTE

The procedure for changing the 6809 configuration to the 6809E configuration is contained in the THEORY OF OPERATION section. Refer to qualified personnel.

SECTION 4 THEORY OF OPERATION

page 4-4 under 6809E HARDWARE CONSIDERATIONS, under third bullitized paragraph

ADD:

The 6809/6809E select jumper on board A2 must be placed in the 6809E position, as described in the procedure below.

NOTE

To be operated with a 6809 microprocessor again, the 6809/6809E select jumper must be returned to the 6809 position.

CHANGING THE 6809 TO THE 6809E CONFIGURATION

Disassemble the PM 111 according to the procedure "PERSONALITY MODULE DISASSEMBLY" steps 1-6, located in the Maintenance and Troubleshooting Section.

DESCRIPTION

On the middle board, A2, move the black terminal link (jumper) from TP1070 and TP1071 (6809 position), to TP1071 and TP2070 (6809E position).

Reassemble the PM111 microprocessor by reversing the disassembly procedure.

page 4-6 under FIRMWARE EPROM 1st sentence

CHANGE TO:

The Firmware EPROM function block consists of a 4kx8 EPROM (U4035) and an 8-bit tri-state buffer driver (U5035).

page 4-19 under CYCLE DECODER PROM 1st paragraph

CHANGE TO:

The Cycle Decoder PROM is a 4kx8 EPROM containing two sets of seven decorder tables each. One set of tables is required for the 6809, and the other set for the 6809E . The two sets of tables are required because the 6809 and 6809E microprocessors have differing numbers of invalid memory address cycles in their internal operations for two instructions and fifteen indexed postbytes. A jumper has been provided to select the appropriate half of the EPROM, according to which processor is being used.

SECTION 5 PERFORMANCE CHECK

page 5-8 under item 2

ADD:

3. The Self Test Acquisition check may be run with the PM111 in either the 6809 or 6809E configurations of board A2. In the 6809E mode, however, the self test acquisition between ADDR 1014 and ADDR 191F will appear as follows:

DESCRIPTION

```
035 1014 LBSR 191D          0
036 1015  09    READ        0
037 1016  06    READ        0
038 FFFF  00    READ        0
039 FFFF  00    READ        0
040 1919 NEG  @00           0
041 FFFF  00    READ        0
042 191B  19    WRITE       0
043 191C  19    WRITE       0
044 191D  19    READ        0
045 191E  1A    READ        0
046 191F ORCC #03           0
```

SECTION 6 MAINTENANCE AND TROUBLESHOOTING

page 6-14 Table 6-1 partial

CHANGE TO:

TP1071	A2	EPROM A11
TP2070	A2	+5

page 6-23 to NOTE

ADD:

Signatures must be taken with jumper connecting A2TP1070 and A2TP1071 (6908 position).

REPLACEABLE MECHANICAL AND ELECTRICAL PARTS CHANGES

SECTION 7 REPLACEABLE ELECTRICAL PARTS

page 7-5 A2U2060 part number

CHANGE TO:

A2U2060	160-1352-01

SECTION 9 REPLACEABLE MECHANICAL PARTS

page 9-3 Fig and Index NO 41

CHANGE TO:

Qty
4

DESCRIPTION

DIAGRAM CHANGES

SECTION 8 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

DIAGRAM 3

CHANGE AS SHOWN:

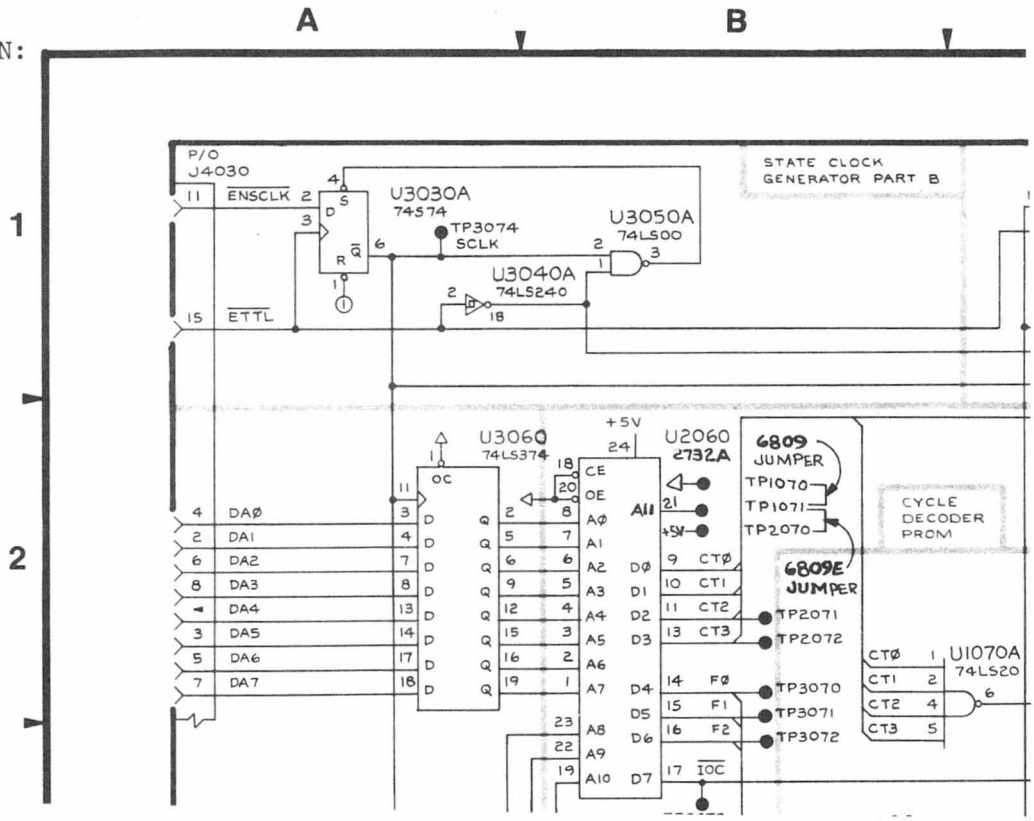

Figure 8-2 A2 Middle board component locations (partial)

CHANGE AS SHOWN: