# 7F10 <br> O/E CONVERTER MODULE 



The following service instructions are for use by qualified personnel only. To avoid personal injury, do not perform any service other than that contained in operating instructions unless you are qualified to do so. Refer to Operator's Safety Summary and Service Summary prior to performing any service.

## Please Check for CHANGE INFORMATION at the Rear of This Manual

## Theory of Operation - 7F10 O/E Module

## Overview

The O/E Optical Module consists of an optical attenuator with fiber input and output, having four attenuator steps of $2.5 \mathrm{~dB}, 5.0 \mathrm{~dB}, 10 \mathrm{~dB}$ and 20 dB for an attenuation range of 0 to 37.5 dB . The output fiber of the optical attenuator is coupled to the Ge-APD on the preamplifier board after running through a certain length of optical fiber, serving as an optical delay line. This delay in the O/E preamplifier is similar to the delay used in the 7A29 vertical amplifier plug in unit. In the 7A29 the delay is achieved by a fixed length of coax cable or via an adjustable mechanical delay line, in the 7F10 by a length of optical fiber. The preamplifier board contains the Ge-APD photo detector, followed by a discrete two stage RF amplifier. The output of this amplifier is further amplifier by a MMIC gain block, which is AC coupled to a SMA connector. This output is connected to the input of the amplifier main board from the 7A29, which is used in the 7F10 O/E converter plug in unit. The preamplifier printed circuit board also rooms a reference voltage circuit, an APD voltage bias regulator circuit, an overload detection circuit and +12 V and -12 V voltage regulators.

## O/E Converter Circuit Detail

The Ge-APD is AC coupled to the first amplifier stage Q1 through C1. AC feedback is provided by R1 and C2. The DC operating point of Q1 is established by feeding back the collector current of Q1 (DC component) through R22, which is determining the collector current of Q4, the current source biasing the RF amplifier stage Q1. This also sets the DC operating point of Q2 and Q3. The gain of this stage is depending on the series impedance of the Ge-APD, which at room temperature is a couple of hundred Ohms. It amplifies the high impedance signal from the Ge-APD detector, providing a low impedance at the collector of Q1. Gain of this stage is in the order of $G_{1} \sim 2-3$. Capacitor C3* (part of the PCB) and R4 are used for RF compensation if needed.
The stage following with Q2 is an emitter follower, buffering the output impedance at the collector of Q1 from the input load of the second gain stage $Q_{3}$. The second gain stage has a gain of approx. $G_{2}=1.0$ when terminated into the 50 Ohms input impedance of MMIC gain block U1. It is made up of Q3, having a 50 Ohm collector resistor R8. R10 sets the DC operating current, R9 sets the AC gain, R11 and C6 provide RF gain peaking. This stage drives the MMIC gain block U1. The gain of U1 is adjusted by R13 to set the overall gain of the O/E preamplifier. R25 is adjusted to meet the MMIC operating current of $\mathrm{I}_{\mathrm{D}}=$ 30 mA for 12 V operation. Both R13 and R25 are trimmed. Gain of this stage is approx. $\mathrm{G}_{3}=4$. The overall voltage gain of the $\mathrm{O} / \mathrm{E}$ preamplifier is approx. $\mathrm{G}_{\mathrm{O} / \mathrm{E}}=8-12$, and is depending largely upon the Ge-APD series impedance.

## Reference Voltage and Regulator

The temperature compensated, high stability reference diode VR30 sets the basic reference voltage to nominally $U_{\text {VR30 }}=6.2 \mathrm{~V}$. This is divided by R31 and R32, buffered by Q30 and adjusted by R38 to a reference voltage input for U 40 of 1.0 V to 2.0 V . The bias voltage needed by the APD is typically 30 V . The temperature coefficient of Q30 of $\Delta \mathrm{U}_{\mathrm{BE}}=-2.2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ translates to a temperature coefficient of the APD bias voltage of $\Delta \mathrm{U}_{\text {APD }}=+0.11 \% /{ }^{\circ} \mathrm{C}$, which compensates for the temperature dependent breakdown voltage and gain of the Ge-APD. High input impedance JFET operational amplifier U40, together with transistor Q40, form a shunt regulator with load resistors R47 and R48. R45 and R46 serve as current limiting resistors for the APD bias output voltage regulator. Feedback to the operational amplifier U40 is via R40 and R41, setting the gain of the voltage regulator to $G_{R E G}=21$. Adjustment range for the APD bias voltage is from approx. 20 V to 40 V via trimming potentiometer R38. Network R44, C14 and capacitor C40 provide stability against oscillation of the bias voltage regulator.

## Overload Detector

Current through R45 will start to bias Q50 at approx. $180 \mu \mathrm{~A}$, in turn triggering comparator U50 when a sufficient collector current is flowing through R50. The comparators output is connected to J604 pin 6, and will turn on the overload LED on the 7F10 front panel directly.

## Voltage Regulators

U60 and U61 are integrated +12 V and -12 V voltage regulators. The +50 V supply is filtered by L3, R45 and C43 for low noise.

## Maintenance - 7F10 O/E Module

## General

The optical electrical module contains static sensitive devices, especially the Ge-APD detector, the microwave transistors and the MMIC. When repairing the module, only do so at an ESD protected environment, using antistatic tools, grounded soldering iron etc. and using personal ESD protection. The components in the O/E converter section use miniaturized SMT components, which are ESD sensitive and mechanically fragile as well.

## Operational Check

In case a malfunction of the O/E module is suspected, check the voltages on the module as given in the schematics section. Start by testing the supply voltages ( $+12 \mathrm{~V},-12 \mathrm{~V},+50 \mathrm{~V},+5 \mathrm{~V}$ ), then check the APD bias voltage to be in the range of 20 to 40 V , typically around 30 V . Set the jumper J 11 to the TEST position, the APD bias voltage should now be essentially zero. Check the reference voltage at VR30 to be approx. 6.2 V , and the voltage at the emitter of Q40 to be approx. 2.0V.

Check the DC voltages on the O/E preamplifier. If these are correct, apply an optical input signal of 1 MHz to the O/E module, using a fast LED transmitter driven by a square wave signal with a mark / space ratio of $1: 1$ ( $50 \%$ modulation). Adjust the amplitude so that you observe a 20 mV Pp square wave signal amplitude at the emitter of Q2, where the output impedance is low. Due to the low signal amplitude, it is suggested to use a FET probe with $x 1$ sensitivity like the P6201 or similar, and a 7A13 comparator plug in amplifier with a sensitivity of $1 \mathrm{mV} /$ div when using a 7000 series oscilloscope mainframe. Alternatively a 7A15(A) amplifier may be used as well.
With this setup you should be able to trace the signal from the amplifier input to the output at the SMA connector. If you check the O/E module outside the 7F10 vertical plug in, terminate the SMA connector with a 50 Ohm termination resistor.

## Repair Work

For general repair work refer to the corresponding section of the 7F10 instruction manual. Observe all precautions, especially when soldering on SMT components. Performing soldering work on the sensitive SMT components used in the $\mathrm{O} / \mathrm{E}$ module preamplifier section requires specialized soldering equipment suitable for this task.

Tektronix Serial / Assembly No.


## Replaceable Electrical Parts <br> 7F10 Instruction - O/E Module

Tektronix
Component No. Part No. Effective Dscont Effective Dscont Name \& Description Mfr. Code Mfr. Part No.

RES., FXD, CHIP: 560 OHM,5\%, 0.125W
RES., FXD, CMPSN:10K OHM , 5\%, 0.125W
RES., FXD, CMPSN 1.0 K OHM , 5\%, 0.125 W
RES., FXD, CHIP: AOT, 0.125W,
RES., FXD,CHIP: 50 OHM , $5 \%$, 0.125 W
RES., FXD,CHIP: 680 OHM , 5\%, 0.125 W
RES., FXD, CHIP: 10 OHM , $5 \%, 0.125 \mathrm{~W}$, CHIP
RES., FXD, CHIP: 50 OHM , $5 \%, 0.125 \mathrm{~W}$, CHIP
RES., FXD, CHIP: 22 OHM , 5\%, 0.125W, CHIP
RES., FXD, CHIP: 560 OHM $, 5 \%, 0.125 \mathrm{~W}, \mathrm{CHIP}$
RES., FXD, CHIP: 10 OHM , 5\%, 0.125W
RES., FXD, CHIP: AOT 218 OHM , 0.125W
RES., FXD, CMPSN: 2.0 K OHM , $5 \%, 0.125 \mathrm{~W}$,
RES., FXD, CMPSN:10K OHM , 5\%, 0.125W
RES., FXD, CMPSN: 390 OHM , $5 \%$, 0.125 W
RES., FXD, CMPSN: 100 OHM , 5\%, 0.125W
RES., FXD, CMPSN: 100 OHM , 5\%, 0.125W
RES., FXD, CHIP: AOT 20 OHM , 0.125W
RES. FXD, FILM: 523 OHM, 1\%, 0, 25W
RES. FXD, FILM: 1.24 K OHM, $1 \%, 0,25 \mathrm{~W}$
RES. FXD, FILM: 953 OHM, 1\%, 0,25W
RES. FXD, FILM: 1.0K OHM, 5\%, 0,25W
RES. FXD, FILM: $49.9 \mathrm{~K} \mathrm{OHM}, 1 \%, 0,25 \mathrm{~W}$ RES. FXD, FILM: 49.9K OHM, 1\%, 0,25W RES, VAR, NONWW: 1.0K OHM, 0.5W

RES. FXD, FILM: 1.00M OHM, 1\%, 0,25W RES. FXD, FILM: 49.9K OHM, 1\%, 0,25W RES. FXD, FILM: 470 OHM, $5 \%, 0,25 \mathrm{~W}$ RES. FXD, FILM: 1.0K OHM, 5\%, 0,25W RES. FXD, FILM: 150 OHM, 5\%, 0,25W

RES. FXD, FILM: $3.40 \mathrm{~K} \mathrm{OHM}, 1 \%, 0,125 \mathrm{~W}$
RES. FXD, FILM: 10 K OHM, $5 \%, 0,25 \mathrm{~W}$
RES. FXD, FILM: 1.0 K OHM, $5 \%, 0,25 \mathrm{~W}$
RES. FXD, FILM: 18K OHM, 5\%, 0,25W
RES. FXD, FILM: 1.0K OHM, 5\%, 0,25W
RES. FXD, FILM: 120K OHM, 5\%, 0,25W
RES. FXD, FILM: 200 OHM, 5\%, 0,25W
RF AMPLIFIER GAIN BLOCK, MICRO-X REPLACE BY MSA-0235 OR MSA-0236 MICROCKT, LINEAR: VOLT REG, + 12V

MC78L12 MICROCKT, LINEAR: VOLT REG, - 12V MICROCKT, LINEAR: OPNL AMPL, JFET, DIP-8 MC79L12 LF351N MICROCKT, LINEAR: COMP, DIP-8 LM311C

SEMICOND DEV, ZENER, SI, 0.4W, 6.2V




