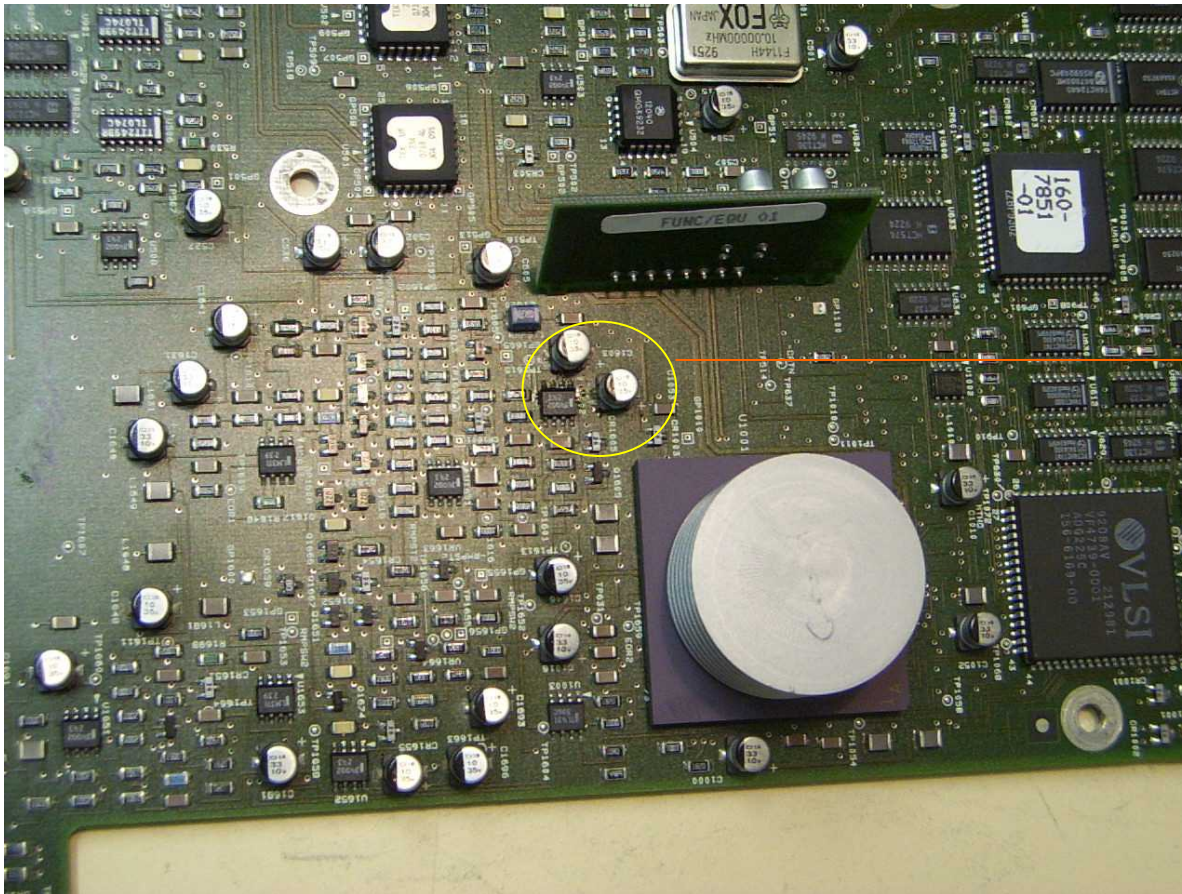# TDS540 ACQUISITION BOARD – REPEAT MODE FAILURE

Leaky caps

This shot shows the area of the Acquisition Board that does the Repeat mode.
This board shows leakage around the Electrolytic Caps (10uF 35V). This leakage caused the board to fail Repeat after running SPC. The display shows lots of noise and data errors at sampling speeds above 1Gs/s.

To fix, clean board, replace ALL caps and any corroded components to restore normal operation.

U1602 – if faulty, will show problems in Equivalent Time (above 1G/S). This can be steps on the waveform or gaps in the display. This part is similar to the TL072 JFET OpAmp.
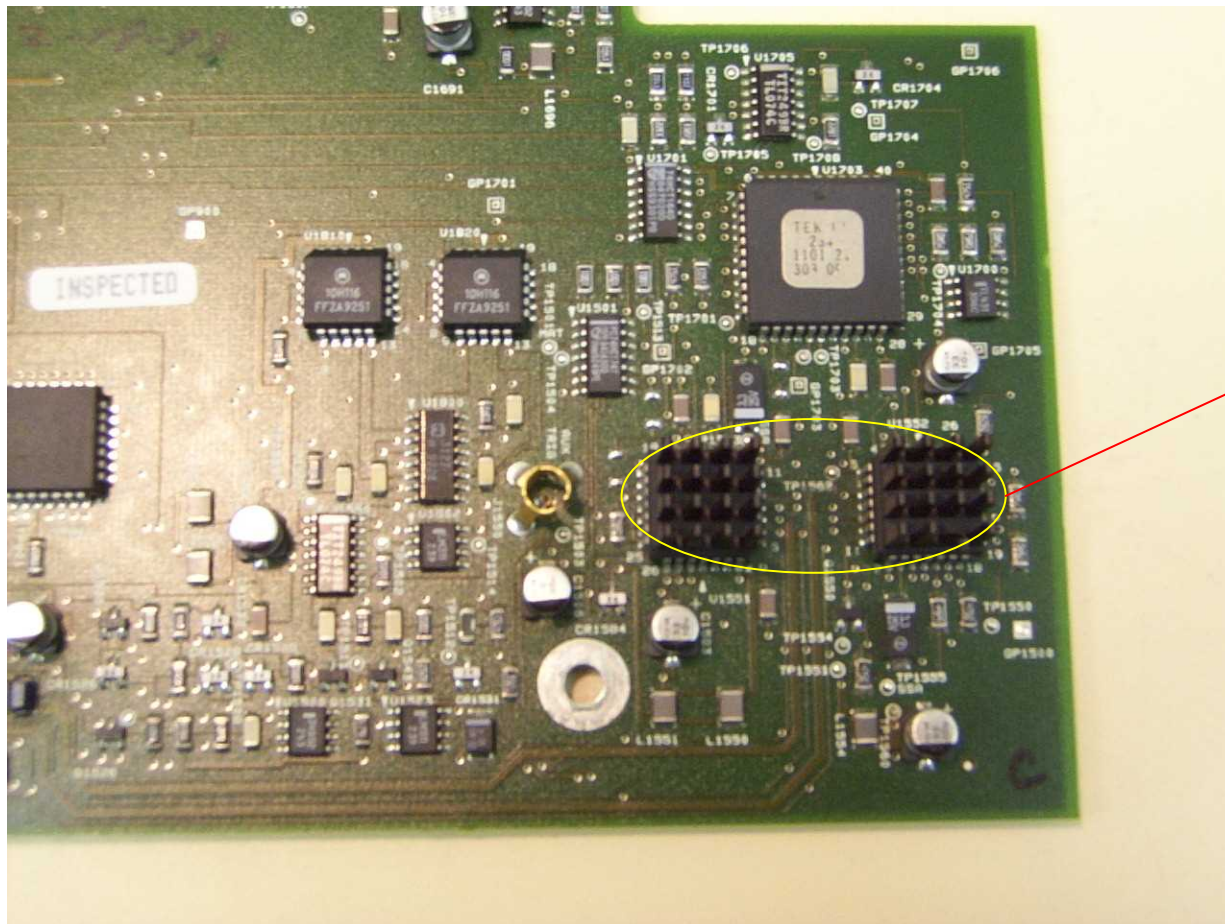
These 2 IC's are the Trigger PreAmps
The one on the outer edge showed no signal output on pin 23 while the other showed several hundred millivolts of signal (50KHz Sine Wave).
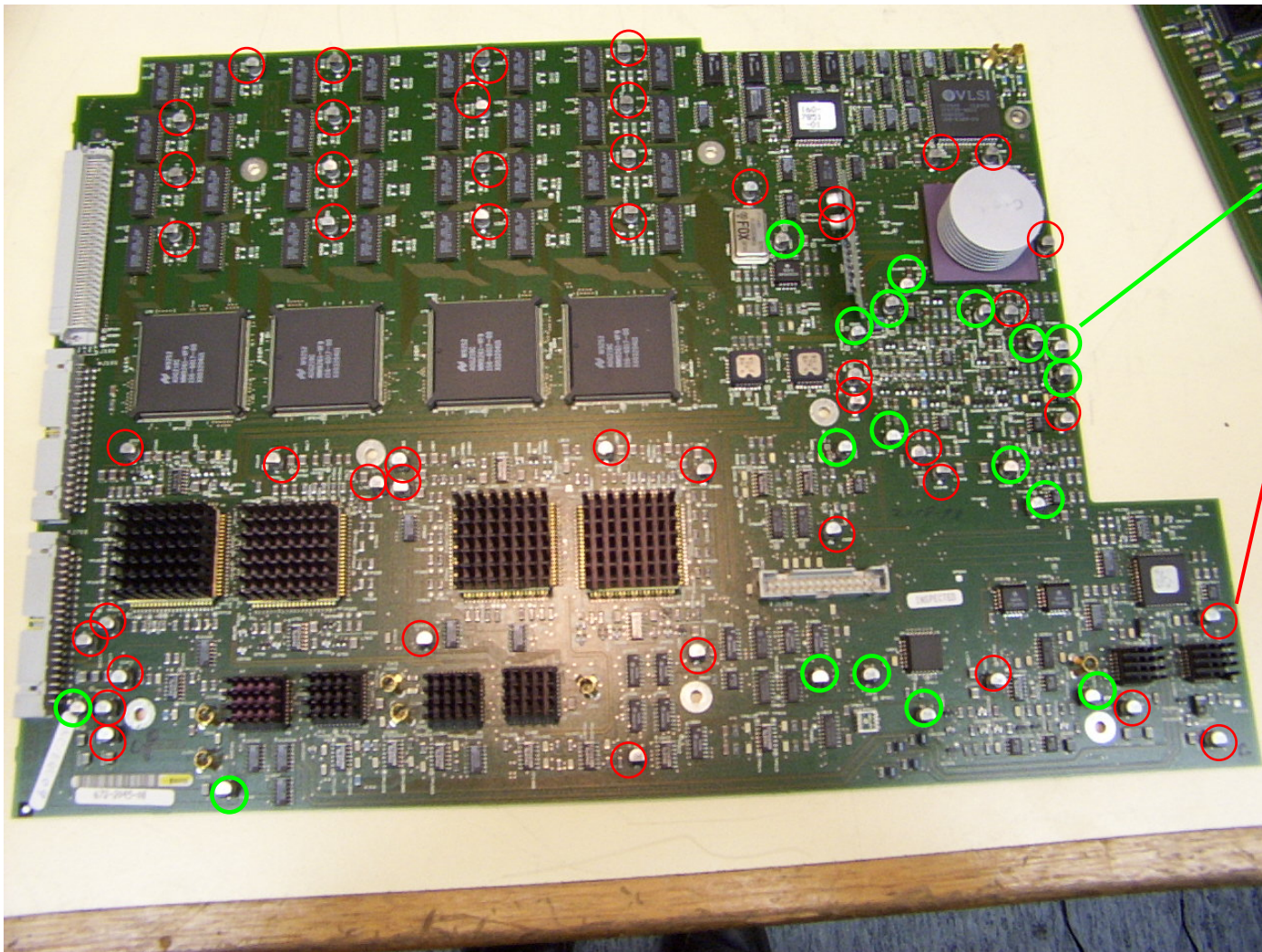This is with the input signal connected to a Vertical Channel and Aux Trig .
Note – chips are oriented 180 degrees from each other.

On screen symptom was no Triggering on any channel but Aux Trigger worked OK
See next page for detailed description of Acquisition system reverse engineered.

TDS540 ACQUISITION BD – TRIGGER SECTION

Location of surface mount
Electrolytic Caps

10uF 35V - 18 caps

33uF 10V – 48 caps

These caps leak and are the
major cause of failures in this
board.
Symptoms include –
Failed SPC
No Repetitive mode
Major DC balance problems.
Traces off screen or high ripple
on traces.
Always check these caps on
every TDS5XX

Acquisition board info

This information was extracted during several repairs to these boards.
Input signal is 500mVPP 50KHz sinewave.

Input section
The input to each channel coming from the Attenuator board goes to pin 24 of the preamp IC's (U1400-Ch1 , U1300-Ch2 , U1200-Ch3 , U1100-Ch4)
I will cover Ch1 as the same applies for each channel (note- IC orientation on board changes).
The signal is then passed to U850 pins 4 & 6 via pins 4 & 6 (180mV) on U1400 .
The signal also show at pin 45 (320mVpp) and pin 2. Pin 2 is the Trigger pickoff signal.

Trigger Section
The Trigger signal goes to U1552 - Pin 9 is Ch1 , Pin 8 is Ch2 , Pin 10 is Ch3 , Pin 7 is Ch4 input.
The inputs are selected by BCD code applied to pins 1,2,3.
The logic is Ch1 – Pin1 **L** , Pin 2 **H** , Pin 3 **H** . Ch2 – Pin 1 **H ,** Pin 2 **L** , Pin 3 **H.** Ch3 - Pin 1 **L ,** Pin 2 **H ,** Pin 3 **L.** Ch4 – Pin 1 **H**, Pin 2 **L** , Pin 3 **L**.
All are high to switch output off when U1551 is selected for Aux Trigger.
The Trigger amp IC (U1552) has it's output (about 3V or more)on pins 20 & 21, this output is only present if the vertical channels are selected and the Trigger Level input on pin 16 is between the range of +/-700mV.
The trigger level is obtained from the DAC system. The output from U1552 goes to U1703 – pins 1 & 2 via a termination network which reduces it's level to about 1.5V. Pins 42 & 43 have about 900mV of trigger signal, Pin 1 has the trigger signal from U1551 (pin 20) at about 350mV (pin 2 and pin 21 are the compliments). U1703 (pin 23) and TP1703 will have 400mV negative going pulses 20us apart with a triggered 50KHz sinewave into Ch1. The compliment is on Pin 22.+
+

DAC System
The DAC system consists of a main DAC (U900) an AD667, a number of switch IC's and the sample & hold Op Amp's.
The DAC output is on pin 9. This goes to large number of various IC switches in the area of the board from U900 to Ch1 input connector and behind the Attenuator connector J1153. The DAC system uses a combination of 4051 CMOS (8 to 1 switches), DG444 (4 x SPST CMOS switches) which demultiplex the DAC output to DC levels for various functions (Trigger level, Vertical gain, offset, DC balance). These outputs are fed to Sample & Hold circuits using TL074 and other Op Amps.
A typical path is the A Trigger Level. This comes from the DAC, is demultiplexed by a 4051 (U931 pin 3 as the input) and outputted via pin 13 to a TL074 (pin 5). This Sample and hold Op Amp outputs the Trigger Level (+/- 700mV DC) to the Trigger Amp (U1552 pin 16) from it's output pin 7.
The DAC system refresh rate seems to be 6.06ms.