Tektronix®

PM 104
PERSONALITY MODULE FOR 8085 MICROPROCESSOR

INSTRUCTION MANUAL

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PM 104
PERSONALITY MODULE FOR 8085 MICROPROCESSOR

INSTRUCTION MANUAL

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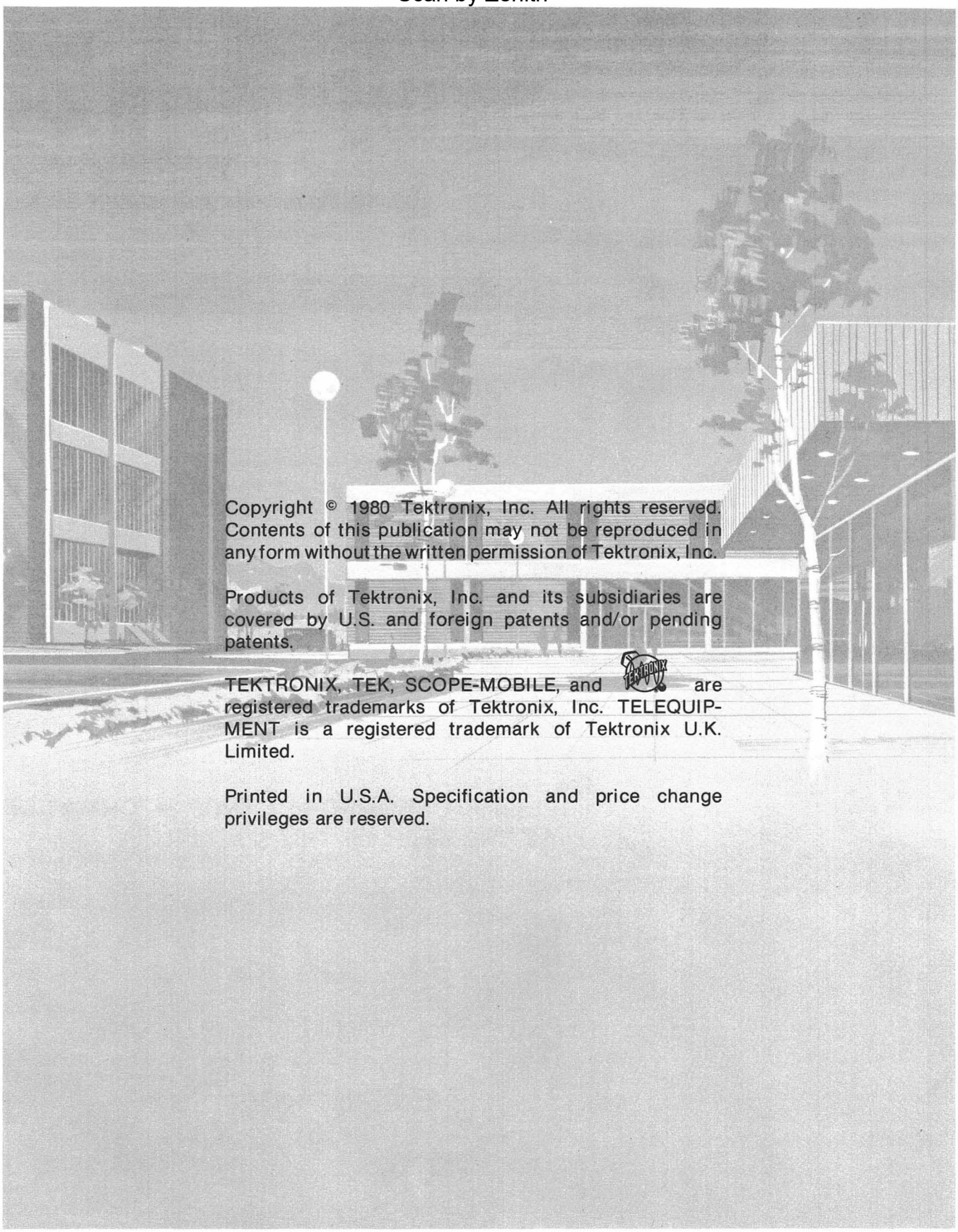

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

Terms In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

Symbols As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see maintenance section.

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

PM 104 Personality Module connected to a 7D02.

GENERAL INFORMATION

Manual Overview

This instruction manual includes complete information for operation and maintenance of the PM 104 Personality Module—a design tool for use by designers of 8085-based microprocessor systems. Section 1 provides a general introduction to the PM 104 and describes its physical construction. Section 2 gives details of connection and operation of the PM 104 with a Tektronix 7D02 Logic Analyzer and an 8085 System Under Test. Section 3 lists electrical, mechanical, and environmental specifications of the PM 104. Section 4 includes details of periodic maintenance and troubleshooting for the Personality Module. Section 5 is a detailed circuit description. Section 6 lists all replaceable electrical parts. Section 7 comprises the Schematics, Section 8 the Mechanical Parts List, and Section 9 a Signal Glossary. For the location of any specific information, refer to the Table of Contents.

Since the PM 104 is a tool for designers of 8085-based systems, it is assumed that you have access to an Intel 8085 Microcomputer System Design Data Manual or other manual relating to this microprocessor.

Reference is made throughout this manual to a Logic Analyzer. The Tektronix Logic Analyzer most often used with the PM 104 Personality Module is the 7D02 Logic Analyzer. For operation of the system as a whole, you will require a Tektronix 7D02 Operators Manual.

Introduction to the PM 104

The PM 104 Personality Module connects a Tektronix Logic Analyzer to an 8085-based System Under Test (S.U.T.). Circuitry in the PM 104 "personalizes" the Logic Analyzer to operate specifically with the 8085 microprocessor.

The PM 104

Physically, the PM 104 consists of a circuitry pod containing electrical components arranged on two printed circuit boards designated the Upper Board (A1) and Lower Board (A2). One end of the circuitry pod connects to a twisted pair woven cable terminating in a microprocessor plug. The other end of the circuitry pod is connected to a ribbon cable which terminates in a Logic Analyzer plug. Figure 1-1 shows the PM 104 connected to a Logic Analyzer and a System Under Test for operation.

The circuitry pod includes:

An interface assembly that "personalizes" the Logic Analyzer to operate with the 8085 microprocessor.

A zero-insertion-force (ZIF) socket on the top side of the pod which contains the 8085 microprocessor from the S.U.T. when the system is connected for Logic Analysis.

Firmware that permits the Logic Analyzer to disassemble the information it receives into the mnemonics of the 8085.

Circuitry to generate the state clock and other inputs to the Logic Analyzer.

System Connection

When the Personality Module is ready for operation, the 8085 microprocessor in the System Under Test is removed from its normal circuit location and plugged into the ZIF socket on the top of the PM 104 circuitry pod. The Microprocessor Plug from the Personality Module is plugged into the microprocessor socket in the S.U.T., and the Logic Analyzer plug is connected to the 7D02. In this configuration, the 8085 drives the System Under Test as before, but through the PM 104. The Logic Analyzer now has access to the address, control, data, and clock lines from the microprocessor, while the Personality Module generates some additional information required by the Logic Analyzer.

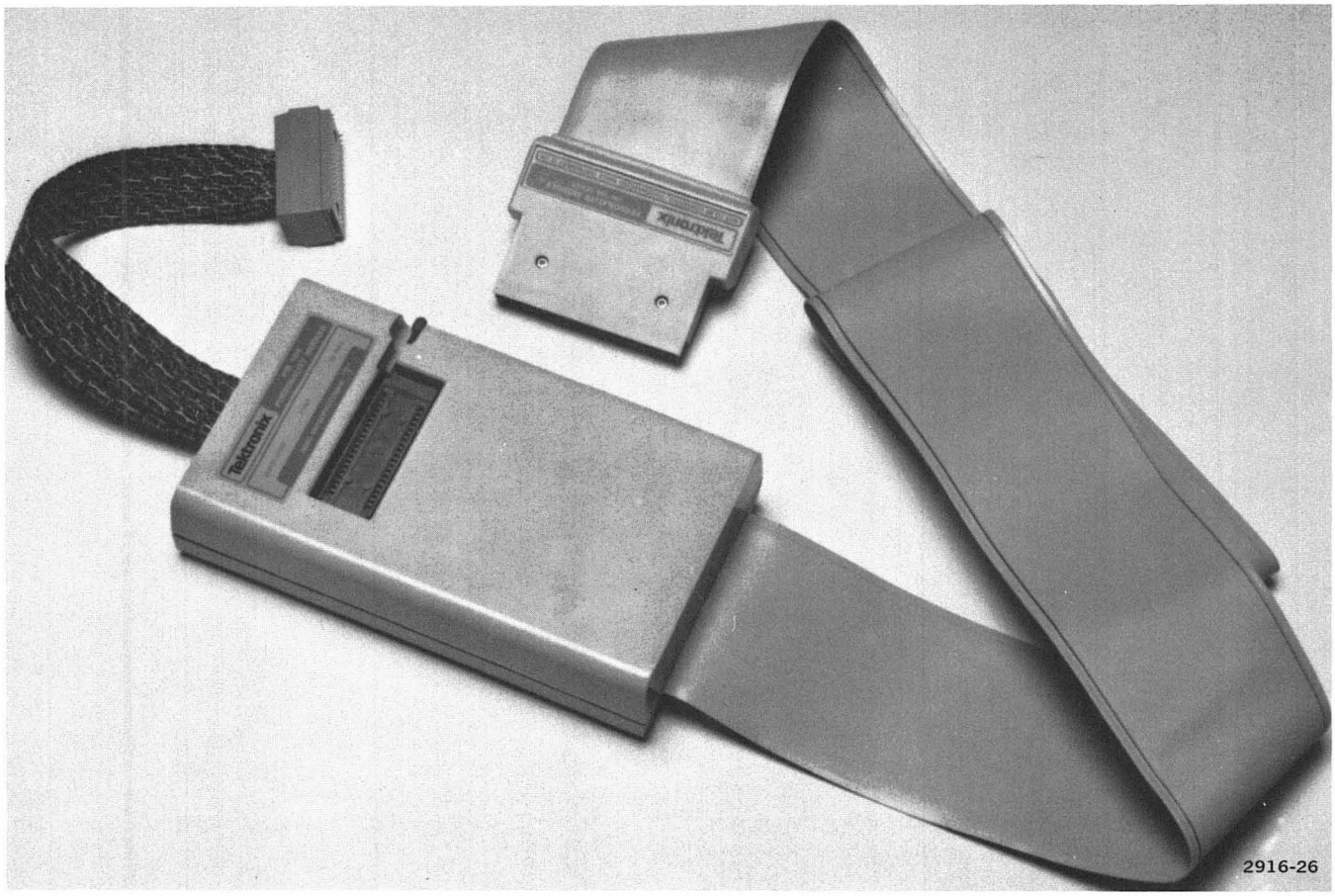

Fig. 1-1. PM 104.

OPERATING THE PM 104

Storing the PM 104

When storing the Personality Module, always protect the Microprocessor Plug with a plastic protector, Tektronix Part No. 200-2445-00. This is necessary to prevent damage to the pins on the plug, and also to protect the Personality Module from static electricity.

Connecting the PM 104 to the Logic Analyzer

CAUTION

Be sure that power is removed from the mainframe before connecting the PM 104 to the 7D02 Logic Analyzer.

With power removed from the mainframe, insert the Logic Analyzer plug from the PM 104 into the socket at the lower edge of the 7D02 front panel. In the proper position for insertion, the label on the PM 104 Logic Analyzer plug is facing up.

Connecting the PM 104 to the System Under Test

CAUTION

Be sure System Under Test power is OFF before attempting to connect the PM 104. Also, before handling the microprocessor in the System Under Test (S.U.T.), ground yourself to drain off static electricity.

Remove the 8085 microprocessor from the S.U.T. and carefully insert it into the Zero Insertion Force (Z.I.F.) socket on the PM 104. Be very careful to insert the 8085 into the ZIF socket with pin 1 next to the lever on the ZIF socket.

To save wear on the microprocessor socket in the System Under Test, it's a good idea to insert an extra socket before actually plugging the PM 104 Microprocessor Plug into the S.U.T. Tektronix Part No. 136-0623-00, available from your Tektronix Field Office, is suitable for the purpose. With the extra socket in place, plug the PM 104 Microprocessor Plug into the microprocessor socket. Again, be sure the pin alignment is correct. Pin 1 of the PM 104 Microprocessor Plug is marked with a notch and an arrow.

Operating the PM 104 with the 7D02

NOTE

Since the PM 104 has no controls that affect the operation of the system, operation of the Personality Module requires that you have a copy of the 7D02 Operators Manual at hand, and are thoroughly familiar with Logic Analyzer operation before attempting to use the PM 104. The manufacturer's documentation of the 8085 being tested is also a necessary tool when logic analysis is being conducted.

Distinctive Characteristics of the PM 104

In setting up data displays on the 7D02, you'll notice that the Word Recognizer Test displays for the PM 104 differ somewhat from those illustrated in the 7D02 Operators Manual. Figures in that manual show an example of Word Recognizer Test #1 using a different Personality Module, with Control Line names somewhat different from those found in the PM 104. With the PM 104, INRQ replaces /NMI in the illustrated display, and IO/M takes the place of /IRQ. INRQ (Interrupt Request), when in a high state, indicates an interrupt request by one or more of the 8085 interrupts. IO/M (Input Output/Memory) designates whether a READ or WRITE operation is to be an IO or a Memory function. If IO/M is in a "1" state, the operation is IO; if "Ø", the READ or WRITE is to Memory. The other PM 104 Control Lines shown in the Word Recognizer test are INACK (Interrupt Acknowledge) and HOLD. In the data display on the Logic Analyzer, the INRQ and IO/M lines are the only ones actually displayed. When INRQ and IO/M are both "1", the indication may be that INACK is in a "1" state. When INRQ and IO/M both show as "1" on the Logic Analyzer Display, one of two conditions may be assumed:

1. There is an interrupt pending during an IO operation.

2. The microprocessor is in an Interrupt Acknowledge Machine Cycle.

This occurs because the microprocessor holds the IO/M line high during an Interrupt Acknowledge operation. You can tell which of the operations has occurred by checking the address for Memory or IO location. If it is a Memory location, the displayed "1"s indicate an Interrupt Acknowledge cycle (INACK). Also, if an Interrupt Acknowledge has occurred, the address following should

show that the microprocessor jumped to an Interrupt routine.

Note in Fig. 2-1 that the program has been set to RISING EDGE OF CLOCK, DELAY CLOCK BY 2, C8=0, and C9=1. C8 corresponds to the ALE (Address Latch Enable) pulse that starts each 8085 Machine Cycle, and C9 corresponds to a Wait State at the microprocessor due to a low signal on the READY line. These two signals are used to synchronize the State Clock Generator with the beginning of each Machine Cycle and to provide a strobe at T3, allowing for Wait States.

Using these standard clock qualifiers, the Logic Analyzer will store once for each Machine Cycle. If you change any of the parameters under USER CLOCK QUAL or USER CLOCK SYNTHESIS, the State Clock is changed accordingly. This feature allows for considerable versatility in observing the operation of the 8085 under test. For instance, if you want to observe what happens on a bus during each "T State", you can change the program to indicate DELAY BY 0. This provides a State Clock for each "T State" and may cause each line of the display to be repeated several times. Other Clock Qualifiers can also be entered to provide a variety of state clock configurations.

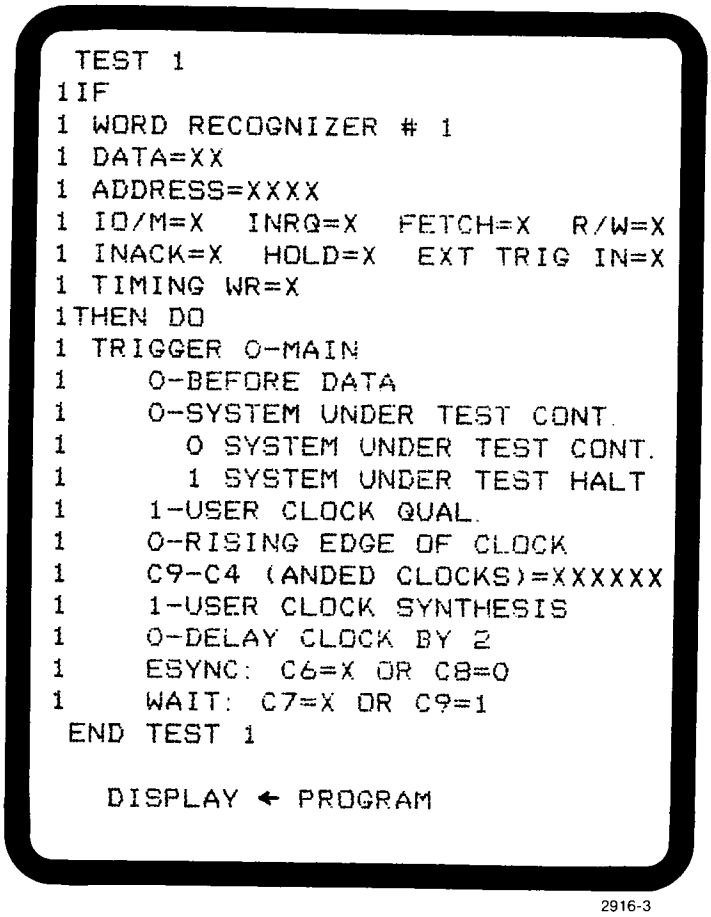

Fig. 2-1. PM 104 characteristics as displayed on the 7D02 screen.

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You need to be aware, however, that information on the busses may be changing during a strobe pulse that occurs at a "T State" other than T3, and it is possible to have random data stored and displayed in such a case. After changing any of the parameters, you can easily return to the standard program setup by re-programming the Word Recognizer test to request STANDARD CLOCK QUAL.

Asterisks in the Display

Asterisks sometimes appear in the data column of a mnemonic display on the 7D02, indicating "No Valid Data Stored" at that location. The PM 104 decodes and displays information by first checking for the mnemonic type, then displaying it. If the mnemonic requires an 8-bit operand, the program advances to the next byte of stored information and tests to determine whether it is a FETCH cycle or a READ/WRITE cycle. If the byte is a READ/WRITE cycle, the data is displayed as the operand of the mnemonic. If it is a FETCH cycle, asterisks are displayed to indicate that no data has been stored for the operand. Asterisks are displayed most frequently in the high byte of the address operand for conditional jumps and calls when the condition is not met.

If the operand includes 2 bytes (an address), the mnemonic is displayed and the program advances two memory locations to get the high byte of the address. Then it decrements one byte to get the low address byte. Each time this operation is repeated, the program checks whether the cycle is a FETCH or a READ/WRITE.

If you choose to change the qualifiers for the State clock, or condense the data stored in memory by using a QUALIFY statement in the Word Recognizer setup, you must be careful to interpret the displayed information correctly. As an example, assume a portion of a program is made up of the following steps:

```
LXI     B,1ØØØH
MVI     M,41H
ADI     A1H
```

The normal 7D02 disassembly would be as follows (LOC, ADDR and INRQ - IO/M were chosen at random):

LOC	ADDR	OPERATION	INRQ—IO/M
015	1234	LXI B,1ØØØH	Ø Ø
016	1235	ØØ READ	Ø Ø
017	1236	IØ READ	Ø Ø
018	1237	MVI M,41H	Ø Ø
019	1238	41 READ	Ø Ø
01A	1239	ADI A1H	Ø Ø
01B	123A	A1 READ	Ø Ø

If you should choose, for example, to qualify on data bytes that end in 1 (i.e., Ø1, 11, 21, etc.), your disassembly would appear as follows:

LOG	ADDR	OPERATION	INRQ—IO/M
015	1234	LXI B, A141H	Ø Ø
016	1238	41 READ	Ø Ø
017	123A	A1 READ	Ø

This is because the Opcode for LXI B, D16 (Ø1H) and the data bytes 41H and A1H all meet the criteria of the qualification. However, the disassembly program cannot take into account the wide variety of qualifiers that are available to you as the operator. Therefore, it assumes that the data following the FETCH is the correct information for the operand. This circumstance can be recognized by checking the displayed addresses.

SPECIFICATION

General

This section of the manual lists the electrical, mechanical, and environmental characteristics of the PM 104 Personality Module. Since the PM 104 operates only as part of a Logic Analyzer system, all operating voltages and currents are furnished by the Logic Analyzer to which the PM 104 is connected.

If verification of these listed electrical characteristics is required for customer incoming inspection or other purposes, the Performance Check protion of Section 4, Maintenance and Troubleshooting, lists all necessary test equipment and describes a procedure for complete verification.

Table 3-1
ELECTRICAL SPECIFICATIONS

Characteristics	Description
Signal Inputs	
Maximum number of channels	34 Data - 8 Address - 16 Control - 10
Control Line Usage	

	Control Line	Stored	Word Recognizer Input	Clock Qualifier
READ /WRITE	- CØ	X	X	
IO /MEM	- C1	X	X	
INRQ	- C2	X	X	
IFC	- C3	X	X	
INACK	- C4		X	X
HOLD	- C5		X	X
RESET OUT	- C6			X
/HALTED	- C7			X
/ALE	- C8			X
WAIT	- C9			X

Microprocessor Capability PM 104	
Signal Inputs	8085A 8085A-2
Clock	
Maximum Frequency in	10 MHz
Processor Halt	STTL level that is approximately 90 ns after the 7D02 stops acquisition. In zero delay mode this is 2 qualified state clocks after the trigger event occurs at the probe tip.

Table 3-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
8085 Probe		
Input Levels		0-7 V signal swings
Input Loading Capacitance		1/2 LSTTL load 40 pf nominal
Voltage in Low Limits	Min. 0.0 V, Max. 0.6 V	
Voltage in High Limits	Min. 2.0 V, Max. 7.0 V	
Current in Low Limits (V. in low - 0.4 V)		−0.2 mA Max
Current in High Limits (V. in high = +2.7 V)		+0.02 mA Max
Threshold Voltage (V_T)		Fixed 1.4 V nominal TTL compatible
Hysteresis	(V_T+ − V_T−)	0.2 V Min.
Maximum Voltage in Non-Operating Non-Destructive		−7 V to +15 V continuous Limited to 5 inputs pulled high simultaneously
Ready Output Drive V_{OH} V_{OL}	 .5 V I_O = −1 mA	 2.4 V I_O = 1 mA
Clock Input Characteristics at Pin 37 of ZIF Socket		
Input Impedance		50 kΩ nominal, 45 pf nom.
Clock Period	20 ns Min.	
Clock Pulse Width (min)		40 ns low, 70 ns high
Voltage in Low Limits (operating)	Min. 0.0 V, Max. 0.6 V	
Voltage in High Limits (operating)	Min. 2.0 V, Max. 7.0 V	
Hysteresis		0.2 V Min.
Threshold Voltage		Fixed 1.4 V nominal
Maximum Voltage in Non-Operating Non-Destructive		−15 V to +15 V
Propagation Delays through Personality Module		
Delay added to READY INPUT	35 ns Max.	From microprocessor plug to ZIF. Measured at 1.4 V with 8085 in ZIF
Address Information A0-A7		Valid at Trailing Edge of ALE

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Table 3-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
C2-INRQ Intr, RST 5.5,RST 6.5		100 ns Max,
RST 7.5, TRAP		95 ns Max.
C3-IFC: IFC		105 ns Max. Following valid signals on S0,S1,IO−/M (S0=S1=1, IO−/M=0)
IFC due to First Machine Cycle of INTR Cycle		130 Max. Following valid signals on S0,S1, IO−/M & INTA S0=S1=IO−/M=1, INTA=0
C4- /INACK		90 ns Max. Following valid signals on S0,S1,IO−/M (S0=S1=IO−/M=1)
C7-HALTED due to: /HALT READY HOLD		 85 ns Max. 90 ns Max. 100 ns Max. A low on /HALT or READY or a high on HOLD will generate a /HALTED on C7
C8-ALE		30 ns Max.
Address Information A0-A7		Valid at Trailing Edge of ALE
C2-INRQ Intr, RST 5.5, RST 6.5	100 ns Max.	
RST 7.5, TRAP		95 ns Max.
C3-IFC: IFC		105 ns Max. Following valid signals on S0,S1,IO−/M (S0=S1=1, IO−/M=0)
IFC due to First Machine Cycle of INTR Cycle		130 Max. Following valid signals on S0,S1, IO−/M & INTA S0=S1=IO−/M=1, INTA=0
C4- /INACK		90 ns Max. Following valid signals on S0,S1,IO−/M (S0=S1=IO−/M=1)
C7-HALTED due to /HALT /READY READY HOLD		 85 ns Max. 90 ns Max. 100 ns Max. A low on /HALT or READY or a high on HOLD will generate a /HALTED on C7
C8-ALE		30 ns Max.
C9-WAIT		75 ns Max. Following low going signal on READY

Table 3-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
Delay, all other Channels		40 ns Max.
Delay through ECL clock		10.5 ns Min. to 14.5 ns Max.
Test Clock		
Clock Period		180 ns Min. 200 ns Max. Measured at TP7010 on lower board
Clock Pulse Width (high and low)		55 ns Min.
Oscillator, Microprocessor Plug		Operates with any recommended oscillator circuit. Refer to MCS-85 User's Manual and /or supplement for further information.
Crystal Mode		Parallel resonant
Frequency of Operation		10 MHz max. 1 MHz min.
LC Mode		
Frequency		6 MHz max. 1 MHz min.
RC Mode		Recommended values R≈10 kΩ C≈20 pf
Frequency		1.5 to 4 MHz Measured at ZIF socket Pin 1
Connections		
External Input Mode		
Probe Input Characteristics at X_1		
Resistance		>400 kΩ at DC
Capacitance		10 pf, typical
Input Signal Requirements		
VIH		+2.5 V min.
VIL		0.6 V max.
Period		100 ns min (8005A-2) 160 ns min (8085/8085A)
t_{high}		ns min.
t_{low}		50 ns min (8085A-2) 70 ns min (8085/8085A)
Clock Input Delay (rising edge to rising edge)		Measured from microprocessor plug Pin 1 (X), to P7020 Pin 1 <40 ns

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Table 3-1 (cont.)

Characteristics	Performance Requirements	Supplemental Information
System Specifications		
With 7D02		
Data		
Set-up Time	50 ns max	Referenced to rising edge of T_3
Hold Time	0 ns max	
Data Acquisition Rate Period	600 ns min.	
Address AØ-A7		Referenced to falling edge of ALE
Set-up Time		5 ns max
Hold Time		35 ns max
Address A8-A15		Referenced to rising edge of T_3
Set-up Time		50 ns max
Hold Time		0 ns max
ALE		ALE high to T_1 rising edge
Set-up Time	40 ns max	
Hold Time	0 ns max	
HOLD		HOLD set-up time to trailing edge of CLK (T_2 or TWAIT)
Set-up Time		120 ns max.
Hold Time		0 ns max.
READY		References to rising edge of T_2
Set-up Time		135 ns
Hold Time		0 ns

Table 3-2

MECHANICAL SPECIFICATION

Characteristics	Performance Requirements	Supplemental Information
Size		12 x 20 x 4.3 cm (4.7 x 8.0 x 1.7 in.)
Weight		1 kg. (2 pounds) with cables, approx.
Cable Length (Logic Analyzer to Pod)		1.22 m (4 ft.), approx.
Cable Length (Replacement Plug to Personality Module Pod)		.33 m (13 in.), approx.

Table 3-3

ENVIRONMENTAL SPECIFICATION

Personality Modules are class 3 instruments, per Tektronix Standard 062-2853-00. Specifications are listed below; exceptions to the standard are noted in the list.

Characteristics	Performance Requirements	Supplemental Information
Temperature		
Operating		−15° C to +55° C
Non-Operating		−62° C to +85° C
Relative Humidity		95 to 97% non-condensing five 24-hour cycles at 30° C to 60° C
Altitude		
Operating		4.5 km (15,000 ft.)
Non-Operating		15 km (50,000 ft.)

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

THEORY OF OPERATION

Block Diagram Description

The personality Module accesses all the address and data lines and most of the status and control lines of the 8085 microprocessor under test. It decodes the information on each of those lines, transmitting it to the Acquisition Memory of the Logic Analyzer for display in hexadecimal, octal, or binary modes. See Fig. 4-1.

NOTE

Throughout this manual, a slash (/) preceding a signal name or a portion of a signal name indicates that the signal is active when in the low state. For example, /HALT indicates that HALT is an active low signal. R/W implies Ø - Write, 1 - Read.

T States

The 8085 microprocessor can be driven by an external clock signal, or will generate its own clock with the addition of a crystal across its X1 and X2 inputs. The 8085 divides the signal at X1 by two and supplies a clock output signal on pin 37 to drive the other system components. Each clock cycle at pin 37 is described as a "T State." The Personality Module operates in synchronism with T States in all its functions, and throughout this description reference is made to each major occurrence as it relates to some part of a T State.

Address and Data Line Operation for a READ Machine Cycle

Sixteen address lines are taken from the 8085 in the ZIF Socket and applied to buffers in the PM 104. Address lines 8 through 15 are buffered by A1U3060, and lines Ø through 7, described as ADØ through AD7 (the 8085 uses a multiplexed bus, and lines Ø through 7 contain both address and data information) are buffered by A1U3050. The lower 8 bits of address (ADØ through AD7) are latched in A1U2050 during the first T State. The 8085 microprocessor generates ALE (Address Latch Enable) at the beginning (T1) of each Machine Cycle. The falling edge of ALE is set to guarantee that the address information is valid, and is used to latch AØ through A7 into A1U2050. Address lines 8 through 15 are sent immediately to the Logic Analyzer in asynchronous fashion, with lines 8 through 11 also used to address PROM A1U2035. All address information is at the 7D02 ready to be strobed in by the end of the first T State. During T2, the information on the lower 8 address lines changes from address to data. 8085 timing ensures that data is valid by the rising edge of T3, and a READ signal is produced to store the information. Thus, the Memory READ has occupied three T States.

ALE and HOLD

The ALE signal is buffered by A1U3020, inverted, and sent directly to the 7D02. /ALE appears at the Logic Analyzer on Control line C8 as ESYNC, which synchronizes the front end board of the 7D02. /ALE is again inverted through A1U2010 and sent to the Personality Module Lower Board (A2), where it is used to synchronize the Wait State Generator and the Instruction Fetch Cycle Generator. The HOLD signal is also inverted in Buffer A1U3020 and sent to the Lower Board to Latch A2U4030. There it is re-inverted and provided as a HOLD REQUEST signal to the Logic Analyzer, where its primary use is as a Word Recognizer.

Interrupts

The 8085 provides five different interrupts: INTR, TRAP, and RST 5.5, RST 6.5, and RST 7.5. The interrupts are buffered by A1U3020, then supplied as inputs to AND Gate A1U3030. The combination of A1U3020 and A1U3030 creates the equivalent of a 5-input NOR gate. Any interrupt that goes high produces a low state at the output of A1U3030. This output is sent to the Interrupt Latch on the Personality Module Lower Board which latches the INRQ line high for at least one instruction fetch cycle.

The ECL Comparator

Pin 37 of the ZIF Socket monitors the clock output of the 8085 on the Ø2 line. This signal is sent to A1U4060, a very fast ECL comparator, which outputs CLK and/CLK signals to the 7D02. The fast comparator is needed to get the Clock signal to the Logic Analyzer as quickly as possible. (The ECL Comparator also provides a constant 50 kΩ input impedance to the clock output, preventing excessive loading from the Personality Module circuitry.) A1Q2071, A1Q1075, and A1Q2070 with their associated circuitry from an ECL to TTL converter, which generates the Ø2TTL input to the Wait State Generator on the Lower Board.

RESET OUT and /INTA

The RESET OUT and /INTA lines are buffered by A1U3010. RESET OUT is then sent directly to the Logic

Analyzer on Control Line C6, and also supplied as inputs to the Interrupt Latch and the IFC Generator on the Lower Board. /INTA also becomes an input to the IFC Generator.

READY

The READY input to the processor is buffered in A1U3010 and combined with the /HALT line in A1U3030. The output is a RDY signal which adds Wait States when necessary between T1 and T3. These Wait States are produced by the Wait State Generator and supplied on Control Line C9. The RDY signal is combined with the HOLD signal in A1U2010-A1U3040 to generate HALTED, which appears on Control Line C7 at the 7D02 as /HALTED.

IO/M, SØ and S1

The IO/M (Input-Output Memory) line is buffered in A1U3010 and appears at the 7D02 on Control Line C1. If IO/M is in a 1 state at C1, an I/O instruction is indicated. If IO/M is in a zero state at this point, a Memory instruction is called for. IO/M is also used as an input to the Instruction Fetch Cycle Generator and Interrupt Acknowledge circuit. SØ and S1 are also buffered by A1U3010, and at its output are combined in AND gate A2U2010-A2U3040 to help produce the INACK (Interrupt Acknowledge) signal at Control Line C4. S1 also appears as RD/WR (Read/Write) on line CØ. Among the three control lines SØ, S1, and IO/M, there can be eight combinations of zero and one states. The combination present at a given instant determines whether there will be an Instruction Fetch, an Interrupt Acknowledge, a Read/Write operation, an I/O Read, etc.

CLOCK OSCILLATOR

The microprocessor replacement plug contains a clock oscillator. This oscillator performs the function of the 8085 internal oscillator and provides low impedance clock signals to the Personality Module and to the 8085.

Self-Test

The Self-Test circuit has been designed into the Personality Module for the purpose of testing the operation of the module itself. This allows any apparent difficulties in the system to be localized to the PM 104 or the 8085 processor under test. It generates a simulated program which exercises most of the functioning circuits of the Personality Module. Self-Test also provides the stimulus for Signature Analysis.

DETAILED CIRCUIT DESCRIPTION

Upper Board

The Upper circuit board (A1) in the PM 104 Personality MOdule contains the buffers for the various processor lines from the ZIF Socket, as well as circuitry that accepts and processes address and data information from the System Under Test so that the disassembled information can be displayed on the 7D02. The ECL Comparator, which processes the incoming clock signal from the processor, is also located on the Upper Board.

Timing and Synchronizing Signals

Ø2 is the Clock signal from the processor on pin 37 of the ZIF Socket. Ø2 is input to pin 2 of ECL Comparator A1U4060, and emerges as two signal outputs; CLK at J1010 pin 2, and /CLK at J1010 pin 3. A1U4060 is a fast ECL Comparator, ensuring that Clock signals are transferred to the 7D02 in the shortest possible time. The CLK output from pin 7 and /CLK on pin 8 are also applied to the ECL-to-TTL converter circuit, A1Q1075, A1Q2070, and A1Q2071, where the Ø2TTL signal is generated for use on the Lower Board.

The other major timing signal from the 8085 processor is ALE (Address Latch Enable). ALE is on pin 30 of the ZIF Socket and is buffered in A1U3020, which also inverts it to /ALE and presents it to the Logic Analyzer as ESYNC on Control Line C8. /ALE acts to synchronize the Front-end board of the 7D02. The /ALE signal from the output of A1U3020 is also re-inverted to ALE in A1U2010 and used to latch AØ through A7 at Latch A1U2050. It is also sent to the Lower Board for use in synchronizing the State Machines via pin 4 of J3005.

Address and Data Lines

During T1 of the 8085 operating cycle, address information enters the Personality Module on ADØ through AD7 (pins 12 through 19 of the ZIF Socket) and on address lines A8 through A15 (pins 21 through 28 of the ZIF Socket.) Address lines AØ through A5 enter buffer A1U3060 through protection hybrids, each of which contains a spark gap with breakdown voltage of about 500 V, and a clamp diode to +15 V protected by an ≈600 Ω current-limiting resistor. From the output of A1U3060, address information on these lines goes directly to J1010 and to the 7D02. A8 through A11 are also used in addressing PROM A1U2035. The lower 8 address bits on lines ADØ through AD7 pass through similar protection hybrids into buffer A1U3050. The 8085 bus, including lines ADØ through AD7, is multiplexed; each of these lines contain address and data at different points in the operating cycle. After the rising edge of T1, ALE goes low, latching address information AØ through A7 into Latch

A1U2050. The output of A1U2050 during T1 is the lower 8 address bits, sent on the Logic Analyzer. During succeeding T States, the information on lines ADØ through AD7 is the Op Code or data that the processor instruction operates on.

After the Acquisition Memory has been filled, the 7D02 pulls the LOOK input (J1010 pin 62) high. This causes A1U3060, A1U3050, and A1U2050 to go to a high-impedance state. The Logic Analyzer can then use the address and data lines on J1010 to access the Personality Module ROM to decode the information stored in memory. After a short delay, the /SEL P signal from the Logic Analyzer turns on the PROM and line driver A1U2020 to gather the decoding information required.

Lower Board

Circuitry on the Lower Board includes the three State Machines—the Wait State Generator, the Interrupt Latch, and the Instruction Fetch Cycle Generator. The Self-Test Circuitry is also located on the Lower Board.

Wait State Generator. The Wait State Generator, comprising A2U1020 and A2U2030, monitors the READY and /HALT inputs, and sends a WAIT signal to the 7D02 when either of the two monitored lines is pulled low. The 8085 processor looks at the READY line at the rising edge of T2. If the READY line is low and meets the required setup times, the processor inserts a Wait State in the machine cycle. One Wait State is added for each rising clock edge that occurs while the READY line is held low. The Wait State Generator checks the READY status between the rising edge of T1 and a time approximately 50 to 100 ns prior to the rising edge of T2. If the READY or /HALT line is low, a WAIT signal is sent to the 7D02 in time to cause the Logic Analyzer to simulate the 8085 and insert Wait States.

The READY and /HALT signals are buffered by A1U3010 on the Upper Board. READY enters the Personality Module through J6020 and passes through a protection hybrid into the A1U3010 buffer. READY and /HALT are buffered in A1U3010 pins 4 and 6 respectively, and are ANDed together at A1U3030 and A1U3040. If either input goes low, A1U3030 pin 12 goes low, and A1U3040 pin 8 goes high. The low at A1U3030 pin 12 pulls the READY input of the 8085 low to add Wait States. The RDY signal at A1U3040 pin 8 is sent to the Wait State Generator. ALE is also buffered and sent to the Wait State Generator via A1U3020 and A1U2010. ALE is high during T1 of all machine cycles except for the DAD instruction and during Bus Idle conditions. State Machine operation is as follows:

1. Assume that the READY and /HALT lines are high (no Wait States added).

Starting condition: A2U1020 pin 5 is low
A2U1020 pin 9 is low.

a) The rising edge of ALE clocks A2U1020-5 high.

b) The rising edge of T1 clocks A2U1020-9 high.

A2U2030D is enabled to check RDY
A2U1020-1 is pulled low and cleared
A2U1020-12 goes low.

c) The rising edge of T2 clocks A2U1020-9 low.

A2U2030D is disabled until the next cycle.

d) The cycle repeats and the WAIT signal stays low.

2. Assume that RDY goes high, and Wait States are added.

a) The rising edge of ALE clocks A2U1020-9 high.
b) The rising edge of T1 clocks A2U1020-9 high.

A2U2030D is enabled to check RDY
A2U1020-1 is pulled low and cleared
A2U1020-12 goes low.

c) A2U2030D pin 11 goes low.

A2U1020-10 is low and pin 9 is held high, regardless of the clock at pin 11.

d) RDY goes low.

A2U2030D-11 goes high.

e) The rising edge of Ø2TTL (T3) clocks A2U1020-9 low.

A2U2030D is disabled until the next cycle.

f) The cycle repeats.

Interrupt Latch. The Interrupt Latch, including A2U2020, A2U3030, and A2U1030, latches any interrupt and holds it to guarantee that the Logic Analyzer will see the interrupt request (INRQ) for at least one Instruction Fetch Cycle (IFC). All five 8085 interrupts—INTR, TRAP, RST 5.5, RST 6.5, and RST 7.5 are buffered by A1U3020 and combined into one signal by A1U3030 on the Upper Board. Any time any of the interrupts are pulled high, the /INT REQ signal to the latch circuit goes low. A2U4030B monitors the Wait State Generator and provides a clock pulse to the Interrupt Latch Circuit for T3 of every machine cycle. (This takes Wait States into account, since any Wait States inserted occur prior to T3). The Latch circuit sends a high signal to the 7D02 on the INRQ line as soon as any INT REQ occurs. This signal stays high until (a) INT REQ goes low, and (b) INRQ has been high for an Instruction Fetch Cycle. State Machine operation is as follows:

System Reset: A2U2020-9 is high
A2U2020-5 and −2 are low
A2U3030 is disabled by a low on pin 10.

1. Assume no interrupts (/INT REQ is high).
   Nothing changes when T3 occurs
   Cycle repeats.

2. Assume Interrupt Request occurs, but not during IFC.

   a) /INT REQ goes low.

      A2U2020-9 goes low
      A high signal is sent to the 7D02 on INRQ
      A2U3030-11 is low (disabled).

   b) The rising edge of T3 occurs.

      Nothing changes.

3. Assume an IFC occurs next, but the request is still valid.

   A2U3030 remains disabled due to the low on pin 11.
   The rising edge of T3 causes no changes.

4. Assume that /INT REQ goes high.

   A2U3030 is enabled to look for the next IFC.

   a) The IFC occurs.

      A2U2020-2 goes high.

   b) The rising edge of T3 occurs.

      A2U2020-5 goes high and clocks A2U2020-9 to a high state
      INRQ goes low
      A2U3030 is disabled by a low on pin 10.

   c) The cycle repeats.

Instruction Fetch Cycle Generator. The Instruction Fetch Cycle Generator, which includes A2U3020, A2U3030, A2U2030, and A2U1030, provides an IFC signal to the 7D02 during all Instruction Fetch Cycles. It also generates IFC during the first machine cycle of an Interrupt Acknowledge (INA) machine cycle, due to a high on the INTR interrupt line.

The control lines SØ, S1, and IO/M can be used to determine most machine cycles of the 8085 processor. For an IFC, SØ and S1 are both 1 and IO/M is Ø. For an Interrupt Acknowledge cycle (INA) all three lines are 1. For most INA cycles, the 8085 is internally set to the RST Vector associated with a particular interrupt. However, the INTR interrupt requires that an external source provide the RST information. Therefore, although the SØ, S1, and IO/M lines signify an INA cycle, the 8085 is actually performing an Instruction Fetch Cycle. This special IFC is signaled by a low on the /INTA line. Since the 8085 is doing an IFC, the information on the data bus may be any valid Op Code. It might be a multiple-byte instruction. If we assume a 3-byte CALL instruction, the 8085 uses three INA cycles during which the /INTA line is pulled low and the SØ, S1, and IO/M lines are high. The /INTA signal has the same timing as the /RD signal in a normal IFC.

The Instruction Fetch Cycle Generator sends an IFC signal to the 7D02 for the first machine cycle of each INA cycle caused by an INTR. The remaining machine cycles of a multiple-byte instruction are READ cycles. State Machine operation is as follows:

System Reset: A2U3020-8 is high
A2U3020-6 and −12 are high
/INTA is high
A2U3020-2 is low
A2U3030-2 is low (disabled).

1. Assume no INA cycles due to INTR.

   a) A2U2030-10 is high (enabled).
   b) If SØ and S1 = 1 and IO/M = Ø, IFC is high to the 7D02.
   c) If SØ, S1, and IO/M = 1, IFC is low and INACK is high.

2. Assume INA due to INTR occurs (3-byte CALL instruction).

   a) SØ, S1, and IO/M = 1.

      A2U2030-9 is high (IFC disabled).

   b) /INTA goes low.

      A2U3020-8 is clocked low
      A2U2030-10 is low (IFC and INACK are both high for this cycle)
      A2U3020-2 is high.

   c) The rising edge of T3 occurs.

      A2U3030-2 goes high (enabled.)

   d) The next ALE occurs.

      A2U3020-13 is pulled low
      A2U3020-8 goes high (enables A2U2030-10).

   e) /INTO goes low.

      Clocks A2U3020-11, but since the D is low, the /Q output stays high IO/M is also high, so A2U2030-1 is low, and IFC goes low
      INACK is high.

   f) Third ALE occurs.

      Steps 4 and 5 above repeat.

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g) The 8085 enters a WRITE cycle due to the CALL instruction.

/INTA stays high
IFC and INACK are low, due to the status of SØ, S1, and IO/M.

h) ALE occurs—nothing changes.

i) The rising edge of T3 occurs.

A2U3020-6 goes high.

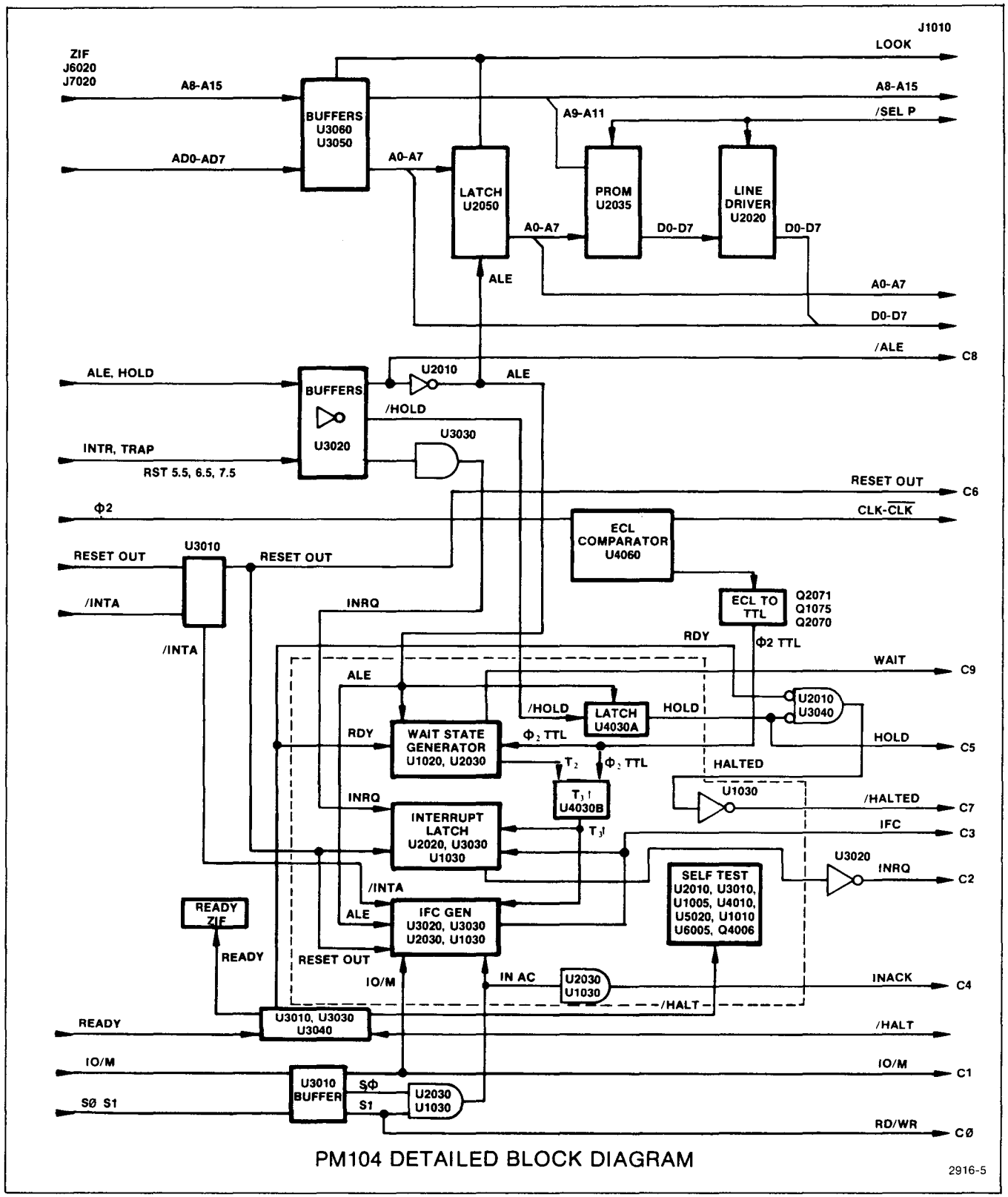
j) The IFC generator is reset and ready for the next INA.

Self-Test

The Self-Test Circuitry in the PM 104 comprises A2U2010, A2U3010, A2U1005, A2U4010, A2U5020, A2U1010, A2U6005, and A2Q4006. When a Self-Test is carried out, the 8085 microprocessor is removed from the ZIF Socket and the Microprocessor Plug is connected to the Self-Test socket on the bottom of the PM 104 Pod. The Self-Test exercises all of the lines from the ZIF Socket and provides the opportunity to observe the operation of each line on the 7D02 display.

A2Q4006 and associated circuitry functions as a 10-MHz oscillator to provide Self-Test timing. A2U2010 accepts the clock signal and generates TCLK and /TCLK signals.

A2U5020 is a buffer which takes its inputs from counter A2U3010 and A2U1005. A2U4010 is a 32-byte PROM which generates a number of different Self-Test functions. The Self-Test operation produces a display at the 7D02 which simulates an actual program, revealing the state of each line in the PM 104 at any given stage of the operation.



PM104 DETAILED BLOCK DIAGRAM

2916-5

Fig. 4-1. Circuit Block Diagram.

PERFORMANCE VERIFICATION

Introduction

The procedures which follow provide a method of checking the operation and performance requirements of the PM 104. The procedure can be used for incoming inspection, familiarization, or system troubleshooting.

There are two parts to the Performance Verification. Part I described a procedure which allows you to verify that the Personality Module circuitry and the connections to the Logic Analyzer are functional and operating as expected. The Personality Module Self Test Stimulus will produce the necessary signals on all address, data, control, and clock lines to provide a preliminary check of the PM 104 circuits.

Part II describes a procedure to test the more specific performance requirements such as input impedance, actual threshold voltages, propagation delays within the module, etc. This procedure requires some physical disassembly of the Personality Module.

PERFORMANCE VERIFICATION, PART I

Test Equipment Required

Test Oscilloscope:

Vertical frequency response DC to 100 MHz
Minimum vertical deflection factor 50 mV to 5 V/Div
Dual Trace
Example, Tektronix Type 465

Pulse Generator:

Tektronix PG 508 or equivalent, with variable pulse width and amplitude

Digital Multimeter:

Tektronix DM 501A or equivalent

40-pin Socket:

40-pin dual in-line package socket, low profile Tektronix Part No. 136-0623-00 or equivalent

Other Equipment:

Small flat blade screwdriver
Phillips screwdriver
3/32" Allen wrench

Preliminary Setup

With the 7D02 Logic Analyzer properly installed in a 7000-Series mainframe and the Power Switch in the OFF position, plug the PM 104 into the 7D02.

Turn the PM 104 upside down. With the flat blade screwdriver, pry open the Test Socket access door by inserting the screwdriver in the small opening at the end of the access door and slowly applying pressure outward.

With the access door removed, plug the Microprocessor Plug into the Test Socket located inside the access opening. Be very sure pin 1 of the plug mates with pin 1 of the Test Socket. **Avoid twisting the cable.**

After checking that all connectors are secure, turn on the 7D02 Power Switch and observe the display. If everything is functioning properly, the "POWER-UP VERIFICATION" will indicate "PASS" for all diagnostic tests, and the display will change to indicate "POWER-UP DIAGNOSTICS COMPLETE."

Set the Channel 1 vertical input of the test oscilloscope to 1 Volt/Div and the horizontal sweep rate to 0.1 μs/Div. Select Channel 1 for Vertical Mode. Then carry out the following steps:

1. Attach the oscilloscope probe ground lead to pin 20 of the ZIF socket (Zero Insertion Force Socket) on the Personality Module. Place the probe tip at pin 1 of the ZIF socket to see a pulse train with a period of 250 to 650 ns and minimum low time >60 ns. This signal is generated by an oscillator in the Microprocessor Plug, and its period is determined by an RC network at the Test Socket. The oscillator can be driven by any of the 8085/8085A or 8085A-2 clock driving circuits specified by Intel. (See Microprocessor Oscillator specifications for more details.(This check simply verifies that the components in the oscillator are functioning.

2. Turn the 7D02 Power Switch OFF and turn the PM 104 upside down again. Move the jumper strap on J6010 (located near pin 1 of the Self Test Socket) from the NORM position to the TEST position. This enables the PM 104 Self Test circuitry for the remainder of the Performance Verification tests.

NOTE

Be sure that the J6010 jumper strap is always restored to the NORM position at the conclusion of testing. This is necessary to conserve power and prolong the life of the components.

3. While holding down any one of the 7D02 input keys, turn the Power Switch ON and wait for the display to appear. The "POWER-UP VERIFICATION" should indicate that the "KEYBOARD" test has failed due to the key being held down. This allows access to the more detailed diagnostics in the 7D02 firmware.

4. Press the X (Don't Care) key on the 7D02 Numeric Entry keypad to enter the Diagnostic Monitor. A diagnostic menu will appear on the display.

5. Press 9 on the Numeric Entry keypad to enter the Personality Module diagnostics. The display will ask for "SELF TEST STIMULUS" which has been connected in earlier steps.

6. Press the START key to begin Self Test diagnostics. These tests check most of the PM 104 circuitry, as well as the connections to the 7D02 for all address, data, and clock lines, and most of the control lines. If everything is functioning properly, the display will indicate that all tests "PASS."

Timing Option Checks

The Personality Module Self Test circuit generates signals to check the Timing Option of the 7D02. If a Timing Option is installed, test these signals by making the following connections:

Connect a P6451 Data Acquisition Probe to the 7D02 Timing Input connector.

Attach the P6451 input leads to J6030 at the lower end of the Self Test Socket as follows:

- GND to J6030 Pin 1 (marked by an arrow on the circuit board)

- Channels 0 to 7 to J6030 pins 2 to 9 respectively. (J6030 pin 10 is used for signature analysis only.)

1. Press X (Don't care) to return to the Diagnostic menu.

2. Press B on the Numeric Entry keypad to enter Timing Option diagnostics.

3. Press START to begin diagnostic tests.

4. The display should show "PASS" for all three tests, indicating that the PM 104 is providing correct information to the 7D02.

5. The remaining checks will be accomplished by putting the 7D02 in its normal operating mode and setting up various conditions via the keyboard. To exit the Diagnostic Monitor, press the X key twice. The display will then read "POWER-UP DIAGNOSTICS COMPLETED."

Wait State Circuitry Check

The PM 104 Self Test generates one Wait State for each simulated machine cycle. The Wait State Circuitry can be checked as follows:

1. Press the WD RECOGNIZER key on the 7D02.

2. Using the CURSOR control keys, move the cursor to the "FETCH-X" box and enter a "1".

3. The cursor will move to the "R/W=X" box. Enter a "0". This sets the Word Recognizer to trigger on an Instruction Fetch Cycle (which is also a Write Cycle). Since this condition never occurs in actual operation, the 7D02 will not trigger.

4. Press TRIGGER.

5. Press START. The 7D02 starts searching for the trigger condition. In the upper right corner of the display, the message "8085 STOPPED" will flash on and off, indicating that the Wait State signals from the PM 104 are sent to the 7D02 correctly. Any of three conditions will produce the "8085 STOPPED" message:

a) The microprocessor READY line is being pulled low by the System Under Test.

b) The 7D02 is programmed to HALT the processor under test.

Test Circuit Data

1. Press the STOP key again to manually trigger the 7D02 and acquire the test circuit data. The information

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displayed is produced by the Self Test circuitry. It does not represent a functioning program, but stimulates various Fetch, Read, and Write machine cycles, by providing the necessary signals on the bus and control lines. This simulated program starts at address ØØØØ and repeats every 64 memory locations. During each program cycle, all of the address, data, and control lines are pulled high and then low at least once to test for stuck lines. If any line contains wrong information, a failure will have occurred during the previously-described diagnostic tests.

2. Press the following keys to continue:

IMMEDIATE
DISPLAY
PROGRAM

3. The display will return to the Word Recognizer program. Using the Cursor control keys and the Numeric Entry keys, input the following information:

FETCH=X
R/W=X

4. Move the cursor to "0-SYSTEM UNDER TEST CONT." and enter a "1". The display will change to "1-SYSTEM UNDER TEST HALT".

5. Press the START key several times while watching for the "8085 STOPPED" message, which will appear after the 7D02 has triggered and should remain on until the new display is generated. Since the Word Recognizer is set to trigger on all "don't cares", the display will show new information each time the START key is pressed.

This concludes Part I of the Performance Verification. Turn the 7D02 Power Switch to the OFF position. Remove the P6451 and the Microprocessor Plug from the Self Test circuitry and move the jumper on J6010 to the "NORM" position. Replace the access door by inserting the end opposite the screwdriver slot first, and applying pressure with the fingers to snap the door into place.

PERFORMANCE VERIFICATION, PART II

Introduction

The performance checks described in this part of the Performance Verification test PM104 specifications that are not checked by the Self Test function. Equipment used in this part of the procedure is the same as that listed at the beginning of the section. These tests will be easier to complete if a 40-pin DIP (Dual In-line Package) socket is plugged on the PM 104 Microprocessor Plug. The PG 508 Pulse Generator can then be connected via short (1-inch) leads from a female BNC connector to the designated pins on the DIP socket.

1. Check Maximum Voltage In Low Limits, Minimum Voltage In High Limits, data Setup Time and Hold Time for address and data lines.

a) Set the Test Oscilloscope as follows:

Vertical Mode	Channel 1
Vertical Deflection Factor	1 V/Div
Time/Div or Delay Time	0.5 μs/Div
Ground	Channel 1 input

Center the trace with the Vertical Position control, and set for DC input. Connect the Channel 1 oscilloscope probe to the BNC plug from the PG 508.

b) Power up the test oscilloscope and the PG 508 and set PG 508 controls as follows:

Period	1 μs
Duration	50 ns
Back Terminated	
High Level	2.0 V
Low Level	0.6 V
Rise/Fall Time	5 ns
Normal/Complement Switch	Complement

c) Observe a negative-going pulse 2 cm high, with a width of 1 cm, on the Test Oscilloscope CRT.

d) Connect the P6508 signal lead to pins 12 (ADØ) and 37 of the Microprocessor Plug. Connect GND to pin 20. Check for a pulse width of 50 ns. Turn on the 7D02 Power switch.

NOTE

Most of the Performance Tests in this section involving the PG 508 require that connection is made to pin 37 (the clock signal), and some other pin on which the test signal is read.

e) To check the Setup and Hold times on the data and address lines, leave the PG 508 connections as described above. Press the Format key on the 7D02. Select binary address and data radices, as shown in Fig. 5-1. Press Format again. Make the following 7D02 key entries in sequence:

ELSE
TRIGGER
USER CLOCK QUAL
USER CLOCK SYNTHESIS
DELAY BY Ø (See Fig. 5-2)
START
SELECT ABSOLUTE DISPLAY MODE

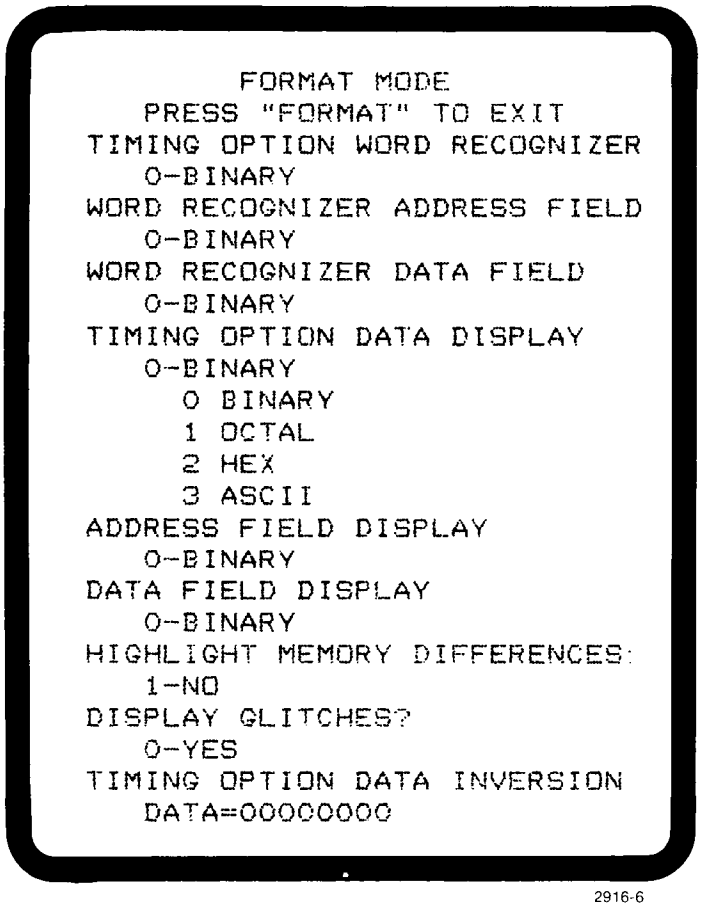
f) Observe on the 7D02 the display that appears in Fig. 5-3. Note that the least significant bit of both the Address and Data displays (indicating the state of multiplexed line ADØ) is Ø. (All other displayed bits show as 1's in the figure, but since all other bits are floating in this display, they can be either 1 or Ø without affecting anything. We are only concerned with the state of Address Ø and Data Ø.)

g) Change the 7D02 program to observe the display triggered on the falling edge of the clock. To do this, press the following 7D02 keys in sequence:

IMMEDIATE
DISPLAY
PROGRAM

Move cursor to RISING EDGE OF CLOCK.
Change program to FALLING EDGE OF CLOCK.
Set the PG 508 output to Normal. Check that the pulse width is still 50 ns at the threshold level.
Press START. Note that now Address Ø and Data Ø are both displayed as 1's.

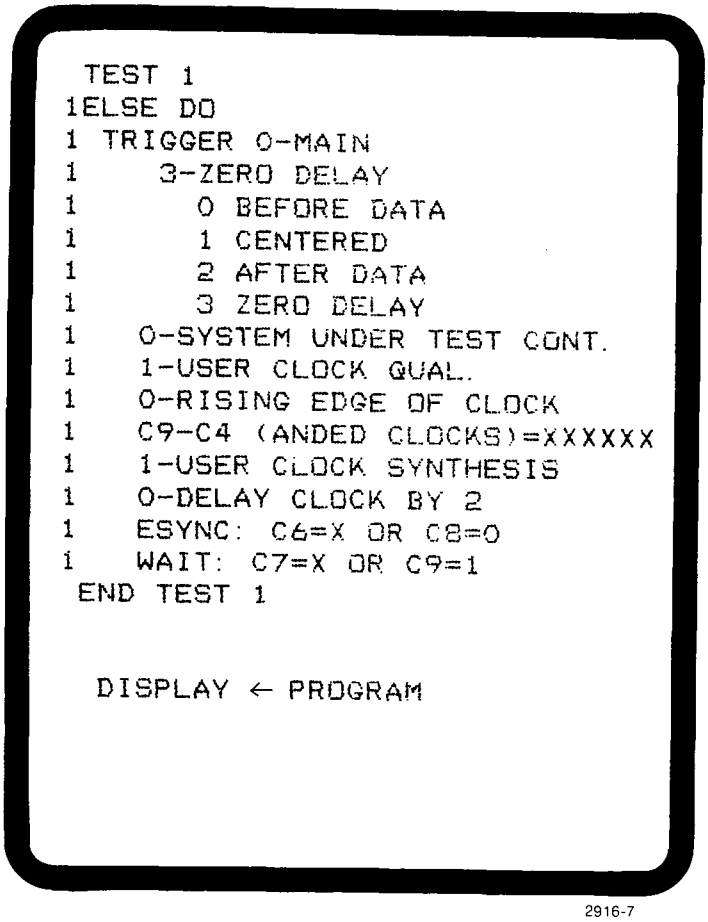
h) Leaving the PG 508 connections on pins 20 and 37, carry out steps e), f), and g) for lines AD1 through AD7 (DIP socket pins 13 through 19) and for Address lines A8 through A15 on DIP socket pins 21 through 28. On lines AD1 through AD7, both the address and data bits in the display will be affected. On Address lines A8 through A15, you'll only be concerned with the Address bit.



2916-6

Fig. 5-1. 7D02 program FORMAT display for checking Setup and Hold times.

@



2916-7

Fig. 5-2. 7D02 delay by 0 triggering arrangement for Setup and Hold time check.

Replacement Plug Pin #	Bits Tested
12	AØ,DØ
13	A1,D1
14	A2,D2
15	A3,D3
16	A4,D4
17	A5,D5
18	A6,D6
19	A7,D7
21	A8
22	A9
23	A10
24	A11
25	A12
26	A13
27	A14
28	A15

2. Check /ALE Setup and Hold.

   a) Turn the 7D02 Power OFF.

   b) Change the PG 508 Duration to 40 ns.

   c) Connect the PG 508 to ZIF socket pins 20 (Gnd), 30, and 37 (clock).

   d) Turn 7D02 power ON.

   e) Press the following 7D02 keys in sequence:

      ELSE
      TRIGGER
      USER CLOCK QUAL
      USER CLOCK SYNTHESIS
      DELAY BY 1 (See Fig. 5-4)
      START

   f) The Logic Analyzer display should show SLOW CLOCK.

   g) Press the following 7D02 keys:

      STOP
      IMMEDIATE
      DISPLAY
      PROGRAM

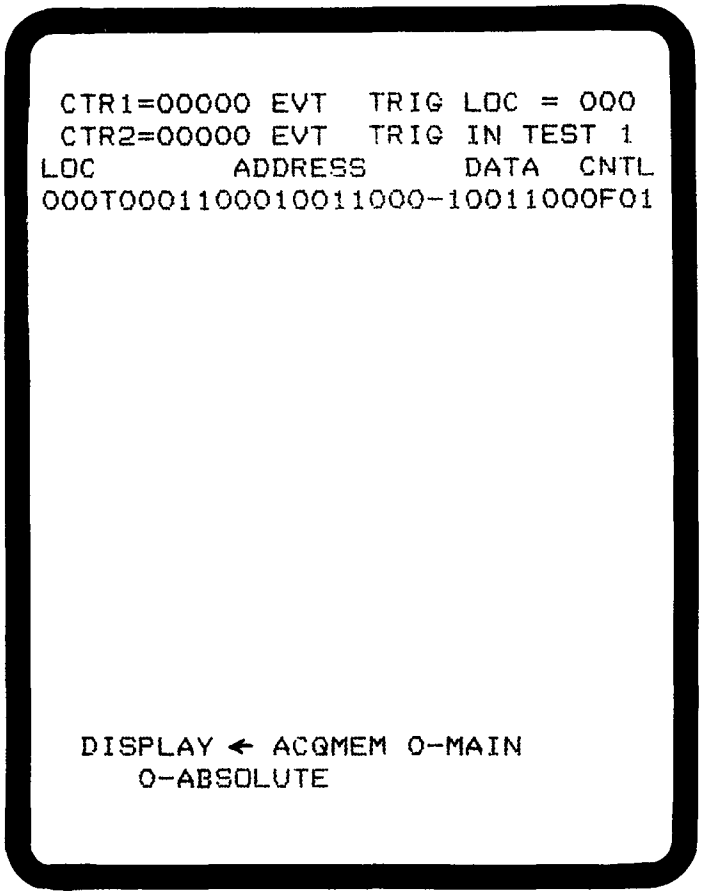


Fig. 5-3. Address and data lines displayed in binary radix. Note that the least significant bit of both address and data show as 0. (AD0 line low.)

h) Change RISING EDGE OF CLOCK to:

FALLING EDGE OF CLOCK
Press START

i) The 7D02 should now trigger and display.

3. Check Delay added to READY ≤35 ns.

a) Connect the PG 508 signal lead to DIP socket pin 35 only.

b) Connect test oscilloscope channel 2 to pin 35 of the ZIF socket on the Personality Module. Set Vertical Deflection factor on the test oscilloscope to 1 V/Div. (Use matched probes for these connections.)

c) Set the test oscilloscope Vertical Mode to Alt.

d) Ground both test oscilloscope channels and position both traces to the center horizontal graticule line.

e) Set both channels to DC.

f) Determine the delay at 1.4 V (it must be <35 ns).

4. Check Wait State Line.

a) With the PM 104 connected to the 7D02 and configured for Self Test, program the 7D02 for Word Recognizer Test #1. Program the following:

ADDRESS Ø000
USER CLOCK QUAL
USER CLOCK SYNTHESIS
DELAY BY Ø

b) Press START, and note that each instruction is repeated three times in the Logic Analyzer display.

c) Change the program to C9=X and press START. Notice that now each instruction is repeated **four** times in the Logic Analyzer display. This shows that the WAIT signal generated by the Self Test circuit is causing the 7D02 to wait one T State. The Self Test circuit generates all four T States, but with C9=1, the Wait State that is inserted is

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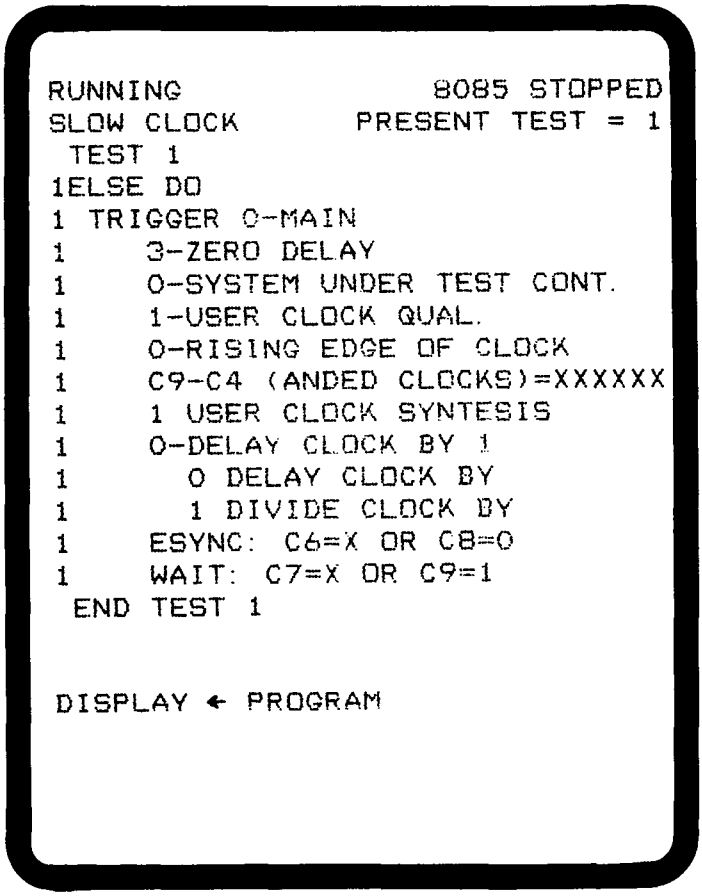


Fig. 5-4. 7D02 delay by 1 triggering arrangement for Setup and Hold check.

not visible because the 7D02 does not store during the Wait State.

This completes the Performance Verification for the PM 104.

MAINTENANCE AND TROUBLESHOOTING

Repair Service

Properly handled and cared for, your PM 104 Personality Module will give dependable service for many years. However, should repair service be needed at any time, Tektronix, Inc. provides complete instrument repair at local Field Service Centers and at the Factory Service Center. Contact your local Tektronix Field Office or representative for further information.

Obtaining Replacement Parts

Most electrical and mechanical parts can be ordered through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from local commercial sources in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Electrical Parts List for the proper value, rating, tolerance, and description.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is important that all of the following information be included to ensure receiving the proper parts.

1. Instrument type (including modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include circuit and assembly numbers).

4. A Tektronix Part Number.

Cleaning Instructions

This instrument should be cleaned as often as operating conditions require. Accumulation of dirt on components acts as an insulating blanket and prevents efficient heat dissipation, which can cause overheating and component breakdown.

Exterior. Loose dust on the Personality Module pod can be brushed off. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

CAUTION

Use only enough water to dampen the cloth or swab. Prevent water from getting inside the pod. Don't allow the Microprocessor Plug or Logic Analyzer Plug to get wet. DO NOT use chemical cleaning agents as they may damage the plastics used in the instrument. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Interior. Dust in the interior should be removed with a jet of dry, low-pressure air, and use of a soft brush. After major repairs, flush the board well with clean isopropyl alcohol. Make certain resin and dirt are removed from the board.

General Operating Precautions

Some simple precautions in operating and handling the PM 104 will prevent unusual wear and tear and generally prolong the useful life of the instrument. These include:

1. Do not attempt to open the test socket door on the bottom of the pod except when Self Test is to be performed.

2. When disconnecting the Microprocessor Plug or the Logic Analyzer Plug, don't pull on the cables. Pull on the plugs themselves.

3. Keep superfluous objects such as hair, dust, jewelry, etc. out of the Pod casing.

Personality Module Disassembly

Access to test points and other interior features of the Personality Module can only be gained by disassembling the Pod case. Eight Allen screws hold the Personality Module together and secure cables and connectors at either end. To remove the top cover from the Pod, remove the four screws nearest the center of the pod with a 3/32" Allen wrench. Lift off the top cover. If the problem is with the Upper Board, troubleshooting can begin at this point.

To gain access to the lower board, remove the four screws attaching the cable hold-down clamps to the bottom cover, using a 3/32" Allen wrench and a 1/4" hex driver or hex wrench.

Remove the hold-down clamps and gently life the circuit boards from the bottom cover. Carefully separate the two boards by disconnecting J3005 from P3005. See Fig. 6-1 for details.

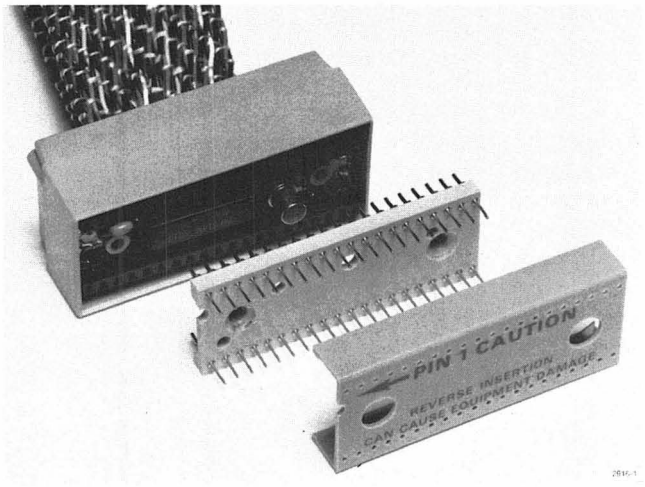


Fig. 6-1. Disassembling the PM 104 plug.

Turn both boards component-side up and reconnect J3005 and P3005 so that the boards lie side by side and all components are exposed. All points are now accessible for troubleshooting.

To re-assemble the PM 104, reverse the above procedure.

Microprocessor Plug Disassembly

The pins on the Microprocessor Plug are very delicate and can be bent or broken quite easily. If this happens, it will be necessary to disassemble the Microprocessor Plug and replace the pin assembly. The pins are replaced as a unit, using the Tektronix Microprocessor Plug Contact Assembly, Tektronix Part No. 352-0536-00. To make this replacement, or to gain access to the circuit board inside the Microprocessor Plug, remove the two Phillips screws holding the contact assembly on the plug. Figure 6-2 shows details of disassembly. With a small screwdriver, gently pry the contact assembly from the circuit board connectors.

To re-assemble the Microprocessor plug, reverse the above procedure. Be sure pin 1 of the contact assembly matches pin 1 of the circuit board assembly. In fitting the protective face over the pins, the edge flanges of the face cover must be pried apart. Be careful that all pins are aligned with the holes and that none are bent down as the face cover is slid into place. Complete the re-assembly by replacing the Phillips screws.

Logic Analyzer Plug Disassembly

If it becomes necessary to disassemble the Logic Analyzer Plug, use the following procedure:

Remove the four screws holding the plug together with a 3/32" Allen wrench. Pull the halves of the connector apart, and remove the cable hold-down clamp. Remove the circuit board by lifting up on the connector end and sliding the board out of the plastic hold-down flanges.

Reverse this procedure for re-assembly of the Logic Analyzer Plug.

Troubleshooting the PM 104

When trouble occurs in the PM 104, several methods are available to the service technician for localizing and identifying the faulty component or circuit. Part I of the Performance Verification in Section 5 tests many of the functions of the Personality Module. The Diagnostic Monitor and Timing Option tests performed by the 7D02 and described below test all of the PM 104's functions—and finally, the Signature Analysis described at the end of this section checks the condition of each logic circuit node in the Personality Module during a selected operating time window.

Preliminary Setup

To obtain access to the test points on the PM 104 Upper and Lower boards, complete the Personality Module dissassembly procedure described earlier in this section.

Connect the Microprocessor Plug to the Self-Test Socket on the Lower Board. (See Fig. 6-3.) Move the jumper strap on J6010 (located near pin 1 of the Self-Test socket) from NORM to TEST position. This enables the Self-Test circuitry of the PM 104 for the remainder of the diagnostic testing procedure.

While holding down any of the 7D02 keys, turn the 7D02 Power Switch ON and wait for the display to appear. The "POWER UP VERIFICATION" will indicate that the "KEYBOARD" test has failed, due to the key having been held down (Fig. 6-4A). This allows access to the more detailed diagnostics in the 7D02 firmware.

Press the X (Don't Care) key on the 7D02 Numeric Entry key pad to enter the Diagnostic Monitor. A diagnostic menu (Fig. 6-4B) will appear on the display.

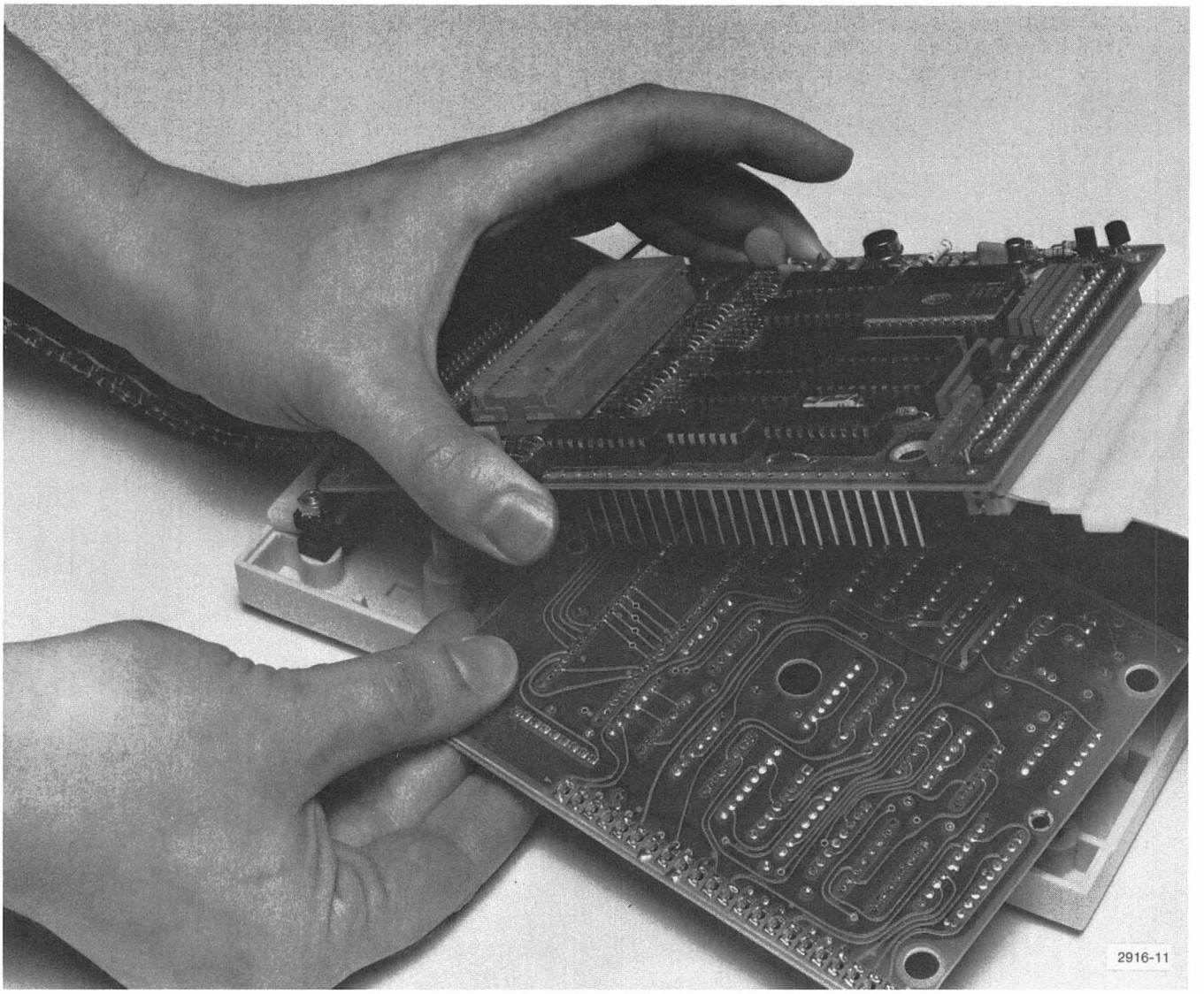


Fig. 6-2. Removing the top board of the PM 104.

Press 9 on the Numeric Entry key pad to enter Personality Module diagnostics. The display next asks for "SELF TEST STIMULUS" (Fig. 6-4C), which has already been provided by connecting the Microprocessor Plug to the Self-Test Socket. Press the START key to begin the Personality Module tests which are described in the following paragraphs. When all tests have been successfully completed, the display shown in Fig. 6-4D appears.

TEST 1

The first test in the Diagnostic Monitor checks the Data line from the 7D02 to the Personality Module ROM for high and low data, checks the Logic Analyzer's ability to read the ROM, and checks the functioning of the /SEL P and LOOK lines from the 7D02 to the PM 104. The test reads a byte (ØE7H) in the Personality Module to determine the length of the ROM. Using this data, it locates the ROM Trailer and reads the value at location 3E7FC. This value is compared with the value at 3E7FD, which should be its complement. If the two bytes are not complementary, the displayed error message for a 2K ROM (the only size used in the PM 104) is:

1 FAIL 3E7FD - X

If an incorrect value is found at 3EØ1Ø, the error message is:

1 FAIL 3YYFD - X

The X signifies the first non-complementary data bit when the two bytes are compared on a bit-by-bit basis from least significant to most significant bit. The most significant part of the address implies the ROM lengths, as indicated by the value at 3EØ1Ø. If the ROM cannot be read correctly,

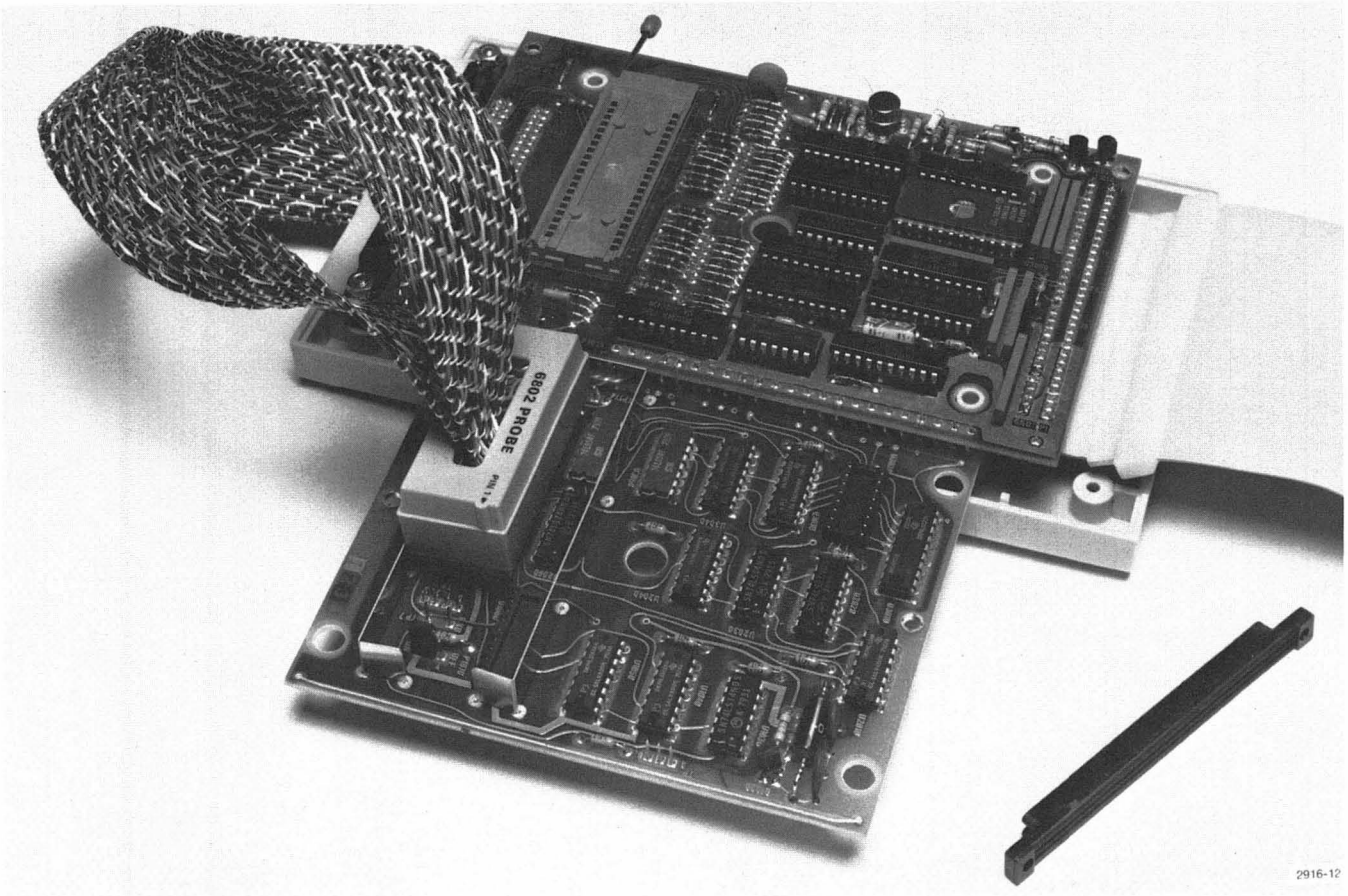


Fig. 6-3. PM 104 boards connected for testing.

this byte may be any random value (as indicated by YY in the second error message display). If the ROM is not present in the circuit, or cannot be read at all, the value will usually be 3FFH.

If the part of the test just described passes, it is assumed that the ROM can be read correctly and the ROM location is checked. The value at 3E7F9 should be equal to ØE7H. If the Location Byte is correct, the test will print "PASS" followed by the ROM part number. If incorrect, the test will print "FAIL" followed by the part number—for example, 1 PASS 0835-00 or 1 FAIL 0835-00. This is the only place in the tests where any data follows the word "PASS". It is not a failure, but actually a way of verifying that the correct ROM is present. The part number prefix is 160-, so the complete ROM part number is this case is 160-0835-00.

TEST 2

This test ensures that all ROM addresses are read correctly, and that the ROM functions properly. A failure in Test 2 may imply a bad address line, or a faulty ROM. If a failure occurs, the information on the address lines may be checked with a test oscilloscope, or by Signature Analysis as described later in this section.

Test 2 calculates a 16-bit checksum on the Personality Module ROM in accordance with standard Tektronix practice. In the test, the ROM Trailer is located using the value read from 3EØ1Ø in Test 1. The starting address of the checksum is determined. All bytes in the ROM except the two highest bytes are checksummed. When this calculation is complete, the result is compared to the sum of the values in the two remaining locations. If the values do not match exactly, the test fails and the calculated checksum value is displayed as 2 FAIL XXXX, where XXXX is the calculated checksum. If the first part of Test 1 failed, this test will probably also fail. However, if the second part of Test 1 failed, this test may still pass, since the checksum is location-independent.

TEST 3

Test 3 checks the clock circuitry and the /ALE line from the Personality Module to the 7D02. Failure of the system to trigger, if caused by the Personality Module, probably means that an address or data line or one of Control lines CØ-C5 has faulty information.

Prior to running this test, the four Word Recognizers are programmed according to data stored in the Per-

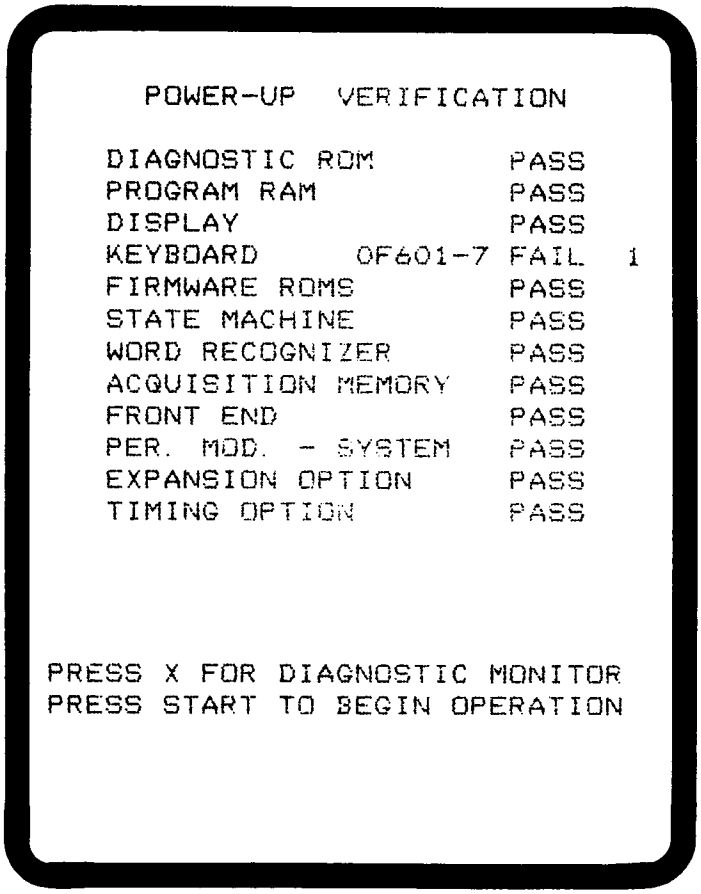


Fig. 6-4A. 7D02 power-up failure display.

sonality Module ROM. Since the PM 104 does not use the Expansion Option, the Address lines A16-A23 and Data lines D8-D16 are set to "Don't Care". The External Trigger and Asychronous Trigger are always set to "Don't Care". The Word Recognizers will remain programmed to these values throughout the remainder of the Personality Module Diagnostic Tests. The state machine is programmed as follows:

```
1    IF WR1 THEN TRIGGER MAIN AND TIMING
1    IF WR2 or WR3 or WR4, THEN DON'T
     TRIGGER
1    GOTO 1
```

and the Acquisition Memory Board is set for Ø Delay. The Front End Qualifiers and Clock Shifter/Divider are programmed according to data stored in the Personality Module ROM. After all setups are complete a DISPLAY command is sent and the slow clock detector is checked. A Slow Clock indication will result in the following error:

```
3    FAIL ØFF6Ø1 ; SLOW, OR NO CLOCK
```

If the clock appears to be running, the Personality Module ROM is read to determine how long the 7D02 should wait for a trigger to occur, then a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory Board is examined to see if the main section has triggered and returned to Display Mode. If the Main Section is still in Store Mode, the following error is generated:

```
3 FAIL  2E8Ø3-7 ; MAIN SECTION FAILED TO
TRIGGER
```

Failure to trigger can be caused by failure of the Personality Module to generate the WR1 value, failure of the Word Recognizer, the State Machine, or the Acquisition Memory to respond, or lack of State Clocks from the Front End board. A faulty Activity Monitor may also be responsible.

If the Main Section has triggered, a DISPLAY command is sent before proceeding further. This makes certain that the Timing Option will not remain in Store Mode and interfere with reading the Personality Module ROM. The next step is to read the "Last Address +1" Buffer and calculate the trigger location. The trigger location in the Acquisition Memory is examined and the data stored there is compared with the data in the Personality Module ROM that was used to program WR1. Any values that were set to "Don't Care" in WR1 are not compared. If the acquired data does not match the expected data, the following error is reported:

```
3 FAIL 2YYZZ-X ; TRIGGER VALUE INCORRECT
```

YYZZ is the Acquisition Memory address which holds the data that does not match. The X is the first bit that did not match when comparison was made from least significant bit through most significant bit. The data is compared one byte at a time in the following order:

A0-A7	
A8-A15	
D0-D7	
C0-C5	

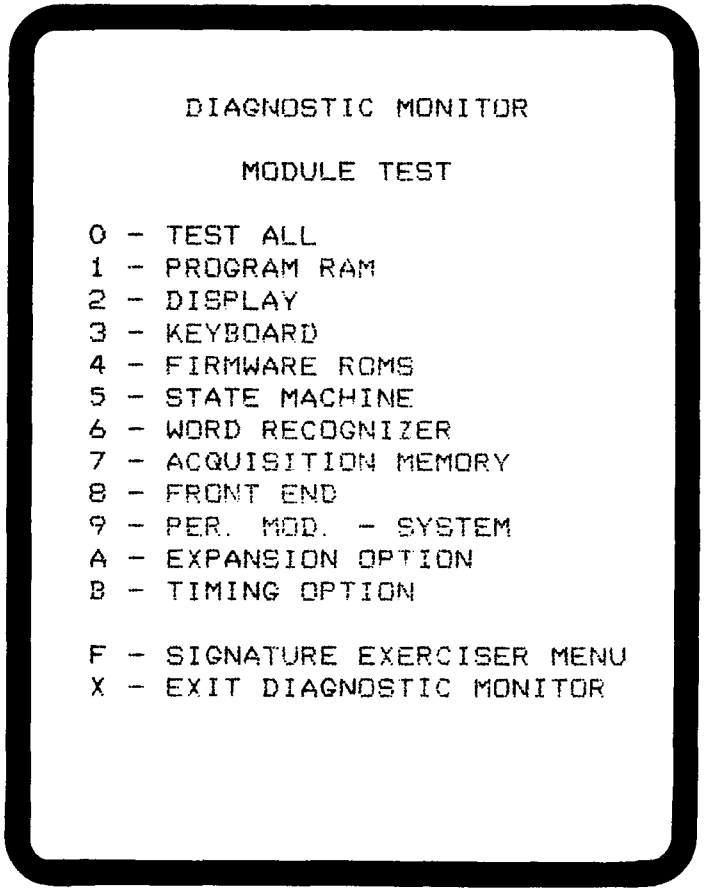


Fig. 6-4B. 7D02 diagnostic monitor module test menu.

The FAIL data is interpreted as follows:

YY=	ZZ=	X9	7	6	5	4	3	2	1	0
E0, E1, E2, E3	X0, X4, X8, XC		A7	A6	A5	A4	A3	A2	A1	A0
E0, E1, E2, E3	X1, X5, X9, XD		A15	A14	A13	A12	A11	A10	A9	A8
E0, E1, E2, E3	X2, X6, XA, XE		D7	D6	D5	D4	D3	D2	D1	D0
E0, E1, E2, E3	X3, X7, XB, XF		-	-	C5	C4	C3	C2	C1	C0

This type of failure may be caused by a faulty part in the Acquisition Memory, a bad Memory Address counter, or a faulty "Last Address +1" Buffer. If the Word Recognizer has triggered on the wrong word, or if the state machine has sent Stop Trace prematurely, this failure might result. Still another possibility is that the Main Section failed to acquire data at all.

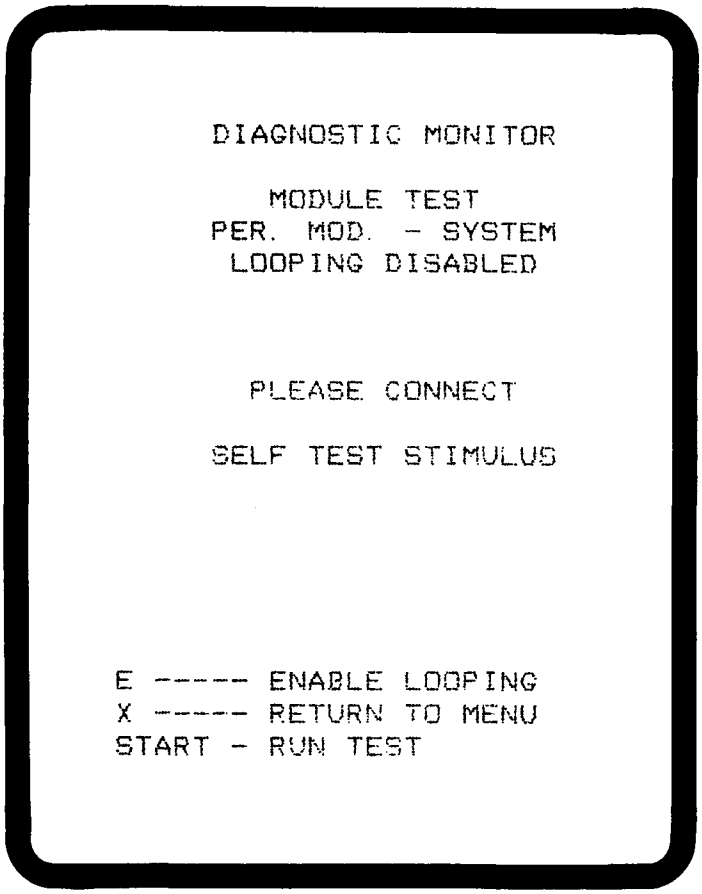


Fig. 6-4C. 7D02 diagnostic monitor SELF TEST STIMULUS display.

TEST 4

This test checks all four Word Recognizers, the two counters, the State Machine, and the Acquisition Memory. The four Word Recognizers are programmed as described in Test 3. The State Machine is programmed as follows:

```
1 QUALIFY ALL
1 IF WR2 OR WR3 OR WR4 THEN GOTO 1
1 IF WR1 THEN RESET CTR1 and CTR2, GOTO 2

2 QUALIFY ALL
2 IF WR1 or WR3 or WR4 THEN GOTO 2
2 IF WR2 THEN GOTO 3
2 ELSE INC CTR1

3 QUALIFY ALL
3 IF WR1 OR WR2 OR WR4 THEN GOTO 3
3 IF WR3 THEN GOTO 4
3 ELSE INC CTR2

4 IF WR1 or WR2 OR WR3 THEN GOTO 4
4 IF WR4 THEN (DON'T QUALIFY), AND
  TRIGGER BOTH
4 ELSE, QUALIFY
```

Starting in State 1, as each of the four Word Recognizers occurs in order, the State Machine advances to the next state. While in State 1, the two counters are reset. While in State 2, Counter 1 is incremented, and while in State 3, Counter 2 is incremented. As this takes place, the Acquisition Memory is acquiring data. When Word Recognizer 4 occurs, that one data sample is not stored, and both the Main Section and the Timing Option are triggered. At this point, the Acquisition Memory Delay Counter begins counting down 240 State Clocks. At the completion of the countdown, it ceases to acquire data. The Acquisition Memory contains the last 16 words generated immediately after Word Recognizer 4. If the Qualify RAM has worked properly, the Word Recognizer 4 value has not been stored. Counter 1 contains the number of clocks that occurred between Word Recognizers 1 and 2, and Counter 2 contains the number of clocks that occurred between Word Recognizer 2 and Word Recognizer 3. The Acquisition Memory Board is set for a delay of 240 clocks, and the Memory Address Counter is preset to ØFDH. The Front End Qualifiers and Clock Shifter/Divider are programmed according to data stored in the Personality Module ROM. After all setups are complete, a DISPLAY command is sent, and the Slow

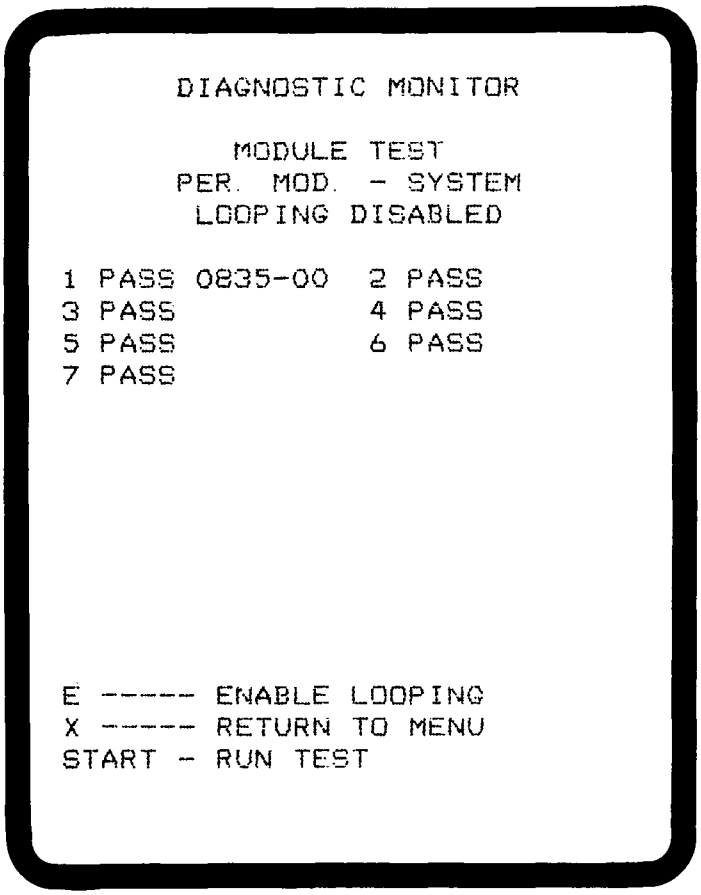


Fig. 6-4D. Successful module test display.

Clock Detector is checked. A Slow Clock indication will result in the following error message:

4 FAIL ØFF6Ø-1 ; SLOW, OR NO CLOCK

If the clock appears to be running, the Personality Module ROM is read to determine how long the 7D02 should wait for a trigger to occur, then a STORE command is sent. After waiting the specified length of time, the Activity Monitor on the Acquisition Memory Board is examined to see if the Main Section has triggered and returned to Display Mode. If the Main Section is still in Store Mode, the following error message is generated:

4 FAIL 2EØ3-7 ; MAIN SECTION FAILED TO TRIGGER

Failure to trigger can be caused by failure of the Personality Module to generate any one of the four Word Recognizer values. Failure of the Word Recognizer, the State Machine, or the Acquisition Memory to respond, or lack of State Clocks from the Front End Board could cause this failure, as could a faulty Activity Monitor.

If the Main Section has triggered, a DISPLAY command is sent before proceeding further. This ensures that the Timing Option will not remain in Store Mode and interfere with the reading of the Personality Module ROM. The Memory Full bit of the Activity Monitor is examined next. As long as there are at least 16 clocks between the occurrence of Word Recognizer 1 and Word Recognizer 4, the Acquisition Memory must be full. If the Memory Full bit indicates otherwise, the following error message will result:

4 FAIL 2E8Ø3-5 ; MEM FULL BIT NOT SET

The next part of the test is a check of the counters. First the most significant bit of Counter 1 is read and compared with the expected value stored in the Personality Module ROM. If it matches, the least significant bit is compared, then Counter 2 is checked. If any byte fails to match exactly, the following error message will be printed:

4 FAIL 1E2Ø2-X ; CTR1 MSB BIT X IS WRONG
4 FAIL 1E2Ø3-X ; CTR1 LSB BIT X IS WRONG
4 FAIL 1E3Ø2-X ; CTR2 MSB BIT X IS WRONG
4 FAIL 1E3Ø3-X ; CTR2 LSB BIT X IS WRONG

If the counters function properly, the next step is to checksum the Acquisition Memory. All bytes between 2EØØØ and 2E3FF are added together and the result is

@

saved. The result of the checksum is compared with the expected data in the PM 104 ROM. Failure of the comparison will result in the following error message:

4 FAIL 3EØ35-X ; MAIN ACQ. MEM. FAILS CHECKSUM

Since this RAM is checked separately in the Acquisition Memory test, this test is primarily a test of the ability of the RAM to acquire data at high speed. This one checksum could point up an error in any of several areas, such as the Memory Address Counter, the Qualify RAM, or the PM 104 Data Buffers on the Word Recognizer Board. The PM 104 itself, the Front End Qualifiers, or the Acquisition Memory could also be faulty.

TEST 5

This test checks the ability of the State Machine time base to generate ms clocks, and the ability of CTR1 to count those clocks while operating in Control Mode. In Control Mode, the State Machine is programmed as follows:

```
1 RESET AND START CTR1 50 MS
1 STOP CTR2
1 GOTO 2

2 CONTINUE CTR1
2 STOP CTR2
2 GOTO 2
2 IF CTR1 = Ø THEN TRIGGER
```

The counters are both loaded with 48 (Desired count - 2) and placed in Control Mode (Decrement). The CTR1 time base is set to MS. A DISPLAY Command is sent, and the Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the PM 104. If none is present, the following error message appears:

5 FAIL ØFF6Ø-1 ; SLOW OR NO CLOCK FROM PER. MOD.

If a clock is present, a STORE Command is sent and the processor enters a delay loop for 46 ms. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see whether the State Machine has timed out and returned to Display Mode. If this has occurred, the following error is displayed:

5 FAIL 2E8Ø-3 ; CTR1 TIMED OUT PREMATURELY

If the Main Section remains in Store Mode, the processor delays another 8 ms, then checks the Activity Monitor again. If the Main Section has not returned to Display Mode, this error message appears in the display:

5 FAIL 2E8Ø3-7 ; CTR1 DIDNT TIME OUT IN 50 MS

Since the processor and Counter Time Base are both derived from the same 6 MHz cyrstal, this is not intended as a check of absolute time base accuracy.

This type of error might be caused by failure of the Time Base Divider on the State Machine Board; by failure of the counter to count clock pulses correctly, or by failure of the State Machine to respond to the Counter reaching zero.

TEST 6

Test 6 checks the ability of the State Machine Time Base to generate μs clocks, and the ability of Counter 2 to count those clocks while operating in Control Mode. The State Machine is programmed as follows:

```
1 RESET AND START CTR2 50000 US
1 STOP CTR1
1 GOTO 2

2 CONTINUE CTR2
2 STOP CTR1
2 GOTO 2
2 IF CTR2 = Ø THEN TRIGGER
```

The counters are both loaded with 49998 (Desired count -2), and placed in Control Mode (Decrement). The CTR2 Time Base is set to μs. A DISPLAY Command is sent and the Acquisition Memory is set for zero delay. The Slow Clock Detector is checked for the presence of a clock from the PM 104. If none is present, the following error is displayed:

6 FAIL ØFF6Ø-1 ; SLOW OR NO CLOCK FROM PER. MOD.

If a clock is present, a STORE Command is sent and the processor enters a delay loop for 46 ms. At the end of the delay, the Acquisition Memory Activity Monitor is checked to see if the State Machine has timed out and returned to Display Mode. If this has occurred, an error message is displayed:

6 FAIL 2E8Ø3-2 ; CTR2 TIMED OUT PREMATURELY

If the Main Section remains in Store Mode, the processor delays another 8 ms, then checks the Activity Monitor again. If the Main Section has not returned to Display Mode, the error message is:

6 FAIL 2E8Ø3-7 ; CTR2 DIDNT TIME OUT IN 50000 US

The processor and Counter Time Base are derived from the same 6 MHz crystal, so this is not intended as a check of absolute Time Base accuracy.

Errors of this type may result from failure of the Time Base Divider on the State Machine Board, by failure of the counter to count the clock pulses correctly, or by failure of the State Machine to respond as the counter reaches zero.

TEST 7

This test checks the Control (Qualifier) lines C4-C9 on the Front End Board. The State Machine is programmed as follows:

```
1 IF WR1 THEN TRIGGER MAIN
1 GOTO 1
```

Word Recognizer 1 was programmed earlier to a value specified by the Personality Module. This test uses each of the Control Lines in turn to qualify out the value to which WR1 has been programmed. If the Control Line operates correctly, the State Clock that occurs with WR1 will be inhibited, and the State Machine will not see the Word Recognizer output. Thus, a PASS condition is indicated by the failure of the Main Section to trigger. A byte in the PM 104 ROM specifies how long the processor should wait for the trigger to occur.

The Clock Shifter/Divider, /ESYNC, and /WAIT are set up in the normal manner as specified by the PM 104 ROM. Six additional bytes in the Personality Module ROM specify the value to write to the Front End Board for each of the six Control Lines to inhibit State Clocks at the occurrence of WR1. The following sequence is repeated six times, once for each Control Line (or until a failure occurs).

```
READ VALUE FROM PER. MOD. ROM
WRITE VALUE TO FRONT END LATCH
SEND STORE COMMAND
WAIT SPECIFIED LENGTH OF TIME
CHECK ACTIVITY MONITOR ON ACQ. MEM.
  BOARD
IF IN DISPLAY MODE PRINT FAIL AND STOP
```

Because of the way this test operates, a PASS indication may be caused by anything that prevents the Store/Display flipflop on the Acquisition Memory Board from returning to Display Mode. For example, lack of a Clock from the PM 104 may produce a PASS. However, if Tests 3 and 4 pass, it can be assumed that TEST 7 is operating correctly. Test failures on the respective Control Lines are indicated by the following error displays:

```
7 FAIL 3EØ39 ; C4 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3A ; C5 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3B ; C6 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3C ; C7 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3D ; C8 DIDNT INHIBIT TRIGGER
7 FAIL 3EØ3E ; C9 DIDNT INHIBIT TRIGGER
```

Summary of Module Test Failures

Failures in the tests just described which result from SLOW or NO CLOCK may indicate one of the following defects:

1. J6010 is not in the Test position.

2. /ALE is not functioning correctly, so there is no ESYNC pulse.

3. WAIT is held high.

4. The Clock circuit of the PM 104 is inoperative.

Failure to read the Personality Module ROM correctly may be caused by a failing address or data line, or a failure on the LOOK or /SEL P lines from the 7D02.

Timing Option Troubleshooting

To set up the 7D02 for troubleshooting using the Timing Option, enter the DISPLAY PROGRAM Mode and move the cursor to the end of the program. Press and hold down the DELETE key to eliminate the existing program. Then perform the keystrokes shown in Table 6-1. (The program display is shown in Fig. 6-5.)

TABLE 6-1

TIMING OPTION TROUBLESHOOTING PROGRAM SETUP

Keystroke	Function
WD RECOGNIZER	Word Recognizer #1
1	Timing WR = 1
Ø	Sync
ØØØØØØØØ	Word Recognizer = ØØØØØØØØ
COUNTER	Counter #1 Ø-Events
COUNTER	
Ø Ø 2 5 Ø	Counter #1 = ØØ25Ø Events
TRIGGER	
1	Trigger 1 - Timing
1	Centered
END	End Test 1

Figure 6-6 is a timing diagram of Timing Option functions.

@

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 IO/M=X  INRQ=X  FETCH=X  R/W=X
1 INACK=X  HOLD=X  EXT TRIG IN=X
1 TIMING WR=1
1    THRESHOLD V.  = 0-PLUS 1.40
1    0-SYNC
1      0 SYNC
1      1 ASYNC
1    WORD RECOGNIZER=00000000
1THEN DO
1 COUNTER # 1 0-EVENTS
1    0-INCREMENT
1OR IF
1 COUNTER # 1 = 00250 0-EVENTS
1THEN DO
1 TRIGGER 1-TIMING
1    1-CENTERED
1    THRESHOLD V.  = 0-PLUS 1.40
1    0-SYNC, TRIGGER IMMEDIATE
 END TEST 1
```

2916-17

Fig. 6-5. Timing Option troubleshooting program.

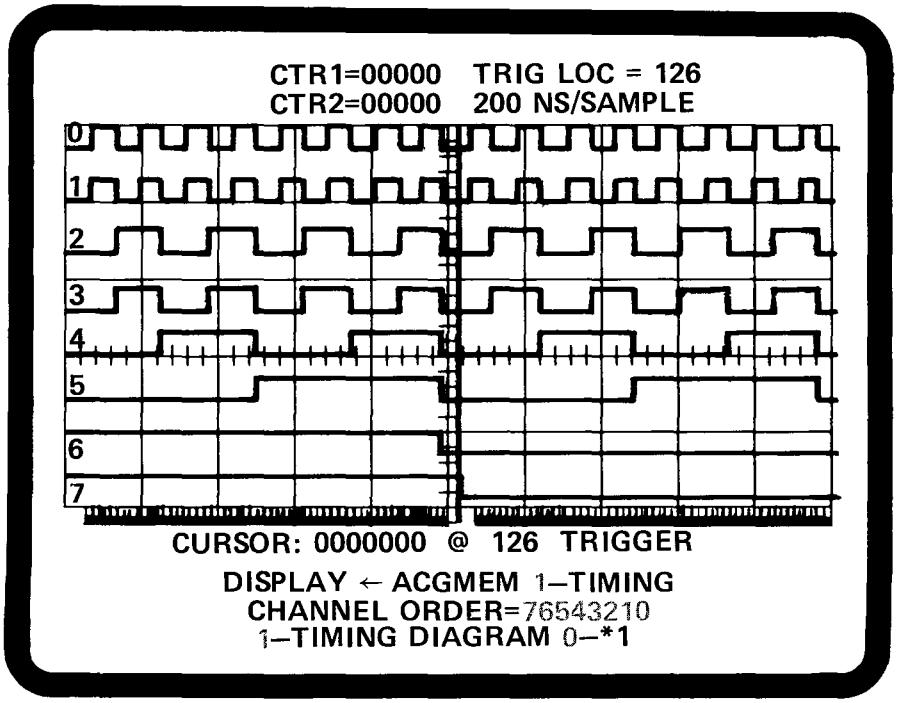


Fig. 6-6. Timing Option diagram.

2918-78

TROUBLESHOOTING BY SIGNATURE ANALYSIS

General Discussion

The recent trend in digital system design is toward bus-structured machines that make use of Large Scale Integration (LSI) components such as microprocessors, ROMs, RAMs, etc. By controlling communication and algorithmic interaction between bus devices, much of the dedicated hardware logic formerly used to handle complex signal and data processing is now replaced by software data manipulation. When logic signals are replaced by data bit streams in a microprocessor system, for example, functional characteristics of the circuit are difficult to associate with a particular part of the circuitry—and when a fault occurs, its location is extremely hard to pin down.

Board exchange and transition counting are two methods of troubleshooting that have been used widely in LSI systems, but both have severe limitations. A new troubleshooting technique that promises faster, more accurate results is Signature Analysis.

The Concept of Signature Analysis

The basic ingredients of Signature Analysis (SA) are "Data Compression" and "Circuit-generated Stimulus."

Data compression is accomplished in the signature analyzer by probing a logic test node from which data is input for each circuit clock cycle occurring within a circuit-controlled time window. Within the signature analyzer is a 16-bit feedback shift register into which the data is entered in either true or complement logic state, according to previous data-dependent register feedback conditions. There are 65,536 (2^{16}) possible states to which the shift register can be set during a measurement window. These states are encoded and displayed as four hexadecimal characters known as a "signature". This four-character signature is a characteristic number representing time-dependent logic activity during a specified measurement interval for a given circuit node. Any change in the behavior of this node (even a transition that occurs one clock cycle late) will produce a different signature, indicating a probable malfunction in the circuit. A single logic state change on a node is all that's needed to produce a useful signature.

The signal that causes the node to produce a signature is the "stimulus." In SA, the stimulus is supplied by the product itself. In this way, a controlled environment is created wherein selected portions of the circuit are tested independently, while maintaining full dynamic operation. Synchronization and measurement intervals for the signature analyzer are controlled by the system under test. In microprocessor systems, the stimulus is a special program—which in the PM 104 is called Self Test.

Signature Analysis Operation

In operation, signals supplied to the signature analyzer start and stop a measurement time period (called a window or a gate). A clock input synchronizes and controls the data sample rate of the signature analyzer probe input so that data is input to the analyzer and processed every clock cycle within a start/stop interval. The start and stop inputs are individually selectable for logic "1" or "0" levels. The clock input is edge triggered, and can be selected for either rising or falling edges. In signature analysis for the PM 104, both start and stop are triggered on negative edges of the clock for all tests. Figure 6-7 illustrates the timing relationships and data generated in a typical measurement window.

PM 104 Signature Analysis

The Signature Tables which follow show the signatures displayed when circuits function properly at each functionally-important pin of each component and connector in the PM 104.

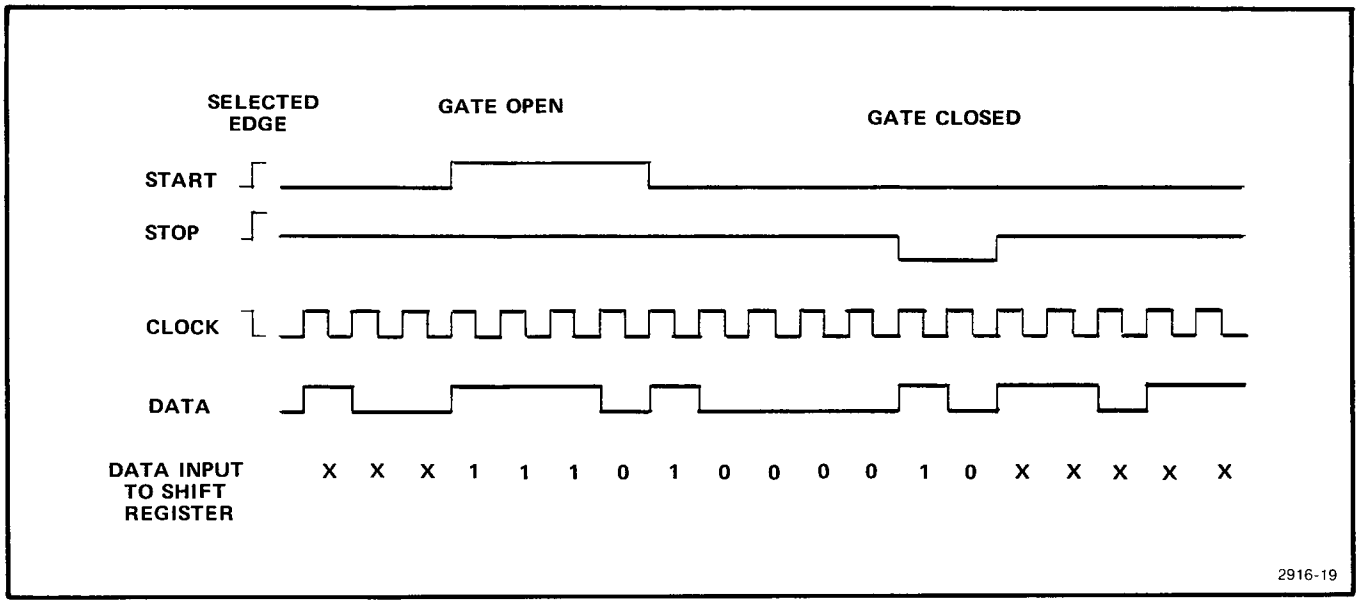


Fig. 6-7. Typical data input to the Signature Exerciser, illustrating the timing relationships between control signals.

PM 104 SIGNATURE TABLES

Signature Analyzer: Sony/Tektronix Type 308 with P6451 Probe

Dissassemble and lay out the Personality Module boards as described in "Personality Module Disassembly" at the beginning of this section. Set Lower board jumper J6010 to the TEST position, and J5030 in NORM position. Connect the Microprocessor Plug to the Self Test Socket on the Lower Board. Connect the Signature Analyzer probe clock lead to TP7010 on the lower board, and the start/stop lead to J6030 pin 9. Set start and stop triggering to negative edge. Power up the 7D02, program WR#1 for Address 111H and push the START button on the 7D02.

Upper Board Signature Tables

A1U2010

Pin	Signature
1	8PP5
2	35H1
3	C8HA
4	03PP
5	FA81
6	71C5
7	0000
8	--
9	--
10	82AH
11	3999
12	--
13	--
14	CC34

A1U2020

Pin	Signature
1	CC34
3	1875
5	7P10
7	6PCP
9	77F7
11	86PA
13	7P25
15	5CP0
17	P5PH

A1U2035

Pin	Signature
1	1875
2	7P10
3	6PCP
4	77F7
5	85PA
6	7P25
7	5CP0
8	P5PH
12	0000
18	CC34
19	7P25
20	CC34
21	CC34
22	5CP0
23	P5PH
24	CC34

A1U2050

Pin	Signature
1	0000
2	1875
3	1875
4	7P10
5	7P10
6	6PCP
7	6PCP
8	77F7
9	77F7
10	0000
11	71C5
12	85PA
13	85PA
14	7P25
15	7P25
16	5CP0
17	5CP0
18	P5PH
19	P5PH
20	CC34

A1U3010

Pin	Signature
1	0000
2	C7F3
3	8P51
4	03PP
5	191F
6	CC34
7	0001
8	--
9	CF1A
10	0000
11	CF1A
12	--
13	0001
14	CC34
15	191F
16	03PP
17	8P5A
18	C7F3
19	0000
20	CC34

A1U3020

Pin	Signature
1	0000
2	71C5
3	CF1A
4	84UU
5	A341
6	8PP5
7	F524
8	451H
9	35H1
10	0000
11	8PP5
12	UP29
13	7P10
14	35H1
15	1875
16	3UFC
17	072P
18	FA81
19	0000
20	CC34

A1U3030

Pin	Signature
1	CC34
2	03PP
3	31U1
4	UP29
5	35H1
6	UA09
7	0000
8	31U1
9	F524
10	A341
11	CF1A
12	03PP
13	CC34
14	CC34

A1U3040

Pin	Signature
1	8P5A
2	C7F3
3	3999
4	35H1
5	03PP
6	9816
7	0000
8	C8HA
9	03PP
10	CC34
11	--
12	--
13	--
14	CC34

A1U3050

Pin	Signature
1	0000
2	1875
3	P5PH
4	7P10
5	5CP0
6	6PCP
7	7P25
8	77F7
9	85PA
10	0000
11	85PA
12	77F7
13	7P25
14	6PCP
15	5CP0
16	7P10
17	P5PH
18	1875
19	0000
20	CC34

A1U3060

Pin	Signature
1	0000
2	9P77
3	P5PH
4	072P
5	5CP0
6	6PCP
7	7P25
8	77F7
9	85PA
10	0000
11	85PA
12	77F7
13	7P25
14	6PCP
15	5CP0
16	072P
17	P5PH
18	9P77
19	0000
20	CC34

IC TEST SOCKET

Pin	Signature
1	--
2	--
3	0001
4	--
5	--
6	8PP5
7	451H
8	7P10
9	1875
10	072P
11	CF1A
12	P5PH
13	5CP0
14	7P25
15	85PA
16	77F7
17	5PCP
18	7P10
19	1875
20	0000
21	P5PH
22	5CP0
23	7P25
24	85PA
25	77F7
26	5PCP
27	072P
28	9P77
29	C7F3
30	71C5
31	--

IC TEST SOCKET (cont.)

32	--
33	8P5A
34	191F
35	03PP
36	0000
37	--
38	--
39	8PP5
40	CC34

A2U1005

Pin	Signature
1	CC34
2	0000
3	--
4	--
5	--
6	--
7	CC34
8	CC34
10	826P
11	6PCP
12	77F7
13	85PA
14	7P25
15	0001

A2U1010

Pin	Signature
1	03PP
2	CC34
3	F96U
4	CC34
5	71C5
6	FA81
8	03PP
9	C8HA
10	CC34
11	--
12	71C5
13	CC34

A2U1020

Pin	Signature
1	5U83
2	CC34
3	71C5
4	CC34
5	71C5
6	FA81
8	5U83
9	P4C7
10	03PP
11	--
12	71C5
13	CC34

A2U1030

Pin	Signature
1	0000
2	253A
3	89FC
4	0001
5	C8HA
6	CF1A
7	A2FU
8	84UU
9	2322
11	9816
12	3UFC
13	C6P2
14	072P
15	03PP
16	CC35
17	32UU
18	9P0P
19	0000

A2U2010

No Signatures Taken

A2U2020

Pin	Signature
1	CC35
2	9P0P
3	F96U
4	CC34
5	5HC1
6	P685
8	--
9	84UU
10	CC35
11	5HC1
12	CC34
13	UA09

A2U2030

Pin	Signature
1	A498
2	82AH
3	C6P2
4	82AH
5	191F
6	32UU
8	A498
9	191F
10	CH84
11	03PP
12	C8HA
13	P4C7

@

A2U3010

Pin	Signature
1	CC34
2	0000
3	--
4	--
5	--
6	--
7	CC34
9	CC34
10	CC34
11	5CP0
12	P5PH
13	725C
14	96PF
15	826P

A2U3020

Pin	Signature
1	CC34
2	072P
3	F96U
4	CC34
5	3072
6	8C46
8	CH84
9	06C0
10	CC34
11	072P
12	8C46
13	6P2U

A2U3030

Pin	Signature
1	71C5
2	3072
3	CC34
4	0001
5	0001
6	6P2U
8	253A
9	A2FU
10	3UFC
11	UA09
12	6P2U
13	CC34

A2U4010

Pin	Signature
1	C7F3
2	8P5A
3	191F
4	7P10
5	1875
6	072P
7	9P77
9	8PP5
10	P5PH
11	5CP0
12	7P25
13	85PA
14	77F7
15	0000

A2U4030

Pin	Signature
1	35H1
2	CC34
3	71C5
4	CC34
5	35H1
6	8PP5
8	725C
9	F96U
10	CC34
11	--
12	5U83
13	CC34

A2U5020

Pin	Signature
1	0000
2	--
3	--
4	5CP0
5	P5PH
6	7P25
7	6PCP
8	85PA
9	77F7
11	77F7
12	85PA
13	6PCP
14	7P25
15	P5PH
16	5CP0
17	--
18	--
19	0000

A2U6005

Pin	Signature
1	9P77
2	71C5
3	UP29
4	072P
5	072P
6	C71A
8	451H
9	UP29
10	UP29
11	F96U
12	725C
13	725C

U6030

Pin	Signature
1	0000
2	P5PH
3	P5PH
4	5CP0
5	5CP0
6	7P25
7	85PA
8	77F7

TEST POINTS

TP	Signature
3020	F96U
7005	0001
7020	03PP
7025	71C5

PM 104 Self-Test Information

The Self Test circuitry in the PM 104 comprises an oscillator, a binary counter, a 32 by 8 PROM, and some additional logic gates which provide the Clock, ALE, and Wait signals. The counter outputs are used to address the PROM and to provide information on certain Address and Data lines. The outputs of the PROM provide signals on the remaining Address and Data lines, as well as the Interrupt and Control lines. These signals are used to drive the PM 104 circuits so as to simulate the information required to test as much as possible of the PM 104 circuitry. When stored in the 7D02 Memory, the test circuit signals can be disassembled and displayed in mnemonic mode. Many of the 8085A mnemonic types are simulated.

The Counter circuit counts from Ø to 63 and resets. During this cycle, each PROM location is addressed twice. Therefore, the information sent out from the PROM is used twice for each Counter cycle. You can see this by comparing the information at Test Circuit Address ØØØØH with 2Ø2ØH, or 41Ø1H with 6121H, etc. The result is that all address, data, control, and interrupt lines have been toggled at least once during each Counter cycle.

Table 6-2 gives detailed information about the signals that occur on the Self Test circuit lines for each Counter Step.

@

Table 6-2

VERSION 0.0 Check Sum = 0284

Binary Counter	Prom Code	Prom Addr (Hex)	Prom Code (Hex)	Cycle	INTA	RESET OUT	INTERRUPT REQUEST	HOLD-C5 HALTED-C7	INACK
AD5-A13 AD4-A12 AD3-A11 AD2-A10 AD1-A9 AD0-A8	Trap,Hold 7.5, A15 INTR,A14 5.5, AD7 6.5, AD6 IO/M S1 S0								
000000	00000001	00	01	WRITE	1	0		0	0
000001	00100111	01	27	FETCH	0	0	INTR	0	1
000010	00000010	02	02	READ	1	0		0	0
000011	00000010	03	02	READ	1	0		0	0
000100	00011011	04	1B	FETCH	1	0	5.5,6.5	0	0
000101	00000010	05	02	READ	1	0		0	0
000110	060011011	0	1B	FETCH	1	0	5.5,6.5	0	0
000111	00011011	07	1B	FETCH	1	0	5.5,6.5	0	0
001000	00000110	08	06	READ	1	0		0	0
001001	00000110	09	06	READ	1	0		0	0
001010	01000011	0A	43	FETCH	1	0	7.5	0	0
001011	00000010	0B	02	READ	1	0		0	0
001100	00000011	0C	03	FETCH	1	0		0	0
001101	00001011	0D	0B	FETCH	1	0	6.5	0	0
001110	00000011	0E	03	FETCH	1	0		0	0
001111	10000111	0F	87	READ	1	0	TRAP	1	1
010000	00000011	10	03	FETCH	1	0		0	0
010001	00011011	11	1B	FETCH	1	0	5.5,6.5	0	0
010010	00000010	12	02	READ	1	0		0	0
010011	00000010	13	02	READ	1	0		0	0
010100	00010011	14	13	FETCH	1	0	5.5	0	0
010101	00011011	15	1B	FETCH	1	0	5.5,6.5	0	0
010110	00000001	16	01	WRITE	1	0		0	0
010111	00000001	17	01	WRITE	1	0		0	0
011000	00010011	18	13	FETCH	1	0	5.5	0	0
011001	00011011	19	1B	FETCH	1	0	5.5,6.5	0	0
011010	00001011	1A	0B	FETCH	1	0	6.5	0	0
011011	00000011	1B	03	FETCH	1	0		0	0
011100	00111111	1C	3F	FETCH	0	0	INTR,5.5,6.5	0	1
011101	00100111	1D	27	READ	0	0	INTR	0	1
011110	00100111	1E	27	READ	0	0	INTR	0	1
011111	00000001	1F	01	WRITE	1	0/1		0	0

Table 6-2 (cont.)

Binary Counter	Prom Code	Prom Addr (Hex)	Prom Code (Hex)	Cycle	INTA	RESET OUT	INTERRUPT REQUEST	HOLD-C5 HALTED-C7	INACK
AD5-A13 AD4-A12 AD3-A11 AD2-A10 AD1-A9 AD0-A8	Trap,Hold 7.5, A15 INTR, A14 5.5, AD7 6.5, AD6 IO/M S1 S0								
100000	00000001	00	01	WRITE	1	0		0	0
100001	00100111	01	27	FETCH	0	0	INTR	0	1
100010	00000010	02	02	READ	1	0		0	0
100011	00000010	03	02	READ	1	0		0	0
100100	00011011	04	1B	FETCH	1	0	5.5,6.5	0	0
100101	00000010	05	02	READ	1	0		0	0
100110	00011011	06	1B	FETCH	1	0	5.5,6.5	0	0
100111	00011011	07	1B	FETCH	1	0	5.5,6.5	0	0
101000	00000110	08	06	READ	1	0		0	0
101001	00000110	09	06	READ	1	0		0	0
101010	01000011	0A	43	FETCH	1	0	7.5	0	0
101011	00000010	0B	02	READ	1	0		0	0
101100	00000011	0C	03	FETCH	1	0		0	0
101101	00001011	0D	0B	FETCH	1	0	6.5	0	0
101110	00000011	0E	03	FETCH	1	0		0	0
101111	10000111	0F	87	READ	1	0	TRAP	1	1
110000	00000011	10	03	FETCH	1	0		0	0
110001	00011011	11	1B	FETCH	1	0	5.5,6.5	0	0
110010	00000010	12	02	READ	1	0		0	0
110011	00000010	13	02	READ	1	0		0	0
110100	00010011	14	13	FETCH	1	0	5.5	0	0
110101	00011011	15	1B	FETCH	1	0	5.5,6.5	0	0
110110	00000001	16	01	WRITE	1	0		0	0
110111	00000001	17	01	WRITE	1	0		0	0
111000	00010011	18	13	FETCH	1	0	5.5	0	0
111001	00011011	19	1B	FETCH	1	0	5.5,6.5	0	0
111010	00001011	1A	0B	FETCH	1	0	6.5	0	0
111011	00000011	1B	03	FETCH	1	0		0	0
111100	00111111	1C	3F	FETCH	0	0	INTR,5.5,6.5	0	1
111101	00100111	1D	27	READ	0	0	INTR	0	1
111110	00100111	1E	27	READ	0	0	INTR	0	1
111111	00000001	1F	01	WRITE	1	0/1		0	0

@

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

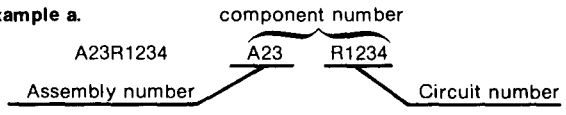
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

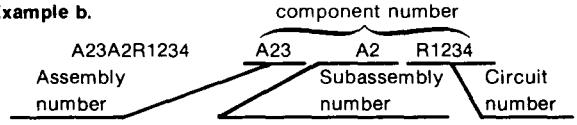
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
52648	PLESSEY SEMICONDUCTORS	1641 KAISER	IRVINE, CA 92714
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-6152-00			CKT BOARD ASSY:PM104	80009	670-6152-00
A2	670-6153-00			CKT BOARD ASSY:PM104	80009	670-6153-00
A3	670-6149-00			CKT BOARD ASSY:PROBE CONNECTOR	80009	670-6149-00
	----- -----			(NO ELECTRICAL PARTS)		
A4	----- -----			CKT BOARD ASSY:8085 PROBE		
	----- -----			(NOT REPLACEABLE ORDER 175-2680-00)		
A1	----- -----			CKT BOARD ASSY:PM104		
A1C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2040	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2050	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C2060	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1C4030	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C4050	283-0346-00			CAP.,FXD,CER DI:0.47UF,+80-20%,100V	72982	8131-M100F474Z
A1C4055	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	72982	1035D2ADC0G569D
A1C4060	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	72982	8101A058C0K159B
A1C4061	283-0160-00			CAP.,FXD,CER DI:1.5PF,10%,50V	72982	8101A058C0K159B
A1C4064	283-0136-00			CAP.,FXD,CER DI:10PF,5%,50V	51642	A100050-NP0-100J
A1C4068	281-0765-00			CAP.,FXD,CER DI:100PF,5%,100V	51642	G1710100X5P101J
A1C5060	283-0136-00			CAP.,FXD,CER DI:10PF,5%,50V	51642	A100050-NP0-100J
A1C7060	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
A1C7061	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A1CR2062	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR2066	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR4020	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4030	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4050	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR4055	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR7060	152-0071-00			SEMICOND DEVICE:GERMANIUM,15V,40MA	14433	G865
A1Q1075	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1Q2070	151-0427-00			TRANSISTOR:SILICON,NPN	80009	151-0427-00
A1Q2071	151-0282-00			TRANSISTOR:SILICON,NPN	80009	151-0282-00
A1R1005	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1020	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1030	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1040	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1050	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R1060	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R2055	307-0721-00			RES.,NTWK,FXD,FI:5,68 OHM,2%,1.5W	91637	MSP10A03680G
A1R2064	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R3070	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A1R3071	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R4020	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A1R4025	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R4055	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A1R4060	321-0290-00			RES.,FXD,FILM:10.2K OHM,1%,0.125W	91637	MFF1816G10201F
A1R4064	321-0631-00			RES.,FXD,FILM:12.5K OHM,1%,0.125W	91637	MFF1816G12501F
A1R5060	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R5064	321-0293-00			RES.,FXD,FILM:11K OHM,1%,0.125W	91637	MFF1816G11001F
A1R5068	321-0208-00			RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1U2010	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04N3
A1U2020	156-0916-02			MICROCIRCUIT,DI:8-2 INP 3-STATE BFR,BURN	27014	DM81LS97

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U2035	160-0835-00			MICROCIR;CUIT,DI:2048 X 8 EPROM,PRGM	80009	160-0835-00
A1U2050	156-1065-01			MICROCIRLCUIT,DI:OCTAL D TYPE TRANS	34335	AM74LS373
A1U3010	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U3020	156-0914-03			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE	80009	156-0914-03
A1U3030	156-0320-03			MICROCIRCUIT,DI:TRIPLE 3 INP NAND GATE	01295	SN74S11NP3
A1U3040	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A1U3050	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U3060	156-0956-04			MICROCIRCUIT,DI:OCTAL BFR W/3	80009	156-0956-04
A1U4010	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4015	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4020	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4030	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4035	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4040	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4050	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U4055	155-0230-00			MICROCIRCUIT,LI:INPUT PROTECTION	80009	155-0230-00
A1U5064	156-1344-00			MICROCIRCUIT,LI:COMPARATOR	52648	SP9685CM
A1VR4030	152-0512-00			SEMICOND DEVICE:ZENER,1W,9.1V,5%	12969	UZ8709
A1VR7060	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A1VR7060	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A1VR7065	152-0611-00			SEMICOND DEVICE:ZENER,0.4W,9V,2%	80009	152-0611-00
A2	----- -----			CKT BOARD ASSY:PM104		
A2C1010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C1510	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C2020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C3540	290-0847-00			CAP.,FXD,ELCTLT:47UF,+50-10%,10V	54473	ECE-B1AV470S
A2C4000	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4001	283-0687-00			CAP.,FXD,MICA D:560PF,2%,300V	00853	D153E561G0
A2C4006	283-0687-00			CAP.,FXD,MICA D:560PF,2%,300V	00853	D153E561G0
A2C4010	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C4030	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C5010	283-0154-00			CAP.,FXD,CER DI:22PF,5%,50V	72982	8111B061C0G220J
A2C5020	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C6005	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2C6006	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
A2L3005	108-0719-00			COIL,RF:805NH	80009	108-0719-00
A2Q4006	151-0190-05			TRANSISTOR:SILICON,NPN	80009	151-0190-05
A2R1030	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R3006	315-0133-00			RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A2R3007	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A2R4020	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R4025	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R5010	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R6005	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2U1005	156-0844-02			MICROCIRLCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A2U1010	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U1020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U1030	156-0914-02			MICROCIRCUIT,DI:OCT ST BFR W/3 STATE OUT	01295	SN74LS240
A2U2010	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U2020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2U2030	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A2U3010	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A2U3020	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74D
A2U3030	156-0722-00			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	80009	156-0722-00
A2U4010	160-0833-00			MICROCIRCUIT,DI:32 X 8 PROM,PRG	80009	160-0833-00
A2U4030	156-0331-00			MICROCIRCUIT,DI:DUAL D-TYPE,FLIP-FLOP	80009	156-0331-00
A2U5020	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	01295	SN74LS244NP3
A2U6005	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4	----- -----			CKT BOARD ASSY:8085 PROBE		
A4C1040	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N08825U104M
A4CR2020	152-0008-00			SEMICOND DEVICE:GERMANIUM,75V,60MA	14433	G1409
A4Q2020	151-1031-00			TRANSISTOR:SILICON,FE,N-CHANNEL,DUAL	80009	151-1031-00
A4R1030	317-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.125W	01121	BB1315
A4R2020	317-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A4R2021	317-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A4R3030	317-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.125W	01121	BB1015
A4U2030	156-0645-00			MICROCIRCUIT,DI:HEX SCHMITT-TRIG INVERTER	80009	156-0645-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

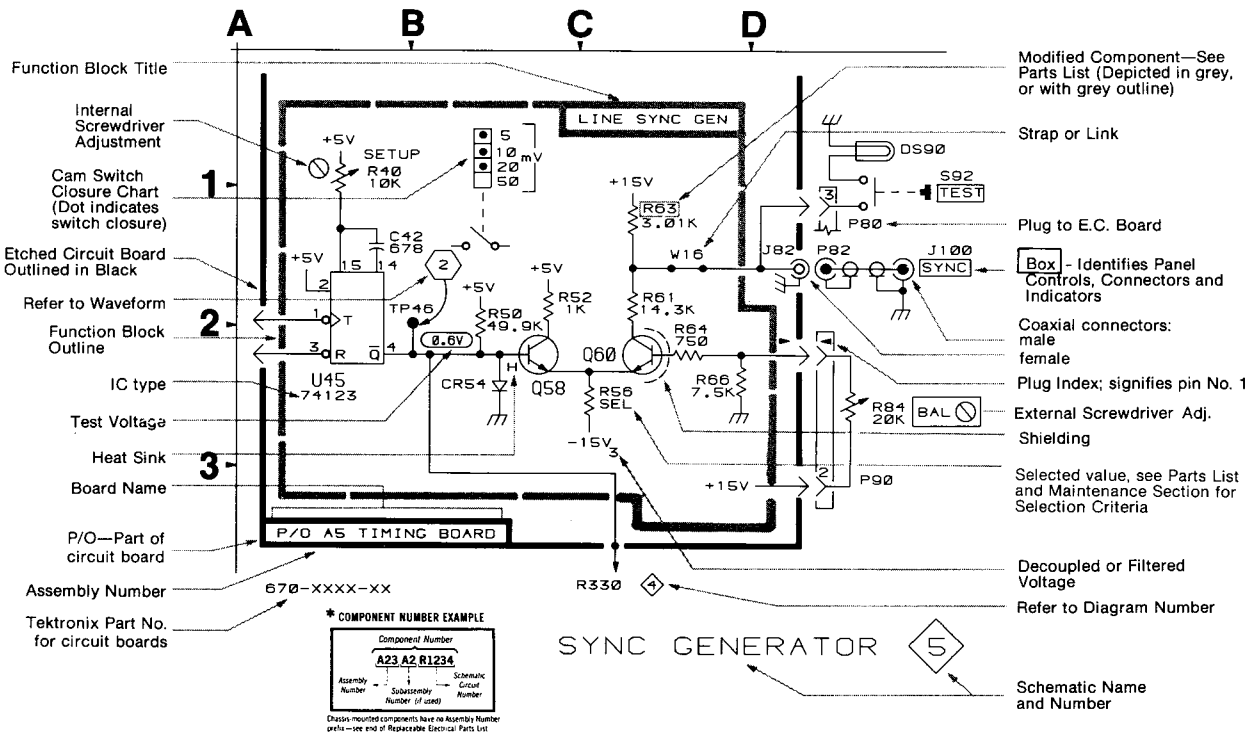
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

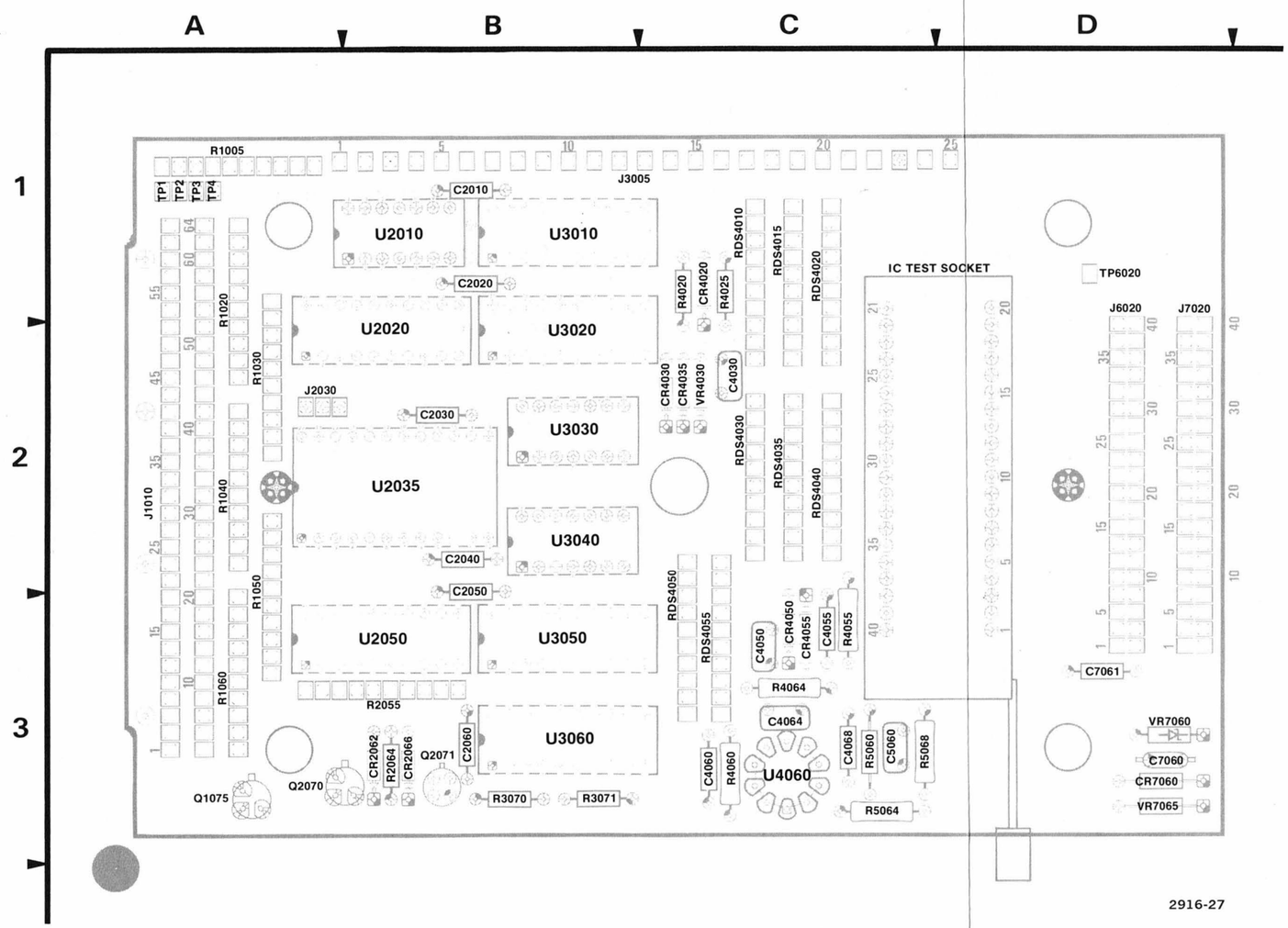
The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



IC Pin Information

Device Type	VCC	GND
2716	24	12
74LS00	14	7
74LS04	14	7
74LS11	14	7
74LS12	14	7
74S74 (LS)	14	7
74LS161	16	8
74LS240	20	10
74LS244	20	10
74LS373	20	10
81LS97	20	10
H1023	1	2
IM5610	16	8

@

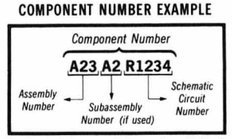


2916-27

Figure 8-1A. A01 Upper board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

@

1 UPPER BOARD DIAGRAM 1A

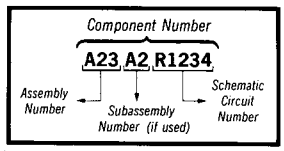
ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C4030	D2	C2	R2055	F3	B3
			R4025	D2	C1
CR4020	D2	C1			
			TP6020	F4	D1
J1010	A5	A2			
J1010	A3	A2	U2010C	C5	B1
J1010	F2	A2	U2020	E4	B2
J1010	E1	A2	U2035	D3	B2
J1010	F5	A2	U2050	C5	B3
J2030	D3	A1	U3020B	C5	B1
J3005	F5	B1	U3050	B3	B3
J3005	F1	B1	U3060	B2	B3
J6020	A5	D1	U4030A	A5	C2
J6020	A2	D1	U4030C	A3	C2
J7020	A3	D1	U4030D	A3	C2
			U4035B	A4	C2
R1005	F1	A1	U4035C	A4	C2
R1005	F5	A1	U4035D	A3	C2
R1030	F4	A2	U4040B	A4	C2
R1040	F4	A2	U4040C	A4	C2
R1040	F2	A2	U4040D	A4	C2
R1050	F3	A3	U4050	A2	C3
R1050	F2	A3	U4055	A2	C3
R1060	F3	A3			
R1060	F2	A3	VR4030	E2	C2
R1060	F4	A3			

Partial A1 also shown on diagram 1B.

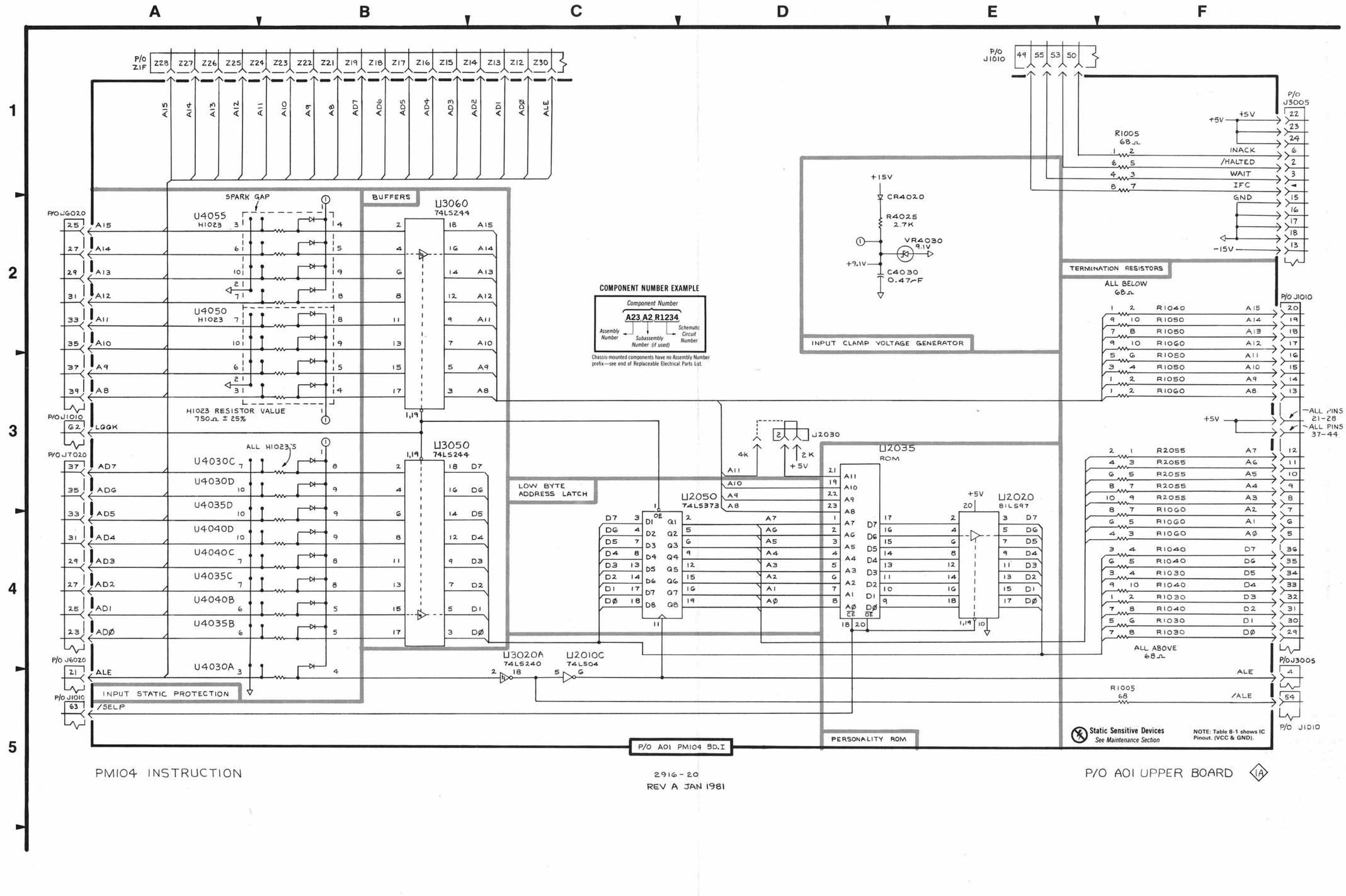
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

C5060



PM104 INSTRUCTION

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REV A JAN 1981

P/O A01 UPPER BOARD 1A

A01 UPPER BOARD

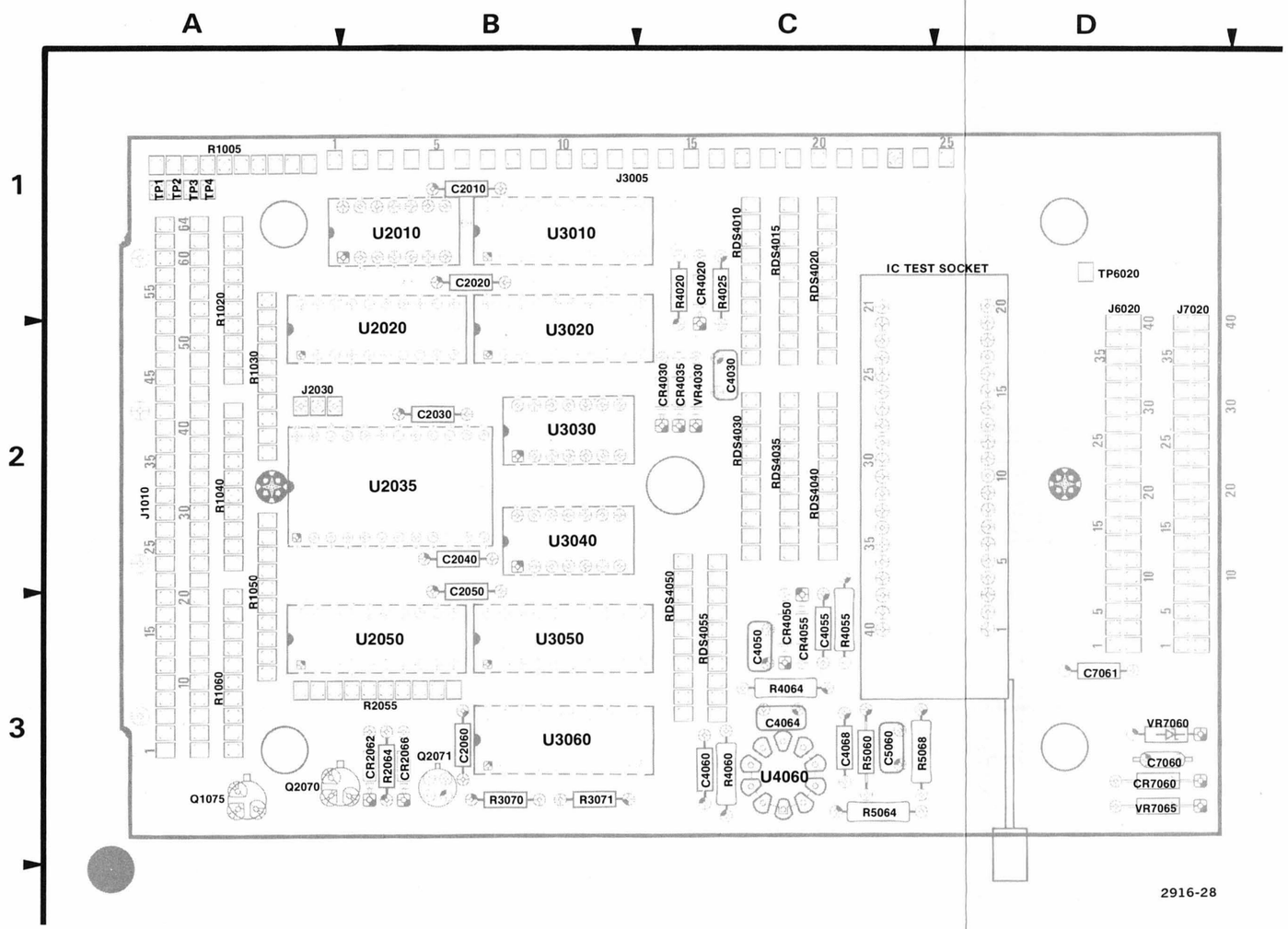
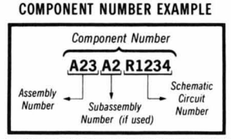


Figure 8-1B. A01 Upper board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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1 UPPER BOARD DIAGRAM 1B

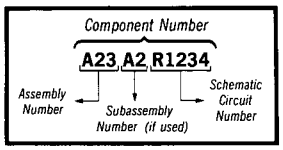
ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2010	C1	B2	J3005	F5	B1	U2010A	C4	B1
C2020	C1	B1	J3005	A4	B1	U2010B	D3	B1
C2030	C1	B2	J3005	F2	B1	U2010E	C2	B1
C2040	C1	B2	J6020	A1	D1	U3010	B3	B1
C2050	C1	B3	J7020	A3	D1	U3010	B2	B1
C2060	C1	B3				U3020B	E1	B1
C4030	E5	C2	Q1075	C5	A3	U3020	B2	B1
C4050	A4	C3	Q2070	D5	A3	U3030A	C3	B2
C4055	A5	C3	Q2071	D4	B3	U3030B	C3	B2
C4060	B5	C3				U3030C	C3	B2
C4064	B5	C3	R1020	F2	A1	U3040A	C2	B2
C4068	B5	C3	R1020	F1	A1	U3040B	D3	B2
C5060	B5	C3	R1020	F4	A1	U3040C	C4	B2
C7060	B5	D3	R1030	F1	A2	U3040D	C1	B2
C7061	C1	D3	R2064	D4	B3	U4010A	A2	C1
			R3070	C5	B3	U4010B	A2	C1
CR2062	C4	B3	R3071	D5	B3	U4010C	A3	C1
CR2066	D4	B3	R4020	E3	C1	U4015A	A2	C1
CR4020	E4	C1	R4025	E4	C1	U4015B	A2	C1
CR4030	E3	C2	R4055	A5	C3	U4015C	A3	C1
CR4035	D3	C2	R4060	B5	C3	U4020A	A3	C1
CR4050	A5	C3	R4064	B5	C3	U4020B	A3	C1
CR4055	A4	C3	R5060	B5	C3	U4020C	A3	C1
CR7060	B5	D3	R5064	B5	C3	U4020D	A3	C1
			R5068	B5	C3	U4030B	A2	C2
J1010	F5	A2				U4035A	A2	C2
J1010	F1	A2	TP1	F4	A1	U4060	B5	C3
J1010	A4	A2	TP2	F3	A1			
J1010	F4	A2	TP3	F3	A1	VR4030	E5	C2
J3005	F4	B1	TP4	F4	A1	VR7060	A4	D3
J3005	E1	B1				VR7065	B5	D3

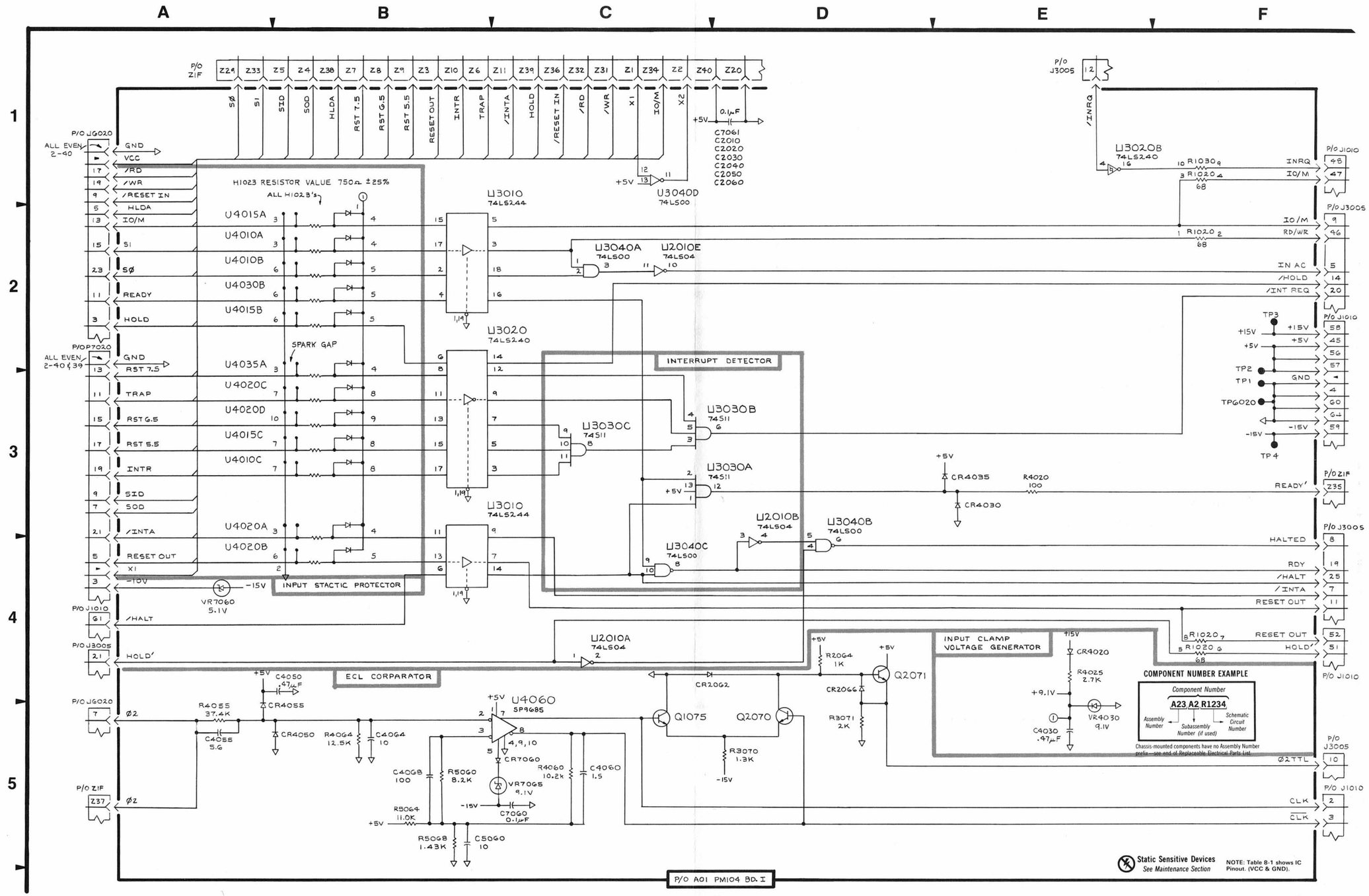
Partial A1 also shown on diagram 1A.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



PM104 INSTRUCTION

P/O A01 UPPER BOARD

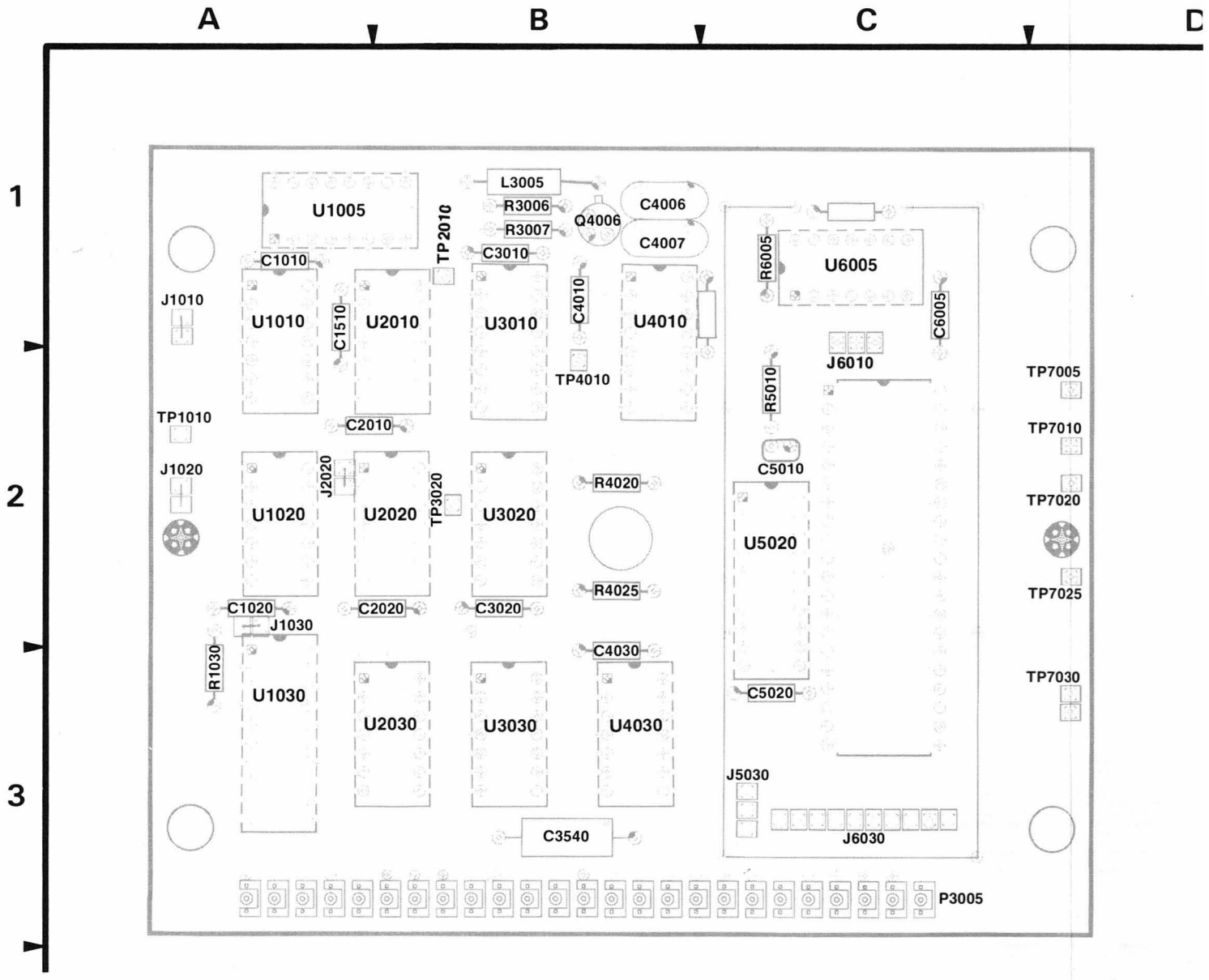


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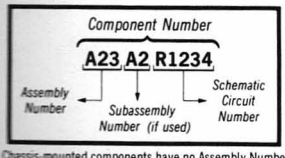
Figure 8-2. A02 Lower board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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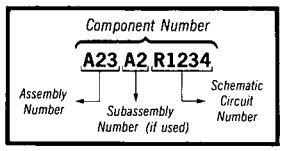
2 LOWER BOARD DIAGRAM 2

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1010	A2	A1	TP4010	A2	B2
C1020	A2	A2	TP7005	D1	D1
C1510	A2	A1	TP7010	E3	D2
C2010	A2	A2	TP7020	D2	D2
C2020	A2	B2	TP7025	D2	D2
C3010	A2	B1	TP7030	A2	D3
C3020	A2	B2			
C3540	A2	B3	U1005	D1	A1
C4006	A1	B1	U1010A	D3	A1
C4007	A1	B1	U1010B	D3	A1
C4010	A2	B1	U1020A	A4	A2
C4030	A2	B3	U1020B	B4	A2
C5010	F1	C2	U1030A	E4	A3
C5020	A2	C3	U1030B	C4	A3
C6005	A2	C1	U1030C	B5	A3
C6006	A2	C1	U1030D	E4	A3
			U1030E	E5	A3
J1010	D3	A1	U1030F	E5	A3
J1020	B4	A2	U1030G	C3	A3
J1030	B3	A2	U1030H	E5	A3
J2020	D4	A2	U2010B	B1	B1
J5030	B1	C3	U2020A	D4	B2
J6010	A1	C1	U2020B	C4	B2
J6030	F4	C3	U2030A	D5	B3
			U2030B	E5	B3
L3005	A1	B1	U2030D	D5	B3
			U2030D	B3	B3
P3005	A1	C3	U3010	C1	B1
P3005	F5	C3	U3020A	C5	B2
			U3020B	D5	B2
Q4006	B1	B1	U3030A	C5	B3
			U3030B	D4	B3
R1030	E4	A3	U3030B	C4	B3
R3006	B1	B1	U3030C	E4	B3
R3007	A1	B1	U4010	E1	B1
R4020	D4	B2	U4030A	E5	B3
R4025	E5	B2	U4030B	B4	B3
R5010	F1	C2	U5020H	B1	C2
R6005	E2	C1	U5020	E3	C2
			U6005A	E2	C1
TP1010	A2	A2	U6005B	E2	C1
TP2010	D1	B1	U6005C	F2	C1
TP3020	C3	B2	U6005D	C3	C1

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TEST OSCILLATOR

SELF TEST GENERATOR

WAIT STATE GENERATOR

INTERRUPT LATCH

INSTRUCTION FETCH CYCLE GENERATOR

J6010 NORM NC +5V TEST

R3007 3.3K Q4006 L3005 805μH C4007 560 C4006 560 R3006 13K -15V

U5020H 74LS244

U2010B 74LS74

J5030

P/O P3005

25 /HALT

TP7030-2 +5V C3540 47μF 0.1 C1010 C4010 C1020 C2010 C3020 C2020 C4030 C6005 C6006 C3010 C5020 C1510

15 GND TP7030-1

16 17 18 TP1010

13 -15V TP4010 -15V

U3010 74LS161 LD CLR ENP ENT RCO QD QC QB TADI TADØ

TP2010

U1005 74LS161 RCO QD QC QB ENP ENT LD CLR TAD5

TP7005 RESET OUT

U4010 IM5610 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 ALE ADD ADC ADB ADA

TAD4 TAD3 TAD2 TAD1 TADØ

C5010 22 pF R5010 10K

RESET OUT SØ S1 IO/M TAD6 RST6.5 TAD7 RST5.5 /INTA TA14 INTR TA15 TRAP HOLD RST7.5

U6005B 74LS00

R6005 1K

U6005A 74LS00 U6005C 74LS00

TP7025

TP7020

U1010A 74LS74 U1010B 74LS74

U6005D 74LS00

TEST JUMPER J1010

U5020 74LS244

TP7010

TADØ TAD1 TAD2 TAD3 TAD4 TAD5

TALE TREADY TCLK TADØ TA8 TAD1 TA9 TAD2 TA10 TAD3 TA11 TAD4 TA12 TAD5 TA13 +5V GND

SELF TEST

J6030

CHØ CH1 CH2 CH3 CH4 CH5 CH6 CH7 SIGNATURE ANAYSIS GND

P/O P3005

WAIT /INRQ HOLD IFC INACK /HALTED

19 RDY

4 ALE

10 Ø2TTL

20 /INT REQ

11 RESET OUT

7 /INTA

9 IO/M

5 IN AC

14 /HOLD

8 HALTED

U2030D 74LS00 U1030G 74LS240

TEST JUMPER J1030

U1020A 74LS74 U1020B 74LS74 U4030B 74S74

TEST JUMPER J1020

TP3020

U2020B 74LS74 U2020A 74LS74

TEST JUMPER J2020

U1030B 74LS240

U3030B 74LS12 R4020 1K +5V

U1030D 74LS240 U3030C 74LS12 U1030A 74LS240 R1030 1K +5V

U3020A 74LS74 U1030C 74LS240 U3030A 74LS12

U3020B 74LS74

U4030A 74S74

U2030D 74LS00 U2030A 74LS00 U1030F 74LS240

U2030B 74LS00 U1030H 74LS240

U1030E 74LS240

R4025 1K +5V

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234 (Assembly Number / Subassembly Number (if used) / Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

NOTE: Table 8-1 shows IC Pinout. (VCC & GND).

A02 PM104 BD. II

PM104 INSTRUCTION

A02 LOWER BOARD 2

PM104

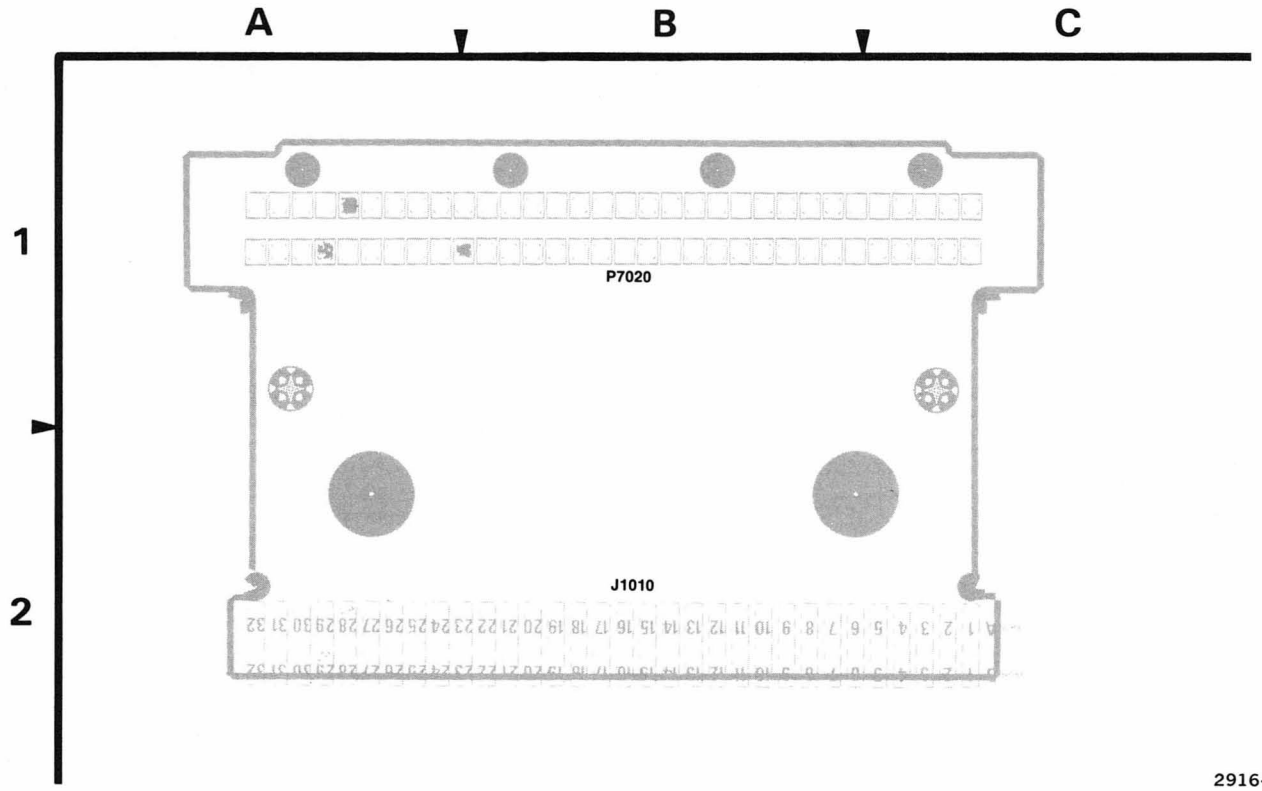
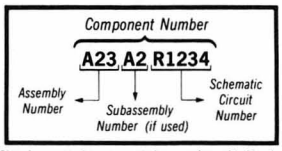


Figure 8-3. A03 Probe connector board component locations.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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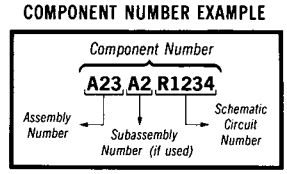
3 PROBE CONNECTOR BOARD DIAGRAM 3

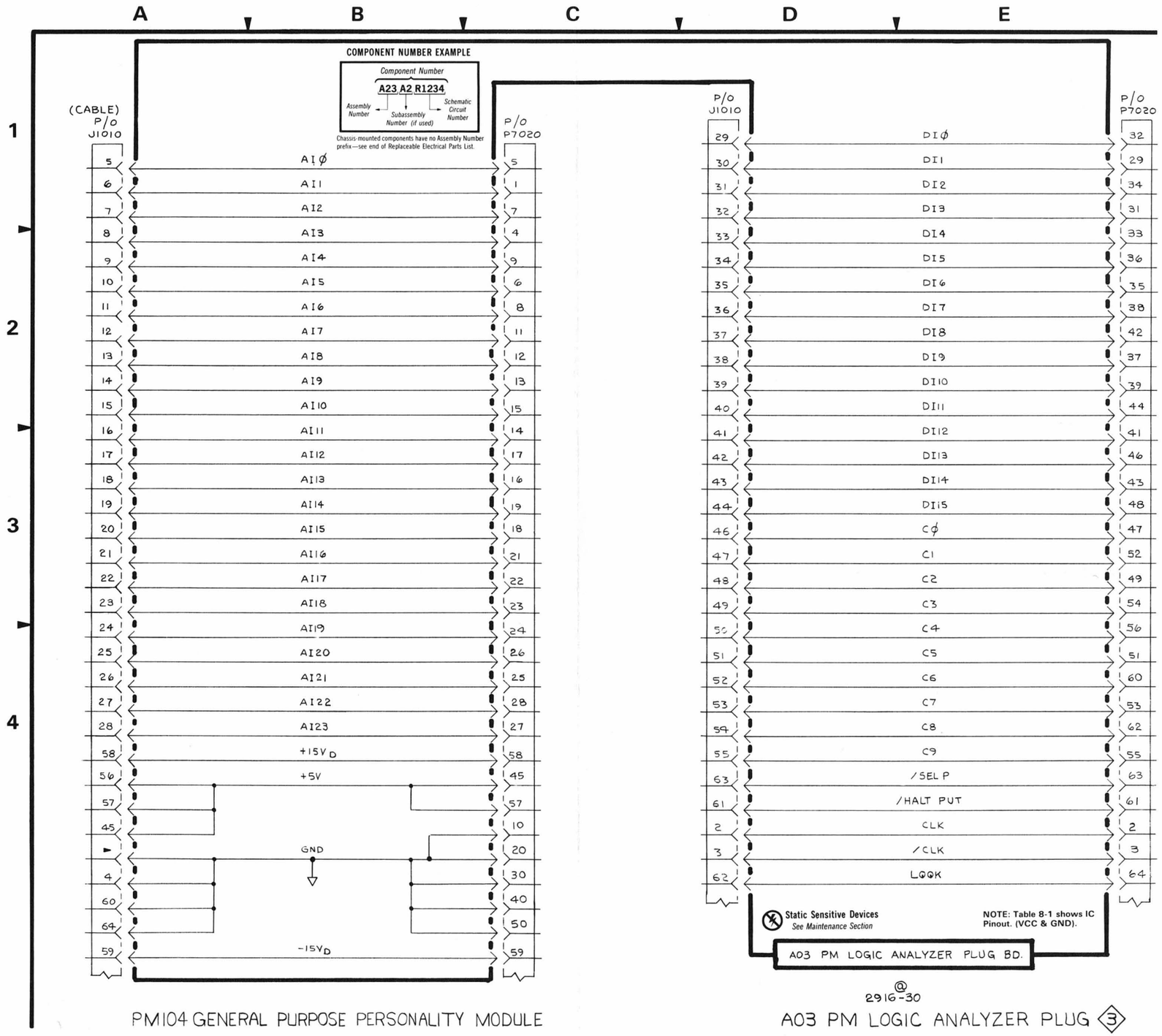
ASSEMBLY A3		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1010	D1	B2
J1010	A1	B2
P7020	E1	B1
P7020	C1	B1

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



PM104 GENERAL PURPOSE PERSONALITY MODULE

@ 2916-30

A03 PM LOGIC ANALYZER PLUG ③

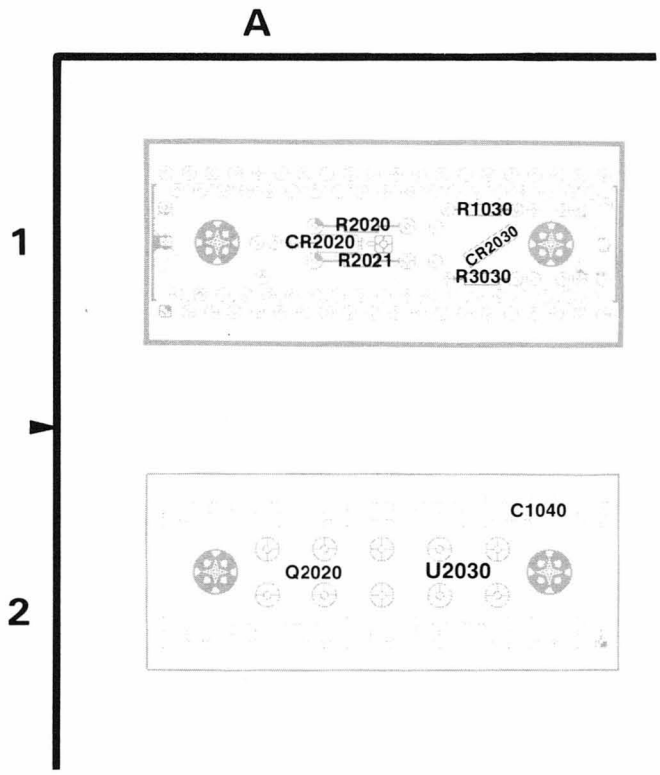


Figure 8-4. A04 PM104 probe plug board component locations.

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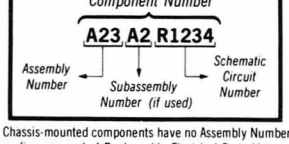
Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

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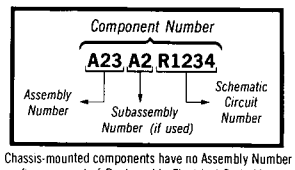
4 PM104 PROBE PLUG BOARD DIAGRAM 4

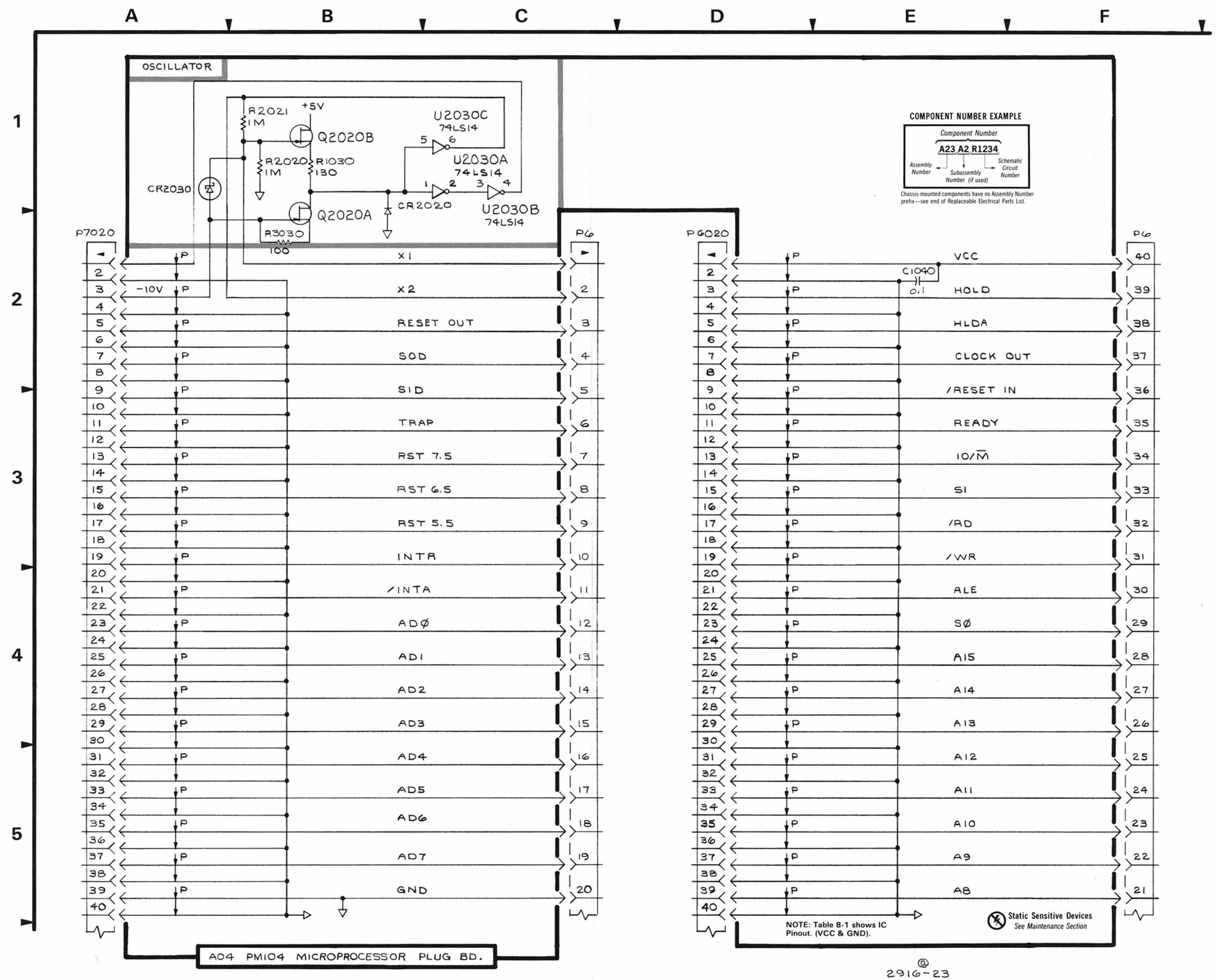
ASSEMBLY A4		
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1040	E2	A2
CR2020	B2	A1
CR2030	A1	B1
P6	C2	A1
P6	F2	A1
P6020	D2	A1
P7020	A2	A1
Q2020A	B2	A2
Q2020B	B1	A2
R1030	B1	A1
R2020	B1	A1
R2021	B1	A1
R3030	B2	A1
U2030A	C1	A2
U2030B	C1	A2
U2030C	C1	A2

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.



PM104 INSTRUCTION

@ 2916-23

A04 PM104 MICROPROCESSOR PLUG ◇4

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000AH	STANDARD PRESSED STEEL CO., UNBRAKO DIV.	8535 DICE ROAD	SANTA FE SPRINGS, CA 90670
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-3726-00			1		PLATE,IDENT:MKD 8085 MICROPROCESSOR	80009	334-3726-00
-2	380-0593-00			1		HSG HALF,CKT BD:TOP	80009	380-0593-00
						(ATTACHING PARTS)		
-3	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
						- - - * - - -		
-4	380-0594-00			1		HSG HALF,CKT BD:BOTTOM	80009	380-0594-00
						(ATTACHING PARTS)		
-5	211-0093-00			4		SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-6	210-0586-00			4		NUT,PL,ASSEM WA:4-40 X 0.25,STL CD PL	83385	OBD
						- - - * - - -		
-7	343-0836-00			4		CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-8	200-2415-00			1		DOOR,ACCESS:PLASTIC	80009	200-2415-00
	175-2680-00			1		CA ASSY,SP,ELEC:40,28 AWG,15.0 L	80009	175-2680-00
-9	386-3814-00			1		. PLATE,CONN BODY:	80009	386-3814-00
-10	352-0536-00			1		. HOLDER,CONTACT:40 PIN,NYLON	80009	352-0536-00
						(ATTACHING PARTS)		
-11	211-0102-00			2		. SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
						- - - * - - -		
-12	334-3754-00			1		. MARKER,IDENT:MKD P7020	80009	334-3754-00
-13	334-3753-00			1		. MARKER,IDENT:MKD P6020	80009	334-3753-00
-14	----- -----			1		. CKT BOARD ASSY:8085 PROBE(SEE A4 REPL)		
-15	131-2093-00			2		. . SKT,PL-IN ELEK:MICROCKT,20 CONT,LOW PF	23880	CSA-3200-208
-16	136-0252-01			6		. . CONTACT,ELEC:0.178 INCH LONG	00779	1-332095-2
-17	136-0252-07			14		. . SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-18	200-2429-00			1		. . CABLE NIP,ELEC:0.69 L X 3.6 W	80009	200-2429-00
	131-2443-00			1		CONN,RCPT,ELEC:CABLE,32/64 MALE	80009	131-2443-00
-19	334-3722-00			1		. PLATE,IDENT:MKD 6460 MICROPROCESSOR	80009	334-3722-00
-20	380-0591-00			1		. HSG HALF,CKT BD:TOP	80009	380-0591-00
						(ATTACHING PARTS)		
-21	211-0225-00			2		. SCR,CAP,SOC HD:4-40 X 0.312 INCH,STL	000AH	OBD
-22	211-0093-00			2		. SCR,CAP,SOC HD:4-40 X 0.75 INCH L,STL	000BK	OBD
-23	210-0551-00			4		. NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	83385	OBD
						- - - * - - -		
-24	380-0590-00			1		. HSG HALF,CKT BD:BOTTOM	80009	380-0590-00
-25	343-0836-00			2		. CLAMP,CABLE:3.72 L,ALUMINUM	80009	343-0836-00
-26	200-2412-00			2		. CABLE NIP,ELEC:3.45 L X 0.05 ID	80009	200-2412-00
-27	175-2683-00			1		. CA ASSY,SP,ELEC:64,28 AWG,48.0 L	80009	175-2683-00
-28	----- -----			1		. CKT BOARD ASSY:PROBE CONNECTOR(SEE A3 REPL)		
-29	131-0608-00			64		. . TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-30	361-0998-00			4		SPACER,CKT BD:0.245 ID X 0.38 OD	80009	361-0998-00
-31	----- -----			1		CKT BOARD ASSY:PM104(SEE A1 REPL)		
-32	131-0590-00			25		. CONTACT,ELEC:0.71 INCH LONG	22526	47351
-33	131-0993-00			1		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-34	136-0269-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-35	136-0537-00			1		. SOCKET,PLUG-IN:40 PIN,W/LOCKING LEVER	19613	240-0333-00-0602
-36	131-0608-00			112		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-37	136-0252-07			10		. SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-38	131-0787-00			40		. CONTACT,ELEC:0.64 INCH LONG	22526	47359
-39	136-0634-00			6		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-40	136-0578-00			1		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE	73803	C S9002-24
-41	----- -----			1		CKT BOARD ASSY:PM104(SEE A2 REPL)		
-42	136-0263-04			25		SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-43	136-0634-00			1		. SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
-44	136-0260-02			1		. SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CLE	71785	133-51-92-008
-45	131-0993-00			6		. BUS,CONDUCTOR:2 WIRE BLACK	00779	530153-2
-46	131-0608-00			34		. TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-47	136-0269-02			2		. SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP,LOW CLE	73803	CS9002-14
-48	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
-49	337-2722-00			1		. SHIELD,ELEC:ACCESS DOOR,BRASS	80009	337-2722-00

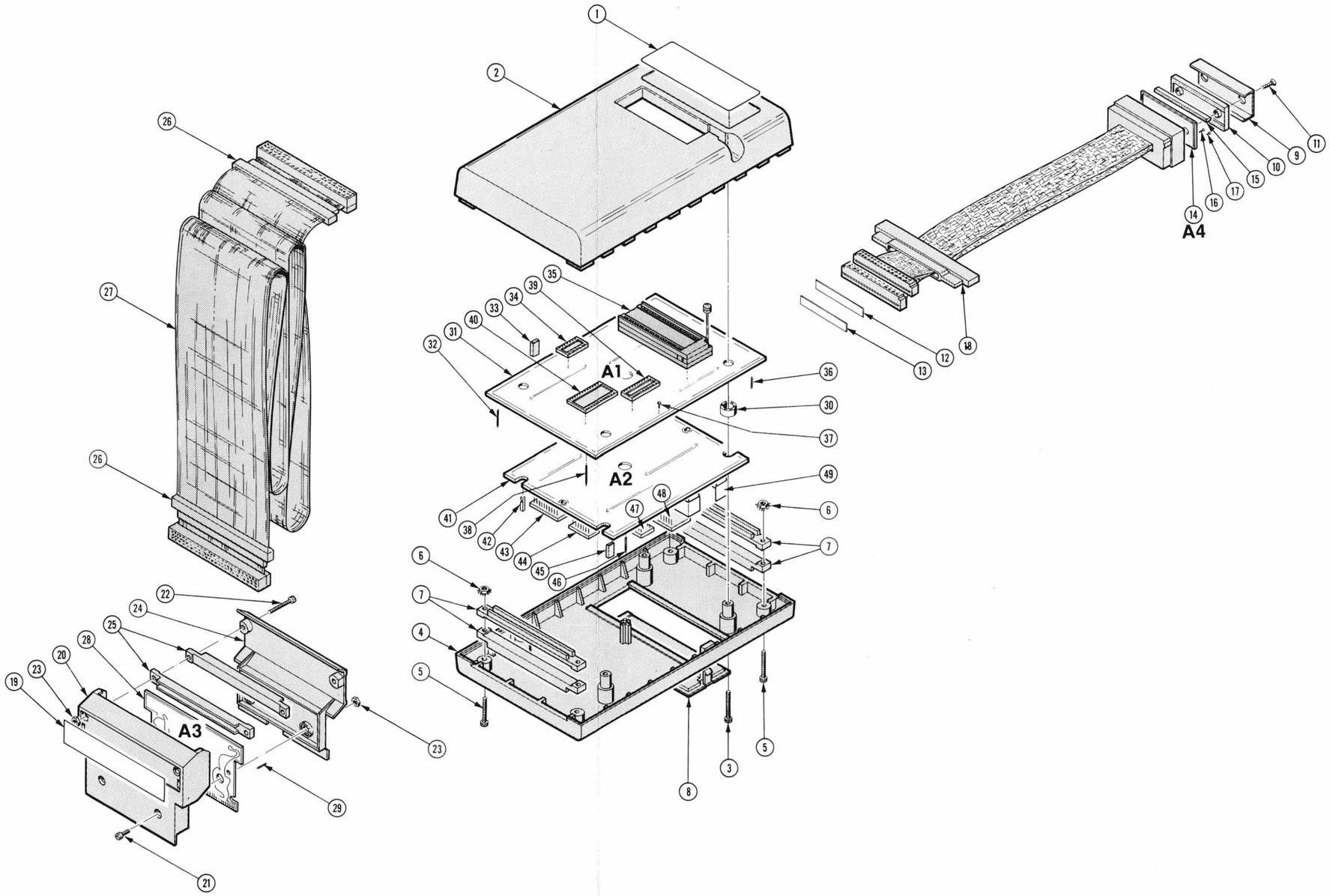


FIG. 1 EXPLODED

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
	070-2916-00			1		MANUAL,TECH:INSTR,010-6460-03,8085	80009	070-2916-00

APPENDIX A
PM 104 SIGNAL GLOSSARY

Introduction

The listings which follow describe each signal line within the PM 104 as it appears at each pin of every connector in the Personality Module. Some line titles appear more than once, and the active state and line definition may differ at one pin as compared to another because of the different purposes served by some signals at different locations within the Personality Module. For additional information, refer to Section 4, Theory of Operation.

1. Signals at J6020, interconnect from the Microprocessor Plug to PM 104 circuitry.

Pin No.	Signal	Definition
1	Vcc	Processor +5 V Supply from System Under Test.
3	HOLD	The Processor HOLD line. In active High level, this signal puts the processor in Hold condition and sends a /HALTED message to the 7D02.
5	HLDA	The Processor Hold Acknowledge. Not used by PM 104.
7	Ø2	The Clock Out signal from Processor Pin 37. An active High signal, used to Clock the System Under Test and synchronize the PM 104.
9	/RESET IN	The RESET signal from the S.U.T. to the Processor in the ZIF Socket. An active Low signal, not used by the PM 104.
11	READY	The READY signal from the S.U.T. to the Processor in the ZIF socket. An Active High signal whose low state causes the processor and the 7D02 to add Wait States.
13	IO/M	A control signal from the Processor used by the PM 104 to decode Processor status and Machine Cycle information. In High state, the indicated operation is to IO; in Low state, to Memory.
15	S1	Same as Pin 13.
17	/RD	/READ. An active Low signal from the Processor, not used by the PM 104.
19	/WR	/WRITE. An active low signal from the Processor, not used by the PM 104.
21	ALE	Address Latch Enable. The ALE signal from the Processor. An Active High signal used to synchronize PM 104 and 7D02 circuits. ALE latches address information from the multiplexed address/data bus used by the 8085.
23	SØ	Same as Pin 13.
25,27, 29,31, 33,35, 37,39	A8-A15	Address 8 through Address 15 information.

2. J7020, interconnect from Microprocessor Plug to PM 104 circuitry.

Pin No.	Signal	Definition
1	X1	Clock input signal from the Microprocessor Plug to the Processor in the ZIF socket.
3	X2	Used to supply negative voltage to the oscillator in the Microprocessor Plug.
5	RESET OUT	The RESET OUT signal from the Processor. Active High from the Processor resets the S.U.T. and the PM 104 State Machines.
7	SOD	Serial Out Data line from the Processor. Not used by the PM 104.
9	SID	Serial In Data line to the Processor. Not used by the PM 104.
11	TRAP	Interrupt Line to the Processor, Active High. Generates an Interrupt Request signal to the 7D02.

13	RST 7.5	Same as Pin 11
15	RST 6.5	Same as Pin 11
17	RST 5.5	Same as Pin 11
19	INTR	Same as Pin 11
21	/INTA	Interrupt Acknowledge from the Processor. Not used in the PM 104.
23,25, 27,29, 31,33, 35,37	ADØ-AD7	The multiplexed Address/Data bus to and from the Processor.

3. J3005, the Interboard connector between Upper and Lower Boards in the PM 104.

Pin No.	Signal	Definition
1	IFC	Instruction Fetch Cycle Signal, Active High. On Control Line C3.
2	/HALTED	Active Low when the READY line is pulled low, the /HALT line is pulled low, or the HOLD line is pulled high. /HALTED provides information for the "8085 STOPPED" message. On Control line C7.
3	WAIT	WAIT is Active High when the READY line is pulled low or /HALT is pulled low. Adds Wait States to the 7D02. Is on Control Line C9.
4	ALE	An Active High signal, used to synchronize the State Machines.
5	IN AC	A partially-decoded Active High control signal used to produce INACK and IFC.
6	INACK	Interrupt Acknowledge. An Active High signal during Interrupt Acknowledge Machine Cycles.
7	/INTA	An Active Low Interrupt Acknowledge Signal from the Processor.
10	Ø2TTL	The TTL Level Clock generated by Ø2.
11	RESET OUT	A RESET signal from the Processor, Active High.
12	/INRQ	This signal is Active Low when any Interrupt line is pulled high.
14	/HOLD	Active Low when the HOLD line goes high.
19	RDY	An Active High signal to the Wait State Generator and the /HALTED Generator when either READY or /HALT is pulled low.
20	/INT REQ	Active Low when any Interrupt line is High.
21	HOLD	Latched High when the HOLD line goes High, this signal indicates a HOLD request. It clears at the next ALE pulse.
25	/HALT	An Active Low signal, used only for testing purposes during manufacturing.

4. J1010, interconnection from the PM 104 to the 7D02.

Pin No.	Signal	Definition
2	CLK	The Processor Clock Out signal at ECL levels.
3	/CLK	The Pin 2 signal inverted.
5-20	AØ-A15	The 16 Address lines to the 7D02.
29-36	DØ-D7	The 8 Data lines to the 7D02.
46	RD/WR	In High state, a READ operation, and in Low State, a WRITE. This is Control Line CØ.
48	INRQ	When this line is High, the 7D02 is told there has been an Interrupt Request. Control Line C2.
49	IFC	An Active High line denoting an Instruction Fetch Cycle. This is Control Line C3.
50	INACK	This line is Active High during Interrupt Acknowledge cycles. Control Line C4.
51	HOLD	An Active High state informs the 7D02 there is a HOLD request. Control Line C5.
52	RESET OUT	This line is High during RESET operations. Control Line C6.
53	/HALTED	/HALTED is Low when the READY or /HALT lines go Low, or when HOLD goes High. It also supplies the "8085 STOPPED" information. Control Line C7.

54	/ALE	This line synchronizes the 7D02 State Clock Generator. It is Low during the ALE signal from the Processor. Control Line C8.
55	WAIT	Used to add Wait States to the 7D02, this line is High when READY or /HALT is Low. Control Line C9.
61	/HALT	An Active Low signal from the 7D02 to the Personality Module, used to Halt the Processor Under Test.
62	LOOK	A normally Low signal. In the High state, it is sent from the 7D02 to turn off the buffers in the Personality Module so that the bus can be addressed by the PROM.
63	/SEL P	Normally in the High state. When this signal goes low, it is sent from the 7D02 to the Personality Module to turn on the PROM and U2020 and read the PROM.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

REV B, JUN 1978

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MANUAL CHANGE INFORMATION

Date: 7-30-81 Change Reference: C3/781

Product: PM 104 PERSONALITY MODULE FOR 8085 MICROPRO Manual Part No.: 070-2916-00

DESCRIPTION

TEXT CHANGES

SECTION 6 MAINTENANCE AND TROUBLESHOOTING

Pages 6-16, 6-17 and 6-18

CHANGE TO:

A2U1010

Pin	Signature
1	03PP
2	CC34
3	F96U
4	CC34
5	71C5
6	FA81
8	03PP
9	C8HA
10	CC34
11	--
12	71C5
13	CC34

A2U1010 J1010 Removed

Pin	Signature
1	CC34
5	CC34
6	0000
8	0000
9	CC34
12	CC34

A2U1020

Pin	Signature
1	5U83
2	CC34
3	71C5
4	CC34
5	71C5
6	FA81
8	5U83
9	P4C7
10	03PP
11	--
12	71C5
13	CC34

A2U1020 J1010 Removed

Pin	Signature
1	0000
3	CC34
5	0000
6	CC34
8	0000
9	CC34
10	0000
12	0000

A2U1020 J1020 Removed

Pin	Signature
1	CC34
5	CC34
6	0000
8	0000
9	CC34
12	CC34

A2U1020 J1030 Removed

Pin	Signature
1	03PP
8	03PP
9	C8HA
10	CC34

DESCRIPTION

A2U1030

Pin	Signature
1	0000
2	253A
3	89FC
4	0001
5	C8HA
6	CF1A
7	CH81
8	84UU
9	2322
11	9816
12	3UFC
13	19UC
14	072P
15	03PP
16	CC35
17	32UU
18	9POP
19	0000

A2U1030 J1010 Removed

Pin	Signature
2	828C
5	CC34
7	P4F7
8	0086
9	0000
11	CC34
12	CCC2
13	5UU3
15	0000
18	39CU

A2U1030 J1020 Removed

Pin	Signature
2	59P1
7	P4F7
8	0086
12	CCC2
13	5UU3
18	P2H5

A2U1030 J1030 Removed

Pin	Signature
2	UP5U
8	5U9A
12	P4AP
18	456C

A2U1030 J2020 Removed

Pin	Signature
2	59P1
8	0086
12	CCC3
18	P2H5

A2U2020

Pin	Signature
1	CC35
2	9POP
3	F96U
4	CC34
5	5HC1
6	P685
8	--
9	84UU
10	CC35
11	5HC1
12	CC34
13	UA09

A2U2020 J1010 Removed

Pin	Signature
2	39CU
3	0000
5	0000
6	CC34
8	CCC2
9	0086
11	0000
13	2163

DESCRIPTION

A2U2020 J1020 Removed

Pin	Signature
2	P2H5
3	0000
5	0000
6	CC34
8	CCC2
9	0086
11	0000

A2U2020 J1030 Removed

Pin	Signature
2	456C
3	P759
5	CC62
6	0056
8	P4AP
9	5U9A
11	CC62

A2U2020 J2020 Removed

Pin	Signature
2	P2H5
5	C868
6	035F
8	CCC2
9	0086
11	0000

A2U2030

Pin	Signature
1	0C81
2	19UC
3	--
4	82AH
5	191F
6	32UU
8	0C81
9	191F
10	CH84
11	03PP
12	C8HA
13	P4C7

A2U2030 J1010 Removed

Pin	Signature
1	HH5P
3	5UU3
8	HH5P
11	0000
12	CC34
13	CC34

A2U2030 J1020 Removed

Pin	Signature
1	HH5P
3	5UU3
8	HH5P
10	66PF
13	CC34

A2U2030 J1030 Removed

Pin	Signature
13	C8HA

A2U2030 J2020 Removed

Pin	Signature
10	129H

A2U3010

Pin	Signature
1	CC34
2	--
3	--
4	--
5	--
6	--
7	CC34
9	CC34
10	CC34
11	5CP0
12	P5PH
13	725C
14	96PF
15	826P

DESCRIPTION

A2U3020

Pin	Signature
1	CC34
2	072P
3	F96U
4	CC34
5	3072
6	8C46
8	CH84
9	06C0
10	CC34
11	072P
12	8C46
13	6P2U

A2U3020 J1010 Removed

Pin	Signature
3	0000
5	0000
6	CC34
12	CC34
13	CC35

A2U3020 J1020 Removed

Pin	Signature
3	0000
5	0000
6	CC34
8	66PF
12	CC34
13	CC35

A2U3020 J1030 Removed

Pin	Signature
3	P759
5	60P5
6	HCH1
8	129H
12	HCH1

A2U3020 J2020 Removed

Pin	Signature
8	129H

A2U3030

Pin	Signature
1	71C5
2	3072
3	CC34
4	0001
5	0001
6	6P2U
8	253A
9	--
10	3UFC
11	UA09
12	6P2U
13	CC34

A2U3030 J1010 Removed

Pin	Signature
1	CC34
2	0000
6	CC35
8	828C
9	P4F7
10	CCC2
11	2163
12	CC35

A2U3030 J1020 Removed

Pin	Signature
2	0000
6	CC35
8	59P1
9	P4F7
10	CCC2
12	CC35

A2U3030 J1030 Removed

Pin	Signature
2	60P5
8	UN5U
10	P4AP

A2U303 J2020 Removed

Pin	Signature
8	59P1
10	CCC2

DESCRIPTION

A2U4010

Pin	Signature
1	C7F3
2	8P5A
3	191F
4	7P10
5	1875
6	072P
7	9P77
9	8PP5
10	P5PH
11	5CPO
12	7P25
13	85PA
14	77F7
15	0000

A2U4030

Pin	Signature
1	35H1
2	CC34
3	71C5
4	CC34
5	35H1
6	8PP5
8	725C
9	F96U
10	CC34
11	--
12	5U83
13	CC34

A2U4030 J1010 Removed

Pin	Signature
3	CC34
5	0000
6	CC34
8	CC34
9	0000
12	0000

A2U4030 J1020 Removed

8	CC34
9	0000
12	0000

A2U4030 J1030 Removed

Pin	Signature
8	5F6H
9	P759
12	03PP

A2U5020

Pin	Signature
1	0000
2	--
3	--
4	5CPO
5	P5PH
6	7P25
7	6PCP
8	85PA
9	77F7
11	77F7
12	85PA
13	6PCP
14	7P25
15	P5PH
16	5CPO
17	--
18	--
19	0000

A2U6005

Pin	Signature
1	9P77
2	71C5
3	UP29
4	072P
5	072P
6	CF1A
8	451H
9	UP29
10	UP29
11	F96U
12	725C
13	725C

DESCRIPTION

A2U6005 J1010 Removed

Pin	Signature
2	CC34
3	2543
8	9P77
9	2543
10	2543

TEST POINTS

TP	Signature
3020	F96U
7005	0001
7020	03PP
7025	71C5

J6030

Pin	Signature
1	0000
2	P5PH
3	P5PH
4	5CP0
5	5CP0
6	7P25
7	85PA
8	77F7

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MANUAL CHANGE INFORMATION

Date: 1-26-82 Change Reference: C5/182

Product: PM 104 PERSONALITY MODULE Manual Part No.: 070-2916-00

DESCRIPTION

TEXT CORRECTION

SECTION 5 PERFORMANCE VERIFICATION

page 5-5 Fig. 5-2

1 0-DELAY CLOCK BY 2

CHANGE TO:

1 0-DELAY CLOCK BY 0

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MANUAL CHANGE INFORMATION

Date: 9-23-81 Change Reference: C4/981

Product: PM 104 PERSONALITY MODULE FOR 8085 MICROPRO. Manual Part No.: 070-2916-00

DESCRIPTION

TEXT CHANGES

SECTION 3 SPECIFICATIONS

Table 3-1 page 3-2 Hysteresis under 8085 Probe

MOVE:

(V_T+-V_T-) from Performance Requirements to Supplemental Information

Ready Output Drive V_{OL}

MOVE:

.5 V I_O = -1 mA from Performance Requirements to Supplemental Information

Clock Input Characteristics

at Pin 37 of ZIF Socket

Input Impedance

CHANGE TO:

200 ns Min.

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MANUAL CHANGE INFORMATION

Date: 8-25-82 Change Reference: C6/882

Product: PM 104 PERSONALITY MODULE Manual Part No.: 070-2916-00

DESCRIPTION

PARTS LIST ADDITIONS

SECTION 7 REPLACEABLE ELECTRICAL PARTS

page 7-3

ADD:

CR2030	152-0322-00	SEMICOND DEVICE:SILCON,15V,HOT CARRIER