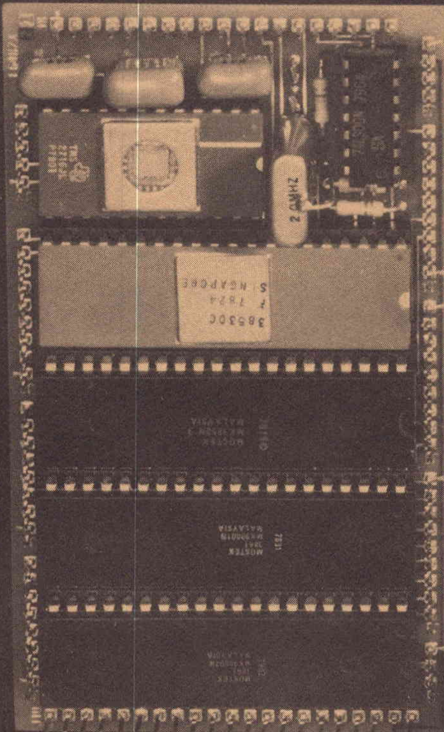
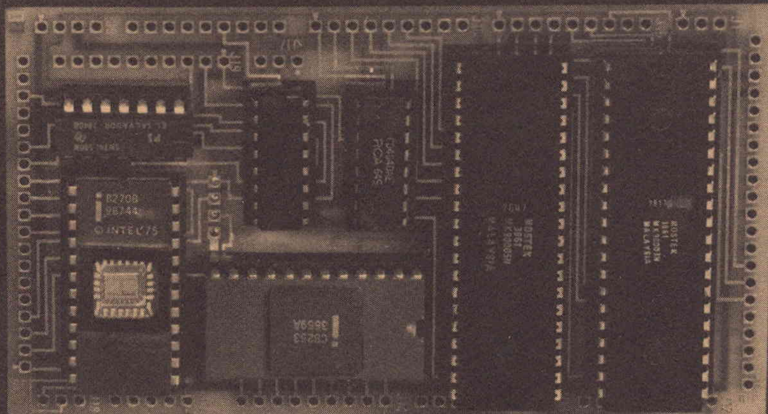
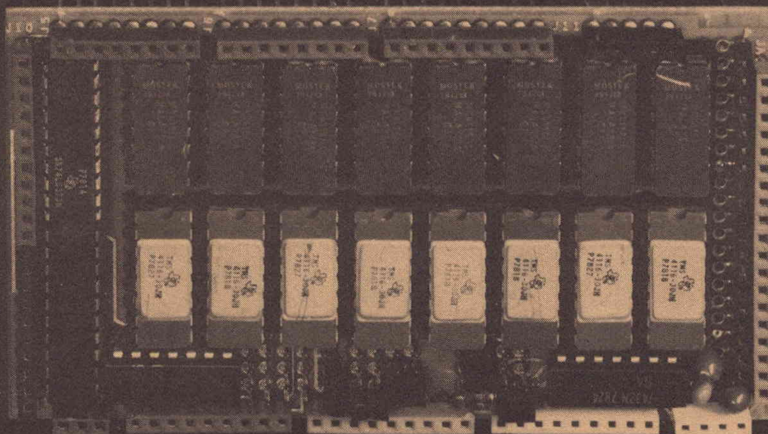
TEKTRONIX, INC. COMPANY CONFIDENTIAL MARCH, 1980

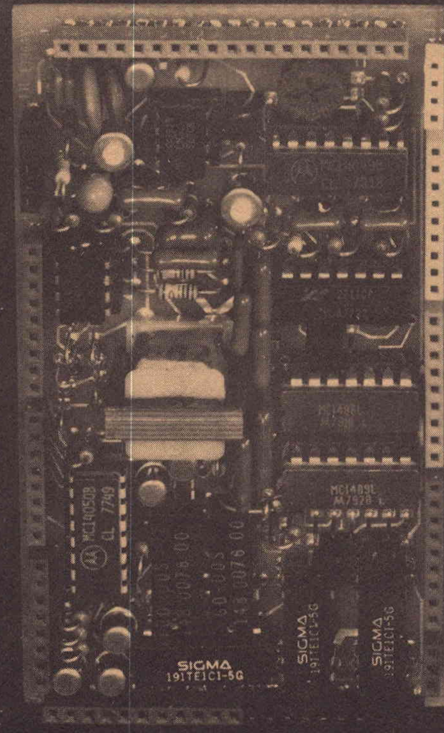
TECHNOLOGY report

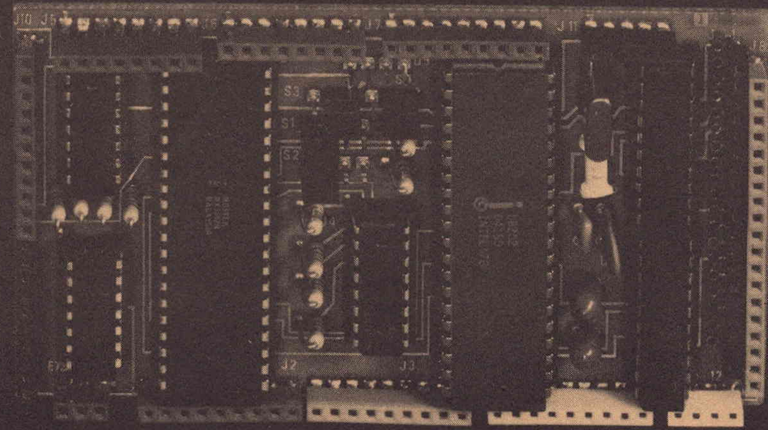
MORE PERFORMANCE IN SMALL MICROCONTROLLER BOARDS











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Why TR?

Technology Report serves two purposes. Long-range, it promotes the flow of technical information among the diverse segments of the Tektronix engineering and scientific community. Short-range, it publicizes current events (new services available and notice of achievements by members of the technical community). □

Contributing to TR

Do you have an article or paper to contribute or an announcement to make? Contact the editors on ext. 8929 (Merlo Road) or write to d.s. 53-077.

How long does it take to see an article appear in print? That is a function of many things (the completeness of the input, the review cycle and the timeliness of the content). But the *minimum* is six weeks for simple announcements and as much as 14 weeks for major technical articles.

The most important step for the contributor is to put the message on paper so that the editor will have something with which to work. Don't worry about organization, spelling, and grammar. The editors will take care of those when they put the article into shape for you. □

DECEMBER PAPERS AND PRESENTATIONS

While providing recognition for Tektronix engineers and scientists, the presentation of papers and the publication of papers and articles contribute to Tektronix' technological leadership image.

The table below is a list of papers published and presentations given during December 1979.

The Technical Communications Services' (TCS) Engineering Support group's charter is (1) to provide editorial and graphic assistance to Tektronix engineers and scientists for papers and articles presented or published outside Tektronix and (2) to obtain patent and confidentiality reviews as required.

If you plan to submit an abstract, outline, or manuscript to a conference committee or publication editor, take advantage of the services that TCS Engineering Support offers. Call Eleanor McElwee on ext. 8924 (Merlo Road). □

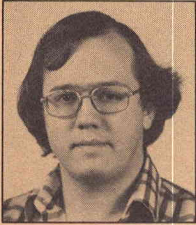
TITLE	AUTHOR	PUBLISHED	PRESENTED
MATERIALS RESEARCH			
□ "Microwave Devices Using YIG Spheres (and Thin-Film YIG)"	Dave Shores	—	Thin-Film Devices Conference
□ "Generalized Computations of the Gray-Body Shape Factor for Thermal Radiation From a Rectangular U-Channel"	Gordon Ellison	IEEE Transactions on Components, Hybrids, and Manufacturing Technology	—

For a copy of a paper or article listed here, photocopy this table, check the appropriate box, and mail to TCS, d.s. 53-077.

NAME ______________________________ D.S. ____________

ELECTRON DEVICES INSTRUMENTATION DEVELOPS

A NEW SERIES OF SMALL MICROCONTROLLER BOARDS



Jeff Eastwood is an engineer in Electron Devices Instrumentation. His association with Tektronix began as a member of the Tektronix-sponsored Explorer Post, Boy Scouts of America. Jeff is working on an E.E. degree at the University of Portland, continuing studies that he pursued at Cornell before joining Tektronix as an employee.

For more information about the new series of microcontroller boards, call Jeff on ext. 7989 (Beaverton).

Electron Devices Instrumentation designs and builds crt test sets for conventional and storage crts, and a variety of microprocessor-based control systems for crt production.

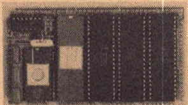
To accommodate demands for more performance in less space we have developed a series of five small (6 by 10.5 cm) microcontroller boards that we use in crt test sets in production applications. Readers can readily adapt these *general-purpose* boards for their purposes. These boards, for example, will fit in 5000, 7000, and TM500 series plug-ins. We can assist you by providing documentation and access to artwork.

HISTORY

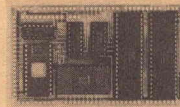
Up to about a year ago our group exclusively used large (12 by 20 cm or 12 by 27 cm) board-bucket boards based on F8 and 6800 microprocessor systems in crt test sets, crt aging and activation systems, crt process controllers, and data collection systems. The boards in these systems reside in a 72-conductor motherboard. A typical assembled central processor unit (CPU) board has on it a processor, four to six 8-bit i/o ports, and one or two serial ports. A typical RAM board has 4k, 8k or 16k bytes of static RAM. Other boards have EPROM, real-time clock circuitry, a/d and d/a converters, and various other circuits needed for controlling and detecting "real-world" events and processes. (Our real-world is the production environment.)

The large boards perform well and by no means are obsolete. However, advancing technology allows us to duplicate or enlarge capabilities in a smaller space.

THE FIRST TWO BOARDS



The first of these new boards, the **E6482X**, implements a microprocessor-based controller and was developed by Tom Brandt, T&D/CPI Evaluation. This controller is designed around the F8 CPU, a memory interface chip, two peripheral input-output (PIO) chips, and either a 1k or 2k byte EPROM. With these five chips, you can have as many as six 8-bit i/o ports, three vectored interrupts, three timers, and 2k of nonvolatile memory all on one small 6 by 10.5 cm board. Replacing one of the PIO chips with a special ROM i/o chip provides a 300- or 110-baud serial port and a powerful system monitor and debugging tool.



A companion board, the **E6505X**, also designed by Tom Brandt, adds four 8-bit i/o ports, two timers, and two vectored interrupts, 1k or 2k of EPROM, and a special timer/counter chip, the Intel 8253.

These small, low-power-consuming boards are plug-in modules in the P944 Test Set and an Aging Activation System which our group developed. Power supply specifications for the E6482X are 300 mA at 5V, 160 mA at 12V, 50 mA at -5V; for the E6505X they are 300 mA at 5V, 100 mA at 12V, 50 mA at -5V. All of these voltage and currents are maximum ratings.

All these microcontroller boards, including those described in the next section, simply plug in to a set of square pins on the system board that they are to control. They require no motherboard. There is a bus of sorts: a set of standard signals (address, data, all of the i/o ports) around the perimeter of each microcontroller board. These design features enable the designer to stack the boards vertically, saving space.

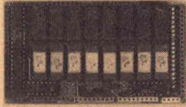
THREE ADDITIONAL BOARDS

After completing the two microprocessor-based controller boards more than a year ago, we developed three more small boards.

The first, the **E7364XA**, is a 300-baud, *originate-mode modem* with phone-line interface and auto-pulse dialing capability. This modem, used in a floppy-disc uploader, is based on a design in the **Exar Application Data Book.** Adding auto-pulse dialing and serial RS-232/TTL signal circuitry enables the Exar design to function as a floppy-disc uploader for use with the Scientific Computer Center's Cyber 175. RS-232/TTL-level signal switching circuitry allows communication between a terminal and the Cyber, an external processor and a terminal, or an external processor and the Cyber.

Continued on page 4

Although part of the small F8 controller board set, the E7364XA originate-mode modem is processor independent. Our F8-based board, the E6482X, connects to the 7364XA modem only through i/o ports and the serial RS-232/TTL lines. Designed for 300-baud, originate-mode operation, changing a few component values on the EE7364 allows answer-mode operation and operation at different baud rates.



Two of the boards in this series provide dynamic-RAM capability. One board, the **E7370X,** has on it 32k bytes of dynamic RAM using 4116-type RAM chips. This board may be addressed as two separate 16k blocks. The E7370X provides a board-disable function so that up to eight boards can be used in one 65k byte address space.

The second, a companion board to the E7370, is the **E7374X** dynamic-RAM controller based on the Intel 8202 dynamic-refresh controller chip. Surprisingly, this board is the least complex of any board in this series. By using the 8202, the designer is relieved of the design restraints generally associated with dynamic RAM (complex timing and critical rise and fall times.)

The basic circuitry consists of the 8202 and two 8-bit buffers. The remaining four chips on the board support (1) the 3852 dynamic-memory interface (DMI) chip (part of the F8 chip set) and (2) addressing. By removing the DMI and changing some straps on the board, this board can be processor independent. The 8202 dynamic-RAM controller chip is very flexible and easy to design with; therefore, using this dynamic-RAM board with any other processor should be very straightforward.

FUTURE DEVELOPMENTS

Although the five boards form the basis for a very capable microcontroller system, the future will probably require different capabilities. Now, we are using only 4k bytes of EPROM because that's all the boards will hold. Therefore, a 24k EPROM board is a future candidate for design because a designer can put up to 24k bytes on a board this size.

Our group is considering the use of the 6801 microprocessor. The 6801, with its on-board i/o ports, ACIA, and timer, could be very useful in the applications our group specializes in. We could easily install the 6801 and one or two peripheral interface adapters on one of our small boards to provide the same sort of capabilities as our F8 controller board.

Many circuits that in the past took several boards and hundreds of small-scale integration and medium-scale integration IC's can now be implemented on these small boards. Possibilities include hardware math (using the AMI 9511 or 9512, for example), or floppy-disc, printer, or video controllers. □

DESIGNER	BOARD	DESCRIPTION
Tom Brandt ext. 3287 Wilsonville	E6482X Microprocessor	F8 microprocessor. Six 8-bit i/o ports or five parallel and one serial terminal port. 1k or 2k of EPROM, three timers, three vectored interrupts.
Tom Brandt	E6505X Auxiliary memory, i/o timer, counter	Augments E6482X with four more 8-bit i/o ports, two timers and two vectored interrupts for the F8. Also 1k or 2k additional EPROM and a counter/timer chip (Intel 8253).
Jeff Eastwood ext. 7989 Beaverton	E7364X Modem/pulse dialer	300-baud originate-mode modem. Parameters may be altered with a few components. RS-232 or TTL levels. Processor independent.
Jeff Eastwood	E7370X 32k dynamic RAM	Addressable as two 16k blocks. Board disable for bank switching. Needs external refresh.
Jeff Eastwood	E7374X Dynamic-RAM controller	Uses Intel 8202 dynamic-RAM refresh controller chip. Can refresh 16k or 4k RAMs. Processor independent.

Table 1. Electron Devices Instrumentation developed a series of small microcontroller boards (described above) to meet requirements for higher performance in a smaller space in CRT production instrumentation.

VLSI PRESENTS TESTING DILEMMA

Doug Smith was a member of the CAD Development group at the time he wrote this article. Before working for Tektronix, Doug worked for Singer Business Machines and AMI Semiconductors. Doug obtained a B.S. degree in physics from Reading University in England.

Doug based the following article on a presentation he made at Forum 16, one of a series of forums sponsored by the Engineering Activities Council to promote the communication of engineers' views about new technology to Tektronix management.

For more information about testing VLSI *(very large-scale integration) circuits, call Ron Bohlman on ext. 221 (Town Center).*

INTRODUCTION

Since the introduction of LSI in the early 1960's, complexity (the number of gates per chip) has doubled every two years. Figure 1 illustrates this increased complexity. In figure 1, landmark LSI devices appear on the curve, based on their probable gate count (manufacturers of commercial LSI are not always inclined to release this information).

This growth in functional complexity has been a boon to the logic design engineer and produced the microprocessor revolution; however, as with all growth situations, there have been growing pains, the most notable of which has been the increased difficulty in testing more complex LSI. For example, the inability to test VLSI (a device with more than 50,000 gates) functions seriously limits its development. This article describes the state of the testing art, and suggests some ways to avoid the testing dilemma, a situation in which the most complex devices are untestable without advances in testing techniques.

WHAT IS LSI/VLSI TESTING? WHAT ARE THE PROBLEMS?

Testing is the process of verifying a component against its specification. This corresponds closely to the old military criteria "form, fit, and function." Form and fit are primary characteristics (such as physical characteristics and power supply drain) and are easy to verify with existing test equipment. A major problem arises in verifying that the device will perform its designed function, that is, when we test the device functionally.

In **functional testing,** the tester presents digital words, previously stored within the tester, at high speed to the inputs of the device under test. The tester compares words appearing at the device outputs against expected output words, also previously stored in the tester. Refer to figure 2. Any unexpected data received from the device indicates the device is suspect. The combination of an input word and an output word is a **test vector.**

There are three main concerns in functional testing:

- How to generate the original vectors.
- How many vectors are required?
- What is the fastest clock that can be applied to the test vectors?

Let's examine these three areas in more detail.

VECTOR GENERATION

Testers usually generate test vectors by simulating (modeling) the device to be tested. For very simple devices, test designers can perform this conceptually and then enter the test vectors manually into a mass-storage device. Designers base the vectors on their understanding (modeling) of the device to be tested.

This method is usable for most random-logic devices having fewer than 2000 gates, such as the 4040 microprocessor. The method's usefulness rapidly diminishes with increased complexity. Consider the problem of generating and entering by hand 20,000 error-free bits. This would correspond to 1000 vectors, 20-bits wide, possibly enough for the 4040 device.

The most common test-vector generation method is computer simulation. In this method, a computer constructs a model of the

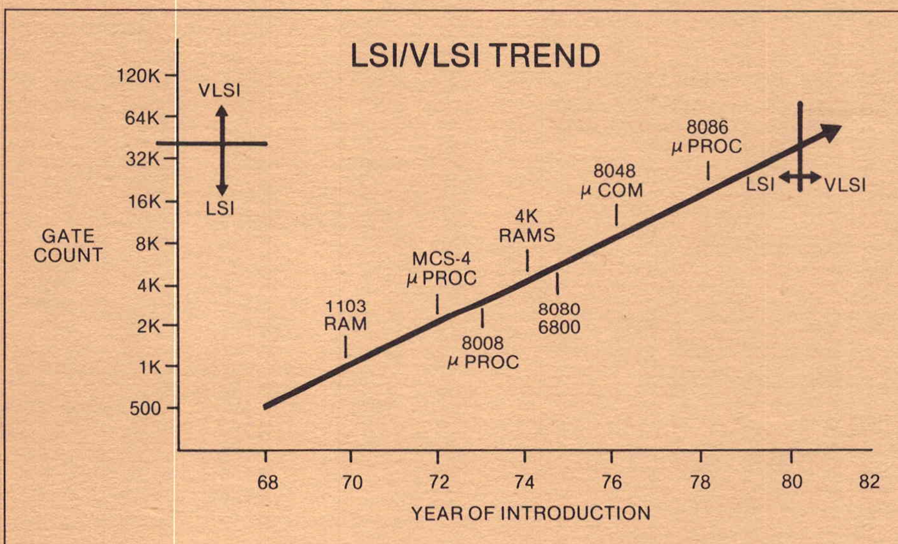


Figure 1. In the last ten years, LSI complexity has doubled every two years.

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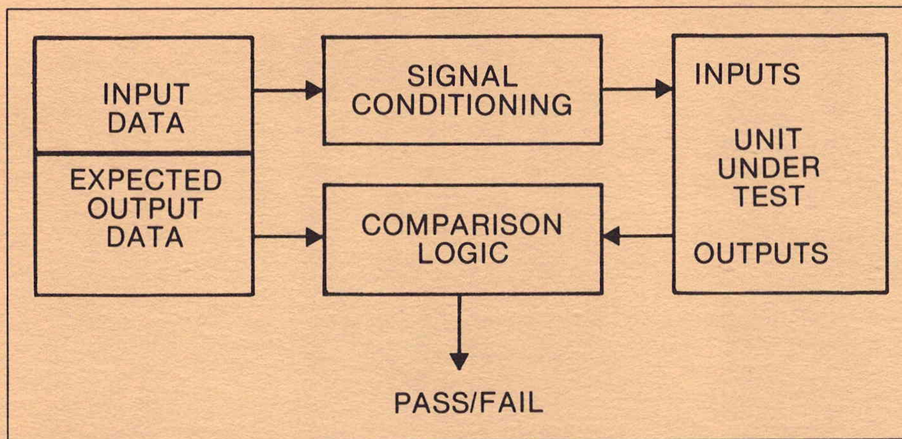

Figure 2. In functional testing, the tester presents digital words, previously stored within the tester, at high speed to the inputs of the device under test. The tester compares words appearing at the device outputs against expected output words, also previously stored in the tester.

device; then software exercises the model to generate the needed test vectors. This method, although significantly better than manual generation, has problems too.

HOW MANY VECTORS ARE NEEDED?

Using a simulator model that checks that no node on a given gate is either stuck at logic-one or logic-zero, we find that the number of vectors that a tester requires to test a given function increases exponentially with the gate count of the device. Figure 3 relates the amount of computer time needed to generate test vectors to the number of gates on the device.

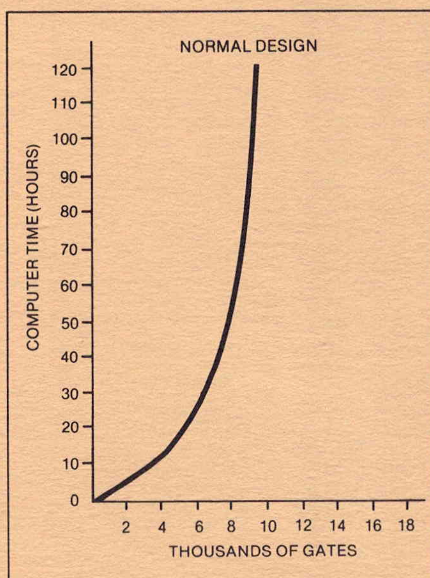

Figure 3. Based on data provided by Sperry-Univac Co., this graph relates the amount of computer time needed to generate test vectors to the number of gates on the device.

Standard "stuck 1/0" simulators become unusable around the 10,000-gate level of complexity, and are probably useless above 20,000 gates, the level of the Intel 8086.

Even if we could build a simulator that is fast enough, we also have to face the problem that no test system is available that can handle the billions of test vectors that VLSI devices require. Furthermore, if such a test system were available, it would not be fast enough for manufacturing test time limits.

HOW FAST SHOULD VECTORS BE PRESENTED?

Over the past ten years, the increase in complexity of LSI devices has gone hand-in-hand with other performance improvements, especially operating speed. Early devices trundled along at around 500kHz, while devices now operate at nearly 30MHz. Current trends indicate that clock and data rates greater than 50MHz will be common by 1985. Increases in speed and the number of vectors required are the two major problems in functional testing today.

WHAT CAN BE DONE?

There are two courses of action manufacturers can take if VLSI development is not to be slowed down by the testing dilemma:

- Reduce the vector count required by technique and design improvements.
- Increase the testers' speed and vector handling capabilities.

Economic constraints will probably cause manufacturers to follow both paths. Let's examine several ways electronic manufacturers might reduce the number of vectors required.

REDUCING TEST VECTOR COUNT

One method of reducing the number of test vectors consists of first partitioning the unit into several easily simulated subunits, testing each subunit, and then manually melding the resultant test vectors into the total test package. The method works, but it is comparable to assuming that a given board or system will work if all of its unconnected subunits work. It ignores the interactions of the subfunctions, and it's really only an interim patch.

A key approach to minimizing vector count is to design testability into the product. In fact, for VLSI, testability and vector count are practically synonymous. Incorporating testability into design is already occurring in the semiconductor industry. Both the 68000 and the Z8000 microprocessors include self-test circuitry. Tektronix should strongly encourage this trend, both to keep our suppliers honest and to greatly ease our test burden.

Nevertheless, there is no such thing as a free lunch. To include testability into VLSI will, inevitably, increase chip size and degrade performance. Tektronix designers should examine each new Tektronix VLSI design and identify the tradeoffs between chip size and testability. Realize, however, that a VLSI device that cannot be tested cannot be manufactured.

Features we can easily implement are:

- reset circuitry that places the device into a known state with the minimum number of steps,
- access to intermediate test points whenever possible, and
- the ability to break logical feedback loops.

This list is not inclusive, but suggests the types of techniques available.

The testing community has recently shown much interest in **scan/set design.** In scan/set, a shift register is part of the active circuitry; each of the elements of the shift register connects in a master/slave relationship to each of the flip-flops in the device. In this

Continued on page 7

WHICH INDUSTRY COMMITTEES HAVE TEKTRONIX REPRESENTATION?

Al Zimmerman, Digital Products Coordination manager, believes it is important to identify which industry efforts have Tektronix people involved. Therefore, **Technology Report** is publishing Al's list as a pump primer.

If you can contribute to the list, send your inputs to Art Andersen, delivery station 53-077. Please give organization name, the committee name, its function, its Tektronix representatives, and their positions. **Technology Report** will publish accordingly an updated list for those who could benefit from the work of these committees, or who could potentially offer inputs, or who would want to be involved in or know about the work of these committees. □

PARTIAL LIST OF TEK'S INVOLVEMENT IN INDUSTRY-WIDE TECHNICAL COMMITTEES

IEEE Technical Committee on Automated Instrumentation

- Robert Chew, member, ext. 5626 (Beaverton), 50-383

IEEE Computer Society Test Technology Committee

- Harley Perkins, newsletter editor, ext. 6186 (Beaverton), 58-134
- Steve Pataki, chairperson, Subcommittee on Digital Test, ext. 6073 (Beaverton), 58-299

International Purdue Workshop

- Maris Graube, chairperson, TC5 Interface Committee, ext. 6234 (Beaverton), 50-454
- Maris Graube, chairperson, Interface Committee (American), ext. 6234 (Beaverton), 50-454
- Maris Graube, chairperson, SP72 Advisory Committee to IEC-WG6 (American), ext. 6234 (Beaverton), 50-454

IEC SG65/WG6 Subcommittee on Physical Data Transmission

- Maris Graube, chairperson, ext. 6234 (Beaverton), 50-454

IEEE Computer Society Committee for Local Network Standards

- Maris Graube, chairperson, ext. 6234 (Beaverton), 50-454

Instrument Society of America, GPIB Committee

- Maris Graube, member, ext. 6234 (Beaverton), 50-454

IEEE Instrument Society, GPIB Committee

- Maris Graube, member, ext. 6234 (Beaverton), 50-454

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way, the tester can either serially set (write) or serially scan (read) each circuit of a unit.

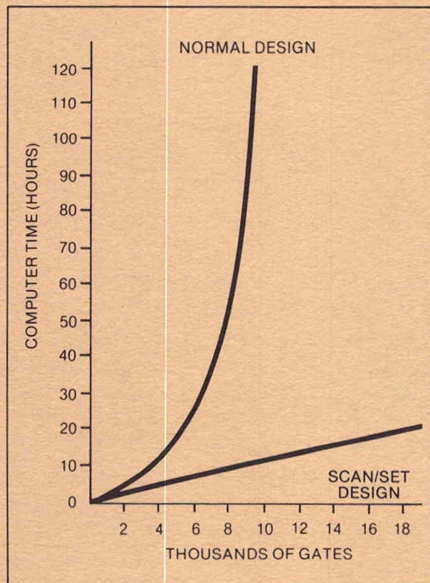


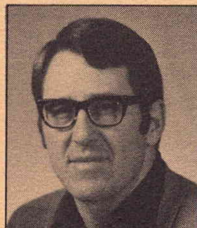
Figure 4. Using the scan/set VLSI design technique reduces design time from an exponential to a linear function.

Referring to figure 4, note that using scan/set design reduces an exponentially increasing function to a linear function. For medium-scale integration functions, scan/set reduces performance up to 20%, whereas for LSI/VLSI designs the reduction is up to 5%. This is because pin-count rather than number of logic gates generally limits highly integrated devices. I am not advocating that we immediately endorse scan/set for ourselves and our vendors, merely indicating what we can achieve when testability is a design criterion.

CONCLUSION

Testability will greatly impact VLSI applications at Tektronix and the test equipment we need to manufacture and service our products. We must design for testability, and we must carefully evaluate the tradeoffs involved. □

CAD DEVELOPMENT INTEGRATES CAD INTO TESTING ENVIRONMENT



Ron Bohlman has been with Tektronix for eight years. Before coming to Tektronix, Ron worked for Sandia Labs and Univac. His educational background includes an MS in math from the University of Oregon and an MSEE from the University of New Mexico.

Besides being a member of the Engineering Activities Council since January 1979, Ron manages CAD Development, a group whose charter is to develop design aids for Tektronix engineers and engineering support people.

For more information about CAD (computer-aided design) testing, call Ron on ext. 221 (Town Center).

The following article is based on a presentation that Ron made at Forum 16 in November 1979. The Engineering Activities Council sponsors forums to promote the communication of engineers' views of new technology to Tektronix management.

CAD and *testing* have been buzz words in the electronics industry for many years. However, only in the past two years have discussions of integrating CAD tools into the testing environment become significant. Before examining the integration of CAD with testing, let's look at a few basic CAD tool and systems concepts.

AUTOMATED ROUTER

The primary function of an automated router system is to place circuit components on an etched circuit board (ecb) and route the circuit paths on the ecb to connect the appropriate component pins together. This is the central ecb layout problem.

Routers for IC's also exist that have logical cells analogous to discrete components. The basic methodology of placing components and routing circuit paths consists of using algorithms implemented on a computer (usually a large mainframe system). Inputs to an automated router include circuit connect information, component information (physical and logical), board dimensions, and board parameters. Outputs include photoplotter tapes, drill tapes, check plots, and computer listings.

Figure 1 is a demultiplexer-circuit schematic. From this schematic the designer laid out the circuit on a 2-inch by 2-inch board with small-scale integration (SSI) components. Figure 2 shows the input file for this circuit board. (The designer used PIRATE, a set of automated router programs which reside on the Scientific Computer Center's Cyber 175 computer system.) Note that the input file contains component information such as "DIP 14, 3-in nand, inverter," and circuit path names such as "SDI, SELECTA-, 2YI." Figure 3 presents graphic outputs (check plot from Calcomp, an electromechanical plotter, and filmwork from the Gerber system, an in-house photoplotter system).

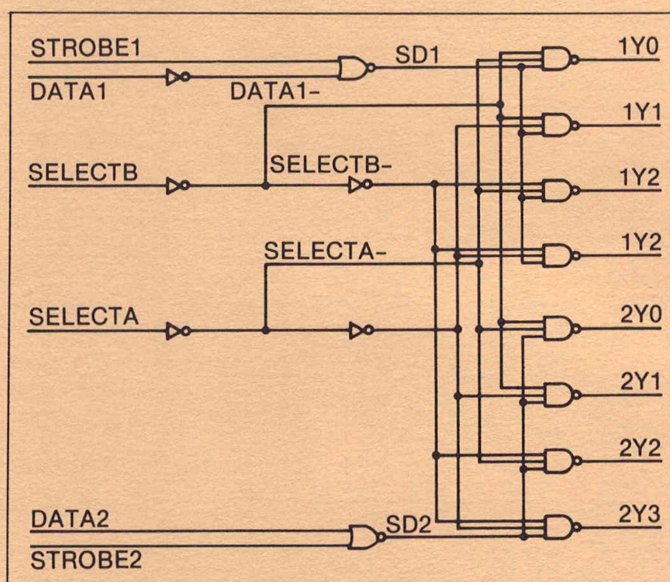


Figure 1. This schematic represents a demultiplexer circuit for which a designer created a data file for input to PIRATE, a set of automated router programs residing on the Scientific Computer Center's Cyber 175 computer system.

CIRCUIT SIMULATION

Tektronix designers have used circuit simulation for several years. Computer programs like SPICE, COMPACT, and GLUMP are well known component-level simulators in which circuit designers can model devices such as bjt's, MOSFET's, resistors, capacitors, and transmission lines.

The next level of simulation is **logic simulation** where gate-level primitives (AND, OR, inverter) are the building blocks of a circuit description. This step upward in generality nets larger circuit descriptions and simulation but with the loss of timing information (rise times, overshoots, and ringing).

Several logic simulators have been used at Tektronix. CAD Development obtained the present logic simulator from a Sandia Laboratories computer program, SALOGS, and

Continued on page 10

```
$ PIRATE INPUT FILE, DESCRIBES A SMALL BOARD WHICH IMPLEMENTS
$ A 74LS155 DEMULTIPLEXER.
GRIDSIZE = 50
SIZEX = 2000
SIZEY = 2000
REFX = 0
REFY = 0
TITLE = PHILTEST

DOLLY = DIP14,780,400,14
 -300,150,-62,39 / -200,150,62,39 / -100,150,62,39
   0 ,150,62,39 /  100,150,62,39 /  200,150,62,39
  300,150,62,39 / 300,-150,62,39 /  200,-150,62,39
  100,-150,62,39 / 0, -150,62,39 /  -100,-150,62,39
 -200,-150,62,39 / -300,-150,62,39

$ 74LS10 IS A TRIPLE 3-IN NAND.
PACKTYPE = 74LS10,3,LS10,LS10,LS10
 14, I*IN,1 = I*IN,1 = I*IN,2 = I*IN,2 = I*IN,2 $ 1 TO 5
  O*OUT,2 = I*GND,0 = O*OUT,3 = I*IN,3 = I*IN,3 $ 6 TO 10
  I*IN,3 = O*OUT,1 = I*IN,1 = I*VCC,0

$ 74LS04 IS SIXTUPLE INVERTER
PACKTYPE = 74LS04,6,LS04,LS04,LS04,LS04,LS04,LS04
 14, I*IN,1 = O*OUT,1 = I*IN,2 = O*OUT,2 = I*IN,3  $1 TO 5
   O*OUT,3 = I*GND,0 = O*OUT,4 = I*IN,4 = O*OUT,5  $ 6 10
   I*IN,5 = O*OUT,6 = I*IN,6 = I*VCC,0             $ 11 TO 14

USEPACK=74LS04,DIP14
 *VCC=VCC
 *GND=GND
USEPACK=74LS10,DIP14
 *VCC=VCC
 *GND=GND
GATE = LS04
 *IN = DATA1
 *OUT = DATA1-
GATE = LS04
 *IN = SELECTB
 *OUT = SELECTB-

$ LS10'S ARE OUTPUT NAND'S
GATE = LS10
 *IN = SELECTB-,SELECTA-,SD1
 *OUT = 1Y0
GATE = LS10
 *IN = SELECTB-,SELECTA,SD1
 *OUT = 1Y1
GATE = LS10
 *IN = SELECTB,SELECTA-,SD1
 *OUT = 1Y2
GATE = LS10
 *IN = SELECTB,SELECTA,SD1
 *OUT = 1Y3
GATE = LS10
 *IN = SELECTB-,SELECTA-,SD2
 *OUT = 2Y0
GATE = LS10
 *IN = SELECTB-,SELECTA,SD2
 *OUT = 2Y1

END
```

Figure 2. This is the input data file for the schematic shown in figure 1.

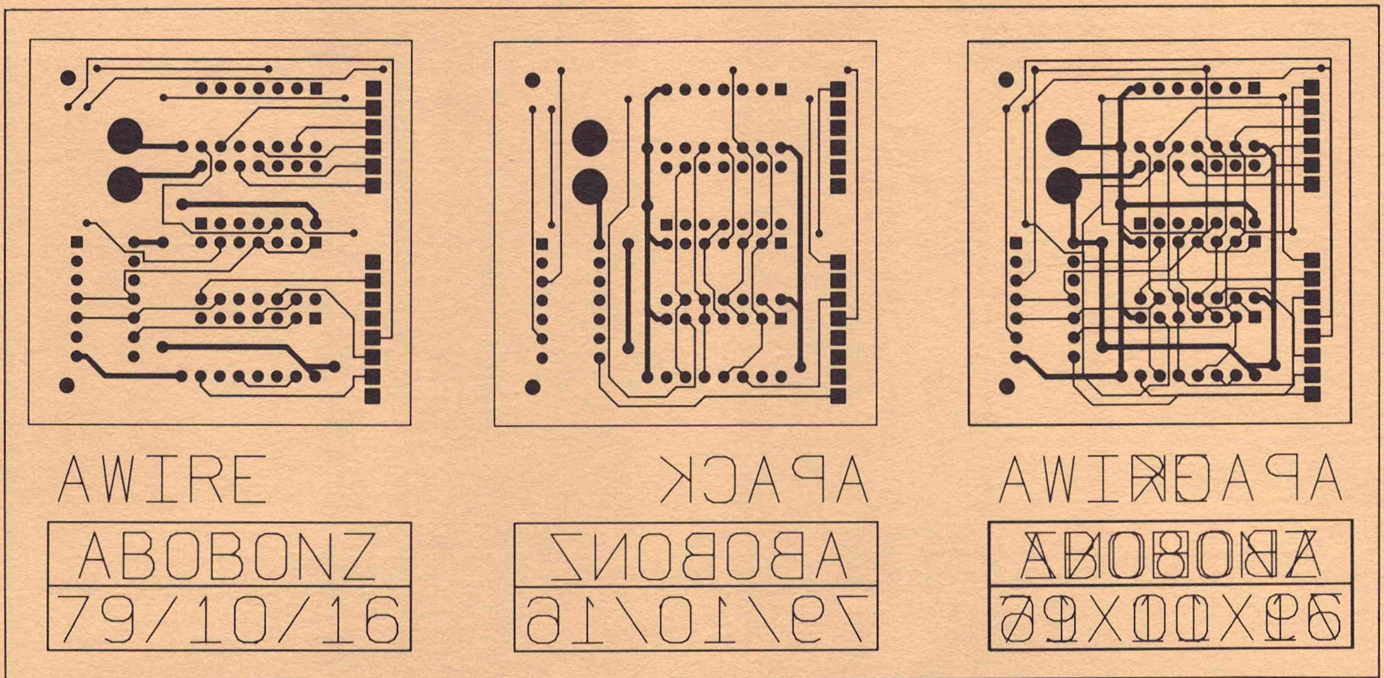


Figure 3. These are graphic outputs of PIRATE, a set of automatic router programs, after it worked with the schematic shown in figure 1.

Continued from page 8

enhanced it. Logic simulation has not shared the wide acceptance that SPICE has received. LSI design engineers are the most frequent users of our logic simulator.

Functional simulation is the next higher level of simulation: logical blocks, such as encoders, decoders, shift registers and adders, are the commonly-used primitives. Some users call this type of simulator a "register transfer level (rtl) simulator." Graeme Boyle, CAD Development, recently developed such a simulator based on SPLICE, a program written at the University of California at Berkeley. CAD Development is testing this simulator.

Fault simulation is a type of simulation which tests the test for a circuit. A source generates test vectors for a circuit; the simulator then injects faults, usually stuck-at-1's (SA1) and stuck-at-0's (SA0), into the circuit and applies the set of test vectors to the circuit.

If the simulator can propagate the injected fault through the circuit and detect it at an output by a change in the output pattern of a faultless circuit, then the test pattern covers that fault. Evaluating all injected faults (usually SA1's and SA0's of all inputs and outputs of all gates of a circuit) to see whether they are covered yields a percentage called **circuit coverage.** Few people at Tektronix use fault simulators.

The last classification is **automatic test generation** (atg) in which algorithms, usually run on a large mainframe computer, generate test vectors. Use of atg systems within the industry is varied. Some companies, such as IBM, use them extensively. Other companies are very apprehensive about using these systems and often use alternatives.

CAD STATIONS

Tektronix has used CAD stations (digitizing stations) for several years. (**Digitizing** is the process of taking hand-developed board layout artwork and entering this data into a computer file for editing or further processing to generate tapes for the fabrication process.)

The Applicon system, at Walker Road, is a CAD station and processes ecb layout artwork. The Redac system in Wilsonville is really an automated routing system which

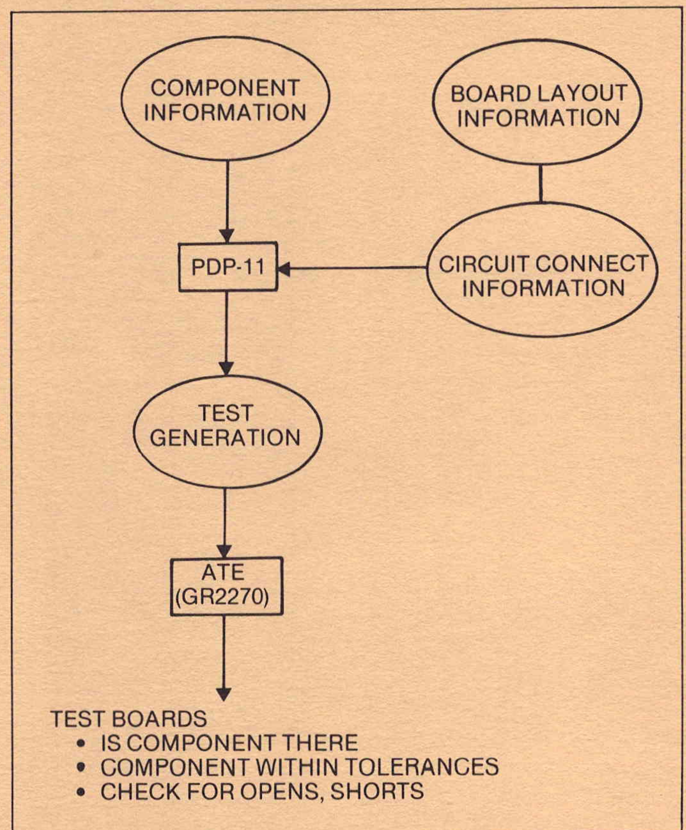


Figure 4. This diagram shows a typical automated board-testing operation at Tektronix.

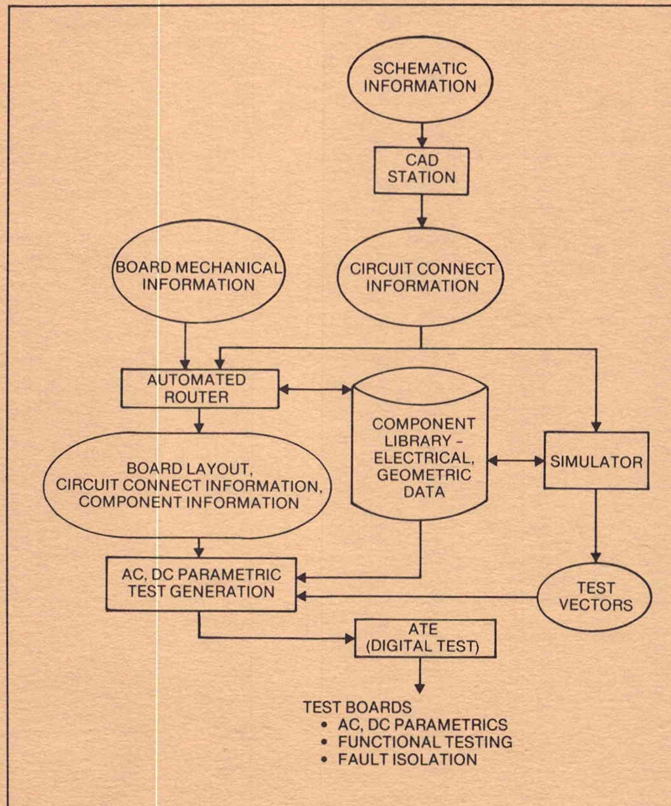


Figure 5. This flow of circuit information from a set of typical CAD tools into a testing environment is standard for most of the electronics industry.

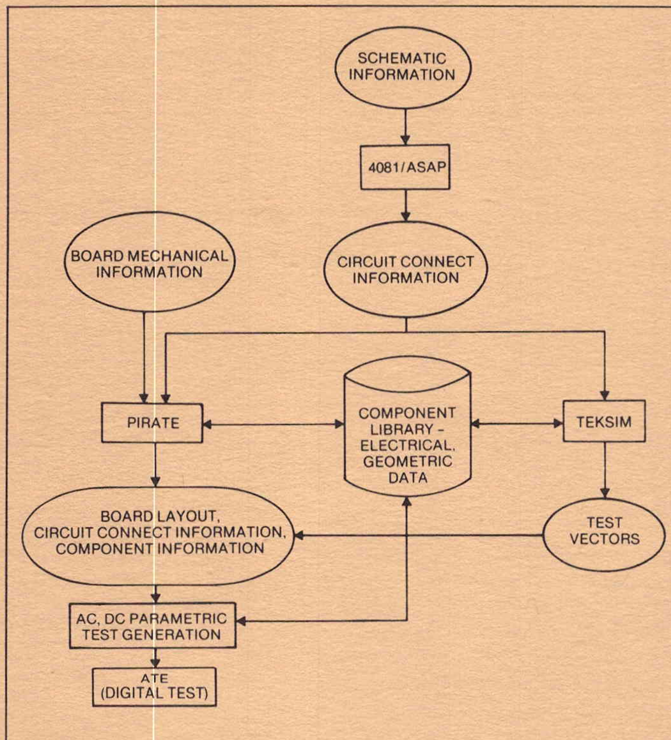


Figure 6. For in-house CAD testing, Tektronix has the 4081/ASAP system to handle most schematics, PIRATE (an automated router), simulation programs, and a component library. Tektronix does not have a target ATE or a test generation package.

includes an operator who inputs circuit connect, component, and board information to the system. The output is a final board layout. The David Mann system in the LSI design area digitizes manually produced IC layout artwork, and develops a pattern generator tape which system operators use to generate reticules for the chip.

A newcomer to the CAD station scene is the Tektronix IGS (Interactive Graphic System) 4081. This system is an intelligent terminal that IDD designed around an Interdata 7/16 (a 16-bit minicomputer with 65k bytes of accessible memory). The system includes a 19-inch direct-view storage tube with refresh capability. Peripheral equipment can include floppy discs, hard discs, graphic tablet, digital plotter, magnetic tape drive, and printer. A software group in IDD wrote the original ASAP (a graphic editor) for the 4081. Using this editor, a user can create a file (which the user can represent graphically), edit, save, and load a file. (There are actually two versions of ASAP at the present time — an IDD version and a heavily modified version written by the CAD Development staff.)

Prime applications of 4081/ASAP are schematic and ecb artwork digitization. Active users of this system include TM500, Manuals Maintenance, CAD/Graphics and Prototype (Wilsonville). (The total 4081/ASAP system is strictly an internal development and is not in the marketplace.)

PRESENT BOARD-TESTING ENVIRONMENT

Figure 4 is a flow diagram of a typical board-testing operation at Tektronix. The primary input is the board artwork for a given circuit. From the layout artwork, the following data is obtained: component types, circuit-connect information, and bed-of-nails positioning for the tester. This data enters a computer which has a test generation software package usually supplied by the ATE vendor. The computer/ATE vendor package generates the tests and the ATE implements them. Present test capabilities are in-circuit checks which determine:

- If a specific component is at a specific location.
- If a component parameter is within tolerance.
- If there is a short or open between specific points.

In the Tektronix design environment, a designer must generate all the input data by hand. Even though much of the information exists on files in other computers, the designer must recompile it and submit to another data "sink."

THE INTERFACE

Figure 5 shows the flow of circuit information from a set of typical CAD tools into a testing environment. The circuit designer or support person initiates the flow by entering a circuit schematic, including component types, into a CAD station. The result is a digitized file. The circuit-connect information can be extracted from the digitized file and submitted to the automated router or the simulator or both. Ecb mechanical information must be submitted to the router and additional component geometric information obtained from the component library to enable the router to produce a board layout. Circuit-connect information coupled with component electrical information can be

Continued on page 12

technical standards

To borrow or order copies of standards, call ext. 241 (Town Center).

NEW STANDARDS

DOD-STD-100C — **Engineering Drawing Practices.** Replaces MIL-STD-100B.

DOD-HDBK-248A — Military Handbook Superseding MIL-HDBK-248 (AS). Guide for Application and Tailoring of Requirements for **Defense Material Acquisitions.**

MIL-C-17E; Amendment 2 — **Cables,** Radio Frequency, Flexible and Semirigid.

MIL-STD-454F; Notice 3 — General Requirements for **Electronic Equipment.**

MIL-S-9395E; Amendment 2 — **Switches,** Pressure, (Absolute, Gage and Differential).

MIL-C-3098G; Supplement 1 — **Crystal Units Quartz,** General Specs.

MIL-STD-1568A — Materials and Processes for **Corrosion Prevention and Control** in Aerospace Weapons Systems.

MIL-S-28788A — **Switches,** Air and Liquid Flow, Sensing.

MIL-C-38999G; Amendment 3 — **Connector,** Electrical Circular, Miniature, High Density Quick Disconnect (Bayonet, Threaded, and Breech Coupling), Environment Resistant, Removable Crimp and Hermetic Solder Contacts.

MIL-C-55036A; Amendment 1 — **Cable,** Telephone.

MIL-M-63007 (TM) — **Manuals,** Technical and Catalogs, Supply: Hand Receipt.

MIL-S-81619C — **Switches,** Solid State Transducer, (Analog and Digital).

MIL-I-23053/2C; Amendment 1 — **Insulation Sleeving,** Electrical, Heat Shrinkable, Polyvinyl Chloride, Flexible, Crosslinked and Non-Crosslinked.

MIL-I-23053/3A; Amendment 1 — **Insulation Sleeving,** Electrical, Heat Shrinkable, Polyvinyl Chloride, Semirigid, Crosslinked and Non-Crosslinked.

MIL-I-23053C; Amendment 2 — **Insulation Sleeving,** Electrical, Heat Shrinkable.

MIL-S-24236/11E — **Switch,** Thermostatic, (Bimetallic), Type I, Hermetically Sealed, Single Pole, Single Throw (SPST), 1 Ampere.

MIL-S-24236/17C — **Switches,** Thermostatic, (Bimetallic), Subminiature, Type II, Watertight, Single Pole, Single Throw (SPST), 2 Amperes.

MIS-S-24236/22B — **Switches,** Thermostatic, (Bimetallic), Type II, Hermetically Sealed, Single Terminal, .5 Ampere.

MIL-S-24236/23B — **Switches,** Thermostatic, (Bimetallic), Type II, Hermetically Sealed, Single Pole, Single Throw (SPST), 2 Amperes.

MIL-S-24236/25A — **Switches,** Thermostatic, (Bimetallic), Type I, Hermetically Sealed, Single Pole, Single Throw, (SPST), 2 Amperes.

QQ-S-365C — General Requirements for **Silver Plating, Electrodeposited.**

ISO 4578 — Determination of Peel Resistance of **High-Strength Adhesive Bonds,** Floating Roller Method.

UL 62; 1979 — Flexible **Cord and Fixture Wire.**

UL 817; Seventh Edition, Revision Pages — **Cord Sets and Power-Supply Cords.**

MIL-S-9395E; Amendment 2 — **Pressure Switches,** (Absolute, Gage and Differential).

MIL-S-81619C; (USAF) — Solid State **Transducer Switches.**

FCC; Volume III, Transmittal Sheet No. 11 — **Rules and Regulations,** August 1976 Edition. □

Continued from page 11

submitted to the simulator to aid in design verification and test vector generation. With board-layout information and test vectors available, a test generation package can be developed which tests the specific ecb.

These tests may include:

- DC parametrics
- AC parametrics
- Functional testing
- Fault isolation

THE GOOD NEWS

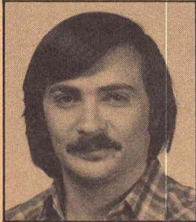
Figure 6 illustrates in-house CAD testing capabilities. The 4081/ASAP system can handle most schematics generated in-house. Circuit connect lists are available with ASAP in Wilsonville and should be available (in six months) from ASAP in Beaverton. PIRATE, an automated router, has been running for over a year; and, within CAD Development, we have successfully routed six major boards (11 inches by 16 inches with 160 equivalent DIP's). Simulation programs, at several levels, are available to assist the design verification and test vector generation efforts. The software structure of the component library is in place and some data already resides in it.

THE BAD NEWS

The remainder of the flow diagram in figure 6 needs to be filled in: the target ATE (probably a Zehntel machine), a test generation package, and a complete library. □

PATENT RECEIVED: No. 4,160,276

NEGATIVE IMPEDANCE TERMINATOR IMPROVES APERTURE CORRECTOR



Dan Baker, TV Engineering, ext. 5638 (Beaverton).

This invention compensates a non-ideal lossy delay line by terminating it with a negative resistance over the required bandwidth. It is an active terminator which can produce complex impedances not possible with passive components: negative real parts, positive-capacitive imaginary parts, and negative-inductive imaginary parts.

ADVANTAGES

The invention is used in a television picture monitor as an improved aperture-correction circuit. An aperture corrector enhances the high-frequency response of a kinescope (television-display crt) which is limited by the non-zero beam spot and picture-element size.

The corrector is a transversal filter consisting of a single delay line with only an input Zo termination. With this invention a lossy line appears as a lossless line that has an output reflection coefficient of unity or more. This characteristic is of special interest because the non-minimum phase response of the corrector requires a high degree of positive and negative edge symmetry to properly compensate for kinescope apperture distortion.

In addition to adding energy to the line to make it appear lossless, the invention serves as a a buffer to subsequent stages.

HOW THE CIRCUIT WORKS

The delay line in figure 1 can be modeled as a lossless line terminated in Zo at the input and terminated in a somewhat higher resistance at the output. (See figure 2.)

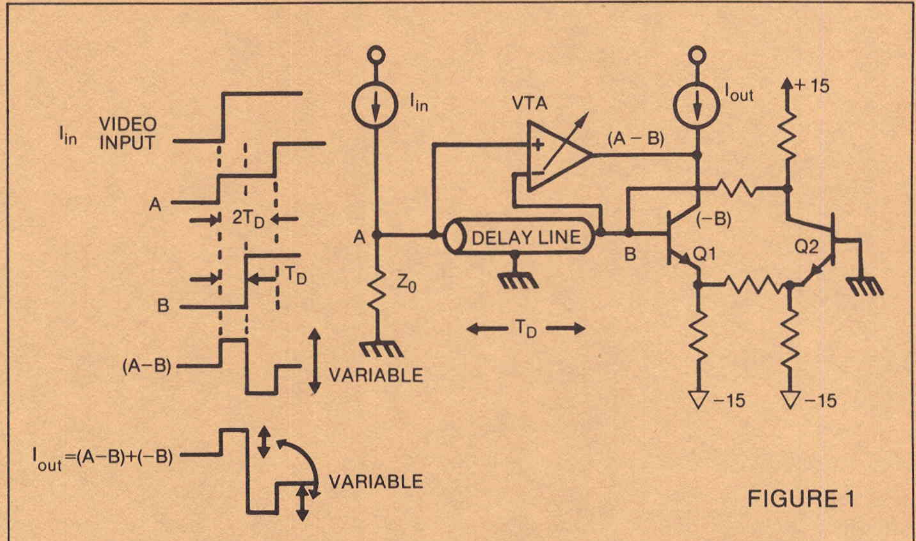


FIGURE 1

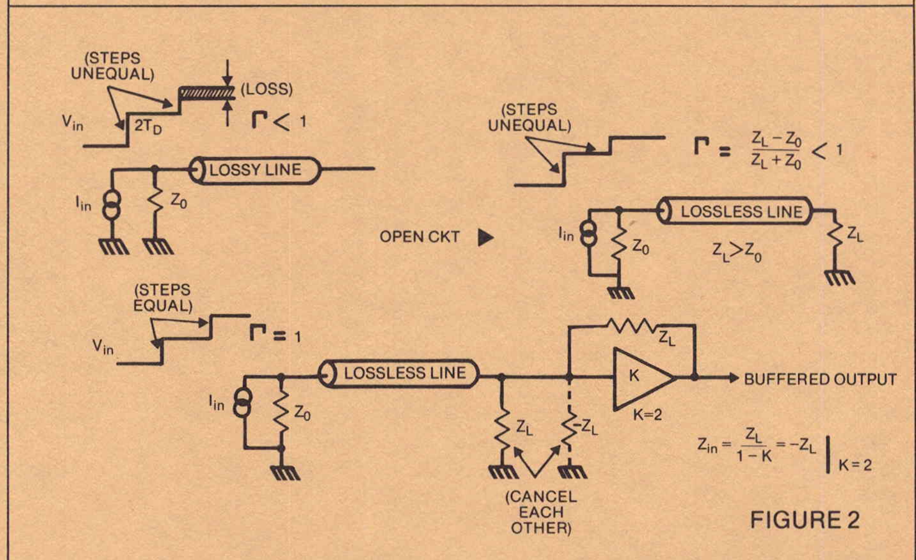


FIGURE 2

Q1 and Q2 provide the buffered output and the input energy that restores reflection coefficient of the line to unity. Reflection coefficients higher than unity are possible and stability is maintained as long as the total impedance is positive.

APPLICATION

Any product employing a transversal filter might benefit from this invention because it compensates for spurious impedance at delay line taps. Since the input impedance of the buffer can be complex; cancellation of capacitive, inductive, or even frequency-dependent losses can be achieved with circuits handling signals having limited bandwidth.

The invention is presently used in the Tektronix 653HR Series of high-resolution picture monitors. □

ENGINEER V PROFILE:
Charlie Rhodes

Charles W. Rhodes, Television Engineering, ext. 7068 (Beaverton).

Engineer/Scientist IV's and V's serve as technical resources for consultation by others at Tektronix. To increase their visibility to the Tektronix technical community, *Technology Report* will publish a series of profiles of these individuals.

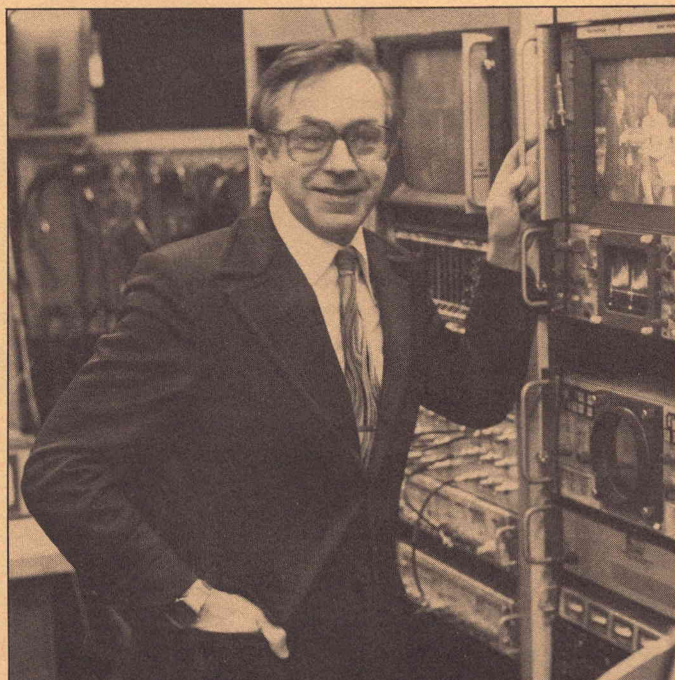
Charles (Charlie) W. Rhodes has a world-wide reputation in the broadcast-television engineering community. He earned that reputation with his innovations in television instrumentation and with several decades of effort to improve picture quality. He is particularly known for his work with vertical interval test signals. In recognition of his efforts in developing vertical interval test signals, Charlie was nominated for an "Emmy" award by the Academy of Motion Picture and Television Arts and Sciences.

Charlie's industry committee activities include chairing the Subcommittee on Studio Facilities (EIA), participating in the Subcommittee on Digital Technology (SMPTE), and working on numerous study groups and subcommittees of the Institute of Electrical and Electronic Engineers, and The Electronic Industries Association. He was recently appointed *Fellow of The IEEE.* He is active in the Society of Motion Picture and Television Engineers, the Royal Television Society (U.K.), the JCIC, The Satellite Technical Operations Committee, the Society of Broadcast Engineers, and the CCIR.

With nineteen U.S. and foreign patents granted and others pending, Charles W. Rhodes has contributed to the substantial respect and marketing position that Tektronix enjoys in video processing.

To keep in touch and to spread the word, Charlie travels widely. Internationally, his tours include annual consultations in Europe and Japan. Recently, the Peoples Republic of China invited Charlie to present lectures on tv measurement techniques. Think of a location where video progress is being made, and Charlie's been there.

Today, Charlie is studying the digital techniques for processing, transmitting, and measuring the television signal. These digital techniques represent a major change from the analog processes now dominant in television. This change creates business opportunities for Tektronix. The change to digital also presents the challenge of changing practices that Tektronix engineers, like Charlie, helped establish back when color-television broadcasting was new.



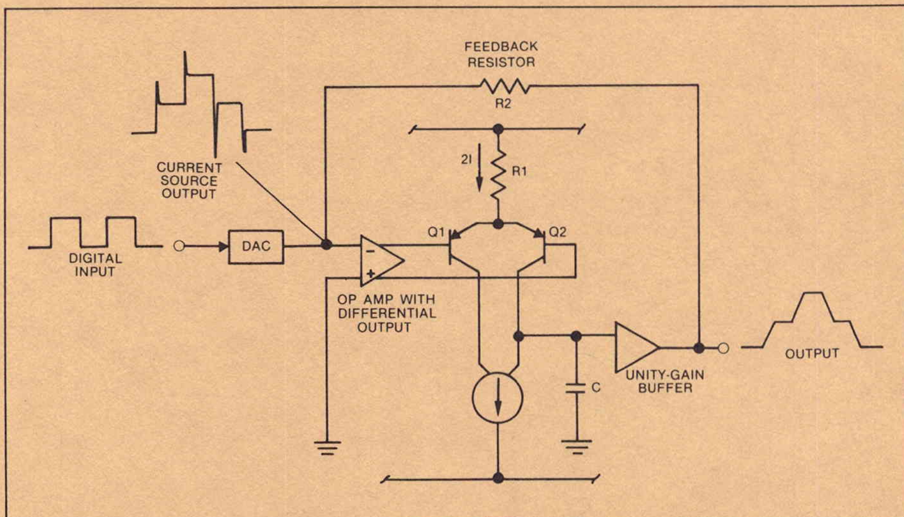
Charlie attended the University of California from 1947 to 1950. In 1956 he joined Tektronix from the Columbia Broadcasting System. □

Patent Received: No. 4,163,948

GLITCH FILTER FOR D/A CONVERTER

Michael Rieger, Signal Processing Research, ext. 5020 (Beaverton).

Martin Singer, Terminals and Displays Engineering, ext. 3976 (Wilsonville).



The patented circuit shown here is a nonlinear filter that attenuates spikes (glitches) occurring on the output waveforms of digital-to-analog converters (dacs) when an input digital word changes. This invention is most useful when the dac is used to produce a continuous curve where the binary-number input to the dac changes in unit increments. Previous filtering techniques included sample-and-hold circuits, which are too slow, and low-pass linear filters that smooth but do not completely eliminate glitches. This new circuit is fast and simple, yet it costs about the same as a sample-and-hold circuit.

HOW DOES THE INVENTION WORK?

Our nonlinear filter provides a small-signal, wide-bandwidth amplifier which is slew-rate limited. (The derivative of the output is constrained within specific amplitude limits.) The slew-rate of the circuit must be lower than the maximum desired rate of output waveform change.

The output of the dac contains glitches whenever the input digital word changes. These spikes are caused by either (1) unequal propagation delays among the bits arriving at the input, or (2) by variations in the transient responses of the binary-weighted elements within the dac, or (3) by a combination of (1) and (2).

The output of the dac is a current source presented to a high-gain operational amplifier which has a differential output. This differential output drives differential transistor-pair Q1-Q2 which is biased so that the common emitter current is equal to 2I. The collector current ranges from 0 to 2I. A current sink is connected to collector of Q2 so that the current available to the capacitor ranges from –I to +I. The voltage across the capacitor changes at a rate limited by + or – I/C. A unity-gain buffer stage presents the high-impedance output needed in most display applications. The loop closes through feedback resistor which determines the amplitude of the output.

APPLICATION

The glitch filter is being used in the GMA102 Display, Option 43 Vector Generator where it produces smooth lines and curves at the fast plotting rates of this product. ☐

Technology Report

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