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## I. INTRODUCTION

## A. General Information

1. The Type 422 is a 15 mc portable oscilloscope, designed to meet certain environmental specifications.
2. Two plug-on power supplies are available.
a. The AC Supply.
b. The AC-DC Supply.
(1) The AC-DC Supply will operate from the AC line, EXT DC source or from self-contained rechargeable batteries.
(2) The AC-DC Supply an internal battery charger.
3. The scope has a $10 \mathrm{mv} / \mathrm{DIV}$ dual trace vertical at DC to 15 mc .
a. A $\times 10$ GAIN AC switch increases the gain of Channel 2 by a factor of 10 (lowers the BP to 5 mc ).
4. The scope is a compact and light weight portable unit.
a. Front panel size is $6-3 / 4^{\prime \prime} \times 8-1 / 2^{\prime \prime}$, allowing two instruments to be mounted side by side in a $7^{\prime \prime} \times 19^{\prime \prime}$ rack space .
b. Net weight is about 20 pounds with the AC supply and accessories and about 30 pounds with the AC-DC supply and batteries.
B. Characteristics
5. Vertical
a. Frequency response: $D C$ to 15 mc .
(1) With $\times 10$ GAIN AC swtich pulled out, 5 cps to 5 mc .
b. Risetime: 23 nsec.
(1) In X 10 GAIN AC position, 70 nsec .
c. Deflection factors: $10 \mathrm{mv} /$ DIV to $20 \mathrm{v} /$ DIV in 11 calibrated steps.
(1) CH 2 gain can be increased ten times with $\times 10$ GAIN AC switch.
(2) A VARIABLE control in each channel provides an uncalibrated deflection factor of 2.5 times indicated deflection of at least $50 \mathrm{v} /$ DIV in the $20 \mathrm{v} /$ DIV position.
d. Accuracy: $\pm 3 \%$ of indicated deflection with VARIABLE fully clockwise (UNCAL light off), display centered.
(1) CH 2 accuracy is $\pm 7.5 \%$ in X 10 GAIN AC position.
e. Vertical Linearity: Less than . 2 division compression or expansion of a 2 division signal at the extremes of the display (includes CRT non-linearity).
f. Input RC characteristics: 1 meg paralleled by approximately 30 pf.
g. Input Coupling: AC or DC coupling selected by a front panel switch.
(1) Low frequency limit in $A C$ is 2 cps .
(2) The coupling switch includes a GND position that grounds the Vertical input.
h. Maximum Input Voltage: $\pm 300 \mathrm{v}$ combined DC and peak AC.
i. Operating Modes:
(1) Algebraically Added.
(2) CH 1 only.
(3) Dual Trace, chopped at a 100 kc rate.
(4) CH 2 only.
(5) Dual Trace, alternate.
i. Polarity of Channel 2 can be inverted.
k. Common mode rejection ratio: At least 100:1 at 50 kc with optimum gain setting.
6. Between channel isolation at $100,000: 1$ or greater at 1 kc .
m. Input grid current: Less than 2 nanoamps .
7. Triggering:
a. Source
(1) Internal -- TRIG IN connector.
(2) From CH 1 and CH 2 .
(3) CH 1 only.
b. Coupling
(1) $A C$.
(2) AC LF REJ.
(3) DC .
c. Polarity: A SLOPE switch selects positive or negative slope.
d. Modes
(1) AUTO.
(2) Adjustable triggering at a desired level.
(3) Free run.
e. Signal Requirements, Internal
(1) DC: Minimum of .2 divisions of deflection, $D C$ to 5 mc , increasing to 1 division at 15 mc .
(2) AC : Same as DC from 50 cps to 15 mc .
(3) AC LF REJ: Same as DC with decreasing sensitivity below 50 kc .
(4) AUTO: Minimum of .8 divisions of deflection, 50 cps to 4 mc ; increasing to 2.6 divisions at 15 mc .
f. Signal Requirements, External
(1) DC: Minimum of . 125 volts, DC to 5 mc , increasing to .6 v at 15 mc .
(2) AC : Same as $\mathrm{DC}, 50 \mathrm{cps}$ to 15 mc .
(3) AC LF REJ: Same as DC with decreasing sensitivity below 50 kc .
(4) AUTO: Minimum of $.5 \mathrm{v}, 50 \mathrm{cps}$ to 7 mc , increasing to 1.2 v at 15 mc .
g. Trigger Input RC: 100k paralleled by 35 pf (approximately).
h. Maximum External Trigger Input Voltage
(1) AC and AC LF REJ, DC component not to exceed $\pm 250$ volts with an AC component less than $100 v$ RMS.
(2) DC, maximum of 100 v RMS or peak voltage less than $\pm 250 \mathrm{v}$.
8. Horizontal Deflection:
a. Sweep Rates
(1) $.5 \mu \mathrm{sec} /$ DIV to $.5 \mathrm{sec} /$ DIV in 19 calibrated steps.
(2) $\mathrm{A} \times 10$ magnifier extends the calibrated range to $.05 \mu \mathrm{sec} /$ DIV.
(3) A VARIABLE control provides UNCALIBRATED sweep rates to at least 2.5 times the TIME/DIV setting or a maximum of at least $1.25 \mathrm{sec} /$ DIV.
b. Sweep Accuracy: Within $\pm 3 \%$ with VARIABLE fully clockwise (UNCAL light off) and X 10 MAG switch pushed in.
c. Sweep Magnification: A PULL FOR X10 MAG switch allows each sweep rate to be increased 10 times by expanding the center division of the display.
(1) Accuracy is within $\pm 5 \%$ with VARIABLE fully clockwise.
(2) Mag linearity (between first and ninth graticule lines), $\pm 1 \%$ over entire sweep length (exclusive of the first $1 \%$ of sweep) in all TIME/DIV positions except $.5 \mu \mathrm{sec}, \pm 3 \%$ in $.5 \mu \mathrm{sec}$.
d. External Horizontal Amplifier
(1) Deflection factor approximately 10 v/DIV with $\times 10$ MAG control pushed in.
(2) Deflection factor approximately 1 v/DIV with $\times 10$ MAG control pulled out.
(3) HORIZ ATTEN control (ganged with Triggering LEVEL) provides $\geq 10: 1$ variable deflection factor within the above ranges.
(4) Frequency response: DC to 500 kc .
(5) Input RC Characteristics: 300 k paralleled by 35 pf (approximately).
9. Calibrator:
a. Waveshape: square wave.
b. Polarity: Negative going with baseline near zero.
c. Amplitude: 2 volts from a front panel jack.
(1) Internal .2v.
d. Accuracy -- front panel jack: $\pm 2.7 \%$ at $25^{\circ} \mathrm{C} ; \pm 3.6 \%$ over entire operating temperature range.
e. Accuracy -- Internal: $\pm .7 \%$ at $25^{\circ} \mathrm{C} ; \pm 1.6 \%$ over entire operating temperature range.
f. Repetition rate, $\pm 20 \%$.
g. Risetime: About $6 \mu \mathrm{sec}$.
h. Fall Time: About $1 \mu \mathrm{sec}$.
i. Output impedance (front panel jack): approximately 2 k .
10. Gate Out Signal:
a. Waveshape: Rectangular pulse.
b. Polarity: Negative going with baseline at zero.
c. Amplitude: About 600 mv .
d. Duration: Approximately the same as the sweep.
e. Source Impedance: Approximately 600 .
11. CRT Circuit:
a. CRT Type: T4220-31-1.
b. Phosphor: P31 standard.
c. Unblanking: DC coupled deflection unblanking.
d. Accelerating Voltage: Apprxoimately 6.3 kv .
e. External Blanking: From EXT BLANKING jack.
(1) +2 volts completely blanks the trace.
(2) Input Z: Approximately $235 \Omega$.
f. Graticule: Edge lighted internal graticule.
(1) Area: 8 DIV vertically by 10 DIV horizontally -each division is .8 cm .
12. AC Power Supply:
a. $\quad 115 \mathrm{v}$ AC $\pm 10 \%$ or 230 v AC $\pm 10 \%$.
(1) Additional transformer windings provide for inputs of $105 v, 125 v, 210 v$ and $250 v( \pm 10 \%)$.
(2) Sine wave $<1 \%$ distortion.
b. Line Frequency: 50 cps to $400 \mathrm{cps} \pm 10 \%$.
c. Power Consumption: Approximately 34 nominal .
d. Thermal protection: Automatic resetting thermal cutout set at $187^{\circ} \mathrm{F}$.
13. AC-DC Power Supply:
a. AC Source
(1) $115 \mathrm{AC} \pm 20 \%$.
(2) $230 v \mathrm{AC} \pm 20 \%$.
(3) Input power selection is made by the POWER MODE switch on the power supply's rear panel.
(4) Frequency 45 to 440 cps -- at 45 cps the upper voltage limits are derated to $10 \%$. The derating begins at 50 cps .
b. AC Power Consumption: Typically 27 watts for all voltages .
c. DC External
(1) 11.5 v to 35 v DC.
(2) Power consumption, typically $23 w$.
d. DC Internal
(1) $24 v$ battery (rechargeable).
(2) $20,1.2 \mathrm{v}, 3.5$ amper hour $\mathrm{N}_{\mathrm{i}} \mathrm{C}_{\mathrm{d}}$ cells.
(3) Power consumption typically $23 w$.
(4) About 4 hours running time .
e. A 400 ma battery charger is included.
14. Environmental Characteristics with AC Supply:
a. Temperature
(1) Operating: $-15^{\circ} \mathrm{C}$ to $+55^{\circ} \mathrm{C}$.
(2) Non-Operating: $-55^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$.
b. Altitude
(1) Operating: 15,000 feet maximum .
(2) Non-Operating: 50,000 feet maximum .
c. Humidity: Meets Mil-Std-202B, method 106A through

5 cycles (120 hours), freezing and vibration included.
d. Vibration
(1) Operating: . 025 inch peak-to-peak total displacement ( 5 G at 55 cps ) from 10-55-10 in 1 minute cycles on each axis. Held for 3 minutes at 55 cycles. Total vibration time, 55 minutes.
(2) Non-Operating: Resonant searches performed along each axis with .030 inch total displacement from 10-55 cps. All major resonances above 55 cps .
e. Shock
(1) Operating: 20G, one-half sine, 11 msec duration. Two shocks each direction along each of the three major axes (total of 12 shocks).
(2) Non-Operating: 60G, one-half sine, 11 msec duration. One shock each direction along each of the three major axes (total of 6 shocks).
f. Radio Frequency Interference (RFI)
(1) Operating, test procedures and limits described in Mil-1, 6181D and Mil-1-16910A, paragraph 3.6.1.1.5.1 used.
(2) Tests performed within an electrically shielded enclosure with the instrument equipped with a line filter and CRT mesh filter. Checks made for radiated interference within specified limits over a range of 14 kc to 1000 mc , and conducted inferference within the specified limits from 150 kc to 25 mc .
10. Environmental characteristics with the AC-DC Supply: a. All characteristics are the same as the AC supply when the AC-DC Supply is used without batteries.
b. With batteries, the temperature range is derated:
(1) Charge temperature range: $-5^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
(2) Discharge (operate): $-15^{\circ} \mathrm{C}$ to $+40^{\circ} \mathrm{C}$.
(3) Non-Operating: $-40^{\circ} \mathrm{C}$ to $+60^{\circ} \mathrm{C}$.

## II. CHANNEL I INPUT AMPLIFIER

A. The Channel I Input Amplifier amplifies a nd attenuates the input signal.

1. The circuit provides a push-pull current drive to the Vertical Amplifier.
2. A Channel 1 trigger signal is also provided.
B. Circuits that comprise the Channel 1 Input Amplifier:
3. Attenuator and Input Switches.
4. INPUT CF, VI3.
5. CF CURRENT SOURCE, Q24.
6. Feedback Amplifier; Q34, Q44.
7. Paraphase Inverter; Q84, Q94.
8. Position Driver; Q64, Q74.
9. CH 1 TRIG EF, Q53.

D. Block Logic
10. The Input Amplifier has a current output of $.45 \mathrm{ma} / \mathrm{div}$ per side.
a. Since the amplifier has a current output and a voltage input, the signal transfer is rated as transadmittance*.
b. Transadmittance gain, $T_{Y}=\frac{\mathrm{I}_{\text {out }}}{\mathrm{E}_{\text {in }}}$
11. A calibrator position and 11 sensitivity positions are available on the VOLTS/DIV switch.
12. The amplifier changes its basic sensitivity (and gain) in the $.01 \mathrm{v} / \mathrm{div}$ and $.02 \mathrm{v} / \mathrm{div}$ positions of the VOLTS/DIV switch.
a. At. $01 \mathrm{v} / \mathrm{div}, T_{Y}=45,000 \mu \mathrm{mhos}$.
(1) $T_{Y}=\frac{i_{\text {out }}}{E_{\text {in }}}$
(2) $T_{Y}=\frac{.45 \mathrm{ma} / \mathrm{div}}{10 \mathrm{mv} / \mathrm{div}}$
b. At. $02 \mathrm{v} / \mathrm{div}, \mathrm{T}_{\mathrm{Y}}=22,500 \mu \mathrm{mhos}$.
(1) $T_{Y}=\frac{.45 \mathrm{ma} / \mathrm{div}}{20 \mathrm{mv} / \mathrm{div}}$
c. At. $05 \mathrm{v} / \mathrm{div}$ and all other sensitivities $(.05 \mathrm{mv} / \mathrm{div}$ to $20 \mathrm{v} / \mathrm{div}$ ), $\mathrm{T}_{\mathrm{Y}}=9000 \mu$ mhos.
(1) $T_{Y}=\frac{.45 \mathrm{ma} / \mathrm{div}}{50 \mathrm{mv} / \mathrm{div}}$
d. In the CAL position, the calibrator is connected to provide a 4 div display.
13. Input impedance is 1 meg at approximately 30 pf .
14. V13 is the input CF nuvistor.
15. A two stage transistorized feedback amplifier includes a section of the VOLTS/DIV switch that changes the basic sensitivity of the amplifier.
a. In the . 01 VOLTS/DIV position, the feedback amplifier has a gain of 5 .
b. In the . 02 VOLTS/DIV position, the feedback amplifier has a gain of 2.5.
c. In the .05 VOLTS/DIV to 20 VOLTS/DIV and in the CAL position, the feedback amplifier has unity gain.
16. The STEP ATTEN BAL control, operating through the CF current source transistor, Q24, adjusts potentials at the feedback amplifier so changing sensitivity positions will not shift the trace.
17. The output from the feedback amplifier at about $45 \mathrm{mv} / \mathrm{div}$ is fed via the CH 1 Trigger EF, Q53, to the Trigger Amplifier .
18. The single ended voltage signal becomes a push-pull current drive in the Paraphase Inverter, Q84, Q94.
19. The POSITION control, through Position Drivers, Q64 and Q74, feeds positioning information through the Paraphase Inverter to the Vertical Amplifier.
20. The current drive to the Vertical Amplifier through the switching circuit is $.45 \mathrm{ma} /$ div per side.
E. Attenuators and Input Switches
21. The circuit includes the AC/DC/GND switch, the VOLTS/DIV switch and the four attenuators.
22. The input jack is a BNC connector.
23. Input $Z$ is a 1 Meg at about 30 pf .
a. The input is not standardized with the conventional "30 pf" standardizer.
b. The suggested procedure is to compensate a probe with Channel 1 input capacitor (C12) at mid range, then adjust Channel 2 to match the probe.
24. The input is limited to a voltage excursion of $\pm 300 \mathrm{v}$.

25. A front panel lever-wafer switch is used for the AC/DC switch.
a. The AC position inserts a. . $1 \mu \mathrm{f}$ tubular capacitor .
b. The GND position opens the input connection and grounds the Input CF grid.
c. The DC position connects through the attenuators, if any, to the Input CF .
26. Stacked attenuators are used.
a. The first bank includes $a \div 1$ (straight wire), $a \div 10$ and $\div 100$.
b. The second bank has a $\div 2$ and $\div 4$.
27. The CALIBRATE position of the VOLTS/DIV switch disconnects the INPUT and connects the calibrator to the Input CF.
a. The CH 1 Input Amplifier is in its 50 mv /div sensitivity.
b. The Calibrator signal is 200 mv peak-to-peak.
c. This provides a 4 division Calibrator display.
28. The $.01 \mathrm{v} / \mathrm{div}$ and $.02 \mathrm{v} /$ div positions of the VOLTS/DIV switch use no attenuators ( $\div 1$ attenuator).
a. Sensitivities are changed in the feedback amplifier stage.
29. Positions . 05 VOLTS/DIV through 20 VOLTS/DIV use various attenuator combinations to achieve the required attenuator range.
30. R9 breaks up lead inductance in the input lead.
31. The Attenuators are the conventional compensated attenuators.

$\div 4$


a. $\quad 1 \%$ precision resistors are used.
b. The attenuators are standardized using a probe compensated to CH 1 in a straight through position (. $01 \mathrm{v} / \mathrm{div}$, $.02 \mathrm{v} / \mathrm{div}$, or $.05 \mathrm{v} / \mathrm{div}$ ) with $\mathrm{C} 12^{*}$ (Input CF circuit) set to mid range.
c. Calibrator accuracy is spec ${ }^{\prime} d$ at $\pm 3 \%$.
F. Input CF, V13
32. The input CF provides a high $Z$ input impedance and isolates the input from any change in impedance as gain or sensitivity of the amplifier is changed.
a. Grid current should not exceed 2 nanoamps.


* C12 and C112 (CH 2 INPUT AMP) are both variable to facilitate production calibration.

2. V13 is a 8056 nuvistor with a mu of about 10 .
a. The diodes are 6185 silicon diodes.
3. CF has a gain of about.9.
a. With the high $Z$ cathode tail through Q 24 , gain is about $\frac{\mu}{\mu+1}$.
4. Circuit protection:
a. The Input is limited to $\pm 300 \mathrm{v}$.
b. R11 is a protective resistor that limits V13 grid current to $300 \mu \mathrm{a}$, if the input is raised to 300 v .
(1) C 11 bypasses the protective resistor for AC .
(2) It provides charging current for V13 input $C$.
c. B 12 provides reverse protection when V 13 grid is dropped below its carhode.
(1) B12 fires at about 80 v and burns at 60 v .
(2) V13 cathode is protected from arc over.
(3) If the input drops to -300 v , about $300 \mu$ a would flow through R11 and B12.
d. D14 and D15 protect V13 grid during tube warm-up.
e. D17 protects Q24 from base-collector breakdown.
(1) D17 conducts if V13 grid and cathode are raised enough to lift Q24 collector above 12 v .
5. C 12 standardizes the input at about 30 pf in the "straight through" position of the VOLTS/DIV switch.
6. $\mathrm{R} 13, \mathrm{C} 13$ decouples V 13 plate supply.
G. CF Current Source, Q24
7. Q24 is a variable current source for V13.
a. Using the STEP ATTEN BAL control, V13 current is adjusted so that Q34 emitter sets at ground potential.
b. Under this condition, the VOLTS/DIV switch can change Q34 emitter return resistance without causing a trace shift.
8. Q24 is a $151-108,2 \mathrm{~N} 2501$ silicon NPN transistor.
9. Q24 base, connected to the STEP ATTEN BAL control, can set voltages from -6.3 v to -8.5 v .
a. D21, a 5.1v zener diode, provides a constant voltage drop across the STEP ATTEN BAL pot, referenced to the -12 v supply.
b. Any change in the -12 v supply will all appear at Q 24 base to match the change on Q24 emitter.
c. Without the zener, only a divided down portion of a voltage change on the -12 v bus would appear on Q24 base.
10. D22, a 6185 silicon diode, temperature compensates Q24 base-emitter junction.
11. C 22 couples any AC on the -12 v supply to Q 24 base to match the same $A C$ on the emitter.
H. Feedback Amplifier; Q34, Q44
12. The feedback amplifier is a transistor pair that controls the basic sensitivity of the CH 1 Input Amplifier.
a. Q34 is a 151-108, 2N2501 silicon NPN transistor.
b. Q44 is a 151-133, MM999 silicon PNP transistor.
13. As a feedback amplifier, gain is virtually independent of transistor beta.
a. $A=1+\frac{R_{f}}{R_{a}}$
(1) $R_{f}$ is R39.
(2) $R_{a}$ is $R 30$ in the $.01 \mathrm{v} /$ div position of the VOLTS/DIV switch.
(3) $R_{a}$ is $R 32$ in the $.02 \mathrm{v} / \mathrm{div}$ position.
(4) There is no $R_{a}$ in the $.05 \mathrm{v} /$ div position.
b. In the . $01 \mathrm{v} / \operatorname{div}$ position $A=5$.
(1) $A=1+\frac{511}{127}$
$A \approx 5$
c. In the . $02 \mathrm{v} / \mathrm{div}$ position, $\mathrm{A}=2.5$.
(1) $A=1+\frac{511}{340}$
$A \approx 2.5$
d. In the $.05 \mathrm{v} /$ div through $20 \mathrm{v} /$ div position, $A=1$.
(1) $A=1+\frac{511}{\infty}$

$$
A \approx 1
$$

2. Proper setting of the STEP ATTEN BAL control sets Q34 emitter at 0 v .
a. Operating Q34 emitter at ground allows simple gain switching with R30 and R32 returned to ground.
3. L30 and C30 provide HF correction in the . $01 \mathrm{v} / \mathrm{div}$ position.
4. D16, a 6185 silicon diode, temperature compensates Q34 base-emitter junction.
5. D41, a $1 \mathrm{~N} 753 \mathrm{~A}, 6.2 \mathrm{v}$ zener, provides a low impedance 6 v emitter supply for Q44.
a. It is referenced to the +12 v supply.
b. If any change in the +12 v supply through R34, R35 appears on Q44 base, it will be balanced by an identical change on Q44 emitter.
c. C41 couples any $A C$ on the $+12 v$ supply to $Q 44$ emitter . It also filters out zener noise.
d. L41 improves the transient response by introducing HF degeneration.
6. The VARIABLE BALANCE adjusts the current through Q34 and Q44 to set the voltage at Q84 base.

a. Q84 base sets at about -4 v to match the level on Q94 base.
b. When the two bases are at equal potentials, no static current flows through the VARIABLE control.
c. Rotating the VARIABLE control does not shift the trace, indicating Variable Balance.
7. There is little interaction between the STEP ATTEN BAL and the VARIABLE BALANCE controls.
a. As the VARIABLE BALANCE control is adjusted, Q34 emitter moves about 1\% as far as Q84 base.
b. The ratio of change is proportional to the ratio of $Q 34 R_{e}$ (about 6 $\Omega$ ) to R39.
8. The signal level at Q44 collector is about $45 \mathrm{mv} / \mathrm{div}$.
I. Paraphase Inverter; Q84, Q94
9. The Paraphase Inverter provides a push pull drive to the Vertical Amplifier.
a. Since the Vertical Amplifier is an operational amplifier, the Paraphase Inverter functions as a current drive.
b. The collector load appears in the Vertical Amplifier circuit.
10. Q84 and Q94 are 151-108 silicon NPN transistors.
11. R84 and R94 provide thermal balance* for the push pull stage.
a. C84 bypasses R84 to keep signal voltage off Q84 collector, thereby eleminating Miller capacitance.
12. VARIABLE (VOLTS/DIV) control and the GAIN adj are in series between the emitters .

a. When the VARIABLE BALANCE control is properly adjusted, no static current flows through GAIN and VARIABLE controls.
b. The VARIABLE control has a $3: 1$ range with the GAIN adj set at mid range.
c. A CALIBRATED detent is available in the full clockwise position.
d. An UNCALIBRATED light indicates the control is in use.
13. Output signal current is . $45 \mathrm{ma} / \mathrm{div}$ per side.
a. Signal current can be calculated as $i=\frac{V_{e}}{R_{e}}$, where $V_{e}$ is Q84 emitter signal voltage and $R_{e}$ is the emitter resistance plus R83 in series with the GAIN control -- VARIABLE will be set at CALIBRATE $-=0 \Omega$.
b. $i=\frac{45 \mathrm{mv} / \mathrm{div}}{100 \Omega}$ $i=.45 \mathrm{ma} / \mathrm{div}$
14. Operating current for Q84 and Q94 is supplied by the Position Driver transistor .
a. About 6 ma per side is supplied.
15. Q94 base is tied to an equivalent -3.8 v through $208 \Omega$.
a. The divider connects to the -12 v supply.
b. D78, a 6.2 v zener, references the point to ground, however .
J. Position Drivers; Q64, Q74

16. The Position Driver transistors are actually a current source for the Paraphase Inverter.
a. The POSITION control changes the static current through Q84 and Q94 to position the trace.
17. Q64 and Q74 are 151-108, silicon transistors like those used in the Paraphase Inverter.
18. The POSITION control changes the bias on Q64 and Q74. a. Q64 and Q74 in turn furnish current to Q84 and Q94.
b. Rotation of the POSITION control will increase static current in one side of the Paraphase Inverter while decreasing current in the other side.
19. The control has a range of about 20 graticule divisions.
20. About 6 ma of static current flows through each side of the Paraphase Inverter .
a. The POSITION control can swing this current $\pm 5 \mathrm{ma}$. (from 1 ma to 11 ma ).
b. The POSITIONING control has a 4 v range at each arm.
21. As the static current is changed in Q84 and Q94 as a result of Positioning, Q84 and Q94 emitters move relative to one another. a. Q84 and Q94 each have about $6 \Omega r_{e}$.
b. Full swing of the POSITION control will move each emitter about 75 mv .
22. A first-order correction* is provided by resistor, R75.
a. The 4 v POSITION control swing is picked off Q74 emitter.

* First order correction: A gross correction -- in the ball park.
b. The $4 v$ swing is divided down by R75, R77 and R78 to 180 mv and fed to Q94 base.
c. Polarity and amplitude of the voltage is right to correct for the unbalance between Q84 and Q94 emitters.
d. It keeps the VAR BAL in adjustment for any position on the screen.

8. R65 provides an emitter impedance and current return for Q64 to match that introduced by R75.
9. C63 and C73 bypass Q64 and Q74 bases .
a. L63 and L73 prevent the circuit from oscillating.
K. CH 1 Trigger EF, Q53
10. The Trigger EF provides a single ended trigger to the Internal Trigger circuit.

11. $\quad$ Q53 is a 151-108, silicon NPN transistor.
12. The signal at Q 53 base is about $45 \mathrm{mv} / \mathrm{div}$.
13. The CH 1 Trigger EF drives a feedback amplifier in the trigger circuit.
a. R54 is $R_{i}$ for the feedback amplifier.
b. R54 at 6.81 k is one-tenth the value of the $\mathrm{CH} 1-\mathrm{CH} 2$ $R_{i}$ in the Vertical Amplifier.
c. The difference compensates for the difference in signal level of the CH 1 take-off and the main Vertical Trigger take-off.
14. R56 places the CH I Trigger take-off at a 0 v DC level compatible with the other trigger sources.
15. R59 breaks up lead $L$ in the cable to the trigger circuit.

## III. CHANNEL 2 INPUT AMPLIFIER

A. The Channel 2 Input Amplifier is the same as the Channel 1 Input Amplifier with three exceptions:

1. The addition of a PULL FOR X10 GAIN AC switch and circuit.
2. The addition of a PULL TO INVERT switch.
3. The amplifier does not have a Trigger Out circuit.
B. Input CF Differences

4. The HF correction used in Q34 emitter return in the . $01 \mathrm{v} / \mathrm{div}$ position of the VOLTS/DIV switch is not needed in the Channel 2 Input Amplifier.
a. Differences in layout apparently make the difference.
5. C114 appears at V113 cathode to match the transient response of the two preamps.
C. X10 Anaplifier, Q154


TYPE 422 CHANNEL 2 INPUT AMPLIFIER
B-422-0009
PARAPHASE INVERTER
$1-18-165 \mathrm{dl}+$ (1)

1. The circuit provides an $A C$ coupled $\times 10$ gain increase. a. All VOLTS/DIV switch readings should be divided by 10 when the switch is pulled.
2. Q154 is a 151-133 silicon PNP transistor.
3. $A \times 10$ gain increase is actually a $X 9$ signal added to the existing X1 signal.
4. The X 1 signal is applied to the base of Q 184 .
a. The X 9 signal is inverted in Q154 and applied to the base of Q194.
5. Frequency response is reduced to 5 mc in the X 10 position.
6. Low frequency cut-off is 5 cps ( $A C-D C$ switch in $A C$ ).
a. The X 9 signal is AC coupled while the X 1 signal may be DC coupled*.
b. If the input is DC coupled, the response below 2 cps drops 20 db to the DC coupled X 1 signal level .
c. R151 and C151 determines the low frequency cut off.
7. Q154 is an operational amplifier.
a. R153 is $R_{f}$.
b. R151 is $R_{\mathbf{i}}$ (plus the output $Z$ of the Feedback Amplifier and the input $Z$ of Q154).
c. Since Q154 has somewhat less than infinite open loop gain (actually it is about 115), the formula $A=\frac{R_{f}}{R_{i}}$ must be modified.
d. The zero signal voltage point appears, not at Q184 base but about $25 \Omega$ from the base along R 153 .
e. $R_{f}$, therefore, becomes $R 153$ minus $25 \Omega$ and $R_{i}$ becomes R151 plus $25 \Omega$, plus $4 \Omega$ output $Z$ of the Feedback Amplifier.
f. A $10 \%$ loss occurs in divider R156, R175 and from some feedback through R175, Q174 to Q194 emitter.
g. The result is the required X 9 gain.
D. Pull to Invert Switch
8. The switch merely inverts the Channel 2 input.
9. Useful in ADDED ALGEBRAICALLY mode.

## IV. VERTICAL SWITCHING AND OUTPUT AMPLIFIER

A. The Vertical Amplifier provides deflection voltage to the CRT vertical deflection plates.

1. CRT deflection sensitivity is $6.1 \mathrm{v} / \mathrm{div}^{*}(3.05 \mathrm{v} /$ div each plate).
2. The circuit provides dual trace switching for the CH 1 and CH 2

Input Amplifier.
3. An Internal Trigger signal is provided.
4. A Chop Blanking pulse is also provided.
5. Signal delay of about 150 nsec is included.
6. There are only four tweaks in the entire vertical.
B. Block Diagram


TYPE 422 VERTICAL SWITCHING \& OUTPUT AMPLIFIER B-422-0010 BLOCK DIAGRAM $\quad 1-14-65 \mathrm{~ms}$

* CRT spec is $5.3 \mathrm{v} / \mathrm{div}$ to $6.2 \mathrm{v} / \mathrm{div}$.
C. Circuits that comprise the Vertical Switching and Output circuits:

1. Switching Logic Gates.
2. Driver Amplifier; Q224, Q234.
3. Output Amplifier; Q244, Q254.
4. Switching Multi; Q265, Q275, Q283.
5. Alt Sync Pulse Amplifier, Q264.
6. Chop Blanking Amplifier, Q294.
D. Block Logic
7. The T4220 CRT has a vertical sensitivity of $6.1 \mathrm{v} / \mathrm{div}(3.05 \mathrm{v} / \mathrm{DIV}$ per side).
a. Since the Vertical Amplifier has a current input and a voltage output, the signal transfer is rated as transimpedance*.
b. Transimpedance, $T_{Z}=\frac{e_{\text {out }}}{i_{\text {in }}}, \frac{3.05 \mathrm{v} / \mathrm{DIV}}{.45 \mathrm{ma} / \mathrm{DIV}}$.
c. $\quad T_{Z}=6.75 \mathrm{k}$.
8. Gain of the entire Vertical system changes with settings of the VOLTS/DIV switch.
a. . 01 VOLT/DIV position has a voltage gain of 610.
(1) $\frac{6.1 \mathrm{v} / \mathrm{div}}{.01 \mathrm{v} / \mathrm{div}}=610$.
(2) or $A=T_{Y} \times 2 T_{Z}{ }^{* *}$.

$$
A=45 \times 10^{-3} \times 13.5 \times 10^{3}=610
$$

b. . $02 \mathrm{v} / \mathrm{div}$ position has a gain of 305 .
(1) $\frac{6.1 \mathrm{v} / \mathrm{div}}{.02 \mathrm{v} / \mathrm{div}}=305$.
(2) or $A=22.5 \times 10^{-3} \times 13.5 \times 10^{3}=305$.

* See June 1963 Service Scope.
** The push pull amplifier has a value of $2 T_{Z}$.
c. $.05 \mathrm{v} / \mathrm{div}$ through $20 \mathrm{v} /$ div positions have a gain of 122 .
(1) $\frac{6.1 \mathrm{v} / \mathrm{div}}{.05 \mathrm{v} / \mathrm{div}}=122$.
(2) or $A=9 \times 10^{-3} \times 13.5 \times 10^{3}=122$.
d. Channel 2 Input Amp in the X 10 position would increase these gain figures by a factor of 10 .

3. The Switching Logic circuit passes a current signal of $.45 \mathrm{ma} /$ DIV. a. Signal voltage at this point is in the microvolts range.
4. The Switching Multi switches the outputs from the Channel 1 and Channel 2 Input Amplifiers.
5. Five modes of operation may be selected by the MODE switch. a. ALT: The outputs from the two Input Amplifiers switch alternately at the end of each sweep.
b. $\quad \mathrm{CH}$ 1: The output from Channel 1 Input Amp is selected.
c. CH 2: The output from Channel 2 Input Amp is selected.
d. CHOPPED: Channel 1 and Channel 2 are switched at a 100 kc rate.
e. ALG ADD: The outputs of both channels are added algebraically.
6. A Chop Blanking signal is fed to the CRT Unblanking circuit to blank out chopped blanking switching transients .
7. The . $45 \mathrm{ma} /$ DIV current drive (per side) is amplified in the Driver stage (an operational amplifier) to a $1.9 \mathrm{ma} /$ DIV signal (per side) to drive the Output stage.
8. The signal passes through a 150 nsec delay line to the output stage .
9. The Output Amplifier converts the $1.9 \mathrm{ma} /$ DIV signal to a push-pull voltage swing of $6.1 \mathrm{v} /$ div to drive the CRT deflection plates.

## E. Switching Logic Gates

1. The Logic Gates consist of two sets of diodes in bridge configurations.
a. One bridge for Input Channel 1 and a bridge for Channel 2.
b. D201, D204, D205, D208 are 6185 silicon diodes.
c. D202, D203, D206, D207 are 6075 germanium diodes.


TYPE 422 VERTICAL SWITCHING \& OUTPUT AMPLIFIER B-422-00II SWITCHING GATES 1-15-65 ms
2. Switching voltage is supplied by the Switching multi .
a. The swittching voltage will swing from about lv positive to 2 v negative .
3. About 6 ma of static current flows through each of the diodes (D201, D204, D205, D208) in the signal path.
4. R215 (COMMON MODE CURRENT adj) is set to place the top of R213 and the bottom of R214 (Q224, Q234 bases) at . 6 v .
a. The $0 v$ adjustment is actually set at Q224, Q234 emitters .
b. This places Q224, Q234 bases at . 6v (a silicon junction above 0 v ).
c. The circuit input of the conducting channel would also be at 0 v (a silicon junction . 6 v down).
5. Assume that multi output $B$ is at lv and output $A$ is at -2 v .
a. D206 and D207 anodes, connected to lv, are lifted into conduction.
b. The 12 ma total static current and the signal current is diverted through D206 and D207 to the multi .
c. D205 and D208 cathodes are lifted to cut off.
d. Channel 2 is opened.
e. D202 and D203 anodes are pulled down to $-2 v$ cutting off the diodes.
f. D201 and D204 conduct with the 6 ma (each side) static current .
g. Channel 1 signal current is passed to the Driver Amplifier .
6. T201 and T202 provide a high impedance path for common mode AC signals.
a. Push-pull signals pass unimpeded.
b. The transformers consist of a twisted pair of wires fed through a ferrite bead.
F. Switching Multi, Alt Sweep Sync Amp and Chop Blanking Amp; Q265, Q275, Q283, Q264, Q294

1. The Switching Multi is a transistorized Eccles Jordan multivibrator that may be operated in either an astable or bistable mode.

2. Q265, Q275 and Q283 are 151-087, 1 N 1131 silicon PNP transistors.
a. Q264 and Q294 are 151-108, 2N2501 silicon NPN transistors.
3. D264, D274, D281 and D282 are 6185 silicon diodes.
4. In the ALT mode, the multi operates as a bistable multi.
a. A pulse arriving at the end of each sweep switches the multi.
b. Quiescently, Q264, the Alt Sync Pulse Amp, is cut off.
(1) Both the base and emitter are returned to ground.
c. Q265 and Q275 emitters are returned through D264 or D274 and R260 to $+12 v$.
5. Assume Q275 is conducting and Q265 is cut off.


TYPE 422 VERTICAL SWITCHING
B-422-0015 MULTI CURRENTS, ALT MODE
a. D274 will be conducting Q275 emitter current.
b. As a positive going sync pulse arrives, Q264 conducts for the pulse duration.
c. As Q264 conducts, all the current is robbed from D274 and Q275.
d. Q275 emitter current having been interrupted momentarily, Q275 cuts off.
e. As Q275 collector drops (to -2 v ), the negative step drops Q265 base .
f. For the sync pulse duration, the charge on C267 and C279 holds Q265 bias so Q265 will conduct, holding Q275 cut off.
(1) The time constant composed of R279, C279 holds Q265 base down until the initiating sync pulse has passed.
(2) The sync pulse has a duration of about $1 \mu \mathrm{sec}$ while the cross coupling network TC (R279, C279) is about $50 \mu \mathrm{sec}$.
6. Collector current for the CH 2 Paraphase Inverter is supplied through Q275 when CH 2 is cut off.
a. About 12 ma flows from D206, D207.
b. When conducting, total collector current for Q275 is about 19 ma .
7. Collector current for the CH 1 Paraphase Inverter is shunted through Q265 when the channel is cut off.
8. Q283 is an emitter follower connected in a DC feedback circuit whose purpose is to maintain the same voltage drops across the Gate diodes even though the DC level on the input buses might change.

a. Q283 base samples the voltage at Q224, Q234 emitters (nominally 0 v ).
b. The voltage level at Q283 base is stepped up one silicon junction to .6 v at the emitter and another .6 v to 1.2 v at D281 anode (assuming Q275 conducting).
c. This places D206, D207 anodes at 1.2 v above Q224, Q234 emitters.
d. Since Q224, Q234 bases will set . 6v above their emitters, D205, D208 anodes will set . 6 v below D206, D207 anodes.
e. In this condition, D206, D207 conduct with their cathodes one germanium junction below (.3v) their cathodes at .9 v .
f. D205 and D208 are reverse biased by . $3 v$ opening Channel 2.
g. Through DC feedback action, this relationship is maintained.
h. If the signal bus should rise one volt, all voltages in the loop would rise 1 volt.
i. Voltage drops would remain constant.
i. At the same time, D282 will be cut off (assuming Q265 cut off).
k. Current through R282 helps maintain the voltage at Q265 collector about 2 v below the level at Q224, Q234 emitters.
I. D201, D204 cathodes will be at the same level as Q224, Q234 emitters (one silicon junction voltage rise through the transistor and one silicon junction drop through the diode).
m. D202 and D203 will be reverse biased lv.
n. Channel 1 is connected.
9. In the CHOP mode, the multi becomes astable, running at $100 \mathrm{kc} \pm 20 \%$.
a. D264 and D274 are disconnected.
(1) Their anode supply is removed by the mode switch.
b. Emitter current for Q265, Q275 is supplied through R264 and R274 to $12 \mathrm{v}^{*}$.
10. Assume Q275 is conducting.
a. Voltage levels on Q275:
(1) Base, 2v.
(2) Emitter, 2.7v.
(3) Collector, 1.2v.
b. Voltage levels on Q265:
(1) Base, 4.8 v .
(2) Collector, -1.7 v .
(3) Emitter, increasing from .7 to +5.4 v .
c. As Q265 emitter reaches a point . 6 v more positive than its base, Q265 begins to conduct and the multi flips.
d. As Q275 cuts off, its collector drops $2.9 v$ (from 1.2 v to $-1.7 v)$.
(1) The collector is caught at -1.7 v by current through the cross coupling resistors and R281.
e. The 2.9 v negative step (coupled through C279) drops Q265 base to 2 v (from 4.8 v ).
(1) Q265 emitter follows the drop to 2.7 v .
f. As Q265 emitter drops, the negative going step is coupled through C267 to Q275 emitter.

(1) At the time the multi switched, C267 had a 2.7 v charge.
(2) The charge is maintained as Q275 emitter drops to .7 v .
g. Q275 is reverse biased about 4 v .
h. C267 begins to discharge toward $11 v$ ( 12 v decoupled).
i. In about $5 \mu \mathrm{sec}$, Q275 emitter will reach 5.4 v where the multi will switch again.
11. Currents switched by the multi in the CHOP mode are essentially the same as in the ALT mode.
12. Q294, the CHOP Blanking Amplifier, inverts and amplifies the CHOP switching transients to provide CHOP Blanking to the CRT.
a. Quiescently, the transistor is saturated with all elements at ground.
b. Each time the multi switches, a negative going pulse passes C266 and C276 to Q294 base .
c. Since a $2 v$ negative step appears on each emitter each time the multi switches, either C266 or C276 would pass the CHOP blanking pulse.
d. Two caps balance the capacitive load on the multi, however.

c. The pulse cuts off Q294 momentarily.
d. The result is an 8 ma positive going current pulse with a time constant of about $1 \mu \mathrm{sec}$.
(1) C266 and R291 determine the time constant.
e. The pulse is fed to the unblanking circuit to blank the CRT during the multi switching time.

13. In the CH 1 or CH 2 position of the Mode Switch, the Switching multi is turned off.
a. The Mode Switch opens the emitter supply to both transistors.
14. In CH 1 position, D206 and D207 anodes are connected through R273 (4302) to 11 v ( 12 v decoupled) .

a. The 12 ma from the CH 2 Paraphase Inverter is diverted through R273.
b. D205 and D208 are cut off opening Channel 2 signal path.
c. D202, D203 anodes are pulled down to $-2 v$, cutting them off.
d. D201 and D204 conduct, passing the Ch 1 signal current.
15. In the ALG ADD (Algebraically Added) position, the Switching multi is turned off by opening the emitter supply.
a. The anodes of all shunting diodes, D202, D203, D206 and D207 are tied to $-2 v$.

b. The shunting diodes are cut off.
c. Both Ch 1 and Ch 2 signal currents flow to the Driver Amplifier.
d. A total of 24 ma of static current ( 6 ma for each series diode) also flows through the Switching Gate.
e. Since no current is diverted by the shunting diodes, a circuit is required to dispose of the added 12 ma of static current.
f. The junction of R210 and R211 is tied through the Mode Switch to llv (12v decoupled).
g. 6 ma per resistor is shunted to the 12 v supply.
15. D210, D211 prevent the signal bus from dropping below -. 6 v .
a. During ALT switching, both sides of the multi are cut off simultaneously as the ALT Trace Sync pulse interupts multi emitter current.
b. For this brief period, 12 ma of static current per side flows through the diode gates (instead of 6 ma ).
c. As the bus drops to -.6 v , D210 and D211 conduct diverting the extra 6 ma to ground.
G. Driver Amplifier (Operational Amplifier); Q224, Q234

1. The Driver Amplifier provides a $X 4$ current gain.
a. Signal input is $.45 \mathrm{ma} /$ DIV.
b. Signal output is $1.8 \mathrm{ma} /$ DIV.
2. Q224 and Q234 are 151-127 silicon NPN transistors.
3. The circuit is an emitter coupled push-pull operational amplifier.
4. DC conditions, center screen:
a. Bases, . 6 v .
b. Emitters, 0 v .
c. Collectors, $3 v$ to 3.6 v , depending on setting of mode switch .
5. The COMMON MODE CURRENT control is adjusted so Q224 and Q234 emitters set at 0 v .

a. In practice, the level at the common emitters will be different with each Input Amplifier.
b. In this case, a compromise adjustment must be made with the emitters setting equally above and below 0 v .
6. D213 and D21.4 limit push-pull voltage excursion at Q224, Q234 bases to a total $\pm .6 \mathrm{v}$.
7. Static collector current in Q224 or Q234 is 15.1 ma.
a. 2.4 ma flows through feedback resistors, R221 and R224 (or R231, R234) .
b. This 2.4 ma plus 3.6 ma (each side) through the COMMON MODE CURRENT control makes up the 6 ma static current from the Input Amplifier's Paraphase Inverter .
c. About 17.6 ma of static current flows through each side of the delay line to the Output Amplifier .
8. The delay line is a counter-spiral wound 150 nsec line of the type used in the Type 647.
a. It is unshielded, thereby increasing the impedance to about $100 \Omega$, each side.
(1) The lack of shielding does introduce a 30 mc wrinkle.
(2) The wrinkle does not appear on the CRT, however, because of the instrument's bandpass limitation.
b. R226 (or R236) plus the Operational Amplifier output Z provides the $100 \Omega$ input termination for the delay line.
c. R239, C239 provides AC reverse termination for the delay line.
(1) The Operational Amplifier output appears inductive as the frequency increases.
(2) The RC network compensates for the inductive output, and provides a constant delay line termination.
9. Three RC networks tapped off the feedback resistors compensate for various high frequency losses in the amplifier and delay line.
a. The RC networks reduce feedback at higher frequencies, thereby increasing gain at those frequencies.
b. Time constants are staggered.
c. R237 and C237, DELAY LINE COMP, shapes the leading corner of a unit step as it passes the delay line.
10. A Trigger Takeoff circuit provides a single-ended trigger signal for the CH 1 and 2 INT position of the TRIG SOURCE switch.
a. R217 is $R_{i}$ for the Operational Amplifier on the Trigger Amp.
b. C217 provides high frequency peaking.
c. Signal voltage at Q224 collector is about $360 \mathrm{mv} /$ DIV compared to 45 mv /DIV at the CH 1 Trigger Takeoff.
(1) The $\mathrm{R}_{\mathrm{i}}$ for the CH 1 takeoff is one-tenth the value of R217 to help compensate for the difference in signal level.
11. R235, C235 provide a balance for the load of the Trigger Takeoff.
H. Output Amplifier; Q244, Q254
12. The Output Amplifier is a push-pull grounded base stage that provides drive to the CRT Vertical deflection plates.
13. The stage provides a signal current to signal voltage transfer. a. Transimpedance is 3.4 k .
b. $T_{Z}=\frac{e_{\text {out }}}{i_{\text {in }}}$
c. $T_{Z}=\frac{6.1 \mathrm{~V} / \mathrm{DIV}}{1.8 \mathrm{ma} / \mathrm{DIV}}$
d. Push-pull output voltage for 6 cm is 36.6 v .
14. Q244 and Q254 are 151-121, 2N3118 silicon NPN power transistors.
a. The transistors are mounted in beryllium oxide heat sinks.
15. DC levels, center screen:
a. Bases, 7.35v.
b. Emitters, 6.8v.
c. Collectors, $34 \mathrm{v}^{*}$.


TYPE 422 VERTICAL AMPLIFIER
B-422-0013 OUTPUT AMPLIFIER

1-18-'65 ms
5. R242 (and R252) and transistor, $R_{e}$, provide delay line termination.
6. C242 (and C252) compensate for an inductive $r_{e}$ at higher frequencies.

* Assuming the 55 v supply is 55 v . This is an unregulated supply and will appear at 55 v at low line ( 103.5 v ) and 66 v at high line ( 126.5 v ). As much as 1.8 v of 120 cycle ripple may be present on the 55 v supply.

7. The Driver Amplifier supplies $\mathbf{1 7 . 7} \mathbf{~ m a}$ of static current per side.
a. R241 (and R251) draws 5.1 ma .
b. About 12.5 ma is required in each output transistor.
c. The 12.5 ma through the collector load resistors places the center screen deflection plate voltage at $34 \mathrm{v}^{*}$.
8. C247 and C257 provide an AC current return for Q244 and Q254 bases.
a. The transistors bases are separated by lead inductance so a cap at each emitter is required.
9. L245 (and L255) provide peaking in response to deflection plate capacitance.
a. Deflection plate $C$ is about 4.5 pf .
b. The inductance in $T$ coil configuration to present a resistive load $=R^{2} C$.
(1) $R$ is R244 and R245, $1690 \Omega$.
(2) C is the deflection plate capacitance, 4.5 pf .
(3) $L=13 \mu h$.
10. The Output circuit is 3 db down at 16.2 mc .
a. Risetime of the Output Amplifier is 20.6 nsec .
(1) $t_{r}=2.2 R C$.
(2) $R=1690 \Omega$, $R 244, ~ R 245$.
(3) $\mathrm{C}=5.5 \mathrm{pf}, 4.5 \mathrm{pf} \mathrm{C}_{\mathrm{OB}}$ plus 1 pf stray C .
b. Risetime of the T coil circuit is 6.5 nsec .
(1) $t_{r}=\frac{2.2 R C}{K}$.
(2) $R=1690 \Omega$.
(3) $\mathrm{C}=4.5 \mathrm{pf}$ deflection plate C .
(4) $K=2.6$, bandwidth improvement as result of $T$ coil.
c. $\quad t_{r}$ of output, 21.6 nsec .
(1) $t_{r}$ output $=\sqrt{\left(6.5 \times 10^{-9}\right)^{2}+\left(20.6 \times 10^{-9}\right)^{2}}$.

## V. SWEEP TRIGGER

A. The Sweep Trigger circuits provide a waveform of uniform shape and polarity to trigger the Sweep Generator.
B. Circuits that comprise the Trigger Generator:

1. Trigger Source and Coupling Selector circuits.
2. Operational Amplifier; Q323, Q324.
3. Trigger Generator; Q364, D375.
4. AUTO circuit, Q343.
C. Block Diagram


TYPE 422 SWEEP TRIGGER

## D. Block Logic

1. Triggering sources available:*
a. EXT.
b. CH I only.
c. CH 1 and CH 2 .
2. Trigger Coupling:
a. $A C$.
b. $A C$ LF REJ.
c. DC.
3. Triggering Modes:
a. AUTO.
b. TRIGGERED.
4. Trigger Sensitivities:
a. INT.
(1) $D C, .2$ div to 5 mc increasing to 1 div at 15 mc .
(2) $A C$ LF REJ, 2 div from 50 kc to 5 mc , increasing to 1 div at 15 mc . Low frequency response $30 \%$ down at $\approx 25 \mathrm{kc}$.
(3) $\mathrm{AC}, .2$ div from 50 cps to 5 mc , increasing to 1 div at 15 mc . Low frequency response is spec'd at $30 \%$ down at $\approx 25 \mathrm{cps}$.
(4) AUTO, . 8 div from 50 cps to 4 mc , increasing to 2.5 div at 15 mc .
b. EXT:
(1) $D C, 125 \mathrm{mv}$ to 5 mc , increasing to .5 v at 15 mc .
(2) AC LF REJ, 125 mv from 5 kc to 5 mc , increasing to .6 v at 15 mc .
(3) $\mathrm{AC}, 125 \mathrm{mv}$ from 50 cps to 5 mc , increasing to .5 v at 15 mc . Low frequency response $30 \%$ down at $\approx 25 \mathrm{cps}$.
(4) AUTO, .5 v from 50 cps to 7 mc , increasing to 1.2 v at 15 mc 。
c. EXT trigger limits .
(1) AC and AC LF REJ, DC not to exceed 250 v plus 100 v RMS.
(2) DC, 100v RMS. Peaks not to exceed 250 v 。
d. EXT trigger input $Z$.
(1) 100 k paralleled by 35 pf .
e. Triggering within range of the (TRIGGERING) LEVEL control; $\pm 10 \mathrm{v}$.
5. After source and coupling selection, the trigger signal is amplified and inverted in the operational amplifier.
6. A diode limiting circuit limits the output from the operational amplifier to about $\pm .3 \mathrm{v}$ peak-to-peak for small signals and $\pm 1 \mathrm{v}$ for $\pm 10 \mathrm{v}$ signals.
7. The Trigger Generator circuit uses a TD and a transistor that acts as a current switch.
8. When a trigger signal causes the Trigger Generator input to pass through zero volts, the TD switches to its high state.
a. A (TRIGGERING) LEVEL control provides an offset voltage at the Trigger Generator input so that any portion of a triggering waveform may be made to trigger the sweep.
b. A SLOPE switch determines whether the positive or negative slope will provide the trigger.
9. When the TD switches, a trigger of uniform height and shape is fed to the Sweep Generator .
a. The trigger is a 2 to 3 ma current pulse about 15 nsec wide.
10. The AUTO circuit operates at about 50 cps to provide a trace in the absence of triggers (the sweep is triggered by the AUTO circuit at a 50 cps rate).
a. When triggers are applied, the circuit automatically recognizes the triggers and ceases to operate at a 50 cps rate.

## E. Trigger Source and Coupling

1. The Source switch selects either EXT, CH 1\& CH 2, or CH 1 . only inputs.
a. The inputs are grounded when not in use.
2. The coupling switch selects AC, AC LF REJ, or DC.

3. Switching is done at a relatively low impedance point at the input to the Operational Amplifier.
a. R302 is $R_{i}$ for the EXT input.
b. R217 (Vertical Driver Amplifier) is $\mathrm{R}_{\mathrm{i}}$ for the CH 1 and CH 2 input.
c. R54 (CH 1 Input Amplifier) is $\mathrm{R}_{\mathbf{i}}$ for the CH 1 input .
d. $\quad R_{i}$ values are different to compensate for different trigger signal levels*.
4. All three $R_{i}$ resistors are compensated.
a. It is important for good transient response that the time constant of the $R_{i}$ 's and $R_{f}$ 's be the same.
b. The CH $1 \mathrm{R}_{\mathrm{i}}$ compensation (C54) is fixed.
c. All other $R_{i}$ and $R_{f}$ compensations are matched to the CH 1 input, R54, C54.
5. In AC coupled position, the low frequency response is 3 db down at about 25 cps .
a. C306 (AC coupling for CH 1 and CH 2 and EXT trigger) is . $1 \mu \mathrm{f}$ while C309 (AC coupling for CH 1 ) is $1 \mu \mathrm{f}$.
b. The $R_{i}$ - coupling cap products must be the same for each input if the inputs are to have the same LF cut-off point.
c. Calculated LF response is 3 db down at 23.4 cps for INT and 16 cps EXT.
6. In the AC LF REJ position, the low frequency response is 3 db down at 23.4 kc .
a. C305 is one-tenth the value of C308 to match the $\mathrm{R}_{\mathrm{i}}$ values for CH 1 and $\mathrm{CH} 1 \& \mathrm{CH} 2$.
b. EXT input is a compromise, using C305 with a low frequency cut-off of 16 kc .
7. In AUTO triggering, a switch on the (TRIGGERING) LEVEL control opens, providing mandatory AC coupling.
a. AC or AC LF REJ is available.
F. Operational Amplifier; Q323, Q324
8. The Operational Amplifier provides gain and signal polarity reversal to the trigger signal to drive the Trigger Generator circuit.

9. The circuit uses two transistors, six diodes, and a zener diode. a. Q323 is a 151-133, MM999 silicon PNP transistor.
b. Q324 is a 151-108, 2N2501 silicon NPN transistor.
c. D318, D319 and D334 are IN3605 silicon diodes.
d. D332 and D333 are 6075 germanium diodes.
e. D325 is a $3 v$ zener diode.
10. D318 and D319 protect Q323 against damage from very large EXT input voltages.
11. The two stage amplifier has an open loop gain of about 100.
12. Closed loop gain of the amplifier will differ with the different inputs as different values of $R_{i}$ are switched in.
a. Gain is further reduced by a limiting circuit as trigger signals at the Operational Amplifier output exceed $\pm .2 \mathrm{v}$.
b. The limiting circuit increases negative feedback until a $\pm .5$ signal (at the Operational Amplifier output) will be attenuated about 10:1 (over small signal gain).
c. The trigger circuit can be said to have a "window" for small signals.
13. Gain under small signal conditions (below $\pm .2 \mathrm{v}$ at the Operational Amplifier output).
a. Since the Operational Amplifier has relatively low gain, $R_{f}$ and $R_{i}$ must be modified* from the conventional expression, $A=\frac{R_{f}}{R_{i}}$.
b. If the amplifier has an open loop gain of 100, the input signal (Q323 base) will be $1 / 100$ the amplitude of the output (Q324 collector).
c. The Operational Amplifier, therefore, has an input impedance approximately equal to $1 / 100$ the value of $R_{f}$ (R353).


TYPE 422 SWEEP TRIGGER
B-422-0025
OPERATIONAL AMPLIFIER SMALL SIGNAL CONDITIONS
2-6-65 ms
(1) Input $Z=\frac{R_{f}}{1-A}$

$$
\begin{aligned}
& Z=\frac{200 k}{101} \\
& Z \approx 2 k
\end{aligned}
$$

d. A phantom ground can be said to exist at a point $2 k$ along $R_{f}$.
e. $\quad R_{f}$ is effectively decreased by $2 k$ while $R_{i}$ is increased by the same amount.
f. The limiting circuit places an equivalent $5 k$ to ground from Q323 base.
(1) R332 in parallel with R333 through conducting D332 and D333 to ground.
g. Since signal current will flow through the circuit's input $Z$ of 2 k and through the 5 k shunt to ground, gain of the amplifier is modified by $5 / 7$.
h. Gain of the amplifier in the CH 1 input position is 16 .
(1) $A=\frac{R_{f}-2 k}{R_{i}+2 k} \times \frac{5}{7}$
(2) $A=\frac{198 \mathrm{k}}{8.81 \mathrm{k}} \times \frac{5}{7}$
(3) $A=16$.
i. Gain of the amplifier in the CH 1 and CH 2 position is 2 .
(1) $\mathrm{A}=\frac{198 \mathrm{k}}{70.1 \mathrm{k}} \times \frac{5}{7}$
(2) $A=2$
i. Gain of the amplifier in the EXT position is 1.4.
(1) $A=\frac{198 k}{102 k} \times \frac{5}{7}$
(2) $A=1.4$
$k$. The various gain figures together with the different trigger signal levels at the inputs provide near equal signal levels at the Operational Amplifier output .

1. Signal levels at Operational Amplifier output for minimum triggerable CH 1 signals is 144 mv .
(1) $e_{o}=e_{i} \times A$.
(2) CH 1 signal level is $45 \mathrm{mv} /$ DIV.
(3) Minimum triggerable signal is . 2 DIV.
(4) Minimum signal is 9 mv .
(5) $e_{o}=9 \mathrm{mv} \times 16$.
(6) $e_{o}=144 \mathrm{mv}$.
m. Operational Amplifier output signal for minimum triggerable CH 1 and CH 2 signal is also 144 mv .
(1) CH 1 and CH 2 signal level is $370 \mathrm{mv} /$ DIV.
(2) Minimum triggerable signal is . 2 DIV.
(3) Minimum signal is 72 mv .
(4) $e_{o}=72 \mathrm{mv} \times 2=144 \mathrm{mv}$.
n. The output signal level for a minimum triggerable EXT signal is:
(1) Minimum EXT signal level is 125 mv .
(2) $e_{o}=125 \mathrm{mv} \times 1.4$.
(3) $e_{o}=175 \mathrm{mv}$.
o. From the above comparison it appears that the circuit could trigger on an EXT signal of 100 mv .
2. Under small signal conditions, D332 and D333 (in the limiter circuit) conduct about 1 ma each.
a. D331 anode is clamped at about. 3 v and D334 cathode is clamped at -.3 v .
b. No negative feedback occurs.
3. As signal amplitude increases, D331 and D334 must conduct 1 ma each in order to cut off D332 and D333.
a. This condition is not achieved simultaneously, however, as a negative excursion will cut off D332 and a positive signal excursion will cut off D333.
b. When either D332 or D333 is completely cut off, $R_{f}$ becomes 10k (in parallel with 200k, R353).
c. This reduces amplifier gain by about 10:1.
d. The result is a limiting action that will allow a maximum output excursion (operational amplifier output) of about $\pm 1 \mathrm{v}$ with a $\pm 10 \mathrm{v}$ input.
4. D325 sets the level at the Operational Amplifier output so the signal will swing around 0 v with the (TRIGGERING) LEVEL control centered.
a. A trigger is generated wherever the signal passes through zero.
5. The (TRIGGERING) LEVEL control can set the Operational Amplifier output level so any portion of the trigger signal can be made to generate a trigger pulse.
a. R357 constitutes an $\mathrm{R}_{\mathbf{i}}$.
b. The control has a range of $\pm 12 \mathrm{v}$ at the control arm.
c. Heavy feedback through the limiter circuit reduces this swing to $\pm 1.3 \mathrm{v}$ at the Operational Amplifier output.
d. An external trigger of $\pm 10 \mathrm{v}$ can be accommodated by the (TRIG GERING) LEVEL control .
6. Both feedback loops are compensated to match the time constant of the $R_{i}$ compensation networks.
a. The time constant of each $R_{i}$ and $R_{f} R C$ network is about 350 nsec.
b. C353 is adjustable to compensate R353 setting proper feedback time constant.
c. C332 compensates R332.
d. C333 compensates R333.
G. AUTO Circuit, Q343
7. The AUTO circuit supplies a trigger 50 times per second to drive the Sweep Generator at a 50 cycle rate .
a. The result is a reference trace on the screen in the absence of triggers .
b. When triggers of sufficient amplitude arrive, the AUTO circuit drops out allowing the Sweep to operate as a triggered sweep.
c. The (TRIGGERING) LEVEL control is switched out of the circuit in the AUTO mode .

8. When the AUTO circuit is switched in, the Operational

Amplifier becomes a phase-shift oscillator*.
a. Emitter follower, Q343, drives the phase shift network composed of R344, C344, R345, C345, R346, C346 and R347.
b. The phase shift network will shift a 50 cycle signal $180^{\circ}$.
c. Since harmonics are greatly attenuated in the phase shift network, the result is a sine wave output (from the Operational Amplifier) at approximately 50 cps .
d. Since the 50 cycle sine wave returned to Q323 base is in proper phase to sustain oscillation, the path through the AUTO circuit can be considered positive feedback.
e. The Operational Amplifier output swings about 500 mv peak-to-peak**.
f. The sine wave is flattened by action of the limiter circuit.
3. The phase shift network is frequency discriminating.
a. A trigger signal of a much higher frequency (than 50 cps ) could not pass the network.
b. A lower frequency trigger signal could pass the network, but would have to be in phase with the AUTO circuit in order to constitute positive feedback.
(1) A sine wave of 50 cycles could synchronize the phase shift oscillator, however.

* See Radio Engineers Handbook, Terman, Page 506.
** This sine wave amplitude depends on the characteristics of the diodes in the limiting circuit and may vary from 400 to 800 mv .
c. In general, therefore, only the 50 cycles from the phase shift oscillator can be fed back as positive feedback.

4. In the absence of trigger signals, the 50 cycle sine wave is fed back as positive feedback through the phase shift network and on peaks as negative feedback through the limiting circuit.
5. Consider a hypothetical situation where the two feedback paths are present at 50 cps .


TYPE 422 SWEEP TRIGGER
B-422-0026
AUTO CIRCUIT BLOCK
a. Amplifier A has a gain of 100 at $180^{\circ}$.
b. Feedback path $Z_{1}$ has a gain of .02 at $0^{\circ}$.
(1) Feedback path $Z_{1}$ functions only during the 50 cps peaks.
(2) The gain figure, therefore, is average gain.
c. Feedback path $Z_{2}$ has a gain of .03 at $180^{\circ}$.
d. Conditions for oscillation are satisfied when $K \beta=110^{\circ}$.
(1) Where $K=$ the amplifier gain of 100 .
(2) $\beta=$ total net feedback.
e. In the above illustration:
(1) $100 \underline{180^{\circ}}\left(.03 \underline{180^{\circ}}-.02 \underline{0^{\circ}}\right)=1$.
(2) $100 \underline{180}^{\circ} \times .01 \quad \underline{180^{\circ}}=1$.
f. $k \beta=1$; therefore, the circuit oscillates.
6. As a trigger signal is introduced it cannot pass through the frequency discriminating positive feedback path.
a. The trigger signal can pass through the negative feedback path, however.
7. When a small trigger signal is introduced, the signal at the Operational Amplifier output is a composite of the trigger and the 50 cycle signal (see page $5-16$, illustration $B$ ).
a. Although the trigger signal has been added, the action of the limiting circuit keeps the composite signal at the same level.
b. The 50 cycle component, as fed back through the phase shift network, is decreased in amplitude.
8. As the trigger signal is increased in amplitude and the output composite signal remains the same, the 50 cycle component becomes too small to sustain oscillation.
a. K $K$ is less than 1-- oscillation ceases.
b. Only the trigger signal is left to switch the TD.
9. Normally the trigger must be of sufficient amplitude to stop 50 cycle oscillation before stable triggering can occur.




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A Q364 BASE
JUNCTION R347, C346 TUNNEL DIODE CATHODE

INADEQUATE INPUT TRIGGER

B
Q364 BASE JUNCTION R347, C346 TUNNEL DIODE CATHODE

C
ADEQUATE INPUT TRIGGER
Q364 BASE JUNCTION R347, C346

TUNNEL DIODE CATHODE
a. Stable triggering may occur with smaller trigger signals if the signal is a harmonic of the 50 cycle auto signal.
b. The required trigger amplitude is spec'd at .8 div from 50 cps to 4 mc increasing to 2.5 div at 15 mc .
10. When the trigger signal drops below that required for stable triggering the oscillator again begins to function. The scope displays the reference trace.
11. The waveforms above illustrate the operation of the AUTO circuit.
a. Illustration A shows conditions with no trigger input .
(1) Note the TD switches as the sine wave at Q364 base passes through zero.
(2) The 50 cps signal at Q364 base is distorted by the action of the limiter circuit.
(3) The sine wave at the junction of R347, C346 (positive feedback) is sinusoidal (harmonics cannot pass the network), attenuated about $80: 1$ and phase shifted $180^{\circ}$ 。
b. Illustration $B$ shows conditions with a small trigger signal (1 kc calibrator).
(1) The waveform at Q364 base includes both 50 cps and trigger signal.
(2) The 50 cps sine wave at the junction of R347, C346 is reduced in amplitude.
(3) The TD switches only when the composite trigger and 50 cps signal passes through zero.
(4) Triggering is erratic.
c. Illustration $C$ shows a condition when a slightly higher trigger signal is applied.
(1) The oscillator has dropped out; the signal at the junction of R347, C346 is zero.
(2) The signal at Q364 base consists of the trigger signal .
(3) The TD switches with each trigger.
(4) Triggering is stable.
12. D343 provides temperature compensation for Q343 base-emitter junction.
13. The AUTO CENTER control (R350) is adjusted so the 50 cps AUTO signal at Q364 base is centered at zero volts.
a. R349 is $R_{i}$ to the Operational Amplifier.
H. Trigger Generator; Q364, D375

1. The Trigger Generator provides a trigger of uniform shape and amplitude to trigger the Sweep Generator .
a. A SLOPE switch determines whether the plus $\qquad$ or minus ( $\underbrace{}_{\text {) slope will generate a trigger. }}$

2. The circuit uses one transistor, a TD, a signal diode, and a zener diode.
a. Q364 is a 151-108, 2N2501 silicon NPN transistor.
b. D375 is a TD4A, 10 ma tunnel diode.
c. D363 is a 3605 silicon diode.
d. D364 is a 1N753A, 6.2 v zener diode.
3. When the TRIGGERING LEVEL or AUTO LEVEL is properly adjusted, the TD will switch when the trigger signal at Q364 base passes through zero.
a. Since the trigger is inverted in the Operational Amplifier, a plus slope at Q364 base is required when the SLOPE switch is set to minus slope .
4. Operation in the minus slope position of the SLOPE switch. a. D375 anode is clamped at 6.2 v by the zener, D364.

(1) 10 ma to 18 ma through the zener assures a solid 6.2 v supply.
b. 6 ma flows through R374.
c. Q364 collector is tied to the TD cathode so any collector current must pass through the TD circuit.
d. When Q364 is cut off, R377 (the TD load resistor) forms load line $A$ on the TD curve.
e. When Q364 base is at zero volts, about 8.8 ma flows through R363.
(1) Since Q364 and D363 are both silicon junctions, about half the current would flow through D363 and half through Q364.
(2) In practice the junctions may not be exactly equal and a few millivolts either side of zero at Q364 base may be necessary for balanced currents .
f. 4.4 ma through Q364 plus the 6 ma through R374 move the TD load line to position $B$ on the TD curve.
g. Load line B places the TD in the center of the hysteresis region of its bistable configuration.
h. As the signal on Q364 base passes zero volts (moving in a positive direction), Q364 emitter will lift, cutting off D363.
i. As D363 cuts off its current is diverted through Q364 and the TD circuit.
(1) The load line moves to position $D$ (or beyond).
j. The increased current switches the TD to its high state, following AC load line $C$.
(1) The inductance of L377 momentarily removes R377 as a load, leaving R374 to form load line C.
k. The positive going current pulse is formed in T401 secondary .
5. If the trigger signal is of long duration, the TD will remain in its high state held by the bistable load line $D$.
m. As the trigger signal swings Q364 base back through zero volts, D363 conducts, robbing current from Q364.
n. The TD, now operating along load line A, switches to its low state.
o. Hysteresis of the circuit at Q364 base is about 35 mv .
6. Operation in the plus slope position of the SLOPE switch.

a. The TD cathode is tied to the 6.2 v zener supply. (1) 6 ma to 15 ma assures zener operation of D364.
b. Q364 is conducting (D363 cut off); 8.8 ma flows through Q364.
(1) 15 ma flows through R372.
(2) 6 ma flows through TD circuit (load line A).
c. When the trigger signal moves Q364 base to zero volts, collector current reduces to 4.4 ma , moving the TD load line to position B.
d. As the trigger signal drops Q364 base below zero, D363 conducts, reducing Q364 collector current.
e. The increased current through the TD circuit switches the TD to its high state developing the Sweep Trigger pulse.
f. The circuit resets as the trigger signal swings Q364 base back through zero.
7. When triggering on fast signals, the trigger circuit begins to count down at about 4 mc .
a. Count down is a function of $L / R$ time of $L 377, R 377$ and of signal amplitude.
b. After the TD has switched to its high state, the $L / R$ time delays the return to the low state, and again delays the increase in TD current sufficient to flip it to its high state.
c. Since more than one cycle of trigger may occur during the delay, the TD will switch at a sub-multiple of the trigger frequency.
8. The output is a positive going current pulse with a risetime of about 10 nsec (duration 15 nsec ).
a. The pulse is about 5 ma into the transformer.
b. It pulls 2 to 3 ma out of the Sweep Gating TD.
(1) T401 has 2:1 current step down.

## VI. SWEEP GENERATOR

A. The Sweep Generator develops a 3lv positive going linear sweep ramp to drive the Horizontal Amplifier .

1. A Gate Out waveform is provided at a front panel jack.
2. A waveform is generated to unblank the CRT during sweep.
B. Block Diagram


TYPE 422 SWEEP GENERATOR
B-422-0028 BLOCK DIAGRAM

2-15-65 ms
C. Circuits that comprise the Sweep Generator:

1. Sweep Gating Circuits; D405, Q414, Q424, Q429.
2. Miller Integrator; V443, Q441.
3. Sweep Terminating Amplifier; Q464, D455.
4. Sweep Start Locating Amplifier, Q434.
5. Trigger Lockout Circuit.
6. Gate and Unblanking EF, Q473.
D. Inputs
7. A 2 to 3 ma current trigger pulse, about 15 nsec wide from the Sweep Trigger circuit.
E. Outputs
8. The 3lv peak-to-peak positive going linear sweep ramp to the Horizontal Amplifier.
a. The ramp runs from 3 v to 34 v .
b. The fastest free-running sweep rate is about 100 kc .
9. Gate out waveform:
a. The gate out is a negative going 600 mv waveform.
b. The waveform starts at 0 volts and drops to -600 mv for
the duration of the sweep.
10. An unblanking waveform is developed to unblank the CRT during sweep.
a. This is a negative going 5.2 ma current waveform.
F. Block Logic
11. Prior to sweep, the circuit output is clamped at $3 v$ by the Sweep Start Locating transistor, Q434 base-emitter junction.
12. The Sweep Gating TD (D405) is in its low state .
13. Arrival of a trigger switches the TD to its high state.
14. The positive step generated by the TD is amplified and inverted in the Sweep Gating circuit to drop the anode of the disconnect diode (D439).
15. As the disconnect diode cuts off, the Miller Integrator begins to run up.
a. The sweep ramp is fed to the Horizontal Amplifier and is fed back to the Sweep Terminating Amplifier.
16. When the sweep ramp has reached $34 v$, the Sweep Terminating Amplifier robs current from the Sweep Gating TD and it switches to its low state.
17. During sweep, retrace, and an additional $5 \mu \mathrm{sec}$, a lockout pulse is fed back to the Sweep Gating circuit input to prevent the arrival of triggers (trigger lockout circuit).
18. A new sweep cannot start, therefore, until $5 \mu \mathrm{sec}$ after the end of retrace.
19. Provisions are made to free run the sweep.
a. When the TRIGGER LEVEL control is rotated full clockwise, the FREE RUN switch is activated.
20. The negative going rectangular waveform out of the Sweep Gating circuit is fed to the Unblanking and Gate Out EF where it becomes the Unblanking pulse and the Gate Out waveform.
a. The same waveform is fed to the Vertical Switching circuit as the Alt Trace Sync Pulse.
21. The TIMING SWITCH changes timing capacitors and timing resistors to provide the 19 TIME position from $.5 \mu \mathrm{sec} /$ DIV to $.5 \mathrm{sec} /$ DIV.
G. Sweep Gating Circuit; D405, Q414, Q424, Q429; and Sweep Start Locating Amplifier, Q434
22. The circuit develops a negative going step that disconnects D439 and starts sweep.
23. Four transistors, a tunnel diode, and five small signal diodes are used.

a. D405 is a 152-081, 1 N3714, 2.2 ma tunnel diode.
b. Q414 is a 151-108, 2N2601 NPN silicon transistor.
c. Q424 and Q434 are 151-133, MM999 PNP silicon transistors.
d. Q429 is a 151-157, RCA 40232 NPN silicon transistor .
e. D438, D435, D436 and D401 are 6185 silicon diodes.
f. D439 is a 151-173 silicon diode selected from 1N3605.
24. Prior to sweep, D405 is in its low state.
a. 1.26 ma is drawn from the sweep Terminating Amplifier and about . 4 ma through D401.
b. The Sweep Terminating Amplifier output sets at 6 v .
c. Q414 is cut off.
(1) The collector sets at 4.2 v 。
d. Q424 is conducting, with its collector at about ground.
e. D429 is conducting.
f. Q434 and D430 are conducting holding the sweep output at 3 v 。
(1) Q434 collector is held at. 5 v by D435 and D436.
g. D401 is conducting about . 4 ma.

(1) The trigger lockout circuit holds D401 anode (through T401 secondary) at 500 mv .
(2) The TD (D405) in its low state has about 50 mv across it.
(3) D401, therefore, is forward biased about 450 mv .
25. The arrival of a trigger switches the TD (D405) to its high state.
a. The trigger current pulse is formed in T401.
(1) T401 is trifilar wound of 4 turns each on a ferrite core.
(2) Two windings are connected in series to form an 8 turn secondary.
(3) C401 provides a ground for the transformer secondary.
b. The 2 ma trigger through D401 when added to the 1.7 ma quiescent TD current is enough to switch it to its high state.
c. D405 anode rises to 450 mv and Q414 saturates.
d. The TD load resistance is now composed of R405 (300 ) and the few ohms of Q414 base impedance.
(1) The load resistance places the TD in a bistable configuration.
(2) The 1.3 ma quiescent current from the Sweep Terminating Amplifier will hold the TD in its high state.
26. When the TD switches, Q414 saturates and its collector drops to ground (from 4.2v).
a. The negative step passes through C418 to disconnect D439 and start the sweep run up.
(1) R414 allows Q414 collector to drop rapidly.
b. The negative step cuts off Q424; its collector drops toward -12 v , but is caught by D438 at -2.5 v .
(1) D439, having been cut off by the initial step through C418, is now held cut off with its anode at -2.5 v .
(2) Q424 emitter drops from 4.2 v to 3 v .
(3) Q424 base is set solidly at 3.6 v by the voltage regulator transistor, Q429.
c. Q434 also cuts off.
(1) Its emitter drops from 4.2 v to 3 v .
(2) D430 disconnects as the emitter step is conducted through R433 and the sweep begins its run up.
(3) The collector drops toward -12 v from .5 v .
d. As Q434 collector drops, D435 and D436 cut off.
(1) Q434 collector can drop only as fast as C401 and C432 can discharge.
(2) The initial drop, however, cuts off D401.
(3) Triggers cannot pass -- the trigger lockout is functioning.
27. The Miller Integrator Ramp runs up.
a. The ramp output is fed back to the Sweep Terminating Amplifier.
28. When the output ramp reaches 34 v , the Sweep Terminating Amplifier output drops to zero volts (from 6v).
a. The current demand from the TD (D405) drops to zero.
29. The TD, robbed of its 1.3 ma , switches to its low state.
a. The anode drops to 50 mv .
b. Q414 cuts off.
c. As its collector rises, it pulls up on Q424 and Q434 emitters (to 4.2 v ).
d. Q424 turns on; its collector pulls up to ground.
e. D439 connects, terminating sweep and beginning retrace.
f. Q434 is merely enabled, since D430 remains cut off for the duration of retrace.
(1) At the fastest sweep rates, retrace will couple through D430 capacitance to Q434 base .
(2) . Q434 will begin to conduct slightly -- its collector will begin to rise during retrace.
30. At the end of retrace the Sweep Terminating Amplifier output again raises to 6 v .
a. The 1.3 ma through D405 enables the TD.
(1) D401 is cut off, however, so triggers are still locked out .
31. When retrace has dropped D430 cathode to about 3 v , D430 conducts establishing the sweep starting point at $3 v$.
32. As D430 conducts, Q434 turns on.
a. Q434 collector rises exponentially as C401 and C432 charge .
(1) About $5 \mu \mathrm{sec}$ is required for C401 and C432 to charge.
(2) The $5 \mu \mathrm{sec} *$ constitutes hold-off.
b. When Q434 collector reaches 500 mv , D435 and D436
conduct, clamping the Trigger Lockout bus at this level.

[^0]12. D401 can now pass triggers to start a new sweep.
13. The sweep cycle is complete.
14. L423, R423 and R425, C425 prevent an oscillation at the end of retrace .
15. R432, C432 increase hold-off time at slow sweep speeds.
16. Regulator transistor, Q429 (through Q424, Q434) provides a constant starting voltage for the sweep.
a. Without Q429, varying timing resistor currents and timing capacitor currents during retrace could move Q434 emitter voltage and the sweep starting point.
H. Miller Integrator; V443, Q441


1. The Miller Integrator produces the 31v positive going linear sweep ramp.
a. The ramp runs from $3 v$ to $34 v$ at Q441 collector .
2. The circuit uses a nuvistor, a transistor and two diodes.
a. V443 is a 8393 nuvistor.
b. Q441 is a 151-103, 2N2219 (with relaxed specs) NPN silicon transistor.
c. D439 is a 152-173 low leakage silicon diode.
d. D430 is a 6185 silicon diode .
3. Basically, the circuit is the familiar Miller Integrator.
a. Timing caps and timing resistors are switched in to provide the 19 timing ranges.
b. The ramp output is taken from Q441 collector to drive the Horizontal Amplifier and to feed back through the Sweep Terminating circuit.
c. Ramp linearity is about $0.075 \%--60 \mathrm{mv}$ change at the top of $R_{T}$ out of 80 v across it.
4. A nuvistor is used to keep leakage currents to the timing capacitor down, and a transistor is used as the gain stage.
a. The nuvistor has 2-3 nanoamps leakage current.
b. The timing capacitor (TEK made) has a leakage of about .5 namp and the low leakage diode contributes about 15 nanoamps at 5 v .
(1) At . $5 \mathrm{sec} /$ DIV, about $5.5 \mu \mathrm{a}$ flows in the timing resistor.
(2) 20 nanoamps would contribute about $.4 \%$ timing error .
c. Q441 provides a gain of 200 to 500 .
5. Prior to sweep, V443 grid rests at -800 mv nominally.
a. This level is established by Q441 base-emitter junction and V443 bias.
(1) Bias may vary with different Gm nuvistors.
b. The output at $3 v$ is set by the Starting Locating Amplifier through D430.
(1) Current path is through Q441 and D430 to the Start Locating Amplifier.
6. D439 is disconnected when the Sweep Gate drops the anode to -2.5 v 。

Trigger

Q424 Collector

V443 Grid

Q441 Collector

a. Timing resistor current previously flowing through D439 is diverted to the timing capacitor .
b. The timing capacitor begins to charge .
c. V443 grid begins to fall toward -81 l .
d. The cathode follows, driving Q441 base.
e. The voltage change applied to Q441 base is amplified and inverted in the transistor.
f. The output ramp begins its run-up.
g. The amplified change (positive going ramp) is fed back to the top of the timing capacitor.
(1) The positive change conducted through the timing cap opposes the change on V443 grid.
(2) The grid will run down about 60 mv .
(3) The grid change depends on system gain.
h. Since the voltage drop across the timing resistor remains virtually constant, the current into the timing capacitor will be virtually constant.
i. A constant current into a capacitor will result in a linear ramp across it.
¡. A linear sweep ramp is assured.
7. At the end of sweep, the Sweep Gating circuit lifts D439 anode to about zero volts.
a. D439 conducts, pulling V443 grid up to -800 mv (from -860 mv ).
b. Q441 conducts heavily (about 13 ma ) pulling its collector down to $3 v$ as fast as $C_{T}$ can discharge.
(1) Discharge path for $C_{T}$ is through $Q 441$ collector, $C_{T}$, and D439 to the Sweep Gating circuit .
8. At the end of retrace, D430 conducts, again establishing the sweep starting point at 3 v 。
9. L445 and R445 suppress aberrations on the sweep waveform at the start of sweep and during retrace at fast sweep speeds.

1. Sweep Terminating (Sweep Length) Amplifier; Q464, D455
2. The circuit is essentially a current shunt for the Sweep Gating TD (D405) .
a. Prior to sweep and during sweep, the circuit provides a
1.3 ma current path from the Sweep Gating TD.


TYPE 422 SWEEP GENERATOR
b. When the sweep ramp reaches its maximum amplitude, the circuit forms a shunt that robs the Sweep Gating TD of current, allowing it to switch to its low state.
c. Sweep length is spec'd at 11.2 DIV*, $^{\prime} \pm 1$ div.
2. The circuit uses one transistor and a tunnel diode.
a. Q464 is a 151-108, 2N2501, NPN silicon transistor.
b. D455 is a 1 N 3713 or TDIA, 1 ma tunnel diode.
3. The fed back sweep ramp controls the Sweep Terminating circuit.
4. Prior to sweep and during sweep, D455 is in its low state.
a. With the output ramp at $3 \mathrm{v}, .53$ ma flows through R452, .46 ma through R457 and about . 1 ma through R451 .
b. D455, therefore, is only slightly forward biased.

Q441 Collector

D455 Anode

Q464 Collector


* No sweep length control is provided.

5. As the sweep ramp runs up, D455 forward biased increases, then as the ramp reaches 34 v , the TD flips to its high state. a. At $34 \mathrm{v}, 1.1$ ma flows through R451.
b. The increase current switches the 1 ma TD to its high state.
6. Prior to sweep and during sweep, Q464 is cut off.
a. The base sets at 400 mv .
7. 1.3 ma flows through the Sweep Gating TD (D405), R406, R464 to $+12 v$.
a. The divider places Q464 collector at 6 v .
8. When the sweep ramp reaches $34 v$ and D455 switches to its high state, Q464 saturates.
9. Current previously flowing through D405 is diverted through Q464. a. Q464 draws 2.6 ma through R464.
10. D405 switches to its low state, stopping sweep.
11. As retrace starts, less and less current is pulled out of D455, until at the end of retrace the TD switches to its low state.
12. Q464 turns off as its base drops to 400 mv .
13. Current through D405 again increases to 1.3 ma .
a. The TD is enabled, awaiting a trigger to start another sweep.

## J. Free Run Mode

1. A switch ganged with the (TRIGGERING) LEVEL control activates the Free Run mode.
a. The switch is activated in the full clockwise position of the control.
2. When the FREE RUN switch is activated, the ground return for D435 and D436 is opened.
a. The diodes are now cut off with their cathodes tied through R436 to $12 v$.
b. The switch also adds 4.3 k to Q 434 collector resistance increasing the value to 8.62 k , increasing D405 current.

3. At the end of retrace, when Q434 conducts, its collector rises until D401 comes into conduction.
a. Charging of C401 introduces about $5 \mu \mathrm{sec}$ hold-off.
b. Only 1.4 ma of collector current is available through R434, R435 to $-12 v$.
c. An additional 1 to 2 ma must be supplied by D405 through D401.
d. When added to the 1.3 ma from the sweep terminating circuit, this current will switch the TD to its high state starting sweep.
4. As sweep starts, Q434 cuts off and its collector drops toward -12 v .
a. D401 cuts off.
b. Q434 collector drops exponentially as C401 discharges .
5. At the end of sweep D405 switches to its low state .
a. Q434 is enabled but cannot conduct until the end of retrace.
6. At the end of retrace, the sweep terminating circuit again pulls
1.3 ma through D405.
a. D401 remains cut off.
b. As D430 connects, D434 conducts and its collector raises as C401 charges.
c. When D401 anode raises above 500 mv , the diode conducts.
d. C401 charging current to Q434 collector now transfers to D405 (through D401) to switch the TD to its high state, again starting sweep.

## K. EXT HORIZ Mode

1. In the EXT HORIZ mode, the sweep is disabled and the CRT unblanked.
2. D403 and D404 are silicon diodes.
3. In the EXT HORIZ position of the TIME/DIV switch, D403 cathode is tied to -12 v .
a. About 4 ma flows through the diode and R403.
b. $\quad 1.3$ ma flows through R405, R406 to the Sweep Terminating circuit.

c. The balance supplies Q434 collector current through D401.
d. Some negative current flows through D405 keeping it back biased .
e. The Sweep Generator cannot function.
4. D404 cathode is also connected to -12 v .
a. 5.2 ma drawn through the diode actuates the unblanking circuit to unblank the CRT.
L. GATE OUT and Unblanking EF, Q473
5. The circuit delivers the GATE waveform to the front panel GATE OUT jack, unblanking to the CRT circuit, and unblanking to a front panel EXT BLANKING jack.
a. The EXT BLANKING jack will accept positive external unblanking information.
(1) About $+2 v$ is required to blank the CRT.
b. An ALT SWEEP SYNC pulse is also provided.

6. The circuit uses one transistor, two diodes, and a zener.
a. Q473 is a 151-133 PNP silicon transistor.
b. D476 and D479 are silicon diode.
c. D474 is a $1 \mathrm{~N} 753,6.2 \mathrm{v}$ zener diode.
7. The source of Gate, Unblanking and Alt Trace Sync is the collector of Q414.
a. Prior to sweep, Q414 collector sets at 4.2 v .
b. During sweep the collector drops to ground as the transistor saturates.
8. The Alt Trace Sync pulse is the positive going 4.2 v step at the end of sweep.
a. The pulse is fed via coax to the Alt Trace Switching circuit.
9. The -4.2 v negative going square wave is divided down to a 2.8 v waveform and applied to Q473 base .
a. C471 compensates the divider.
10. Q473 collector is zener-clamped at -6.2 v .
11. Q473 emitter swings from $0 v$ prior to sweep to -2 . Iv during sweep.
12. The waveform is further attenuated by the divider (R478, R479) to the 600 mv negative going GATE OUT.
a. Source impedance is $800 \Omega$.
b. D479 prevents chop blanking information from appearing on the GATE OUT waveform.
c. Chop blanking is a positive going signal, causing D479 to disconnect.
13. The unblanking signal is a 5.2 ma current waveform (voltage excursion is about 140 mv ).
14. External Blanking can be applied via the EXT BLANKING jack (front panel BNC).
a. About $+2 v$ is required to blank the CRT.
b. D476 prevents chop blanking from kicking back out the EXT BLANKING jack.

## M. Timing Switch

1. The Timing Switch provides the 19 sweep timing positions from $.5 \mu \mathrm{sec} /$ DIV to $.5 \mathrm{sec} /$ DIV.
a. The switch also selects EXT HORIZ mode of operation.

2. Timing capacitors are arranged in a $2,5,10$ sequence.
a. The same capacitor is used in the 2,5 , and 10 msec ranges, for example.
3. Various combinations of 147 k and 1.47 M resistors form the required values of timing resistances.
a. The resistors are $1 \%$ metal film units.
b. 5 msec uses 1.47 M .
c. 2 msec uses $590 \mathrm{~K}-\mathrm{-} .4 \times 1.47 \mathrm{M}$.
d. $\quad 10 \mathrm{msec}$ uses $2.94 \mathrm{M}-2 \times 1.47 \mathrm{M}$.
4. Maximum timing current ( $.5 \mu \mathrm{sec} /$ DIV position) is .555 ma .
5. Minimum timing current (. $5 \mathrm{sec} /$ DIV position) is $5.5 \mu \mathrm{a}$.
6. All timing caps, except for the 68 pf , are low leakage Tek made dry polystyrene caps (the $1 \mu \mathrm{f}$ for example has a resistance better than $2.25 \times 10^{11}$ ohms at 35 v ).
7. The VARIABLE (TIME/DIV) control has its calibrated detent in the full clockwise position.
a. The control arm is at the -8lv end of the control.
b. An UNCAL light indicates an uncalibrated setting of the control.
c. The control has a 2.5:1 range which extends the timing range to $1.25 \mathrm{sec} /$ DIV, uncalibrated.
8. The only timing adjustment is a variable cap (C440A) in the . 5 to $10 \mu \mathrm{sec} /$ DIV positions.
9. R440T and C440T suppress an oscillation on retrace and start of sweep at the fastest sweep speeds.

## VII. HORIZONTAL AMPLIFIER

A. The Horizontal Amplifier supplies the push-pull sweep sawtooth to drive the CRT horizontal deflection plates.

1. Push-pull sawtooth amplitude for 11.2 divisions is about 125 v .
2. CRT deflection sensitivity is 10.4 v to $12 \mathrm{v} / \mathrm{div}$ ( $11.2 \mathrm{v} / \mathrm{div}$ nominal).

B . Circuits that comprise the Horizontal Amplifier:

1. Operational Amplifier; Q513, Q524, Q453.
2. Paraphase Inverter; Q544, Q554.
C. Block Diagram


TYPE 422 HORIZONTAL AMPLIFIER
B-422-0038
D. Block Logic

1. The sweep sawtooth waveform from the Sweep Generator is applied to the Operational Amplifier Input.
a. Sawtooth amplitude is about 31v (from $3 v$ to $34 v$ ) for an
11.2 division sweep.
2. Gain of the Operational Amplifier in the $X 1$ and $X 10$ position is changed by switching in different values of $R_{f}$.
3. The sawtooth at the Operational Amplifier Output is a negative going 3.5 signal ( $\times 1$ position).
4. The Paraphase Inverter converts the negative going sweep ramp into a push-pull sawtooth 125 v peak-to-peak.
5. A POSITION control with a range of 20 divisions can position the trace off screen to the right and to past center on the left.
a. A VERNIER control with a back lash coupling covers about 1 division.
6. A section of the TIME/DIV switch connects the front panel HORIZ IN jack to the circuit input.
a. The Sweep Generator is connected but disabled in this position.
b. EXT HORIZ sensitivity is $10 \mathrm{v} / \mathrm{DIV}$ (lv/DIV on $\times 10$ MAG), uncalibrated.
7. Nominal CRT horizontal deflection sensitivity is 11.2 v/DIV (spec is 10.4 to $12 \mathrm{v} / \mathrm{DIV}$ ).
a. Push-pull sawtooth required is 125 v .
(1) $11.2 \mathrm{v} \times 11.2 \mathrm{DIV}=125 \mathrm{v}$.
8. Gain of the Paraphase Inverter is nominally 35.7.
a. Sawtooth amplitude into the Paraphase Inverter is, therefore, . $314 \mathrm{v} /$ DIV. (1) $\frac{11.2 \mathrm{v} / \mathrm{DIV}}{35.7}=.314 \mathrm{v} /$ DIV.
b. Total sawtooth input into the Paraphase Inverter is 3.5 v for 11.2 div.
9. The Operational Amplifier has a nominal gain of about . 12 (in the X1 position).
a. Output from the Sweep Generator is a 3lv sawtooth .
b. $A=\frac{e_{\text {out }}}{e_{\text {in }}}$.
$A=\frac{3.5 v}{31}$
$A \simeq .12$.
10. Total gain of the Horizontal Amplifier is about 4 with the SWEEP CAL adj set at mid range .
E. Operational Amplifier; Q513, Q524, Q543
11. The Operational Amplifier provides input mixing and control of gain (X10 MAG).
a. Circuit gain is virtually independent of transistor beta.
12. The circuit uses three transistors and two diodes.
a. Q513 is a 151-126, 2N2484 silicon NPN transistor .
b. Q524 and Q543 are 151-133 silicon PNP transistors.
c. D512 and D513 are 6185 silicon diodes.
13. The amplifier has an open loop gain of about 1000.
a. Positive feedback from Q543 to Q524 emitter increases the open loop gain from about 400 (without Q543) to 1000.

b. Open loop gain of the amplifier may change as much as $30 \%$ with temperature change.
c. Higher open loop gain makes the closed loop gain more nearly independent of transistor beta and temperature changes.
14. The basic circuit has four $R_{i}$ 's and two negative feedback paths.

a. $\quad R_{i}$ 's are provided for the sweep input, the External Horizontal input, and each of the POSITION controls.
b. In the XI position of the PULL FOR $\times 10$ MAG control, two negative feedback paths are in parallel -- an equivalent 14.2 k .
c. In the X10 (MAG) position, a 145 k value of $R_{f}$ is used.
15. For the sweep sawtooth input, a current divider is formed of R511 to the Sweep Generator and R512, R355B, R504 to ground. a. With the SWEEP CAL set at mid range a $\frac{6.75}{8}$ current division is made.
b. With the pot full clockwise, no current division is made.
c. CCW a $\frac{5.5}{8}$ division is made.
16. Gain of the Operational Amplifier is modified by this current divider.
a. $\quad A_{\text {mid scale }}=\frac{R_{f}}{R_{i}} \times \frac{6.75}{8}$

$$
A=\frac{14.2 \mathrm{k}}{100 \mathrm{k}} \times \frac{6.75}{8}
$$

$$
A=.12
$$

b. $\quad A_{C W}=\frac{14.2}{100 \mathrm{k}}$

$$
=.142
$$

c. $\quad A_{C C W}=\frac{14.2}{100 \mathrm{k}} \times \frac{5.5}{8}$

$$
=.098
$$

7. Since a gain of . 12 is required in the $X 1$ position, system design places the SWEEP CAL pot near the center of its range.
8. Sawtooth level at the Operational Amplifier output is a negative going . $314 \mathrm{v} /$ DIV.
a. For 11.2 DIV, sawtooth amplitude is 3.5 v .
9. Signal current at the Operational Amplifier input is $22 \mu \mathrm{a} / \mathrm{DIV}$.
a. $i=\frac{E_{\text {out }}}{R_{f}}$

$$
\begin{aligned}
& i=\frac{31.4 \mathrm{v} / \text { DIV }}{14.2 k} \\
& i=22 \mu \mathrm{a} / \mathrm{DIV}
\end{aligned}
$$

10. In the EXT HORIZ position of the TIME/DIV switch, the TRIG IN or HORIZ jack (front panel) is connected to the Horizontal Amplifier Input.
a. Other sections of the switch lock out the Sweep Generator, and unblank the CRT.
b. R501 (300k) becomes $R_{i}$.
11. A current divider formed from $R 355 B$ and $R 504$ reduces the signal applied to the Operational Amplifier by $\frac{5.5 \mathrm{k}}{8 \mathrm{k}}$.
a. EXT HORIZ sensitivity is about 10 v/DIV in the XI position of the MAG switch with the HORIZ ATTEN switch fully clockwise (test spec $\pm 25 \%$ ).
(1) $e=R_{i} \times i_{i n} \times \frac{8}{5.5}$.
$\mathrm{e}=300 \mathrm{k} \times 22 \mu \mathrm{a} /$ DIV $\times \frac{8}{5.5}$.
$\mathrm{e}=9.6 \mathrm{v} /$ DIV .
(2) There is no gain adjustment in EXT HORIZ.
(3) Sensitivity is a function of CRT sensitivity and pot tolerances.
b. With the HORIZ ATTEN pot in its CCW position, the External Horizontal input is not completely attenuated, but is reduced to about one-tenth its CW value -- to about 100 v/DIV.
(1) $e=300 \mathrm{k} \times 22 \mu \mathrm{a} / \mathrm{DIV} \times \frac{8}{.5}$.
$\mathrm{e}=105 \mathrm{v} /$ DIV.
c. In all sweep positions of the TIME/DIV switch, R501 is grounded, preventing noise pickup.
12. The POSITION controls use one knob in a "back lash" coupling. a. The COURSE control, using a $27 k R_{i}$, can swing the trace about 19 divisions.
(1) The control can position the trace off screen to the right and past center on left.
b. The VERNIER control (with a $100 \mathrm{k} \mathrm{R}_{\mathrm{i}}$ ) is ganged with the COURSE control, except for the back-lash area where the VERNIER only has control.
c. The VERNIER control covers about 1 DIV.
d. When the trace is positioned off screen, the Operational Amplifier output limits at 0 v and -9 v .
(1) If the output limits, the feedback no longer functions.
(2) The Operational Amplifier input, which normally has a total voltage excursion of about 3 mv , will swing to -440 mv when the trace is positioned off screen to the left.
13. In the $\times 10$ (MAG) position, $R_{f}$ increases to 145 k as R 537 is switched out.
a. The gain of the Operational Amplifier is increased by 10.
b. The ramp slope is increased by 10 although the sweep ramp is limited to $0 v$ at the top and at $-9 v$ at its negative excursion.
14. The MAG REGISTER control is an adjustment that assures magnification about screen center.
a. The control is adjusted in the XI position so a center screen marker will remain stationary as the PULL FOR X10 MAG switch is moved to the X 10 position.
b. The control can be considered an $\mathrm{R}_{\mathrm{i}}$.

c. When adjusted, no current flows through the switch at the time the sweep passes center screen.
15. In the $\times 10$ position, the 15.8 k feedback leg is grounded through L535.
a. The inductor (a ferrite bead) breaks up a 200 mc oscillation introduced by PC card layout.
16. $R_{i}$ for the Sweep Generator sawtooth input (R511) and both $R_{f}$ 's are compensated.
a. The time constants are about 250 nsec.
17. $R_{i}$ for the EXT input is not compensated, however.
a. Any C connected to the arm of R355B would form a time constant in the current shunt (R355B, R504).
b. Since the HORIZ ATTEN control is ganged with the (TRIGGERING) LEVEL control, any adjustment of the LEVEL control would change the time constant.
18. D512 and D513 protect Q513 from damage if a large voltage is connected to the EXT. HORIZ IN jack.
19. Q543 provides a current balance for Q524 and Q544 (Paraphase Inverter) .
a. Signal current through R524 is in phase with signal currents through R546 (Paraphase Inverter emitter).
b. Signal currents through R543 are out of phase with currents through Q524, Q544.
c. These signal currents balance out, providing a constant load on the -12 v supply (while the trace is on screen).
d. Note that the value of R543 equals the parallel combination of R524, R546.

## F. Paraphase Inverter

1. The Paraphase Inverter converts the single ended Horizontal signal to a push-pull drive to the CRT deflection plates.
2. The circuit uses two transistors and two zener diodes. a. Q544 and Q554 are 151-124, 2N3119 silicon NPN transistors.
b. D549 and D559 are 1N718A, 15v 5\% zener diodes.
3. The stage has a nominal gain of 35.7 .

a. Input is $.31 \mathrm{v} /$ DIV.
b. Output to the CRT is $11.2 \mathrm{v} /$ DIV (CRT deflection sensitivy is spec'd at 10.4 v to $12 \mathrm{v} /$ DIV).
c. Total push-pull output for 11.2 DIV is 125 v .
4. The collector supply for the two transistors is the $95 v$ unregulated supply.
a. The supply may vary from 95 v at low line to 116 v at high line.
b. As much as 3.3 v of 120 cycle ripple may be present.
c. Although the ripple is present at the deflection plates, it is common mode and does not effect the display.
5. R556 raises the emitter tying impedance, and reduces the effect of a temperature drift at Q544 base-emitter junction.
a. C556 provides HF peaking.
6. The presence of R556 (with R546) constitutes a current divider, reducing the drive to Q554.
a. Q554 operates with about half as much static and signal current as Q544.
b. The larger value of Q554 collector load resistor (compared with Q544 collector load resistor) provides equal voltage drive to the deflection plates.
c. The lower current in Q554 constitues a saving important in portable scopes.
7. Capacitance at Q554 collector is about 15 pf .
a. This $C$ includes $C_{\text {ob }}$, about 5.6 pf of deflection plate $C$ and some PC strays.
8. Q544 collector capacitance is about 20 pf including CRT C and strays.
9. The time constant of R544 and the 20 pf of Q544 collector capacitance is about 150 nsec .
a. This TC is matched by the degenerative TC of R546, C546 in parallel with R556, C556.
10. The time constant of R554 and Q554 collector $C$ is about 200 nsec. a. The TC is matched by the current drive TC of R556, C556.
11. Worst case condition occurs with a 12 v/DIV CRT, and with the fastest sweep speed when Q554 collector is pulled down close to ground at the end of sweep.
a. Under these conditions, a $2 \%$ sweep linearity error may occur.
b. Timing spec is $\pm 3 \%$ normal and $\pm 5 \%$ magnified.
c. When used as an External Horizontal amplifier, bandpass of the system is limited to 500 kc .
12. Zener diodes, D549 and D559, drop the DC level on Q544, Q554 collectors 15 v to place the horizontal deflection plates at a potential near that of the vertical plates.
a. Center screen voltage for both vertical and horizontal plates is 34 v at low line.
b. R548 and R558 provide about . 33 ma of static current to each zener diode.

## 8-1

## VIII. CRT AND HIGH VOLTAGE

A. The circuit includes the CRT, its voltage sources, and the Unblanking circuit.

1. The T4220 CRT is an aluminized, rectangular, $3.34 \times 3.84$ inch flat-faced tube featuring a mesh-shielded post-deflection accelerator.
2. No $Z$ axis modulation is provided.
B. Outputs from the high voltage supply.
3. 4900 v for the CRT post accelerator anode.
4. -1400 v for the CRT cathode.
a. The grid uses the cathode supply.
C. Block Diagram


TYPE 422 CRT AND HIGH VOLTAGE
B-422-0042 BLOCK DIAGRAM

3-17-'65d| (1)
D. Circuits that comprise the CRT and High Voltage circuit.

1. High Voltage Inverter (multi); Q675, Q685.
2. High Voltage Multiplier .
3. CRT Circuit, V859.
4. Deflection Unblanking Amplifier; Q863, Q864.
E. Block Logic
5. A transistorized multivibrator on the $A C$ power supply chassis develops a 20 kc voltage (the frequency may be from 15 kc to 25 kc or about 4 kc from the $\mathrm{AC}-\mathrm{DC}$ supply).
a. The multi uses the regulated -12 v and +12 v supplies.
b. This provides primary regulation for the HV supply.
6. The 20 kc voltage, a. 96 v square wave, is applied to the High Voltage transformer primary .
7. The transformer has two secondary windings.
a. A 6.3 v winding supplies the CRT heater -- after rectification.
b. A 700 v peak-to-peak winding supplies the two high voltage supplies.
8. A voltage "septupler" (seven solid state diodes) provides the 4900v CRT anode supply.
a. This supply is not re-regulated.
b. Deflection in a mesh tube is little effected by a change in post accelerator voltage.
c. Removing the post deflection anode will change sensitivity about $10 \%$.
9. In the negative supply, a voltage tripler develops about -2100 v 。
a. The voltage is regulated at $-1400 \mathrm{v} \pm 5 \%$ by a gas tube.
b. The regulated -1400 v supplies the CRT grid and is divided down by a variable divider (INTENSITY control) to supply the CRT cathode at a slightly less negative potential and the focus anode at about 400 v less negative that the cathode.
10. The CRT features trace rotation supplied by current from the +12 v and -12 v supplies.
11. Deflection unblanking (and blanking) is used.
a. Unblanking during the duration of sweep is accomplished by amplifying and applying to the deflection unblanking plates a waveform generated in the Sweep Generator circuit.
b. Blanking during the time chopping transients are present in accomplished by chop blanking pulses generated in the Trace Switching Multi.
c. External blanking may be fed to the Unblanking Amplifier from a front panel jack.
d. Provisions are made to unblank the CRT when the TIME/DIV switch is in the EXT HORIZ position.
F. High Voltage Inverter (multi); Q675, Q685
12. The Inverter develops a 20 kc voltage ( 15 kc to 25 kc ) to supply the High Voltage transformer and the High Voltage multipliers.
a. The circuit is an astable multi that utilizes the HV transformer primary (T801) and transistor beta to establish its frequency.
b. The circuit is mounted on the AC Power chassis.
c. When the DC supply is used, the 4 kc output from the DC-to-AC inverter is used to drive the HV supply.

13. The circuit uses two transistors and two diodes.
a. Q675 and Q685 are 151-148, selected RCA 40250 silicon NPN transistors.
b. D675 and D685 are 151-185 silicon diodes -- replaceable by 1 N 3506 , or CD6538.
14. The multi is supplied solely from the $-12 v$ and $+12 v$ regulated supplies.
a. The output, therefore, does not reflect line voltage changes.
15. With pins 2 and 5 of the blue ribbon connector tied together at $12 v$, T801 can be thought of as having a single center tapped primary .
a. Pins 3 and 4 are used with the $A C-D C$ supply only.
b. Decoupling network C689, R689 keeps the 20 kc off the 12 v supply bus.
16. The waveform decoupled at pins 1 and 3 of the blue ribbon connector is a push-pull 96 v square wave.
a. The voltage at pins 1 and 6 each swings from $+36 v$ to $-12 v$, or $\pm 24 v$ referenced to $+12 v$.
17. Sequence of operation:
a. Assume Q685 has just begun to conduct and Q675 has cut off.
b. Q685 collector drops 24 v (from 12v to -12 v ), transformer action (inductive coupling) raises Q675 collector 24 v (from $12 v$ to $36 v$ ).
d. The rising voltage at Q675 collector pulls Q685 base up, holding the transistor saturated.
e. Current continues to flow into T801 primary and Q685 until the base can no longer hold Q685 saturated.
f. When Q685 collector starts to rise, the field collapses, dropping Q675 collector toward the 12 v supply.
g. The falling voltage coupled through R675, C675 to Q685 base cuts off the transistor.
h. As Q685 collector rises, the positive step passing through R685, C685 lifts Q675 base, turning on the transistor holding it saturated.
i. Q675 collector is pulled down to -12v (through inductive coupling), as Q865 collector raises to 36 v .
¡. The circuit has completed one-half cycle of oscillation.
18. D675 and D685 protect reverse base-emitter breakdown.
a. When a conducting transistor drops its collector, the cross coupling capacitor would apply a 48 v negative going step to the alternate transistor base .
b. The diodes prevent the bases from dropping below -. 6 v .
19. R675 and R685 allow the collector of the cut off transistor to rise rapidly while the cross coupling cap (C675 or C685) is charging.

## G. Frequency Multipliers

1. Three rectifier systems are used to supply the CRT.
a. A seven diode voltage multipler provides the 4900 v post accelerating anode potential.
b. A three diode voltage tripler supplies the CRT grid and cathode.
c. A single half wave rectifier supplies the CRT heater .
d. A (selected) GV4-S1400 gas discharge tube* provides CRT grid and cathode regulation.
2. The diodes used in the voltage multipliers are 152-170, 1 N 4441 silicon 100 ma diodes with a PIV of 1500 v .
a. D849 in the heater supply is a 153-007.

3. All capacitors are . $01 \mu \mathrm{f} 2 \mathrm{kv}$ disc ceramic units .
4. The high voltage transformer's (T801) high voltage secondary develops 700 v peak.
a. One side is tied to ground.
5. The entire high voltage circuit, including the VR tube, is mounted on two PC cards and with the HV transformers housed in a plastic box.
a. An aluminum shield slides over the plastic box.
6. The positive supply is a conventional solid state half wave voltage multiplier, developing about 4900v.
a. R810 protects the supply should the post accelerating anode load become grounded.
7. The negative supply is a solid state voltage tripler developing about -2100 v .
8. B 820 and C 820 reduce a load placed on the inverter multi at turn on time.
a. If the instrument is turned off then turned on during a certain critical time period, the inverter multi may not start.
b. As the scope is turned off, C821, C823 and C828 begin to discharge .
(1) C822 has no discharge path initially.
(2) The junction of C822, D823 remains at -1400 v .
c. As C821, C823 discharge to -1400 v , D823 conducts.
d. A shunt is formed across T801 secondary, composed of C822, D823, C823 and C821 .
e. If the scope is turned on during this period, the added load reflected to the transformer primary will prevent the inverter from starting.
f. During this period, C 820 will have maintained a -1400 v charge.
g. When the junction of C822, D823 has raised to a point $80 v$ less negative than -1400 v , neon B820 fires.
(1) B820 is an indicator type neon so the 80 v igniting and 60 v holding potentials may vary $\pm 10 \%$.
h. The voltage drop across B820 immediately drops to 60 v .
i. The 20 v change, distributed between C820 and C822, pulls up on D823 cathode cutting off the diode.
$i$. Since the capacitive shunt is open, the multi can start.
$k$. There will be brief intervals during discharge time when D823 will connect and disconnect.
(1) The time intervals are short.
(2) The multi can start any time D823 is cut off.
9. V829, the GV4S gas discharge tube, provides grid and cathode supply regulation.
a. The -2100 v supply drops about 700 v across R825.
b. The tube can maintain 1400 v across it within 15 v over the $750 \mu$ a current change demanded by the CRT cathode.
c. About 1.25 ma is delivered by the voltage tripler .
d. About $200 \mu \mathrm{a}$ flows through the bleeder string (R831, R832, R833, R834, R837, R838).
e. When the CRT grid is driven 50 v above cut off, the cathode draws about $750 \mu \mathrm{a}$.
f. $300 \mu \mathrm{a}$ flows through V829.
g. When the CRT is cut off, $1050 \mu \mathrm{a}$ flows through V829.
(1) V829 is vendor selected to a $1300 \mu$ a spec.
(2) The catalog GV4 S-1400 is spec'd at $800 \mu \mathrm{a}$.
10. R829, C829 form a 1.8 sec compensating time constant for V 829 .
a. A sudden current change through V829 will result in greater than average change in voltage drop across it.
(1) Current change results in a temperature change which results in a change in gas pressure.
(2) The effect is a 1.8 sec voltage overshoot.
b. The RC network compensates for the overshoot.
11. Although the gas tube regulates to within 15 v , the voltage drop across R829 will add another 17 v of charge.
a. The total load change of $300 \mu$ a to $1050 \mu$ a results in a voltage change across R 829 of 16.8 v .
12. The CRT heater is supplied from its own transformer secondary.
a. The heater uses 90 ma at 6.3 v .
b. The transformer delivers $\approx 14 \mathrm{v}$ peak-to-peak, rounded square wave from the $A C$ supply or a series of alternate $7 v$ positive and $7 v$ negative pulses from the AC-DC supply.
c. Since the RMS value of the waveforms delivered by the two power supplies are different, AC could not be used to supply the CRT heater.
d. The supply is rectified by D849 and filtered by C848 and C849.
e. Since very large caps are used (for the frequency), the DC output will be a function of the AC peak value, not the RMS value.
13. R846 ties the CRT heater to the cathode to elevate it to -1400 v , thereby preventing cathode heater breakdown.
a. B846 protects the CRT during warm-up when the cathode could drop far below the heater while C848 was charging .
14. C839, C846 help filter the -1400 v supply.

## H. CRT Circuit, V859

1. The CRT is a Type T4220 aluminized, rectangular ( $3.34 \times 3.84$ inch) flat-faced tube with a mesh-shielded post-deflection accelerator, lighted internal graticule and a low current heater.
a. The tube is 12 inches long, $\pm 1 / 2$ inch.
b. P1, P2, P7, P11 and P31 phosphors are available -- a P31 is standard.

2. The CRT uses the following potentials, relative to the cathode.
a. Grid No. 1-55 to $-75 v$ for cut off.
b. Post-accelerator

6300 volts
c. Post-accelerator grid
-39 volts
d. Isolation shield 1400 volts
e. Average deflection plate voltage

1400v
f. D1-D2 shield

1388-1495 volts
g. Astigmatism electrocle

1388-1455 volts
h. Focusing electrocle
$320-520$ volts
i. Acceleration

1373 volts
j. Blanking ( $\mathrm{I}_{\mathrm{k}} 750 \mu \mathrm{a}$ )
$\pm 15$ volts
k. Heater
6.3 volts
I. Heater current

90 ma
3. The post-accelerator is supplied 4900 v from the voltage multiplier supply.
a. Since the cathode is at -1400 v , the 6300 v requirement is satisfied.
b. Typical beam current ranges from zero to a theoretical $35 \mu \mathrm{a}$ when the CRT grid is 50 v above cut off.
c. About $13 \mu \mathrm{a}$ flows through the 200 megohm helix.
4. The cathode (pin 2) draws a theoretical maximum of $750 \mu$ when the grid is 50 v above cut off.
a. Cut off is between 55 and 75 volts, defined as visual extinction of an undeflected spot.
5. All tube elements past the grid are supplied by unregulated voltages.
a. Since all voltages will change with line voltage change and with ripple, the pin voltages will remain fairly constant relative to one another.
6. The focus anode is variable from 320-520 volts less negative than the cathode or -880 to -1180 with respect to ground . a. The voltage range is taken from the FOCUS control; a part of the bleeder string.
7. Pin 7 connects to the accelerator anode and the unblanking plate return.
a. The potential is about $12 v$ with respect to ground (at low line).
8. The astigmatism electrode (pin 10) is connected to the front panel ASTIGMATISM control.
a. The control has a range from the 55 v supply potential to $-12 v$.
9. The D1-D2 shield (pin 8) is connected to the GEOMETRY control -a screwdriver adjustment located on the left side of the scope. a. The control ranges from the 95 v supply voltage to -12 v .
10. The isolation shield ( $\operatorname{pin} 5$ ) is connected to a divider from the 55 v supply.
a. Pin 5 voltage sets at 38.8 v when the 55 v supply is at 55 v .
b. The 200 megohm helix is connected to the isolation shield.
11. The post accelerator grid, or mesh grid, is grounded.
12. Trace rotation is accomplished by passing current through the trace rotation coil wrapped around the CRT.
a. The coil is composed of 2400 turns of No. 38 wire.
b. The TRACE ROTATION control is a screwdriver adjustment on the scope rear panel; accessable by removing the power supply chassis.
c. With the control clockwise, 10 ma flows through the Trace Rotation coil.
d. CCW -. 9 ma flows through on equivalent 4.4 k to -5 v .
e. The control swings the beam about $4^{\circ}$ with a little overlap as the current reverses.
f. Connection is made to pins on the Horizontal Amplifier board.
(1) The pins may be reversed to provide full $8^{\circ}$ rotation.
(2) Reversing rotation by removing pins provides a current saving.
I. Unblanking Amplifier; Q863, Q864

1. The CRT features deflection unblanking.
a. $\pm 15 \mathrm{v}$ is required to blank the CRT when cathode current is $750 \mu \mathrm{a}$ ( 30 v for flare free blanking).
b. When CRT pins 7 and 12 are at the same potential $( \pm 3 \mathrm{v})$, the CRT is unblanked.
2. The circuit uses two transistors, four diodes and a zener diode.
a. Q863 is a 151-103, 2N2219 silicon NPN transistor with relaxed specs.
b. Q864 is a 151-121, 2N3118 silicon NPN transistor.
c. D864, D865, D866 and D867 are 6185 silicon diodes.
d. D841 is a $152-167,1$ N976, $43 \mathrm{v} 10 \%$ zener diode.
3. Q864 base is clamped at . 6 v by D865.

a. About 2 ma of keep-alive current flows through D865 and R865.
b. The diode temperature compensates Q864 base emitter junction.
c. The emitter is always at ground potential.
4. Q864 collector is supplied through R864, R863, R861 by the 55 v unregulated supply.
a. This supply is 55 v at low line and 66 v at high line.
b. The supply contains an average of 1.2 v of 120 cps ripple.
5. Since the collector load looks into a high collector impedance, Q864 collector (and the CRT deflection plate, pin 12) is free to move with changes in the 55 v supply.
a. In order to prevent changes in the 55 v supply from modulating the beam, the deflection plate return, $\operatorname{pin} 7$, is also connected to the 55 v supply.
b. D841, a $43 \mathrm{v} 10 \%$ zener, drops the 55 v supply by 43 v at the deflection plate.
(1) At low line, CRT pin 7 will set at 12 v .
(2) At high line, however, CRT pin 7 will rise to 24 v .
(3) Considering worst case conditions (zener at extreme tolerance and line voltages to their limits), pin 7 can be as low as 7.7 v and as high as 27.3 v .
6. About 7 ma flows through Q864 during unblanking to provide a 43 v drop across the collector load resistors.
a. The $43 v$ drop is compatible with the $43 v$ of D841 on the alternate unblanking plate.
b. The UNBLANKING CENTER control (R869, a screwdriver adjustment) is provided to match the voltage at pin 12 during unblanking with the voltage at pin 7.
(1) Since D841 is a $10 \%$ devise, R869 must be able to move Q864 collector at least $\pm 7.3 \mathrm{v}$ to compensate for the $10 \%$ tolerance diode and the $\pm 3 \mathrm{v}$ deflection unblanking tolerance.
(2) R869 is a tapered pot to provide a linear control of the .5 ma to 3.3 ma range of currents required with different zeners.
c. Nominally, 1.9 ma flows through the UNBLANKING CENTER control (further discussion will consider an ideal zener and a 55 v supply).
d. 5.1 ma flows from the Unblanking signal source .
7. In the EXT HORIZ mode of the TIME/DIV switch, R867 is
tied to -12 v through diode, D404*.
a. $\quad 5.1$ ma flows through R867.
b. This current plus 1.9 mathrough R 869 provides the 7 ma required to drop Q864 collector 43 v below the 55 v supply .
c. The CRT is unblanked.
8. In the Sweep positions of the TIME/DIV switch, D404 is cut off.
a. No current flows through R867.
9. Prior to sweep, the Unblanking input at R477 is at ground.
a. No current flows through R866.
b. $\quad 1.9$ ma from the emitter tail flows through Q864.
c. Q864 collector (and CRT pin 12) is at 45 v .
d. With CRT pin 7 at $12 v$, the $32 v$ difference between the deflection unblanking plates cuts off the CRT.
10. At the start of sweep, R477 drops to $-2 v$ as the Sweep Generator develops the Unblanking pulse.
a. 5.1 ma flows through R477, R866.
b. Added to the 1.9 ma emitter tail current, the 7 ma required to drop Q864 collector to $12 v$ is present.

[^1]c. As Q864 collector drops to 12 v , D864 conducts pulling pin 12 to $12 v$ to equal the voltage on pin 7 -- the CRT is unblanked.
(1) Emitter follower, Q863, cannot follow the fast negative step, so current to charge the unblanking plate C is furnished by D864.
(2) Q863 has no function during Unblanking turn on.
d. R866 is a damping resistor to suppress ringing caused by the input L of Q864 emitter .
11. At the end of sweep, the 5.1 ma from the Sweep Generator stops.
a. As Q864 collector rises, emitter follower, Q863, pulls CRT pin 12 to 45 v to again blank the CRT .
b. Q863 functions only during unblanking turn off -- at the end of sweep.
c. R864 biases Q863 to slight conduction during sweep so it can turn on rapidly at the end of sweep.
12. External Blanking may be applied at a front panel BNC jack.
a. About $2 v$ is required to blank the trace.
b. 3.lv at the EXT BLANKING jack would completely neutralize the 5.1 ma from the Unblanking waveform.
c. Input impedance is $283 \Omega$.
13. During dual trace CHOP operation, chop blanking pulses from the Dual Trace Switching Multi and Q294 appear at R295.
a. Quiescently this point is at ground.
b. When the Dual Trace Switching Multi switches, a $4 v$ positive going pulse appears.
c. An 8 ma current pulse robs both the unblanking current and Q864 emitter tail current .
d. Q864 cuts off and CRT pin 12 raises to 55 v for the pulse duration.
14. D476 prevents chop blanking pulses from kicking back out the EXT BLANKING jack.
a. Since the chop blanking pulses are positive going, D476 will disconnect with each pulse.
15. D866 and D867 protect Q864 from damage from an excessive EXT voltage.

## IX. CALIBRATOR

A. The Calibrator provides a voltage square wave to the Vertical Preamp and to a front panel pin jack.

1. The waveform has a repetition rate of $1 \mathrm{kc} \pm 20 \%$.
2. The voltage applied to the front panel jack is a negative going 2 v square wave with the base line near ground.
a. Amplitude accuracy is $\pm 2.7 \%$ at $25^{\circ} \mathrm{C}$ and $\pm 3.6 \%$ over the entire operating temperature range.
b. The primary purpose is for probe calibration.
c. Risetime is about $6 \mu \mathrm{sec}$ and fall time is about $1 \mu \mathrm{sec}$.
d. Duty cycle is $45 \%$ to $55 \%$.
e. Source impedance is about 2 k .

3. When either Vertical Preamp is set to CALIBRATOR, a . 2 v square wave is connected to the Preamp input.
a. Preamp gain is set at $.05 \mathrm{v} /$ div.
b. Four divisions of square wave are displayed.
c. The waveform may be used to set the gain of the Vertical Amplifier.
B. The Calibrator circuit is a transistorized common emitter astable multivibrator.
4. The circuit uses two transistors and six diodes.
a. Q765 and Q775 are 151-087 selected 2N1131 silicon PNP transistors.
b. The diodes are 152-185, 6185 silicon diodes -- replaceable by 1 N 3605 .
5. No provision is made to turn off the calibrator.
6. Sequence of operation:
a. Assume Q765 has just turned on.
b. As the transistor saturates, its collector pulls up to ground.
c. The positive step passing through C765 lifts Q775 base and D770 anode to cut off at $1.2 v$.
d. Q775 collector drops toward -81v to be caught at -13 v by D773 and D769.
(1) This forms the bottom of the calibrator square wave.
e. Q775 base begins to fall asymptotically toward -12 v as C765 charges through R773.
f. In approximately $500 \mu \mathrm{sec}$, Q775 base will have dropped to - -.6 volts where the transistor can conduct .
g. As Q775 begins to conduct and its collector rises (D773 cuts off), the positive change is coupled through C775 and D761 to Q765 base, raising the base and D760 anode to cut off at 1.2 v .

Q775 Collector

Q765 Collector

Q765 Base

Q775 Base
(1) D761 provides a low Z coupling path across R761.
(2) Since C775 must discharge before Q775 collector may rise to ground, risetime of the waveform is about $6 \mu \mathrm{sec}$ 。
h. Through multi feedback action, the multi switches as Q775 saturates and Q765 cuts off.
i. Q775 collector now rests at ground, forming the top of the calibrator square wave.
i. Q765 base begins to drop as C775 charges through R763.
k. Although Q765 is cut off, its collector can drop only as fast as C 765 can charge through R 764 .
(1) Saturated Q775 clamps C765 return solidly to -. 6 v .
(2) Q765 collector, dropping toward -12 v , reaches -5.5 during the multi half cycle.

1. When Q765 base has dropped to . 6 v (in $500 \mu \mathrm{sec}$ ), Q765 turns on and the multi switches, beginning the next cycle.
(1) As Q775 collector drops, D761 disconnects allowing the collector to drop to -12 v without waiting for C775 to discharge.
2. Diodes, D760, D762 and D770, limit the base rise to 1.2 v assuring cut off but preventing base-emitter reverse breakdown.
a. C762 holds D760 and D770 cathodes so the diodes will disconnect when one of the transistor bases starts to drop.
3. D769 keeps the multi from "sticking" with both transistors saturated when the scope is turned on.
a. If both transistors are saturated, both bases and both collectors would pull up to ground.
b. D773 would disconnect .
c. The junction of D769 and C769 would raise toward ground (disconnecting D769) as C769 charged through R763 and R773.
d. Base current, holding the transistors in saturation, would gradually decrease.
e. When one transistor begins to come out of saturation, the multi would start to operate .
4. When Q775 cuts off and its collector drops to -13v, D779 disconnects, allowing the output to be set by a voltage divider.

a. Calibrator amplitude, therefore, is independent of the multivibrator.
b. The CAL AMPL adj (a screwdriver adjustment on the CALIBRATOR board) can set the output to precisely $-2 v$.
(1) Resistance changes with temperature can effect the output, however.
(2) All resistors in the divider are 1\% components.
c. When the 2 VOLT PROBE CALIBRATOR output is $2 v$, the square wave to the Vertical Input Amplifier is divided down to $.2 v$.
5. When Q775 saturates, D779 conducts, pulling the junction of D779 and R783 to -.75 v .
a. Currents through the dividers and the diode are such that the CALIBRATOR output sets at just a few millivolts above ground.
b. The output baseline is dependent upon voltage across the saturated Q775 and across D779.
(1) Temperatures will effect these potentials.

## X. REGULATORS

A. Two regulators, supplying 20 v and -81 v are provided in the oscilloscope main frame.

1. Additional regulated and unregulated voltages are available from the AC or AC-DC supplies .
a. +95v unregulated*.
b. +55 v unregulated*.
c. $\quad+12 \mathrm{v}$ unregulated (for scale illumination)**.
d. $\quad+12 \mathrm{v}$ regulated.
e. -12 v regulated.
f. -110v unregulated*.
2. All voltages from the AC-DC supply are regulated.


* These values are at low line.
** Actually 12 v to 15.5 v or 12 v with the $\mathrm{AC}-\mathrm{DC}$ Supply.
B. Blue Ribbon Connections

1. The blue ribbon connector mounting can be easily removed and the cable released to form a power chassis test extension.
2. V13 and V113, the Input Amplifier nuvistors, are supplied (in series) from the +12 v regulated supply.
a. The nuvistors draw 125 ma heater current at 5.75 v .
(1) R725 drops the heaters to 5.75 v each for longer life.
3. The scale illumination bulbs are supplied from the 12 v unregulated supply.
a. 12 v unregulated sets at 12 v at low line and 15.5 v at high line.
b. The bulbs are 336 incandescent lights that draw 80 ma at $14 v$.
c. Typical life expectancy is 1000 hours.
d. The front panel SCALE ILLUM control supplies the full voltage in the CW position and opens the supply (OFF position) in the CCW position.
4. Pins 24 and 13 are jumpered to form an AC interlock.*
5. V443, the Sweep Generator miller integrator tube leater, is supplied from the -12 v regulated supply.
a. The tube draws 60 ma .
6. The POWER indicator neon is supplied through 100 k from the 95 v unregulated supply.
7. 75 v for the miller tube plate is tapped down from the 95 v unregulated supply.
a. The tube uses about 3 ma .

* This is a DC interlock when the AC-DC supply is used.
b. The 75 v supply is referenced to ground by D729, a 75 v $5 \%$ zener.
c. The zener holds the 75 v supply to within $1 / 2 \mathrm{v}$ from low to high line.

8. The three UNCAL lights (CH 1 VOLTS/DIV, CH 2 VOLTS/DIV, and TIME/DIV) are supplied from the -110 v unregulated.
a. The lights are indicator type neons drawing about $230 \mu \mathrm{a}$ each.
C. 20v Regulator
9. The 20 v Regulator output is used in the Vertical Preamp on the nuvistor plates and in the Horizontal Amplifier.
a. About 9 ma is used.

10. The regulator uses a zener as reference, making it independent from the -12 v adjustment.
11. The circuit uses two transistors and two zener diodes.
a. Q714 is a 151-157, RCA 40232 silicon NPN transistor.
b. Q717 is a 151-136, 2N3053 silicon NPN transistor.
c. D713 and D714 are $6.2 \mathrm{v}, 5 \%$ zener diodes.
12. The error signal taken from the 20 v output is divided down in feedback divider R718, R719.
a. The error voltage is compared with the zener reference voltage in Q714.
b. The difference voltage appears amplified and inverted at Q714 collector .
c. Fed back through emitter follower, Q717, the error voltage holds the 20 v output constant.
d. Dynamic impedance of the supply is nominally 3 to 4 ohms.
13. No adjustment is provided for the 20 v regulated output.
a. The output could be adjusted by selecting D713, R718 and R719.
b. D713 is a $5 \%$ component and R718, R719 are $1 \%$.
14. D714 references Q714 collector supply to the 20 v regulated output.
a. The 55 v unregulated supply ranges from 55 v at low line to $66 v$ at high line.
b. The junction of D714 and R714 showed a change (with line voltage) of 60 mv on one instrument tested.
c. The zener increases the output $Z$ of the regulator by introducing a small amount of positive feedback.
15. R716, C715 decouple the 55 v supply, effectively filtering the unregulated supply's 120 cycle ripple.
D. -81v Regulator
16. The -81v Regulator output is used to supply current to the Sweep Generator, the Calibrator, and the Trigger Take-Off circuit.
a. Approximately 3.9 ma is used at fastest sweep speeds.
b. 3.4 ma is used at slower sweep speeds.

17. The - 81 v supply uses a voltage regulator tube, V 739 , as reference . a. The supply is independent from the -12 v adjustment.
18. The circuit uses two transistors, a VR tube, a zener and a signal diode.
a. Q734 is a 151-136, 2N3053 silicon NPN transistor .
b. Q737 is a 151-134, 2N2905 silicon PNP transistor .
c. $\quad \mathrm{V} 739$ is a ZZ1000 voltage regulator tube.
(1) The tube has a temperature coefficient of $.0015 \%$ per ${ }^{\circ} \mathrm{C}$.
d. D739 is a $1 \mathrm{~N} 753 \mathrm{~A}, 6.2 \mathrm{v}, 5 \%$ zener diode.
e. D735 is a 6185 silicon signal diode .
19. Q734 is a constant current source for V739.
a . Q734 supplies 3.2 ma .
b. Constant current is achieved by providing a constant voltage across R733.
c. Q734 emitter is returned to -110 v unregulated.
(1) -110 v supply varies from -110 v at low line to -135 v at high line.
d. Q734 base is referenced to -110 v through D739, the 6.2 v zener.
e. Since Q734 emitter (through the base emitter junction and D739) will move with the -110 v supply, a constant voltage drop across $R 733$ is assured.
f. Q734 circuit is, therefore, a constant current device.
20. D735, R735 assures adequate starting voltage for V739.
a. On initial turn-on, D735 is reverse biased 55 v .
b. V739 requires 120 v starting voltage .
c. With 55 v on the anode and the cathode at -81 , ignition is assured.
21. At $3.2 \mathrm{ma}, \mathrm{V} 739$ has 81 v drop across $\mathrm{it}, \pm .9 \mathrm{v}$.
a. Considering the . 6 v across $\mathrm{D} 735, \mathrm{~V} 739$ cathode sets at $-81.6 v$.
b. The . $6 v$ drop across Q737 base emitter junction brings the regulated output at Q737 emitter back to -81v.
22. Q737 is an emitter follower supplying the -81 v load.
a. Output impedance is the $r_{e}$ of the transistor -- about 10 10 .
b. The load will vary from 3.4 ma at slow sweep speeds to 3.9 ma at higher sweep speeds.
c. The output on one test instrument varied 40 mv from low to high line, but showed no measurable* voltage change with change in sweep speed.
23. C739 filters zener noise.
24. C736 filters noise from V739.

## XI. AC POWER SUPPLY

A. The AC Supply is a removable power supply for the scope.

1. The supply operates on $115 \mathrm{v} \pm 10 \%$ or $230 \mathrm{v} \pm 10 \%$.
2. Additional transformer windings provide connection for inputs of $105 \mathrm{v}, 125 \mathrm{v}, 210 \mathrm{v}$ and $250 \mathrm{v}( \pm 10 \%)$.
3. For other than $115 \mathrm{v}( \pm 10 \%)$, solder connections must be changed on the transformer.
4. The supply will operate from 50 cps to $400 \mathrm{cps} \pm 10 \%$.
5. No AC at line frequency is used in the scope.
6. The scope uses 32 watts with the AC Supply.
B. Block Diagram

C. Six DC output voltages are supplied.
7. $+95 v$ unregulated $(95 v$ to $116 v$ ).
8. +55 v unregulated ( 55 v to 66 v ).
9. +12 v unregulated ( 16 v to 19.5 v ).
10. +12 v regulated $( \pm .25 \mathrm{v})$.
11. -12 v regulated (adjustable).
12. -110 v unregulated $(-110 \mathrm{v}$ to $-135 \mathrm{v})$.
D. Power Transformer and Rectifiers
13. The transformer is assembled without the customary case and terminal board.
a. A weight, cost and space saving is made.
b. A mu metal shield surrounds the center section.
14. Both sides of the input $A C$ line are broken by a two pole switch that is mounted on the power supply board.


TYPE 422 A C POWER SUPPLY
a. The push-pull type power knob mounted on the front panel is linked mechanically with the switch.
b. TK601 is a $187^{\circ}$ thermal cutout.
c. The primary fuse is a . 6 a $3 A G$ Slow Blo for 115 operation. (1) A. 3 a is used for 230 v operation.
3. The transformer has two secondary windings .
a. The smaller winding supplies the -12 v regulated supply.
(1) A center tapped winding of No. 24 wire is used.
(2) $30 v$ RMS is developed.
b. The larger winding supplies all except the -12 supply.
c. The winding is center tapped, with several taps for the various supplies.
4. All rectifiers are silicon diodes.
a. D651, D652, D610 and D611 are 152-198 Motorola MR1032A.
(1) The diode is a 3a device with a PIV of 200v.
b. D645, D646, D661 and D662 are 152-107, replaceable by 1 N647.
(1) These are 400 ma diodes with a PIV of 400 v .
5. The +12 v supply is fed from the center portion of the center tapped secondary -- center tap grounded.
a. The winding develops 30v RMS.
(1) No. 24 wire is used.
b. A full wave silicon rectifier develops 16 v to 19.5 v (depending on line voltage).
c. C652, a $2000 \mu \mathrm{f} 20 \mathrm{v}$ filter reduces 120 cps ripple to about 1.6 v peak-to-peak.
d. The unregulated voltage feeds the $12 v$ Regulator and the scale illumination bulbs.
e. The regulator uses about 530 ma and the graticule lights another 160 ma when full on.
6. The 55 v supply is fed from the second pair of taps on the transformer secondary (from the center tap).
a. The winding develops a total of 108 v RMS (39v each side, plus 30 v from the center portion of the winding).
(1) No. 33 wire is used.
b. A full wave silicon rectifier develops 55 v to 66 v (depending on line voltage).
c. C666, a $350 \mu \mathrm{f}$ cap, filters the 120 cps ripple to an average $1.2 v$ peak-to-peak.
d. The 55 v supply is used in the Vertical Amplifier, the Sweep Generator, 20 v and -81 v Regulators, the Horizontal Amplifier and the CRT and Unblanking circuits.
e. About 60 ma is used.
(1) The load will vary about 4.5 ma at slow sweep speeds as the Sweep Generator ramp runs up .
f. R661 ( $10 \Omega 1 / 4 w$ ) functions as a fuse if the supply becomes shorted.
g. R666 bleeds the supply, discharging C666 when the blue ribbon connector is disconnected.
7. The 95 v supply is fed from the third pair of taps (from the center tap) .
a. No. 37 wire is used in this portion of the secondary.
(1) A total of 168 v RMS is developed.
b. A full wave silicon rectifier develops 95 v to 116 v
(depending on line voltage).
c. C665 filters the 120 cps ripple to an average 2.lv peak-to-peak.
d. The $95 v$ is used in the CRT circuit and as the Miller tube plate supply in the Sweep Generator.
e. About 20 ma is used at the fastest sweep speeds.
(1) The load will fluctuate about 4 ma at slower sweep speeds with the varying demand of the Horizontal Amplifier.
f. R662 (10 1/4w) functions as a fuse .
g. R665 bleeds the supply, discharging C665.
h. R664 limits the current to the POWER indicator neon.
8. The -110 volt supply is taken from a single ended outer tap of the transformer secondary.
a. No. 37 wire is used in this section of the winding.
(1) A total of $96 v$ RMS is developed.
b. A half wave silicon rectifier develops -110 v to -135 v (depending on line voltage).
c. C642 filters the 60 cps ripple to an average 2 v peak-to-peak.
d. The -110 v supply is used to light the three UNCAL neons and to supply current to the -81v Regulator.
e. About 8 ma is used -- the neons use about $230 \mu \mathrm{a}$ each.
f. R641 ( $10 \Omega 1 / 4 \mathrm{w}$ ) fuses the supply.
g. R642 bleeds the supply, discharging C642.
9. The $-12 v$ Regulator has its own center tapped secondary winding.
a. The winding develops 30 v RMS.
(1) No. 24 wire is used.
b. A full wave silicon rectifier develops $-16 v$ to $-19.5 v$ (depending on line voltage).
c. The negative side of the supply is tied to the -12 v

Regulator output .
d. The positive side of the supply will move with a change in line voltage from +3.5 v to +7.5 v .
e. The -12 v supply feeds the -12 v Regulator, and is not used, unregulated, anywhere else in the scope.
f. C611 filters the rectifier output.

## E. - 12 Volt Regulator

1. The -12 v Regulator output is used in every major circuit in the scope .
a. The load draws about 530 ma from the supply.

2. The regulator uses four transistors and a zener diode.
a. Q633 is a 151-103 silicon NPN, a 2N2219 with relaxed specs.
b. Q624 and Q634 are 151-151 silicon NPN transistors*.
c. Q737 is a 151-134 silicon NPN selected 40250 transistor.
d. D622 is a 1 N 936 9v $5 \%$ zener .
3. Q624 and Q634 form a differential comparator which compares a sample of the -12 v regulated output on Q 634 base with the zener reference foltage at Q624 base.
4. Q633 and Q637 are current amplifiers.
a. Q633 is the driver amplifier.
b. Q637 is the series regulator .
c. Q637 is a power transistor mounted on the aluminum chassis.
5. Sequency of operation:
a. Assume an added load is applied increasing the current demand.
b. The -12 v output would move to a less negative voltage .
c. The error voltage developed across the error divider R637, R638, R639 is applied to Q634 base.
d. The signal difference between the error voltage on Q634 base and the reference voltage on Q624 base is amplified in Q634.
e. The amplifier error voltage at Q634 collector would rise lifting Q624 base .
f. Q633, the driver amplifier, causes Q637 to deliver more current, satisfying the increased load current requirement.
g. Q637 collector is pulled down.
(1) Q637 emitter is tied to ground and cannot move.
h. Since the voltage drop across the rectifier output is fixed (for a given line voltage), the drop at Q637 collector will drop the -12 v regulated output.
i. The result of the feedback circuit is having kept the regulated output constant.
6. When the line voltage changes, the positive side of the unregulated supply moves from 3.5 v at low line to 7.5 v at high line.
a. The positive side of the supply can move quite easily since it looks into the high impedance collectors of Q633 and Q637.
7. Dynamic output impedance is less than $.1 \Omega$ (. $02 \Omega$ on one test scope).
8. R614 protects Q637 should the supply become grounded.
F. $\quad+12 v$ Regulator
9. The regulated 12 v output is used in every major circuit in the scope.
a. The load draws about 530 ma from the supply.
10. The regulator uses three transistors, a zener diode, and a signal diode.
a. Q653 and Q654 are 151-103 silicon NPN transistors.
b. Q657 is a 151-148, 40250 silicon power transistor.
c. D655 is a 1 N969A, $22 \mathrm{v} 10 \%$ zener diode.
d. D653 is a 152-185 silicon diode.
11. Q654, a voltage amplifier, has its emitter referenced to ground through D653.
a. D653 temperature compensates Q654 base-emitter junction.
b. R653 supplies Q654 emitter current and about 2.5 ma keep-alive current for D653.
c. Q654 collector load resistor, R654, is tied to an equivalent $34 v$.

(1) By zener referencing to the regulated $12 v$, a stable 34 v is assured.
(2) On one test instrument, the 34 v point moved 170 mv from low to high line while the unregulated 55 v increased to 67 v .
12. Q653 and Q657 are current amplifiers.
a. Q657 is a power transistor mounted on the aluminum chassis.
13. Sequence of operation as the 12 v load changes.
a. An error voltage at the 12 v regulated output is taken off the feedback divider, R658 and R659, and fed to Q654 base.
(1) C658 couples fast changes across the divider.
b. Amplified and inverted in Q654, the error voltage biases Q653 and Q657 to correct for the current change in the load.
c. The result is a stable output voltage as the load varies.
14. Dynamic output impedance is less than .l ohm (it was $.02 \Omega$ on one instrument tested.
15. R652 bleeds the supply, discharging C652.
16. R657 limits current to the graticule lights, thereby extending their life expectancy.
A. The AC-DC Power Supply is a removable power supply for the scope.
17. AC power source:
a. $115 \mathrm{v} \mathrm{AC} \pm 20 \%$.
b. $230 \mathrm{v} A C \pm 20 \%$.
(1) Input power selection is made by the POWER MODE switch on the supply's rear panel.
c. Frequency 45 to 440 cps .
(1) At 45 cps , the upper voltage limits are derated to $+10 \%$.
(2) This is a linear derating starting with 50 cps at $+20 \%$.
d. Power remains virtually constant at 27 watts for all input voltages.
18. DC External:
a. 11.5 v to 35 v DC, typically 23 watts.
19. DC Internal:
a. 24 v battery (rechargeable), 23 watts .
(1) $20,1.2 v, 3.5$ ampere hour $N_{i} C_{d}$ cells
b. About 4 hours running time.
20. Output voltages available:
a. Pin $9,+95 v \pm 2 \%$.
b. $\operatorname{Pin} 15,+55 \mathrm{v} \pm 2 \%$.
c. Pin $20,+12 v$ to graticule lights.
d. $\operatorname{Pin} 19,+12 v \pm 2 \%$.
e. Pin $7,-12 v \pm 1 \%$, adjustable.
f. Pin $11,-110 v \pm 3 \%$.
g. Pins 1, 4 and 3,5 , the $\approx 26$ v peak-to-peak pulsed output to drive the high voltage transformer.

## B. Block Diagram


C. Circuits That Comprise The AC-DC Power Supply:

1. Multi; Q1105, Q1115.
2. Steering Switch; Q1104, Q1114.
3. Energy Storage Switch; Q1174, Q1184.
4. Block Oscillator, Q1120.
5. Pulse Amplifier; D1155, Q1163, Q1164.
6. Error Amplifier; Q1134, Q1144, Q1154.
7. Start Circuit; Q1193, Q1194.
8. 12 v supply.
9. Transformer and rectifier circuit.
D. Block Logic
10. Most of the circuitry in the AC-DC supply is involved in delivering a constant 23 watts to the load.
a. The supply is $\simeq 80 \%$ effective so only $\simeq 18.5$ watts is delivered to the main frame; the rest is used in the supply.
b. The input to the $A C-D C$ supply is a $D C$ voltage from the AC-DC power selector circuit.
c. The voltage may vary from 11.5 v to 35 v .

11. Consider the simplified circuit (previous page).
a. L has an inductance of $177 \mu \mathrm{~h}$.
b. The battery may be 11.5 v to 35 v .
12. When the switch is closed, current flows into the inductor at an increasing rate.
a. A voltage drop equal to the battery potential appears across the inductor.
b. D is cut off.
13. When the current into the inductor reaches 5.9 amps , the switch is opened.
14. As the electromagnetic field collapses, polarity of the voltage drop across $L$ reverses .
15. The diode conducts as the stored energy is dumped into the capacitor and the load.
16. The switch closes again storing more energy to start the next cycle.
17. The amount of energy stored and delivered to the load can be expressed as $J=1 / 2 L i^{2}$.

Where: $\quad J=$ energy in joules or watt-seconds

$$
\mathrm{L}=\text { the inductance, } 177 \mu \mathrm{~h}
$$

$$
\mathrm{i}=\text { the maximum current into } \mathrm{L}, 5.9 \mathrm{a} .
$$

a. $\mathrm{J}=\frac{1.77 \times 10^{-4} \times 5.9^{2}}{2}$
$\mathrm{J}=3.08 \mathrm{mi}$.
9. The expression $e=-L \frac{d_{i}}{d_{\dagger}}$ illustrates the circuit requirements.
a. Solving the differential equation gives $t=-L \frac{i}{e}$.
b. L is a constant at $177 \mu \mathrm{~h}$.
c. $i$ is $5.9 a$ into the inductor.
d. e may vary from 11.5 v to 35 v .
e. t, therefore, must vary inversely with e.
10. The waveforms (below) illustrate the current, voltage and time relationships.
a. Waveforms A illustrate a relatively low battery voltage.

b. Waveforms $B$ show a higher battery voltage .
c. The first time period represents ON TIME, the time the switch is closed; the battery is applied across the inductor and current is flowing into the inductor at an increasing rate.
d. Note that as the battery voltage increases, the ON TIME decreases.
(1) The ON TIME area (shaded area) remains the same.
e. The switch is opened, in either case, when current into the inductor reaches 5.9a.
f. When the switch is opened (second time period), the voltage across the inductor reverses.
g. The inductive voltage will always be $35 v--$ the voltage is a function of the inductance, the energy stored and the load.
11. In the AC-DC Supply, an electronic switch (Energy Storage Switch) connects the battery (the DC power input) to the inductor (one-half T1201 primary).

a. The diode and capacitor in the simplified circuit represent the composite rectifier diodes and filter caps in the actual circuit.
12. The heart of the $A C-D C$ Regulator is the 7.5 kc free running Blocking Oscillator which controls the Energy Storage Switch turn-on.
13. Whenever the Blocking Oscillator fires, two simultaneous operations occur that turns on the Energy Storage Switch. a. The Blocking Oscillator switches the Multi (a flip flop multi -- a 2:1 countdown device).
b. The Steering Switch guides the Multi output to help turn on one side of the Energy Storage Switch.
c. Simultaneously the Blocking Oscillator switches the Pulse Width TD which turns on the Pulse Amplifier.
d. The Pulse Amplifier in turn supplies current to the Steering Switch allowing the Steering Switch to turn on the Stored Energy Switch.
14. The switch connects the battery (DC power input) to one-half T1201 primary.
15. When current into the transformer reaches 5.9a, the Pulse Amplifier output turns off the Stored Energy Switch.
a. The Error Amplifier circuit through the Reference Zener Bridge senses the transformer ( T 1201) output. $^{\text {. }}$
b. The Error Amplifier sets operating conditions for the Pulse Width TD.
c. Current from the Error Amplifier combines with decaying current from the Blocking Oscillator to switch the TD.
d. As the TD switches the Pulse Amplifier turns off; in turn, turning off the Stored Energy Switch.
16. Feedback through the Error Amplifier, therefore, maintains a constant output by varying the ON TIME -- the time the battery is connected to T1201 primary.
a. If the battery voltage increases, the ON TIME decreases -the output remains constant.
17. When the Stored Energy Switch turns off, the energy stored in T1201 is dumped into the load.
18. The Energy Storage Switch is a push-pull circuit.
a. First, one side of the transformer then the other is connected to the battery .
b. Two connections are made during each cycle of the multi.
c. The transformer receives a charge, therefore, first + then at a 3.75 kc rate.
19. Maximum time required for current into the inductor to reach 5.9a when the battery is $11.5 \mathrm{v}^{*}$ is $95 \mu \mathrm{sec}$.

$$
\text { a. } \begin{aligned}
e & =-L \frac{d_{i}}{d_{t}} \\
t & =-L \frac{i}{e} \\
t & =\frac{1.77 \times 10^{-6} \times 5.9}{11} \\
t & =95 \mu \mathrm{sec}
\end{aligned}
$$

b. 7.5 kc (the BO frequency) has a period of $133 \mu \mathrm{sec}$.
c. When e $=35 \mathrm{v}, \mathrm{t}=30 \mu \mathrm{sec}$.

* When the battery is 11.5 v , various lead loss and diode junction drops place 11 v at the inductor.

20. If the battery is connected to the inductor at a 7.47 kc rate (nominal BO frequency) for a long enough period of time to store 3.08 mj of energy each cycle, the 23 w load requirement will be met.
a. $\quad \mathrm{P}=$ watt-seconds $\times 7.47 \mathrm{kc} /$ second
b. $P=3.08 \times 10^{-3} \times 7.47 \times 10^{3}$
$P=23 w$
21. The $\pm 12 \mathrm{v}$ supply is the regulated operating supply for the Blocking Oscillator, the Multi, the Steering Switch, the Pulse Amplifier and the Error Amplifier.
22. The Starting Circuit supplies the above circuits on initial turn=on. a. When the $A C-D C$ supply begins to function, the Starter Circuit drops out, and the 12 v supply takes over.

## E. Energy Storage Switch; Q1174, Q1184

1. The Energy Storage Switch connects and disconnects the Input DC Supply to T1201 primary for a period indicated by the Pulse Width TD.
a. The length of time the supply is connected is in inverse proportion to the Input DC Supply potential.
(1) When the DC input is 11.5 v the supply is connected for $95 \mu \mathrm{sec}$.
(2) When the DC input is 35 v , the supply is connected for $30 \mu \mathrm{sec}$.
2. The switch is a push-pull transistorized electronic switch that connects the supply to the transformer primary at a 7.5 kc rate. a. The supply is disconnected by the Pulse Width TD through the Pulse Amplifier.
3. The circuit uses two transistors, five diodes and two zener diodes.
a. Q1174 and Q1184 are 151-163, 2N 189910 amp silicon NPN power transistor.
b. D1176 and D1186 are 151-180, 5a, 100 PIV silicon diodes.
c. D1 177 and D1187 are 6061 silicon signal diodes.
d. D1174 and D1184 are 152-069, 1N3041B, 75v, 5\%, 1w zener diodes.
4. Quiescently, Q1174 and Q1184 are cut off.
a. The bases and emitters are tied to the negative side of the DC power input.


TYPE 422 AC-DC POWER SUPPLY
B-422-0059 ENERGY STORAGE SWITCH
5. T1201 center tap is connected to the plus side of the DC power input.
a. The supply voltage may be at any level from 11.5 v to 35 v .
b. T1201 is wound on a 2 inch molypermaloy core.
c. In an attempt to quiet magnetostriction of the core at 7.5 kc , the transformer is dipped in silicon rubber and wrapped in sheet polyethatine foam before being inserted in its shield.
d. Primary inductance is $177 \mu \mathrm{~h}$, each side.
6. At the time the Blocking Oscillator fires, drive from the Steering switch and output from the Pulse Amplifier combine to induce a current in T1171 secondary.


* $35 v$ +DC Power Input level.
a. The current will be of a polarity to forward bias either Q1174 or Q1184, but not both.
b. Assume Q1174 saturates .
c. Q1174 collector pulls down to near zero volts (-DC Power Input).
d. Through D1176 and the saturation resistance of Q1174, the top end of T 1201 is pulled down to -DC Power Input level.
e. The DC Input potential is applied across the top half of T1201 primary.
f. Through transformer coupling, the bottom end of T1201 primary will rise to twice the DC power input voltage.
(1) T1201 primary center tap is connected to +DC Power Input.

7. When current flowing into T1201 primary has reached 5.9a (the current increases as a linear ramp), a signal from the Pulse Amplifier turns off the current into Q1174 base.
a. The transistor cuts off.
b. As the electromagnetic field collapses, a momentary inductive kick lifts the top of T1201 primary to about 50 v above the +DC Power Input.
(1) If the Power Input bus is 25 v or above (to total 75 v ), D1174 limits the rise at 75 v .
(2) D1174 protects Q1174 from base-collector breakdown.
(3) After the initial kick, the potential drops to 35 v above +Power Input level.
c. As coupling to the transformer secondary swings the bottom half of the secondary positive, D2 conducts dumping the stored energy into the capacitor and the load.
(1) D2 is the composite of all diodes connected to the bottom half of T1201 secondary.
d. The load placed on the transformer by D2 conduction clamps the top end of T1201 primary at 35 v .
e. Total transformer secondary current decreases as a linear ramp from the instantaneous maximum value.
f. The bottom of T 1201 primary drops to 35 v below the center tap voltage.
g. D1186 disconnects and Q1184 collector drops slowly toward 0 v with probe loading and/or transistor leakage current.
8. When T1201 secondary current has dropped to zero, D2 cuts off .
a. The entire circuit rings for several cycles at about 50 kc .
b. Both Q1174 and Q1184 are cut off during this period.
9. When the Blocking Oscillator again fires, the Steering Switch and the Pulse Amplifier send a current pulse through T1171 to turn on Q1184.
a. The transistor saturates.
b. Through D1176, Ol184 collector pulls the bottom end of T1201 primary to near the -DC Power Input level ( 0 reference).
c. Current again flows into T1201 at an increasing rate.
10. When the current reaches 5.9 a, a signal from the Pulse Amplifier cuts off Q1184.
a. The stored energy in T1201 is dumped into the load as DI conducts.
11. When the secondary current has dropped to zero, DI cuts off and the circuit again rings for a few cycles.
12. When the Blocking Oscillator again fires, a new cycle begins.
13. The ON time (the time interval that the DC input supply is connected to the transformer primary) is inversely proportional to the DC Power Input.
a. The Regulator will regulate the ripple out by varying pulse width (ON time) at ripple frequency.
b. 120 cycle ripple on the DC Power Input will, therefore, cause the ON time to change at a 120 cycle rate*.
c. The time interval change (with ripple) will appear as a jitter to any waveform of the Energy Storage Switching circuit.
14. As the rather high currents are switched on and off by Q1174 and Q1184, C1171 and C1172 supply the peak AC current surges.
a. L1 172 and L1 182 isolate the current changes from the DC Input Supply.
b. R1172 and R1182 lower the Q of the circuit so the inductors won't ring with the stray $C$ of the circuit.
15. C 1177 (and C 1187 ) protect the transistors during turn off.
a. At turn off, current into T 1201 is at a maximum at a time when voltage across the transistor tends to rise to a maximum.
(1) Without Cl177 (and C1187) peak switching power could be as high as 210 w .
b. When Q1174 turns off, D1177 conducts.

[^2]c. C1177 (and C1184) delay the change of voltage across Q1174 (and Q1184) until the high collector current falls to a lower value.
d. When Q1174 turns on, D1177 cuts off.
(1) Q1174 collector can pull down rapidly without waiting for Cl 177 to discharge .
e. Stored charge in the D1177 does pull some rather heavy current out of Cl 177 at the first instant of transistor turn on, however .
(1) During this brief period, L1 189 delays the current through the switching transistor until it saturates.
(2) D1189 prevents any inductive kick from L1 189 from adding to the already sizeable kick from T1201.
F. Steering Switch; Q1104, Q1114


1. The Steering Switch circuit provides the current pulse through Q1163 that turns on the Energy Storage Switch transistors .
a. The Steering Switch is controlled both by the Multi and by the Pulse Amplifier.
2. The circuit uses two transistors and two diodes.
a. Q1104 and Q1114 are 151-087, 2N1131 silicon PNP transistors.
b. D1104 and D1114 are 6061 silicon diodes.
3. Both emitters are tied to 12 v .
4. The bases are directly coupled to the Multi collectors.

D1115 Cathode

Q1114 Collector

Q1183 Emitter T1171 Primary Center Tap

D1114 Cathode

D1115 Collector Q1114 Base

Dl155 Anode

5. When the Blocking Oscillator fires, and the Multi switches, the Sieering Switch also switches .
a. One transistor turns off and the other on.
6. The conducting Multi transistor pulls down on its associated Steering transistor base turning it on.
7. Simultaneously (as the BO fires and the TD turns on), the Pulse Amplifier circuit ties the center tap of T1171 primary to the 0 v reference ( - DC Power Input).
8. Assume Q1114 has just turned on and Q1104 turned off.
a. Q1114 collector pulls up to 12 v .
b. D1114 connects, lifting the top end of T1171 primary to 12 v 。
c. Through inductive coupling, the bottom end of T1171 primary drops to -12 v .
d. The current drive in Tll71 secondary turns on one of the Stored Energy Switch transistors .
9. When the Error Amplifier senses that current into T1201 has reached 5.9a, the Pulse Amplifier lifts T1171 primary center tap to $12 v$.
a. The bottom end of T1171 primary (D1 104 cathode) raises momentarily to 24 v (from -12v) cutting off D1104.
b. The bottom end of T1171 primary then drops to 12 v .
10. When the BO fires, and the Multi switches, Q1104 conducts and Q1114 cuts off.
a. The switching spike from the Blocking Oscillator drops Q1104 and Q1114 bases about $2 v$-- the emitters and the 12 v bus drop about 1 v for the spike duration.
G. Multi; Q1105, Q1115

1. The Multi is a flip-flop multivibrator driving the Steering Switch transistors.
a. It is a $2: 1$ count-down device, triggered at a 7.5 kc rate by the Blocking Oscillator.
2. The circuit uses two transistors and two diodes*.
a. Q1105 and Q1115 are 151-103, 2N2219 silicon NPN transistors.
b. The diodes are 6061 silicon components .

3. The output is DC coupled to the Steering Switch transistor bases.
4. The multi triggered by a negative going 5 v spike from the Blocking Oscillator.

[^3]5. Assume Q1115 is conducting and Q1104 is cut off.
a. Q1115 collector sets at 11.2 v .
b. Q1105 collector is at 12 v .
c. About 5 ma flows through Q1115.
6. When the Blocking Oscillator fires, a negative going 5v spike of . $2 \mu \mathrm{sec}$ duration pulls down on D1105 and D1115 cathodes.

a. Q1115 cuts off.
b. Both transistors are turned off for the pulse duration.
c. The emitters drop about $3 v$ during the cut-off period.
7. The charge on the commutating capacitor, C1106, determines which transistor will turn on.
a. When conducting, Q1115 emitter sets about 200 mv more positive than Q1105 emitter.
b. When Q1115 cuts off, C1106 retains the 200 mv charge .
c. After the trigger pulse has passed, the transistor with the lowest potential on the emitter will conduct.
d. The charge on C1116 assures that the transistor previously cut off during the previous half cycle will now conduct.
e. Through multi action, Q1115 is held cut off as Q1105 conducts.
8. The multi switches at the 7.5 kc Blocking Oscillator rate.
9. With the opening of the return to T 1171 primary CT , the drop across the transistors changes as they stop conducting.
a. A step occurs on all waveforms in the Multi and Steering Switch circuits.
H. Blocking Oscillator, Q1120

1. The Blocking Oscillator is a free running sawtooth blocking oscillator, operating at a nominal frequency of 7.47 kc . a. The output drives the Multi and the Tunnel Diode.
b. The OSC FREQ control allows control of frequency $\pm 15 \%$ from the nominal 7.47 kc .
c. The control is necessary to compensate for tolerance in inductance values of T1201.
2. The circuit uses one transistor and three diodes.
a. Q1120 is a 151-103, 2N2219 silicon NPN transistor.
b. D1120, D1117 and D1118 are 6061 silicon diodes.
3. The BO transformer is composed of three 6 turn trifilar toroid windings on a ferrite core.
4. Q1120 base is set at 1.4 v by D1117 and D1118.

a. 5 ma is drawn from the Multi to provide the 1.4 v drop across the two silicon junctions.
b. C1117 holds the bottom of T1120 feedback winding solidly.
5. Q1120 emitter is returned to zero reference through two parallel paths; R1125, R1124 and R1123, D1155.
6. Q1120 collector is tied through T1120 to 12 v .
7. Q1120 will conduct when power is applied on initial turn on.

D1115 Cathode

Q1120 Emitter

Q1120 Base

a. As Q1120 collector pulls down (5v below the 12 v quiescent level), the negative going 5 v trigger spike appears across the Multi take-off winding to trip the Multi .
b. The emitter pulls up to $6 v$, discharging C1121.
c. A $5 v$ positive going spike from the feedback winding provides the $B O$ positive feedback.
8. The pulse is $.2 \mu \mathrm{sec}$ long .
a. As the inductive field collapses, Q1120 base drops to slightly below zero reference, then settles down at 1.4 v .
b. Q1120 cuts off.
c. D1120 prevents the inductive kick from lifting Q1120 collector above 12 v .
d. R1120 and C1120 isolate the current surges from the 12 v bus.
(1) About a volt of pulse does appear on the 12v supply, however.
9. After Q1120 cuts off, the emitter falls exponentially toward zero reference as C 1121 charges through the two emitter returns.
a. When Q1120 emitter reaches .8 v , the transistor again conducts, beginning the next cycle .
b. The time constant (and the BO frequency) is controlled by R1125, a screwdriver adjustment on the front of the AC-DC supply board.
I. TD and Pulse Amplifier; D1155, Q1163, Q1164


1. The Pulse Amplifier is a duty cycle control circuit (controlled by the TD) that turns off the Energy Storage Switching transistors when current into T1201 primary has reached 5.9a.
2. The output is a negative going 12 v pulse (from 12.6 v to .6 v ) that is fed to the center tap of T1171 primary.
a. The pulse controls the length of time the switching transistors stay on.
3. The circuit is a two stage DC coupled amplifier driven by D1155 and the Error Amplifier.
4. The circuit uses two transistors and a tunnel diode.
a. Q1163 is a $151-087,2 N 1131$ silicon PNP transistor .
b. Q1164 is a 151-103, 2N2219 silicon NPN transistor .
c. Dl155 is a TD-1, 1 ma tunnel diode .
5. Quiescently, D 1155 is in its low state.
a. Current from the error amplifier varies from 3.5 ma at AC low line to 4.6 ma at high line*.
b. 1 ma flows through R1163.
c. D1155, therefore, is reverse biased at something between 2.7 ma (low line) and 3.6 ma (high line) -- about 3 ma at 115 v line.
d. Q1164 is turned off placing its collector at 12 v .
e. Q1163, an emitter follower, is cut off with its emitter, the circuit output, at 12 v .
6. When the Blocking Oscillator (Q1120) fires, $\approx 6$ ma flows through R1123.

[^4]a. Dll55 is forward biased from 3.4 ma to 4.3 ma depending on line voltage.
b. The 1 ma TD switches to its high state .
c. As D1155 anode raises approximately $450 \mathrm{mv}, \mathrm{Q} 1164$ saturates, pulling Q1163 base down to near zero volts (relarive to the minus $D C$ power input).
d. Dll63 emitter pulls down to about lv.
e. Current for the Steering Switch circuit is supplied through Q1163.

D1155 Anode

Q1120 Emitter

Q1163 Emitter T1171 Primary Center Tap

7. After the Blocking Oscillator fires, Q1 120 emitter voltage begins to fall exponentially.
a. Current through R1123 will decrease at the same rate.
8. When current through D 1155 reaches $180 \mu$ (TD valley current), the TD will switch to its low state .
a. The time interval the TD will remain in its high state depends upon the coincidence of the decaying current through R123 and the Pulse Width control current from the Error Amplifier .
b. The Error Amplifier Pulse Width control current is a direct function of any error in the AC-DC Supply output.
c. When the algebraic sum of all the currents at the junction of D1155, R1123, R1162 and the Error Amplifier output equals $180 \mu \mathrm{a}$, the ID switches.
9. Q1164 cuts off -- its collector rises to 12 v .
a. Q1163 emitter follows to 12 v .
b. The current supply to the Steering Switch circuit has been removed.
c. The Stored Energy Switch turns off.
10. When the BO fires again, a new cycle begins.
J. Error Amplifier; Q1134, Q1144, Q1154

1. The Error Amplifier supplies a current to the TD and Pulse Amplifier that is in direct proportion to any error in the AC-DC supply output.
2. The circuit uses three transistors, three diodes, and a zener diode.
a. Q1134 is a 151-133, MM999, silicon PNP transistor.
b. Q1144 is a $151-087,2 N 1131$ silicon PNP transistor .
c. Q1154 is a 151-103, 2N2219 silicon NPN transistor with relaxed specs.


TYPE 422 AC-DC POWER SUPPLY
B-422-0062
ERROR AMPLIFIER AND I2v SUPPLY
4-12-'65 d/ ${ }^{-14)}$
d. D1132, D1232 and D1233 are 6061 silicon signal diodes, although D1232 and D1233 are used as supply rectifiers.
e. D1135 is a 151-123, 1N935A, 9v 5\% zener.
3. The error signal is taken from a secondary winding of T1201.
a. The voltage is rectified (full wave) to $+12 v$ by D1232 and D1233.
b. About 12 ma is drawn from the supply.
4. R1232 and C1232, C1233 filter the rectifier output.
a. The 7.5 kc switching frequency is filtered to about 150 mv , but not the 100 cycle to 800 cycle ripple frequency from the $A C$ line.
b. The Error Amplifier must follow the 800 cycles in order to regulate the ripple out of the supply at 400 cycle line .
c. R1232 and C1232, C1232 $T_{c}$ is equal to the $T_{c}$ of the $\pm 12 v$ scope supply.
5. A portion of the error signal is picked off the error divider (R1131, R1130, R1132) and applied to Q1134 base .
a. D1135, the 9 v zener, is used as reference.
b. The error signal is compared with the reference voltage in Q1134.
(1) The error divider and the zener divider are connected in a bridge configuration with Q1134 sensing its output.
c. R1130, the -12 v adj, is set to -12 v at pin 7 of the blue ribbon connector.
d. D1132 temperature compensates Q1134 base-emitter junction.
e. C1133 across Q1134 junction and R1136 constitute a time constant that will not pass 7.5 kc but will allow the Error Amplifier to sense the line ripple.
6. The amplified error voltage is DC coupled to Q1144 base.
7. Amplified in Q1144, the signal is applied, DC coupled, to Q1154 base.
8. Further amplified in Q1154, the amplified error signal appears as a varying current through R1154.
a. This current plus the current through R1161 is fed to the Pulse Width TD to help switch the TD to its low state .
b. The current will vary from 3.5 ma at low AC line to 4.6 ma at high AC line.
c. About . 8 ma of 120 cycle ripple current is present through R1154 at 115v AC line.
d. For DC input, current through R1154 and R1161 varies from 2.75 ma at 11.5 v to 5 ma at 35 v .
9. The Error Amplifier is the only circuit receiving power from the minus side of the $\pm 12 \mathrm{v}$ supply.
K. $\quad \pm 12 \mathrm{v}$ Regulator Supply

1. The supply provides operating power for the regulator circuits.

a. The supply output (nominally 12 v ) will vary with varying the load from low to high line.
b. The load changes as the pulse width (from the Pulse Amplifier) changes.
2. The supply has its own T 1201 secondary.
3. Two full wave rectifiers (all 6061 silicon diodes) supply the plus and minus 12 volt DC outputs.
4. The plus 12 v supply is "brute force filtered" by C1195 and C1199.
a. The primary consideration is the reduction of the 7.5 kc ripple.
b. The 120 cycle ripple is removed by regulation.
5. The minus $12 v$ supply uses a Pi filter with C 1246 , L 1246 and C 1245 .
6. The plus side delivers $25-30 \mathrm{ma}$ at high line.
7. The minus side delivers 2 to 6 ma.
L. Starter Circuit; Q1193, Q1194
8. The Starter Circuit provides power to the regulator circuits during initial turn on.
a. The circuit supplies $7.5 v$ to the $12 v$ bus.
b. When the 12 v supply comes on, the Starter Circuit drops out.
9. The circuit uses two transistors, a zener diode and a signal diode.
a. Q1193 is a 151-103, 2N2219 silicon NPN transistor with relaxed specs.
b. Q1194 is a 151-087, J3138 silicon PNP transistor enclosed in a thermalloy heat sink.
c. D1192 is a 1 N755A, $7.5 \mathrm{v} 5 \%$ zener.
d. D1191 is a 6061 silicon signal diode.
10. When power is first applied, D1192 and D1191 set Q1193 base at 8.2 v .

a. The amount of zener current will vary from .76 ma (DC power input at 11.5 v ) to 6.2 ma (DC power input at 35 v ).
11. Q1193 conducts.
a. As Q1193 collector drops, it turns on Q1194.
b. Q1194 supplies current to the +12 v bus .
c. Q1193, Q1194 now become a series regulator circuit with the 12 v bus setting at 7.5 v (.7v below Q1193 base).
d. Q1194 saturates while C1195, C1199 is charging.
(1) During this period (about 2 msec ), Q1194 collector is pulled up to the power input supply voltage.
e. After C1194, Cl199 have charged, Q1194 collector drops to about 7.5 v .
12. When the 12 v supply comes on (in about 200 msec ), it lifts Q1193 emitter to cut off.
a. As Q1193 cuts off, its collector rises, turning off Q1194.
13. D1191 temperature compensates Q1193 base-emitter junction.
a. Without D1 191 the switching transistors might not switch at low temperatures due to inadequate drive.
b. If the zener is at the low end of its $5 \%$ tolerance rating, and low temperature has increased the junction drop across Q1193 base-emitter, the 12 v bus would set somewhat below 7.5 v .
c. At low temperatures, the drop across D1191 would increase enough to compensate for the increased drop across Q1193.
d. Use of a higher voltage zener would require a lower value for R1191, thereby increasing the zener current at high line.
(1) The choice of the lowest value zener and the highest value for R1191 to do the job assures a relatively low stand-by current .
M. $\quad \pm 12 v$ Scope Supply
14. The $\pm 12 \mathrm{v}$ Scope Supply output is used in every major circuit in the scope.
a. The 12 v supply delivers about 280 ma .
b. The -12 v side delivers about 260 ma .
c. Dynamic output impedance is about $1 \Omega$ (the 12 v Series Regulators in the AC supply have less than $.1 \Omega$ output Z).
d. The scope load is designed to be constant.
(1) Although the $A C-D C$ supply regulates effectively with line voltage changes, it is less effective with changes in load.


TYPE 422 AC-DC POWER SUPPLY $\pm 12 v$ SCOPE SUPPLY

B-422-0064
4-7-'65dl
2. Both the plus and minus supplies have identical full wave rectifiers.
a. D1212, D1213, D1216 and D1217 are 152-179, SM1004, la diodes with 50 v PIV.
b. A Pi filter on each side of the supply reduces the 7.5 kc ripple to about 20 mv .
(1) 120 cycle ripple is reduced to about 5 mv by the Regulator.
3. L1219, Cl 219 (and $\mathrm{L} 1213, \mathrm{Cl213)}$ suppress a 10 mc oscillation on the $\pm 12 \mathrm{v}$ leads to the indicator.
4. A separate full wave rectifier supplies the graticule lights.
a. D1214 and D1215 are 6061 signal diodes.
b. The two 336 bulbs are rated at 80 ma each at 14 v .
c. With the AC-DC supply, they operate at 12 v .
5. The $\pm 12 \mathrm{v}$ supply uses the center section of T1201 center tapped secondary.
a. The waveform could be loosely described as a series of pulses at a 3.75 kc rate.
b. The AC voltage is used to drive the rectifiers and to drive the High Voltage Transformer*.

Pin 1
Blue Ribbon Connector


[^5](1) The CRT supply uses about 5 w .
c. Portions of the waveform can be described as follows:
(1) Area A: One of the switching transistors connects the battery to the transformer .
(2) Area B: D1212, D1215 and D1217 conduct.
(3) A period of 50 kc oscillation.
(4) Area C: The other switching transistor connects the battery to the transformer.
(5) Area D: D1213, D1214 and D1216 conduct.
(6) 50 kc oscillation.
5. The -12 v potential can be set by the -12 v adj in the Error Amplifier.
N. $55 \mathrm{v}, 95 \mathrm{v}$, and -110 v Supplies

1. The 55 v supply is taken from the second set of taps (from the center) of T1201 secondary.
a. A full wave rectifier using 6061 diodes, supplies 51 ma to the scope.
b. Source impedance is about $27 \Omega$.
c. C 1204 reduces the 7.5 kc ripple to about .6 v .
d. C1205, L1204 suppress a 10 mc ringing on the 55 v lead to the indicator.
2. The 95 v supply is taken from the output tap of T 1201 secondary winding.
a. A full wave rectifier using 152-224 (300 PIV) diodes delivers 16 ma to the scope.
b. Source impedance is $78 \Omega$.
c. A simple capacitive filter reduces the 7.5 kc ripple to about 800 mv .

3. The -110 v supply is taken from one side of the 55 v transformer secondary winding.
a. A half wave voltage doubler using 6061 diodes, supplies 7.4 ma to the scopes -81 v regulator.
b. About 500 mv of 7.5 kc ripple is present at the blue ribbon connector.
O. Grounds
4. The relatively high switching currents and voltages present in the AC-DC Supply necessitate some careful grounding considerations.
5. Several factors contribute to the grounds problem.
a. The AC-DC Power Supply is mounted on two etched wiring boards.
b. Several support brackets and/or chasses are used.
c. The chasses are not bonded together or grounded except by the cabinet.
d. All grounds shown in the illustrations (AC-DC Supply and AC-DC Power Selector, Sections 12 and 13) are ground points or ground plates on the PC boards and tied through pins 17 and 22 (blue ribbon connector) to the scope chassis.
e. In the EXT DC mode, the -DC POWER bus (Ov reference) is not grounded to the indicator chassis.
f. Some of the circuits are physically separated by the hole in the chassis that provides space for the CRT neck.
g. The transformer ( T 1201) has approximately $1 \mu \mathrm{~h}$ primary to secondary leakage inductance and about 230 pf leakage capacitance.
h. The switching transistors (Q1174, Q1184) switch 5.9 amp peak AC current -- fast.
i. The switching transistors (Q1174, Q1184) collectors swing up to 75 v -- fast .
h. The result was the presence of switching currents, ringing at about 10 mc , in the scope chassis and cabinet.
(1) The currents would interfere with sensitive circuits throughout the instrument.

6. One problem area was the mounting chassis and end-plate that houses the switching transistors, Q1174 and Q1184.
a. The transistor cases are tied to the collectors.
b. The transistors are quite large, offering rather high capacitance coupling to the mounting chassis.
c. Simultaneously, capacity currents couple from T1201 primary to the secondaries and thence to ground.
(1) The Error Amp secondaries and $\pm 12 \mathrm{v}$ Regulator Supply

Secondaries return to ground through C1232 and C1233 .
e. These switching currents must be short coupled back to the switching circuit rather than flow back to the switching circuit through the scope and scope cabinet.
f. A current path is provided through the common grounds at T1201 secondary center taps, through C1173 and C1183 to the switching circuit.
(1) Both the plus and minus sides of the switching circuit are driven common mode by the two capacitors.
g. Currents, coupled to the switching transistor mounting chassis, are coupled through C 1181 to the common ground point and returned through C1173 and C1183 to the switching circuit.
(1) When the cabinet is installed, the mounting chassis is grounded through the cabinet to the scope main frame.
(2) C 1181 , therefore, is grounded at both ends.
(3) The function of the capacitor, however, is to provide a short return path to the switching currents from the mounting chasses to Q1174, Q1184 emitters.
4. The -DC POWER INPUT BUS (0 reference voltage) also presents a problem in returning currents.
a. The pulse out of the Pulse Amplifier pulls about 80 ma out of the 12 v supply (via the Steering Switch circuit)
b. The $12 v$ bus (on the PC board) circles around the CRT access hole -- a distance of about 8 inches.
c. The current pulse sets up an inductive field around the 12 v bus that radiates to adjacent circuits .

d. The negative return is placed parallel to the 12 v bus on the back side of the PC board; separated only by the board base material.
e. The negative return runs the full length of the 12 v bus, connecting to the -DC Power input at a tie point near the 12 v supply.
(1) Also connected to the same tie point are the $\pm 12 \mathrm{v}$ Power supply returns and their filter capacitors.
f. Since the same current pulse flows in the ground return as flows in the 12 v bus, the inductive fields cancel.
g. The main current return is located at the low end of the Zener Reference Bridge .
(1) The Error Amplifier, Pulse Amplifier, Pulse Width TD and the Transformer (T1201) feedback winding are returned to the same tie point.
h. R1163 (2.7 ) is connected between the Pulse Amplifier end of the negative return bus and the adjacent -DC Power Input tie point.
(1) The resistor prevents T1171 primary return current from flowing through the reference return, while still providing a ground reference from Q1163 to the adjacent-DC Power Input tie point.
(2) The return current flows through a separate return to the low side of the +12 v supply.
(3) A DC short appears across the resistor since both ends eventually return to the -DC Power Input.

## XIII. AC-DC POWER SELECTOR

A. The Power Selector circuit includes the POWER MODE switch, the Battery Charger, and the Low Voltage Indicator circuit.

1. The POWER MODE switch, located in the AC-DC supply's rear panel, selects six operating modes:
a. 115v.AC-CHARGE
b. 115v AC - OPERATE
c. INT BAT - OPERATE
d. EXT DC - OPERATE
e. $230 v \mathrm{AC}$ - OPERATE
f. $230 v A C-C H A R G E$


TYPE 422 AC-DC POWER SELECTOR
B-422-0068
BLOCK AND SWITCHING DIAGRAM
4-23-65 dl
2. The Battery Charger provides a constant 400 ma charge rate.
a. It requires about 12 hours to fully charge a set of fully discharged batteries.
b. Batteries are trickle charged at a 20 ma rate in the $A C$ operating mode.
c. AC voltage tolerance, when charging, is $+10 \%,-20 \%$ for 45 cps to 440 cps .
3. The Low Voltage Indicator circuit causes the front panel POWER indicator light to blink when the batteries have reached their low operating limit.
a. The scope will operate about 4 hours on a set of fully charged batteries.
b. The scope should not be operated more than 15 minutes after low batteries are indicated.
B. AC Inputs

1. The use of $A C$ power requires the use of a special three wire power cord.
a. The power plug is indexed in such a way that the AC cord cannot be connected to the DC input section of the power jack.
2. The $A C-D C$ supply will operate on $115 v A C \pm 20 \%$ or $230 v A C$ $\pm 20 \%$ from 50 cps to 440 cps .
a. The supply can be operated at 45 cps , but the upper operating voltage limit is reduced to $10 \%$.
b. No "EXPORT" taps are required.
c. The wide (voltage) range of operation is due to efficient regulation of the $A C-D C$ supply.
3. The scope and the AC-DC supply use a typical $27 w$ when operated on $A C$.

4. $\quad 115 v( \pm 20 \%)$ or $230 v( \pm 20 \%)$ is selected by means of the POWER MODE switch.
a. The transformer primaries are connected in parallel for 115 v operation and in series for 230 v operation.
b. The AC input circuits are also used when the POWER MODE switch is in its two CHARGE positions.
5. The fuse must be changed when switching from 115 v to 230 v operation*. a. F1000, the primary fuse, is .5a 3AG Slo-Blo for 115 operation. b. A. 3 a 3 AG Slo-Blo is used for 230 v .

* At time of printing, a $3 / 4$ fast blo was being considered for both voltage ranges.

6. A line filter with a cut off at 1 mc is composed of T 1000 and C1000.
a. T1000 is composed of two 10 turn bifilar windings on a toroid core .
7. TK 1000 is a $158^{\circ} \mathrm{F}$ thermal cut-out protecting the AC input.
8. A single center tapped power transformer secondary is used.
9. Four MR1032A silicon diodes are used in a tapped bridge configuration to supply the two DC voltages.
a. The negative end of the bridge is tied to the -DC Power Output bus.
(1) The -DC Power Output is the 0 reference in the AC-DC supply.
(2) The -DC Power Output is grounded when the POWER MODE switch is in AC OPERATION or CHARGE.
b. The top of the rectifier bridge is used to power the Battery Charger .
(1) The DC varies from 40 v at low line to 65 v at high line.
c. The transformer ( $\mathbf{T} 1001$ ) secondary center tap supplies the AC-DC Regulator.
(1) The supply is termed the +DC Power Output.
(2) The +DC Power Output varies from 18 v at low line to $32 v$ at high line.
(3) It is connected by means of the POWER MODE switch in the two AC OPERATE positions.
10. The +DC Power Output bus is broken by a section of the POWER switch.
a. The bus also passes through pins 24 and 13 of the blue ribbon connector where a jumper provides an interlock. b. TK 1039, a $158^{\circ} \mathrm{F}$ thermal cutout, protects the supply.
(1) TK 1039 and TK 1000 are mounted adjacent to the power transformer to sense transformer overheating.
(2) TK 1039 also senses the temperature of the switching transistors.
11. C1003 and C1004 filter the supply to about 2 v of 120 cycle ripple (low line).
12. An attempt to operate the scope on 115 v with the POWER MODE switch in the 230 v position will drop the supply out of regulation, but a display may be seen.
a. If the switch is in the 115 v position when connected to 230 v , the primary fuse, F 1000 , will blow*.

## C. DC Inputs

1. When operated on EXT DC, a special 3 wire power cord is used. a. The cord is indexed so that it cannot be connected to the $A C$ input.
b. The plug can be inserted in just one way, thereby assuring proper DC polarity -- providing the supply end of the cable is connected properly.
c. There is $a \simeq .3 \mathrm{v}$ drop in the power cord provided (at 11.5 v input).
2. In the EXT DC - OPERATE position of the POWER MODE switch, the minus side of the External DC Input is connected to the -DC Power Input bus ( 0 v reference) .
*Additional damage may occur. At printing time further protection was being investigated.
a. The minus bus is isolated from chassis ground.
b. The minus end of the DC input supply can be elevated $\pm 200$ v (relative to chassis) .

3. The scope is designed to operate on DC supply voltages of 11.5 v to 35 v .
a. The AC-DC supply and the scope uses a typical 23 w from the DC line.
4. A line filter with a 1 mc cut-off frequency consists of $\mathrm{T} 1010, \mathrm{C} 1010$, C1011 and C1012.
a. T1010 is composed of two 10 turn bifilar windings on a toroid core.
5. F1015 fuses the DC input.
a. The supply is shipped with a 3a 3AG Fast Blo.
6. Should the EXT DC supply become reversed, D 1014 will conduct, blowing F1014.
a. F1014 will blow even though the POWER switch is OFF
7. The POWER switch opens the DC line after having passed through three sections of the POWER MODE switch.
8. TK 1039, the $158^{\circ} \mathrm{F}$ thermal cutout, protects DC line.
9. After passing through the interlock at the blue ribbon connector, the DC line ties to the +DC POWER INPUT.

## D. Internal Battery Operation

1. Twenty $1.2 \mathrm{v}, 3.5 \mathrm{amp}$-hour Nickle Cadmium batteries are connected in series to power the scope in the INT BAT - OPERATE mode.
a. The scope should operate for approximately four hours of continuous operation on a set of fully charged batteries.
b. The front panel POWER indicator light will blink to indicate discharged batteries.
c. The scope should not be operated longer than 15 minutes after the light begins to blink.
(1) Prolonged operation will probably reverse the polarity of one of the batteries.
(2) Since a reversed polarity battery takes considerably longer to charge, it will probably not reach a charge during the normal charge cycle.
(3) Consequently, there will be considerable cell unbalance after many cycles where the battery pack is allowed to go into deep discharge.
d. Fully charged, total battery voltage is nominally 28 v .


TYPE 422 AC-DC POWER SELECTOR B-422-0072
DC INPUTS
5-3-'65d|
2. The battery pack and batteries weigh about 6 pounds.
3. If the batteries are installed in the battery pack so their polarities are reversed, F1014 will blow, even though the POWER switch is OFF.
4. The 20 batteries are soldered in series to assure a good noncorrosive connection.
5. The battery output passes through TK 1039, the POWER switch, and the interlock before tying to the + DC INPUT POWER bus .
6. The minus side of the battery pack is tied to the - DC Input Power bus ( 0 v reference) and ground.
E. Battery Charger; Q1023, Q1033


1. The Battery Charger provides a constant 400 ma charge rate to the $201.2 v$ internal batteries.
a. Batteries reach a full charge in about 12 hours.
b. AC line voltages in the CHARGE modes are limited to $115 v+10 \%-20 \%$ from 45 cps to 440 cps .
2. The circuit uses two transistors, a zener diode, and a rectifier diode.
a. Q1023 is a 151-135, 2N3053 NPN silicon transistor.
b. Q1033 is a $151-148$, RCA 40250 NPN silicon transistor mounted on an aluminum chassis.
c. D 1022 is a $1 \mathrm{~N} 755 \mathrm{~A}, 7.5 \mathrm{v} 5 \%$ zener diode .
d. D1016 is a $152-198$, MR 1032A 3a silicon diode with a 200v PIV rating.
3. Battery charger power is taken from the top of the silicon bridge.
a. The voltage will vary from 40 v at low line to 65 v at high line.
4. The Charger operates at 400 ma in the two CHARGE positions of the POWER MODE switch and at a 30 ma trickle charge rate in AC OPERATE modes.
5. Q1023 is a voltage setting device and Q1033 is the current source for the batteries under charge.
6. D 1022, the 7.5 v zener, sets Q1023 base about 8 . Iv above the battery voltage (D1016 raises the battery voltage by .6v) .
7. The 8.1 lv level (above the batteries) at Q1023 base is dropped $1.2 v$ across the two base-emitter junctions of Q1023 and Q1033 to a level of 6.9 v (above the batteries) at Q1033 emitter.
a. Since the voltage drop across R1033 is constant, the charging current through it is constant.
8. TK 1033 , a $105^{\circ} \mathrm{F}$ thermal cutout, is located (physically) close to the battery compartment to sense when the ambient temperature is too high to safely charge the batteries.
a. When the cutout opens, the charger switches to trickle charge.
9. In the trickle charge positions, R1031 is added to R1033 making a total $196 \Omega$ emitter return resistance for Q1033.
a. Trickle charge current becomes 30 ma .
10. D1016 disconnects when the Battery Charger is off, preventing leakage discharge of the batteries.
E. Low Voltage Indicator; Q1045, Q1055
11. The Low Voltage Indicator operates in the INT BAT - OPERATE mode of the POWER MODE switch to indicate discharged batteries.
a. The POWER indicator light blinks at a $1 / 2 \mathrm{cps}$ rate when the voltage at pin 13 (blue ribbon connector) falls below 22 v 。
12. The circuit uses two transistors, four signal diodes and a zener diode.
a. Q1045 is a 151-087, 2N1131 PNP silicon transistor.
b. Q1055 is a 151-096, 2N1893 NPN silicon transistor.
c. D1042, D 1054, D 1055 and D1057 are 6061 silicon diodes.
d. D1041 is a 1 N 962 , $11 \mathrm{~V} 5 \%$ zener diode.
13. Q1045 and Q1055 form a bistable multi .

a. The multi has a "both on" - "both off" sequence.
b. When the batteries are adequately charged, both transistors are turned off.
14. Q104.5 emitter is returned through D 1042 to a 11 v zener supply. a. $\quad 1.6$ ma through R 1041 holds the diode in its zener range.
15. A divider composed of R 1046, R 1047 and R1048 is connected across the battery when the POWER MODE switch is in the INT BAL OPERATE mode.
a. About 1 ma flows through the network.
16. R1047, the LOW VOLTAGE INDICATOR adi, is set to place Q1045 base in the cut-off range.
a. Q1045 compares a sample of the battery voltage with the zener reference.
b. R1047 is a screwdriver adjustment located on the AC-DC Power Selector board.
c. It is adjusted by connecting a variable power supply to the battery terminals.
d. Starting at 35 v , reduce the supply voltage slowly to 22 v .
e. Adjust R1047 slowly until the pilot light begins to blink.
17. With Q1045 cut off, its collector holds Q1055 base at ground.
18. Q1055 is also cut off.
a. The collector is pulled toward 95 v .
b. D 1054 and D1055 are cut off.
19. The POWER neon (pilot light) is conducting with current flowing through two paths to 95 v .
a. About $40 \mu$ flows through R1059.
b. About $400 \mu$ flows through D1057 and R1057.
20. When the voltage at pin 13 (blue ribbon connector) has dropped to 22 v , Q1045 begins to conduct.
a. As Q1045 collector rises, it lifts Q1055 base into conduction.
b. As Q1055 collector drops, D1054 conducts pulling down on Q1054 base.
c. This constitutes multi feedback, switching both transistors to saturation -- "both on" state.
21. Q1055 collector pulls down to ground.
a. As D 1057 cuts off, a relaxation oscillator is formed of the POWER neon and C1047.
b. The circuit oscillates at a $1 / 2$ cycle rate.
22. When the neon fires (with each cycle), D1055 conducts preventing Q1055 collector from being driven negative.
23. D1042 prevents Q1045 base-emitter junction from reverse breakdown damage when operating in the other than INT BALOPERATE position of the POWER MODE switch.
a. In these positions, Q1045 base is pulled up to the +DC POWER OUTPUT potential ( 11.5 to 35 v ) while the emitter returns to llv.
24. C1041 prevents the circuit from indicating "low batteries" on initial turn on, by allowing Q1045 emitter supply to come up slowly.
a. If Q1045 emitter voltage came up before the base, the multi would start in its "both on" state (the POWER neon would indicate low batteries).
b. The multi has a rather wide (about 8 v ) hysteresis).
c. Once the multi is in its "both on " state, the battery potential would probably not be high enough to switch it to its "both off" state.
d. The POWER neon would continue to indicate "low batteries".

| CH 1 INPUT AMP | SWEEP GENERATOR |
| :---: | :---: |
| B-422-0001 | B-422-0028 |
| 0002 | 0029 |
| 0003 | 0030 |
| 0004 | 0031 |
| 0005 | 0032 |
| 0006 | 0033 |
| 0007 | 0034 |
|  | 0035 |
| CH 2 INPUT AMP | 0036 |
| CH 2 NPUT AMP | 0037 |
| B-422-0008 |  |
| 0009 | HORIZONTAL AMPLIFIER |
| VERT SWITCHING AND OUTPUT AMP | B-422-0038 |
|  | 0039 |
| B-422-0010 | 0040 |
| -0011 | 0039 |
| 0014 | 0041 |
| 0015 |  |
| 0014 | CRT AND HIGH VOLTAGE |
| 0016 | CRT AND HIGH VOLTAGE |
| 0019 | B-422-0042 |
| 0016 | 0043 |
| 0017 | 0044 |
| 0018 | 0045 |
| 0012 | 0046 |
| 0013 |  |
| SWEEP TRIGGER | CALIBRATOR |
|  |  |
| B-422-0020 | B-422-0047 |
| $\begin{aligned} & 0020 \\ & 0021 \end{aligned}$ | 0048 |
| 0022 |  |
| 0025 |  |
| 0023 OC REGULATORS |  |
|  |  |
| 0027 | B-422-0050 |
| 0024 | 0051 |
| D-12a-0008 |  |
| B-422-0024.1 | AC POWER SUPPLY |
|  | B-422-0053 |
|  | 0054 |
|  | 0056 |
|  | 0055 |

422 Slide List (cont.)

```
AC-DC POWER SUPPLY
B-422-0057
            0058
            0073
            0057
            0 0 5 9
            0074
            0060
            0075
            0 0 6 0
            0076
            0 0 6 1
            0077
            0061
            0078
            0062
            0063
            0064
            0 0 7 9
            0065
            0066
            0067
```


## AC-DC POWER SELECTOR

```
B-422-0068
0069
0072
0070
0071
```

SCHEMATIC SLIDES FROM MANUAL
B-422-0150
C-422-0001
0005
0010
0015
0020
0025
0030
0035
0040
0045
0050

## Schematic Symbols

The following symbols are used on the schematics:


Screwdriver adjustment.
Front-panel control or connector.
Connection made at indicated pin on etchedwiring board.

Connection soldered to etched-wiring board.
Blue line encloses components located on etched-wiring board.
Input from or output to indicated schematic.


## IMPORTANT

## VOLTAGE AND WAVEFORM CONDITIONS

Circuit voltages measured with $20,000 \Omega$ /voit VOM. All readings in volts.
Waveforms shown are actual waveform photographs taken with a Tektronix Oscilloscope Camera System and Projected Graticule. Test oscilloscope was DC coupled (except where noted) using a $10 \times$ Probe.

Voltage and waveform measurements given on the schematics are not absolute and may vary between instruments. Apparent differences between voltage levels measured with the voltmeter and those shown on the waveform are due to circuit loading.

Voltages and waveforms are indicated on the schematics in blue.
Voltage readings and waveforms were obtained under the following conditions:
Vertical Controls (both channels where applicable)
VOLTS/CM . 05
VARIABLE CAL
AC GND DC GND
POSITION Midrange
Mode CH 1
INVERT Pushed in
$\times 10$ GAIN AC
Pushed in
Horizontal Controls
POSITION Midrange
TIME/DIV . 5 mSEC
VARIABLE
CAL
$\times 10$ MAG
Pushed in
Triggering Controls

Source
Coupling
SLOPE
LEVEL

Other Controls
INTENSITY
FOCUS
ASTIGMATISM
SCALE ILLUM
POWER
Line voltage
Signal applied

CH 1 \& 2
AC
Positive going
Centered (AUTO for waveforms)


(2) INPTT AMAMLLIFER













[^0]:    * Hold-off may be as short as $2 \mu \mathrm{sec}$ at faster sweep rates if C 401 doesn't get a change to fully discharge to -12 v .

[^1]:    * See Sweep Generator, page 6-17.

[^2]:    * Ripple frequency will increase with the input line frequency, of course, to a maximum of 800 cycles.

[^3]:    * Early instruments had diodes in series with R1106 and R1116 also.

[^4]:    * Operation on EXT DC would increase the range of currents out of the Error Amplifier to 2.75 ma at 11.5 v DC input and 5 ma at 35 v DC input.

[^5]:    * See CRT and High Voltage, Section 8.

