Tektronix®
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MULTIPURPOSE TEST STATION

M.P.T.S.

GPIB programmable

SWITCH MATRIX

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number 3

Ø62-65Ø1-ØØ

PORTABLE MPTS TEST ENG.

FIRST PRINTED 22-Mar-85

Printed in U.S.A. Specification and price change privileges are reserved.

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

STATIC-SENSITIVE COMPONENTS

The following precautions are applicable when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by their bodies, never by their leads.

Table 6-1
Susceptibility
to Static Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]Voltage equivalent for levels: (Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

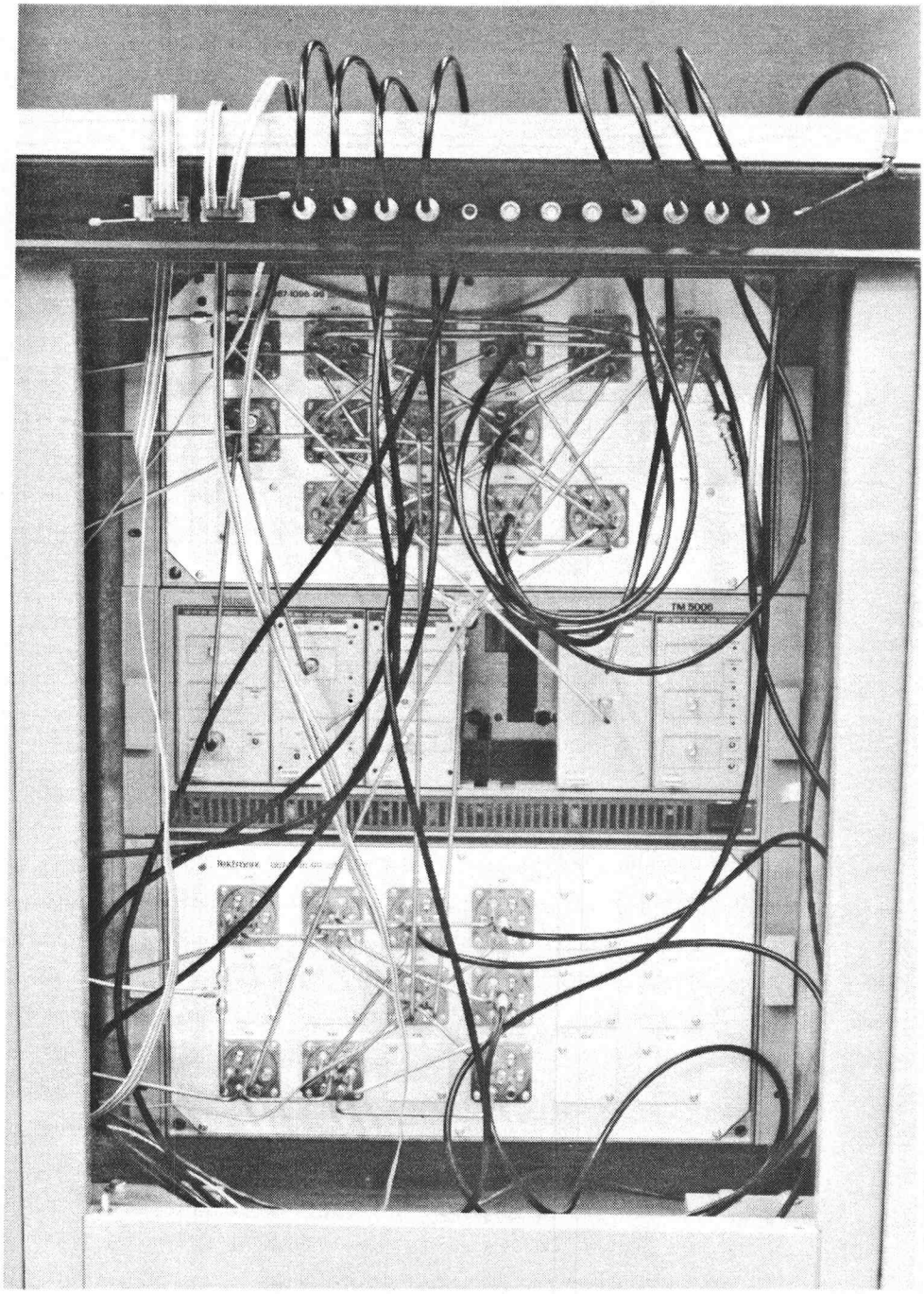
1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V(est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.



Frontispiece: I/O Switching Matrices

SECTION 1

INTRODUCTION AND SPECIFICATION

1.1 DESCRIPTION

The Ø67-1Ø96-99 Switching Matrix provides microwave path switching for the Ø67-1Ø93-99 MPTS Automatic Test System. It is a GPIB programmable instrument with a 5Ø ohm characteristic impedence. The matrix configuration is a 6 by 6 crosspoint, ie each of the six inputs can be connected to any of the six outputs. A 6 to 1 preselector (a switch with 6 inputs, one output) is in series with each of the 6 inputs. This makes a 36 by 6 crosspoint configuration. Crosspoints and preselectors can by programmed separately: any combination of relay closures can be made simultaneously. However, if more than one crosspoint is closed on any one path, the impedance of the path will no longer be 5Ø ohms.

1.2 GENERAL SPECIFICATIONS

Power:	1Ø9-125/218-25Ø VAC 47/63 Hz 15Ø VA
Configuration:	36 x 6 crosspoint when the six, 6 : 1 preselectors are included.
Interface:	IEEE-STD-488-1978 L2
Device Address:	Switch Selecteble

1.3 PERFORMANCE SPECIFICATIONS

Closed Path

Frequency:	DC to 3 GHz
Risetime:	< 70ps
Impedance:	50 ohms
VSWR:	<=1.2 : 1
Insertion Loss:	<= 1.0 db @ 1 GHz <= 1.5 db @ 2 GHz <= 2.0 db @ 3 GHz
Isolation:	> 60 db @ 100 MHz > 52 db @ 300 MHz
Thermal Offset:	<= 100 uV
DC Resistance:	<= 100 mohm
Max Voltage:	200 Volts

Open Path

Max Voltage:	1000 V (contact to contact) 1000 V (contact to shield)

Transition

Switching Time:	<= 500 ms
Power:	50 Watts (average)

Reliability

MTBF:	>= 1,000,000 cycles per contact

1.4 PHYSICAL CHARACTERISTICS

Size:	8.75"x19"x20" Rack Mountable
Weight:	30 lb.

SECTION 2

OPERATOR/PROGRAMMER INSTRUCTIONS

2.1 INSTALLATION AND REMOVAL, GENERAL

The front panel of the switching matrix has mounting holes to install up to 18 single-pole-six-throw, SP6T, solenoid-activated microwave coaxial switches. Depending on the system requirements where the switching matrix is being applied, there may be fewer than 18 relays installed. The card cage backplane, however, is always wired to energize all 18 relays.

The rack mounts for the matrix are standard 19 inch which slide out.

In MPTS, the number of relays on the input matrix is different from that for the output matrix. This difference is shown by the following table which is ordered according to the physical placement of the relays.

TABLE 2-1: MPTS INPUT MATRIX RELAY CONFIGURATION

K11	K21	K31	K32	K22	K12
K16	K26	K36	K33	K23	K13
				UNUSED	UNUSED
K15	K25	K35	K34	K24	K34
UNUSED					UNUSED

TABLE 2-2: MPTS OUTPUT MATRIX RELAY CONFIGURATION

K11	K21	K31	K32	K22 UNUSED	K12 UNUSED
K16 UNUSED	K26 UNUSED	K36	K33	K23 UNUSED	K13 UNUSED
K15	K25	K35	K34	K24 UNUSED	K34 UNUSED

2.2 INSTALLATION AND REMOVAL, CABLING

In MPTS, the matrix connections are all made to the front panel with 3 mm SMA female connectors using Ø.141 inch OD semirigid coaxial cable and flexible coaxial cable.

!!!!!!!! CAUTION !!!!!!!!

TO PREVENT DAMAGE TO THE INSTRUMENT, GO TO THE FRONT AND REMOVE ALL POWER CORDS AND ALL COAXIAL CABLES WHICH CONNECT TO OTHER INSTRUMENTS BEFORE SLIDING MATRIX FOR INSTALLATION OR REMOVAL. DO NOT USE EXCESSIVE FORCE TO CONNECT OR DISCONNECT THE COAXIAL CABLES.

In installation, the cables should be the last items to connect. In removal the cables should be the first items to disconnect. Especially in the case of the semirigid coax, avoid the use of excessive force on the cables or their connectors. They are easily damaged.

An easy method of making the front panel cable connections is to use an assembled MPTS System as a model. The cable connection are shown below and on the I/O Matrix Pullout. The "drawings" of the cable types listed below are shown in Figures 2-1 and 2-2.

TABLE 2-3: MATRIX CABLING, LOADS AND SHORTS

Item	Part Number	Location	
		Input Matrix	Output Matrix
50 Ohm Load	015-1022-00		K154
Shorting Caps	015-1020-00	K112	K364
"	"	K313	K344
"	"	K323	K334
"	"	K333	K324
"	"	K343	K314
"	"	K353	K153
"	"		K340

TABLE 2-4: INPUT MATRIX CABLING

Connections	Cable	Connections	Cable
K110-K210	G	K324-K242	B
K160-K260	G	K334-K243	D
K220-K120	G	K216-K361	D
K252-K325	A	K261-K316	E
K352-K225	A	K266-K366	F
K214-K341	A	K265-K356	E
K314-K241	A	K332-K223	D
K262-K326	B	K255-K355	F
K362-K226	B	K354-K245	B
K251-K315	B	K254-K345	B
K213-K331	B	K344-K244	F
K264-K346	B	K212-K321	B
K215-K351	B	K322-K222	F
K263-K336	C	K211-K311	F
K253-K335	B	K312-K221	B
K224-K342	B		

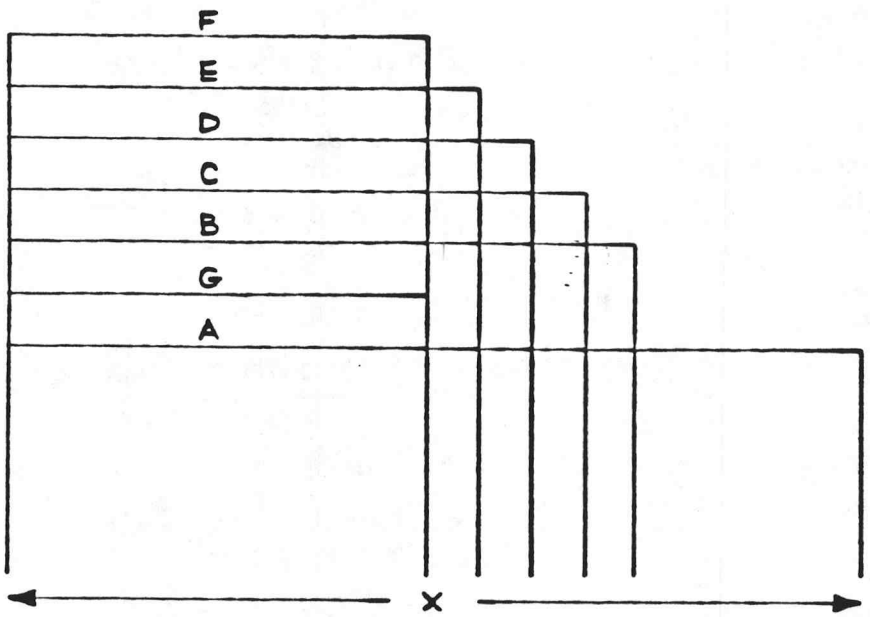
TABLE 2-5: OUTPUT MATRIX CABLING

Connection	Cable	Connection	Cable
K110-K210	G	K250-K150	G
K211-K311	F	K251-K315	B
K212-K321	B	K252-K325	A
K213-K331	B	K253-K335	B
K214-K341	A	K254-K345	B
K216-K361	D	K256-K365	D

TABLE 2-6: INTERCONNECT MATRIX CABLING

Connection	Cable
HP 8656, K164*	H
WAVETEK, K163	I
WAVETEK, K113	J
ATTEN OUT, K161	K
NOR OSC SENSE, K122	L
PS 5Ø3, K123	N
K116	O
K166	P
K126	Q
K121	R
K36 COMMON (INPUT)	S
K24 COMMON,K25 COMMON	T
K363 OUTPUT MATRIX	U
K124	V
PULSE GEN TO ATTEN	W
K111, NOR OSC OUT	X
DMM BNC BLOCK	Y
K116 OUTPUT MATRIX	Z
K156 OUTPUT MATRIX	AA
DMM BNC BLOCK	BB
K115 OUTPUT MATRIX	CC
A Gate Sel. Output to Counter A Gate Input	DD
X HATCH TO I115	EE
Y HATCH TO I116	FF
Z HATCH TO I125	GG
0155, A Gate Sel. Input	HH
HP 8656, K164	II

* Note: K164 means J164 of K16, etc.

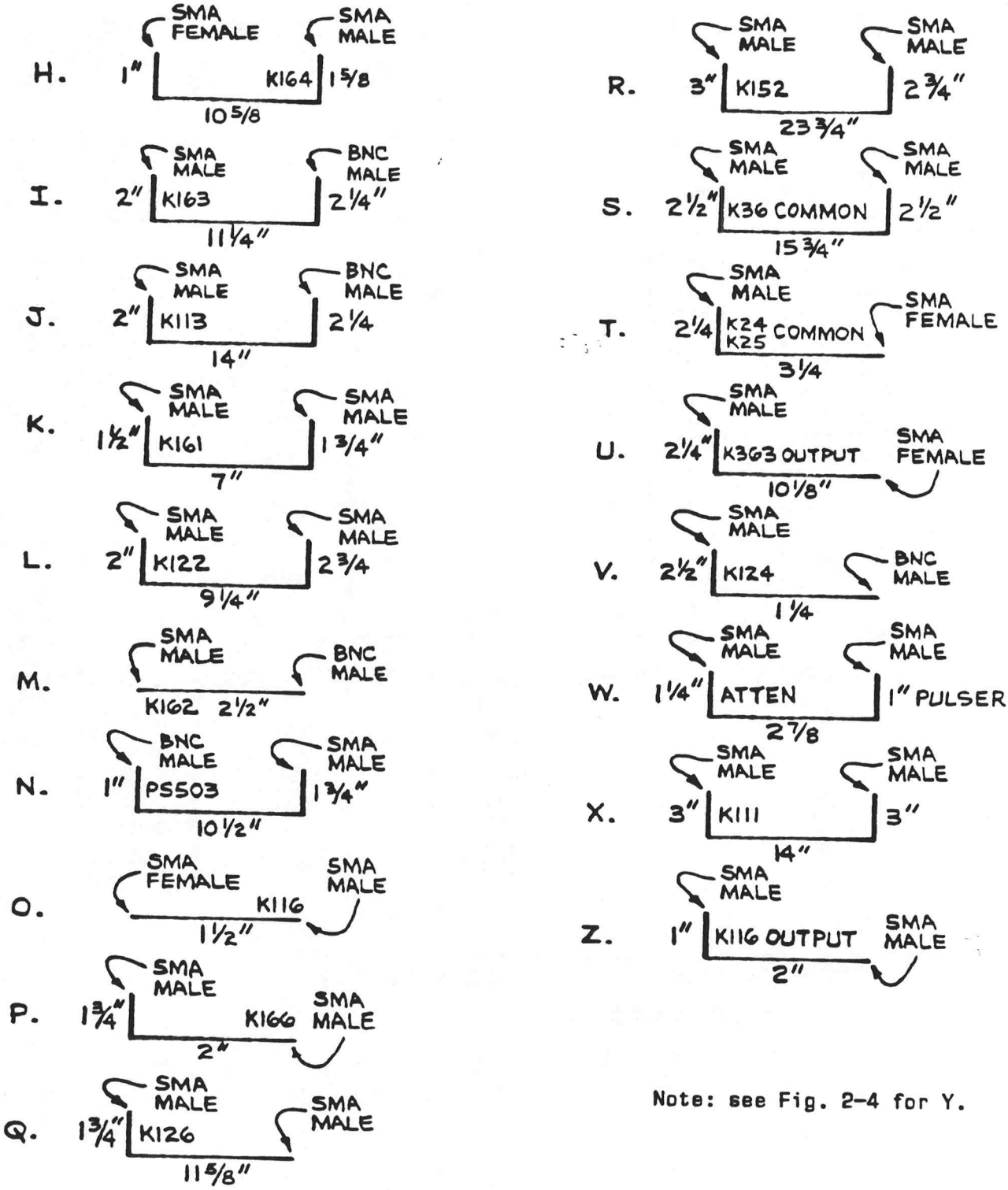


CABLE	QUANTITY	CENTER TO CENTER ("X")	OVERALL LENGTH
A	6	5.562"	8.000"
B	18	4.312"	8.000"
C	1	3.750"	8.000"
D	5	3.250"	8.000"
E	2	2.812"	8.000"
F	6	2.375"	8.000"
G	5	2.375"	5.500"

M.P.T.S. SEMIRIGID CABLE LENGTHS

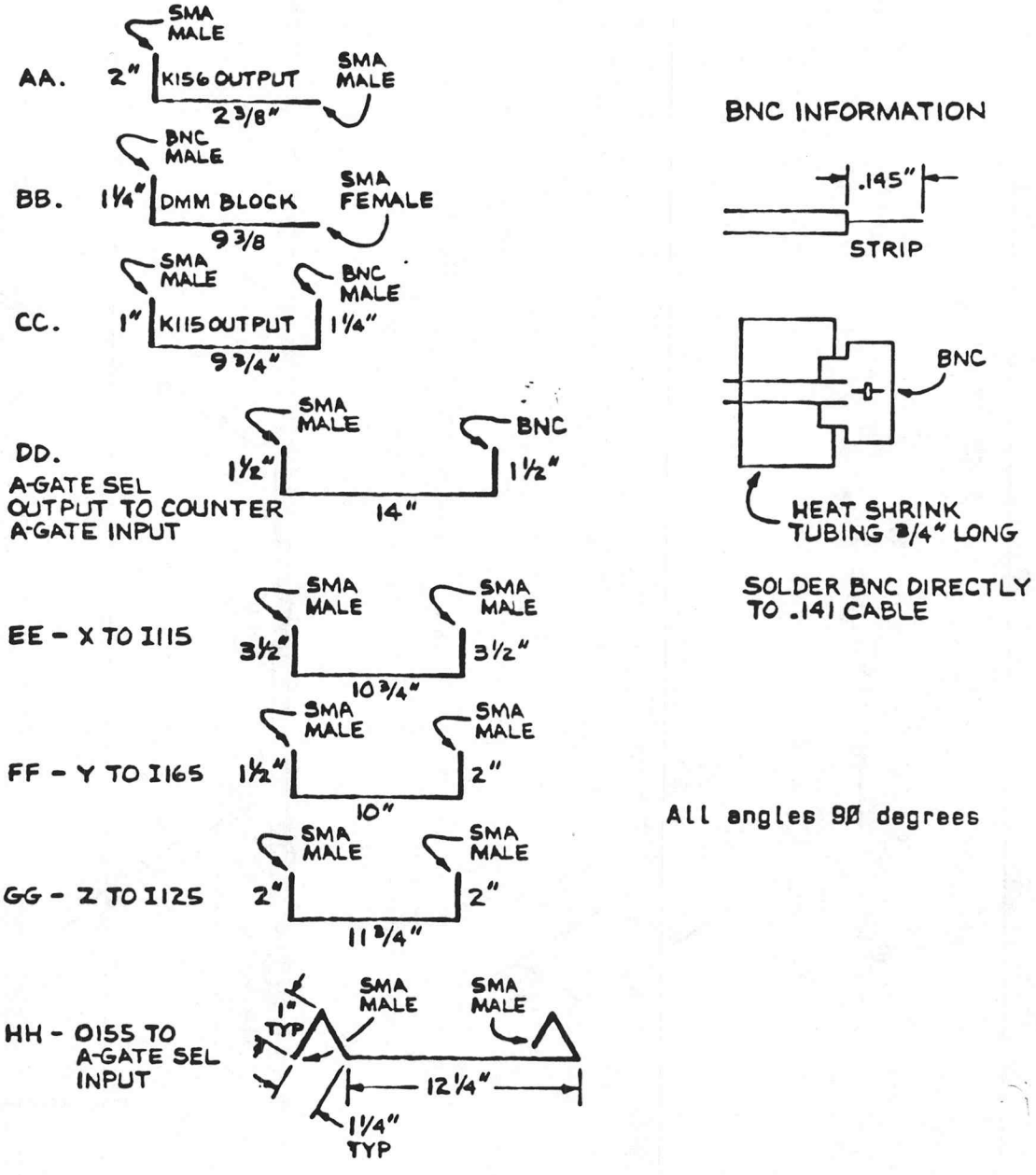
16 SETS REQUIRED

Figure 2-1: Semirigid Interconnect Cables (A-G)



Note: see Fig. 2-4 for Y.

Figure 2-2: Semirigid Interconnect Cables (H-Z)



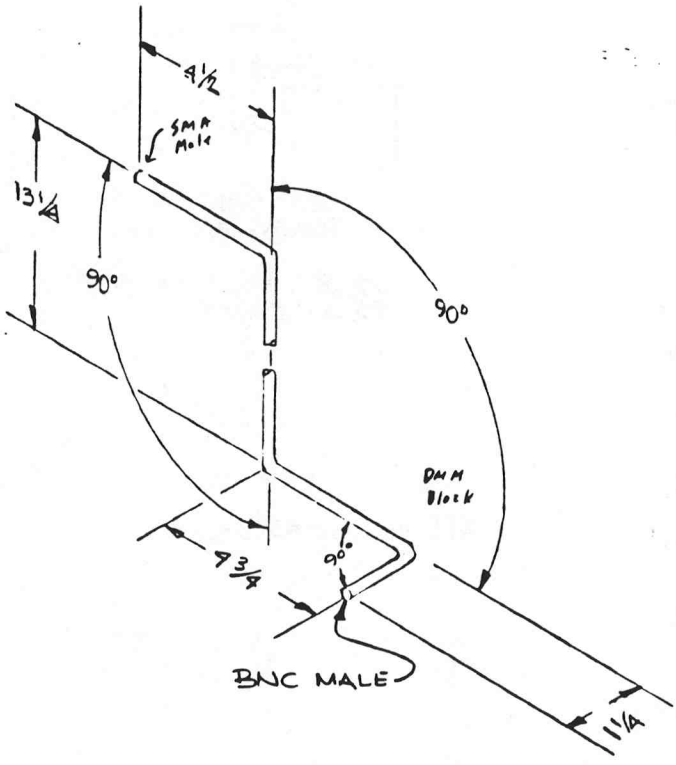
BNC INFORMATION

SOLDER BNC DIRECTLY TO .141 CABLE

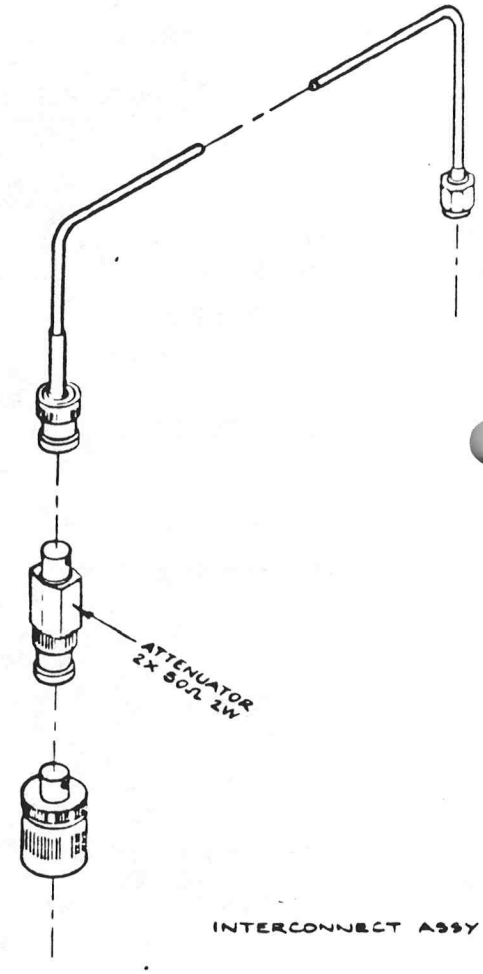
All angles 90 degrees

X-Y-Z PATTERN GEN CABLES
A-GATE PHASE SEL CABLES

Figure 2-3: Additional Interconnect Cables (AA-HH)



Cable Y



Cable II

Figure 2-4: Additional Interconnect Cables (Y and II)

2.3 FRONT PANEL CONTROLS AND INDICATORS.

Other than the extensive cable connectors already mentioned, there are no indicators or manual controls on the front or rear panels. The Switching Matrix can be controlled only from the GPIB.

2.4 PERFORMANCE CHECK

After all semirigid cabling has been installed on the relays, the paths between the "preselector" inputs and the "outputs" should be verified for both path resistance and 50 ohm integrity. See circuit description for the meanings of preselector and output relays.

Path closures can be accomplished by using either Kermit or BASIC with direct GPIB instructions. See the Programming Section which follows this section. Consult the Matrix Schematic, Pullout 6, for individual J numbers.

The series path resistance should be less than 500 milliohms.

The integrity of the 50 ohm characteristic impedance path should be verified using a TDR procedure. A 7S12 with a S-52 pulse generator head and 1S6 sampling head or similar TDR sampling system should be used. Consult either the 7S12 or S-52 Operator manual for a detailed explanation. All paths from the preselector to the outputs should be verified for 50 ohm +-0.5 ohm.

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual contains the theory of operation of the circuitry used in the Ø67-1Ø96-99 Programmable Microwave Switching Matrix. Individual descriptions are separated into the following parts: GPIB Listener Interface, Latch-Drivers Circuitry, Diode Relay Circuits, MPTS I/O Matrix, Card Cage Backplane Wiring, and Power Supplies. The diagrams are segmented according to circuit function. Refer to appropriate diagrams in the Diagram Section of this manual while reading the circuit description.

3.1.1 BLOCK DIAGRAMS <Ø>

There are two block diagrams. The General Block Diagram <Ø> (Figure 6.1) gives the general structure of the matrix system. Although two relays from the input matrix are show as examples, the output matrix has essentially the same structure. The main changes are the number of relays, the line and relay numbers and the direction of signal flow in the matrix lines.

Very simply stated, when the GPIB Interface receives a relay command string it energizes the latch drivers which switch the relays to the desired positions.

While the second or Detailed Block Diagram <1> (Figure 6.2) does not show specific relays, it does show more schematic detail. It also shows the diamond <> numbers for handy reference to the schematics which follow. To keep oriented, one should refer to it from time to time as one studies the diagrams and reads the circuit descriptions.

3.2 GPIB LISTENER INTERFACE <2>

The discussion to the circuitry of the GPIB Listener Interface assumes that the reader has some familiarity with the IEEE Std 488-1975. Supplemental reading in the "GPIB System Concepts" part at the end of this section will be of help. In addition, there are good booklets on the subject.

Referring to <2> Figure 7.3, the Interface Card in the card cage contains the Fairchild 96LS488 GPIB chip, U42Ø. This chip is a TTL LSI circuit containing all of the logic necessary to interface talk, listen, and talk/listen type instruments and system components in accordance with the IEEE 488 standard for programmable instrumentation.

In this application, the U42Ø is configured to be a listener. There are several components near U42Ø. The device address switch, S41Ø, consists of five SPST switches whose positions determine the listen address of the instrument. The addressed LED, DS 3ØØ, lights when the instrument is in the listening mode. RC components set the clock frequency and initialize the chip. Connections to ground and to pull-up resistors establish the listener mode.

The connections from the GPIB connector to the GPIB chip also go to inverting buffers, U231. these invert the negative logic signals on the bus to pr[illegible] logic signals for the Latch Drivers in the remainder of the card cage. [illegible]s a tri-state device; it is enabled only when the GPIB chip gets its [illegible] address and the 'NOT-LAD' signal goes low.

The outputs of the tri-state buffer, U231, drive inputs of U13Ø, an eight bit comparator, and backplane pins A1 through A6. The eight bit comparator is arranged to watch seven data lines of the bus with half of its inputs. It compares these bits with the bit pattern: ØØØ11Ø1 which is hard wired to the other half of its inputs. (ØØØ11Ø1 is the ASCII character for the 'carriage return'.)

When the interface is processing bytes to the Latch Driver circuit cards, U13Ø pin 19 (SHIFT/NOT-LOAD STEERING) remains high. This high state enables U14Ø pin 1Ø and disables U14Ø pin 4.

For each valid byte, the RXST output, pin 3Ø of U42Ø, goes high. U241 is a two bit shift register that is clocked by U42Ø pin 42, the 'NOT-CP' signal. RXST is applied to the input of the two bit shift register. The 'NOT-Q' output (pin 8 of U241, which is jumper-connected to the RXRDY input) by going low signals the 488 chip that the data transfer is complete.

The signal at pin 8 of U241, called the SHIFT-LOAD PULSE, is high for two clock periods, and when the U13Ø pin 19 output is high and U14Ø pin 1Ø is enabled, this produces a shift pulse, BSHF, on interface pin A7.

When the data on the bus is a carriage return, the output of U13Ø pin 19 goes low, disabling U14Ø pin 1Ø, and enabling U14Ø pin 4. The SHIFT-LOAD PULSE is then steered to interface pin A9 and becomes the BLOAD pulse.

A command on the GPIB bus called INIT, or CLEAR will excite the 488 chip to produce a 'not CLR' output on U42Ø pin 32. This is applied to the card cage interface through U16Ø pins 3-4-5-6 and becomes the 'not BCLR' signal to clear the bits in the latch-driver cards.

When the command string directed to the switching matrix interface is completed, the controller issues the UNLISTEN command. This makes the GPIB interface inactive, 'not LAD' goes high... turning off the ADDRESSED LED and switching the U231 buffers to their disabled state.

3.3 LATCH-DRIVER CIRCUITRY <3>

Each Latch Driver card is capable of storing two "bytes" of six bits. Since there are six latch-driver cards in the card cage, the total capacity is 12, six-bit bytes. In accordance with the GPIB standard, the data string sent to this instrument will always be composed of 12 bytes terminated by a carriage return.

Each latch-driver card (<3> Figure 7-4) consists of four hex-D type flip-flops, 12 transistor-relay drivers and their respective base resistor networks. The inputs on the connector backplane C1 through C6 are ccted to the inputs of U3; the outputs of U3 feed the inputs of U4. The outputs of U4 connect to connectors A1 through A6 to shift data on to the next latch-driver card.

The outputs of U3 and U4 are also applied to the inputs of U1 and U2. The outputs of U1 drive six base resistor networks for relay driving transistors Q1 through Q6. U2 outputs do the same for Q7 through Q12. A high bit on the output of any flip-flop will turn on its respective transistor and complete the circuit to energize the relay coils attached to that transistor output.

The BSHF shift pulse, on connection C7, is connected to shift the U3 and U4 flip-flops. C9, the BLOAD signal, loads the U3 and U4 outputs into the U1 and U2 flip-flops, respectively. When a BCLR signal which is an active low occurs on C8, all the flip-flop bits are set to zero (the cleared state).

The inputs of the first latch-driver card in the card cage receives data from the GPIB listener interface card; each succeeding latch-driver card receives data from the card preceding it. When the GPIB listener interface card outputs a shift pulse, BSHF, the data on the inputs of U3 shifts into U3, the data on the outputs of U3 shifts into U4, the data from the outputs of U4 shifts into the U3 flip-flops of the next card, and so on...

When there have been 12 shifts, the first data in has reached the sixth latch-driver card and rests in the U4 flip-flops there. When the carriage return character, which indicates the end of the data string sent to this switching matrix, is recognized and decoded by the 8-bit comparator of the GPIB listener interface, a BLOAD signal is generated. This BLOAD signal excites all

U1 and U2 flip-flops and causes them to load themselves with the outputs of all the corresponding U3 and U4 flip-flops. Those outputs which are high will turn on their respective transistors and the relays will energize the next path configuration.

3.4 DIODE RELAY CIRCUITS <5>

Mounted on the rear of each relay is a circular circuit board, <5> Figure 7-6, that provides the means for connecting the relay coils to the driver transistors in the latch-driver cards. The circuit boards contain a diode across each relay coil to clamp the inductive back-emf when the relay is de-energized.

3.5 MPTS I/O COAXIAL MATRIX <6>

The relays used in the Ø67-1Ø96-99 GPIB Programmable Microwave Switching Matrix are single-pole-six-hrow, SP6T, solenoid activated microwave switches. The operating frequency range is from DC to 18 GHz. They have 5Ø ohm characteristic impedance and low insertion loss and VSWR. The connectors are 3mm SMA female, and the coaxial "plumbing" in the matrix can be semirigid or flexible coax cable. All switches are independently activated by the bits set in the latch-driver cards in the matrix card cage as described under Latched Driver Circuitry.

The front panel of the switching matrix has mounting holes to install up to 18 coaxial switches. Depending on the system requirements where the switching matrix is being applied, there may be fewer than 18 relays installed. The card cage backplane, however, is always wired to energize all 18 relays.

<6> Figure 7.7 shows the standard MPTS Input Matrix of 14 relays and the MPTS Output Matrix of 9 relays. The relays with the connectors labeled in the "J-one hundreds" are called the preselectors. The connectors labeled "J-two hundreds" and "J-three hundreds" form the outputs. The relays connected to J1XX, comprise a maximum of 36 inputs; the relays connected to J3XX comprise a maximum of 6 outputs, so the MAXIMUM format of each matrix is a 36 to 6 crosspoint matrix. As previously stated, MPTS does not at present use the maximum configuration either in the Input or the Output Matrix.

The labeling of the J- numbers is devised so that the source and destination of the paths can easily be traced. For example, J121 input on the preselectors goes to the trunk 12Ø and on to 22Ø on the output relay. The 221 path ends up at 312. To simplify the labeling, the J's were omitted from the internal lines.

Except for the number of relays, the Input and Output matrices have the same components, the same line and essentially the same component labels. K11 is labeled "IN" in the input matrix and "OUT" in the output matrix, but otherwise the labeling is exactly the same.

Signals can flow equally well in either direction in the matrices. This means that the terms 'input' and 'output' used in describing the matrix are not to be taken seriously. In the Output Matrix the preselector is really a post-selector.

3.6 CARD CAGE BACKPLANE <4>

The card cage contains seven card connectors which are wired according to <4>. The right-most card slot (the left-most in <4>) is configured to receive a GPIB listener interface card ONLY! The other six card slots are identical and configured to accept the latch-driver cards. The backplane is wire-wrapped to bus the supplies and grounds to all circuit boards. The GPIB data, handshake, and bus management signals are wired from the GPIB connector on the rear panel of the switching matrix package to the GPIB interface card slot. Data out of the interface is applied to the data in connections of the adjacent slot. Data connections are "daisy-chained" throughout the latch-driver card slots as described in 4.3 above. The signals produced by the GPIB listener interface: BSHF, BLOAD, and BCLR are bussed to all latch-driver cards.

The latch-driver transistor outputs are brought out in seven conductor ribbon cabling, containing the six outputs plus the 24 volt supply which completes the relay energizing circuit. There are 18 sets of 7 conductor ribbon cables; 6 comprise the bits and drives for the preselectors, and 12 comprise the connections to the pairs of relays that form the output relay paths.

3.7 POWER SUPPLIES <1>

The supplies for the switching matrix are the +5 volt supply for the card cage electronic circuits, and a +24 volt supply for the microwave coaxial relays. The supplies are conventional linear regulated ones mounted in an open frame beside the card cage. The supply is OEM currently obtained from the POWER MATE company.

3.8 GPIB SYSTEM CONCEPTS

GPIB SYSTEM CONCEPTS

INTRODUCTION

The GPIB is a digital interface that allows efficient communication between the components of an instrumentation system.

The primary purpose of the GPIB is to connect self-contained instruments to other instruments or devices. This means that the GPIB is an interface system independent of device functions.

There are four elements of the GPIB: mechanical, electrical, functional, and operational.

Of these four, only the last is device-dependent. Operational elements state the way in which an instrument reacts to a signal on the bus. These reactions are device-dependent characteristics and state the way in which the instruments use the GPIB via application software.

Mechanical Elements

The standard defines the mechanical elements: cables and connectors. Standardizing the connectors and cables ensures that GPIB-compatible instruments can be physically linked together with complete pin compatibility.

The connector has 24 pins, with 16 assigned to specific signals and eight to shields and grounds. Instruments on the bus may be arranged in a linear or star configuration.

Electrical Elements

The voltage and current values required at the connector nodes for the GPIB are based on TTL technology (power source not to exceed −5.25 V referenced to logic ground). The standard defines the logic levels as follows: Logical 1 is true state, low-voltage level (≤ -0.8 V), signal line is **asserted**. Logical 0 is false state, high-voltage level (≥ -2.0 V), signal line is **not asserted**.

Messages can be sent over the GPIB as either active-true or passive-true signals. Passive-true signals occur at a high-voltage level and must be carried on a signal line using open-collector devices. Active-true signals occur at a low-voltage level.

Functional Elements

The functional elements of the GPIB cover three areas:

1. **Ten interface functions** (listed in Table 3-9) that define the use of specific signal lines so that an instrument can receive, process, and send messages. The ten inter-

face functions—with their allowable subsets—provide an instrumentation system with complete communications and control capabilities.

Not every instrument on the bus has all ten functions because only those functions important to a particular instrument's purpose need be implemented.

2. The **specific protocol** by which the interface functions send and receive their limited set of messages.

3. The **logical and timing relationships** between allowable states for the interface signal lines.

Table 3-9

MAJOR GPIB INTERFACE FUNCTIONS

Interface Functions	Symbol
Source Handshake	SH
Acceptor Handshake	AH
Talker or Extended Talker	T or TE
Listener or Extended Listener	L or LE
Service Request	SR
Remote-Local	RL
Parallel Poll	PP
Device Clear	DC
Device Trigger	DT
Controller	C

A TYPICAL GPIB SYSTEM

Figure 3-5 illustrates an example of the GPIB and the nomenclature for the 16 active signal lines. Only four instruments are shown, but the GPIB can support up to 15 instruments connected directly to the bus. However, more than 15 devices can be interfaced to a single bus if they do not connect directly to the bus but are interfaced through a primary device. Such a scheme can be used for programmable plug-ins housed in a mainframe where the mainframe is addressed with a primary address code and the plug-ins are addressed with a secondary address code.

The instruments connected to a single bus cannot be separated by more than 20 meters (total cable length) and at least one more than half the number of instruments must be in the power-on state. To maintain the electrical characteristics of the bus, a device load must be connected for each two meters of cable length. Although instruments are usually spaced no more than two meters apart, they can be separated farther if the required number of device loads are lumped at any one point.

Controllers, Talkers, and Listeners

A **talker** is an instrument that can send data over the bus; a **listener** is an instrument that can accept data from the bus. No instrument can communicate until it is enabled to do so by the controller in charge of the bus.

A **controller** is an instrument that determines, by a software routine, which instrument will talk and which instruments will listen during any given time interval. The controller also has the ability to assign itself as a talker or listener whenever the program routine requires. In addition to designating the current talker and listeners for a particular communication sequence, the controller has the task of sending special codes and commands (called **interface messages**) to any or all of the instruments on the bus.

Interface Messages

The IEEE standard specifies that the interface messages, as shown in Fig. 3-6, ASCII & IEEE 488 (GPIB) Code Chart, be used to address and control instruments interfaced to the GPIB. Interface messages are sent and received only when the controller asserts the ATN bus line. The user can correlate interface message coding to the ISO 7-bit code by relating data bus lines DI01 through DI07 to bits 1 through 7, respectively.

Interface messages include the primary talk and listen addresses for instruments on the bus, addressed commands (only instruments previously addressed to listen respond to these commands), universal commands (all instruments, whether they have been addressed or not respond to these), secondary addresses for devices interfaced through their primary instrument, and secondary commands. At present, the standard classifies only two interface messages as secondary commands: Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD). (Parallel Poll Enable means that *after* the controller configures the system for a parallel poll (PPC command), all instruments respond at the same time with status information on receipt of PPE.)

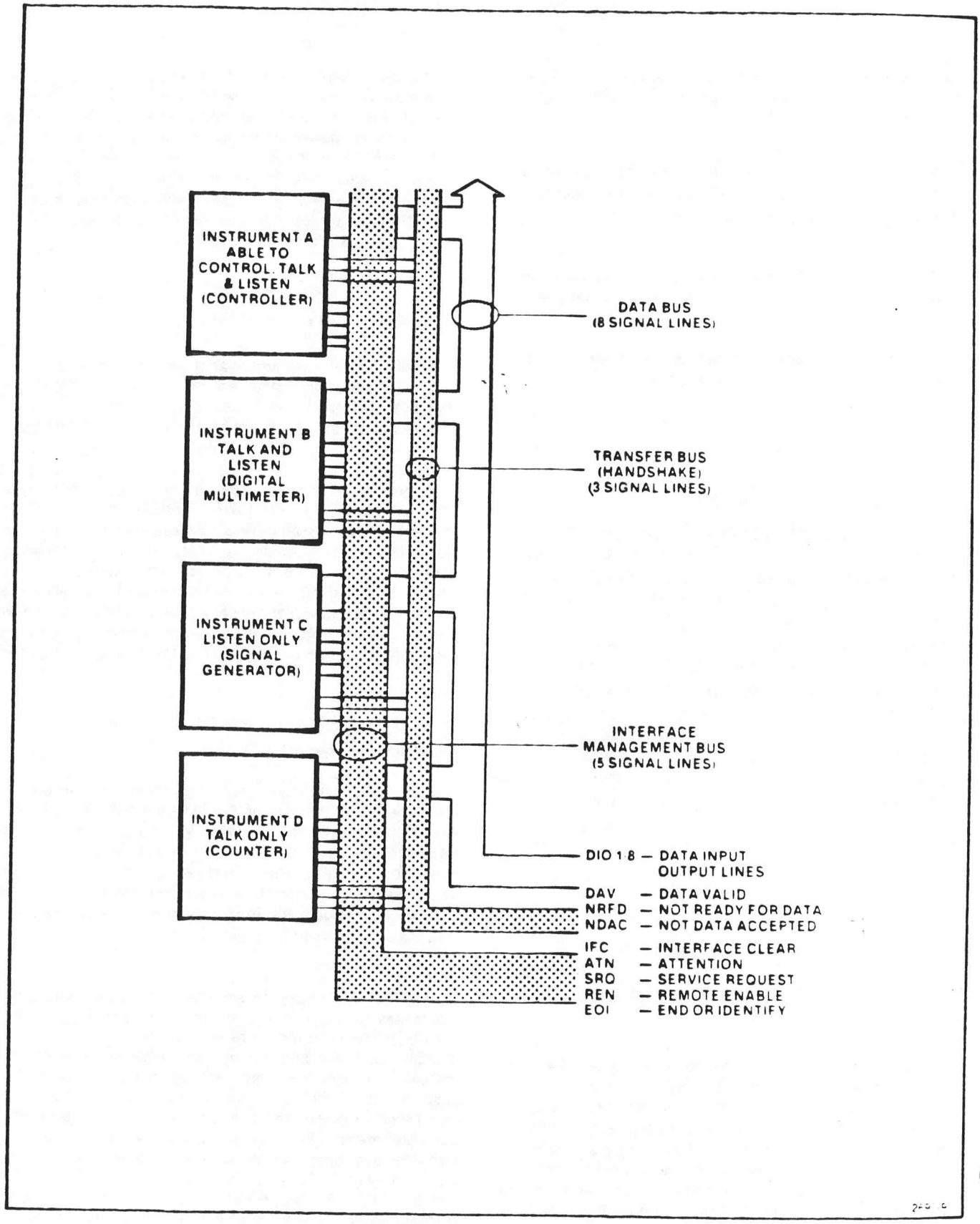


Fig. 3-5. A typical system using the general purpose interface bus (GPIB).

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
0 0 0 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 TCT HT 9 9	31 SPD EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 < 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 | 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 UNL ? 3F 63	117 O 4F 79	137 UNT _ 5F 95	157 o 6F 111	177 RUBOUT (DEL) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS	

KEY

octal 25 PPU — GPIB code
NAK — ASCII character
hex 15 21 — decimal

Fig. 3-6. ASCII & IEEE 488 (GPIB) Code Chart.

Device Dependent Messages

The IEEE standard does not specify coding of device-dependent messages, messages that control the device's internal operating functions. After addressing (via interface messages) a talker and listener(s), the controller unasserts the ATN bus line. When ATN becomes false, any commonly-understood 8-bit binary code may be used to represent a device-dependent message.

The standard recommends that the alphanumeric codes associated with the numbers, symbols, and upper case characters (decimal 32 to decimal 94) in the ASCII Code Chart be used for device-dependent messages. One example of a device-dependent message is the ASCII character string

MODE V; U/D 5E-3; FREQ 1E3

which may tell an instrument to set its front-panel controls to the voltage mode, with 5.0 millivolt output at a frequency of 1000 Hz.

When 8-bit binary codes other than the ISO 7-bit code are used for device-dependent messages, the most significant bit must be on data line DI08 (for bit 8).

To summarize the difference between interface and device-dependent messages, remember that any message sent or received when the ATN line is asserted (true) is an interface message. Any message (data bytes) sent or received when the ATN line is unasserted (false) is a device-dependent message.

GPIB SIGNAL LINE DEFINITIONS

Figure 3-5 shows the 16 signal lines of the GPIB functionally divided into three component busses: an eight-line data bus, a three-line transfer control (handshake) bus, and a five-line management bus.

The Data Bus

The data bus has eight bidirectional signal lines, DI01 through DI08. Information, in the form of data bytes, is transferred over this bus. A handshake sequence between an enabled talker and the enabled listeners transfers one data byte (eight bits) at a time. Data bytes in an interface or device-dependent message are sent and received in a byte-serial, bit-parallel fashion over the data bus.

Since the GPIB handshake sequence is an asynchronous operation, the data transfer rate is only as fast as the slowest instrument involved in a data byte transfer at any one time. A talker cannot place data bytes on the bus faster than any one listener can accept them.

Figure 3-7 illustrates the flow of data bytes when a typical controller sends ASCII data to an assigned listener on the bus. The first data byte, decimal 44, enables device 12 as a primary listener and the secondary address, decimal 108, enables a plug-in device as the final destination of the data to follow. The data is the two ASCII characters, A and B (decimal 65 and decimal 66).

The decimal value for B is specified as negative to activate the EOI line and signify the end of the device-dependent message. The controller activates the ATN line again and sends the universal unlisten (UNL) and untalk (UNT) commands to clear the bus. Six handshake cycles on the Transfer Bus are required to send the six data bytes.

The Transfer Bus (Handshake)

Each time a data byte is sent over the data bus, an enabled talker and all enabled listeners execute a handshake sequence via the **transfer bus**. The transfer-bus signal lines are defined below. Figure 3-8 illustrates the basic timing relationship between the three signals. The ATN line is shown to illustrate the controller's role in the process. A flowchart for the handshake sequence is shown in Fig. 3-9.

Not Ready For Data (NRFD). An asserted NRFD signal line indicates one or more assigned listeners are not ready to receive the next data byte from the talker. When all of the assigned listeners for a particular data byte transfer have released NRFD, the NRFD line becomes unasserted (high). The RFD message (Ready For Data) tells the talker it may place the next data byte on the data bus.

Data Valid (DAV). The DAV signal line is asserted (low) by the talker after the talker places a data byte on the data bus. When asserted, DAV tells each assigned listener that a new data byte is on the data bus. The talker is inhibited from asserting DAV as long as any listener holds the NRFD signal line asserted.

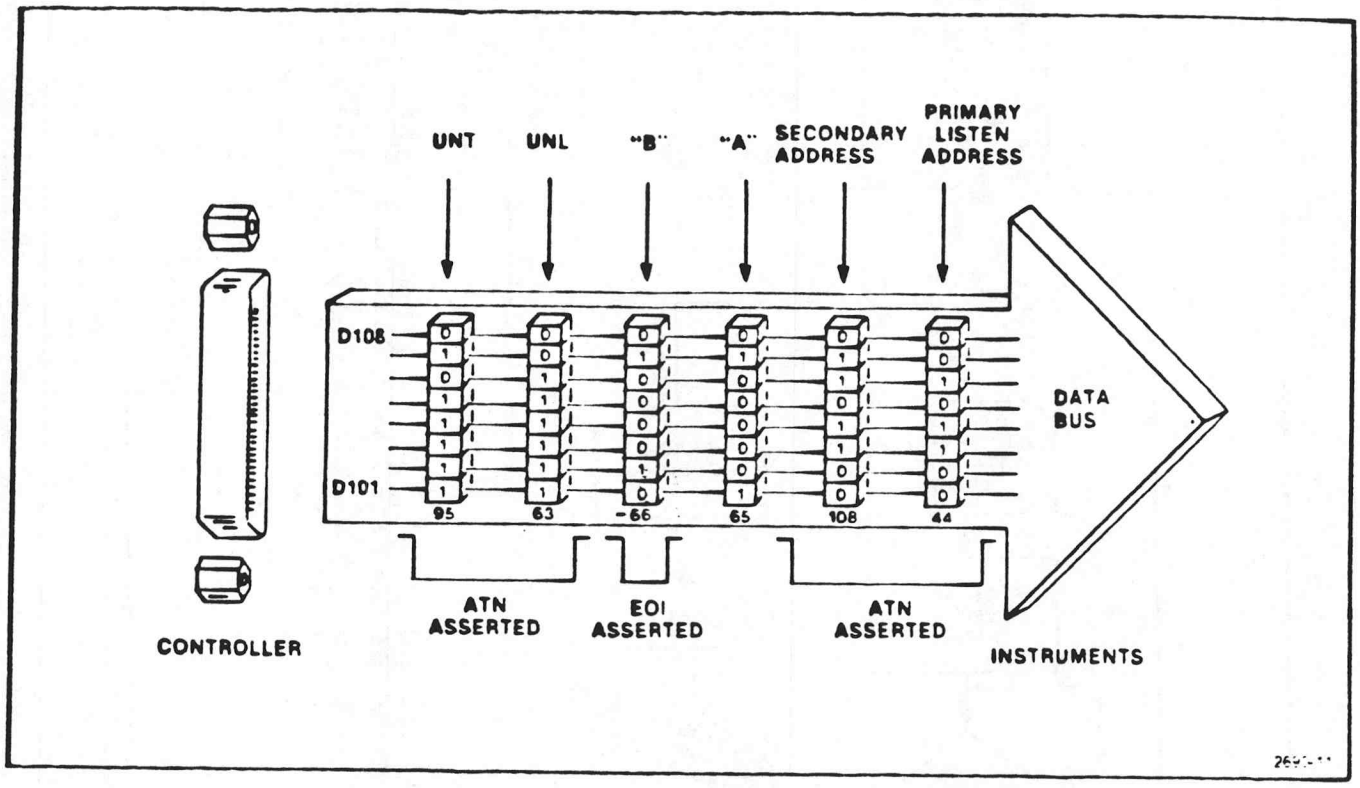


Fig. 3-7. An example of data byte traffic on the GPIB.

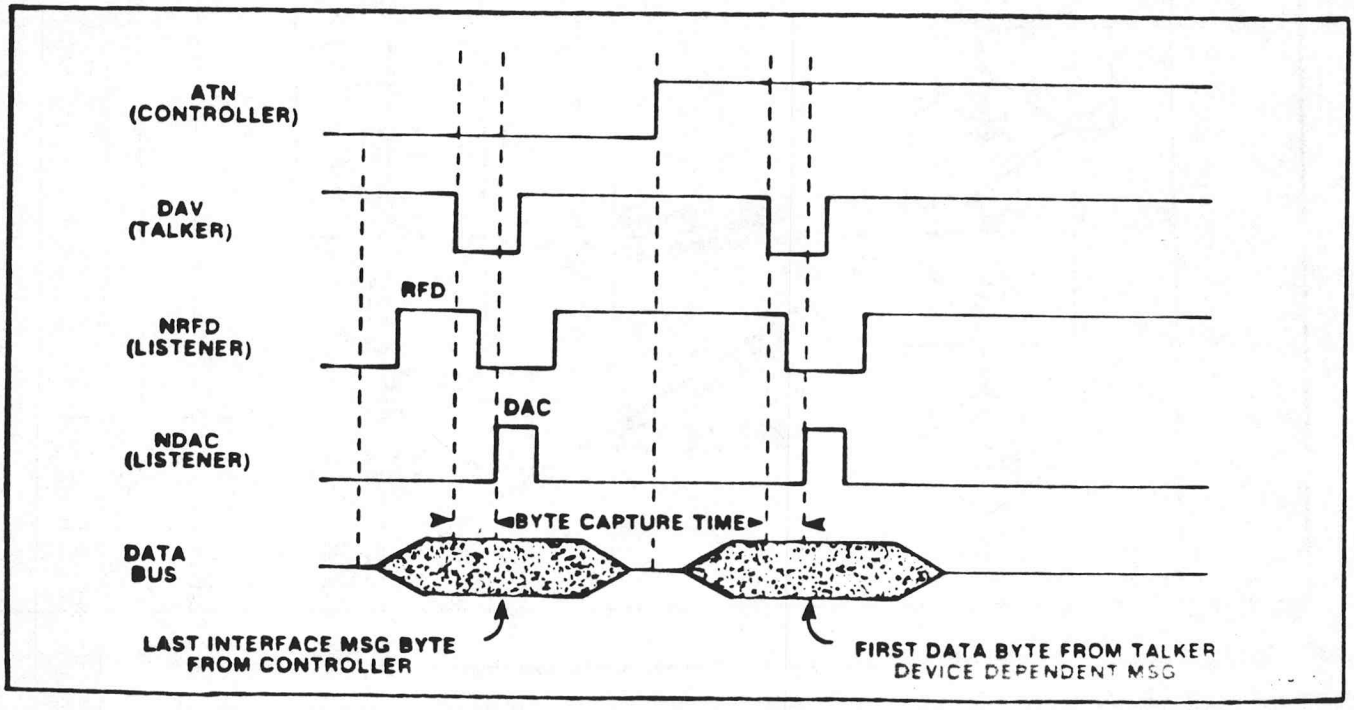


Fig. 3-8. A typical handshake timing sequence (idealized). Byte capture time is dependent on the slowest instrument involved in the handshake.

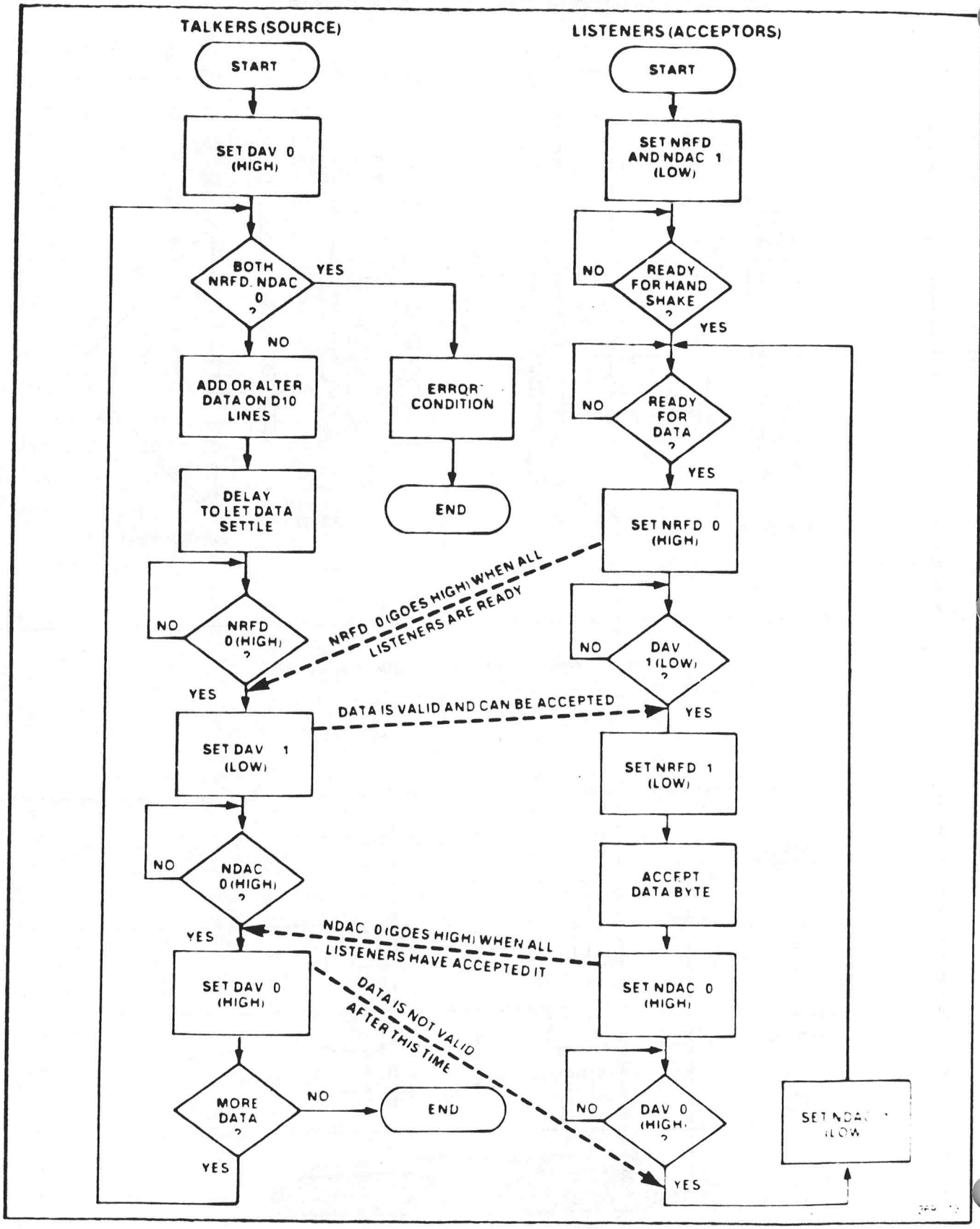


Fig. 3-9. The handshake flow chart.

Not Data Accepted (NDAC). Each assigned listener holds the NDAC signal line low-true (asserted) until the listener accepts the data byte currently on the data bus. When all assigned listeners accept the current data byte, the NDAC line becomes unasserted, telling the talker to remove the data byte from the bus. The DAC message (Data Accepted) tells the talker that all assigned listeners accepted the current data byte.

When one handshake cycle transfers one data byte, the listeners reset the NRFD line high and the NDAC line low before the talker asserts DAV for the next data byte transfer. NDAC and NRFD both high at the same time is an invalid state on the bus.

The Management Bus

The management bus is a group of five signal lines which are used to control the operation of the GPIB IFC, ATN, SRQ, REN, and EOI.

Interface Clear (IFC). The system controller asserts the IFC signal line to place all interface circuitry in a predetermined quiescent state which may or may not be the power-on state.

Only the system controller can generate this signal. The IEEE standard specifies that only three interface messages (universal commands) be recognized while IFC is asserted: Device Clear (DCL), Local Lockout (LLO), and Parallel Poll Unconfigure (PPU).

Attention (ATN). A controller asserts the ATN signal line when instruments connected to the bus are being enabled as talkers or listeners and for other interface control traffic. As long as the ATN signal line is asserted (ATN = 1), only instrument address codes and control messages are transferred over the data bus. With the ATN signal line unasserted, only those instruments enabled as a talker and listener(s) can transfer data. Only the controller can generate the ATN signal.

Service Request (SRQ). Any instrument connected to the bus can request the controller's attention by asserting the SRQ line. The controller responds by asserting ATN and executing a serial poll to determine which instrument is requesting service. (An instrument requesting service identifies itself by asserting its DIO7 line after being addressed.) After the instrument requesting service is found, program control is transferred to a service routine for that instrument. When the service routine is completed, program control returns to the main program. When polled, the instrument requesting service unasserts the SRQ line.

Remote Enable (REN). The system controller asserts the REN signal line whenever the interface system operates under remote program control. Used with other control messages, the REN signal causes an instrument on the bus to select between two alternate sources of programming data. A remote-local interface function indicates to an instrument that the instrument will use either information input from the front-panel controls (Local) or corresponding information input from the interface (Remote).

End or Identify (EOI). A talker can use the EOI to indicate the end of a data-transfer sequence. The talker asserts the EOI signal line as the last byte of data is transmitted. In this case, EOI is essentially a ninth data line and must observe the same setup times as the DIO lines. When the controller is listening, it assumes that a data byte received is the last byte in the transmission (if the EOI signal line has been asserted). When the controller is talking, it may assert the EOI signal line as the last byte is transferred. The EOI signal is also asserted with the ATN signal if the controller conducts a parallel polling sequence. EOI is not used during serial polling.

NOTE

For detailed information on GPIB specifications refer to IEEE 488-1975 (Revised 1978), published by the Institute of Electrical and Electronics Engineers 245 East 47th Street, New York, New York 11117.

SECTION 4

PROGRAMMING INFORMATION

4.1 INTRODUCTION

Because the Switch Matrix is the heart of the MPTS system, it is desirable that this section include fairly complete programming information. It is divided into two headings: Programming Using Drivers and Low-Level Programming.

4.2 PROGRAMMING USING MPTS DRIVERS

Matrix connections for the two Ø67-1Ø97-99 matrices are specified by the CONNECT and DISCONNECT driver calls.

Calling convention

Calling the driver to open relays is done with:

```
DISCONNECT[COMMAND$, RESULT$, ECODE%]
```

In this case, COMMAND$ usually has two components separated by a space: a matrix pin designation, and a device port name. (See Section 18.3). Calling the CONNECT driver is analogous to the DISCONNECT call.

Commands

Disconnect and Connect commands include the following:

COMMAND:	ACTION:
INIT	At the next XQT command open all relays and clear pending relay commands.
XQT	The XQT command simultaneously enables all relay closures and openings specified

since the last XQT was received.

pin port — At the next XQT command, connect or disconnect the path between the matrix pin designation (I31Ø, I32Ø... or O31Ø, O32Ø...) and the specified test device port.

Matrix pins designations include the following:

INPUT PINS:	DESCRIPTION:
I31Ø or CH1	channel 1 on the IUT
I32Ø or CH2	channel 2 on the IUT
I33Ø or CH3	channel 3 on the IUT
I34Ø or CH4	channel 4 on the IUT
I35Ø or ZAXIS	Z axis output of IUT
I36Ø or INCOM	common path to output matrix

OUTPUT PINS:

O31Ø or AGATE	A gate output from the IUT
O32Ø or BGATE	B gate output from the IUT
O33Ø or CALOUT	calibrator output from IUT
O34Ø	unused on the IUT
O35Ø	unused on the IUT
O36Ø or OUTCOM	common path to input matrix

Test device port names include the following:

INPUT DEVICE PORT NAMES:	DESCRIPTION:
SNWAVE	sinewave generator
FUNCT	function gen. standard output
SQWAVE	function gen. precision sqwave
CALIB	calibration generator
PULSE	pulse generator
NOROUT	normalizer oscillator output
NORSEN	normalizer oscillator sense
DMMHI	digital multimeter
XHATCH	X output of pattern gen.
YHATCH	Y output of pattern gen.
ZHATCH	Z output of pattern gen.
SPLITA	power splitter output A
SPLITB	power splitter output B
COMMON	common line to out matrix
GND	ground
2ØVOLT	2Ø VOLT DC supply
CH2OUT	Ch 2 I.U.T output

OUTPUT DEVICE PORT NAMES:	DESCRIPTION:
CNTRA	counter/timer input A
CNTRB	counter/timer input B
SPLIT	power splitter input
GND	system ground
LOAD	50 ohm load
COMMON	common line to in matrix

For detailed information on exactly how to implement these commands, see Section 19, "Writing a Program" in MPTS CB PROGRAMMING MANUAL.

The matrix terminal also can be specified in lieu of a name (i.e. J111 etc.). See section 22, "Advanced Programming Techniques" in MPTS CB PROGRAMMING MANUAL.

4.3 LOW-LEVEL PROGRAMMING

In MPTS programs, we normally use MPTS drivers to send commands to the switching matrices. However, for diagnostics and other purposes it may be necessary to talk more directly to the matrices. This is called low-level programming.

Even in low-level programming, we talk to the input and output matrices using the GPIB. The input matrix address is 100. The output matrix address is 101. Following the address, a string of 12 ASCII characters plus a carriage return is sent to the matrix. Each character represents the binary code for one relay. The system can best be explained by the an example.

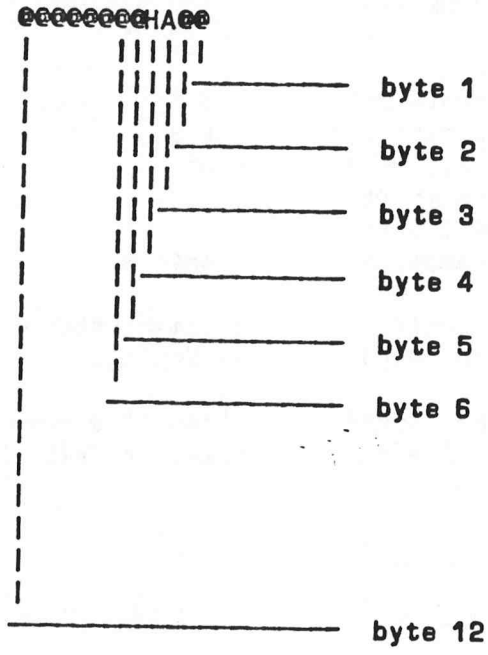
To connect the calibrator (CALIB) to channel 1 (CH1) the string is:

```
@100 @@@@@@@@@HA@@                          (in Kermit)

PRINT@100,"@@@@@@@@@HA@@"                   (in BASIC)
```

The @'s are open-relay commands. The bytes are conventionally numbered as shown in the table below:

TABLE 4-1: STRING/BYTE RELATIONSHIPS



The only bytes without open-relay commands, are numbers 3 and 4. Each byte sets a particular relay as shown in the next table.

TABLE 4-2: RELAY-BYTE RELATIONSHIPS

INPUT MATRIX	
RELAY	BYTE NO.
K11	2
K12	4
K16	12
K21	1
K22	3
K24	7
K25	9
K26	11

BYTE NO.	RELAY
1	K21
2	K11
3	K22
4	K12
5	—
6	—
7	K24
8	—
9	K25
10	—
11	K26
12	K16

OUTPUT MATRIX	
RELAY	BYTE NO.
K11	2
K13	5
K15	10
K21	1
K25	9

BYTE NO.	RELAY
1	K21
2	K11
3	—
4	—
5	K13
6	—
7	—
8	—
9	K25
10	K15
11	—
12	—

In our example, byte 4 sets K12, and byte 3 sets K22. The next thing is to determine what "H" in byte 4 does to K12 and what "A" in byte 3 does to K22. This we get from Table 3.

TABLE 4-3: BINARY-ASCII-DECIMAL CHART

Binary Numbers	ASCII Single Closures	ASCII Multiple Closures	Decimal Equivalent (Notes)
Ø1 ØØØ ØØØ	@	@	64 (open relay)
Ø1 ØØØ ØØ1	A		65
Ø1 ØØØ Ø1Ø	B		66
Ø1 ØØØ Ø11		C	67
Ø1 ØØØ 1ØØ	D		68
Ø1 ØØØ 1Ø1		E	69
Ø1 ØØØ 11Ø		F	7Ø
Ø1 ØØØ 111		G	71
Ø1 ØØ1 ØØØ	H		72
Ø1 ØØ1 ØØ1		I	73
Ø1 ØØ1 Ø1Ø		J	74
Ø1 ØØ1 Ø11		K	75
Ø1 ØØ1 1ØØ		L	76
Ø1 ØØ1 1Ø1		M	77
Ø1 ØØ1 11Ø		N	78
Ø1 ØØ1 111		O	79
Ø1 Ø1Ø ØØØ	P		8Ø
Ø1 Ø1Ø ØØ1		Q	81
Ø1 Ø1Ø Ø1Ø		R	82
Ø1 Ø1Ø Ø11		S	83
Ø1 Ø1Ø 1ØØ		T	84
Ø1 Ø1Ø 1Ø1		U	85
Ø1 Ø1Ø 11Ø		V	86
Ø1 Ø1Ø 111		W	87
Ø1 Ø11 ØØØ		X	88
Ø1 Ø11 ØØ1		Y	89
Ø1 Ø11 Ø1Ø		Z	9Ø
Ø1 Ø11 Ø11		[	91
Ø1 Ø11 1ØØ		\	92
Ø1 Ø11 1Ø1		]	93
Ø1 Ø11 11Ø		^	94
Ø1 Ø11 111		_	95
Ø1 1ØØ ØØØ	`		96

In the table above, only the last 6 bits are of much interest. Since the single closures: ASCII A B D H P ' are the most important, they will be explained in detail.

The matrix paths 1 through 6 may be selectively closed by setting the corresponding bit in a message byte high (=1). The correspondence between bit numbers and paths is show in the Table 4:

TABLE 4-4: MESSAGE BYTE FORMAT

BIT6	BIT5	BIT4	BIT3	BIT2	BIT1
path 6	path 5	path 4	path 3	path 2	path 1

As shown in Table 3, message bytes for the six single-closure paths correspond to the following ASCII codes:

PATH SELECTED	ASCII CHAR
none	@ (64)
1	A (65)
2	B (66)
3	D (68)
4	H (72)
5	P (80)
6	` (96)

Path number 1 above always corresponds to a line number ending in 1 on the MPTS I/O Matrix Diagram, path number 2 corresponds to a line number ending in 2 etc. Referring to the MPTS I/O Matrix Diagram in the Pullout Section for the connections, we see that in relay K12, and K22 for example:

PATH SELECTED	K12 LINE NO.	K22 LINE NO.
1	J121	221
2	J122	222
3	J123	223
4	J124	224
5	J125	225
6	J126	226

From Table 4 and the MPTS I/O Matrix Diagram, it should now be clear that the "H" in byte 4 of our example connects J124 of K12 to line 120 (the calibrator), and the "A" in byte 3 connects line 220 of K22 to line 221.

However for relays in the 6X6 matrix, this is not the complete story. Look again at the MPTS I/O Matrix Diagram. The relays are hard-wired so that if 211 of K21 is connected to 210, then 311 of K31 also is connected to I310; or if 212 of K21 is connected to 210, then 321 of K32 also is connected to I320; etc. Therefore, the A in byte 3 also connects line 312 of K31 to I310 which is channel 1 of the oscilloscope. This completes the explanation of our example.

More than one path in a given relay can be selected at a given time by setting more than one bit in a message byte. The details of how to do this are shown in

Table 3. However, this will result in loss of the 5Ø ohm environment within the matrix path, and should only be used in low frequency or high impedance applications.

SECTION 5

CALIBRATION

This unit does not need calibration. See Section 2-4 for performance check.

SECTION 6

REPLACEABLE PARTS LIST Ø67-1Ø96-99

6.1 Parts ordering information

Replacement parts are available from or through your local Tektronix Inc. Field Office or representative.

It is important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

Change information, if any, is located at the rear of this manual.

6.2 Component Number System

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number is known, this list will identify the assembly in which the part is located.

A numbering method has been used to identify assemblies, subassemblies, and parts. For example the Component Number:

A1C14Ø

consists of Assembly Number, A1 followed by Circuit Number, C14Ø. Read: Capacitor 14Ø of Assembly A1.

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram is marked with the assembly number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly

A2 with it subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

REPLACEABLE ELECTRICAL PARTS 67Ø-7694-ØØ (<2> Listener Interface A1) of SWITCH MATRIX

COMPONENT NUMBER	PART NUMBER	DESCRIPTION	NOTES
A1	67Ø-7694-ØØ	Listener Inter. Bd Assy	
	388-8Ø72-ØØ	Raw Board	
	(8Ø93XB)	Film Number	
A1C12Ø	283-Ø238-ØØ	CAP .Ø1uf	
A1C14Ø	283-Ø238-ØØ	CAP .Ø1uf	
A1C15Ø	283-Ø238-ØØ	CAP .Ø1uf	
A1C22Ø	283-Ø238-ØØ	CAP .Ø1uf	
A1C24Ø	283-Ø238-ØØ	CAP .Ø1uf	
A1C32Ø	283-Ø114-ØØ	CAP 15ØØpf	
A1C33Ø	285-1187-ØØ	CAP .47uf	
A1C411	283-Ø238-ØØ	CAP .Ø1uf	
A1CR323	152-Ø141-ØØ	DIODE SI .4"	
A1DS3ØØ	15Ø-1Ø2Ø-ØØ	LED INDICATOR	
A1J15Ø	131-`993-ØØ	Connector, 2 Cond.	'Jumper'
A1P15Ø	131-1857-ØØ	Sq. Pins	Use 3 of 1X36 strip.
A1P17Ø	XXX-XXXX-XX	72 Pin CB Connector	MUPAC P/N 3612Ø56-Ø1
A1R23Ø	315-Ø1Ø2-ØØ	RES 1K OHM 1/4W 5%	
A1R31Ø	315-Ø1Ø3-ØØ	RES 1ØK OHM 1/4W 5%	
A1R311	315-Ø1Ø3-ØØ	RES 1ØK OHM 1/4W 5%	
A1R312	315-Ø1Ø3-ØØ	RES 1ØK OHM 1/4W 5%	
A1R313	315-Ø1Ø3-ØØ	RES 1ØK OHM 1/4W 5%	
A1R314	315-Ø1Ø3-ØØ	RES 1ØK OHM 1/4W 5%	
A1R321	315-Ø151-ØØ	RES 15Ø OHM 1/4W 5%	
A1R322	315-Ø151-ØØ	RES 15Ø OHM 1/4W 5%	
A1R33Ø	315-Ø1Ø2-ØØ	RES 1K OHM 1/4W 5%	
A1R34Ø	315-Ø1Ø2-ØØ	RES 1K OHM 1/4W 5%	
A1S41Ø	26Ø-1827-ØØ	SWITCH 5 SPST MINIDIP	Address Switch
A1U13Ø	156-1273-ØØ	IC 25LS2521 2ØDIP	8BIT COMPARATOR
A1U141	156-Ø382-ØØ	IC 74LSØØ 14DIP	QUAD 2 INPUT
A1U16Ø	156-Ø323-Ø1	IC 74SØ4 14DIP	HEX INVERTER
A1U231	156-Ø914-ØØ	IC 74LS24Ø 2ØDIP	OCTAL BUFFER
A1U241	156-Ø388-ØØ	IC 74LS74 14DIP	DUAL D FLOP
A1U42Ø	156-1666-ØØ	IC 96LS488 48DIP	GPIB IC FAIRCHILD
			USE 2 24DIP SOCKET

REPLACEABLE MECHANICAL PARTS 67Ø-7694-ØØ (<2> Listener Interface A1)
of SWITCH MATRIX

PART NUMBER	QTY PER	DESCRIPTION	NOTES
1Ø5-Ø16Ø-ØØ	2	Circuit Board Ejector	
136-Ø269-Ø2	3	IC Socket 14DIP	
136-Ø578-ØØ	2	IC Socket 24DIP	
136-Ø634-ØØ	1	IC Socket 2ØDIP	
214-Ø579-ØØ	16	Test Points	
214-1337-ØØ	2	Pin, Roll	

REPLACEABLE ELECTRICAL PARTS 67Ø-7691-ØØ (<3>Latch Driver A2) of SWITCH MATRIX

COMPONENT NUMBER	PART NUMBER	DESCRIPTION	NOTES
A2	67Ø-7691-ØØ	Latch Driver Board Assy	
	388-8Ø69-ØØ	Raw Board	
	(E818ØXB)	Film Number	
A2CØ1	281-Ø775-ØØ	CAP .1uf	
A2CØ2	283-Ø238-ØØ	CAP .01 uf	
A2CØ3	283-Ø238-ØØ	CAP .01 uf	
A2CØ4	283-Ø238-ØØ	CAP .01 uf	
A2CØ5	283-Ø238-ØØ	CAP .01 uf	
A2CØ6	29Ø-Ø525-ØØ	CAP 4.7uf 5Øv	
A2QØ1	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ2	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ3	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ4	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ5	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ6	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ7	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ8	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2QØ9	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2Q1Ø	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2Q11	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2Q12	151-Ø496-ØØ	DARLINGTON XSTR D4ØK2	
A2RØ11	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ12	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ21	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ22	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ31	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ32	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ41	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ42	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ51	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ52	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ61	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ62	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	

REPLACEABLE ELECTRICAL PARTS 67Ø-7691-ØØ (<3> Latch Driver A2) of SWITCH MATRIX

COMPONENT NUMBER	PART NUMBER	DESCRIPTION	NOTES
A2RØ71	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ72	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ81	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ82	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ91	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2RØ92	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R1Ø1	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R1Ø2	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R111	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R112	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R121	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2R122	315-Ø1Ø2-ØØ	RES 1Kohm 1/4W 5%	
A2U1	156-Ø391-Ø2	I.C. 74LS174 16 DIP	
A2U2	156-Ø391-Ø2	I.C. 74LS174 16 DIP	
A2U3	156-Ø391-Ø2	I.C. 74LS174 16 DIP	
A2U4	156-Ø391-Ø2	I.C. 74LS174 16 DIP	

REPLACEABLE MECHANICAL PARTS 67Ø-7691-ØØ (<3> Latch Driver A2)
of SWITCH MATRIX

PART NUMBER	QTY PER	DESCRIPTION	NOTES
1Ø5-Ø16Ø-ØØ	2	PANEL EJECTORS, NYLON	
136-Ø2Ø6-ØØ	4	IC SOCKET 16DIP	
156-Ø391-ØØ	4	IC 74LS174 16DIP	
214-1337-ØØ	2	PIN, ROLL	
XXX-XXXX-XX	1	PLUG RIGHT ANGLE MUPAC 3612Ø56-1	FURNISHED IN MUPAC 92Ø1ØØØ-Ø1

REPLACEABLE ELECTRICAL PARTS Ø67-7693-ØØ (<5> Relay Diode Board A4) of SWITCH MATRIX

COMPONENT NUMBER	PART NUMBER	DESCRIPTION	NOTES
A4	67Ø-7693-ØØ	Relay Diode Board Assy	Finished
	388-8Ø71-ØØ	Raw Board	
	(8182XB)	Film Number	
A4CRØ1	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ2	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ3	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ4	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ5	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ5	152-Ø141-Ø2	Diode,Si. 1N4152	
A4CRØ6	152-Ø141-Ø2	Diode,Si. 1N4152	

REPLACEABLE MECHANICAL PARTS 67Ø-7693-ØØ (<5> Relay Diode Board A4) of SWITCH MATRIX

	PART NUMBER	QTY PER	DESCRIPTION	NOTES
	131-1857-ØØ	7	Straight Pin Carrier	Use 7 of 1X36 strip.

REPLACEABLE ELECTRICAL PARTS MP-1Ø96-Ø3 (<6> MPTS I/O Matrix A5) of SWITCH MATRIX

COMPONENT NUMBER	PART NUMBER	DESCRIPTION	NOTES
A5K11IN	XXX-XXXX-XX	RF Coax Switch Q6-413K3	DYNATEK/U-Z part number
A5K12IN	"	"	"
A5K16IN	"	"	"
A5K21IN	"	"	"
A5K22IN	"	"	"
A5K25IN	"	"	"
A5K26IN	"	"	"
A5K31IN	"	"	"
A5K32IN	"	"	"
A5K33IN	"	"	"
A5K34IN	"	"	"
A5K35IN	"	"	"
A5K36IN	"	"	"
A5K11OUT	"	"	"
A5K15OUT	"	"	"
A5K21OUT	"	"	"
A5K25OUT	"	"	"
A5K31OUT	"	"	"
A5K32OUT	"	"	"
A5K33OUT	"	"	"
A5K34OUT	"	"	"
A5K35OUT	"	"	"

REPLACEABLE MECHANICAL PARTS of SWITCH MATRIX Ø67-1Ø96-99

PART NUMBER	QTY PER	DESCRIPTION	NOTES
Ø12-Ø63Ø-Ø5	1	1 METER GPIB CABLE	
1Ø5 Ø787-ØØ	2	RETAINING LATCH	TO FAB SIDE
1Ø5-Ø786-ØØ	2	RELASE LATCH	TO FAB SIDE
119-Ø389-ØØ	1	LINE RECEPTACLE-RFI FILTER	
119-XXXX-XX	1	PWR SUPPLY ED 524CV	
124-Ø32 -ØØ	1	TERMINAL STRIP 4 SECTION	
124-Ø354-Ø2	4	STRIP, TRIM	FROM 255-Ø63Ø-Ø2
161-Ø1Ø4-Ø4	1	LINE CORD 98INCH	
175-XXXX-XX	1	RIBBON CABLE KIT RELAY	Set of (18) 7-Conductor
175-XXXX-XX			Ribbon Cable.
175-XXXX-XX	1	RIBBON CABLE KIT GPIB	Cable Harness from Back
175-XXXX-XX			Panel to Card Cage-GPIB
2ØØ-Ø237-Ø4	1	FUSE HOLDER COVER	
2ØØ-2264-ØØ	1	FUSE CAP	
2Ø4-Ø832-ØØ	1	FUSE HOLDER	
21Ø-ØØ54-ØØ	14	4 SPLIT WASHER	
211-ØØ97-ØØ	14	4-4Ø SRW	
26Ø-19Ø2-ØØ	1	POWER ON-OFF SWITCH	
351-Ø1Ø4-ØØ	?	SLIDE	
351-Ø1Ø4-ØØ	1PAIR	CHASSIS TRACK SECTION	
351-Ø636-ØØ	?	BRACKET	
367-Ø282-ØØ	1	HANDLE BOW RIGHT	"
367-Ø283-ØØ	1	HANDLE BOW LEFT	"
384-Ø544-Ø3	4	RETAINER CORNER	
39Ø-Ø737-ØØ	1	CABINET TOP	
39Ø-Ø738-ØØ	1	CABINET BOTTOM	
39Ø-XXXX-XX	1	CABINET SIDE RIGHT	ASSY'S
39Ø-XXXX-XX	1	CABINET SIDE LEFT	"
426-1588-ØØ	1	FRAME CABINET REAR	
426-1629-ØØ	1	FRAME CABINET FRONT	
67Ø-7694-ØØ	1	A1 - LISTENER INTERFACE BD <2> (388-8Ø72-ØØ Raw)	
67Ø-7691-ØØ	X	A2 - LATCH/DRIVER BOARD <3> (388-8Ø69-ØØ RAW)	X=6 for Input Matrix; X=5 for Output Matrix
XXX-XXXX-XX	1	A3 - BACKPLANE WIRING <4>	Wiring only. No board.
67Ø-7693-ØØ	X	A4 - RELAY DIODE BOARD <5> (388-8Ø71-ØØ RAW)	X=14 for Input Matrix. X=9 for Output Matrix.
XXX-XXXX-XX	1	A5 - COAX LINE CONNECTIONS <6>	Connections, No Board.

REPLACEABLE MECHANICAL PARTS of SWITCH MATRIX Ø67-1Ø96-99

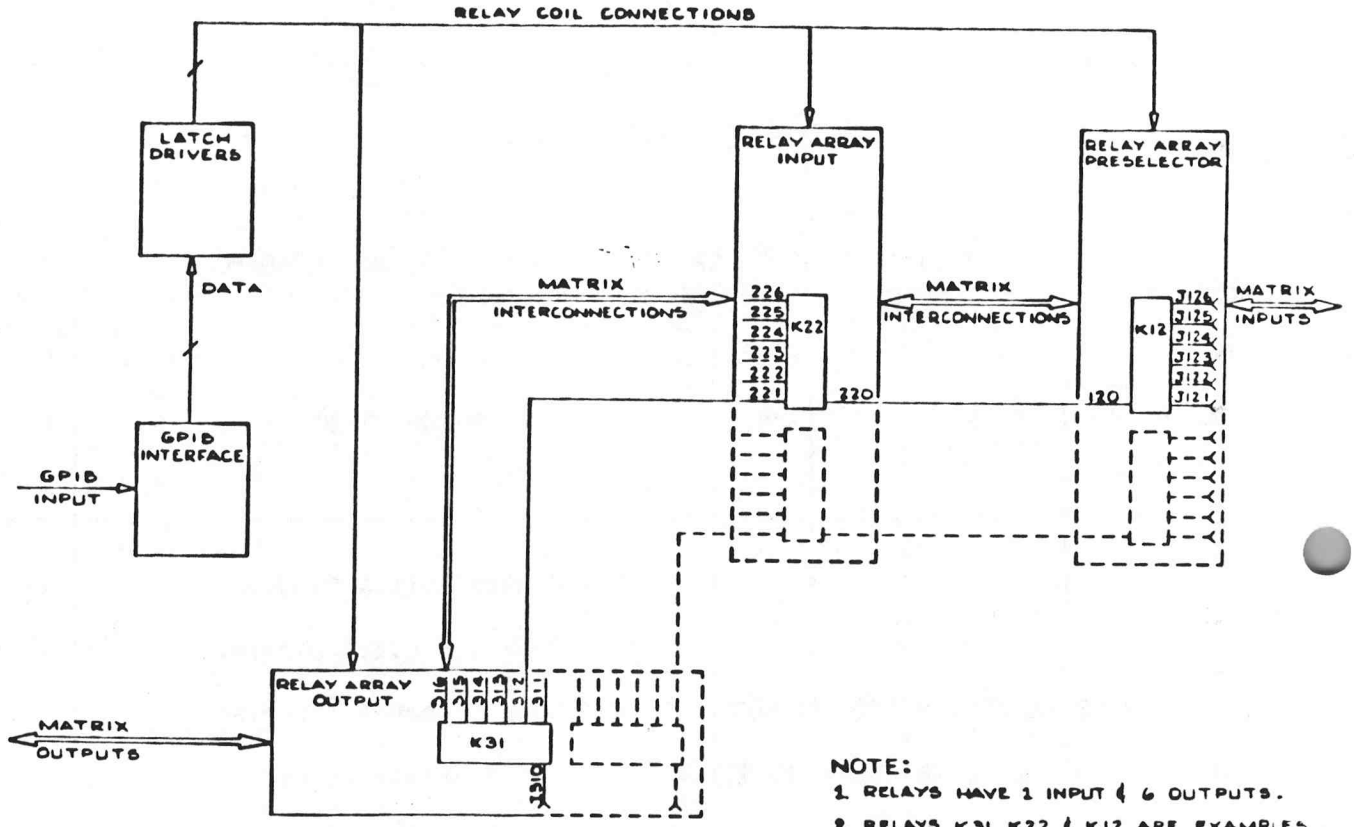
PART NUMBER	QTY PER	DESCRIPTION	NOTES
67Ø-7695-ØØ		A6 - EXTENDER CARD BOARD <7> (388-8Ø73-ØØ RAW)	EB181XB. Used in diagnostics only. Not part of product.
XXX-XXXX-XX	1	CORNER BOTTOM RIGHT HAND	FROM 251-1556-ØØ
XXX-XXXX-XX	1	CORNER BOTTOM LEFT HAND	" " "
XXX-XXXX-XX	2	CORNER TOP RIGHT & LEFT HAND	" " "
XXX-XXXX-XX	2	SIDE REINFORCE BAR RACK MT	FROM 251-165Ø-ØØ
XXX-XXXX-XX	2	TOP/BOTTOM REINFORCE BAR	" " "
XXX-XXXX-XX	2	SUPPORT	1/4X1/2
XXX-XXXX-XX	1	FRONT PANEL	
XXX-XXXX-XX	1	BACK PANEL	
XXX-XXXX-XX	1	DOOR,BACK PANEL	
MP-1Ø96-Ø1	1	HINGE,BACK PANEL	
XXX-XXXX-XX	1	CARD CAGE,(REWORK)	
MP-1Ø96-Ø2	1	PWR SUPPLY (REWORK	
XXX-XXXX-XX	?	8 BOLTS	
XXX-XXXX-XX	?	8 NUTS	
XXX-XXXX-XX	1	FUSE,2AMP SLO-BLO	
XXX-XXXX-XX	X	RELAY MICROWAVE Q6-413K3	X=14 for Input Matrix
XXX-XXXX-XX			X=9 for Output Matrix
XXX-XXXX-XX	1	CARD CAGE MUPAC 92Ø1ØØØ-Ø1	
XXX-XXXX-XX	6	CARD GUIDES MUPAC 3351ØØØ-Ø7	
XXX-XXXX-XX	7	WIREWRP CONNECTOR 3612251-Ø1	

SECTION 7

DIAGRAMS

TABLE 7-1: LIST OF SCHEMATICS, ASSEMBLIES, and DIAGAMS

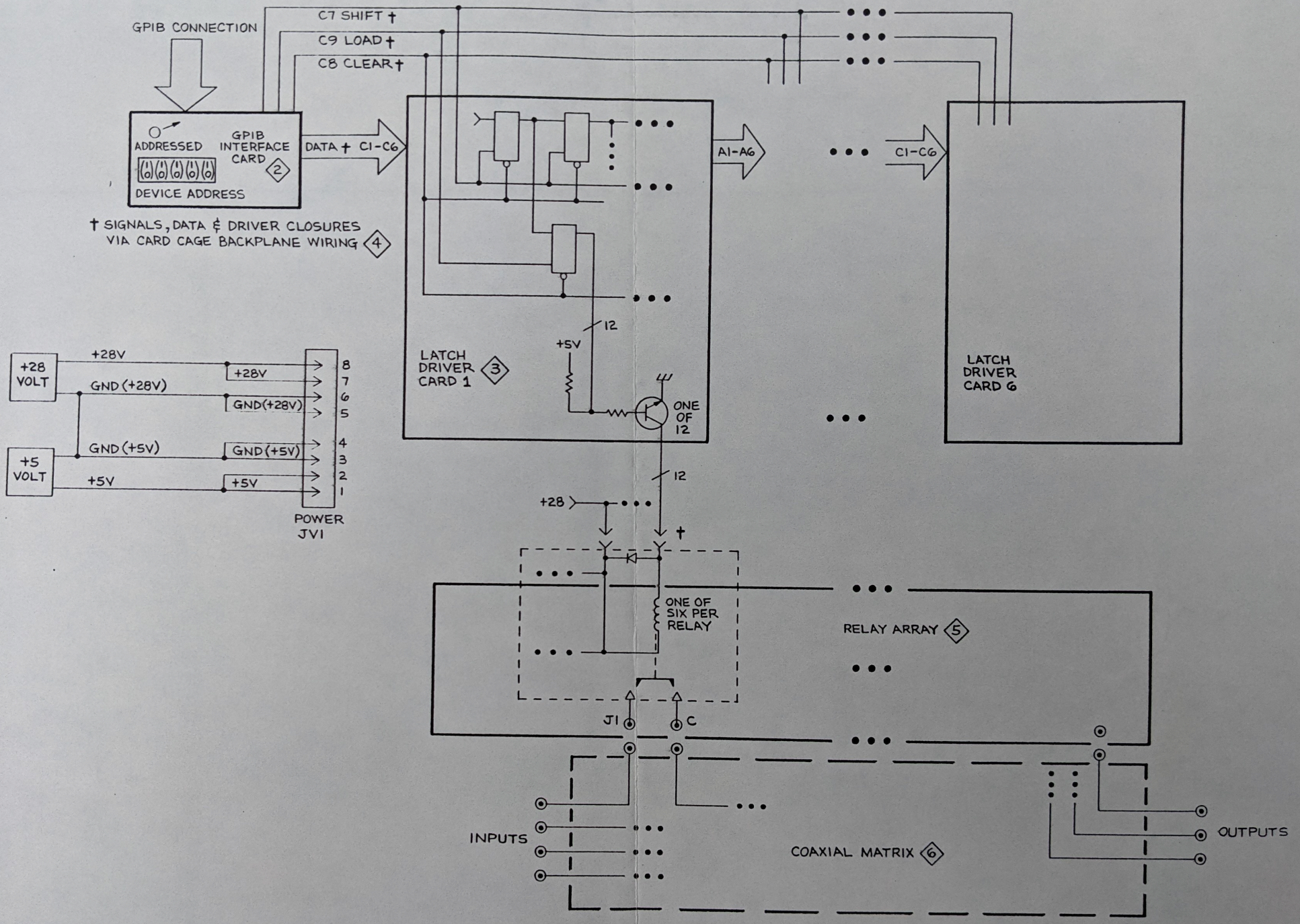
RAW BOARD	FILM NUMBER	FINISHED BOARD	ASSY	< >	DESCRIPTION	BOM. pg	M. PART S	E. PART S	DOLLY
x	x	x	x	<0>	General Block Diagram	x	x	x	x
x	x	x	x	<1>	Detailed Block Diagram	x	x	x	x
388-8072-00	E 8093-XB	670-7694-00	A1	<2>	GPIB Listener Interface	5			y
388-8069-00	E 8180-XB	670-7691-00	A2	<3>	Latch Driver Cards	4	y	y	
x	x	x	A3	<4>	Backplane Wiring	x	x	x	x
388-8071-00	E 8182-XB	670-7693-00	A4	<5>	Relay Diode Board	3			y
x	x	x	A5	<6>	MPTS I/O Matrix (coax. line connections)	x	x	y	x
388-8073-00	E 8181-XB	670-7695-00	A6	<7>	Extender Card (For test purposes only; not part of product)			x	



BLOCK DIAGRAM
PROGRAMMABLE
MICROWAVE (COAXIAL)
SWITCHING MATRIX
067-1069-99

FIGURE 3

Figure 7-1 GENERAL BLOCK DIAGRAM <Ø>

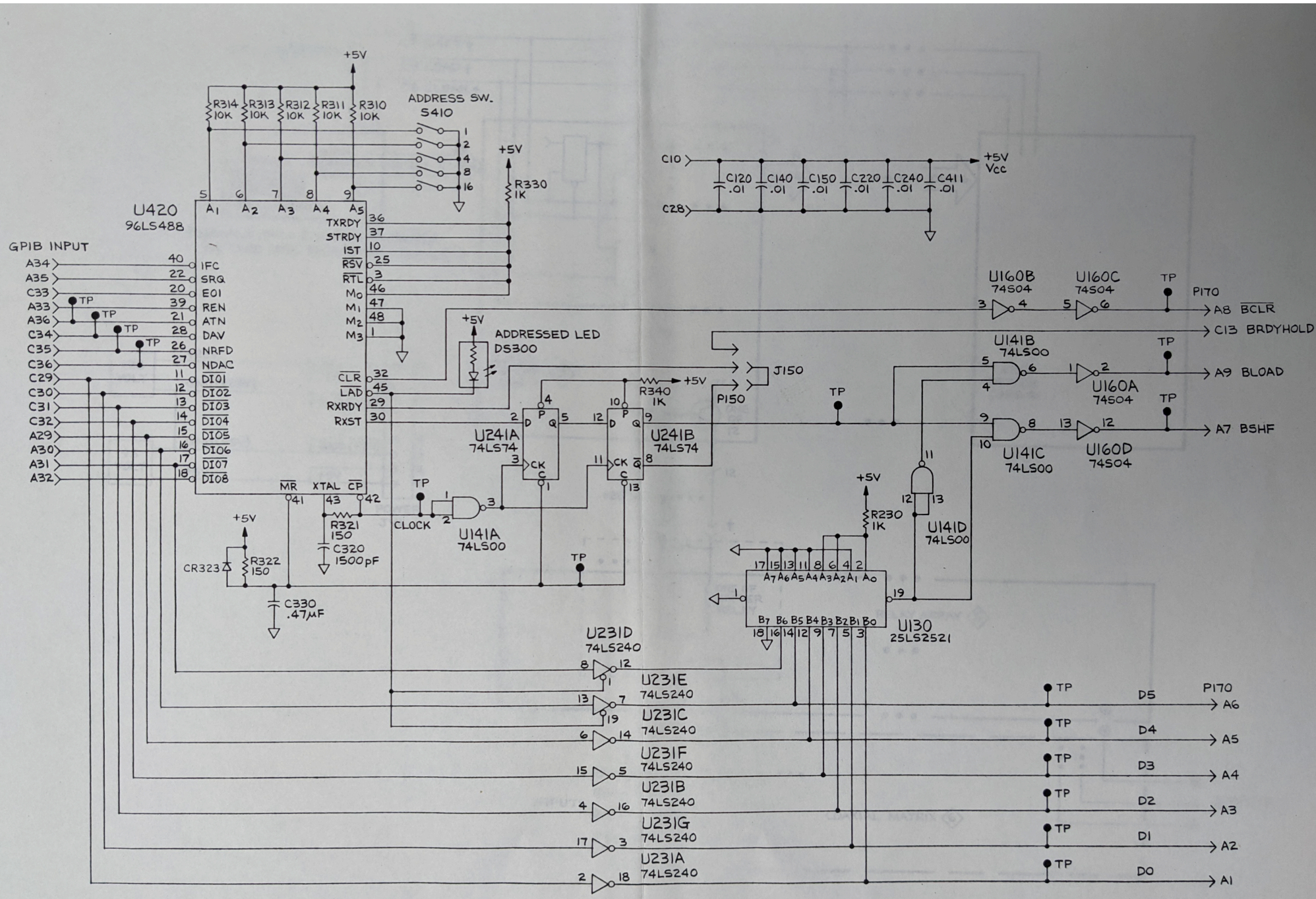


067-1096-99

DWG # MP-1096-99-4

DETAILED BLOCK DIAGRAM 1

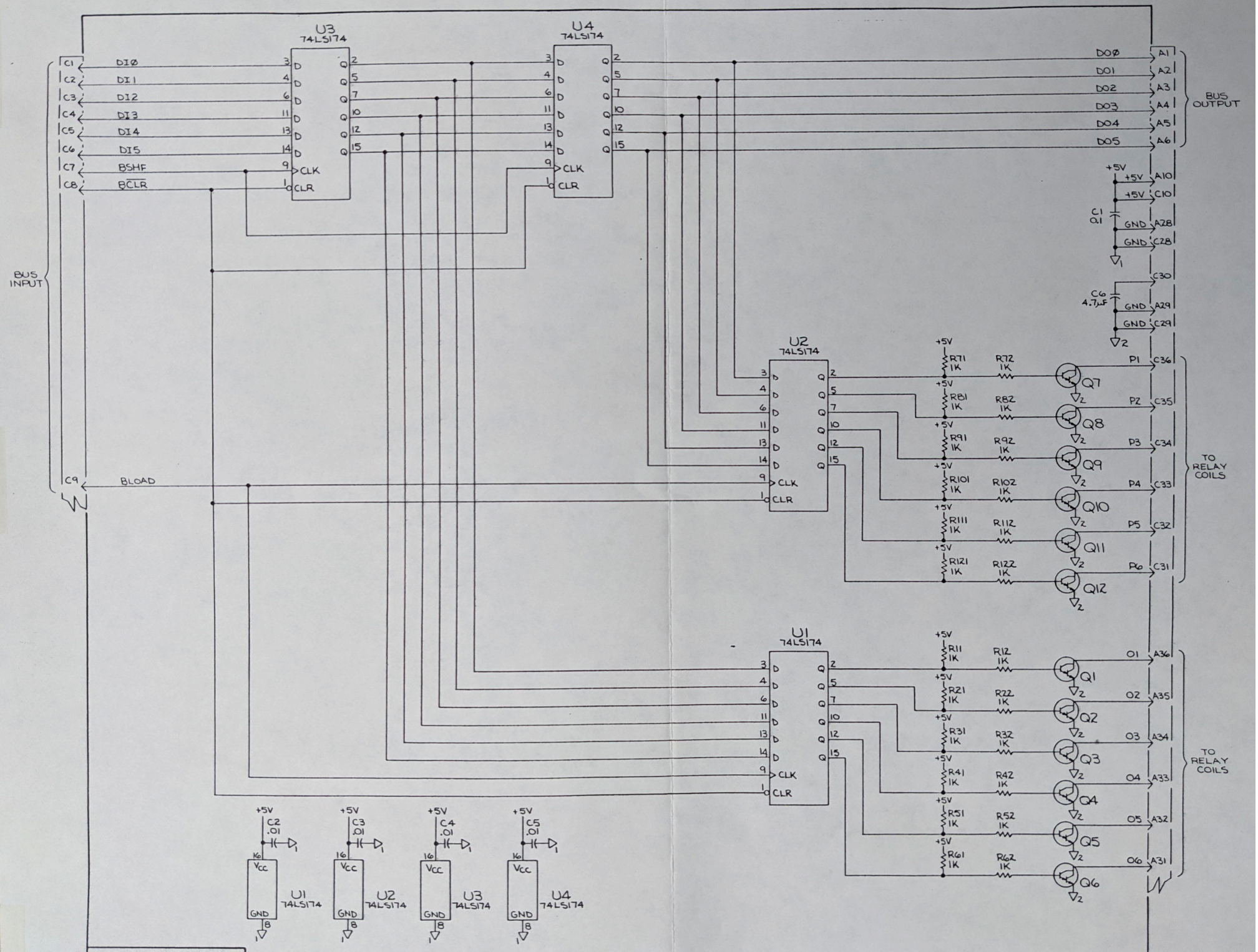
PROGRAMMABLE MICROWAVE SWITCHING MATRIX



067-1096-99

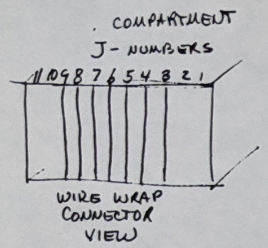
GPIB LISTENER INTERFACE (2)

DWG. # MP-1096-99-3 1/85



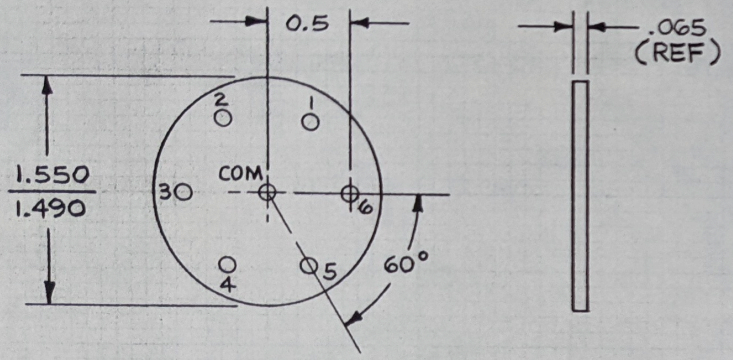
LATCH DRIVER CARD SCHEMATIC <3>

067-1096-99
BACKPLANE WIRING DIAGRAM FOR CARD CAGE IN MICROWAVE SWITCH MATRIX.
W7 7/1/81 (CONNECTOR VIEW)
DRAWING NO. MP-1096-99-2



Resp C-C 2747-02
Project # 504-105
Warren Finke x 4327
Bob Beville x 4327
3/1/82

MECHANICAL LAYOUT

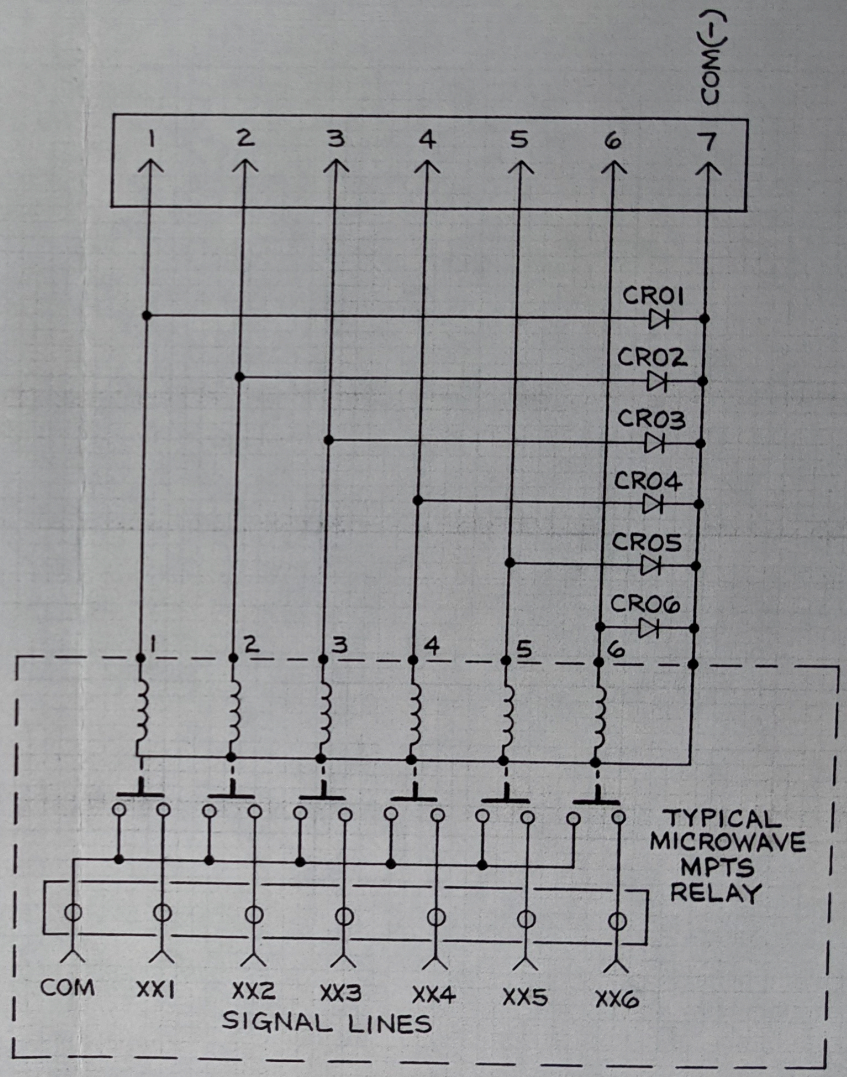


NOTE :

CIRCUIT BOARD MUST SLIDE OVER TERMINAL POSTS ON RELAYS.

DIODE MOUNTING IS NOT CRITICAL.

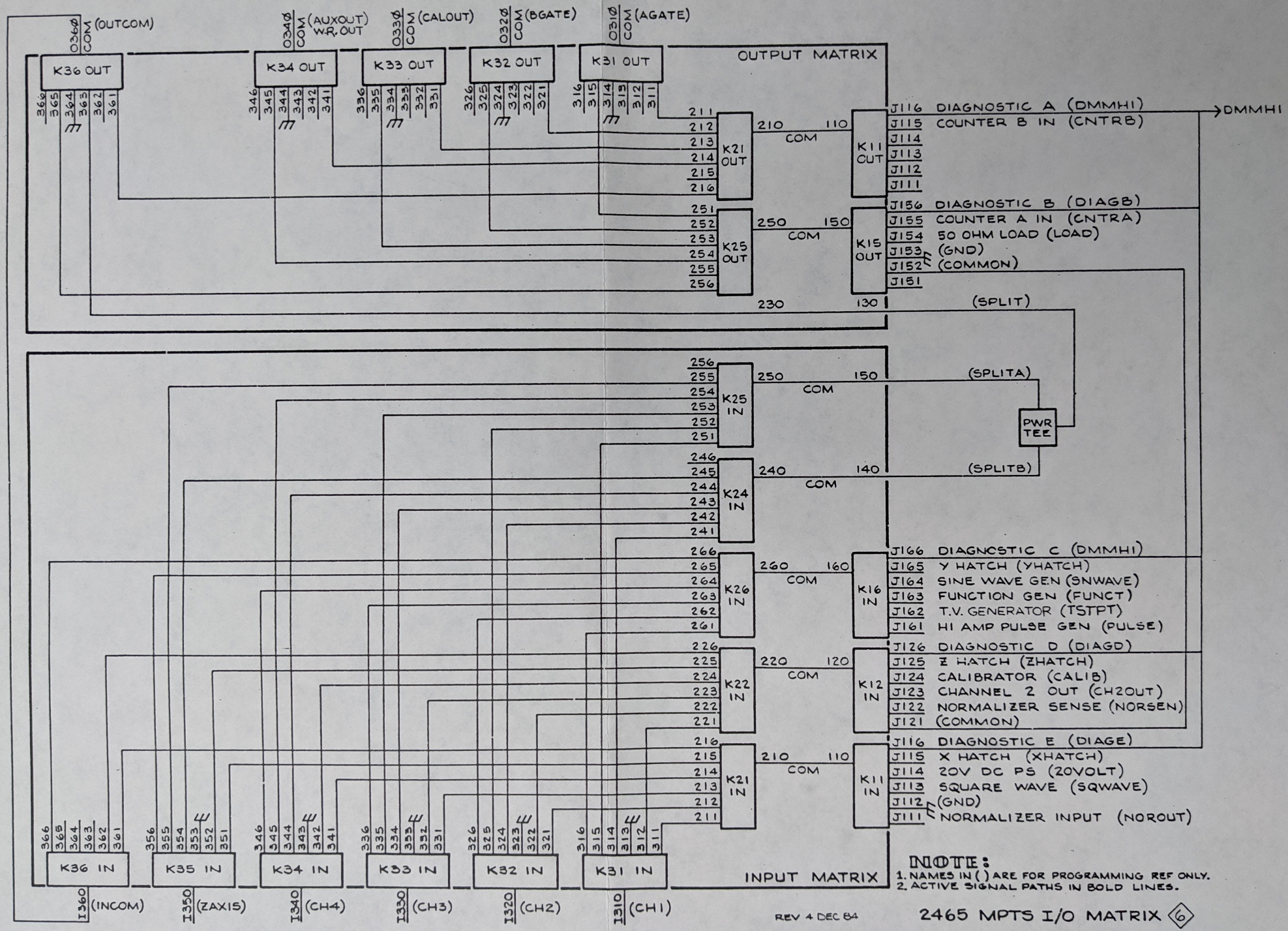
SCHEMATIC



670-7693-00

RELAY DIODE BOARD ◇5

(PART OF SWITCH MATRIX 067-1096-99)



NOTE:
1. NAMES IN ( ) ARE FOR PROGRAMMING REF ONLY.
2. ACTIVE SIGNAL PATHS IN BOLD LINES.

REV 4 DEC 84

2465 MPTS I/O MATRIX 6

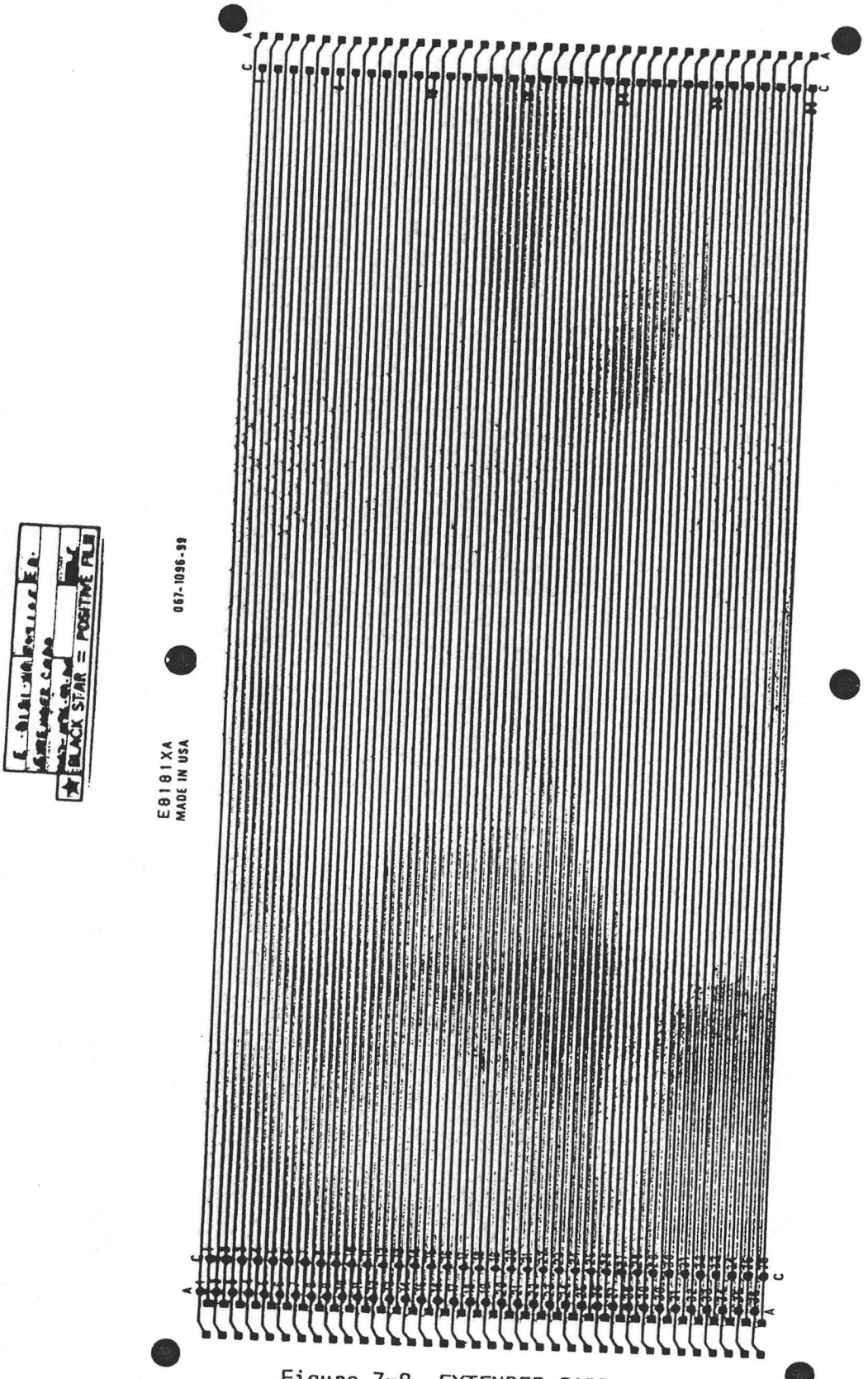


Figure 7-8 EXTENDER CARD <7>

SECTION 8

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